CANON POCKETRONIC SERVICE MANUAL

BATTERY CHARGER 20A, 10A

Canon Inc.

PREFACE

This manual is the guide for service after sales with the main purpose of quality performance of the Canola Pocketronic and is also useful for marketing promotion as well as repair service.

Pocketronic, utilizing the LSI's with a newly developed print-out system, is the world's smallest, cordless electronic calculator which has destroyed the image of the desktop size.

Due to the epochal print-out system together with the LSI's, the Pocketronic was developed with the viewpoint of miniaturizing the desktop calculator, so that anyone may personally use it whether at home or travelling.

Since one LSI is equivalent to one printed card unit, it is impossible to check or repair part by part as in the former Canola series; thus, the servicing method is greatly different.

Basic System & Principles of the Pocketronic is vastly different to any of the other Canola series; thus, the contents should be mastered, while the proper servicing should be done by using the Pocketronic Checker and referring to How to Repair of this manual.

When parts are needed, it is important to order them to the following address by referring to the diagrams in How to Repair and Parts Catalog.

Canon Inc.
Service Parts Dept.
30-2, Shimomaruko 3-chome,
Ohta-ku, Tokyo, 144, Japan

Unless there is need of a revised edition due to any major amendment information will be sent as a Service Manual Report.

Any comments and querries about this service manual would be greatly appreciated by us.

Canon Inc.
Business Machines Service Dept.
9-9, Ginza, 5-chome,
Chuo-ku, Tokyo, 104, Japan

GENERAL OUTLINE

This service manual consists of four parts: Pocketronic, Hi-speed Battery Charger 20A, Battery Charger 10A and Pocketronic Checker.

Pocketronic

1. General

   Specifications and proper manual calculation operations are described which should be memorized to understand the software of the Pocketronic.

2. System

   The general description of the operation system and structure of each component are given.

3. Basic Circuit

   MOS (metal oxide semiconductor) principle is fully explained to understand the basic circuit of the shift registers.

4. Operation Principle

   The operation procedures by means of a flow chart explain the different operations in relationship with the timing for the various calculations.

5. Operation Procedure

   The actual operation of the components of the circuits which are based on Operation Principle are described in detail in relationship to the operation of LSI's and thermal head.

6. How to Repair

   Operation check program, trouble-shooting and repairing necessary for actual service are described.

Canon Hi-speed Battery Charger 20A

Principle of quick charging and service tips for charger 20A are described.

Canon Battery Charger 10A

Specification and circuit of charger 10A are given.

Pocketronic Checker

How to check the thermal head and LSI are explained.

Logic & Timing Chart

This section consists of various waveforms and logic diagrams of the Pocketronic circuits.

Parts Catalog

Exploded view of assembly units with key numbers. When parts are ordered, it is

important to write the complete part's nomenclature and its serial number.

Service Manual Report

Reports of any modification which should be known by all service personnels and agencies will be issued and forwarded as soon as published.

It is important to keep them, so they should be filed in this section for future reference.

Important Points when using Pocketronic

Following are some items to be remembered about the usage of the Pocketronic and its battery charger.

1. Precautions for Users

   1) Never leave the POWER switch ON when not in use, unless it is connected to Hi-speed Charger 20A.

   2) Be certain the thermal print tape is inserted in properly.

      i) If the cassette is not fully inserted, then the tape does not make contact with the thermal head so there is no print out.

      ii) If the cassette is pushed in too hard, the tape movement is not smoothly carried out with an overlapping of the print-out characters.

   3) Be sure that the Pocketronic is only used under its specification.

2. Hi-speed Battery Charger 20A

   1) If the Pocketronic has been left unused for one month or more, whether the POWER switch is ON or OFF except when connected to the Hi-speed Charger 20A, then charge the battery for approx. 12 ~ 18 hours. Even though POWER switch is OFF and has not been in use for one month or so, capacity drops to approx. 70% of its nominal capacity.

   2) If the Hi-speed Charger 20A is connected to the Pocketronic, in approx. 2 ~ 3 minutes it is ready for calculation operations; but if disconnected after such a short charging time, then it will not carry out the calculation due to a lack of charge.

   3) The Pocketronic is usually operated with it being connected to the charger 20A and it may be connected for any length of time.

   4) If fully charged, the Pocketronic battery will last for over 3 hours of continuous operation of a 12 digit ±12 digit calculation per minute.

   5) Pocketronic can only be charged by either the Hi-speed Battery Charger 20A or Battery Charger 10A, and these chargers cannot be used to charge any other products.

6) Battery lifetime is determined by the number of repetitive charge discharge cycles, and in the Pocketronic, it is more than 500 cycles; but, the lifetime can be prolonged by operating the calculator while it is connected to the Hi-speed Charger 20A.

3. Battery Charger 10A

1) Never operate the Pocketronic while it is connected with this charger.

2) Normal charging time is 14 ~ 20 hours, and never charge it for more than 20 hours because this charger is not provided with an overcharging prevention circuit.

3) Only use this charger at its specified voltage, because it has no voltage selector switch.

4. Operational

1) When the power is switched on, the Pocketronic may print out random numerals, symbol or nothing at all, depending on the operational state of the calculator at that time.

2) Press [C] before starting any calculation.

3) Print-out becomes vague as the voltage decreases. When the voltage drops below a certain point, the thermal tape stops feeding, and in some cases, nothing is printed out or miscalculation are made even though the tape transport is normal. In such cases, charge the battery.

4) Always follow the operating check sheet when making sure for proper calculation of the Pocketronic.

5) Know what types of calculations can be accomplished on the Pocketronic so as to give a definite reply to any questions.

6) Never make an entry until the print-out has ended, because even though the Pocketronic makes the correct calculation, the entry is not printed out.

7) When a double entry is made, the logic sum is printed out.

8) Be sure to charge the battery first whenever a sympton of a malfunction is detected.

9) Always follow the proper remedial steps of "How to Repair".

CONTENTS

GENERAL

CONTENTS

1. General

1.1 Introduction

Canon "Pocketronic" is the smallest electronic desk-top calculator in the world, which employs the world's first thermosensitive printing system with built-in batteries. This miniaturized and lightweight machine with a 12-digit printing system is very convenient at a conference, convention in a large hall, auditorium, in the open-air or while travelling in a car, train, plane --- works anywhere, anytime --- needs no cord connection.

The circuit consists of three LSI's (large scale integration) which guarantee high reliability and stability. Its cassette type printing paper can be replaced simply by one-touch operation, and the printed letters, composed of 4 columns and 5 rows, are quite legible.

1.2 Appearance

Fig. 1-1 Appearance

1.3 Keyboard Arrangement

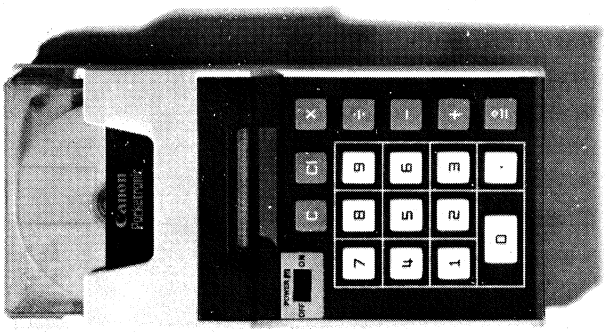


Fig. 1-2 Keyboard Arrangement

[C]	Clear key:	Clears register and control circuits.
[CI]	Clear entry key:	Clears buffer register.
[×]	Multiplication set key:	For multiplication and division. Constant multiplication or division can be done by pressing a variable and [=] key.
[÷]	Division set key:	
[−]	Subtraction key:	For addition and subtraction. Repeat addition or subtraction possible.
[+]	Addition key:	
[=]	Total & equal key:	Prints-out calculated result.
[·]	Decimal point key:	For registration.
[0]~[9]	Numeral key:	

1.4 Specification

1.4-1 General Specifications

Model:	Miniaturized electronic printing desk-top calculator.
Printing System:	Thermosensitive printing system.
Entry:	Successive printing
Result:	Automatic printing
Print-out Digits:	15 digits max. (8-digit integer and 4-digit fraction with 1 digit for decimal point, sign, and symbol)
Basic Operation:	Addition, subtraction, multiplication, and division.
Decimal Point:	Fixed decimal point 4-digit fraction with consecutive fractions being dropped off.
Binary Code:	8-4-2-1 code
Clock Frequency:	30 ~ 60 KHz
Register Capacity:	Buffer Register 1 word Accumulator 2 words (1 word = 13 digits)

Calculation Capacity:	Operation	Result	
Addition & Subtraction:	12 ± 12	12	Digits
Multiplication:	12 × 12	12	Digits
Division:	12 ÷ 12	12	Digits

Calculation Speed:	2 seconds max. (Includes printing time)
Types of Calculations:	Addition, subtraction, multiplication, and division Chain multiplication and division Constant multiplication and division Square and power calculation Repeat addition and subtraction Mixed calculation and applied calculation
Negative Number:	True value indicated with minus symbol
Circuit Elements:	Three LSI's Control Chip (TMC1730) Data Chip (TMC1731) Timing Chip (TMC1732) Transistors and diodes

Printing Paper: Thermosensitive Printing Paper
(cassette type, 6mm width × 80m length)

Thermal Print Head: 5 × 4 dots (heater element)

Other Functions:

Overflow:

Registration

When 9 or more integer digits or 5 or more fractions are registered, following registration stops automatically.

Cleared by pressing [CI] or [C] .

Result Overflow:

Automatically clears with "C" printed. When the number of integer digits of calculated result becomes more than 9 digits, it automatically clears with the printing of "C" symbol.

* When the number of fractional digits of the result is more than 4 digits, the following fractions are dropped off.

Printed Letters:

0,1,2,3,4,5,6,7,8,9, • (Decimal point), +, −, ×, ÷, =, C, E

Indicator window has a 1.3 × magnification to make easier reading. Integer section has 0 suppressor.

Printing Space: 1—letter space after printing an order
2—letter space after printing result

DC Power Voltage:

V_H: (−16.0V): For driving thermal head and solenoid
V_{DD}: (−7.5V): For LSI cards

1.4-2 Working Conditions

Allowable Voltage Fluctuation Range: −15.0V ~19V in output voltage of battery unit (NR-AA × 6, NR-2/3AA × 7,13 pcs.)

Ambient Temperature Range: 0 ~ +40° C

Compensation for Variable Temperature: Automatically controls the printing time to minimize variation of printing darkness due to temperature change.

Ambient Humidity:	Below 90%
Power Consumption:	1W

1.4-3 Structure

Dimensions:	101mm (W) × 208mm (D) × 49mm (H)
Weight:	820g (cassette 60g)
Battery:	Built-in NiCd batteries Continuous operation approximately 3 hours after a rapid charge of 3 ~ 5 hours using Canon Hi-Speed Battery Charger 20A.
Charger:	Rapid charging system (3 ~ 5 hours)

1.5 Calculating Operations

1.5-1 Addition and Subtraction

Example 1-1 2 + 3 + 8 + 7 = 20

Operation [2][+][3][+][8][+][7][+][=]

Print 2+ 3+ 8+ 7+ = 20.0000

Example 1-2 −2.34 + 3.456 − 8 = −6.884

Operation [2][.][3][4][−][3][.][4][5][6][+][8][−][=]

Print 2.34- 3.456+ 8- =-6.8840

1.5-2 Repeat Addition and Subtraction

Example 1-3 2 + 2 + 6 − 8 − 8 − 8 = −14

Operation [2][+][+][6][+][8][−][−][−][=]

Print 2+ + 6+ 8- - - =-14.0000

1.5-3 Multiplication and Chain Multiplication

Example 1-4 2 × 4 = 8

Operation [2][×][4][=]

Print 2× 4= 8.0000

Example 1-5 2.3 × (−4.5) × 8 = −82.8

If there is a minus value in the middle of a chain calculation, omit the minus sign in the calculation operation and manually enter it in the final result or enter the minus sign after the first numeric as shown in following examples, then it will be printed out in the final result;

(a) Operation [2][.][3][×][4][.][5][=][×][8][=]

Print 2.3× 4.5= 10.3500 × 8= 82.8000

(b) Operation [2][.][3][−][×][4][.][5][=][×][8][=]

Print 2.3- × 4.5=-10.3500 × 8=-82.8000

1.5-4 Division and Chain Division

Example 1-6 $1 \div 3 = 0.3333$

Operation [1][÷][3][=]

Print `1÷ 3= .3333`

Example 1-7 $56.7 \div (-7) \div 3 = -2.7$

Chain division is done in the same procedure as in chain multiplication by taking into consideration the signs of the numerics.

Operation [5][6][·][7][÷][7][=][÷][3][=]

Print `56.7÷ 7= 8.1000 ÷ 3= 2.7000`

Operation [5][6][·][7][−][÷][7][=][÷][3][=]

1.5-5 Constant Multiplication and Division

Example 1-8

$2 \times 3.14 = 6.28$
$4 \times 3.14 = 12.56$
$5 \times 3.14 = 15.70$

Operation [3][·][1][4][×][2][=][4][=][5][=]

Print `3.14× 2= 6.2800 4= 12.5600 5= 15.7000`

Example 1-9

$1 \div 3 = 0.3333$
$2 \div 3 = 0.6666$
$4 \div 3 = 1.3333$

Operation [1][÷][3][=][2][=][4][=]

Print `1÷ 3= .3333 2= .6666 4= 1.3333`

1.5-6 Mixed Calculation

Example 1-10 $1 \times 2 + 3 = 5$

Operation [1][×][2][=][+][3][+][=]

Print `1× 2= 2.0000 + 3+ = 5.0000`

1.5-7 Square and Power Calculation

Example 1-12 $123^2 = 15129$

Operation [1][2][3][×][=]

Print `123× = 15129.0000`

Example 1-13 $2^n =$

Operation [2][×][=][=][=][=]

Print `2× = 4.0000 = 8.0000 = 16.0000 = 32.0000`

Example 1-14 $2^{2^n} =$

Operation [2][×][=][×][=][×][=]

Print `2× = 4.0000 × = 16.0000 × = 256.0000`

2. Outline of the system

The system greatly differs from those of the former Canola IC series, because of a more simplified system where the operation is mostly done by three LSI's which receive the input signals from the keyboard and its output signals are fed to the thermal head to print out the calculated result. These LSI's are virtually treated as an individual "Black Box". However, it is necessary to understand the internal structure and system.

Hardware of Pocketronic can be divided into the following blocks;

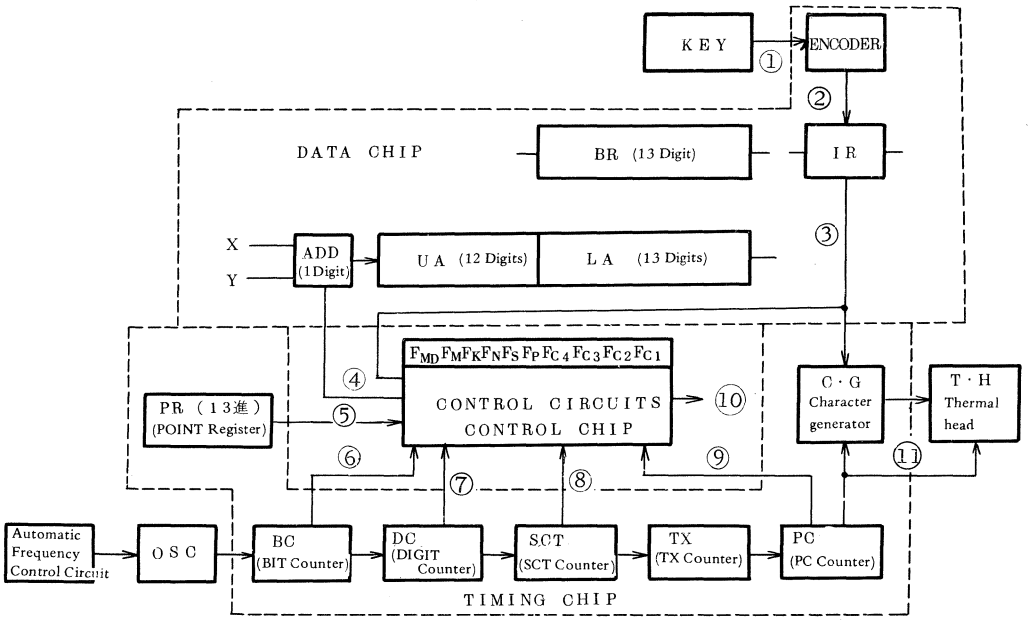


Fig. 2-1 Block Diagram of Pocketronic

1 Key signal
2 Encoded key signal
3 Print-out signal
4 CA signal
5 PR signal
6 BIT signal
7 DIGIT signal
8 SCT signal
9 PC signal
10 Control signal for Timing & Data chips
11 Timing signal

i) Keyboard

ii) Data Chip; Composed of key encoder, indication register (IR) for registration & print-out, buffer register (BR), accumulator (ACC), adder (ADD) & the data matrix, etc.

BR: Composed of 52-bit shift register and used for the same purpose as in former models.
Registered data in IR enters BR through gate BR–IN, and since it is a static shift register, the data can be transferred the required number of bits or stopped by controlling the emitting time of the shift pulse.

ACC: Composed of an upper (UA) & lower (LA) accumulator which together have 101 bits and an adder (ADD).
Since the ADD circuit has 3 bits, then ACC has 104 bits, or 26 digits.
Since 8-4-2-1 code is used, then direct subtraction system can be used.
Registered data enters IR from the encoder, and is printed out immediately. Then, the data stored in IR transfers to BR with a left shift occurring every time an integer registration is done.
In the registration of the fractional digits, PR–1 is carried out instead of left shifting.
Addition and subtraction are carried out between UA & BR, and the result is transferred to BR from UA.
Multiplication & division are carried out between UA·LA & BR, and the calculated result is transferred to BR from UA.

iii) Timing Chip: Generates various timing pulses required for the calculation operation.

BC (Bit counter):	4–bit counter generating $TB_0 \sim TB_3$
DC (Digit counter):	13–bit counter generating $TD_0 \sim TD_{12}$
SCT (Sector counter):	2–bit counter generating SCT_0 & SCT_1
TX (Step-down counter):	5–bit counter generating $TX_0 \sim TX_4$
PC (Print counter):	10–bit counter generating $P_0 \sim P_9$ which determine the print-out timing.
PR (Point register):	13–bit register counting $PR_0 \sim PR_{12}$

The timing chip also includes a character generator, timing matrix and other data circuits.

iv) Control Chip: Consists of control circuit and various flip flops for the calculation operation, and its "Product" and "Sum of Product" circuits are composed according to PLA system. (Programmable Logic Array)

Pocketronic adopted shift registers & counters which differ from those of the former Canola IC series where the data always circulates in the delay line and registers; in Pocketronic system, during a preset time and only under certain condition does the data circulate to complete certain calculation functions, and when there is no functional operation it statically remains in that position.

BASIC CIRCUIT

CONTENTS

3. BASIC CIRCUIT

3. Basic Circuit

Pocketronic greatly differs from the conventional Canola IC series in structure and operation system.

These differences are comparable to transition from transistorized machines to IC machines.

Integrated circuit is an interconnected array of transistors, resistors, capacitors and other elements integrated on a single silicon substrate, and can be treated as an independent block (Black Box) which is capable of performing at least one complete electronic circuit function. This concept and scale has been advanced and expanded to LSI.

Generally, an IC has several tens to a few hundreds of elements integrated on a silicon substrate of $1 \sim 3mm^2$, while the MSI (Medium Scale Integration) has from a hundred to several hundred elements, and that of the LSI having an integration of about $100 \sim 200$ times that of the conventional IC's.

In order to obtain such high integration, the structural and manufacturing process of LSI greatly differs from that of IC, where LSI employs MOS's (Metal Oxide Semiconductor) whose characteristics will be explained in detail later.

Therefore, partial checking, change or replacement in the circuit becomes impossible, and replacing a LSI corresponds to replacing a card unit in the conventional IC series.

Pocketronic has another distinguishing feature; the thermosensitive printing system with a newly-developed thermal head. Unlike the printing system of EP 150, it is of semiconductors and miniaturized, yet it provides legible printing. In EP 150, printing is performed by discharging a voltage to break down the thin aluminum layer on the printing paper and then the black layer appears at the point of a discharge.

In Pocketronic, the dots of the thermal head divided into 20 blocks generate an intense heat instantaneously according to signals from the circuits; thus, a figure is printed on the paper by heat. Therefore, printing is carried out very smoothly without noise and with no risk of catching fire nor giving off an unpleasant smell.

The explanation of the basic circuit starts with the MOS and although this may seem unnecessary, the LSI cannot be treated as respective independent circuits; thus, it is useful to have as basic knowledge.

3.1 Features of MOS FET (MOS Field-Effect Transistor)

1) No electrical isolation is needed between each transistor or element. In the bipolar type, the isolation is required between elements so that an area occupied with elements becomes comparatively large, and its manufacturing process takes much time.

Thus, the area on chip affects the scale of integration, yield, and cost. MOS LSI needs no isolation and is economical.

2) MOS transistor is also used as load resistor, thus the area occupied with many elements is minimized.

In the bipolar type, a high resistor of several ten thousand ohms is not applicable, because large area is needed. In the MOS type, the area occupied on the chip is minimized since it can be treated as a non-linear pure resistor by controlling the gate voltage of MOS transistor.

3) MOS has a large noise margin and less power consumption. Unlike the bipolar type, the channel current is not controlled by the flowing of a current into the gate, but controlled by applying an electromagnetic field to the gate.

4) Input resistance is very high and about 10^{10} ohms, since the gate (input electrode) is insulated from the silicon substrate with a silicon dioxide layer.

Also, since a capacitor is formed by the gate electrode and the substrate, then it has several PF capacitance, and its impedance decreases in higher frequency range. From the view point of subminiaturization (LSI), fan-out of over 25 can be driven.

5) Large Voltage Swing is obtainable.

Since an amplitude of over 10V is obtained with its high impedance and vacuum tube-like characteristics, so ON-OFF discrimination is very easy.

3.2 Principle of N Channel MOS IC

The MOS IC based fundamentally on MOS Field Effect Transistor is employed for subminiaturizing IC's to the ultimate limit accompanying scale-up of IC's and increase of reliability.

This has advantages in cost reduction and highly dense integration greater than an IC using ordinary bipolar transistors. Now, the MOS transistor will be introduced before detailing its principle and characteristics.

3.2-1 N-Channel Enhancement MOS Transistor

1) Unlike the conventional bipolar transistor, surface conductivity of MOS transistor is controlled by vertically applying an electronic field to the semiconductor through a thin insulating layer of silicon dioxide. For the structural principle, see Fig. 3-1 (a), (b), (c).

As shown in the Fig. 3-1 (a), the prototype structure is very simple with two N-type regions on P-type silicon substrate insulated by a thin insulating layer of silicon dioxide on which an electrode is provided.

The two N-type regions are called "Source" and "Drain". The electrode (center) on the silicon dioxide layer is called "Gate". This gate electrode and the P-region beneath the dioxide layer serve as a capacitor (C_G).

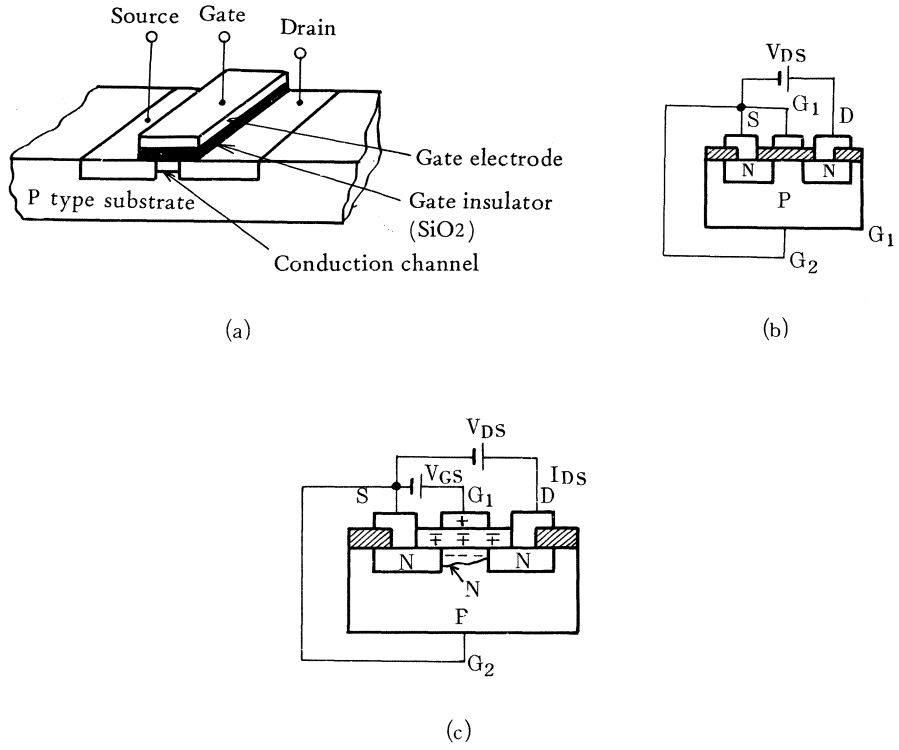


Fig. 3-1 Principle drawing of N channel MOS Transistor

When V_{DS} is applied between the source and the drain, and connect the gate is connected to the source as shown in Fig. 3-1 (b), nothing will occur in the silicon substrate beneath the dioxide layer; but slight leakage current flows. Since the substrate is P-type silicon, then normally, only the holes exist. However, when V_{GS} is applied between the gate and the source, hole movement is gradually cancelled by induced electrons.

Further increase of the gate voltage produces N-type channel (See Fig. (c)) between the source and the drain due to electron conduction, and the current starts flowing.

The MOS transistor with P-type silicon substrate and N-type conductive channel is called "N channel MOS FET", while one with N-type silicon substrate and P-type conductive channel is called "P channel MOS FET".

On the other hand, the concentration of electrons or holes beneath the insulating layer varies according to the gate conditions, and the two types of transistors are obtained from the operation characteristics as shown in Fig. 3-3.

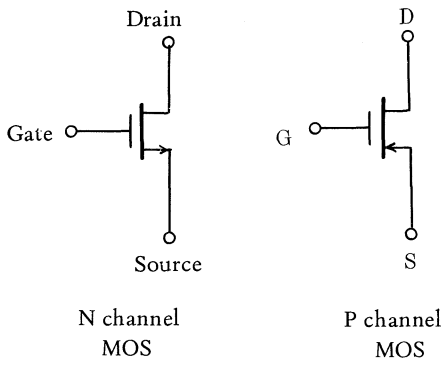


Fig. 3-2 MOS Symbol

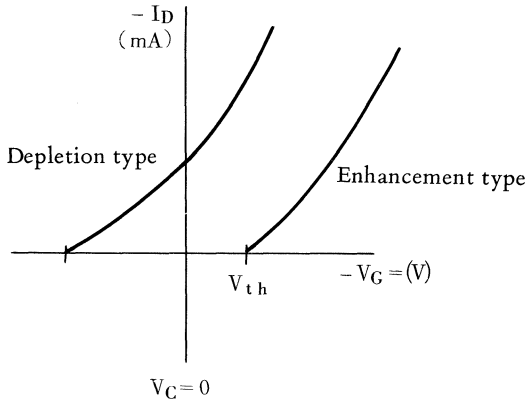


Fig. 3-3 MOS Characteristics

(a) Depletion type (B) in which carriers are present in the channel with zero bias.

(b) Enhancement type (A) in which the current does not flow when no gate voltage is applied; but the current flows when forward bias is applied to the gate.

3.2-2 P-channel Enhancement Type MOS Transistor

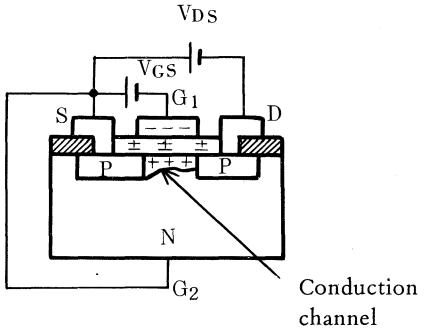


Fig. 3-4 Principle drawing of P-channel MOS Transistor

P-channel type represents characteristics entirely opposite to those of N-channel type. When a negative gate voltage is applied, the channel is induced and only the channel beneath the gate electrode becomes a conductive region. The characteristics of the P-channel MOS transistor are the same as in the N-channel type, but the polarity of the applied voltage is opposite.

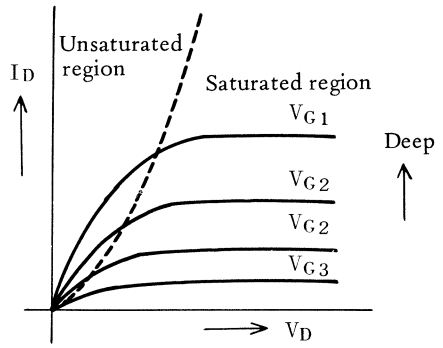


Fig. 3-5 MOS Transistor Characteristics

The unsaturated and saturated regions in Fig. 3-5 depend on the following relation between V_D and V_G.

Unsaturated region: $|V_D| < |V_G| - |V_{th}|$

Saturated region: $|V_D| \geqq |V_G| - |V_{th}|$

Employing these saturation characteristics, MOS transistor can be used as a load resistor in the MOS inverter circuit.

Generally, in the manufacturing process, P-channel type becomes the enhancement type and N-channel type the depletion type.

3.3 MOS LSI Basic Circuit (Positive Logic)

The shift register and R O M partially use negative logic in EP 150 according to the relation with other circuits. However, in Pocketronic, only the positive logic is used; but care must be taken in the definition of the signal levels because they differ from that in the conventional positive logic.

3.3-1 Load MOS

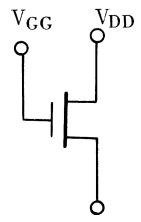


Fig. 3-6 Load MOS

In MOS IC or LSI, MOS transistors can be used as load resistor; but in the bipolar type, difused resistors must be used to the transistors, thus increasing the area needed. This is the great difference in the characteristic between MOS and bipolar types.

When the gate and drain in Fig. 3-6 are connected in common, the enhancement mode of MOS always operates in a saturated area, because the saturation condition of MOS is $|V_D| \geq |V_G - V_{th}|$

where V_D: Drain voltage
V_G: Gate voltage
V_{th}: Threshold voltage

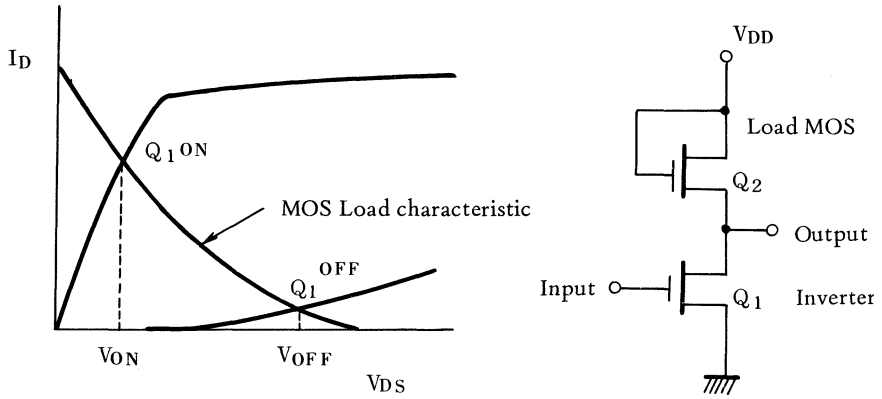


Fig. 3-7 Load Characteristics of MOS

Usually, an inverter of MOS IC or MOS LSI is connected to a MOS load resistor which has such characteristics. This inverter circuit has the characteristic of a momentary storage with the gate capacitance.

MOS gate input impedance has a very high capacitance since the gate is bonded to the insulating layer on the substrate, and as shown in Fig. 3-8, information can be stored for a considerably longer time by charging to the input capacitance.

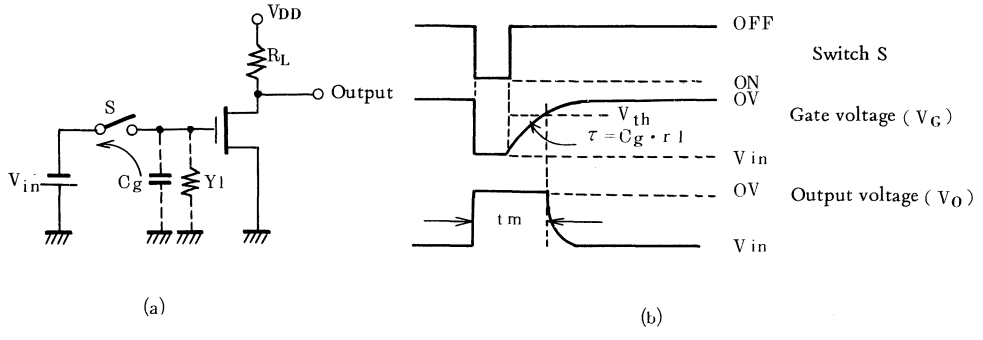


Fig. 3-8 Capacitor Memory of MOS transistor

When the initial gate voltage is OV, then as soon as the switch S is turned on, the input capacitor Cg is charged according to the input voltage Vin, then MOS transistor turns ON. When turning off the switch S, the gate input terminal is released, and if it is in the ideal state, there is no leak resistance, thus there is no discharge; but actually there is a leak resistance of the gate ($10^9 \sim 10^{10}\Omega$), therefore, Cg starts discharging through it. The time constant (τ) is the product of the input capacitor and leak resistor, then the decrement of the gate voltage V_G can be expressed by;

$$V_G = -Vin \exp\left(\frac{-t}{\tau}\right)$$
$$\tau = Cg \cdot r\ell$$

Even though switch S is released, MOS transistor Q_1 is still conducted and until V_G comes to the Q_1's threshold voltage V_{th}, it remains ON; but as soon as V_G becomes lower than V_{th}, it becomes OFF. The time required until the gate voltage V_G diminishes to V_{th} level can be called information storage time of MOS transistor with the input capacitor. Utilizing this characteristic, a dynamic shift register is constructed as described later.

3.4 Logic Circuit

Since LSI's are partially used in EP 150, negative logic is employed for the LSI's. However, Pocketronic uses all LSI's with positive logic; therefore, NOR, NAND & other circuits in this series are the reverse to those in EP 150. In this positive logic, the working voltage differs from those in the conventional IC circuits and LSI's.

	IC	LSI
"1" level	+5V	OV
"0" level	OV	V_{DD}

In IC's the allowable voltage ranges are as follows;

	Input voltage		Output voltage
"0"	Below 1V	"1"	Over 4.3V
"1"	Over 2.2V	"0"	Below 0.25V

In LSI, the signals from keyboard and the output voltage of MOS LSI are as follows;

"0" level	between $-5.2V \sim V_{GG}$
"0" level	between $0 \sim -1.5V$

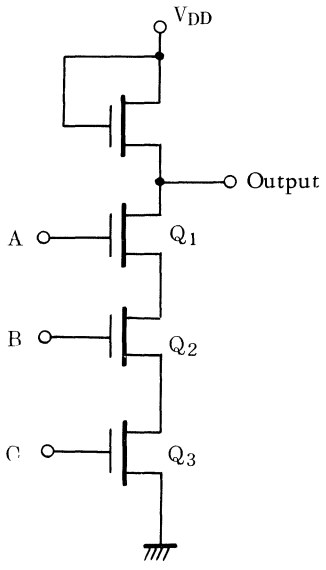
The operating voltages applied to LSI's are as follows;

	Rating	Fluctuation range
V_{DD} (Drain voltage)	−7.5V	−6.75 ~ −8.5
V_{GG} (Gate voltage)	−14V	± 10%

3.4-1 NOR Circuit (Positive Logic)

Each transistor is turned ON when the input signal becomes "0". The output signal is almost the same as V_{DD}, and Q_1, Q_2 & Q_3 are ON only when all input signals are "0", and the output signal becomes "1" (ground potential). If any of the input signals is "1", the corresponding transistor turns OFF with no drain current flowing, causing the output to become "0" (V_{DD}).

If only input A is "0" and B & C are "1", only Q_1 is conducted while Q_2 & Q_3 are not conducted. Therefore, no drain current flows and the output is "0".



A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

$$Q = \overline{A+B+C}$$

Table 3-1 Truth Table of NOR Gate

Fig. 3-9 NOR Circuit

3.4-2 NAND Circuit

When any input A, B or C is "0", the corresponding transistor turns ON, then its drain current flows. Therefore, the output voltage rises to the ground potential and becomes "1". The output becomes "0" only when all transistors turn OFF where all input signals are "1".

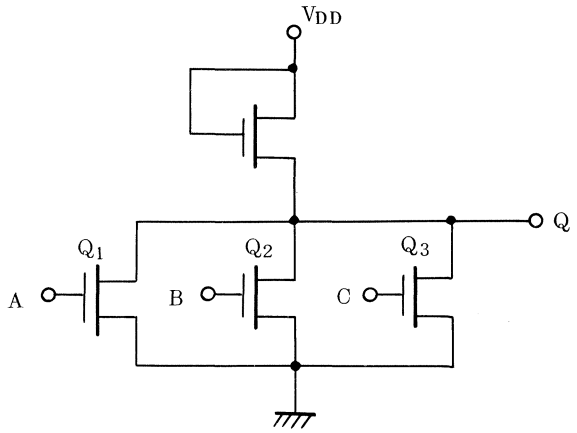


Fig. 3-10 NAND Gate

A	B	C	Q
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q = \overline{A \cdot B \cdot C}$

Table 3-2 Truth Table of NAND Gate

3.5 Flip-flop

3.5-1 Flip-flop

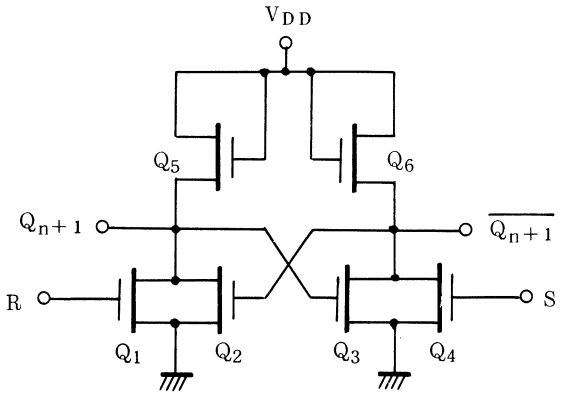


Fig. 3-11 R–S Flip-flop Circuit

In the R–S flip-flop of the MOS's, when R is "0" with S being "1"; then, Q_1 turns ON with Q_4 being OFF. So, Q_1's drain becomes "1" causing Q_3 gate to become "1". Since Q_3 & Q_4 are OFF, their drains become "0" which turns Q_2 ON. Therefore, Q_{n+1} is "1" while $\overline{Q_{n+1}}$ is "0".

When R is "1" with S being "0", Q_1 turns OFF with Q_4 being ON. Since Q_1's drain is "0", Q_3 turns ON, and the drain potential of Q_3 & Q_4 becomes "1". Therefore, Q_2 turns OFF with $Q_n + 1$ being "0" and $\overline{Q_n + 1}$ being "1".

When both R and S are "0", Q_1 & Q_4 turn ON irrespective of Q_2 & Q_3 conditions; so both $Q_n + 1$ & $\overline{Q_n + 1}$ are "1". Actually, this is the inhibiting condition.

R	S	Q_n+1	$\overline{Q_n+1}$	
1	1	Q_n	$\overline{Q_n}$	No change
1	0	0	1	
0	1	1	0	
0	0	1	1	Inhibit

Table 3-3 Truth Table

3.5-2 R–S–T Flip-flop

R or S input with clock pulse T passing through AND gate forms the R–S–T flip-flop, so as to synchronize R–S flip-flop with the clock pulse.

When R is "0" with S being "1", then clock pulse T becomes "0", thus Q_2 & Q_6 turn ON, so Q_1 also turns ON; but Q_5 can not turn ON and remains OFF state.

Since the drain of Q_5 is "0", then Q_3 turns ON, thus the output Q becomes "1" with $\overline{Q}$ being "0".

When the input R is "1" with S being "0" and the clock pulse T becomes "0", then Q_2 & Q_6 turn ON. Due to this, Q_5 turns ON with Q_1 remaining OFF, thus Q becomes "0" with $\overline{Q}$ being "1". Therefore, R–S–T flip-flop is always synchronized by the clock pulse.

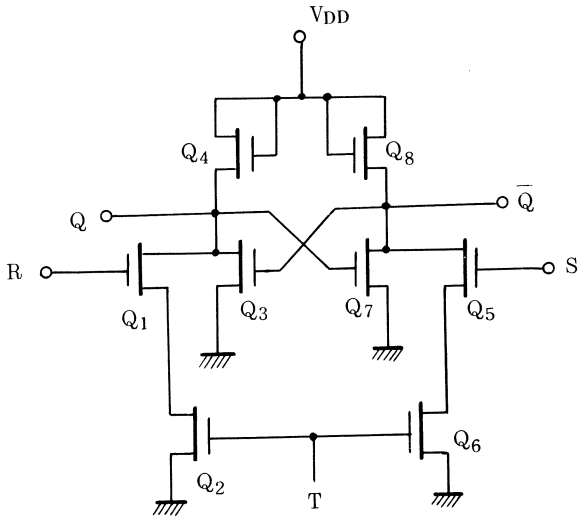


Fig. 3-12 R–S–T Flip-flop

3.5-3 Master-slave Flip-flop

The basic function of the master-slave flip-flop is about the same as in IC circuit. It consists of a master flip-flop and a slave flip-flop where the data entered in the master flip-flop is temporarily stored and then shifts to the slave flip-flop. Fig. 3-13 shows the detailed circuit structures.

In Fig. 3-13 (a), transistors $Q_1 \sim Q_4$ are a cross-coupled type DC flip-flop which forms the master flip-flop while $Q_5 \sim Q_8$ form the slave flip-flop. Fig. 3-13 (b) shows five additional transistors mounted on the substrate.

Q_9, Q_{10}, Q_{12} & Q_{13} change the basic circuits into an R–S flip-flop so that the master flip-flop can control the slave flip-flop. Q_{11} presets these functions as required.

Q_{14} & Q_{15} separate the functions between the master and the slave, so that they operate independently to stabilize their operation. Input data is stored in the master flip-flop by CP and then transferred to the slave flip-flop by $\overline{CP}$.

Q_{16} & Q_{17} convert the R–S flip-flop into a J–K flip-flop as shown in Fig. 3-13 (d) and as seen in the truth table, R–S flip-flop does not have an inhibited state; thus, when the input J or K is "0", the output has always the opposite condition of the previous state just before becoming the output signal.

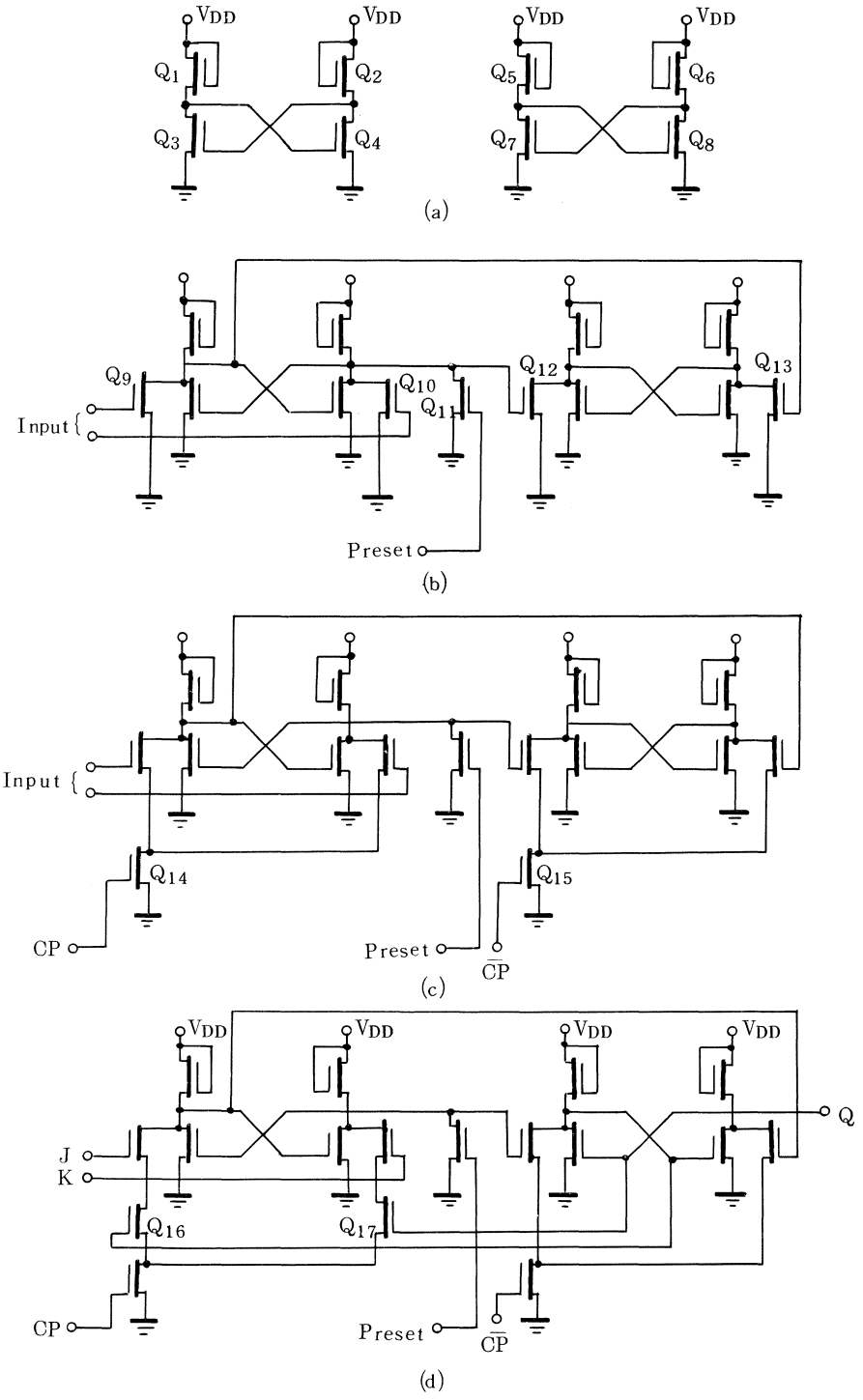


Fig. 3-13 Master-slave Flip-flop

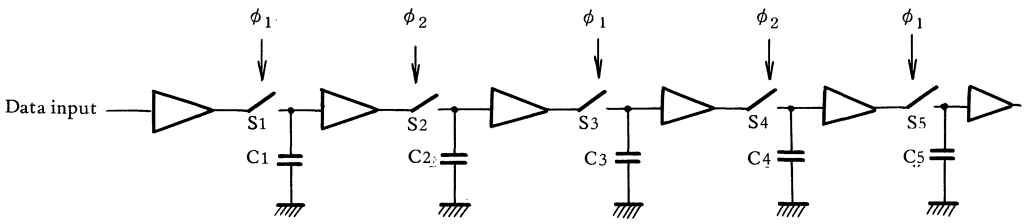
J_n	K_n	Q_n+1	$\overline{Q_n+1}$
0	0	Q_n	$\overline{Q_n}$
0	1	0	1
1	0	1	0
1	1	$\overline{Q_n}$	Q_n

Table 3-4 Truth Table of the Master-slave Flip-flop

3.6 Shift Register

3.6-1 Two-phase Shift Register

Utilizing the electronic characteristics of MOS, temporary storage of information can be done as previously described where a shift register having a specified capacity can be composed. This shift register can be classified into two-, three-, four- phase, etc. according to the number of clock pulses used. The principle concept consists of amplifiers, memory capacitance, and switches as shown in Fig. 3-14 (a).



(a) Principle of 2-phase Shift Register

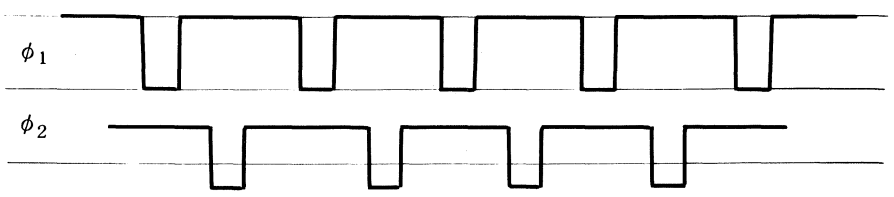


Fig. 3-14 (b) Waveforms of $\phi 1$ & $\phi 2$

The input data charges the gate capacitance of the second stage with $\phi 1$ clock pulse through the amplifier when S1 is closed. This output is fed to the next stage by $\phi 2$ when S2 is closed, thus the output is successively fed forward step by step according to the shift pulses $\phi 1$ & $\phi 2$. These switches are closed by $\phi 1$, $\phi 2$ whose phases differ from each other.

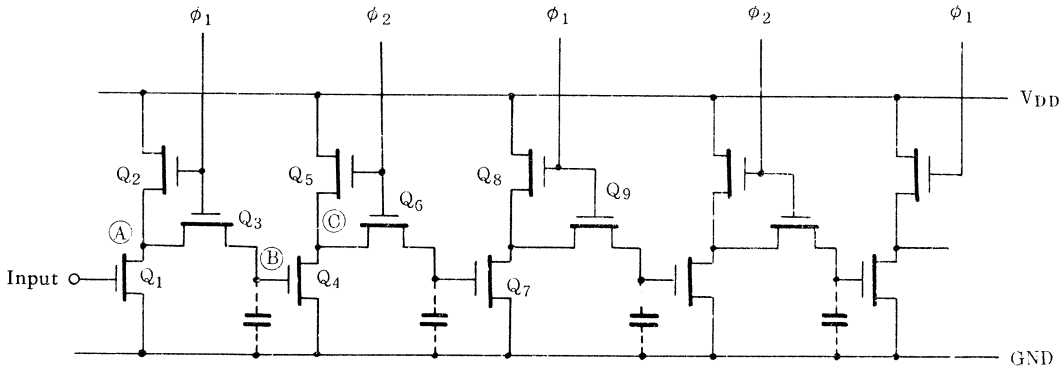


Fig. 3-15 Two-phase Shift Register

However, even though, the switch is open after $\phi 1$ time has elapsed, information is being stored by the gate capacitance until the next $\phi 2$ is applied. Fig. 3-15 shows a principle model of the Two-phase Shift Register with waveforms and phases at each stage.

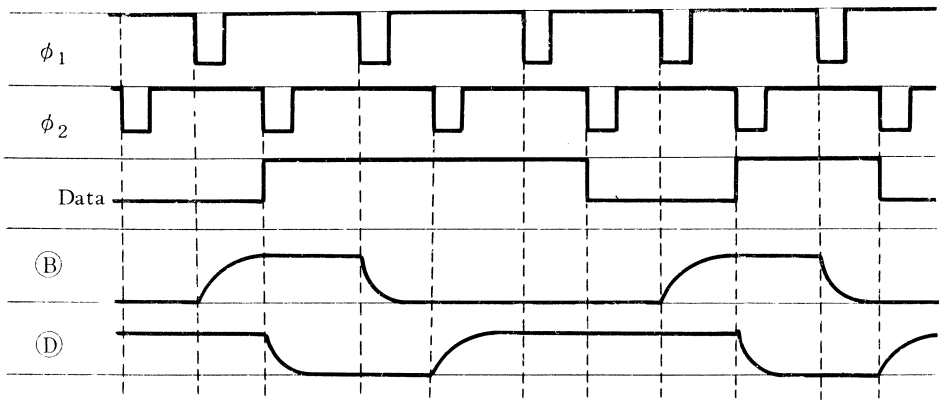


Fig. 3-16 Waveforms of Two-phase Shift Pulses $\phi 1$ & $\phi 2$

Assuming that two-phase clock pulses $\phi 1$ & $\phi 2$ are applied to the model circuit, then when the input data changes at the fall time of the clock pulse $\phi 2$, it is temporarily stored in the input gate capacitance causing Q1 to be ON with point

Ⓐ becoming "1". At this time ϕ_1 enters to control Q_2 & Q_3 gates, so Q_2 & Q_3 turn ON and point Ⓑ of Q_4 gate becomes "1".

Thus, the input signal of the first stage appears in the reverse polarity of this stage and temporarily stored at point Ⓑ. At this time, since the gate potential of Q_4 is "1", then Q_4 is OFF; so drain Ⓒ is "0". When ϕ_2 then enters, Q_5 & Q_6 turn ON to charge the gate capacitance of Q_7.

Since this capacitance remains "0" even though ϕ_2 becomes "1", then the input signal appears through these two stages after 1 bit time.

The same procedure is repeated thereafter; that is when the input data is "1", Q_1 is turned OFF by the next ϕ_1, and the input capacitor of Q_4 is charged to "0" by Q_3. When the next ϕ_2 enters, Q_7 turns OFF through Q_6 since Q_4 is ON'

Thus, data is shifted 1 bit successively by ϕ_1 & ϕ_2. Since the circuit stores the data only temporarily by the gate capacitance, the lower level of the clock frequency is limited by the time constant when charged capacitance is discharged.

The time constant is τ=CR where C is MOS gate capacitance and R is leakage resistance when MOS transistor is OFF which is about 10^{10} ohms.

The standard lower limit of the frequency is 10KHz while the upper limit is 250KHz ~1MHz.

ϕ_1, ϕ_2 are specified in Pocketronic as follows;

ϕ_1 shift pulse width:	2.5μs. (min)
ϕ_2 shift pulse width:	10μs. (min)
Phase difference T_1:	100ns. (min)
Phase difference T_2:	1μs. (min)

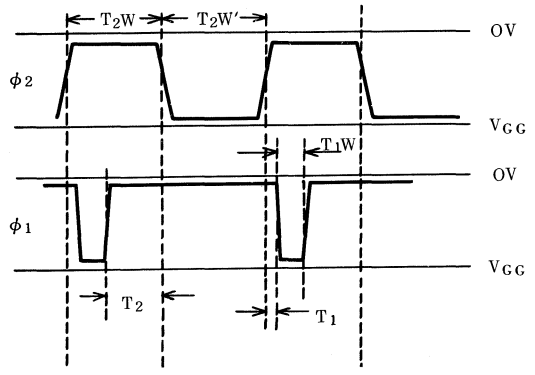


Fig. 3-17 Time Relation between ϕ_1 and ϕ_2

Fall time of the shift pulses are;

$\phi 1$	Less than 300nsec
$\phi 2$	Less than 300nsec

Clock pulse level of $\phi 1$, $\phi 2$

"1"	Minimum	−1V	Maximum	0V
"0"	Minimum	V_{GG}	Maximum	V_{GG} −1.0V

3.6-2 Three-phase Shift Register

The two-phase shift register is a dynamic shift register, in which data disappears when $\phi 1$ & $\phi 2$ clock pulses are not applied. Therefore, in the two-phase shift register, data should be successively shifted repeatedly by clock pulses.

The three-phase shift register is designed so that it can function under a static condition. Data is shifted by the shift pulse consisting of three clock pulses $\phi 1$, $\phi 2$ & $\phi 3$. Therefore, even though $\phi 1$ disappears, the data still remains as long as $\phi 2$ & $\phi 3$ are applied. The data can be shifted a certain number of required bits when necessary and stores the data when it is not necessary to shift. This is the special feature of the three-phase shift register.

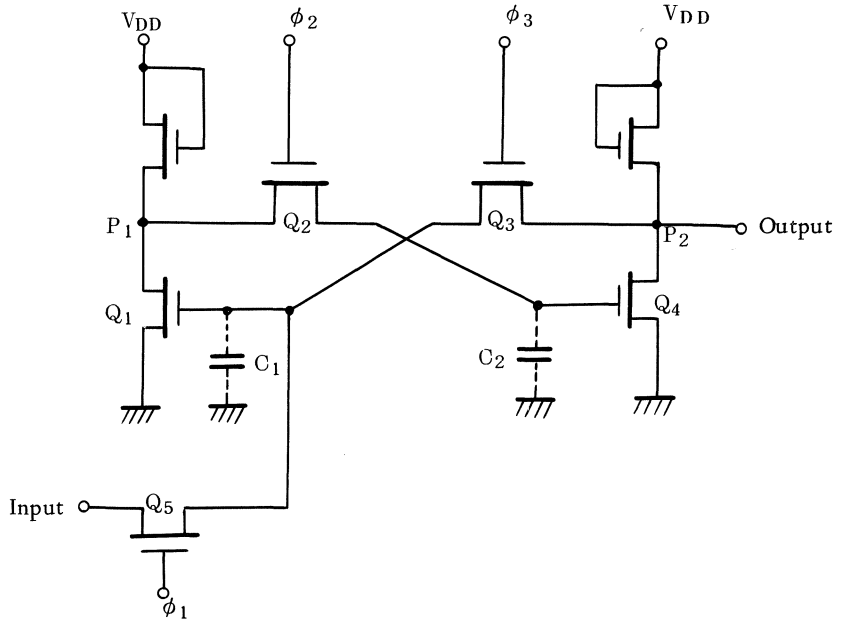


Fig. 3-18 Three-phase Shift Register

The three-phase shift register circuit is a dynamic shift system employing MOS gate capacitance combined with ordinary cross-coupled type flip-flop and functions under a static condition, and it prevents data extinction due to DC current.

When the input data of Q_5 is "1", and ϕ_1 becomes "0", then Q_5 is turned ON, so Q_1 gate becomes "1" causing Q_1 to be turned OFF.

Since Q_1 is OFF, the drain P_1 of Q_1 is "0", and when ϕ_1 is "0", then ϕ_2 & ϕ_3 are "1" with Q_2 & Q_3 being OFF. When ϕ_2 & ϕ_3 become "0", then Q_2 & Q_3 turn ON, and since P_1 is "0", the gate capacitance C_2 of Q_4 is charged by Q_2 to turn ON Q_4. When Q_4 is ON, P_2 becomes "1", then Q_1 gate becomes "1" by Q_3 and this condition is maintained until the next ϕ_1 clock pulse is applied.

ϕ_2 is designated so that its fall time is faster than that of ϕ_3; thus, when both ϕ_2 & ϕ_3 are ON and since the going low edge of ϕ_3 is after ϕ_2, then the data first shifts from P_1 to Q_4 gate and then from P_2 to Q_1 gate.

If waveforms of both ϕ_2 & ϕ_3 are the same, the gate voltages of Q_1 & Q_4 become very unstable with no distinction between ON & OFF condition.

When the input data is "0", Q_5 is turned ON by ϕ_1 with C_1 of Q_1 gate being charged causing Q_1 to be ON; thus P_1 becomes "1".

As soon as ϕ_1 becomes "1", ϕ_2 becomes "0", then "1" of point P_1 passing through Q_2 causes Q_4 to become OFF. A few moments later, Q_3 turns ON with point P_2 of Q_4 becoming "0"; thus, Q_1 gate becomes "0" by Q_3. Therefore, even though the clock pulse disappear, the condition of the output being "0" is still maintained.

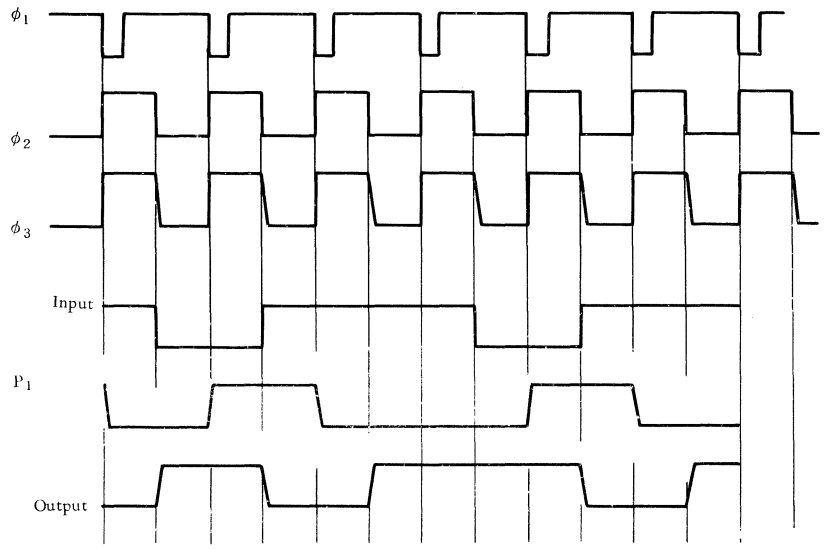


Fig. 3-19 Three-Phase Shift Register Timing

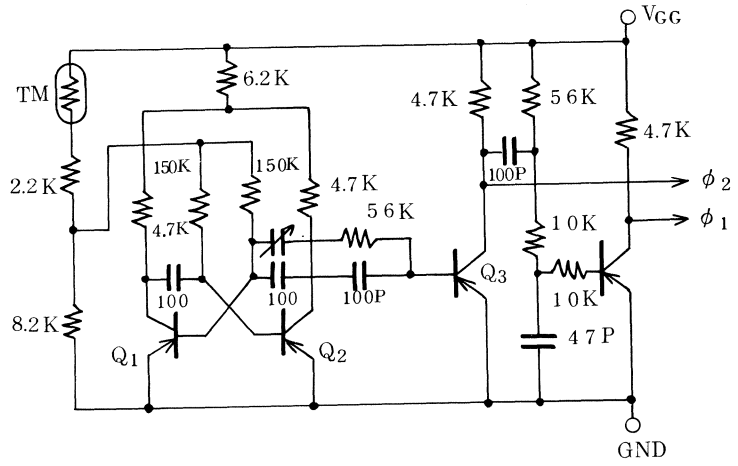


Fig. 3-20 $\phi 1$, $\phi 2$ Generator Circuit

Fig. 3-20 shows the $\phi 1$ & $\phi 2$ generator circuit of Pocketronic. The respective outputs of this free running multivibrator are $\phi 1$ & $\phi 2$. The variable range of the oscillation frequency is 30~60KHz, and this oscillator circuit is thermally compensated with a thermister TM. $\phi 1$ is produced by feeding the waveforms of the multivibrator output into the differential and integral circuit. Fig. 3-17 shows the timing relation of them. For adjustment, see troubleshooting procedure. Actually, this static shift register is used independently or groups of the shift registers are connected in series. The latter method is most widely used.

In Pocketronic, TB (4 bits), TD (13 digits), SCT (2 words) are dynamic registers while PR, PC, BR, ACC are static shift registers. The dynamic registers are used in such circuits where selection of time and bit numbers are not required.

3.7 PLA System (Programmable Logic Array)

Unlike the conventional models, Pocketronic employs PLA system with LSI's.

3.7-1 Purpose

Mainly used to reduce input/output terminals of LSI's.

3.7-2 Definition

This is a logic circuit system, in which program gates composed in a matrix form and flip-flops are provided in a chip for obtaining external output signals according to the programs made by combining the flip-flop states with external input signals and also for controlling these flip-flops according to the programs.

3.7-3 Features

(1) ROM (Read Only Memory)

* Logic (program) can easily be changed or added simply by modifying the aluminum mask in the production process.

* Since logic array is uniform and simple, logic error can easily be found in its designed process, and inspection after manufacturing can also be done easily.

* Since the matrix gates require no wiring, each chip has high density integration.

* Parallel connection of chips for "wired OR" coupling, and series connection of the chips are easily done.

(2) PLA (Programmable Logic Array)

* Since the chip has flip-flop circuits for timing control or certain a memory for conditions, the time control can automatically be done in the chip without external control.

3.7-4 Structure of PLA

(1) Block diagram

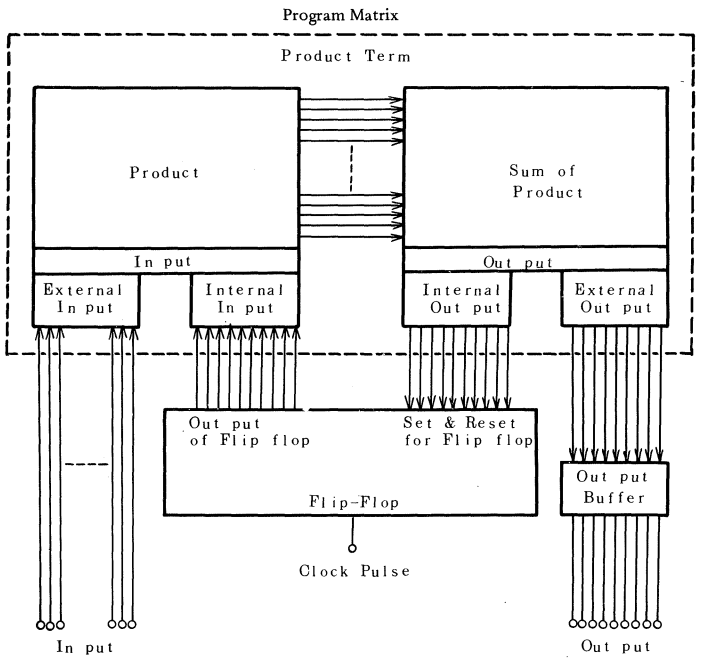


Fig. 3-21 Block Diagram of PLA System

(2) Logic Diagram

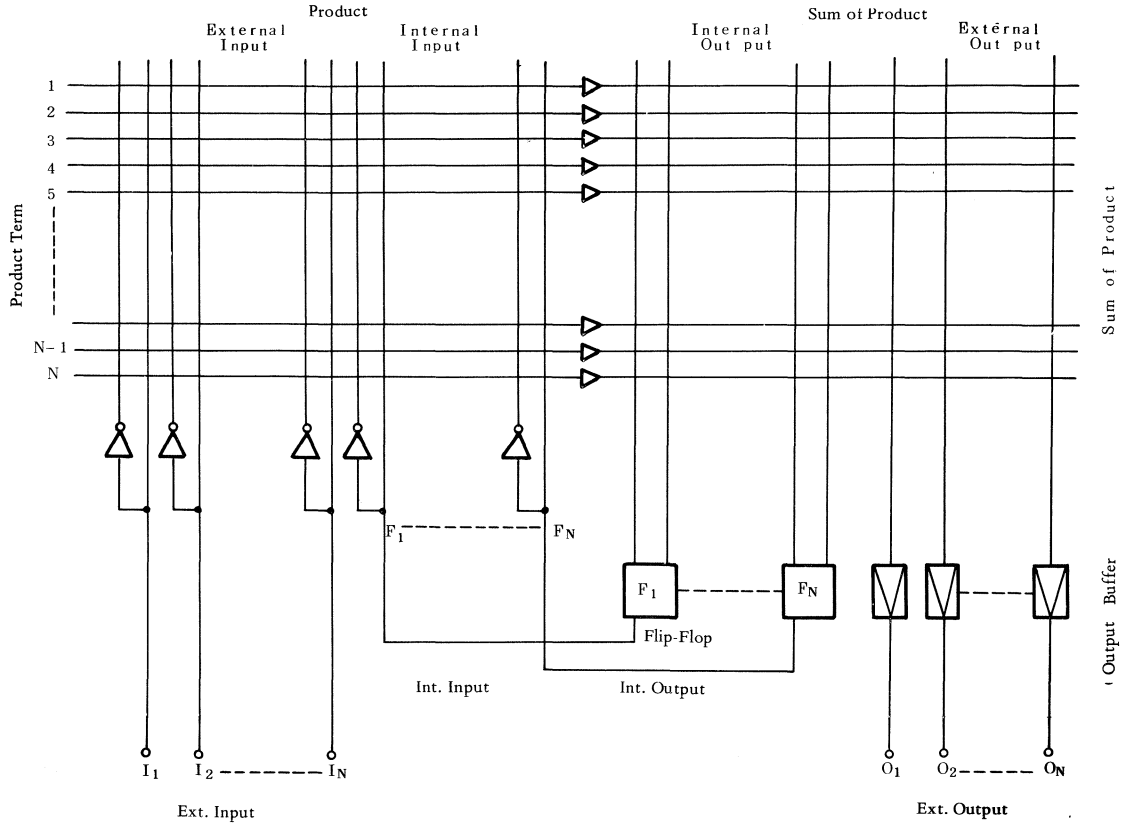


Fig. 3-22 Logic Diagram of PLA System

In this model, only the control chip uses the PLA system. When signals are applied from the data chip or timing chip to the input (external input) of the control chip, the internal output (controlling the flip-flop circuits) and the external output (controlling the data chip & timing chip) are obtained according to the combinations with the outputs (internal input) of the flip-flop circuits inside the control chip and external inputs. Thus, the control signals are successively fed from the control chip to the data and timing chips, so that the operation is done according to the programs.

For instance, when a command signal is applied, the flip-flop circuits inside the chip are set or reset when the signal meets the preset condition, thus causing the change in ON-OFF state of the chip with its own self-control.

In ROM, the output is affected only by the input signals with the corresponding output being obtained, while in the PLA circuit, the desired operation can be proceeded by generating control signals in the chip or changing the flip-flop states.

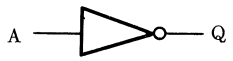
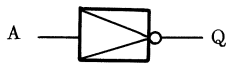
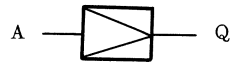
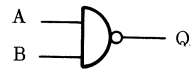
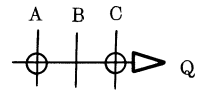
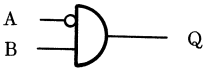
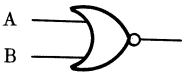
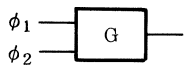
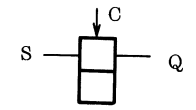
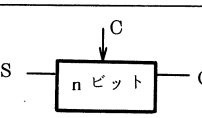
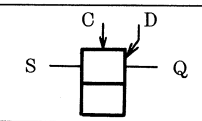
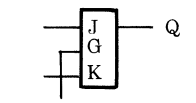
Symbol	Names	Logic	Remarks
	Inverter	$Q = \overline{A}$	
	Inverter	$Q = \overline{A}$	Without load MOS
	Inverting Buffer	$Q = \overline{A}$	
	Buffer AMP.	$Q = A$	
	NAND Gate	$Q = \overline{A \cdot B}$	
	NAND Gate	$Q = \overline{A \cdot C}$	P · L · A
	AND Gate	$Q = \overline{A} \cdot B$	
	NOR Gate	$Q = \overline{A + B}$	
	ϕ_3 Generator		
	Static Shift Register	$\begin{array}{c\|c} S & Q_n+1 \\ \hline 0 & 0 \\ 1 & 1 \end{array}$	
	n-bit Shift Register		
	Direct Set Static Shift Register	$\begin{array}{c\|c\|c} Q_n & D & Q_n+1 \\ \hline 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{array}$	
	J-K Flip-flop		

Table 3-5 Logical Symbols

3.8 Control Chip (TMC-1730)

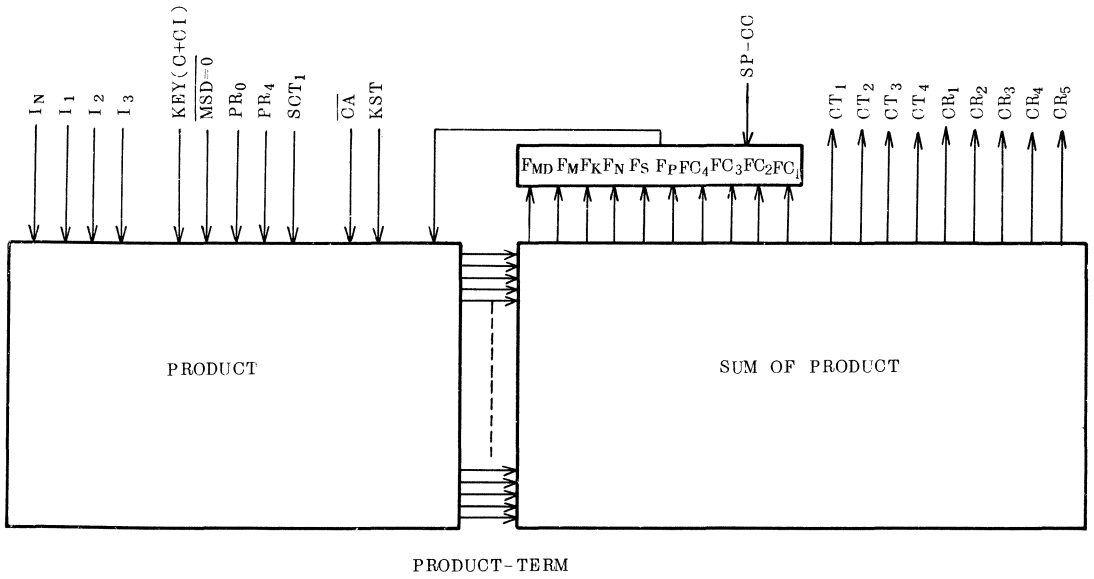


Fig. 3-23 Block Diagram of Control Chip in PLA System

As described in PLA system, the control chip is provided with external/internal inputs and internal/external outputs. Fig. 3-23 shows this control chip system where according to inputs PR_0, PR_4, SCT_1 & SP–CC from the timing chip, I_N, I_1, I_2, I_3, KEY (C+CI), $\overline{MSD=0}$, $\overline{CA}$ & KST from the data chip, and internal inputs F_{MD}, F_M, F_K, F_N, F_S, F_P & $FC_4 \sim FC_1$ of the internal outputs of the corresponding flip-flops, form external outputs $CT_1 \sim CT_4$ which control the timing chip, and external outputs $CR_1 \sim CR_5$ controlling the data chip.

$I_N \sim I_3$: Order signals from the data chip IR where $I_1 \sim I_3$ represent data symbols, and I_N discriminates between numeric and symbol signals.

$I_N = 1$	Numeric data
$I_N = 0$	Symbol data

PR_0 : 0 signal of point register

PR_4 : 4 signal of point register

$CT_1 \sim CT_4$: Output signals of control chip for controlling timing chip

$CR_1 \sim CR_5$: Output signals of control chip for controlling data chip

FM : Sets during multiplication

FM D : Sets during multiplication or division

FN : Discriminates whether the first digit registered numeral or the successive numeral and also discriminates others as described later.

FS : Sign flip-flop

FP : Discriminates whether decimal point key is pressed or not, and also discriminates releasing condition of zero suppressor & jumping condition from $\overline{CC11}$→$\overline{CC12}$→$\overline{CC9}$ during MLT or DIV.

FK : Discriminates whether the first constant division or the successive one.

FC1 ~ FC4 : Control Counters

3.9 Timing chip (TMC-1732)

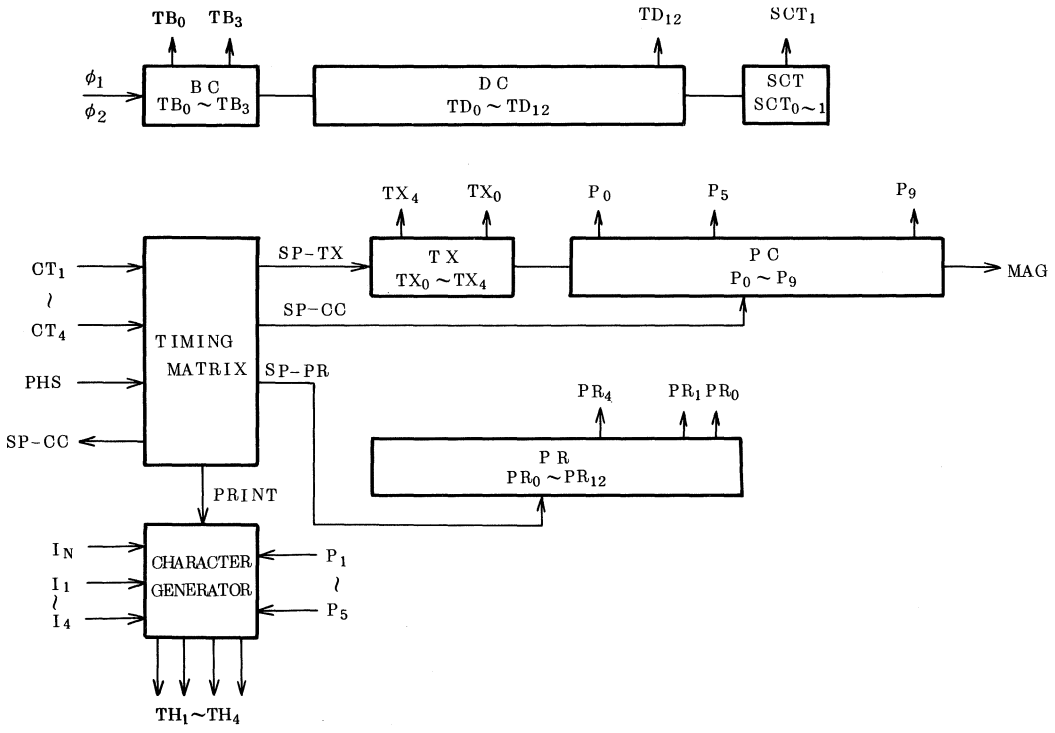


Fig. 3-24 Block Diagram of Timing Chip

The timing chip and data chip do not employ PLA system. These circuits are composed of gates, counters and registers. The bit counter (BC), digit counter (DC) & sector (SCT) are always counting. When the control signals $CT_1 \sim CT_4$ from the control chip enter the timing matrix and forms the timing of the output signals SP–Tx, SP–PC, SP–PR, PRINT & SP–CC. (SP: Shift pulse)

SP–Tx signal is counted by Tx counter which is 5-bit counter, SP–PC is counted by PC print counter which is 10-bit counter and SP–PR shifts PR point register which is 13-digit counter.

When PRINT signal is emitted during the time of $P_1 \sim P_9$, it forms the output $TH_1 \sim TH_4$ signals to the thermal heads (TH) for print-out on the thermosensitive paper. SP–Tx, SP–PC & SP–PR are shift pulses for the respective counter & register. When a certain condition is met in the matrix, the necessary pulses are generated and they start counting, and when there is no shift pulses they stop, which is one of the features of the static register.

3.10 Data Chip (TMC-1731)

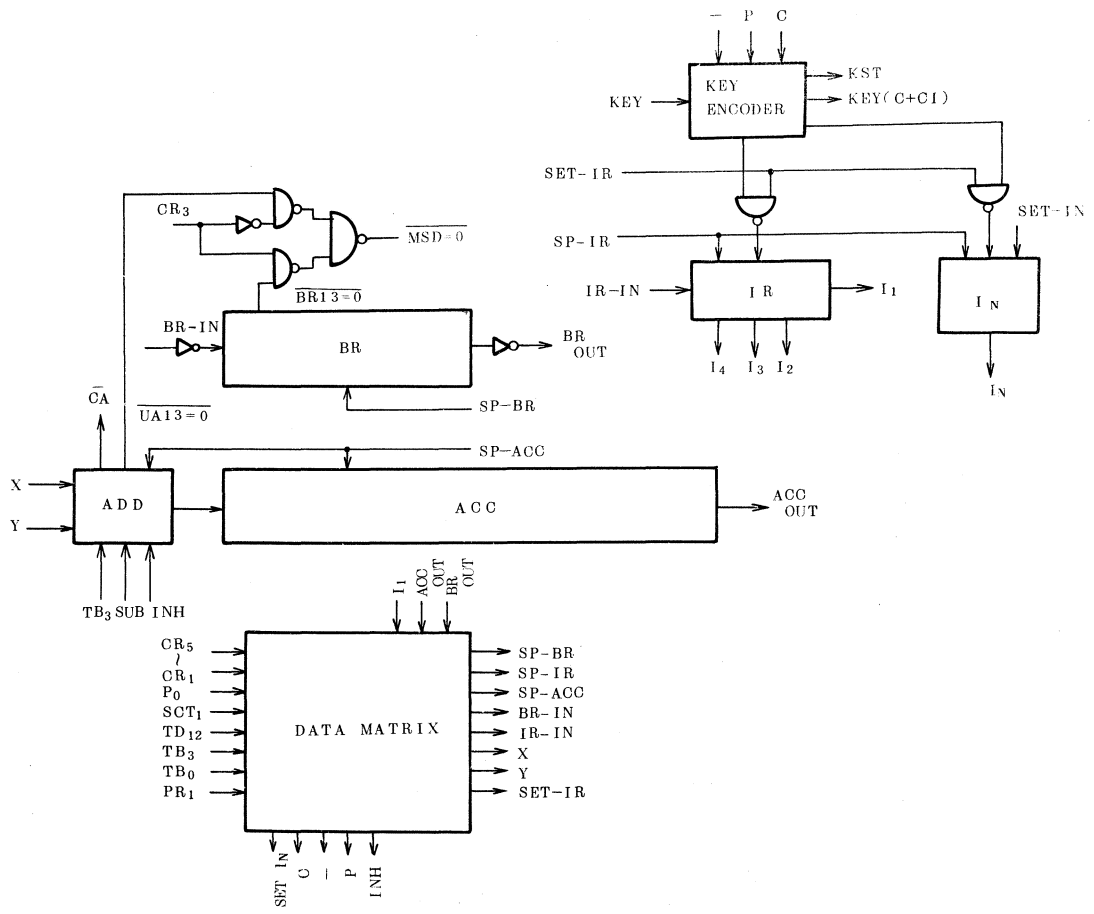


Fig. 3-25 Block Diagram of Data Chip

The data chip is composed of key encoder, indication register (IR), buffer register (BR), accumulator (ACC), adder/subtractor (ADD) and data matrix for controlling these elements. When $CR_1 \sim CR_5$ signals from the control chip, and SCT_1, TD_{12}, TB_3, TB_0, P_0 & PR_1 signals from the timing chip enter the data chip, then the output signals $\overline{MSD=0}$, $\overline{CA}$, KST, KEY (C+CI), I_N & $I_1 \sim I_3$ transfer to the control chip with I_N & $I_1 \sim I_4$ transferring to the timing chip. ACC is composed of UA and LA which are connected in series. MSD of UA is an external digit for compensating ADD. In the Fig. 3-25, C, −, P & SET I_N are the signals for the print-out in the calculated result.

SET−I_N:	Signal for setting I_N. When the calculated result or numeral is printed out, I_N is set. When the symbols of P, − & C are printed out, it is not set.
SET−IR:	Signal for setting IR
IR−IN:	IR input signal
SP−IR:	Shift pulse for IR
BR−IN:	BR input signal
BR−OUT:	BR output signal
SP−BR:	Shift pulse for BR
ACC−OUT:	Accumulator output signal
SP−ACC:	Shift pulse for accumulator
$\overline{UA_{13}=0}$:	Discriminating signal whether the 13th digit of UA is "0" or not.

3.11 Thermal Head

The thermal print head adopted in this printing system is divided into 20 blocks which consist of 5 rows and 4 columns and by the selection of these 20 blocks, letters, numerals & symbols are printed out. The collector resistors of the transistors of the selected blocks are heated instantaneously to about 100° C, thus printing on the thermosensitive paper is accomplished.

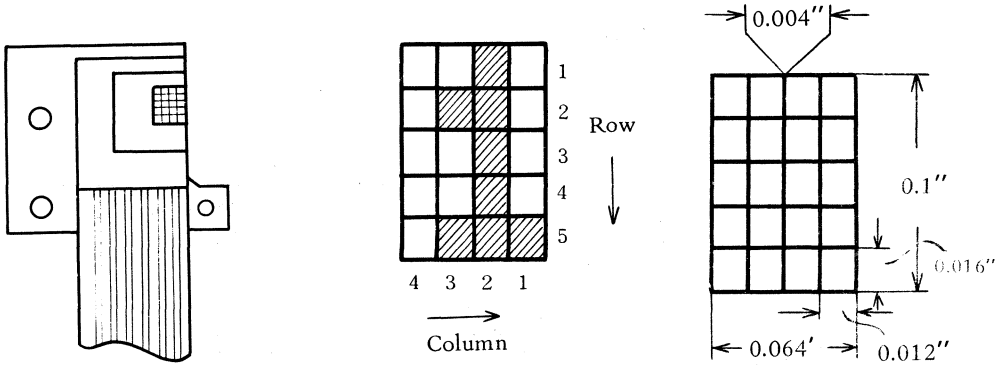
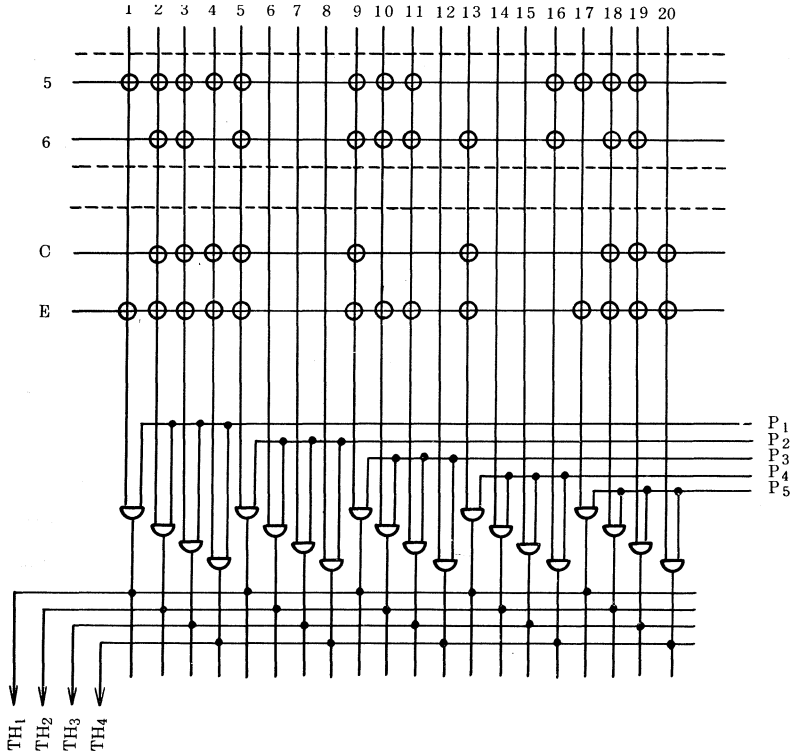


Fig. 3-26 Thermal Head

The size of the letter is determined by the dimension of the element which is 0.1″ high × 0.064″ wide while each block is 0.016″ high × 0.012″ wide. Each block is completely isolated and insulated from the others with a space of 0.004″.



		TH1	TH2	TH3	TH4
5	P1	1	1	1	1
	P2	1	0	0	0
	P3	1	1	1	0
	P4	0	0	0	1
	P5	1	1	1	0

P & TH signals of "5"

		TH1	TH2	TH3	TH4
6	P1	0	1	1	0
	P2	1	0	0	0
	P3	1	1	1	0
	P4	1	0	0	1
	P5	0	1	1	0

P & TH signals of "6"

		TH1	TH2	TH3	TH4
E	P1	1	1	1	1
	P2	1	0	0	0
	P3	1	1	1	0
	P4	1	0	0	0
	P5	1	1	1	1

P & TH signals of "E"

Fig. 3-27 Principle Block Diagram of the Print-out Matrix

In Pocketronic, the registered numeral and symbols are immediately printed after being decoded into printing signals in the printing matrix. Assuming that 5 key is pressed, then 1, 2, 3, 4, 5, 9, 10, 11, 16, 17, 18 & 19 become "1".

During the individual time of the $P_1 \sim P_5$ signals if a signal or signals are generated, then the corresponding $TH_1 \sim TH_4$ output signals are emitted in the thermal head to be printed out as shown in Fig. 3-28.

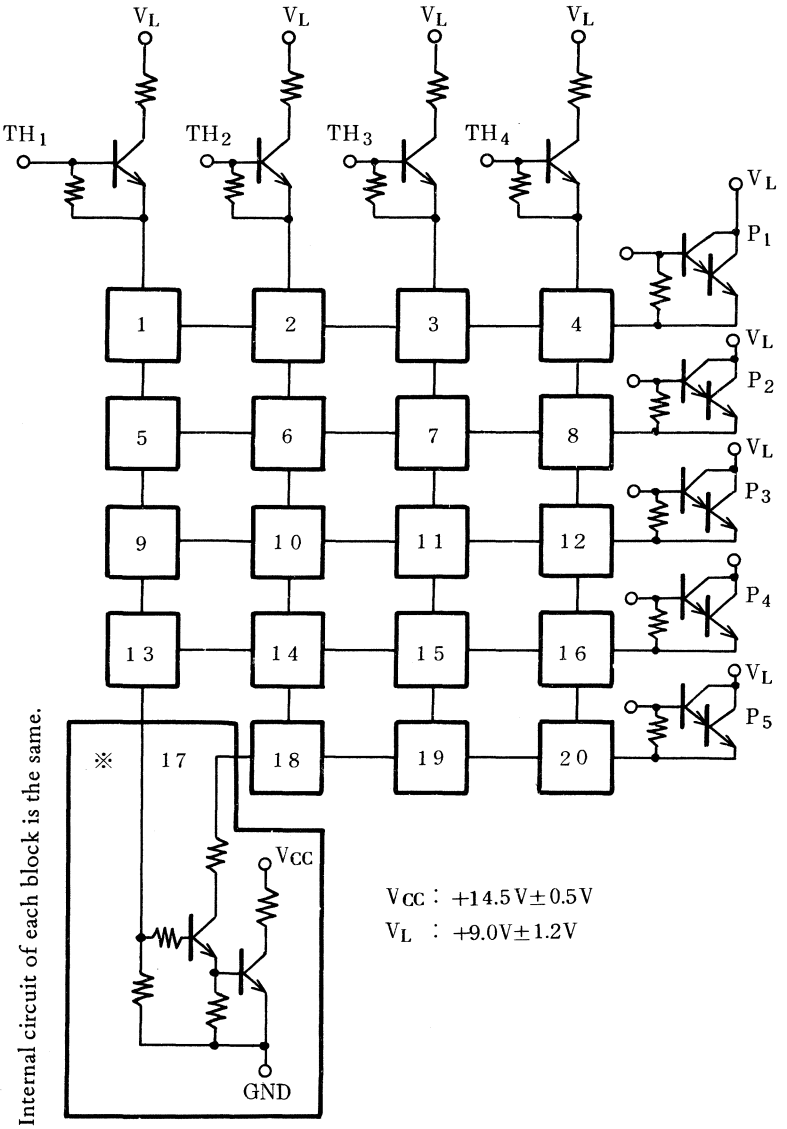


Fig. 3-28 Block Diagram of the Thermal Head

When [5] key is pressed, $TH_{1,2,3\ \&\ 4}$ become "1" during P_1 time, so the drive transistor for the thermo-transistor switches on, and according to the collector, certain parts of the element are heated. In this case, all of the first row of the matrix is ON, so the element block 1～4 in Fig. 3-28 are heated. During P_2 time, only TH_1 becomes "1", so only the element block 5 is heated.

Since $TH_{1,2\ \&\ 3}$ become "1" during P_3 time then element blocks 9, 10 & 11 are heated, and in P_4 time, only TH_4 is "1", so the element block 16 is heated while during P_5, $TH_{1,2\ \&\ 3}$ become "1" with element blocks 17, 18 & 19 being heated. Thus, when [5] is pressed, the figure is printed on the thermo-sensitive paper as shown in Fig. 3-29.

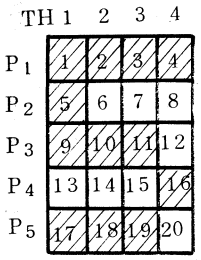


Fig. 3-29 Printing of Numeral 5

When [6], [CI] or [C] key is pressed, the printing is done as shown below;

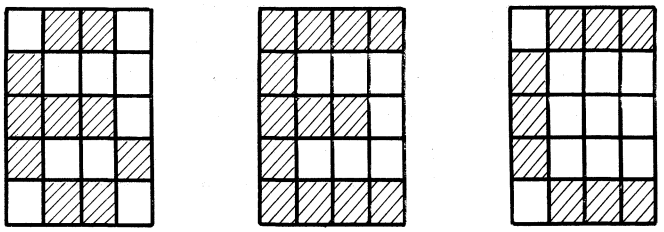


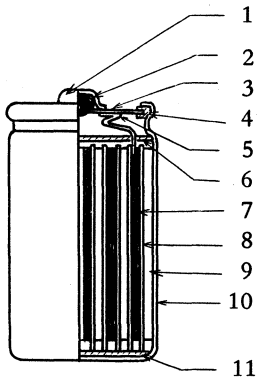
Fig. 3-30 Print-out of 6, E & C

3.12 Nickel-Cadmium Battery

3.12-1 Battery Structure

The Pocketronic is powered by a nickel-cadmium battery with both high rate discharge characteristics and excellent temperature characteristics. This battery, combined with Hi-speed Battery Charger 20A, shortens the conventional charging time of 14 ~ 20 hours to about 3 ~ 5 hours.

This compact get reliable high-performance nickel-cadmium type battery is also used to power space satellites. Constructed as illustrated below, it has very little internal resistance and is vibration-proof and mechanically solid in other respects.



1. Anode Cap (+) (Anode Terminal)
2. Safety Cap
3. Sealed Cover
4. Isolation Gasket.
5. Lead to Anode
6. Insulator
7. Anode Plate
8. Separator
9. Cathode Plate
10. Case (−)
11. Insulator

Fig. 3-31 Principle Structure of Ni-Cd Battery

3.12-2 Characteristics

(1) Specifications

NR-AA Ni-Cd Battery

Nominal Voltage	1.2V
Nominal Capacity	450mAh
Lifetime	More than 300 charge 1 discharge cycles
Charge Current	45mA
Charging Time	15 hours

NR-23AA Ni-Cd Battery

Nominal Voltage	1.2V
Nominal Capacity	225mAh
Lifetime	More than 300 charge 1 discharge cycles
Charge Current	45mA
Charging Time	15 hours

(2) Charge Characteristics

The charging method is divided into two ways, the constant current and constant voltage charge system.

i) In the constant current method, the battery is ordinarily charged at less than 0.1C current, and it is charged to actual capacity when approx. 140% of discharge is replenished.

Fully charging a battery which is 100% discharged, takes 14～16 hours.

ii) In the constant voltage method, charging is performed by a constant voltage and its current, large at the initial stage, decreases as charging proceeds. In this method, charging time is relatively short, but a special charger is required.

Either of two battery chargers is used to power.

For charging the Pocketronic, the Canon Hi-speed Battery Charger 20A utilizes the constant voltage charging system while the Canon Battery Charger 10A is the constant current charging system.

* "0.1C" is a charge and discharge current value which is expressed in the multiple of the nominal capacity (C).

For instance, if a battery has a nominal capacity of 450mAh, then 0.1C means 45mA; thus "0.2C" is 90mA.

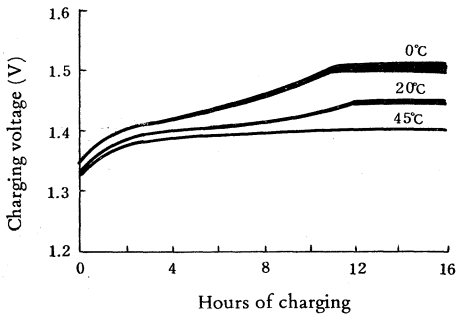


Fig. 3-32 Typical charge characteristics as a function of temperature (0.1C)

Charging should be carried out in a temperature range of 0°~+45°C to guard against a dropping of gas absorbability at low temperature and a dropping of charge efficiency at high temperature.

(3) Discharge Characteristics

Fig. 3-33 & 3-34 show the discharge characteristics of the NR-AA type battery.

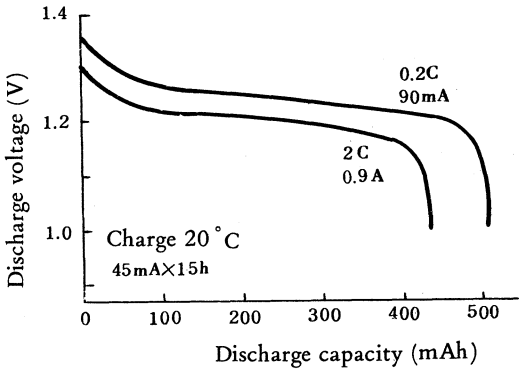


Fig. 3-33 Typical Discharge Characteristics of NR-AA

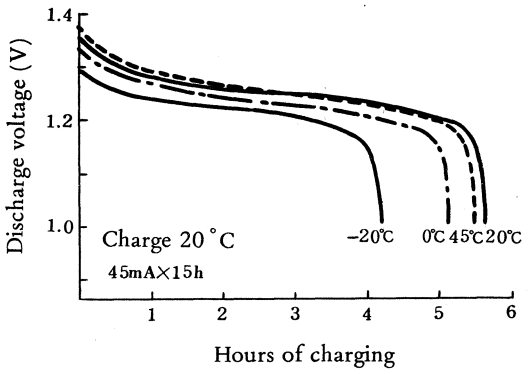


Fig. 3-34 Typical Discharge Characteristics of NR-AA between −20° and +45°C

As may be seen from Fig. 3-33, the voltage curve is on a plateau up to a certain point and the difference of capacity is also small.

As shown in Fig. 3-34, the change in discharge characteristics is relatively small in the wide range between -20° and +45°C.

Fig. 3-35 shows the internal resistance change during discharging of the NR-AA battery and a dry battery.

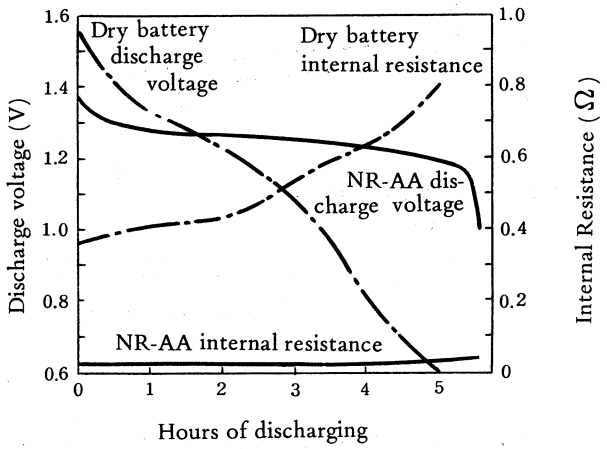


Fig. 3-35 Internal Resistance Change During Discharging

As shown in the above figure, the capacity per charging cycle is very large and the internal resistance change is very small.

(4) Lifetime

Battery lifetime, which is the number of times charging and discharging can be repeated with the battery characteristics not changing, depends on the user's condition.

Ordinarily, the battery lifetime is more than 500 charge 1 discharge cycles at room temperature; so the battery is very economical.

(5) Storage

Fig. 3-36 shows the self-discharge curves.

Self-discharge is relatively large as compared with that of a Manganese dry cell; but it is about the same as that of a lead dry cell.

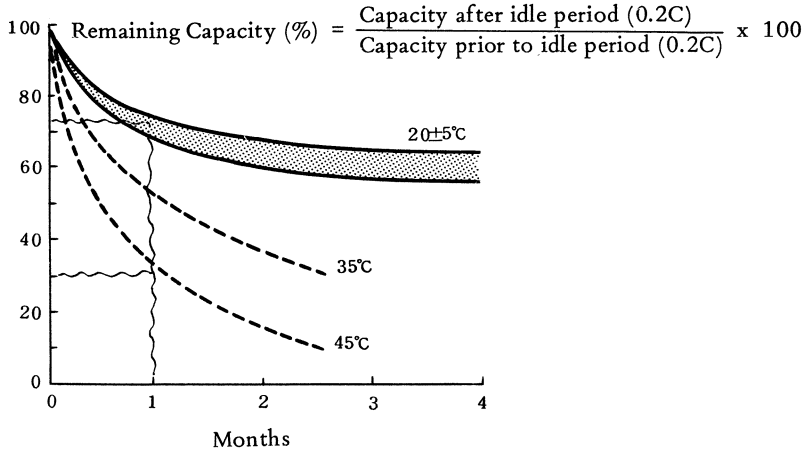


Fig. 3-36 Typical Self-discharge Curves

As shown in Fig. 3-36, self-discharge is about 30% in a month at room temperature; but the higher the temperature, the greater the speed of self-discharge; so it is advisable to store the battery in a cool and dry place.

OPERATION PRINCIPLE

CONTENTS

4. Operation Principle

This chapter concerns the registration of numerals, decimal point & orders and the functional operation process of the order keys ×, ÷ , C, CI, =, etc according to the flow chart. As described in the specifications, Pocketronic adopted the fix decimal point system of 4 digits with K constant key being always locked. Therefore, care must be taken on these two points in the understanding of the data decimal point and sign operation.

4.1 Print-out (except calculated result)

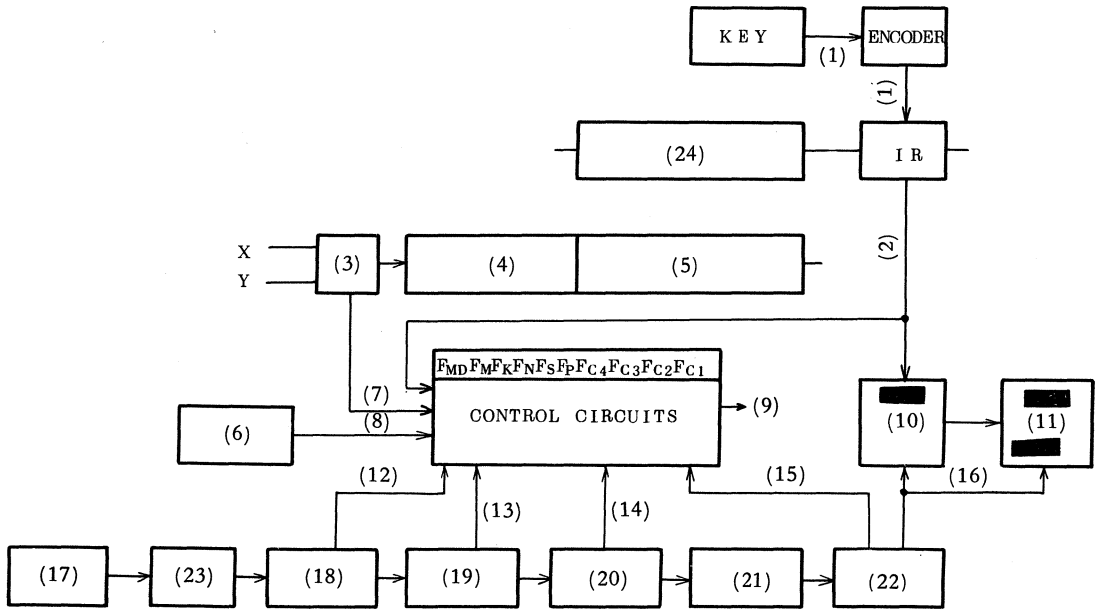


Fig. 4-1 Block Diagram

1) Key signal
2) Print-out signal
3) ADD (1-digit)
4) UA (12-digit)
5) LA (13-digit)
6) PR (13-digit) (POINT Counter)
7) CA signal
8) PR signal
9) Command of Timing & Data chips
10) CG (Character Generator)
11) TH (Thermal Head)
12) BIT signal
13) DIGIT signal
14) SCT signal
15) PC signal
16) Timing signal
17) Automatic Frequency Control Circui
18) BC (4-bit) (BIT Counter)
19) DC (13-digit) (DIGIT Counter)
20) SCT (Binary) (SCT Counter)
21) Tx (5-bit) (Counter)
22) PC (Decimal) (PRINT Counter)
23) Oscillator
24) BR (13-digit) (Buffer Register)

Pocketronic, when any key is pressed, first prints out the figure, because the key signal is encoded to its predetermined code and enters IR which includes IN. When a print instruction is emitted from the control chip to the timing chip, Tx & PC counters start counting. Then, the registered data in IR is fed to the character generator (CG) and its output is transmitted to the thermal head. Thus, a pattern corresponding to pressed key is printed out on the thermosensitive paper.

4.2 Registration

4.2-1 Numeral Registration of 1st Digit

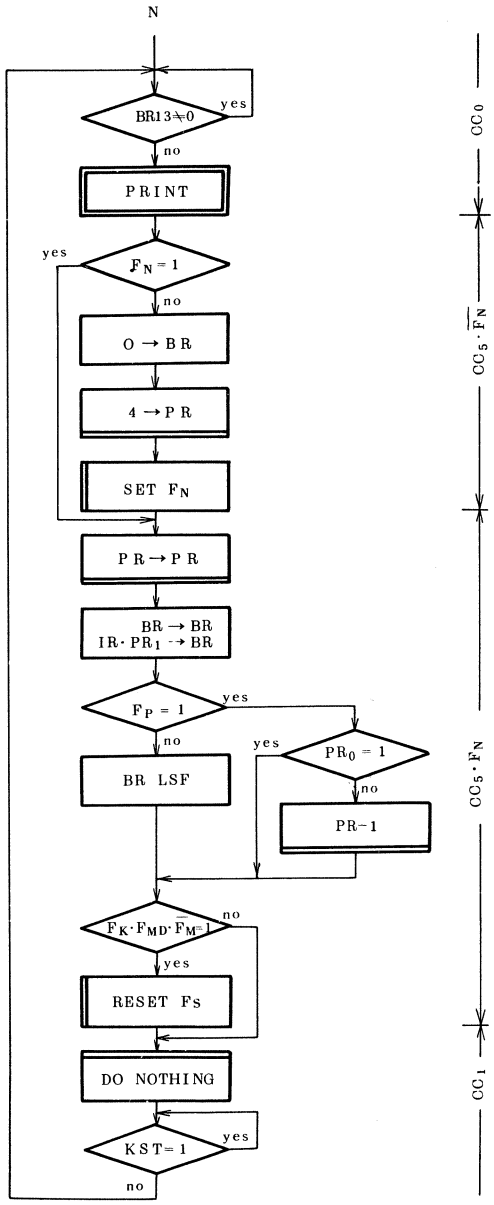


Fig. 4-2 Flow Chart of Numeral Keys

Registration method greatly differs from those of the former models, because the decimal point is fixed at 4 which complicates the conception of the logical structure.
However, the discrimination of the 1st numeral entry and 2nd or following numerals is the same as in the former models.

(1) When a numeral key is pressed, discrimination is done to check whether data is in the 13th digit of BR or not. When data enters the 13th digit there is no overflow function; but all operations stop whether registration or calculation and can only be started by pressing [C] or [CI]. This is one of the features of this model.
If BR13=0, the figure corresponding to the pressed key is printed out.

(2) After the pattern has been printed out, it proceeds to CC_5 to discriminate FN whether it is the first entry registration, where transfer of 0→BR which is the clearing of BR and shifting till PR_4 (4→PR) which coordinates the decimal point to 4. FN is set.

(3) At $CC_5 \cdot FN$, the data registered in IR when the key was pressed, transfers to BR. Since the decimal point is fixed at 4, so the transferring to the correct position in BR must be carried out at certain specified timing.

IR data enters BR when PR becomes PR_1 ($PR_1 \cdot IR \rightarrow BR$) which is during the operations of PR → PR & BR → BR, and enters the 4th digit position of BR.
If a numeral registration is done before pressing ⊡ where $\overline{FP}$ is "1", then a left shift of one digit is done since it is an integer. (In numeral registration after pressing ⊡, see 4.2-4).
Also, in the dividend registration of the 2nd constant division, Fs is reset because F_K is "1".

(4) At CC_1, nothing happens except the discrimination of KST whether the key is kept pressed or released. The former models employ the one-shot multivibrator (KST → OS → FT → FU).
However, Pocketronic does not have this circuit, so operation stops at CC_1 if the key is kept pressed and returns to CC_0 after the key is released.

4.2-2 Registration of 2nd or Following Digit

After the printing is done at CC_0, since FN=1, then 0 → BR & 4 → PR operations are not done; but the operations of BR → BR, $PR_1 \cdot IR$ → BR, & the left shift of BR are done.

Thus, the numeral registers in the 4th digit position of BR and then shifts left one digit which is above the fixed decimal point position. This is the same procedure for all successive integral numerals after the 1st numeral has been registered.

4.2-3 Registration of Decimal Point

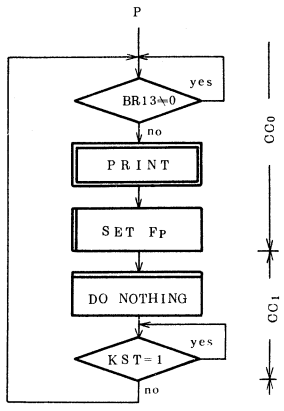


Fig. 4-3 Flow Chart of Decimal Point

The decimal point registration procedure is the same whether the numeral key is pressed before or after the ⊡ key.

When ⊡ is pressed, the discrimination of BR13=0 is done at CC_0, and if there is no data in 13th digit of BR, then the decimal point is printed out which is the same as pressing a numeral key.

At the end of CC_0, FP sets and proceeds to CC_1, but nothing happens until the key is released and as soon as it is released, it returns to CC_0.

4.2-4 Numeral Registration after Pressing ⊡ Key

There are two different conditions, one is when a numeral is entered before pressing ⊡ key (N ⊡ .....), and the other is when the ⊡ key is pressed first with the numerals being entered later (⊡ N .....).

In the former case, the operation proceeds to $CC_5 \cdot FN$ from CC_0; but in the latter case it is from $CC_0 \rightarrow CC_5 \cdot \overline{FN} \rightarrow CC_5 \cdot FN$. At $CC_5 \cdot FN$, the transferring of BR → BR and $PR_1 \cdot IR \rightarrow$ BR are done with the data entering the 4th digit position of BR; but since FP=1, the left shift of BR is not done; but the discrimination of PR_0 to detect the underflow of fraction is performed.

If $\overline{PR_0}$ is "1", then PR−1 is done. Following operations are practically the same procedure as in numeral registration before pressing ⊡ key.

PR−1 detects the number of registered digits below decimal point. If the registration continues, the BR→BR & $PR_1 \cdot IR \rightarrow$ BR operations are done at CC_5 FN, and since PR−1 is also carried out, the fractional numeral enters the following digit position until it becomes PR_0.

If this continues one more time, the data enters the 13th digit position of BR with all operation stopping. This is called underflow.

4.3 ⊠ or ⊡ Key Operation

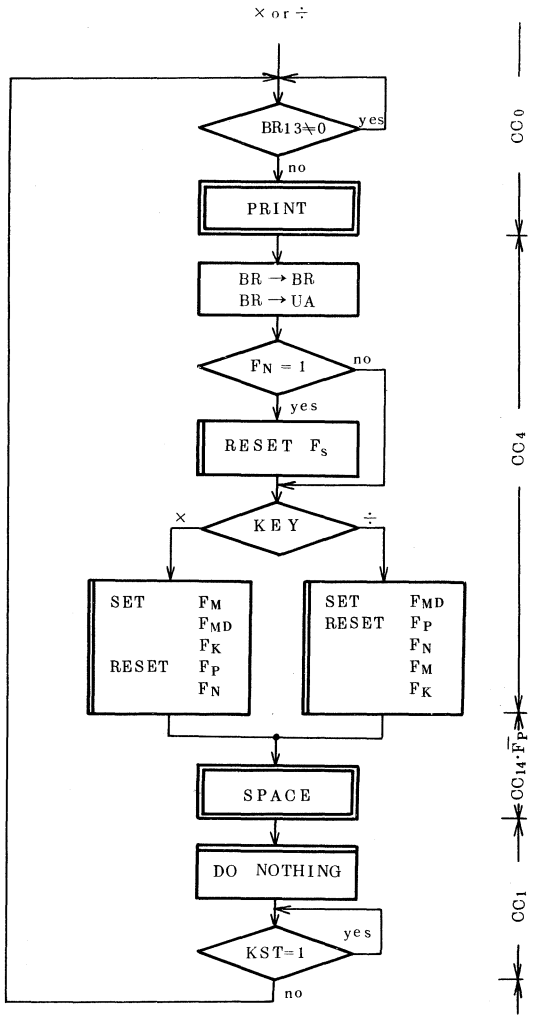


Fig. 4-4 Flow Chart of ⊠ or ⊡ key

(1) When ⊠ or ⊡ is pressed, the control counter does not proceed if it is BR13≠0 due to an overflow; but if BR13=0, then x or : symbol is printed out and operation proceeds to CC4.

(2) The transferring of BR→BR & BR→UA is done at CC4. This permits square calculation. If FN=1, it means it is a new calculation, and if the previous calculated result is negative with FS being set, then FS resets. The relation between FM and FMD is as follows;

FM	FMD	
0	0	..... Addition or Subtraction
0	1	..... Division
1	1	..... Multiplication

When ⊠ is pressed, FMD, FM & FK are set while FP & FN are reset.
When ⊡ is pressed, FMD is set while FP, FN, FM & FK are reset.

(3) At CC14·$\overline{FP}$, there is always one space blank after an order symbol.

(4) At CC1, nothing happens unless $\overline{KST}$ is "1" which is when the key is released with the operation returning to CC0.

4.4 [C] or [CI]

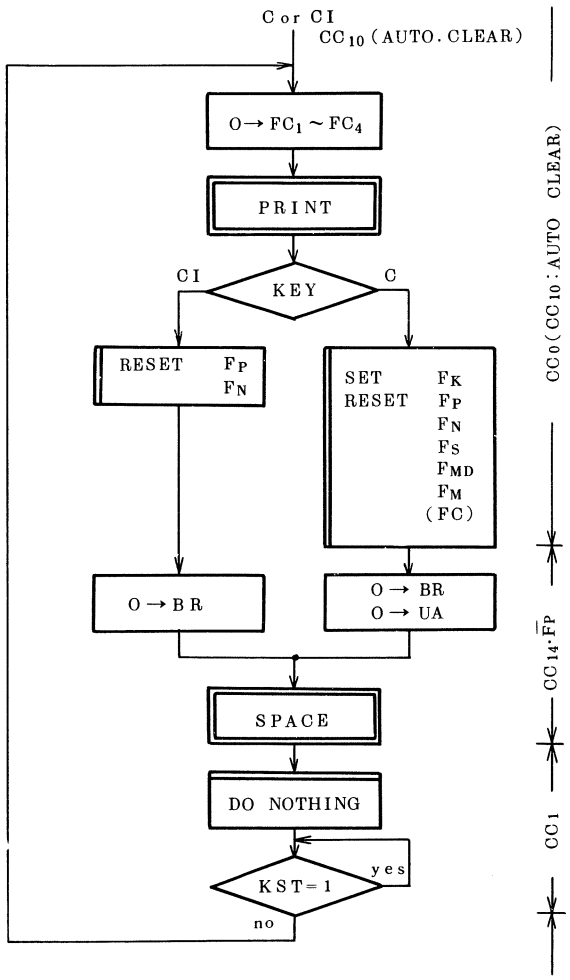


Fig. 4-5 Flow Chart of [C] or [CI] key

(1) When turning on the power switch, registers and various flip-flop conditions are at random; thus, it may have stopped at any control counter CCx, but usually it has returned to CC0 after passing through its preceding successive steps. Therefore, it must be cleared the calculator before starting any calculation by pressing [C] or [CI] key, then FC1 ~ FC4 are reset and control counter returns to CC0.

(2) At CC0, Symbol C or E is printed out. When [C] key is pressed, FK sets while FP, FN, FS, FND & FM are reset, but when [CI] key is pressed, FP & FN are reset and proceed to $CC_{14}\cdot\overline{FP}$.

(3) When [C] key is pressed, at SCT0 of $CC_{14}\cdot\overline{FN}$, the transferring of 0 → BR and ACC → ACC are done, and at SCT1, the transferring of BR → BR and BR → UA are then done; therefore BR & UA are cleared. However, when [CI] key is pressed, the transfer of 0 → BR is carried out, it means clearing of BR.

(4) At CC1, the procedure is the same as in registration.

(5) In an addition, subtraction, multiplication or division where overflow occurs, the operation proceeds to CC10 cycle and is processed in the same procedure as though [C] key is pressed with the flip-flop and registers clearing with symbol C being printed out. This is called auto clear in overflow operation.

4.5 ⊞ or ⊟

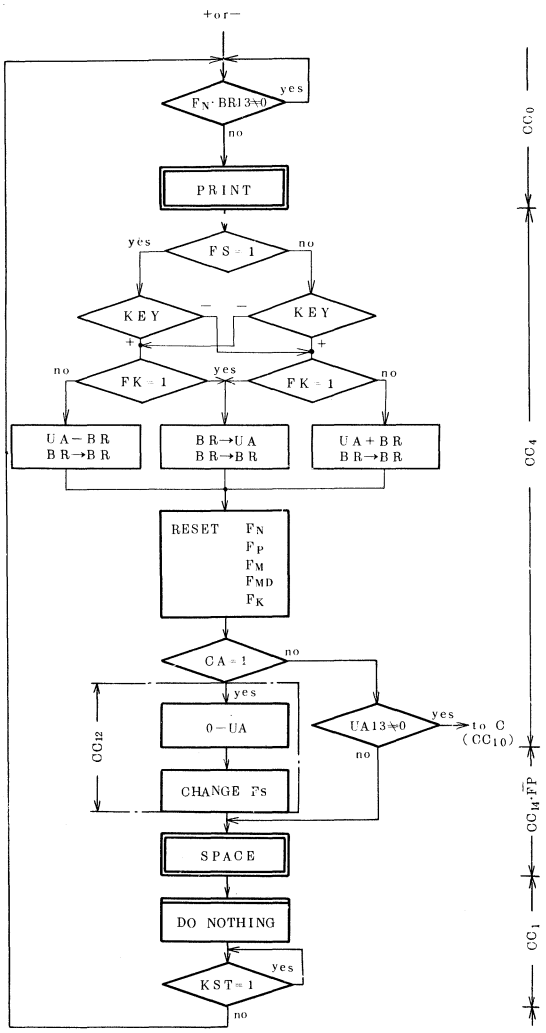


Fig. 4-6 Flow Chart of ⊞ or ⊟

(1) When ⊞ or − key is pressed, BR13=0 is discriminated, and if BR13=0, the + or − sign is printed out.

(2) At CC_4, FS is discriminated to see whether the previous operation result is positive or negative.

$\overline{FS}\cdot$⊞ ..... Addition
$\overline{FS}\cdot$⊟ ..... Subtraction
FS·⊞ ..... Subtraction
FS·⊟ ..... Addition

Addition or subtraction is done according to the above states which show what operation is done when ⊞ or ⊟ key is pressed with FS being set or reset. The addition & subtraction operations differ according to the conditions of FK.

Since FK sets as soon as C key is pressed, so when ⊞ or ⊟ key is pressed after certain numeric entering, then BR data transfers to UA. But, if either ⊞ or ⊟ key is pressed after next numeric entering, then the BR±UA operation is carried out because FK is reset. Since circulation of BR → BR, is carried out in this time, addition or subtraction can be done, then, FN, FP, FM, FMD & FK are reset.

In subtraction, if CA is emitted which is when + <− or − <+, then it proceeds to CC_{12} where 0→UA→UA & sign change of FS is done and then proceeds to $CC_{14}\cdot\overline{FP}$. If CA is not emitted, then the discrimination of UA13=0 which is the addition or subtraction overflow detection is carried out and proceeds to $CC_{14}\cdot FP$; but if it is UA13=0 operation proceeds to CC_{10} as though C key is pressed.

(3) At CC_{14}·FP, one space blank is given and operation proceeds to CC_1, where it remains and does nothing if the key is kept pressed; but it returns to CC_0 as soon as the key is released.

4.6 [=]

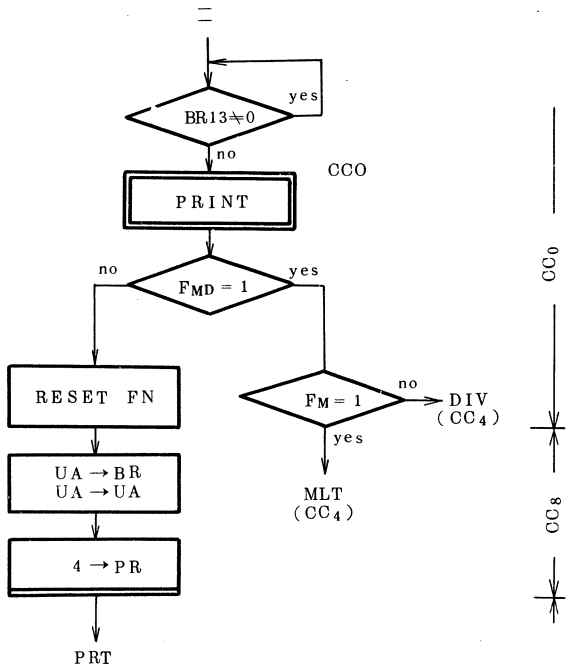


Fig. 4-7 Flow Chart of [=] key

(1) [=] key is the total key in addition or subtraction and the equal key in multiplication or division. In the discrimination of BR13≠0, = symbol is printed out when BR13=0 .
As described in [×] & [÷] key operation, in the FM D discrimination, FM D is "0" in addition & subtraction while FM D is "1" in multiplication or division, and FM is "1" for multiplication while FM is "0" for division.

(2) At the end of CC_0, FN is reset to proceed to CC_8, where the addition or subtraction result stored in UA is transferred to BR in the UA→UA & UA→BR operation and also the 4→PR operation is carried out since the decimal point is fixed at four. After these preparations, it proceeds to PRT for print out.

4.7 Multiplication

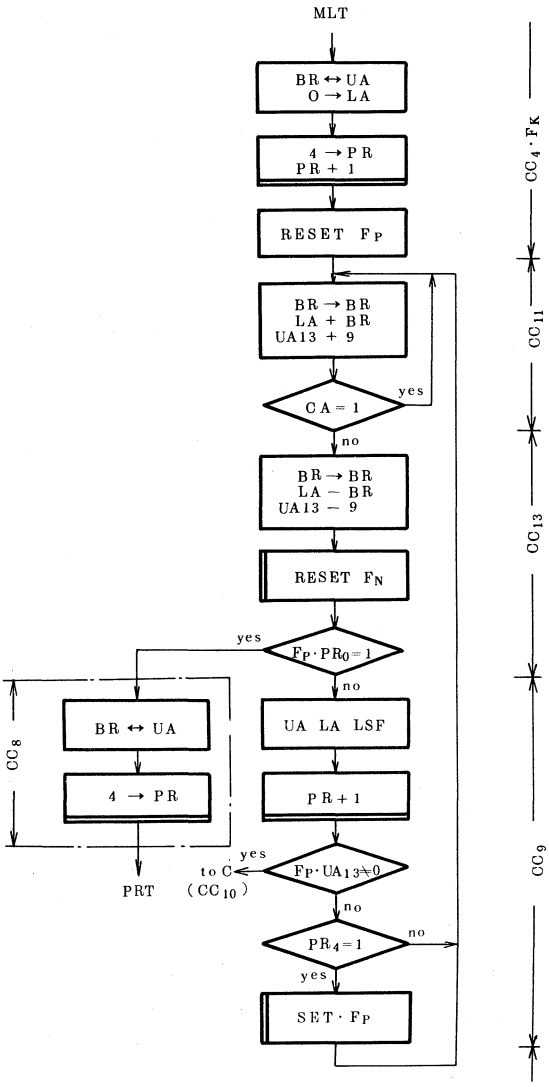


Fig. 4-8 Flow Chart of Multiplication

(1) At $F_{MD} \cdot F_M = 1$, multiplication is done, and since F_K becomes "1" in the first multiplication, then at $CC_4 \cdot F_K$, the interchange of BR ↔ UA is carried out, so that its multiplicand is the constant.
Then, the clearing of 0 → LA, presetting of decimal point of 4→PR & the PR+1 operation for the prevention of incorrect discrimination of PR_0 are performed, and then F_P is reset.

(2) Since multiplier is stored in UA, then at CC_{11}, UA13+9 which is the same as MSD−1 in the former models and the repetitive addition of LA+BR are carried out until CA is not emitted, then the partial product being obtained.
When no CA is emitted, then it has over-added one time.

(3) Since CA is not emitted, it proceeds from CC_{11} to CC_{13} with 9 being subtracted from UA13 to make it 0. Since overaddition was done one time too many, the correction cycle of LA−BR for the partial product is carried out which is BR→BR, LA−BR & UA13−9.

At CC_{13}, F_N resets which does not concern multiplication, only division as explained in 4.8 (3) so as to reduce the controlling signals for resetting of F_N for division.
At CC_{13}, discrimination of $F_P \cdot PR_0$ which is the jampping condition from the repetitive cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ is performed, that is, if $F_P \cdot PR_0$ is "1", it proceeds to CC_8 from CC_{13}; but if not, it proceeds to CC_9.

(4) At CC_9, left shift of partial product stored in UA·LA is done, and PR+1 is repeated each time the left shift is done, and when PR becomes PR_4 during PR+1, then FP sets. When FP is set, the cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ is repeated until PR becomes PR_0. If data enters the 13th digit position of UA after FP is set, it overflows and proceeds to the clear cycle of CC_{10}.

(5) When FP·PR_0 becomes "1" during repetitive cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$, operation proceeds to $CC_{11} \rightarrow CC_{13} \rightarrow CC_8$, and the product stored in UA interchanges with the multiplicand (constant) in BR, then PR is fixed to PR_4 which is the fixed decimal point 4. (BR$\longleftrightarrow$UA & 4 $\rightarrow$PR)

After these procedures, the operation proceeds to PRT cycle for print-out.

4.8 Division

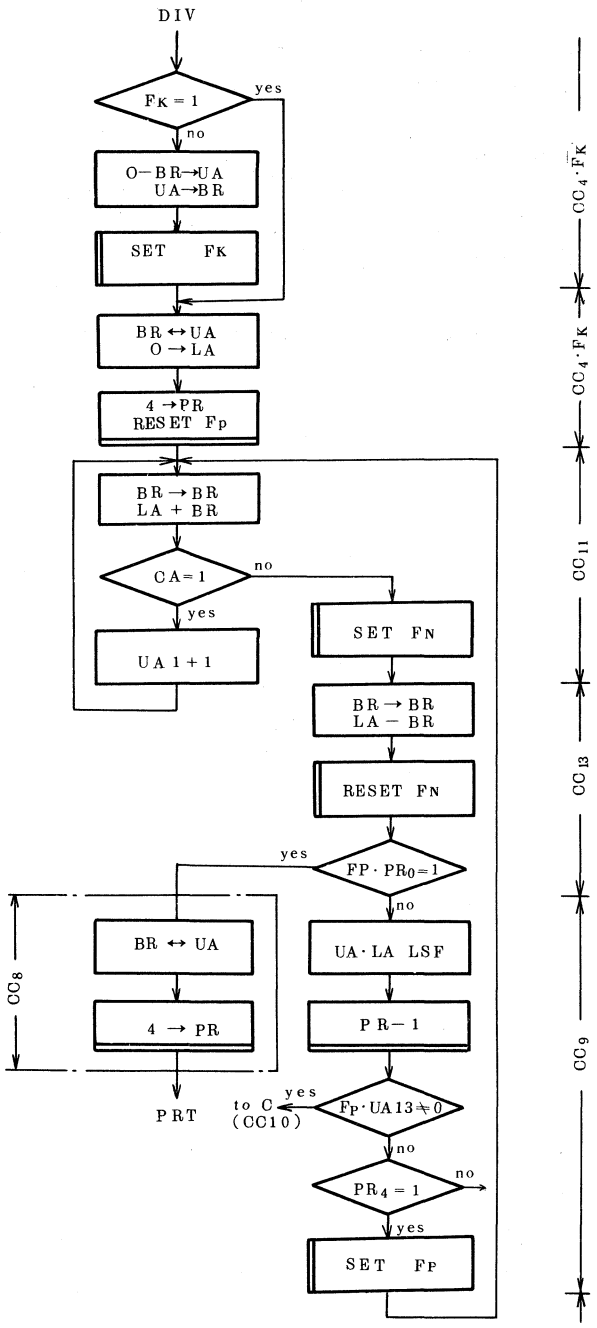


Fig. 4-9 Flow chart of division

(1) At $F_{MD} \cdot \overline{F_M} = 1$, division operation starts and the discrimination of F_K whether it is "1" or "0" is carried out at CC_4. In constant division, data processing differs according to the first and second division calculation.
In the first calculation operation can proceed without the interchange of the data, but to coordinate the operation with multiplication operation so as to reduce the LSI's inputs, then at $CC_4 \cdot \overline{F_K}$, 0−BR→UA, the transfer of UA→BR, setting of F_K & resetting of FP are done.
At $CC_4 \cdot F_K$, the interchange of BR↔UA, clearing of 0→LA & 4→PR operations are done and it proceeds to CC_{11}.
In the second or following calculation operations, since F_K is "1", only BR↔UA, 0→LA & 4→PR are done with the operation proceeding to CC_{11}.

(2) Dividend is stored in UA, and in order to perform a division operation of all digit, LA+BR (Actually LA−BR, because BR is a complement) is done at CC_{11} and if a CA is emitted, then UA_1+1 (UA·LSD+1) is done.
BR→BR, LA+BR & UA_1+1 are repeated until CA is not emitted, then F_N is set and operation proceeds to CC_{13}.
F_N setting is to memorize or store the fact that CA was not emitted in the LA+BR of SCT_0.

(3) At CC_{13}, LA−BR is done to correct over-addition of BR at CC_{11}.
BR→BR, LA−BR resetting of F_N which was set at CC_{11} are done with the discrimination of $F_P \cdot PR_0$ which in the jampping condition from the repetitive cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ takes place. That is, if $F_P \cdot PR_0$ is "1", it proceeds to CC_8 from CC_{13}; but if not, it proceeds to CC_9.

(4) At CC_9, the left shift of UA·LA with PR−1 being done until PR becomes PR_4 where F_P sets, and the $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ cycle is repeated until PR_0. If data is in UA13th digit position after FP is set at CC_9, it overflows and proceeds to the clearing cycle of CC_{10}.

(5) When $FP \cdot PR_0$ becomes "1" in the repetitive cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$, it then proceeds to $CC_{11} \rightarrow CC_{13} \rightarrow CC_8$ with the quotient in UA being interchanged with the divisor (constant) in BR, then PR_0 shifts until it becomes PR_4 which is the fixed decimal point 4. (BR↔UA, 4→PR).
After these procedures, operation proceeds to PRT cycle for print-out.

4.9 PRT (Printing of entry or calculated result)

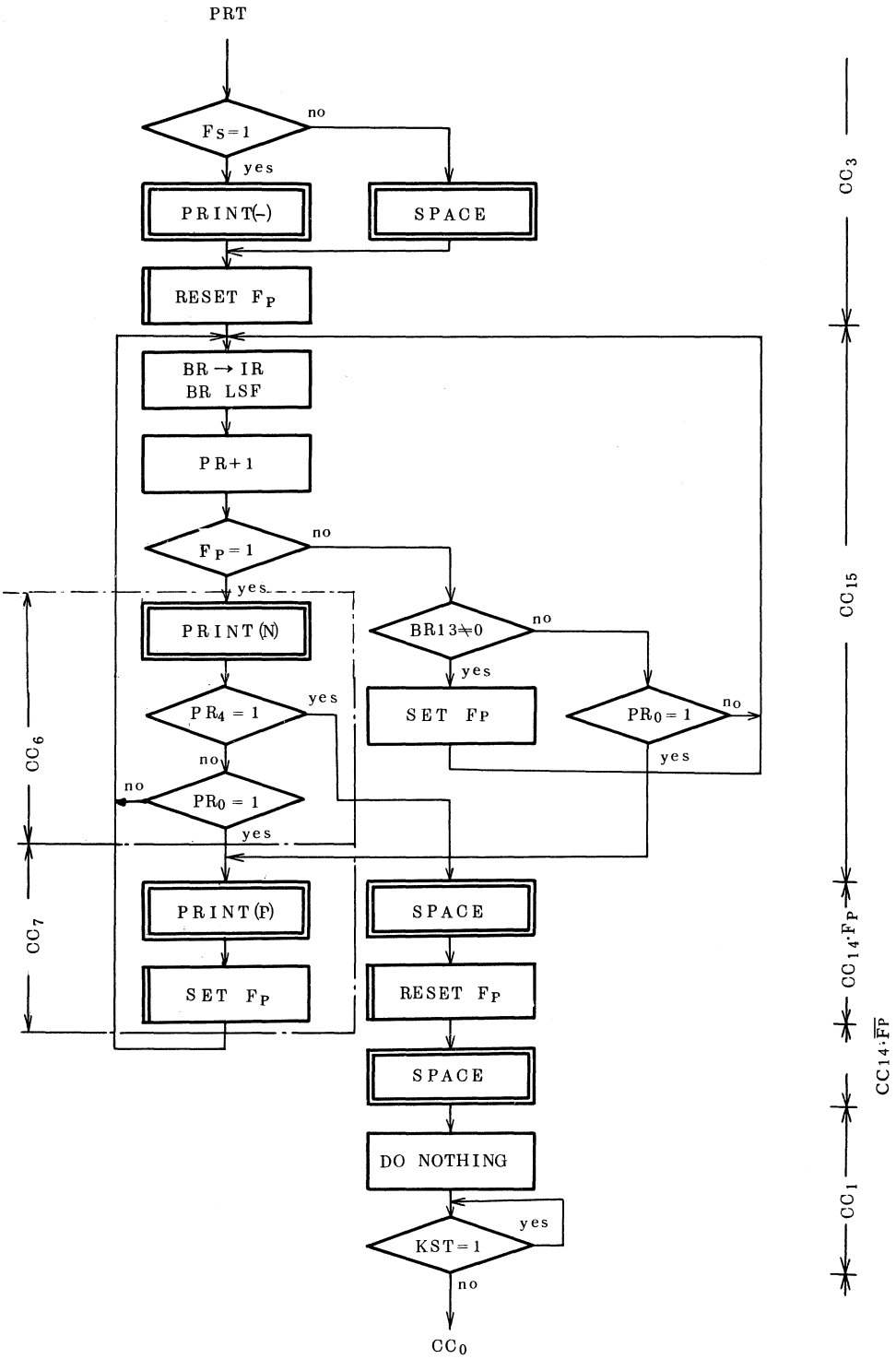


Fig. 4-10 Flow Chart of the Print-out

(1) After the calculated result is transferred to BR, it is ready for print-out by proceeding to PRT cycle.

(2) If F_S is set at CC_3, − sign is printed out. If $\overline{F_S}$ is "1", the paper is only fed without any printing, thus making a blank-space, and after F_P resetting at the end of the print-out cycle, it proceeds to CC_{15}.
Transferring of BR→BR and BR→IR are done at $CC_{15} \cdot SCT_0$ with the data of the 13th digit of BR entering IR.
At SCT_1, the left shift of BR with PR+1 for coordinating the printing position of the decimal point are done. At this time, F_P resets, so no print-out is done, thus BR_{13} is not printed out, and then discriminating $BR13 \neq 0$ is carried out. If $BR13 \neq 0$, F_P sets and returns to $CC_{15} \cdot SCT_0$.
When BR13=0, and if $PR_0=1$, then it proceed to CC_7 to print out the decimal point, and then F_P sets to print out the following successive data. IF $PR_0 \neq 1$, then the CC_{15} cycle is repeated.
Thus, BR→IR, BR left shift and PR+1 are repeated until $BR13 \neq 0$ (zero suppression).
Therefore, printing is done whether there are 0's or data after the decimal point.
If $BR13 \neq 0$ is obtained before becoming PR_0, then F_P sets with CC_{15} cycle being repeated, and proceeds to CC_6, where the PR_0 discrimination is repeated until PR becomes PR_4.
Then, if $PR_0=1$, it proceeds to CC_7 where the decimal point is printed out and returns to CC_{15} where the numeric is printed out.
If it becomes PR_0 in the procedure, it proceeds to CC_7 where · (point) is printed-out.

(3) In the PR+1 operation in CC_{15}, when PR becomes PR_4 after the print-out cycle, it then enters $CC_{14} \cdot F_P$ cycle where a blank space is left with F_P again resetting and proceeds to $CC_{14} \cdot \overline{F_P}$ where another blank space is left. Therefore, at the end of printing the calculated result has two blank spaces to separate two different calculations.

(4) At CC_1, the discrimination whether the key is kept pressed or not is performed, and if the key is released, it proceeds to CC_0.

OPERATION PROCEDURES

CONTENTS

5. Operation Procedures

5.1 LSI's

The circuit elements in Pocketronic are mainly the three LSI's which are control Chip (C·C), Data chip (D·C) & Timing Chip (T·C) and another important element called the Thermal Head (T·H).

The operations are carried out by controlling these chips. To perform the calculation and print-out operations. There are 65 different order (Product Term) and control signals which are formed by the combination of the conditions of the different flip-flops in the control chip with the signals of the timing chip or the data chip.

5.1-1 Control Chip

The external inputs to the control chip are $I_1 \sim I_3$, I_N, KEY(C+CI), $\overline{MSD}$=0, PR_4, PR_0, SCT_1, $\overline{CA}$ & KST, while the internal inputs are F_{MD}, F_M, F_K, F_N, F_S, F_P & $F_{C1} \sim F_{C4}$, and according to the different combination of these external & internal signals, 65 control signals are generated by this control chip.

$CT \sim CT_4$ signals control the timing chip and $CR_1 \sim CR_5$ signals control the data chip.

The ten internal flip-flops are J–K type master-slave flip-flops which operate by the control signal of SP–CC which comes from the timing chip.

I_N is the discrimination flip-flop of whether a numeral key or an order key is pressed, and when I_N is "1", it signifies that it is a numeral key; but if I_N is "0", it is an order key.

Because the encoded signal of the numeral keys and the order keys are the same, so it is necessary to distinguish the difference by discriminating I_N signal.

The outline of the operations in this chip is as follows; For example, when the numeral key is pressed, I_N signal enters the control chip.

In the product circuit of the chip, $\overline{FC_1}$, $\overline{FC_2}$, $\overline{FC_3}$ & $\overline{FC_4}$ and I_N from NAND gate.

$FC_1 \sim FC_4$ are constructed in this chip, so they reset in this time.

Since the output signal of NAND is connected with the set side of FC_1 & FC_3, then when SP–CC signal appears, FC_1 & FC_3 set and it proceeds to CC_5.

In this operation procedure, the combination of the conditions of flip-flops and the external signals are specified and the matrix circuit in the chip are set; therefore, if one of the combinations fulfills a certain condition, the output signal of the product matrix circuit goes to the Sum of Product circuit with certain flip-flops operating and certain external signals being emitted from this chip to control the other chips.

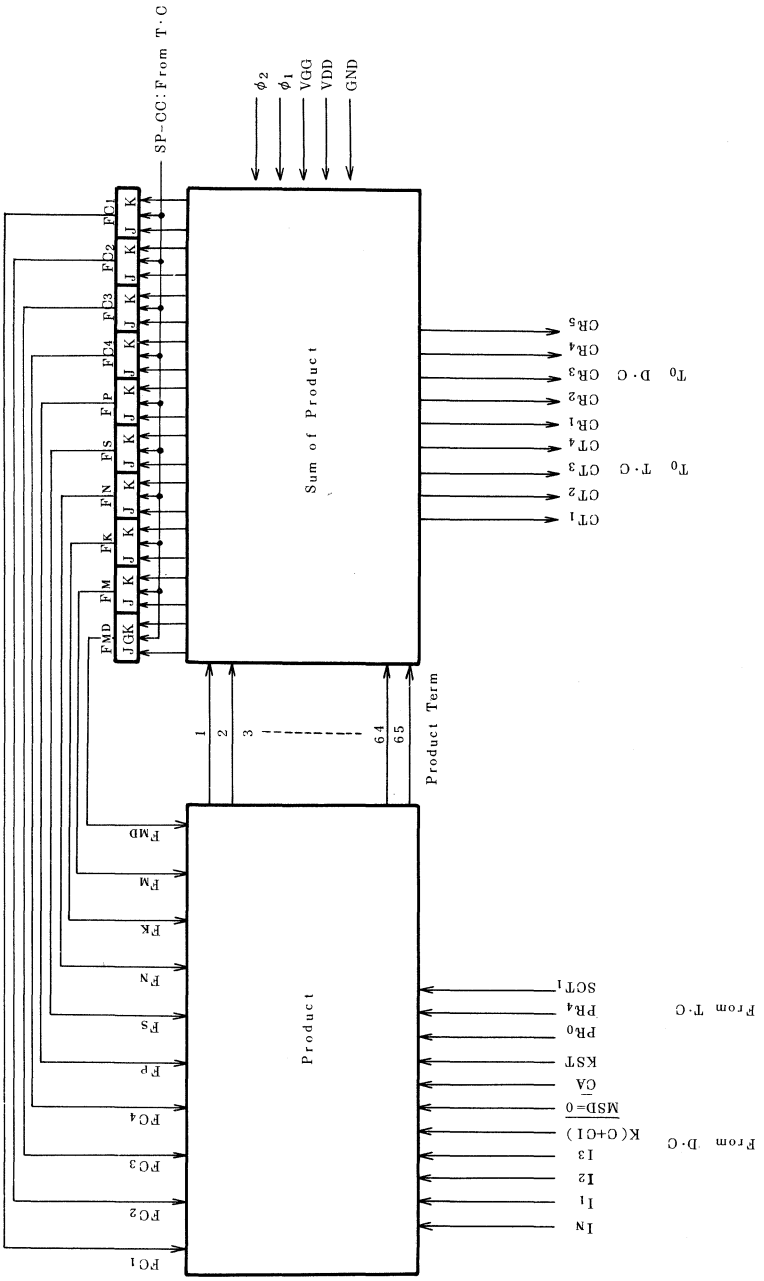


Fig. 5-1 Control Chip

5.1-2 Timing Chip

The timing chip generates the shift pulses of SP–PC, SP–Tx, SP–PR & SP–CC and PRINT signals by the timing matrix. The input signals to generate these signals in the matrix are $CT_1 \sim CT_4$ which are emitted from the control chip, and $\overline{P_9}$, P_0, $\overline{Tx_4}$, $\overline{Tx_0}$, SCT_1, TD_{12}, TB_3 & PR_4 which are the internal input signals.

Sector (SCT_0 & SCT_1), digit counter (DC . . . $TD_0 \sim TD_{12}$), and bit counter (BC . . . $TB_0 \sim TB_3$) are dynamic timing pulse generators; but step-down counter (Tx . . . $Tx_0 \sim Tx_4$), print counter (PC . . . $P_0 \sim P_9$) and point register (PR . . . $PR_0 \sim PR_{12}$) are static shift registers.

The clock pulse of ϕ_2 and ϕ_3 are always applied to these counters or registers; but ϕ_1 is applied at only certain timing to count or shift a certain number of times or bits.

That is, when SP–Tx, SP–PC or SP–PR signal appears, then the NAND output of ϕ_1 and this signal operates certain counter or register.

SCT counter (SCT_0 & SCT_1), digit counter ($TD_0 \sim TD_{12}$) & bit counter ($TB_0 \sim TB_3$) are always operating to generate the timing pulse.

The output of NAND gate of SP–Tx and ϕ_1 controls Tx counter which normally stops at Tx_0, and starts to count whenever a shift pulse is applied to it with Tx_0 becoming Tx_1, Tx_2, Tx_3 & Tx_4. SP–PC controls the print counter (PC) which always stops at P_0 and it starts to count whenever a shift pulse is applied to it with PC becoming P_0 . . . P_9 (10-bit) step by step.

The $P_1 \sim P_5$ output signals of PC and $I_1 \sim I_4$ signals from data chip with the PRINT signal are generated in the timing matrix, transfer to the character generator where the $TH_1 \sim TH_4$ signal is formed according to the specified character pattern, and then are transmitted to the thermal head (TH).

During the time of $P_6 \sim P_9$, MAG signal energizes the solenoid which activates the plunger that feeds the paper.

SP–PR operates the point register PR. Normally, PR is set at 4 (PR_4) and if a shift pulse is applied, then it changed from PR_4 to PR_3, PR_2 . . . PR_5 (13-bit shift register).

Therefore, PR–1 is carried out when only one shift pulse is applied, while PR+1 is carried out by applying the shift pulse 12 times.

SP–CC is transferred to the control chip to control 10 flip-flops.

Normally, SP–CC is emitted at the time of $SCT_1 \cdot TD_{12} \cdot TB_3$, but if a print-out operation is completed, it is emitted at the time of $P_9 \cdot Tx_4 \cdot SCT_1 \cdot TD_{12} \cdot TB_3$.

Also in division, if no carry appears in the LA+BR operation at $CC_{11} \cdot SCT_0$, then SP–CC is emitted at the time of $SCT_0 \cdot TD_{12} \cdot TB_3$.

5.1-3 Data Chip

Numeral and order key signals from the keyboard are combinationally grouped are distinguished by discriminating IN signal.

The key matrix encodes the numeral and the order key signals into 8-4-2-1 code, then $I_1 \sim I_4$ & IN are directly set according to the encoded signal when SET–IR signal is emitted from the data matrix circuit.

In the data matrix, many different signals are generated such as SP–BR, SP–IR, SP–ACC, BR–IN, IR–IN, X, Y, SET–IR, SET–IN, $(\overline{-})$, $\overline{P}$, $\overline{C}$, & INH by combining $CR_1 \sim CR_5$ which come from the control chip with SCT_1, TD_{12}, TB_3, TB_0, P_0 & PR_1 which come from the timing chip, and BR out, ACC out & I_1 which are the internal input signals.

IR which is a 5-bit shift register stores the Numeral, Sign & Symbol data to be registered at certain time and it emits $I_1 \sim I_3$ & IN to the control chip and $I_1 \sim I_4$ & IN signal to the timing chip.

On the other hand, IR·BR data enters the data chip from IR or IN and it is shifted by the clock pulse which is the NAND output signal of SP–IR & $\overline{\phi_1}$.

BR which is a 52-bit shift register (13 digits) operates by SP–BR.

The data of BR, IR or ACC enters BR from BR–IN at a certain timing. ACC consists of UA (52 bits) and LA (52 bits) and has 104 bits (26 digits), and its data is shifted by SP–ACC clock pulse. The upper most 3 bits of UA are used for the correction of the adder. ADD is a full adder/subtractor (8-4-2-1 code) which operates by X & Y, input signals and is connected to ACC.

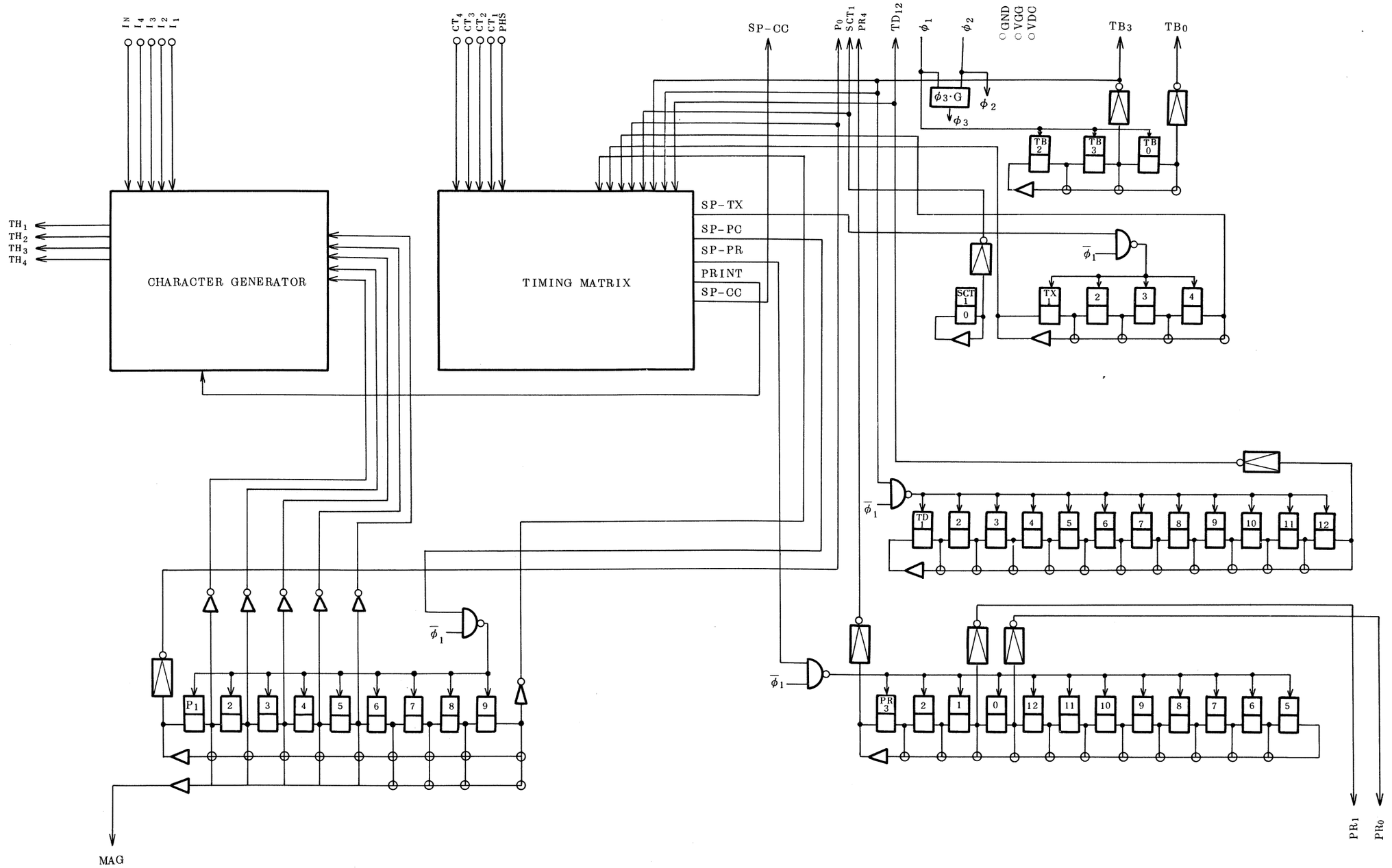


Fig. 5-2 Timing Chip

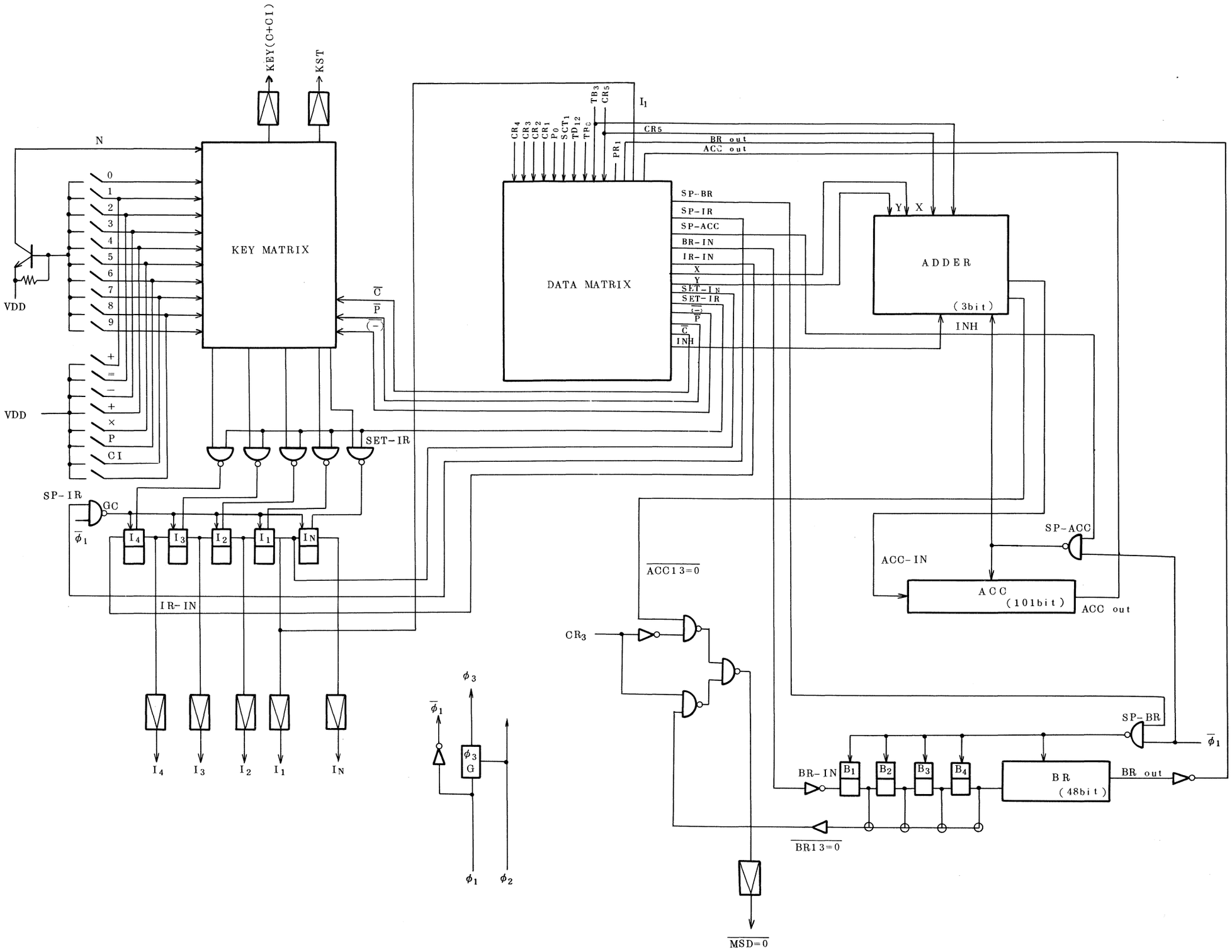


Fig. 5-3 Data Chip

5.2 Registration Circuit

5.2-1 Key Circuit & IR·IN

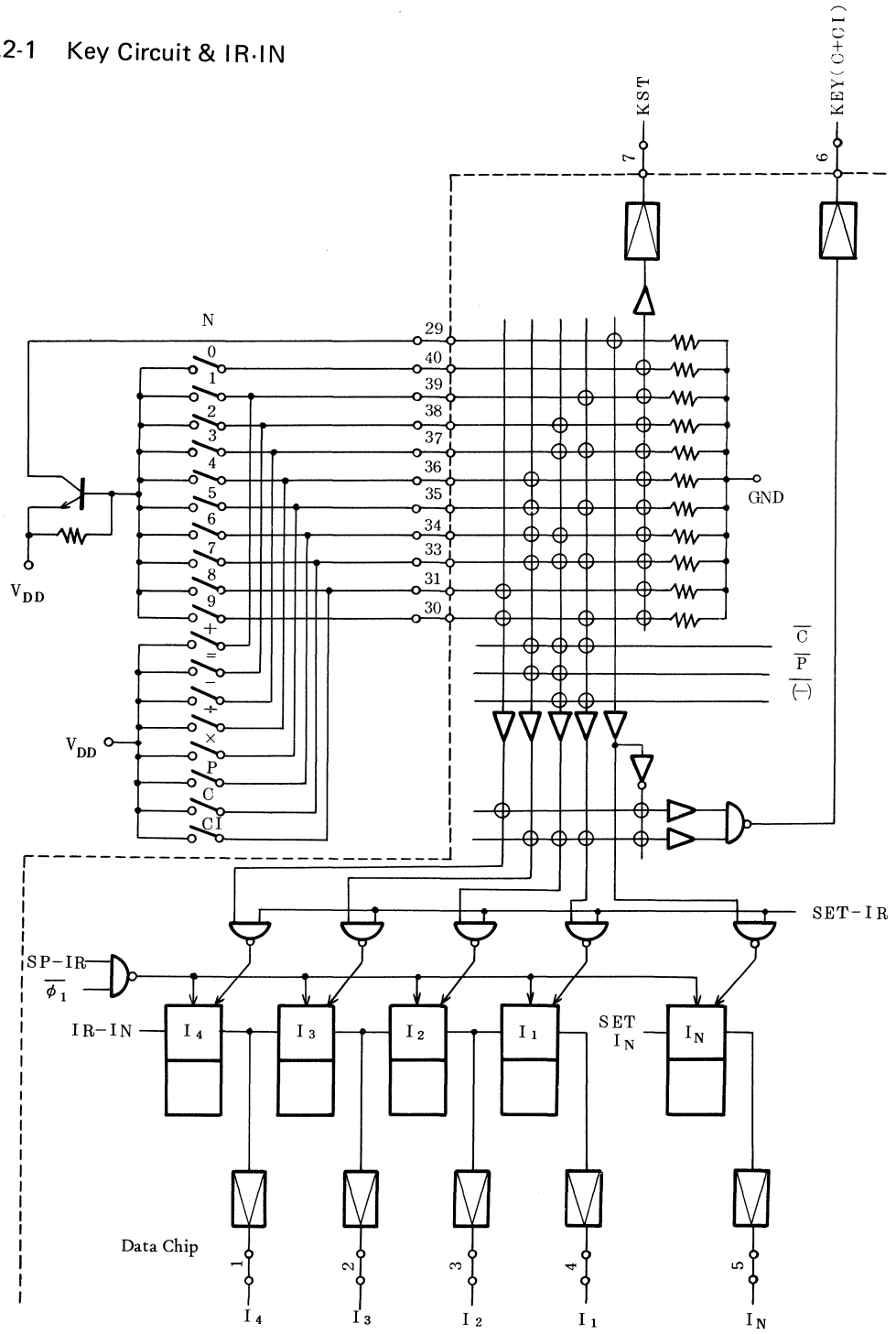


Fig. 5-4 Key Encoder

In order to minimize the wirings from the keyboard as well as the inputs to LSI's, numeral and order keys are combined in groups of 1 & +, 2 & ÷, 3 & −, 4 & ÷, 5 & ×, 6 & P, 7 & C and 8 & CI, each combination of numeral and order keys is discriminated according to IN state whether it is "1" or "0".

I1 ~ I4 correspond to the 8-4-2-1 code, and the actual encoded outputs become as follows;

ENCODER

$I_N = 1$

	I_1		
I_2	3	7	6	2
I_4	9			8
	1	5	4	0
		I_3		

$I_N = 0$

	I_1		
I_2	−	C	P	=
I_4				E
	+	×	÷	
		I_3		

5.2-2 Registration of First Integral Digit

When a numeral key is pressed, data enters the key matrix of the data chip from which its output is obtained.

KST is sent to the control chip, the print command is emitted to both data and timing chips according to the pressed key.

1) The timing chip controls the print command according to the conditions of CT1 ~ CT4 sent from the control chip, and also SP–TX, SP–PC, PRINT, SP–CC signals are emitted.

   When SP–TX is emitted, TX counter counts TX0, TX1 . . . & TX4, and when becoming TX4, SP–PC is emitted with the print counter P0, P1 . . . & P9 counting.

   Therefore, IR is cleared so that it can receive the contents of the next pressed key for print out.

   When the print counter in the timing chip reaches P1, SET–IR is emitted, and I1 ~ I4·IN are directly set according to the key matrix outputs.

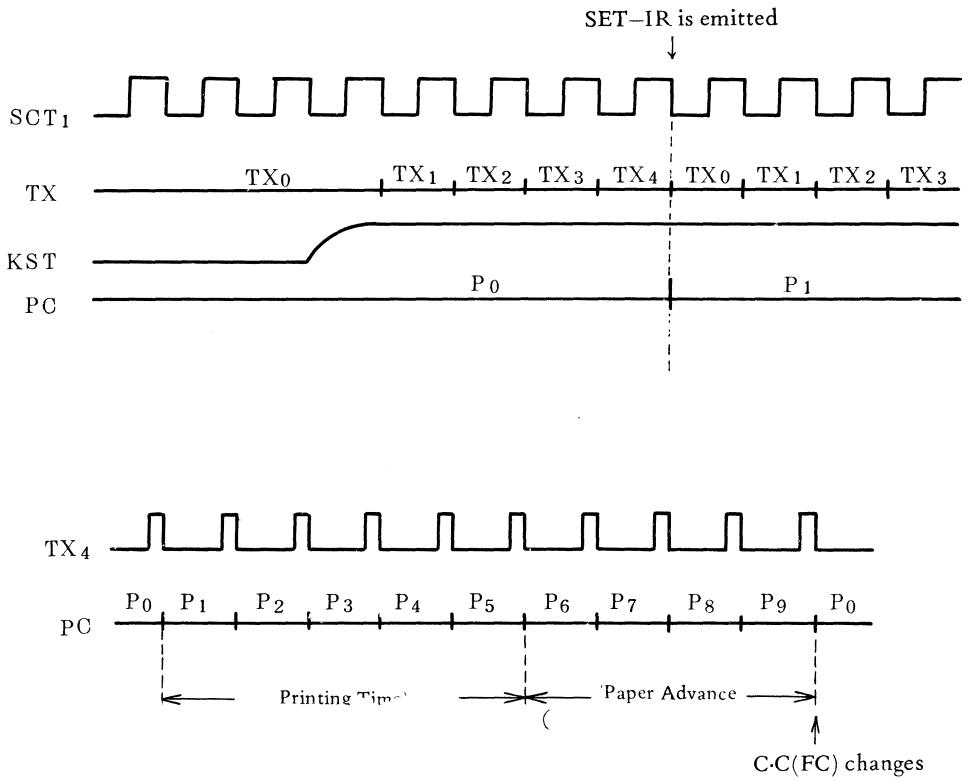


Fig. 5-5 Key Siganl Timing

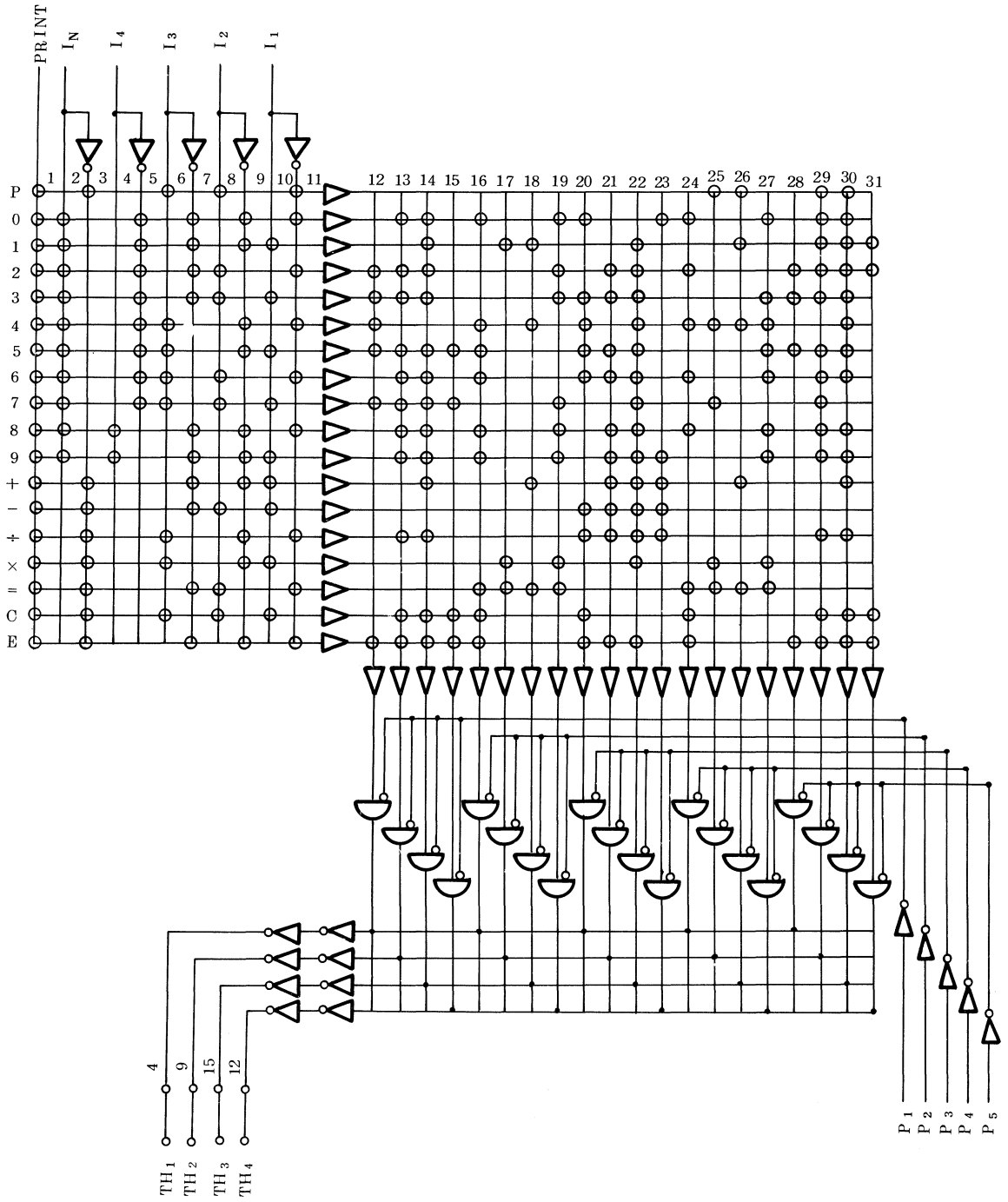


Fig. 5-6 Character Generator (Print Matrix)

The character generator in the data chip forms the print-out patterns $TH_1 \sim TH_4$ according to the inputs of $I_1 \sim I_4$ according to the inputs of $I_1 \sim I_4$ & I_N. When the PRINT signal is emitted, the $TH_1 \sim TH_4$ output signals are fed to the thermal head with the character being printed out during $P1 \sim P_5$ time.

For example, when 0 is printed, $I_1 \sim I_4$ are "0" while I_N is "1", so the following outputs are obtained.

P_1 time			TH_2	TH_3	
P_2 time		TH_1			TH_4
P_3 time		TH_1			TH_4
P_4 time		TH_1			TH_4
P_5 time			TH_2	TH_3	

Fig. 5-7 Pattern of 0

At $P_6 \sim P_9$, MAG signal is emitted which energizes the solenoid that starts the feeding of the paper. At the end of P_9 which is the end of a character printing cycle, if SP–CC from the timing chip is emitted to the control chip at $P_9 \cdot SCT_1 \cdot TD_{12} \cdot TB_3$, then FC_1 & FC_3 sets with it proceeding to $CC_5 \cdot \overline{F_N}$ cycle.

2) The clearing of 0 → BR command is supplied to the data chip and 4 → PR which is the fixed decimal point shift command to the timing chip respectively from the control chip.

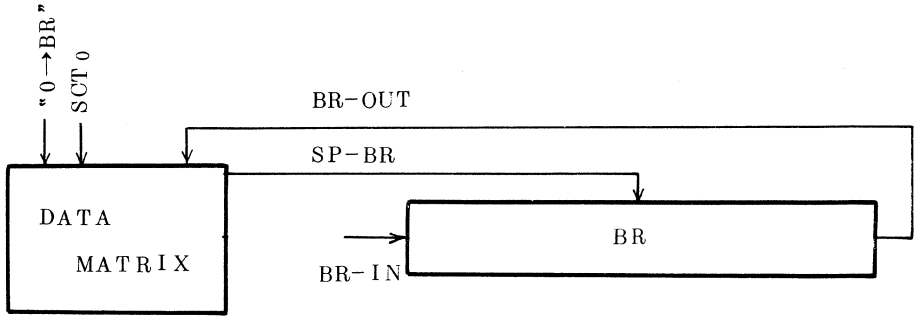


Fig. 5-8 Block Diagram of 0 → BR & 4 → PR

SP–BR is emitted from the data chip at SCT0; but, since BR–IN is closed, no data enters BR when the data in BR is successively shifting; thus BR is cleared (0 → BR).

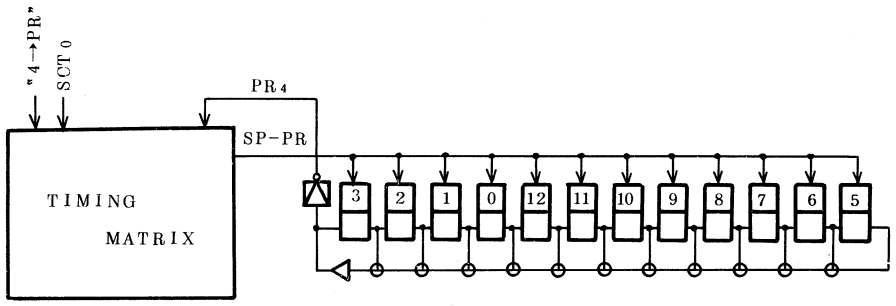


Fig. 5-9 PR (Decimal Point Register)

SP–PR is emitted from the timing chip at SCT·$\overline{PR4}$, and when it becomes PR4, the shifting stops (4 → PR).

SP–CC is emitted at the end of SCT1, and enters the control chip with FN setting.

3) In the first registration since FP is still "0" at CC5·FN, then the following operations PR → PR, BR → BR & IR·PR1 → BR are carried out.

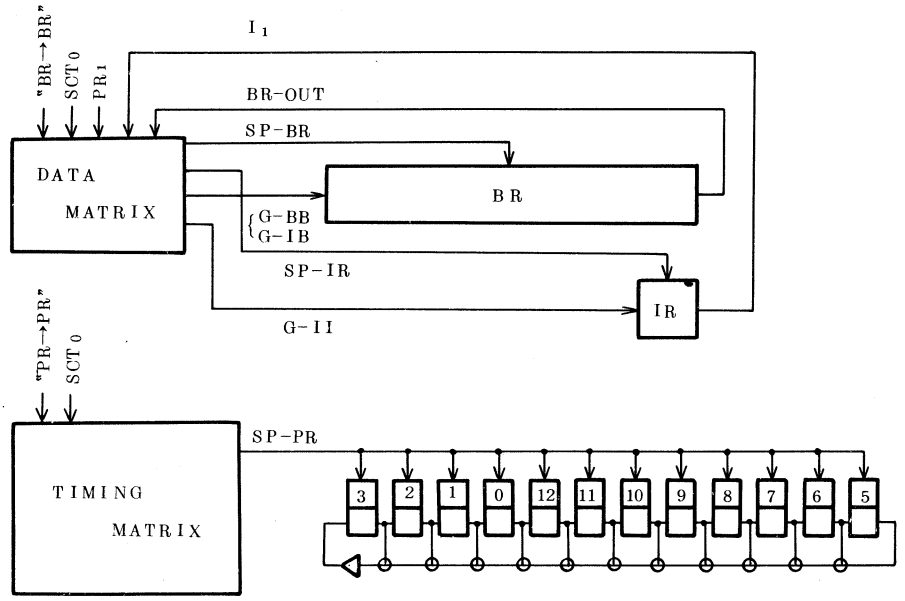


Fig. 5-10 BR & PR Block Diagram

When SP–PR is emitted from the timing chip at SCT0, the shifting continues, and since SP–PR is emitted 13 times in SCT0, it returns to its original PR state at the same time of SCT0, the data chip emits SP–BR & SP–IR which open G–BB & G–IB at PR1; therefore, IR data enters BR when PR of the timing chip becomes PR1.

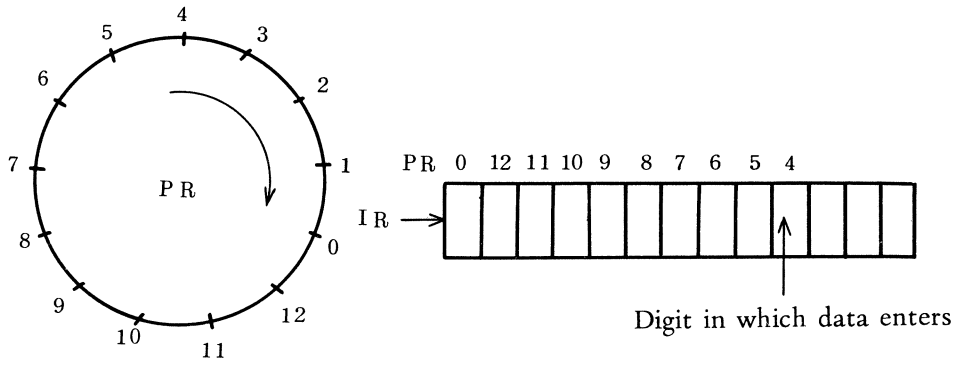


Fig. 5-11 PR Operation

PR becomes PR4 at $\overline{FN}$ time and then shifts in the descending order of PR3, PR2 . . . PR5 until it stops at PR4 which indicates the IR data entered the fourth digit of BR.

Since G–BB is open at SCT1, and when SP–BR is emitted at SCT1·$\overline{TD12}$ a left shift is done after the 1 digit shifts (left shift). At the end of SCT1, SP–CC is emitted to the control chip, where FC3 is reset and proceeds to CC1. If FS is "1" at the second or any subsequent registration, it is reset.

4) At CC1, nothing occurs except the KST discrimination. If KST is "1", it remains at CC1 and returns to CC0 after KST becomes "0". In other words, if the entry key is kept pressed, at CC1, it remains at CC1; but if the key is released, it returns to CC0.

Since Pocketronic does not have the former OS → FT → FU key start circuit, CC1 cycle is utilized in the discriminating of KST.

5.2-3 Registration of Decimal Point

1) When [·] key is pressed, BR13≠0 is discriminated, and if BR13=0, the point (.) is printed out. Paper is fed during the time of $P_6 \sim P_9$ with FP·PC1 setting at the end of P_9, and then proceeds to CC_1.

2) KST is discriminated at CC_1, and if KST is "0", it returns to CC_0.

5.2-4 Registration after [·] key

1) When the first entry of a numeric is the decimal point and then, a numeral is entered, the print-out & the discrimination of FN is carried out at CC_0 and then the operations of 0 → BR, 4 → PR & the setting of FN is done at the time of $CC_5 \cdot \overline{FN}$ and proceeds to $CC_5 \cdot FN$. But if the [·] key is pressed after entering a numeral or numerals, then when a numeral key is pressed, it goes directly to $CC_5 \cdot FN$ after the print-out.

   At $CC_5 \cdot FN$, the transferring of PR→ PR, BR → BR and IR·PR1 → BR are done; and since FP is set, PR−1 is carried out but the left shift of BR is not done.

   The following fractional registrations are done in the same procedure of PR → PR, BR → BR, IR·PR1 → PR with PR−1 and the IR data entering the digit below the preceding fraction.

   When PR_0=1, the PR−1 operation is not carried out. Then, if IR·PR → BR is done, the registered data enters the 13th digit position of BR (BR·MSD); thus all registration stops which is the detection of an underflow (overflow).

5.3 ⊠ or ÷

1) When ⊠ or ÷ key is pressed, symbol x or ÷ is printed with FC_3 setting at the end of P_9, and then proceeds to CC_4.

2) At CC_4, the transfer of BR→UA is done for the square calculation.

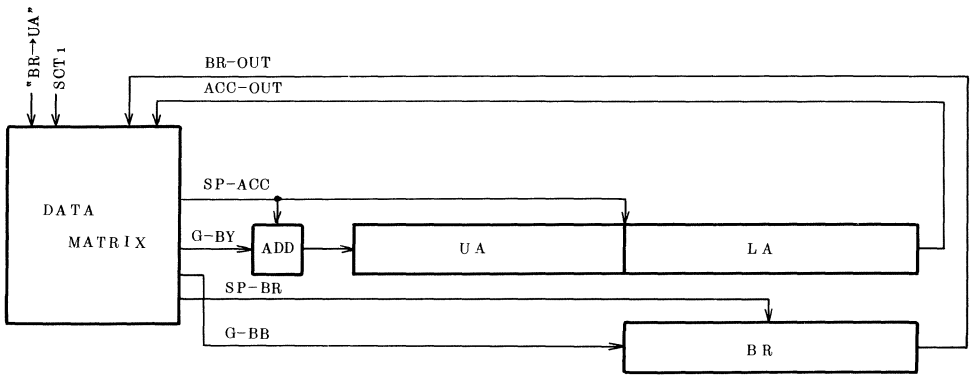


Fig. 5-12 BR → UA at CC_4

When SP–ACC is emitted at SCT_0, LA clears with UA data transferring to LA. SP–ACC & SP–BR are emitted at SCT_1 to open G–BY & G–BB with BR data circulating in BR and also entering UA through ADD; thus, BR→BR & BR→UA are done. Then, F_N is discriminated, and if F_N=1, then F_S resets when SP–CC is emitted at the end of SCT_1.

If F_N is "0" and when ⊠ or ÷ is pressed, the result of the previous calculation becomes the multiplicand or dividend of the following entered data making it a continuous calculation; but if F_N is "1", it is a new individual calculation.

In multiplication, F_{MD}, F_M & F_K are set and F_P & F_N are reset at the end of SCT_1; but, in division, F_{MD} is set and F_P, F_N, F_M & F_K are reset. Below are the discrimination combinations for the different calculation operations.

F_{MD}	F_M	
0	0	..... Addition & subtraction
1	0	..... Division
1	1	..... Multiplication

In the control chip, when $FC_2 \cdot FC_3$ & FC_4 are set, it proceeds to $CC_{14} \cdot \overline{FP}$.

3) At $CC_{14} \cdot \overline{FP}$, SP–Tx & SP–PC are emitted to operate the print counter (PC); but when no PRINT signal is emitted, the feeding of the paper only is done which is during the $P_6 \sim P_9$ time of no printing.

FC_1 sets and FC_2, FC_3 & FC_4 reset at the end of P_0 and then, it proceeds to CC_1 and becomes CC_0 if KST=0.

5.4 + or – (addition or subtraction)

1) When these keys are pressed, first, the 13th digit of BR is discriminated, and if BR13=0, the + or – symbol is printed out. FC_3 sets at the end of P_9 and it proceeds to CC_4 where F_S is discriminated and performs either addition or subtraction according to the combination with the pressed ⊕ or ⊖ key.

F_S	Key	Operation
"0"	+	Addition
	–	Subtraction
"1"	+	Subtraction
	–	Addition

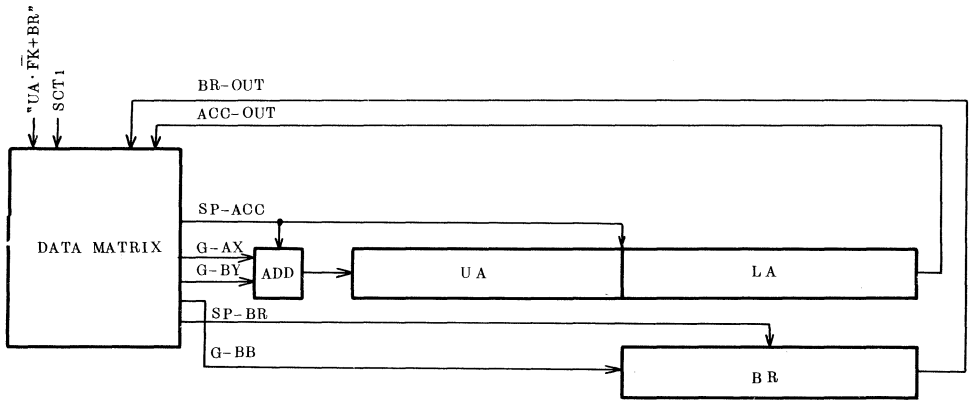


Fig. 5-13 Block Diagram of Addition & Subtraction

At SCT_0, SP–ACC is emitted to clear LA with UA data transferring to LA, and at SCT_1, SP–ACC & SP–BR & SP–BR are emitted to open G–BB, G–BY & G–AX. Therefore, the addition of BR+UA and the circulation of BR→ BR are done, but, if F_K=1, G–AX is closed; so the transfer of BR→UA is done instead of the addition of BR+UA.

If CA is emitted during this addition or subtraction, that is, +A <—B or —A <+B in the ±A±B operation, then F_N, F_P, F_M, F_{MD} & F_K resets, and proceeds to CC_{12}, where the clearing of 0 → UA is done for the conversion of the complement to its true value. At this time, F_S is also converted, that is if F_S is "1", it is converted to "0" or vice versa, and then, it enters $CC_{14}\cdot\overline{F_P}$ cycle. If CA is not emitted, F_N, F_P, F_M, F_{MD} & F_K are reset. In the discrimination of UA13≠0, if UA13=0, it proceeds to $CC_{14}\cdot\overline{F_P}$; but if UA13≠0, it returns to CC_{10} due to an overflow, and proceeds as though the [C] key is pressed.

2) At $CC_{14}\cdot\overline{F_P}$, the feeding of the paper is done enter multiplication or division operation and returns to CC_0 if KST=0 at CC_1.

5.5 [=] (equal or total) key

1) When [=] key is pressed, BR≠13 is discriminated, and if it is 0, the = symbol is printed out. After printing, F_{MD} is discriminated, if F_{MD} is "0", then F_N & FC_4 are set and proceed to CC_8 where the transfer of UA → BR is done to printout the result of addition or subtraction.

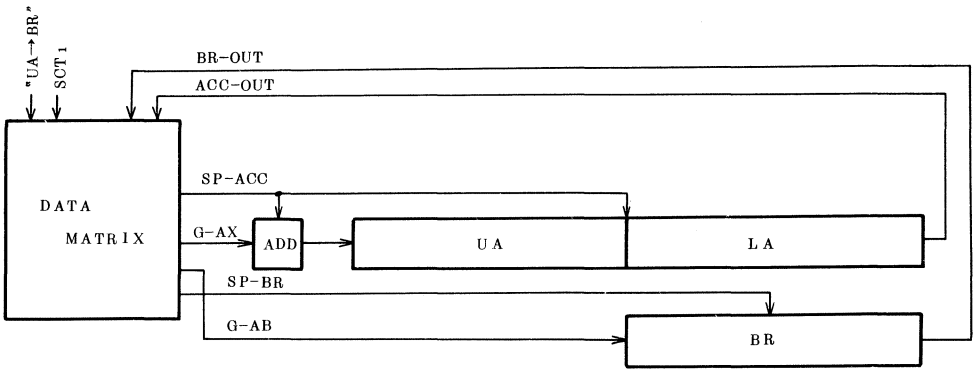


Fig. 5-14 Block Diagram of UA—BR

At SCT_0, SP—ACC is emitted to clear LA, with UA transferring to LA. At SCT_1, SP—ACC & SP—BR are emitted to open G—AB & G—AX. Therefore, UA → UA & UA → BR are done. Since the decimal point is fixed PR_4 in the timing chip, then 4 → PR is performed. When SP—CC is emitted at the end of SCT1, operation enters to PRT cycle.

On the other hand, when F_{MD} is "1", F_M discrimination of whether it is multiplication or division is done, and if F_M is "1", it proceeds to MLT cycle, but if F_M =0, it goes to DIV cycle.

5.6 MLT (multiplication)

1) When [=] key is pressed in multiplication, $F_{MD} \cdot F_M$ becomes "1" with the operation entering $CC_4 \cdot F_K$ where the interchange of BR↔UA and the clearing of 0 → LA are done so that the multiplicand remains as the constant. At SCT_0, SP–ACC is emitted to perform the clearing of 0 → LA, and at SCT_1, SP–ACC & SP–BR are emitted to open G–AB & G–BY to perform the interchange of UA↔ LA. Since the decimal point is fixed in Pocketronic, 4 → PR operation is performed with PR+1 being done.

That is, PR shifts at SCT_0 until it becomes PR_4, and then it shifts in SCT_1 during the time of $\overline{TD_{12}}$, thus PR+1 is performed. At the end of SCT_1, F_P resets, and it enters CC_{11} cycle.

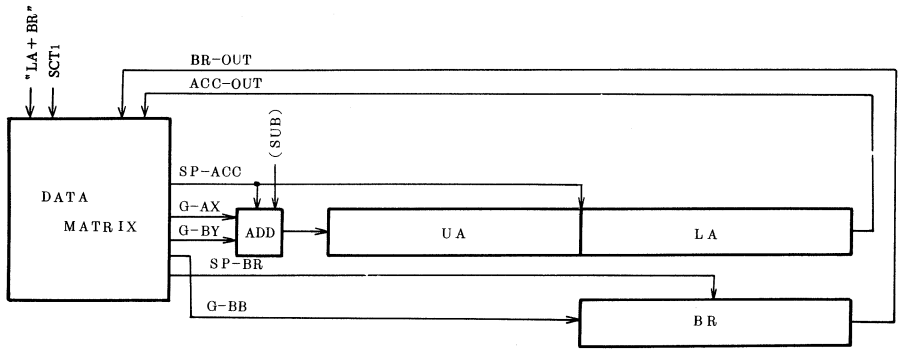


Fig. 5-15 Block Diagram of LA+BR

2) At $CC_{11} \cdot SCT_0$, LA+BR is carried out and UA13+9 (MSD–1) is performed at SCT_1.

LA+BR is performed when SP–ACC & SP–BR appear at SCT_0 with G–AX & G–BY opening.

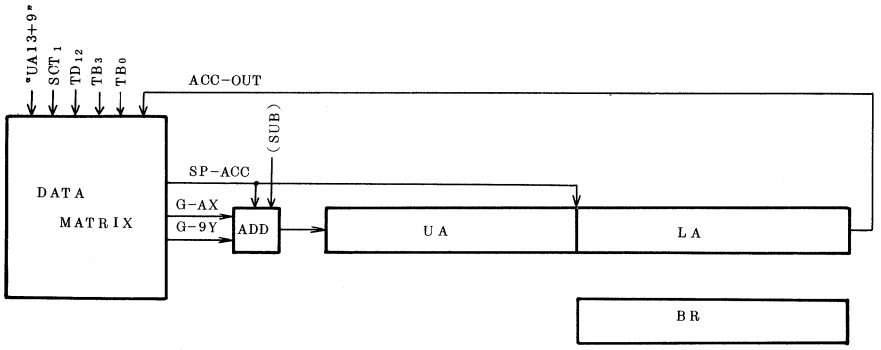


Fig. 5-16 Block Diagram of UA13+9

In UA13+9 operation at CC_{11} cycle, SP–ACC is emitted at SCT_1 to open both G–AX and G–9Y which only opens at TD_{12}; so if a CA is emitted (UA13≠0), during UA13+9 operation, then it is repeated until a CA is not emitted: Thus, it proceeds to CC_{13} from CC_{11}. In the addition of LA+BR operation in the CC_{11}, the partial product of that digit is obtained.

3) At CC_{13}, the subtraction of LA–BR is done to correct the one time over-addition of LA+BR at CC_{11}, and also, 9 is subtracted from UA13, thus UA13 become 0 with the correct partial product.

F_M resets at the end of SCT_0, but this function has no connection with multiplication except to minimize the control circuit for division. At the end of CC_{13}, the discrimination of $F_P \cdot PR_0$ which is the releasing condition from the repetitive $\overbrace{CC_{11} \rightarrow CC_{13} \rightarrow CC_9}$ cycle is carried out, and if $F_P \cdot PR_0$ is "1", it proceeds to CC_8 from CC_{13} where the result enters the cycle for print-out; but if $F_P \cdot PR_0$ is "0", it proceeds to CC_9 from CC_{13} with the left shift of UA & LA and PR+1 operations being done.

4) In CC_9, the left shift of LA & UA is done by the opening of G–AX at $SCT_0 \cdot \overline{TD_{12}}$ and at SCT_1 when SP–ACC is emitted. PR+1 is performed by 12 times left shifting when SP–PR is emitted at $SCT_0 \cdot \overline{TD_{12}}$, and if UA13≠0 after F_P sets, then it proceeds to CC_{10} because there was an overflow in the calculation result. PR_4 is also discriminated, and if PR_4 is "1", then F_P sets and returns to CC_{11}; but if PR_4 is "0", it directly returns to CC_{11}.

5) PR operation in multiplication is shown in Fig. 5-16. In the LA+BR & UA13+9 operations of CC_{11}, when CA is not emitted, it proceeds to CC_{13} to perform the correction operation of LA–BR & UA13–9, and then proceeds to CC_0 where the left shift of UA & LA and PR+1 are done.

This repetitive $\overbrace{CC_{11} \rightarrow CC_{13} \rightarrow CC_9}$ cycle is repeated until PR becomes PR_4 with F_P setting, and again the same repetitive operation is carried out until PR become PR_0.

However, if UA13=0 before F_P sets in the $\overbrace{CC_{11} \rightarrow CC_{13} \rightarrow CC_9}$ cycle, then there is an overflow in the calculation.

6) When it enters the CC_8 leaving the repetitive $\overbrace{CC_{11} \rightarrow CC_{13} \rightarrow CC_9}$ cycle, the interchange of BR → UA is done to print-out the result with PR leaving PR_0 to become PR_4 (4 → PR), and then, it enters PRT (print) cycle.

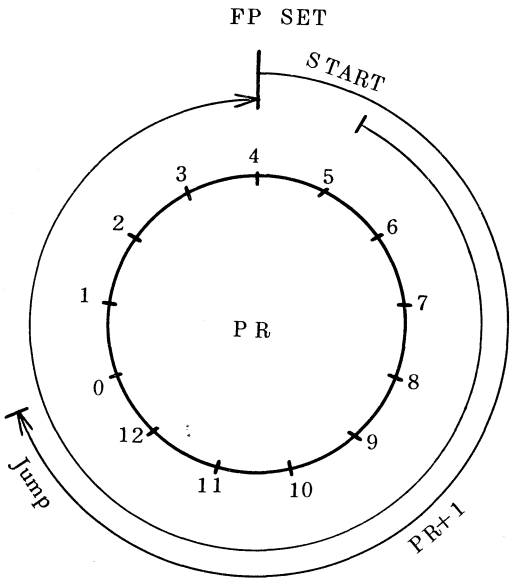


Fig. 5-17 PR Operation of Multiplication

5.7 DIV (division)

1) When ÷ key is pressed, F_{MD} becomes "1" with F_M being "0", and then, it proceeds to CC_4. Since Pocketronic always performs constant division, the first calculation procedure differs from the second or any subsequent calculations, because at the begining of the first division calculation; F_K is "0", so the 0–BR → UA, UA → BR, F_K setting & F_P resetting are done at $CC_4 \cdot \overline{F_K}$ cycle and then it proceeds to $CC_4 \cdot F_K$.

   In the complement transfer of 0–BR → UA operation, SP–ACC is emitted at SCT_0 with the transferring of UA to LA and clearing UA. Since SP–ACC & SP–BR are emitted at SCT_1, then G–AB & G–BY open with the SUB signal (subtraction command) which was emitted at $CC_4 \cdot F_K$; thus the 0–BR → UA & UA–BR operations are done.

2) When F_K is set, it enters $CC_4 \cdot F_K$ cycle to perform the BR ↔ UA, 0 → LA & 4 → PR operations and proceeds to CC_{11}.

3) At CC_{11}, the addition of LA+BR is done; but since BR is a complement at this time, then actually LA–BR is done.

   When a CA is emitted, it signifies that a subtraction was possible; therefore, UA1+1 (formerly LSD+1) is done with a repetition of the CC_{11} cycle.

The addition of LA+BR is done at SCT_0 and if there is no CA at the end of $TD_{12} \cdot TB_3$, then SP–CC is emitted which sets F_N and proceeds to CC_{13}.

Since CA signal has only the time of one bit; therefore F_N is utilized to store the information that no CA was emitted at $SCT_0 \cdot TD_{12} \cdot TB_3$ for the duration of SCT_1 and in the discrimination of F_N at SCT_1, if F_N is "1", it proceeds to CC_{13}; otherwise if F_N is "0" it repeates the CC_{11} cycle.

4) At CC_{13}, the subtraction of LA–BR is carried out to correct the one time over-addition of LA+BR at CC_{11} when a CA did not appear, and also F_N is reset. In this cycle, the discrimination of $F_P \cdot PR_0$ is carried out and if $F_P \cdot PR_0$ is "1", it proceeds to CC_8 where the result is prepared to enter the print out cycle; but if $F_P \cdot PR_0$ is "0", it proceeds to CC_9 and continues the repetitive cycle of $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$.

5) At CC_9, the left shift of UA & LA and PR–1 are done, where SP–PR is emitted at $SCT_0 \cdot TD_{12}$ to shift PR one time. Then, $F_P \cdot UA13 \neq 0$ & PR_4 are discriminated, and if $UA13 \neq 0$, it proceeds to CC_{10} due to an overflow in the calculation, and when PR_4 is "1", then F_P sets and returns to CC_{11}; but if PR_4 is "0", it directly returns to CC_{11}.

6) The PR operation in division is shown in Fig. 5-18. LA+BR is done at $CC_{11} \cdot SCT_0$, and if CA is emitted, UA1+1 is performed at SCT_1. If CA is not emitted, F_N sets and proceeds to CC_{13} where the correction of one time over-addition by LA–BR is done. Then, F_N resets and proceeds to CC_9. Then the left shift of UA & LA and PR–1 are done.

When it becomes PR_4, then F_P sets and the repetitive $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ cycle continues until PR becomes PR_0 where it leaves this repetitive cycle in the procedure of $CC_{11} \rightarrow CC_{13} \rightarrow CC_8$. If it is $UA13 \neq 0$ before F_P sets in $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ cycle, then there is an overflow in the calculation.

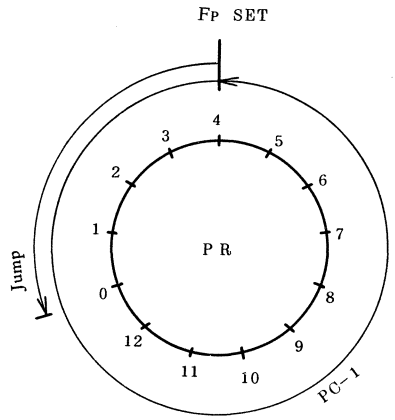


Fig. 5-18 PR Operation of Division

7) When it enters CC_8 after leaving $CC_{11} \rightarrow CC_{13} \rightarrow CC_9$ cycle, the interchange of BR↔ UA is done with PR_0 shifting to the fixed decimal point PR_4, and then, it enters PRT cycle.

5.8 PRT (Printing)

1) After proceeding to CC_3 cycle from CC_8 for the print-out of the calculated result, F_S is discriminated at CC_3, and if F_S is "1", minus (−) sign is printed; but, if F_S is "0", the feeding of the paper is done with F_P resetting at the end of P_9 to proceed to CC_{15}.

2) Assuming that the resultant data to be printed out is 1234567.8901 (PR_4=1), then at CC_{15}, the following steps of Fig. 5-19 ~22 are necessary.

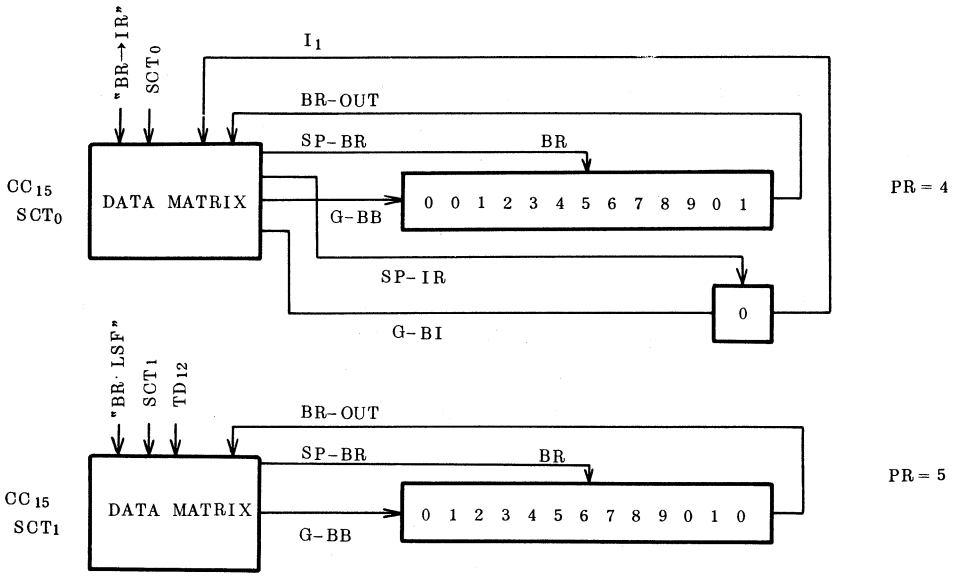


Fig. 5-19 Data Flow of PR_4 & PR_5 Timing

SP−IR & SP−BR are emitted at SCT_0 to open G−BB & G−BI. When the data of BR_{13} enters IR, then SP−IR is not emitted which means that it has shifted 13 times (1-word shift). Then, SP−BR is emitted at $\overline{TD_{12}}$ of SCT_1 to open G−BB for the left shift to be performed.

Also, PR+1 is done in the timing chip to determine the printing position of the decimal point. Then, if FP is set, the print-out is done; but if FP is reset, then the discrimination of BR13≠0 is carried out without print-out. If it is BR13≠0 after the left shift of BR, then FP sets with it returning to CC_{15}·SCT_0; but when BB_{13}≠0, then it enters the discrimination cycle of PR_0, and when PR_0 is "0", it returns to CC_{15}; but if PR_0 is "1", it proceeds to CC_7 which is the decimal point print-out cycle and sets FP for fraction print-out.

In Fig. 5-19 (b), since BR_{13} is "0" and it is PR=5, therefore, in the discrimination of BR13≠0, it is "0" and enters the PR_0 discrimination; but since PR_0 is "0" (PR=5), it returns to CC_{15}·SCT_0.

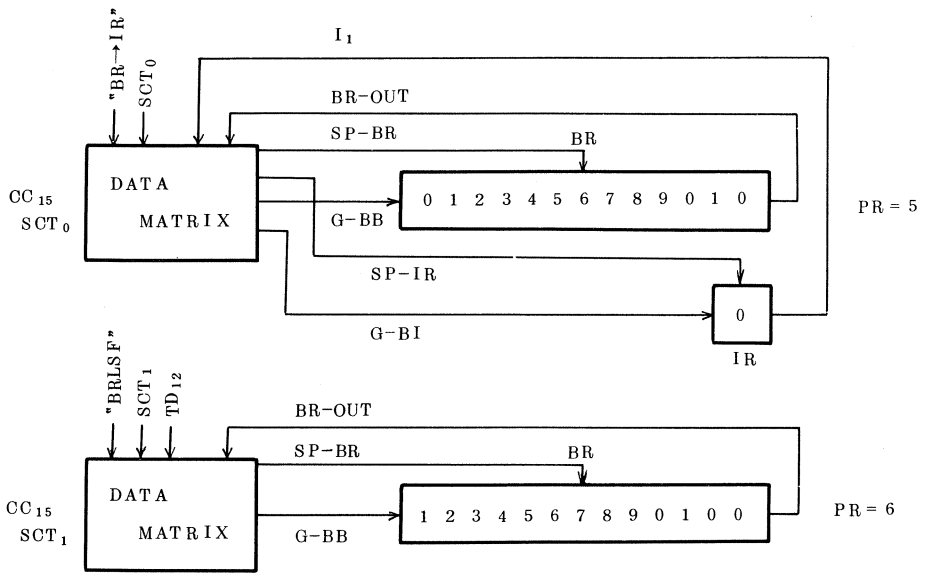


Fig. 5-20 Block Diagram at PR=5 & 6

After BR→BR, BR→IR, BR·LSF & PR+1 is performed, then it becomes BR13≠0 with setting FP and proceeds to CC_{15}·SCT_0. Where BR→BR, BR →IR, BR·LSF & PR+1 again takes place.

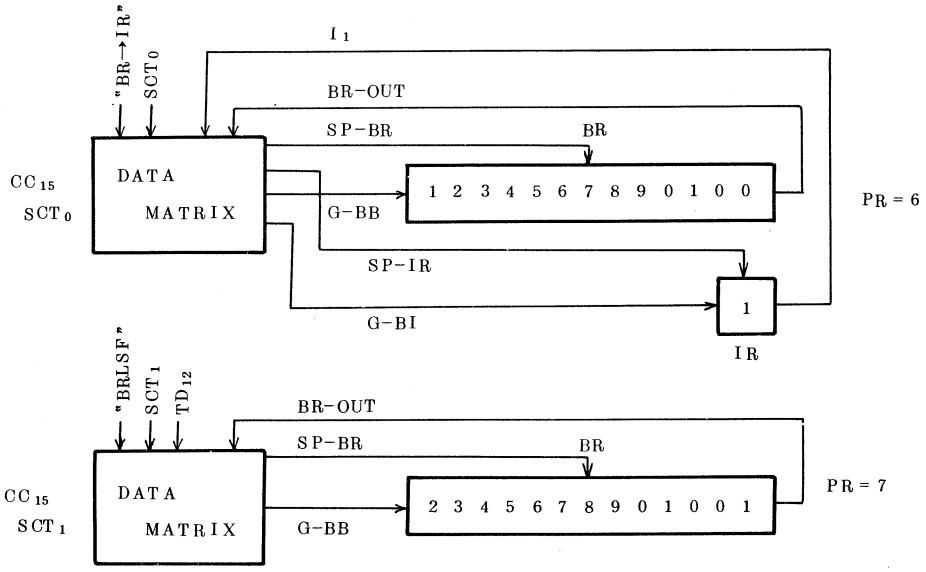


Fig. 5-21 Block Diagram at PR=6 & 7

At this time, since FP is set, then the print command is emitted from the control chip. Due to this, 1 which is the content in IR is printed on the tape.

After print-out completion, operation proceeds to CC6 to discriminate PR0·PR4. If PR0 is "1" which is the time to print-out the decimal point, then it advances to CC7 to print-out the point, and after that, retunrs to CC15·SCT0.

If PR0 is not equal 1, then operation returns to CC15·SCT0 without CC7.

If PR is PR4, it means that the prinr-out operation is completed, then advances to CC14·FP.

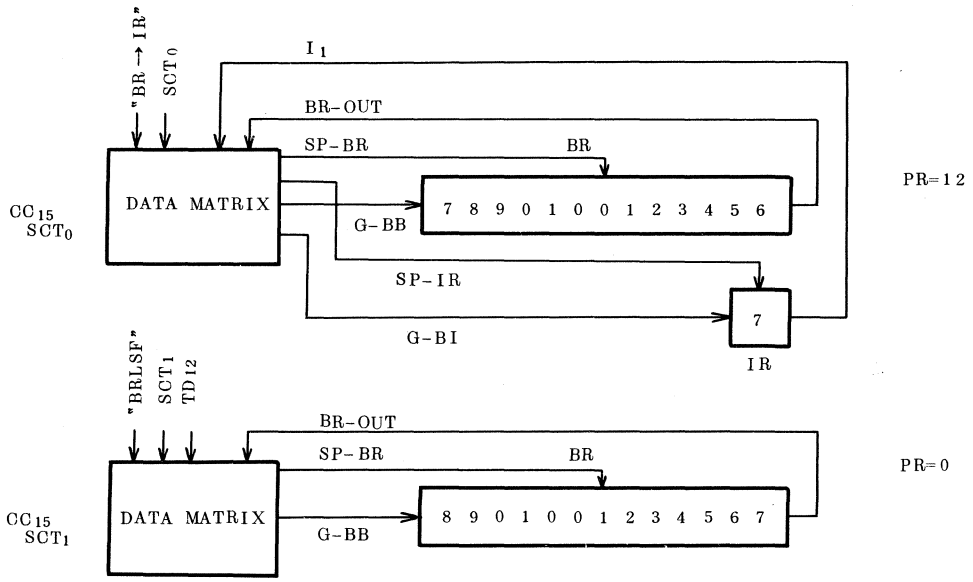


Fig. 5-22 Block Diagram at PR_{12} & PR_0

Fig. 5-22 shows that the conditions when PR becomes PR_0.

After print-out of 7 which is the content in IR, PR becomes PR_6 at CC_6 cycle, thus it proceeds to CC_7 to print-out the decimal point and returns to CC_{15}.

After operations are print-out of the fractional digits.

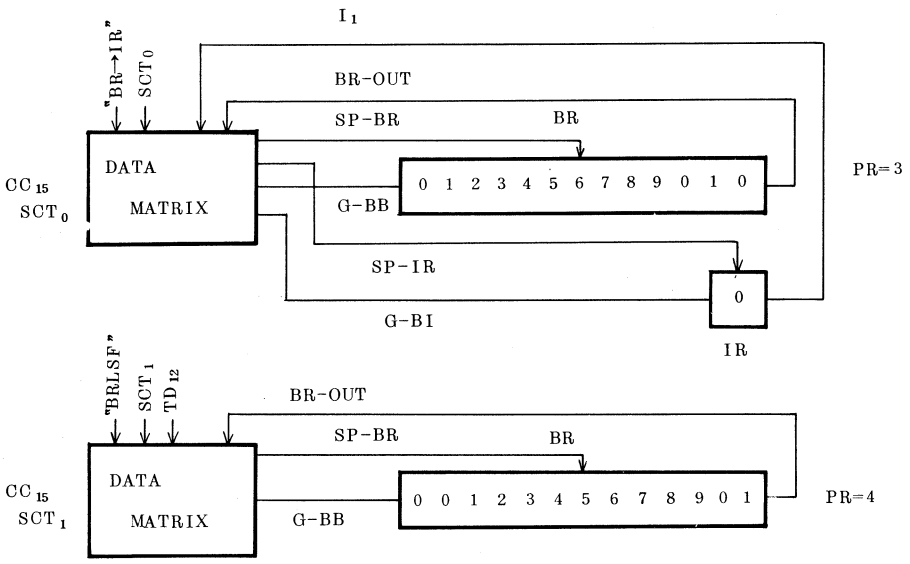


Fig. 5-23 Block Diagram at PR3 & PR4

The discrimination of the printing operation completion is carried out by PR4. That is, when PR becomes PR4 during BR·LSF & PR+1 operations, control counter proceeds to $CC_{14}\cdot F_P$ from CC_6.

3) After print-out operation, there are 2-letter spaces. Therefore, one space paper feed is performed at $CC_{14}\cdot\overline{F_P}$ and one more time at $CC_{14}\cdot F_P$. At the end of P_9, operation proceeds to CC_1 to discriminate KST. If KST is "0", it becomes CC_0, otherwise it remains at CC_1.

HOW TO REPAIR

CONTENTS

6. How to Repair

6.1 Operation Check Program

The following Table 6-1 is used to check the calculting operation of the Pocketronic.

NO.	KEY	PRINT	REMARKS
1	C	C	
2	1−÷·0C=	1- ÷ .0C = .0000	Clear Check
3	−012345678·9++	- 012345678.9+ +	Entry & Addition
4	=	= 24691357.8000	
5	12345678·9−−−	12345678.9- - -	Subtraction
6	=	=-12345678.9000	
7	13−÷ 15=	13- ÷ 15=-.8666	Division
8	45=	45= 3.0000	Constant Division
9	123−×	123- ×	
10	1234567891	123456789	Entry Overflow
11	CI·1234056	E .123405	
12	CI1·23=	E 1.23=-151.2900	Multiplication
13	456=	456=-56088.0000	Constant Multiplication
14	×=	× =C	Multiplication Overflow
15	2+=	2+ = 2.0000	Mixed Calculation
16	×=	× = 4.0000	
17	÷2·=	÷ 2.= 2.0000	
18	×+3+=	× + 3+ = 5.0000	
19	99999999+	99999999+C	Addition Overflow

Table 6-1 Operation Check Program Sheet

6.2 Remedies and Adjustments

6.2-1 Power Circuit

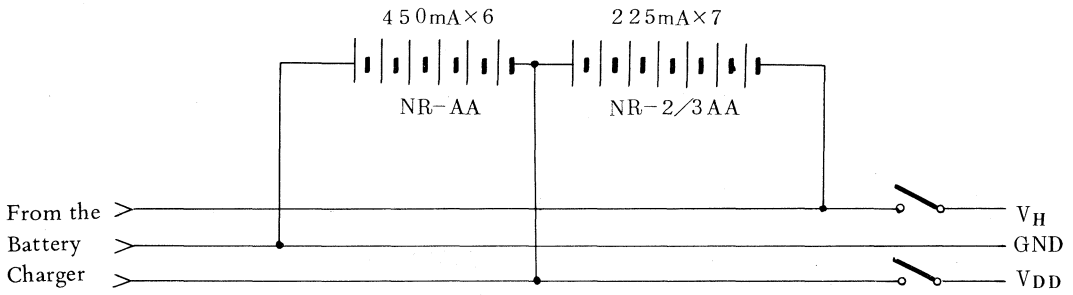


Fig. 6-1 Power Circuit

VH and VDD are obtained by connecting two different sets of batteries, one set of them, consist of six NR-AA type, and other is seven NR-2/3 type batteries. specification of the batteries are as follows.

	Nominal Voltage	Capacity (AH)
NR-AA	1.2V	450m
NR-2/3A	1.2V	225m

VH: −16.0V
Fluctuation range −15.0～−19.0V
For thermal head and solenoid circuit

VGG: −14.0V
Fluctuation range ±10%
For oscillation circuit and LSI

VDD: −7.5V
Fluctuation range −6.75 ～ −8.5V
For LSI, key circuit and thermal head

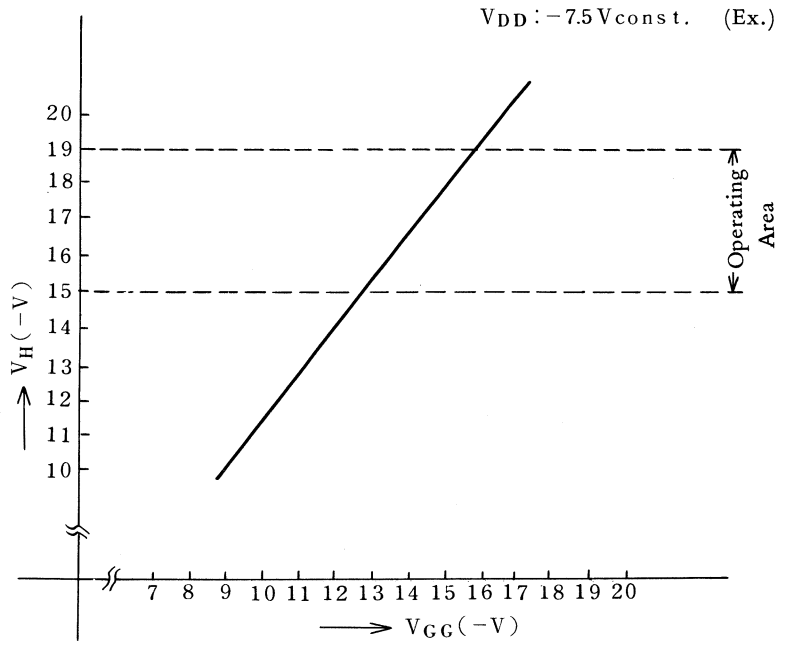
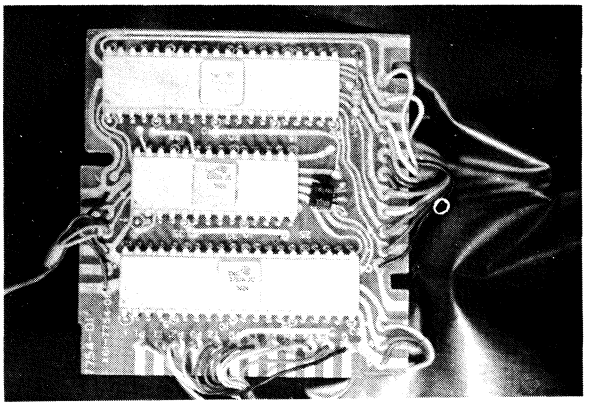


Fig. 6-2 VH & VGG Characteristics

6.2-2 LSI



TMC1730 . . . . . Control Chip

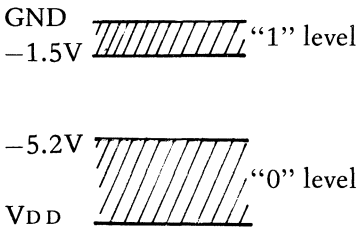
TMC1731 . . . . . Data Chip

TMC1732 . . . . . Timing Chip

Fig. 6-3 LSI Card Set

The output signal levels are specified as follows.

"0" level	−5.2V ~ VDD
"1" level	−1.5V ~ GND



Only TH1 ~ TH4 and P1 ~ P5 which are output signals of the Timing Chip are specified as follows.

[Ex.]

P1 ~ P5

"0" level	−15.0V ~ −15.6V
"1" level	−6.8V ~ −7.2V

TH1 ~ TH4

"0" level	−15.4V ~ −15.8V
"1" level	−12.2V ~ −12.8V

(1) Control chip (TMC1730)

Pin Location

Pin No.	Signal	Pin No.	Signal
1		15	CR2
2		16	CR3
3	I1	17	CR4
4	IN	18	CR5
5	SCT1	19	ϕ1
6	PR0	20	ϕ2
7	PR4	21	SP−CC
8	GND	22	VGG
9	VDD	23	$\overline{\text{MSD=0}}$
10	CT4	24	$\overline{\text{CA}}$
11	CT3	25	KST
12	CT2	26	KEY (C+CI)
13	CT1	27	I2
14	CR1	28	I3

Table 6-2 Control Chip Pin Locations

(V_{DD}=−7.5V V_H=−16V "1" level GND ~ −1.5V "0" level −5.2V ~ V_{DD})

Output	Pin No.	Ex. 1		Ex. 2		Ex. 3	
		"0"	"1"	"0"	"1"	"0"	"1"
CT_1	13	−7.2	−0.3	−7.2	−0.2	−7.1	−0.2
CT_2	12	−7.1	−0.2	−7.1	0	−7.1	−0.1
CT_3	11	−7.1	−0.1	−7.1	0	−7.1	−0.2
CT_4	10	−7.3	−0.2	−7.3	−0.2	−7.4	−0.3
CR_1	14	−7.1	−0.1	−7.0	−0.1	−7.1	−0.1
CR_2	15	−7.1	−0.2	−7.1	−0.1	−7.3	−0.2
CR_3	16	−7.1	−0.1	−7.0	0	−7.2	−0.1
CR_4	17	−7.1	−0.2	−7.2	−0.1	−7.3	−0.2
CR_5	18	−7.1	−0.2	−7.1	−0.1	−7.2	−0.1

Table 6-3 Control Chip Signal Level

(2) Data Chip (TMC1731)

Pin Location

Pin No.	Signal	Pin No.	Signal
1	I_4	21	TB_0
2	I_3	22	
3	I_2	23	
4	I_1	24	P_0
5	I_N	25	PR_1
6	KEY (C+CI)	26	V_{DD}
7	KST	27	GND
8	$\overline{CA}$	28	V_{GG}
9	$\overline{MSD=0}$	29	N
10	V_{DD}	30	9
11	ϕ_2	31	8
12	ϕ_1	32	
13	CR_5	33	7
14	CR_4	34	6
15	CR_3	35	5
16	CR_2	36	4
17	CR_1	37	3
18	SCT_1	38	2
19	TD_{12}	39	1
20	TB_3	40	0

Table 6-4 Data Chip Pin Locations

(V_{DD}=−7.5V & V_H=−16V)

Output	Pin No.	Ex. 1		Ex. 2		Ex. 3	
		"0"	"1"	"0"	"1"	"0"	"1"
KST	7	−7.2	−0.2	−7.3	−0.1	−7.0	−0.1
KEY(C+CI)	6	−7.2	−0.2	−7.2	−0.2	−7.1	−0.1
$\overline{CA}$	8	−7.2	−0.1	−7.2	−0.1	−7.0	0
I_N	5	−7.3	−0.3	−7.2	−0.2	−7.0	−0.1
I_1	4	−7.2	−0.3	−7.2	−0.1	−7.0	−0.1
I_2	3	−7.2	−0.3	−7.2	−0.1	−7.1	−0.2
I_3	2	−7.3	−0.3	−7.2	−0.1	−7.1	−0.2
I_4	1	−7.3	−0.3	−7.2	−0.1	−7.0	−0.2
$\overline{MSD=0}$	9	−7.2	−0.3	−7.2	−0.2	−7.1	−0.1

Table 6-5 Data Chip Signal Level

(3) Timing Chip (TMC1732)

Pin Location

Pin No.	Signal	Pin No.	Signal
1	MAG	21	SP−CC
2	P_0	22	TB_0
3	P_1	23	TB_3
4	TH_1	24	TD_{12}
5		25	SCT_1
6		26	PR_1
7	P_2	27	PR_0
8	P_3	28	PR_4
9	TH_2	29	V_{GG}
10	GND	30	CT_1
11	P_5	31	CT_2
12	TH_4	32	CT_3
13		33	CT_4
14	P_4	34	PHS
15	TH_3	35	I_N
16		36	I_1
17		37	I_2
18	ϕ_1	38	I_3
19	ϕ_2	39	I_4
20	V_{DD}	40	

Table 6-6 Timing Chip Pin Locations

(V_{DD}=−7.5V & V_H=−16V)

Output	Pin No.	Ex. 1		Ex. 2		Ex. 3	
		"0"	"1"	"0"	"1"	"0"	"1"
SP−CC	21	−7.3	−0.2	−7.2	−0.2	−7.4	−0.3
TB_0	22	−7.3	−0.2	−7.2	0	−7.3	−0.1
TB_1	23	−7.2	0	−7.2	0	−7.2	0
TH_1	4	−15.4	−12.8	−16.6	−12.8	−16.6	−12.6
TH_2	9	−15.8	−12.4	−16.6	−12.4	−16.6	−12.4
TH_3	15	−15.8	−12.2	−16.6	−12.2	−16.6	−12.6
TH_4	12	−15.8	−12.2	−16.6	−12.4	−16.8	−12.4
P_0	2	−7.0	0	−7.0	−0.1	−6.8	0
P_1	3	−15.4	−7.2	−15.0	−6.4	−15.4	−6.8
P_2	7	−15.0	−6.8	−15.0	−5.2	−15.2	−7.0
P_3	8	−15.4	−6.8	−15.8	−5.2	−15.6	−6.8
P_4	14	−15.4	−6.8	−15.0	−5.0	−15.4	−7.0
P_5	11	−15.4	−7.2	−15.2	−6.4	−15.6	−7.2
MAG	1	−15.6	−2.4	−15.8	−2.0	−15.8	−1.8

Table 6-7 Timing Chip Signal Level

(4) Precaution for LSI's

Generally, LSI's are comparatively strong against heat, but they are easily affected by electrostatic charge.

MOS LSI's have an oxide film with a very high insulating resistance, and since the oxide film is approximately 1000Å thickness, then the field strength becomes 5×10^6 V/cm, or close to the dielectric breakdown limit when 50V is applied to it.

When a transient voltage is applied, then the oxide film brakes down, and the gate & substrate is shorted. High insulation facilitates an accumulation of static charge which breaks the insulating film.

For example, by the rubbing of the clothing, which may hold a static charge of about 1000V, and if the clothing or the person wearing the clothing touches a gate, the voltage applied to the oxide film will cause a gate break down.

Be sure to avoid such incidents during repair work, and following points should be carefully followed.

1) Keep all LSI's in their designated box with all of their pins inserted in the conduction rubber.

2) Be sure the soldering iron is always grounded.

3) If a LSI is accidentally dropped, always check it with the LSI checker before using it.

4) Be sure turn OFF the POWER switch before repair work or attaching a LSI on the LSI checker.

5) Never bend the Prong of the LSI.

6) When using the soldering iron, do it as quickly as possible, so as to prevent the LSI from getting overheated.

7) Never leave or keep the LSI in a strong electric field.

6.2-3 AVR (Automatic Voltage Regulator)

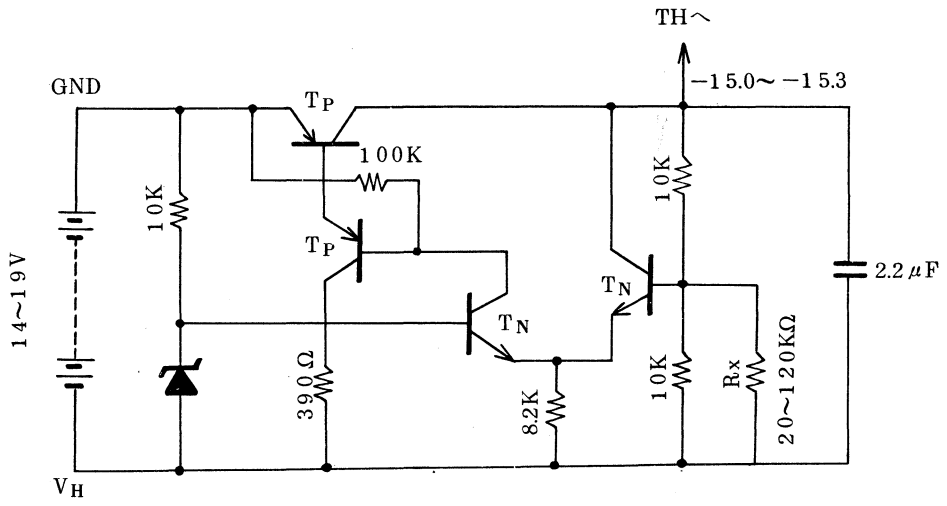


Fig. 6-4 AVR Circuit of the Thermal Head

Automatic Voltage Regulator is a break down prevention circuit for the thermal head and its output voltage is set at 15.0～15.3V replacing with a suitable Rx resistor.

This stabilized power supply circuit provide a constant 15.0～15.3V voltage to the head even though the battery voltage drops while in use.

6.2-4 Solenoid Circuit (Paper Feed)

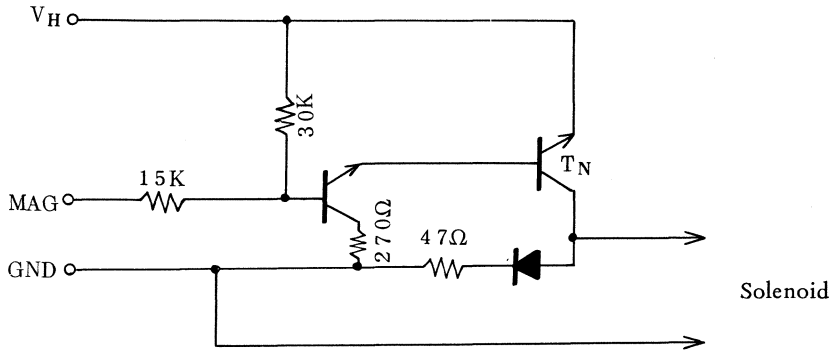


Fig. 6-5 Solenoid Circuit

If the MAG signal is emitted from the Timing chip during the P6 ~ P9 timing, "1" signal is applied to the base of the 1st-stage transistor and switched ON with also the 2nd stage transistor being switched ON.

When a current flows through the solenoid, then the plunger in the solenoid is drawn which engates the one-way clutch, so the paper feed roller rotates only in one direction.

When the flow of a current stops, the plunger returns to its original position by a spring. At this time only the plunger and the shaft of the feed roller rotate; but the rubber roller itself is idle.

6.2-5 Clock Pulse Generator

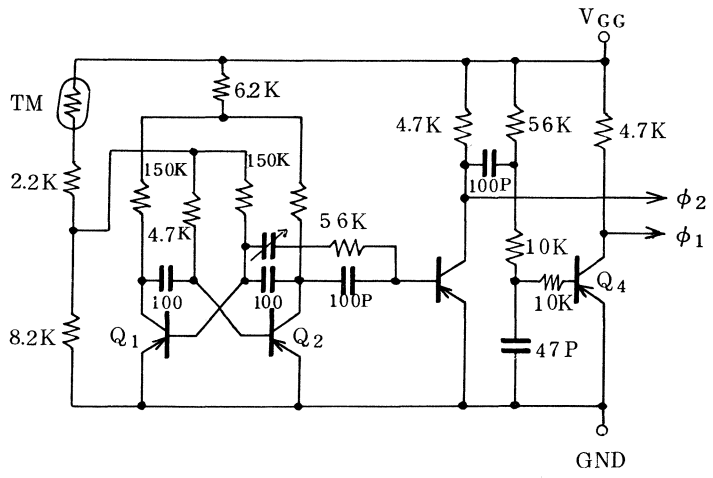


Fig. 6-6 $\phi 1$ & $\phi 2$ Clock Pulse Generator

$\phi 1$ & $\phi 2$ from the multivibrator which generates two clock pulses, and $\phi 1$ is formed by amplifying of $\phi 2$ and passing through the differentiating & integrating circuits.

Fig. 6-7 shows the differential waveform of $\phi 2$ clock pulse and Fig. 6-8 shows the integral waveform.

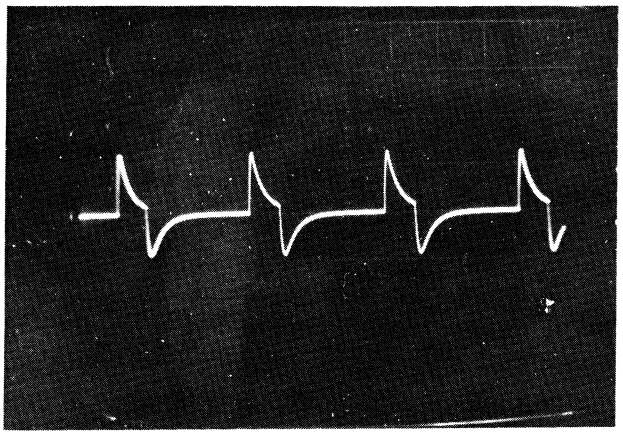


Fig. 6-7 Differential Waveform

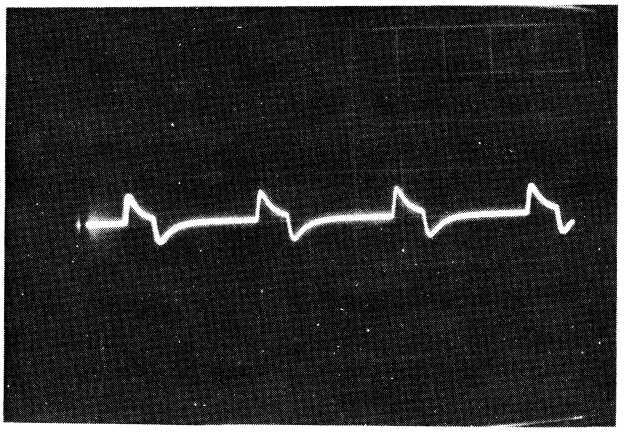


Fig. 6-8 Integral Waveform

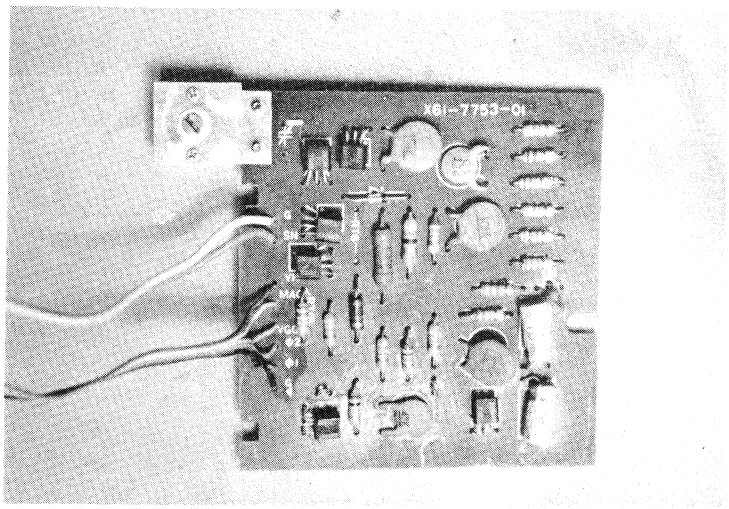


Fig. 6-9 Discrete Card

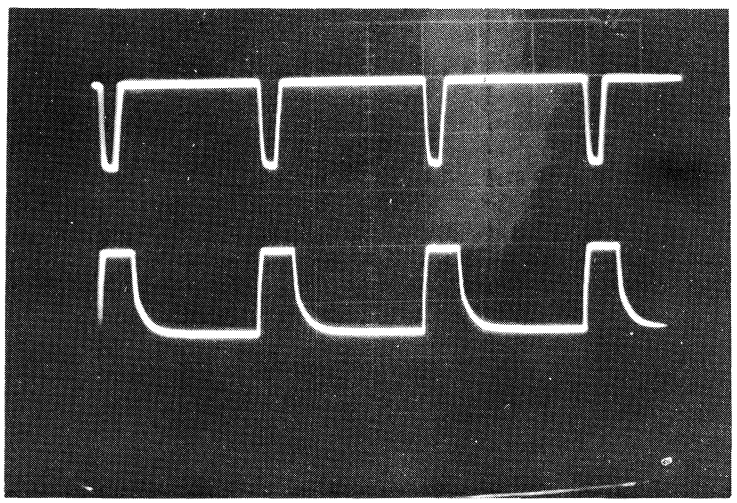
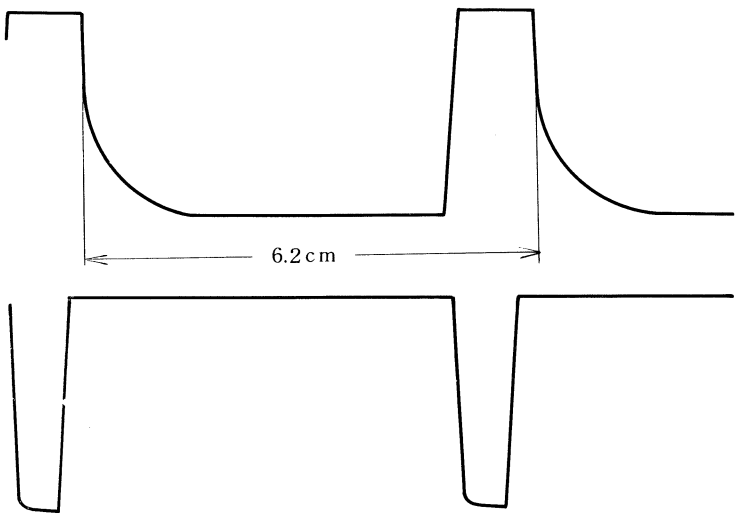


Fig. 6-10 $\phi 1$ & $\phi 2$ Waveforms



5V/cm

5 μsec/cm

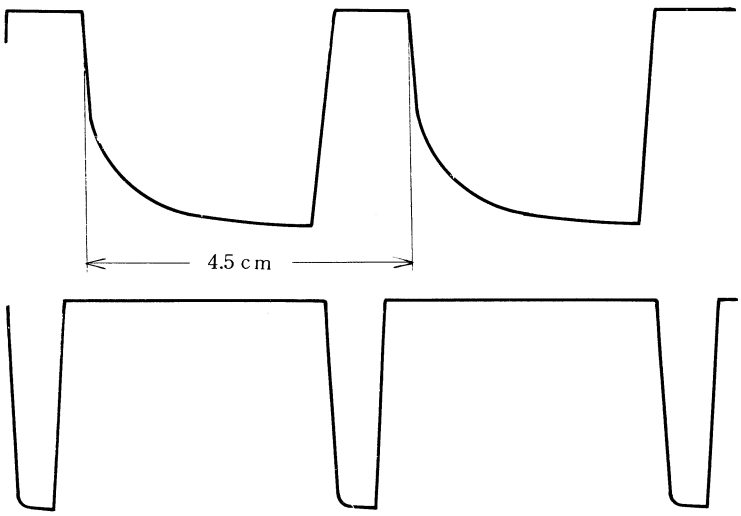
Cmax.

6.2×5 = 31〔μsec〕

$f = \frac{1000}{31} = 32.3$〔KHz〕

T = 31×520 = 6120

16.12〔ms〕



5V/cm

5 μsec/cm

Cmin.

4.5×5 = 22.5〔μsec〕

$f = \frac{1000}{22.5} = 44.4$〔KHz〕

T = 22.5×520 = 11700

11.7〔ms〕

Fig. 6-11 ϕ_1 & ϕ_2 Waveforms

Fig. 6-11 shows the waveforms of ϕ_1 & ϕ_2 when the variable capacitor in the oscillation circuit is adjusted at the maximum and minimum positions. Each printing time of $P_1 \sim P_5$ must be adjusted at 15 msec. in standard.

Since 15 msec. is the standard printing time at room temperature, and there are 520 clock pulses due to

$$5(Tx) \times 2(SCT) \times 13(digit) \times 4(bit)$$

Therefore,

$$\frac{15000}{520} = 28.85\ \mu sec$$

$$F = \frac{1}{T} = \frac{1}{28.85 \times 10} = 34662\ Hz$$

Thus, the oscillation frequency is

34.66 KHz

6.3 How to Detect Malfunctions

If a trouble occurs, confirm its conditions and localize the cause of the trouble, then the proper measures are taken.

Before making any repairs or replacements, always be sure to follow the checkings point of 6.3-2.

6.3-1 Service Equipments

(1) LSI Checker

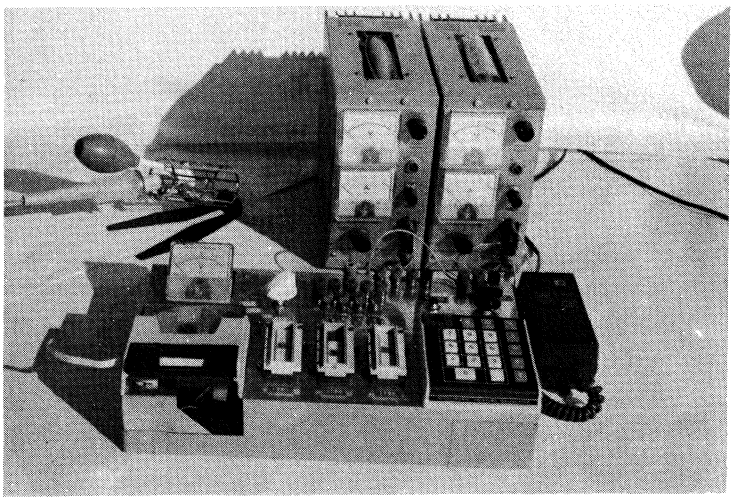


Fig. 6-12 Service Equipment

Three LSI's and thermal head can be checked by this checker.

The checking method is described in the checker's service manual.

(2) Stabilized Power Supply Set

Two stabilized DC power supply units are used for checking the voltage margin of the LSI's.

(3) Work Bench & Tools

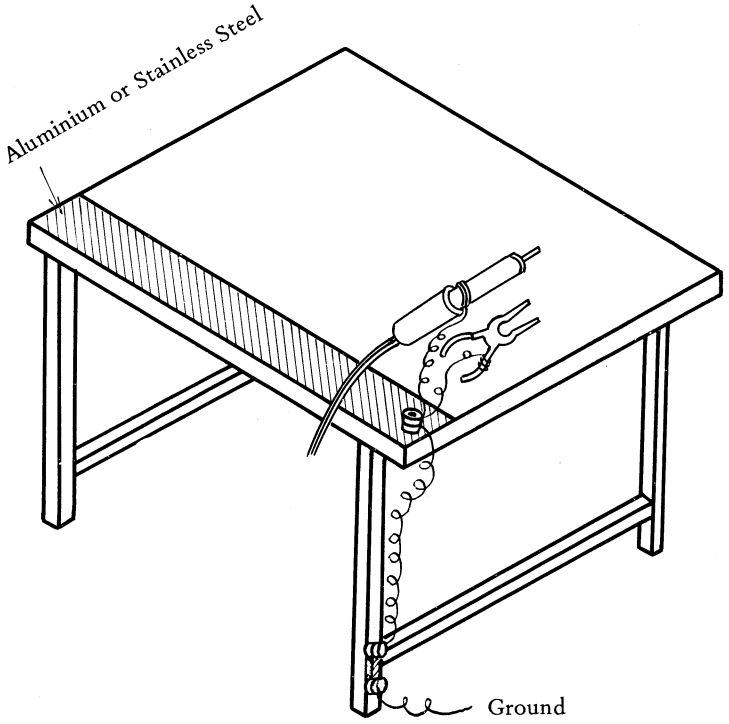


Fig. 6-13 Work Bench

Attach an aluminium or stainless steel strip along the side of the work bench, and ground it as shown in Fig. 6-13.

When replacing or checking any LSI's, the various parts, equipments or tools are always in contact with the grounded strip during the repair work; the soldering iron should always be grounded to avoid any leakage of the power, otherwise it will cause a breakdown in the LSI's.

6.3-2 Points to be Checked

If any trouble occurs, first check the following power voltages and then the signals.

(1) Power Supply Circuit

Remove the 4 retaining screws at the bottom of the machine and measure the voltages of GND, V_{DD} & V_H. A highly reliable circuit tester must be used to measure these rating voltages are as follows;

GND	.....	OV
V_{DD}	.....	$-6.75 \sim -8.5$V
V_H	.....	$-15.0 \sim -19.0$V

Always connect the Hi-Speed Battery Charger to it, and confirm the operations and voltages before proceeding with any repairing.

(2) Oscillation Circuit

Set the time range of the oscilloscope at 0.5 msec. position to measure the waveform of $\phi 1$ & $\phi 2$ shift pulses.

Since the standard printing time is about 15 msec, confirm whether the time length of one cycle of $\phi 1$ & $\phi 2$ is 5.77 cm on the cathode ray tube or not, and also whether their signal level of V_{GG} to GND is -14.0V$\pm 10\%$ or not.

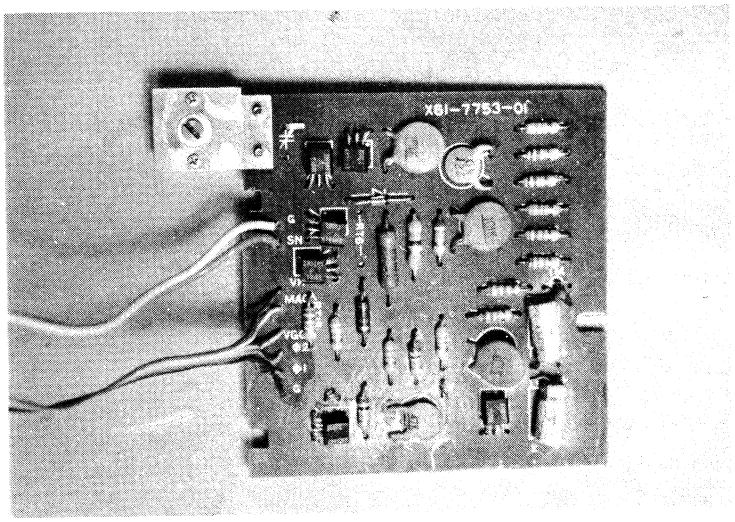


Fig. 6-14 Discrete Card

(3) LSI Card

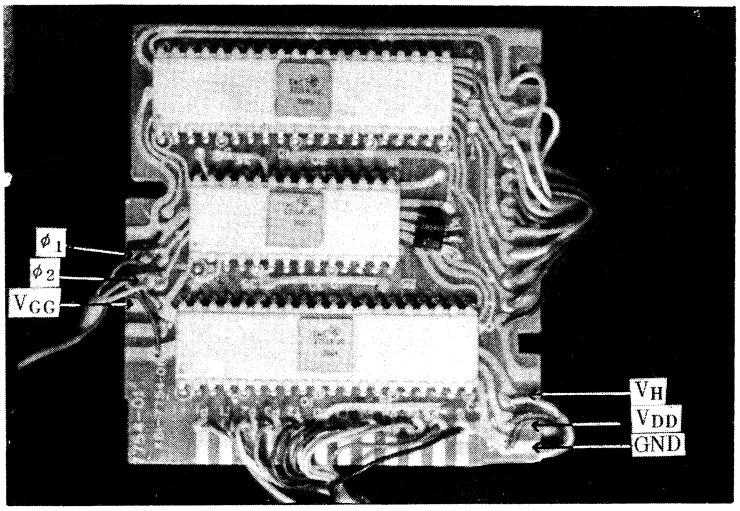


Fig. 6-15 LSI Card

Check the voltage of the following DC power supplies.

V_H	.....	$-15.0V \sim -19.0V$
V_{DD}	.....	$-6.75 \sim -8.5V$
V_{GG}	.....	$-14.0V \pm 10\%$
GND	.....	0V
$\phi 1$, $\phi 2$	.....	34.7 KHz

(4) Thermal Head

Input Term.			
# 1	AVR	# 8	TH_2
# 2	P_5	# 9	P_3
# 3	TH_4	#10	P_2
# 4	VH	#11	TH_1
# 5	P_4	#12	
# 6	TH_3	#13	
# 7	V_{DD}	#14	P_1

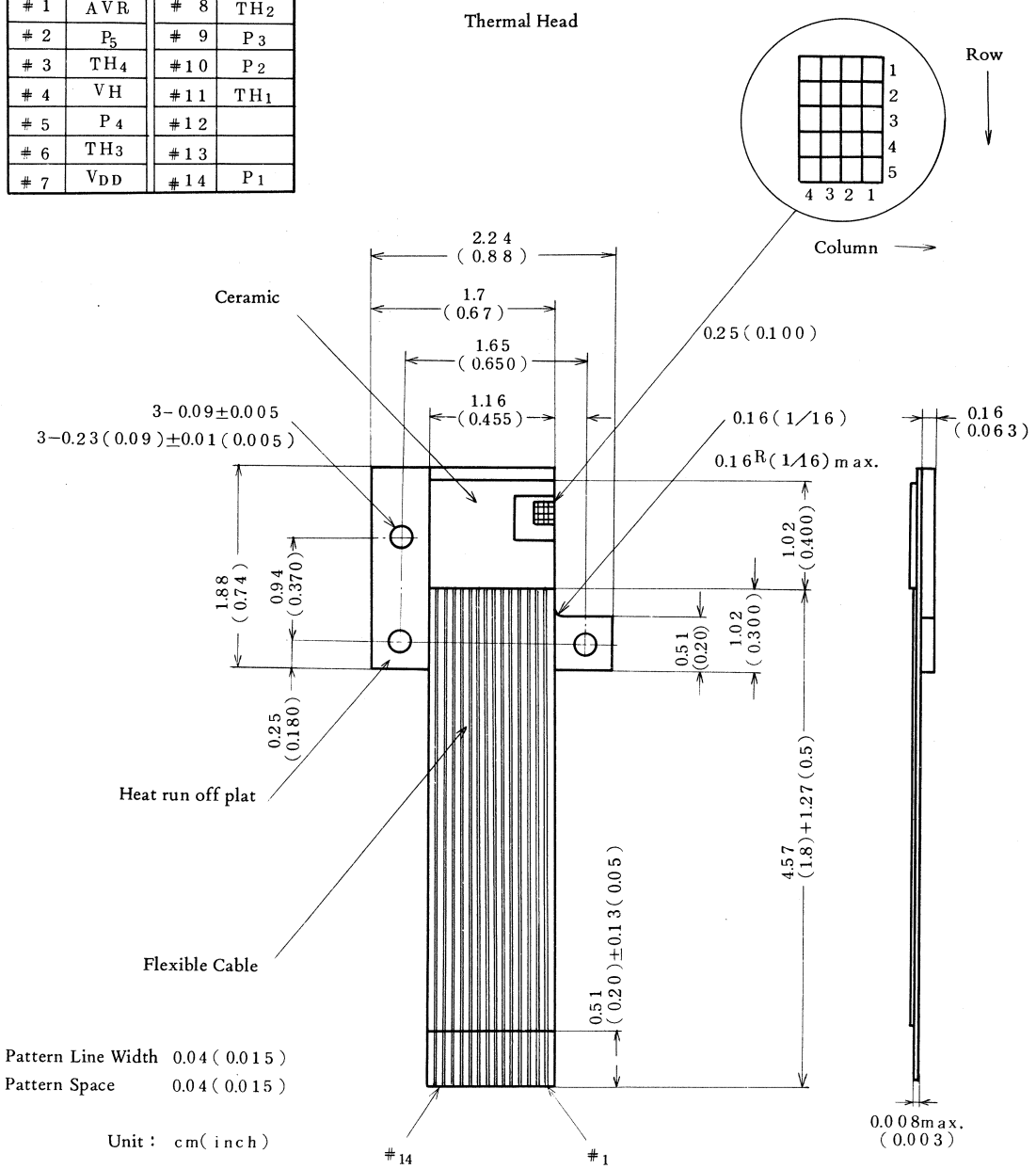
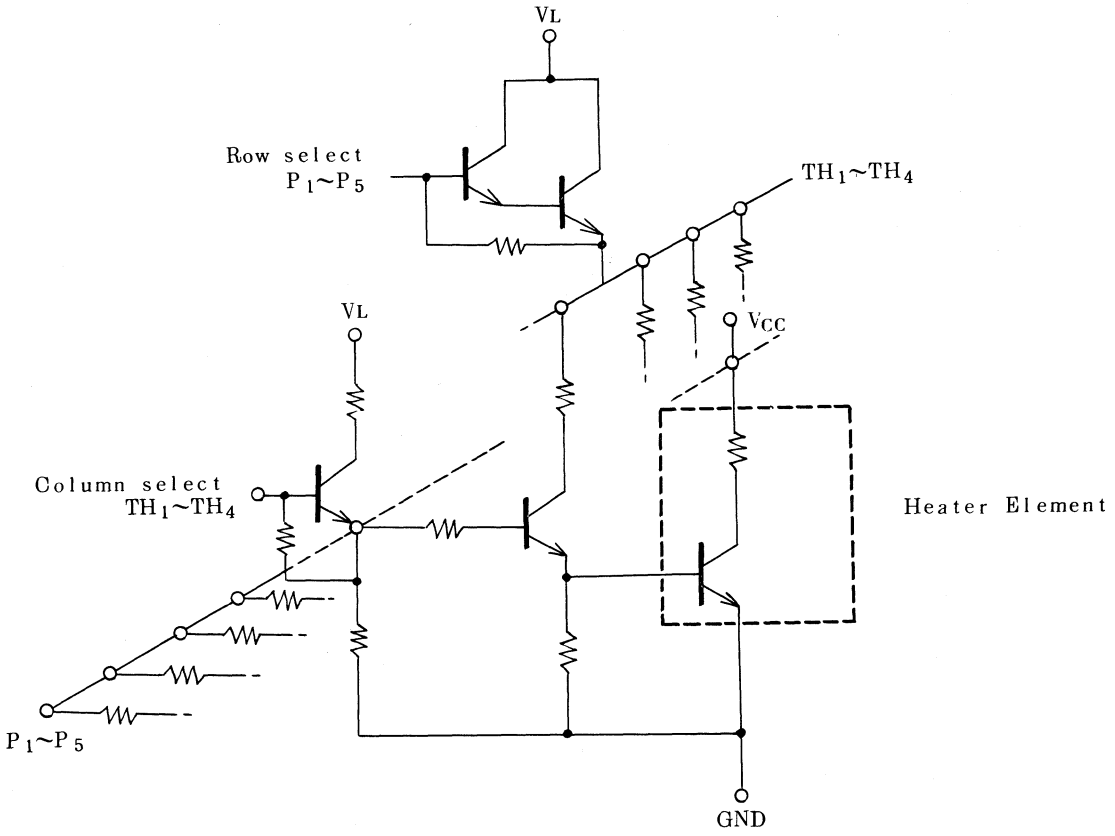


Fig. 6-16 Thermal Head



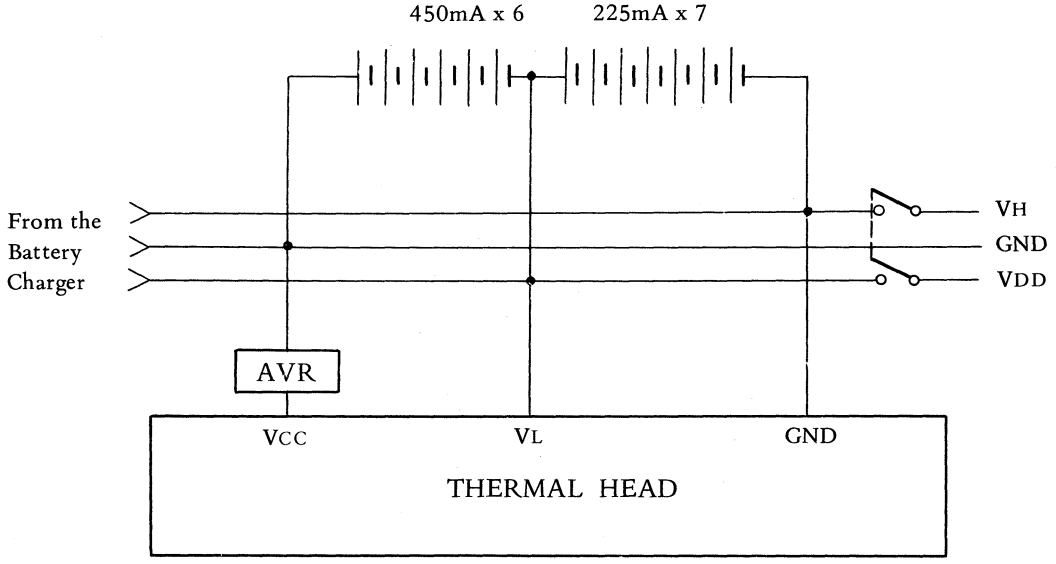


Fig. 6-17 Thermal Head Circuit

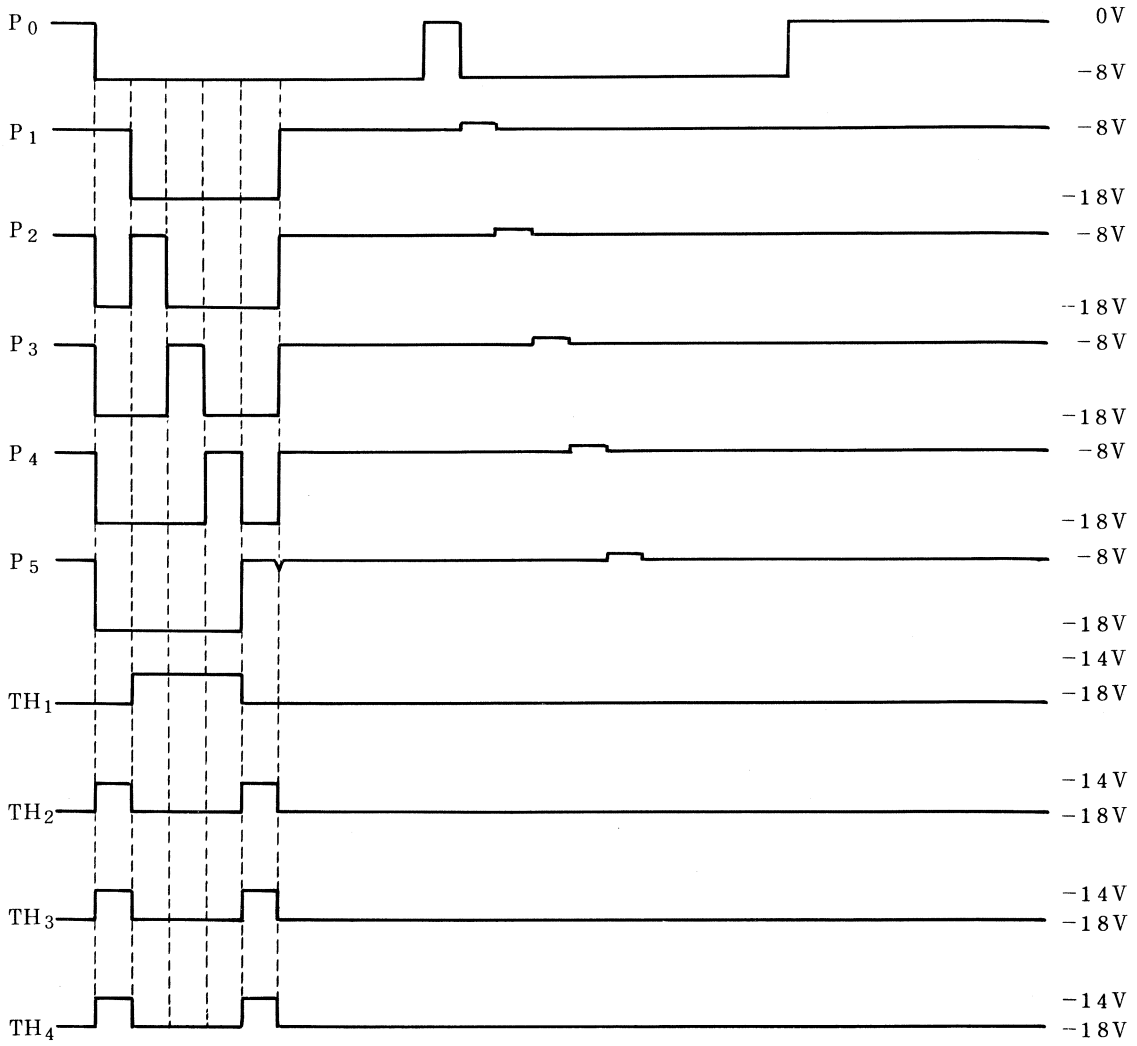


Fig. 6-18 Printing Signal Waveform

Fig. 6-18 show the timing of $P_0 \sim P_5$ and $TH_1 \sim TH_4$ in the print-out of the symbol C.

The "1" level of P_0 signal changes to "0" level which is from GND to V_{DD}, while the $P_1 \sim P_5$ level change of "1" to "0" is from V_{DD} to V_H and the $TH_1 \sim TH_4$ level change of "1" to "0" is from −12V to −16V.

In the symbol of C, TH_2, TH_3 & TH_4 signals become "1" at P_1 time;

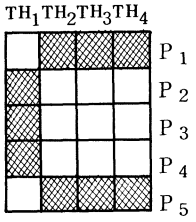
At P_2 time, TH_1 becomes "1"

At P_3 time, TH_1 becomes "1"

At P_4 time, TH_1 becomes "1"

At P_5 time, TH_2, TH_3 & TH_4 become "1"

As shown the following figure.



By the same method, symbols, sign and numerals are printed out as shown in Fig. 6-19.

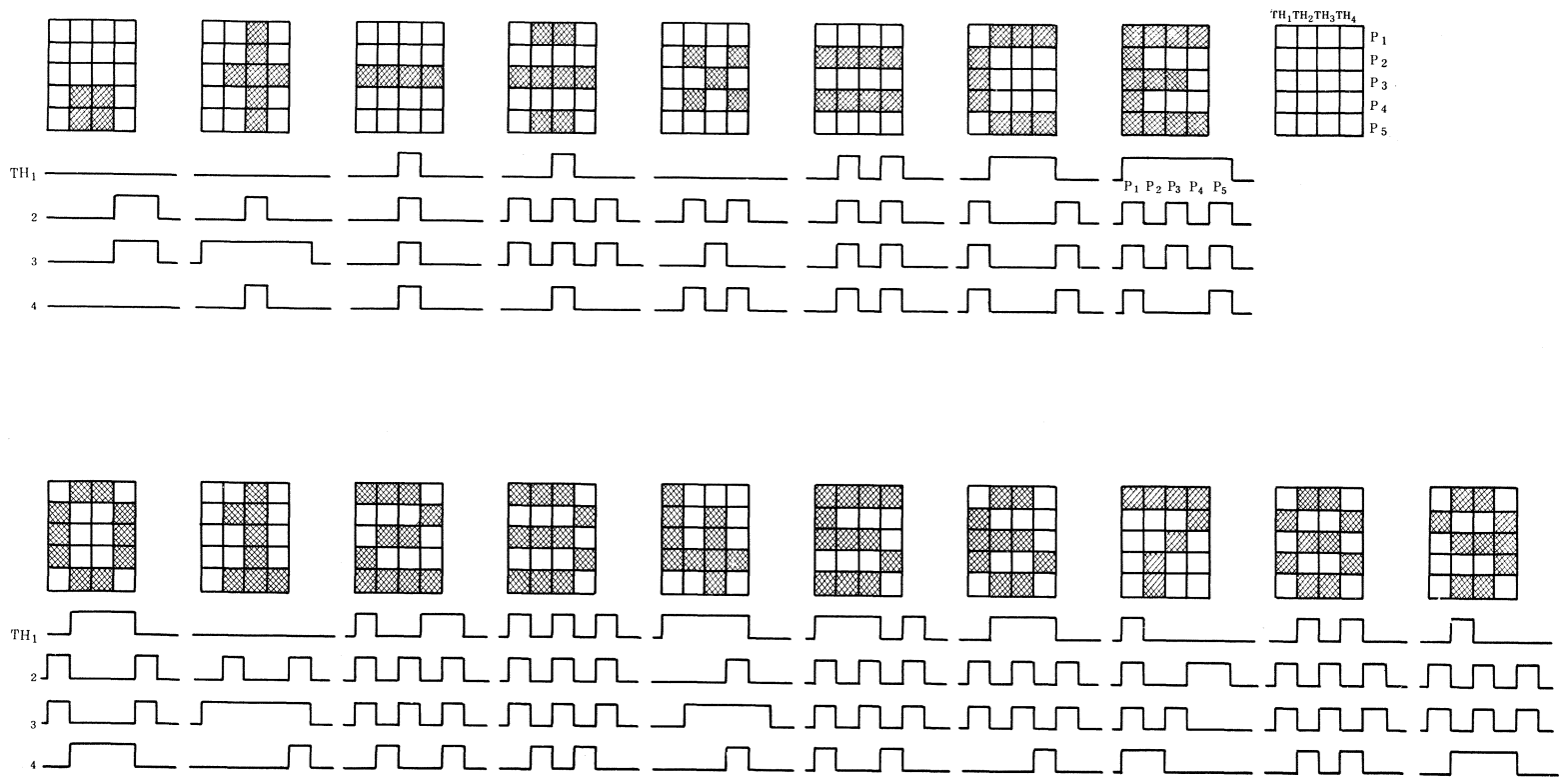


Fig. 6-19 Character Patterns of Thermal Head with Waveforms

6.4 Trouble-Shooting

The trouble-shooting of this calculator greatly differs from that of the former IC series.

Localizing the causes of troubles is carried out by checking the input or output waveform of IC, transistor or diode with the triggering to a suitable timing.

Since this mode employs LSI's and also PLA system, then one LSI corresponds to a card of the former IC model; thus the inspection of any special circuit or to check a waveform of certain circuit with triggering at a suitable timing in the LSI can not be done.

Thus, in this model, trouble-shooting is carried out by removing the doubtful LSI and checking it with the Pocketronic Checker to determine whether it is damaged or good.

Since LSI's are easily damaged by static charge, heat of the soldering iron or breaking off of the prongs when removing the LSI; therefore, check any LSI very thoroughly.

6.4-1 Repair Work Precautions

1. Always confirm whether it is an operational error or not.

   (i) Voltage drop in the battery will cause a faulty paper feeding or wrong operation.

   Attach the Hi-speed Battery Charger and after about 3～5 minutes wait, check the operation again.

   (ii) Inproper insertion of the tape will cause a faulty print-out and paper feeding.

   (iii) Erroneous calculation entry by the operator such as: [3] [+] [3] [=] 3.0000 (no addition) should be [3] [+] [3] [+] [=] 6.0000.

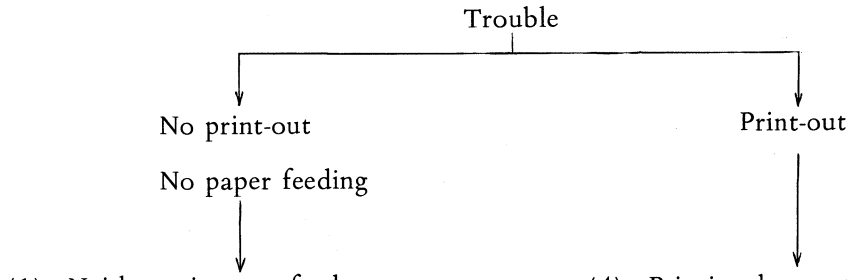
2. Always turn OFF the POWER switch when making any repairs.

3. After removing the cover, check the connection of the wiring between the discrete card & LSI card, especially the wiring for $\phi 2$ signal because if $\phi 2$ line is disconnected when POWER switch is turned ON, the thermal head will be instanteously damaged.

4. Always must be checked all LSI's voltages and signal levels when any trouble occurs. When checking any signal, always check all LSI's terminal points connected with that signal by referring to the LSI Terminal Diagram of Logic & Timing Chart.

5. If the signal level is not correct or no signal appears, check wirings and printed patterns; but if there is no defects in the wiring or pattern, then the output source component is faulty.

6.4-2 Trouble-Shooting Chart



(1) Neither prints nor feeds
(2) Prints but does not feed
(3) Feeds but does not print

(4) Printing does not stop
(5) No space after order key or calculation
(6) Only one digit registers
(7) Wrong numeral registers
(8) Dot locking in pattern
(9) Too many dots
(10) Miscalculation
(11) Certain key does not register

(1) Neither print nor feeds

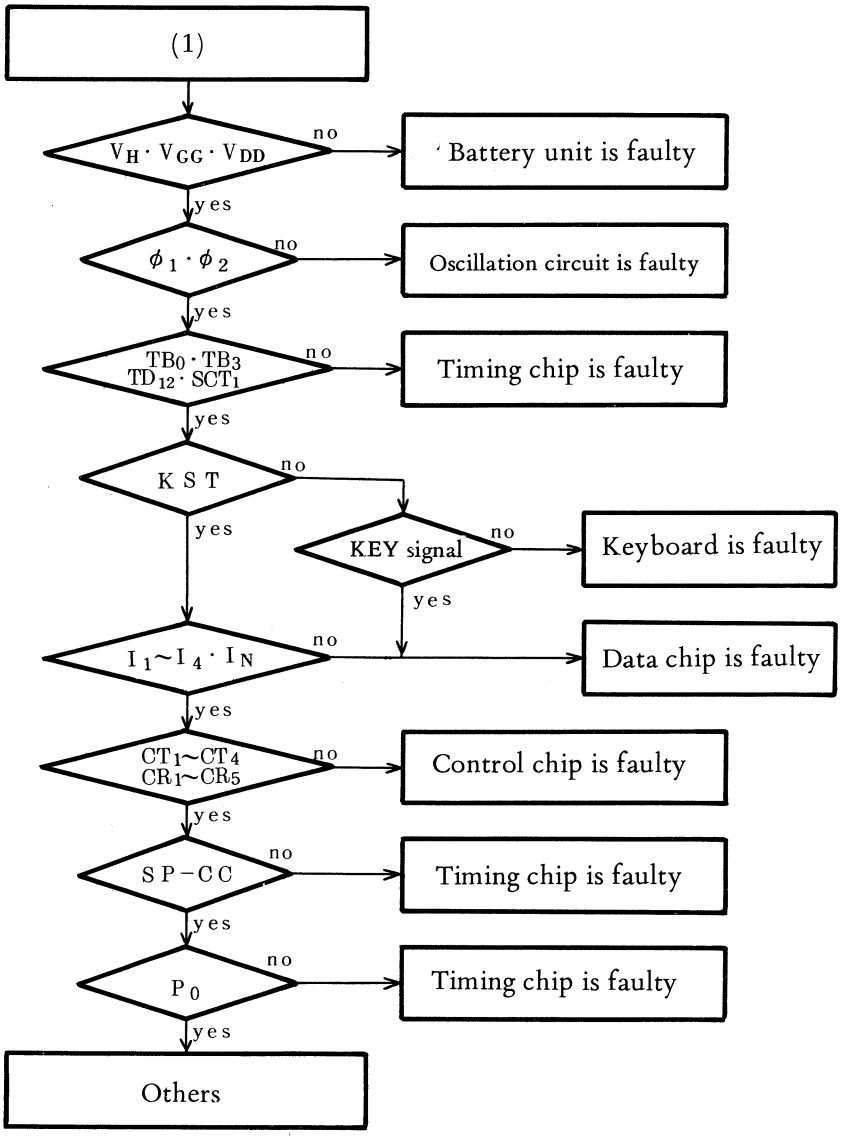


Fig. 6-20 Trouble Shooting Flow Chart

(i) Check whether the power supply voltages (V_H, V_{GG}, V_{DD} & GND) are normal or not, and also check the voltages at the LSI pins.

(ii) Check the clock pulses of $\phi 1$, $\phi 2$, TB_0, TB_3, TD_{12} & SCT been generated by using an oscilloscope. (Refer to Fig. 6-11 for correct waveforms)

(iii) Check the waveform of KST by pressing [C] key with the "+" trigger of SCT_1.

KST signal becomes "1" when [C] key is pressed and it is "1" as long as the key is being pressed; but as soon as it is released, KST signal becomes "0".

If KST is not emitted when [C] key is pressed, check data chip pin No. 33, and if there is a signal entering it, then the data chip is defective.

When there is no key signal entering the data chip, check the C & 7 signal of the keyboard.

(iv) Check whether $I_1 \sim I_4$ & I_N signals of the data chip are normal or not. For instance I_1, I_2 & I_3 are "1" with I_4 & I_N being "0" when [C] key is pressed.

(v) Check the waveforms of $CT_1 \sim CT_4$ & $CR_1 \sim CR_5$ by "+" trigger of KST. Following signals appear when [C] key is pressed.

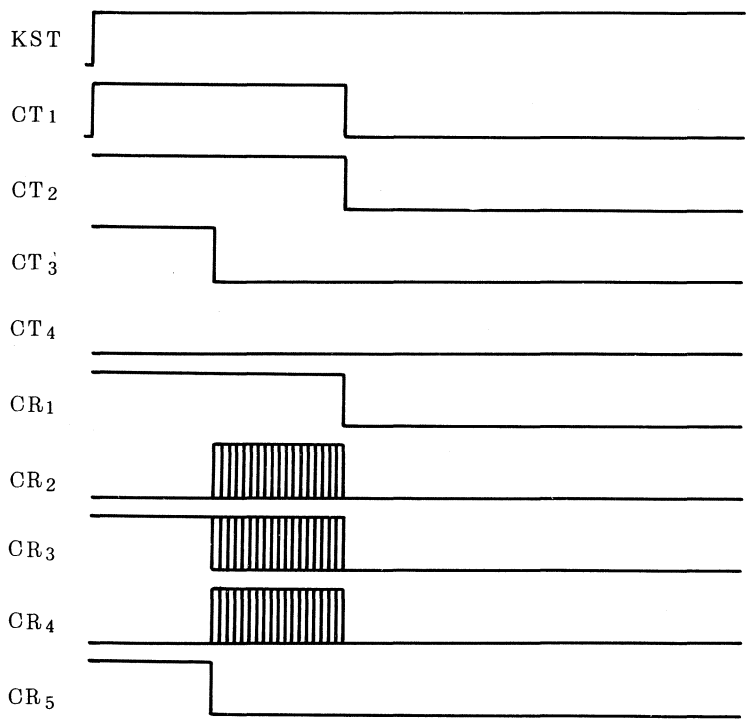


Fig. 6-21 CT & CR Waveforms

(vi) Check the waveform of SP–CC by "+" trigger of KST.

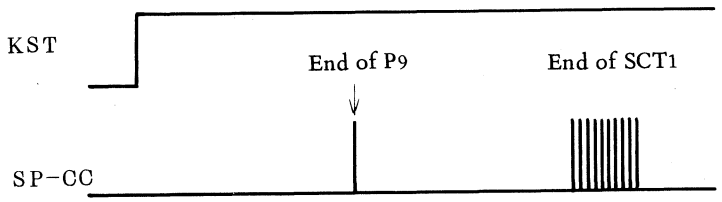


Fig. 6-22 SP–CC Waveform

(vii) Check the timing of P0 signal by triggering with its own signal.

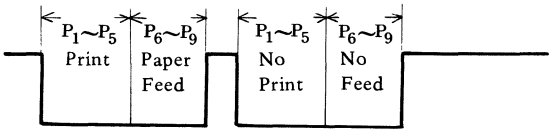


Fig. 6-23 P0 Waveform

(2) Prints but does not feed

In this case, first confirm that correct operation is performed or not by observing a number of spaces after [=] key is pressed. For instance, when [1] [2] [3] [×] [=] [=] [=] keys are pressed in sequence, there are 12 spaces by the first [=] key, 16 spaces by the second [=] key and 3 spaces by the last [=] key. If these spacing can be done correctly, arithmetic operations in the LSI's are correct, otherwise certain LSI or LSI's are faulty.

Even though there are correct spaces with no print-outs, then the thermal head is faulty. If the spacing operation is not correct, check the circuit according to the following method.

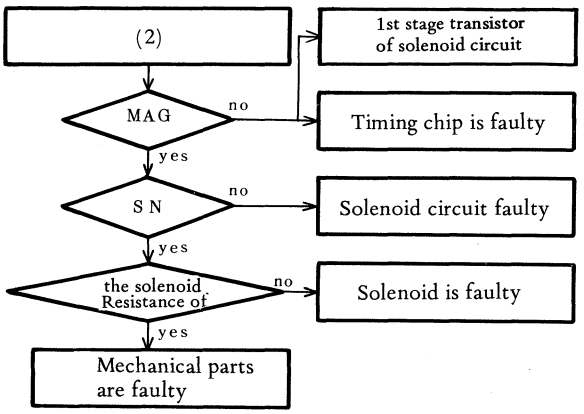


Fig. 6-24 Trouble Shooting Flow Chart

(i) Check the waveform of MAG signal by "–" trigger of P_0.

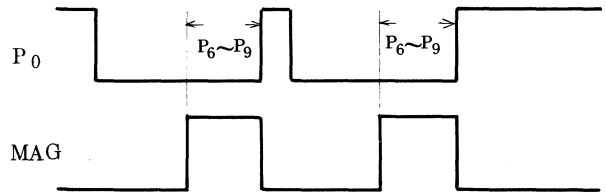


Fig. 6-25 MAG Waveform

If MAG signal is not emitted, the timing chip is faulty.

(ii) Check if MAG signal is applied to the solenoid circuit of the discrete card, then check its output SN.

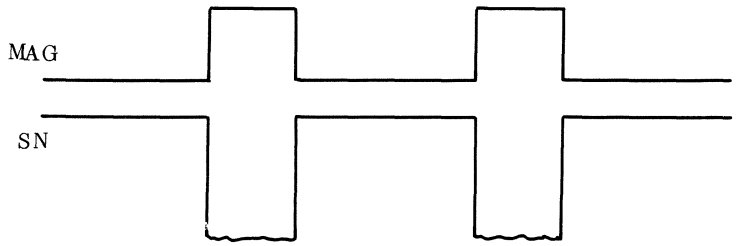


Fig. 6-26 SN Waveform

(iii) If the plunger does not move to rotate the roller even though SN signal is normal, check the resistance of the solenoid whose resistance is about 35 ohms.

(iv) If the roller does not rotate even though the resistance of the solenoid is normal with a current flows, then the mechanical parts are faulty.

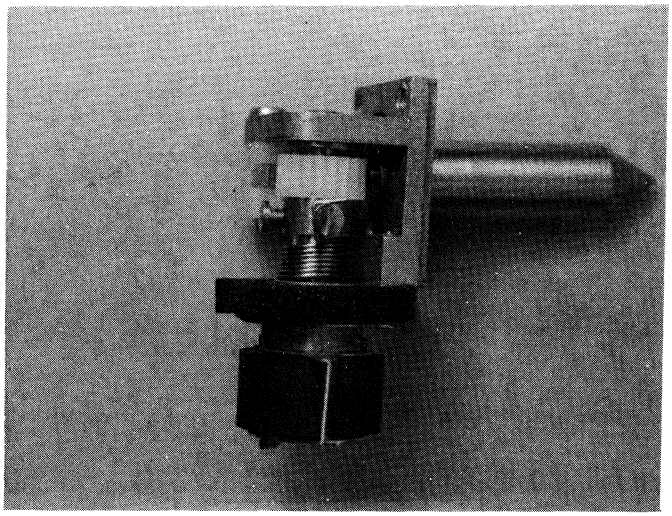


Fig. 6-27 Paper Feeding Roller

(3) Feeds the paper but does not print

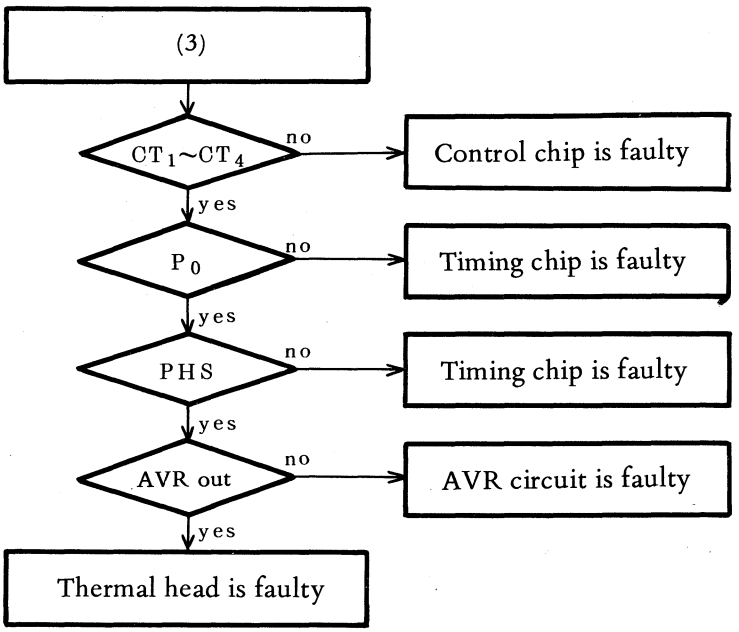


Fig. 6-28 Trouble Shooting Flow Chart

i) Check $CT_1 \sim CT_4$ by pressing [C] key with "+" trigger of KST. (Refer to Fig. 6-21 the correct waveforms)

ii) Check the timing of P_0 signal by triggering with its own signal. (Refer to Fig. 6-23 for correct waveforms)

iii) In this machine PHS signal is not used, then it is always connected to GND to make it "1".

iv) Check the output voltage of the Automatic Voltage Regulator whether 15.0 ~ 15.3V is supplied to the thermal head or not.

v) If no print-out is carried out even though correct GND & V_{DD} voltages are supplied to the thermal head, then the thermal head is faulty.

(4) Printing does not stops.

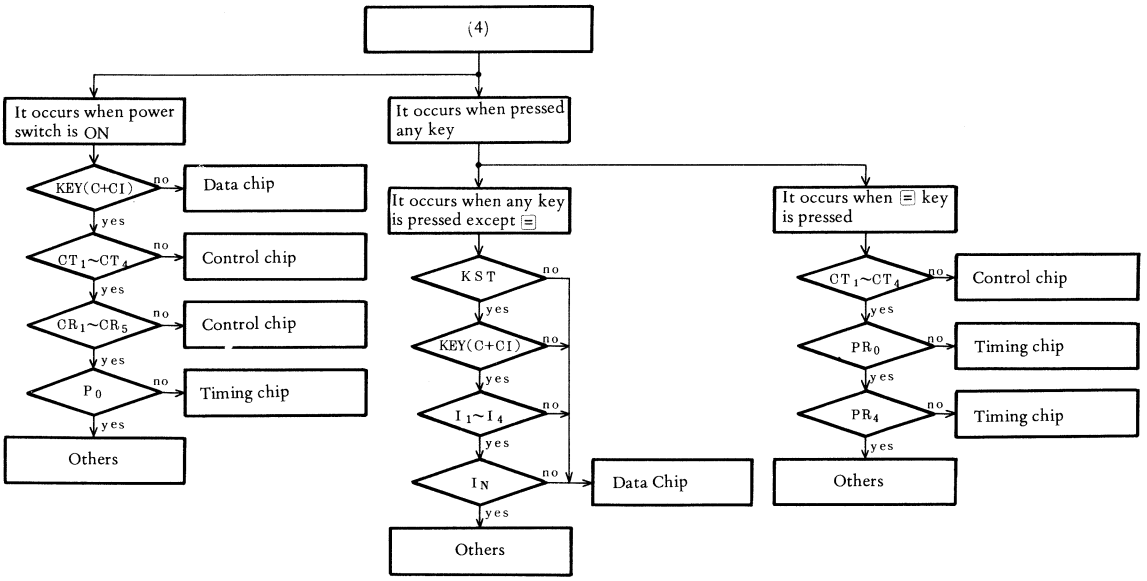


Fig. 6-29 Trouble Shooting Flow Chart

This phenomenon occurs when the POWER switch is turned ON, when any key is pressed or when = key is pressed.

When the POWER switch is turned ON, sometimes a few digits are printed; but this operation is no faulty, so always must be distinguish between the trouble and normal operation. Also, if the pin connection is faulty between LSI and its socket when checking the LSI by using the LSI checker, then sometimes happen these symptoms mistakenly, thus always must be inserted it surely to the checker.

(4)-1 Printing does not stops when the POWER switch is turned ON.

In this case, printed characters are usually C or E symbols. When CR_5 signal level is not normal, then C symbols are printed, and when CT_1 or KEY(C+CI) is "1" or if P_0 signal level is not normal, then E symbols are printed out.

i) Check the signal level of KEY(C+CI) signal by triggering SCT_1.
When [C] or [CI] key is not pressed, KEY(C+CI) signal should be "0".
Thus, if this signal is "1", then the keyboard is faulty.

ii) Check the P_0 signal level and its timing by triggering with its own signal. (See correct P_0 waveform when [C] key is pressed in Fig. 6-23)

iii) Check the waveform of $CT_1 \sim CT_4$ and $CR_1 \sim CR_5$ by triggering with P_0 signal.
When E symbol is being printed, CT_4 & CR_2 are "0"; but in the C symbol only CT_4 is "0".
At the same time, the other signals of CT & CR change from one state to the other at the end of P_9 time.

(4)-2 Printing does not stops when any key is pressed except [=] key.

i) Check KST signal level by triggering with SCT_1.

ii) Check KEY(C+CI) signal level by triggering with SCT_1.

iii) Check $I_1 \sim I_4$ and I_N signal timing and its level by triggering with P_0 signal. Since $P_1 \sim P_9$ can be observed if the time length of the oscilloscope is set at 20 msec.
In this observation, the timing of $P_1 \sim P_9$ must be observed by referring $I_1 \sim I_4$ & I_N signals.

(4)-3 Printing does not stop when [=] key is pressed.

In this case, the print-end timing is not fixed when PR_4 signal is not normal.

i) Check $CT_1 \sim CT_4$ signal timing and its level by triggering with P_0.
When print-out the calculated result, CT_1 is "1", CT_4 is "0" and CT_2 & CT_3 are changed at the end of P_9 time.

ii) Check PR_0 & PR_4 signal level by triggering with SCT_1.

(5) No Space After Order Key or Calculation

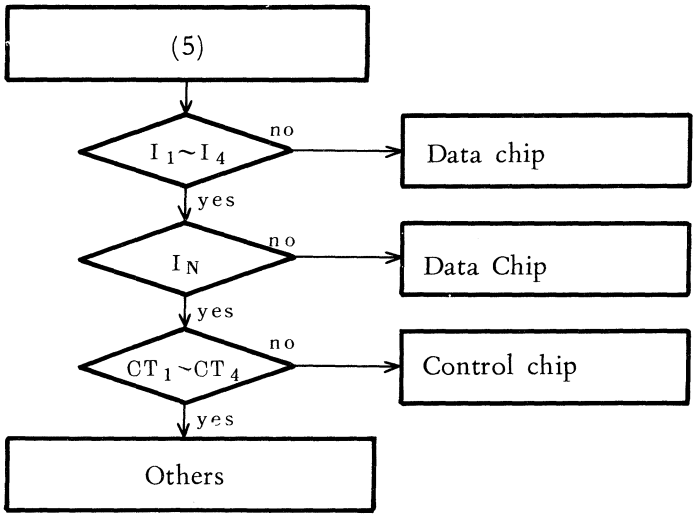


Fig. 6-30 Trouble Shooting Flow Chart

The order key has 1-digit space and a calculated result has 2-digit spaces, then if no spacing trouble occurs, check the machine according to the following ways;

i) Press the key, and check respective $I_1 \sim I_4$ & I_N by triggering with SCT_1.

ii) Check $CT_1 \sim CT_4$ signal level, expecially CT_3 & CT_4 by "+" trigger of SCT_1.

(6) Only One Digit Registers

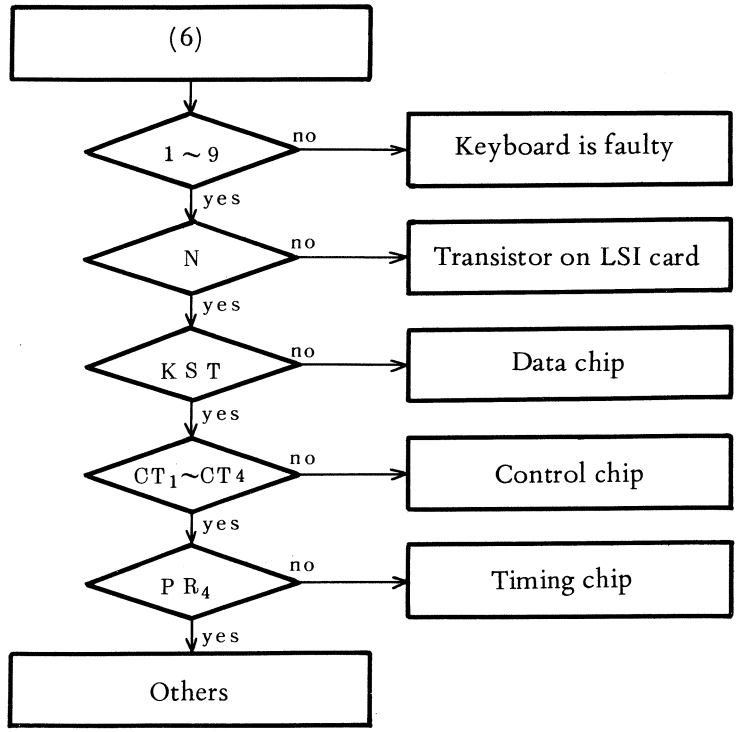


Fig. 6-31 Trouble Shooting Flow Chart

In this case, two cases may be considered, that is, operation does not return to CC0 by the key keeping pressed, and other is that overflow occurs when the first key is pressed.

i) Check 1 ~ 9 & N signal.

1 ~ 9 key signals are "1" (GND) when no key is pressed, but respective key signals become "0" when certain key is pressed.

ii) After checking KST signal, check CT1 ~ CT4 signal level by triggering KST.

iii) Check PR4 signal which is "0" or "1" after [C] key is pressed.

If PR4 signal is "0", it becomes "1" when a numeral key is pressed.

If PR4 signal is "1", it becomes "0" when a numeral key is pressed after a registration of the decimal point

(7) Wrong Numeral is Registers

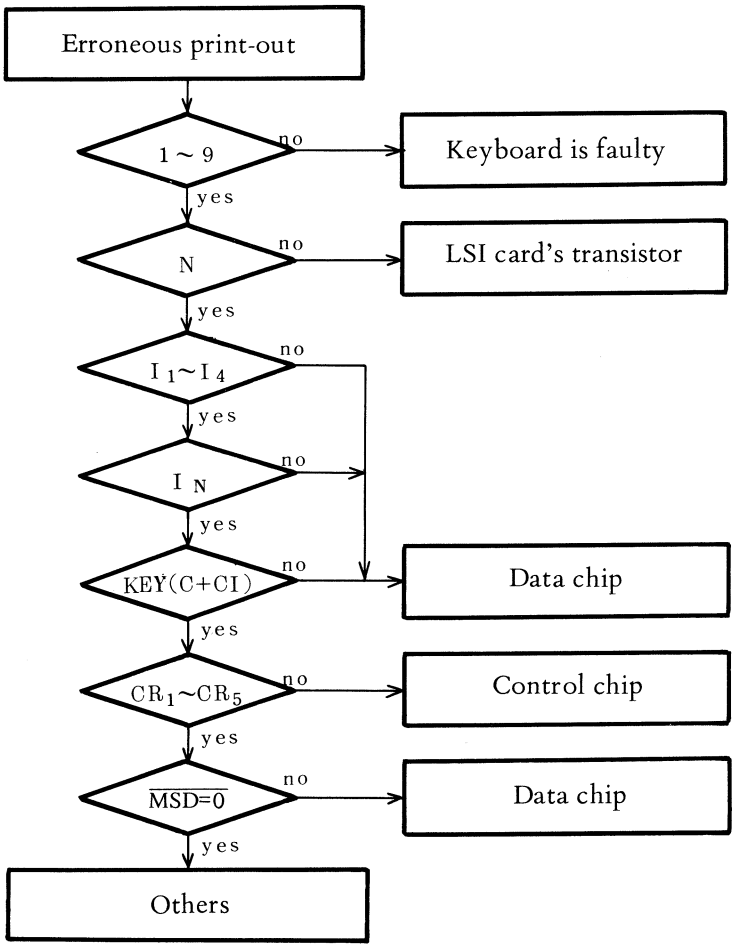


Fig. 6-32 Trouble Shooting Flow Chart

i) Check 1 ~ 9 & N key signals of the keyboard by triggering with SCT1.
1 ~ 9 & N signals are exactly the same with (6) case.

ii) Check I1 ~ I4 & IN signals by triggering with P0 signal.
Since SET-IR signal is emitted at the beginning of P1 time, then by referring to the key encoder pattern and observe the I1 ~ I4 & IN signals after determining the start position of P1 on the cathode ray tube.

iii) Check KEY(C+CI) signal by triggering with KST.
KEY(C+CI) signal becomes "1" when [C] or [CI] key is pressed.

vi) Check $CR_1 \sim CR_5$ signals.

v) $\overline{MSD=0}$ signal becomes "1" when there are 9 integer digits or 5 fractional digits registration.

(8) Dot Lacking in Pattern

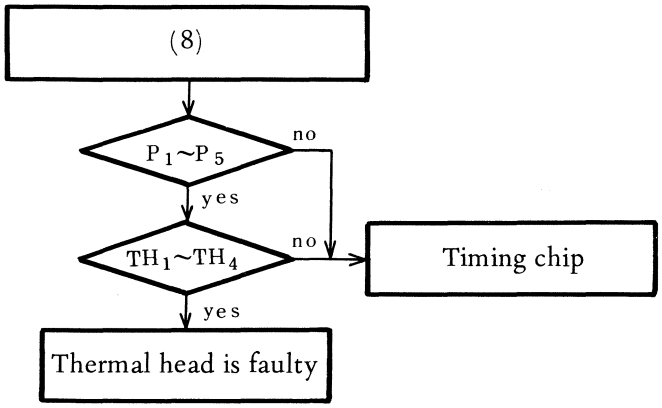


Fig. 6-33 Trouble Shooting Flow Chart

If $P_1 \sim P_5$ & $TH_1 \sim TH_4$ signals are normal when check then referring to the timing chart of Fig. 6-18 then the thermal head is faulty.

(9) Too Many Dots

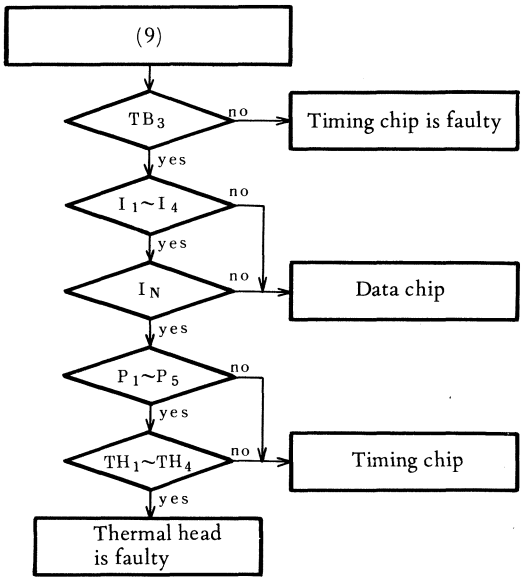


Fig. 6-34 Trouble Shooting Flow Chart

i) Check TB_3 pulse by triggering with TD_{12}.

ii) Check $I_1 \sim I_4$ signals by the same procedures with (7).

iii) Check $P_1 \sim P_5$ & $TH_1 \sim TH_4$ signals by the same procedures with (8).

iv) If above items are normal, the thermal head is faulty, however if it is abnormal, always same dot position is missed.

(10) Miscalculation

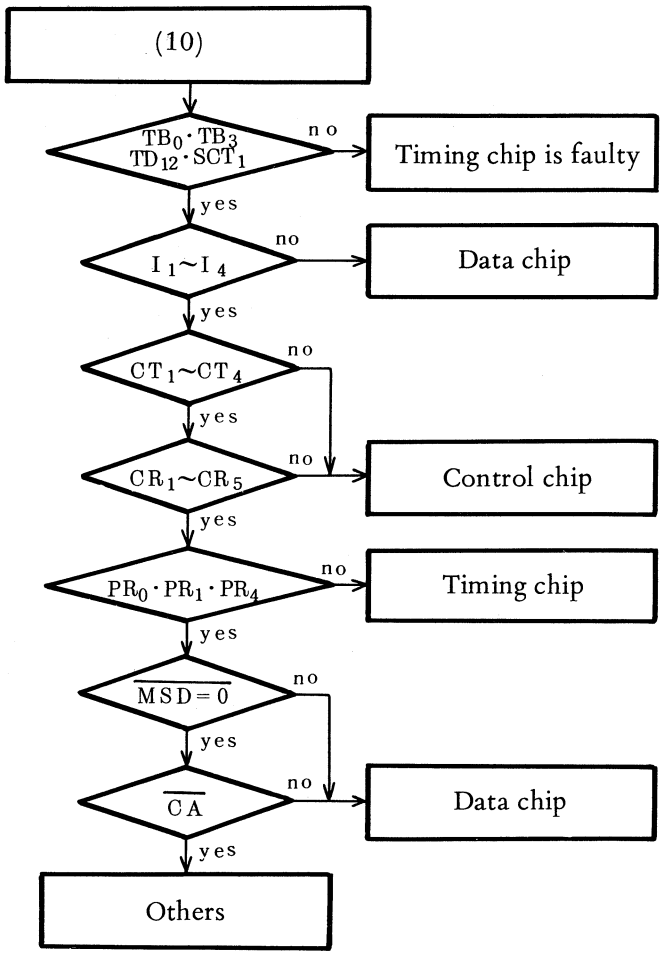


Fig. 6-35 Trouble Shooting Flow Chart

i) Check TB_0, TB_1, TD_{12} & SCT_1 clock pulses.

ii) If $I_1 \sim I_4$ signals are no good, then it can be found out the cause in the registration, however, sometimes these symptoms will be occured only during calculation operation, so check $I_1 \sim I_4$ by the same way with (7).

iii) Check PR_0, PR_1 & PR_4 signal in registration.

iv) Check $\overline{MSD=0} \cdot \overline{CA}$ (See Table 6-8)

(11) Certain key does not register

In this case, the wiring of the keyboard, the other related wiring and its signal must be checked first.

6.5 Service Tips

NOTE: i) Always switch OFF the POWER.

ii) Check to see that all tools, soldering iron and metal strip of the work bench are all grounded well.

iii) Serviceman should always neutralize his electrostatic charge before handling or servicing any equipment.

6.5-1 LSI's

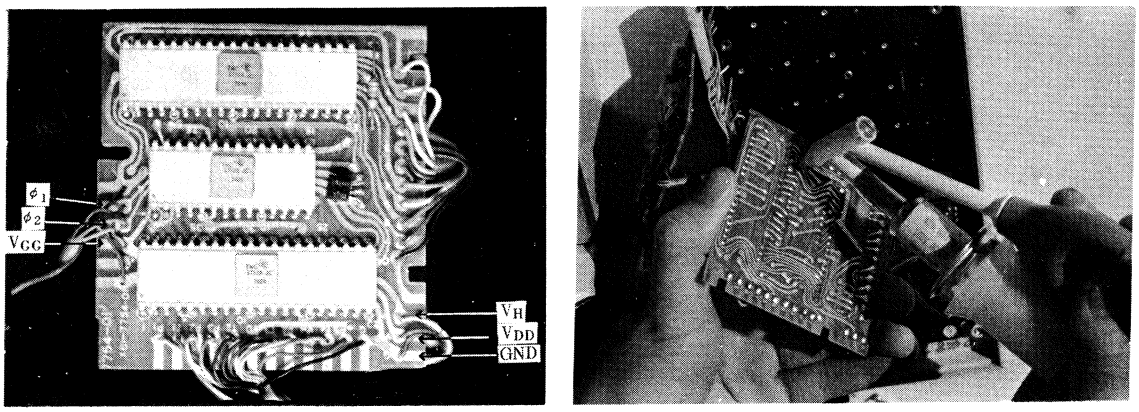


Fig. 6-36 LSI Replacement

(1) Remove V_H (orange), V_{DD} (purple) & GND (green) wires from their terminal, so as to prevent any damage to the LSI & thermal head.

Be careful that there is no bridging of the terminals when removing the solder of the connections.

(2) There are always two long pins bent into the pattern which are inserted diagonally to each other so as to hold the LSI in position for soldering; these two pins must be first straightened out before removing the LSI from the card.

(3) Use suction type soldering iron when unsoldering the pins of the LSI to prevent any bridging and to have a clean pin hole. Place the soldering tip to the soldered pin until the solder starts to melt and then suck in the melted solder.

(4) After unsoldering all the pins, take a sharp pointed tweezers and check whether the ends of the pins are loosened from the card or not.

(5) Check to see that all pinholes are clean.

(6) The two long pins for holding a new LSI in position should protrude about 3 ~ 4mm from the card. Bend & solder them.

Solder all pins and then cut off the excessive ends of the pins.

6.5-2 Thermal Head

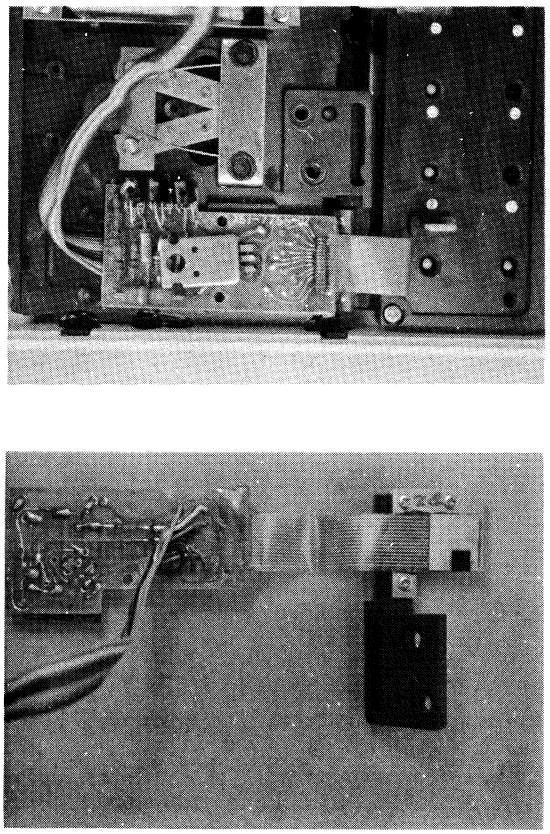


Fig. 6-37 Thermal Head Unit Replacement

(1) Remove the screw and space screw that hold the discrete & LSI cards.

(2) Unsolder the ribbon wire from the LSI card terminals.

(3) Remove the thermal head bracket and AVR printed board.
Be careful that thermal head is not scratched or chipped when removing it.

(4) Remove the three retaining screws of the thermal head.

6.5-3 Keyboard & Keytop

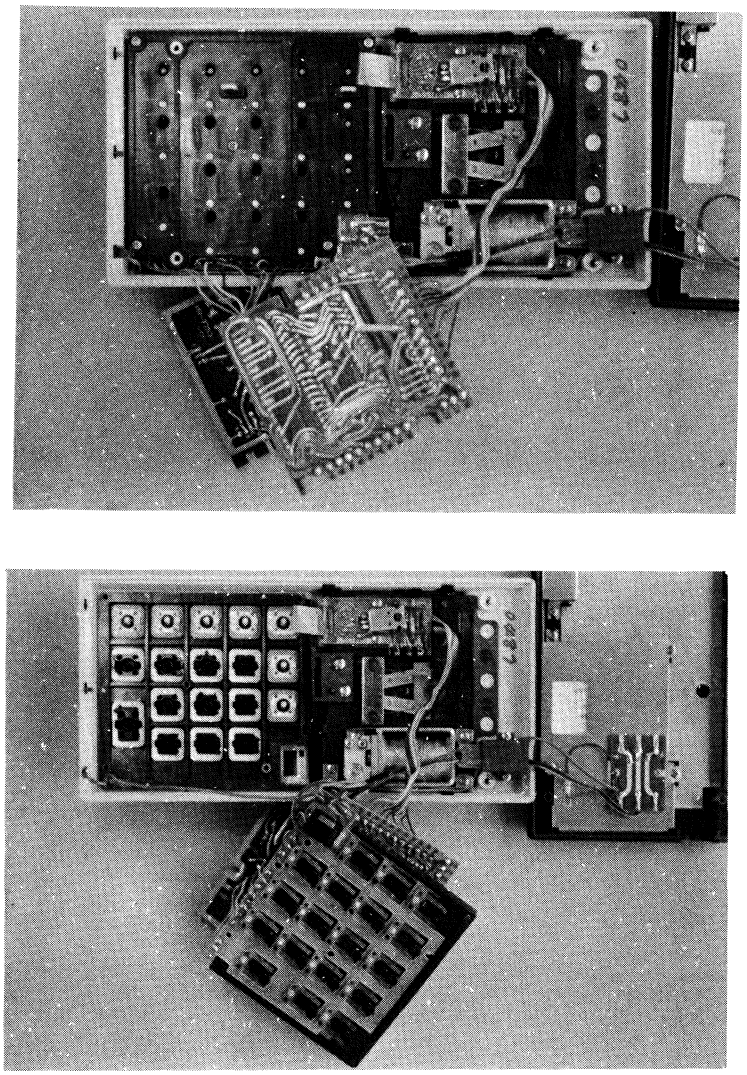


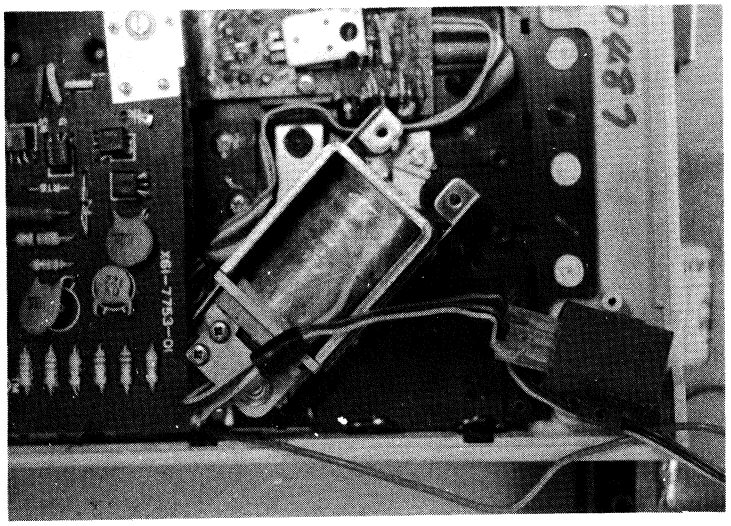
Fig. 6-38 Keyboard Unit Replacement

(1) Remove the screw and space screw.

(2) Remove the fine retaining screw of the keyboard. When removing the keyboard always have the Keytops facing downwards.

(3) The key contacts are spot-welded to the keyboard, so if any key contact is damaged, the keyboard unit must be replaced.

6.5-4 Solenoid



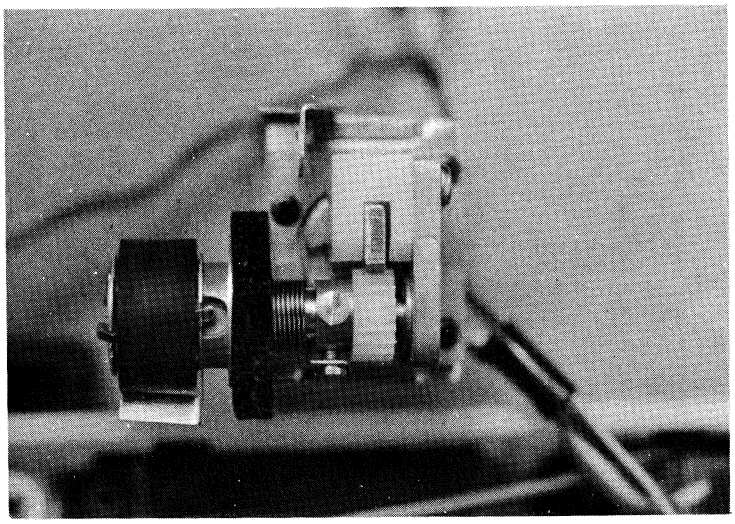


Fig. 6-39 Solenoid & Roller Unit Replacement

(1) After removing the three retaining screws, turn the solenoid coil inward and then lift it upward.

(2) Before removing the feed roller unit, spot mark the gear to the side of the bracket, then unscrew the three retaining screws at the top of the solenoid coil.

(3) Be sure that the spot mark are in alignment when attaching it to the solenoid coil, or else the print-out is not in the proper viewing position.

6.5-5 Feed Roller

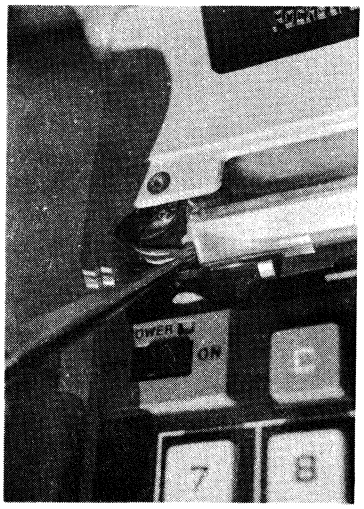


Fig. 6-40 Tear off the Paper

(1) When the paper wraps around the roller.

i) Remove the hood assembly by unscrewing the pinface screw.

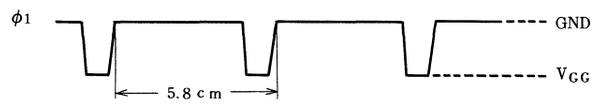
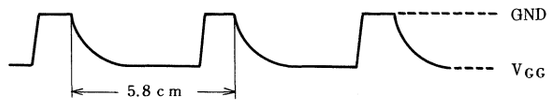
ii) With a tweezers, tear off the paper wound around the roller.

(2) When the paper slips on the roller.

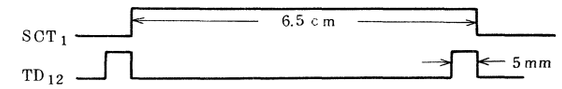
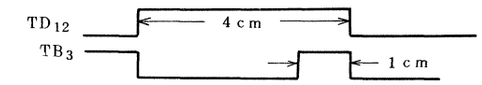
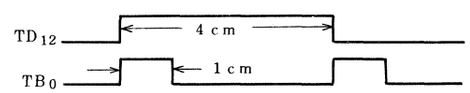
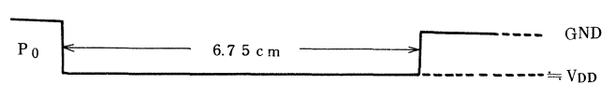
i) Take a damp cloth and wipe the roller thoroughly until all of the coating substance is cleared.

Table 6-8 Signal Check Sheet (1)

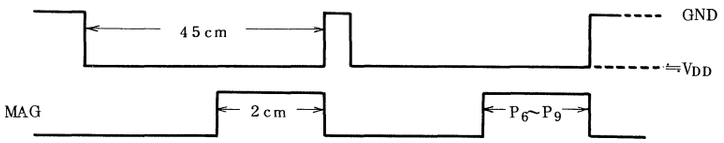
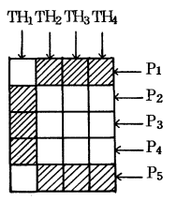
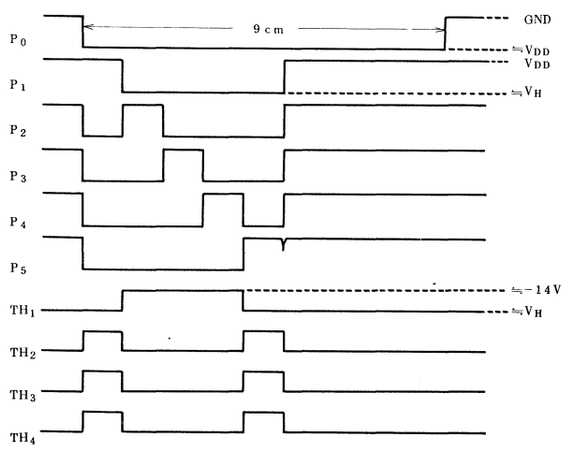
Pin No.	Signal	Source	Destination	Oscilloscope			Voltage Range	Function of Signal	Waveform Observation
				Trigger	V/cm	sec/cm			
C·C 3	I_1	D·C	T·C 36 D·C 4	ϕ_1	.5	.5m	V_{DD} ↔ GND	Weight of 1 of 8-4-2-1 key encoder.	Becomes "1" when [1], [3], [5], [7], [9], [+], [−], [×] or [c] is pressed, and in IR·PR_1 → BR & IR → IR operations, flickers of "0" signals appear; but when any other key is pressed, it remains "0" with flickers of "1" signals appearing in IR → IR operations.
C·C 4	I_N	D·C	T·C 36 T·C 5	ϕ_1	.5	.5m	V_{DD} ↔ GND	Discriminate numeral from order keys.	Becomes "1" when [0] [9] is pressed & [=] for print-out; but becomes "0" when any other key is pressed.
C·C 5	SCT_1	T·C	T·C 25 D·C 18	SCT_1	.5	.5m	V_{DD} ↔ GND	52-bit time	Length of SCT_1 is (CP) 28.85 μsec x (bit) 4 x (digit) 13 = 1500·2 [μsec]. 1.5 [msec] ÷ 0.5 [msec/cm] = 3 [cm] 
C·C 6	PR_0	T·C	T·C 27	ϕ_1	.5	.5m	V_{DD} ↔ GND	PR signal becomes "1" when point register is 0.	PR is "0" or "1" when switched ON. When PR_0=1 and numeral key is pressed after [c], it becomes PR_4 with PR_0 being "0". When PR_0 and [·][1][2][3][4] are pressed after pressing [c], then PR_0 becomes "1". During PR → PR and PR operation in calculation, flickers of "1" signals appear.
C·C 7	PR_4	T·C	T·C 28	ϕ_1	.5	.5m	V_{DD} ↔ GND	PR signal becomes "1" when point register is 4.	When PR signal is "1" and [·][1] are pressed after [c], then PR_4 becomes "0". When PR signal is "0" and numeral key or keys are pressed after [c], PR_4 is "1", but as soon as [·] with numeral key are pressed, PR_4 becomes "0".
C·C 8	GND	Power Supply	T·C 10 D·C 27	Free Running	.5		OV	Ground	Confirm the ground level of GND, then check DC.
C·C 9	V_{DD}	Power Supply	T·C 20 D·C 10, 26	Free Running	.5		−7.5V±10%	Drain voltage of LSI	Same as checking for GND.
C·C 10	CT_4	C·C	T·C 33	ϕ_1	.5	2m	V_{DD} ↔ GND	Timing Chip control signal	Normal is "0", but flickers of "1" when 1st numeral is entered or [=] is pressed in multiplication or division.
C·C 11	CT_3	C·C	T·C 32	ϕ_1	.5	20m	V_{DD} ↔ GND	Timing Chip control signal	Normal is "1", but flickers of "0" when any key is pressed. Remains "0" when key is held down, but becomes "1" when released.
C·C 12	CT_2	C·C	T·C 31	ϕ_1	.5	20m	V_{DD} ↔ GND		Same as CT_3.
C·C 13	CT_1	C·C	T·C 30	ϕ_1	.5	20m		Timing Chip control signal	Normal is "0", but flickers of "1" when any key is pressed. When [=] is pressed in multiplication or division, waveform of 0-1-0-1 appear; but during print-out it is "1" and becomes "0" when it ends.
C·C 14	CR_1	C·C	D·C 17	ϕ_1	.5	20m	V_{DD} ↔ GND	Data Chip control signal	Normal is "1", but flickers of "0" when any key is pressed and remains "0" if key is held down, but becomes "1" if released. In multiplication or division, when [=] is pressed, waveform of 0-1-0-1 appear, but during print-out it is "0" and becomes "1" when it ends.

Pin No.	Signal	Source	Destination	Oscilloscope			Voltage Range	Function of Signal	Waveform Observation
				Trigger	V/cm	sec/cm			
C·C 15	CR_2	C·C	D·C 16	$\phi 1$	.5	20m	$V_{DD} \leftrightarrow$ GND	Data Chip control signal	Normal is "0", but CC_{14}·SCT_1 appears when [C] is pressed & flickers of "1" when [÷][×][+][−] or [=] is pressed; but is "0" during print-out & when any of other keys is pressed.
C·C 16	CR_3	C·C	D·C 15	$\phi 1$	.5	20m	$V_{DD} \leftrightarrow$ GND	Data Chip control signal	Normal is "1", but flickers of "0" appear when any key is pressed. During calculation & print-out is "0" with flickers of "1". CC_{14}·SCT_0 appears when [C] is pressed. When key is held down it is "0"; but becomes "1" when released.
C·C 17	CR_4	C·C	D·C 14	$\phi 1$	.5	20m	$V_{DD} \leftrightarrow$ GND	Data Chip control signal	Normal is "0", but CC_{14}·SCT_0 appears when [C] is pressed. When [CI], [=] or numeral key is pressed, flickers of "1" appear; but when other keys is pressed, it is always "0".
C·C 18	CR_5	C·C	D·C 13	$\phi 1$	.5	20m	$V_{DD} \leftrightarrow$ GND	Data Chip control signal	Normal is "1", but flickers of "0" appear when key is pressed. When key is held down, it is "0", but becomes "1" when released.
C·C 19	$\phi 1$	OSC	T·C 18 D·C 12	$\phi 1$	.5	5μ	$V_{GG} \leftrightarrow$ GND	Shift clock pulse	Check frequency of $\phi 1$. Each printing time of $P_1 \sim P_5$ must be adjusted at 15msec. $\frac{15000}{5(TX) \times 2(SCT) \times 13(digit) \times 4(bit)} = 28.85\ [\mu sec]$ $\frac{28.85\ \mu sec}{5\ \mu sec/cm} = 5.77\ [cm]$ 
C·C 20	$\phi 2$	OSC	T·C 19 D·C 11	$\phi 1$	.5	5μ	$V_{DD} \leftrightarrow$ GND	Shift clock pulse	Check frequency of $\phi 2$ which is the same as $\phi 1$. 
C·C 21	SP-CC	T·C	T·C 21	$\phi 1$	.5	.2m	$V_{DD} \leftrightarrow$ GND	Triggers J-K flip-flop in control chip. Emitted at end of P_9 or SCT_1 (sometime at SCT_0)	Flickers of "1" appear when a key is pressed or during calculation cycle. Check to see if it stops at CC_1 and SP-CC continuously appears when key is held down.
C·C 22	V_{GG}	Power Supply	T·C 29 D·C 28	Free Running	.5		−12.4 ↔ −16V	Gate voltage of LSI (MOS FET)	Check it the same way as for GND.
C·C 23	$\overline{MSD=0}$	D·C	D·C 9	$\phi 1$	.5	.2m	$V_{DD} \leftrightarrow$ GND	Check if data in 13th digit of UA or BR.	Normal is "0", but becomes "1" if data enters 13th digit of BR at CR_3=1 or when data enters 13th digit of UA at CR_3=0. In entry overflow or underflow such as [1][2][3][4][5][6][7][8][9] or [·][1][2][3][4][5], it becomes "1".
C·C 24	$\overline{CA}$	D·C	D·C 8	$\phi 1$	.5	.2m	$V_{DD} \leftrightarrow$ GND	Carry in addition or borrow in subtraction	Normal is "1". Press [1][+][1][+] and check to see that carry is not emitted at the first [+]; but when second [+] is pressed, it becomes "0".
C·C 25	KST	D·C	D·C 7	$\phi 1$	.5	.2m	$V_{DD} \leftrightarrow$ GND	Indicate key is held down	Becomes "1" when any key is pressed, but becomes "0" when key is released.
C·C 26	KEY (C+CI)	D·C	D·C 6	$\phi 1$	.5	.2m	$V_{DD} \leftrightarrow$ GND	Indicates [C] or [CI] is held down	Becomes "1" when [C] or [CI] is pressed, but becomes "0" when it is released. In calculation overflow, flickers of "0" appear.

Check Sheet (3)

Pin No.	Signal	Source	Destination	Oscilloscope			Voltage Range	Function of Signal	Waveform Observation
				Trigger	V/cm	sec/cm			
C·C 27	I_2	D·C	D·C 37 D·C 3	ϕ_1	.5	.2m	V_{DD} ↔ GND	Weight of 2 of 8-4-2-1 key encoder	When [2] [3] [6] [7] [=] [−] [·] or [C] is pressed, it becomes "1"; but when [=] is pressed, flickers of "1" appear since data of IR is transferring.
C·C 28	I_3	D·C	T·C 38 D·C 2	ϕ_1	.5	.2m	V_{DD} ↔ GND	Weight of 4 of 8-4-2-1 key encoder	When [4] [5] [6] [7] [÷] [×] [·] or [C] is pressed, it becomes "1". When any other key is pressed, flickers of "1" appear since data of IR is transferring.
D·C 1	I_4	D·C	T·C 39	ϕ_1	.5	.2m	V_{DD} ↔ GND	Weight of 8 of 8-4-2-1 key encoder	When [8] [9] or [CI] is pressed, it becomes "1". When any other key is pressed, flickers of "1" appear since data of IR is transferring.
D·C 19	TD_{12}	T·C	T·C 24	SCT_1	.5	.2m	V_{DD} ↔ GND	Indicates 4-bit (1 digt) time or 13th digit	Set SCT_1 width of 6.5 cm.  TD_{12} should appear 5mm before end of SCT_1.
D·C 20	TD_3	T·C	T·C 23	TD_{12}	.5	20μ	V_{DD} ↔ GND	Indicates 1-bit time & weight of 8-4-2-1 code	Set TD_{12} width to 4 cm.  TB_3 should appear 1 cm before end of TD_{12}.
D·C 21	TB_0	T·C	T·C 22	TD_{12}	.5	20μ	V_{DD} ↔ GND	Indicate 1-bit time & weight of 1 of 8-4-2-1 code	Set TD_{12} width to 4 cm.  TB_0 should appear at beginning of TD_{12} and be the length of 1 cm.
D·C 24	P_0	T·C	T·C 2	P_0	.5	20m	V_{DD} ↔ GND	Time when not printing or transporting of tape	Check time of P_1 ~ P_9 which should be 135 [msec] since P_1 is 15 [msec]. 15 x 9 = 135 [msec] $\frac{135\ [msec]}{20\ [msec/cm]} = 6.75\ [cm]$  Normal is "1"; but when print-out of transport, it is "0".

Check Sheet (4)

Pin No.	Signal	Source	Destination	Oscilloscope			Voltage Range	Function of Signal	Waveform Observation
				Trigger	V/cm	sec/cm			
D·C 25	PR1	T·C	T·C 26	ϕ1	.5	20μ	VDD ↔ GND	Indicates second position of point register (PR1)	When power is switched ON, it is "1" or "0". If it is "1", then after [C] operation, in first numeral registration it performs 4→PR and becomes "0". If "0" and [·] [1] [2] 3 are pressed after [C], then PR1 becomes "1".
D·C 29	N	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Discriminates between numeral and [·] or order key.	Normal is "1" and becomes "0" when numeral key is pressed.
D·C 30	9	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [9] is pressed	Normal is "1" and becomes "0" when [9] is pressed.
D·C 31	8	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [8] or [CI] is pressed	Normal is "1" and becomes "0" when [8] or [CI] is pressed.
D·C 33	7	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [7] or [C] is pressed	Normal is "1" and becomes "0" when [7] or [C] is pressed.
D·C 34	6	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [6] or [·] is pressed	Normal is "1" and becomes "0" when [6] or [·] is pressed.
D·C 35	5	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [5] or [×] is pressed	Normal is "1" and becomes "0" when [5] or [×] is pressed.
D·C 36	4	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [4] or [÷] is pressed	Normal is "1" and becomes "0" when [4] or [÷] is pressed.
D·C 37	3	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [3] or [−] is pressed	Normal is "1" and becomes "0" when [3] or [−] is pressed.
D·C 38	2	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [2] or [=] is pressed	Normal is "1" and becomes "0" when [2] or [=] is pressed.
D·C 39	1	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [1] or [+] is pressed	Normal is "1" and becomes "0" when [1] or [+] is pressed.
D·C 40	1	KB	KB	ϕ1	.5	20μ	VDD ↔ GND	Indicates [0] is pressed	Normal is "1" and becomes "0" when [0] is pressed.
T·C 1	MAG	T·C		P0	.5	20m		Activates solenoid	Set P0 pulse width to 4.5 cm.  MAG should appear 2 cm before end of P0 for the time of P6 ~ P9.
T·C 3	P1	T·C	T·H	P0	.5	10m	VDD ↔ VH	 Print pattern of [C]	Set P0 pulse width to 9 cm. Press [C] 
T·C 4	TH1	T·C	T·H	P0	.5	10m	−14V ↔ VH		
T·C 7	P2	T·C	T·H	P0	.5	10m	VDD ↔ VH		
T·C 8	P3	T·C	T·H	P0	.5	10m	VDD ↔ VH		
T·C 9	TH2	T·C	T·H	P0	.5	10m	−14V ↔ VH		
T·C 11	P5	T·C	T·H	P0	.5	10m	VDD ↔ VH		
T·C 12	TH4	T·C	T·H	P0	.5	10m	−14V ↔ VH		
T·C 14	P4	T·C	T·H	P0	.5	10m	VDD ↔ VH		
T·C 15	TH3	T·C	T·H	P0	.5	10m	−14V ↔ VH		

BATTERY CHARGER 10A · 20A

Canon Hi-Speed Battery Charger 20A

1. General

1.1 Appearance

Fig. 1-1 Appearance

1.2 Introduction

Battery Charger 10A or Hi-Speed Battery Charger 20A may be used in charging the nickel-cadmium battery of the Pocketronic.

Battery Charger 10A is the conventional type charger which takes approximately 5 times longer than the Hi-Speed Battery Charger 20A.

Hi-Speed Battery Charger 20A has an overcharge protect switch circuit with a rapid charging system. Thus, a rapid charge with the charging current being automatically controlled to prevent an overcharge, and also, the Pocketronic being operatable while it is being charged.

These are the principal features of this Hi-Speed battery charger.

The CHARGE pilot lamp indicates whether the battery is being charged or fully charged.

2. Specifications

2.1 General Specifications

Power:	AC 100V, 110～120V & 220～240V (by Voltage Selector) 50/60Hz
Power Consumption:	7VA
DC Output:	8.5V, 150mA 10.0V, 110mA
Battery:	NiCd Battery NR-AA ..... 6 pcs. NR-2/3AA .... 7 pcs.
Charging Time:	Approx. 3～5 hours
Temperature:	0°C～40°C

2.2 Characteristics

Battery Voltage at End of Charge:

Temp.	NR-AA(x6)	NR-2/3AA(x7)
0°C	8.6～8.9V	10.1～10.45V
20°C	8.6～8.8V	10.1～10.3V
40°C	8.35～8.7V	9.8～10.2V

Charging Current:	A circuit (NR-AAx6) 110～170mA B circuit (NR-2/3AAx7) 90～130mA
Charging Time and Capacity (at 20°C):	Capacity after 5 hours charge .... 80% Capacity after 10 hours charge 85%
Noise (1μV/m ..... 0dB):	150KHz ..... 50dB max. 500KHz ..... 40dB max. 5MHz ～ 30MHz .. 26dB max.

3. Operation Principle

This battery charger is one type of a relay circuit which is developed for controlling both the opening and closing of the circuit between the power source and applied load. This is done by discriminating the input signals.

Being a chemical reaction power source, the battery generates hydrogen gas during charging and discharging alike, and the volume of gas increases when it is overcharging. But, the battery itself is so constituted to absorb or release the gas to prevent damaging the battery.

Since a rapid charge is carried out by a current which is a few times larger than that for ordinarily charging a battery; thus, an overcharge protector is incorporated in this charger to control the gas it generates.

When the battery voltage Ein increases to EH_1, Tr_1 is ON and Tr_2 & Tr_3 are OFF with the load circuit being closed; but when Ein decreases to EH_2, then Tr_2 & Tr_3 become ON. There is a hysteresis characteristics between EH_1 & EH_2.

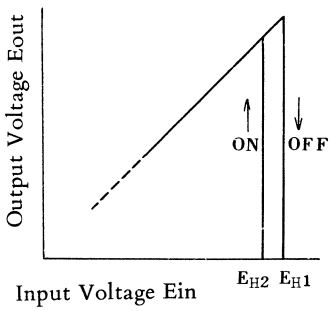


Fig. 3-1 Graphic Illustration of the Characteristics of Upper Limit Voltage Switch Circuit

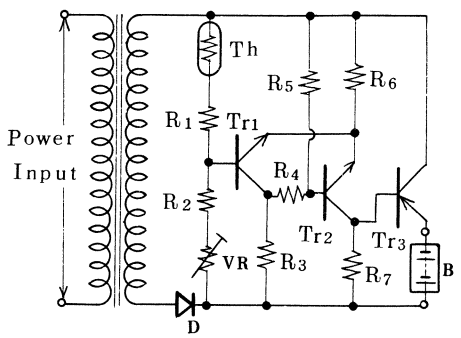


Fig. 3-2 Battery Charger Circuit

When the battery voltage Ein drops to EH_2, the battery is charged with relatively large current; but when Ein rises to EH_1, the charging stops. Thus, the switch circuit turns ON and OFF alternately.

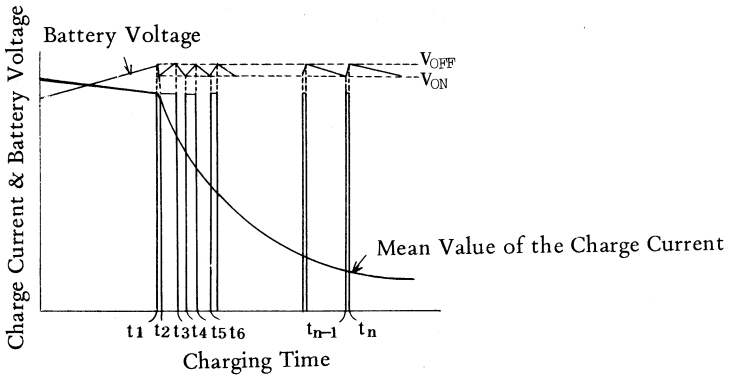


Fig. 3-3 Graphic illustration of the performance characteristics of the battery charger upper limit voltage switch circuit

Thus, the charge current flows intermittently into the battery. As shown in the Fig. 3-3, the mean value of the charge current decreases as the charging proceeds.

The charge lamp flickers since the charge current flows in intermittently. The lamp keeps on flickering but grows dimmer towards the end of the charging time.

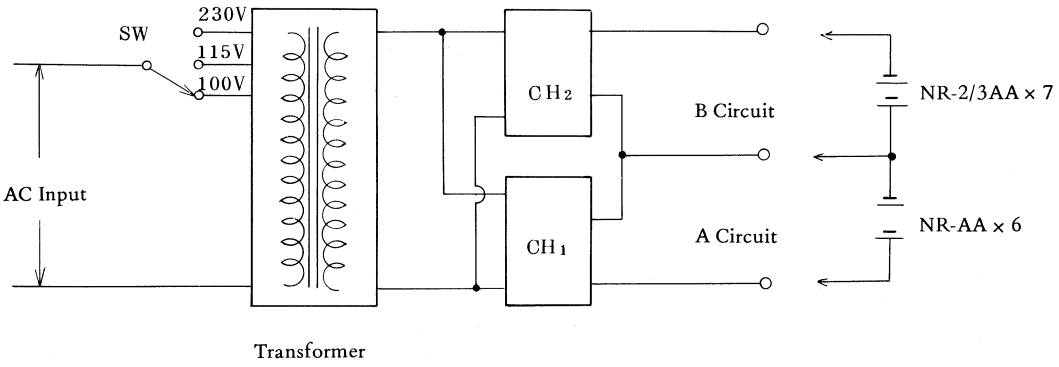


Fig. 3-4 Charging Circuit

The NR-2/3AA's in the B circuit & NR-AA's in the A circuit are alternately charged by half of an AC cycle due to the CH_2 & CH_1 voltage switch circuits respectively.

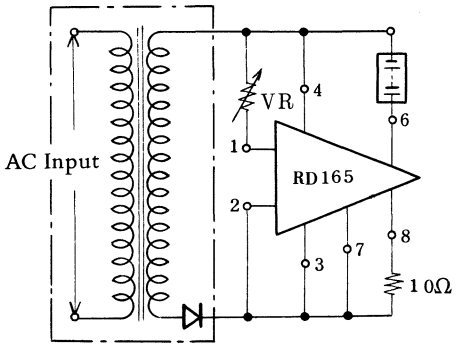


Fig. 3-5 Voltage Switch Circuit

This charger has an IC voltage switch circuit as shown in Fig. 3-5; thus two IC's are used —— one for the A circuit and the other for the B circuit.

4. Service Tips (for Charger 20A)

4.1 Circuit Diagram

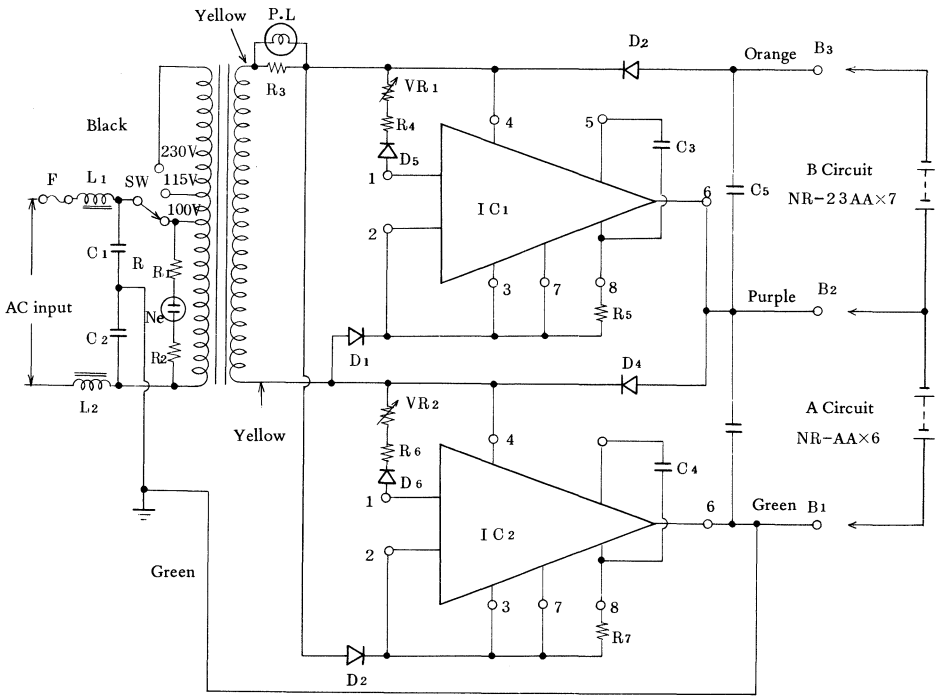


Fig. 4-1 Circuit Diagram of Hi-Speed Battery Charger 20A

The upper limit voltage is preset at a precise optimum level of a determined temperature range at the factory; therefore never try to adjust the variable resistor (VR), unless special equipments are used in temperature controlled condition.

4.2 Disassemble

4.2-1 Removal of Top Cover

Unscrew the 4 retaining screws at the bottom of the charger to remove the top cover.

4.2-2 Removal of Chassis

Remove 3 screws to detach the chassis from the casing.

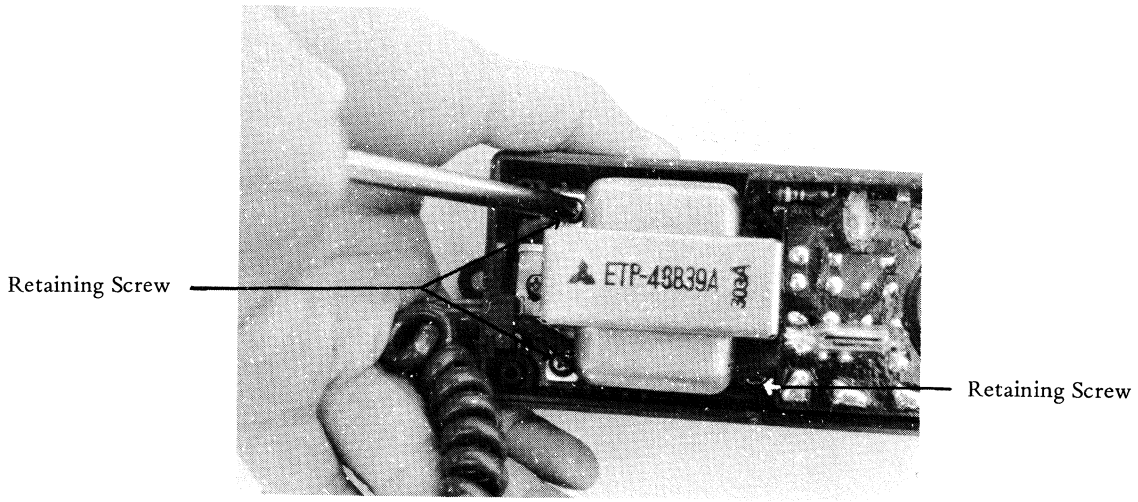
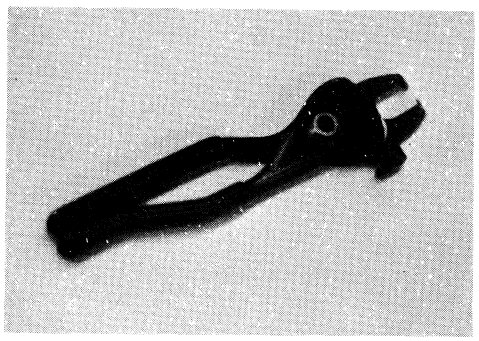


Fig. 4-2 Removal of Chassis

4.2-3 Removal of AC Cord

Remove cord strain relief bushing by using the special plier (cord bushing release plier). Then unsolder the cord terminals.



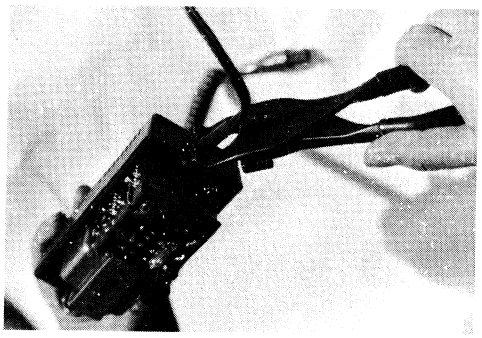


Fig. 4-3 Plier or Removing AC Cord

4.2-4 Removal of Printed Board

(1) Power Voltage Setting

This charger can be set for power supply voltage of 100V, 110～120V & 220～240V (50/60Hz).

(2) Replacing of Printed Board "A"

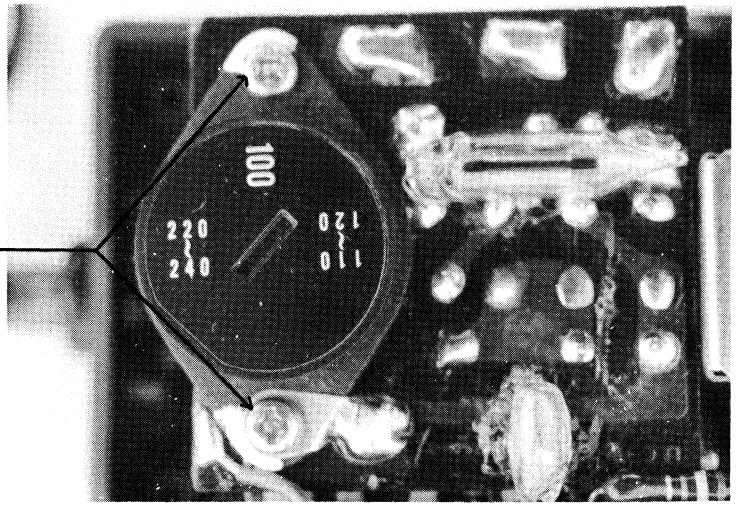


Fig. 4-4 Removal of Printed Board "A"

Remove 2 screws as illustrated in Fig. 4-4 to take out Printed Board "A".

Unsolder the white, blue, gray, black & brown lead wires of the transformer, the green ground wire and the AC cord.

When any component of printed board "A" is replaced, no adjustment of the upper limit charge voltage is required.

4.2-5 Replacing Printed Board "B"

Never replace any faulty component on the printed board "B"; because special equipments under certain conditions are necessary to make the proper adjustments.

Replace it with a new printed board "B" unit which requires no adjusting, and send the faulty printed board back to the company for repairs.

Battery Charger 10A

1. General

1.1 Appearance

Fig. 1-1 Appearance

1.2 Introduction

This is a simple charger for charging as compared with Hi-Speed Battery Charger 20A. Battery Charger 10A has neither an overcharge protect circuit nor a power voltage selector.

2. Specifications

Charging Time:	14 ~ 20 hours
Power:	100V, 115V, 220V & 240V
Power Consumption:	2VA

Ambient Conditions Temp.:	0℃ ~ 40℃
Relative humidity:	90%
Dimensions:	50(W) x 50(D) x 49(H) mm
Weight:	200g

3. Circuit of Charger 10A

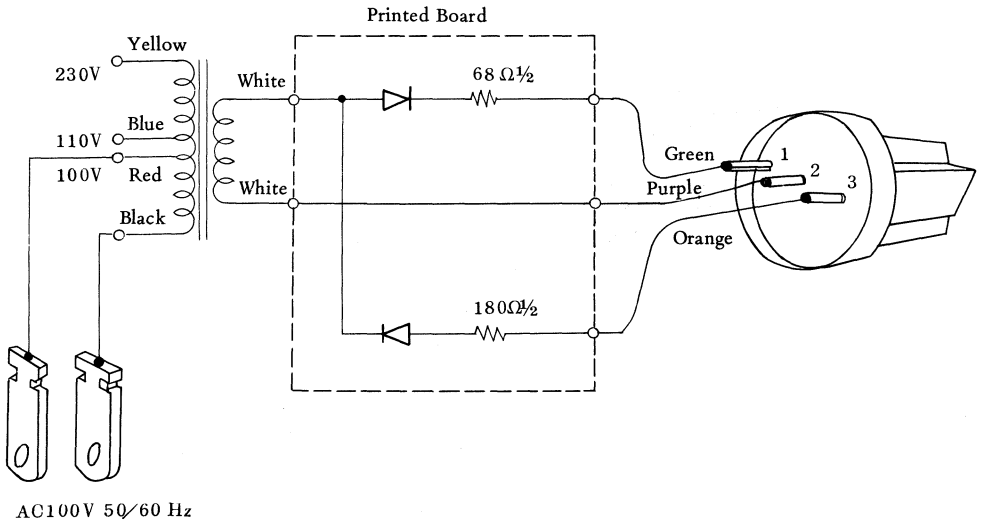


Fig. 3-1 Charging Circuit

OPERATING INSTRUCTION
FOR
POCKETRONIC CHECKER

Operating Instruction for Pocketronic Checker

The Pocketronic checker is used to check the 3 LSI's and the thermal head, and also the voltage margin of them in the field servicing of the Pocketronic.

The checking of the LSI and the thermal head by this checker are quite simple, that is, remove the doubtful LSI or thermal head from the Pocketronic, and then place it in the position where the flawless one is already inserted in the checker, so as to verify whether it is faulty or not by the calculating operations of the checker whether the checker can be operated correctly or not.

The built-in batteries with the Hi-speed charger 20A and pair of constant-voltage power sources are used in the checker for the internal and the external power supplies respectively.

1. Operation

1.1 How to Operate

(1) Turn off the POWER switch, and then connect the Hi-speed charger 20A to it to charge the built-in batteries. At this time, confirm if the "POWER" and "CHARGE" lamps light up.

(2) External power sources.

(i) Ground the output terminal "+" to "GND" of each constant-voltage power sources, and then connect "GND" terminals of both power sources.

(ii) Connect "–" of the right-hand power source to the V_H terminal of the checker as shown in Fig. 1.

(iii) Connect "–" of the left-hand power source to the V_{DD} terminal of the checker.

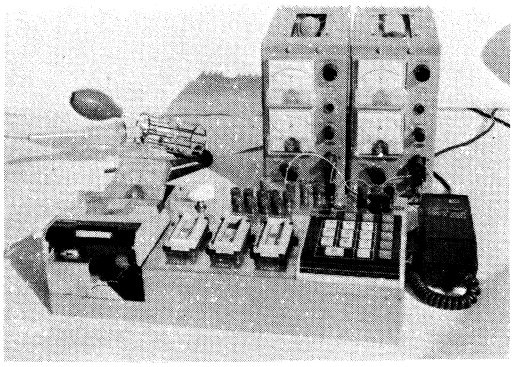


Fig. 1 Pocketronic Checker

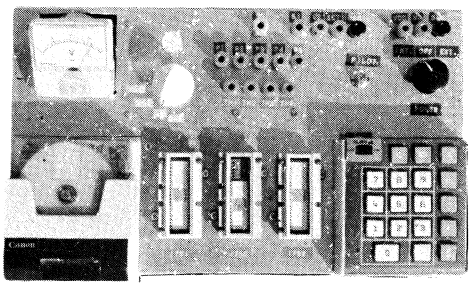


Fig. 2 Outer View

(3) Make sure 3 LSI's are properly inserted on the sockets. The LSI's must be set on the socket so as to coordinate the black dot of LSI with that of the carry.

(4) Insert the cartridge tape properly and set the power switch to "INT" position.

(5) Set the voltage meter selection switch to "V_H", "V_{GG}" and "V_{DD}" in sequence, and confirm their respective voltages.

After that, confirm whether calculations are properly done or not.

(6) Switch ON both power sources and set the voltages at 17.0V (V_H) and 7.5V (V_{DD}) by adjusting "VOLTAGE" knobs.

(7) Change the power switch to "EXT" to operate the checker by the external two power sources.

1.2 LSI Check

(1) Remove the doubtful LSI from the Pocketronic and thoroughly clean the LSI's prongs.

Do it as quickly as possible so as to prevent LSI from becoming overheated.

(2) After making sure the power switch is turned OFF (center position of the power switch), then remove the LSI from the checker to change with the doubtful LSI which has been used in Pocketronic.

(3) Set the LSI on the socket in such a way that the black dot of LSI coordinate the position of the black dot marked on the carry of the socket.

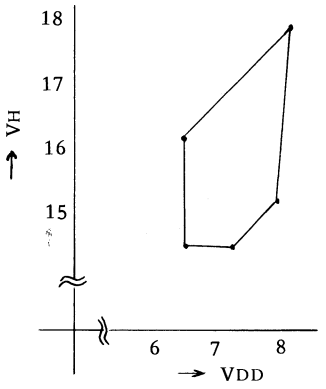
(4) Set the power switch to "INT", and then check the operation according to the operating check program sheet.

(See Pocketronic Operating Check Sheet.)

(5) If the checker operate properly, change the power switch to "EXT" to check the voltage margin of the LSI by referring with Table 1.

V_{DD}	V_H
−6.75V	−15.3V & −17.0V
−7.50V	−15.3V
−8.25V	−16.0V
−8.50V	−18.8V

Table 1. Voltage Margin



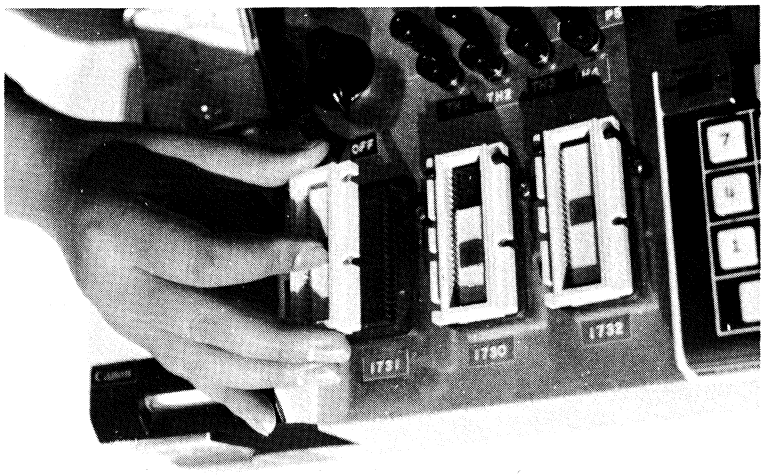


Fig. 3 Placing a LSI on the Socket

During this procedure, even though the thermal head has Automatic Voltage Regulator, never set the voltage over −19V.

(3) If the checker operates properly with the doubtful LSI, then the other LSI's must be checked in the same way.

1.3 Thermal Head Check

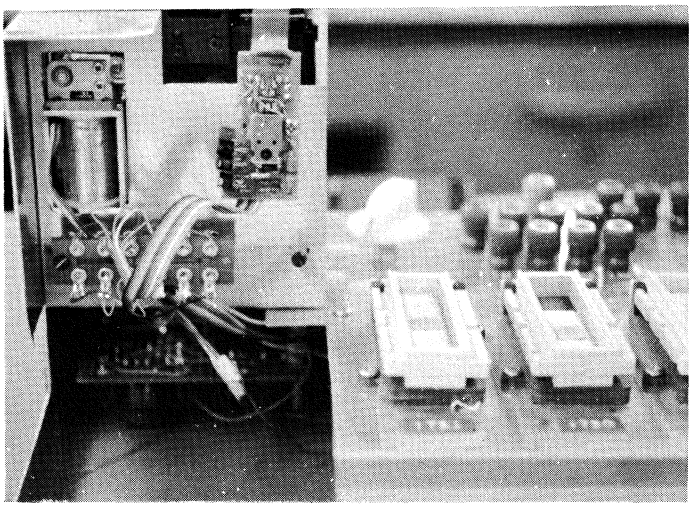


Fig. 4 Replacement of the Thermal Head

(1) Open the left-hand side of the chassis, and unsolder the wiring of the thermal head unit from the lug terminals, then remove the thermal head from the checker.

(2) Attach the faulty thermal head of the Pocketronic to the checker.

(3) Set the power switch to "INT", and then confirm the print-out by pressing [C1], [0] and [=], then all dots can be observed.

TPH Protector

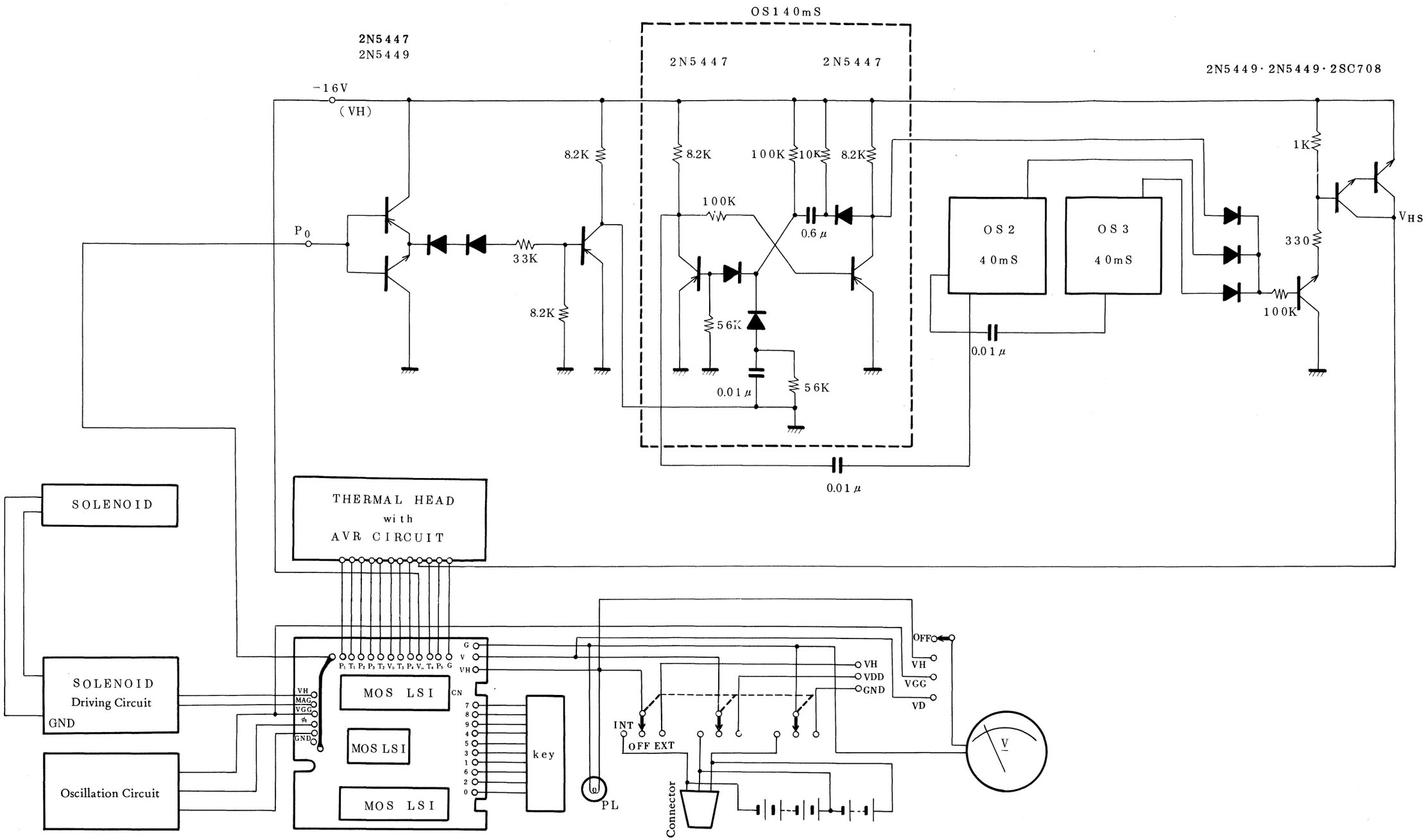
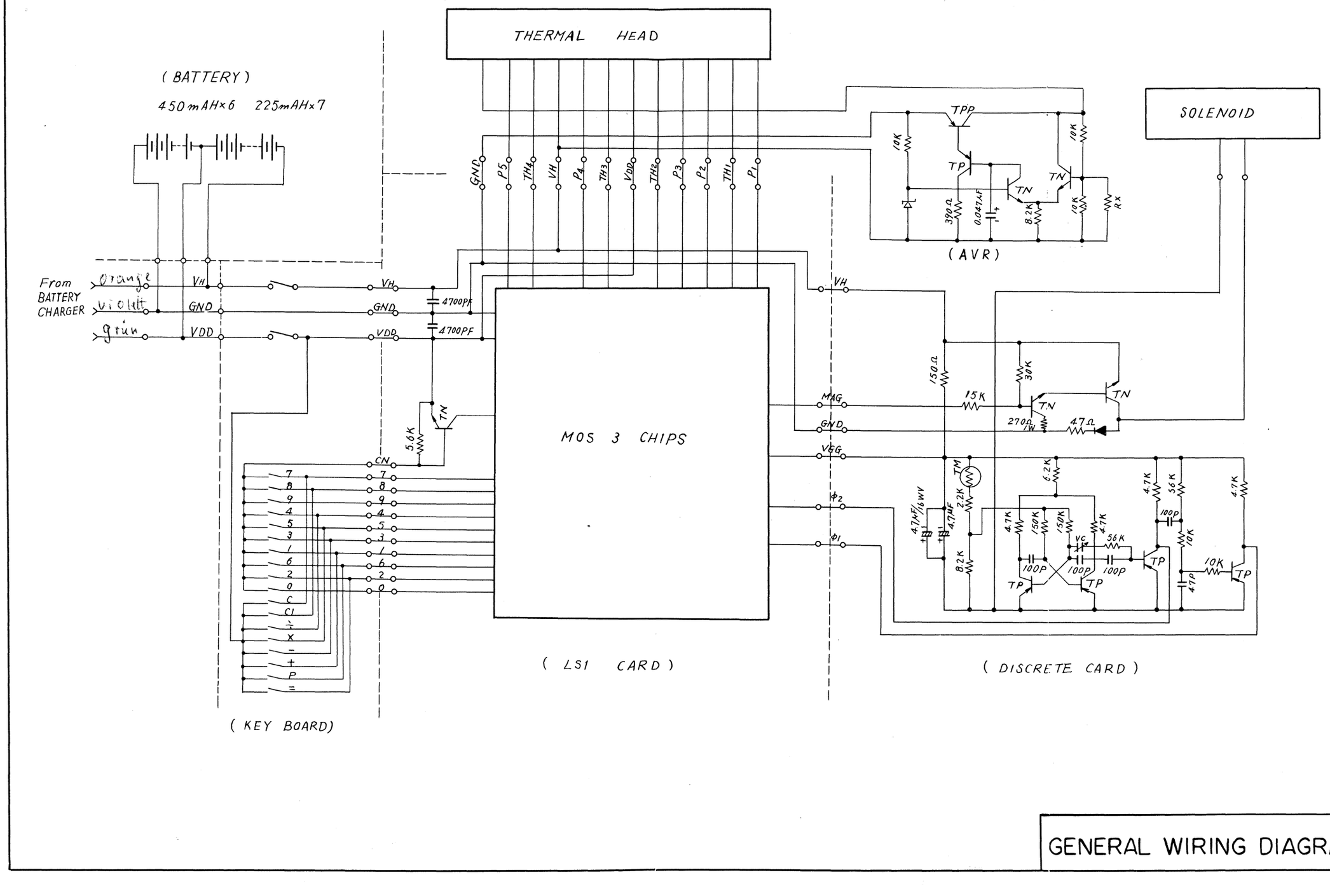
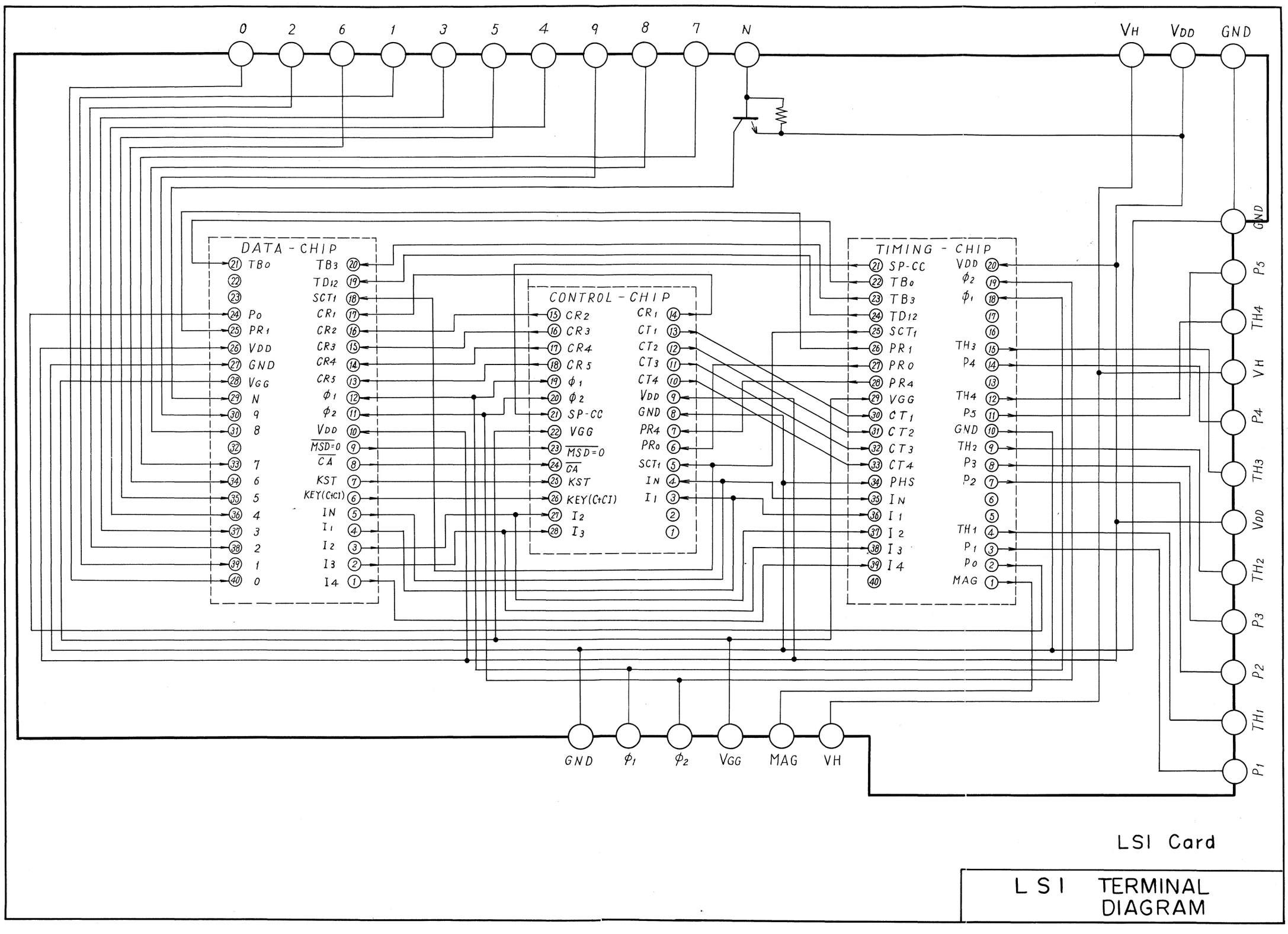


Fig. 5 Checker Circuit for Pocketronic

LOGIC & TIMING CHART



GENERAL WIRING DIAGRAM


0 2 6 1 3 5 4 9 8 7 N
VH VDD GND
DATA - CHIP
TB0 TB3 TD12 SCT1 CR1 CR2 CR3 CR4 CR5 φ1 φ2 VDD MSD=0 CA KST KEY(C+C1) IN I1 I2 I3 I4
P0 PR1 VDD GND VGG N 9 8 7 6 5 4 3 2 1 0
CONTROL - CHIP
CR2 CR3 CR4 CR5 φ1 φ2 SP-CC VGG MSD=0 CA KST KEY(C+CI) I2 I3
CR1 CT1 CT2 CT3 CT4 VDD GND PR4 PR0 SCT1 IN I1
TIMING - CHIP
SP-CC TB0 TB3 TD12 SCT1 PR1 PR0 PR4 VGG CT1 CT2 CT3 CT4 PHS IN I1 I2 I3 I4
VDD φ2 φ1 TH3 P4 TH4 P5 GND TH2 P3 P2 TH1 P1 P0 MAG
GND P5 TH4 VH P4 TH3 VDD TH2 P3 P2 TH1 P1
GND φ1 φ2 VGG MAG VH
LSI Card
LSI TERMINAL DIAGRAM

DATA CHIP

TERMINAL	NAME	FROM	TO	TERMINAL	NAME	FROM	TO
21	TB0	TC		20	TB3	TC	
22	(OPEN)			19	TD12	TC	
23	(OPEN)			18	SCT1	TC	
24	P0	TC		17	CR1	CC	
25	PR1	TC		16	CR2	CC	
26	VDD			15	CR3	CC	
27	GND			14	CR4	CC	
28	VGG			13	CR5	CC	
29	N	KB		12	ϕ_1		
30	9	KB		11	ϕ_2		
31	8	KB		10	VDD		
32	(OPEN)			9	$\overline{MSD=0}$		CC
33	7	KB		8	$\overline{CA}$		CC
34	6	KB		7	KST		CC
35	5	KB		6	KEY(C+CI)		CC
36	4	KB		5	IN		CC·TC
37	3	KB		4	I1		CC·TC
38	2	KB		3	I2		CC·TC
39	1	KB		2	I3		CC·TC
40	0	KB		1	I4		TC

CONTROL CHIP

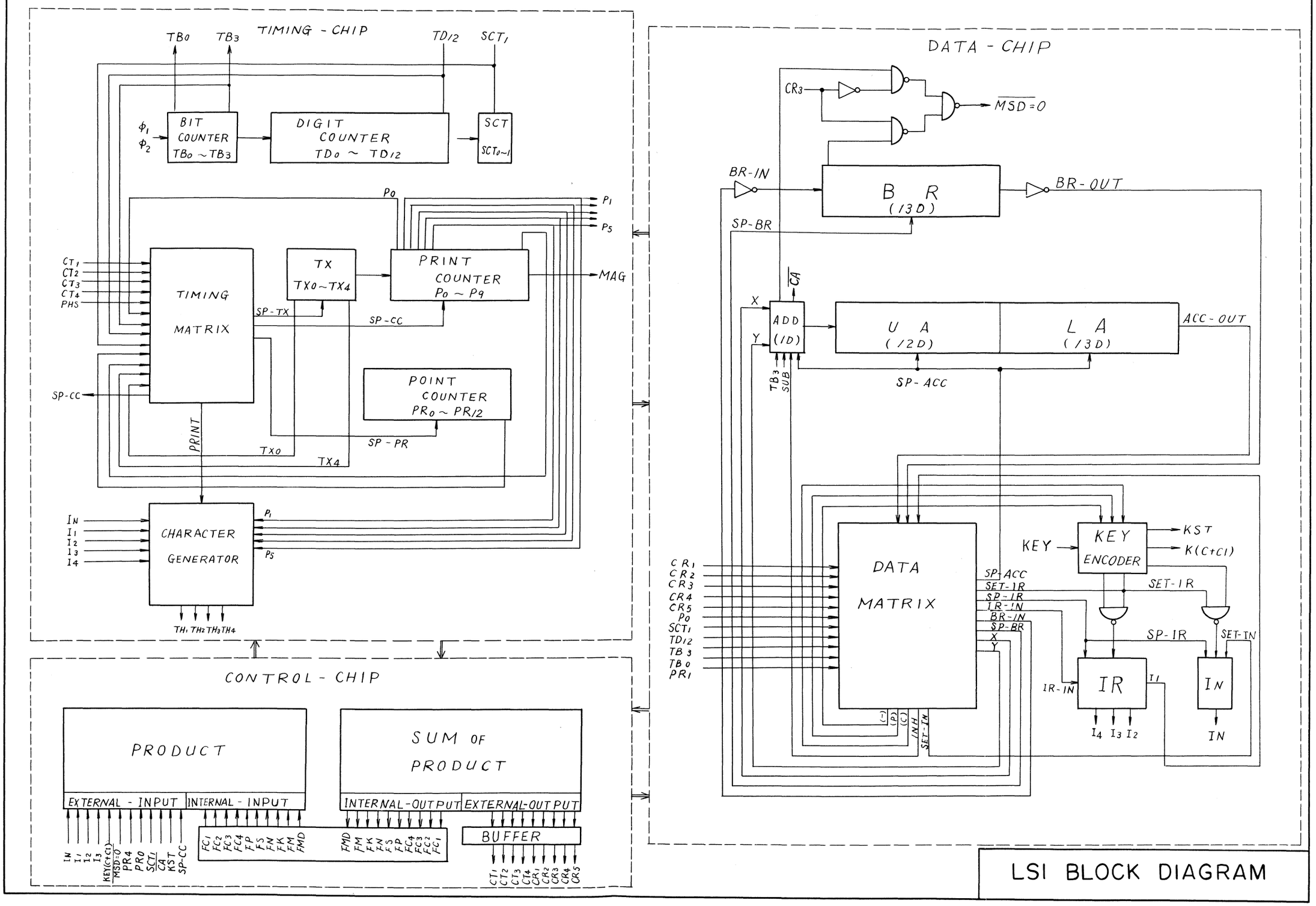
TERMINAL	NAME	FROM	TO	TERMINAL	NAME	FROM	TO
15	CR2		DC	14	CR1		DC
16	CR3		DC	13	CT1		TC
17	CR4		DC	12	CT2		TC
18	CR5		DC	11	CT3		TC
19	ϕ_1			10	CT4		TC
20	ϕ_2			9	VDD		
21	SP-CC	TC		8	GND		
22	VGG			7	PR4	TC	
23	$\overline{MSD=0}$	DC		6	PR0	TC	
24	$\overline{CA}$	DC		5	SCT1	TC	
25	KST	DC		4	IN	DC	
26	KEY(C+CI)	DC		3	I1	DC	
27	I2	DC		2	(OPEN)		
28	I3	DC		1	(OPEN)		

TIMING CHIP

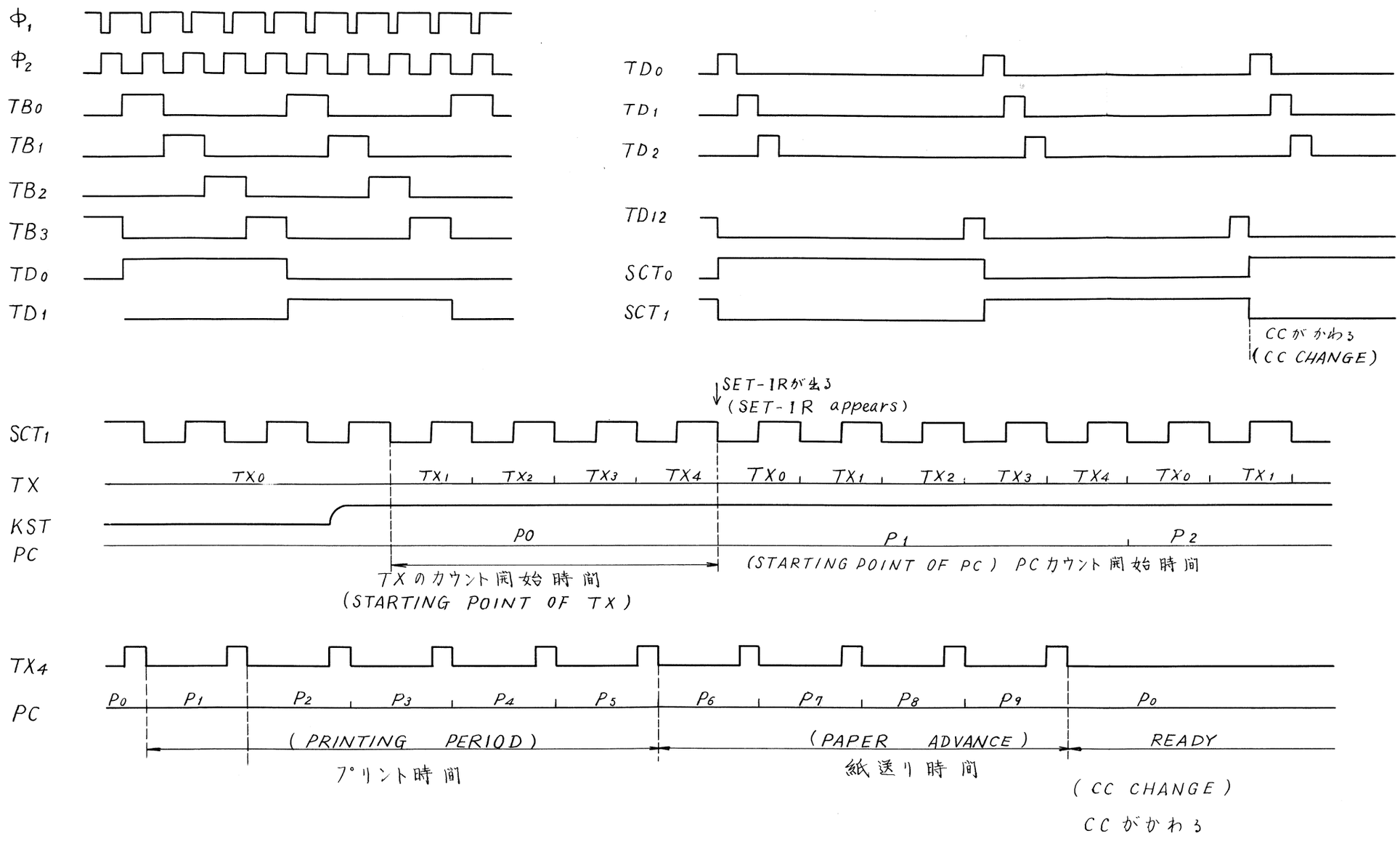
TERMINAL	NAME	FROM	TO	TERMINAL	NAME	FROM	TO
21	SP-CC		CC	20	VDD		
22	TB0		DC	19	ϕ_2		
23	TB3		DC	18	ϕ_1		
24	TB12		DC	17	(OPEN)		
25	SCT1		DC·CC	16	(OPEN)		
26	PR1		DC	15	TH3		TH
27	PR0		CC	14	P4		TH
28	PR4		CC	13	(OPEN)		
29	VGG			12	TH4		TH
30	CT1	CC		11	P5		TH
31	CT2	CC		10	GND		
32	CT3	CC		9	TH2		TH
33	CT4	CC		8	P3		TH
34	PHS			7	P2		TH
35	IN	DC		6	(OPEN)		
36	I1	DC		5	(OPEN)		
37	I2	DC		4	TH1		TH
38	I3	DC		3	P1		TH
39	I4	DC		2	P0		DC
40	(OPEN)			1	MAG		TH

CC: CONTROL CHIP
DC: DATA CHIP
TC: TIMING CHIP
TH: THERMAL HEAD
KB: KEY BOARD

INPUT & OUTPUT SIGNAL TABLE OF LSI



LSI BLOCK DIAGRAM

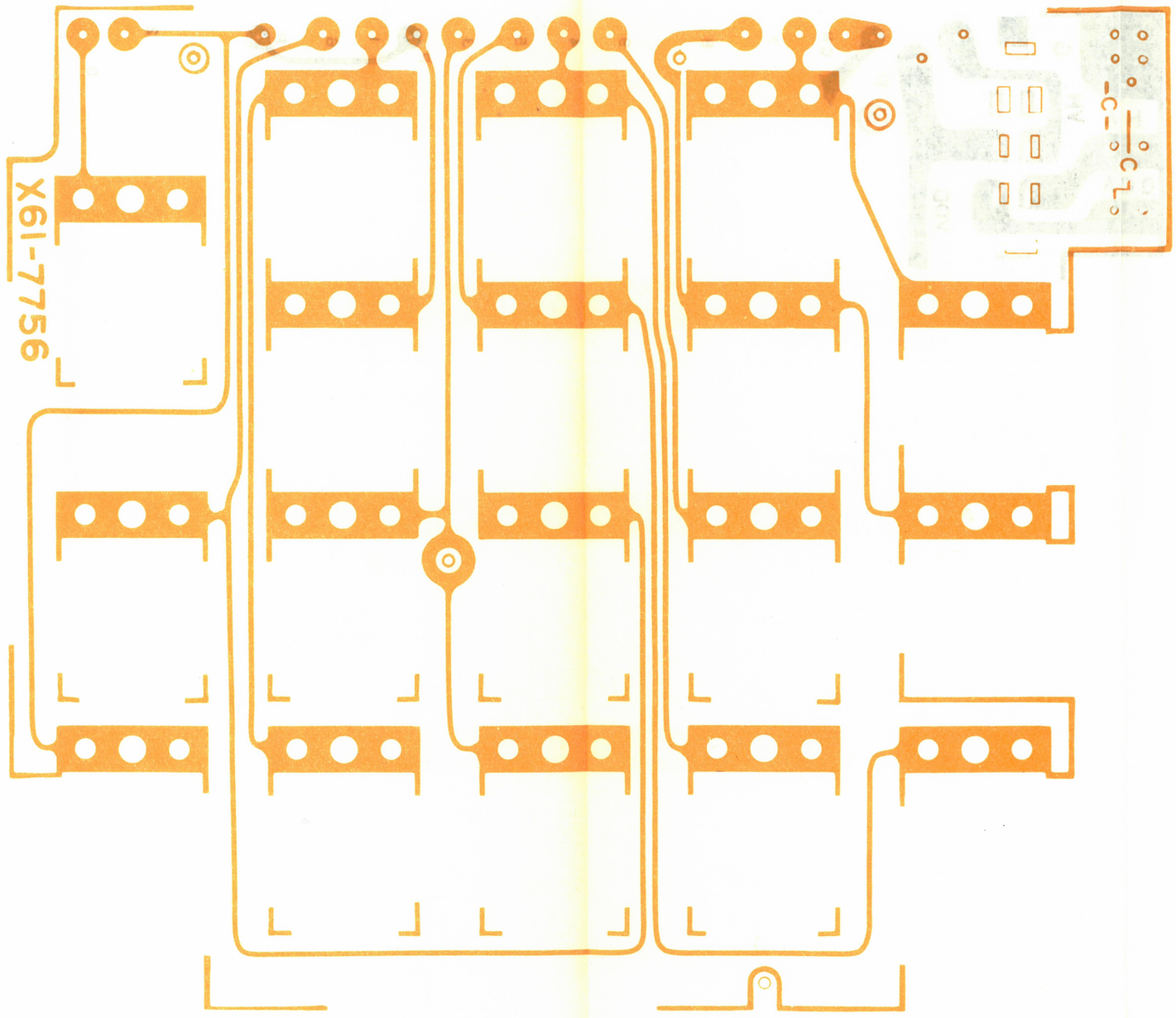


TIMING CHART

1 KEY CONTACT UNIT

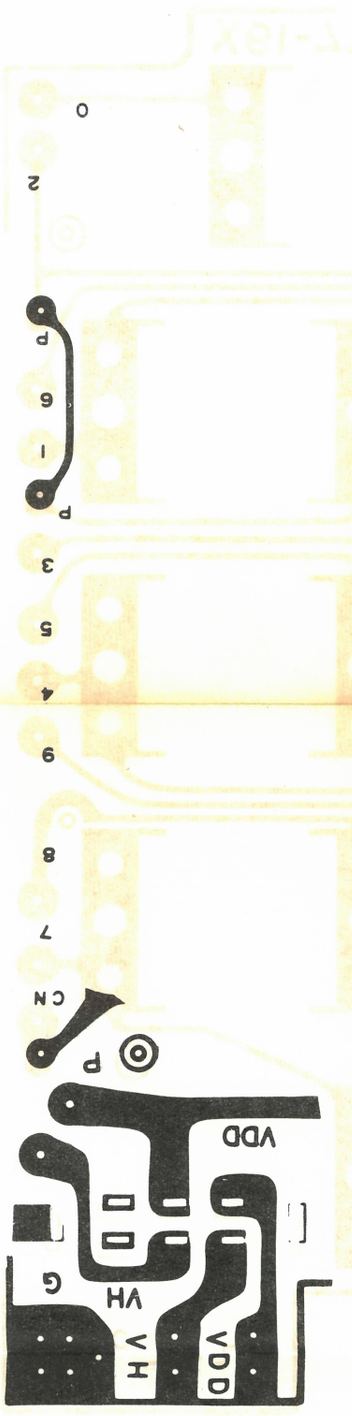
（キー接点ユニット）

88-0635-02



改　　訂　　版

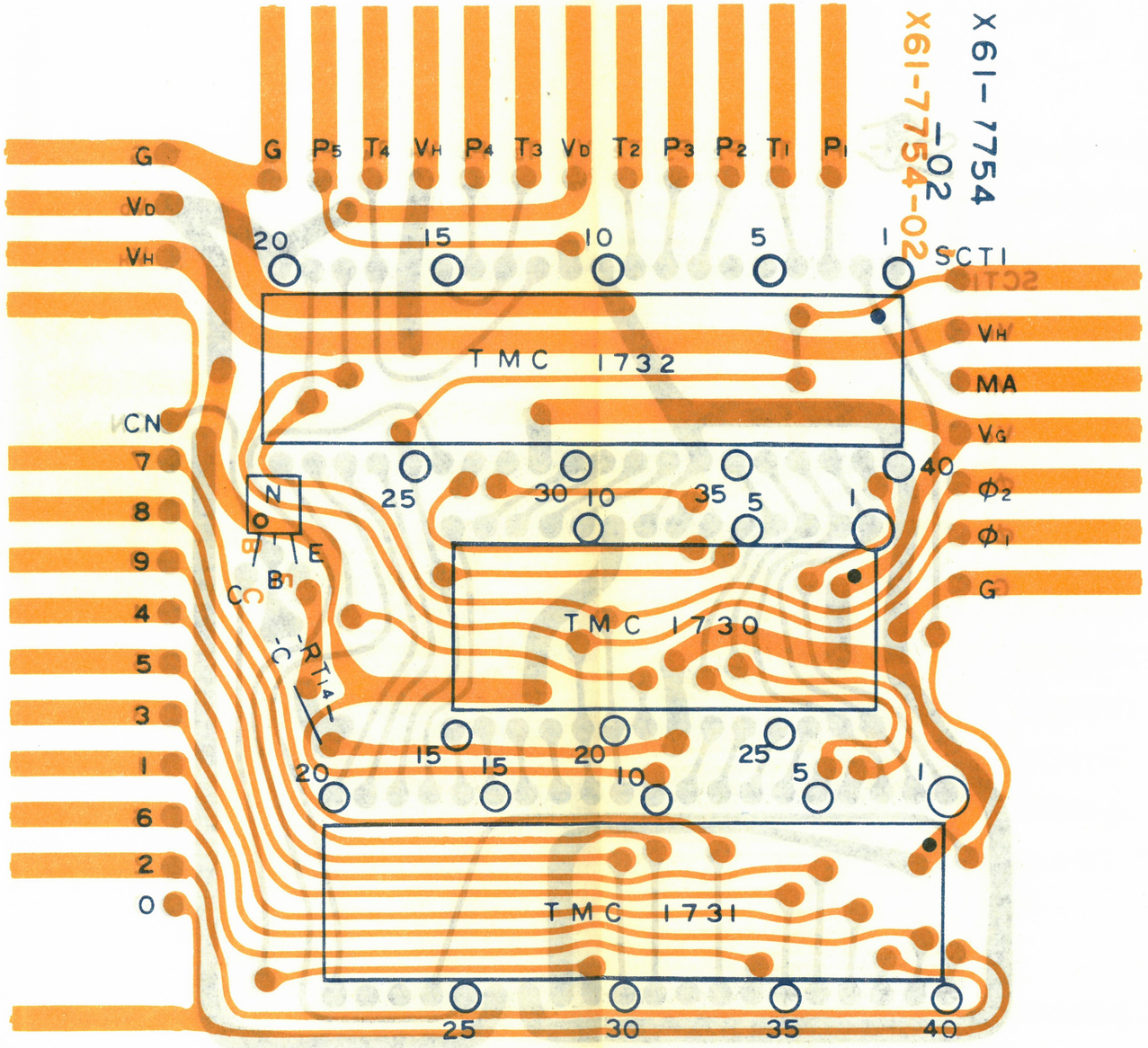
REVISED EDITION


0
2
P
6
1
P
3
5
4
9
8
7
CN
P
VDD
G
VH
VH
VDD

2 LSI CARD UNIT

（LSI カードユニット）

88-0638-02



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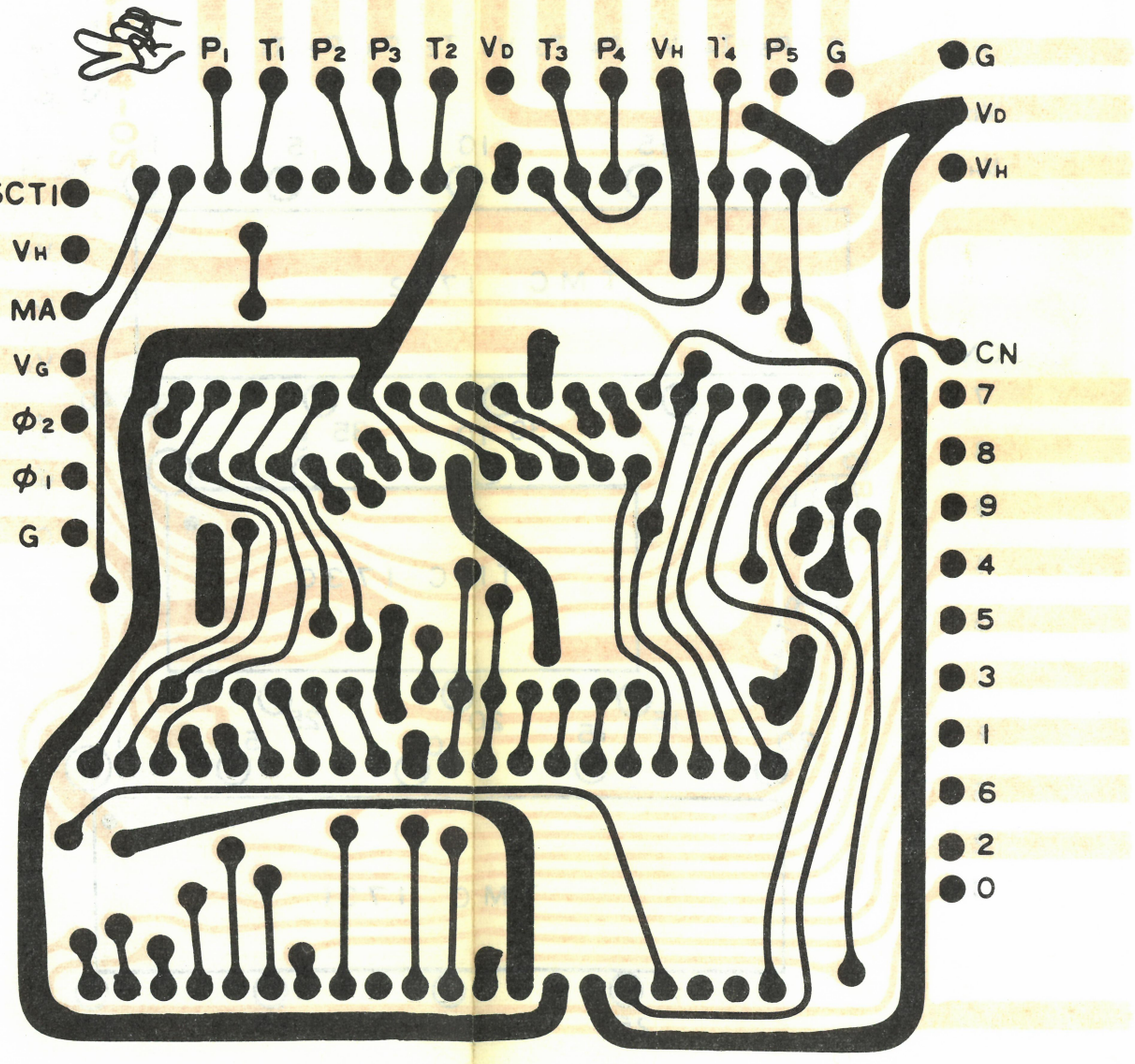
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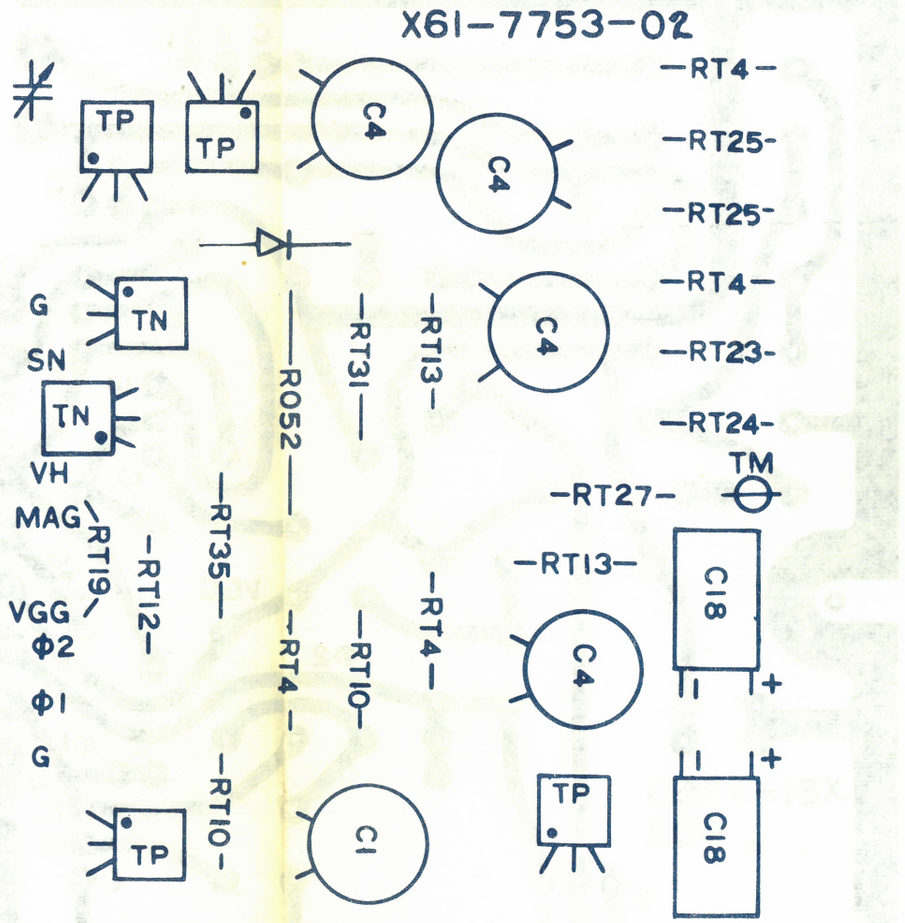
T1
P2
P3
T2
VD
T3
P4
VH
T4
P5
G
SCTI
VH
MA
VG
Φ2
Φ1
G
G
VD
VH
CN
7
8
9
4
5
3
1
6
2
0

3 DISCRETE CARD UNIT

（デイスクリートカードユニット）

88-0639-02



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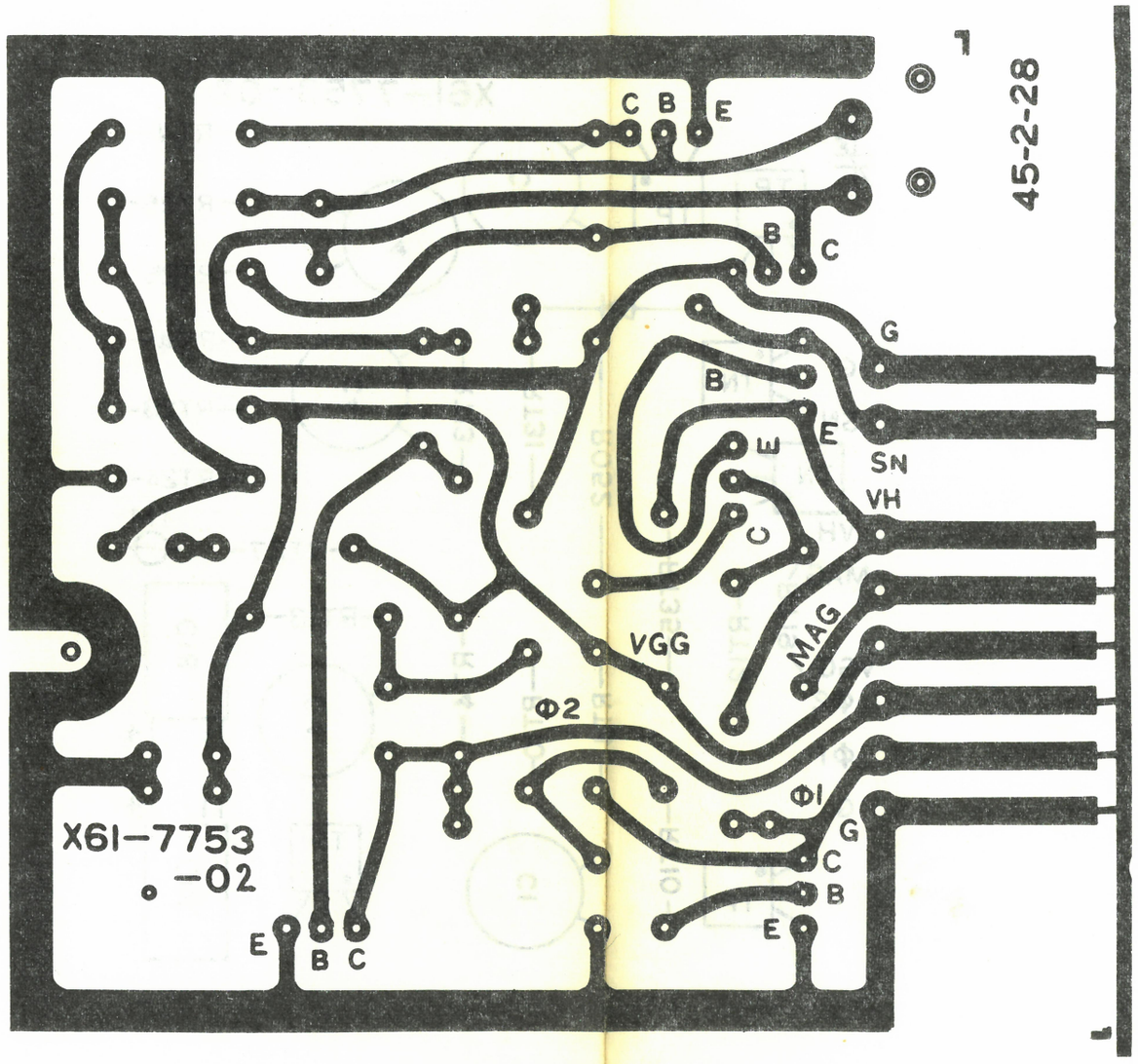
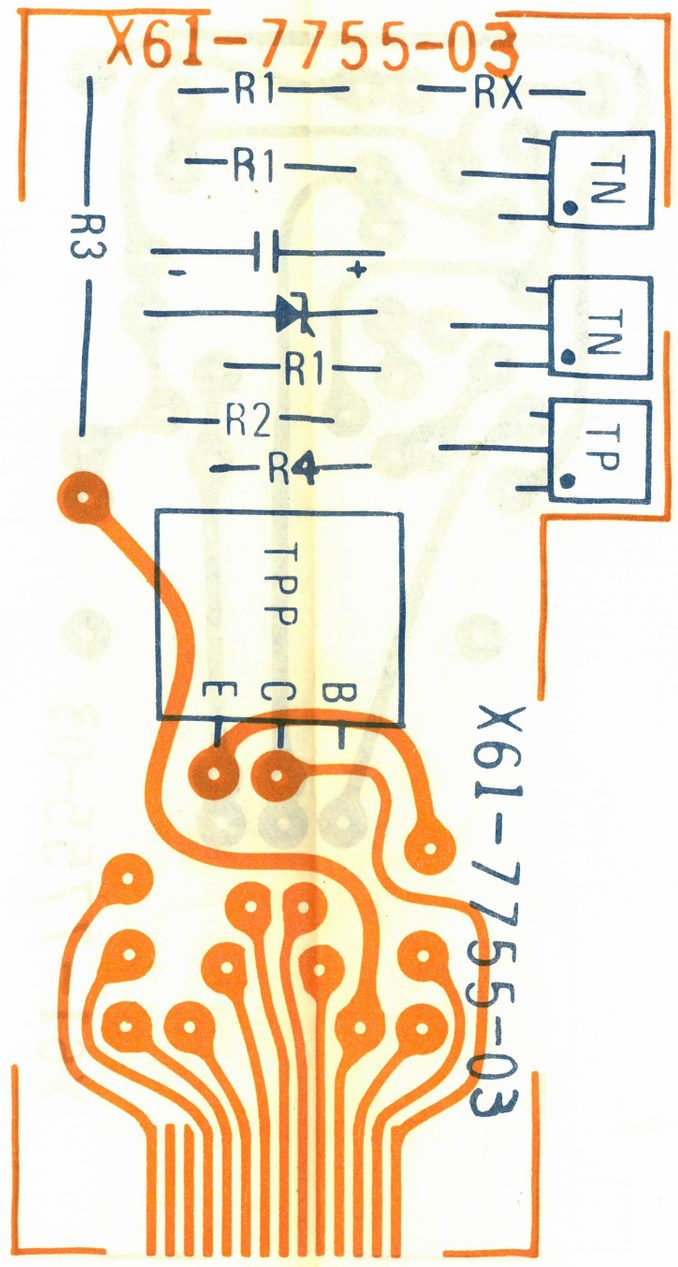

45-2-28
C B E
B C
G
B
E
E
SN
VH
C
VGG
MAG
Φ2
Φ1
G
C
B
E
X61-7753
-02
E
B C

4 THEMAL HEAD PRINTED BOARD

（サーマルヘッド　プリント板）

X61-7755-03



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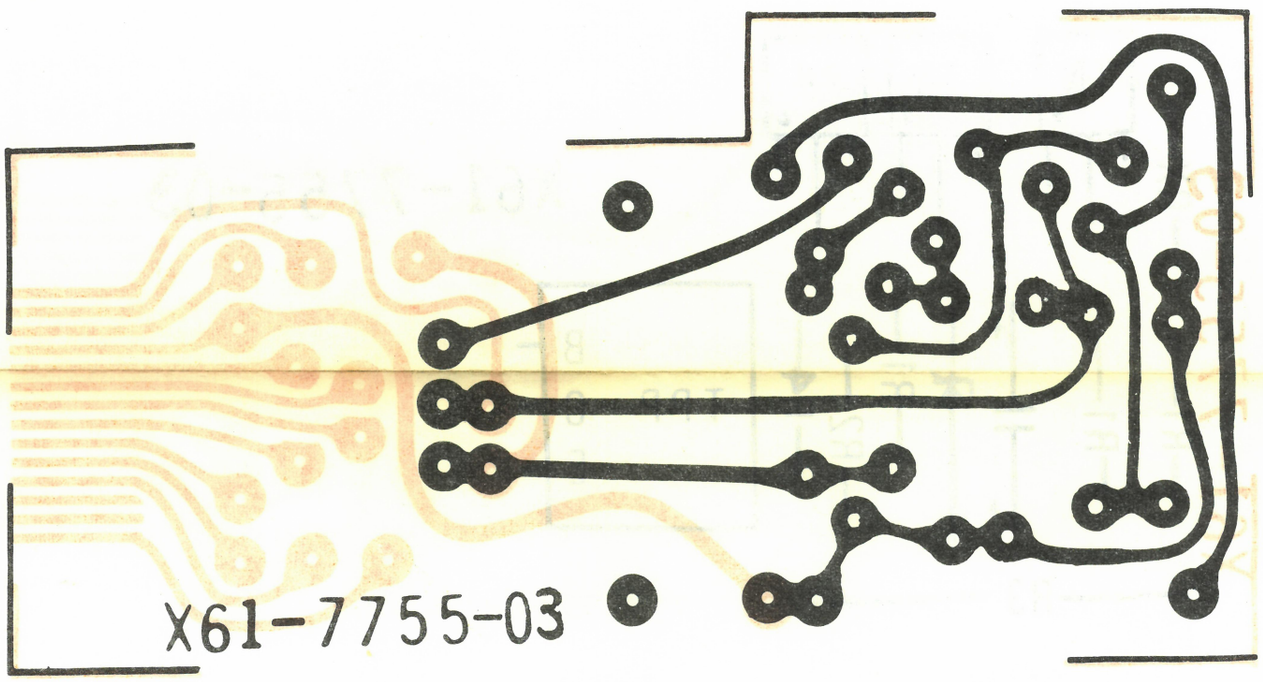
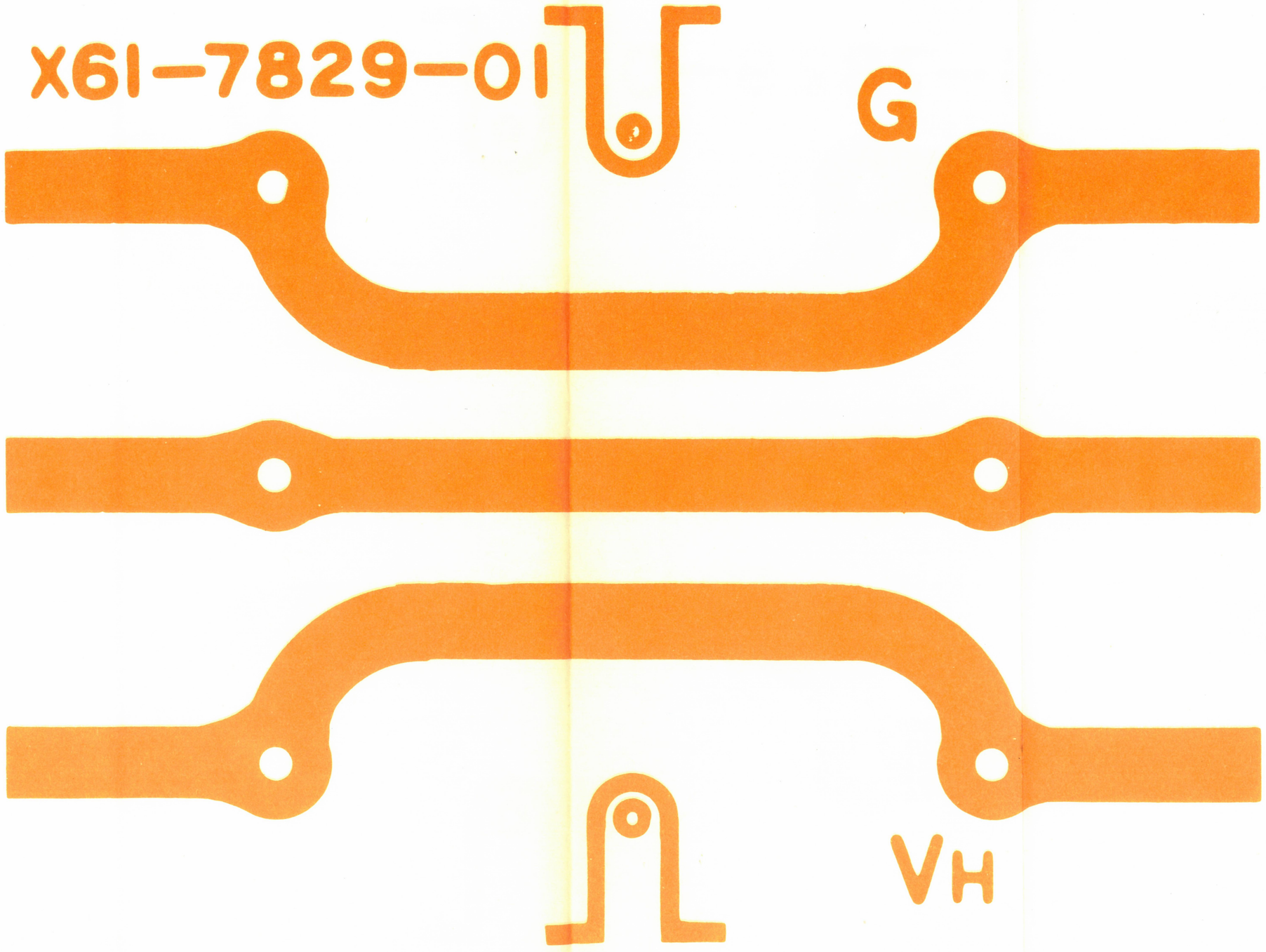

X61-7755-03

5 BATTERY CASE PRINTED BOARD

（電池ケース　プリント板）

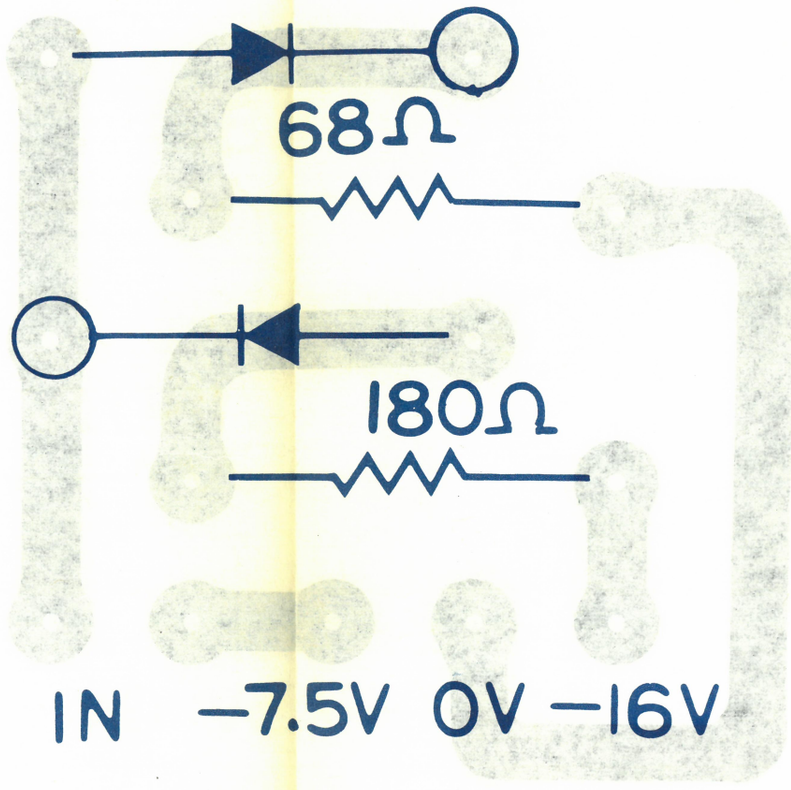
X61-7829-01



Canola Pocketronic Battery Charger 10A

Y80-0108-01

X61-7833-02



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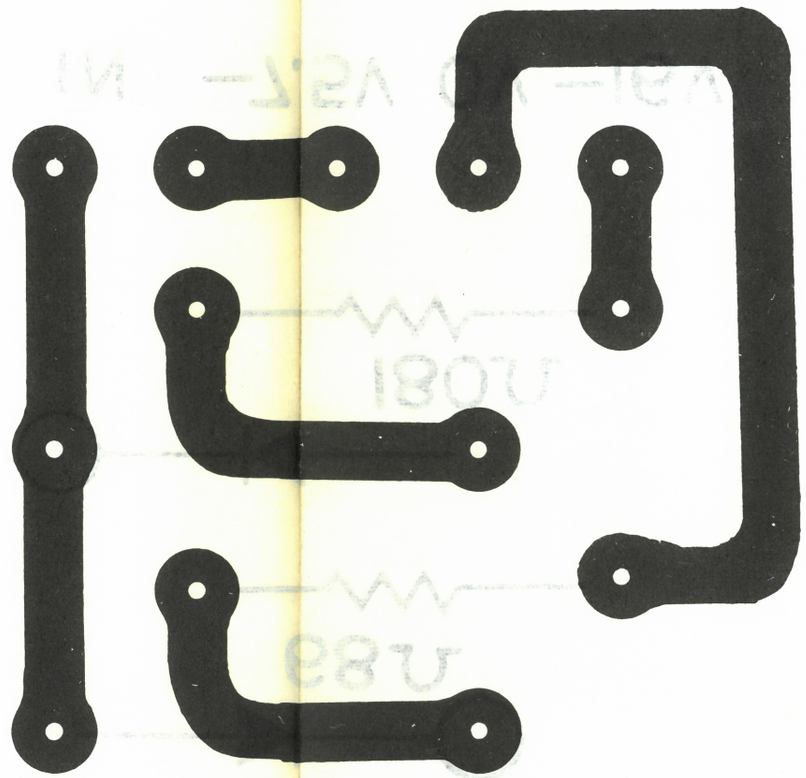
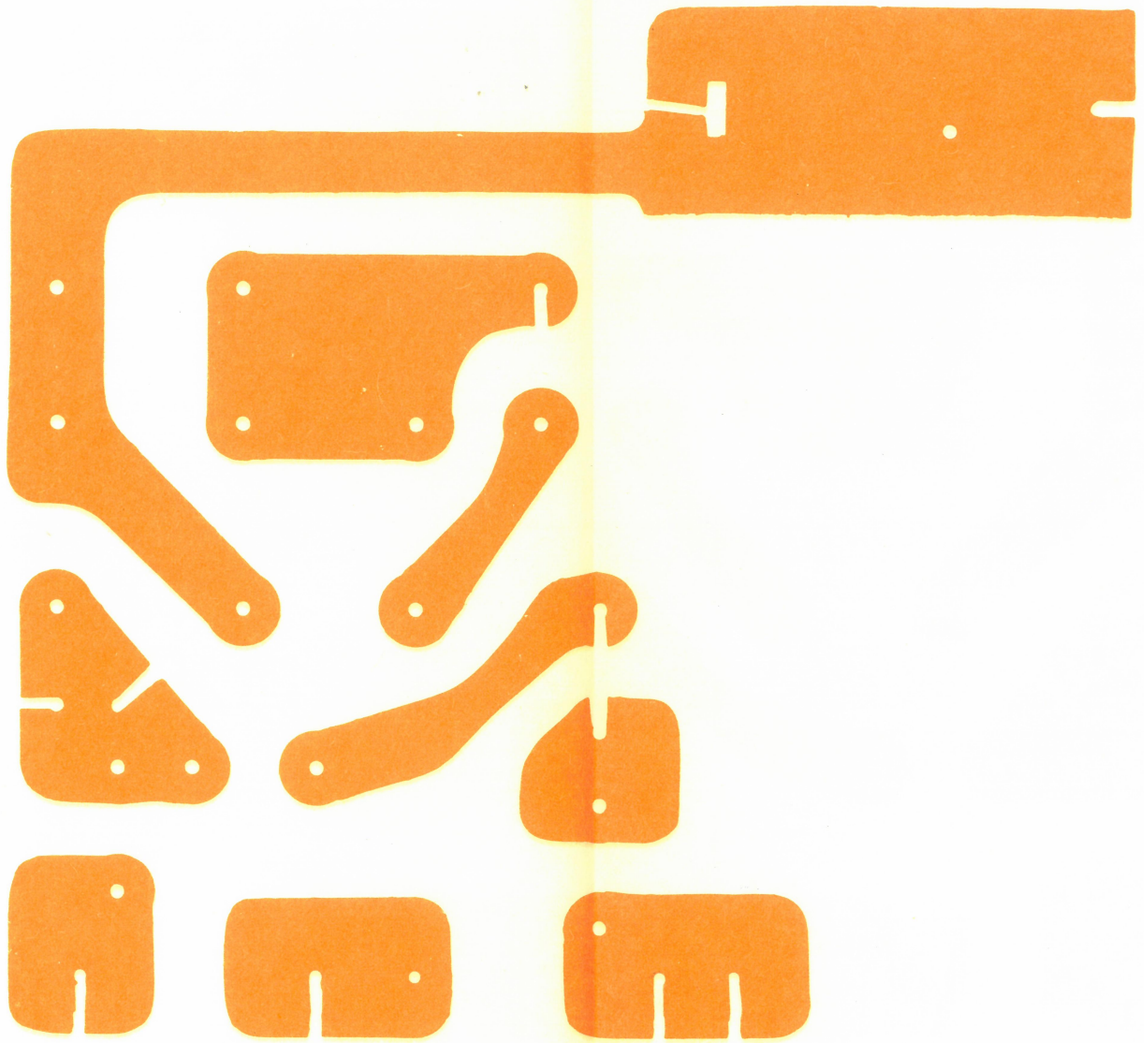


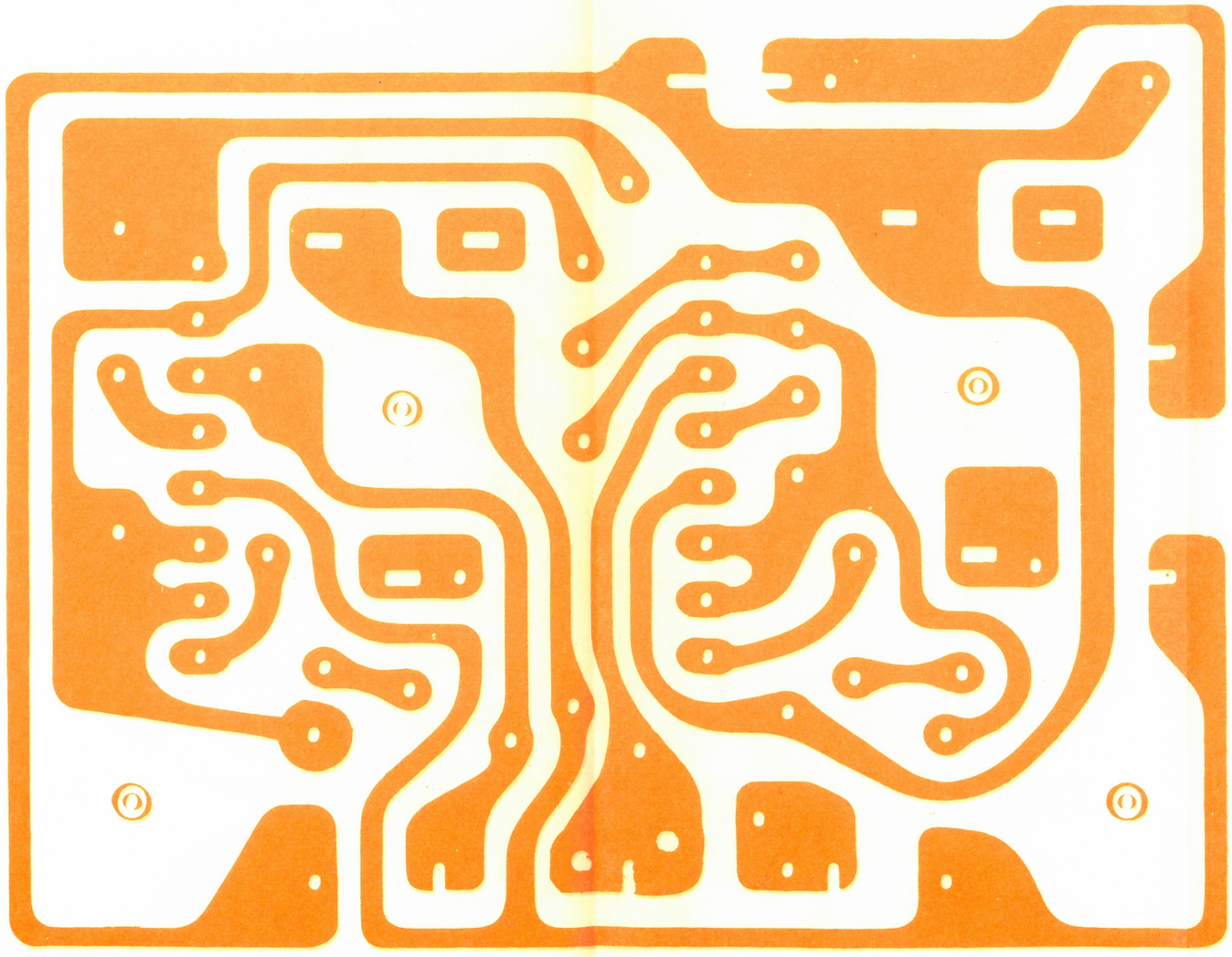
Canola Pocketronic Hi-speed Battery Charger 20A

88-0687-01



Canola Pocketronic Hi-speed Battery Charger 20A

88-0687-01



PARTS CATALOG

PARTS CATALOG

All parts which are used in Canola Pocketronic are listed in this Parts Catalog.

When ordering any part or parts, first, confirm with the Part's Diagram in the Parts Catalog, and specify the part by its description, part's serial number and quantity.

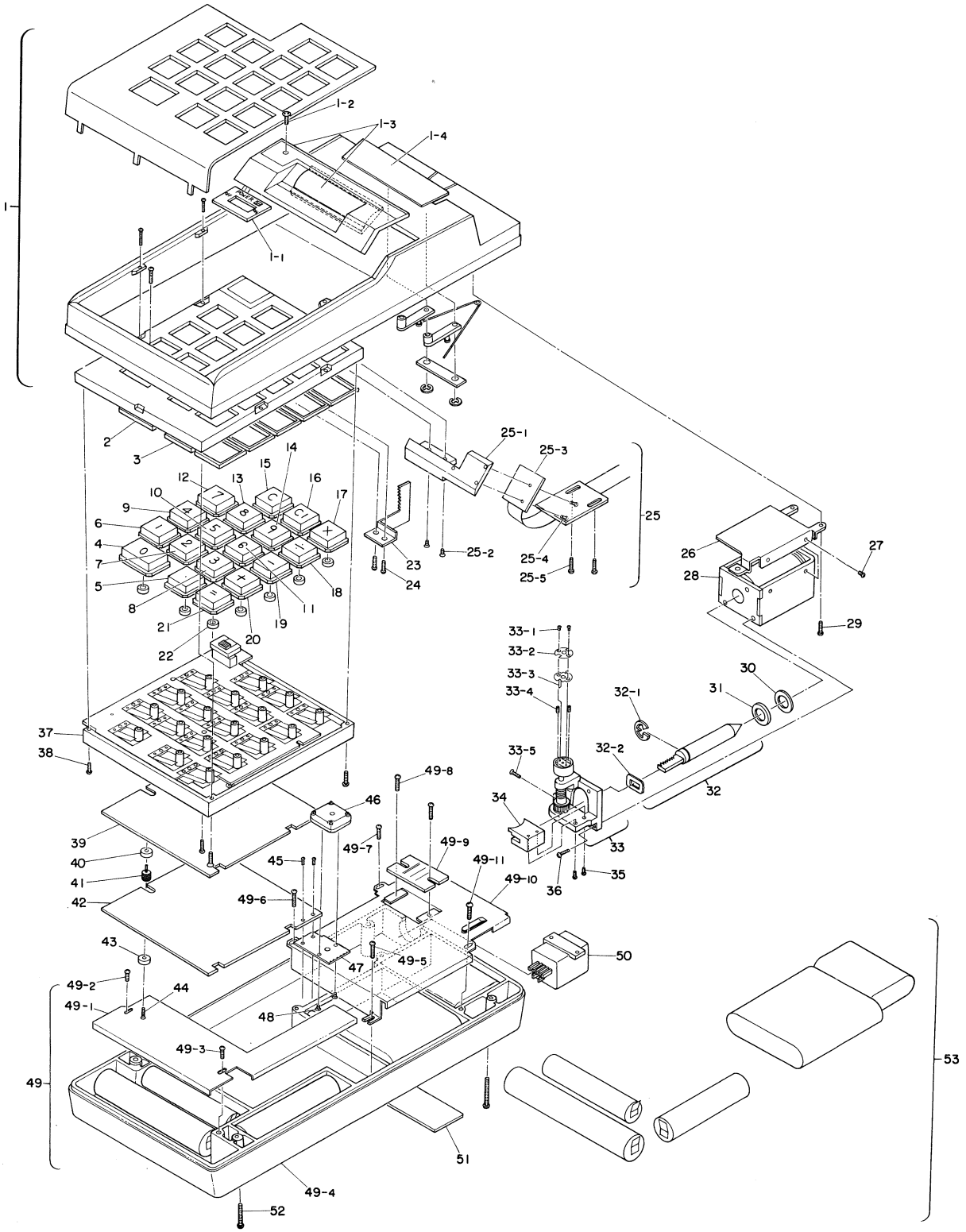
When any part in this list has been modified, a Service Manual Report will be issued to inform you about the modification with its modified serial number.

Please, enter it in this Parts Catalog section as soon as the information has been received.

August, 1970

1. Exploded View

（分　解　図）



KEY NO.	PARTS NO.	QTY.	DESCRIPTION	
1	Y80-0098-01	1	Upper Cover Unit	上カバーユニット
1-1	83-7150-01	1	Power Switch Plate	電源スイッチプレート
1-2	86-0094-01	1	Screw, Pin Face 2 x 3.2	カニメネジ
1-3	Y80-0123-01	1	Hood Ass'y	フードアッセイ
1-4	96-8284-01	1	Name Plate	ネームプレート
2	83-7088-01	1	Damper	ダンパー
3	83-7089-01	17	Damper	ダンパー
4	83-7069-01	1	Keytop 0	キートップ 0
5	83-7070-01	1	Keytop ⊡	キートップ ⊡
6	83-7071-01	1	Keytop 1	キートップ 1
7	83-7072-01	1	Keytop 2	キートップ 2
8	83-7073-01	1	Keytop 3	キートップ 3
9	83-7074-01	1	Keytop 4	キートップ 4
10	83-7075-01	1	Keytop 5	キートップ 5
11	83-7076-01	1	Keytop 6	キートップ 6
12	83-7077-01	1	Keytop 7	キートップ 7
13	83-7078-01	1	Keytop 8	キートップ 8
14	83-7079-01	1	Keytop 9	キートップ 9
15	83-7080-01	1	Keytop ⓒ	キートップ ⓒ
16	83-7081-01	1	Keytop ⓒ'	キートップ ⓒ'
17	83-7082-01	1	Keytop ⊠	キートップ ⊠
18	83-7083-01	1	Keytop ⊞	キートップ ⊞
19	83-7084-01	1	Keytop ⊟	キートップ ⊟
20	83-7085-01	1	Keytop ⊕	キートップ ⊕
21	83-7086-01	1	Keytop ⊜	キートップ ⊜
22	83-7087-01	18	Damper	ダンパー
23	83-7106-02	1	Cutter	カッター
24	X71-5294-01	2	Screw, BH 2 x 5	バイントタッピンネジ
25	88-0640-01	1	Thermal Head Ass'y	サーマルヘッドアッセイ
25-1	83-7108-01	1	Thermal Head Bracket	サーマルヘッドブラケット
25-2	X16-260505	2	Screw, PH 2.6 x 5	十字ナベネジ
25-3	Y80-0113-01	1	Thermal Head Set	サーマルヘッドセット
25-4	X16-200405	3	Screw, PH 2 x 4	十字ナベネジ
25-5	X36-200505	2	Screw, tapping PH 2 x 5	ナベタッピンネジ
26	83-7139-01	1	Plate	トリツケイタ
27	X16-200405	4	Screw, PH 2 x 4	十字ナベネジ
28	89-3010-01	1	Coil Unit	コイルユニット
29	X36-200505	3	Screw, tapping PH 2 x 5	ナベタッピンネジ
30	83-7131-01	1	Washer	ワッシャ
31	83-7133-01	1	Damper	ダンパー
32	Y80-0125-01	1	Core Ass'y	磁芯アッセイ
32-1	X32-401582	1	Washer, retaining	緊定ワッシャ
32-2	83-7134-01	1	Damper	ダンパー
33	Y80-0099-01	1	Roller Unit	ローラーユニット
33-1	X16-170205	2	Screw, PH 1.7 x 2	十字ナベネジ
33-2	83-0120-01	1	Cover	カバー
33-3	83-7147-01	1	Spring	バネ
33-4	83-7127-01	2	Roller	ローラー
33-5	X16-200405	1	Screw, PH 2 x 4	十字ナベネジ

KEY NO.	PARTS NO.	QTY.	DESCRIPTION	
34	83-7138-02	1	Core Guide	コアガイド
35	X36-200807	2	Screw, tapping PH 2 x 8	ナベタッピンネジ
36	X16-200505	3	Screw, PH 2 x 5	十字ナベネジ
37	Y80-0114-01	1	Keyboard Card Unit	キーボードカードユニット
38	X36-260507	5	Screw, tapping PH 2.6 x 5	ナベタッピンネジ
39	88-0638-01	1	LSI Card Unit	LSIカードユニット
40	83-7096-01	1	Washer	ワッシャ
41	83-7097-01	1	Clamp	クランプ
42	Y80-0115-01	1	Discrete Card Set	ディスクリートカードセット
43	83-7096-01	1	Washer	ワッシャ
44	X36-260505	1	Screw, tapping 2.6 x 5	ナベタッピンネジ
45	X16-200405	2	Screw, PH 2 x 4	十字ナベネジ
46	X61-8034-01	1	Variable Condenser	可変コンデンサ
47	83-7107-01	1	Condenser Plate	可変コンデンサ取付板
48	X16-170205	2	Screw, PH 1.7 x 2	十字ナベネジ
49	Y80-0116-01	1	Battery Unit (A), (D)	電池ユニット(A)日本国内
	Y80-0124-01	1	Battery Unit (B), (O)	電池ユニット(B)日本国外
49-1	83-7109-01	1	Battery Cover (A)	電池カバー (A)
49-2	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-3	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-4	89-0739-01	1	Base Cover	底カバー
49-5	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-6	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-7	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-8	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
49-9	X61-7829-01	1	Battery Unit Printed Board	電池ユニットプリント板
49-10	83-7110-01	1	Battery Cover (B)	電池カバー (B)
49-11	X37-200505	1	Screw, tapping BH 2 x 5	バイントタッピンネジ
50	88-0641-01	1	Receptacle Unit	リセプタクルユニット
51	96-8336-01	1	Rating Plate, (D)	定格銘板 日本国内
	96-8338-01	1	Rating Plate, (O)	定格銘板 日本国外
52	X71-5291-01	4	Screw, BH 2.6 x 22	バイントネジ
53	Y80-0101-01	1	Battery Set (A), (D)	電池セット(A)日本国内
	Y80-0112-01	1	Battery Set (B), (O)	電池セット(B)日本国外

2. LSI Card Unit
(LSI カードユニット)
88-0638-01

KEY NO.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
	88-0638-01	1	LSI Card Unit	LSI カードユニット
	X64-0833-02	1	Carbon Resistor 10KΩT1/8W	炭素皮膜固定抵抗器
	X65-5091-01	1	Transistor 2N5449	トランジスタ
	X65-7012-01	1	LSI TMS-1732	LSI TMS-1732
	X65-7013-01	1	LSI TMS-1731	LSI TMS-1731
	X65-7014-01	1	LSI TMS-1730	LSI TMS-1730

3. Discrete Card Unit
(ディスクリートカードユニット)
88-0639-02

KEY NO.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
	88-0639-02	1	Discrete Card Unit	ディスクリートカードユニット
	X63-3114-01	2	Chemical Condenser 4.7μF, 16WV	ケミカルコンデンサ
	X63-2009-01	11	Ceramic Condenser 47pF, 50V	セラミックコンデンサ
	X63-2010-01	4	Ceramic Condenser 100pF, 50V	セラミックコンデンサ
	X64-0122-01	1	Carbon Resistor 47ΩT1/4W	炭素皮膜固定抵抗器
	X64-0634-02	1	Carbon Resistor 6.8KΩT1/8W	炭素皮膜固定抵抗器
	X64-0635-02	1	Carbon Resistor 8.2KΩT1/8W	炭素皮膜固定抵抗器
	X64-0636-02	2	Carbon Resistor 150KΩT1/8W	炭素皮膜固定抵抗器
	X64-0828-01	1	Carbon Resistor 1KΩT1/8W	炭素皮膜固定抵抗器
	X64-0833-02	2	Carbon Resistor 10KΩT1/8W	炭素皮膜固定抵抗器
	X64-0836-02	2	Carbon Resistor 56KΩT1/8W	炭素皮膜固定抵抗器
	X64-0853-02	4	Carbon Resistor 4.7KΩT1/8W	炭素皮膜固定抵抗器
	X64-0855-02	1	Carbon Resistor 2.2KΩT1/8W	炭素皮膜固定抵抗器
	X65-5045-01	1	Diode WG-599	ダイオード
	X65-5090-01	4	Transistor 2N5447	トランジスタ
	X65-5091-01	2	Transistor 2N5449	トランジスタ
	X65-9504-01	1	Thermistor 32D27	サーミスタ
	X64-0723-01	1	Metal Resistor 150Ω	酸化金属皮膜抵抗器
	X62-8946-01	1	Metal Resistor 270Ω	酸化金属皮膜抵抗器
	X64-0860-01	1	Metal Resistor 15KΩT1/8W	酸化金属皮膜抵抗器
	X64-0835-01	1	Metal Resistor 33KΩT1/8W	酸化金属皮膜抵抗器

4. A.V.R. Card Unit

（A.V.R. カード）

Y80-0113-01

Nomen.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
	X61-6910-01	3	Pin	虫　　ピ　　ン
	X62-8805-01	1	Chemical Condenser 10V 2.2μF	ケミカルコンデンサー
	X64-2210-01	1	Solid Resistor 390ΩT1/2W	ソリッド抵抗器
	X64-2323-01	1	Solid Resistor 8.2KΩT1/8W	ソリッド抵抗器
	X64-2415-01	3	Solid Resistor 10KΩT1/8W	ソリッド抵抗器
	X64-2508-01	1	Solid Resistor 100KΩT1/8W	ソリッド抵抗器
	X65-5090-01	1	Transistor 2N5447	トランジスタ
	X65-5091-01	2	Transistor 2N5449	トランジスタ
	X65-5124-01	1	Zenor Diode IN4736	ツェナーダイオード
	X65-6126-01	1	Transistor TIP30	トランジスタ

3. Parts Index
（部品索引）

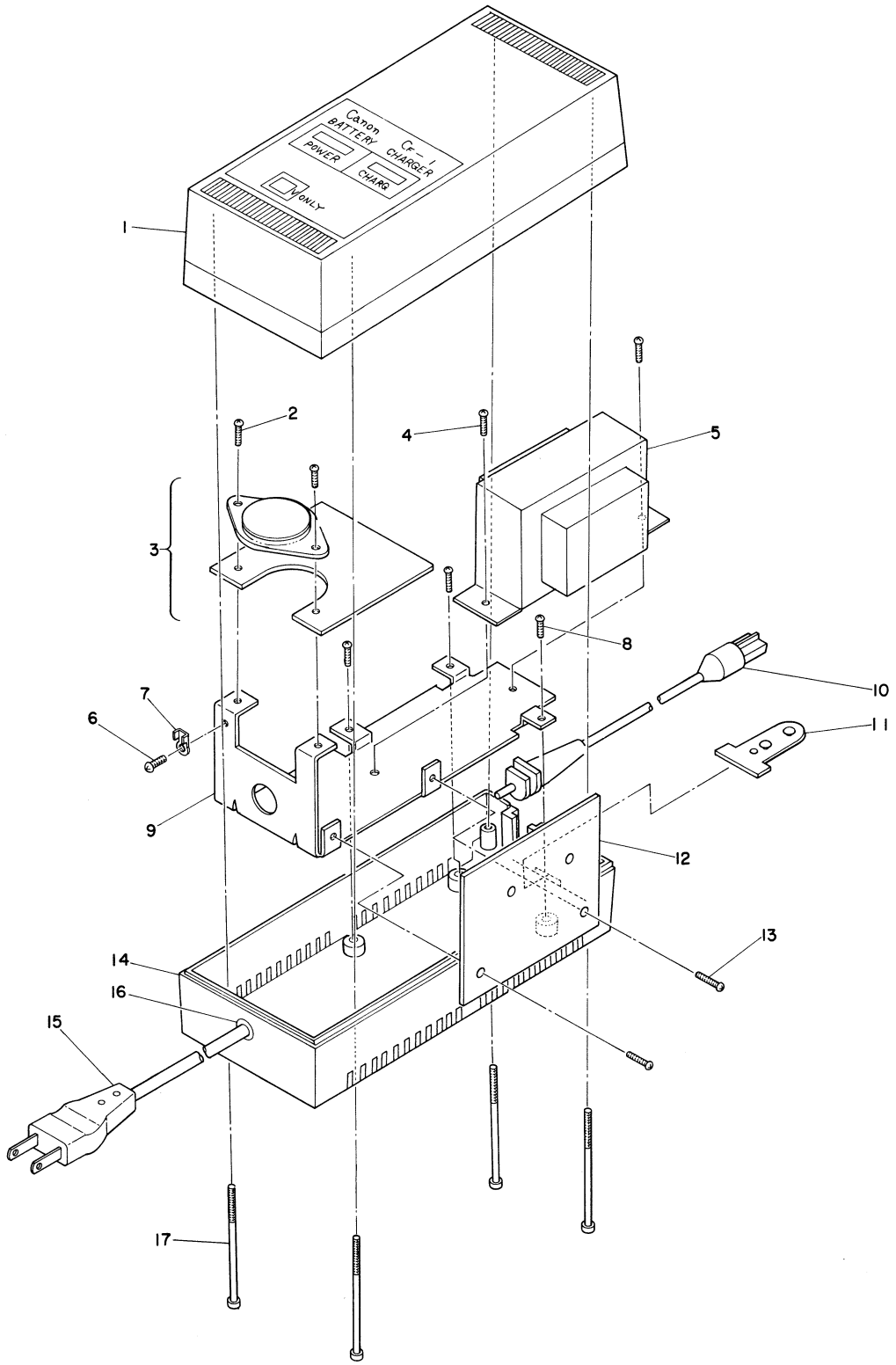
PARTS NO.	UNITS PER ASS'Y	REVISION NO. – REPORT NO.				
Y80-0098-01	1	–	–	–	–	3-1
Y80-0099-01	1	–	–	–	–	3-33
Y80-0101-01	1	–	–	–	–	3-49-13, 3-53
Y80-0112-01	1	–	–	–	–	3-49-13, 3-53
Y80-0113-01	1	–	–	–	–	3-25-3
Y80-0114-01	1	–	–	–	–	3-37
Y80-0115-01	1	–	–	–	–	3-42
Y80-0116-01	1	–	–	–	–	3-49
Y80-0123-01	1	–	–	–	–	3-1-3
Y80-0124-01	1	–	–	–	–	3-49
Y80-0125-01	1	–	–	–	–	3-32
X16-170205	4	–	–	–	–	3-33-1, 3-48
X16-200405	8	–	–	–	–	3-25-4
X16-200505	3	–	–	–	–	3-36
X16-260505	2	–	–	–	–	3-25-2
X32-401582	1	–	–	–	–	3-32-1
X36-200505	5	–	–	–	–	3-25-5, 3-29
X36-200807	2	–	–	–	–	3-35
X36-260507	5	–	–	–	–	3-38
X36-260505	1	–	–	–	–	3-44
X37-200505	7	–	–	–	–	3-49-2, 3-49-3, 3-49-5
X61-8034-01	1	–	–	–	–	3-46
X61-7829-01	1	–	–	–	–	3-49-9
X61-6910-01	3	–	–	–	–	4
X62-8946-01	1	–	–	–	–	4
X62-8805-01	1	–	–	–	–	4
X63-2009-01	11	–	–	–	–	4
X63-2010-01	4	–	–	–	–	4
X63-3114-01	2	–	–	–	–	4
X64-0122-01	1	–	–	–	–	4
X64-0634-02	1	–	–	–	–	4
X64-0635-02	2	–	–	–	–	4
X64-0636-02	2	–	–	–	–	4
X64-0723-01	1	–	–	–	–	4
X64-0828-02	3	–	–	–	–	4
X64-0833-02	3	–	–	–	–	4
X64-0835-01	1	–	–	–	–	4
X64-0836-02	2	–	–	–	–	4
X64-0853-02	4	–	–	–	–	4
X64-0860-01	1	–	–	–	–	4
X64-2210-01	1	–	–	–	–	4
X64-2323-01	1	–	–	–	–	4
X64-2415-01	3	–	–	–	–	4
X64-2508-01	1	–	–	–	–	4
X65-5045-01	1	–	–	–	–	4
X65-5090-01	5	–	–	–	–	4
X65-5091-01	5	–	–	–	–	4
X65-5124-01	1	–	–	–	–	4
X65-6126-01	1	–	–	–	–	4
X65-7012-01	1	–	–	–	–	4
X65-7013-01	1	–	–	–	–	4
X65-7014-01	1	–	–	–	–	4

PARTS NO.	UNITS PER ASS'Y	REVISION NO. – REPORT NO.				
X65-7016-01	1	–	–	–	–	4
X65-9504-01	1	–	–	–	–	4
X71-5291-01	4	–	–	–	–	3-52
X71-5294-01	2	–	–	–	–	3-24
83-0120-01	1	–	–	–	–	3-33-2
83-7069-01	1	–	–	–	–	3-4
83-7070-01	1	–	–	–	–	3-5
83-7071-01	1	–	–	–	–	3-6
83-7072-01	1	–	–	–	–	3-7
83-7073-01	1	–	–	–	–	3-8
83-7074-01	1	–	–	–	–	3-9
83-7075-01	1	–	–	–	–	3-10
83-7076-01	1	–	–	–	–	3-11
83-7077-01	1	–	–	–	–	3-12
83-7078-01	1	–	–	–	–	3-13
83-7079-01	1	–	–	–	–	3-14
83-7080-01	1	–	–	–	–	3-15
83-7081-01	1	–	–	–	–	3-16
83-7082-01	1	–	–	–	–	3-17
83-7033-01	1	–	–	–	–	3-18
83-7084-01	1	–	–	–	–	3-19
83-7085-01	1	–	–	–	–	3-20
83-7086-01	1	–	–	–	–	3-21
83-7087-01	18	–	–	–	–	3-22
83-7088-01	1	–	–	–	–	3-2
83-7089-01	17	–	–	–	–	3-3
83-7096-01	2	–	–	–	–	3-40, 3-43
83-7097-01	1	–	–	–	–	3-41
83-7106-02	1	–	–	–	–	3-23
83-7107-01	1	–	–	–	–	3-47
83-7108-02	1	–	–	–	–	3-25-1
83-7109-02	1	–	–	–	–	3-49-1
83-7110-01	1	–	–	–	–	3-49-10
83-7127-01	2	–	–	–	–	3-33-4
83-7131-01	1	–	–	–	–	3-30
83-7133-01	1	–	–	–	–	3-31
83-7134-01	1	–	–	–	–	3-32-2
83-7138-02	1	–	–	–	–	3-34
83-7139-01	1	–	–	–	–	3-26
83-7147-01	1	–	–	–	–	3-33-3
83-7150-01	1	–	–	–	–	3-1-1
86-0094-01	1	–	–	–	–	3-1-2
88-0638-01	1	–	–	–	–	3-40, 4
88-0640-01	1	–	–	–	–	3-25
88-0641-01	1	–	–	–	–	3-50
		–				
89-0739-01	1	–	–	–	–	3-49-4
89-3010-01	1	–	–	–	–	3-28
96-8284-01	1	–	–	–	–	3-1-4
96-8336-01	1	–	–	–	–	3-51
96-8338-01	1	–	–	–	–	3-51

CANON POCKETRONIC

HI-SPEED BATTERY CHARGER 20A

Hi-speed Battery Charger 20A



Hi-speed Battery Charger 20A

KEY NO.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
1	89-3020-02	1	Upper Cover Unit	上カバーユニット
2	X06-300603	2	Screw, PH 3 x 6	十字ナベネジ
3	88-0687-02	1	Card Unit (A)	カードユニット
4	X06-300403	2	Screw, PH 3 x 4	十字ナベネジ
5	X61-1164-01	1	Power Transformer	電源トランス
6	X06-400403	1	Screw, PH 4 x 4	十字ナベネジ
7	X62-7972-01	1	Lug Terminal	ラグ端子
8	X06-300403	3	Screw, PH 3 x 4	十字ナベネジ
9	83-7679-02	1	Chassis	シャーシ
10	88-2520-01	1	Curl Code Unit	カールコードユニット
11	83-7680-01	1	Eyelet, hanger	ツリカン
12	88-0688-01	1	Card Unit (B)	カードユニット(B)
13	X06-300603	2	Screw, PH 3 x 6	十字ナベネジ
14	Y80-0176-01	1	Base Cover Unit, 100V	底カバーユニット
	Y80-0178-01	1	Base Cover Unit, 110V～120V	底カバーユニット
	Y80-0179-01	1	Base Cover Unit, 220V～240V	底カバーユニット
15	88-2501-01	1	Power Supply Cord Unit, 100V	電源コード
	88-2502-01	1	Power Supply Cord Unit, 115V	電源コード
	88-2504-01	1	Power Supply Cord Unit, 240V	電源コード
	88-2543-01	1	Power Supply Cord Unit, 220V	電源コード
16	X62-6979-01	1	Cord Bush, 100V, 115V	コードブッシュ
	X62-6980-01	1	Cord Bush, 220V, 240V, 115UL	コードブッシュ
17	X16-264005	4	Screw, PH 2.6 x 40	十字ナベネジ

Card Unit (A)
(カードユニット)
88-0687-02

Nomen.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
	X61-0036-02	1	Switch	スイッチ
F	X61-7933-01	1	Fuse 0.3A	ヒューズ
L1,L2	X62-1517-01	2	Coil 2.2mH	コイル
	X62-6972-01	1	Lug Terminal	ラグ端子
Ne	X62-7530-01	1	Neon Lamp	ネオンランプ
C1,C2	X63-2811-01	2	Ceramic Condenser 150V 1000PF	セラミックコンデンサー
R1,R2	X64-0489-01	2	Carbon Resistor 68KΩ T 1/4W	炭素被膜固定抵抗器
	E10126	0.3m	Wire	電線

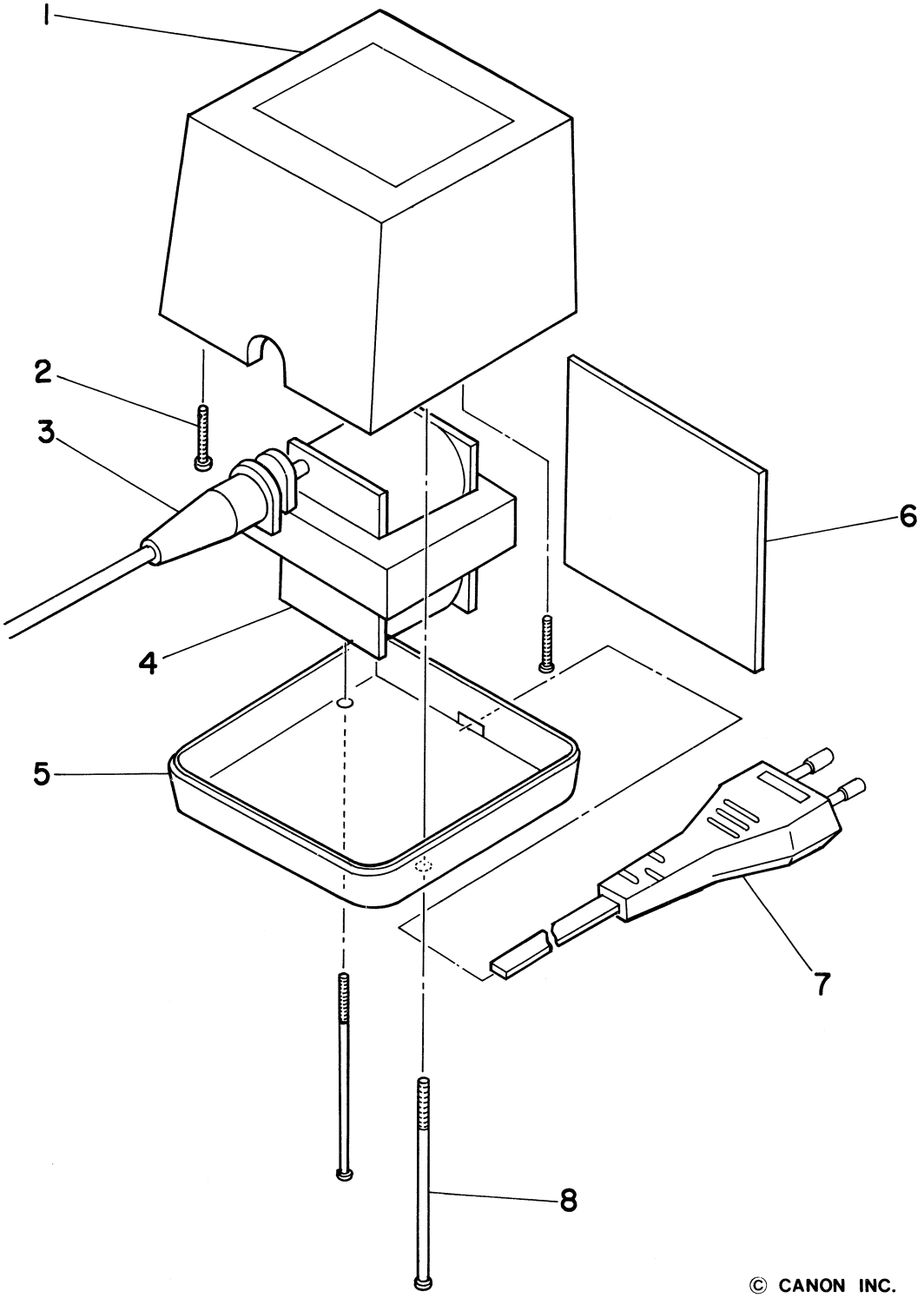
Card Unit (B)
(カードユニット)
88-0688-02

Nomen.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
P.L	X61-7103-02	1	Charger Lamp	チャージャーランプ
R3	X62-8338-01	1	Resister	抵抗
C3~C6	X63-2037-01	4	Ceramic Condenser 50V 0.1μF	セラミックコンデンサー
R5,R7	X64-0161-01	2	Carbon Resistor 10Ω T1/4W	炭素被膜固定抵抗器
R6	X64-0465-01	1	Carbon Resistor 1.2KΩT1/4W	炭素被膜固定抵抗器
R4	X64-0490-01	1	Carbon Resistor 1.5KΩT1/4W	炭素被膜固定抵抗器
VR1, VR2	X64-4333-01	2	Variable Resistor 5KΩ 1/4W	可変抵抗器
D1~D4	X65-5110-01	4	Diode 10D-05	ダイオード
D5,D6	X65-5111-01	2	Diode MA-26	ダイオード
	X65-7021-01	2	Protector Switch	過充電防止スイッチ

CANON POCKETRONIC

BATTERY CHARGER 10A

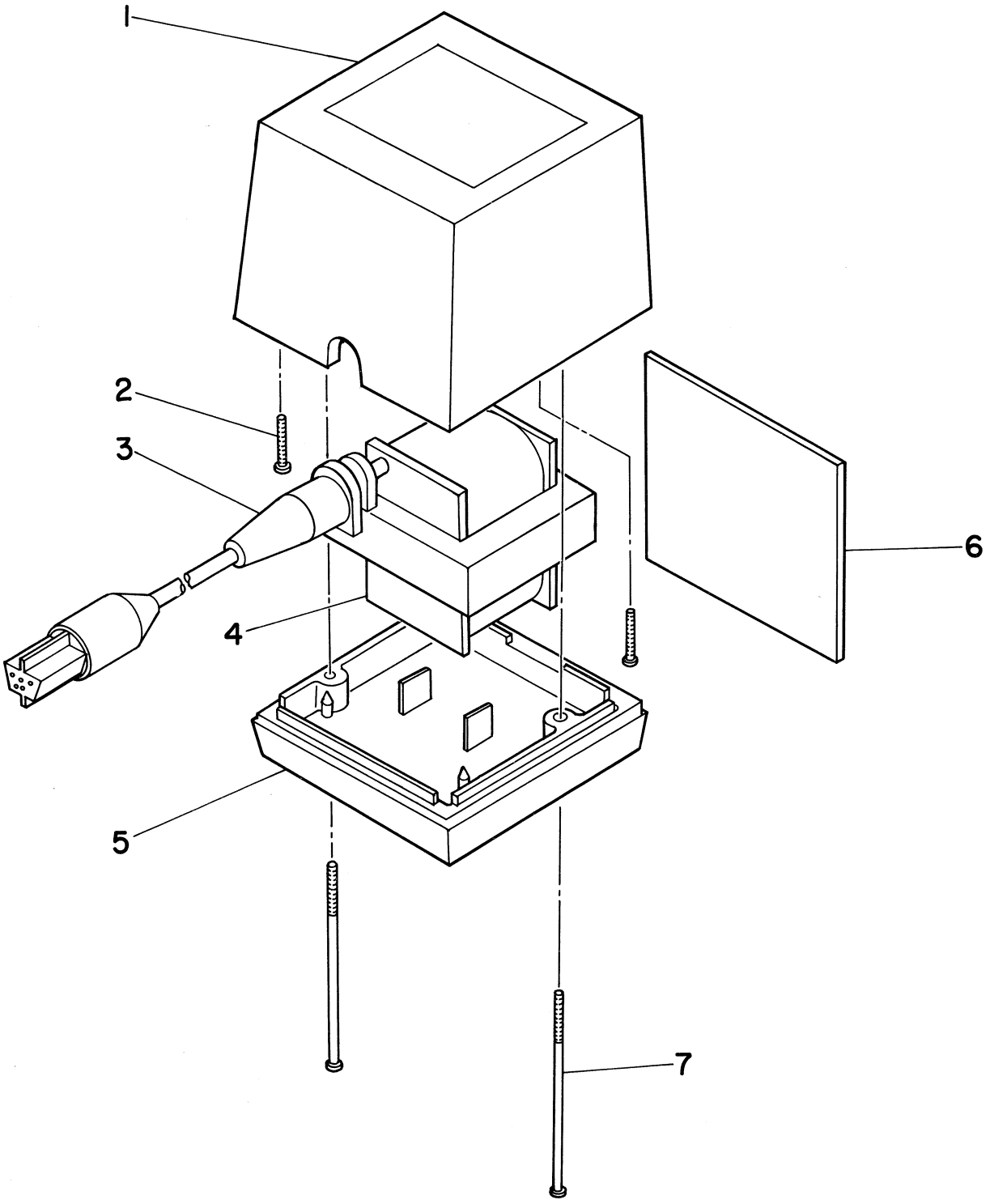
Canon Pocketronic Battery Charger 10A
220V, 240V



Canon Pocketronic Battery Charger 10A
220V, 240V

KEY NO.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
1	Y80-0187-01	1	Upper Cover Unit, 220～240V	上カバーユニット
2	X71-0177-01	2	Screw, BH 2.6 x 17.5	バイントタッピンネジ
3	88-2519-01	1	Curl Cord Unit	カールコードユニット
4	X61-1155-01	1	Power Transformer	電源トランス
5	83-7495-02	1	Base Cover 220V	底カバー
	86-0143-01	1	Base Cover 240V	底カバー
6	Y80-0108-01	1	Charger Card Unit	チャージャーカードユニット
7	X61-7963-01	1	Power Supply Cord 220V	電源コード 220V
	X61-7964-01	1	Power Supply Cord 240V	電源コード 240V
8	X71-0176-01	2	Screw, BH 2.6 x 38	バイントタッピンネジ
*	Y80-0108-01			
	X64-0678-01	1	Carbon Resistor 68Ω T1/2W	炭素被膜固定抵抗器
	X64-0679-01	1	Carbon Resistor 180Ω T1/2W	炭素被膜固定抵抗器
	X65-5100-01	2	Diode IS2080	ダイオード

Canon Pocketronic Battery Charger 10A
100V, 115VUL, 115V



Canon Pocketronic Battery Charger 10A
100V, 115VUL, 115V

KEY NO.	PARTS NO.	UNITS PER ASS'Y	DESCRIPTION	
1	Y80-0186-01	1	Upper Cover Unit 100V	上カバーユニット
	Y80-0187-01	1	Upper Cover Unit 115V	上カバーユニット
2	X71-0177-01	2	Screw, BH 2.6 x 17.5	バイントタッピンネジ
3	88-2519-01	1	Curl Cord Unit	カールコードユニット
4	X61-1155-01	1	Power Transformer	電源トランス
5	89-0733-01	1	Base Cover	底カバー
6	Y80-0108-01	1	Charger Card Unit	チャージャーカードユニット
7	X71-0176-01	2	Screw, BH 2.6 x 38	バイントタッピンネジ
*	Y80-0108-01			
	X64-0678-01	1	Carbon Resistor 68ΩT1/2W	炭素被膜固定抵抗器
	X64-0679-01	1	Carbon Resistor 180ΩT1/2W	炭素被膜固定抵抗器
	X65-5100-01	2	Diode IS2080	ダイオード