INTERIM

FIELD SERVICE MANUAL

KEY-EDIT

SERIES 50 PHASE 1

March 1973

CONSOLIDATED COMPUTER INC

TORONTO - OTTAWA

INTRODUCTION

General

Key Edit 50 is a data preparation system. It consists of several data entry stations, an intermediate storage device, a final storage device, and a computer to control the flow of data. The block diagram (Figure 1) shows the printed circuit boards and interconnections used in a Phase 1 system.

Data Entry Stations

Key-Edit 1000 Key Data Terminals (KDT) are used to enter data from source documents to the Series 50 system. The terminal consists of a keyboard and a graphic display. The terminal operator uses the keyboard to transfer the data on the source document to the system core memory. Information about the batch and record being keyed is displayed for her on the graphic display.

Data is transferred to and from a KDT on a 12 bit data standard interface (12 BDSI) cable. Series 50 transfers KDT data in bit-serial format on a two twisted pair cable. Data transmission from the computer to a KDT involves translating bit-parallel data from the external bus to bit-serial data and then back again to bit-parallel form. Data reception involves the same translations in reverse order. The Video Control Unit (VCU) Terminal Control pcb interfaces the external bus to four bit-serial lines. At the KDT end of the line, an L/150 Adaptor consisting of a Serial/Parallel Converter and 12 BDSI Simulator interfaces a bit-serial line to the KDT.

Data is received from the keyboard by the programmed I/O facility. Data is transmitted to the graphic display by the direct memory access (DMA) facility. All KDT addressing and all initializing of DMA transfers is done on the VCU DMA Control pcb.

Intermediate Storage Device

A CCI Model 015 Disc is used to store records until a complete batch or set of batches is ready for further processing by another computer.

This rotating magnetic memory consists of a single rotating disc that can store 1.4M 6-bit characters. Data is written bit serially on 128 tracks on both sides of the disc. Each track is divided into 128 sectors of forty 12-bit characters. To maintain software compatability with earlier Key-Edit systems, each disc track is subdivided to appear as two 64-sector tracks.

Data transfers between a disc and core memory are initiated by software. The actual transfer uses the DMA facility. Requests for memory access or break requests are initiated by the Disc Control pcb. The Drum/MTT/VCU Multiplexor sorts all of the peripheral break requests by priority and grants memory access to the highest priority peripheral. The disc has the highest priority in the system.

Data is transferred to and from the disc in bit-serial format. The Disc Data pcb is used to translate between the bit-serial disc and the bit-parallel Derandomizer pcb. The derandomizer is a 6-word buffer used as temporary storage of data in transit between the disc and core memory. It is necessary because the disc transfer rate of 4M bits/second causes conflicts in the timing of memory accesses required by and allowed to the disc.

Final Storage Device

The final storage of data is on magnetic tape. Key-Edit 50 uses a Cipher Model 100X magnetic tape transport (MTT) to record data for further processing by another computer. The following table shows the options available to the customer.

MTT OPTIONS

7-or 9-Track
Read after Write
Overwrite
Tape Speeds (IPS): 45, 37.5, 25, 18.75, or 12.5
Data Density (BPI): 800, 556, 200
Dual Density Combinations (BPI): 800/556, 800/200, 566/200
Local Density Selection
Facade Colour (white is standard)

Data transfer between the MTT and core memory uses the DMA facility in the same way that a disc does. These data transfers are initiated by the supervisor when the software informs her that a batch is complete.

Computer

The computer used is a Digital Equipment Corp. PDP-8/E The following is a list of options included with each processor.

Processor	PDP-8/E	
Data Break Interface	KD 8/E	
Positive I/O	KA 8/E	
Memory Extension Control	MC 8/E	
8k Core	MM 8/EJ	two used
Omnibus Expander	BE 8/E	

Options

Key Data Terminal

A maximum of four groups of terminals can be connected to a system. Each group can contain up to four terminals.

Disc

A maximum of four discs can be addressed. The four discs contain 512 tracks and can store 5.6M characters.

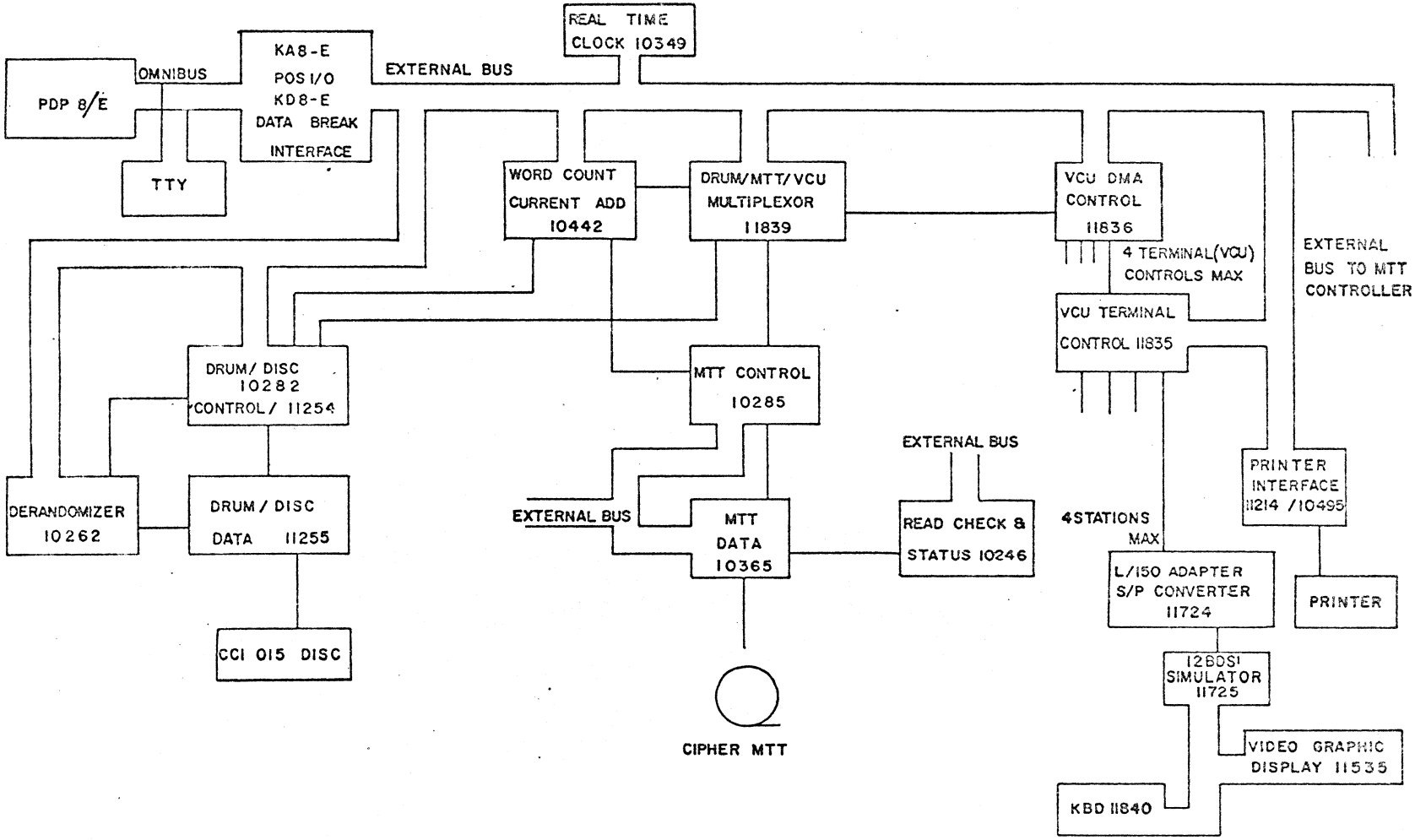
Real Time Clock

The real time clock is a counter that is incremented once a second. The counter output can be read by entering a command through the teletype.

Printers

There are four printers that can be used on a Key-Edit 50. They are:

Centronics Model 101
Centronics Model 101A
Data Products Model 2310
Data Products Model 2410



rev	eco	description	date	by	chk	apprvd

used on

scale | date: 26 FEB 73

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

drawn: R.W.T.

design apprvl

checked

final apprvl

material

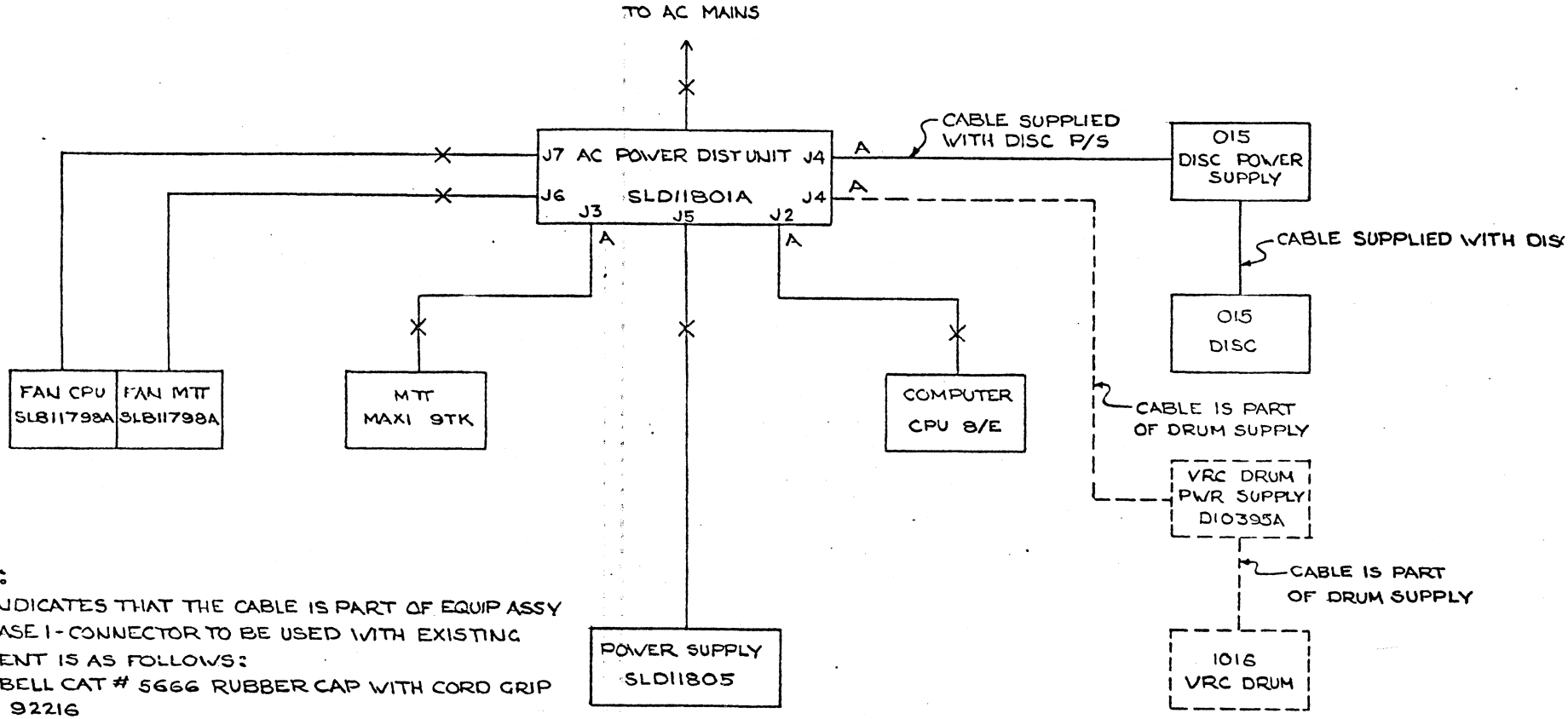
CONSOLIDATED COMPUTER INC. OTTAWA

SERIES 50
PHASE I
BLOCK DIAGRAM

title

sheet of

no.



NOTES:

1 —X— INDICATES THAT THE CABLE IS PART OF EQUIP ASSY

2 FOR PHASE I - CONNECTOR TO BE USED WITH EXISTING EQUIPMENT IS AS FOLLOWS:
A - HUBBELL CAT # 5666 RUBBER CAP WITH CORD GRIP
CCI No 92216

rev	eco	description	date	by	chk	approvd
1		PRE PROD REL	17JAN73			

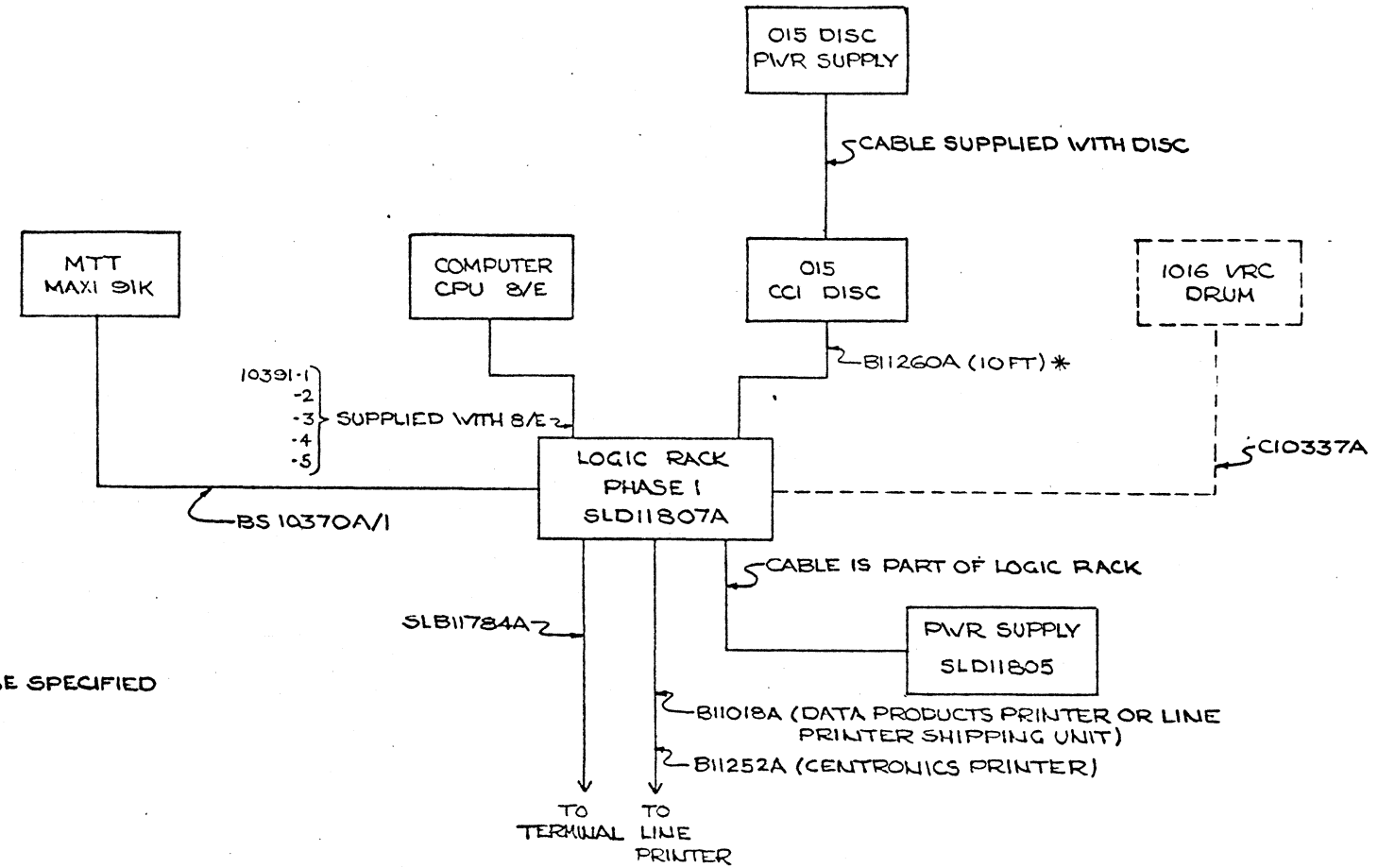
used on: SERIES L PHASE I
scale / date: 12 JAN 73
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
drawn
design
checked
final approvl
material
finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: AC CABLES SERIES 50 PHASE I 220/240 V.

sheet 1 of 1

no. SLB11848 I



NOTE:
* LENGTH MUST BE SPECIFIED

rev	description	date	by	chk	approved
1	PRE PROD REL	17 JAN 73			

used on: SERIES L PHASE I
scale / date: 15 JAN 73
unless specified
00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0 30'
drawn
design
checked
material
finish

CONSOLIDATED COMPUTER INC.
OTTAWA

title: D.C CABLES SERIES 80 PHASE I 220/240 V

sheet of

SLB11850I

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ILLUSTRATIONS

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(Cont'd)

APPENDICES

12 Bit Data Standard Interface

SERIES L KEY DATA TERMINAL SUBSYSTEM

General

The Series L Video Keystation subsystem consists of a CCI Series 1000 Data Terminal and a Series L Video Keystation Controller. (Figure 1).

The Series L Keystation Controller consists of a Video Control Unit located in the System cabinet and an L/150 Adapter located in the Series K terminal.

The CCI Series 1000 Keystation consists of a Series 1000 Keyboard and a Series 1000 Graphic Display. It will be referred to in this manual as a Series K terminal (KDT). SERIES K TERMINAL

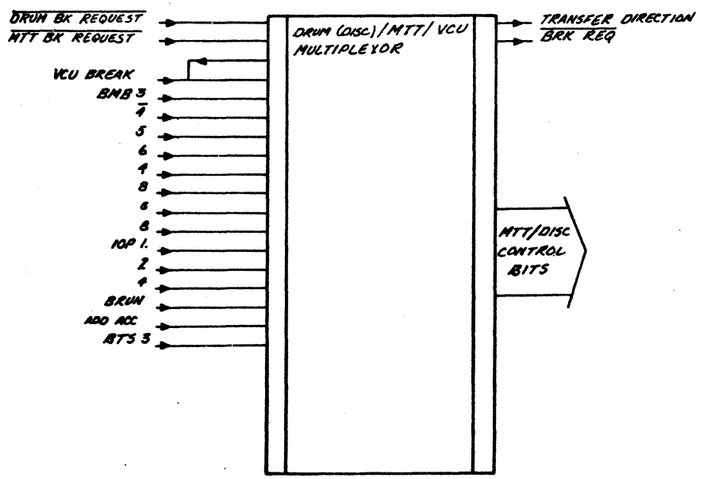
Video Control Unit

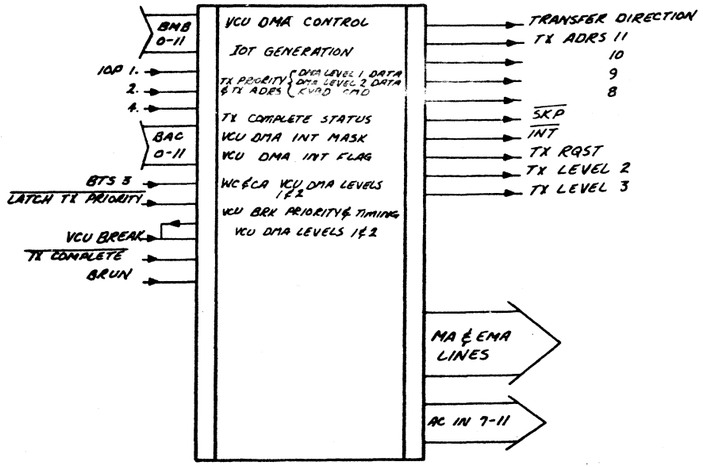
The Video Control Unit (VCU) consists of three printed circuit boards. They are the VCU Terminal Control, the VCU DMA Control and the Drum (Disc)/MTT/VCU Multiplexor. These three cards control three levels of transmission to the Series K terminal and one level of reception from the terminal. The three levels of transmission consist of two levels of single cycle direct memory access (DMA) and one level of program interrupt. The two DMA levels are used to display information on the Series 1000 Video Graphic Display and the program interrupt transmits commands to the Series 1000 Keyboard. Reception from the Series 1000 Keyboard is by program interrupt.

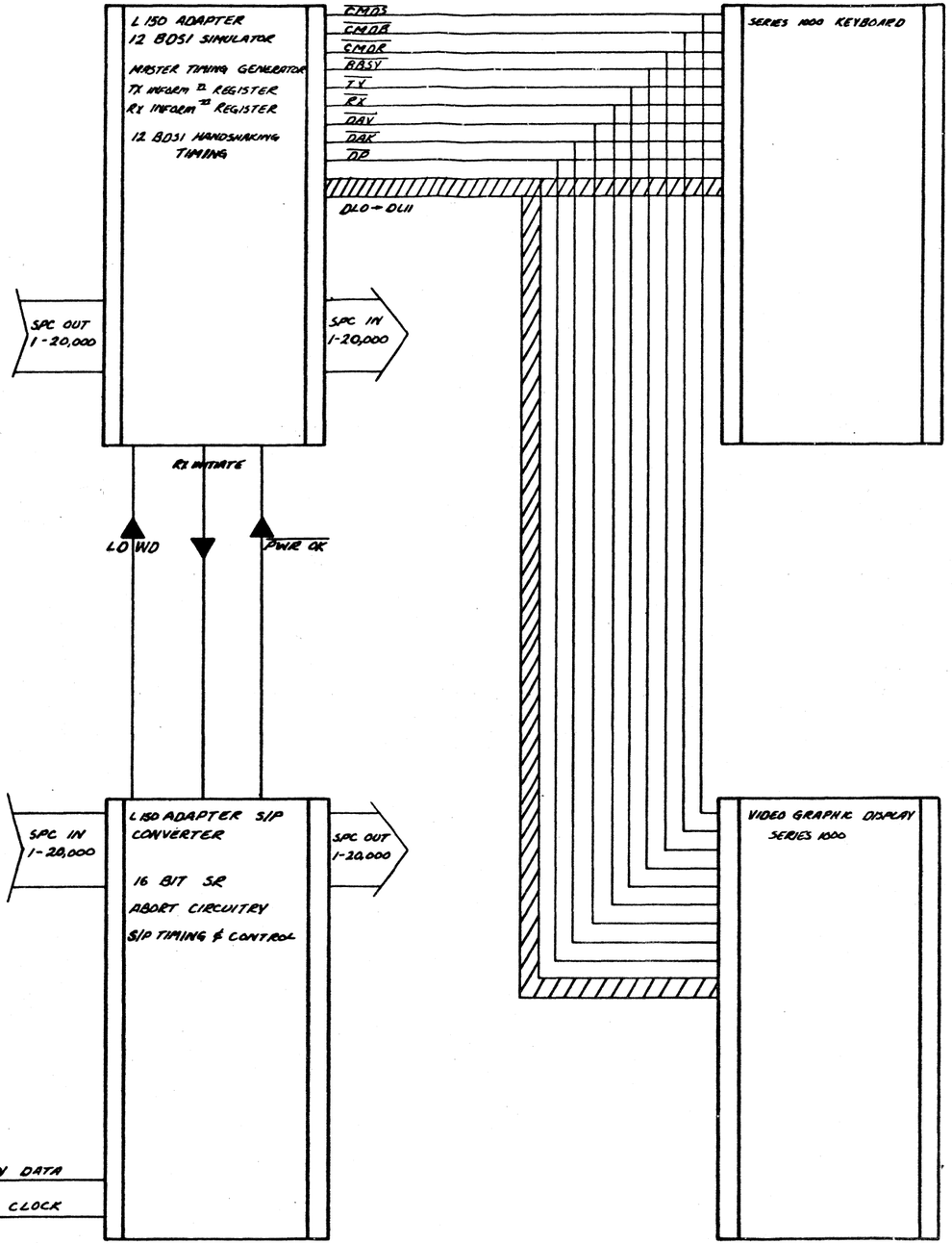
Data transfer to and from the VCU is serial mode on a twisted pair cable for each Series K terminal.

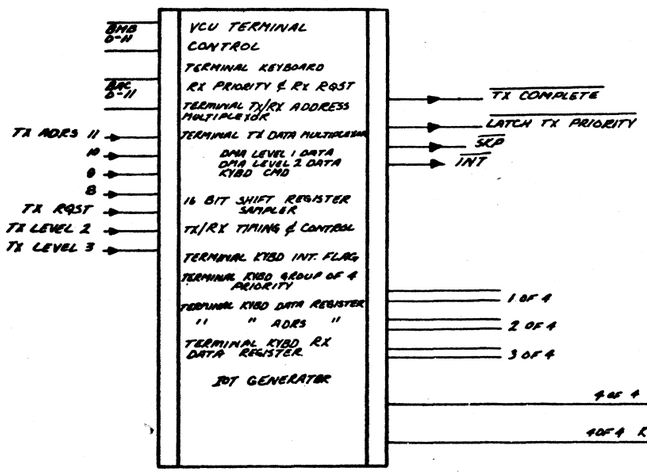
L/150 Adapter

The L/150 Adapter consists of two cards. They are the Serial/Parallel Converter and the 12 BD SI Simulator. These two cards interface the VCU to the Series K terminal. (Figure 2.)









rev	eco	description	date	by	chk	approvd

used on		drawn R.W.T	CONSOLIDATED COMPUTER INC. OTTAWA
proto	date 4 JAN 73	design apprvl	
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0 30'		checked	
		final apprvl	
material	finish	title	DATA TERMINAL SUBSYSTEM BLOCK DIAGRAM.
		sheet of	no. FIGURE 1 rev

TRANSTEX 10 220-0-72

FIGURE 2

L/150 ADAPTER 100V 1 PHASE 1

FUNCTIONAL REPRESENTATION

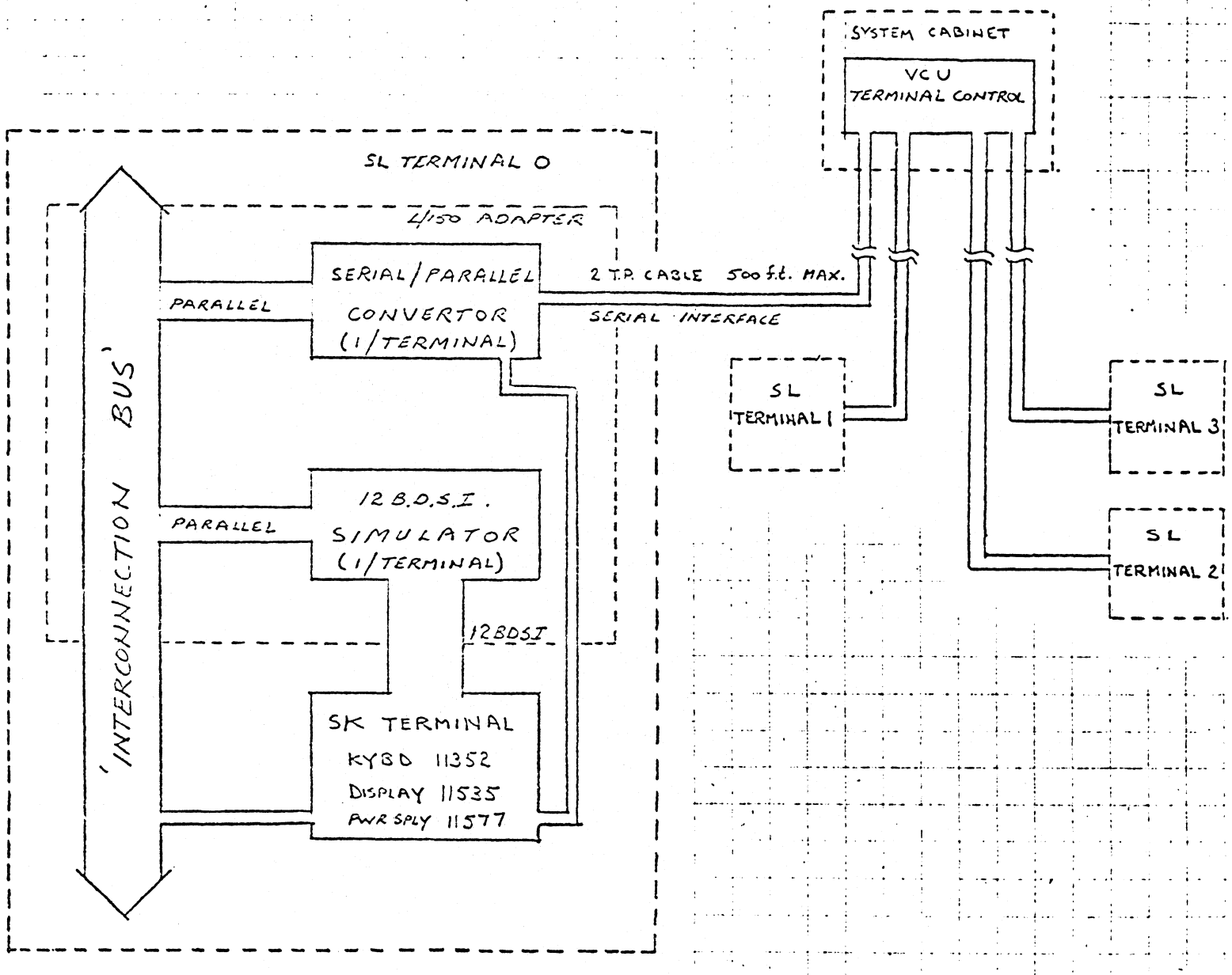
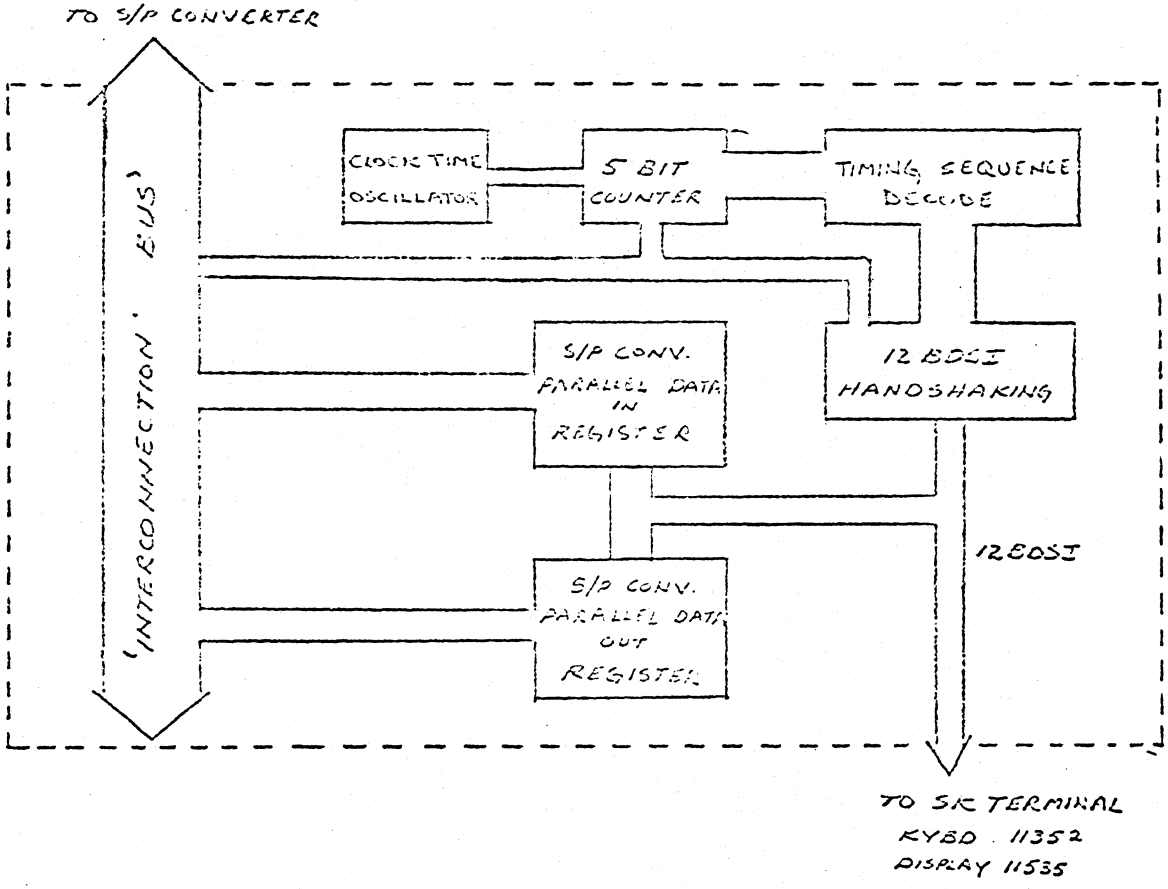


FIGURE 3

12 BDSI SIMULATOR 100 V, PHASE 1 & PHASE 2

FUNCTIONAL REPRESENTATION



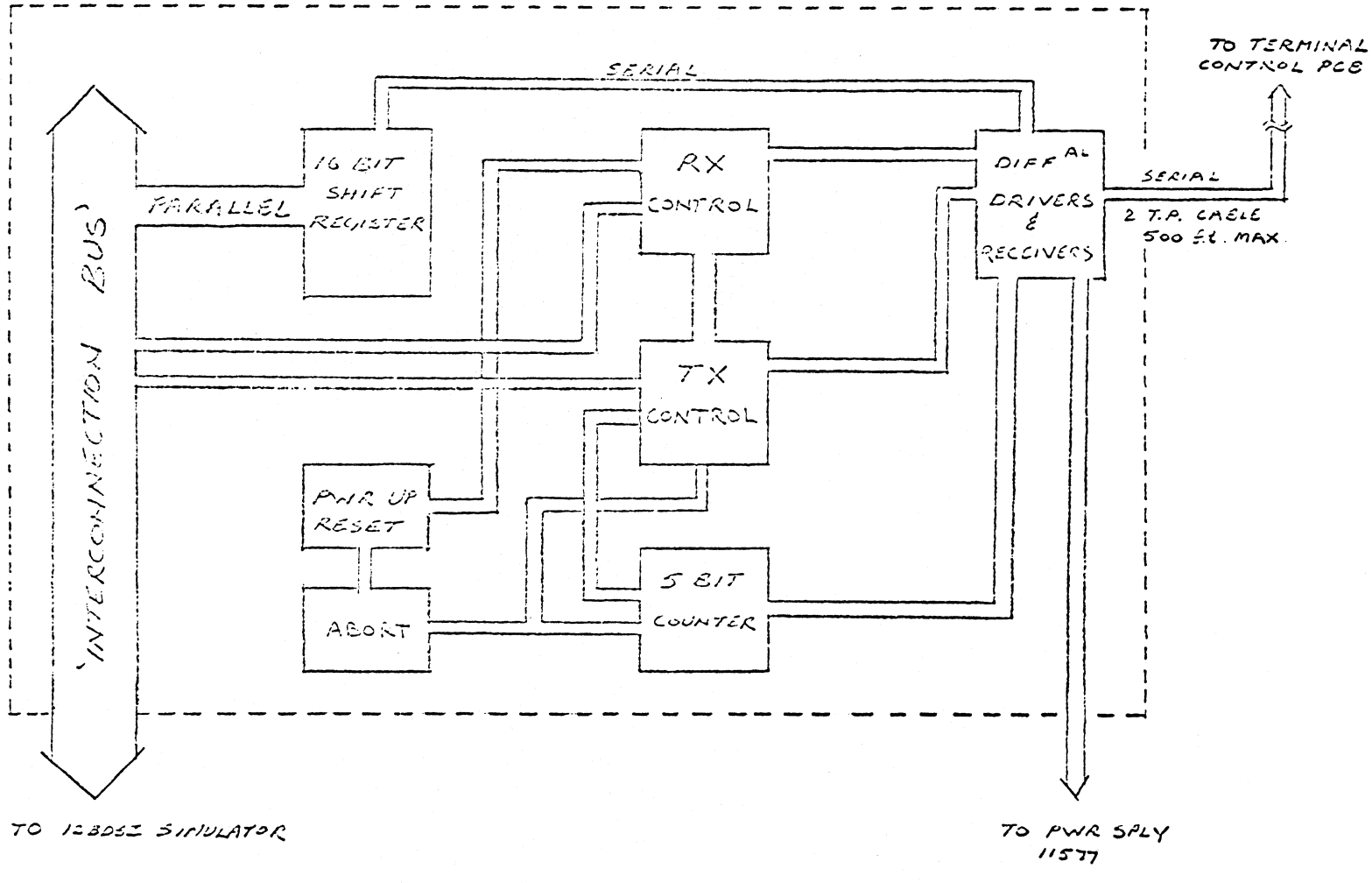
S/P Converter (Figure 4, D11724L) PCB 11724

Circuit	Function
16 Bit Shift Register	Register used to shift data between the VCU Terminal Control and the 12 BDSI simulator. Inputs are the signals SPC IN xxxx and Data Serial In (DS IN) Outputs are SPC OUT xxxx and Data Serial Out ($\overline{\text{DS OUT}}$).
Abort Circuit	Resets the control circuits if a data transfer to or from the VCU Terminal Control is not completed within a 20 μs time slot.
S/P Timing and Control	Produces the control bits to condition the 16 bit shift register and the data line. Loads the data into the 12 BDSI simulator.

FIGURE 4

S/P CONVERTOR 100V, PHASE 1 & PHASE 2

FUNCTIONAL REPRESENTATION



Video Control Unit Circuit Functions

VCU DMA Control (Figure 5, SLD 11836L) PCB 11836

Circuit	Function
IOT Generator	Generates IOT pulses from IOT commands.
Transmit Priority and Address	Senses the level of transmission in use and enables the proper transmit address register.
Transmit Status	Provides a flag when a transmission is finished and contains the level information for that transmission.
Word Count Registers	Two registers that contain the word count for the two levels of DMA.
Current Adrs Registers	Two registers that contain the current address for the two levels of DMA.
Break Timing	Sorts VDU break requests by priority and requests a DMA cycle.

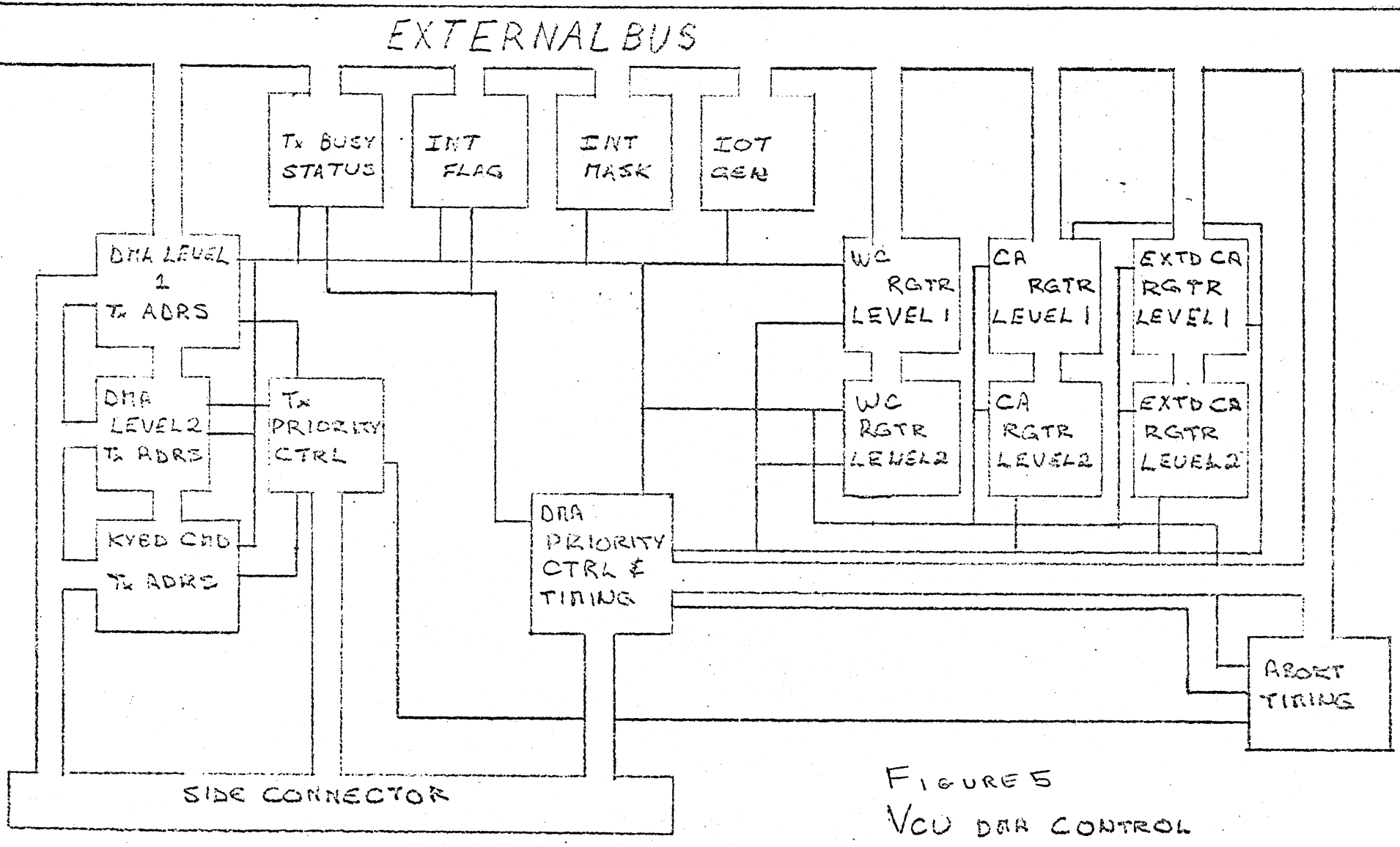


FIGURE 5
VCU DAR CONTROL
BLOCK DIAGRAM

VCU Terminal Control (Figure 6, C11835L) PCB 11835

Circuit	Function
16 Bit Shift Register	Transfers data between the parallel CPU lines and the serial L/150 lines.
Data Multiplexor	Multiplexes three registers of data and loads the 16 bit shift register according to the level of transmission enabled by the VCU DMA control.
Group Priority	Enables a buffer register to allow the CPU to read the data received from the Series K terminal.
Terminal Priority	Enables Receive Request (RX RQST) and sorts terminal receive priorities from within one group of four terminals.
Terminal Address Selection	Enables the desired terminal during transmission cycle.
Receive Data Register	Latches data received from the keyboard of a terminal until it is read by the CPU.

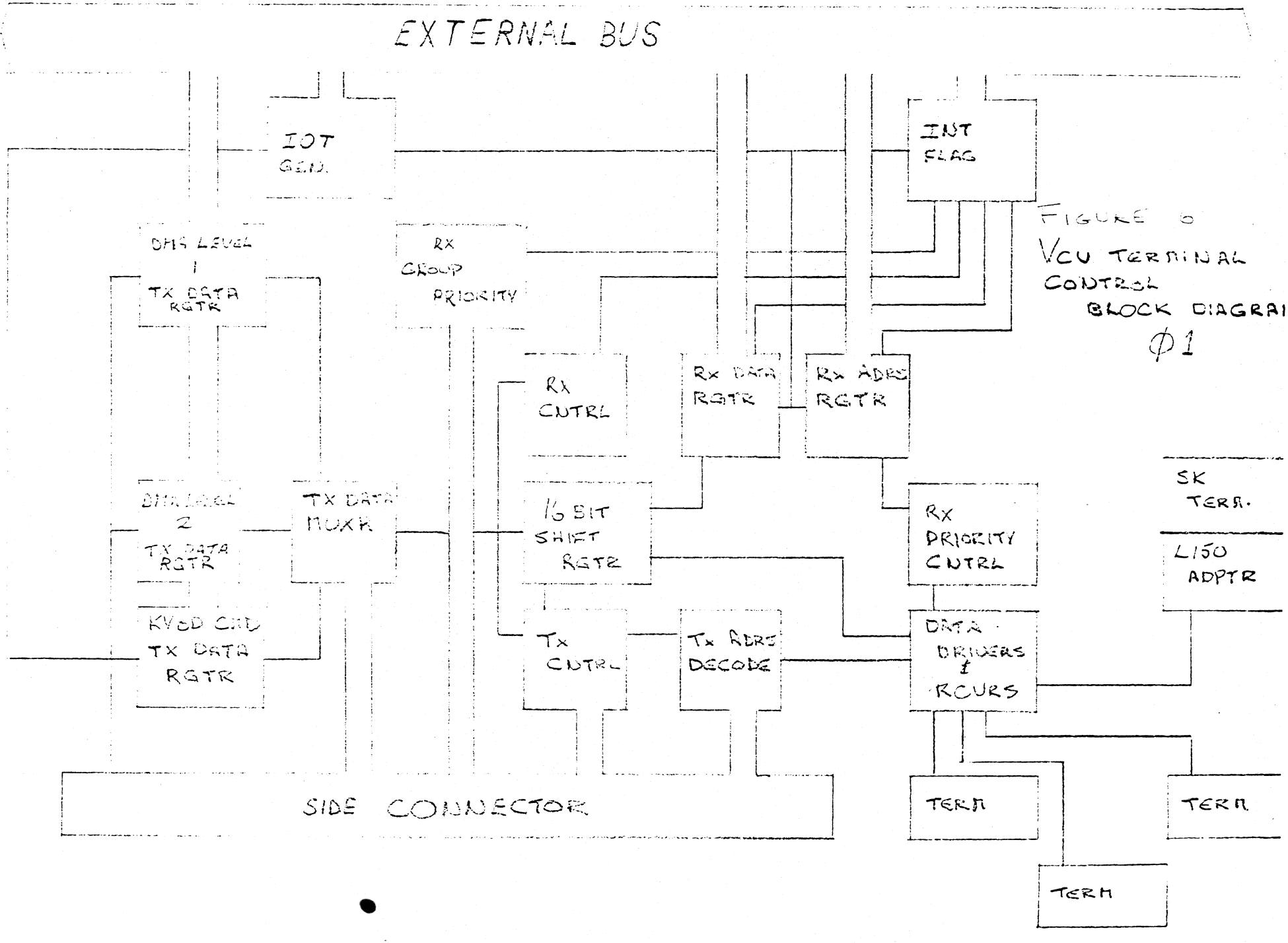


FIGURE 6
VCU TERMINAL CONTROL BLOCK DIAGRAM
$\phi 1$

	1	2	3	4	5	6	7	8	9	10	11	12	13
F									3001				
E											7400		
D											9321	7404	7540
C											7404	75107	7570
B										7402	7401	75107	7540
A										3021	74278	9322	7540

R5 1.2K

SR DATA IN (D8-2,3 F6-2,12)

R16 2.2K — TX ADRS 11 (SIDE pin P)

R13 2.2K — TX ADRS 10 (SIDE pin 15)

R14 2.2K — TX ADRS 9 (SIDE pin R)

R15 2.2K — TX ADRS 8 (SIDE pin 14)

SELECT LINE (E10-5)

R8 2.2K — SECOND 8 JUMPER W1

R7 2.2K — SECOND 4 JUMPER W2

$\overline{\text{SECOND 4}}$ (D10-9) $\overline{\text{SECOND 8}}$ (D10-5)

TX RQST (SIDE PIN 4).

$\overline{\text{TX RQST}}$ (E10-2)

Rx ADRS 21 (E2-13) RX ADRS 2° (E2-14)

RX RQST (E10-12)

$\overline{\text{LATCH RX PRIORITY}}$ (E10-8)

DS OUT (E12-8)

TX DATA ENBL (F13-6)

LINE CLOCK (E12-4)

KYSTN 0 DATA / KYSTN 0 CLOCK

KYSTN 1 DATA / KYSTN 1 CLOCK

KYSTN 2 DATA / KYSTN 2 CLOCK

KYSTN 3 DATA / KYSTN 3 CLOCK

rev	eco	description	date	by	chk	approvd
2	SL 033	CLEAN UP DWG ERRORS	12MAR73	WB		
1		PRE PRODUCTION RELEASE	17-JAN 73	DW		

used on SLC11835A — drawn D WALSH — scale / — date 17-JAN73 — design ENG D WALSH — checked — final apprvl

unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles ± 0 30'

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title: VCU TERMINAL CONTROL SERIES 4 - PHASE 1

sheet 1 of 5 — no. SLB11835L — 2 rev

DMA BUS PIN #

41 DMA MO 4000 — A9 — BMO 4000
44 DMA MO 400 — A9 — BMO 400
45 DMA MO 200 — A8 — BMO 200
46 DMA MO 100 — A9 — BMO 100
47 DMA MO 40 — A9 — BMO 40
48 DMA MO 20 — A8 — BMO 20
49 DMA MO 10 — A8 — BMO 10
50 DMA MO 4 — A8 — BMO 4
51 DMA MO 2 — A6 — BMO 2
52 DMA MO 1 — A6 — BMO 1

AC BUS PIN #

14 BAC 400 — A5 — BBAC 400
15 BAC 200 — A5 — BBAC 200
16 BAC 100 — A5 — BBAC 100
17 BAC 40 — A5 — BBAC 40
18 BAC 20 — A4 — BBAC 20
19 BAC 10 — A4 — BBAC 10
20 BAC 4 — A4 — BBAC 4
21 BAC 2 — A6 — BBAC 2
22 BAC 1 — A6 — BBAC 1

DMA BUS PIN #
16 B INITIALIZE — A4 — D2 — B B INITIALIZE (E9-4)
B B INITIALIZE (F3-5)

	1	2	3	4	5	6	7	8	9	10	11	12	13
F													
E													
D		7432											
C					8309	8309	8309	8309	8309	384			
B				4015	74174	4015	74174	4015	74174				
A				384	384	384		384	384				

DISPLAY DATA REGISTER 1

BMO 4000 — B9 — DDR1 4000
BMO 400 — B9 — DDR1 400
BMO 200 — B9 — DDR1 200
BMO 100 — B9 — DDR1 100
BMO 40 — B9 — DDR1 40
BMO 20 — B9 — DDR1 20

BMO 10 — B8 — DDR1 10
BMO 4 — B8 — DDR1 4
BMO 2 — B8 — DDR1 2
BMO 1 — B8 — DDR1 1

DDR1C (SIDE PIN N) — C10 — 3,4,5,11,12

DISPLAY DATA REGISTER 2

BMO 4000 — B7 — DDR2 4000
BMO 400 — B7 — DDR2 400
BMO 200 — B7 — DDR2 200
BMO 100 — B7 — DDR2 100
BMO 40 — B7 — DDR2 40
BMO 20 — B7 — DDR2 20

BMO 10 — B6 — DDR2 10
BMO 4 — B6 — DDR2 4
BMO 2 — B6 — DDR2 2
BMO 1 — B6 — DDR2 1

DDR2C (SIDE PIN S) — C10 — 3,4,5,11,12

COMMAND DATA REGISTER

BBAC 400 — B5 — CDR 400 (C9-10)
BBAC 200 — B5 — CDR 200
BBAC 100 — B5 — CDR 100
BBAC 40 — B5 — CDR 40
BBAC 20 — B5 — CDR 20

BBAC 10 — B4 — CDR 10
BBAC 4 — B4 — CDR 4
BBAC 2 — B4 — CDR 2
BBAC 1 — B4 — CDR 1

6351 (D3-10) — 3,4,5,11,12

DDR1 400 — C9 — SRPD IN 400 (D6-7) (DL8)
DDR2 400
CDR 400
DDR1 200 — SRPD IN 200 (D7-4) (DL7)
DDR2 200
CDR 200

DDR1 100 — C8 — SRPD IN 100 (D7-5) (DL6)
DDR2 100
CDR 100
DDR1 40 — SRPD IN 40 (D7-6) (DL5)
DDR2 40
CDR 40

DDR1 20 — C7 — SRPD IN 20 (D7-7) (DL4)
DDR2 20
CDR 20
DDR1 10 — SRPD IN 10 (D5-4) (DL3)
DDR2 10
CDR 10

DDR1 4 — C6 — SRPD IN 4 (D5-5) (DL2)
DDR2 4
CDR 4
DDR1 2 — SRPD IN 2 (D5-6) (DL1)
DDR2 2
CDR 2

DDR1 1 — C5 — SRPD IN 1 (D5-7) (DL0)
DDR2 1
CDR 1

DDR1 4000
DDR2 4000
Vcc — C5 — 1 SRPD IN 10000 (CMBR) (D8-7)

C10 — TX LEVEL (SIDE PIN E)
C10 — TX LEVEL (SIDE PIN J)
SRPD IN 1000 (D6-6) (DL 9)

rev	eco	description	date	by	chk	apprvd
2		SEE SHT 1				
1		PRE PRODUCTION RELEASE	17-JAN-73	DWALSH		

used on: SLC1835A
scale:
date: 17-JAN-73
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ±0 30'
D WALSH drawn
D WALSH design
checked
final apprvl
material
finish

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sheet 2 of 5
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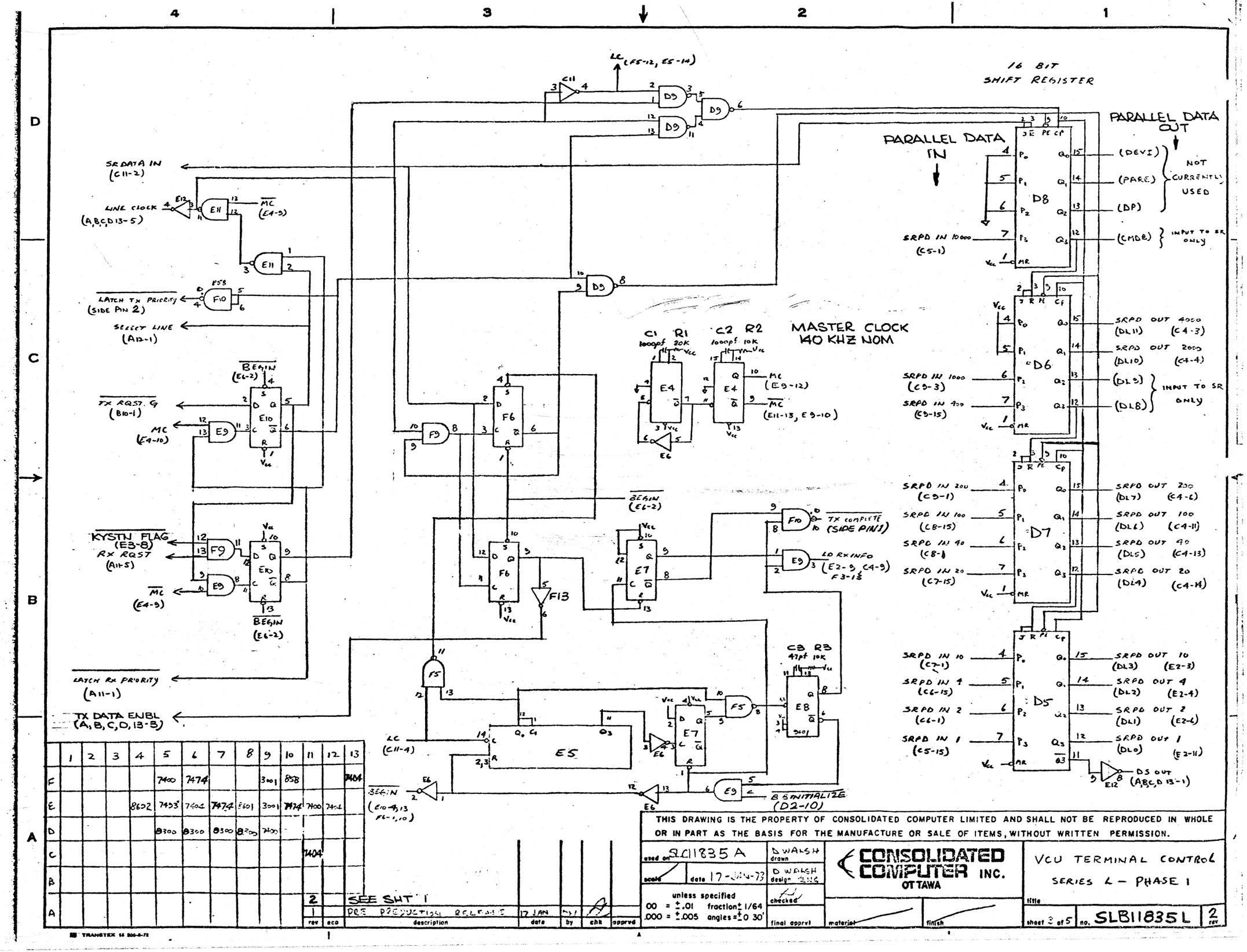
2 rev


16 BIT SHIFT REGISTER
PARALLEL DATA IN
PARALLEL DATA OUT
D8
D6
D7
D5
(DEVI)
(PARE)
(DP)
NOT CURRENTLY USED
(CMDB)
INPUT TO SR ONLY
SRPD OUT 4000 (DL11) (C4-3)
SRPD OUT 2000 (DL10) (C4-4)
(DL9)
(DL8)
SRPD OUT 200 (DL7) (C4-6)
SRPD OUT 100 (DL6) (C4-11)
SRPD OUT 40 (DL5) (C4-13)
SRPD OUT 20 (DL4) (C4-14)
SRPD OUT 10 (DL3) (E2-3)
SRPD OUT 4 (DL2) (E2-4)
SRPD OUT 2 (DL1) (E2-6)
SRPD OUT 1 (DL0) (E2-11)
DS OUT (A,B,C,D 13-1)
MASTER CLOCK 140 KHZ NOM
C1 R1 1000pf 20K
C2 R2 1000pf 10K
C3 R3 47pf 10K
LC (E5-12, E5-14)
SR DATA IN (C11-2)
LINE CLOCK (A,B,C,D 13-5)
LATCH TX PRIORITY (SIDE PIN 2)
SELECT LINE (A12-1)
TX RQST. G (B10-1)
KYSTN FLAG (E3-8)
RX RQST (A11-5)
LATCH RX PRIORITY (A11-1)
TX DATA ENBL (A,B,C,D,13-8)
TX COMPLETE (SIDE PIN 1)
LD RX INFO (E2-9, C4-9) F3-13
LC (C11-4)
B INITIALIZE (D2-10)
BEGIN (E6-2)
MC (E4-9)
MC (E4-10)
MC (E11-13, E9-10)
MC (E9-12)
SEE SHT 1
PRE PRODUCTION RELEASE
17 JAN
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used on 9C11835A
D WALSH drawn
date 17-JAN-73
D WALSH design
checked
final apprvl
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material
finish
CONSOLIDATED COMPUTER INC. OTTAWA
VCU TERMINAL CONTROL SERIES L – PHASE 1
title
sheet 3 of 5
no. SLB11835L
2 rev
TRANSTEK 15 800-8-72

	1	2	3	4	5	6	7	8	9	10	11	12	13
F		7402	7404								8309	7427	7404
E		7474	7474									7404	7401
D										7404	3321		
C				74174									
B	858	858											
A	858	858	858										

RX DATA REGISTER

ACC BUS PIN #
58 $\overline{AC\ 0}$
59 $\overline{AC\ 1}$
62 $\overline{AC\ 4}$
63 $\overline{AC\ 5}$
64 $\overline{AC\ 6}$
65 $\overline{AC\ 7}$
66 $\overline{AC\ 8}$
67 $\overline{AC\ 9}$
68 $\overline{AC\ 10}$
69 $\overline{AC\ 11}$

RX DATA REG 1000 (C4-2)
RX DATA REG 400 (C4-5)
RX DATA REG 200 (C4-7)
RX DATA REG 100 (C4-10)
RX DATA REG 40 (C4-12)
RX DATA REG 20 (C4-15)
RX DATA REG 10 (E2-2)
RX DATA REG 4 (E2-5)
RX DATA REG 2 (E2-7)
RX DATA REG 1 (E2-10)

(B RX ADRS 8)
(B RX ADRS 4)
B RX ADRS 2 (E2-13)
B RX ADRS 1 (E2-15)

SRPD OUT 1000 (D6-15)
SRPD OUT 2000 (D6-14)
SRPD OUT 200 (D7-15)
SRPD OUT 100 (D7-14)
SRPD OUT 40 (D7-13)
SRPD OUT 20 (D7-12)
C4
RX DATA REG 1000 (A3-8)
RX DATA REG 400 (A3-12)
RX DATA REG 200 (A3-1)
RX DATA REG 100 (A3-5)
RX DATA REG 40 (A2-5)
RX DATA REG 20 (A2-12)

SRPD OUT 10 (D5-15)
SRPD OUT 4 (D5-14)
SRPD OUT 2 (D5-13)
SRPD OUT 1 (D5-12)
RX ADRS 2 (F9-3)
RX ADRS 1 (F9-6)
74174
E2
RX DATA REG 10 (A2-1)
RX DATA REG 4 (A2-5)
RX DATA REG 2 (A1-13)
RX DATA REG 1 (A1-8)
B RX ADRS 2 (A1-1)
B RX ADRS 1 (A1-6)

LD RX INFO (E9-3)
B INITIALIZE (A4-3)

ACC BUS D851
57 $\overline{SKP}$
56 $\overline{INT}$

KYSTN FLAG (F9-12)

LATCH GROUP PRIORITY (F2-1)
FH
F12
LR9 2.2K PRIORITY 0-3 (SIDE PIN A)
LR10 2.2K PRIORITY 4-7 (SIDE PIN C)
LR11 2.2K PRIORITY 10-13 (SIDE PIN D)
LR12 2.2K PRIORITY 14-17 (SIDE PIN E)

SECOND 4 (A10-1)
SECOND 8 (A10-4)

D11
7401
$\overline{PRIORITY\ 0-3}$ (SIDE PIN A)
PRIORITY 4-7 (SIDE PIN C)
PRIORITY 10-13 (SIDE PIN D)
PRIORITY 14-17 (SIDE PIN E)

6331 (D3-1)
6332 (D3-4)
6334 (D3-13)

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rev	eco	description	date	by	chk	approvd
2		SEE SHT 1				
1		PRE PRODUCTION RELEASE	17-JAN-73	DWA		

used on SLC11935A | drawn DWALSH | date 17-JAN-73 | design ENG DWALSH | checked | final approval

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ±0 30'

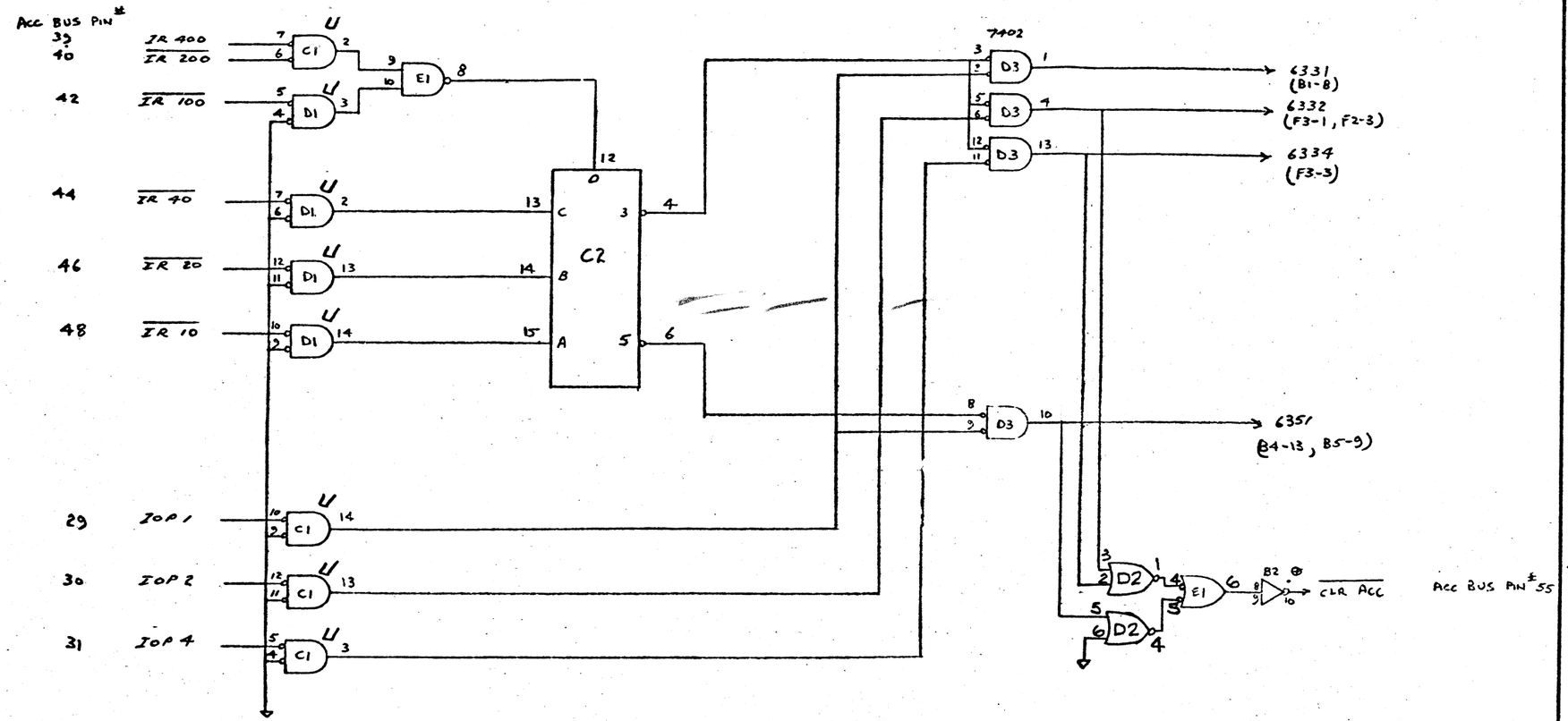
material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: VCU TERMINAL CONTROL SERIES L - PHASE L

sheet 4 of 5 | no. SLB11835L | 2 rev

TRANSTEX 15 880-6-72



	1	2	3	4	5	6	7	8	9	10	11	12	13
F													
E	7400												
D	380	7402	7402										
C	380	7442											
B		859											
A													

rev	eco	description	date	by	chk	apprvd
2		SEE SHT 1				
1		PRE PRODUCTION RELEASE	17-JAN 73	DW		

used on SLB11835A | drawn D WALSH | scale | date 17-JAN 73 | design | checked | final apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

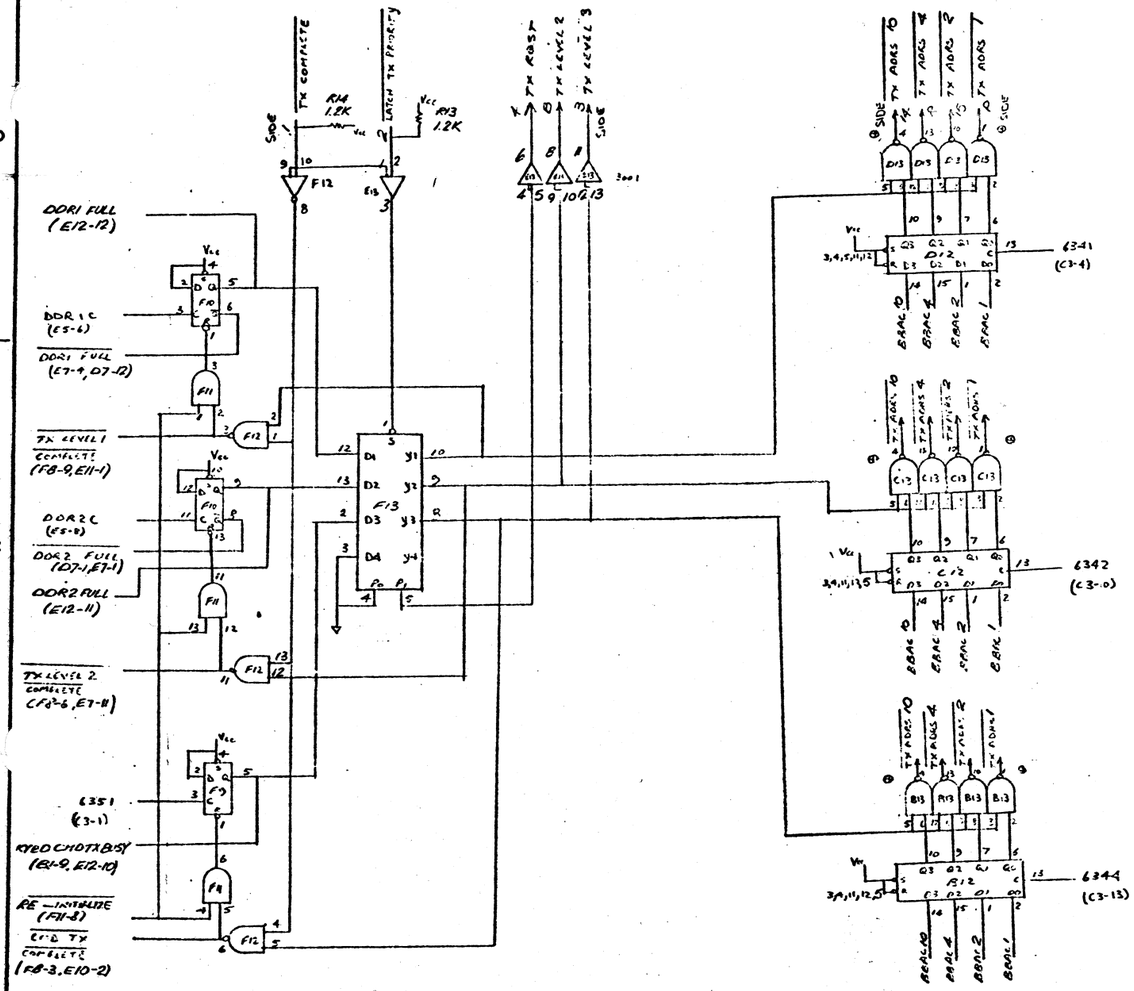
material | finish

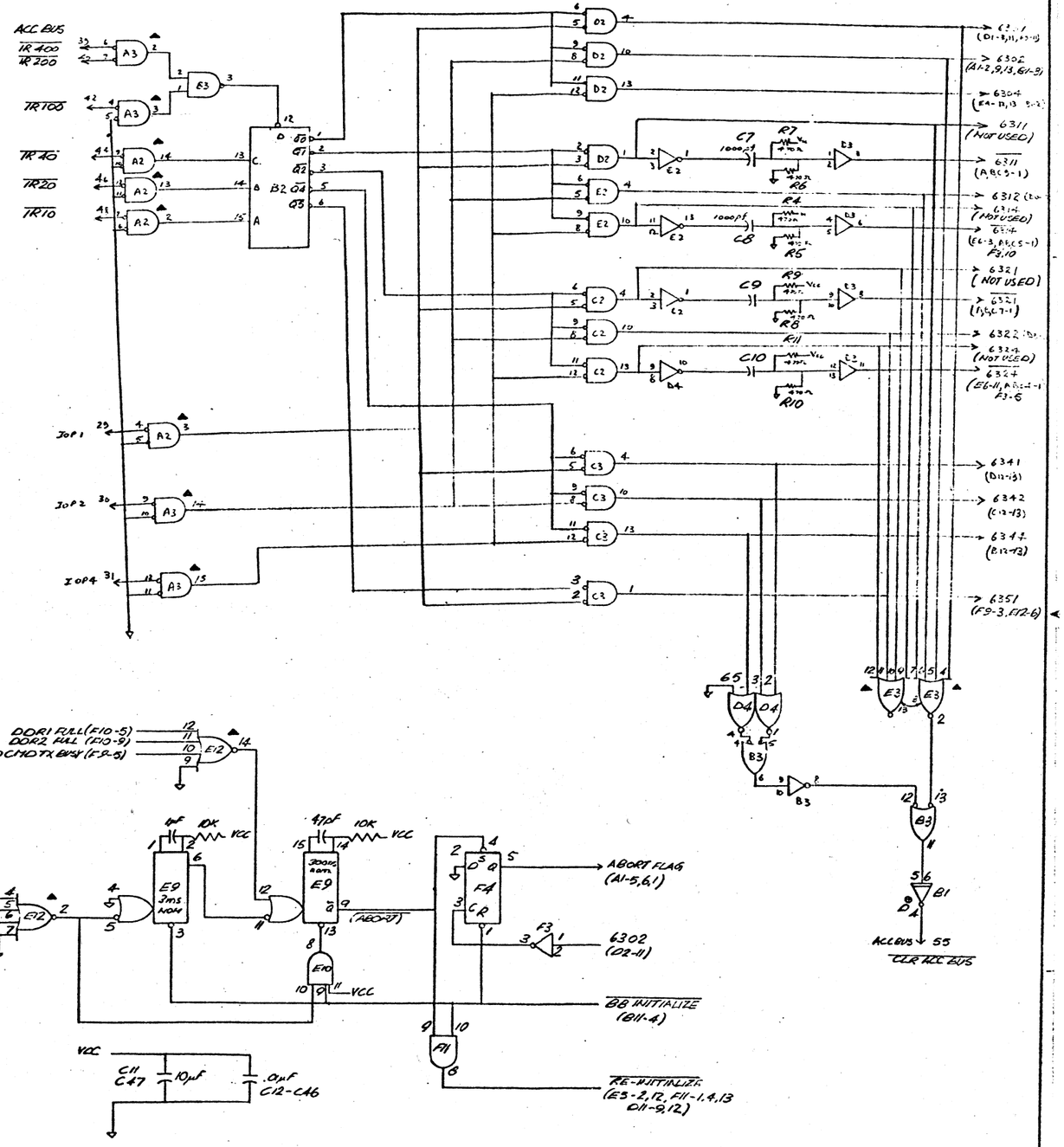
CONSOLIDATED COMPUTER INC. OTTAWA

title: VCU TERMINAL CONTROL SERIES L - PHASE 1

sheet 5 of 5 | no. SLB11835L | 2 rev

TRANSTEX 10 800-0-72





	1	2	3	4	5	6	7	8	9	10	11	12	13
F			7400	7479	2	2	3	4	7113	7112	3001	7400	7276
E		7412	317	2	5	3	2		8602	3006	2	317	7414
D	2	7412	3001	2	2	3	3	2	2	2	2	4015	7401
C	3	7402	7402	2	3	2	2	2	2	2	2	4015	7401
B	858	7442	7400	2	2	3	2	2	2	2	2	4015	7421
A	2	3	2	2	2	2	2	2	2	2	2	2	2

rev	eco	description	date	by	chk	approved
2						
1		PRE PROD RELEASE	15FEB73 17JAN73			

used on	C11836A
scale	date 10 JAN 73
unless specified	.00 = ±.01 fraction = 1/64; .000 = ±.005 angles = 0 30'
drawn	C WALSH
design eng	C WALSH
checked	
final approval	
material	finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: 10U DMA CONTROL SERIES L-PHASE I

sheet 1 of 2 | no. B11836L | rev 2

TX LEVEL 1 COMPLETE (F12-3)

DDR1 FULL (F10-6)

BK LEVEL 1 (F8-8)

6314 (B3-6)

WC OVERFLOW LEVEL 1 (F3-5)

BK LEVEL 1 (D7-13)

BK LEVEL 2 (F8-5)

6324 (D3-11)

RE-INITIALIZE (F11-6)

WC OVERFLOW LEVEL 2 (F3-4)

BK LEVEL 2 (D7-2)

DDR 2 FULL (F10-8)

TX LEVEL 2 COMPLETE (F12-11)

.5ms NOM

NDRIC (F10-3, E12-4)

BDDRIC SIDE

BDDR2C ICE

DDR2C (F10-11, E12-5)

CMA BUS

CMA MA1 · MA2 · MA4 · MA10 · MA20 · MA40 · MA100 · MA200 · MA400 · MA1000 · MA2000 · MA4000 · DMA14 4000

6311 (D3-3)

BBAC 1 · BBAC 2 · BBAC 4 · BBAC 10 · BBAC 20 · BBAC 40 · BBAC 100 · BBAC 200 · BBAC 400 · BBAC 1000 · BBAC 2000 · BBAC 4000

6321 (D3-8)

CMA BUS DMA MA1 · MA2 · MA4 · MA10 · MA20 · MA40 · MA100 · MA200 · MA400 · MA1000 · MA2000 · MA4000

6322 (E2-10)

CMA BUS DMA MAE1 · DMA MAE2 · DMA MAE4

6312 (E2-4)

BBAC 10 · BBAC 20 · BBAC 40

345 11 12

ABORT FLAG (F4-5)

ACC BUS

INT · ACNT0 · ACNT1 · ACNT2 · ACNT3

TX BUS STATUS

NBDCMC TX BUS (F3-5)

BK LEVEL 2 (E6-5)

DDR2 FULL (F10-7)

BK LEVEL 1 (E6-5)

DDR1 FULL (F10-6)

6302 (D2-10)

TX COMPLETE INT. MASK

BBAC 4 (C6-14)

BBAC 2 (C6-3)

BBAC 1 (C6-2)

6301 (D3-4)

BB INITIATE (B11-4)

KYBD CMD

DMA LEVEL1

DMA LEVEL2

CMD TX COMPLETE (F12-6)

BK LEVEL 2 (E6-5)

BK LEVEL 2 COMPLETE (F12-11)

BK LEVEL 1 (E6-5)

BK LEVEL 1 COMPLETE (F12-3)

ABORT (E9-9)

BB INITIALIZE (B11-4)

6304 (D2-12)

ACC BUS B-5 57 SKIP

ACC BUS B-5 56 INT

VCU BRK RQST 19 CMA BUS

RE-INITIALIZE (F11-6)

BTS 3

DMA BUS

C3 .1mfd

C5 1.0 mfd

BB INITIALIZE

(F4-1, E9-3, D11-13, F9-13, C1-1-13, E10-9, F11-10)

C4 100pf

C5 .1mfd

WC OVERFLOW LEVEL 1 (E5-1)

WC OVERFLOW LEVEL 2 (E5-13)

	1	2	3	4	5	6	7	8	9	10	11	12	13
F			7403		8-02	7432	74218	7432	7419	①		①	①
E		⑤	①	7402	3001	7429	3002			3006	3001		①
D	7429	⑤	⑥	7402	836	①	7437	7400	4015	4015	3001	①	①
C	7429	⑤	①	74177	74177	332	74177	858	74177	858	858	①	①
B	858	①	⑤	7429	74177	332	74177	858	74177	858	858	①	①
A	858	①	⑤	74177	74177	384	74177	852	74177	858	7432	836	332

rev	eco	description	date	by	chk	approved
2		PRE PROD. RELEASE				
1						

based on	C 11826A
scale	date JAN 73
unless specified	.00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ± 0 30'
drawn	
design	
checked	
final coord	
material	finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: VCU DMA CONTROL SERIES L — PHASE 1

sheet 2 of 2 | no. B 11826 L | rev 2

TRIANGTEK M 500-0-72

8 7 6 5 4 3 2 1

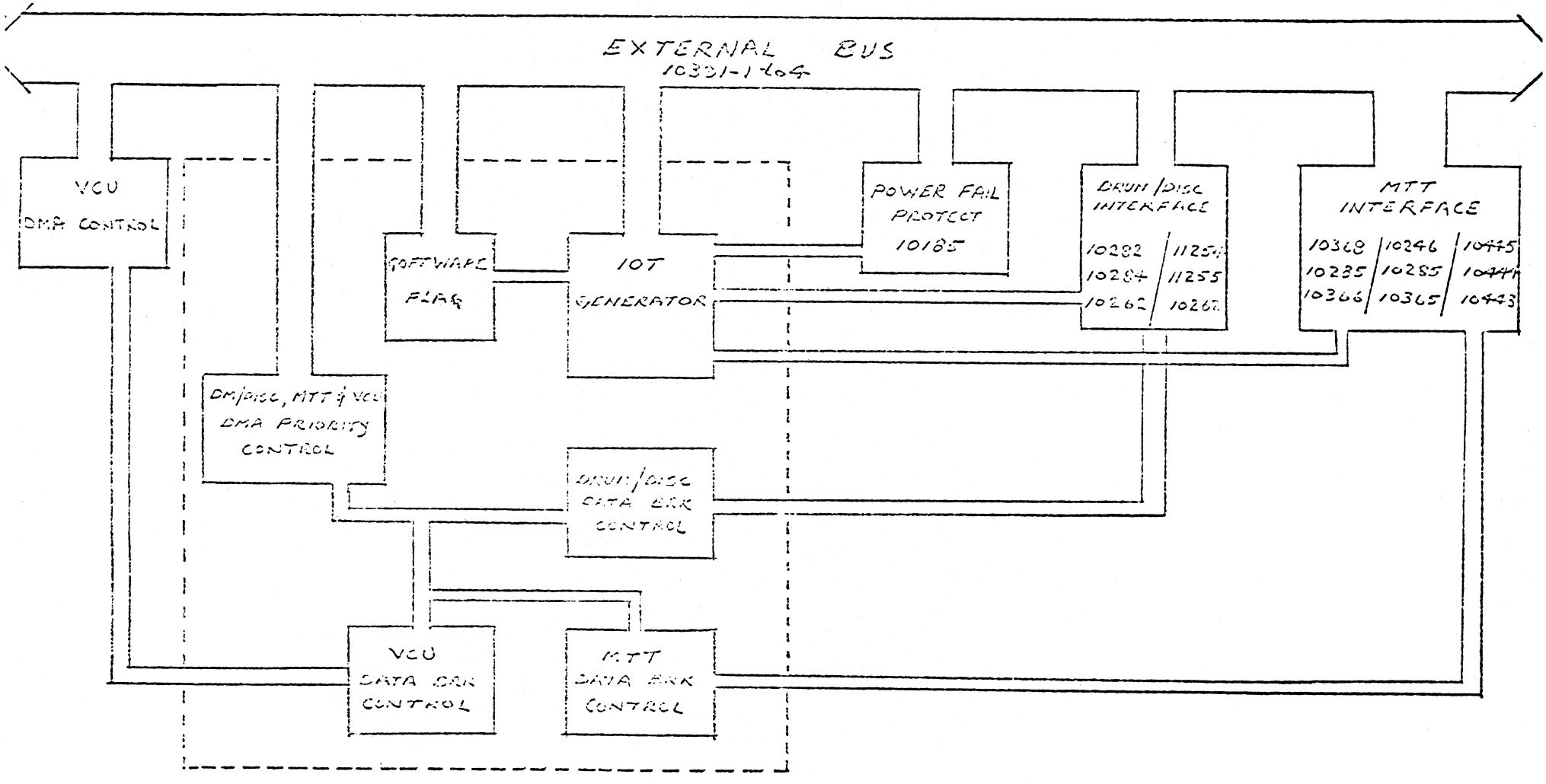
Drum/MTT/VCU Multiplexor (Figure 7, D11839L) PCB 11839

Circuit	Function
Break Priority	Enables direct memory access cycle and sorts peripheral break requests by priority. Inputs are $\overline{\text{DRUM BRK REQ}}$, $\overline{\text{MTT BRK REQ}}$ and VCU BK REQ. Output is $\overline{\text{BRK REQ}}$
Drum and MTT Control	Provides control bits to condition drum and magnetic tape transport controllers. Input is from priority circuit and $\overline{\text{Address Accepted}}$ ($\overline{\text{ADRS ACC}}$) from CPU
IOT Generator	Generates IOT pulses from IOT commands.

FIGURE 7

DRUM, MTT AND VCU MULTIPLEXOR 100V & PHASE 1

FUNCTIONAL REPRESENTATION



CHIP CHART SHT 1					
	1	2	3	4	5
A	——	7430	7404	7400	858
B	——	7410	7442	——	7437
C	——	7430	7400	7437	7437
D	——	——	——	7437	7437
E	——	——	——	7437	7437
F	——	——	7437	——	——
G	——	——	——	7437	7437

BMB3 ← A38
BMB4 ← B38
BMB5 ← B40
B2

BMB6 ← A39
BMB7 ← B41
BMB8 ← B42
B3

IOP1 ← A2
IOP2 ← A4
IOP4 ← B5
BRUN ← A13
VCC ← A1, B1
GND ← A43, B43
C8 10UF
C9-C29 .01UF

R3 470Ω C4 1000PF R2 470Ω
R9 470Ω C6 1000PF R8 470Ω
R5 470Ω C5 1000PF R4 470Ω
R11 470Ω C7 1000PF R10 470Ω

B2 → 6501
B3 → 6501
B4 → 6502
A3 → 6502
A5 → 6504
B6 → 6504
A7 → 6511
A6 → 6511
B8 → 6512
B10 → 6512
A12 → 6514
A11 → 6514
B13 → 6521
B14 → 6521
B15 → 6522
B16 → 6522
B18 → 6524
A18 → 6524
B20 → 6531
B19 → 6531
B22 → 6532
B23 → 6532
B24 → 6534
A24 → 6534
B26 → 6541
B27 → 6541
A31 → 6542
B29 → 6542
B32 → 6544
A33 → 6544
B34 → 6551
A34 → 6551
A35 → 6552
B35 → 6552
B37 → 6554
B36 → 6554
B9 → SKIP
A9 → INT
A22 → 6574
A11 → CLR ACC

rev	eco	description	date	by	chk	approved
1		PRE-PROD RELEASE	17 JAN 73	DJ		

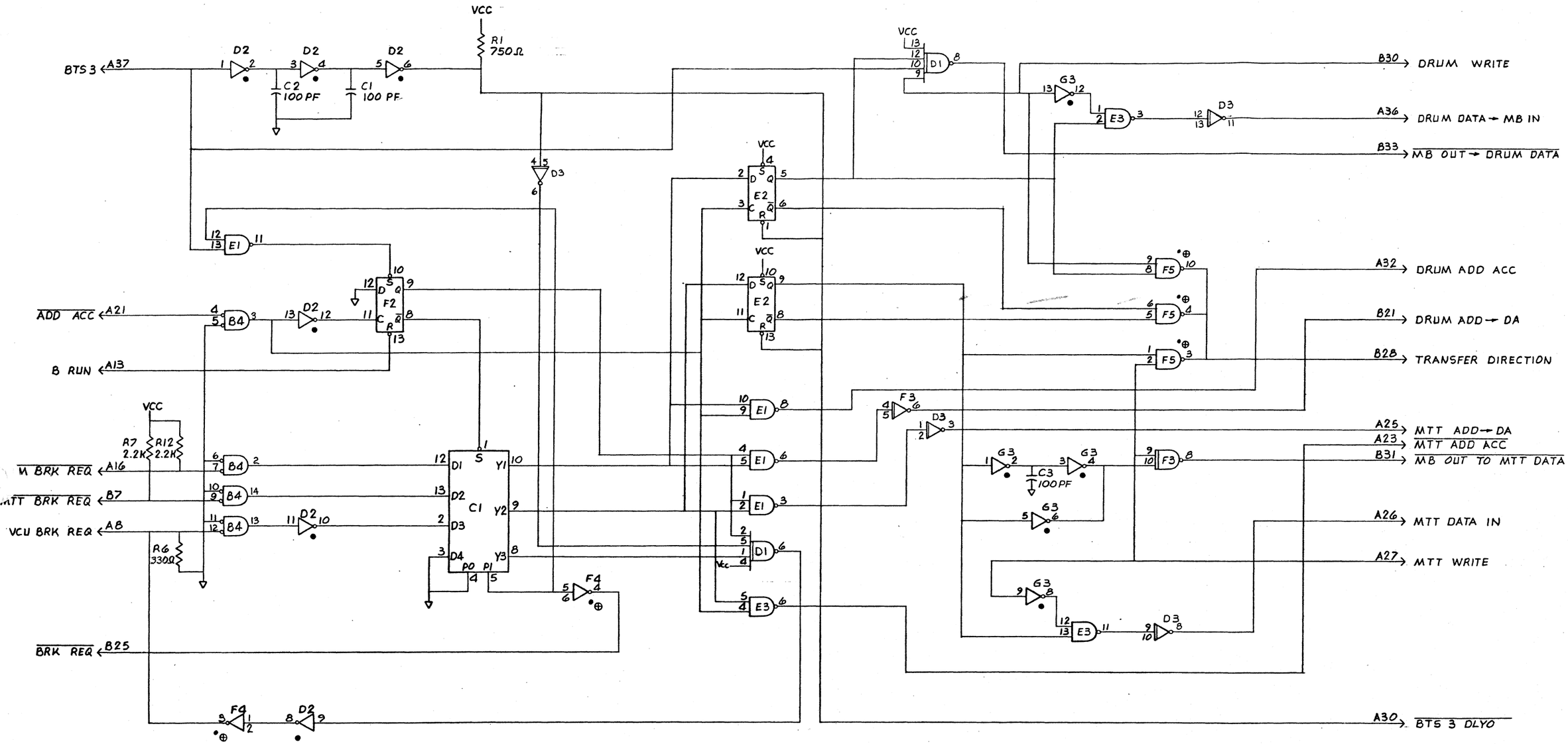
used on SLD11807A / SLD11806A
scale —— date 17 JAN 73
unless specified .00 = ±.01 fraction = 1/64 .000 = ±.005 angles = ±0 30'
drawn DJ
design ENG. D. WALSH
checked
final approval
material
finish

CONSOLIDATED COMPUTER INC. OTTAWA

LOGIC DIAGRAM
DALM, MTT AND VCU
MULTIPLEXOR
SERIES L-PHASE I

sheet 1 of 2 no. SLD 11839L rev 1

8 7 6 5 4 3 2 1



CHIP CHART SHT 2					
	1	2	3	4	5
A	——	——	——	——	——
B	——	——	——	380	——
C	74278	——	——	——	——
D	7440	836	7437	——	——
E	7400	7479	7400	——	——
F	——	7479	7437	858	858
G	——	——	836	——	——

rev	eco	description	date	by	chk	approvd
1		PRE-PROD RELEASE	17 JAN 73	DJ		

copied on SLD11806A	drawn DJ
scale ——	date 17 JAN 73
design ENG	check
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0 30'	final approval
material	finish

CONSOLIDATED COMPUTER INC. OTTAWA

title LOGIC DIAGRAM DRUM, MTT AND VCU MULITPLEXOR SERIES L - PHASE 1

sheet 2 2 of | no. SLD11830L | rev 1

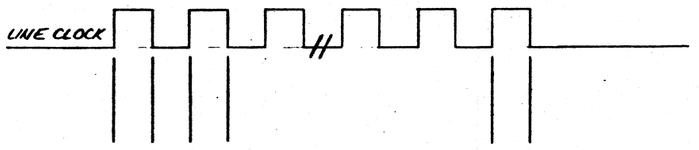
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

KDT Controller Flows

Figures 8A through 10B show the controller modes of operation. Each mode is shown on two pages. The written flow shows a sequence of events and signal locations. The block diagram shows the pcb interconnections and timing charts that are involved in that particular sequence of events. Refer to Appendix 2 for an explanation of the use of the flow diagrams.

SOFTWARE DECISION TO SEND DATA
IOT 634X LOADS TX ADRS REGISTER (11B36 5C, C12E012)
IOT 6301 LOADS INTRPT MASK (11B36, 2, 1C, F-9)
IOT 6311 LOADS CA REGISTER (11B35, 2, 4D A9-C9)
IOT 6314 LOADS WC REGISTER (11B36, 2, 4B, A5-C5)
SETS BK LEVEL X FLOP (11B36, 2, 8C, E6-5, 9)
THE OUTPUT OF THE PRIORITY CHIP (11B36, 2, 7D, F7) REFLECTS THE HIGHEST PRIORITY BK LEVEL
VCU BREAK (11B36, 2, 8A, C11-9) ENABLES HIGH
THE OUTPUT OF THE PRIORITY CHIP (11B39, 2, 6B, C1) REFLECTS THE HIGHEST PRIORITY BREAK REQUEST.
$\overline{\text{BRK REQ}}$ (11B39, 2, 8B, PIN B25) ENABLES LOW
AT BTS3 (11B39, 2, 8D, PIN A37) TIME
THE MUXR PRIORITY CHIP IS LATCHED.
BTS3 DELAYS IN THE MUXR & VCU DMA CONTROL BEGIN TIMING OUT
VCU DMA BTS3 DELAYED (11B36, 7A, DB-11) ENABLES LOW
THE PRIORITY CHIP LATCHES
MUXR BTS3 DELAYED ENABLES LOW
VCU BREAK DISABLES.

WITH THE NEXT BTS3 · BTS3 DELAYED CYCLE
BRK ENBL FLOPS (11B36, 2, 6C, F6-X) ARE CLOCKED TO LATCH THE BK LEVEL X INFORMATION.
DDRXC ENABLES (11B36, 2, 5D, D11)
DISPLAY DATA REGISTER X (11B35, 2, COL, 3) ENABLES
DMA X FLOP (11B36, 1, 8C, F10) SETS.
THE OUTPUT OF THE PRIORITY CHIP (11B36, 1, 7C, F13) REFLECTS THE HIGHEST PRIORITY TRANSMISION LEVEL AVAILABLE.
TX ADRS REGISTER (11B36, 1, COL. 5, B12-D12) ENABLES
TX RQST (11B36, 1, 7C, F13-5) ENABLES.
$\overline{\text{TX RQSTG}}$ (11B35 1, 4A, E11-6) ENABLES LOW
ADRS DECODER (11B35, 1, 3C, D11) ENABLES
TX RQST FLOP (11B35, 3, 4C, E10-5) RESETS WITH MC (11B33, 3, 2C, E4-10)
ONLY IF THE RX REQST FLOP (11B35, 3, 4B, E10-9) IS RESET
LATCH TX PRIORITY (11B35, 3, 4C, F10-4) ENABLES LOW TO LATCH THE TRANSMISSION LEVEL PRIORITY CHIP (11B36, 1, 7C, F13)
SELECT LINE (11B35, 3, 4C, E10-5) ENABLES LOW.
ADRS DECODER OUTPUT IS GATED TO ENABLE THE PROPER DATA & CLOCK LINES.
CLOCK ENABLE (11B35, 3, 4C, E11-3) DISABLES HIGH
CLOCK LINE ENABLES
LINE CLOCK (11B35, 3, 4D, E12-4) ENABLES
THE FALLING EDGE OF THE LINE CLOCK STROBES DATA FROM THE VCU TERMINAL CONTROL 16 BIT SHIFT REGISTER TO THE KSTN DATA DRIVER. THE RISING EDGE OF THE LINE CLOCK STROBES DATA FROM THE KYSTN DATA RECEIVER TO THE S/P CONVERTER 16 BIT SHIFT REGISTER. THE SEQUENCE IS AS FOLLOWS:



AT COUNT TIME 2: THE VCU TERMINAL CONTROL SR LOADS FROM DISPLAY DATA REGISTER
THE FIRST BIT OF DATA IS PROVIDED ON THE KYSTN DATA LINE TX DATA ENABLE, ENABLES HIGH
AT COUNT TIME 1: RX RQST FLOP IS HELD DISABLED
AT COUNT TIME 3: THE S/P CONVERTOR LOADS THE FIRST BIT OF DATA
AT COUNT TIME 4: THE VCU TERMINAL CONTROL LOADS THE SECOND BIT OF DATA THIS SEQUENCE CONTINUES UNTIL 16 BITS OF DATA HAVE BEEN TRANSFERED
AT COUNT TIME 5: $\overline{\text{RESET}}$ (11724, 2B, C2-7) ENABLES LOW FOR 200 nSEC.

RK LATCH (11724, 3C, E3-6) RESETS
BIT CNTR (11724, 4B, F3) RESETS
RK/TX FLOP (11724, 5D, F2-5) RESETS
LD WD (11724, 6C, C3-11) ENABLES FOR 200 nSEC
LD WD INITIATES THE SEQUENCE SHOWN IN THE LOWER LEFT TIMING SHEET DIAGRAM
AT COUNT TIME 6
$\overline{\text{BEGIN}}$ (11B35, 3, 3A, E6-2) ENABLES LOW FOR 200 nSEC
RX RQST FLOP RESETS
TX RQST FLOP SETS
SR MODE FLOP (11B35, 3, 3C, F6-6) RESETS.
TX ENBL FLOP SETS
$\overline{\text{TX CPLT}}$ (11B35, 3, 2B, F10-10) ENABLES LOW FOR 200 nSEC
DMA X FLOP RESETS
TX RQST DISABLES
$\overline{\text{TX LEVEL X COMPLETE}}$ ENABLES LOW FOR 200 nSEC
VCU CYCLE DELAY BEGINS TO TIME OUT. AFTER 1/2 MSEC ANOTHER TX RQST CAN BE GENERATED. THE FLOW WILL REPEAT ITS SEQUENCE UNTIL THE WC REGISTER OVER FLOWS.
WC RGTR OVERFLOWS
$\overline{\text{INT}}$ ENABLES LOW
CPU RESPONDS WITH IOT CMDS TO DETERMINE WHICH DMA LEVEL HAS FINISHED.

END

used on	ØI
drawn	R.W.T.
date	19 FEB 73
design eng	
checked	
final approv	
material	
finish	

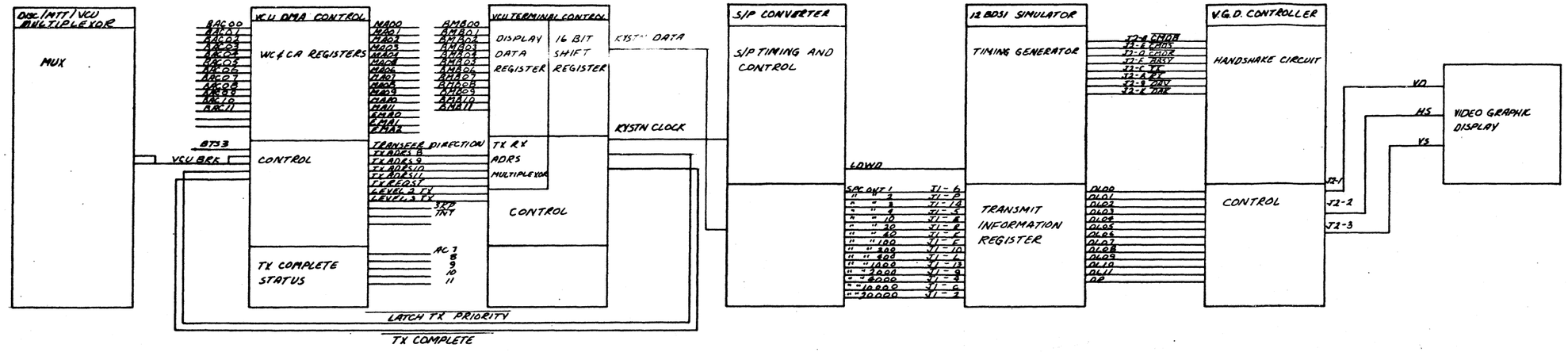
unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0°30'

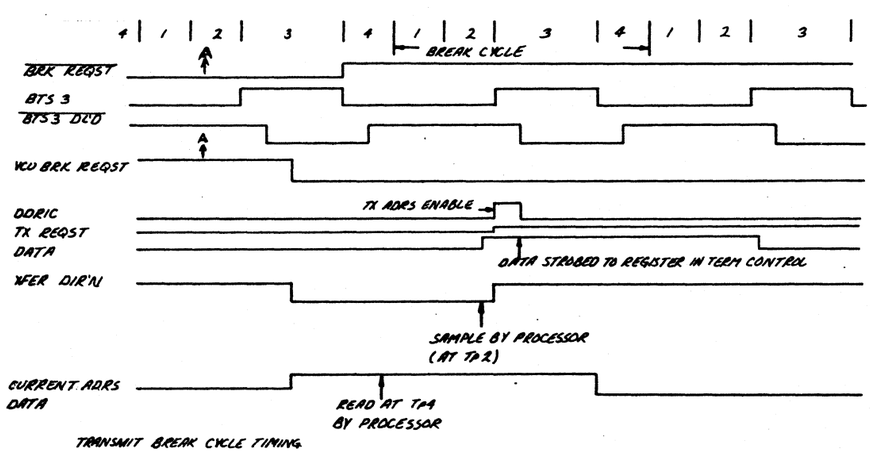
CONSOLIDATED COMPUTER INC. OTTAWA

KEYSTATION SUBSYSTEM TRANSMIT MODE

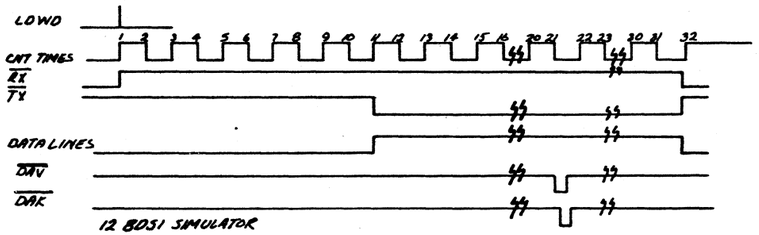
sheet of no. FIGURE 8A rev

rev	eco	description	date	by	chk	approved

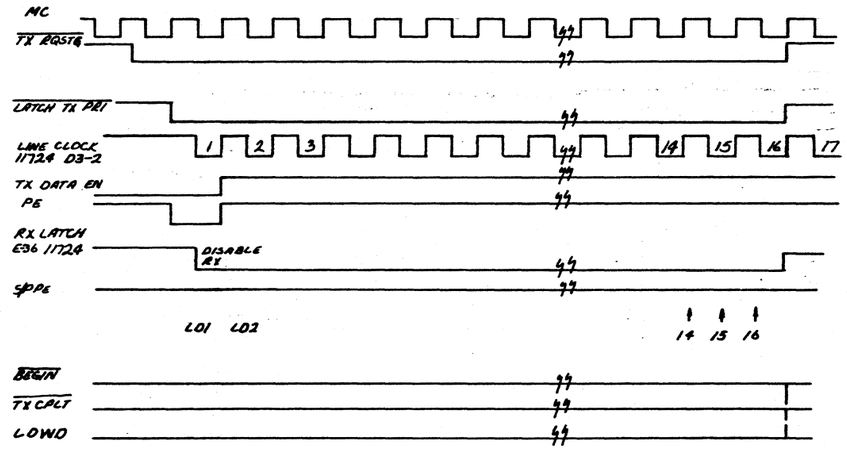




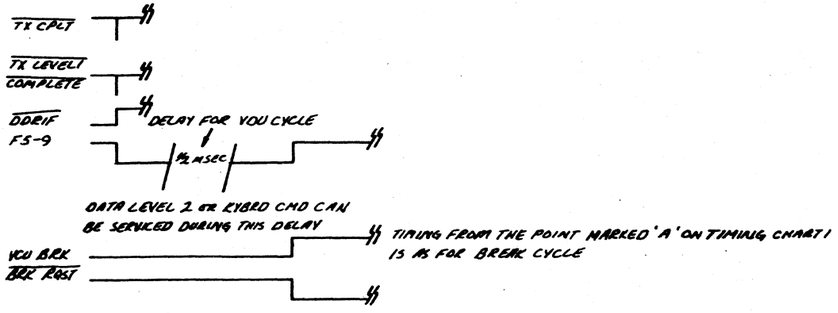
TRANSMIT BREAK CYCLE TIMING.



12 BDSI SIMULATOR TRANSMIT TIMING.



TERMINAL CONTROL AND S/P CONVERTER TRANSMIT TIMING.



DATA LEVEL 2 OR KYBRD CMD CAN BE SERVICED DURING THIS DELAY

TIMING FROM THE POINT MARKED 'A' ON TIMING CHART 1 IS AS FOR BREAK CYCLE

VCU DMA TIMING TO INITIATE BREAK REQUEST AFTER THE FIRST WORD OF A FILE HAS BEEN TRANSFERED.

rev	eco	description	date	by	chk	approvd

used on	drawn R.W. Taylor	CONSOLIDATED COMPUTER INC. OTTAWA
scale — date 25 JAN 73	design apprvl	KEYSTATION SUBSYSTEM TRANSMIT MODE
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0 30'	checked	
material	finish final apprvl	title sheet of no. FIGURE 8B rev

KEY IS DEPRESSED

$\overline{DAV}$ (11725, C1, SIDE 9) ENABLES LOW

500 MSEC DELAY - $\overline{DAK}$ (11725, C1, SIDEK) ENABLES LOW

RX INITIATE (11725, A6, D3; B) ENABLES HIGH RX INITIATE FLOP (11724, D3. B2-14) SETS

DATA STROBED INTO RX INFORMATION REGISTER

500 MSEC DELAY - $\overline{DAV}$ DISABLES

500 MSEC DELAY $\overline{DAK}$ DISABLES

RX INITIATE DISABLES

RX/TX FLOP (11724, D5, F2-5) SETS ONLY IF RX LATCH (11724. C4, E3-6) IS RESET

SHIFT REGISTER CLOCK ENABLES (11724, D6, D2-11)

RX INITIATE FLOP RESETS

ALL TRANSMIT MODE SIGNALS DISABLE

KYSTN DATA DRIVER ENABLES

RX RQST (11835, 1, C2, A11-5) ENABLES HIGH

RX RQST FLOP (11835, 3, B4, E10-9) SETS WITH THE LEADING EDGE OF $\overline{MC}$ (11835, 3, C2, E4-9) ONLY IF TX RQST FLOP IS SET.

SELECT LINE (11835, 3, 4C, E10-5) IS HIGH

$\overline{LATCH\ RX\ PRIORITY}$ (11835, 3, 4C, F10-4) ENABLES LOW

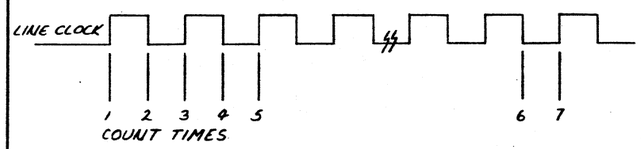
THE OUTPUT OF THE PRIORITY CHIP (11835, 1, C2, A11) REFLECTS THE HIGHEST PRIORITY KYBD REQUESTING AN INTRPT. THE OUTPUT PARTIALLY ENABLES THE RELEVANT CLOCK & DATA LINES.

RX ADRS BITS (11835. 3, D4, E12-4) ENABLE .

RX LATCH SETS

ABORT (11724, B2, C2-10) BEGINS TIMING OUT

THE RISING EDGE OF THE LINE CLOCK IS USED TO CLOCK THE VCU TERMINAL CONTROL SHIFT REGISTER. THE FALLING EDGE IS USED TO CLOCK THE S/P CONVERTER SHIFT REGISTER. THE SEQUENCE IS AS FOLLOWS.



AT COUNT TIME 1 THE LINE CLOCK ENABLES & THE VCU TERMINAL CONTROL LOADS WHATEVER DATA THE KYSTN DATA LINE HAPPENS TO PRESENT.
AT COUNT TIME 2 THE S/P CONVERTER PRESENTS THE FIRST BIT OF DATA ON THE KYSTN DATA LINE.
AT COUNT TIME 3 THE VCU TERMINAL CONTROL LOADS THE FIRST BIT OF DATA INTO THE 16 BIT SHIFT REGISTER.
AT COUNT TIME 4 THE S/P CONVERTER PRESENTS THE 2nd BIT OF DATA ON THE KEYSTATION DATA LINE
AT COUNT TIME 5 THE VCU TERMINAL CONTROL LOADS THE 2nd BIT OF DATA INTO THE 16 BIT SHIFT REGISTER
THIS SEQUENCE CONTINUES UNTIL 16 BITS OF DATA HAVE BEEN TRANSFERED TO THE VCU TERMINAL CONTROL.
COUNT TIME 6
S/P BIT 17 DECODER (11724, B2, E3-11) ENABLES LOW

$\overline{RESET}$ (11724, B2, C2-7) ENABLES LOW FOR 200 NSEC

BIT CNTR (11724, B4, F3-11) RESETS.
16TH BIT FLOP (11724, B3, E2-5) RESETS
ABORT RESETS
RX LATCH RESETS

COUNT TIME 7
VCU TERMINAL CONTROL BIT 17 DECODER (11835, 3, A2, F5-8)
ENABLES LOW

$\overline{BEGIN}$ (11835, 3, A3, E6-2) ENABLES LOW FOR 200 NSEC

RX RQST FLOP RESETS
SR MODE FLOP RESETS

LD RX INFO (11835, 3, B2, E9-3) ENABLES HIGH FOR 200 NSEC

RX DATA REG (11835, 4, B4, E2 E C4) ARE LOADED.

$\overline{INT}$ (11835, 4, B3, B1-11) ENABLES LOW

END

WHEN $\overline{INT}$ ENABLES THE CPU RESPONDS WITH IOT COMMANDS TO READ THE ADRS AND DATA FROM THE KYBD.

IN ORDER TO LOCATE A SIGNAL NAMED IN THE FLOW FIND THE FIRST PLACE IT IS USED. THEN USE THE DIAGRAM TO DECODE THE LOCATOR.

RX RQST FLOP (11835, 3, B4, E10-9)

- CHIP LOCATION & OUTPUT PIN
- LOCATION ON LOGIC DIAGRAM
- LOGIC DIAGRAM PAGE
- LOGIC DIAGRAM & PCB NUMBER

THE LOGIC DIAGRAM PAGE NUMBER IS ONLY INCLUDED FOR MULTIPLE PAGE LOGIC DIAGRAMS.

rev	eco	description	date	by	chk	apprvd

used on	PHASE I
assy	date 25 FEB 73
drawn	R.V.T
design eng	
checked	
final apprvl	

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0°30'

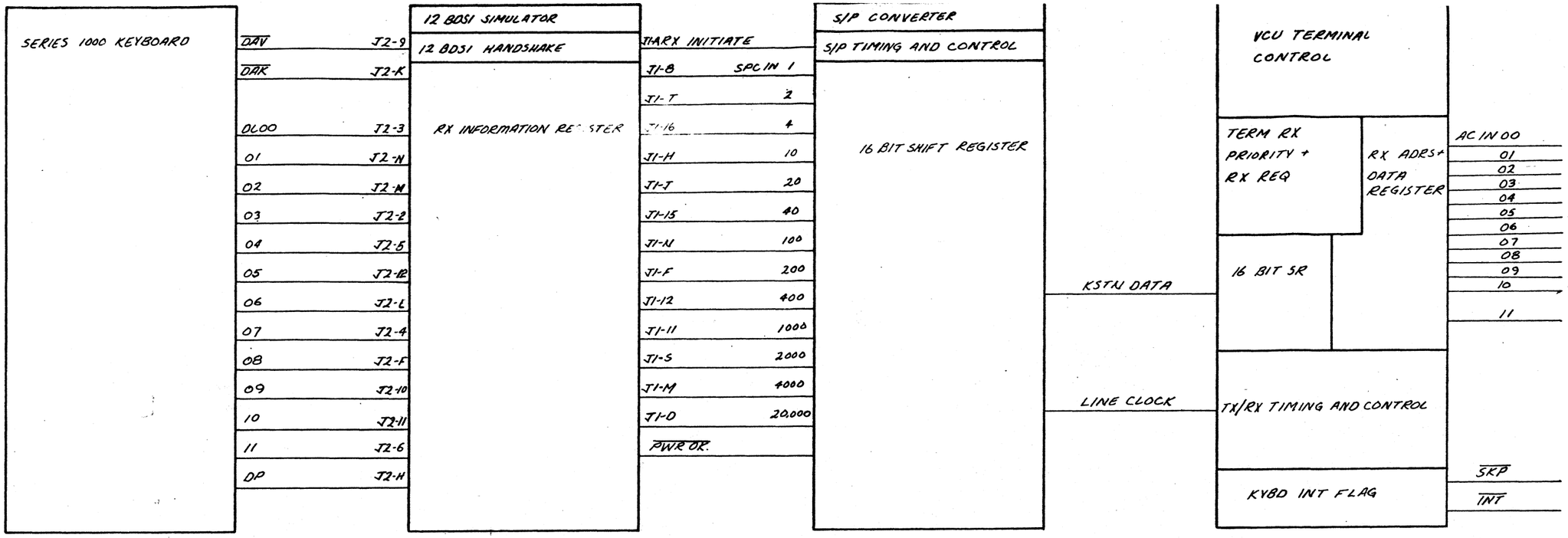
material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: KEYSTATION SUBSYSTEM RECEIVE MODE

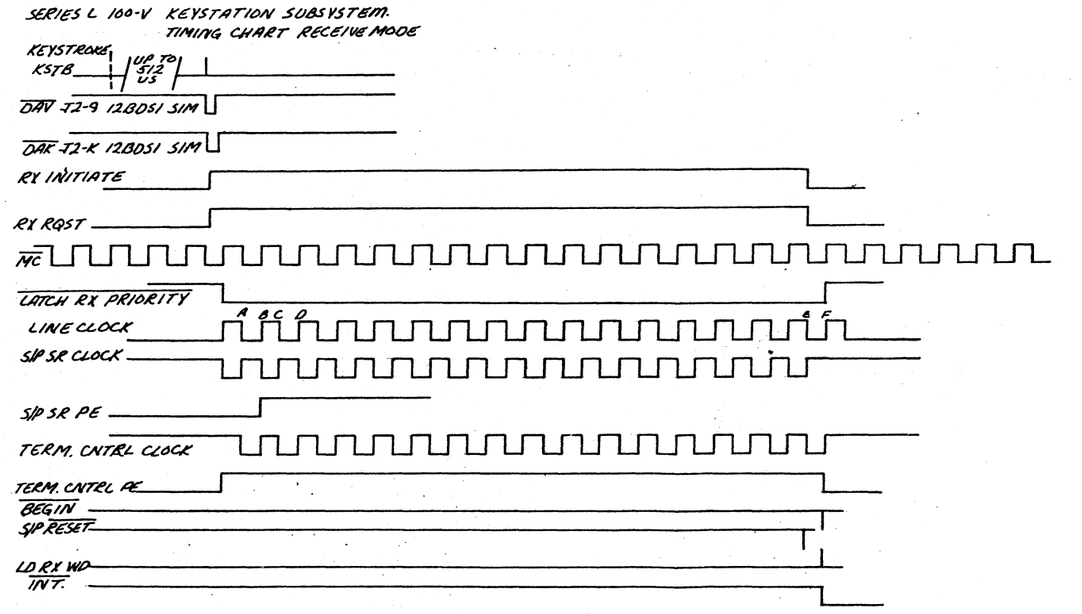
sheet of | no. FIGURE 9A | rev

8 7 6 5 4 3 2 1




```
*1000     CLACLL      7300
          TAD ADRS    1113      KEYSTATION ADDRESS
          LD ADRS     6364        0        0000
          TAD CMD     1114        1        0001
          LD CMD      6371        2        0010
          SKP ON FLG  6331        3        0011
          JMP.-1      5205
          RD ADRS     6332
          STORE ADRS  7421
          RD DATA     6334
          JMP.-5      5205
          ADRS   See table.
          CMD         0100
```

This program will turn the keystation selected by ADRS on-line and then read the keyboard address and data. The address is stored in the Memory Quotient Register and the data is stored in the Accumulator. Each time a key is depressed the information is updated.



rev	eco	description	date	by	chk	apprvd

used on | drawn R.W.T. | CONSOLIDATED COMPUTER INC. OTTAWA | KEYBOARD SUBSYSTEM .RECEIVE MODE

scale | date 18 JAN 73 | design apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

checked | final apprvl | material | finish | title | sheet of | dn. FIGURE 98 | rev

DTEX 11 004-5-72

8 7 6 5 4 3 2 1

SOFTWARE DECISION TO SEND CMD

IOT 6344 LOADS TX ADRS REGISTER (11836, 1, 5B, B12)

IOT 6351 LOADS CMD DATA REGISTER (11835, 2, 3B, B4 & B5)

SETS KBD CMD FLOP (11836, 1, 8B, F9-5)

TX ADRS REGISTER ENABLES

CMD DATA REGISTER ENABLES

TX RQST (11836, 1, 7D, SIDE 4) ENABLES HIGH

$\overline{\text{TX RQST G}}$ (11835, 1, 4A, E11-6) ENABLES LOW

ADRS DECODER (11835, 1, 3C, D11) ENABLES

TX RQST FLOP (11835, 3, 9C, E10-5) RESETS WITH MC (11835, 3, 2C, E4-10)

ONLY IF THE RX RQST FLOP (11835, 3, 9B, E10-9) IS RESET

SELECT LINE (11835, 3, 9C, E10-5) ENABLES LOW

ADRS DECODER OUTPUT IS GATED TO ENABLE THE PROPER DATA & CLOCK LINES

$\overline{\text{LATCH TX PRIORITY}}$ (11835, 3, 9C, F10-4) ENABLES LOW TO LATCH THE TRANSMISSION LEVEL

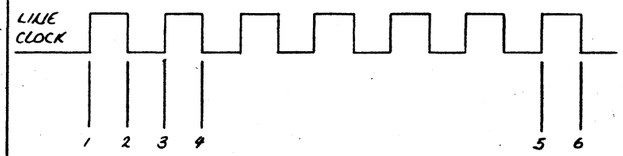
PRIORITY CHIP (11836, 1, 7C, F13)

CLOCK ENABLE (11835, 3, 4C, E11-3) DISABLES HIGH.

CLOCK LINE ENABLES

LINE CLOCK (11835, 3, 9D, E12-4) ENABLES.

THE FALLING EDGE OF LINE CLOCK STROBES DATA FROM THE VCU TERMINAL CONTROL 16 BIT SHIFT REGISTER TO THE KYSTN DATA DRIVER. THE RISING EDGE OF THE LINE CLOCK STROBES DATA FROM THE KYSTN DATA RECEIVER TO THE S/P CONVERTER 16 BIT SHIFT REGISTER. THE SEQUENCE IS AS FOLLOWS.



AT COUNT TIME 2: THE VCU TERMINAL CONTROL SR LOADS FROM DISPLAY DATA REGISTER

THE FIRST BIT OF DATA IS PROVIDED ON THE KYSTN DATA

LINE TX DATA ENABLE ENABLES HIGH.

AT COUNT TIME 1: RX RQST FLOP IS HELD DISABLED.

AT COUNT TIME 3: THE S/P CONVERTER LOADS THE FIRST BIT OF DATA

AT COUNT TIME 4: THE VCU TERMINAL CONTROL LOADS THE SECOND BIT OF DATA

AT COUNT TIME 5: $\overline{\text{BEGIN}}$ (11835, 3, 3A, E6-2) ENABLES LOW FOR 200 nSEC

RX RQST FLOP RESETS

TX RQST FLOP SETS

SR MODE FLOP (11835, 3, C3, F6-6) RESETS

TX ENBL FLOP SETS.

$\overline{\text{TX CPLT}}$ (11835, 3, 2B, F10-10) ENABLES LOW FOR 200 nSEC

KYBD CMD FLOP RESETS

TX RQST DISABLES.

AT COUNT TIME 6: $\overline{\text{RESET}}$ (11724, 2B, C2-7) ENABLES LOW FOR 200 nSEC

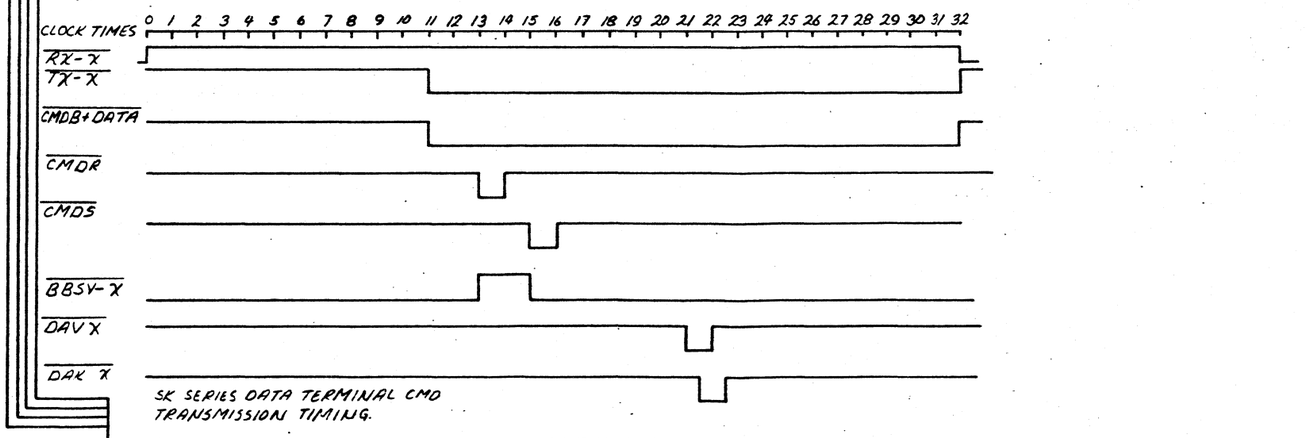
RX LATCH (11724, 3C, E3-6) RESETS

BIT CNTR (11724, 9B, F3) RESETS

RX/TX FLOP (11724, D5, F2-5) RESETS.

LOWD (11724, 6C, C3-6) ENABLES FOR 200 nSEC

LOWD INITIATES THE SEQUENCE SHOWN IN THE LOWER LEFT TIMING DIAGRAM.



SK SERIES DATA TERMINAL CMD TRANSMISSION TIMING.

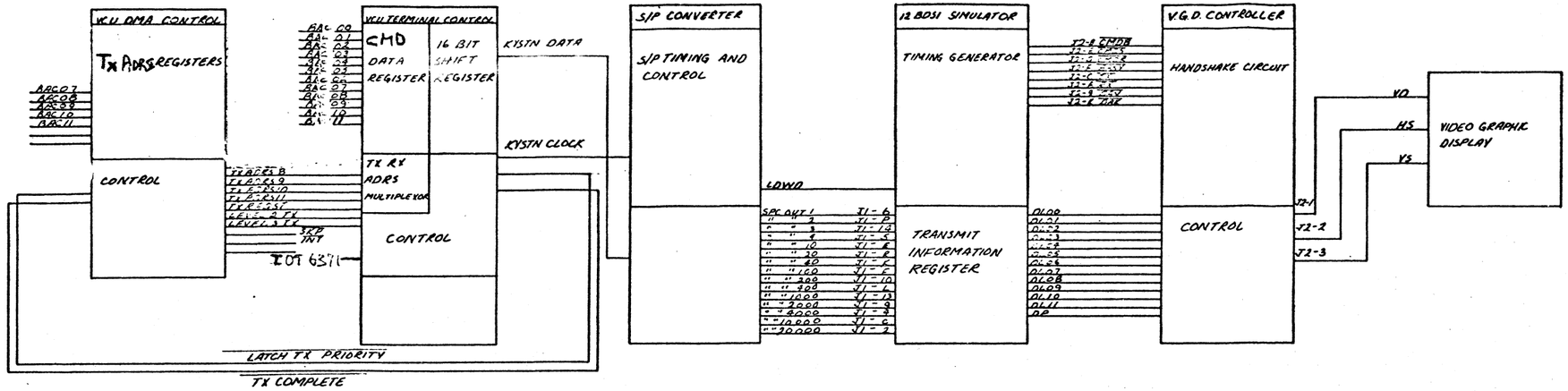
END

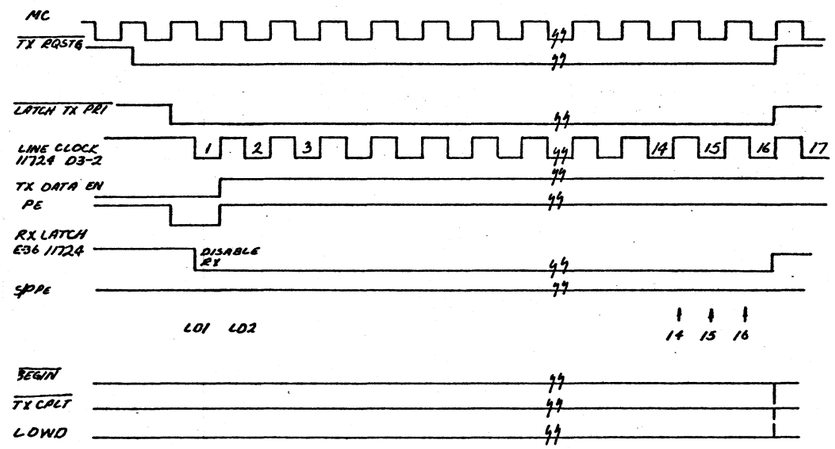
rev	eco	description	date	by	chk	approvd

spec no.		drawn	R.W.T
scale	date 21 FEB 73	design eng	
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0°30'		checked	
		final approv	
material	finish	sheet of	no. FIGURE 10A rev

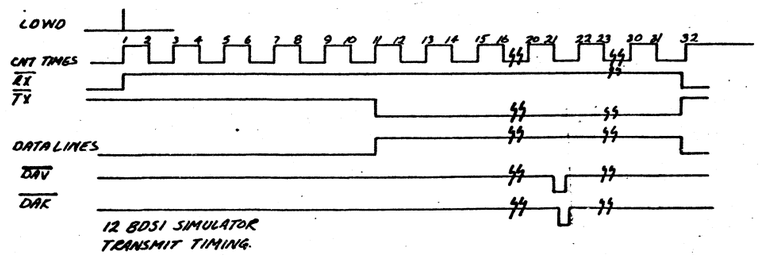
CONSOLIDATED COMPUTER INC. OTTAWA

title: KEYSTATION CMD TRANSMIT MODE





TERMINAL CONTROL AND S/P CONVERTER TRANSMIT TIMING.



12 BDSI SIMULATOR TRANSMIT TIMING.

rev	eco	description	date	by	chk	approd

used on		drawn R.W. Taylor	CONSOLIDATED COMPUTER INC. OTTAWA
scale	date 25 JAN 73	design apprvl	title KEYSTATION CMD TRANSMIT MODE
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ± 0 30'		checked	
		final apprvl	material / finish / sheet of / no. FIGURE 10B

TRANSTEX 15 000-0-72

8 7 6 5 4 3 2 1

Keyboard Controller

The Keyboard Controller is a single pcb mounted in the Series 1000 Data Terminal underneath the operator keys. The pcb number is SKD 11840 A.

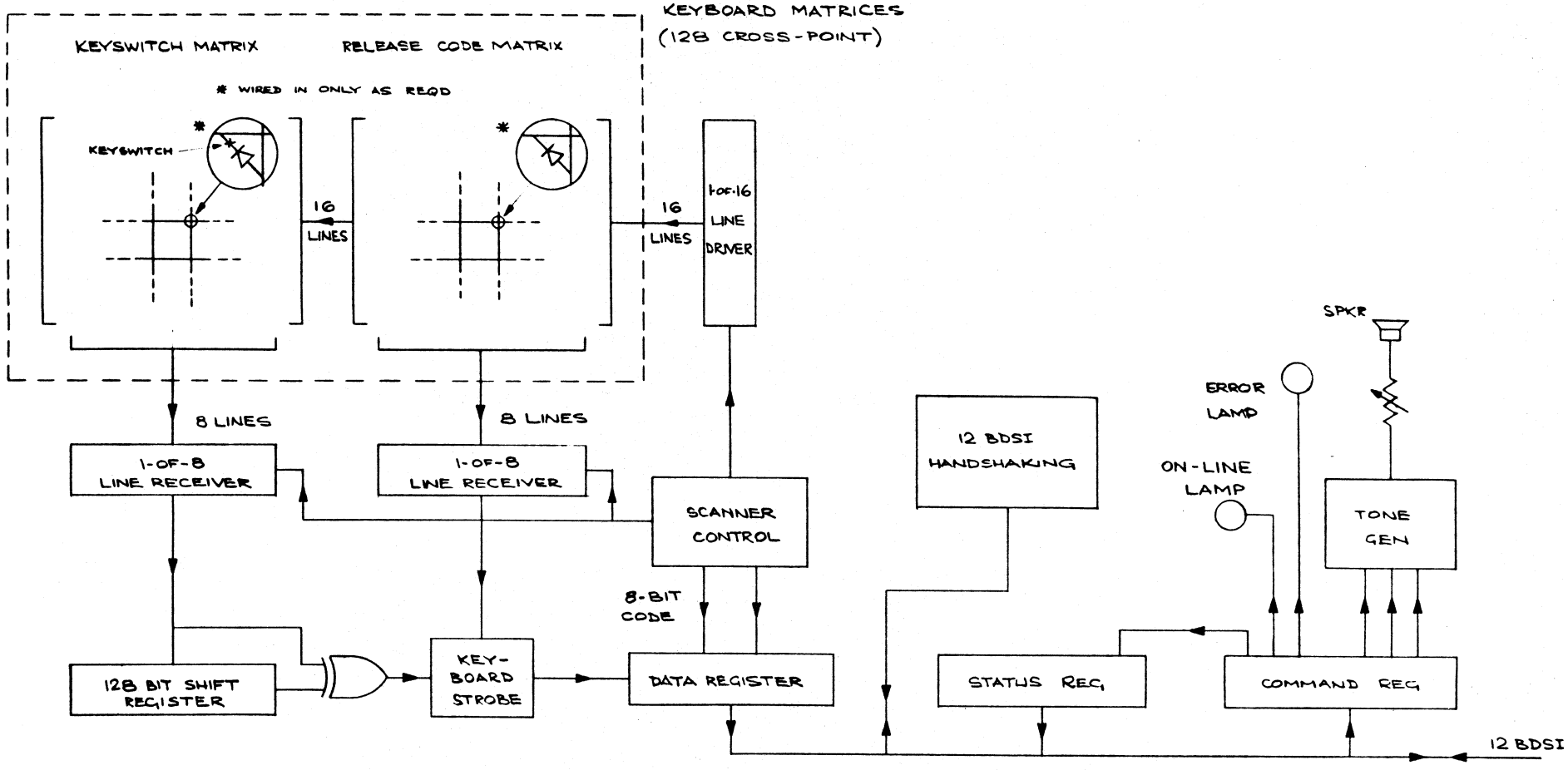
The controller assembles data words as the operator strikes keys. The assembled word is transferred to the Terminal Controller by a 12 Bit Data Standard Interface (12 BDSI).

Figure 11 is a block diagram of the Keyboard Controller. The standard Keyboard layout is illustrated by drawing SLB 11822 X.

Keyboard Controller Flows

The sequence of events during both of the modes of operation are shown in Figures 12 and 13.

NOTE: On the Keyboard Controller Error and Receive Flows, the pcb number used is 11352. This should read 11840.



rev	eco	description	date	by	chk	apprvd

used on | drawn
scale | date | design apprvl
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
checked
final apprvl
material | finish

CONSOLIDATED COMPUTER LIMITED
OTTAWA

title: KEYSTATION BLOCK DIAGRAM
sheet of | no. FIGURE 11

Key Strobe (KSTB,11352,2, 8B ,B5-5) enables for 1 msec

Error flop (11352,2, 7B ,B6-5) is clocked and remains reset only if the Error gate (11352,2, 7B ,C6-3) is disabled

Data Latches (11352,2, col 8 ,A3-A4) are clocked only if the FULL flop (11352,2, 7B ,B7-9) is reset

FULL flop is clocked only if it was reset

DAVF flop (11352,2, 7B ,B8-8) is set only if the Receive Gate (11352, 2, 7B ,B8-11) is enabled

DL10 flop (11352,2, 6B ,B6-9) is clocked and remains set only if the Error flop is reset

Data Available (DAV-X,11352,2, 6A ,A8-6,J1-9) enables

After 500 msec Data Acknowledge (DAK-X,11352,2, 4A ,C2-9,J1-k) enables

DAK gate (11352,2, 8A ,C7-14) enables only if the Transmit gate (11352, 2, 6A ,A12-14) is disabled

After 500 msec the FULL flop resets
DAVF flop resets
DAV-X disables

After 500 msec DAK-X disables

Error Detection

Parity Errors

A parity bit is generated by the keyboard for both data and status words. This bit is used by the terminal controller to check the word parity. If an error is detected the software responds by sending a command to the terminal in the same manner as any other command.

Keyboard Errors

The keyboard controller must ensure that the present word in the Data Latch is received by the terminal controller before another word is generated. There are two ways that the keyboard controller can detect errors. A timer is used to limit the interval between keystrokes to at least 10 msec, and gating is used to ensure that the terminal controller has responded to one Data Available pulse before issuing another.

Data Line 10 is used to indicate to the terminal controller that the keyboard has detected an error.

Assume that the channel controller is in the transmit mode when the KSTB enables

KSTB enables
FULL flop sets
Receive gate is held disabled
Error gate enables

KSTB enables
Error flop sets
After some time RX enables
DAVF flop sets

DL10 flop sets
DL10-X enables
DAV-X enables
After 500 nsec DAK-X enables
EODT enables
After 500 nsec the FULL flop resets
DAVF flop resets
DAV-X disables
The DL10 flop will be reset when the next data transfer occurs.

If two keystrokes occur within 10 msec the controller responds as follows:

KSTB enables
Full Flop (11352,2, 7B ,B7-9) sets
Normal receive cycle follows
Error Flop (11352, 7B ,B6-5) is clocked and remains reset
10 msec timer (11352,2, 7B B5-7) is set
Error gate (11352,2, 7B ,E6-3) enables
Within 10 msec KSTB enables
Error flop (11352, 7B ,B6-5) sets
Tone 2 flop (11352,2, 5C B9-6) sets
Error Lamp flop (11352,2, 5B ,D9-9) sets
Full flop sets
DAVF flop (11352,2, 7B ,B8-8) sets
DL10 Flop (11352,2, 7B ,B6-8) sets
DL10-X (11352,2, 6B ,A8-11.J1-11) enables
Data Available (DAV-X, 11352,2, 6B ,A8-6,J2-9) enables
After 500 msec Data Acknowledge (DAK-X 11352,2, 8A ,C7-9,J1-K) enables
End of Data Transmission (EODT,11352,2 7A ,C7-2) enables
Error flop reset
After 500 msec the FULL flop resets
DAVF flop resets
DAV-X disables
After 500 msec DAK-X disables

rev	eco	description	date	by	chk	apprvd

used on SKC11352A
scale | date
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
drawn | design apprvl | checked | final apprvl
material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: SERIES 1000 KEYBOARD CONTROLLER RECEIVE & ERROR FLOWS

sheet of | no. FIGURE 12 | rev

TRANSTEK 11 006-0-72

8 7 6 5 4 3 2 1

Key Strobe (KST8,11352,2, 8B ,B5-5) enables for 1 msec

Error flop (11352,2, 7B ,B6-5) is clocked and remains reset only if the Error gate (11352,2, 7B ,C6-3) is disabled

Data Latches (11352,2, col 8 ,A3-A4) are clocked only if the FULL flop (11352,2, 7B ,B7-9) is reset

FULL flop is clocked only if it was reset

DAVF flop (11352,2, 7B ,B8-8) is set only if the Receive Gate (11352, 2, 7B ,B8-11) is enabled

DL10 flop (11352,2, 6B ,B6-9) is clocked and remains set only if the Error flop is reset

Data Available (DAV-X,11352,2, 6A ,A8-6,J1-9) enables

After 500 msec Data Acknowledge (DAK-X,11352,2, 4A ,C2-9,J1-k) enables

DAK gate (11352,2, 8A ,C7-14) enables only if the Transmit gate (11352, 2, 6A ,A12-14) is disabled

After 500 msec the FULL flop resets
DAVF flop resets
DAV-X disables

After 500 msec DAK-X disables

Error Detection

Parity Errors

A parity bit is generated by the keyboard for both data and status words. This bit is used by the terminal controller to check the word parity. If an error is detected the software responds by sending a command to the terminal in the same manner as any other command.

Keyboard Errors

The keyboard controller must ensure that the present word in the Data Latch is received by the terminal controller before another word is generated. There are two ways that the keyboard controller can detect errors. A timer is used to limit the interval between keystrokes to at least 10 msec, and gating is used to ensure that the terminal controller has responded to one Data Available pulse before issuing another.

Data Line 10 is used to indicate to the terminal controller that the keyboard has detected an error.

Assume that the channel controller is in the transmit mode when the KSTB enables

KSTB enables
FULL flop sets
Receive gate is held disabled
Error gate enables

KSTB enables
Error flop sets
After some time RX enables
DAVF flop sets

DL10 flop sets
DL10-X enables
DAV-X enables
After 500 msec DAK-X enables
EODT enables
After 500 msec the FULL flop resets
DAVF flop resets
DAV-X disables
The DL10 flop will be reset when the next data transfer occurs.

If two keystrokes occur within 10 msec the controller responds as follows:

KSTB enables
Full Flop (11352,2, 7B ,B7-9) sets
Normal receive cycle follows

Error Flop (11352, 7B ,B6-5) is clocked and remains reset
10 msec timer (11352,2, 7B B5-7) is set
Error gate (11352,2, 7B ,E6-3) enables
Within 10 msec KSTB enables

Error flop (11352, 7B ,B6-5) sets
Tone 2 flop (11352,2, 5C B9-6) sets
Error Lamp flop (11352,2, 5B ,09-9) sets

Full flop sets
DAVF flop (11352,2, 7B ,B8-8) sets

DL10 Flop (11352,2, 7B ,B6-8) sets
DL10-X (11352,2, 6B ,A8-11.J1-11) enables

Data Available (DAV-X, 11352,2, 6B ,A8-6,J2-9) enables

After 500 msec Data Acknowledge (DAK-X 11352,2, 8A ,C7-9,J1-K) enables

End of Data Transmission (EODT,11352,2 7A ,C7-2) enables
Error flop reset

After 500 msec the FULL flop resets
DAVF flop resets
DAV-X disables

After 500 msec DAK-X disables

rev	eco	description	date	by	chk	apprvd

used on SKC/11352A
scale
date
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
drawn
design apprvl
checked
final apprvl
material
finish

CONSOLIDATED COMPUTER INC. OTTAWA

SERIES 1000
KEYBOARD CONTROLLER
RECEIVE & ERROR FLOWS

title
sheet of
no. FIGURE 12
rev

TRANSTEX 18 006-0-72

8 7 6 5 4 3 2 1

Command Transmission

Software decision to send a command

The DTC 8 assembles a word

Receive (RX,11352,2, 2C ,A12-13,J1-A) disables.

Full-RX (11352,2, 7B ,B8-11) disables to present the Full flop enabling a receive cycle.

After a 20 usec delay Command Bit and Data Bit enable

Transmit (TX,11352,2, 6A ,A12-14,J1-C) enables.

Command Register buffers (11352,2, clo 5 ,A9-A10) enable

After 4 usec Command Reset (CMDR,11352,2, 3B ,A11-5,J1-D) enables for 2usec

Bus Busy (BBSY,11352,2, 2B ,C11-6,J1-7) disables only if the data contains the proper device address.

After 4 usec Command Set (CMDS,11352,2, 3B ,A11-12,J1-E) enables for 2 usec

BBSY enables

After 12 usec Data Available ($\overline{\text{DAV-X}}$,11352,2, 6B ,A10-7,J1-9) enables

After 500 nsec the Command Register (11352,2, col 5 ,B9-D9) is clocked

Data Acknowledge ($\overline{\text{DAK-X}}$,11352,2, 4A ,A8-8,J1-K) enables

After 500 nsec $\overline{\text{DAV-X}}$ disables

After 500 nsec $\overline{\text{DAK-X}}$ disables

If the command contained a request for keyboard status the flow continues from the time that the Command Register is clocked.

STAT flop (11352,2, 5E ,D9-5) sets

STR flop (11352,2, 7A ,B7-5) sets only if the FULL flop is reset

STAT flop resets

STR•(TX•RDY) (11352,2, 7A ,D8-11) disables the key address drivers and enables Data Line 11 (11352,2, 1C ,A1-3,J1-6)

STR•(TX•RDY) enables the Status Register drivers

FULL flop (11352,2, 7B ,B7-9) sets

DAVF flop (11352,2, 7B ,C8-8) sets

$\overline{\text{DAV-X}}$ enables

After 500 nsec $\overline{\text{DAK-X}}$ enables

End of Data Transmission (EODT,11352,2, 7A ,C4-2) enables

STR flop resets

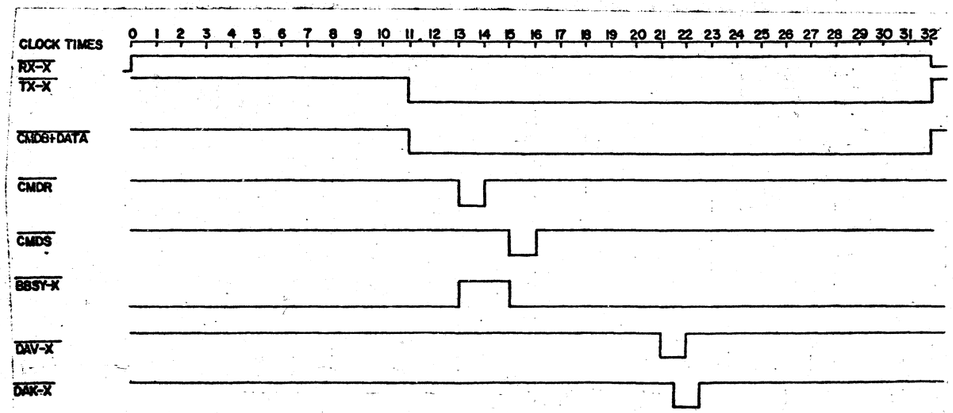
Status Register drivers disable and key address drivers enable

After 500 nsec DAVF flop resets

FULL flop resets

After 500 nsec $\overline{\text{DAK-X}}$ disables

EODT disables



SK SERIES DATA TERMINAL COMMAND TRANSMISSION TIMING

rev	eco	description	date	by	chk	approv

used on: SKC 11352 A

scale | date

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

drawn | design apprvl | checked | final apprvl

material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: SERIES 1000 KEYBOARD CONTROLLER COMMAND TRANSMISSION FLOW

sheet of | no. FIGURE 13

Keyboard Controller Circuit Function

(Figure 11, SKD11840L, sht 1)

CIRCUIT	FUNCTION
Data Generator	Assembles a data word whenever a key is depressed and produces Keystroke (KSTB) to load the Data Buffer with the data word.

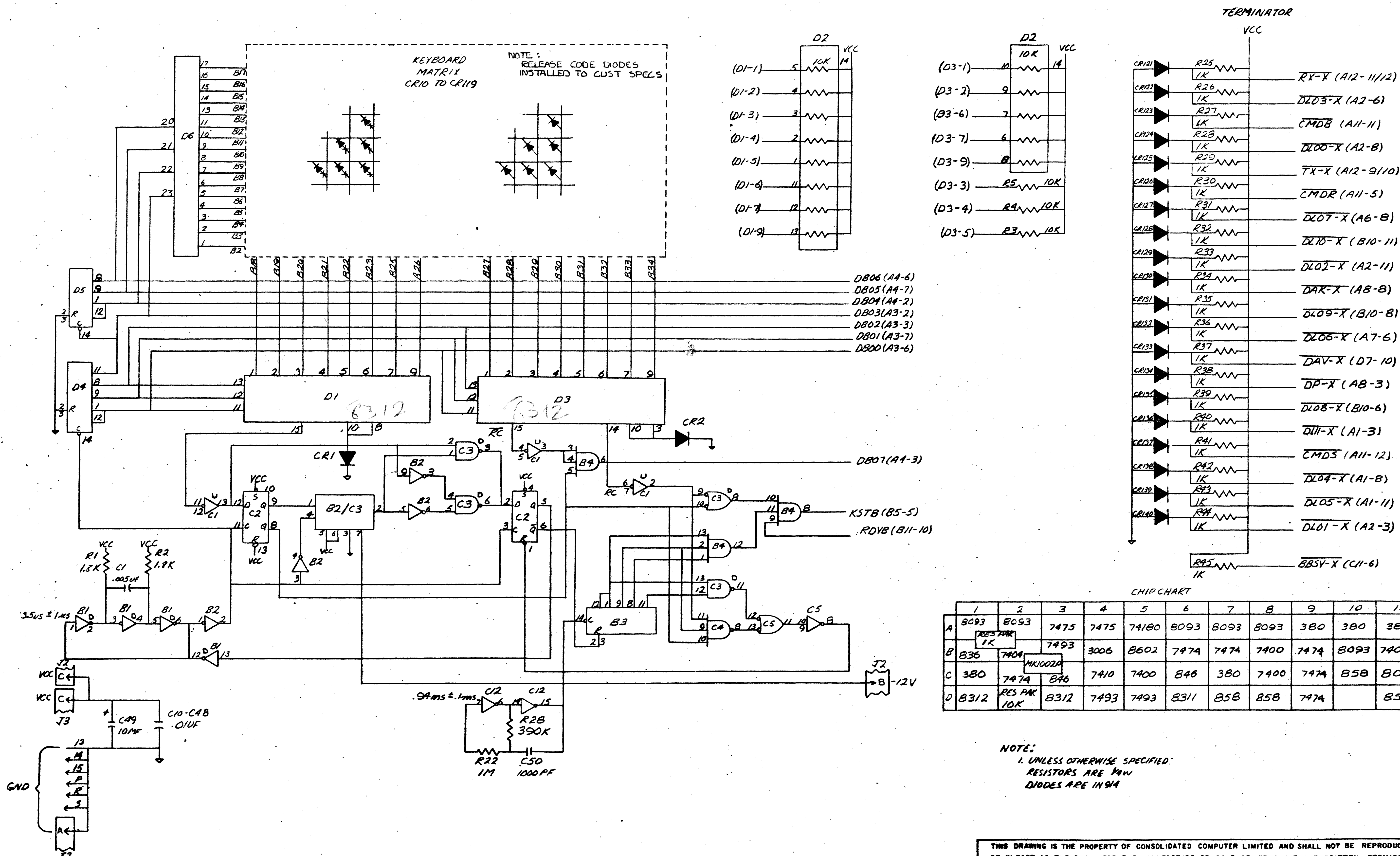
(Figure 11, SKD11840L, sht 2)

CIRCUIT	FUNCTION
Data Buffer	Contains the last data word assembled by the Data Generator. Drives the 12 BDSI cable.
Data Transfer Control	Controls the Data Available/Data Acknowledge handshaking. Senses keyboard errors. Enables the proper line drivers to transfer key data or status data.
Command Register	Controls the terminal response to command words.
Status Register	Contains a data word to identify the key top configuration.
12 BDSI Handshaking	Performs Bus Busy (BBSY) handshaking with the terminal controller.

L/150 Adapter Circuit Functions

12 BDSI Simulator (Figure 3, D11725L) PCB 11725

Circuit	Function
Timing Generator	Produces the clock pulses used to control the transmit sequence. The enabling signal is $\overline{\text{Receive}}$ ($\overline{\text{RX}}$) high. The outputs are timing counts (CNTxx).
Receive Information Register	Stores data being transferred to the S/P Converter. Input is the data lines from the Series K terminal. Output is a set of signals called SPC IN xxxx. The register is clocked by $\overline{\text{DAK}}$ from the handshake control.
Transmit Information Register	Stores data being transferred to the Series K terminal. Input is a set of signals called SPC OUT xxxx. Output is the terminal data lines. The register is clocked by LOAD WORD (LD WD) from the S/P Converter.
12 BDSI Handshake Timing	Produces the control bits used by the Series K terminal during data transfers.



CHIP CHART

	1	2	3	4	5	6	7	8	9	10	11	12
A	8093	8093	7475	7475	74180	8093	8093	8093	380	380	380	380
	RES PAK 1K											
B	836	7404	7493	3006	8602	7474	7474	7400	7474	8093	7402	7410
		MK1002P										
C	380	7474	846	7410	7400	846	380	7400	7474	858	8093	CD4009
D	8312	RES PAK 10K	8312	7493	7493	8311	858	858	7474		858	

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE ¼W
DIODES ARE IN914

ECO	rev	description	date	by	chk	approved
SK098	A	ECO INCORP	8 MAR 73	RAP		
SK031	2	ECO INCORP	6 FEB 73	EAP		
	1	PRE-PROD REL	19 JAN 73	RWT		

used on | scale | date: 13 JAN 73 | drawn: RWT | design | checked | final/approval

unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

material | finish

title: LOGIC DIAGRAM KEYBOARD DATA TERMINAL

sheet 1 of 2 no. SKD11840L rev A

DATA BUFFER

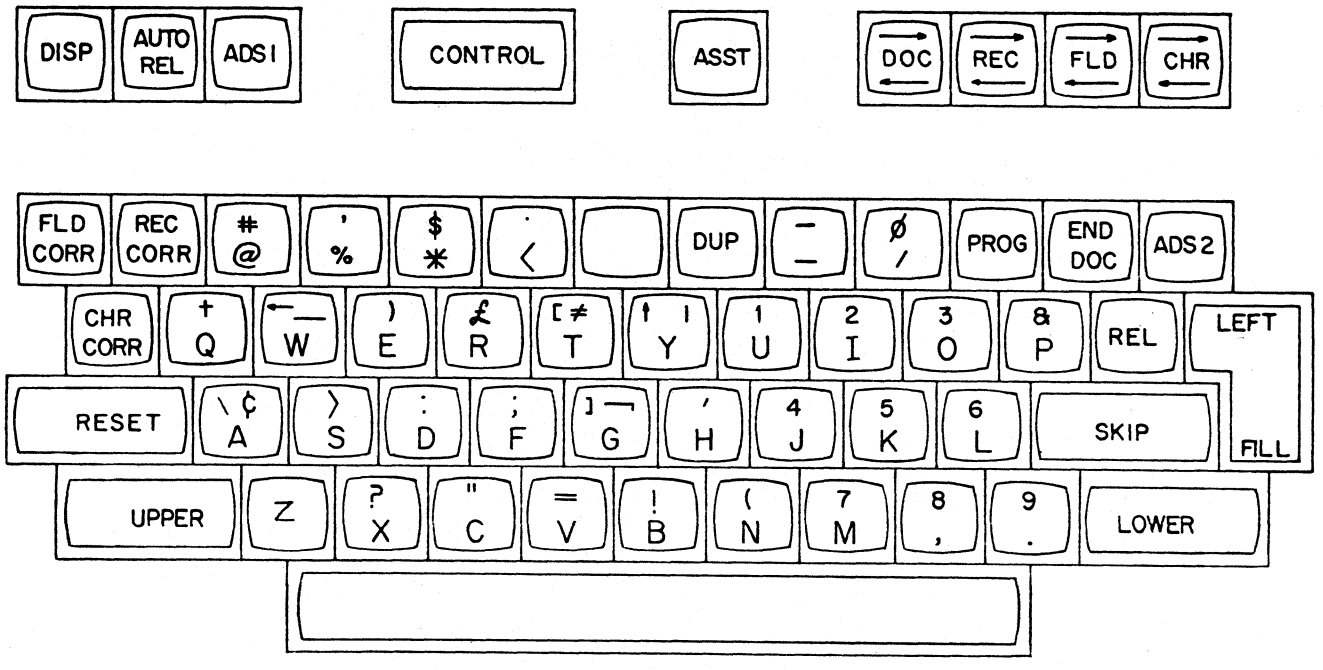
COMMAND REGISTER

DATA TRANSFER CONTROL

STATUS REGISTER

12 BDSI HANDSHAKING

CONSOLIDATED COMPUTER INC. OTTAWA	drawn EWT	LOGIC DIAGRAM KEYBOARD DATA TERMINAL	
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0 30'	date 18 JAN 73	title	
material	finish	sheet 2 of 2	no. SKD11840L rev A



FOR NOTES SEE SHEET 2

rev	eco	description	date	by	chk	approvd
4	SL-524	2 KEY BUTTONS CHANGED	20FEB73	WB		
3	SL-535	NOTES ADDED	5 JAN 73	GT		DJW
2	SL-529	KEY SIZE CHANGED	29 JAN 73	GT		
1		PRE PROD REL	16JAN73			

used on: SL811821A
scale: 1 : 1
date: 16 JAN 73
drawn:
design:
checked:
final approval:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material:
finish:

CONSOLIDATED COMPUTER INC.
OTTAWA

title: STANDARD KEYBOARD LAYOUT SERIES L PHASE 1

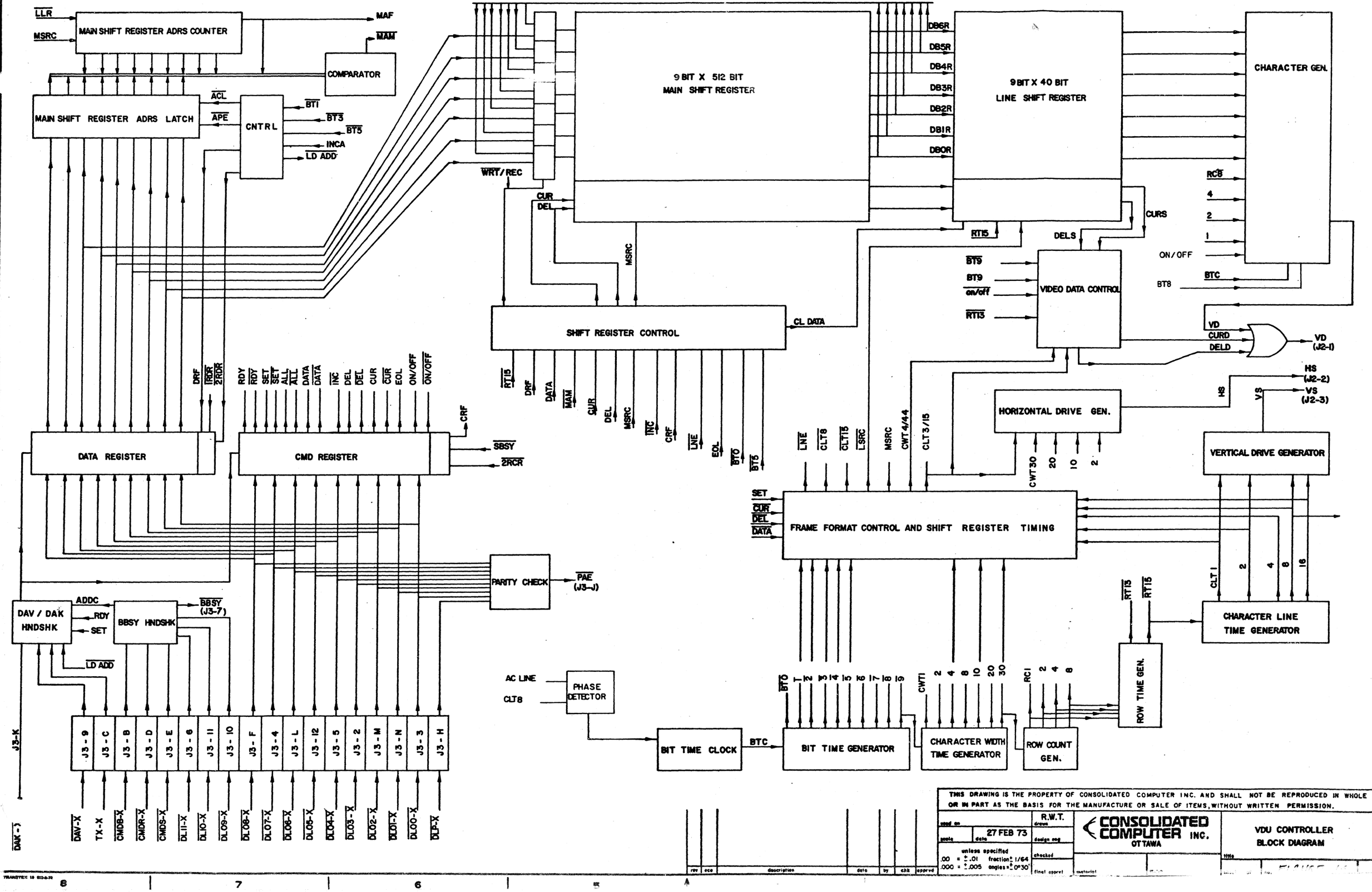
sheet 1 of

VDU CONTROLLER

General

The VDU Controller is a single pcb mounted in the Series 1000 Data Terminal underneath the video display. The pcb number is SKD 11535A.

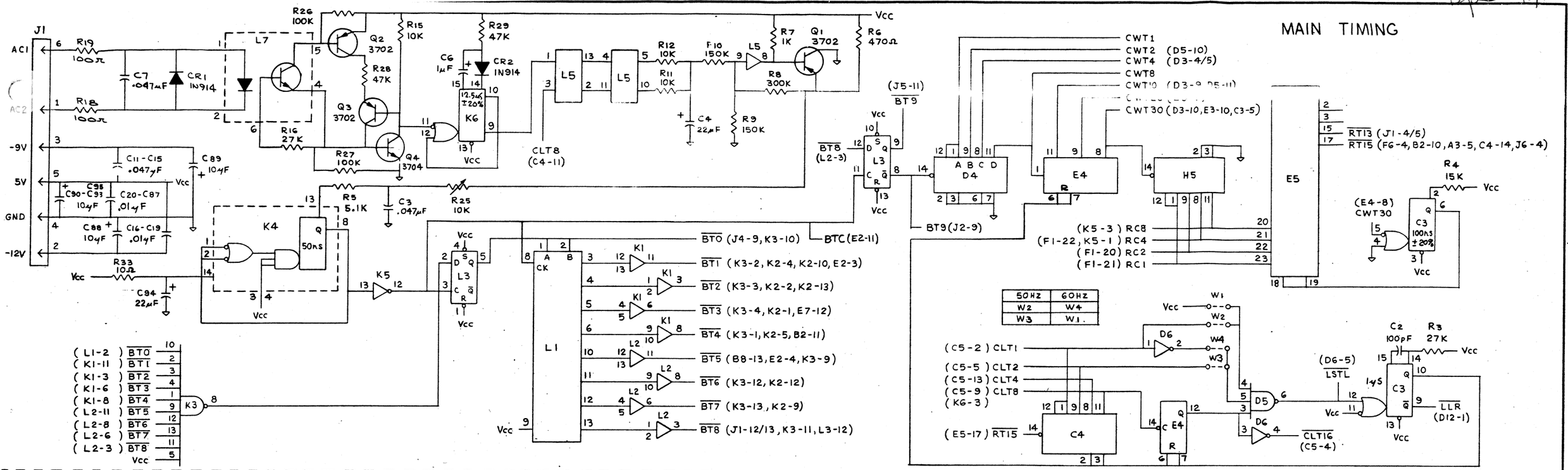
The controller accepts commands and data transmitted to it from the CPU main memory. It provides the video display with horizontal and vertical synchronization pulses and translates the data received into video display information. Refer to Figure 14.



used on		drawn	R.W.T.
scale	date 27 FEB 73	design eng	
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0°30'		checked	
		final approv	
material		title	VDU CONTROLLER BLOCK DIAGRAM

CONSOLIDATED COMPUTER INC. OTTAWA

rev	eco	description	date	by	chk	approvd


MAIN TIMING
CWT1
CWT2 (D5-10)
CWT4 (D3-4/5)
CWT8
CWT30 (D3-10,E3-10,C3-5)
RT13 (J1-4/5)
RT15 (FG-4, B2-10, A3-5, C4-14, J6-4)
(K5-3) RC8
(F1-22, K5-1) RC4
(F1-20) RC2
(F1-21) RC1
50HZ | 60HZ
W2 | W4
W3 | W1
(C5-2) CLT1
(C5-5) CLT2
(C5-13) CLT4
(C5-9) CLT8
(KG-3)
(E5-17) RT15
(D6-5) LSTL
CLT16 (C5-4)
LLR (D12-1)
BT0 (J4-9, K3-10)
BT1 (K3-2, K2-4, K2-10, E2-3)
BT2 (K3-3, K2-2, K2-13)
BT3 (K3-4, K2-1, E7-12)
BT4 (K3-1, K2-5, B2-11)
BT5 (B8-13, E2-4, K3-9)
BT6 (K3-12, K2-12)
BT7 (K3-13, K2-9)
BT8 (J1-12/13, K3-11, L3-12)
BTC (E2-11)
(J5-11) BT9
BT8 (L2-3)
BT9 (J2-9)
CLT8 (C4-11)
(L1-2) BT0
(K1-11) BT1
(K1-3) BT2
(K1-6) BT3
(K1-8) BT4
(L2-11) BT5
(L2-8) BT6
(L2-6) BT7
(L2-3) BT8
DISPLAY FORMAT
(D3-3) CLT8
(D6-4) CLT16
(C4-1) CLT1
(C4-9) CLT2
(C4-8) CLT4
(C4-11) CLT8
(D4-8) CWT4
(E4-8) CWT30
(E4-11) CWT10
CLT 3/15 (J1-9)
CLT15 (B5-4)
CLT8 (C5-1)
CWT 4/44
CWT 4/44 (J5-12, J1-1)
(A3-6) RT15
MSRC (C7-11) (D12-2)
MSRC (B7-4) (B7-2) (D7-9) (D1-14)
LSRC (FG-6)
VIDEO & SYNC OUTPUTS
(B5-8) CLT3/15 VD+CD (J2-12)
(E4-8) CWT30
(E4-9) CWT20
(E4-11) CWT10
(D4-9) CWT2
(D5-6) LSTL
J2
GND
VD
HS
VS
R30 220Ω
R31 1K
R32, 1K
R1 5.6K
R4 15K
C3 100nS ±20%
MAIN SHIFT REGISTER UPDATE SEQUENCE
(A3-8) RT15D
(B1-9) 512
(B1-8) 1024
(A3-12) 32
(B5-3) CLT15
(E5-17) RT15
(K1-8) BT4
RECYCLE COUNTER
32 (B5-5)
512 (B4-12)
1024 (B4-13)
(B7-11) MSRC
(E5-17) RT15
RT15D (B4-10)
LINE END COUNTER
C2 100nS ±20%
LNE (A8-1)
(E10-9) SET
(H10-14) CUR
(H10-8) DEL
(E10-1) DATA
LD ADD (F11-4)
DRF (C9-5)
(L2-11) BT5
(K1-6) BT3
(B8-3) INCA
ACL (D10-2)
2RDR (C8-5)
APE (D10-9)
MAF (B11-9)
THIS DRAWING IS THE PROPERTY OF CONSOLIDATED COMPUTER LIMITED AND SHALL NOT BE REPRODUCED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS, WITHOUT WRITTEN PERMISSION.
SKD11535A
3 AUGUST 72
CONSOLIDATED COMPUTER LIMITED OTTAWA
LOGIC
VDU CONTROLLER
DATA TERMINAL
SKD11535L
A SK102 PROD RELEASE 8 MAR 73 DJ
1 PRE PROD REL 13 OCT 72 RC

Circuit Functions

(Figure 14, SKD 11535L/1, sht 1)

Circuit	Function
12 BDSI Handshake	Provides the signals that respond to 12 BDSI Bus Busy and Data Available/ Data Acknowledge Handshaking. Generates a Strobe (STB) pulse to clock the Data and Command Registers.
12 BDSI Line Receivers	Isolates the 12 BDSI from the VDU Controller.
Data Register	Latches each data word as it is provided by the 12 BDSI.
Command Register	Latches each command word as it is provided by the 12 BDSI.
Parity Check	Generates an output called Parity Error ($\overline{PAE}$) to provide the terminal controller with a check on the parity of each word transferred through the 12 BDSI.
Memory Address Match	This circuit consists of three sections, a counter, latch and comparator. The counter reflects the present Main Shift Register address available. The latch contains the Main Shift Register address required. The comparator generates Memory Address Match ($\overline{MAM}$) when the latch and counter are coincident.

Circuit Functions

(Figure 14, SKD 11535L/1, sht 2)

Circuit	Function
Character Generation	The Character Generator consists of a latch, three Read Only memories, and a shift register. The latch contains part of the addressing that enables the ROMs to generate the character presently being displayed. The ROMs contain the bit patterns that generate characters. The shift register changes the parallel output of the ROMs to a serial bit pattern for use as noncomposite video data.
Line Shift Register	Contains forty data words for the present line. These words are loaded into the Character Generation latch sixteen times during each Character Line Time.
Main Shift Register	Contains 480 data words. These words are loaded forty at a time into the Line Shift register to write a complete line of characters during each Character Line Time.

Circuit	Function
Data Multiplexor	Loads the Main Shift Register either from its own output (recirculate mode) or from the Data Register (upgrade mode).
Shift Register Control	Clocks the Shift Register and controls the Data Multiplexor. Provides Clear Data, Cursor and Delineator information to the Line Shift Register.
Video Data Control	Controls the Video Data, Cursor Data and Delineator Data flops.

Circuit Functions

(Figure 14, SKD 11535L/1, sht 3)

Circuit	Function
Bit Time Clock	Produces a train of 50 nsec clock pulses synchronized with the local mains.
Bit Time Generator	Produces Bit Time pulses, ten of which form one Character Width Time (CWT). Input is the Bit Time Clock.
Character Width Time Generator	Generates timing pulses that define the width of one character on the screen. Sixty CWTs from one Row time (RT).
Row Time Generator	Generates timing pulses that define which row of the 10x16 character matrix is being written on the screen and provide addressing data to the ROMs to enable the required bit pattern. Sixteen Row Time form one Character Line Time (CLT).
Character Line Time Generator	Generates Character Line Time (CLT) pulses that define the height of one character on the screen. Generates the Last Line ($\overline{\text{LSTL}}$) pulse that is used as a vertical sync pulse by the video display unit. Input is $\overline{\text{RT15}}$.

Circuit	Function
Horizontal Drive Pulse Generator	Generates the horizontal drive pulse used by the video display unit. Input is from the CWT generator.
Frame Format Control and Shift Register Timing	Provides the clock pulses for the two memory shift registers and the memory address match circuit. Defines the frame size in terms of character widths and character lines. Provides Line End ($\overline{\text{LNE}}$) signal.

VDU Controller Flows (Figures 15 & 16)

General Description

The VDU Controller accepts 12 BDSI Command and Data words from the data terminal controller. Command words are used to determine the controller mode of operation. Data words are used as addresses in the Character Generation ROMs and as addresses in the Main Shift Register.

Any block of words transmitted to the VDU Controller has a format of Command and Data words mixed together. A sequence to perform the loading of a data character into an address would be as follows:

Command.	Load Address
Data.	Address
Command.	Load Data Same Address
Data	Character Data

Once the data character is loaded into an address in the Main Shift Register it is rotated through to the Line Shift Register by the Shift Register Timing. This timing ensures that the character is written on the video display screen at the proper place.

The flows show the loading of a data character into the Main Shift Register and then the generation of the bit pattern that writes the character on the video display screen.

The word sequence to load a data character is:

		CODE
Command	Load Address	4600
Data	Main Shift Reg. Address	000 to 479
Command	Load Data Same Address	4441
Data	Data Character for "A"	0101

In order to load a data address, both the Load Address and the Main Shift Register flows must be completed.

Load Address Flow

Terminal Controller assembles a word.

Transmit (TX-X, 11535, 1, 8B, F12-13, pin 12, J1-C) enables.
Command Bit (CMDB, 11535, 1, 7B, E12-3, pin 5, J1-B) enables.
Data Bits (DL07-X and DL01-X, 11535, 1, 8D, J1-4, F) enable
After 4 μsec Command Reset (CMDR, 11535,1,7B, F12-3, pin 5) enables for 2 μsec.

Bus Busy (BBSY, 11535, 1, D4, C13-11) disables.

After 4 μsec Command Set (CMDS, 11535, 1, 7B, F12-2, J1-E) enables for 2 μsec.

BBSY enables.

After 12 μsec Data Available (DAV-X, 11535, 1, 8A, D13-3, J1-9) enables.

After 500 nsec STB (11535,1,6A, E11-4) enables.

Command Register (11535, 1, col.4) is clocked.

Ready (11535, 1, 4D, E10-10) enables
Set (11535, 1, 4D, E10-9) enables.

Load Address (LOADD, 11535, 3, 6A, E13-6) enables.

Data Acknowledge (DAK-X, 11535, 1, 8A, C13-8, J1-K) enables.

After 500 nsec DAV-X disables

After 500 nsec DAK-X disables.

At this time the flow stops until the Data Register Full (DRF,11535, 1, 6B, C9-5) signal enables. This signal enables when the Data Register has been loaded with the required Main Shift Register Address. The flow is:

Terminal controller assembles a data word.

Data lines enable
DAV-X enables
After 500 nsec STB enables.
The Data Register is clocked
DAK-X enables
DRF enables

At BT1, Address Parallel Enable (APE, 11535, 3,5A, B7-8) enables
During BT3 Address Clock (ACL, 11535, 3, 58, E7-1) enables

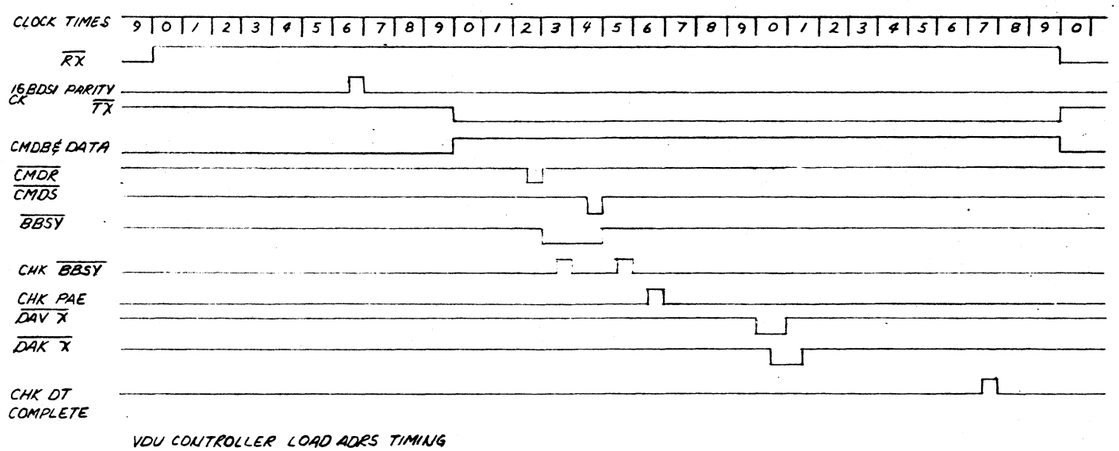
Memory Address Latch (11535, 1, 2B, C10 and B10) loads the address.

2 Reset Data Register (ZRDR, 11535, 3, 5A, D8-11) enables

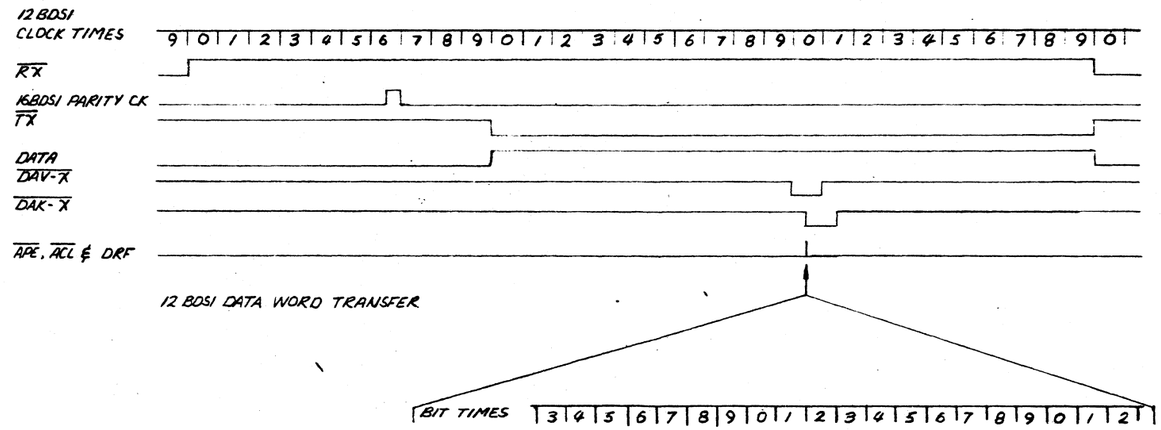
DRF disables

After 500 sec DAV-X disables

After 500 nsec DAK-X disables.



VDU CONTROLLER LOAD ADRS TIMING



VDU CONTROLLER TIMING

rev	eco	description	date	by	chk	apprvd

used on		drawn	CONSOLIDATED COMPUTER INC. OTTAWA
scale	date	design eng	LOAD ADDRESS FLOW VDU CONTROLLER
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0°30'		checked	
		final apprvl	
material	finish		title
			sheet of — no. FIGURE 16 — rev

TRANSLITEX IN 000-0-70

Character Generator Flow

The first data character is loaded by the Character Generator at Bit Time 0, Row Count 0, Character Width Time 4 of Character Line Time x where x is 3-15

The data character bits and the row count combine to address a bit pattern in the character generator ROMs.

At Bit Time 8 ($\overline{BT8}$, 11535,3,5C,L2-3) the bit pattern is loaded into a shift register (11535,2,2B,E1-9).

the Video Data Flop (11535,2,2B,E2-8) is reset

At Bit Time 9 the first bit of data is presented to the video display unit. Each Bit Time Clock presents another bit of data until ten have been sent. These bits make up the first row of the first character on the screen.

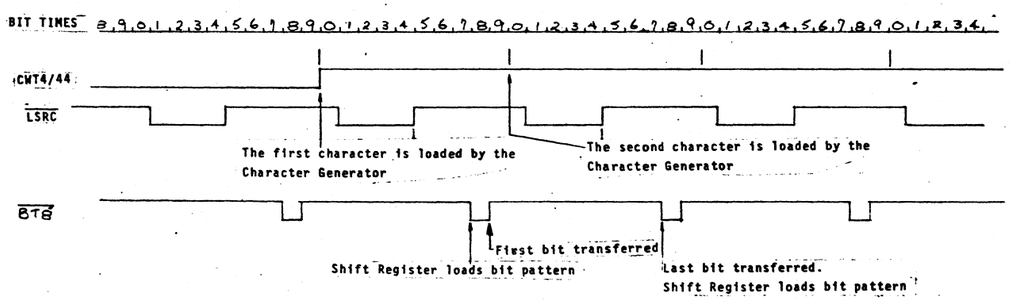
At $\overline{BT0}$ of Character Width Time 5, the second data character is loaded by the character generator and is transferred to the video display unit.

This sequence of load and display repeats until Character Width Time 4/44 (CW 4/44, 11535,3,6B,D2-13) disables.

Line Shift Register Clock ($\overline{LSRC}$, 11535,3,6B,D3-11) disables.

When the timing sequence returns to CWT4 $\overline{LSRC}$ enables and the next row of bit patterns is written on the video display screen.

During Row Time 15 ($\overline{RT15}$, 11535,3,2D,E5-17) the line Shift Register is loaded with forty data characters.



This sequence repeats until CWT4/44 disables.

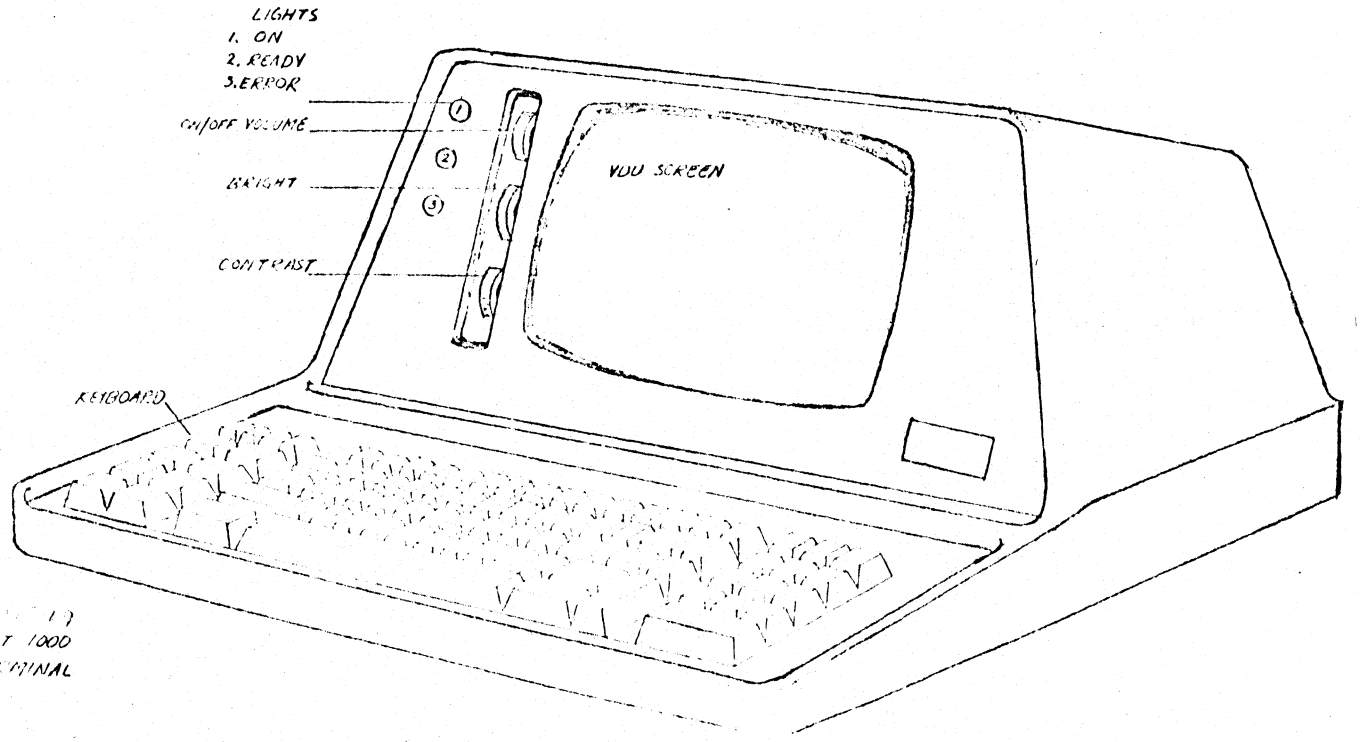
CONSOLIDATED COMPUTER INC. OTTAWA

VDU Controller Character Generator Flow

FIGURE 16

Key Data Terminal Operator Controls

The Key Data Terminal (KDT) includes three controls that the operator uses to adjust the volume of the tone used to signal errors, and the brightness and contrast of the information on the display screen. The KDT status is shown by three indicator lamps on the left side of the graphic display front panel, ON, READY, and ERROR. Figure 19 shows the controls and their functions.



KEY-EDIT 1000
DATA TERMINAL

Keyboard Controller Adjustment

The only adjustment provided on the keyboard controller pcb is the 10 ms one shot used in the error detection circuits. The adjustment sequence is:

1. Remove the data terminal cover and turn the terminal on.
2. Adjust R8 until the pulse seen at B5-7 is 10 ms long. The pulse can be initiated by pressing any key on the keyboard.

Keyboard Controller Adjustments

NAME	MEASURE	ADJUST	LIMITS
10 ms delay	B5-7	R8	10ms ± 1ms

VDU Controller Adjustments

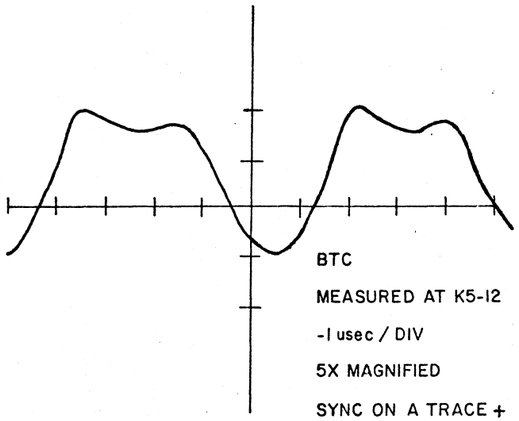
1. Remove the terminal cover and slide the keyboard and VDU controllers forward in order to allow access to R25 and R6 on the VDU Controller.
2. Turn the terminal on and adjust R25 until the voltage at the junction of R6 and R8 is 4.2 volts. If a large change is made, allow the meter to settle before reading.
3. Check that the raster is stable. If not, adjust R25 as necessary and check the voltage.
4. The voltage should be 4.2v ± .1v in order to allow the phase lock loop circuit the widest possible control range. Any major variation from this value indicates a possible problem in the main timing sequence. Each of the major timing pulses should be checked, using the VDU checkout procedure in Figures 17 and 18.

VDU Controller Adjustments

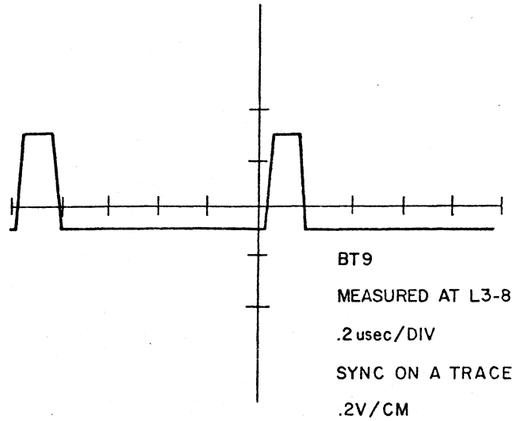
NAME	ADJUST	MEASURE	LIMITS
Bit Time Clock Freq.	R25	R6 voltage	4.2 ± .1v

CAUTION: Do not ground the oscilloscope to the pcb if the terminal is connected to the system.

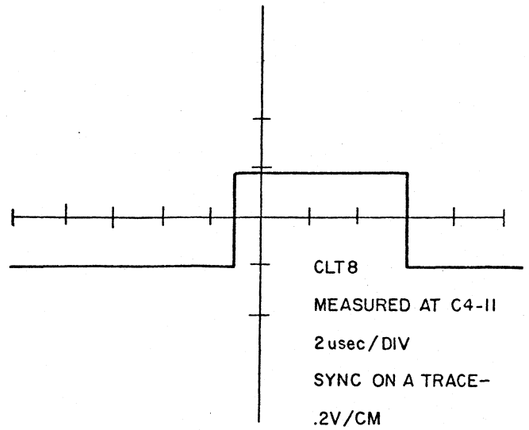
If the raster on a KDT is completely unrecognizable, the timing circuits on the VDU Controller may be malfunctioning. Disconnect J2 immediately to avoid damaging Q106 on the Ball Bros. video display unit.



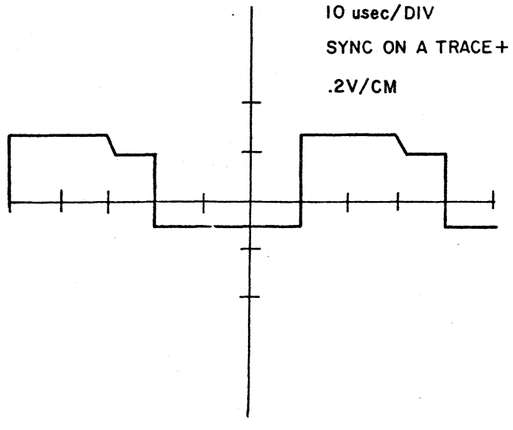
BTC
MEASURED AT K5-12
-1 usec / DIV
5X MAGNIFIED
SYNC ON A TRACE +
.2V/CM



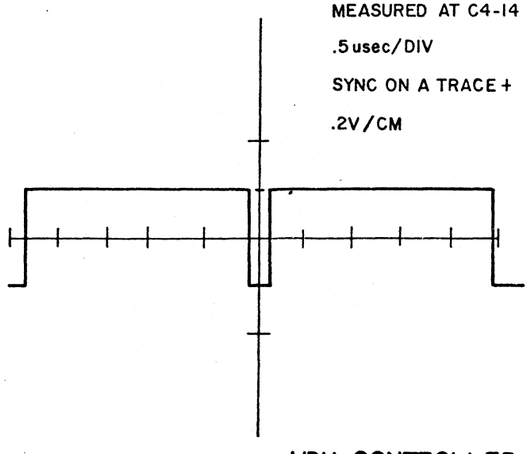
BT9
MEASURED AT L3-8
.2 usec/DIV
SYNC ON A TRACE +
.2V/CM



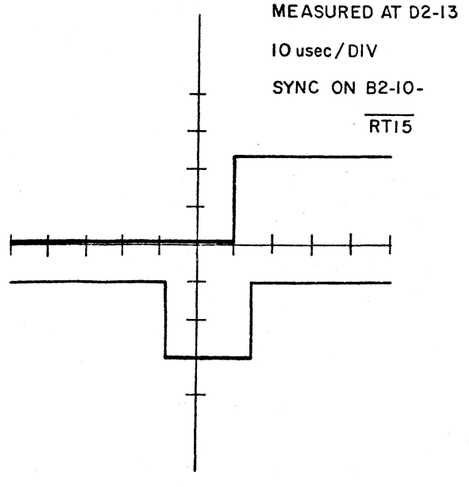
CLT8
MEASURED AT C4-11
2 usec/DIV
SYNC ON A TRACE-
.2V/CM



CWT 30
MEASURED AT E4-8
10 usec/DIV
SYNC ON A TRACE+
.2V/CM



$\overline{RT15}$
MEASURED AT C4-14
.5 usec/DIV
SYNC ON A TRACE +
.2V/CM



CWT4/44
MEASURED AT D2-13
10 usec/DIV
SYNC ON B2-10-
$\overline{RT15}$

VDU CONTROLLER MAJOR TIMING PULSES
FIGURE. 17 (SHEET 1 OF 2)

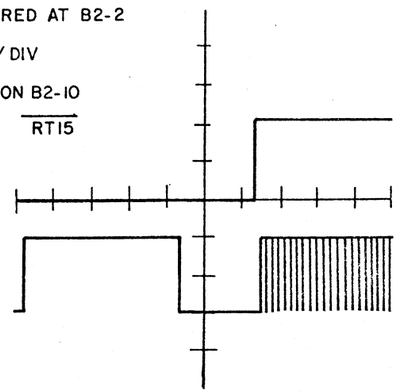
LSRC

MEASURED AT B2-2

5 usec / DIV

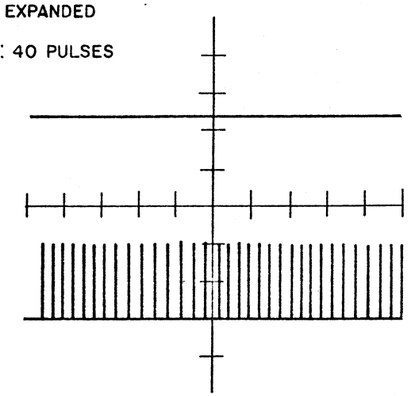
SYNC ON B2-10

$\overline{\text{RT15}}$



LSRC EXPANDED

NOTE: 40 PULSES



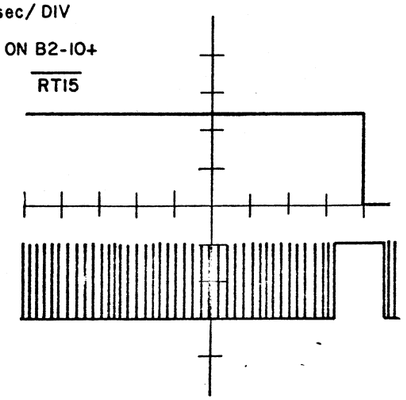
MSRC

MEASURED AT D6-12

100 usec / DIV

SYNC ON B2-10+

$\overline{\text{RT15}}$



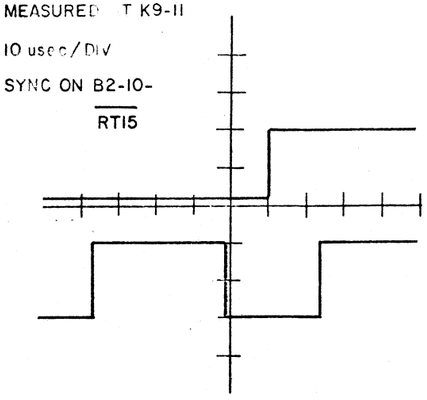
HS

MEASURED AT K9-11

10 usec / DIV

SYNC ON B2-10-

$\overline{\text{RT15}}$



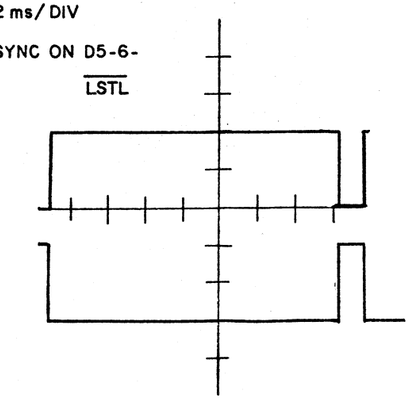
VS

MEASURED AT K9-9

2 ms / DIV

SYNC ON D5-6-

$\overline{\text{LSTL}}$

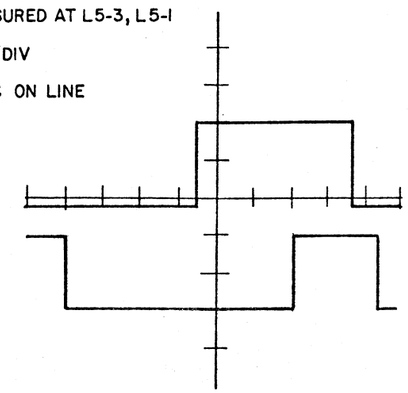


PHASE LOCK LOOP

MEASURED AT L5-3, L5-1

2ms/DIV

SYNC ON LINE



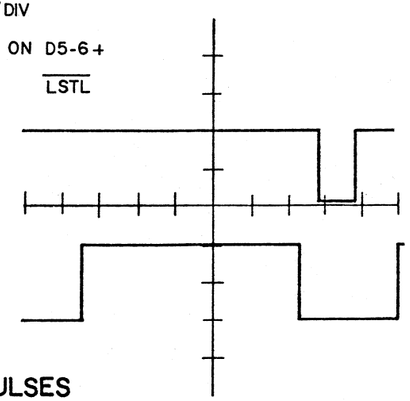
CLT 3

MEASURED AT B5-8

2 ms / DIV

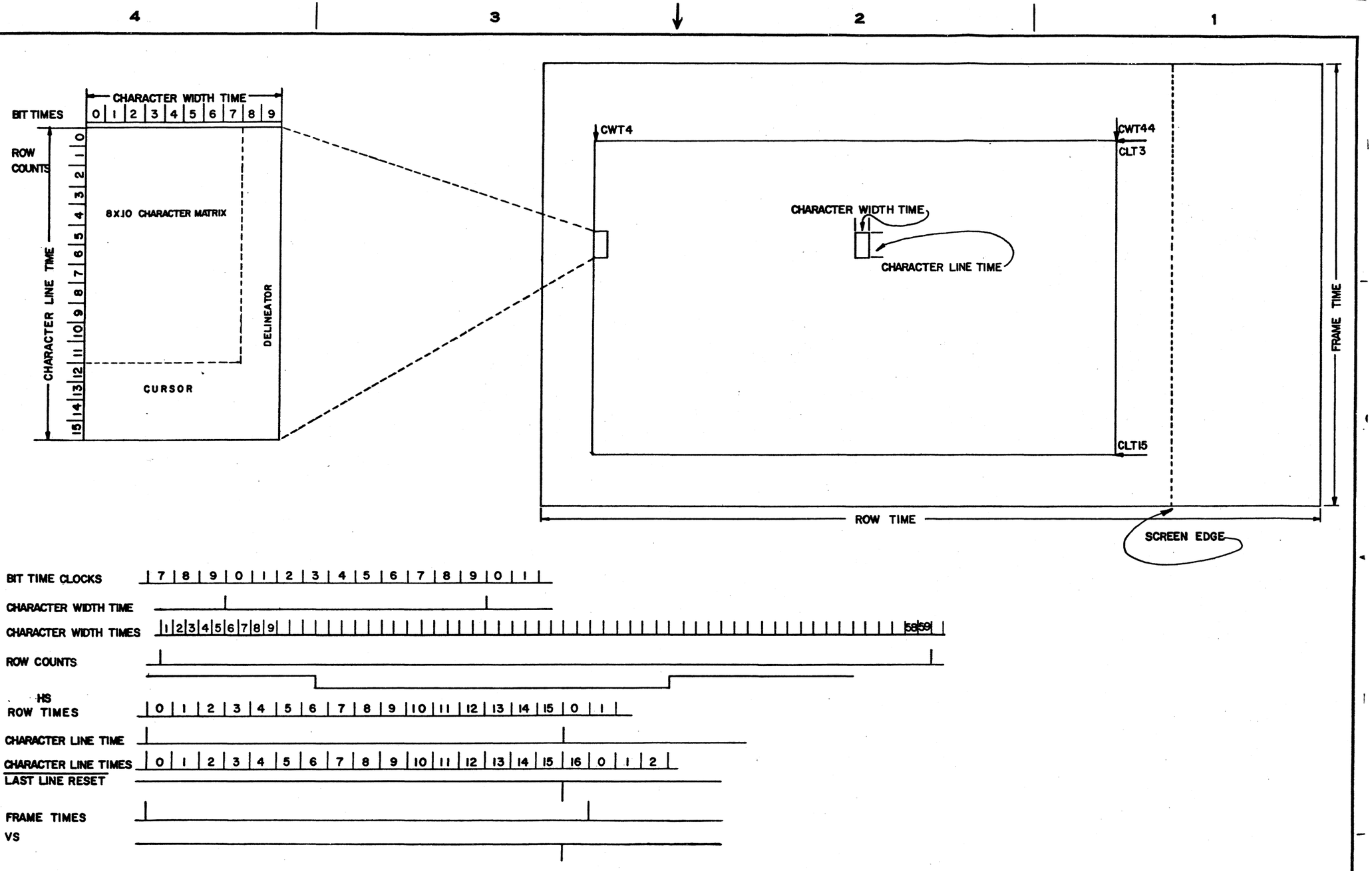
SYNC ON D5-6+

$\overline{\text{LSTL}}$



VDU CONTROLLER MAJOR TIME PULSES

FIGURE. 17 (SHEET 2 OF 2)



rev	eco	description	date	by	chk	apprvd

used on

scale | date: 1 MAR 73

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

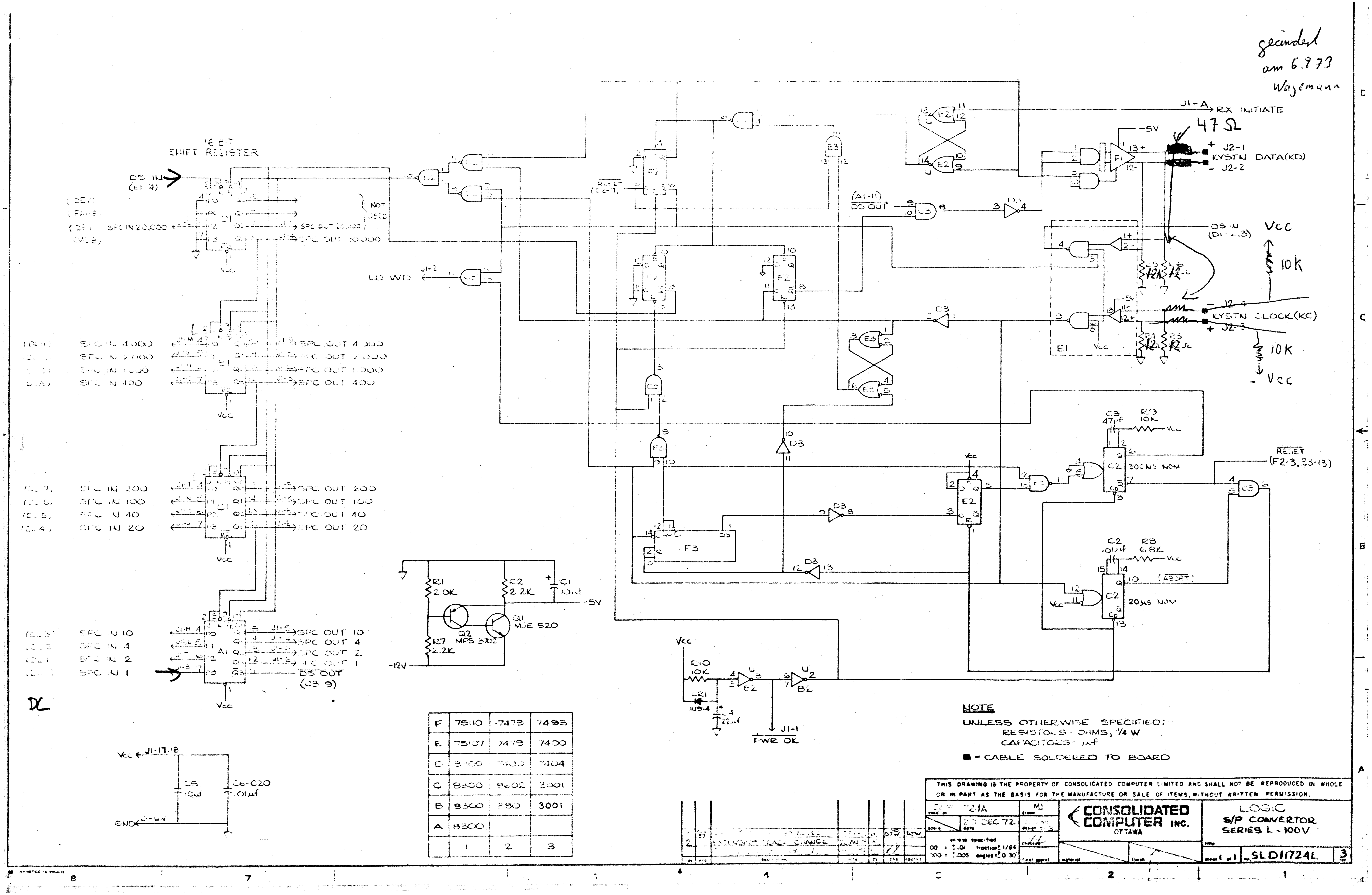
drawn: R.W.T.
design apprvl
checked
final apprvl

CONSOLIDATED COMPUTER INC. OTTAWA

material | finish

title: VDU CONTROLLER MAIN TIMING

sheet of | no. FIGURE 18 | rev



	1	2	3
F	75110	7473	7495
E	75107	7479	7400
D	8300	7400	7404
C	8300	8602	3001
B	8300	880	3001
A	8300		

NOTE

UNLESS OTHERWISE SPECIFIED:
RESISTORS - OHMS, 1/4 W
CAPACITORS - µf

■ - CABLE SOLDERED TO BOARD

CONSOLIDATED COMPUTER INC. OTTAWA

LOGIC
S/P CONVERTOR
SERIES L-100V

20 DEC 72

SLD11724L 3

0	0	ILLEGAL
0	1	TEST CLOCK; TEST MODE OPERATION
1	0	CLOCK TIME OSCILLATOR; NORMAL OP.
1	1	ILLEGAL

W3	FUNCTION
-	PARITY OPTION INSTALLED
	!TY OPTION DELETED

CLOCK TIME OSCILLATOR SOCKET (CTO)

C1 330pF R1 20K Vcc — C2 330pF R2 10K Vcc — H6 — H5 — W1 W2 — CTO — TC

TEST CLOCK (J2-1)

S/P CONVERTER PARALLEL DATA IN — H4 — (CNT 1) (CNT 2) (CNT 4) (CNT 8) (CNT 16) — C3 100pF — F2 — (RESET) — D3 — F6 — F4 — R25 2.2K Vcc

S/P CONVERTER PARALLEL DATA OUT

SPC OUT 20000 J1-C — SPC OUT 10000 J1-4 — SPC OUT 10 J1-5 — SPC OUT 1 J1-6 — SPC OUT 20 J1-E — SPC OUT 200 J1-F — SPC OUT 4000 J1-9 — SPC OUT 400 J1-10 — SPC OUT 100 J1-K — SPC OUT 1000 J1-L — SPC OUT 2000 J1-13 — SPC OUT 4 J1-14 — SPC OUT 2 J1-P — SPC OUT 40 J1-R

D2 D3 C3 B3 A3 C2 B2 A2 — CMD (D5-11) — F4 D3

12 BDSI BUS

R3 1K J2-H DP — R22 1K J2-J PARE — R28 1K J2-B CMDB — R4 1K J2-2 DL3 — R5 1K J2-3 DLO — R6 1K J2-5 DL4 — R7 1K J2-4 DL7 — R8 1K J2-6 DL11 — R9 1K J2-F DL8 — R10 1K J2-L DL6 — R11 1K J2-10 DL9 — R12 1K J2-11 DL10 — R13 1K J2-M DL2 — R14 1K J2-N DL1 — R15 1K J2-12 DL5

R21 2.2K R.D. W3 — R30 2.2K — F6 — PARE (F6-8)

SPC IN 20000 J1-D — SPC IN 40.000 J1-B — SPC IN 10 J1-H — SPC IN 1 J1-B — SPC IN 20 J1-J — SPC IN 200 J1-7 — SPC IN 4000 J1-M — SPC IN 400 J1-12 — SPC IN 100 J1-N — SPC IN 1000 J1-11 — SPC IN 2000 J1-S — SPC IN 4 J1-16 — SPC IN 2 J1-T — SPC IN 40 J1-15

J1-A Rx INITIATE

LD WD J1-2 — F4

Vcc { J1-17 J1-18 — C6 10UF + — C7-C21 .01UF Vcc

GND { J1-U J1-V — J2-P J2-R J2-S J2-13 J2-14 J2-15 GND

PWR OK J1-1

(CNT 1) (CNT 2) (CNT 4) (CNT 8) (CNT 16) — F3 — H3 — F1 — H1 (CHK OF CPT) — (STOP TIME 2) — (CHK BBSY) — (CHK BBSY) — H2 — STOP TIME 3 (F2-11) — E2 — H5 — CHK PARE (F6-9)

F5 (TRENBL) — (BEGIN) — F5 — STOP TIME 3 (W2-3) — F2

SPC IN 100.000 J1-3 — D4

R26 1K — C4 470pF — D5 — E4 — R24 1K J2-K DAK

R27 1K — C5 470pF — D4 D5 — F4 — E2 (DTFE)

E3 — E2

R20 2.2K — F6 — PARE (D4-14) — CHK PARE (H1-12)

12 BDSI BUS

R17 1K J2-D CMDR — R16 1K J2-E CMDS — R18 1K J2-7 BBSY — CMD (D2-11)

R19 1K J2-C TX — R20 1K J2-A EX — R21 1K J2-8 DEVI — R23 1K J2-9 DAV

NOTE: UNLESS OTHERWISE SPECIFIED:
RESISTORS - OHMS 1/4 W

CHIP CHART

	1	2	3	4	5	6
H	8836	3001	3001	7493	7400	8602
F	7410	7479	7404	7402	7479	858
E		3001	7479	8093	858	
D		7475	7437	380	380	
C		7475	7475	8093	380	
B		7475	7475	8093	380	
A		7475	7475	8093	380	

rev	eco	description	date	by	chk	approvd
3	EC 0683	CRCUIT CHANGES	16 FEB 73			DJW
2	EC 0611	CLEAN UP	16 FEB 73			DJW
1		PREPRODUCTION RELEASE	8 DEC 72	ST		

used on: SLD 11725A — NONE — scale — 8 DEC 1972 — date — unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0° 30'

G. TURNER drawn — D WALSH design engr — checked — final apprvl — material — finish

CONSOLIDATED COMPUTER INC. OTTAWA

Title: LOGIC DIAGRAM SERIES L - 100 V 12 BDSI SIMULATOR

sheet 1 of 1 — SLD 11725 L — rev 3

TRANSTEX IS 000-0-72

8 7 6 5 4 3 2 1

Data Terminal Power Supply Adjustments

The +15 volt power supply can be adjusted for voltage and short circuit current output. The adjustment sequence is:

1. Disconnect the cables at J6 and J7.
2. Adjust R5 until the voltage between R14 and ground is 15 volts.
3. Turn R3 fully counter-clockwise.
4. Adjust the short circuit current between R14 and ground to 750 ma.
5. Reconnect the cables to J6 and J7 and check the supply output voltage.

The +5 volt power supply adjustment sequence is:

1. Disconnect the cables from J8 and J9.
2. Adjust R12 until the voltage between R15 and ground is 5 volts.
3. Turn R10 fully counter-clockwise.
4. Adjust the short circuit current between R15 and ground to 2 amp.
5. Reconnect the cables to J8 and J9 and check the supply output voltage.

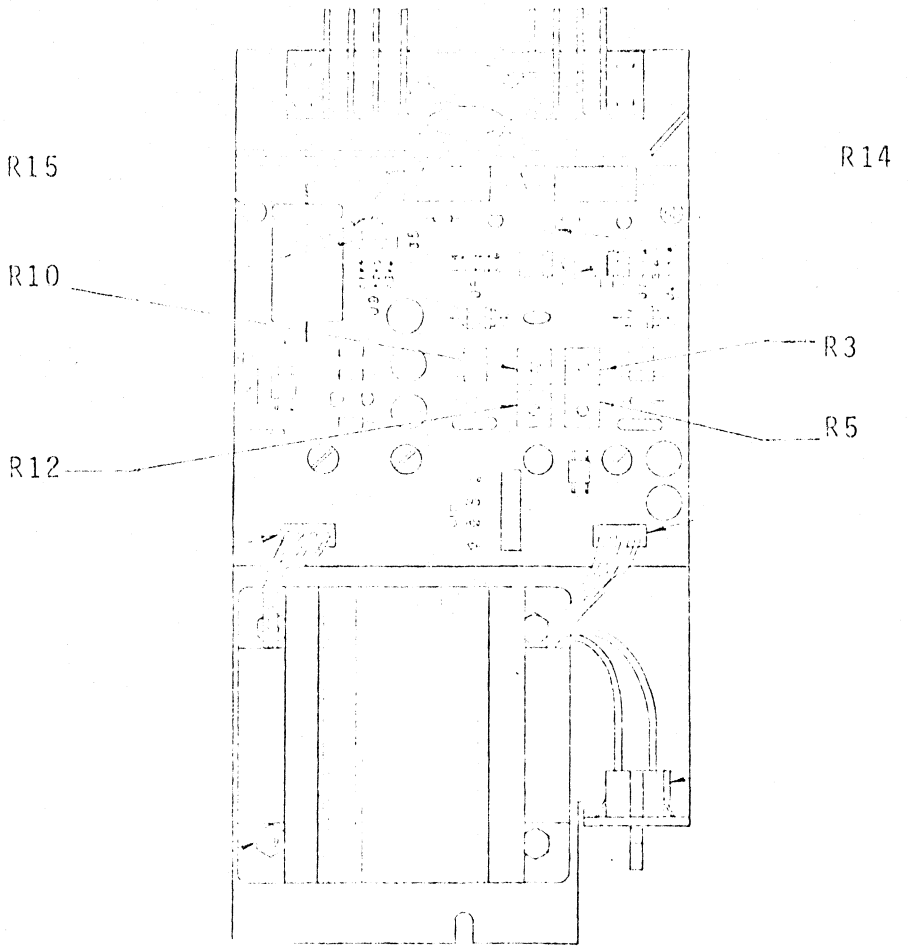
CAUTION: Do not short circuit these power supplies without adjusting R3 and R10 fully CCW.

The -12 and -9 volt power supplies are not adjustable or short circuit protected. The -12 volt power supply output can be checked between J8-1 and J8-6 and the -9 volt supply between J8-2 and J8-6.

Do not disconnect the +5 volt power supply from the L150 adaptor without disconnecting the -12 volt power supply. If either supply is left connected, damage to the line drivers and receivers may result.

Data Terminal Power Supply Adjustments

SUPPLY	ADJUSTMENT	METER CONNECTIONS	LIMITS
+15 v	Voltage,R5	R14, GND	15v ± .1v
	Short Circuit Current, R3	R14, GND	750 ma ± 50
+5 v	Voltage, R12	R15, GND	5v ± .05v
	Short Circuit Current, R10	R15, GND	2A ± 200 ma
-12 v	Voltage	J8-1, J8-6	-12v ± .6v
-9 v	Voltage	J8-2, J8-6	-9v ± .5v



PCB ASSY. 11579A

VOLTAGE	JUMPER	L	N
115	1-3 & 2-5	2	1
220	2-3	4	1
230	2-3	5	1
240	2-3	6	1
250	2-3	7	1

NOTES:
- UNLESS OTHERWISE SPECIFIED RESISTOR. ARE IN OHMS, 5% 1/4W CAPACITOR ARE IN µF

REV	ECO	description	date	by	chk	approved
1		PRE PROD REL	14 DEC 73	RC		

SKD11577A	R.C.
unless specified .00 = ±.01 fraction = 1/64 .000 = ±.005 angles = ±0 30'	

CONSOLIDATED COMPUTER INC. OTTAWA

SCHEMATIC POWER SUPPLY DATA TERMINAL

SKD11577S

APPENDIX 1 - Mnemonics

ACL	Address Clock
APE	Adress Parallel Enable
BAC	Buffered Accumulator
BBSY	Bus Busy
BDSI	Bit Data Standard Interface
BMB	Buffered Memory Bus
BRUN	Buffered Run
BT	Bit Time
BTS	Buffered Time State
CLT	Character Line Time
CMDB	Command Bit
CMDR	Command Reset
CMDS	Command Set
CRF	Command Register Full
CUR	Cursor
CWT	Character Width Time
DAK	Data Acknowledge
DAV	Data Available
DEL	Deliniator
DL	Data Line
DP	Data Parity
DRF	Data Register Full
DS IN/OUT	Data Serial In/Out
EOL	End of Line
HS	Horizontal Signal
INCA	Increment Address
IOP	Input/Output Pulse

KSTB	Keystrobe
LD WD	Load Word
LLR	Last Line Reset
LNE	Line End
LSTL	Last Line
MAF	Match Flop
MAM	Memory Address Match
MSRC	Master Shift Register Clock
PAE	Parity Error
RC	Row Count
RDR	Reset Data Register
ROM	Read Only Memory
RT	Row Time
SPC IN/OUT	Serial/Parallel Convertor In/Out
VD	Video Data
VS	Vertical Signal
WRT/REC	Write Recirculate

APPENDIX 2 - FLOW DIAGRAM EXPLANATION

Flow diagrams

The flow diagrams given in this document show the sequence of events that occur during a particular operation of a controller. The peculiar format is used to show which events are dependent on others,as well as which events are simultaneous. A signal locator is provided to reduce the amount of time wasted looking for signals in the logics.

The flows are read from left to right, starting at the top left corner. Figure 1 shows examples of the format used in these flows. The first example shows that XXXX enables, then YYYY enables, then ZZZZ. The second shows AAAA enables, causing both BBBB and CCCC to enable simultaneously. The third example combines both possibilities to show that EEEE and HHHH are dependent on DDDD and that FFFF is dependent on EEEE.

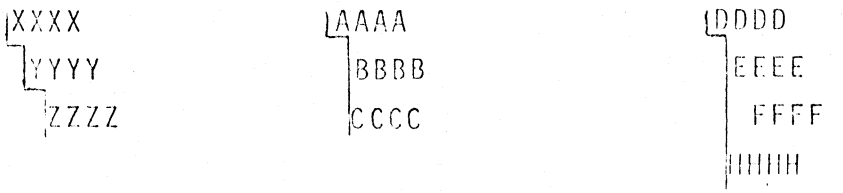


FIGURE 1

The locator is provided to show where the signal can be found in the logic rack. Figure 2 shows the meaning of each part of the locator.

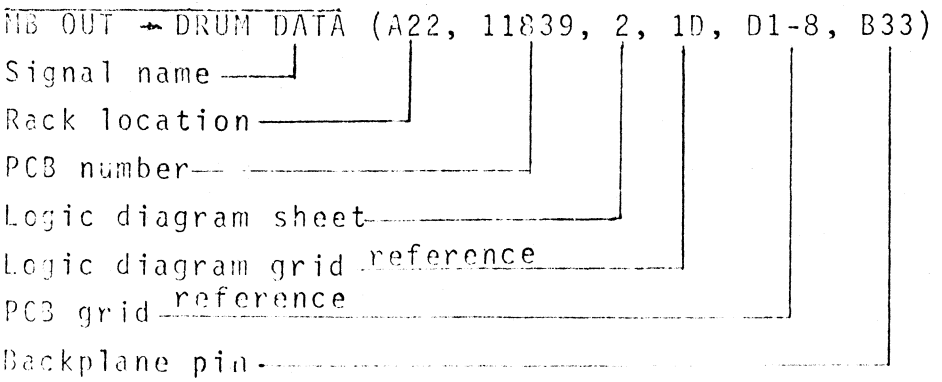


FIGURE 2

Using the locator involves reading only as much as necessary. When MB OUT-DRUM DATA occurs, it can be found in the disc write flow; the locator shows where it appears in the system. The outer numbers, A22 and B33 give the rack location and pin number that the signal should appear on. If MB OUT-DRUM DATA is not true at the proper time, the next two numbers, 11839 and D1-8, locate the pcb and IC pin in question. Gate chasing if necessary begins on the logic diagram at page 2, location 1D.

There are three exceptions to these rules. The logic diagram page number is included only if the logic has more than one page. The backplane pin number is given only of the signal being located actually appears on the backplane. The third exception is in the case of multiple IC registers and buffers. These are located on the logics only by row or column and on the pcb by IC location without output pin numbers, i.e.,

Track Address Select Register (A24, 11254, row B, G5, H5)

APPENDIX 3 - VCU IOT LIST

IOT 6301 Load VCU TX, Complete Interrupt Mask, and then Clear Accumulator.

The Accumulator contents will specify which transmission level, or levels (DMA 1, 2, or KYBD CMD), will cause an Interrupt to the CPU upon completion of transmission as follows:

BAC 4 (9).....KYBD CMD, Terminals 0 to 17_8
BAC 2 (10)....VCU DMA Level 2, Terminals 0 to 17_8
BAC 1 (11)....VCU DMA Level 1, Terminals 0 to 17_8

The VCU INT Mask will be cleared (reset) at power turn on, and by the Clear All Flags (CAF) IOT, 6007.

The VCU INT Mask will not affect the action of the VCU TX Abort Flag (see IOTs 6302 and 6304).

IOT 6302 Clear Accumulator, Read VCU Transmission Status, and then Clear (Reset) VCU TX Abort Flag.

AC IN 10 (AC 8)...TX Abort Flag Set (true), Terminals 0 to 17_8
AC IN 4 (AC 9)...KYBD CMD, TX Busy, Terminals 0 to 17_8
AC IN 2 (AC 10)..VCU DMA Level 2, TX Busy, Terminals 0 to 17_8
AC IN 1 (AC 11)..VCU DMA Level 1, TX Busy, Terminals 0 to 17_8

The three VCU TX levels (DMA 1, 2, and KYBD CMD) will be busy until the final transmission has been completed to their respective terminals.

The Abort Flag will be set (true), the VCU TX Complete INT Flag set, and an Interrupt generated to the CPU when any of the three TX levels is still busy after a period of 3 ms. This timeout will begin from the time that data is available to the VCU for transmission on any of the three TX levels. The TX busy status and the Abort Flag will be cleared (reset) at power turn on and by the Clear All Flags (CAF) IOT, 6007.

The TX busy status will also be cleared when the TX Abort Flag is set (true).

IOT 6304 Skip if VCU TX Complete Interrupt Flag is set (true), and then Clear VCU INT Flag.

The VCU INT Flag will be set (true) when the final transmission of any of the three TX levels (DMA 1, 2, or KYBD CMD) has been completed. This action will be independent of the VCU INT Mask. However, an Interrupt to the CPU will be allowed as a function of the VCU INT Mask (see IOT 6501).

The VCU INT Flag will be cleared (reset) at power turn on and by the Clear All Flags (CAF) IOT, 6007.

IOT 6311 Load Memory Address Register for VCU DMA Level 1, and then Clear Accumulator.

The Accumulator contents will specify the Starting Memory Address of the DMA transfer. Any Starting Address from 0000_8 to 7777_8 will be legitimate. The contents of this register will be indeterminate at power turn on.

IOT 6312 Load Extended Memory Address Register for VCU DMA Level 1, and then Clear Accumulator.

The Accumulator contents will specify the Extended Memory Address (field) of the DMA transfer as follows:

(MSB) BAC 40 (6).....DMA EMA 4 (EMA 0)
BAC 20 (7).....DMA EMA 2 (EMA 1)
(LSB) BAC 10 (8).....DMA EMA 1 (EMA 2)

Any field from 0 to 7 will be legitimate. The contents of this register will be indeterminate at power turn on.

IOT 6314 Load Word Count Register for VCU DMA Level 1, Clear Accumulator, and Initiate Transfer.

The Accumulator contents will specify the two's complement of the number of words in the transfer.

Any word count from 7777_8 (1 word) to 0000_8 (4096_{10} words) will be legitimate. The contents of this register will be indeterminate at power turn on.

IOT 6321 Load Memory Address Register for VCU DMA Level 2, and then Clear Accumulator.

The Accumulator contents will specify the Starting Memory Address of the DMA transfer. Any starting address from 0000_8 to 7777_8 will be legitimate. The contents of this register will be indeterminate at power turn on.

IOT 6322 Load Extended Memory Address Register for VCU DMA Level 2, and then Clear Accumulator.

The Accumulator contents will specify the Extended Memory Address (field) of the DMA transfer as follows:

(MSB) BAC 40 (6)...DMA EMA 4 (EMA 0)
BAC 20 (7)...DMA EMA 2 (EMA 1)
(LSB) BAC 10 (8)...DMA EMA 1 (EMA 2)

Any field from 0_8 to 7_8 will be legitimate. The contents of this register will be indeterminate at power turn on.

IOT 6324 Load Word Count Register for VCU DMA Level 2, Clear Accumulator, and Initiate Transfer.

The Accumulator contents will specify the two's complement of the number of words in the transfer.

Any word count from 7777_8 (1 word) to 0000_8 (4096_{10} words) will be legitimate.

The contents of this register will be indeterminate at power turn on.

The format of terminal graphic display data as provided via VCU DMA Level 1 or 2 will be as follows:
(Ref: SK HWHS-225A-1)

(MSB) DMA MO 4000 (BMB 0).....CMDB
DMA MO 2000 (BMB 1).....Not Used
DMA MO 1000 (BMB 2).....Not Used
DMA MO 400 (BMB 3).....DL 8
DMA MO 200 (BMB 4).....DL 7

DMA MO 100 (BMB 5).....DL 6
DMA MO 40 (BMB 6).....DL 5
DMA MO 20 (BMB 7).....DL 4
DMA MO 10 (BMB 8).....DL 3
DMA MO 4 (BMB 9).....DL 2
DMA MO 2 (BMB 10).....DL 1
(LSB) DMA MO 1 (BMB 11).....DL 0

The 12 BDSI Address (DL 9 to DL 11) will be provided by hardware.

IOT 6331 Skip if Terminal-Keyboard 0 to 17_8 Interrupt Flag is Set (true).

The fact that the KYBD INT Flag is set (true) will cause an Interrupt to the CPU.

The KYBD INT Flag for KYBD Group 0 to 17_8 will be set (true) when KYBD Data and terminal address information are available to be read by the CPU.

The KYBD INT Flag will be cleared (false) at power turn on by the Clear All Flags (CAF) IOT, 6007, and by IOT 6334.

IOT 6332 Clear Accumulator, Read Terminal-Keyboard 0 to 17_8 Address, and remove the KYBD INT Condition to the CPU.

The Accumulator will be loaded with the binary representation of the terminal address of the highest priority terminal-keyboard with available data in Keyboard Group 0 to 17 . (Terminal-keyboard 0 will have highest priority and keyboard 17 will have lowest priority.)

The bit assignment will be as follows:

(MSB) AC IN 10 (AC 8).....KYBD RX ADRS 10
AC IN 4 (AC 9).....KYBD RX ADRS 4
AC IN 2 (AC 10).....KYBD RX ADRS 2
(LSB) AC IN 1 (AC 11).....KYBD RX ADRS 1

This IOT does not clear (reset) the KYBD INT Flag.

IOT 6334 Clear Accumulator, Read Terminal-Keyboard 0 to 17_8 Data, and then Clear Terminal-Keyboard 0 to 17_8 Interrupt Flag.

The Accumulator will be loaded with the data of the highest priority terminal-keyboard with available data in KYBD Group 0 to 17_8. (KYBD 0 will have highest priority and KYBD 17_8 will have lowest priority.)

The bit assignment of KYBD data will be as follows: (Ref: SK EQHS 224A-1)

(MSB) AC IN 4000 (AC 0)...DL 11 (true to indicate KYBD Status)
AC IN 2000 (AC 1)...DL 10 (true to indicate KYBD Error)
AC IN 1000 (AC 2)...Not Used
AC IN 400 (AC 3)...Not Used
AC IN 200 (AC 4)...DL 7
AC IN 100 (AC 5)...DL 6
AC IN 40 (AC 6)...DL 5
AC IN 20 (AC 7)...DL 4 — KYBD Data or
AC IN 10 (AC 8)...DL 3 — KYBD Status
AC IN 4 (AC 9)...DL 2
AC IN 2 (AC 10)..DL 1
(LSB) AC IN 1 (AC 11)..DL 0

This IOT must be preceded by IOT 6332.

Two types of KYBD error can be detected and notified via AC IN 2000 (AC 1). These are as follows: (Ref: SK EQHS-224A-1)

1. Two keys are depressed within a period of 10.0 ms.
2. A data character is generated at the keyboard before the previous data character has been transferred to the 12 BDSI.

IOT 6341 Load Terminal-Graphic Display Address Register for VCU DMA Level 1 Transmission to one of Terminals 0 to 17_8, and then Clear Accumulator.

The bit assignment will be as follows:

```
(MSB)  BAC 10 (8).....Transmission Address 10 (8)
       BAC  4 (9).....Transmission Address  4 (9)
       BAC  2 (10)....Transmission Address  2 (10)
(LSB)  BAC  1 (11)....Transmission Address  1 (11)
```

The contents of this register will be indeterminate at power turn on.

IOT 6342 Load Terminal-Graphic Display Address Register for VCU DMA Level 2 Transmission to one of Terminals 0 to 17_8, and then Clear Accumulator.

The bit assignment will be as follows:

```
(MSB)  BAC 10 (8).....Transmission Address 10 (8)
       BAC  4 (9).....Transmission Address  4 (9)
       BAC  2 (10)....Transmission Address  2 (10)
(LSB)  BAC  1 (11)....Transmission Address  1 (11)
```

The contents of this register will be indeterminate at power turn on.

IOT 6344 Load Terminal-Keyboard Address Register for KYBD Command Transmission to one of Terminals 0 to 17_8, and then Clear Accumulator.

The bit assignment will be as follows:
(Ref: SK EQHS-224A-1)

```
(MSB)  BAC 400 (3).....DL 8  (Not Used)
       BAC 200 (4).....DL 7  (Not Used)
       BAC 100 (5).....DL 6  (On Line)
       BAC  40 (6).....DL 5  (Not Used)
       BAC  20 (7).....DL 4  (Tone 2 Bit)
       BAC  10 (8).....DL 3  (Tone 1 Bit)
       BAC   4 (9).....DL 2  (1/2 Second)
       BAC   2 (10)....DL 1  (Status)
(LSB)  BAC   1 (11)....DL 0  (Error Lamp)
```

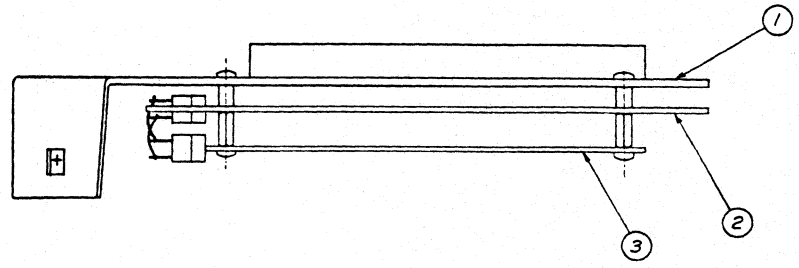
The 12 BDSI Address (DL 9 to 11) and the CMDB will be provided by hardware.

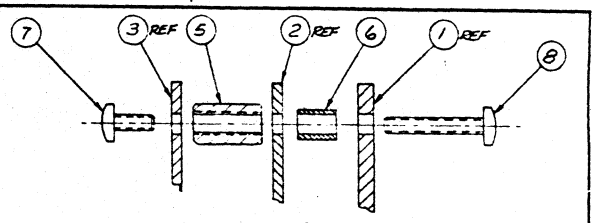
6351 Load Terminal-KYBD Data Register for KYBD Command TX Level and then clear Accumulator.
The Bit Assignment is as follows: (REF. SKEQHS-224A-1)

BAC 0 to 2 ----- Not Used
BAC 3 ---------- DL 8 (Not Currently Used) (MSB)
BAC 4 ---------- DL 7 (Not Currently Used)
BAC 5 ---------- DL 6 (On Line)
BAC 6 ---------- DL 5 (Not Currently Used)
BAC 7 ---------- DL 4 (Tone 2 Bit)
BAC 8 ---------- DL 3 (Tone 1 Bit)
BAC 9 ---------- DL 2 (1/2 Second)
BAC 10 --------- DL 1 (Status)
BAC 11 --------- DL 0 (Error Lamp) (LSB)

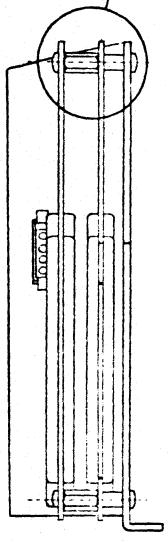
APPENDIX 4

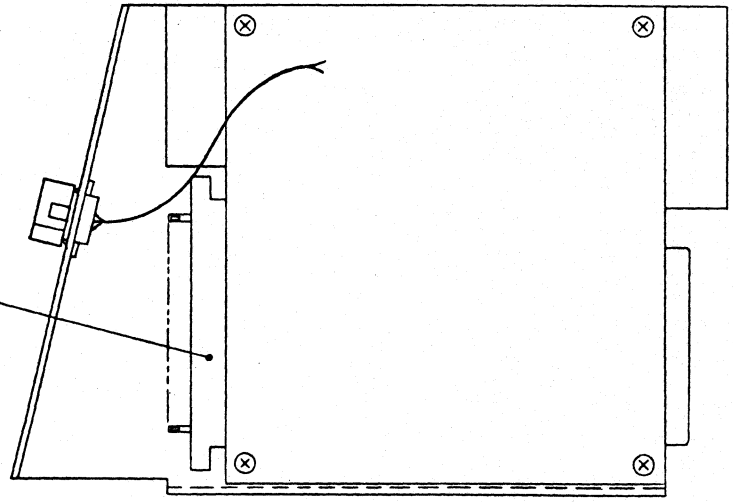
Assembly Drawings and Parts Lists





TYPICAL 4 PLACES





FOR PARTS LIST SEE SHEET 2

rev	orn	description	date	by	chk	approved
1		PREPRODUCTION REL.	5 DEC 72	GT		

used on: SLD11755A & SLD11311A
drawn: GT
scale: 1/1
date: 5 DEC 72
design: [illegible]
checked:
unless specified
.00 = ±.01 fractions ± 1/64
.000 = ±.005 angles ± 0° 30'
material:

CONSOLIDATED COMPUTER INC.
OTTAWA

ASSEMBLY
L150 ADAPTER
SERIES L 100 V

title
sheet 1 of 2
SLB11739A
rev 1

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: GT	DATE 5 DEC 72	APPROVED BY D WALSH
USED ON ASSEMBLY SLD1175A & SLD11817A	DRAWING REV 1	
ASSEMBLY NO SLB11739A	SHT 2 OF 2	

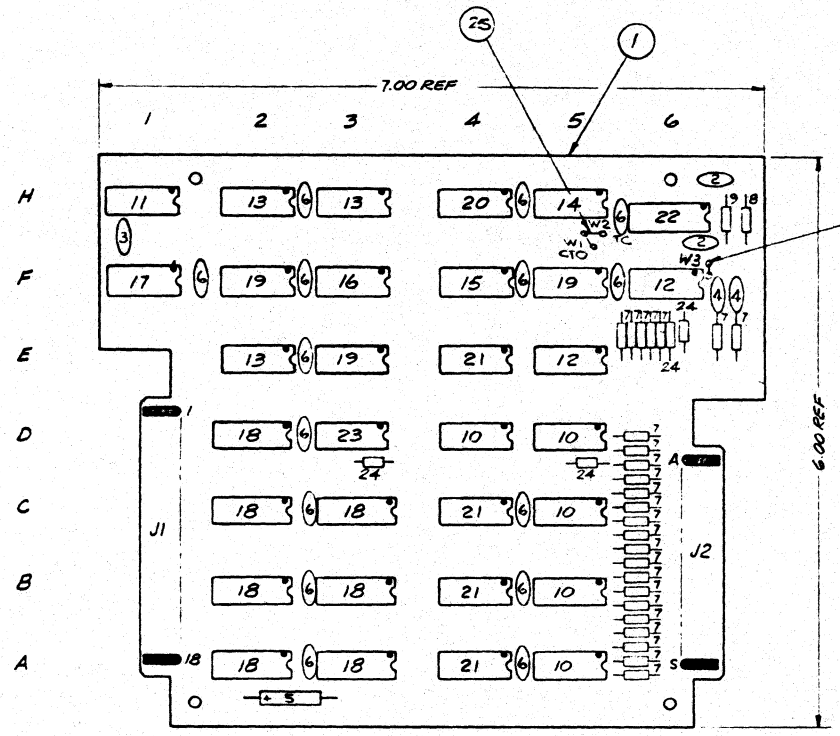
TITLE: ASSEMBLY
L150 ADAPTER
SERIES L-100V

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLC11726 M		1	MOUNTING BRACKET			
2	SLC11725A		1	P.C.B. ASSY, 12 BDSI SIMULATOR			
3	SLB11724-A		1	P.C.B. ASSY, S/P CONVERTER			
4	SLB11729A		1	ASSY. L150 ADAPTER INTERCONNECT			
5	93152		4	SPACER, HEX. TAPPED 4-40 X .438 LG	CAMBION-350-7416-06 AMATOM-8105-A-0440		
6	93151		4	SPACER, ROUND, NO. 4 CLEAR X .250 LG	SPAE-NAUP SPA-2		
7	90043-12		4	SCREW, PAN HD, 4-40 X .25 LG			
8	90043-15		4	SCREW, PAN HD, 4-40 X .62 LG			
9							
10							



NOTE:

W1	W2	FUNCTION
0	0	ILLEGAL
0	1	TEST CLOCK; TEST MODE OR
1	0	CLOCK TIME OSCILLATOR ; NORMAL OPERATION
1	1	ILLEGAL

W3	FUNCTION
0	PARITY OPTION INSTALLED
1	PARITY OPTION DELETED

FOR PARTS LIST SEE SHEETS 2&3

rev	eco	description	date	by	chk	approvd
2	SL 1162	JUMPERS & TABLE ADDED	16 FEB 73	[illegible]	[illegible]	DJW
1		PREPRODUCTION RELEASE	8 DEC 72	GT		

used on: SLC 11739A | drawn: G. TURNER | scale: 1/1 | date: 8 DEC 1972 | design: D WALSH | checked | final apprvl | material | finish

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

title: P.C.B. ASSEMBLY SERIES L-100V 12 BDSI SIMULATOR

sheet 1 of 3 | no. SLC 11725A | 2

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: G. TURNER	DATE 3 DEC 78	APPROVED BY D WALSH	
USED ON ASSEMBLY SLC 11739A		DRAWING REV 2	
ASSEMBLY NO SLC11725A		SHT 2 OF 3	

TITLE: P.C.B. ASSEMBLY
SERIES L - 100V
12 BDSI SIMULATOR
(FOR DWG SEE SHEET 1)

QTY RUN

DATE ISSUED

CONTROL

PR

W

S

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓
1	SLB11725P		1	P.C.B. BLANK				
2	90115		2	CAPACITOR 330PF	C1, C2			
3	90710		1	CAPACITOR 100PF	C3			
4	90107		2	CAPACITOR 470PF	C4, C5			
5	90087		1	CAPACITOR TANTALUM 10UF 20V	C6			
6	90119		15	CAPACITOR .01 UF	C7 TO C21			
7	90430-63		26	RESISTOR 1K 1/4W	R3 TO R24 R26 TO R28			
8	90430-87		1	RESISTOR 10K 1/4W	R2			
9	90430-94		1	RESISTOR 20K 1/4W	R1			
10	91407		5	I.C. SP220A	A5, B5, C5, D4, D5			
11	90322		1	I.C. MC836P	H1			
12	90323		2	I.C. MC859P	E5, F6			
13	90324		3	I.C. MC8001P	H2, H3, E2			
14	90331		1	I.C. MC7400P	H5			
15	90315		1	I.C. MC7402P	F4			
16	90392		1	I.C. MC7404P	F3			
17	90333		1	I.C. MC7410P	F1			
18	90390		7	I.C. MC7475P	A2, A3, B2, B3, C2, C3, D2			
19	90338		3	I.C. MC7479P	E3, F2, F5			
20	90339		1	I.C. MC7493P	H4			
21	92570		4	I.C. DM8093N	A4, F4, C4, E4			
22	90389		1	I.C. MC8602P	H6			
23	91777		1	I.C. SN7437N	D3			

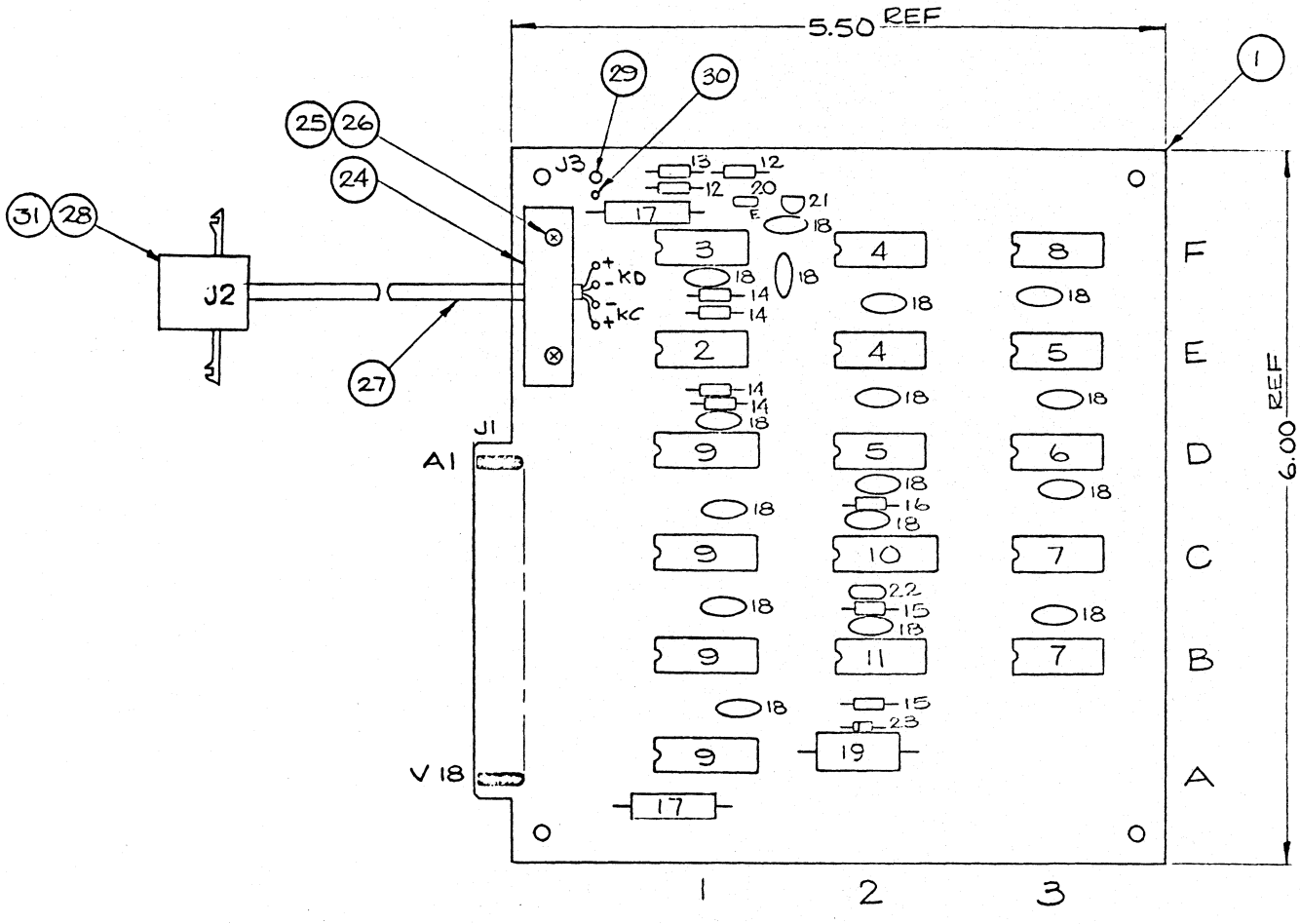
CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: G. TURNER	DATE 4 DEC 72	APPROVED BY D WALSH	QTY RUN
USED ON ASSEMBLY SLC 11739A		DRAWING REV 2	DATE ISSUED
ASSEMBLY NO SLC 11726A		SHT 3 OF 3	CONTROL

TITLE: P.C.B ASSEMBLY
SERIES L-100V
12 BDSI SIMULATOR (FOR DWG SEE SHT 1)

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90430-71		4	RESISTOR 2.2K 1/4W	R25, R29, R30, R31		
25	90077		1"	JUMPER WIRE, 24AWG-PLASTIC INS, ORN	W1, W2, W3		
REF	SLD11725L			LOGIC DIAGRAM			



FOR P/L SEE SHTS 2 & 3

no	description	date	by	chk	apprvd
7	REVISED ITEMS 17, 20, 21. ADDED ITEMS 7 & 19	20FEB73	GY	GB	DJW
	EXTENSIVE TRACK CHANGE	22JAN73	MJ		
	PRE PRO REL	21DEC72	MJ		

used on: SLC11733A
drawn: MJ
scale: 1:1
date: 13DEC72
design: D WALSH
checked:
final approval:
material:
finish:

unless specified
00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

title: PCB ASSEMBLY S/P CONVERTOR SERIES L-100 V

sheet 1 of 3 no. SLC11724A

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
MJ	8 DEC 72	D WALSH

TITLE: PCB ASSEMBLY S/P CONVERTOR SERIES L-100V FOR DWG SEE SHT 1

USED ON ASSEMBLY	DRAWING REV
SLC11739A	3
ASSEMBLY NO SLB11724A	SHT 2 OF 3

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLB11724P		1	PCB BLANK			
2	92705		1	IC SN75107AN	E1		
3	92704		1	IC SN75110N	F1		
4	90338		2	IC MC 7479P	E2, F2		
5	90331		2	IC MC 7400P	D2, E3		
6	90392		1	IC MC 7404P	D3		
7	90324		2	IC MC 3001P	C3, B3		
8	90339		1	IC MC 7493P	F3		
9	90391		4	IC MC 8300P	A1, B1, C1, D1		
10	90389		1	IC MC 8602P	C2		
11	91407		1	IC SP 380A	B2		
12	90480-71		2	RESISTOR, 2.2K 1/4 W	R2, R7		
13	90480-70		1	RESISTOR, 2.0K 1/4 W	R1		
14	90480-31		4	RESISTOR, 62Ω 1/4 W	R3-R6		
15	90480-81		2	RESISTOR, 10K 1/4 W	R9, R10		
16	90480-8=		1	RESISTOR, 6.8K 1/4 W	R8		
17	90087		2	CAPACITOR, 10 uf 20V TANTALUM	C1, C5		
18	90119		16	CAPACITOR, .01uf 50V	C2, C6-C20		
19	90103		1	CAPACITOR, 22 uf 35V TANTALUM	C4		
20	92365		1	TRANSISTOR, MJE 520	Q1		
21	90598		1	TRANSISTOR, MPS 3702	Q2		
22	90116		1	CAPACITOR, 47pf 100V	C3		
23	92003		1	DIODE IN914	CR1		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: MJ | DATE 5 DEC 72 | APPROVED BY D WALSH

USED ON ASSEMBLY SLC1173 DA | DRAWING REV 3

ASSEMBLY NO SLB1172-1A | SHT 3 OF 3

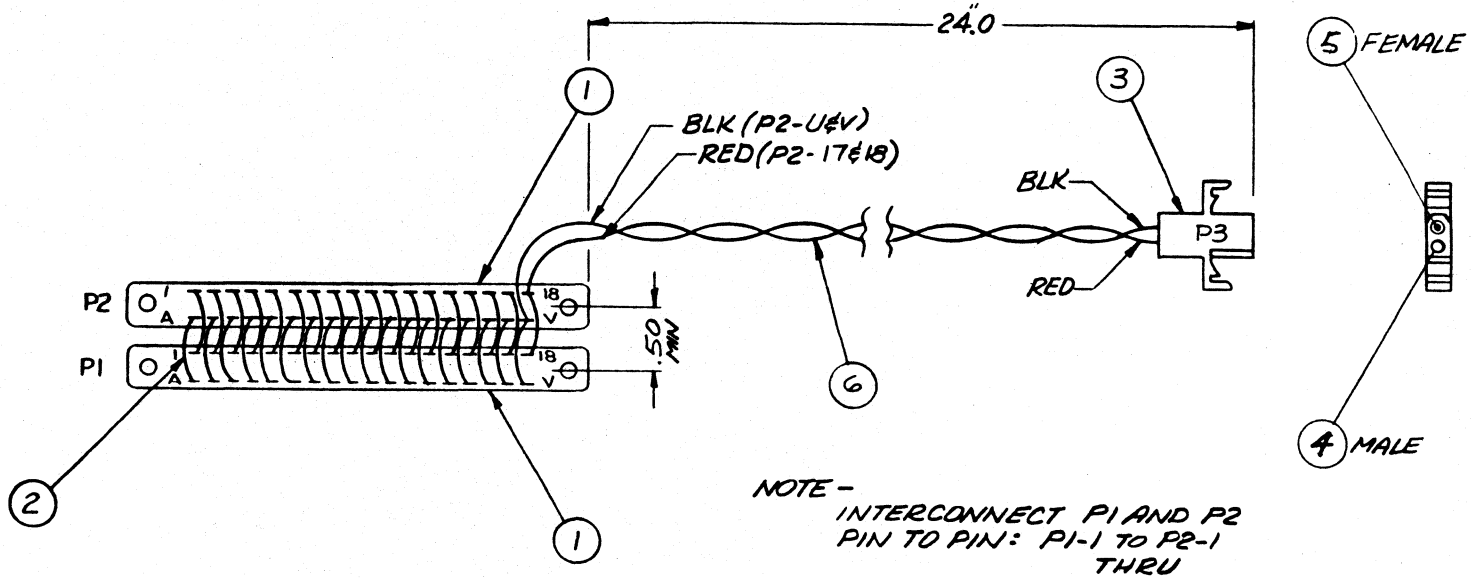
TITLE: PCB ASSEMBLY
S/P CONVERTOR
SERIES L 100V

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	B11343M		1	CABLE CLAMP			
25	90013-13		2	SCREW, 4-40UNC x 3/8 LG PPH			
26	90767		2	KEPNUT, 4-40			
27	92999		8"	CORD, 2pr 22AWG STRANDED	BELDEN 8723		
28	92892		1	CONNECTOR, RECEPTACLE, (MOLEX)	J2(1625-4R, 03-061041)		
29	92734		1	CONNECTOR PIN (FEMALE)	BEAD ELECT M93-10		
30	92733		1	CONNECTOR PIN (MALE)	BEAD ELECT R62-3		
31	92893		4	CONNECTOR PIN (HALE)	MOLEX 1625-1530		
REF	SLD11724L			LOGIC			



NOTE –
INTERCONNECT P1 AND P2
PIN TO PIN: P1-1 TO P2-1
THRU
P1-V TO P2-V

FOR PARTS LIST SEE SHEET 2

rev	eco	description	date	by	chk	apprvd
2	S1034	CABLE ADDED	2 FEB 73	GT	WB	DJW
1		PREPRODUCTION RELEASE	20 DEC 72	GT		

used on: SLC 11739A
drawn: G. TURNER
scale: 1/1
date: 20 DEC 1972
design ENG: D WALSH
checked:
final apprvl:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material:
finish:

CONSOLIDATED COMPUTER INC.
OTTAWA

title: ASSEMBLY SERIES L-100V L150 ADAPTER INTERCONNECT
sheet 1 of 2
no. SLB11729A
rev 2

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

QTY RUN

COMPILED BY: G. TURNER | DATE 20 DEC 72 | APPROVED BY D WALSH

TITLE: ASSEMBLY (FOR DWG SEE SHT 1)
SERIES L - 100V
L150 ADAPTER INTERCONNECT

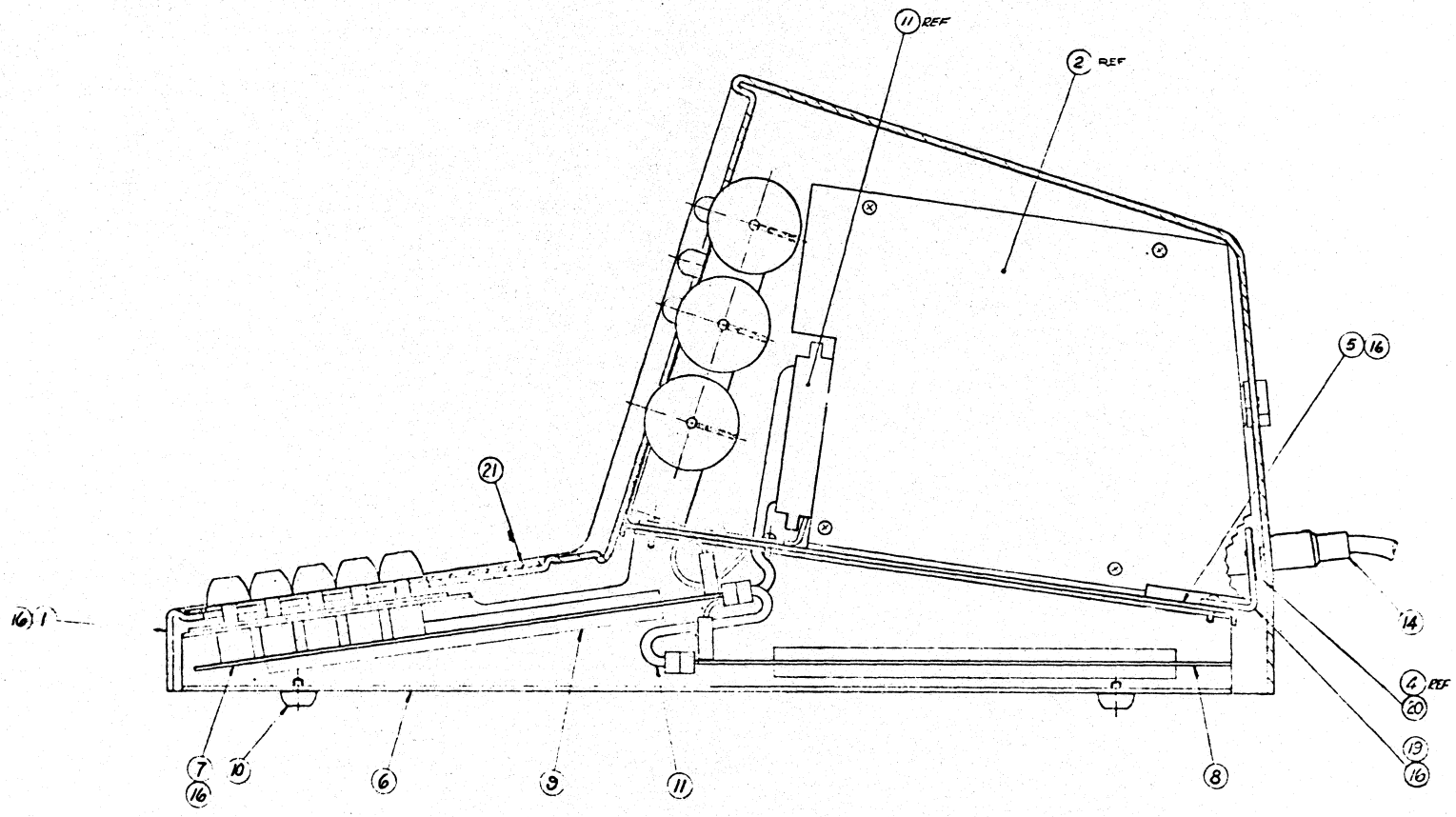
DATE ISSUED

USED ON ASSEMBLY SLC 11739A | DRAWING REV 2

ASSEMBLY NO SLB11729A | SHT 2 OF 2

CONTROL

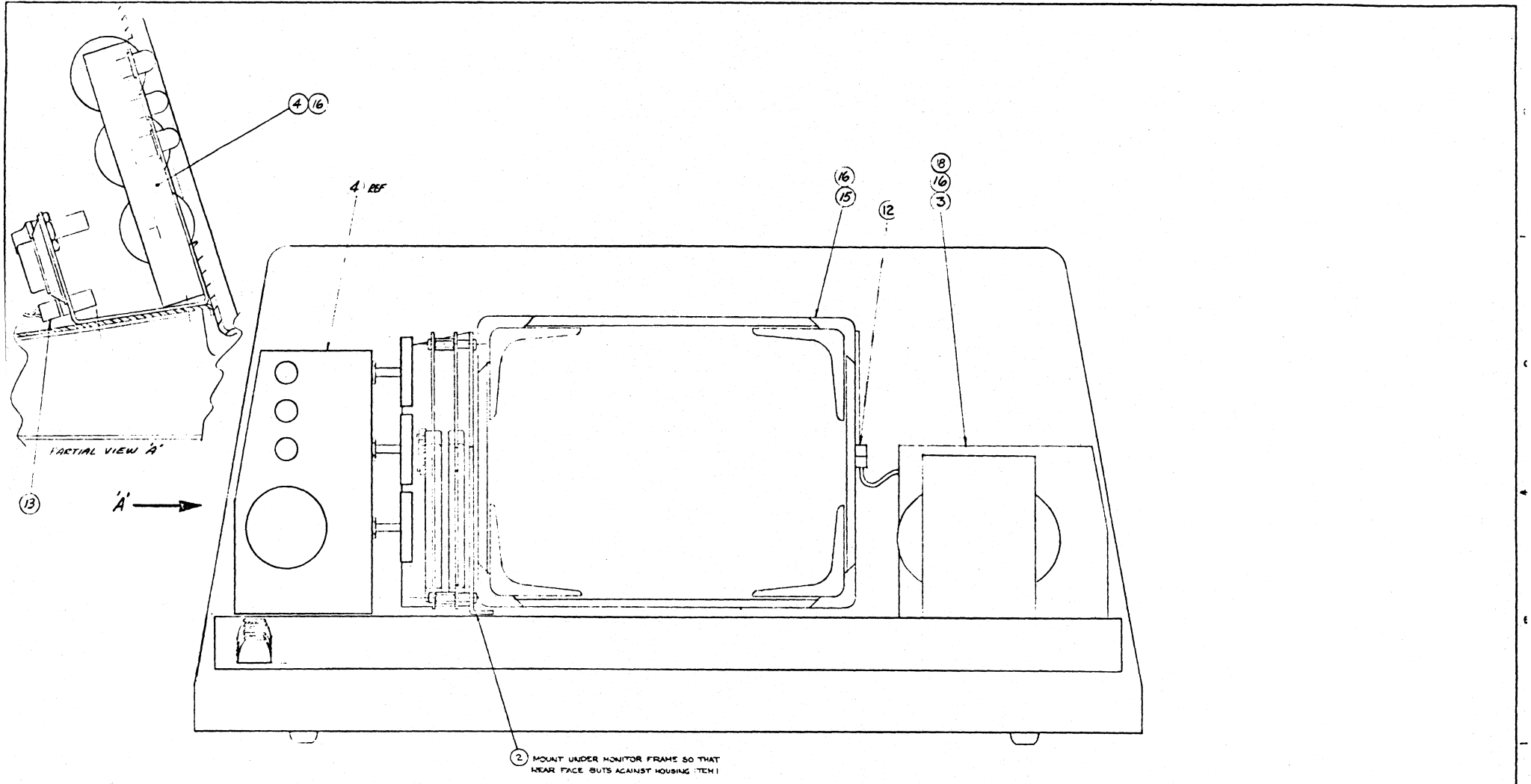
ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	90153		2	CONNECTOR, RECEPTACAL, 18/36 PIN	ELCO 6007-036-450-012		
2	90606-0		36.0 IN	WIRE 22 AWG BLK			
2 3	93181		1	CONNECTOR, RECEPTACLE	MOLEX 1625-2-03-06-1023		
4	92893		1	CONTACT, CONNECTOR, MALE	MOLEX 1625-1560		
5	92894		1	CONTACT, CONNECTOR, FEMALE	MOLEX 1625-1561		
2 6	30624-0-2		24 IN	WIRE, TWISTED PAIR, 18 AWG RED/BLK			
REF	SLB11755I			} DIAGRAM CABLE CONNECTION 100V			
REF	SLB11817I			} PHASE I			



FOR PARTS LIST SEE SHEET 2

DATA TERMINAL ASSY

1141 7A



FOR PARTS LIST SEE SHEET 3

CONSOLIDATED COMPUTER INC. OTTAWA

DATA TERMINAL ASS'Y

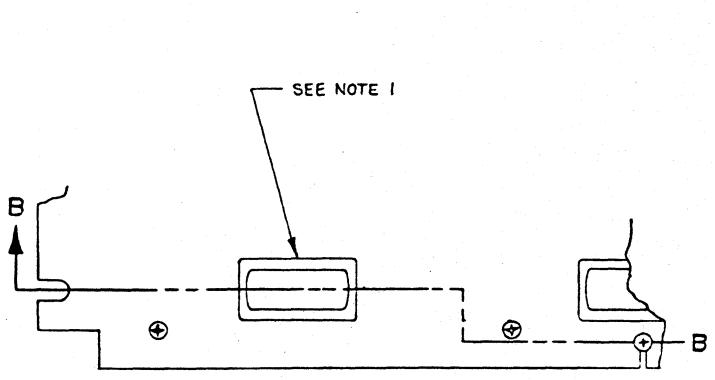
CONSOLIDATED COMPUTER INCORPORATED

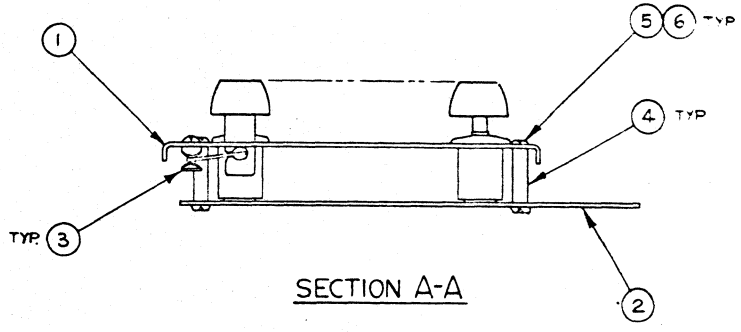
ASSEMBLY PARTS LIST

COMPILED BY:	DATE 17 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY		DRAWING REV 2	DATE ISSUED
ASSEMBLY NO SLD11317A		SHT 3 OF 3	CONTROL

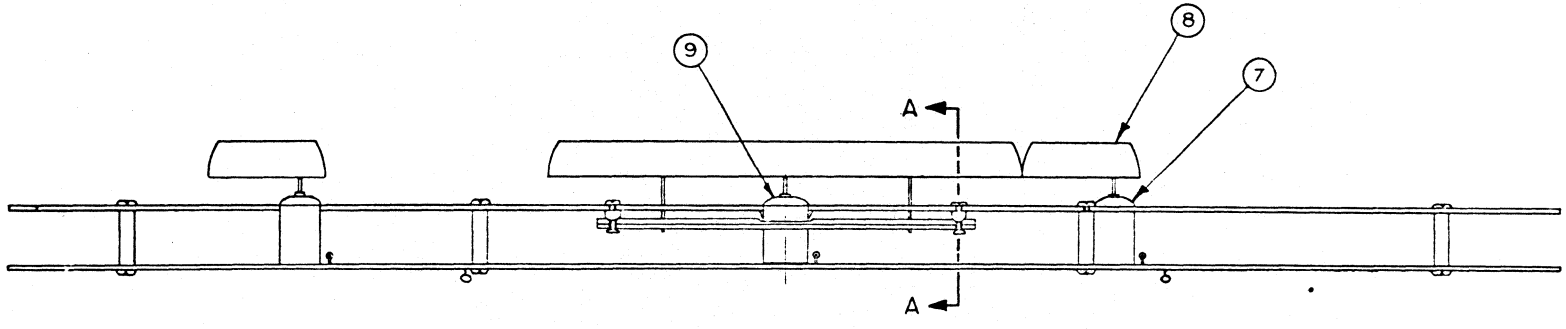
TITLE: DATA TERMINAL ASSY (BALL TYPE) SERIES L - PHASE I FOR DWG SEE SHT 1 & 2

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLB 11566MA		1	HOUSING			
2	SLB11570M		1	L 150 ADAPTER			
3	SKD11577A		1	POWER SUPPLY			
4	SKD11570A		1	SWITCH MTG BRACKET SUB ASSY			
5	SLB11569M		1	MOUNTING BASE			
6	SLB 11568MA		1	BASE			
7	SKB11822A		1	KEYBOARD ASSY	REF SLB11822X		
8	SKD11585A		1	P.C.B. ASSY VDU CONTROLLER			
9	SLB11571		4	CARD GUIDE			
10	PB-19		4	RUBBER FOOT	SPAE-NAUB #RB51		
11	SKB11632A		1	CABLE ASSY DATA INTERCONNECT			
12	SKB11633A		1	CABLE ASSY POWER D.C.			
13	SKB11634A		1	CABLE ASSY VIDEO CONTROL			
14	32001		1	P.W.R. CORD 250V	MOLDED		
15	12"-10		1	MONITOR 9" SCREEN 10" SLOPE	BALL B.C.O.S.		
16	30043-5		1	SCREW PPH 8-32 x 5/16 LG			
17							
18	SLB11727A		1	CABLE ASSY PWR SUP TO T/T CONVERTER			
19	SKB11633M		1	MTG. BRACKET SOCKET			
20	30043-15		2	SCREW PPH. 4-40 UNC x 3/8 LG			
21	SLD11302A		1	DRESS PANEL			
22							
REF	SKB11817I			DIAGRAM, CABLE CONNECTION			





SECTION A-A



SECTION B-B

NOTE:
1- FOR BUTTON & SWITCH CONFIGURATIONS SEE DWG SLB11822X

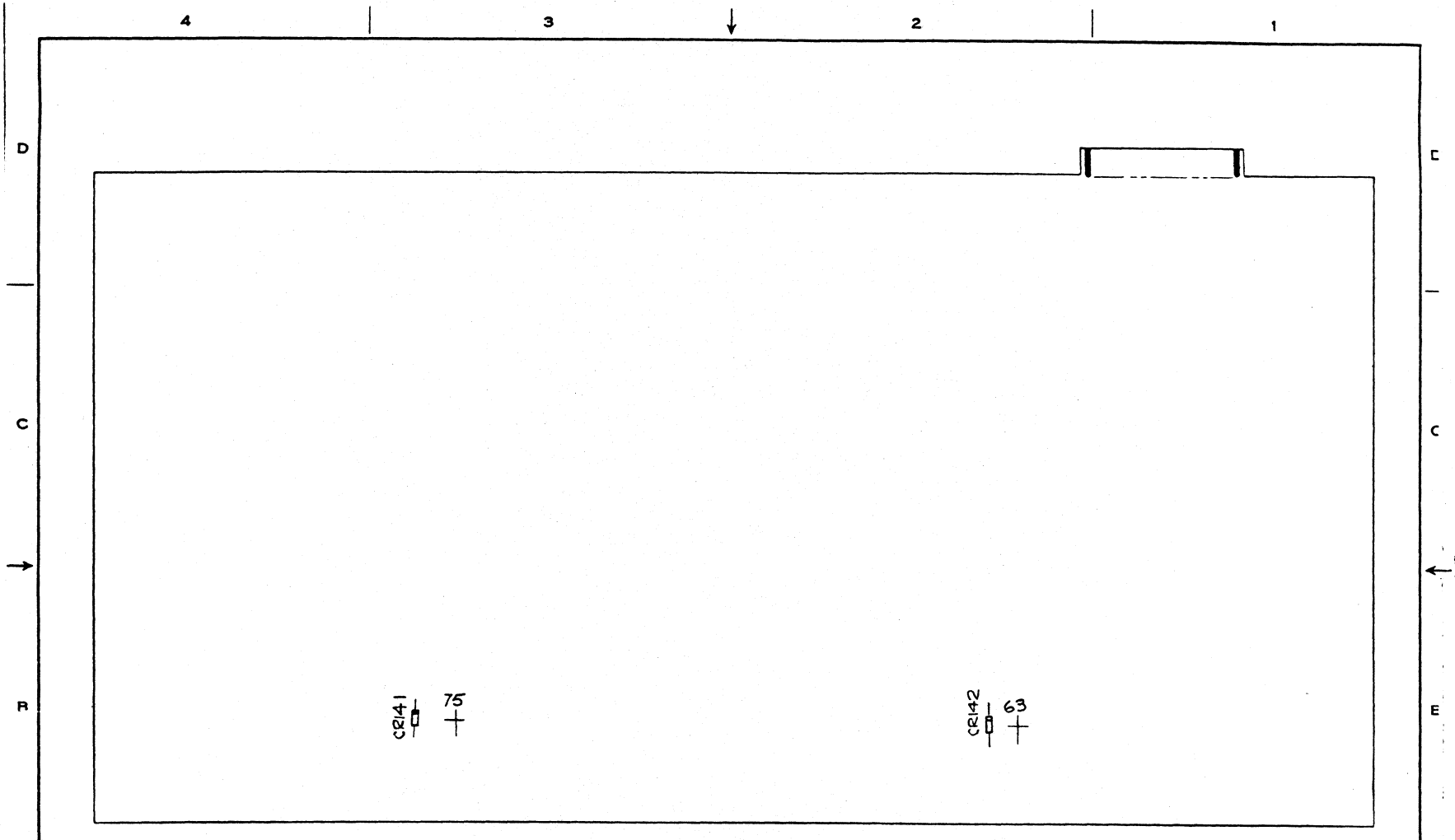
(FOR PARTS LIST SEE SHT 3)

rev	eco	description	date	by	chk	approved
2	31-035	REF DWGS CHANGED	3 FEB 73	ST	[illegible]	JW
1		PRE PROD REL	17 JAN 73	[illegible]	[illegible]	[illegible]

used on SLD11817A | drawn [illegible]
scale 1/2 | date 17 JAN 73 | to size | design spec
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ± 0 30' | checked [illegible]
tol. applic. | material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: ASSEMBLY KEYBOARD DATA TERMINAL SERIES [illegible]
sheet 1 of 3 | no. SLD11817A | rev 2



(SOLDER SIDE SHOWN)

(FOR PARTS LIST SEE SHEET 3)

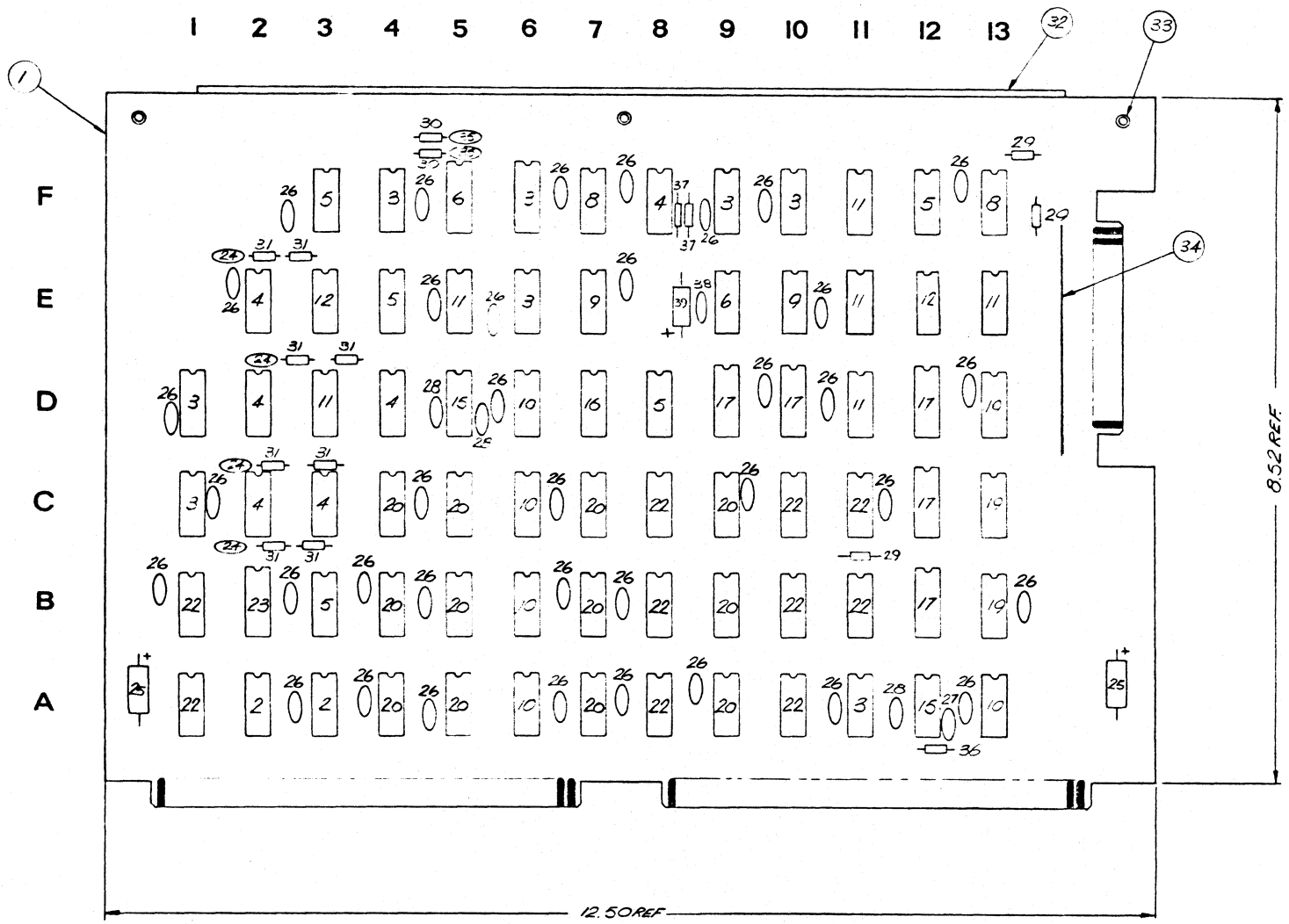
rev	eco	description	date	by	chk	approved
2		SEE SHEET 1	SEP 78	GT		DJW
1		PRE PROD REL	17 JAN 73			

used on SLD11817A | drawn | scale 1:2 | date 17 JAN 73 | design | checked | unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ±0 30' | tool material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: ASSEMBLY KEYBOARD DATA TERMINAL SERIES [illegible]

sheet [illegible] of [illegible]



rev	eco	description	date	by	chk	apprvd
2	5256	DWG UPDATE & PIL CHANGES	15 FEB 73			
1		PREPROD. RELEASE	17 JAN 73			

used on D118074, D118066A

scale 1:1 | date 17 JAN 73 | drawn | design | checked | final approval

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: PCB ASSEMBLY VCU DMA CONTROL SERIES L - PHASE I

sheet 1 of 2 | no. C 11925 A | rev

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY:	DATE 17 JAN 73	APPROVED BY D WALSH	
USED ON ASSEMBLY SLD11817A		DRAWING REV 2	
ASSEMBLY NO SLB11821A		SHT 3 OF 3	

TITLE: ASSEMBLY, KEYBOARD, DATA TERMINAL SERIES L-PHASE 1 (SEE SHT 1&2 FOR DWG)

QTY RUN	PR
DATE ISSUED	W/
	S/
CONTROL	

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓
1	SKD572M		1	MOUNTING PLATE, KEYBOARD, DATA TERMINAL				
2	SKD572-1A		1	PCB ASSY, KEYBOARD, DATA TERMINAL				
3	92744		1	SPACE BAR MECH				
4	92743		5	SPACER TAPPED 4-40, 3/16 O.D. x 5/8 LG	SPAE-NAUR SPA-104			
5	92745		16	SCREW 4-40 x 1/4, PPH	SPAE-NAUR MS-254...			
6	92306		16	LOCKWASHER, TOOTHED, #4	SPAE-NAUR 42-SN			
7	92816		#	SWITCH, KEYBOARD, 2 1/2 OZ	CHERRY P/N 261-0100			
8	SKCS1581 I		#	BUTTONS KEYBOARD DATA TERMINAL				
9	93075		1	SWITCH, KEYBOARD, 6 oz.				
10	92003		2	DIODE IN914	CR141, CR142			
				# FOR BUTTON & SWITCH QUANTITIES & CONFIGURATIONS SEE DWG SLB 11822X				

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

RUN

COMPILED BY:	DATE	APPROVED BY
M.N.	17/Jan/73	

TITLE: SERIES L - PHASE I
PCB ASSEMBLY
VCU DMA CONTROL

DATE ISSUED

USED ON ASSEMBLY	DRAWING REV
C11834 11835A	A

ASSEMBLY NO C11835A SHT 2 OF 3

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	11836P		1	PCB BLANK			
2	91407		2	IC SP 380A	A2, A3,		
3	90338		8	IC MC 7479P	A11,C1,D1,E6,E4,F9,F10	F6	
4	90315		6	IC MC 7402P	C2,C3,D2,E2, ,D4,F8		
5	90331		5	IC MC 7400P	B3,D8, E4 ,F12,F3		
6	90389		2	IC MC 8902P	F5,E9		
7							
8	92978		2	IC SN 74278N	F7,F13		
9	92501		2	IC MC 3006P	E7,E10		
10	92112		5	IC SP 384A	A13,C6,B6,A6 06		
11	90324		6	IC MC 3001P	D11,E5,C3,F11,E11,E13,		
12	92396		2	IC SP317A	E3,E12		
13							
14							
15	90322		2	IC MC 836P	A12,D5		
16	91777		1	IC SN 7437N	D7		
17	90330		5	IC MC 4015P	D9,D10,D12,C12,B12		
18							
19	90332		3	IC MC 7401P	B13,C13,D13		
20	92398		12	IC SN 74177N	A4,A5,A7,A9,B4,B5,C5, C7,C9,B7,B9,C4		
21							
22	90323		10	IC MC 858P	A1,A8,A10,B1,B8,B10 B11,C8,C10,C11,		
23	91625		1	IC MC 7442P	B2		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: M.N. | DATE 22/Nov/72 | APPROVED BY RLD

USED ON ASSEMBLY [illegible] | DRAWING REV 2

ASSEMBLY NO C1183-64 | SHT 3 OF 3

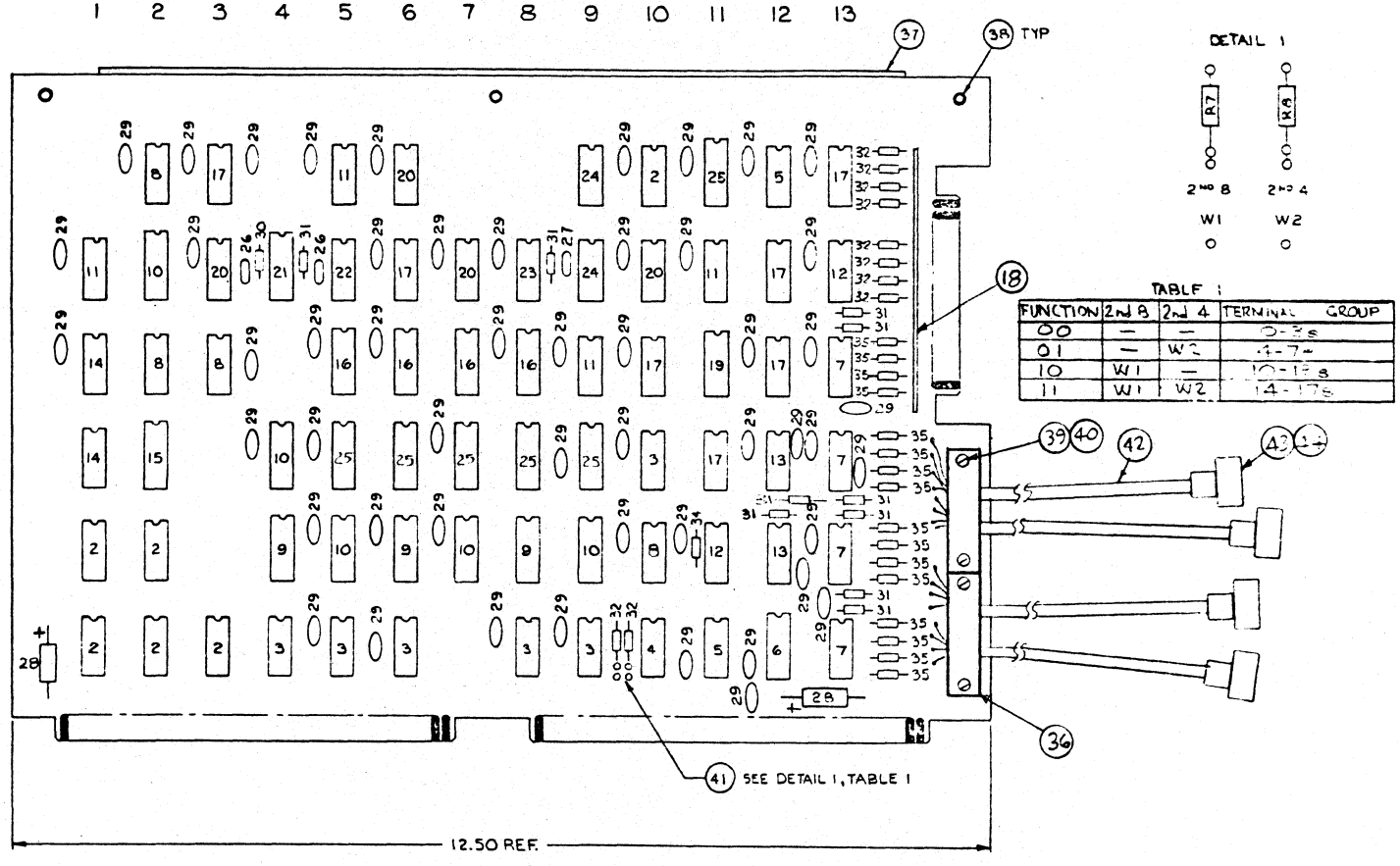
TITLE:
PCB ASSEMBLY
SERIES L - PHASE I
VCU DMA CONTROL

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90114		4	CAPACITORS 1000 pf, 100V	C7-C10		
25	90087		2	CAPACITORS 10 uf, 20V, TANTALUM	C11, C47		
26	90119		37	CAPACITORS .01 uf	C12-C46, C48, C49		
27	90113		1	CAPACITOR 68 pf 100V	C5		
28	90710		3	CAPACIOTRS 100 pf, 100V	C3, C4, C6		
29	90480-65		3	RESISTORS 1.2 K, 1/4 W.	R15, R13, R14		
30	90480-99		2	RESITORS 33 K 1/4 W.	R2, R3		
31	90480-55		8	RESISTORS 470 Ω 1/4 W.	R4-R11		
32	C1172311		1	STIFFENING BAR			
33	91837		3	Rivet, Dome Head 1/8" x3/8 LG			
34	92393		1	PCE POWER DIST. BUS BAR			
35	92388		2	CAPACITORS .05μF	C1, C2		
36	90480-47		1	RESISTOR 220Ω 1/4W	R12		
37	90480-87		2	RESISTOR, 10K, 1/4W	R16, R17		
38	90116		1	CAPACITOR, 47pf, 100V	C47		
39	91656		1	CAPACITOR, 1uf, 35V, TANTALUM	C50		



FOR PARTS LIST SEE SHEETS 2 AND 3

rev	eng	description	date	by	chk	approved
2	CS	DWG & P/L UPDATE	7MAR73	DJ		DJW
1		PRE-PROD RELEASE	16 JAN 73	DJ		

used on: SLD118066A, SLD118074 | drawn: DJ
scale: 1:1 | date: 16 JAN 73 | design eng: DJW
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ±0 30' | checked:

CONSOLIDATED COMPUTER INC. OTTAWA

title: SERIES L-PHASE 1 VCU TERMINAL CONTROL

sheet 1 of 4

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

PILED BY: J	DATE 16 JAN 73	APPROVED BY D WALSH	
D ON ASSEMBLY 11806A, SLD11807A		DRAWING REV 2	
EMBLY NO SLC 11835A		SHT 2 OF 4	

TITLE: SERIES L - PHASE 1

VCU TERMINAL CONTROL

for assy see sht 1

QTY RUN	PROJECT
DATE ISSUED	W/O
	S/O

CONTROL STOR

ITEM	PART NO.	REV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓	ISS
	SLC11835P		1	PCB Blank					
	90323		6	IC MC 858P	A1,A2,A3,B1,B2,F10				
	92112		6	IC SP 384A	A4,A5,A6,A8,A9,C10				
	91294		1	IC MC 3021P	A10				
	92978		2	IC SN 74278N	A11,F12				
	92096		1	IC U7B 93225P	A12,				
	92704		4	IC SN 75110N	A13,B13,C13,D13				
	90315		4	IC MC 7402P	B10,D2,F2,D3				
	90330		3	IC MC 4015P	B4,B8,B6				
	92836		5	IC SN 74174N	B5,B7,B9,C4,E2				
	90331		4	IC MC 7400P	,D9, ,E1,E11,F5				
	90332		2	IC MC 7401P	B11,E13				
	92705		2	IC SN 75107AN	B12,C12				
	91407		2	IC SP 380A	C1,D1				
	91625		1	IC MC 7442P	C2				
	90391		4	IC MC 8800P	D7,D8,D5,D6				
	90392		7	IC MC 7404P	C11,D12,E6,E12,F3,F13	D10			
	92393		1	PCB POWER DIST BUS BAR					
	930-92		1	IC U7B 9321	D11				
	D1804		4	IC SN 7474N	E3,E7,E10,F6				
	90389		1	IC MC 8602P	E4				
	90339		1	IC MC 7493P	E5				

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

MPILED BY: D J	DATE 16 JAN 73	APPROVED BY D WALSH	QTY RUN
D ON ASSEMBLY SLD11806A, SLD11807A		DRAWING REV 2	DATE ISSUED
EMBLY NO. SLC 11835A		SHT 3 OF 4	

TITLE:

SERIES L - PHASE I

VCU TERMINAL CONTROL

for assy see sht 1

PROJECT

W/O

S/O

CONTROL

STOP

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓	ISS
3	91376		1	IC MC 6601P	E8				
4	90324		2	IC MC 3001P	E9, F9				
5	93093		6	IC MC 8309P	F11 C5 C6 C7 C8 C9				
6	90114		2	CAPACITORS 1000 pf, 100V	C1, C2				
7	90116		1	CAPACITORS 47 pf, 100V	C3				
8	90087		2	CAPACITORS 10uf 20V, TANTALUM	C4, C57				
9	90119		51	CAPACITORS .01uf 50V	C5-C55				
0	90480-94		1	RESISTORS 20K 1/4W	R1				
1	90480-87		10	RESISTORS 10K 1/4W	R2-R4 R6, R33-R38				
2	90480-71		10	RESISTORS 2.2K 1/4W	R7-R16				
3									
4	90480-65		1	RESISTORS 1.2K 1/4W	R5				
5	90480-34		16	RESISTORS 62 Ω	R17-R32				
6	B11343M		2	CABLE CLAMP					
7	SLC 11723M		1	STIFFENING BAR					
8	91837		3	RIVET, DOME HEAD 1/8 x 3/8 LG					
9	90043-13		4	MACHINE SCREW, 4-40 x 3/8	PAN HEAD				
0	90767		4	KEPNUT, 4-40					
1	90077		2	WIRE, SOLID, 24 AWG 3/4	W1, W2				
2	92999		4	CORD 2Pr 22 AWG STRANDED 2'-6" LONG					
3	92892		4	CONNECTOR PLUG HOUSING	MOLEX 1625-40306104				
4	92893		16	CONNECTOR PIN (MALE)	MOLEX 1625-1560				

CONSOLIDAT COMPUTER INCORPORATED

ASSEMBL PARTS LIST

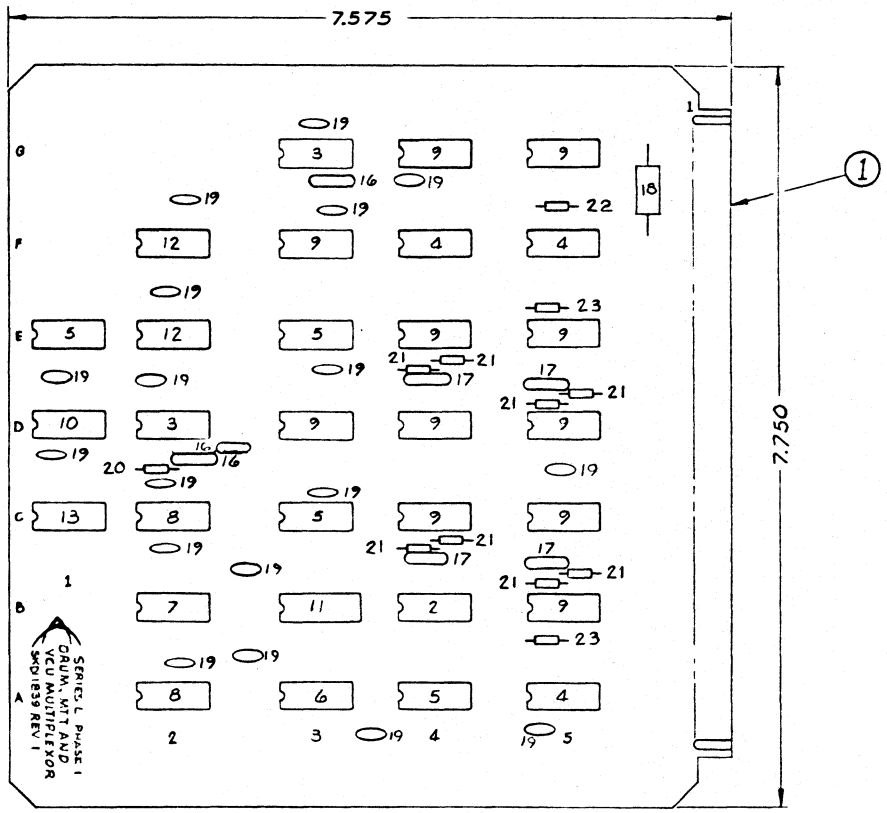
QTY RUN

PROJECT

PILED BY:	DATE 16-JAN-72	APPROVED BY D WALSH	W/O
D ON ASSEMBLY LD11806A, SLD11807A		DRAWING REV 2	DATE ISSUED / S/O
EMBLY NO SLC 11835A		SHT 4 OF 4	

TITLE:
SERIES L-PHASE I
VCU TERMINAL CONTROL
FOR ASSY SEE SHT 1

EM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	CONTROL QTY. REQ.	CONTROL AVAIL	✓	STOR ISS
EF	SLC11835L			LOGIC					
EF	SLC11721M			OUTLINE DWG					



FOR PARTS LIST SEE SHTS 2 AND 3

rev	eco	description	date	by	chk	apprvd
1		PRE-PROD RELEASE	17 JAN 73	DJ		

SLD11807A
used on SLD11806A
scale 1:1
date 17 JAN 73
drawn DJ
design
checked
final apprvl
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material
finish

CONSOLIDATED COMPUTER INC.
OTTAWA

PCB ASSEMBLY
DRUM, MTT AND
VCIU MULTIPLEXOR
title SERIES L PHASE I
sheet 1 of 3
no. SLD11806A
rev 1

SOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

QTY RUN

COMPILED BY:	DATE	APPROVED BY
DJ	17 JAN 73	D WALSH

TITLE: PCB ASSEMBLY
DRUM, MTT AND VCU MULTIPLEXOR
SERIES L-PHASE 1 FOR ASSY SEE SHT 1

DATE ISSUED

USED ON ASSEMBLY	DRAWING REV
SLD11807A, SLD11806A	1

ASSEMBLY NO. SLC11839A SHT 2 OF 3

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	11730P		1	PCB BLANK			
2	91407		1	SP380A	B4		
3	90322		2	MC836P	D2, G3		
4	90323		3	MC858P	A5, F4, F5		
5	90331		4	MC7400P	A4, C3, E1, E3		
6	90392		1	MC7404P	A3		
7	90333		1	MC7410P	B2		
8	90335		2	MC7430P	A2, C2		
9	91777		11	SN7437N	B5, C4, C5, D3, D4, D5, E4, E5, F3, G4, G5		
10	90316		1	MC7440P	D1		
11	91625		1	MC7442P	B3		
12	90338		2	MC7479P	E2 F2		
13	92978		1	SN74278	C1		
14	———	———	———	———			
15	———	———	———	———			
16	90710		3	CAPACITOR 100 PF DURA MICA	C_1, C_2, C_3		
17	90114		4	CAPACITOR 1000PF DURA MICA	C_4, C_5, C_6, C_7		
18	90087		1	CAPACITOR 10UF 20V	C_8		
19	90119		19	CAPACITOR .01UF 50V	$C_9 - C_{29}$		
20	9048060		1	RESISTOR 750Ω 1/4W 5%	R_1		
21	9048055		8	RESISTOR 470Ω 1/4W 5%	$R_2 - R_5, R_8 - R_{11}$		
22	9048051		1	RESISTOR 330Ω 1/4W 5%	R_6		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: DJ | DATE: 17 JAN 73 | APPROVED BY: D WALSH

USED ON ASSEMBLY: SLD11807A, SLD11806A | DRAWING REV:

ASSEMBLY NO. SLC11839A | SHT 3 OF 3

TITLE: PCB ASSEMBLY
DRUM, MTT AND VCU MULTIPLEXOR
SERIES L-PHASE I

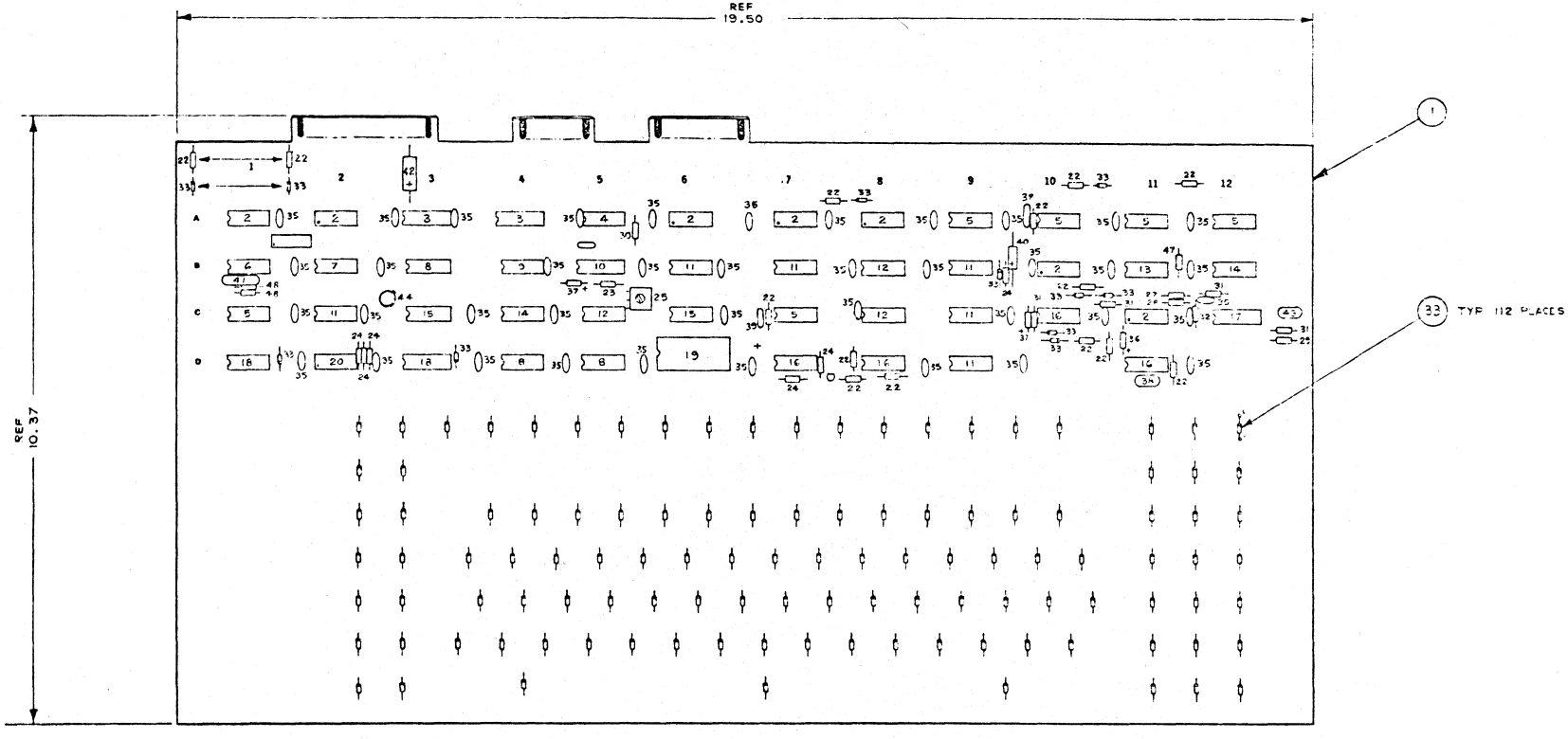
FOR ASSY SEE SHT 1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
23	9048071		2	RESISTOR 2.2K 1/4W 5%	R_7, R_{12}		
REF	CS10088M	D		BOARD OUTLINE			
REF	SLD11839L	1		LOGIC			



(FOR PARTS LIST SEE SHEETS 2 & 3)

CONSOLIDATED COMPUTER INC. OTTAWA

PCB ASSEMBLY
KEYBOARD
DATA TERMINAL

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC | DATE: 5 JAN 1973 | APPROVED BY: J.R. J.C. Gaffney

USED ON ASSEMBLY | DRAWING REV: A

ASSEMBLY NO: SKD11840A | SHT 2 OF 4

TITLE: PCB ASSEMBLY, KEYBOARD, DATA TERMINAL (FOR DWG SEE SHT 1)

QTY RUN | DATE ISSUED | CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓
1	SKD11840P		1	PCB, BLANK				
2	92570		7	I.C., DM8093N	A1, A2, A6-A8, B10, C11			
3	90590		2	I.C., MC7475P	A4, A3			
4	91786		1	I.C., MC74150	A5			
5	91407		6	I.C., SP380A	A9 -A12, C7, C1			
6	90322		1	I.C., MC836P	B1			
7	90392		1	I.C., MC7404P	B2			
8	90339		3	I.C., MC7493P	B3, D4, D5			
9	92501		1	I.C., MC3006P	B4			
10	90389		1	I.C., MC9602P	B5			
11	91804		6	I.C., SN7474N	B6, B7, B9, C2, C9, D9			
12	90331		3	I.C., MC7400P	B8, C5, C8			
13	90315		1	I.C., MC7402P	B11			
14	90333		2	I.C., MC7410P	B12, C4			
15	90341		2	I.C., MC846P	C3, C6			
16	90323		4	I.C., MC858P	C10, D8, D11, D7			
17	92571		1	I.C., CD4009	C12			
18	92226		2	I.C., MC8312P	D1, D3			
19	92401		1	I.C., MC8311P	D6			
20	92339		1	RESISTOR PACK, THICK FILM, 10K	D2 (EPITEK)			
21	92338		1	RESISTOR PACK, THICK FILM, 1K	A1/B2 (EPITEK)			
22	90480-63		30	RESISTOR, 1K, 1/4W	R47, R48, R9, R11, R12, R20, R21, R25-R45, R , R			
23	90480-93		1	RESISTOR, 30K, 1/4W	R7			

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC	DATE 5 JAN 1973	APPROVED BY [signature]	QTY RUN
USED ON ASSEMBLY		DRAWING REV A	DATE ISSUED
ASSEMBLY NO SKD11840A		SHT 3 OF 4	CONTROL

TITLE: PCB ASSEMBLY, KEYBOARD, DATA TERMINAL (FOR DWG SEE SHEET 1)

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90480-87		6	RESISTOR, 10K, 1/4 W	R3, R4, R5, R13, R , R		
25	92740		1	RESISTOR, VARIABLE, 20K, 1/2 W	R8		
26							
27	90480-111		1	RESISTOR, 100K, 1/4 W	R16		
28	90480-103		1	RESISTOR, 47K, 1/4 W	R17		
29	90480-125		1	RESISTOR, 390K, 1/4 W	R23		
30	90480-70		1	RESISTOR, 2K, 1/4 W	R6		
31	90480-135		4	RESISTOR, 1M, 1/4 W	R14, R15, R19, R22		
32	90480-108		1	RESISTOR, 75K, 1/4 W	R18		
33	92003		139	DIODE, IN914	CR1, CR2, CR3-CR119, CR121-CR140		
34							
35	90119		39	CAPACITOR, .01 uf, 50V	C8, C10-C48		
36	91583		1	CAPACITOR, TANTALUM, .1 uf, 35V	C51		
37	91656		2	CAPACITOR, TANTALUM, 1 uf, 35V	C3, C7		
38	90710		2	CAPACITOR, 100 pf, 100V	C2, C9		
39	90107		2	CAPACITOR, 470 pf, 100V	C4, C5		
40	90103		1	CAPACITOR, TANTALUM, 22 uf, 35V	C6		
41	92739		1	CAPACITOR, .005 uf, 100V	C1		
42	90106		1	CAPACITOR, 10 uf, 50V	C49		
43	90114		1	CAPACITOR, 1000 pf, 100V	C50		
44	92567		1	I.C., MK1002L	B2/C3		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC | DATE: 5 JAN 73 | APPROVED BY:

USED ON ASSEMBLY:

DRAWING REV: A

ASSEMBLY NO: SKD11840A | SHT 4 OF 4

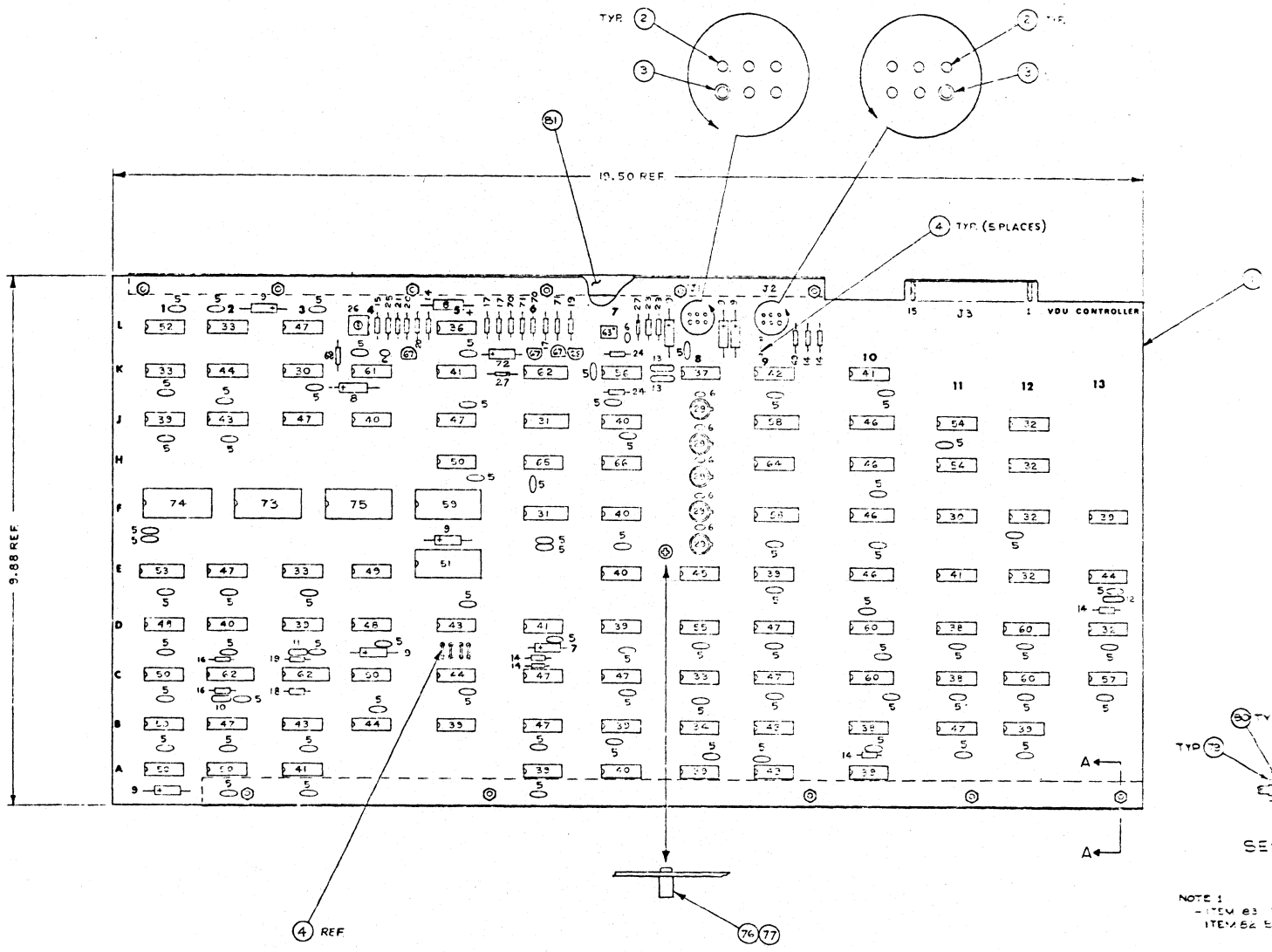
TITLE: PCB ASSEMBLY, KEYBOARD, DATA TERMINAL (FOR DWG SEE SHEET 1)

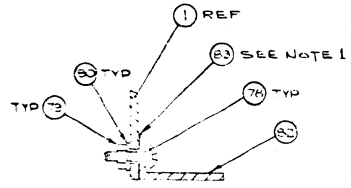
QTY RUN:

DATE ISSUED:

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓
47	90480-23		1	RESISTOR, 22Ω, 1/4W	R46			
48	90480-69		2	RESISTOR, 1.8K, 1/4W	R1, R2			
REF	SKD11840M			OUTLINE, PCB				
REF	SKD11840L			LOGIC				





SECTION A-A
SCALE 2/1

NOTE 1
- ITEM 83 TO BE ON TOP SURFACE OF ITEM 82 BETWEEN ITEM 1 AND ITEM 82

FOR PART LIST SEE SHEETS 2,3,4&5

CONSOLIDATED COMPUTER LIMITED
OTTAWA

PCB ASSEMBLY
VDU CONTROLLER

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC	DATE 8 AUG 72	APPROVED BY [illegible]	QTY RUN
USED ON ASSEMBLY		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SKD11535A		SHT 2 OF 5	CONTROL

TITLE: PCB ASSEMBLY
VDU CONTROLLER
DATA TERMINAL FOR DWG. SEE SHT.1

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SKB11535P		1	PCB BLANK			
2	92733		10	MALE CONTACT	R62-3, BEAD ELEC.		
3	92734		2	FEMALE CONTACT	M93-102, BEAD ELEC.		
4	90609-0		3.5"	WIRE, JUMPER, 28 AWG STRANDED	W1-W5		
5	90119		72	CAPACITOR .01μF 50V ±10%	C16-C19, C20-C87		
6	92500		7	.047μF 5V ±20%	C3, C7, C11-C15		
7	91583		1	.1μF 35V ±10%	C5		
8	90103		2	22μF 35V ±10%	C4, C94		
9	90106		7	10μF 50V ±5%	C88, C89, C90-C93, C95		
10	91436		1	56pF 100V ±5%	C1		
11	90710		1	100pF 100V ±5%	C2		
12	90107		1	470pF 100V ±10%	C10		
13	92737		2	CAPACITOR 3,300pF 500V ±5%	C8, C9		
14	90480-63		6	RESISTOR 1KΩ 1/4W ±5%	R7, R32, R14, R23, R24, R31.		
15	90480-80		1	5.1KΩ	R5		
16	90480-81		2	5.6KΩ	R1, R2		
17	90480-87		3	10KΩ	R11, R12, R15		
18	90480-91		1	15KΩ	R4		
19	90480-97		2	27KΩ	R3, R16		
20	92735		2	150KΩ	R9, R10		
21	92736		1	300KΩ	R8		
22							
23	90480-39		2	RESISTOR 100Ω 1/4W ±5%	R18, R19		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
RC	8 AUG 72	

USED ON ASSEMBLY

DRAWING REV 1

ASSEMBLY NO SKD11535A SHT 3 OF 5

TITLE: PCB ASSEMBLY
VDU CONTROLLER
DATA TERMINAL FOR DWG. SEE SHT. 1

QTY ..UN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90480-43		2	RESISTOR 150Ω 1/4W ±5%	R17, R20		
25	90480-55		1	RESISTOR 470Ω 1/4W ±5%	R6		
26	92732		1	RESISTOR VARIABLE, 10K	R25		
27	92003		2	DIODE IN914	CR1, CR2		
28	90597		1	TRANSISTOR MPS3704	Q4		
29	92723		5	IC ML1403	F8, FE8, FH8, HJ8, KJ8		
30	90388		2	MC1805P	F11, K3		
31	92724		2	2519 (SIGNETIC)	F6, J6		
32	91407		5	SP380A	D13, E12, F12, H12, J12		
33	90324		4	MC3001P	C8, E3, L2, K1		
34	90325		1	MC3003P	B8		
35							
36	91632		1	MC4044P	L5		
37	92728		1	IM5013	K8		
38	92726		3	MC7242P	B10, C11, D11		
39	90331		11	MC7400P	A6, A8, A10, B5, B7, B12 D3, D7, E9, F13, J1		
40	90315		6	MC7402P	A7, D2, E7, F7, J4, J7		
41	90392		5	MC7404P	A3, D6, E11, K5, K10		
42	91772		1	SN7406N	K9		
43	90333		5	MC7410P	A9, B3, B9, D5, J2		
44	90334		4	MC7420P	B4, C5, E13, K2		
45	90337		1	IC MC7451P	E8		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
RC	8 AUG 72	

USED ON ASSEMBLY | DRAWING REV 1

ASSEMBLY NO SKD11535A | SHT 4 OF 5

TITLE: PCB ASSEMBLY
VDU CONTROLLER
DATA TERMINAL FOR DWG SEE SHT. 1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
46	90390		4	IC MC7475P	E10, F10, H10, J10		
47	90338		11	MC7479P	B2, B6, B11, C6, C7, C9 D9, E2, J3, J5, L3		
48	92067		2	MC7490P	D1, D4		
49	92097		1	MC7492P	E4		
50	90339		6	MC7493P	A1, A2, B1, C1, C4, H5		
51	91781		1	SN74154N	E5		
52	91785		1	SN74164N	L1		
53	92566		1	SN74165N	E1		
54	91786		2	SN74180N	H11, J11		
55	91295		1	MC857P	D8		
56	90323		1	MC858P	K7		
57	92570		1	DM8093N	C13		
58	92727		2	8267 (SIGNETICS)	F9, J9		
59	92400		1	MC8308P	F5		
60	90349		4	MC8316P	C10, C12, D10, D12		
61	91376		1	MC8601P	K4		
62	90389		3	U7B960259	C2, C3, K6		
63	92729		1	IC MCT2 (MONSANTO)	L7		
64	92338		1	RESISTOR PACK, 1K EPITEK #1113-102K	H9		
65	92730		1	RESISTOR PACK, 3K EPITEK #1113-302K	H6		
66	92731		1	RESISTOR PACK, 4.7K EPITEK #1113-472K	H7		
67	90598		3	TRANSISTOR MPS 3702	Q1, Q2, Q3		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC | DATE: 8 AUG 72 | APPROVED BY: [signature]

USED ON ASSEMBLY:

DRAWING REV: 1

ASSEMBLY NO: SKD11535/ | SHT 5 OF 5

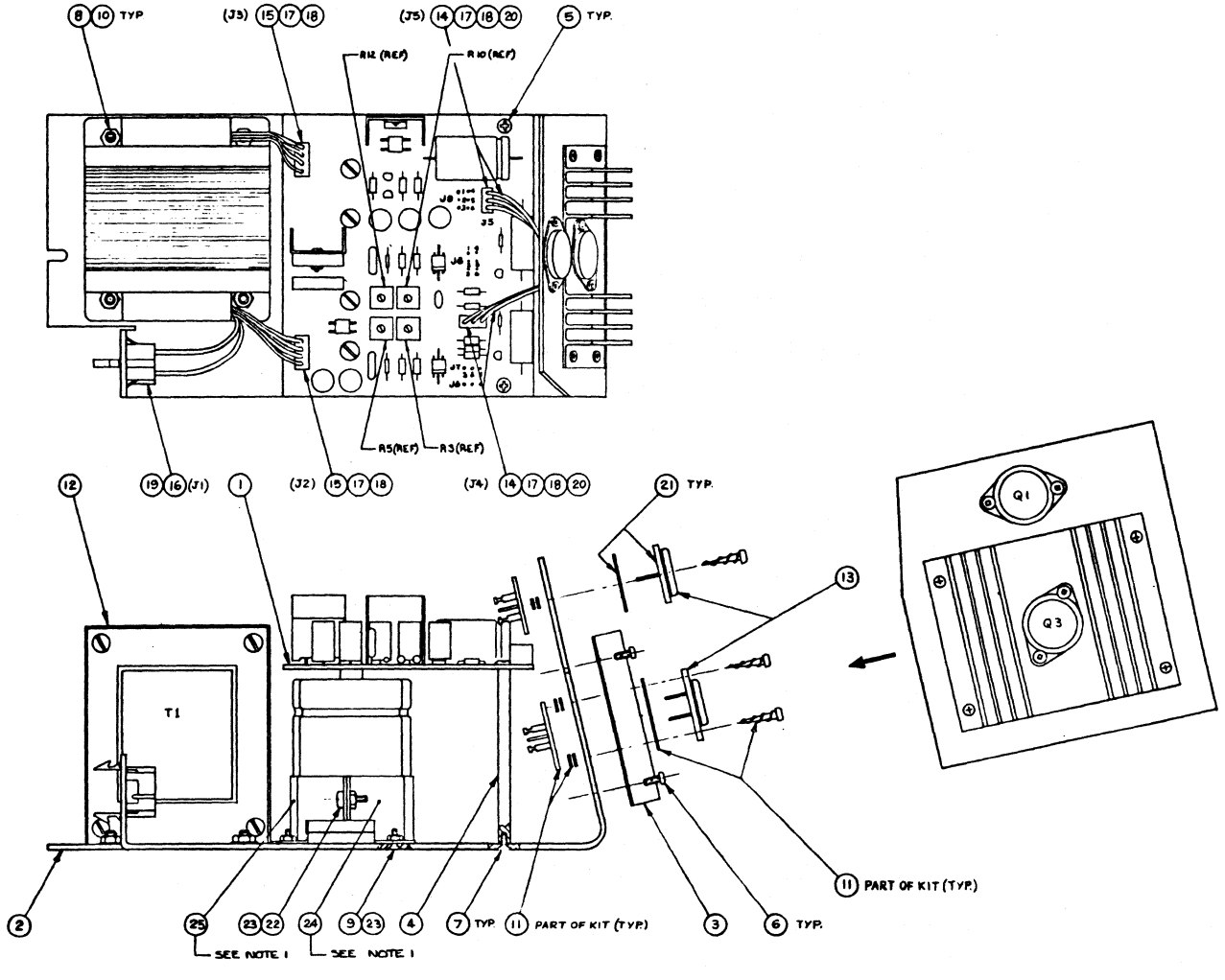
TITLE: PCB ASSEMBLY
VDU CONTROLLER
DATA TERMINAL FOR DWG. SEE SHT.1

QTY RUN:

DATE ISSUED:

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
68	90480-15		1	RESISTOR 10Ω 1/4W ±5%	R33		
69	90480-47		1	RESISTOR 220Ω 1/4W ±5%	R30		
70	90480-103		2	RESISTOR 47K 1/4W ±5%	R28, R29		
71	90480-111		2	RESISTOR 100K 1/4W ±5%	R26, R27		
72	91656		1	CAPACITOR 1μF 35V ±10%	C6		
73	92960		1	IC ROM TYPE A7C-3514-191 FAIRCHILD CCL CUSTOM # 30335	F2/3		
74	92959		1	IC ROM TYPE A7C-3514-191 FAIRCHILD CCL CUSTOM # 30336	F1		
75	92961		1	IC ROM TYPE A7C-3514-191 FAIRCHILD CCL CUSTOM # 30334	F4		
76	92971		1	SPACER 3/16 O.D. X 3/8 LG TAPPED BRASS	I.D. #4. (SPAE NAUR) SPA-63		
77	90043-12		1	SCREW 4-40 X 1/4 PH PAN HD			
REF	SKD11535L		3	LOGIC DIAGRAM			
REF	SKD11535M		1	PCB OUTLINE			



NOTES

1 - ADJUST CAPACITOR CLAMPS ITEMS 24 & 25 SO THAT PCB ASSY IS LEVEL

2 - (a) PLUG FROM Q1 GOES TO J4
(b) PLUG FROM Q3 GOES TO J5

(FOR PARTS LIST SEE SHEET 2 OF 3)

1	PRE PROPEL	14 DEC 72	JB		

SKD11565A — RC

1:1 — 3 OCT 1972

unless specified: .00 = ±.01, .000 = ±.005, fraction = 1/64, angular = ±0°30'

CONSOLIDATED COMPUTER INC. OTTAWA

ASSEMBLY
POWER SUPPLY DATA TERMINAL
(SMALL VERSION)

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

QTY RUN

COMPILED BY: RC | DATE: 30 OCT 72 | APPROVED BY: [illegible]

TITLE: ASSEMBLY
POWER SUPPLY, DATA TERMINAL
(FOR ASSY SEE SHEET 1)

DATE ISSUED

USED ON ASSEMBLY: SKD11565A | DRAWING REV: 1

ASSEMBLY NO: SKD11577A | SHT 2 OF 3

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SKC11579A		1	PCB ASSY, POWER SUPPLY			
2	SKD11578M		1	CHASSIS, POWER SUPPLY			
3	SKB11552M		1	HEATSINK (MODIFIED 92514)			
4	92916		2	STANDOFF 1/4 DIA X 3" LG 4-40 THD	AMATOM 8180-A0440		
5	90043-13		2	SCREW, PAN HD, 4-40 X 3/8 LG			
6	90043-12		4	SCREW, PAN HD. 4-40 X 1/4 LG			
7	90040-12		2	SCREW, FLAT HD, 4-40 X 1/4 LG			
8	90040-46		4	SCREW, FLAT HD. 10-32 X 3/8 LG			
9	90040-24		6	SCREW, FLAT HD. 6-32 X 3/8 LG			
10	91301		4	KEPNUT 10-32			
11	92531		2	MOUNTING KIT, TRANSISTOR			
12	92981		1	TRANSFORMER (HAMMOND)	102840		
13	92827		2	TRANSISTOR MJ3000			
14	92917		2	CONNECTOR (3 CONTACT)	MOLEX 1625-3R		
15	92892		2	CONNECTOR (4 CONTACT)	MOLEX 1625-4R		
16	92798		1	SOCKET HOUSING (9 CONTACT)	MATE-N-LOK 1-480274-0		
17	92893		6	CONTACT MALE	MOLEX 1560		
18	92894		8	CONTACT FEMALE	MOLEX 1561		
19	92922		7	CONTACT SOCKET	MATE-N-LOCK 61314-1		
20	90604-0		18"	WIRE STRANDED 18 AWG, BLACK			
21	90890		1/R	THERMAL COMPOUND			
22	90043-24			SCREW, PAN HD. 6-32 X 3/8 LG			
23	91202		8	KEPNUT 6-32			

C OLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

Y RUN

COMPILED BY:	DATE	APPROVED BY
RC	3 OCT 72	[illegible]

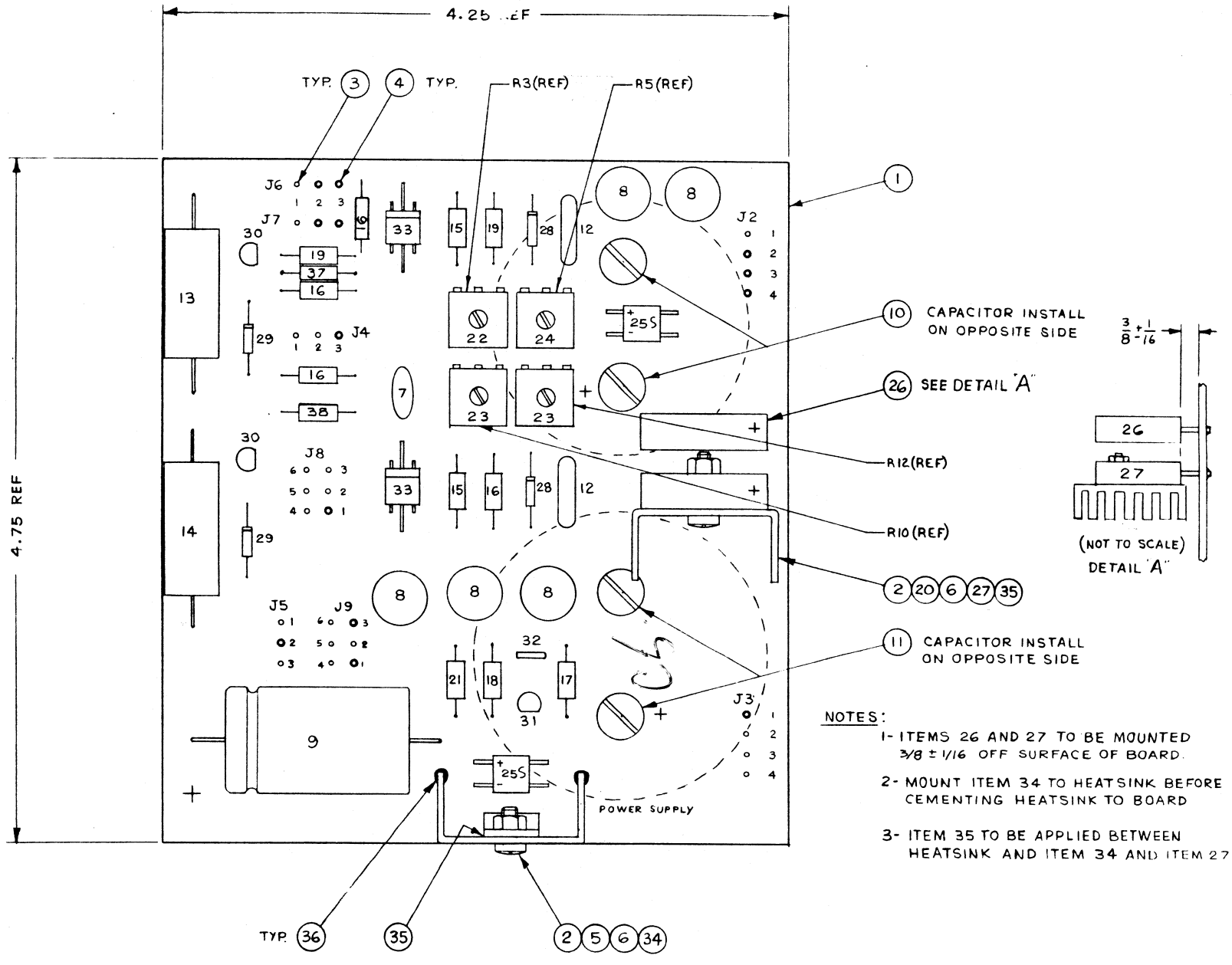
TITLE: ASSEMBLY
POWER SUPPLY, DATA TERMINAL
(FOR ASSY SEE SHEET 1)

DATE ISSUED

USED ON ASSEMBLY	DRAWING REV
SKD11565A	1

ASSEMBLY NO SKD11577A SHT 3 OF 3

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	CONTROL QTY. REQ.	CONTROL AVAIL
24	92956		1	CLAMP, MOUNTING CAPACITOR	MALLORY VR6		
25	91836		1	CLAMP, MOUNTING CAPACITOR	MALLORY VR8		
REF	SKD11577S		1	SCHEMATIC DWG			
REF	SKA11577W		1	WIRING LIST			



NOTES:

1- ITEMS 26 AND 27 TO BE MOUNTED 3/8 ± 1/16 OFF SURFACE OF BOARD.

2- MOUNT ITEM 34 TO HEATSINK BEFORE CEMENTING HEATSINK TO BOARD

3- ITEM 35 TO BE APPLIED BETWEEN HEATSINK AND ITEM 34 AND ITEM 27

(FOR PARTS LIST SEE SHEETS 2 & 3)

key	eco	description	date	by	chk	apprvd
1	SK008	PRE PROD REL	30 OCT 72	EC	RAP	[illegible]

used on: SKD11577A | drawn: RC | scale: 2:1 | date: 30 OCT 72 | design ENG | checked: RAP | final apprvl | material | finish

unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: PCB ASSEMBLY - POWER SUPPLY DATA TERMINAL

sheet 1 of 3 | no. SKD11579A | rev 1

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: R.C.	DATE 3 OCT 72	APPROVED BY WBSS	QTY RUN
USED ON ASSEMBLY SKD11577A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SKC11579A		SHT 2 OF 3	CONTROL

TITLE: PCB ASSEMBLY
POWER SUPPLY, DATA TERMINAL
(FOR DRWG SEE SHEET 1)

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SKC11579P		1	PCB BLANK			
2	92519		2	HEATSINK	THERMALLOY INC. 6106B-14		
3	92733		19	MALE CONTACT	R62-3, BEAD ELEC.		
4	92734		13	FEMALE CONTACT	M93-102, BEAD ELEC		
5	90043-12		1	SCREW, PAN HD, 4-40 UNC X 1/4 LG			
6	90767		2	KEPNUT 4-40 UNC			
7	90119		1	CAPACITOR .01μF 50V ±10%	C6		
8	92875		5	100 μF, 25V	C1, C4, C8, C10, C11		
9	90099		1	1,000 μF, 25V	C9		
10	92874		1	11,000 μF 25V	C2 (U2L)		
11	92873		1	29,000 μF 25V	C5 (V2L)		
12	90098		2	CAPACITOR 2,200 pF, 500V	C3, C7		
13	91818		1	RESISTOR, 0.22 Ω 4W	R14		
14	92871		1	0.150Ω 4W	R15		
15	90480-9		2	5.6Ω 1/4W	R1, R7		
16	90480-63		4	1KΩ	R2, R9, R13, R19		
17	90480-71		1	2.2KΩ	R8,		
18	90480-87		1	10KΩ	R16		
19	90480-84		2	RESISTOR 7.5KΩ 1/4W	R4, R6		
20	90043-13		1	SCREW, PAN HD, 4-40 UNC X 3/8 LG			
21	90480-72		1	RESISTOR 2.4KΩ 1/4W	R17		
22	92870		2	RESISTOR, VARIABLE, 500Ω	R3, R10		
23	92529		1	RESISTOR, VARIABLE, 1KΩ	, R12		

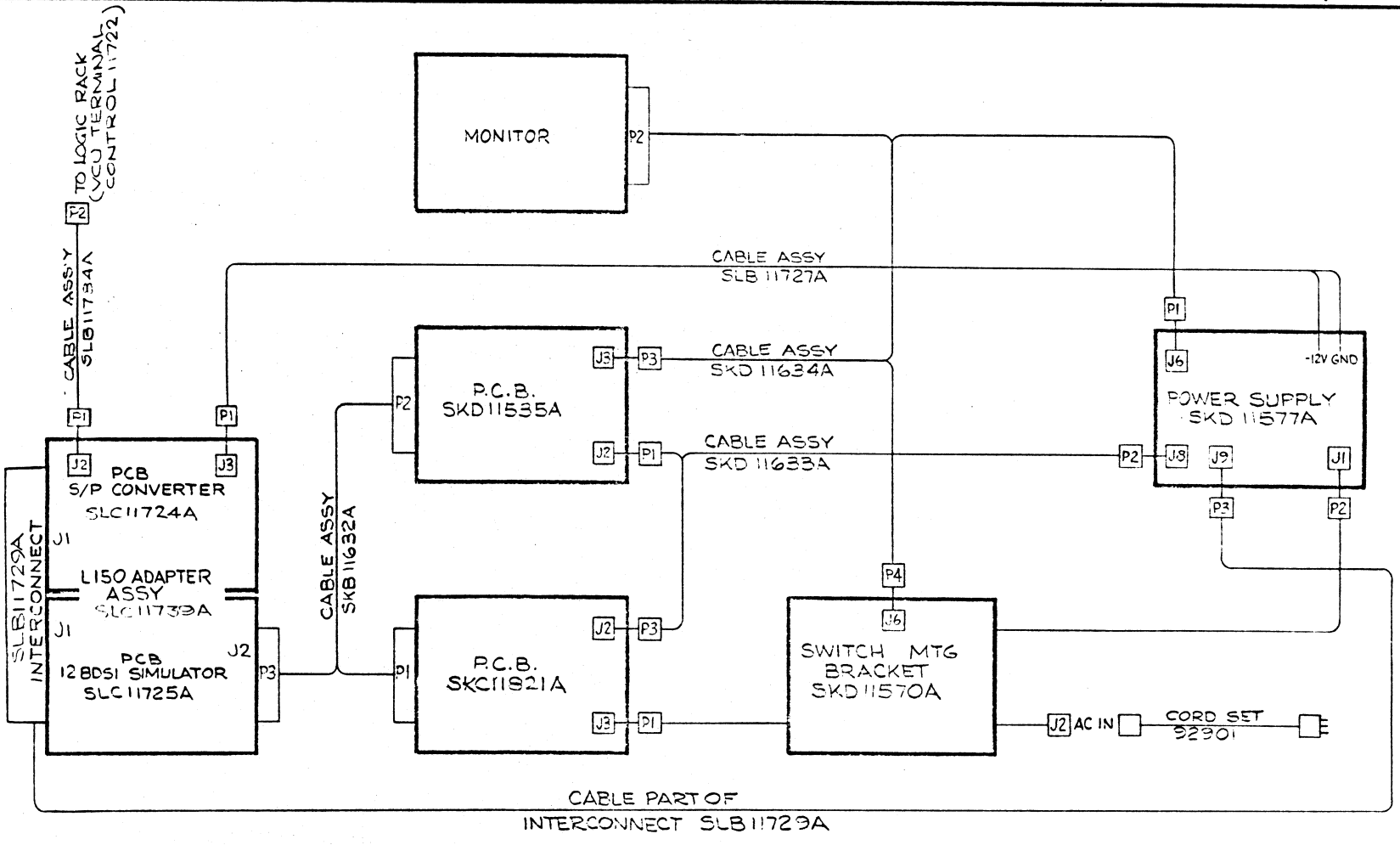
CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: RC	DATE 3 OCT 72	APPROVED BY WBS	QTY RUN
USED ON ASSEMBLY SKD11577A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SKC11579A		SHT 3 OF 3	CONTRO

TITLE: PCB ASSEMBLY
POWER SUPPLY, DATA TERMINAL
(FOR DRWG SEE SHEET 1)

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVA
24	92824		1	RESISTOR, VARIABLE, 2KΩ	R5		
25	92526		2	RECTIFIER, BRIDGE MDA 922-1	CR1, CR4		
26	90501		1	RECTIFIER BRIDGE MDA 960-2	CR2		
27	92527		1	RECTIFIER BRIDGE MDA 970-1	CR3		
28	91300		2	DIODE IN4151	CR6, CR8		
29	92831		2	DIODE MCL 1304	CR5, CR7		
30	90597		2	TRANSISTOR MPS 3704	Q2, Q4		
31	90598		1	TRANSISTOR MPS 3702	Q6		
32	92865		1	TRANSISTOR MJE 520	Q7		
33	91767		2	VOLTAGE REGULATOR MFC 6030	VR1, VR2		
34	92863		1	VOLTAGE REGULATOR MA7812	VR3		
35	90890		A/R	THERMAL COMPOUND			
36	924-47		A/R	ADHESIVE EC 1368 (3M)			
37	90480-94		1	RESISTOR 20K	R18		
38	90480-65		1	RESISTOR 1.2K	R11		
REF	SKD11577S			SCHEMATIC			



rev	eco	description	date	by	chk	apprvd
2	5F	CABLE INFO ADDED, NEW DWG NO	5 FEB 73	GT	GB	BJW
1		PREPRODUCTION RELEASE	17 JAN 73			

used on: SLD11617A
scale: NONE
date: 17 JAN 73
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC.
OTTAWA

title: DIAGRAM CABLE CONNECTIONS DATA TERMINAL SERIES 1 PHASE 1

sheet of | no. | rev 2

CONSOLIDATED COMPUTER INC.

EDRM-203A-0

Original

June 1972

Revisions

ENGINEERING DATA REFERENCE MANUAL

KEY-EDIT SERIES 100

DISC INTERFACE TO CCI 015 DISC

Approval:

Originator J. R. Pullen

Mgr Prod Line Engineering Robert B. Welden

Mgr Prod Line Development

CONTENTS

CONTENTS

ILLUSTRATIONS

1. INTRODUCTION

1.1 This equipment technical description describes the CCI disc interface to the CCI Model 015 Rotating Magnetic Memory.

1.2 The interface is designed to replace the drum controller as used on Mark V Key-Edit Series 100.

1.3 The interface consists of five pcbs located in the system logic rack. They are listed below, with a column of changes with respect to the Mark V drum controller:

PCB		Changes from drum controller
Word Count and Current Address	10442	No change
Drum and Mag. Tape IOT Generator and Multiplexor	10298	Modified by ECO
Derandomizer	10262	Modified by ECO 321
Disc Control	11254	New pcb
Disc Data	11255	New pcb

1.4 In addition to the above changes some back-plane wiring is required, and a -5v power supply, number , must be included. For further details see Equipment Installation Procedure

1.5 The interface will service up to four Model 015 discs by 'daisy-chaining' the I/O cables to the discs. (See Section 4 and Figure 8).

2. GENERAL SYSTEM OPERATION

2.1 Figure 1 shows the system flow diagram and demonstrates how the disc interface is incorporated in the system.

2.2 The disc is a single cycle data break peripheral, capable of both reading and writing information into core (CPU memory). The data is available on the omnibus from the memory and is controlled from there by the positive I/O interface, and the data break interface situated in the DEC PDP-8/E housing. The five pcbs of the disc interface control the data flow from the external bus to the disc, and vice versa.

2.3 When data is being written on the disc, it is taken from the core memory in parallel (12 lines) and stored temporarily in the Derandomizer (Figure 2). This pcb controls the data breaks from the CPU, demanding a break whenever its temporary data buffer content is getting low. The data is transferred from the buffer, on request, to the data pcb (11255), where it is arranged in serial by a shift register, and then sent to the disc.

2.4 When data is being read it is sent from the disc to the data pcb, where it is converted to 12 parallel lines of data and stored in the temporary buffer of the Derandomizer, which in conjunction with the Multiplexor, and the Word Count and Current Address pcbs, places the data in the core memory of the CPU via data breaks.

2.5 The Derandomizer, Multiplexor, and Word Count and Current Address pcbs are fully described in the Key-Edit Series 100/100 Mk V Technical Manual. The changes to the Derandomizer and the Multiplexor are detailed in Section 3 of this document.

2.6 The function flow of the Disc Data and Disc Control pcbs have been merged, and are shown in Figure 3. The address of the track, upon which the data is to be written, or read, is placed on the BAC lines (BAC 04-11). BAC00 is set high for a write, or low for a read operation. An IOT strobes the track address into the Track Address Buffer, and BAC00 into the Read-Write control circuitry. Thus the required track address is available on the Track Select Lines and the Read-Write control circuitry has been set up for the required mode of operation.

2.7 The starting sector address is then placed on BAC lines 04-11 and strobed into the Sector Address Buffer by an IOT. The output from this buffer is applied to the Sector Address Comparator with the Current Sector Address from the disc. The latter is continuously generated by a synchronous counter in the disc, and indicates which sector is currently under the read-write heads of the memory. When these two inputs to the comparator are the same a Match signal is produced.

2.8 The above procedure is common for a Read or Write operation. For a Write operation the following procedure then takes place: having achieved a match, one sector before the required sector, the derandomizer presents the Shift Register with the first word to be written. As soon as the next sector clock is received the write command will be given to the disc, which will send Read-Write Clock to the controller. This is used to shift the data in the Shift Register both to the CRC Register and to the disc.

During the shifting operation the derandomizer presents the next word on the parallel inputs to the Shift Register. This new word is strobed into the Shift Register as soon as the previous one is clear, and is shifted out in the same way. The Bit/Word Counter ensures that the parallel data is strobed in at the correct time.

2.9 Forty 12-bit words are shifted to the disc and the CRC Register in this way. Then the CRC Register acts as a shift register and sends out one more 12-bit word, which is the Cyclic Redundancy Check Character (CRCC). The control logic then removes the write command. This whole procedure may be repeated in the next sector(s) if required.

2.10 For a Read operation, the sequence of events described in 2.6 and 2.7 takes place and then the following procedure continues: at the beginning of the relevant sector the control logic will issue the Read Command, and after the disc has read its own preamble, it will present the first serial bit of data on the Read Data line coincident with the Read-Write Clock. This data is entered into the Shift Register and the CRC Register. At the appropriate time the contents of the shift register are transferred to the Read Buffer, allowing the Shift Register to accommodate the next word being clocked into it. This procedure is controlled by the Bit/Word Counter.

2.11 After the forty 12-bit words have been treated in the same way the CRC Register receives the last word, the CRCC, and uses it to check that the forty words preceding were read correctly. An indication is made on the status lines to the CPU if there was an error. The only action that can be taken is to reread.

2.12 Multiple disc configurations

The interface allows up to four CCI Model 015 discs to be attached to the system. This is achieved by using differential drivers and receivers in the discs and the interface. Each disc is allotted an address from 00_2 to 11_2, and a jumper is placed on the I/O pcb of the disc accordingly. The two most significant bits of the 9-bit track address determine which disc is being selected. This method is described more fully in Section 4.

3.0 Hardware Description

3.1 Disc Control pcb, 11254

The Disc Control pcb, 11254, is located in slot B23 of the Series 100, Level III Logic Rack, and performs the following functions: (Refer Dwg. D11254L)

- Track/Disc Selection
- Starting Sector Selection and Match
- Words per Sector Count
- Start/Stop Control
- Break Request
- Disc and Control Status Indication
- Interrupt and Skip

3.1.1 Track/Disc Selection

The track (head) addressing scheme is illustrated in Figure 4. Nine track address lines (D0, D1, S, XB, XA, YD, YC, YB, YA are made available to the disc to select one of 128_{10} tracks as a function of BAC 02 to BAC11 from the CPU. The disc clocking is such that each of the disc tracks is divided into 128_{10} sectors, each of 40_{10} data words. Since the Key-Edit Level III requirement is that tracks be divided into 64_{10} sectors of 40_{10} data words each, the disc tracks have each been sub-divided into two sections corresponding to disc sector addresses 00_8 to 77_8 and 100_8 to 177_8 respectively. The half-track selection is achieved via the sector selection circuitry (Refer Starting Sector Selection and Match description) as a function of the least significant bit of the track address (BAC 11) from the CPU. Thus all even track addresses (BAC 02 to BAC 11) correspond to the first half (Sector Clocks {SC} 00_8 to 77_8) of a specific

disc track and all odd track addresses (BAC 02 to BAC 11) correspond to the second half (SC 100_8 to 177_8) of a specific disc track. The effect is to double the total available track addresses per disc from 128_{10} to 256_{10}. 'Daisy-Chaining' will permit the installation of a maximum of four discs for a total of 1024_{10} available track addresses (256_{10} per disc). IOT 6504 (B21, lower centre of D11254L) loads the track address bits (BAC 02 to BAC 11) into two quad D-flops (G5, H5) and two D-flops (A5-5 and -9) on the disc control pcb. The address lines to the discs are driven by differential drivers. (See Section 4.)

3.1.2 Starting Sector Selection and Match

The starting sector address (00_8 to 77_8) of the data transfer is loaded into two quad D-flops (G4, H4) by IOT 6502. The output of these flip-flops, and the least significant bit of the track address (G5-10), provide the B inputs to two 4-bit comparators (G2, H2). Sector status bits SS0 to SS6 from the I/O pcb in the disc are received by differential receivers (D1, E1, G1, F1) and provide the A inputs to the comparators. These status bits are the outputs of a synchronous counter in the disc. The counter is reset by Index Clock (IC) and incremented by Sector Clock (SC) (counts from 000_8 to 177_8). Thus the binary output of the counter is always one count greater than the current sector address (e.g., SC 00 will increment the counter to 01). The most significant sector status bit (SS6), which distinguishes sector addresses 00_8 to 77_8 from 100_8 to 177_8 is compared (through F1-4) with the least significant bit (BAC 11) of the track address. Thus all even track addresses (BAC 11 low) correspond to the SC 00_8 to 77_8 half of a track, and all odd track addresses (BAC 11 high) correspond to the SC 100_8 to 117_8 half of a track. (Refer Track/Disc Selection description).

The X and Y outputs of the two comparators (G2, H2-6 and -9) will both be high when their respective A and B inputs are equal (i.e., when a sector match occurs). These outputs are applied through NAND gate F2-8 to the D input of the Sector Match flop, E2-9. Thus E2-9 pin 12 will be low for one sector before the selected starting sector address of the data transfer.

F3-1, a 40μs one-shot multivibrator, inhibits the Sector Match circuitry to allow sufficient track settling time. It is triggered on the leading edge of IOT 6504, and for 40 μs it applies a high level pulse through E5-1 to the strobe inputs of the two comparators (G2-8, H2-8). This action forces the comparator X and Y outputs to the low state and thus inhibits a sector match. The pulse is also applied through D3-6 to inhibit NAND gate D3-11 pin 12 and thus hold the Sector Match flop set.

When the pulse has expired, the direct set on E2-9 will be released and a sector match will be permitted at E2-9 pin 11. The match will be clocked through D2-6 by the next sector clock (i.e., the sector clock corresponding to the selected starting sector address) provided that the conditions on D2-6 are satisfied (Clock = SC·$\overline{\text{BRK}}$ $\overline{\text{RQST}}$·$\overline{\text{Matched}}$). D2-6 pin 5 will be high because E2-9 pin 10 was previously set by the 40μs pulse; D2-6 pin 4 will be high if a disc data break is not being requested. When the match is clocked through on the leading edge of Sector Clock, E2-9 pin 8 will go high while E2-9 will go low to D2-6 pin 5 to prevent further Sector Clocks from clocking E2-9 until shutdown. For example, if starting sector address 23 was loaded by IOT 6502, the sector match would occur at SC 22 (i.e., F2-8 low) and would be clocked through to E2-9 pin 8 by SC 23.

3.1.3 Words per Sector Count

The last bit of the Previous WD

When the disc data pcb is activated, the transfer of each word to or from the disc is indicated by the signal LWLB (last word last bit, from the disc data pcb), which corresponds to the negative-going portion of the 12th Read-Write Clock. A 40 Word (ripple) counter (A4, B4) on the control pcb is incremented on the negative-going leading edge of LWLB at pin B34, and will count the number of words that have been transferred. When 40 words have been transferred, the signal $\overline{\text{40 Word}}$ at pin B40 will go true (i.e., low at R-S flip-flop B5-8) to the disc data pcb to inititate CRCC Write (disc write operation) or CRCC Read and Check (disc read operation). The LWLB pulse associated with the CRCC word will increment the 40 Word Counter (A4, B4) to 41 and enable NAND gate C2-3 pin 1; pin 2 was conditioned previously by 40 Word. The output of the gate, C2-3, is one of the conditions of shutdown (Refer Start/Stop Control).

The 40 Word Counter, is reset by the signal $\overline{\text{Match}\cdot\overline{\text{SC}}\cdot\overline{\text{Interrupt}}}$ at the output of NAND gate E3-8. The conditions on the gate are that a sector match has occurred (E2-9 pin 8 high to E3-8 pin 11), that the disc $\overline{\text{Interrupt}}$ line is false (E5-13 high to E3-8 pin 10) and that $\overline{\text{SCB}}$ (SC Buffered) is true at E3-8 pin 9. This signal goes high corresponding to SC. The inverse of it at B3-6 resets the 40 Word R-S flop B5-8, and, as Match$\cdot\overline{\text{SC}}$ at pin B36, is used as a reset pulse on the disc data pcb.

3.1.4 Start/Stop Control

Start control is initiated by IOT 6504. This IOT loads either the Read or Write command into the Read and Write select D-flops, C4-5 or C3-5 respectively, according to the state of BAC 00 from the CPU (BAC 00 low is disc Read command; BAC 00 high is disc Write command).

These two flip-flops were previously reset by IOT 6501 at pin B26, or when the CPU was in the stop mode, pin B25. The $\overline{Q}$ outputs are routed through IOR gate D4-8 to enable NAND gate D3-11 pin 13. D3-11 output will go true, after the 40 μs pulse from F3, to make inverter D3-8 output high to indicate that the disc controller is busy. The high level will release the direct set input of the Sector Match flop, E2-9, to permit a sector address compare and match operation (Refer Starting Sector Selection and Match).

The Q outputs of the Read and Write select flops, in conjunction with the sector match signal (E2-9 pin 8 high is sector match), enable the signals $\overline{\text{Read}\cdot\text{Match}}$ at B31, and $\overline{\text{Write}\cdot\text{Match}}$ at B38, to the disc data pcb and derandomizer pcb. Another signal, Write•Select, pin B30, is enabled to the derandomizer when the write command has been loaded (C5-11 pin 12 high) and when the disc interrupt is inactive (C5-11 pin 13 high).

The stop control, or shutdown, is initiated by resetting the Read and Write selection flops. This results in D4-8 going low and applying a clock input, via D4-11, to the disc Flag flop, C4-9 pin 11. This results in a low level output at C4-9 pin 8 and via D2-8 and F5-4 to the $\overline{\text{INTRPT}}$ line to the CPU, pin B20. Disc Control Busy at D3-8 is also low to directly set the Sector Match flop, E2-9 pin 10.

The conditions for shutdown at Sector Clock time must be satisfied at the inputs of NAND gate F2-6. These conditions are: $\overline{\text{Word Count Overflow}}$ at B28 must be low to indicate that the final data break has been accepted to write the last data word into, or read the last data word from, the CPU memory; C2-3 must be low to indicate that Word 41 has been read or written from the disc;

Inhibit Shutdown at B41 must be high to pin 2 in the Write mode to indicate that the derandomizer (both the RAM and the output buffer) is empty (inhibit shutdown is always high in the read mode); NAND gate E3-8 must be high to pin 5.

3.1.5 Break Request

The Disc Break Request flop, C3-9, issues break requests via pin B24 to the Drum & MTT IOT PCB, 10298, under control of the signal $\overline{\text{1 to Drum BRK REQ}}$, pin B33, from the derandomizer pcb. This action indicates that the derandomizer is ready to receive a data word from CPU memory (disc Write operation) or transfer a word to CPU memory (disc Read operation).

The break request flop is cleared by the signal $\overline{\text{Drum BRK ADRS ACPTD}}$ from the Drum & MTT IOT pcb. This signal originates in the Positive I/O pcb and indicates that the break request has been accepted by the CPU. The flop is directly set by the WC Overflow signal and further break requests are thus inhibited (D4-3 to E3-12 pin 1, D3-3 to C3-9 pin 10).

3.1.6 Disc and Control Status Indication

The status of the disc and the disc controller are available to the CPU on demand. IOT 6512 at pin B13 enables the disc status bits to the CPU accumulator. When the disc control is busy D3-8 is high to C2-8 pin 9 and F5-1 pin 2. When the disc is not ready there is a high level on pins W and 19. D-flop E2-5 pin 1 will be directly reset by C2-8 to produce an Interrupt signal to the CPU via D2-8 and F5-4, and to indicate that an illegal status condition exists. The Disc Not Ready status, AC 00 at pin B11, and the Disc Control Busy status, AC 02 at pin B16, indicate this condition.

$\overline{\text{AC OI IN}}$ is a status indication for an abort function. It is represented by:

Abort = Start Control plus 40ms· Control Busy·$\overline{\text{Flag}}$ + SC.
(Read command + Write Command)

This prevents the controller from holding up the system should a track be unusable, even though the disc status is good. The latter half of the equation is a hardware check, as the Write or Read commands should never be true during sector clock time.

Monostable A1 is triggered on pins 1 and 2 by IOT 6504, and holds F4-6 pin 4 low for 40ms, after which time F4-6 is enabled. This 40ms is sufficient for any transfers to be completed. Then, if the Flag flop is still false (C4-9 pin 8 to F4-6 pin 5), and the controller is still busy (D3-8 to F4-6 pin 2), F4-6 will go low true and set the Abort flop B1-5. Similarly $\overline{\text{Write Command}}$, pin B27, or $\overline{\text{Read command}}$, pin B12, are IORed at B3-8 and applied to the D input of the Abort flop. SC is applied to the C input, consequently the flop will be set if either of the write or read commands (sent to the disc) are true at SC time. If B1-5 is set (high) then E5-10 pin 9 will be true and status bit one will be set upon interrogation by IOT 6512. Simultaneously an Interrupt will be generated: B1-5 pin 6 will be low, and through D2-8 pin 10 and F5-4 assert $\overline{\text{INTRPT}}$ at pin 20.

3.1.7 Interrupt and Skip

The Interrupt line to the CPU (B20) will go low true via the Positive I/O pcb to indicate that the disc has completed the initiated operation, or that an illegal status condition exists.

When the CPU recognizes the interrupt it will perform a JMS 0 to field 0 and begin to search for the interrupting device. The test to see if the interrupt was initiated by the disc consists of issuing IOT 6511 and thus conditioning the CPU Skip line at pin B23. If the disc has initiated the interrupt, F5-10 pin 9 will be low, and thus IOT 6511 will assert the Skip line to the CPU. This condition is interpreted by the CPU program as indicating a disc interrupt condition and appropriate action is taken to service the interrupt.

3.2 DISC DATA PCB, 11255

The Disc Data pcb, 11255, is located in slot B22 of the Series 100, Level III Logic Rack, and performs the following functions: (Refer Dwg D11255L)

Write Data Word Control and Serializing
Read Data Word Control and Assembly
CRCC Calculation and Serializing
CRCC Read and Check

3.2.1 Write Data Word Control and Serializing

The disc Write operation data flow is shown in Figure 2.

When the disc Write Command is loaded by IOT 6504 the Derandomizer pcb, 10262, will request six consecutive data break cycles to fill the four RAM locations (only 4 of the 16 available RAM locations are used), and the RAM Input and Output Buffers with the first six data words to be written on the disc. Twelve-bit Write Data words are then available at the output of the RAM Output Buffer, OB0 to OB11, and loaded (under control of the data pcb) into three 4-bit shift registers on the data pcb D5, C5, A5 for serializing to the disc.

The first data word to be written is loaded into the 12-bit Shift Register during sector clock time, as illustrated in Figure 5. The Shift Register is enabled to the parallel or load mode at pin 1 from B5-8 and E5-8 as a function of $\overline{SCB}$, pin B14, and $\overline{Write \cdot Match}$, pin B11. A strobe pulse at pins 12 and 13 is provided from the pulse shaping circuit R8, C35, CR3 and F5-12. As shown in Figure 5, the effect of this circuit is to provide a load strobe to the Shift Register while the latter is in the parallel mode, and thus load the first Write Data word from the RAM Output Buffer (OB1 to OB11) into the Shift Register.

It is desirable to fetch the next data word from the RAM to the RAM Output Buffer while the current word is being written on the disc. This allows a maximum of 12 bit times (3μs) to perform the necessary RAM read operation. The RAM read is inititated by the signal $\overline{Load \cdot Preamble}$, pin B16, on the disc Data pcb. The signal is set either at sector clock time to inititate fetching the second data word to the RAM Output Buffer (E5-8, B5-8, to E5-3 pin 1), or from the trailing edge of $\overline{RWC}$ 10 to the trailing edge of $\overline{RWC}$ 11 (Figure 5) to initiate fetching of each of the data words, 3 to 40, in a sector (E5-11, B5-8, to E5-3 pin 1) in turn from the RAM to the RAM output buffer. Note that NAND gate E5-3 pin 2 is conditioned if the signal $\overline{40\ Word}$ pin B5 from the 40 Word Counter on the disc control pcb is false (high). Thus load preamble will not occur after 40 words have been written on the disc until the 40 Word Counter is reset by $Match \cdot \overline{SC}$ (the CRCC word is made available by the data pcb and written as word 41 on the disc).

Whenever a word is read from the RAM into the RAM Output Buffer, the derandomizer will sense that it is no longer full and will write the word currently in the Input Buffer into the empty location in the RAM. Simultaneously, the derandomizer will request a data break cycle from the CPU to refill the input buffer. Break requests may not be answered for up to 4.6μs, so it is possible that the derandomizer may be deficient two words from the full condition of six words. In this case, consecutive break requests will be made to ensure that the data pcb will always have a supply of six words on which to draw during a disc write operation.

The condition that 11 Read-Write Clocks (RWC) have occurred (to enable E5-3 pin 1) is determined by the Bit/Word Counter, a synchronous counter consisting of the group of seven D-flops A3-5 to D3-5. This counter is reset by the signal Match·$\overline{SC}$, at pin B13, from the control pcb and incremented on the leading edge of RWC (H2-4 to F4-8). Figure 6 illustrates the counting sequence. A count of 11 is decoded from D3-5, and C3-5 pin 6, to NAND gate E3-6 pins 4 and 5 respectively; the output of E3-6 will be true (low) until the counter is reset. During a disc write operation ($\overline{\text{Write·Match}}$ true {low} at pin B11) NAND gate E5-11 will be true (low) on count 11 to provide the mode select via B5-8 to the Switch Register, and to set the $\overline{\text{Load Preamble}}$ signal via E5-3 to pin B16. In addition, a count of 12 is decoded from C3-9 pin 8, and D3-5, to NAND gate E3-8 pins 9 and 10 respectively. The output of E3-8 is typically 50 ns wide and E3-8 resets the Bit/Word Counter and hence inhibit both E3-8 and E3-6 (high).

The least significant bit of the Shift Register output, A5 pin 2, is made available to the disc and the CRCC circuitry as Write Data. The write data is routed to the disc via D1-11, E1-6, and differential driver A1 when the following conditions are satisfied: Write•Match is true (high) at E1-6 pin 5 (from pin B11 through inverter G5-2) thus indicating that a disc write operation is in progress, and $\overline{\text{40 Word}}$ (pin B5) is false (high) to inhibit D1-8 pin 9 through inverter B4-11 and thus enable D1-11 pin 12. When a data word is loaded in parallel into the Shift Register from the derandomizer output buffer, the least significant bit (OB11 at A5 pin 2) is immediately available to the disc. The disc loads write data and provides the disc data pcb with the signal $\overline{\text{RWC}}$ (negative-going edge) to synchronize the shifting of the next data bit to the disc. The $\overline{\text{RWC}}$ signal is received via differential receiver H2 from pins 6 and F, and clocks the Shift Register (in the serial mode via B4-8 and E5-6 if not at sector clock or count of 11) and makes the next data bit available at A5 pin 2.

3.2.2 Read Data Word Control and Assembly

The data flow for a disc Read operation is illustrated in Figure 2.

Serial $\overline{\text{Read Data}}$ is made available by the disc at pins W and 19, and shifted into the Shift Register and the CRCC Register on the data pcb in synchronism with the $\overline{\text{RWC}}$ signal. The Shift Register will be in the serial mode for the entire disc Read operation since $\overline{\text{Write•Match}}$, from pin B11, false (high) inhibits E5-8 pin 10 and B5-8 to ensure a low level at pins 1 of the register. A shift to the right occurs on the negative-going edge of $\overline{\text{RWC}}$, thus ensuring that the Shift Register clock occurs approximately in the centre of the Read Data signal (Refer Figure 8).

The first eleven bits of data word are shifted into the register; the twelfth RWC loads these eleven bits (available at the register Q outputs) and the twelfth bit of Read Data (MSB available at the serial data input of the Shift Register, D5 pin 10) into the Disc Read Buffer (DRB), formed by three quad D-flops D4, C4, A4. The Shift Register will be shifted as usual by RWC 12 (Refer figure 7) and therefore the DRB must be loaded before the register is shifted, so that the data to the DRB is correct. The DRB load sequence is initiated typically 20 ns before the Shift Register shift. RWC 12 to the DRB is equivalent to $\overline{\text{LWLB}}$ and is provided as shown in Figure 7. A count of 11 is decoded from the Bit/Word Counter and conditions B5-6 pins 4 and 5 via E3-6 and G5-10. The output of B5-6 will go true (low) when the positive-going portion of RWC 12 enables B5-6 pins 1 and 2. Both the Bit/Word Counter (incremented by RWC) and the 40 Word Counter (incremented by $\overline{\text{LWLB}}$) are operational during the disc Read operation. Figure 7 shows that a clock is provided to the Shift Register during sector clock time from the pulse shaping circuit associated with F5-12. This clock is essentially a 'don't care' condition since read data does not arrive until after the preamble time. The Read Command to the disc is set via flop I5-9 to H1-13 pin 2 on the trailing edge of sector clock if $\overline{\text{Read}\cdot\text{Match}}$ is true (low).

The $\overline{\text{Read Last}}$ signal at pin B29 removes the 12-bit Read Data word from the DRB before the next word, currently being assembled in the Shift Register, is loaded into the DRB (12 bit times - 3μs - between DRB loads). $\overline{\text{Read Last}}$ goes true from the leading edge (negative-going of $\overline{\text{RWC}}$ 11 to the leading edge (negative-going) of $\overline{\text{RWC}}$ 12 (Figure 7) at the output of NAND gate F5-6. A count of 11 from the Bit Word Counter is decoded at E3-6 and applied through inverter G5-10 to enable F5-6 pin 4.

F5-6 pin 3 will be true when the Read Command is enabled to the disc from I5-9, on the trailing edge of sector clock after $\overline{\text{Read·Match}}$ goes true. As with $\overline{\text{Load Preamble}}$, the signal $\overline{\text{Read Last}}$ does not occur after $\overline{\text{40 Word}}$ goes true from pin B5 via F5-6 pin 5.

$\overline{\text{Read Last}}$ is applied to the derandomizer pcb where it initiates a RAM Write operation to write the word from the DRB into the RAM. A total of six locations, four RAM locations plus the input and output buffers, are available in the derandomizer pcb for temporary storage of disc read data. The RAM Scaler Flag, C1, senses the state of the RAM and will issue a break request to the CPU when the RAM is not empty during a disc read operation. The first data word written in the RAM will automatically be read (from the RAM) into the output buffer, and thus made available to the CPU. When the data break request is accepted the data currently in the output buffer is written into memory and a RAM Read operation is initiated, if the RAM is not empty, to fetch the next word to the output buffer. Since break requests may not be answered for a maximum of 4.6μs, it is possible to have a data word in the RAM output buffer and a data word in the RAM during a disc Read operation. In this case, two consecutive break requests will be demanded by the derandomizer to return the RAM to the empty condition.

3.2.3 CRCC Calculation and Serializing

In addition to the forty 12-bit data words written in each sector of a disc track, a 12-bit Cyclic Redundancy Check Character (CRCC) is also written as word 41 in each sector. The CRCC is an exotic check-sum character accumulated, by a register on the disc data pcb (A2 to F2), on the 40 data words currently being written in a disc sector.

The CRCC calculation follows the polynomial:

$X^{12} + X^{11} + X^3 + X^2 + X + 1$

where X= Position of XORS in the CRCC Register.

The current write data bit to the disc (LSB of the Shift Register) is provided to the CRCC Register through NAND gate G4-6, IOR gate G1-6, and XOR gate B1-13 pin 14. This action is conditional on $\overline{\text{Write}\cdot\text{Match}}$ being true (high) at G4-6 pin 5 (from G5-2) and $\overline{\text{40 Word}}$ false (high) at G4-6 pin 4. The latter condition dictates that write data from the Shift Register (A5 pin 2) will no longer be available to the CRCC Register after the $\overline{\text{LWLB}}$ pulse associated with data word 40 (this pulse increments the 40 Word Counter to 40, and thus inhibits $\overline{\text{40 Word}}$ via G4-6 pin 4). Thus B1-13 pin 14 will be low during the CRCC write time.

Until $\overline{\text{40 Word}}$ goes true (low) the output of NAND gate D1-8 will be false, $\overline{\text{40 Word}}$ inhibits D1-8 pin 9 through inverter B4-11, to enable NAND gate D1-11 pin 12 and thus permit write data to the disc through D1-11 pin 13 to E1-6 pin 4. In addition, D1-8 false (high) will enable G1-11 pin 12 to permit the LSB of the CRCC Register (F2-9) to condition one input of XOR gate B1-13, via G1-11 and G1-8. Thus the LSB of the CRCC Register and the current write data bit from the Shift Register are XORed through B1-13 (as the polynomial) and clock the XOR gates, and flop A2-5 D input, of the CRCC Register.

The CRCC Register is reset on the leading edge (negative-going) of sector clock, from inverter G5-6 through power drivers E4-6 and -8, and clocked on the trailing edge (positive-going) of RWC from H2-4 and inverted through F3-8. This is the same edge of RWC that

When $\overline{\text{40 Word}}$ goes true the CRCC Register will supply the write data for word 41 (CRCC word), and the output of the Shift Register will be inhibited. Thus G4-6 pin 4 will be low, and G1-6 will be low to XOR gate B1-13 pin 14. NAND gate D1-8 will be true (low) to inhibit G1-11 pin 12 and provide a low level at B1-13 pin 15. The output of B1-13 will be low until the $\overline{\text{40 Word}}$ signal is inhibited; this action will force all the XOR gates in the CRCC circuit to act as non-inverting buffers between stages. The effect is that the CRCC circuit is then a 12-bit shift register. The CRCC which has been calculated on the 40 data words, and which is currently in the CRCC Register, will be shifted by RWC from left to right to the Write Data line without being altered by the XOR gates.

The LSB of the CRCC Register is presented to the Write Data line (pins S and 15) to the disc via NAND gate E1-12 and IOR gate E1-6. E1-12 pin 2 is conditioned through inverter B4-11 when the signal $\overline{\text{40 Word}}$ is true (low).

Twelve bit times are required to shift the contents of the CRCC Register to the Write Data line. However, the shifting will continue as long as RWC is available to clock the CRCC Register. The signal $\overline{\text{40 Word}}$ will go false (high) and thus inhibit further data from the CRCC Register to the Write Data line when the 40 Word Counter is reset at sector clock time. The LSB of the Shift Register will then provide the write data through D1-11 pin 13 (D1-11 pin 12 is conditioned because $\overline{\text{40 Word}}$ false inhibits D1-9 pin 9) until $\overline{\text{40 Word}}$ goes true again. Data written after the CRCC word and before sector clock time is the Postamble, and will have a binary value of zero because B1-13 is low to A2-5 pin 2 (i.e., zeros will be shifted after the 12th bit of CRCC until sector clock time).

The signal Load Preamble was inhibited by 40 Word true (low) to E5-3 pin 2. Thus when a count of 11 associated with the CRCC word, conditions NAND gate E5-3 pin 1, the other input, pin 2, will be previously inhibited by 40 Word. This action excludes the possibility of initiating a RAM Read operation after the last bit of the CRCC word has been written, at least until the next sector clock.

3.2.4 CRCC Read and Check

The CRCC calculated on the 40 write data words of a sector, and written as word 41 in the sector, is such that if it were included in a new CRCC calculation as an additional data word to the original 40, the new CRCC would be zero. Therefore, during a disc read operation, if the 40 data words, plus the CRCC word, that were written previously are put through the CRCC Register, the result should be a calculated CRCC value of zero (Q outputs of A2 to F2 should be low). If the result is not zero a CRCC error condition exists and the Read Data is in question.

During a disc read operation, Read Data is made available to the CRCC Register from differential receiver H2-9, via G1-3, G1-6, and XOR gate B1-13. NAND gate G1-3 pin 1 is conditioned when the Read Command is enabled to the disc by flop I5-9 (on trailing edge of Sector Clock). The CRCC Register will operate as during a disc write operation until the signal 40 Word goes true (when word 40 has been read from the disc). At this time, inverter B4-11 will go high to condition D1-8 pin 9 and E1-12 pin 2 (as during a disc write). However, D1-8 pin 10 is inhibited (low) because Write·Match from inverter G5-2 is false (low). Therefore, G1-11 pin 12 will remain high to maintain the input at XOR gate B1-13 pin 15 from the LSB of the CRCC Register via F2-9, G1-11 pin 13, G1-8, B1-13 pin 15).

Thus, the action of the CRCC Register is allowed to continue to include the CRCC word (previously written) in the calculation. Note that the Write Data line to the disc is held high during a disc Read operation because Write•Match is false (low) at E1-6 pin 5.

When the last bit of the CRCC word has been clocked into the CRCC Register, the $\overline{Q}$ outputs of A2 to F2 will all be high. Multiple input IOR gates F3-6 and G2-8 sense the condition of the $\overline{Q}$ outputs and through NOR gate G3-10 condition the D input of flop I5-5. If one of the $\overline{Q}$ outputs is low (thus indicating a CRCC error condition) the data input to I5-5 will be low and when the flop is clocked from F5-8 the $\overline{Q}$ output will go high to NAND gate H5-10 pin 9. This gate is conditioned on pin 8 by IOT 6512 (Read Status) from the CPU. Its output is applied to the CPU accumulator ($\overline{AC03\ IN}$), and when it is true (low) it indicates a CRCC Error condition.

The CRCC Error status is cleared by the signal $\overline{Drum\ Write\ Sync}$, at pin B3, from the disc control pcb. This signal occurs when IOT 6501 (Reset Disc Done Flag and Control) is issued, or when the CPU is in the stop mode (B Run false). When $\overline{Drum\ Write\ Sync}$ is true (low) D-flop I5-5 is set to inhibit H5-10 pin 9 (low).

The CRCC Error flop, I5-5, is clocked when NAND gate F5-8, pin 10 is inhibited. Read•Match true (high) will condition F5-8 pin 11 so that CRCC Error status is only checked during a disc Read operation. After the 40th word has been read from the disc, $\overline{40\ Word}$ true (low) will condition F5-8 pin 9 through inverter B4-11. When a Read Command (pins 8 and J) is enabled to the disc (on trailing edge of sector clock) by I5-9 true, input F5-8 pin 10 will be enabled. Thus F5-8 will be true (low) when the CRCC word (word 41) is being read into the CRCC Register.

When $\overline{\text{40 Word}}$ goes true (low), the data input of flop D3-9 pin 12 will go high from inverter B4-11. The trailing edge (positive-going) of the $\overline{\text{LWLB}}$ signal associated with the CRCC word (word 41) will clock D3-9 to the set condition. Thus D3-9 pin 8 will be low to IOR gate F1-6 pin 4, to directly reset I5-9 and thus inhibit both the Read Command to the disc, and gates F5-8 pin 10 and G1-3 pin 1. F5-8 will go high to clock the CRCC Error flop, I5-5, and hence sample the state of the CRCC Register Q outputs. When G1-3 pin 1 is inhibited B1-13 pin 14 is conditioned low (from G1-6) to ensure that the contents of the CRCC Register are maintained.

During a disc Write operation, the action of flop D3-9 will inhibit the Write Command to the disc on the trailing edge (positive-going) of $\overline{\text{LWLB}}$ associated with the CRCC word.

When shutdown is initiated on the disc control pcb, the signal $\overline{\text{Match·SC}}$ will go low, and stay low, until a new disc operation is initiated. This action will hold the Bit/Word Counter on the disc data pcb in the reset condition (pin B13 through E3-3). In addition, the signals $\overline{\text{Write·Match}}$ and $\overline{\text{Read·Match}}$ from the disc control pcb will be false (high) to inhibit the Write and Read Commands to the disc via the data pcb (pin B11 through inverter G5-2 to H1-8,9, and pin B15 through inverter G5-4 to H1-12,13).

The Write Data line to the disc will be held high when $\overline{\text{Write·Match}}$ is inhibited by G5-2 to E1-6 pin 5. Derandomizer control signals $\overline{\text{Read Last}}$ and $\overline{\text{Load Preamble}}$ will both be inhibited under shutdown conditions. The former at F5-6 pin 3 when $\overline{\text{Read·Match}}$ false resets I5-9, and the latter at E5-3 pin 1 when Write Match false through inverter G5-2 inhibited NAND gate E5-8 to IOR gate B5-8 pin 12, and when B5-8 pin 13 is inhibited by the Bit/Word Counter reset (E3-6 false to inhibit NAND gate E5-11). The signal $\overline{\text{LWLB}}$ will be inhibited when the Bit/Word Counter is held reset (G5-10 low to B5-6).

Thus all control signals from the disc data pcb to the Disc, derandomizer pcb and disc control pcb will be invalidated under shutdown conditions.

4. SPECIAL DEVICES

4.1 General

To enable up to four discs to be used on one system the method of 'daisy-chaning' was used, see Figure 8. This required using differential drivers and receivers because of the length of cable involved. The controller has 62Ω terminating resistors included at the end of the cable, and terminator number is required in the socket of the last disc.

4.2 Daisy-Chaining

The principle of 'daisy-chaining' involves sending all the interface signals to every disc, but the two most significant bits of the track address (D0 & D1) represents the disc address:

D0	D1	Disc
0	0	0
1	0	1
0	1	2
1	1	3

These two bits of the track address are decoded in each disc and the decode is fed to the inhibit input of the drivers and receivers in that disc. Thus only one disc is allowed at a time.

4.3 Special Integrated Circuits

The differential drivers and receivers are Texas Instruments SN 75110 and SN 75107A respectively, with an inhibit input.

They were chosen because of this extra input and because of their speed. The maximum delay through either of the devices is 25ns. These devices require a -5v power supply, thus supply number is used in the logic rack.

For full details of these devices and the way in which they are used see Texas Instruments book 'The Integrated Circuits Catalog' page 3-132 to 3-148.

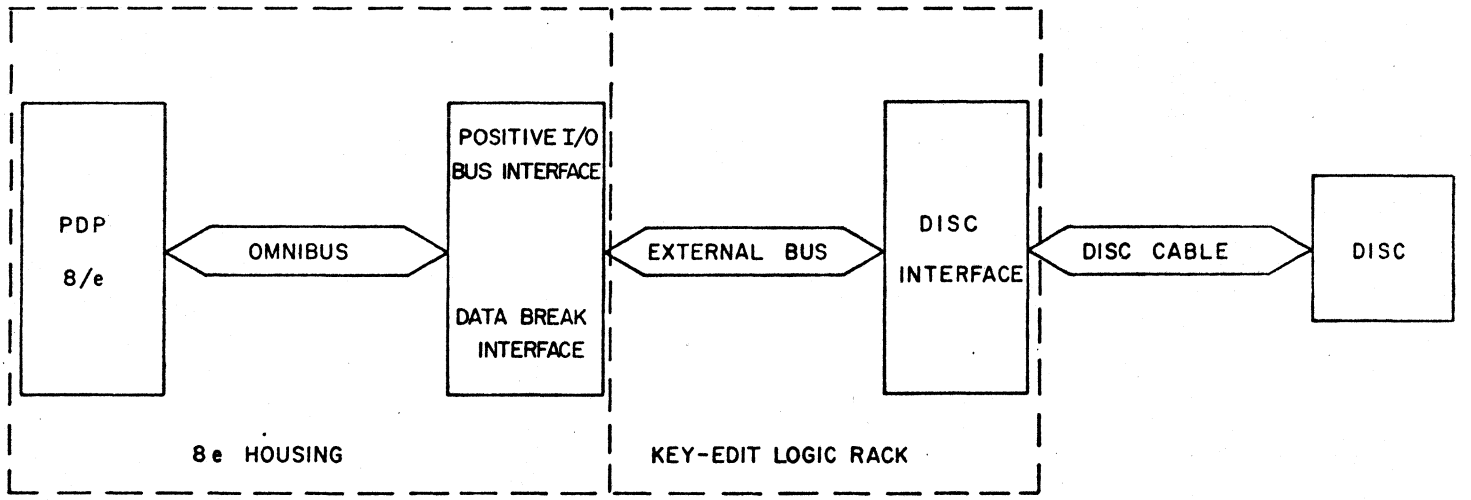
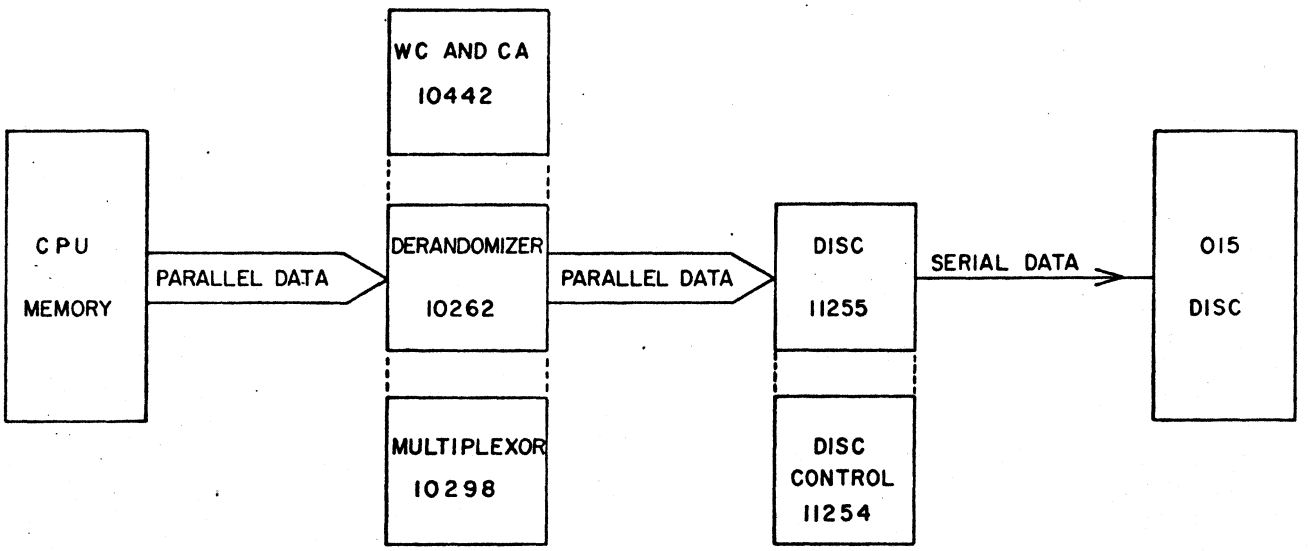
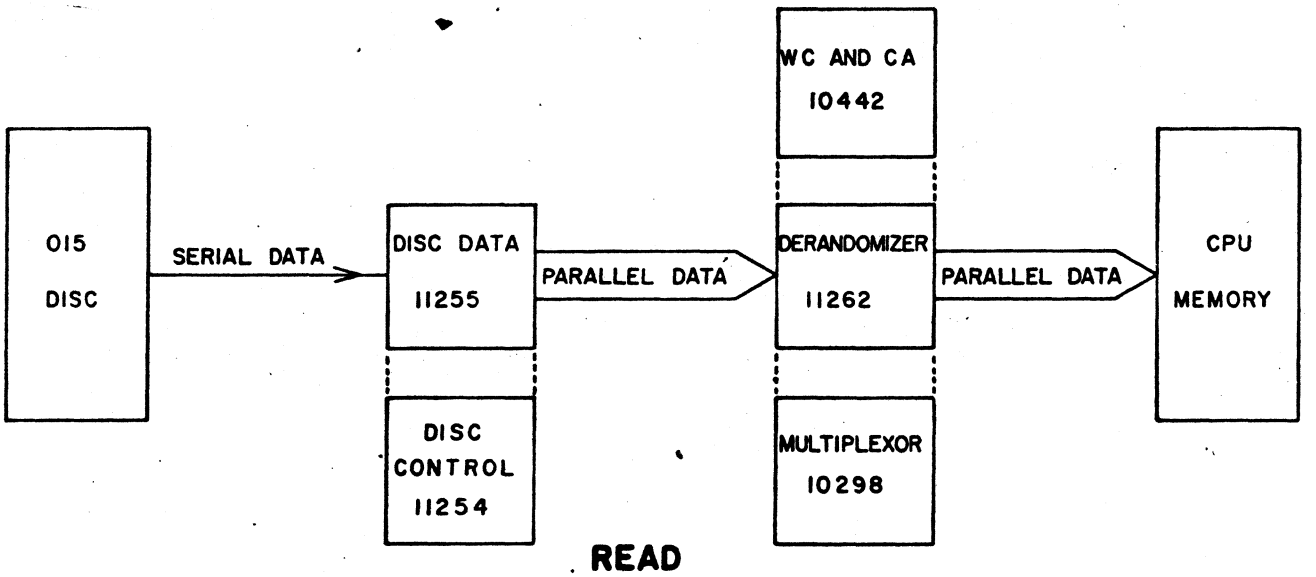


FIGURE 1
SYSTEM FLOW DIAGRAM



WRITE



READ

FIGURE 2
SYSTEM DATA FLOW

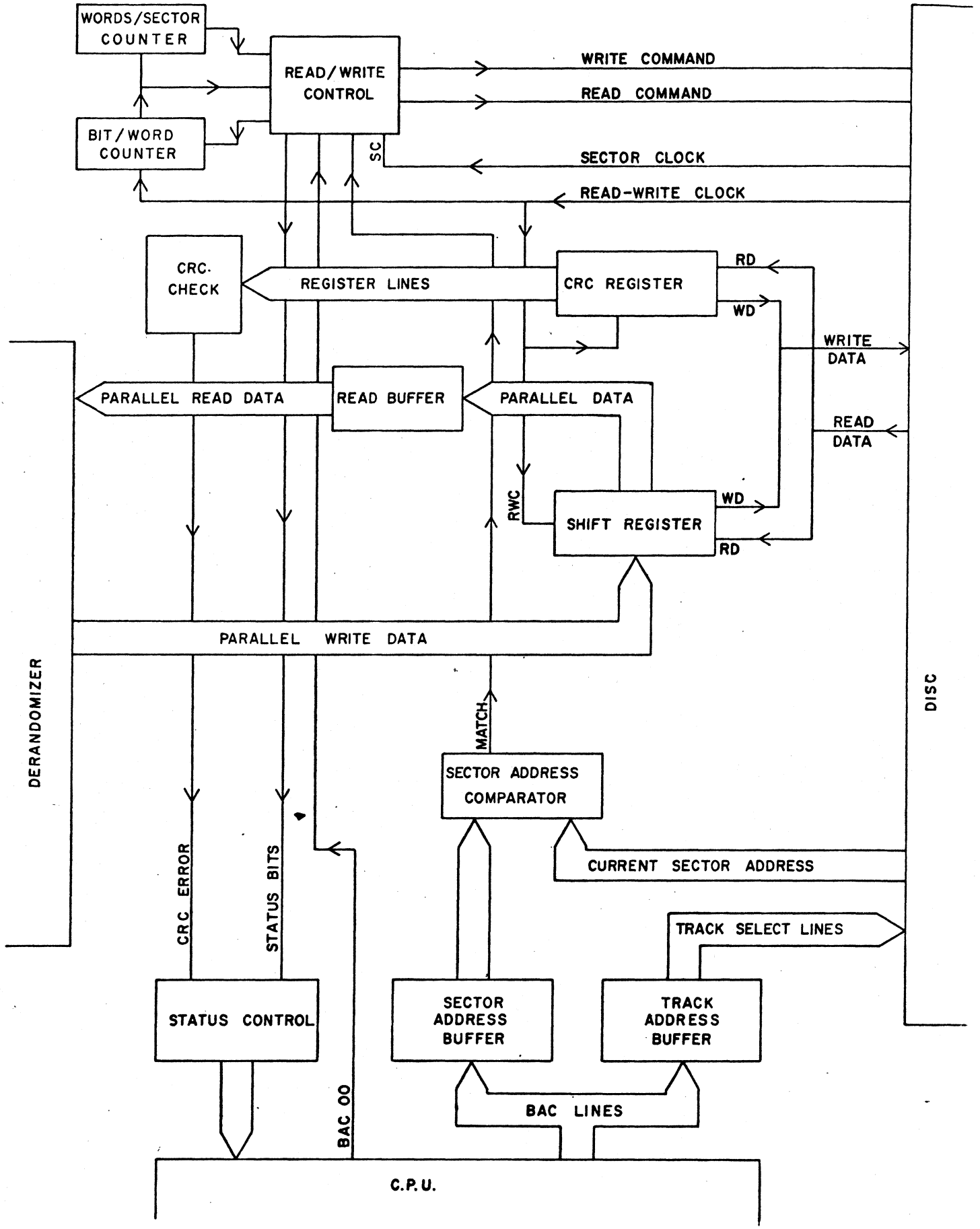
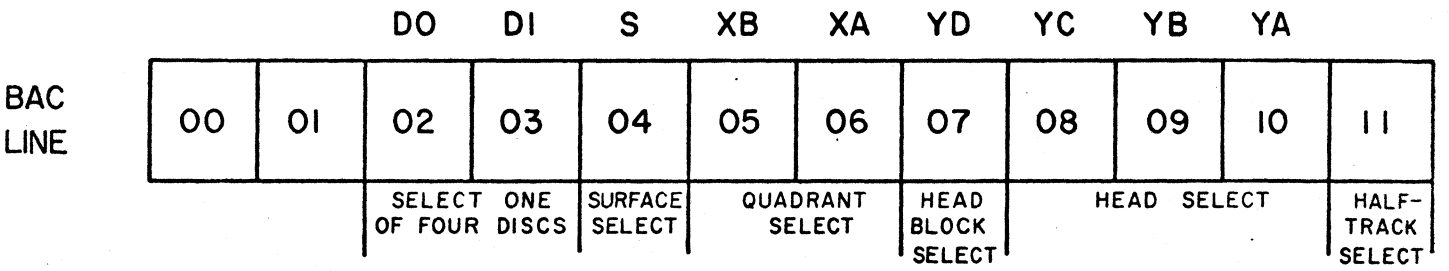
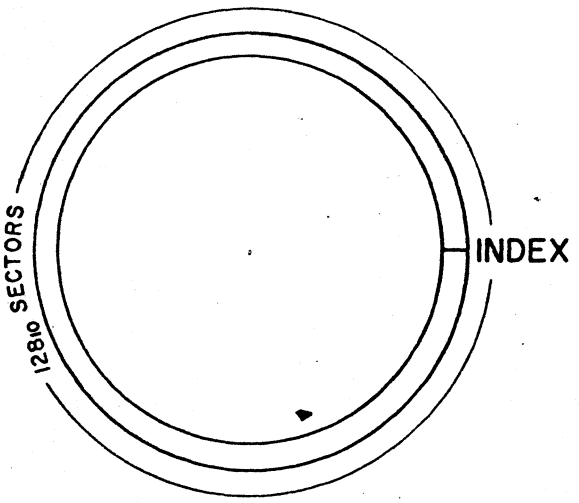


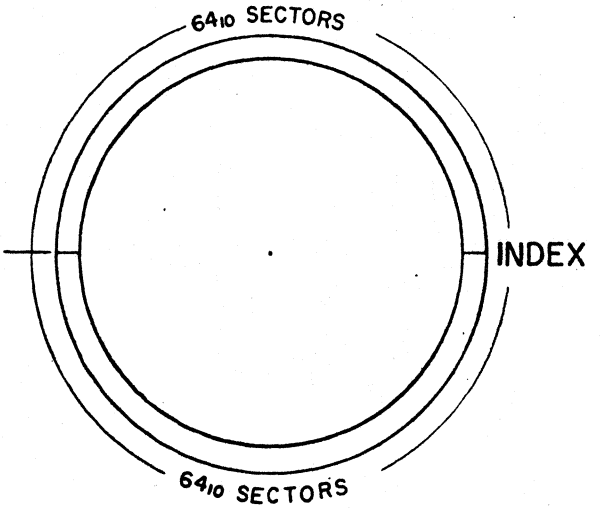
FIGURE 3

INTERFACE FUNCTION FLOW DIAGRAM





PHYSICAL TRACK CONFIGURATION



TRACK CONFIGURATION PRESENTED TO THE SOFTWARE BY THE CONTROLLER.

FIGURE 4
TRACK ADDRESS

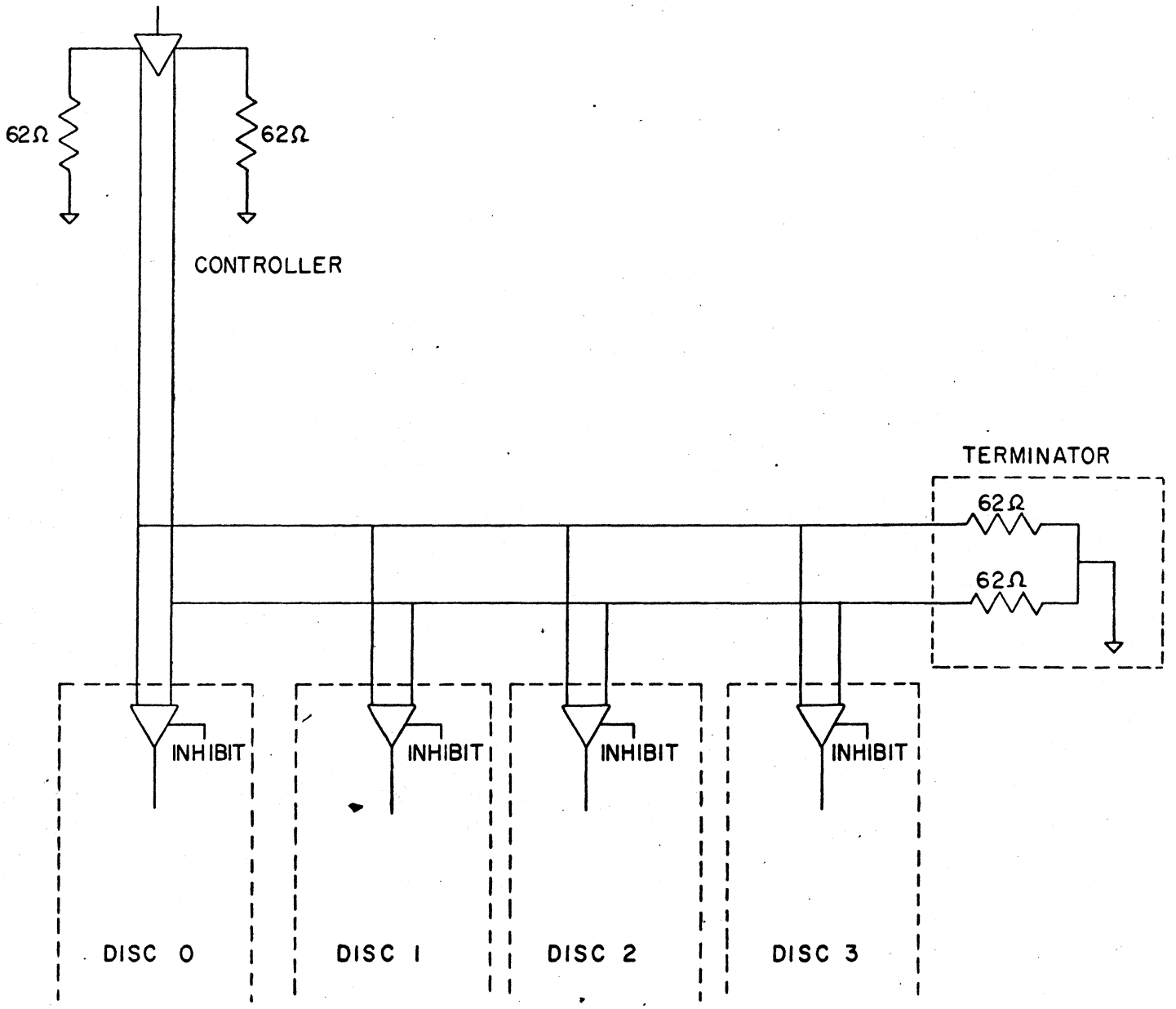


FIGURE 8
METHOD OF DAISY-
CHAINING FOUR DISCS

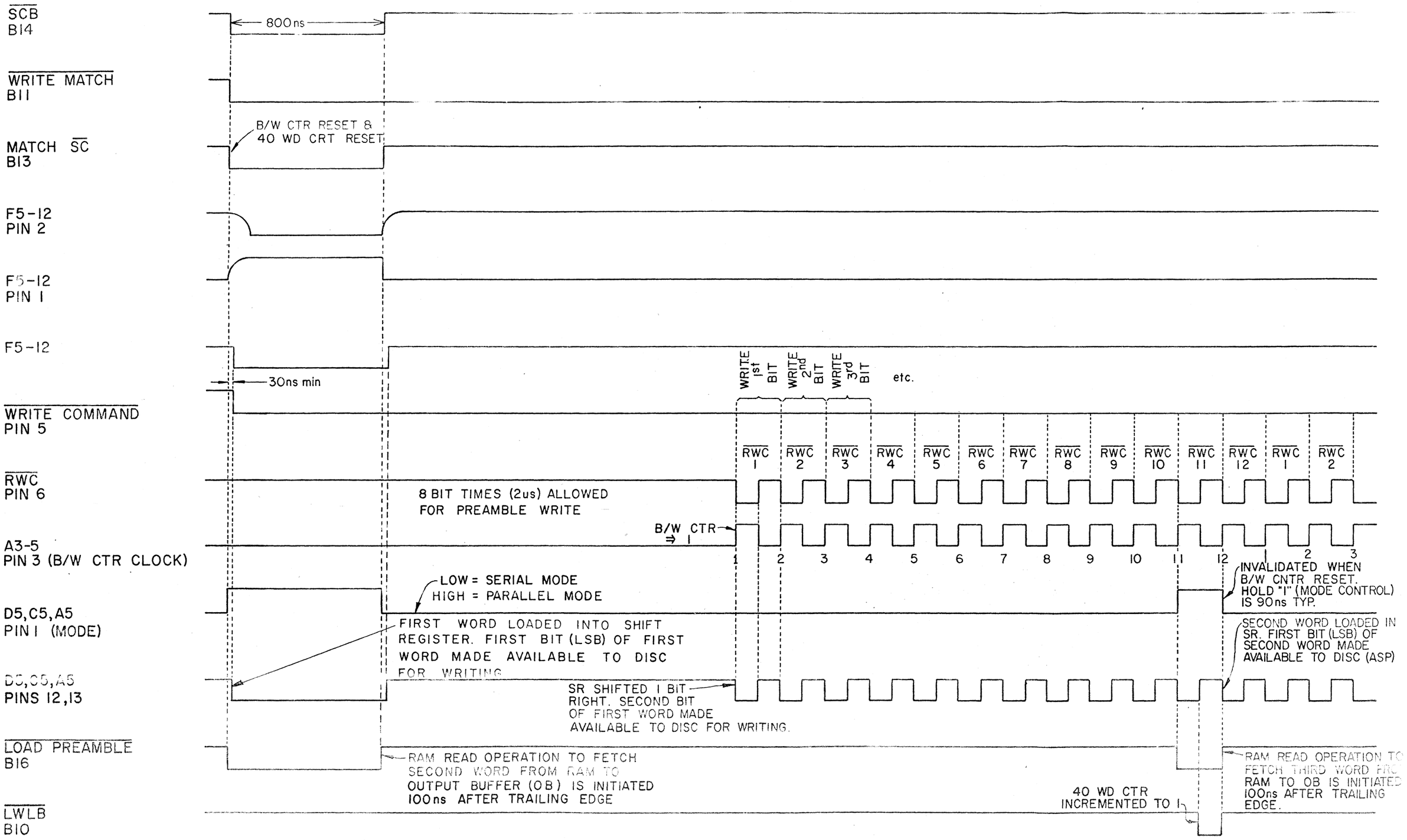


FIGURE 5
DISC DATA PCB 11255 – WRITE TIMING 125 ns/div

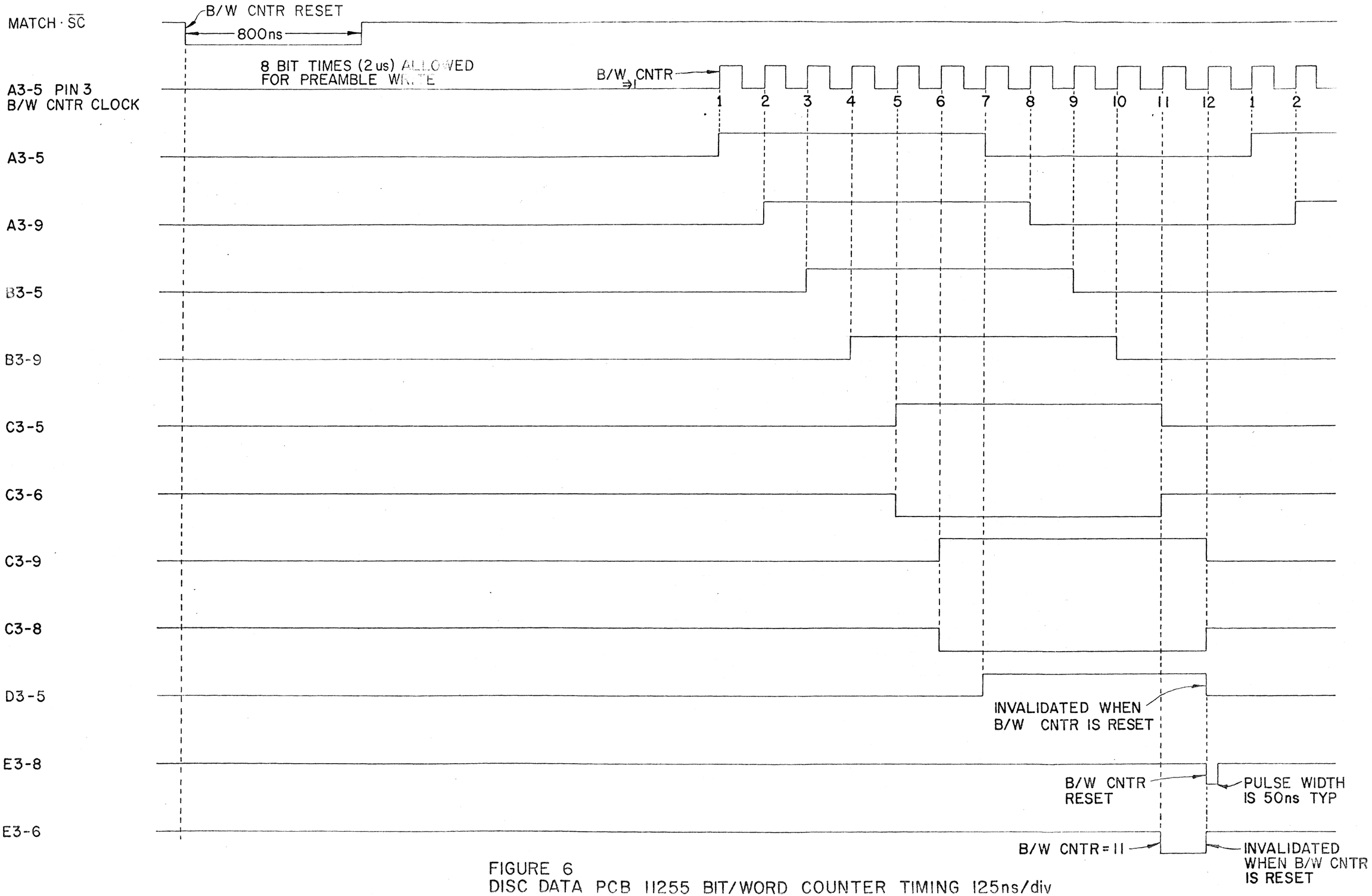


FIGURE 6
DISC DATA PCB 11255 BIT/WORD COUNTER TIMING 125ns/div

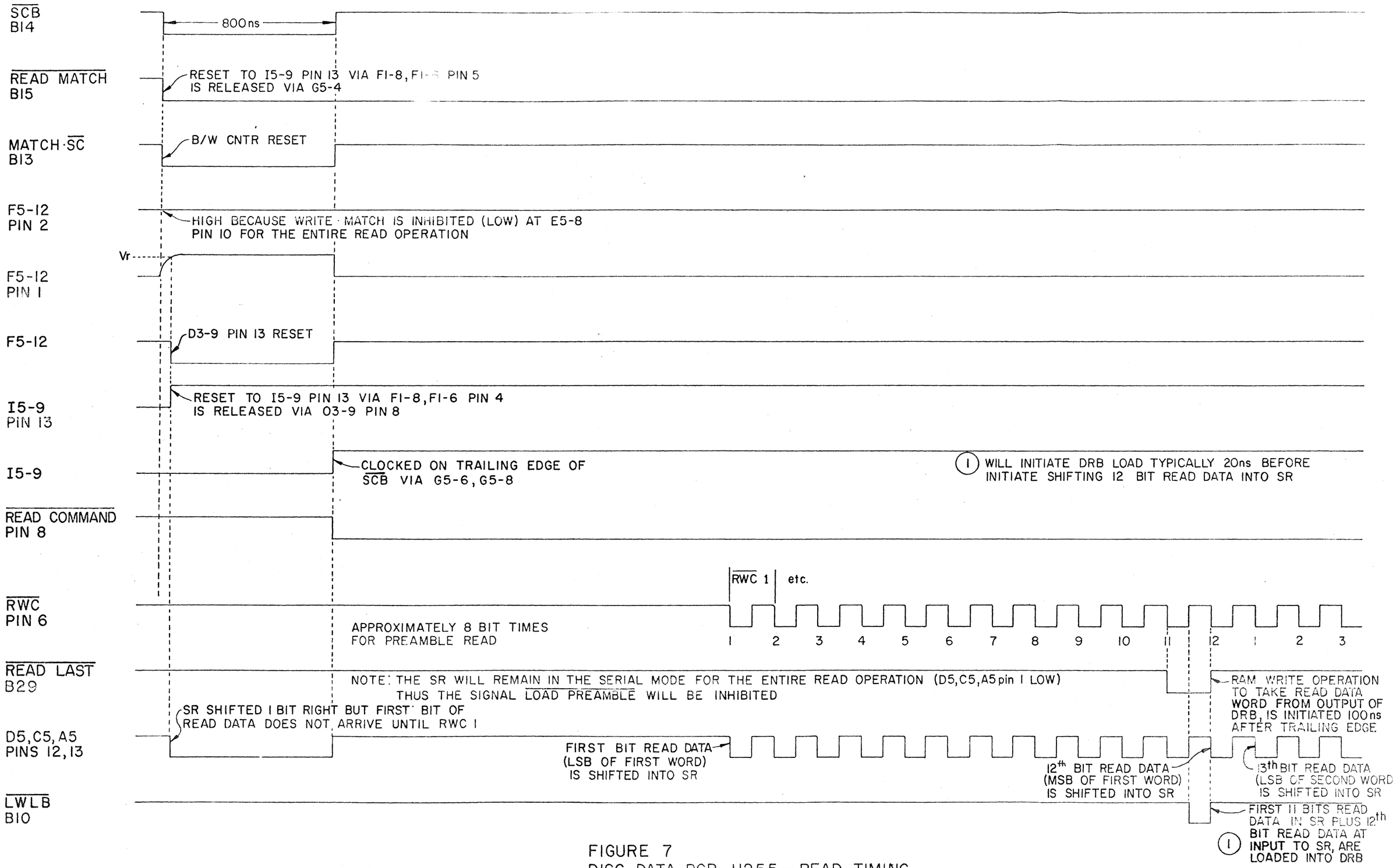


FIGURE 7
DISC DATA PCB 11255 – READ TIMING

NOTE
DIFFERENTIAL RECEIVERS AND DRIVERS INVERT THE SIGNAL IF THE + AND - LEADS ARE INTERCHANGED. THE FOLLOWING GATES HAVE MADE USE OF THIS:

B2 - 12, 13

40 WORD COUNTER

40 WD

DISC BRK REQ

DISC CONT BUSY

SECTOR CLK

SECT MATCH

SECTOR STATUS

SECTOR ADDRESS

TRACK ADDRESS

DUAL LINE RCVRS

DUAL LINE DRIVERS

TRACK SELECT (DISC)

DISC SELECT (DISC)

NOTE
UNLESS OTHERWISE SPECIFIED:
-RESISTORS ARE 62Ω ¼W
-RESISTORS OHMS, ¼ WATT
-CAPACITORS: μf

CHIP CHART

	1	2	3	4	5
H	7510	7420	7430	4015	4075
G	7507	8200	7400	4016	4016
F		7420	7401	7440	7401
E					
L					
C	7507	7400	7479	7476	7400
B	7475	7402	7400	7493	8305
A					

DEV ENG RELEASE 24AUG71 MJ

rev	eco	description	date	by	chk	approved

used on	drawn ECIC
scale	date 24 AUG 71
unless specified	design apprvl
.00 = ±.01 .xxx = ±.005	checked
angles = ±0.30'	final apprvl
material	finish

CONSOLIDATED COMPUTER LIMITED
OTTAWA

LOGIC
CCI DISC CONTROL

sheet 1 of 1 no. C11254L rev

1 2 3 4 5

CRCC REGISTER

CRCC ERROR

BIT/WORD COUNTER

WRITE • MATCH

NOTE:
DIFFERENTIAL RECEIVERS AND DRIVERS INVERT THE SIGNAL IF THE + AND - LEADS ARE INTERCHANGED. THE FOLLOWING GATES HAVE MADE USE OF THIS:
H2 - 9
H1 - 13,12
H1 - 5,9

DISC READ BUFFER

SHIFT REGISTER

LSB

MSB

CHIP CHART

	1	2	3	4	5
I					7473
H	75110	7810?			
G	7400	7430	7402	7410	7404
F	7400	7479	7440	7440	7410
E	3005	7479	7400	7440	7420
D	3000	7479	7473	4011	4012
C	9014	7479	7479	4011	4012
B	9014	7479	7479	3011	7447
A	75110	7479	7474	4011	4012

NOTE:
UNLESS OTHERWISE SPECIFIED RESISTORS ¼ WATT

rev	eco	description	date	by	chk	approved
A	66	ENG. CHANGES, CORRECTIONS PRESENT				
Ø		DEV. ENG. RELEASE				

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: LOGIC DISC DATA

sheet 1 of ns | L112554 | rev A

GENERAL

The Magnetic Tape Transport (MTT) Controller provides the Key-Edit interface between the PDP-8/E processor and the PEC magnetic tape data storage devices. Up to four transports may be used with the controller; they may be either 7-1/2 inch reel (mini-) or 10-1/2 inch reel (maxi-) tape transports.

The MTT primarily provides the final data storage for the system, but it can also be used to read in programs or dumped data.

Refer to the PEC manuals for more detailed information.

BRIEF DESCRIPTION

The controller accomodates either 7- or 9-track magnetic tapes with 200, 556, or 800 bpi density, at speeds of 25 or 12.5 ips in an NRZI format: the 200 bpi density is available only on the maxi-tape units. (A 1600 bpi density is available as an option.) The sequential access time is approximately 50 ms.

The electrical requirements are 117 or 230 vac, 48 to 400 hz; the operating temperature range is 35.5 to 123F (2 to 50C).

The maxi-transport is fitted with a dual gap head. The read and write heads are separated by 0.15 inch, which enables simultaneous read after write operations to be performed for vertical, longitudinal, and cyclic redundancy check purposes. (These checks are also performed on read operations.) An adjacent erase head is automatically activated during write operations.

Illuminating push-switch controls are mounted on the front panel. The three control pcbs are mounted beneath the deck and are accessible by sliding the transport out from the cabinet.

A Tape Adapter must be used when more than one MTT is employed in a system. Where only one MTT is used a cable connects the logic rack interface pcbs (locations B24, B25, B26) and the MTT. Where more than one MTT is used the pcbs are connected to the adapter, which in turn provides outlets for cables to each MTT (refer Figure 6-2-1).

Logic signal levels for the MTT are approximately:

true (low) , 0 to 0.4v
false (high), 3v

CONTROLLER DESCRIPTION

The controller comprises three dedicated pcbs, some ancilary pcbs devoted to drum-to-MTT data transfer controls, and the interconnecting cables.

The basic pcbs are:

1. MTT Control, pcb 10285
2. MTT Data, 7-Track, pcb 10366
   or 9-Track, pcb 10365
3. MTT Readcheck and Status, 7-Track, pcb 10368
   or 9-Track, pcb 10246

These pcbs are located in the Key-Edit logic rack, locations B25, B24, and B26 respectively.

The ancillary pcbs are:

1. Drum and MTT IOT Generator, pcb 10298
2. Word Count and Current Address, pcb 10442

These pcbs are located in the logic rack locations A21 and A29 respectively; their operation is described in this Section.

BRIEF OPERATING THEORY

The controller provides the following functions:

1. MTT motion and timing control
2. MTT to CPU data transfer control
3. MTT read, and read after write, error detection.

Refer Figure 5-1. The CPU initiates commands to the control pcb which then generates status and control information to the readcheck circuitry and the MTT respectively. The status information is returned to the CPU, and the MTT issues a read strobe to the control pcb and data to the CPU via the data pcb. The control pcb generates Read Clocks for the data pcb, and the data pcb provides the parity checks.

Figures 5-2 and 5-3 illustrate the Read and Write Data flow and 5-4 and 5-5 the cycle timing.

LEVEL 3 IOT INSTRUCTIONS

6521 Select Tape Drive.

AC 08 - Transport 1
09 - 2
10 - 3
11 - 4

6531 Skip if Tape Done flag is false.

6532 Clear Tape Done flag and control and stop tape. This instruction clears the following status bits:

AC 01 Lateral parity
AC 02 Longitudinal parity
AC 03 Illegal command
AC 07 Record too long
AC 08 Record too short
AC 09 EOF
AC 10 Tape control busy
AC 11 CRCC error

6534 Set Tape Done flag and cause an interrupt if interrupt facility is on.

6541 Clear Accumulator.

Read magnetic tape status and control status

1. AC 00 Transport Not Ready

   Set status - off-line or power off.
   Clear - on-line and power on.

2. AC 01 Lateral Parity

   Set status - Vertical Parity Error detected.
   Clear - 6532

3. AC 02 Longitudinal Parity

   Set status - Longitudinal Parity Error detected.
   Clear - 6532

4. AC 03 Illegal Command

   (Sets Tape Done flag if motion is commanded)
   Set Status - Issue Write Command with no write ring present.
   - Issue 6542, 6552, or 6551 when Busy status is already up.
   - Tape improperly selected.
   Clear 6532

5. AC 04 No Write Ring

   Set status - Write enable ring not present.
   Clear - Write enable ring present.

6. AC 05 EOT Tab Sensed

   Set status - Set and held when leading edge of EOT tab is sensed.
   Clear - Issue Rewind command or sense leading edge of EOT tab during reverse motion.

7. AC 06 BOT Tab Sensed

Set status - Sense BOT
Clear - BOT tab clear of detector

8. AC 07 Record Longer than Word Count

Set status - Word count expired before IRG is found during read forward.
Clear - 6532

9. AC 08 Record Shorter than Word Count

Set status - IRG encountered before word count has expired during forward read.
Clear - 6532

10. AC 09 EOF Detected

Set status - A one frame record of 17_8 on forward read only.
Clear - 6532 unconditionally

11. AC 10 Tape Control Busy

Set status - 6551
Clear - Stop tape motion, or 6532

12. AC 11 CRCC Error

Set status - CRCC error detected
Clear - 6532

6542 Load Command and Clear Accumulator.

The appropriate bits are loaded into the accumulator and then IOT 6542 is issued.

AC 00 1 Write
0 Read

AC 01 1 Forward motion
0 Reverse motion

AC 02 1 Write long gap

AC 03 1 Write EOF

AC 04 1 Rewind to BOT

AC 05 1 Rewind to BOT and go Off-Line

6551 Load Word Count, Clear Accumulator, and Start motion.

AC 00 to AC 11 contains the two's complement of the word count.

6552 Load Current Address (buffer address) and Clear Accumulator.

AC 00 to AC 11 contains the buffer address.

6554 Load Extended Current Address from AC bits 06, 07, and 08 and Clear Accumulator.

The MTT Control (PEC) pcb provides the timing and start/stop commands for the MTT.

START PROCEDURES

The operation is defined by six of the D flops at the bottom left of the diagram; I4-5, I4-9, I5-5, I5-9, H5-5, H5-9. These command flops are initially set by the accumulator bits BAC 00 to BAC 05, and IOT 6542.

IOT 6551, at connector pin B33 (left side), starts the MTT when the flops are set. Whenever a Write command is issued the Write flop, I5-9, $\overline{Q}$ automatically sets the Forward flop (I4-5) to ensure write routines are done in the forward motion. Similarly Write Long Gap (WLG) or Write End of File (WEOF) commands set either H5-5 or H5-9 to set the Write flop (I5-9) via G5-3 and G5-6, and consequently set the Forward flop.

The five flops - Rewind, Rewind and Off Line, Write, WLG, and WEOF - are reset simultaneously when either IOT 6532 or B Run, at connector pins B18 and B19, are applied to IOR gate F5-3, whose output is inverted by B2-6 to reset the Done flop, F4-5. The inverted output also provides one input to IOR gate F5-6 pin 5, whose output is then inverted to reset the five command flops.

Two adjacent flops, H4-5 and H4-9, control the stop circuitry. H4-5 is set by the first Read Clock, from connector pin 8, and enables the D input to flop H4-9. After the block of data has been read by the data pcb a 1 to Stop signal is received, via connector pin B11, to set the Stop flop and initiate shutdown procedures.

The commands requested by the six command flops are effected when a start motion signal, IOT 6551, is applied to connector pin B33. The Motion and Write Enable flops, F2-5 and H2-5, will set providing an illegal status does not exist.

The Illegal flop, F2-9, will set and an illegal status will exist if any of the following conditions occur:

1. IOT 6551, IOT 6552, or IOT $\overline{6542}$ is issued when the MTT is busy; the flop D input will be high from D1-11 and D1-8.
2. A Write Select command is issued with no write ring present; the flop D input will be high from D1-11, D1-6, D1-3, and G3-8.
3. The MTT had not been selected properly; the flop D input will be high from D1-11, D1-6, D1-3, and connector pin B42 (Set Illegal).

When the Illegal flop D input is high the output of inverter B1-2 will be low. This output is applied (wired OR) with G1-10, G2-11, and G2-3, to the Motion flop, H2-5, to prevent motion.

The Illegal flop is normally set by IOT 6551. When the flop sets F2-9 goes high, appears as an Illegal signal at connector pin B31, and sets the Done flop, F4-9.

EOT DETECTION AND RESET

The EOT flop, H2-9, is set via G2-8 pin 9, and G1-4 from connector pin A; G2-8 pin 10 is only enabled when Forward motion is selected. The EOT flop will set when Forward and EOT signals are present on G2-8 pins 10 and 9. NAND gate G2-6 pin 5 senses the EOT signal, pin 4 senses the Reverse motion condition and the gate resets the EOT via H1-13. When the leading edge (first edge encountered on Forward motion) of the EOT tab has been sensed G2-6 will go low, and a pulse will be generated at H1-13 to clock the flop; the D input is ground, therefore the flop will reset.

The Rewind pulse at connector pin S is applied directly to reset the flop at H2-9 pin 13. Thus, the EOT flop can only be reset by a backspace over the EOT tab, or by a Rewind command.

WRITE SEQUENCE

The Write flop is set by IOT 6542 and the appropriate AC bit. The Motion flop is set by IOT 6551 if no illegal conditions exist; the flop Q output and Ready input from connector pin C, inverted by G1-8, enable NAND gate F1-11. The gate pulls down the $\overline{\text{Tape Run}}$ line at connector pin B35 to transfer the Motion command to the data pcb. The Motion Flop $\overline{Q}$ output is routed via IOR gate G4-6 to indicate a Busy condition to the Readcheck and Status pcb via connector pin B14.

When the Forward flop sets the Forward command from the Q output is issued to the MTT via NAND gate C1-11 and connector pin T.

The Write Enable flop, H2-5, also sets and activates the MTT tape write drivers via NAND gate F1-10 pin 9 and connector pin J, Write Permit.

The $\overline{\text{Tape Run}}$ signal at F1-11 is inverted by B1-4 and applied as a high level to NAND gates C1-11 pin 13 and C1-3 pin 1, which provide the FWD and RVS signals at connector pins R and T. B1-4 also releases the Read flop, C3-5 (top), enables it (at C3-2), and enables NAND gate G4-11 pin 13. C3-5 pin 6 is high, therefore G4-11 goes low to IOR gate G4-8 pin 10. G4-8 output will go high to remove the reset condition from the adjacent Motion Oscillator B3 flops; the output is also inverted by A5-12 to remove the reset from Scalers C4, B4, D4, and E4.

The Motion Oscillator 511.57 khz output is divided by the B3 flops and the Scalers. When Scaler D4-11 goes high, after approximately 16 ms, NAND gate D5-12 pin 13 will go high. WEOF and WLG conditions are non-existent on D5-12 pin 1 and the BOT signal at connector pin B41 has not set the Read Inhibit R-S flop, D3-8 and D3-11, whose output is applied to D5-12 pin 2. Thus the gate is enabled and its output will go low. D5-8 will then go high and set the Read flop, causing C3-5 pin 6 to go low. NAND gate G4-11 will be disabled and consequently inhibit both the Motion Oscillator and the Scaler. Inverter A5-2 output will also go high from the Read flop set and release the Data Oscillator flop, C3-9, which permits the division of the oscillator output. The flop output activates the data pcb via connector pin B40.

Simultaneously the Gated Read Clock pulse is applied through connector pin F (top left) and inverter H1-4 to clock the D flop H3-5. The flop will only set if the D input is high as a result of a read data parity error signal from the Read Check pcb via connector pin B24. Two concurrent clocks and a parity error are necessary before a parity error is issued to the flop (because the last character from the LRCC could contain a parity error).

The data pcb presents $\overline{\text{1 to Break}}$ pulses at connector pin B35 (lower right). The trailing edge of the ground true pulses (going high) set the MTT Break flop C2-9; $\overline{Q}$ issues an MTT $\overline{\text{Break Request}}$ signal, via connector pin B36, to the multiplexor to request more data from the CPU.

During a Write sequence the data must be held ready for transfer in the data pcb. The MTT Break flop is set via NAND gate D2-8, providing:

the MTT Write Select is a 1 at D2-8 pin 10,

IOT 6551 is present on D2-8 pin 9,

the WLG or WEOF command does not exist on D2-8 pin 11.

The break requests are inhibited because they are only required during Read or Write Forward sequences. The 8-input IOR gate E2-8 provides the inhibiting function for all other conditions (WLG, WEOF, Reverse, Stop, Break Requests, MTT Address Accepted).

The Data Permit flop, C2-5, issues a $\overline{\text{Write Data}}$ signal to inform the data pcb, via connector pin B33, when to transmit data. R-S flop F3-6, F3-8 sets when the word count overflow occurs; F3-8 will go low via E2-8 to the Data Permit flop, C2-5 pin 2. Thus the next $\overline{\text{1 to Break}}$ pulse resets the Data Permit flop.

SHUTDOWN PROCEDURE

When the data pcb detects or writes blanks it issues a 1 to Stop pulse to the control pcb via connector pin B11 (bottom centre) to set the Stop flop, H4-9. The Read Sync flop, H4-5, is true, therefore the Stop flop will set and commence shutdown procedures.

The Stop flop $\overline{Q}$ output will go low to IOR gates G4-8 pin 9 and G4-6 pin 5. G4-6 applies a Busy condition to the Readcheck and Status pcb via connector pin B14. G4-8 enables the Motion Oscillator flops, which permit scaling until D4 pins 12 and 11 go high to enable NAND G4-3, after 18 ms with 7-track application. G4-3 will go low to IOR gate E5-11 pin 13; pin 11 will go high to E5-6 pin 4; pin 5 is enabled by the Stop flop set. Therefore pin 6 goes low to IOR gate F3-3 pin 2. The gate output is inverted and applied as a low level to reset the Motion flop and stop the MTT.

The Motion Osc continues functioning until approximately 64 ms have elapsed and scaler E4-9 enables NAND gate E5-3 pin 1; pin 2 is set when the Stop flop is true. E5-3 causes F5-11 pin 12 to go low. The gate output is inverted by E3-10 and sets the Done flop, which applies an interrupt via E3-12 and connector pin B28 to the CPU to indicate completion of the data transfer. The low output from E5-3 is also applied to IOR gate F5-6 pin 4 to initiate the complete control reset where all conditions return to zero, including the Stop flop.

During a Read sequence the 8-input NAND gate B5-8 (adjacent to the Scalers) pre-empts C5-6 (activated in 4.85 ms) to determine when the tape motion stops. Normal shutdown procedures continue as described.

The Magnetic Tape Data, 7-Track, pcb controls data transfers between the CPU and a 7-track Magnetic Tape Transport. The bottom and extreme right of the logic diagram shows data control circuitry; the remainder of the diagram shows data handling circuitry.

The logic consists of the following main blocks:

1.	Data Register	B2, D2, E4, F4
2.	Data Output Drivers	B4, B5, D4, D5, E5, F5
3.	Data Receivers	E2
4.	Parity Generator and Check	C4, E1
5.	Timing Circuits and Control Circuits	I2, H2
6.	End of File Detection	C2, G4, H4, E3

WRITE DATA SEQUENCE

When the MTT control pcb, 10285, starts motion of the tape transport, it issues a $\overline{\text{Tape Run}}$ signal to the data pcb, connector pin B5. This signal is inverted and enables gate I5-6; it is also applied to I5-3 pin 2. The output of I5-3 resets scaler I2 and is inverted and applied to I3-11 pin 12. I3-1 output resets scaler H2. $\overline{\text{Tape Run}}$ inverted is also used to reset flip-flops H4-5 and F2-9.

Immediately after motion has started the control pcb issues an $\overline{\text{MTT Break Request}}$ to fetch the first character to be written on tape from the CPU. The CPU responds by sending an $\overline{\text{MTT Address Accepted}}$ signal to the data pcb at connector pin B9, and to the control pcb to reset the BRK REQ flip-flop. The $\overline{\text{MTT Address Accepted}}$ signal is inverted by H3-3 and is gated with Write Select, from connector pin B12, by G3-8 to reset the Data Register – B2, D2, F4, E4. The CPU then applies an $\overline{\text{MB Out to MTT Buffer}}$ signal to connector pin B23. The signal is inverted by G2-3 to enable NAND gates F3, D3, and B3. This allows the data from the CPU, available on BMB 00 to BMB 11 lines at connector pin group B18 to B26, to pass through these gates and direct set the Data Register. As soon as the register has been loaded its outputs apply the data to the Data Output Driver NAND gates, where it waits to be strobed out to the MTT.

When writing on 7-track tape, a 12-bit word must be divided into two 6-bit bytes. This means that for every 12-bit word of data, there are actually two 6-bit words written on tape. This leaves one track on the tape for the parity bit.

When tape motion is started flop H4-5 is reset by $\overline{\text{Tape Run}}$ via I3-8. The flop $\overline{Q}$ output enables gates H5-3 and I4-12. I4-12 is also enabled by a Write Select and $\overline{\text{WLG+WEOF}}$. Therefore the output of I4-12 is true (low). This is inverted by I3-3 to enable output drivers F5-4, E5-4, D5-4 and 10, and D4-4 and 10.

When the tape reaches speed the control pcb sends (Data) Clock pulses to the data pcb, connector pin B3. These pulses are applied to I5-6 pin 5. I5 was previously enabled by $\overline{\text{Tape Run}}$. The gate output, I5-6, drives the clock input of scaler I2, which divides the clock pulses by a factor of 16. The scaler output is shaped to a pulse by an RC network and gated with Write Select at H3-11. The output of H3-11 is inverted and applied to G3-6 pins 4 and 5. G3-6 has been enabled by the $\overline{\text{Write Data}}$ signal from the control pcb via connector pin B8 and gate G2-8. The output of G3-6 is the Write Clock, which, via I5-11, H5-6, H4-6, and I4-12, strobes the six most significant bits of data out to the MTT via the enabled output drivers. The Write Clock also resets scaler H2 via I3-11, and clocks flop H4-5 via I5-11 and H5-6. Flop H4-5 then toggles, thus disabling gates H5-3 and I4-12, and enabling gates H5-11 and I4-8. This disables the six most significant output drivers and enables the six least significant, i.e., gates F5-10, E5-10, B5-4 and 10, and B4-4 and 10. Scaler I2 continues to scale until a second Write Clock is produced as described previously. This Write Clock strobes the second byte of data out to the MTT, and is also applied to H5-8 pin 10 via I5-11. The output of H5-8 is the $\overline{\text{1 to BRK}}$ pulse which is applied to the control pcb to initiate a second Break Request. The second Write Clock is also used to toggle flop H4-5 again to disable the six least significant drivers and re-enable the six most significant drivers.

NOTE: The propagation delay through H5-6 and H4-5 is slow enough that H4-5 will not change states until a $\overline{\text{1 to BRK}}$ pulse has been produced by H5-8.

Each successive word of data is written as described above until the complete record has been written. The controller then writes LRCC on the tape then stops the tape motion.

WRITE LRCC

After the last byte has been written on tape the control pcb cancels the $\overline{\text{Write Data}}$ signal at connector pin B to disable gate G3-6 via G2-8, thus eliminating any further Write Clocks. Because there are no Write Clocks to reset scaler H2 it is allowed to continue scaling: H2-8 and I2-11 will then go hgih simultaneously. Consequently the output of H3-6 will go low, sending a Write Reset signal to the MTT via connector pin F. Write Reset automatically writes LRCC on the tape.

STOP SEQUENCE

H2 continues to scale until its last stage, H2-11, goes high. This is the 1 to Stop signal, and it is sent to the control pcb via connector pin B7 to stop the tape motion.

WRITE LONG GAP

The control pcb issues a $\overline{\text{WLG+WEOF}}$ signal to the data pcb via connector pin B6 to write a long gap on tape. This disables I4-8 and I4-12, thus disabling the data output drivers so that nothing can be written on the tape. The control pcb starts tape motion but does not issue any (Data) Clocks until the long gap has been written. After it has been written, clock pulses are sent to the data pcb and I2 and H2 begin to scale. During a Write Long Gap, $\overline{\text{Write Data}}$ is false (high) and WEOF is false (low) to disable G2-8 via G2-11. The output of G2-8 disables G3-6 to prevent the production of Write Clocks.

When the scalers have scaled to the end, so that H2-11 goes high, a 1 to Stop is issued to stop the tape motion.

PARITY GENERATION AND CHECKING

Parity is generated by the parity tree C4-8 (top left). It senses the Write Data lines and produces the correct parity bit for each byte of data applied to its inputs. C4-8 pin 12 can generate either even (high) or odd (low) parity.

Parity is checked by the parity tree D1-8. It operates in the same manner as the generator, but it senses the data from the MTT Read Data Lines. If it detects a parity error the signal, Parity Error, is applied to the control pcb via connector pin B24 for processing.

By definition the EOF code (17) must always be even parity. Therefore, the choice of odd parity is controlled by the signal $\overline{\text{WLG+WEOF}}$. For a normal data write sequence $\overline{\text{WLG+WEOF}}$ is high at connector pin B6, forcing I5-8 low, and C4-8 pin 12 and D1 pin 12 low. This sets the pcb to generate and check for odd parity. When writing an end of file, $\overline{\text{WLG+WEOF}}$ is low, causing C4-8 pin 12 and D1 pin 12 to generate and check for even parity. (This forcing of even parity prevents the detection of false parity errors when the EOF is read after a write operation. The PEC MTT is a Read after Write model.) When an EOF is detected during a read operation it is accompanied by a parity error if the data pcb is set to operate in odd parity.

WRITE END OF FILE

The control pcb issues two signals to the data pcb - WEOF and $\overline{\text{WLG+WEOF}}$ - to write a File Mark on tape. $\overline{\text{WLG+WEOF}}$ at connector pin B6 disables the data output drivers in the same manner as it does when writing a Long Gap. It also conditions the output data lines with the EOF code 17 via I5-8 and the C3 inverters (top left).

The WEOF signal at connector pin B15 releases the reset of flop F2-5, places a high level on the D input and enables gate G2-11 at pin 13. The control pcb sends clock pulses to the data pcb and I2 and H2 begin to scale. When the first Write Clock is produced at G3-6 it strobes the EOF level via I5-11, H5-6, H4-5, H5-11 and H4-9, out to the MTT at connector pin B14. The clock trailing edge clocks and sets flop F2-5. The $\overline{Q}$ output of F2-5 goes low, causing the output of G2-11 to go false (high) to disable G3-6 via G2-8 and prevent any further Write Clocks being issued.

I2 and H2 continue to scale to produce a Write Reset at connector pin F to put LRCC on tape and to produce a 1 to Stop to initiate a normal stop sequence.

READ DATA SEQUENCE

The control pcb starts tape motion and applies $\overline{\text{Tape Run}}$ to the data pcb at connector pin B5. When the start sequence has finished, the control pcb begins sending (Data) Clock pulses to the data pcb via connector pin B3. The MTT reads the first character on tape and applies it to the data pcb via a cable to the Read Data inputs at pin group N to A. The parity checker senses the data and checks for a parity error. The data is received by the E2 inverters and applied to the D inputs of the Data Register. The MTT also sends a Read Clock signal to the control pcb, which then applies a $\overline{\text{Read Clock}}$ level to the data pcb at connector pin B4.

$\overline{\text{RD RCL}}$ resets the scalers I2 and H2 via I5-3 and is applied to gates H5-3 and H5-11 via inverter G2-6. H5-3 is enabled at pin 2 by flop H4-5 $\overline{Q}$. Therefore the data is clocked into the most significant byte of the data register by the $\overline{\text{RD RCL}}$ via H5-3 and inverter G5-6. $\overline{\text{RD RCL}}$ also clocks flop H4-5 via I5-11 and H5-6. This causes H4-5 to set and enable gates H5-11 and H5-8. When the second character on tape is applied to the inputs of the Data Register, the $\overline{\text{RD RCL}}$ clocks the data into the least significant byte of the register and toggles H4-5 back to the reset condition to receive the next character from tape. Two 6-bit bytes from the tape have then been assembled into one 12-bit word in the Data Register and applied to the Output Drivers. The second $\overline{\text{RD RCL}}$ also clocks H5-8 to produce a 1 to BRK signal which is applied to the control pcb to initiate an $\overline{\text{MTT BRK REQ}}$ to the multiplexor. The multiplexor responds by sending a Data In pulse to the data pcb via connector pin B16, which then strobes the data out to the CPU via the Output Drivers.

RD RCL pulses to the data pcb terminate when the entire record has been read. I2 and H2 are allowed to scale through to the end to produce a 1 to Stop signal, at connector pin B7, which then initiates a normal stop sequence.

READ LONG GAP

When the controller begins a normal read sequence and no Read Clocks are applied to the control pcb, $\overline{\text{RD RCL}}$ pulses to the data pcb are inhibited. The absence of $\overline{\text{RD RCLs}}$ allows I2 and H2 to scale to the end and initiate a normal stop sequence.

READ EOF

The EOF code is recognized by gates C2-8 and E3-6. The inputs of C2-8 and E3-6 will all be true when the code 1717 has been assembled in the Data Register, causing their outputs to be true. These are inverted by G4-3 and E3-8 and applied to G4-6, causing its output to be treu to the D-input of flop H4-9.

When the $\overline{\text{RD RCL}}$ pulse clocks the least significant byte into the Data Register, via H5-11 and G5-8, H5-11 also clocks flops H4-9 and F2-9. This causes F2-9 to set and if the EOF code is present H4-9 will reset. The $\overline{Q}$ output of H4-9 goes high to send the EOF signal to the readcheck pcb.

The Q output of F2-9 enables gate G4-8. If another $\overline{\text{RD RCL}}$ arrives indicating that the EOF just detected was not a true EOF, then the output of G4-8 will go low (true) and set flop H4-9 to remove the EOF signal from the readcheck pcb.

The Magnetic Tape Data, 9-Track, pcb controls data transfers between the CPU and 9-track Magnetic Tape Transport. The lower portion of the logic diagram shows data control circuitry and the upper portion shows data handling circuitry.

The logic consists of the following main blocks:

1.	Data register	E2, E3
2.	CRCC register	C2-9, C3, C4
3.	CRCC Drivers	A3, B2-13, B3
4.	Data Drivers and Receivers	C1-6, C1-7, F2, A5, B5, A4, B2-1, B4
5.	Timing Circuits	I4, I5
6.	Parity Generator and Check	F4, F3
7.	End of File Detection	H3, H4

WRITE DATA SEQUENCE

When the MTT control pcb starts motion of the MTT it issues a $\overline{\text{Tape Run}}$ signal to the data pcb, connector pin B5. The signal is inverted and applied to gate I3-3 pin 2, it also enables gate I3-11 at pin 13. The output of I3-3 resets Timing Scaler I4 and is also inverted and applied to I3-6 pin 4, whose output resets scaler I5.

Immediately after motion has started, the control pcb issues an MTT Break Request to fetch from the CPU the first character to be written on tape. The CPU responds with an MTT Address Accepted signal which is applied to the control pcb to reset the Break Request flip-flop, and to connector pin B9 of the data pcb where it is applied to IOR gate H2-3 pin 1. The output of H2-3 is gated with Write Select, from connector pin B12, at F1-6 to reset the Data Register flip-flops. The CPU then applies an MB Out to MTT Data signal, to connector pin B23, which is inverted and gated with Write Select at H1-8. The output of H1-8 is inverted and used to enable NAND gates E4 and C5 to allow the data available on BMB 4 to BMB 11, connector group B28 to B26, to direct set the Data Register.

When the Data Register is loaded its outputs apply the data to the CRCC Generator Circuit, the Parity Generator circuit F4, and the Output Driver NAND gates A4 and B4. The parity bit generated by F4-8 is applied to the Parity Driver, B2-1 pin 3. The Output Drivers and the Parity Driver – A4, B4, B2-1 – are enabled by the $\overline{\text{Write Data}}$ signal from connector pin B8. The signal is routed via IOR gate H2-11 and applied to NAND gate H2-8 with the inverted WEOF signal from connector pin B15. Thus the driver gates have the complete data word available at their outputs.

When the tape reaches speed the control pcb sends (Data) Clock pulses to the data pcb connector pin B3. These pulses are applied to I3-11 pin 12, which was enabled by $\overline{\text{Tape Run}}$. The output of I3-11 drives the clock input of scaler I4. The scaler divides the clock pulses by a factor of 16 and this output is used to trigger the Monostable, I1. The 3 µs pulse output is gated with the Write Select, from connector pin B12, by H2-11 whose output is inverted and gated by I3-8 with the Write Data signal from H2-11. The output of I3-8 is applied to G5-6 pin 5, I3-6 pin 5, and H1-6 pin 5 to produce the 1 the Break signal at connector pin B11.

The output of G5-6 is gated by G5-8 with the $\overline{Q}$ output of flip-flop G2; G2 is held in the reset state except during a WLG or WEOF condition. Thus G5-8 is enabled and produces a $\overline{\text{Write Clock}}$ signal at connector pin J. The signal strobes the data available at the outputs of the driver gates – A4, B4, and B2-1 – into the MTT data electronics via the cable connected at pin group X to D (top left).

The output of I3-6 is used to reset scaler I5 every time the monostable, I1, initiates a $\overline{\text{Write Clock}}$ during a normal write data sequence.

The next word of data is requested by the trailing edge of the 1 to BRK signal, at connector pin B11, which sets the BRK REQ flip-flop on the control pcb. The 1 to BRK signal is produced at the same time as the Write Clock signal. The circuit then operates as previously described for each successive break request until the complete record has been written. The controller then writes LRCC and CRCC on the tape, then stops the tape motion.

WRITE CRCC

When the last Address Accepted pulse comes from the computer an MTT WC Overflow pulse is issued by the WC and CA pcb, 10442, to the MTT control pcb to inhibit any further Break Requests from the MTT. When the data pcb issues the 1 to BRK pulse, which corresponds to the last Write Clock, the control pcb cancels the Write Data signal so that connector pin B8 goes high. This inhibits I3-8 via H2-11 and prevents the 3 µs pulse produced by I1 from enabling gate I3-8; thus any further 1 to BRK signals and the reset of scaler I5 are inhibited; I5 continues to scale.

Because Write Data is high, G3-6 pin 6 will be high to enable gates G4-6 and H2-6; F5-1 pin 2 will also be high and prevent clocking of the CRCC Register.

When scaler I4-11 goes low, I5-12 will go high and enable G4-6. When I4-11 next goes high, the monostable will produce a 3 µs pulse to be gated with Write Select by H1-11, inverted by G3-2 and applied to G4-6 pin 3. The output of G4-6 is then applied to H2-3 pin 2 whose output is gated by F1-6 with Write Select from connector pin B12 to reset the Data Register.

When scaler I5-8 goes high, four character times after the last data word was written, H2-6 output will go low and H5-12 pin 2 will be enabled. The low signal at the output of H2-6 is inverted by B1-9 and enables the CRCC Driver gates A3, B3, and B2-13. The CRC character available at the CRCC Register flop outputs is then applied, via the inverters B1 and C1 and the output drivers, to the write data lines to the MTT.

While I5-8 is still high I4-11 will go high, causing the monostable to produce a pulse which is applied to H5-12 pin 13 via H1-11 and G3-2. H5-12 pin 12 will go low, causing G5-6 to go high. This high is applied to G5-8 pin 9, which is enabled by G2-5 pin 6, and a Write Clock is produced at connector pin J to write the CRC character on tape.

When the 3 µs pulse terminates H5-12 pin 12 will return to the high state and clock the flip-flop G2-5. G2-5 pin 6 will go low and disable gate G5-8, thus inhibiting any further Write Clocks.

WRITE LRCC

Scaler I5-11 will go high four character times after I5-8 goes high, or four character times after CRCC was written on tape. When I5-11 goes high, G5-3 pin 3 will go low to send a Write Reset signal to the MTT via connector pin F. The signal resets the Write amplifiers and the MTT automatically writes the correct LRC character on tape.

STOP SEQUENCE

When I5-11 goes low again the output of adder D4 will go high and clock flip-flop I2-9 to set the flip-flop, which then sends a 1 to Stop signal to the control pcb via connector pin B7 in initiate the stop sequence.

Flip-flop G2-5 will be reset to allow Write Clock pulses when the control pcb removes the Write Select signal.

WRITE LONG GAP

To write a long gap on tape the control pcb issues a WLG+WEOF signal to the data pcb via connector pin B6. This low signal is applied to G5-11 pin 12 and H5-12 pin 1. G5-11 will be high, forcing E5-8 pin 8 low to hold the CRCC Register reset for the time the long gap is being written. G5-11 pin 11 will also force E5-6 pin 6 low to hold the EOF detection flip-flops (H3 and H4) reset while writing a long gap. WLG+WEOF also holds the output of H5-12 high. This prevents a Write Clock from being produced through G5-6 and G5-8 when I5-8 goes high.

The control pcb inhibits clocks to the data pcb until the long gap has been written. When the clocks begin scalers I4 and I5 start to scale and tape motion is stopped by the normal Stop Sequence.

WRITE EOF

The control pcb sends a WLG+WEOF signal to the data pcb to write an EOF on tape. The WLG+WEOF signal conditions the data pcb in the same manner as it does when writing a long gap.

The WEOF signal at connector pin B15 releases the reset and conditions the D-input of flip-flop I2-5, and also enables NAND gate H1-3. Because flip-flop K2-5 is reset, pin 6 is high and H1-3 output will go low to H2-11 pin 12. The output of H2-11 enables I3-8 pin 9, and is also inverted by G3-6 and applied as a low to H2-6 pin 4 to disable the CRCC Driver gates – A3, B3, and B2-13.

WEOF is also inverted by C1-1. This low level is applied to H2-8 pin 9 to disable the Output Drivers – A4, B4, and B2-1. It is also applied to inverter E1-8 whose output is applied to inverters A2-1, A2-4, and A2-13 The outputs of these gates go low to place the EOF code 23 on the output data lines.

The control pcb inhibits clocks until a long gap has been written then issues them to the data pcb and I4 begins to scale. When I4-11 goes high the monostable I1 produces a pulse which is applied to H1-11, inverted, and applied to I3-8. The output of I3-8 clocks flip-flop I2-5 on the trailing edge. I2-5 pin 6 then goes low, forcing the output of H1-3 high. This causes H2-11 to go low and disable I3-8 to inhibit any further pulses from the monostable. The single pulse allowed to pass I3-8 enables G5-6 to produce a single Write Clock at G5-8 pin 8 and connector pin J.

This Write Clock strobes the first word of the EOF code to the MTT to be written on tape. I5 is then allowed to scale: when I5-11 goes high it enables G5-3. When I4-11 goes high it triggers the monostable which applies a pulse to G5-3 via H1-3 and G3-2. The output of G5-3 goes low and applies a Write Reset signal to the MTT via connector pin F. This Write Reset writes the second word of the EOF code on the tape.

When I5 finishes scaling and I5-11 goes low it sets flip-flop I2-9 and a normal stop sequence is initiated.

READ DATA SEQUENCE

The control pcb starts tape motion and sends the Tape Run signal to the data pcb as for the Write Data Sequence. When the start sequence is complete the control pcb sends clock pulses to the data pcb. The MTT reads the first character and sends the data to the data pcb via cable connector pin group S to K where it is received by inverters F2, C1-6, and C1-7. The inverted data is applied to the D inputs of the Data Register flip-flops and the inputs of the Parity Checker F3. The output of F3 is applied to flip-flop G2-9 pin 12. Simultaneously the MTT reads the character and sends a Read Clock signal to the control pcb and to the data pcb via cable connector pin H. The control pcb produces a Gated Read Clock which it sends to connector pin B4 of the data pcb. This signal is applied to H1-6 pin 4 to produce a 1 to BRK pulse at connector pin B11: it also applied to inverter G1-13 pin 12. The output of G1-13 is applied to inverter E1-6 whose output clocks the data into the Data Register. The Data Register outputs then apply the data to the inputs of Data Driver gates A5 and B5 to await transfer to the CPU. The Read Clock signal at connector pin H clocks the Parity flip-flop G2-9. If there is a parity error G2-9 will set and send a Read Parity signal to the control pcb, via connector pin B24, to be processed.

The $\overline{\text{1 to BRK}}$ pulse produces an $\overline{\text{MTT BRK REQ}}$ at the control pcb. This is sent to the multiplexor which responds with a Data to MB In signal at connector pin B16 to strobe the data out to the CPU via output Data Drivers A5 and B5.

When motion starts $\overline{\text{Tape Run}}$ releases scalers I4 and I5. When the start sequence has ended the control pcb sends clocks to the data pcb and I4 and I5 will scale. Each $\overline{\text{Gated Read Clock}}$ resets the scalers via I3-3, G1-1, and I3-6. When the record has been read the $\overline{\text{Gated Read Clock}}$ signals stop and I4 and I5 are allowed to scale through to initiate a normal stop sequence.

READ LONG GAP

The controller starts a normal read sequence. When no $\overline{\text{Read Clock}}$ signals reach the control pcb, no $\overline{\text{Gated Read Clock}}$ signals are produced to send to the data pcb. The absence of a $\overline{\text{Gated Read Clock}}$ for 16 word times causes the most significant bit of scaler I5 to set and produce a 1 to Stop signal. This indicates a blank detect condition to the control pcb which will then start a normal stop procedure.

READ EOF

An EOF is coded as two successive 23 octal characters. Gates F5 and G4-12, and G4-8 recognize the code of 23; G4-8 enables gate H5-6 and flip-flop H3-9 via inverter G3-9. The trailing edge of the first $\overline{\text{Gated Read Clock}}$ sets flip-flops H3-9 and H3-6. H3-9 enables H5-6 previously conditioned by G4-8 and $\overline{\text{WEOF}}$ on pins 5 and 3 respectively. H5-6 output puts a low level on the D input of H3-5. The Gated Clock leading edge clocks H4-12 to a set condition. The second $\overline{\text{Gated Read Clock}}$ toggles H4-12 to a reset condition and the Q output clocks H4-9 to a set state. Flip-flop H4-9 set condition indicates that two characters have been read. The trailing edge of the second $\overline{\text{Gated Read Clock}}$ resets H3-5. The output of H5-8 then goes low, and is inverted by G3-7, and applied to the control pcb via connector pin B14 to indicate an EOF has been received.

When H4-9 is set the $\overline{Q}$ output disables the K input of H4-12. H4-12 can now only be set, and not reset. If a third $\overline{\text{Gated Read Clock}}$ arrives it sets H4-12 and the $\overline{Q}$ output disables H5-8. This invalidates any EOF codes by removing the EOF signal. Any further clocks will have no effect.

The MTT motion stops in the normal manner.

CRCC GENERATION

The CRCC Register is originally reset so that its content is zero. The Q outputs of the CRCC Register are applied to one input of the full adders D1, D2, D3, D4, D5; the Q outputs of the Data Register are applied to another input. The Parity Generator output from F4 is applied to adder D5-9 pin 12 via F4-6 and G3-1. The outputs of the full adders are applied to the next most significant flip-flop in the CRCC Register. When the CRCC Register is clocked (at the same time as $\overline{\text{Write Clock}}$) the adders accomplish the add and shift portion of the CRCC generation. The output of adder D5-7 is fed back to an input of each of D1-9, D2-7, D2-9, and D3-7. This causes register flop Q outputs at C3-10, C3-7, C3-6, and C4-9 to be inverted if the parity bit, at flop C4-6 output, becomes a 1 when the register is shifted. Inverters B1 and C1 invert the contents of the CRCC Register, except flops C3-10 and C3-6, to write the CRC character on tape.

NOTE: A description of how CRCC is actually written on tape is contained in the Write Data Sequence portion of this description.

The 7-track MTT Readcheck and Status pcb operates in exactly the same manner as the 9-track pcb, 10246. The cyclic redundancy check character circuitry is not used on 7-track magnetic tape and is not included on this pcb.

The MTT Readcheck and Status pcb provides error detection during a read data sequence, including read after write, by enabling appropriate status bits to the CPU. Status bits are also generated to indicate to the CPU the current state of the MTT.

The pcb contains a longitudinal redundancy check character register (LRCC), the cyclic redundancy check character register (LRCC), the cyclic redundancy check character register (CRCC), and the status output gates.

LRCC

The parity bit and eight data bits are applied to the pcb via connector pin group B to L, left side. The inputs are applied via DTL receiver-inverters H1-2 to E1-6 to the J and K inputs of the LRCC register - J-K flip-flops H2-13 to A2-8. The Read Clock input to the pcb, via connector pin B32, is applied through gates A5-8, C2-6, and A1-6 to the C inputs of the register flops.

The flop resets are connected in common to power driver A3-8, which is pulsed by the output of monostable C5-6. The monostable is triggered by the Tape Run pulse at connector pin B8 and resets the register each time a Tape Run pulse occurs.

When the first data word occurs the register J-K inputs will be either high or low, depending upon whether the corresponding data bit is a 1 or 0. Any flop with a high input will toggle when a Read Clock arrives; any flop with a low input will remain in the same state. Thus a flop receiving an even number of ones will always be in the reset condition.

The number of ones on each track in NRZ magnetic tape recording is always even because of the LRCC written by the write amplifier reset strobe. Therefore if the LRCC is correct the register will be all reset at the end of each data transfer.

The $\overline{Q}$ outputs of all the J-K flops are applied to the multiple inputs of IOR gate C1-8. When a correct LRCC state exists all the $\overline{Q}$ outputs will be high, causing C1-8 to be low. This low level is applied to NAND gate J5-11 as a positive going pulse. IOT 6541 is applied to connector pin B3 at Read Status time to strobe the LRCC status to the CPU accumulator via J5-11 and connector pin B7.

During Reverse motion connector pin B9, Forward, will be high to D5-8 pin 9, which will make C2-6 pin 4 low to cause an inhibit state and prevent Read Clocks being applied to the register.

CRCC

CRCC Handling

Nine-track magnetic tapes are written with a Cyclic Redundancy Check Character (CRCC) at the end of each data block.

The CRCC is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only. When reading, it can also be used in conjunction with the VRC and LRCC checks for error correction, provided that the errors are confined to a single channel.

The character is generated in the CRCC register, which consists of nine flops, designated CP, and C0 to C7. (IBM use the designations P, parity, and 0 to 7, ie. 2^7 to 2^0).

With the register originally reset to zero the CRCC character is generated as follows (refer to the following figure and tables).

1. All data characters are added to the CRCC register without carry (each bit position n is exclusive ORed to C).
2. Between additions the CRCC register is shifted one position (CP to C0.....C7 to CP).
3. If a shift causes CP to become 1 the bits being shifted into C2, C3, C4, and C5 are inverted.
4. After the last character has been added the CRCC register content shifts again in accordance with steps 2 and 3.
5. Before writing the register contents onto tape the contents of all positions, except C2 and C4, are inverted. The parity CRCC is odd if the number of data characters within the block is even, and the parity is even if the number of characters within the block is odd. The CRCC may only contain all 0-bits if the number of data characters is odd.
6. Its value is such that the LRCC always has odd parity.

To check CRCC in a Forward command the CRCC register recalculates the CRCC. When the original CRCC is combined with the new CRCC, the result should be a match pattern of 111010111 in the CRCC register; Table 1b shows this function.

To check CRCC in a Reverse command, the significance of the data bits entering the CRCC register must be reversed; Table 1c shows this function.

The figure gives details of circuit implementation. The full adders can be used to provide the exclusive OR and inverse exclusive OR function by the setting of Ci to a 0 or a 1, for example:

ci	A	B	S	
0	0	0	0)	
0	0	1	1)	
0	1	0	1)	exclusive OR
0	1	1	0)	
1	0	0	1)	
1	0	1	0)	not exclusive
1	1	0	0)	OR/equivalence
1	1	1	1)	

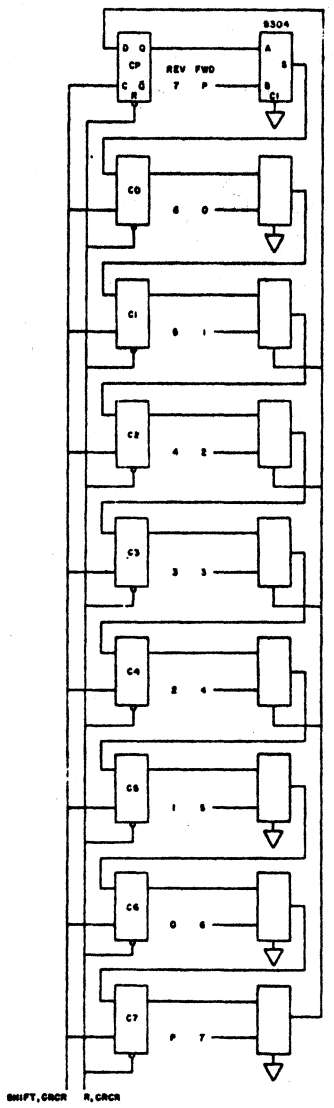


Table 1a: FORWARD CRCC GENERATION

IBM SIG		P	0	1	2	3	4	5	6	7	
BIT SIG		P	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
CP 1/P = 1		CP	C0	C1	$\overline{C2}$	$\overline{C3}$	$\overline{C4}$	$\overline{C5}$	C6	C7	
CRC TO TAPE		$\overline{CP}$	$\overline{C0}$	$\overline{C1}$	C2	$\overline{C3}$	C4	$\overline{C5}$	$\overline{C6}$	$\overline{C7}$	CRC PARITY
RESET		0	0	0	0	0	0	0	0	0	
	CHAR 1	0	0	0	0	0	0	0	0	1	
ADD. SHIFT		1	0	0	1	1	1	1	0	0	
	CRC	(0	1	1	1	0	1	0	1	1)	EVEN
	CHAR 2	0	0	0	0	0	0	0	1	0	
ADD. SHIFT		0	1	0	0	1	1	1	1	1	
	CRC	(1	0	1	0	0	1	0	0	0)	ODD
	CHAR 3	0	0	0	0	0	0	1	0	0	
ADD. SHIFT		1	0	1	1	1	0	0	0	1	
	CRC	(0	1	0	1	0	0	1	1	0)	EVEN
	CHAR 4	0	0	0	0	0	1	0	0	0	
ADD. SHIFT		1	1	0	0	0	0	0	0	0	
	CRC	0	0	1	0	1	0	1	1	1	ODD

Table 1b: FORWARD CRC CHECKING

	CHAR 4	0	0	0	0	0	1	0	0	0	
ADD. SHIFT		1	1	0	0	0	0	0	0	0	
	CRC	(0	0	1	0	1	0	1	1	1)	ODD
	CRC	0	0	1	0	1	0	1	1	1	
ADD. SHIFT		1	1	1	0	1	0	1	1	1	TEST FOR MATCH PATTERN

Table 1c: REVERSE CRC CHECKING

IBM SIG		7	6	5	4	3	2	1	0	P	
RESET		0	0	0	0	0	0	0	0	0	
	CRC	1	1	1	0	1	0	1	0	0	
ADD. SHIFT		0	1	1	1	0	1	0	1	0	
	CRC	(1	0	0	1	1	1	1	0	1)	EVEN
	CHAR 4	0	0	0	1	0	0	0	0	0	
ADD. SHIFT		0	0	1	1	0	0	1	0	1	
	CRC	(1	1	0	1	1	0	0	1	0)	ODD
	CHAR 3	0	0	1	0	0	0	0	0	0	
ADD. SHIFT		1	0	0	1	0	1	1	1	0	
	CRC	(0	1	1	1	1	1	0	0	1)	EVEN
	CHAR 2	0	1	0	0	0	0	0	0	0	
ADD. SHIFT		0	1	1	0	1	0	1	1	1	
	CRC	(1	0	0	0	0	0	0	0	0)	ODD
	CHAR 1	1	0	0	0	0	0	0	0	0	
ADD. SHIFT		1	1	1	0	1	0	1	1	1	TEST FOR MATCH PATTERN

CRCC Check

The CRCC Register consists of the nine flops I4-5 to E4-9, CP to C7. The leading edge of the Tape Run signal at connector pin B8, via monostable C5-6 and power driver A3-6, sets the register to its zero state. This ensures that the register is reset before the first data character is received at the beginning of each data block. The Q output of each register flop is applied to the A input of its associated full adder flop, I3-7 to D3-7.

When the first data word is applied from the Read Data connector pins B to L to the B inputs of the adder flops via the receiver-inverters, H1-2 to E1-6, all of the A inputs will be low (the register was reset by Tape Run). Therefore the sum output of the adders will correspond to the applied data at the B inputs (e.g. if the data applied to H3-7 pin 3 is high then pin 7 will be high).

The first data word presented to the register is 1_8, refer to the figure. This will cause the B input of adder flop D3-7 pin 3 to go high; the B input was low from E4-9 because of the initial reset from Tape Run. Consequently the sum output at D3-7 pin 7 will be high and the $\overline{\text{sum}}$ output at pin 6 will be low. Pin 6 is fed back to pin 12 (ci) of H3-10 and G3-10. Pin 7 is fed back to pin 4 (ci) of H3-7 and G3-7 to cause inversion of bits 2^5, 2^4, 2^3, and 2^2 (refer to CRCC Handling).

The CRCC Register will perform an add-shift function for every data word applied to the pcb; the final word is the CRCC as originally written on the tape. When this word is exclusive ORed to the re-generated CRCC the result is a match pattern, refer to the figure. The pattern is checked by 10-input IOR gate H5-8. The gate inputs are individually derived from the Q outputs of the CRCC Register flops. Thus when a match pattern exists in the register all of the inputs to H5-8 will be high, causing pin 8 to go low as a wired OR with inverter D5-6 to CRCC Error flop D4-5 pin 2. The wired OR ensures that the CRCC Error flop can not be set during a Reverse motion.

It is possible for the tape CRCC character to be all zeros, therefore the facility to produce a phantom strobe has been provided for use when it has been determined that the CRCC is zero data. Under normal read data conditions, including read after write, the read data strobe, Read Clock, is applied via connector pin B32 to inverter B3-8 pin 9 and IOR gate A5-8 pin 9. Therefore Read Clocks appear at A5-8 for every word read off the tape. The positive-going clock pulses at B3-8 are applied to a retriggerable 150 µs Monostable 1, B4-7 pin 4. Thus the monostable will be continuously set while Read Clocks are being received. B4-7 $\overline{Q}$ will be low to flop C3-5 pin 3 during this time, causing it to remain reset.

If the read strobe is absent from B4-7 pin 4 for more than 200 µs, i.e., four character spaces, the monostable will not be retriggered. Consequently pin 7 will go high to clock flop C3-5, which in turn triggers the 150 µs Monostable 2, B4-10 whose Q output causes the D input of flop D4-9 to go high. If the CRCC is not zero data a Read Clock pulse will arrive at D4-9 pin 11 and set the flop. The $\overline{Q}$ output is connected to the direct set and latches the flop once it is set; the $\overline{Q}$ output also inhibits NAND gate A5-11 pin 12 to inhibit the phantom strobe, generated by B4-10, to allow the normal read data condition. If the CRCC was zero data D4-9 would not set, therefore NAND gate A5-11 would be enabled and the Read Clock strobe would pass through to clock the registers.

The phantom strobe is generated by the positive to negative transition of Monostable 2. Assuming that the input to inverter A5-6, pins 4 and 5, and NOR gate B5-10 pin 9 are logic high, the output of B5-10 will be low (because of pin 9). When B4-10 goes low B5-10 pin 9 will immediately follow the change, while the input to B5-10 pin 8 is slowed by the 680 pf capacitor. Thus at some time both inputs to the NOR gate are low for a pulse period with the pulse width depending upon the capacitor.

The trailing edge of the phantom strobe circuit output pulse clocks the CRCC Error flop D4-5, via inverter A5-3; the flop is cleared by IOT $\overline{6532}$ from connector pin B2.

The flop E4-5 ensures that the Record Longer than Word Count status does not give a false indication, due to the extra CRCC strobe.

TAPE TRANSPORT SELECTION

The four Transport Select flip-flops, J3 and J4, bottom left, provide capabilities for selecting one of up to four tape transports. The select bit is presented to the D inputs and IOT 6521 is presented to the C inputs of the four flops. The appropriate flop will set and its output will be buffered and inverted by its associated inverter, J1-3, J1-4, J1-10, or J1-11, and applied to the select line of the required MTT via connector pins S, R, T, and U.

If an MTT has not been selected and an attempt is made to issue tape commands a Set Illegal status will be generated, via exclusive OR gates J2 and connector pin B31. This status will also occur if more than one MTT is selected simultaneously.

J3-5 and J3-9 flop outputs are connected to exclusive OR gate J2-8; J4-5 and J4-9 outputs are connected to J2-3. The outputs of both gates are connected to exclusive OR gate J2-6. If none of the Select flops are set the inputs to J2-8 and J2-3 will be low, causing the outputs to be low to J2-6 to provide a Set Illegal condition. When an MTT is correctly selected a high level will appear at J2-6.

STATUS OUTPUT

The status outputs are provided by the 12 power NAND gates FG5-3 to J5-4 (top of illustration) which provide the following status information when enabled by IOT 6541 at connector pin B3:

Vertical Parity	EOF
Illegal Command	Busy
EOT	CRCC Error
BOT	LRCC Error
Record Longer than Word Count	Transport Not Ready
Record Shorter than Word Count	No Write Ring

The circuitry consists basically of four 12-bit binary counters, which control high speed data break transfers between the CPU and magnetic storage drum, and the CPU and magnetic tape transport. The pcb contains two similar circuits: one for the drum and one for the MTT. Each circuit consists of two presettable 12-bit binary counters: one for current address and one for word count. The drum circuitry only will be described.

WORD COUNT (WC)

The drum word count register, D1, F1, H1 counts the number of words transferred between the drum and the CPU. It is initially preset to a value that is the two's complement of the total number of words to be transferred. This value is supplied by the CPU BAC lines 00 to 11, connector pin group B40 to A4. The drum WC register consists of 4-bit binary counters D1, F1, and H1. The register is preset by IOT 6522 via connector pin A2 and inverter H5-12.

The drum word count register is incremented during each break cycle via the Drum Address Accepted pulse at connector pin B4 (lower left). This pulse is routed via F5-3 and gated by B Break (0) at F5-11 to prevent noise from incrementing the registers when a break cycle is not in progress. A pulse generator, consisting of G5-10, G5-6, and G5-4, produces a 150 ns pulse which is transmitted via F5-8 to clock the drum WC register. (It also clocks the drum CA register, consisting of D3, F3, and H3.)

When the most significant bit of the drum WC register changes from a one to a zero (i.e. overflow) a Drum WC Overflow pulse is produced at connector pin B37. This indicates to the Drum Control pcb that the desired number of words have been transferred.

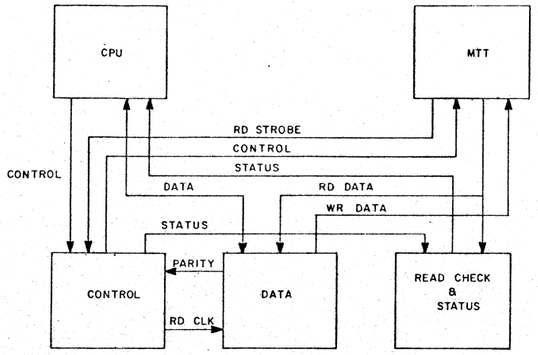
CURRENT ADDRESS (CA)

The Drum Current Address Register consists of 4-bit binary counters D3, F3, and H3. These are preset via IOT 6524 at connector pin B2. The CA register value indicates to the CPU which address in memory is to be used for data transfer. The 12-bits are capable of addressing 4096 memory locations. The drum Extended Memory Address Register consists of three flip-flops E5, D5, and C5. The flops are used to select one of the eight 4096 word memory fields which is to be used in the transfer. This register is loaded via IOT 6544 at connector pin A24 from accumulator bits 06, 07, and 08.

The value held in the drum CA and drum EMA registers is applied to open collector NAND gates E3, G3, I3, and C3. The 15-bit value is gated onto the Data Address bus lines by the Drum Address to DA pulse applied at connector pin A13 (top left).

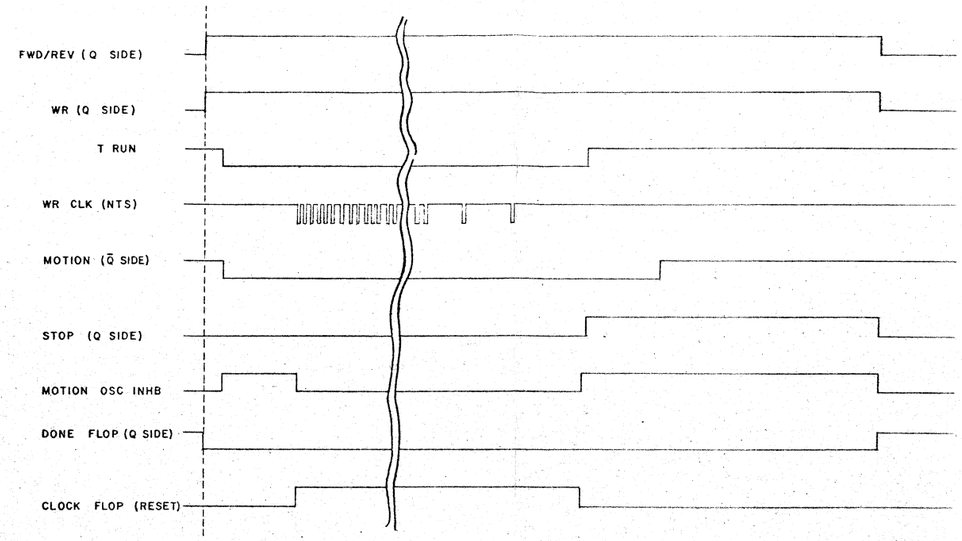
B RUN CONDITIONING

The $\overline{\text{B Run}}$ signal is taken directly from the CPU to connector pin A27 then through a noise suppression circuit consisting of an integrator and Schmitt trigger. This circuit is capable of rejecting high-going noise pulses up to 4 µs wide. The signal is inverted by paralleled power gates, B5-6 and B5-8, and fed to the CCL logic via connector pin A26.



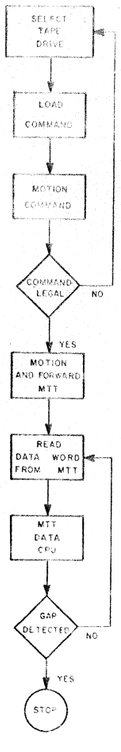
DATA CONTROL AND STATUS ROUTING

FIGURE 5-1



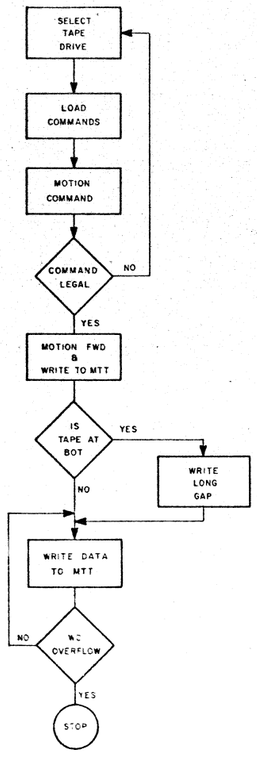
MTT WRITE CYCLE TIMING

FIGURE 5-5



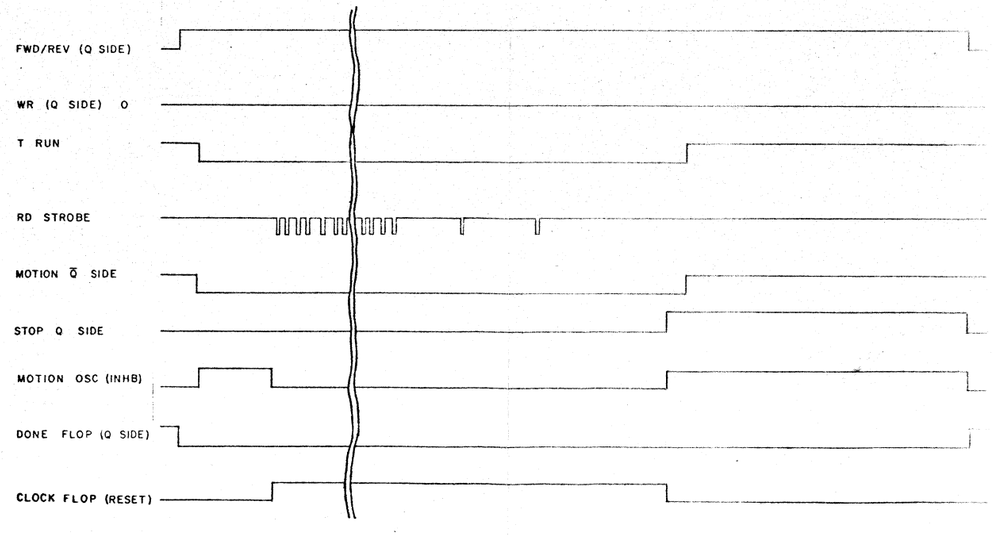
READ DATA FLOW

FIGURE 5-2



WRITE DATA FLOW

FIGURE 5-3



MTT READ CYCLE TIMING

FIGURE 5-4

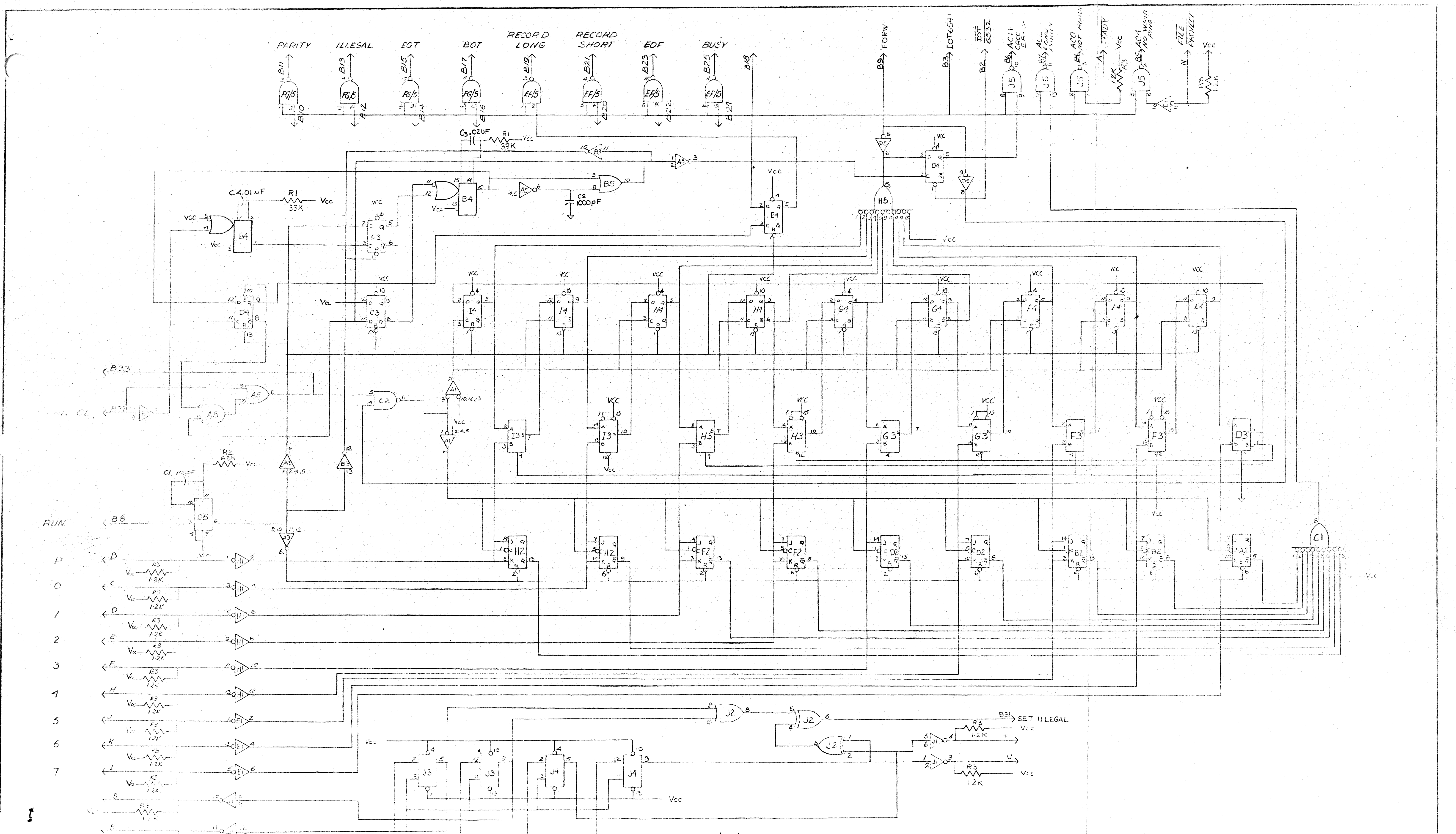
used on		drawn	
scale	23 AUGUST 71 date	design approval	
	unless otherwise specified	checked	
.00 = ± .01 fraction ± 1/64		engineering	
.000 = ± .005 angles ± 0 30'		material	finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

MTT

title

sheet of no.



rev	description	date	by	apprvd
F (EC 048)	CAPACITOR NOTED	10 JAN 73		
E (KE 463)	GATE CHANGED B5-B3, C			
D (ECO KE 338)	[illegible]			
C (ECO KE 273)	COMPONENT & TAPE CHANGES	5 NOV 71	GT	
B (ECO KE 244 AND KE 142A AND KE 229)	11 WAS D102462		RM	
A	[illegible]			

used on: C102424/1

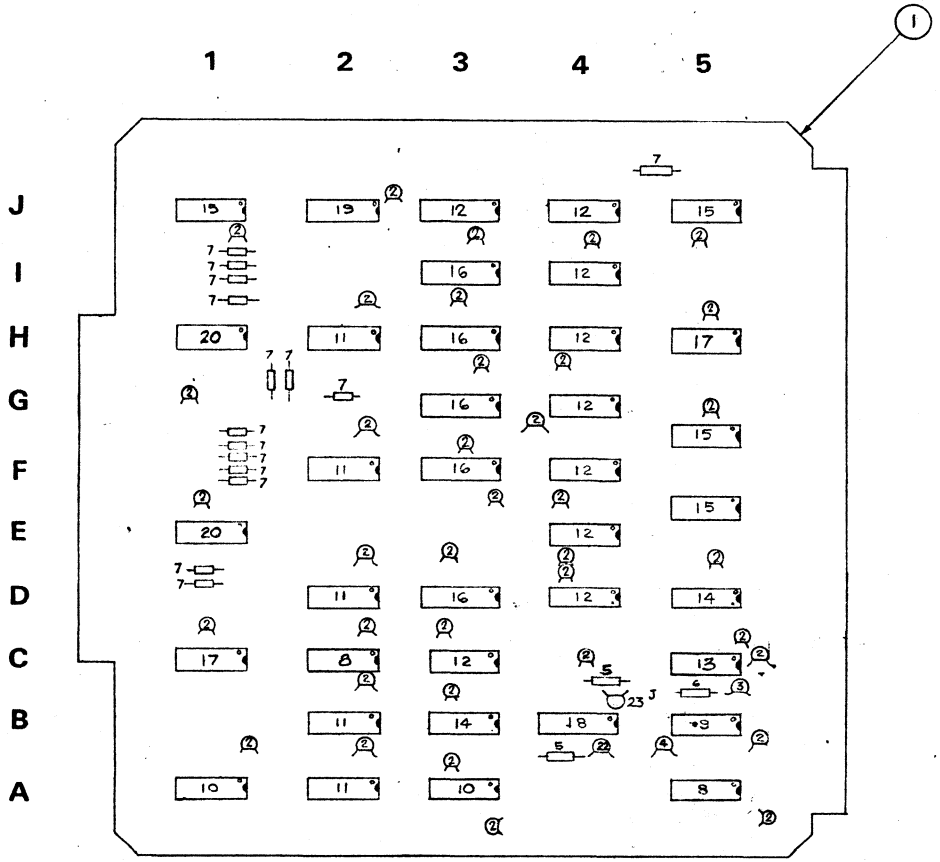
unless specified: fractions ± 1/64; .00 = ± .01; .000 = ± .005; angles = ± 0°30'

scale | date | material | finish | drawn | design apprvl | checked | final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title: [illegible] READ CHECK 9 TRACK (25 IPS)

sheet of | no. D[illegible]



NOTE: ► INDICATES CUT LINE
JUMPER INDICATED ▪---▪
ARE ON SOLDERED SIDE OF PCB.

(FOR P/L SEE SHT 2)

SC 028	E	CAPACITOR CHANGED	10 JAN 73		
ECO KE 338	D	R1 WAS 2.7 K	2 JUNE 72		
ECO KE 273	C	COMPONENT & TAPE CHANGES	15 NOV 71	GT	
ECO KE 244 AND LE 185A AND LE 223	B	11 WAS D1024CA	9 SEPT 71	R.M.	
	A	TAPE CHANGES			
	rev	description	date	by	apprvd

1015 2 A used on	1:1 scale	JULY date 1970	R.C. drawn
unless specified fractions ±1/64 .00 = ±.01 .000 = ±.005 angles: ±0°30'	material		design apprvl
			checked
	finish		final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

ASSEMBLY
MTT READ CHECK
9 TRACK (25 IPS)

title

sheet of | no. C | rev

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R CHARLEB 219 | DATE: 2 JULY 1979 | APPROVED BY:

SERIAL NO.

USED ON ASSEMBLY: 10256 A & 11028A. | DRAWING REV. E

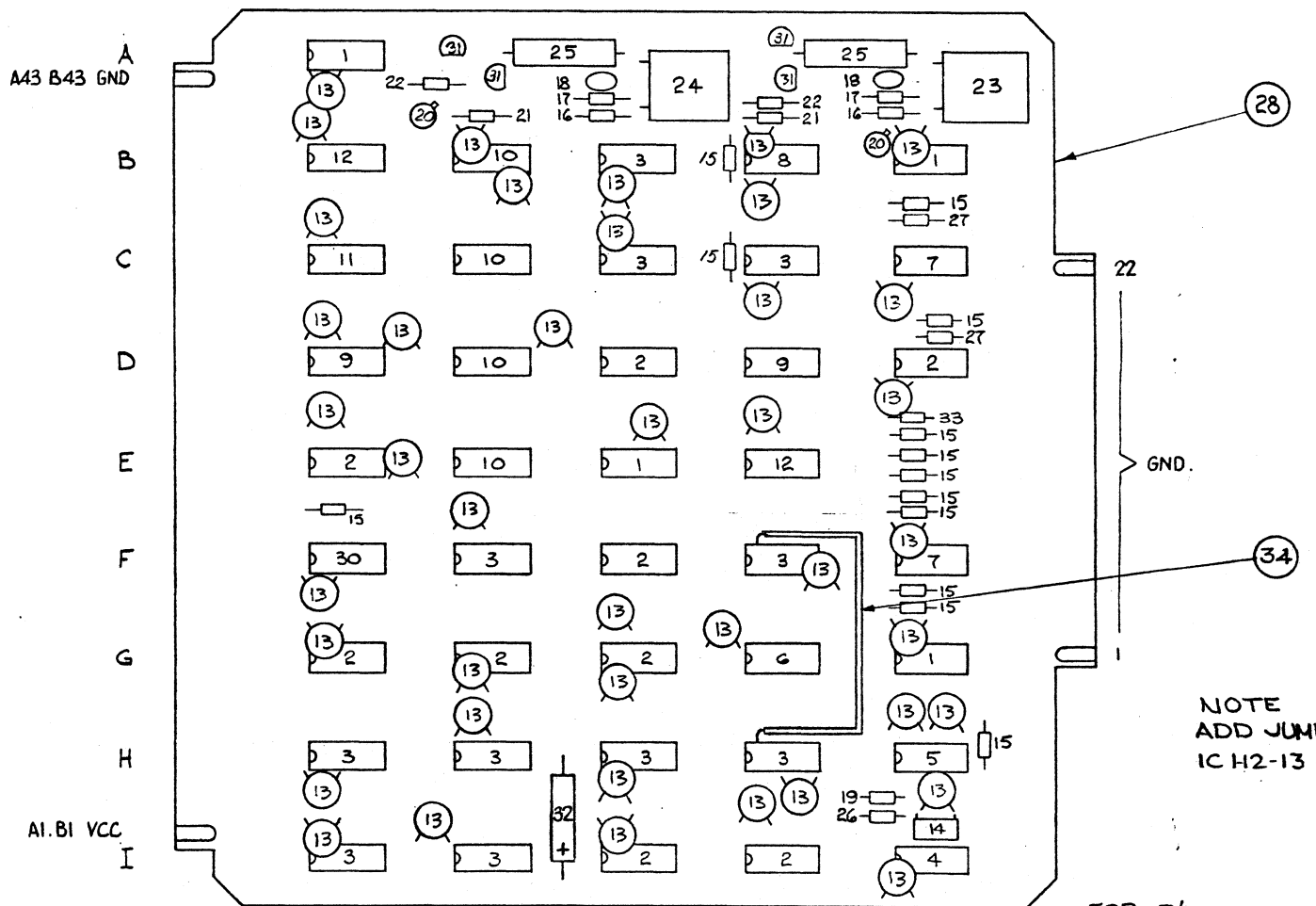
DATE ISSUED

ASSEMBLY NO. C10246A/1 | SHT 2 OF 2

TITLE: ASSEMBLY MTT READ CHECK 9 TRACK (25 IPS) (FOR DWG SEE SHT 1)

PRODUCT

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.
1	10246P		1	P.C.B.		ECO KE24
C 2	90119		37	CAPACITOR 0.01μF 50V	C5-C41	& 18 & 22
3	90112		1	CAPACITOR 100pF DISC CERAMIC	C1	KE 273 (
B 4	90114		1	CAPACITOR 1000pF DURA MICA	C2	KE 338 C
D 5	90480-99		2	RESISTOR 33K 1/4W	R1	SC 048
6	90480-83		1	RESISTOR 6.8K 1/4W	R2	
7	90480-65		15	RESISTOR 1.2K 1/4W	R3	
8	90331		2	MC 7400P	A5 C2	
9	90315		1	MC 7402P	B5	
10	90316		2	MC 7440P	A1 A3	
11	90319		5	MC 7473P	A2, B2, D2, F2, H2,	
12	90338		9	MC 7479P	C3, D4 E4, F4, G4, H4, I4	J3, J4
13	90346		1	MC 74121P	C5	
14	90322		2	MC 836P	B3, D5.	
15	90323		4	MC 858P	E5/F5, F5/G5, J5. J1.	
16	90376		5	MC 8304P	D3, F3, G3, H3, I3	
17	90388		2	MC 1805P	C1, H5,	
18	90389		1	MC 8602P	B4,	
19	91294		1	MC 3021P	J2	
20	90392		2	MC 7400P	H1, E1	
B 21						
C 22	93111		1	CAPACITOR .02 μF	C3	
E 23.	93110		1	CAPACITOR 0.01 ufd	C4	
[illegible]	[illegible]		1	[illegible]		



v	eco	description	date	by	chk	apprvd
	SC 005	JUMPER H2-13 TO F2-13 ADDED	9 JAN 73	[illegible]		
	150	ECO KE 150 INCORP	25 SEPT 72	MJ		
	393	RESISTOR ADDED, ITEM 33	15 SEPT 72	MJ		
	300	ITEM 31 CHANGED TO MPS 3704	26 MAY 72	MN		
	292	REDRAWN, TRACK & TRANSISTOR REV.	19 NOV. 71	RK		

used on: D10152A	drawn: R. KINDS	CONSOLIDATED COMPUTER LIMITED OTTAWA	MTT CONTROL PCB ASS'Y (556 BPI)
scale: 1 : 1	date: 2 NOV. 71	design apprvl: [illegible]	
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ± 0 30'		checked: [illegible]	
		final apprvl: [illegible]	
material: —	finish: —	title	
sheet 1 of 3	no. B10255A/1	rev H	

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
J.R.B	10 AUG 70	RBC

USED ON ASSEMBLY: D10152A

DRAWING REV: H

ASSEMBLY NO: B10285A/1

SHT 2 OF 3

TITLE: MTT CONTROL (556 BPI)

FOR DWG SEE SHT 1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	90322		4	MC 836 P	A5, B1, E3, G1		
2	90331		9	MC 7400 P	D1, D3, E5, F3, I2, I3 G3 G4, G5		
3	90338		11	MC 7479 P	B3, C2, C3, F4, F2, H2, H3, H4, H5, I4, I5		
4	91376		1	MC 8301 P	I1		
5	90315		1	MC 7402 P	H1		
6	90341		1	MC 846 P	G2		
7	90323		2	MC 858 P	C1, F1		
8	90316		1	MC 7440 P	B2		
9	90333		2	MC 7410 P	D2, D5		
10	90339		4	MC 7493 P	B4, C4, D4, E4		
11	90334		1	MC 7420 P	C5		
12	90335		2	MC 7430 P	B5, E2		
13	90119		42	CAPACITOR .01 μF, 50V	C7-C46, C1, C2		
14	90114		1	CAPACITOR 1000 pf, 100V	C3		
C 15	90480-65		13	RESISTOR 1.2 K, 1/4 W	R1-R8, R11, R12, R23-R25		
16	90480-135		2	RESISTOR 1 M, 1/4 W	R16, R18		
17	90480-145		2	RESISTOR 2.7 M, 1/4 W	R15, R17		
18	90110		2	CAPACITOR 33 pf, 100V 5% MICA	C4, C5		
19	90480-51		1	RESISTOR 330 Ω, 1/4 W	R14		
D 20	90531		2	TRANSISTOR 2N706	Q3, Q6		
21	90480-87		2	RESISTOR 10 K, 1/4 W	R19, R20		
22	90480-47		2	RESISTOR 220 Ω, 1/4 W	R21, R22		
23	9011[illegible]2		1	CRYSTAL SITW 511.57 KHZ	Y2		

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
J.R.B	10 AUG. 70	(R.W.C)

USED ON ASSEMBLY: D10152A

DRAWING REV: H

ASSEMBLY NO: B10285A/1

SHT 3 OF 3

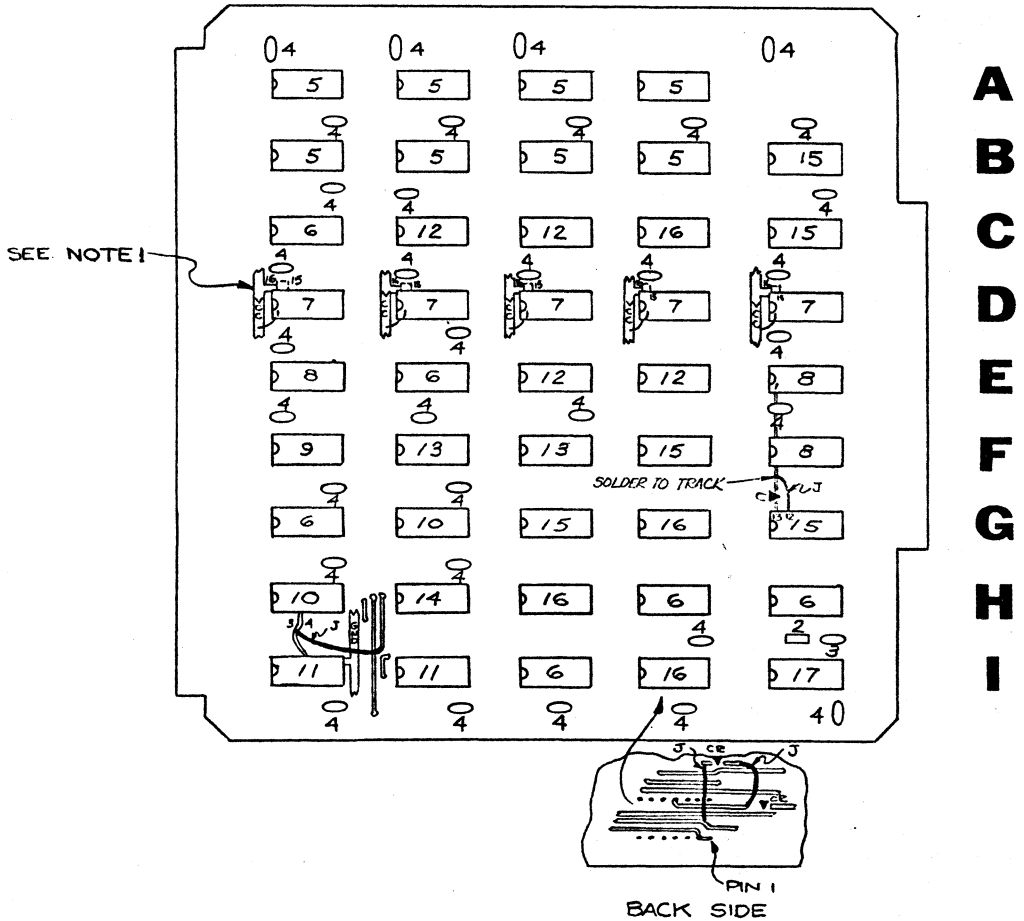
TITLE: MTT CONTROL (556 BPI)

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90184		1	CRYSTAL 444.8 KHZ	Y1		
25	90111		2	CHOKE 4700 MH	L1, L2		
26	90480-91		1	RESISTOR 15K, 1/4W ± 5%	R13		
27	90480-60		2	RESISTOR 750Ω, 1/4W ± 5%	R9, R10		
28	10285P		1	P.C.B.			
29	90668		3"	ELECTRICAL TAPE	INSULATE Y1 & Y2		
C 30	92261		1	MC 7403	F5		
D 31	90597		4	TRANSISTOR MPS3704	Q1, Q2, Q4, Q5		
32	90087		1	CAPACITOR 10uf	C6		
F 33	90480-63		1	RESISTOR, 1K, 1/4W	R26		
G 34	90419		2"	WIRE PTK-26-3B1-2			
REF.	D10285A/1		1	LOGIC			



NOTE: 1- ON D1, D2, D3, D4 & D5 PIN 1, 15 & 16 ARE JUMPERED TO VCC

LEGEND - J - INDICATES JUMPER WIRE
◀ C - INDICATES CUT (COMPONENT SIDE)
◀ CR- " " (SOLDER SIDE)

rev	eco	description	date	by	chk	apprvd
B	266	REDRAWN. CUT TRACK & ADD JUMPER (G1)	15 OCT 71	PAR		

used on: D110225 A
scale: 1:1
date: 13 MAY '70
drawn: R DES
design apprvl:
checked:
final apprvl: IK
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ±0 30'

CONSOLIDATED COMPUTER LIMITED
OTTAWA

material:
finish:

title: ASS'Y PCB MTT DATA 9 TRACK LEV III
sheet 1 of 1
no. C10365A
rev:

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R [illegible] | DATE: 15MAY70 | APPROVED BY:

TITLE: ASSY PCB LEV III MTT DATA 9 TRACK

BASED ON ASSEMBLY:

DRAWING REV. B

SERIAL NO.

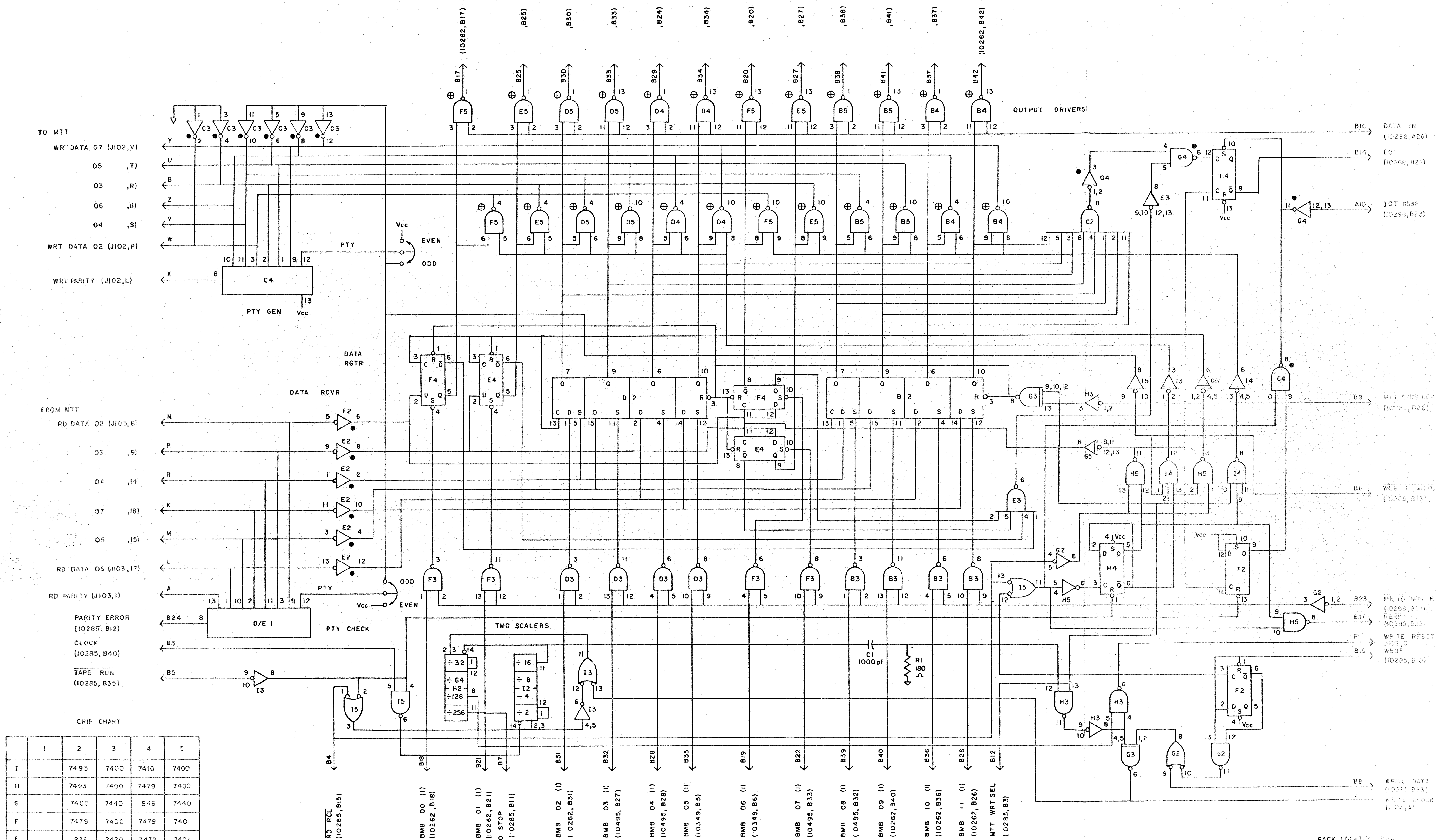
DATE ISSUED

ASSEMBLY NO. C10365A

SHT 1 OF 1

PRODUCT

ITEM	PART NO.	REV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.	QTY REQ
1	10365P	B	1	PCB		KE 266(B)	
2	90480-81		1	RESISTOR 5.6K 1/4W	R		
3	90118		1	CAPACITOR 500pF 500VDC	C1		
4	[illegible]0118		34	CAPACITOR .01μF 150VDC	C		
5	90382		8	IC MC7401P	A5, B5, A4, B4, A3, B3 A2, B2		
6	90381		6	IC MC7400P	C5, G5, E4, I3, H2, H1		
7	90376		5	IC MC8304P	D5, D4, D3, D2, D1		
8	90316		3	IC MC7440P	E5, E1, F1		
9	90315		1	IC MC7402P	F5		
10	90333		2	IC MC7410P	H5, G4		
11	90339		2	IC MC7493P	I4, I5, I4½		
12	90330		4	IC MC4015P	C4, C3, E3, E2		
13	90328		2	IC MC4008P	F4, F3		
14	90319		1	IC MC7473P	H4		
15	90320		5	IC MC475P	G3, F2, G1, C1, B1		
16	90338		4	IC MC7479P	H3, I2, G2, C2		
17	90346		1	IC SN7412N	I1		
REF	D10365A	B		LOGIC			



CHIP CHART

	1	2	3	4	5
I		7493	7400	7410	7400
H		7493	7400	7479	7400
G		7400	7440	846	7440
F		7479	7400	7479	7401
E	4008	836	7420	7473	7401
D		4015	7400	7401	7401
C		7430	836	4008	
B		4015	7400	7401	7401
A					

RACK LOCATION B24

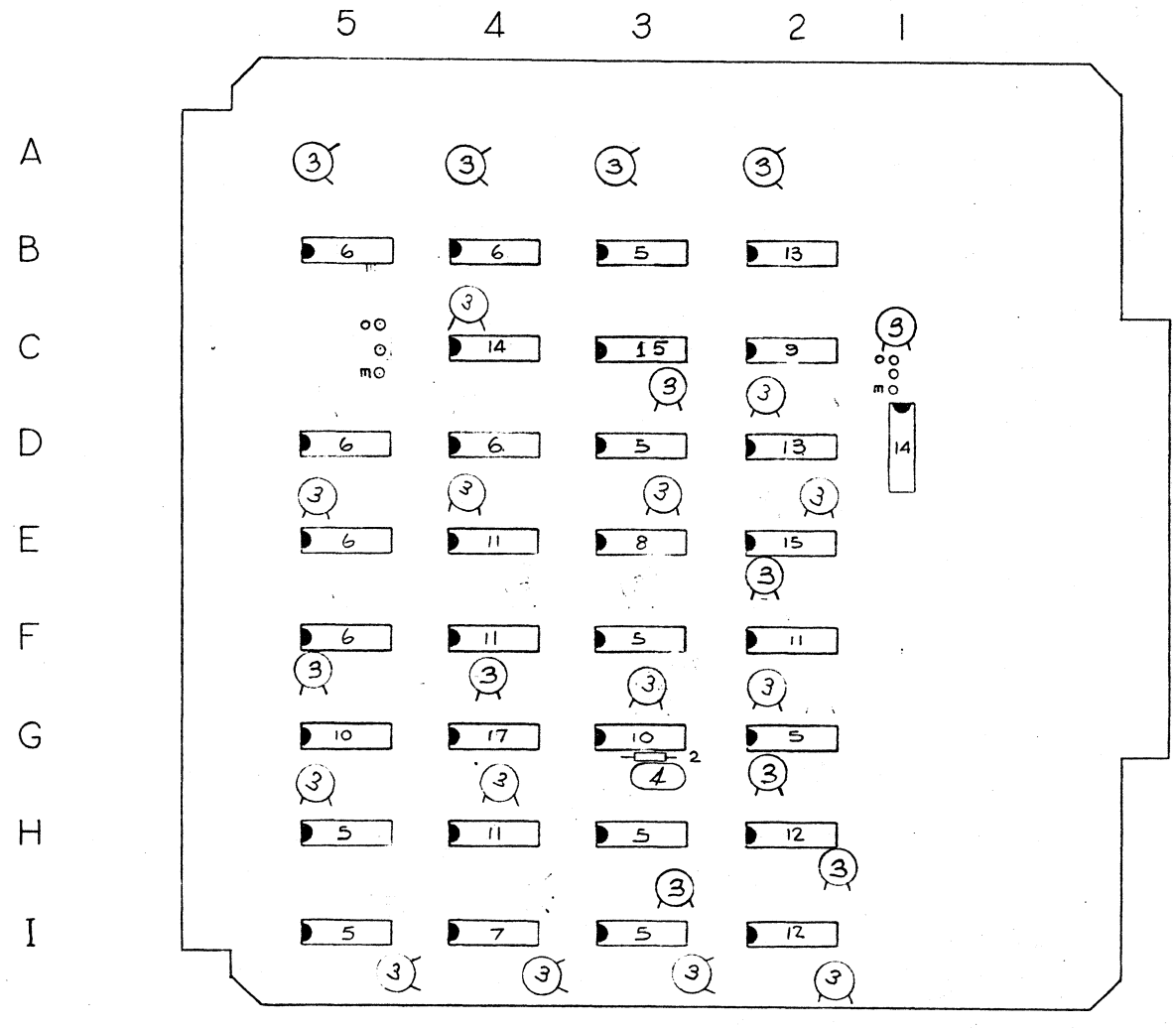
used on | scale — | date 22 JULY 71 | drawn JRB | design apprvl | checked | final apprvl JJD

unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ± 0 30

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: 7-TRACK MTT DATA

sheet 1 of 1 no. D10558 L



FOR P/L SEE SHT 2

description	date	by	apprvd
PRODUCTION RELEASE KE350	13JULY72	MJ	
4 CAPACITORS MOVED DREVO 103	20 SEPT 72	RAP	

used on

unless specified
fractions ± 1/64
.00 = ±.01
.000 = ±.005
angles = ±0°30'

scale 1:1 | date 21. NOV. 70. | drawn JRB

material

finish

design apprvl

checked

final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title MTT DATA 7 TRACK LEVEL III

sheet 1 of 2 | no B 10[illegible] A | rev

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: M.H. | DATE: 18 DEC 70 | APPROVED BY:

TITLE: MAG TAPE DATA 7 T LEVEL III

FOR DWG SEE SHT 1

SERIAL NO.

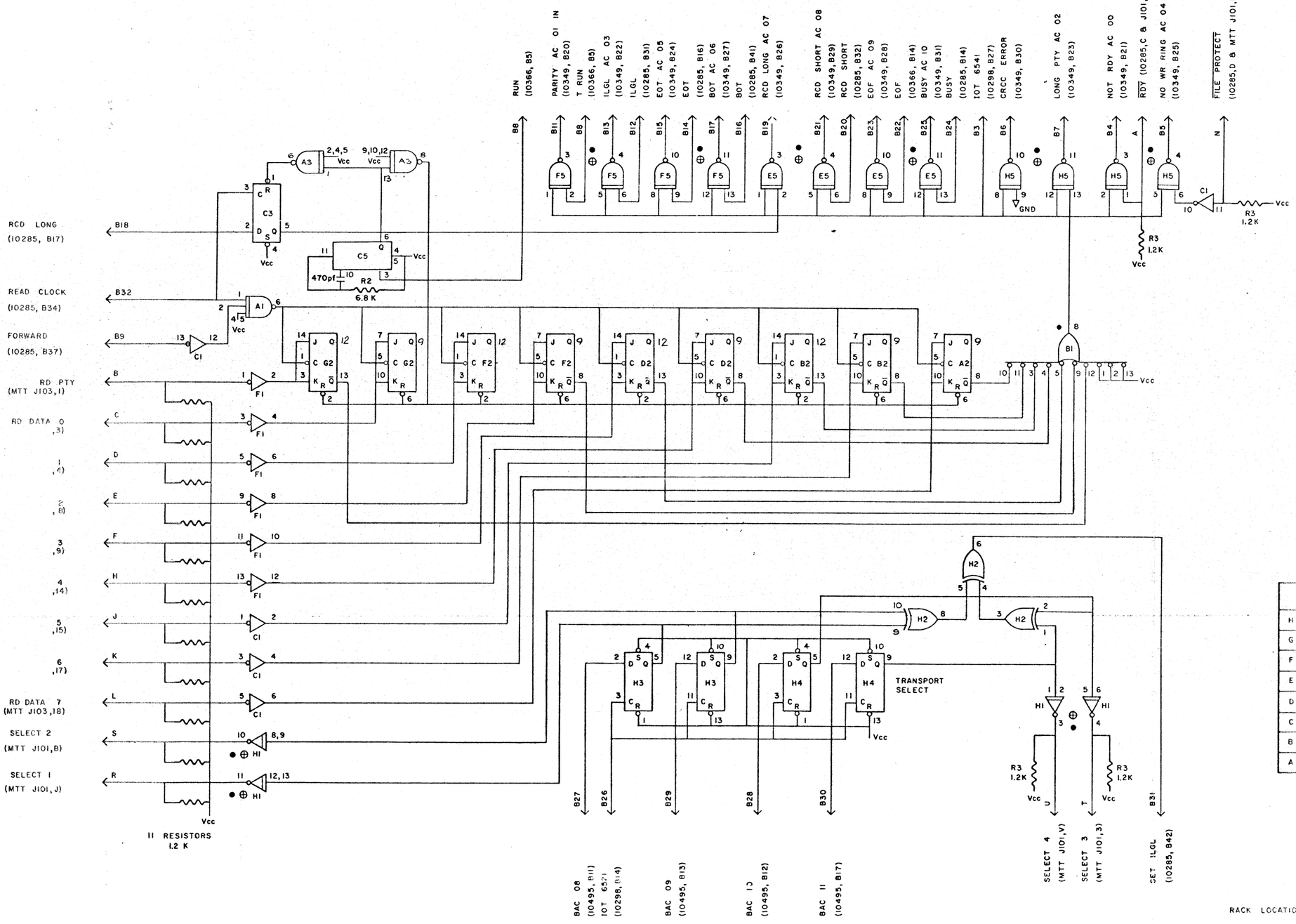
USED ON ASSEMBLY: 10356 A | DRAWING REV. A

DATE ISSUED

ASSEMBLY NO. B10366 A | SHT 2 OF 2

PRODUCT

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.
1.	10366P		1	P.C.B.		M.C.O. 103 Ø1.
2	90480-45		1	RESISTOR 180 Ω 1/4 W	R1	KE 350 (A)
3	90119		26	CAPACITOR 0.01μF 50V	C	
4	90114		1	CAPACITOR 1.000pF 5%	C1	
5	90331		8	MC 7400P	B3.D3 F3 G2 H5.H3	
					I5.I3	
6	90332		6	MC 7401P	B4.B5 D4.D5 E5 F5	
7	90333		1	MC 7410P	I4	
8	90334		1	MC 7420P	E3	
9	90335		1	MC 7430P	C2	
10	90316		2	MC 7440P	G3.G5	
11	90338		4	MC 7479P	E4 F2 F4 H4	
12	90339		2	MC 7493P	H2.I2	
13	90330		2	MC 4015P	B2 D2	
14	90328		2	MC 4008P	D/E1, C4	
15	90322		2	MC 836P	C3.E2	
16			3/4"	JUMPER 20 GAUGE		
17	90341		1	MC 846P (MOTOROLA)	G4	
REF	D10366L			LOGIC		



CHIP CHART

	1	2	3	4	5
H	858	3021	7479	7479	858
G		7473			
F	7404	7473			858
E					858
D		7473			
C	7404		7479		74121
B	1805	7473			
A	7440	7473	7440		

RACK LOCATION B26

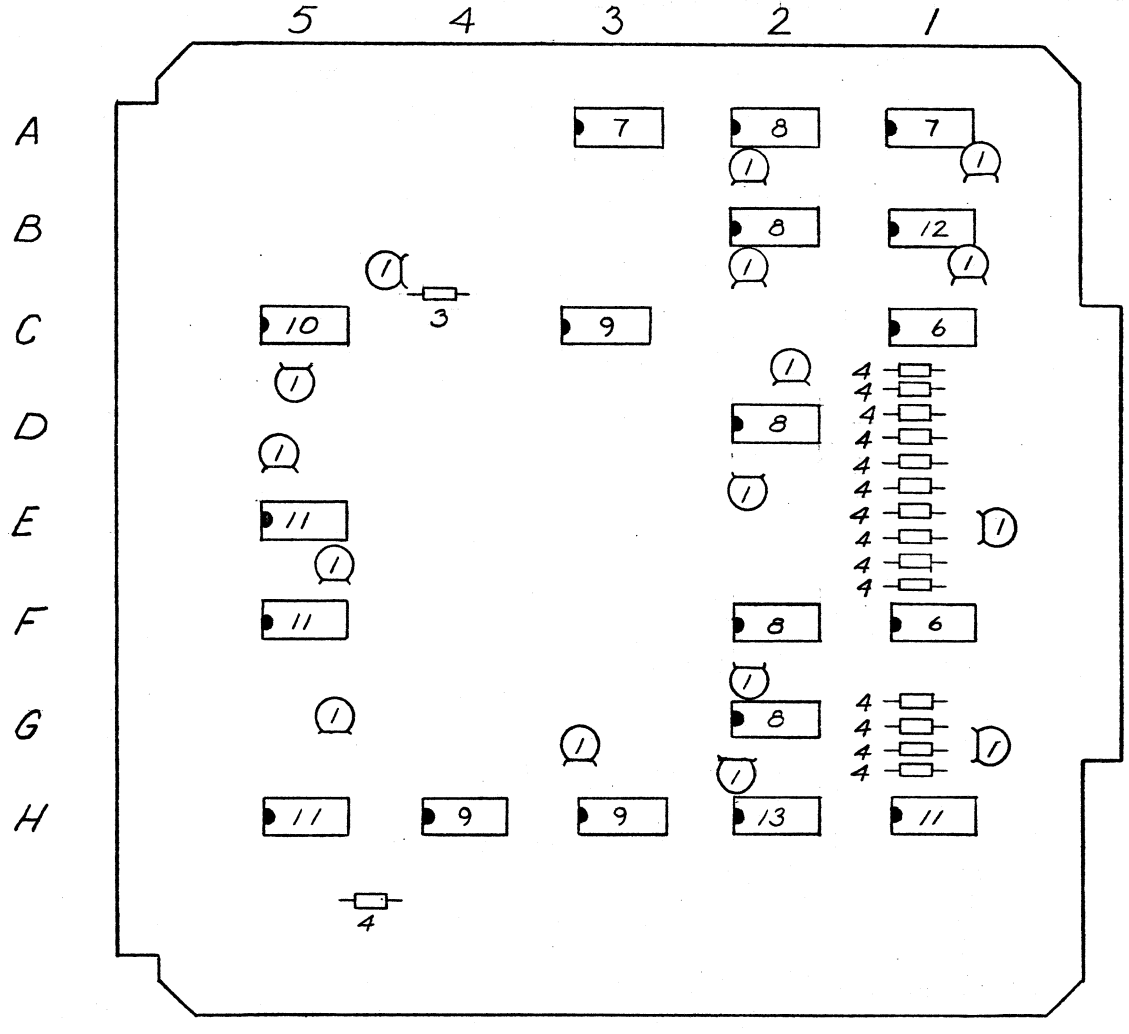
rev	eco	description	date	by	chk	approved
C	KS 434	H3 PIN 9 CONN TO H2-10	71 JULY 16			
E	34	REDRAWN				

used on | drawn
scale | date 16 JULY 71 | design approval
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles ± 0° 30' | checked | JSC final approval
material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

MTT READ CHECK 7-TRACK

title | sheet of | no. D10366 E | rev



rev	description	date	by	apprvd
A	PRODUCTION RELEASE KE 350	8 JULY 72	MJ	

used on	1:1 scale	11 FEB 71 date	R.M. drawn
unless specified fractions ± 1/64 .00 = ±.01 .000 = ±.005 angles = ± 0°30'	material		design apprvl
	finish		checked
			T. KAVÉ final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

MTT READ CHECK
7 TRACK

title

sheet 1 of 1 | no. B 103684

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

COMPILED BY: [illegible] DATE: [illegible] APPROVED BY: [illegible]

USED ON ASSEMBLY:

DRAWING REV. A

ASSEMBLY NO. B10368A SHT 1 OF 1

TITLE: ASSY MTT READ CHECK 7 TRACK

[illegible]K AREA

SERIAL NO.

DATE ISSUED

PRODUCT

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.
1	10368 P		1	P.C.B.		KE 350 (A)
2	90119		16	CAPACITOR 0.1μf 50 V.	C	
3	90107		1	CAPACITOR 470 pf DIPPED 100 WVDC	C1	
4	90490-68		1	RESISTOR 6.8K ¼W	R1	
5	90480-45		15	RESISTOR 1.2K ¼W	R2	
6	[illegible]		2	MC 7404	C1, F1	
7	90315		2	MC 7440 P	A1, A3	
8	90319		5	MC 7473 P	A2, B2, D2, F2 G2	
9	90335		3	MC 7479 P	H3, H4 C3	
10	90346		1	SN 74121 P	C5	
11	90323		4	MC 855 P	E5, F5, H1, H5	
12	90322		1	MC 1805 P	B1	
13	91294		1	MC 3021 P	H2	
REF	D10396 L			LOGIC.		
	>					

CHIP CHART

	1	2	3	4	5
I			858	858	
H	8293	8293	8293	8293	836
G			858	858	836
F	8293	8293	8293	8293	7400
E			858	858	7479
D	8293	8293	8293	8293	7479
C			858	805	7479
B			836	7400	7440
A			858	836	

BUS FOR E4, E3, G4, G3, I4, I3, C2, C3 (10391-2 PINS 9, 11, 17)

GND A10
GND A11
GND A17

MTT ADD → DA A12 (10298 PIN A25)

DRUM ADD → DA A13 (10298 PIN B21)

R4 2.2K
VCC
R5 2.2K

MTT CA

DRUM CA

DATA STROBE D4

D3 D2 D1 F4 F3 F2 F1 H4 H3 H2 H1

VCC A1, B1
C37 10µf
C11-C36 .01µf
GND A13, B13

R21 1K
C7 100pf
C9 100pf

MTT WC OVERFLOW (10293 PIN 23)
6551 (10298 PIN A31)
6522 (10298 PIN B13)
DRUM WC OVERFLOW (10292 PIN 28)

C3 470pf
C1 1000pf
C2 1000pf
C4 470pf

R23 1K

MTT WC
DRUM WC

C6 100pf
C8 100pf

A23 → 6554 (10298, B36)
R24 1K
R25 1K
A24 → 6541 (10298, A33)

A3 → 6552 (10298 PIN B31)
R20 1K
B2 → CLR CA (10298 PIN B16)
R22 1K

CLR ACC (10391-1 PIN 22)

R15 180Ω
CR1 IN4151
A26 → B RUN (10298 PIN A13)
A27 → B TURN (10391-1 PIN 24)
C10 1000pf

MTT ADD ACC (10295 PIN A23)
R1 2.2K
VCC
R2 2.2K
DRUM ADD ACC (10295 PIN A21)
B BREAK (10391-2 PIN B21)
R3 2.2K
VCC

MTT INC
DRUM INC

R6 4.7K … R17 4.7K — VCC

B40 B38 B32 B30 B25 B22 B16 B14 A8 A6 A5 A4

BAC-0 (10391-5 PIN 23)
BAC-1 (10391-5 PIN 1)
BAC-2 (10391-5 PIN 3)
BAC-3 (10391-5 PIN 5)
BAC-4 (10391-5 PIN 12)
BAC-5 (10391-5 PIN 14)
BAC-6 (10391-5 PIN 16)
BAC-7 (10391-5 PIN 18)
BAC-8 (10391-5 PIN 20)
BAC-9 (10391-5 PIN 22)
BAC-10 (10391-5 PIN 24)
BAC-11 (10391-5 PIN 26)

NOTES:
- UNLESS OTHERWISE SPECIFIED:
  RESISTORS - OHMS, ¼W
  CAPACITORS - µF
- REFER TO ECO K.E 356
- RACK LOCATION A23

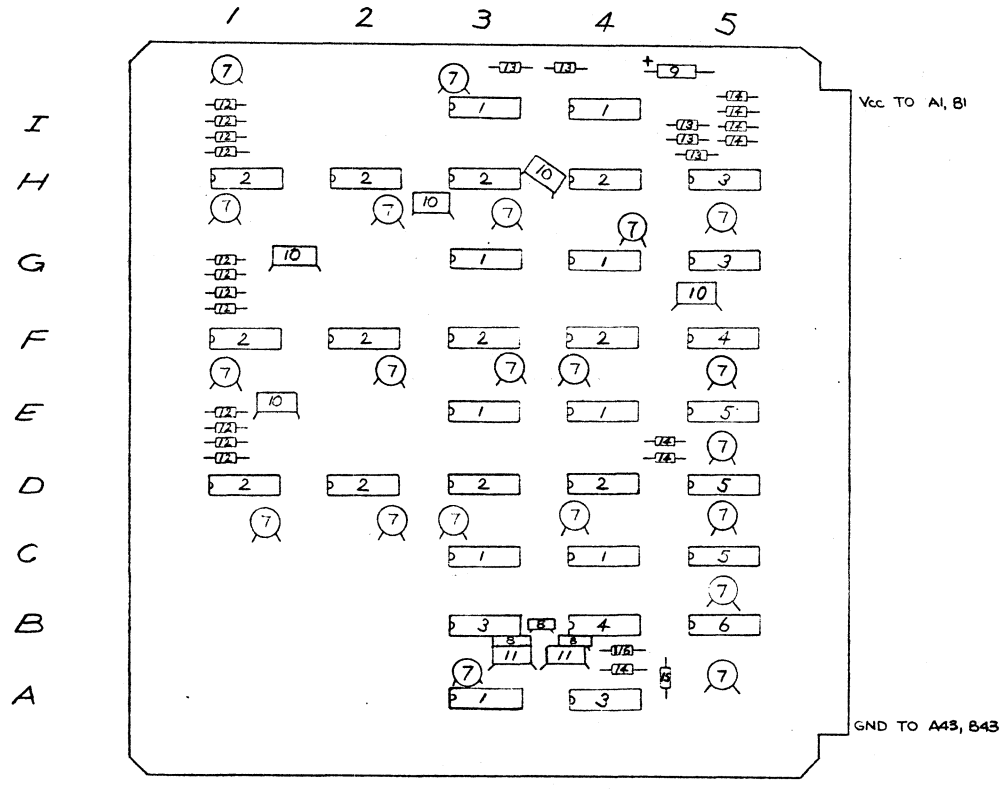
KE471	J	CORRECTION	6-10-72 D.W.
KE454	F	NO CHANGE	15-9-72 MK
KE438	E	REDRAWN (A3 ADDED)	28-8-72 HARP

CONSOLIDATED COMPUTER LIMITED OTTAWA

LOGIC MCBCA ACE

B10422-1 G

sheet 1 of 1



KE 454	F	NO CHANGE	15SEP72	M.N.	JWB
KE 438	E	PARTS LIST CHANGE	17AUG72	M.N.	JWB
KE 365	D	6 DEC. CAP. REMOVED, A3 ADDED	19JULY72	M.N.	JWB
KE 345	C	CHANGE ON LOGIC CARD	19APR72	M.N.	JWB
	B	NEW ART WORK ECO KE 294	1 DEC 71	EAP	
ECO 260	A	PRODUCTION RELEASE	18 OCT 71	EAP	
	Ø3	DREVO 097 INC	3 SEPT 71		
	Ø2	DREVO 097 INC	17 JUNE 71	MJ	
	Ø1	EARLY UNRELEASED			
rev		description	date	by	approvd

used on

unless specified
fractions ±1/64
.00 = ±.01
.000 = ±.005
angles = ±0°30'

material

finish

1:1 scale | 8 DEC/70 date | M.N. drawn | design apprvl | checked | final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title: ASSY WC, & CA

sheet 1 of 1 | no. C 10[illegible]

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: M.N. | DATE: 9 DEC 70 | APPROVED BY:

TITLE: WORD COUNT & CURRENT ADDRESS

SERIAL NO.

USED ON ASSEMBLY:

DRAWING REV. F

DATE ISSUED

ASSEMBLY NO. C10442A

SHT 1 OF 1

PRODUC

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO
E 1	90323		9	MC 858P	C3, C4, E3, E4, G3, G4, I3,	DREVO 007
					I4, A3	REVO 097
2	91433		12	N8293A	D1, D2, D3, D4, F1, F2,	NEW ARTWORK.
					F3, F4, H1, H2, H3, H4	KE 345
3	90322		4	MC 836P	A4, B3, G5, H5	KE 365
4	90331		2	MC 7400P	B4, F5	KE 428
5	90338		3	MC 7479P	C5, D5, E5	KE 454
6	90316		1	MC 7440P	B5	
X Ø3 Ø2 7	90119		21	CAPACITOR .01 µf 50 WVDC	C11-C37	
Ø2 8	90114		3	CAPACITOR 1000 PF 100 WVDC	C1 C2 C10	
Ø1 9	90087		1	CAPACITOR 10 µf TANTALUM 20V	C37	
V3 V1 10	90710		5	CAPACITOR 100 PF 100V	C5-C9	
11	90107		2	CAPACITOR 470 PF 100 WVDC	C3, C4	
12	90480-79		12	RESISTOR 4.7K ¼W	R6-R17	
13	90480-71		5	RESISTOR 2.2K ¼W	R1-R5	
14	90480-63		7	RESISTOR 1K ¼W	R18-R25	
D 15	90480-45		1	RESISTOR 180Ω ¼W	R18	
16	91300		1	DIODE IN 4151	CR1	
17	10[illegible]P	B	1	PCB.		

The contents listed are included in the manual only where they apply to the relevant system.

GENERAL

The Level 3 Drum Controller used in the Mark V systems provides the Key-Edit interface between the 8/E processor and the VRC 1004S or 1016 temporary data storage drum.

BRIEF DESCRIPTION

The drum storage capability is divided into tracks; each track contains 64 sectors. The 1004S drum has 128 tracks and the 1016 drum either 256 or 512 tracks.

The controller sectors contain 40 data words, each of 12 bits, plus one 12-bit CRCC word; the CRCC word is written on the drum and not transferred as data to the CPU. Each sector has an 8-bit preamble and a 3-bit postamble. Thus there are 503 bits in each sector (40x12)+12+8+3 .

There are 64 sectors in each track. The first sector clock, and the index clock, are separated by four bits to facilitate sector synchronization. There are 32,196 bits each track (503x64)+4 . Figure 3-1 illustrates the drum clocking.

CONTROLLER DESCRIPTION

The basic controller consists of three printed circuit boards:

1. Drum Control, pcb 10282
2. Drum Data, pcb 10284
3. Derandomizer, pcb 10262

The pcbs are located in the Key-Edit logic rack, locations B23, B22, and A26 respectively. A cable, part number 10337, connects the control and data pcbs to the storage drum.

BRIEF OPERATING THEORY

The controller performs three main functions (Figure 3.2):

1. Serializing and CRCC Generation and Check (Data pcb)
2. Stop-Start Control (Control pcb)
3. Data Word Handling (Derandomizer pcb)

The Word Count and Current Address, and Drum and MTT IOT Generator pcbs are ancillary to this interface; they are described in the MTT interface section.

The necessary data transfer parameters are:

1. CPU memory starting address
2. Number of words to be transferred
3. Track number
4. Starting sector
5. Read/Write mode

The first two parameters are stored in the Word Count and Current Address pcb; the remaining three are stored in the control pcb.

Figure 3-2 illustrates the controller data handling. The write data sequence is — data word transferred from the CPU to the derandomizer, then via the data pcb to the drum. The function of the ancillary pcbs is explained in detail in Section 5, MTT Controller.

Figures 3-3 and 3-4 illustrate the function flow for the controller Read and Write operations.

The controller is activated when the Read or Write instruction is loaded by IOT 6504. The control pcb will stop the operation of the drum, by an interrupt system, if the drum becomes inoperable during data transfers (low voltage, not up to speed, heads not activated, high temperature).

Three tracks on the drum provide four clocks: ØA and ØB clocks are derived from one track and the Sector and Index clocks from the remaining two tracks.

The ØA and ØB clocks are pulses that occur 32,196 times each drum revolution. The pulses are evenly distributed around the drum and have a width of 125 ± 25 ns; they are 180^0 out of phase with each other (Figure 3-1). The ØA clock is not used by the Level 3 controller. The ØB clocks indicate the location of each bit cell on a track; they are used to synchronize the writing of data on the drum.

The Sector Clock pulse occurs 64 times each drum revolution, and is used to divide the data stored on each track into 64 blocks, or sectors. The pulse width is 275 ± 50 ns and envelopes the first ØB pulse of each sector by a minimum of 25 ns on either side (Figure 3-1). Each sector contains 503 bit cells (ØB pulses): data is stored in 480 cells, the cyclic redundancy check character (CRCC) is stored in 12 cells, and 11 cells are used to store the sector preamble/postamble pattern. The pattern is used for read data synchronization.

The Index Clock pulse occurs once each drum revolution. The pulse width is 275 ± 50 ns and envelopes the first ØB pulse by a minimum of 25 ns on either side. The Index Clock indicates the end of the sixty-fourth sector. Between the Index Clock and the first Sector Clock there are four bit cells which are used for sector synchronization.

A Read Clock signal is generated from the recorded data when data is read from the drum. The clock is used to synchronize the controller, because data will be shifted an unknown amount in relation to the clocks by the delay in the drum electronic circuitry and thermal effects on the drum surface. Since the Read Clocks are generated from the recorded data a certain amount of bit-to-bit jitter will be present. The jitter does not exceed 100 ns and is defined as the difference between the maximum and minimum time between read clocks.

LEVEL 3 IOT INSTRUCTIONS

6501 Clear Drum Done Flag and Control.

This IOT clears the Drum Done Flag and Control. It also clears status bits 01, Sector Not Found and 03, Drum Data Error (See IOT 6512). Note that an interrupt to the CPU is generated when the Drum Done Flag is set. The Drum Done Flag and Control, and Status bits 01 and 03, are also cleared by B Run when the CPU is in the stop mode.

6502 Load Drum Sector Address.

The six bit binary number in AC 06 to AC 11 is transferred to the sector address register to be used as the starting sector for the data transfer, and the accumulator is cleared. To be valid the value specified must be 0_{10} to 63_{10} inclusive. A value greater than 63_{10} is illegal and will result in no data transfer to or from the drum if a transfer is commanded by IOT 6504. Status bit 01, Sector Not Found, will be set with the Drum Done Flag in response to the illegal command.

6504 Load Drum Track Address and Initiate Read/Write Transfer (AC 00 = 0 initiates drum read, AC 00 = 1 initiates drum write).

The nine bit binary number specified in AC 03 to AC 11 is transferred to the track address register, a data transfer to or from the drum is initiated, and the accumulator is cleared. When this IOT is issued the binary value of AC 00 is sensed. If AC 00 is a 0 data is read from the drum into the CPU memory, starting from the specified track and sector. If AC 00 is a 1 data is written onto the drum from the CPU memory, starting at the specified track and sector. Only AC bits 05 to 11 are sensed on a 1004S (128 track) drum, and hence the binary number may be 0 to 127_{10} inclusive. A larger number will result in track address 'wraparound'. i.e. a track address of 128 is identical to specifying track address 0. Similarly wraparound occurs at tracks 256 and 512 respectively for the 1016 256-track and 1016 512-track drums. This feature may be used by the software to sense the size of drum installed in a system.

Since this IOT initiates drum data transfers, all IOTs for specifying Word Count, Current Address, and Sector Address must have been previously executed if a valid transfer is to occur.

6511 Skip If Drum Done Flag Is False.

If the Drum Done Flag is false the CPU program counter is incremented by one so that the next sequential instruction is skipped.

6512 Read Drum Status.

The accumulator is cleared and the drum status bits are transferred to the accumulator. The accumulator bits will be a binary 1 when the stated condition is true:

AC 00	Drum Not Operational
AC 01	Sector Not Found
AC 02	Drum Control Busy
AC 03	Drum Data Error

AC 00 Drum Not Operational.

This bit will be a binary 1 if any of the following conditions are true:

a. Power not applied to drum
b. Drum not up to speed
c. Drum heads not activated
d. Drum ambient temperature above 100F (38C) — corresponds to an internal drum temperature of 118F (48C).

The Drum Done Flag will be set if Drum Not Operational and Drum Control Busy are true.

AC 01 Sector Not Found.

This bit will be set if the selected sector address is greater than 63_{10} and the controller is activated via IOT 6504. It is always accompanied by status bit 02, Drum Control Busy, and will set the Drum Done Flag. This bit is cleared by IOT 6501 or B Run when the CPU is in the stop mode.

AC 02 Drum Control Busy.

This bit is set when IOT 6504 is issued. It is normally cleared after the data transfer requested is complete and the last cyclic Redundancy Check Character (CRCC) is generated or checked. This bit is also cleared by IOT 6501 or B Run when the CPU is in the stop mode.

AC 03 Drum Data Error.

This bit is set if the cyclic redundancy check circuitry indicates a data error after a drum read of one twelve bit word added to each 40 word sector produced using the generating polynominal:

$$x^{12}+x^{11}+x^{3}+x^{2}+x^{1}+1 \quad \text{(IBM CRC-12)}$$

The CRCC is automatically generated and checked by hardware and is not available to be read by the software. This status bit should be checked after every drum read operation. If it is set a number of re-reads may be attempted to establish whether the error is recoverable (read error) or non-recoverable (write error). Bit AC 03 is reset by IOT 6501 or B Run when the CPU is in the stop mode.

6514 Set Drum Done Flag.

This command sets the Drum Done Flag and hence generates an interrupt to the CPU. The complete equation for setting the flag is:

Set Drum Done Flag = IOT 6514
+ Data Transfer Complete (including CRCC)
+ (Drum Not Operational·Drum Control Busy)
+ (Sector Not Found·Drum Control Busy)

6522 Load Word Count.

The binary number contained in the accumulator is transferred to the word count register and the accumulator is cleared. This binary number is interpreted as the two's complement value of the total number of data words to be transferred. Minimum number of words is two; maximum number of words is 2560_{10} (complete track).

6524 Load Current Address.

The binary number contained in the accumulator is transferred to the current address register and the accumulator is cleared. This binary number is the CPU memory address of the first data word in the transfer.

6544 Load Extended Current Address.

The extended current address is loaded from bits AC 06, 07, and 08 (AC 06 most significant, AC 08 least significant), and the accumulator is cleared. Note that the extended current address is not incremented when the current address changes from 7777 to 0000. Because the three bits are loaded, drum transfers may take place into any of the eight PDP-8 memory fields.

It is possible to write multiple sectors with this controller. For example a starting sector of 42 could be specified and the word count set to 240_{10} words. This would result in writing or reading of sectors 42_{10} through 47_{10} in one drum operation. Becuase the last sector (63_{10}) is the same as every other sector it is possible to do multiple sector transfers across the boundary between sector 63_{10} and sector 0_{10}.

The Drum Control pcb handles the drum track and sector selection, the stop/start sequences, the words per sector count, illegal operations, and controller status.

TRACK SELECTION

The track select command pulse from the CPU, IOT $\overline{6504}$ at connector pin B21 (bottom centre), is inverted and clocks the Track Select flops H3, F3, and D3-5 to store the track addressing data BAC 03 to BAC 11, at connector pin group B39 to B10 (bottom right). The nine bits of stored data are applied to the drum, via connector pin group F to 8 and Z, to be decoded to prepare the selected track for use.

SECTOR SELECTION

The sector command pulse from the CPU, IOT $\overline{6502}$ at connector pin B19 (bottom centre), is inverted and clocks the Sector Select flops H2 and F2 to store the available sector address data, BAC 04 to BAC 11, at connector pin group B8 to B10. The flop outputs are applied to an 8-bit comparator (H1, F1) which indicates equal status at E3-8 when the Static and Current Sector flop values are equal.

The drum issues sector clock pulses as it rotates through each sector. The clocks are applied to the pcb at connector pin V (top right) and pass through NAND gate B3-6 and IOT gate B3-11 to clock the Sector Counter at E1-14. The counter (E1-G1) counts sector clocks and the 8-bit outputs are sensed at the comparator inputs with the Sector Select flop outputs. When the outputs from the counter and select flops match at the comparator the output of E2-8 will go low to the D input of the Match flop, D1-5.

The Track Select Command triggers the 40 µs monostable, HJ4, which inhibits the comparator for 40 µs. The delay allows for track switching time before a sector compare occurs.

The drum produces an Index Clock at each complete revolution and applies it via connector pin J to reset the Sector Counter at G1 and E1 pin 2. The clock also pulses the Sector Not Found circuitry – G4-11 and the two G2 flops.

The Match flop is released at pin 4, after a 40 µs delay, by the Drum Controller Busy line when either of the Start flops, C3-5 and C3-9 (bottom left), are set. The flop is clocked by the next Sector Clock, from connector pin V via C2-8 and C1-8, after the Match is made. The Match is allowed when Drum Break Request, at connector pin B24, and $\overline{\text{Match}}$ (D1-5) are high on C2-8 pins 10 and 9. The flop $\overline{Q}$ output is applied to NAND gate E3-12 pin 1. The gate output resets the 40 Word Counter B1, B2, and also activates the Drum Data pcb, 10284, via C1-3 and connector pin B36. The output of E3-12 is inhibited by the $\overline{\text{Sector Clock}}$ and any interrupt condition present on pins 2 and 13 respectively.

START/STOP SEQUENCE

Prior to a Write or Read sequence the sector and track are selected. The condition of BAC 00 determines whether a Read or Write Start sequence will occur (0 = Read, 1 = Write).

The Start sequence commences after the 40 µs delay when either of the C3 Start flops set, depending on the condition of BAC 00 at connector pin B35 (bottom left) when IOT $\overline{6504}$ is issued.

If either flop is clocked by IOT $\overline{6504}$ via inverter E4-6, and the 40 µs monostable is not activated, the $\overline{Q}$ output drives C4-6 true, via B4-3 and B4-11. This true output is the Drum Controller Busy state. NAND gate F4-4 (right side) senses the busy state on pin 6, and IOT 6512 on pin 5, to provide the $\overline{\text{AC 02 In}}$ level to the CPU at connector pin B16.

The Control Busy state also releases the set input to the Match flop, D1-5 pin 4. The flop D input is the sector match and the C input is the Sector Clock (with conditions); when both inputs are true the correct sector has been reached and the flop will lock until the Controller Busy state terminates.

The Q outputs from the Start flops will also make Read Match or Write Match true, at connector pins B31 and B38 respectively, to enable the data pcb, 10284, in the correct mode. Write Match will activate the drum write drivers via the data pcb. The Read Match signal also activates the Derandomizer pcb, 10262.

The Stop sequence is effected by resetting the C3 Start flops. A word count overflow condition will be applied from the Word Count and Current Address pcb (WC & CA), 10442, via connector pin B28 (WC Overflow) to reset the D2 R-S flip-flop. The fortieth word of a sector condition will be transferred from the 40 Word Counter via A2-12 and B4-6, and the Inhibit Shutdown, at connector pin B41 (during a write mode), will indicate that the Derandomizer pcb is empty. These conditions will be strobed from connector pin V at Sector Clock time to enable NAND gate A4-6, whose output is routed via E2-6 and B3-3 to reset the Start flops.

The Drum Flag flop, D3-9, sets when the Drum Controller Busy state terminates. The $\overline{Q}$ output, Drum Flag, applies an interrupt to the CPU via IOR gate E3-8, inverter H4-13, and connector pin B20 (detailed in the subsequent Illegal Operation and Controller Status description).

The Drum Break Request flop, D1-9, will reset active when the 1 to Drum Break Request level from the derandomizer goes true at connector pin B33 (note that the flop operates in reverse). The flop set can be inhibited by a WC Overflow at connector pin B28, or by the Start flops being reset.

WORDS PER SECTOR COUNT

When the data pcb is activated the transfer of each word to or from the drum is marked by a LWLB (Last Word Last Bit) pulse at connector pin B34. The pulses clock the 40 Word Counter – C1, B2 – and the 40 Word signal at connector pin B40 will go true, via A2-12, on a count of 40_{10} (50_8). The signal causes the data pcb to do a CRCC write, or a read and check, and also permits the control pcb shutdown. The counter is reset by the next Sector Clock.

ILLEGAL OPERATION AND CONTROLLER STATUS

An Illegal status can only occur when the Drum Not Operational and Busy conditions are true. The illegal status will not develop if the drum is active and sector synchronization is possible.

The failure-to-synchronize condition is called Sector Not Found. The status occurs when the controller is active and the two flops, G2-5 and G2-9, count two Index Clocks from connector pin J (right side). If the static and current sector values do not match before one drum rotation the second stage of G2 will set; the $\overline{Q}$ output will apply an Interrupt level to the CPU, with the Drum Flag state, via E3-8 and GH4-13 to connector pin B20. G2-9 Q output is sensed with IOT 6512 at NAND gate F4-1 to present AC 01 In to the CPU via connector pin B17.

The Drum Status Switch (right side) will not set when the ac power is below 107 (or 198 or 216) vac, the temperature exceeds 100F (38C), the drum heads are not activated, or the drum is not up to speed. Any of these conditions will set the G3 Illegal R-S flop, via connector pin N and G4-3. The flop will apply an Interrupt to the CPU at connector pin B20. The Drum Status Switch is sensed with IOT 6512 at F4-13 to provide AC 00 In to the CPU at connector pin B11.

The Drum Data pcb provides controls for the transfer of data between the CPU and drum. It exerts five controls on the system (Figure 3-5):

1. Word Handling (Drum Read Buffer, Shift Register, Preamble)
2. Read Control
3. Write Control
4. Word Control
5. CRCC Generation and Check

Figures 3.6 and 3.7 illustrate the pcb Read and Write operation functional flow.

WRITE DATA

The write sequence starts when the $\overline{\text{Write•Match}}$ level at connector pin B11 (bottom left) goes true (ground). The level is generated by the Control pcb, 10282, at the beginning of the selected sector (sector clock time). It is routed via connector pin B11, inverter G4-3, and connector pin 5, as the Write Enable signal to the drum to activate the drum write drivers.

Simultaneously the $\overline{\text{Sector Clock}}$ level at connector pin B14 goes true for 275 ns. It is inverted by F5-1 and applied to NAND gate H1-8 pin 9. $\overline{\text{Write•Match}}$ (from connector pin B11) is inverted by G5-6 and applied to H1-8 pin 10. The gate output will then be true (ground), and be applied to:

1. NAND gate B2-6 to inhibit the Load•$\overline{\text{Preamble}}$ pulse from being issued to the Derandomizer pcb, 10262, via connector pin B16.
2. J2-9 pin 10 to set the Write Preamble Flag flip-flop.
3. The Preamble Insertion circuit – B5, C5, and D3-12 – to insert the 1100001 preamble data.
4. IOT gate I2-6 pin 5 to change the Shift Register – A4, B4, C4 – from a serial to a parallel shift mode.

Except during preamble load the Load $\overline{\text{Preamble}}$ signal is true when the Shift Register is in the load mode.

Write Preamble

Refer Figure 3-8, Drum Data Write Timing.

The conditions are set for Preamble activation, as described above. The $\overline{\text{Write•Match}}$, connector pin B11, and Match•$\overline{\text{Sector Clock}}$, connector pin B13, control levels are true at the beginning of a sector to activate the pcb. NAND gate H1-8 is enabled to activate the Preamble Insertion NAND gates. The preamble pattern of 1100001 is then presented to the Shift Register – B4, C4. The register is in a serial mode to present data serially to the drum when Sector Clock goes false. The drum circuitry synchronizes on the 0 to 1 transition, and the data pcb synchronizes during the final 1. The pattern is applied to the register at the beginning of each sector. All data words are supplied from the derandomizer.

The $\overline{\text{Sector Clock}}$ directly resets the Bit/Word Counter via G2-6 pin 2, and Match will release this direct reset.

Preamble Load

The preamble pattern is activated when ØB, connector pin D, and $\overline{\text{Write•Match}}$, connector pin B11, both go true. ØB is true for 125 ns; $\overline{\text{Write•Match}}$ is inverted by G5-6. Consequently H1-11 clocks the Shift Register, pins 12 and 13, via G2-8.

Therefore the register is in the load mode (Write Match and Sector Clock), the clock is present (ØB and Write Match), and the preamble pattern is available at the NAND gates while D3-12 is enabled: the 7-bit pattern is then loaded on the negative-going trailing edge of ØB.

The Sector Clock terminates before the arrival of the next ØB and returns the Shift Register to the serial mode. $\overline{\text{Match}\cdot\text{Sector Clock}}$ goes true and, via G2-6 and I2-8, releases the reset on the Bit/Word Counter — flops J2-5 to J5-5.

NOTE: The counter shift-reset and the register shift-load occur on the pulse trailing edge.

The Bit/Word Counter will start incrementing on the next ØB, via G4-6. The counter Q outputs are initially all zeros, and successive ØB pulse trailing edges shift all ones from left to right. Simultaneously the data in the Shift Register is being shifted left to right.

The register preamble pattern at C4-2 is sensed at NAND gate D4-3 pin 1; pin 2 is true until 40 data words have been counted. D4-3 therefore enables D5-12 which applies a Write Data level to the drum circuitry via connector pin S. This level causes the pattern to be written on the drum.

The counter will start to shift all zeros from left to right after six ØB pulses (ones) have been counted. When counter flop J5-9 is true at the count of six the output of NAND gate I4-12 will go true; I4-12 pin 2 was enabled by the Write Preamble Flag J2-9. I4-12 output, via I2-6, returns the Shift Register to the load mode

Write Data

The first data word is to be loaded into the Shift Register in parallel and shifted out serially.

The trailing edge of the seventh ØB pulse increments the Bit/Word Counter and loads the first data word from the derandomizer, OB 00 to OB 11, into the Shift Register via connector pin group B18 to B26. Simultaneously $\text{Load}\cdot\overline{\text{Preamble}}$ will go true to the derandomizer. When counter flop J5-5 Q goes false connector pin B16 will go true via I5-3, I5-6, I3-11, and I2-6. The drum writes the last bit on the positive-going leading edge of ØB.

NAND gate I4-6 resets the counter via G2-6 and I2-8. I4-6 is true when the Write Preamble Flag is set (to pin 3) and the counter is at a count of seven (to pins 4 and 5). The reset condition invalidates NAND gate I4-12 and removes the register load mode via I2-6, which terminates the $\text{Load}\cdot\overline{\text{Preamble}}$ to the derandomizer via B2-6. The pulse trailing edge at connector pin B16 causes the derandomizer to transfer the next data word from its Output Buffer into the Shift Register. I4-6 is invalidated by the counter reset; the positive-going trailing edge of the pulse resets the Write Preamble Flag, pin 11, and removes the counter reset via J2-9, I4-6, G2-6, and I2-8.

Thus the preamble sequence is complete; the first data word is in the Shift Register (in serial shift mode), and the derandomizer is transferring the next data word from the RAM to its Output Buffer, which requires between 400 and 800 ns.

The subsequent 11 ØB pulse trailing edges will shift the data word in the register and increment the counter. Write Select at connector pin B11 is true (gnd), G5-6 is false, and I3-11 pin 12 is enabled. The trailing edge of pulse 11 conditions counter J4-5 pin 6; I5-3 goes true to I5-6, I3-11 goes true to I2-6 to condition the register in a load mode. I2-6 output also causes the $\text{Load}\cdot\overline{\text{Preamble}}$ at connector pin B16 to be true.

The counter reset condition removes the load mode from the register via I5-3, I5-6, I3-11, and I2-6. It also terminates the $\text{Load}\cdot\overline{\text{Preamble}}$ level to the derandomizer which causes it to transfer the next data word from the RAM to the Output Buffer.

Thus the first data word has been shifted through the registers and the second data word has been loaded into the register, the Bits/Word Counter is reset, and the derandomizer is internally transferring the next word.

The previous procedure of processing one data word is repeated for every 12 ØB clocks for 40 words per sector. The forty-first word is the CRCC word.

WRITE CRCC

The Cyclic Redundancy Check Character (CRCC) is one 12-bit word added to each 40 word sector produced, using the generating polynomial:

$$x^{12}+x^{11}+x^{3}+x^{2}+x+1$$

where x is the position of the exclusive OR gates in the register.

When the cyclic word is added to the 40 data words the CRCC will have a sum of all zeros. The CRCC generator (flops F1 to A1), top left, is concurrently generating the CRCC while the 40 data words are being written. The final value is derived at the end of the fortieth word. The CRCC is a serial device whose clocking (trailing edge positive-going) is derived from power NAND gate G1-8. The gate is enabled by the Write Preamble Flag being reset (G1-8 pin 9 from J2-9 pin 8), and the clock pulses to the Shift Register (G2-8). The clock pulses are all ØB after the Preamble has been written. Since the CRCC is sector orientated it is reset by $\overline{\text{Sector Clock}}$, connector pin B14, via F5-1 and power gate G1-6.

The CRCC data is supplied by the Least Significant Bit (LSB) of the Shift Register. The output C4-2 is applied to NAND gate D5-8 pin 9; the other two gate inputs are enabled because $\overline{\text{Write}\cdot\text{Match}}$ is true from connector pin B11 via inverter G5-6 to pin 11, and $\overline{\text{40 Word}}$ is true to pin 10. The 40 Word signal will go true when the Drum Control pcb detects that 40 words have been transferred to the drum during a sector. IOR gate D2-6 pin 4 reflects the state of the LSB from the register via D5-8. The data is then presented to XOR gate E2-13 pin 14; pin 15 input is derived from the LSB of the CRCC Generator (part of formula) from A1-9 via D4-6 and D3-6. E2-13 output is applied to the XOR gates and the D input of the generator. Therefore the Write Data bit is added to the CRCC Generator.

The first 40 words of the register LSB (C4-2) are applied to NAND gate D4-3 pin 1; pin 2 is enabled because NAND gate D4-11 is not true when the $\overline{\text{40 Word}}$ signal is not true. When $\overline{\text{Write}\cdot\text{Match}}$ (connector pin B11) enables pin 2, via D4-11, D4-3 inverts the state of the register LSB and applies it to IOR gate D5-12 pin 1. D5-12 is routed via connector pin 5 to the Write Data input of the drum. This level is clocked into the drum write circuitry for each ØB pulse (leading edge, positive-going). When $\overline{\text{Write}\cdot\text{Match}}$ is not true during a read sequence D5-12 pin 2 is held low to avoid unnecessary line fluctuations to the drum.

When $\overline{\text{40 Word}}$ goes true (gnd) the fortieth data word of the current sector has been written, and the CRCC value is to be gated to the Write Data line, connector pin S, as the next word to be written. The $\overline{\text{40 Word}}$ signal, via D3-2, enables D4-8 pin 9. The LSB of the CRCC (A1-9) is applied to D4-8 pin 10 and D4-8 goes to Write Data via IOR D5-12 and connector pin S. The normal data is then inhibited by NAND gate D4-3 pin 2 being disabled by NAND gate D4-11 true ($\overline{\text{40 Word}}$ and $\overline{\text{Write}\cdot\text{Match}}$ true).

D4-11 also inhibits NAND gate D4-6 pin 4 and prevents the CRCC LSB from reaching the XOR gate E2-13. This forces E2-13 pin 15 low, pin 14 is low because D5-8 is inhibited at pin 10 by 40 Word true. Therfore E2-13 goes low. The data input is always low, which forces all XOR gates in the CRCC Generator to function as non-inverting buffers between stages. Thus the CRCC Generator is effectively a normal shift register. The data is then shifted left to right to the Write Data line without being altered by the XOR gates. At this time $\overline{\text{40 Word}}$ also inhibits Load$\cdot\overline{\text{Preamble}}$ (B2-6) and the Read Last pulses at I4-8 pin 9 (explained in READ DATA) because no data words are being transferred.

The contents of the CRCC Generator are shifted to the Write Data line in 12 bit times. Because the Sector Clock is only three bit times away after the last CRCC bit has been written the shifting is allowed to continue past 12 clocks. These three bits are Postamble bits whose binary value are of no consequence.

When the $\overline{\text{Sector Clock}}$ arrives at connector pin B14, Match·$\overline{\text{Sector Clock}}$ goes false for the duration of $\overline{\text{Sector Clock}}$ to reset the Bit/Word Counter and start the same sequence as described in WRITE DATA. If the Drum Control pcb, 10282, requires a shutdown it will occur at the beginning of $\overline{\text{Sector Clock}}$. $\overline{\text{Write·Match}}$ will go false and Match·$\overline{\text{Sector Clock}}$ will stay false and terminate all Drum Data pcb write functions.

READ DATA

When the Write Enable line to the drum is not true, at connector pin 5, the drum circuitry assumes a Read Enable state (Read Clock and Read Data are normally in evidence).

When $\overline{\text{Read·Match}}$ goes true at connector pin B15 at the beginning of Sector Clock the Drum Data pcb is put into a read mode. The Read Data line from the drum, connector pin W, is normally displaced by 1-1/2 bit times from the write timing. The first Read Data the drum will produce is the preamble pattern in the form XXXXX00001 (refer to Figure 3-9). The read control will enable the read clocks in the middle of the zeros, and do a final synchronization on the trailing edge of the clocked 1 — in the following manner.

When $\overline{\text{Read·Match}}$ is true it releases Read Sync Flag 1 — F4-5 pin 1. The flag is set by $\overline{\text{Sector Clock}}$ at connector pin B14, via F5-1 and NAND gate F5-10 pin 8 (F5-10 pin 9 is enabled by $\overline{\text{Read·Match}}$).

Read Sync Flag 1 set permits ØB pulses (connector pin D) to increment the Bit/Word counter via NAND gate G4-6 and IOT gate G4-8. G4-6 pin 4 is enabled by Read Sync Flag 1 $\overline{Q}$ output via G4-11 pin 12; pin 5 is enabled by the ØB pulses.

The first ØB is masked by Sector Clock: Match·$\overline{\text{Sector Clock}}$ does not release the counter until the completion of $\overline{\text{Sector Clock}}$. When six ØB clocks have been counted at J5-9 power NAND gate G5-8, pins 12 and 13, will go true and set Read Sync Flag 2; pin 9 was enabled by Read Sync Flag 1 set. When Read Sync Flag 2 sets it will:

1. reset Read Sync Flag 1, via its Q output to F4-5 pin 3, to prevent subsequent ØB clocks being routed to the counter.
2. enable Read Clocks to reach Read Sync Flag 3 (F3-5 pin 3) via connector pin 6, I1-4 and -6, and F2-3 pin 1.
3. hold the counter reset via F4-9 pin 8, G2-6, and I2-8.

The drum Read Data signal, connector pin W, should be in the middle of the preamble pattern zeros (Figure 3-9).

The Read Data level is applied to the D input of Read Sync Flag 3 — F3-5 pin 2. The flop is clocked by the trailing edge of the Read Clocks, and set by the trailing edge of the final 1 of the preamble pattern. When Read Sync Flag 3 sets it will:

1. reset Read Sync Flag 2 — F3-5 to F4-9 pin 11 — to release the counter — F4-9 pin 8 to G2-6 pin 4.
2. permit Read Clocks to:
   a. increment the counter via connector pin 6, I1-4, I1-6, F2-8, G4-8, and G3-8.
   b. issue clocks to the Shift Register via F2-8 and G2-8 (A2-3, A2-13) pins 9 and 10 (the drum Read Data is the serial data into the register at A4-10).

Thus, the preamble pattern has been read and the first data bit can be shifted into the register and counted by the counter.

There are no load modes to the register during a read operation.

When 11 data bits have been shifted into the register NAND gate I5-3 will be true from J5-5 and J4-5 pin 6 to inverter I5-6, which will enable power NAND gate G3-6, pins 1 and 2, on the trailing edge, to accept the twelfth Read Clock, via F2-6 and F2-8, at pins 4 and 5.

$\overline{\text{Read Last}}$, connector pin B29, is also true via NAND gate I4-8 pin 11 from I5-6 (counter = 11); pins 9 and 10 are enabled by $\overline{\text{40 Word}}$ being false and Read Sync Flag 3 respectively.

When the twelfth Read Clock trailing edge arrives the register data will be strobed by G3-6 into the Drum Read Buffer – A3, B3, C3. The Most Significant Bit (MSB) of the buffer accepts data directly from the drum Read Data line, connector pin W to A3-15.

The counter is then a 12 and NAND gate I5-11 will be true (gnd) to produce $\overline{\text{LWLB}}$ at connector pin B10 and also reset the counter via G2-6 pin 1. The $\overline{\text{LWLB}}$ signal indicates to the Drum Control pcb that a word has been transferred from the drum to the Drum Data pcb.

When the counter resets it will:

1. terminate $\overline{\text{LWLB}}$ via I5-11
2. invalidate G3-6 via I5-3 and I5-6
3. terminate $\overline{\text{Read Last}}$ via I5-6 and I4-8.

When the $\overline{\text{Read Last}}$ signal to the Derandomizer pcb terminates it indicates that a data word is available on DRB lines 00 to 11, connector pin group B17 to B42.

Thus the first data has been read and is stored in the Drum Read Buffer. It is then presented to the Derandomizer, which takes 100 ns to transfer the data to its Input Buffer (Derandomizer description, BMB to RAM), and the counter resets.

The remainder of the 40 data words are handled in the same manner. The forty-first data word is the CRCC word.

READ CRCC

The CRCC is a check word injected as the forty-first word of a sector. When the check word is added to the other 40 words the result is zero. The read operation checks the total, and sets an error flag if it is not zero.

The CRCC Generator is clocked by the same pulses as the Shift Register (Read Clocks after Preamble), via power gates G2-8 and G1-8 pin 10 (Write Preamble flag is false on pin 9). Read Data is applied to the generator via connector pin W, D2-8 pin 9 (top right, pin 10 is enabled by Read Sync Flag 3), D2-6, and E2-13 pin 14.

The 40 data words and one CRCC word are clocked into the register and checked for zero total by B2-8, C2-8, and E3-4. E3-4 output is applied to the CRCC Read Error Flag D input. The positive-going trailing edge of D5-6 clocks the flop at pin 11.

D5-6 is true when the following are true:

1. $\overline{\text{40 Word}}$ (pin 5), via connector pin B5 and inverter D3-2
2. $\overline{\text{LWLB}}$ (pin 3), from the counter via I5-11 and I5-8
3. $\overline{\text{Read·Match}}$ (pin 4), via connector pin B15 and I1-2

Therefore the NAND gate produces a pulse after the twelfth bit of the forty-first word (CRCC word) has been read.

The Read Error Flag will reset and lock-up (Q to R) if it is clocked while its D input is low. The flag is sensed by IOT 6512, connector pin B6, at NAND gate F5-13 to produce AC 03 In true, the CRCC Error, at connector pin B8. The flag is set by $\overline{\text{Drum Write Sync}}$, connector pin B3 (B Run + IOT 6501).

The Derandomizer pcb consists of six parts (Figure 3-10):

1. Random Access Memory (RAM) and flags
2. Input Buffer, with mixer and flags
3. Output Buffer, with drivers and flags
4. Read Control
5. Write Control
6. Data Break Control

Figure 3-11 illustrates a functional flow for a read operation. There are two simultaneous operations: Start illustrates the function of a data transfer from the Drum Data pcb, 10284, to the RAM; Start-1 illustrates a data transfer from the RAM to the CPU. Since the RAM can only perform one function at a time the broken line shows the conflict in timing between the two operations. When a conflict occurs the RAM functions on a first-come first-served basis, with the latest operation delayed until the first is completed.

Figure 3-12 illustrates a functional flow for a drum write operation. The same simultaneous operations occur as in Figure 3-11: Start is for CPU to RAM; Start-1 is for RAM to Drum Data pcb.

The Derandomizer pcb performs five functions:

1. Data transfers from BMB data lines (BMB 00 to 11) to the RAM
2. Data transfers from the Drum Data Read Buffer (DRB 00 to 11) to the RAM
3. Data transfers from the RAM to the CPU Data In lines (Data 00 to 11)
4. Data transfers from the RAM to the Drum Data In lines (OB 00 to 11)
5. Initiates Drum Break Requests

BMB TO RAM (DRUM WRITE)

Break requests are enabled when a write command is issued to the control pcb. When the CPU responds with an Address Accepted level a pulse is issued via the Drum and MTT Multiplexor pcb, 10298, as $\overline{\text{MB Out to Drum Data}}$ at connector pin B7; the data appears as BMB 00 to BMB 11 at connector pin group B18 to B26. The pulse is delayed for 50 ns by inverters C2-12 and C2-10, then applied to power driver B2-6 to drive the Input Mixer NAND gates – B5, B4, and B3 (bottom right). The mixers put the inverted data levels to the Input Buffer – C5, C4, C3. The pulse at B7 is also applied through IOR gate B1-8 and power driver H1-6 to set the Input Buffer Flag, G2-9 pin 10, and load the RAM Input Buffer on its trailing edge.

When the Input Buffer flag is set, the pulse $\overline{\text{MB Out to Drum Data}}$ is complete, the RAM is not full, and a Read sequence is not in progress, then all the input conditions are met and H1-8 will be true (gnd). NAND gate H1-8 output determines the start of a data transfer from the Input Buffer to the RAM – D3, D4, D5. The value of Write Address Scaler – flops D1-5 and D1-9 – is routed via F1-6 and H2-6 and applied to the RAM Address Lines 1 and 0. The RAM Select Line 1 – D5-2, D4-2, D3-2 – is enabled by IOR gate F2-8 and inverter H4-7. The RAM data inputs – D5, D4, and D3 pins 4, 6, 10 and 12 – are applied by the Input Buffer. When all inputs are true inverter C2-4 (lower left) initiates the timing sequence (Figure 3-13). Inverters C2-4, A2-2, and A2-4 provide a 120 ns delay for selection settling time. The Write Enable level at D2-6 is applied to the RAM (D5, D4, and D3 pin 3); after 100 ns inverters A2-12 and A2-10 inhibit NAND gate D2-6. The positive-going trailing edge increments the RAM Scaler (C1, 4-bit shift register, top left) via IOR gate D2-3 and inverter D2-8. C1-9 is asserted as an increment mode via H1-8 and G1-12.

Inverters A2-6 and B1-11 (bottom left) provide a 50 ns delay after Write Enable conclusion, then reset the Input Buffer flag. The reset flag disables H1-8 to terminate the write sequence. Inherent delays in the flops add another 50 ns delay before shutdown. The termination increments the Write Address Scalers, D1-5 and D1-9, through B1-3.

DRB TO RAM (DRUM READ)

The Drum Read Buffer transfers to the RAM are initiated by the $\overline{\text{Read Last}}$ pulse, connector pin B13, from the Drum Data pcb, 10284. The positive-going trailing edge indicates that the read data has been strobed into the DRB (DRB 00 to 11). Inverters H2-3 and H5-6 provide a 100 ns delay to permit the DRB data lines to settle. The delayed pulse is further delayed for 50 ns via H4-2, C2-2, and B2-8 to the Input Mixer gates, A5, A4, and A3 (similar to MB Out to Drum Data). The pulse from B13 is also applied through IOR gate B1-8 and power driver H1-6 to set the Input Buffer Flag. The sequence is then the same as described in the previous section, BMB to RAM.

RAM TO CPU (DRUM READ)

The status of the Output Buffer Flag, G2-5 establishes read operations from the RAM. The $\overline{\text{Drum Write Sync}}$ signal, connector pin B29, initializes the Derandomizer and resets both the Input and Output Buffer Flags, and also both the Read and Write Address Scalers. The flag reset will demand data from the RAM via NAND gate F2-6. The other gate input conditions are RAM not empty, F2-6 pin 3, and Write Control not active, pin 4. When the input conditions are true F2-6 will be true (gnd) and initiate a Read operation. The Read Address Scaler, flops E1-5 and E1-9, gates the RAM Address Lines 0 and 1 via NAND gates F1-8 and F1-11. The RAM Select Line goes true via F2-8, pins 9 and 10, and H4-7.

All inputs to the RAM are then satisfied and the read timing sequence is initiated by inverter G1-10 (from F2-6), which provides a 150 ns delay to permit the RAM to perform its read operation. NAND gate F2-12 produces a signal, buffered through power driver E2-6, to strobe the RAM contents to the Output Buffer, E3, D4, and E5, pins 4 and 13. Inverters G1-4 and G1-2 insert a 100 ns delay before setting the Output Buffer Flag; F2-12 pin 13 then goes false and terminates the strobe. The negative-going trailing edge of the delayed pulse from E2-6 strobes the data into the Output Buffer; the positive-going trailing edge at F2-12 increments the Read Address Scaler, E1-5 pin 3, and applies a clock pulse to the RAM Scaler Flag via D2-3 pin 1 and D2-8. Because a Write mode does not exist (H1-8) the RAM Scaler Flag is decremented at pin 9 by the mode change. When the Output Buffer Flag sets F2-6 pin 5 will go false and terminate the Read operation after a 50 ns gate/flag propagation delay (Figure 3-14).

Thus, when the Output Buffer is full the drum data break request control will place a request to the CPU (refer Drum Break Request Initiate explanation) providing the RAM is not full. The CPU will respond via the multiplexor pcb with the pulse Drum Data to MB In, connector pin B23. The pulse is routed directly to the Output Driver NAND gates, G5 to G3, to transfer the Output Buffer data to the CPU data input lines, $\overline{\text{Data 00}}$ to $\overline{\text{Data 11}}$. The same pulse is also routed via NAND gate H5-3 pin 2 (pin 1 is $\overline{\text{Write Select}}$) H4-6 and NOR gate H3-1 to reset the Output Buffer Flag on the positive-going trailing edge. The flop D input is at ground during a Read operation.

The Output Buffer Flag reset will initiate another RAM to Output Buffer operation if all other conditions of F2-6 are met.

RAM TO DRUM DATA INPUT (DRUM WRITE)

When the Drum Data pcb is loading the data from the Output Buffer (OB 00 to OB 11) into its Shift Register the Load·$\overline{\text{Preamble}}$ pulse is applied to connector pin B16. The pulse is delayed for 100 ns by H5-8, C2-6, and C2-8 before being applied to H3-1 pin 2. The delay provides a wait for the $\overline{\text{40 Word}}$ level at connector pin 3. The Output Buffer Flag D input is normally at ground to ensure the flag is reset to initiate another RAM to Output Buffer sequence. The forty-first word of a sector is the CRCC word, therefore the Load·$\overline{\text{Preamble}}$ must be made invalid. The 40 Word signal will be true at the completion of the fortieth word written after the Load·$\overline{\text{Preamble}}$ pulse terminates. The signal is applied via H3-13 pin 11 (pin 12 is enabled by $\overline{\text{Write Select}}$) and NAND gate A1-6 (pin 5 reflects the current status of the Output Buffer Flag) to the flag D input to ensure a 'no change' state of the Read Control.

DRUM BREAK REQUEST INITIATE

The RAM Scaler Flag is incremented by a Write operation completion, and decremented by a Read operation completion (BMB to RAM, and RAM to CPU explanations). C1 pin 11 is true (gnd) when the RAM is full; C1 pin 15 is false (gnd) when the RAM is empty.

The $\overline{\text{1 to Drum Break Request}}$ signal at connector pin B14 is produced by NAND gates H2-11 and F1-3. The signal conditions are:

1. Drum Write - Write Select is true at H2-11 pin 13, and the RAM is not full (C1 pin 11 is false).
2. Drum Read - Read Select is true at F1-3 pin 2, and the RAM is not empty (C1 pin 15 is true).

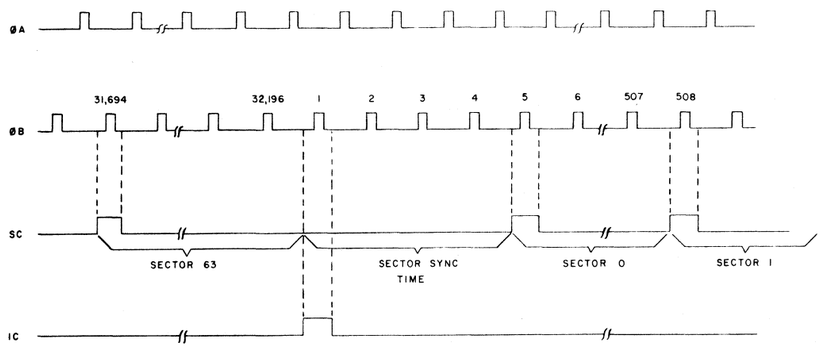
The Input and Output Buffer conditions are not sensed. The CPU will always respond with one additional break cycle to either take the last word from the Output Buffer (Drum Read), or put one to the Input Buffer (Drum Write).

The $\overline{\text{1 to Drum Break Request}}$ is conditioned at the Drum Control pcb, 10282, by the Word Count Overflow and Illegal circuits.

During a Drum Write operation the $\overline{\text{Inhibit Shutdown}}$, connector pin B6, indicates to the Drum control pcb that the Derandomizer is not empty. The conditions for a Drum Control shutdown are that all data words are completed from:

1. CPU to Derandomizer (Word Count Overflow)
2. Derandomizer to Drum Data (Derandomizer empty).

The shutdown circuit involves NAND gate H2-8, which is enabled by Write Select, and IAND gate H5-11. H5-11 pin 12 senses that the RAM is empty, and pin 13 senses that the Output Buffer is empty.

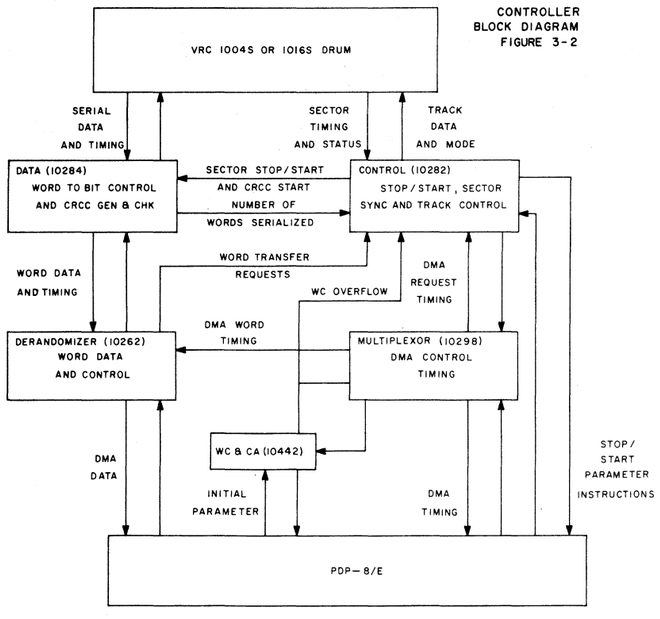


32,196 BITS/TRACK
503 BITS/SECTOR

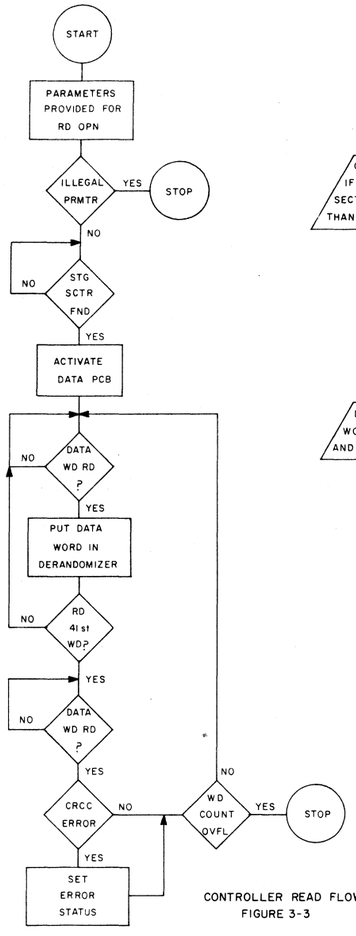
TRACK CLOCKING

ØA - 32,196 PULSES, WIDTH = 125NS ± 25NS.
ØB - 32,196 PULSES, WIDTH = 125NS ± 25NS, 180 DEGREES FROM ØA.
SC - 64 PULSES, WIDTH = 275 ± 50NS,
IC - 1 PULSE, WIDTH = 275 ± 50NS,
SC AND IC PULSES MUST ENVELOPE ØB PULSES BY A MINIMUM OF 25NS ON EITHER SIDE

CLOCK TIMING
FIGURE 3-1



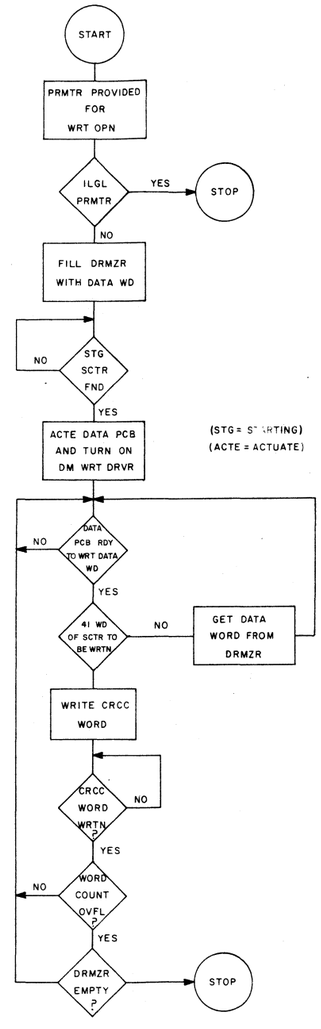
CONTROLLER BLOCK DIAGRAM
FIGURE 3-2



CONTROL PCB DETERMINES IF DRUM OPERABLE AND IF SECTOR SPECIFIED LESS THAN 6410

DERANDOMIZER WILL ACCEPT WORDS FROM DATA PCB AND TRANSFER TO CPU

CONTROLLER READ FLOW
FIGURE 3-3



CONTROL PCB DETERMINES IF DRUM OPERABLE AND SECTOR NUMBER < 6410

(STG = STARTING)
(ACTE = ACTUATE)

DERANDOMIZER WILL TRANFER WORD TO DATA PCB AND S GET NEW WORDS FROM CPU

IF THE DATA WORDS FROM THE DERANDOMIZER HAS STOPPED THE LAST DATA WORD IS REPEATED UNTIL THE CRCC WORD IS WRITTEN

CONTROLLER WRITE FLOW
FIGURE 3-4

rev	description	date	by	apprvd

used on
unless specified
fractions ± 1/64
.00 = ± .01
.000 = ± .005
angles = ± 0°30'
scale
date
material
finish
W Bourdon drawn
design apprvl
checked
final apprvl

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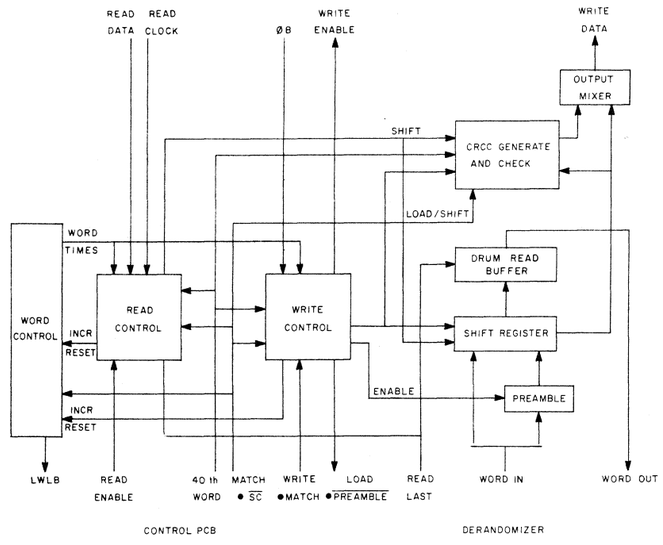
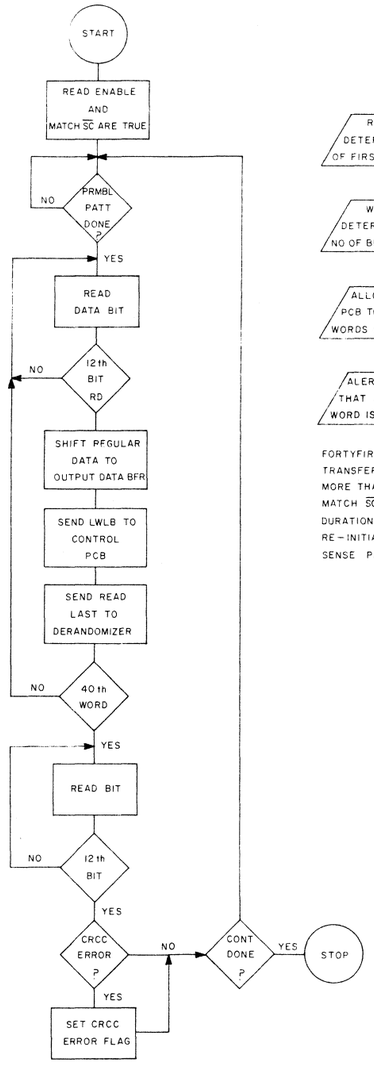
TORONTO-OTTAWA

title: DRUM CONTROLLER

sheet 1 of 1 no. DFIGURES 3-1, 3-2 3-3, 3-4 rev



DRUM DATA BLOCK DIAGRAM
FIGURE 3-5



DRUM DATA READ FLOW
FIGURE 3-6

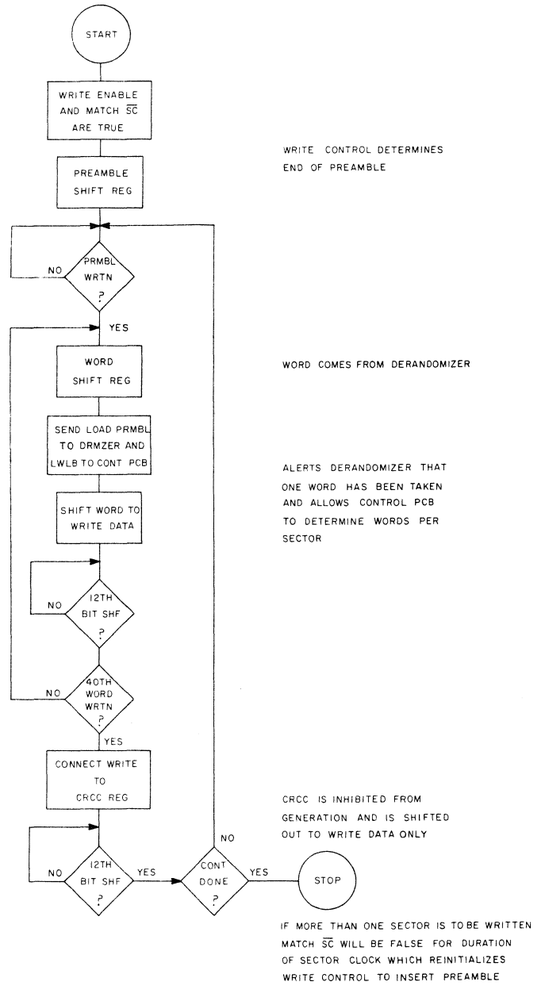
READ CONTROL DETERMINES START OF FIRST DATA WORD

WORD CONTROL DETERMINES THE NO OF BITS A WORD

ALLOWS CONTROL PCB TO DETERMINE WORDS A SECTOR

ALERTS DERANDOMIZER THAT ASSEMBLED WORD IS IN BUFFER

FORTYFIRST WORD OF SECTOR IS NOT TRANSFERRED AS A DATA WORD IF MORE THAN ONE SECTOR IS READ. MATCH $\overline{SC}$ WILL GO FALSE FOR DURATION OF SECTOR CLOCK TO RE-INITIALIZE READ CONTROL TO SENSE PREAMBLE



WRITE CONTROL DETERMINES END OF PREAMBLE

WORD COMES FROM DERANDOMIZER

ALERTS DERANDOMIZER THAT ONE WORD HAS BEEN TAKEN AND ALLOWS CONTROL PCB TO DETERMINE WORDS PER SECTOR

CRCC IS INHIBITED FROM GENERATION AND IS SHIFTED OUT TO WRITE DATA ONLY

IF MORE THAN ONE SECTOR IS TO BE WRITTEN MATCH $\overline{SC}$ WILL BE FALSE FOR DURATION OF SECTOR CLOCK WHICH REINITIALIZES WRITE CONTROL TO INSERT PREAMBLE

DRUM DATA WRITE FLOW
FIGURE 3-7

rev	description	date	by	apprvd

used on

unless specified
fractions ± 1/64
.00 = ± .01
.000 = ± .005
angles = ± 0°30'

scale | date

material

finish

drawn

design apprvl

checked

final apprvl

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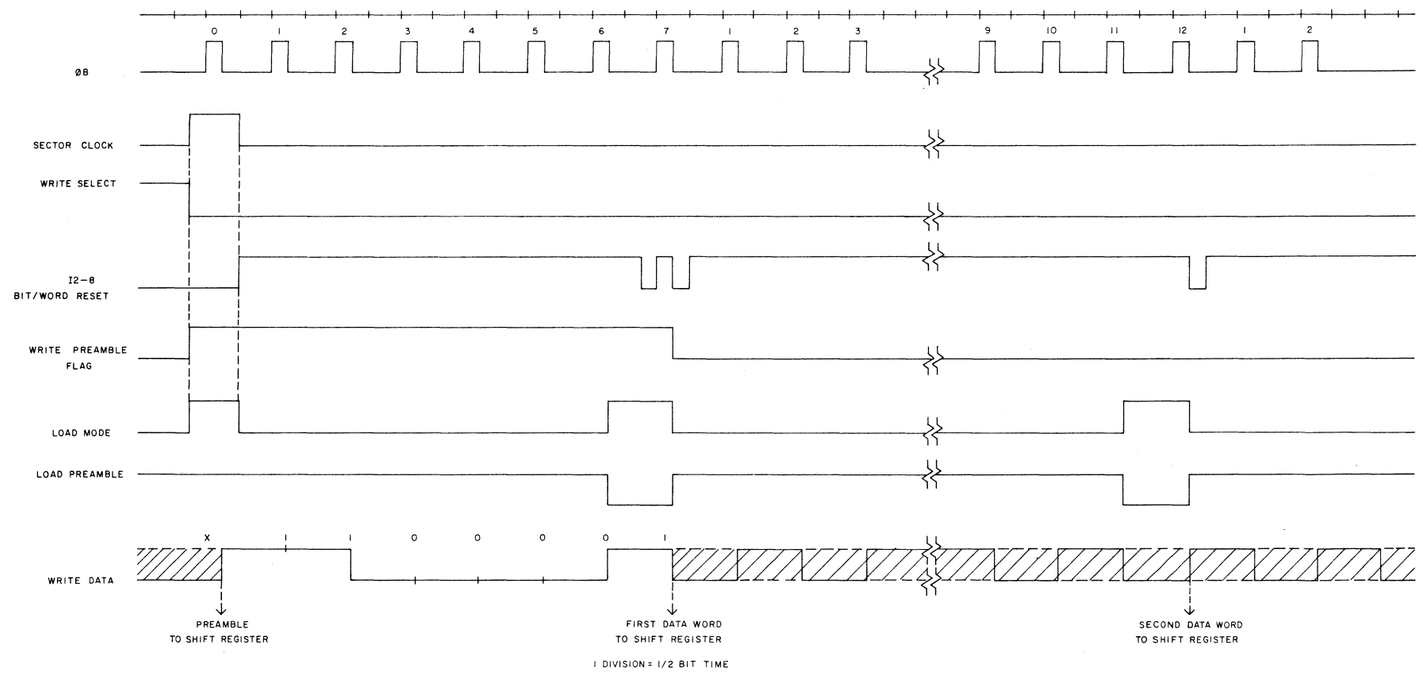
DRUM CONTROLLER

title

sheet of | no. DFIGURES 3-5,3-6,3-7 | rev



rev	description	date	by	apprvd

used on

unless specified
fractions ± 1/64
.00 ± .01
.000 ± .005
angles ± 0°30'

scale | date

material

finish

drawn

design apprvl

checked

final apprvl

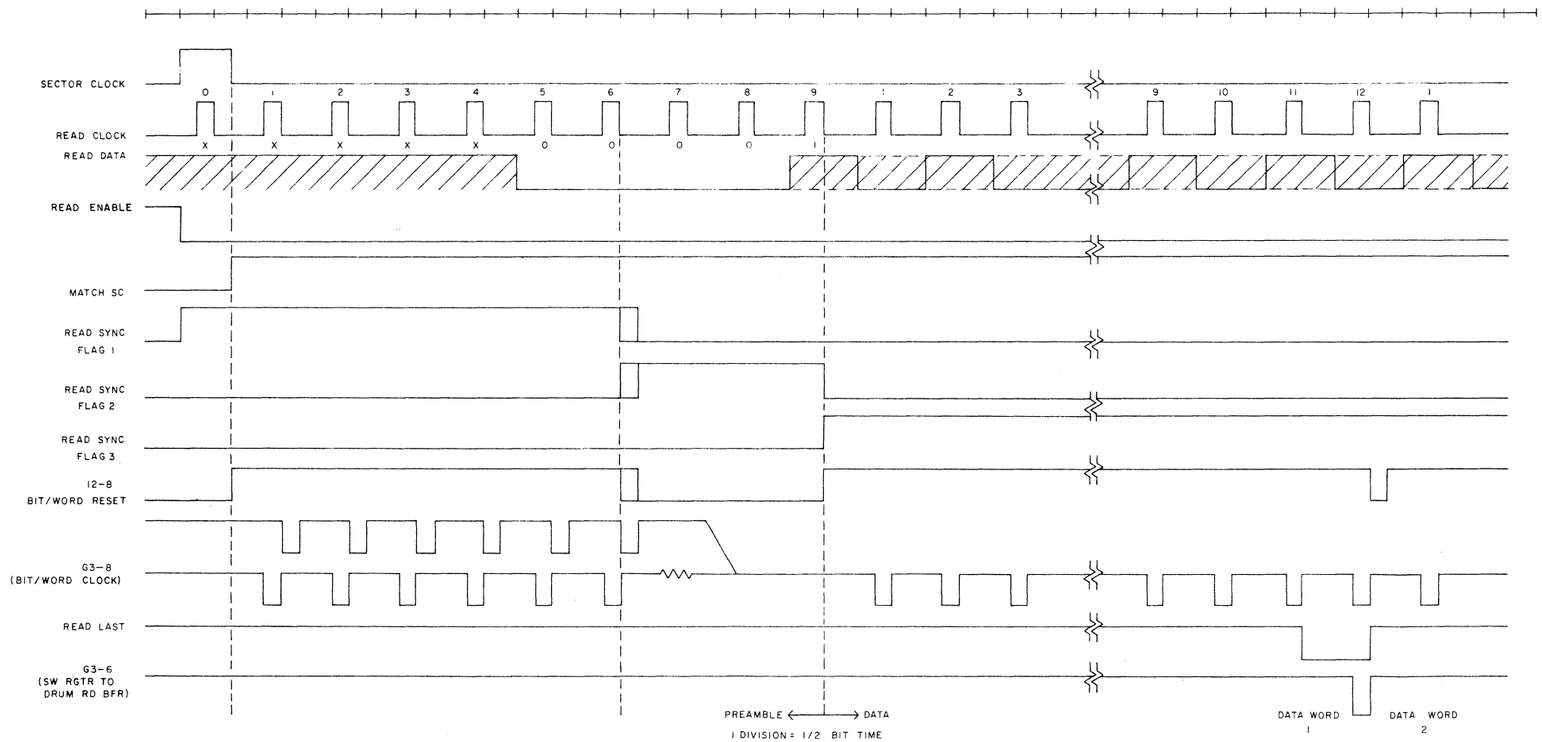
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

DRUM DATA WRITE TIMING

title

sheet of | no. D FIGURE 3-8 | rev

TRANSTEX 18 800-11-70



rev	description	date	by	apprvd

used on

unless specified
fractions ± 1/64
.00 = ± .01
.000 = ± .005
angles = ± 0°30'

scale | 18 FEB 72 date

material

finish

drawn

design apprvl

checked

final apprvl

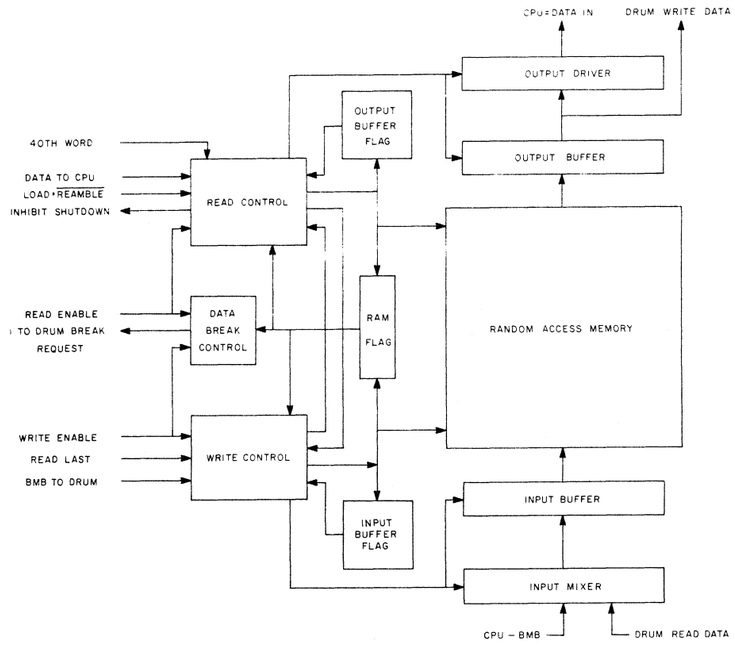
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

DRUM DATA READ TIMING

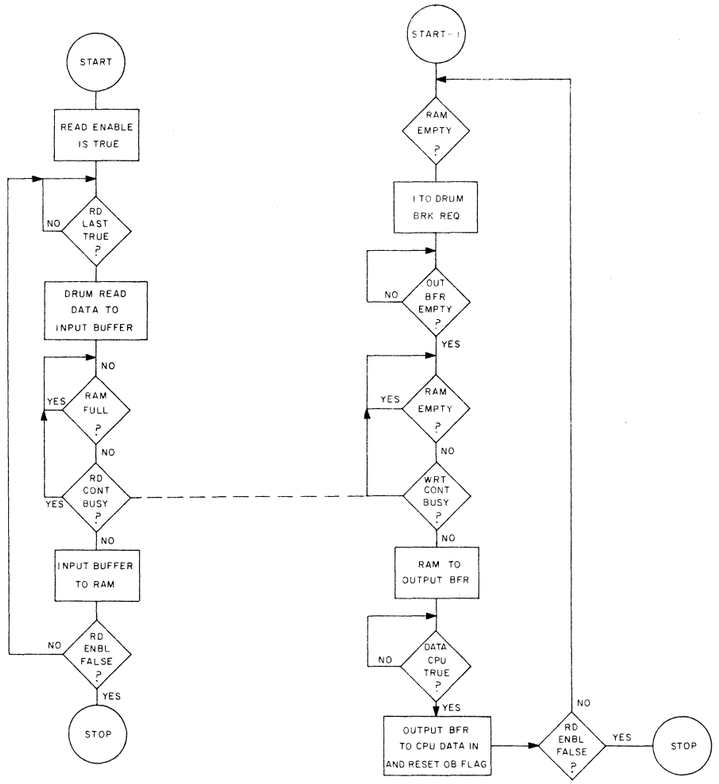
title

sheet of | no. D FIGURE 3-9 | rev.

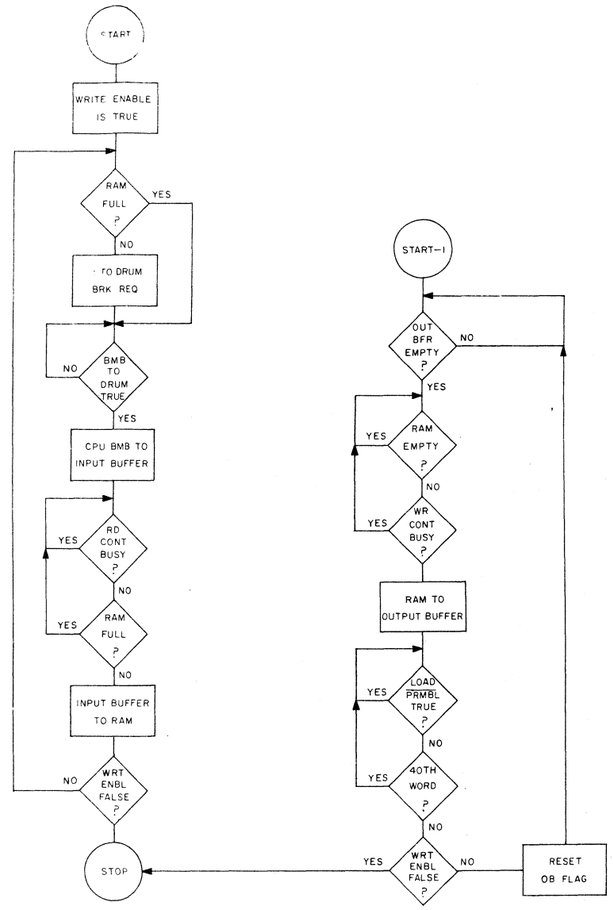
TRANSTEX 15 900-11-70



DERANDOMIZER BLOCK DIAGRAM
FIGURE 3-10



DERANDOMIZER READ FLOW
FIGURE 3-11



DERANDOMIZER WRITE FLOW
FIGURE 3-12

rev	description	date	by	apprvd

used on	scale	drawn
unless specified fractions ± 1/64, .00 = ±.01, .000 = ±.005, angles = ± 0°30'	date	design apprvl
material		checked
finish		final apprvl

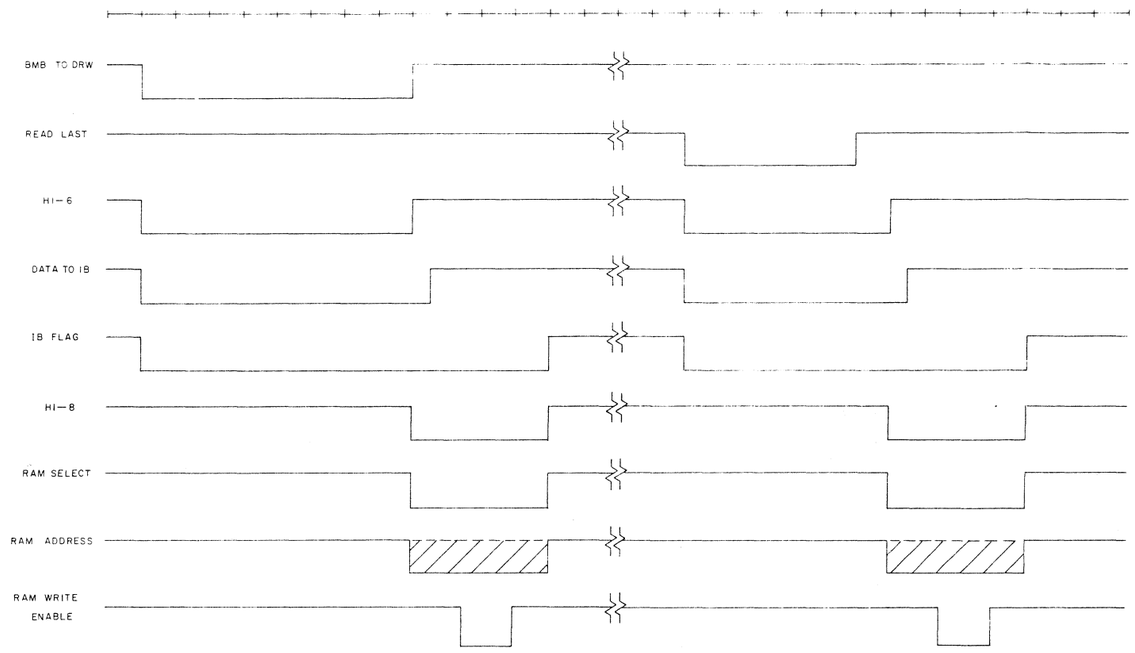
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

DRUM CONTROLLER

title

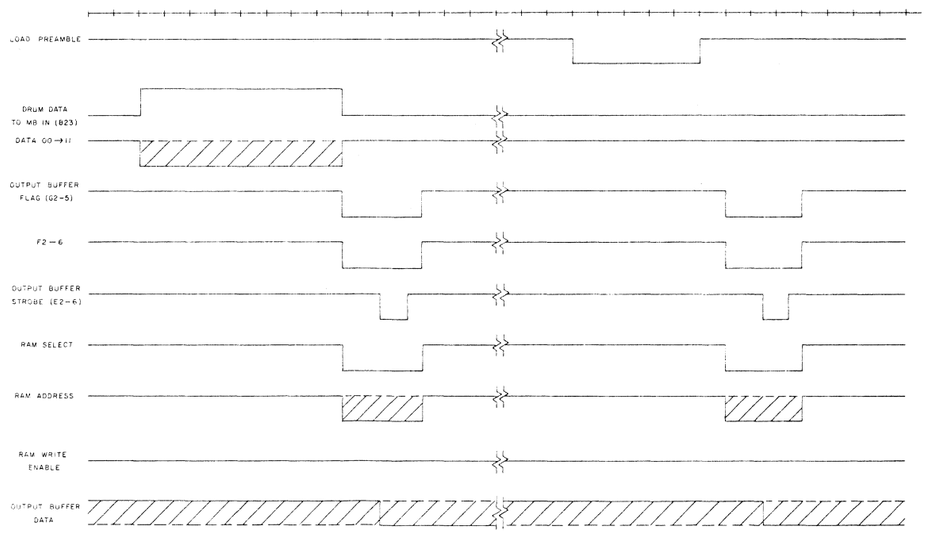
sheet of | no. DFIGURE 3-10,3-11,3-12 | rev

TRANSTEX 15 900-11-70



SCALE 1 DIV = 100NS

DERANDOMIZER WRITE TIMING. FIGURE 3-13



1 DIV = 100NS

DERANDOMIZER READ TIMING FIGURE 3-14

rev	description	date	by	apprvd

used on

unless specified
fractions ± 1/64
.00 ± .01
.000 ± .005
angles ± 0°30'

scale | date

material

finish

drawn

design apprvl

checked

final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title: DRUM CONTROLLER

sheet of | no. DFIGURES 3-13,3-14 | rs

TRANSTEX IS 306-11-70

CHIP CHART

	1	2	3	4	
A		7410		7420	
B	7493	7493	7400	7400	
C	7400	7410	7479	7440	
D	7479	7400	7479	7400	
E	7493	7420	7410	7440	
F	8200	4015	4015	7401	
G	7493	7479	7400	7400	
H	8200	4015	4015	7401	GH
HJ				74121	

40 WORD (10284, B5)

DRUM BK ADD ACC (10298, A32)

TO DRUM BRK REQ (10262, B14)

MATCH • SECTOR CLOCK (10284, B13)

DRUM BRK REQ (10298, A16)

B40 B37 B33 B36 B24

40 WORD COUNTER

LWLB (10284, B10)

B34

DRUM CONTROLLER BUSY

DRUM BRK REQ

(10262, B6) INHIBIT SHUTDOWN

B41

WC OVERFLOW (10442, B37)

B28

DRUM FLAG

IOT 6514 (10298, A12)

B32

DRUM DONE FLAG

RD SEL

WRT SEL

START FLOPS C3

MATCH FLOP

MATCH

SECTOR CLOCK

8 BIT COMPARATOR

SECTOR SELECT

HI

FI

SECTOR COUNTER

ILLEGAL

SECTOR NOT FOUND

DRUM FLAG

STATIC SECTOR

CURRENT SECTOR

TRACK SELECT

SECTOR SELECT

40 μs MONOSTABLE

TRACK COMMAND PULSE

SECTOR COMMAND PULSE

R6 3.3K

R5 4.7K

R8 3.3K

R7 5.6K

C2 2.2 μF

R9 180Ω

CR1 4151

R10

R11

R12

R13

R14

R15

R16

R17 8 RESISTOR, 33Ω

R18 33Ω

W1

R1 2.2K

C1 .01 μF

R3 5.6K

R4 750Ω

2.2K

SECTOR CLOCK (DRUM J1-T)

B29 SECTOR CLOCK (10284, B14)

B20 INTERRUPT (10391-1, B30)

B23 SKIP (10391-1, B28)

B22 IOT 6511 (10298, A6)

B16 AC 02 IN (10295, B13)

B11 AC 00 IN (10295, B11)

B13 IOT 6512 (10298, B10)

B17 AC 01 IN (10295, B12)

INDEX CLOCK (DRUM J1-V)

(DRUM J2-AA) DRUM STATUS SWITCH

E TRACK SELECT (DRUM J1)

B39 BAC 03 (10391-5, B10)

ADDRESS (DRUM J1-K)

B8 BAC 04, B12)

B9 BAC 05, B14)

B7 BAC 06, B16)

B6 BAC 07, B18)

B15 BAC 08, B20)

B18 BAC 09, B22)

B14 BAC 10, B24)

B10 BAC 11, B26)

(ALL 10391-5,

NOTE LINK, W1, IS INSERTED ON 128 AND 256 TRACK SYSTEMS AND REMOVED ON 512 TRACK SYSTEMS

RACK LOCATION B23

DRUM WRITE ENABLE CLEAR (DRUM J2-P)

B14

DRUM WRITE SYNC (10284, B3)

B3

IOT 6501 (10295, B2)

B26

8 RUN (10295, B9)

B25

READ • MATCH (10284, B15)

B31

BAC 00 (10391-5, B4)

B35

0 = RD 1 = WRT

WRITE • MATCH (10284, B11)

B38

WRITE SELECT (10262, B4)

B30

WRITE SELECT (10262, B5)

A5

IOT 6504 (10298, A5)

B21

IOT 6502 (10298, B4)

B19

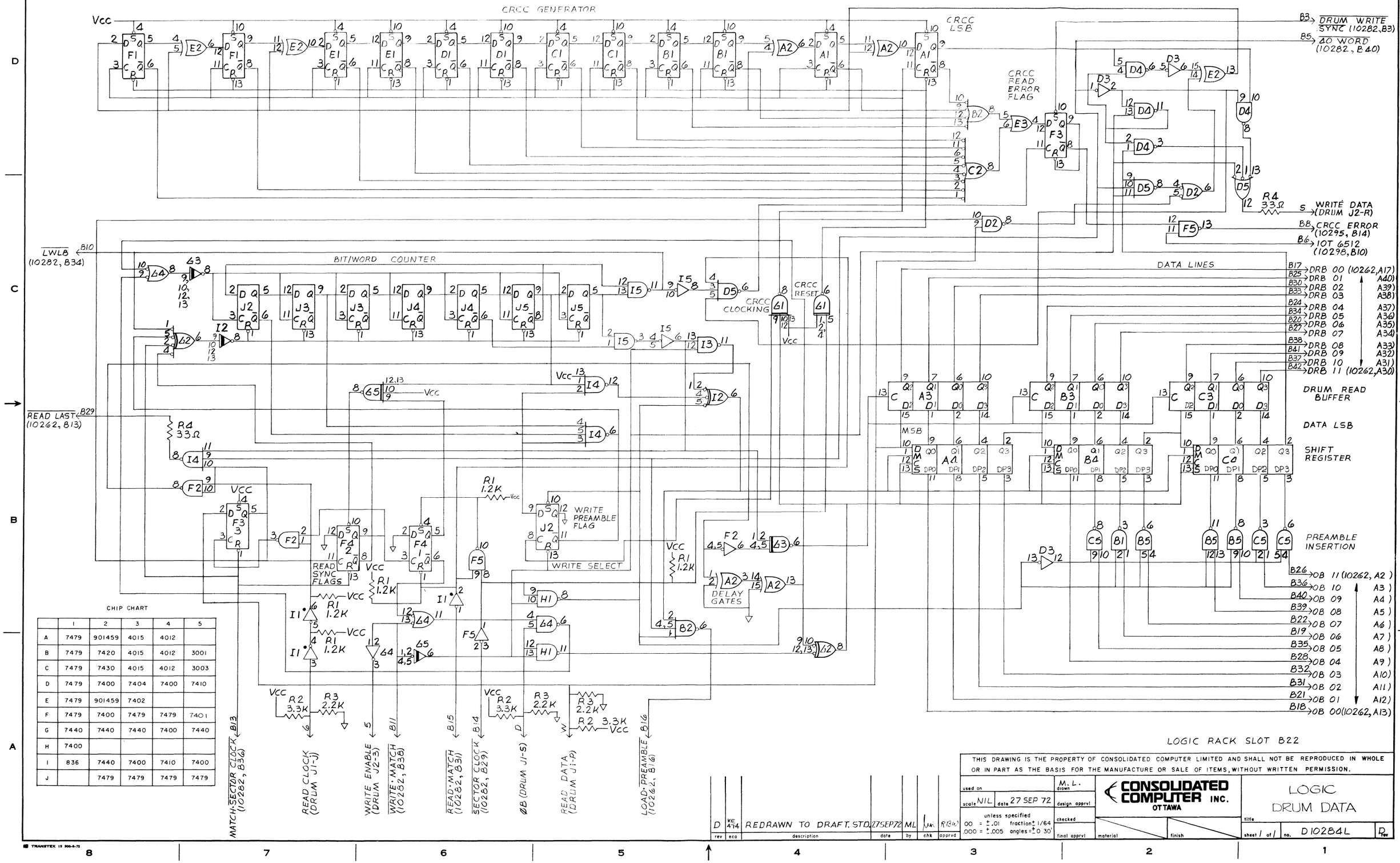
rev	eco	description	date	by	chk	apprvd
P	---	A4 IS ADDED	4 NOV 72	PDG		

used on | drawn | scale | date | design apprvl | unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0 30' | checked | final apprvl | material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

MK V DRUM CONTROL

title | sheet of | no. 10282 L | rev



CHIP CHART

	1	2	3	4	5
A	7479	901459	4015	4012	
B	7479	7420	4015	4012	3001
C	7479	7430	4015	4012	3003
D	7479	7400	7404	7400	7410
E	7479	901459	7402		
F	7479	7400	7479	7479	7401
G	7440	7440	7440	7400	7440
H	7400				
I	836	7440	7400	7410	7400
J		7479	7479	7479	7479

LOGIC RACK SLOT B22

rev	eco	description	date	by	chk	apprvd
D	KE 474	REDRAWN TO DRAFT. STD.	27SEP72	ML		

used on | drawn: M.L. | scale: NIL | date: 27 SEP 72 | design apprvl | checked | final apprvl | material | finish

unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

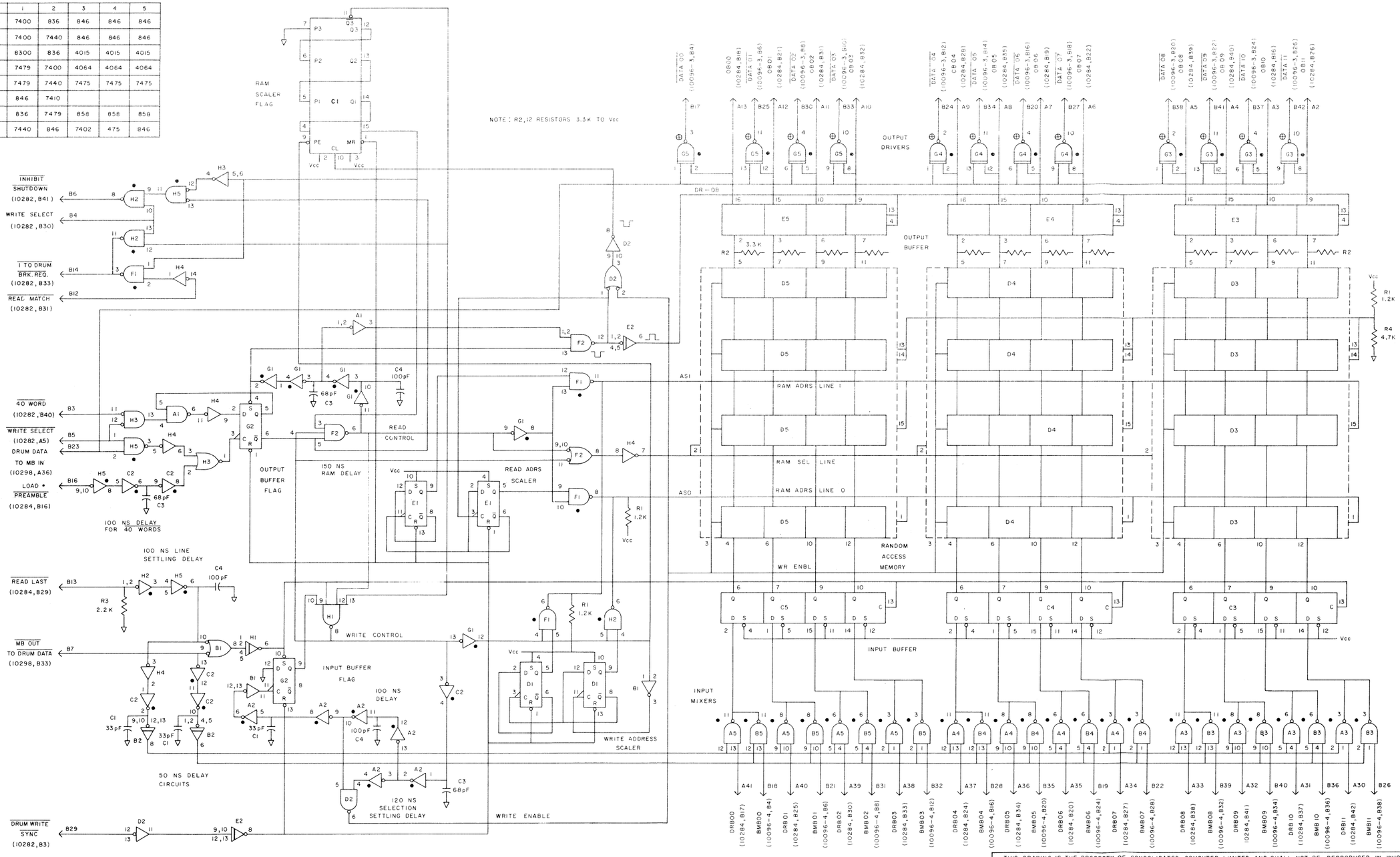
title: LOGIC DRUM DATA

sheet 1 of 1 | no. D10284L | rev D

TRANSTEX 15 800-8-72

CHIP CHART

	1	2	3	4	5
A	7400	836	846	846	846
B	7400	7440	846	846	846
C	8300	836	4015	4015	4015
D	7479	7400	4064	4064	4064
E	7479	7440	7475	7475	7475
F	846	7410			
G	836	7479	858	858	858
H	7440	846	7402	475	846



RACK LOCATION A26

rev	eco	description	date	by	chk	apprvd
A	521	PRODUCTIFIED	5 MAY 72	PDO		

used on | drawn | unless specified: .00 = ±.01 fraction ± 1/64, .000 = ±.005 angles = ±0 30' | design apprvl | checked | final apprvl | scale | date | material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: MK V DERANDOMIZER

sheet of | no. 10262L | rev A

TRANSFER 19 500-8-71

CONTENTS

GENERAL

The Magnetic Tape Transport (MTT) Controller provides the Key-Edit interface between the PDP-8/E processor and the PEC magnetic tape data storage devices. Up to four transports may be used with the controller; they may be either 7-1/2 inch reel (mini-) or 10-1/2 inch reel (maxi-) tape transports.

The MTT primarily provides the final data storage for the system, but it can also be used to read in programs or dumped data.

Refer to the PEC manuals for more detailed information.

BRIEF DESCRIPTION

The controller accomodates either 7- or 9-track magnetic tapes with 200, 556, or 800 bpi density, at speeds of 25 or 12.5 ips in an NRZI format: the 200 bpi density is available only on the maxi-tape units. (A 1600 bpi density is available as an option.) The sequential access time is approximately 50 ms.

The electrical requirements are 117 or 230 vac, 48 to 400 hz; the operating temperature range is 35.5 to 123F (2 to 50C).

The maxi-transport is fitted with a dual gap head. The read and write heads are separated by 0.15 inch, which enables simultaneous read after write operations to be performed for vertical, longitudinal, and cyclic redundancy check purposes. (These checks are also performed on read operations.) An adjacent erase head is automatically activated during write operations.

Illuminating push-switch controls are mounted on the front panel. The three control pcbs are mounted beneath the deck and are accessible by sliding the transport out from the cabinet.

A Tape Adapter must be used when more than one MTT is employed in a system. Where only one MTT is used a cable connects the logic rack interface pcbs (locations B24, B25, B26) and the MTT. Where more than one MTT is used the pcbs are connected to the adapter, which in turn provides outlets for cables to each MTT (refer Figure 6-2-1).

Logic signal levels for the MTT are approximately:

true (low) , 0 to 0.4v
false (high), 3v

CONTROLLER DESCRIPTION

The controller comprises three dedicated pcbs, some ancilary pcbs devoted to drum-to-MTT data transfer controls, and the interconnecting cables.

The basic pcbs are:

1. MTT Control, pcb 10285
2. MTT Data, 7-Track, pcb 10366
   or 9-Track, pcb 10365
3. MTT Readcheck and Status, 7-Track, pcb 10368
   or 9-Track, pcb 10246

These pcbs are located in the Key-Edit logic rack, locations B25, B24, and B26 respectively.

The ancillary pcbs are:

1. Drum and MTT IOT Generator, pcb 10298
2. Word Count and Current Address, pcb 10442

These pcbs are located in the logic rack locations A21 and A29 respectively; their operation is described in this Section.

BRIEF OPERATING THEORY

The controller provides the following functions:

1. MTT motion and timing control
2. MTT to CPU data transfer control
3. MTT read, and read after write, error detection.

Refer Figure 5-1. The CPU initiates commands to the control pcb which then generates status and control information to the readcheck circuitry and the MTT respectively. The status information is returned to the CPU, and the MTT issues a read strobe to the control pcb and data to the CPU via the data pcb. The control pcb generates Read Clocks for the data pcb, and the data pcb provides the parity checks.

Figures 5-2 and 5-3 illustrate the Read and Write Data flow and 5-4 and 5-5 the cycle timing.

LEVEL 3 IOT INSTRUCTIONS

6521 Select Tape Drive.

AC 08 - Transport 1
09 - 2
10 - 3
11 - 4

6531 Skip if Tape Done flag is false.

6532 Clear Tape Done flag and control and stop tape. This instruction clears the following status bits:

AC 01 Lateral parity
AC 02 Longitudinal parity
AC 03 Illegal command
AC 07 Record too long
AC 08 Record too short
AC 09 EOF
AC 10 Tape control busy
AC 11 CRCC error

6534 Set Tape Done flag and cause an interrupt if interrupt facility is on.

6541 Clear Accumulator.

Read magnetic tape status and control status

1. AC 00 Transport Not Ready

Set status - off-line or power off.
Clear - on-line and power on.

2. AC 01 Lateral Parity

Set status - Vertical Parity Error detected.
Clear - 6532

3. AC 02 Longitudinal Parity

Set status - Longitudinal Parity Error detected.
Clear - 6532

4. AC 03 Illegal Command

(Sets Tape Done flag if motion is commanded)
Set Status - Issue Write Command with no write ring present.
- Issue 6542, 6552, or 6551 when Busy status is already up.
- Tape improperly selected.
Clear 6532

5. AC 04 No Write Ring

Set status - Write enable ring not present.
Clear - Write enable ring present.

6. AC 05 EOT Tab Sensed

Set status - Set and held when leading edge of EOT tab is sensed.
Clear - Issue Rewind command or sense leading edge of EOT tab during reverse motion.

7. AC 06 BOT Tab Sensed

Set status - Sense BOT
Clear - BOT tab clear of detector

8. AC 07 Record Longer than Word Count

Set status - Word count expired before IRG is found during read forward.
Clear - 6532

9. AC 08 Record Shorter than Word Count

Set status - IRG encountered before word count has expired during forward read.
Clear - 6532

10. AC 09 EOF Detected

Set status - A one frame record of 17_8 on forward read only.
Clear - 6532 unconditionally

11. AC 10 Tape Control Busy

Set status - 6551
Clear - Stop tape motion, or 6532

12. AC 11 CRCC Error

Set status - CRCC error detected
Clear - 6532

6542 Load Command and Clear Accumulator.

The appropriate bits are loaded into the accumulator and then IOT 6542 is issued.

AC 00 1 Write
0 Read

AC 01 1 Forward motion
0 Reverse motion

AC 02 1 Write long gap

AC 03 1 Write EOF

AC 04 1 Rewind to BOT

AC 05 1 Rewind to BOT and go Off-Line

6551 Load Word Count, Clear Accumulator, and Start motion.

AC 00 to AC 11 contains the two's complement of the word count.

6552 Load Current Address (buffer address) and Clear Accumulator.

AC 00 to AC 11 contains the buffer address.

6554 Load Extended Current Address from AC bits 06, 07, and 08 and Clear Accumulator.

The MTT Control (PEC) pcb provides the timing and start/stop commands for the MTT.

START PROCEDURES

The operation is defined by six of the D flops at the bottom left of the diagram; I4-5, I4-9, I5-5, I5-9, H5-5, H5-9. These command flops are initially set by the accumulator bits BAC 00 to BAC 05, and IOT 6542.

IOT 6551, at connector pin B33 (left side), starts the MTT when the flops are set. Whenever a Write command is issued the Write flop, I5-9, $\overline{Q}$ automatically sets the Forward flop (I4-5) to ensure write routines are done in the forward motion. Similarly Write Long Gap (WLG) or Write End of File (WEOF) commands set either H5-5 or H5-9 to set the Write flop (I5-9) via G5-3 and G5-6, and consequently set the Forward flop.

The five flops - Rewind, Rewind and Off Line, Write, WLG, and WEOF - are reset simultaneously when either IOT 6532 or B Run, at connector pins B18 and B19, are applied to IOR gate F5-3, whose output is inverted by B2-6 to reset the Done flop, F4-5. The inverted output also provides one input to IOR gate F5-6 pin 5, whose output is then inverted to reset the five command flops.

Two adjacent flops, H4-5 and H4-9, control the stop circuitry. H4-5 is set by the first Read Clock, from connector pin 8, and enables the D input to flop H4-9. After the block of data has been read by the data pcb a 1 to Stop signal is received, via connector pin B11, to set the Stop flop and initiate shutdown procedures.

The commands requested by the six command flops are effected when a start motion signal, IOT 6551, is applied to connector pin B33. The Motion and Write Enable flops, F2-5 and H2-5, will set providing an illegal status does not exist.

The Illegal flop, F2-9, will set and an illegal status will exist if any of the following conditions occur:

1. IOT 6551, IOT 6552, or IOT $\overline{6542}$ is issued when the MTT is busy; the flop D input will be high from D1-11 and D1-8.
2. A Write Select command is issued with no write ring present; the flop D input will be high from D1-11, D1-6, D1-3, and G3-8.
3. The MTT had not been selected properly; the flop D input will be high from D1-11, D1-6, D1-3, and connector pin B42 (Set Illegal).

When the Illegal flop D input is high the output of inverter B1-2 will be low. This output is applied (wired OR) with G1-10, G2-11, and G2-3, to the Motion flop, H2-5, to prevent motion.

The Illegal flop is normally set by IOT 6551. When the flop sets F2-9 goes high, appears as an Illegal signal at connector pin B31, and sets the Done flop, F4-9.

EOT DETECTION AND RESET

The EOT flop, H2-9, is set via G2-8 pin 9, and G1-4 from connector pin A; G2-8 pin 10 is only enabled when Forward motion is selected. The EOT flop will set when Forward and EOT signals are present on G2-8 pins 10 and 9. NAND gate G2-6 pin 5 senses the EOT signal, pin 4 senses the Reverse motion condition and the gate resets the EOT via H1-13. When the leading edge (first edge encountered on Forward motion) of the EOT tab has been sensed G2-6 will go low, and a pulse will be generated at H1-13 to clock the flop; the D input is ground, therefore the flop will reset.

The Rewind pulse at connector pin S is applied directly to reset the flop at H2-9 pin 13. Thus, the EOT flop can only be reset by a backspace over the EOT tab, or by a Rewind command.

WRITE SEQUENCE

The Write flop is set by IOT 6542 and the appropriate AC bit. The Motion flop is set by IOT 6551 if no illegal conditions exist; the flop Q output and Ready input from connector pin C, inverted by G1-8, enable NAND gate F1-11. The gate pulls down the $\overline{\text{Tape Run}}$ line at connector pin B35 to transfer the Motion command to the data pcb. The Motion Flop $\overline{Q}$ output is routed via IOR gate G4-6 to indicate a Busy condition to the Readcheck and Status pcb via connector pin B14.

When the Forward flop sets the Forward command from the Q output is issued to the MTT via NAND gate C1-11 and connector pin T.

The Write Enable flop, H2-5, also sets and activates the MTT tape write drivers via NAND gate F1-10 pin 9 and connector pin J, Write Permit.

The $\overline{\text{Tape Run}}$ signal at F1-11 is inverted by B1-4 and applied as a high level to NAND gates C1-11 pin 13 and C1-3 pin 1, which provide the FWD and RVS signals at connector pins R and T. B1-4 also releases the Read flop, C3-5 (top), enables it (at C3-2), and enables NAND gate G4-11 pin 13. C3-5 pin 6 is high, therefore G4-11 goes low to IOR gate G4-8 pin 10. G4-8 output will go high to remove the reset condition from the adjacent Motion Oscillator B3 flops; the output is also inverted by A5-12 to remove the reset from Scalers C4, B4, D4, and E4.

The Motion Oscillator 511.57 khz output is divided by the B3 flops and the Scalers. When Scaler D4-11 goes high, after approximately 16 ms, NAND gate D5-12 pin 13 will go high. WEOF and WLG conditions are non-existent on D5-12 pin 1 and the BOT signal at connector pin B41 has not set the Read Inhibit R-S flop, D3-8 and D3-11, whose output is applied to D5-12 pin 2. Thus the gate is enabled and its output will go low. D5-8 will then go high and set the Read flop, causing C3-5 pin 6 to go low. NAND gate G4-11 will be disabled and consequently inhibit both the Motion Oscillator and the Scaler. Inverter A5-2 output will also go high from the Read flop set and release the Data Oscillator flop, C3-9, which permits the division of the oscillator output. The flop output activates the data pcb via connector pin B40.

Simultaneously the Gated Read Clock pulse is applied through connector pin F (top left) and inverter H1-4 to clock the D flop H3-5. The flop will only set if the D input is high as a result of a read data parity error signal from the Read Check pcb via connector pin B24. Two concurrent clocks and a parity error are necessary before a parity error is issued to the flop (because the last character from the LRCC could contain a parity error).

The data pcb presents $\overline{\text{1 to Break}}$ pulses at connector pin B35 (lower right). The trailing edge of the ground true pulses (going high) set the MTT Break flop C2-9; $\overline{Q}$ issues an MTT $\overline{\text{Break Request}}$ signal, via connector pin B36, to the multiplexor to request more data from the CPU.

During a Write sequence the data must be held ready for transfer in the data pcb. The MTT Break flop is set via NAND gate D2-8, providing:

the MTT Write Select is a 1 at D2-8 pin 10,

IOT 6551 is present on D2-8 pin 9,

the WLG or WEOF command does not exist on D2-8 pin 11.

The break requests are inhibited because they are only required during Read or Write Forward sequences. The 8-input IOR gate E2-8 provides the inhibiting function for all other conditions (WLG, WEOF, Reverse, Stop, Break Requests, MTT Address Accepted).

The Data Permit flop, C2-5, issues a $\overline{\text{Write Data}}$ signal to inform the data pcb, via connector pin B33, when to transmit data. R-S flop F3-6, F3-8 sets when the word count overflow occurs; F3-8 will go low via E2-8 to the Data Permit flop, C2-5 pin 2. Thus the next $\overline{\text{1 to Break}}$ pulse resets the Data Permit flop.

SHUTDOWN PROCEDURE

When the data pcb detects or writes blanks it issues a 1 to Stop pulse to the control pcb via connector pin B11 (bottom centre) to set the Stop flop, H4-9. The Read Sync flop, H4-5, is true, therefore the Stop flop will set and commence shutdown procedures.

The Stop flop $\overline{Q}$ output will go low to IOR gates G4-8 pin 9 and G4-6 pin 5. G4-6 applies a Busy condition to the Readcheck and Status pcb via connector pin B14. G4-8 enables the Motion Oscillator flops, which permit scaling until D4 pins 12 and 11 go high to enable NAND G4-3, after 18 ms with 7-track application. G4-3 will go low to IOR gate E5-11 pin 13; pin 11 will go high to E5-6 pin 4; pin 5 is enabled by the Stop flop set. Therefore pin 6 goes low to IOR gate F3-3 pin 2. The gate output is inverted and applied as a low level to reset the Motion flop and stop the MTT.

The Motion Osc continues functioning until approximately 64 ms have elapsed and scaler E4-9 enables NAND gate E5-3 pin 1; pin 2 is set when the Stop flop is true. E5-3 causes F5-11 pin 12 to go low. The gate output is inverted by E3-10 and sets the Done flop, which applies an interrupt via E3-12 and connector pin B28 to the CPU to indicate completion of the data transfer. The low output from E5-3 is also applied to IOR gate F5-6 pin 4 to initiate the complete control reset where all conditions return to zero, including the Stop flop.

During a Read sequence the 8-input NAND gate B5-8 (adjacent to the Scalers) pre-empts C5-6 (activated in 4.85 ms) to determine when the tape motion stops. Normal shutdown procedures continue as described.

The Magnetic Tape Data, 7-Track, pcb controls data transfers between the CPU and a 7-track Magnetic Tape Transport. The bottom and extreme right of the logic diagram shows data control circuitry; the remainder of the diagram shows data handling circuitry.

The logic consists of the following main blocks:

1.	Data Register	B2, D2, E4, F4
2.	Data Output Drivers	B4, B5, D4, D5, E5, F5
3.	Data Receivers	E2
4.	Parity Generator and Check	C4, E1
5.	Timing Circuits and Control Circuits	I2, H2
6.	End of File Detection	C2, G4, H4, E3

WRITE DATA SEQUENCE

When the MTT control pcb, 10285, starts motion of the tape transport, it issues a $\overline{\text{Tape Run}}$ signal to the data pcb, connector pin B5. This signal is inverted and enables gate I5-6; it is also applied to I5-3 pin 2. The output of I5-3 resets scaler I2 and is inverted and applied to I3-11 pin 12. I3-1 output resets scaler H2. $\overline{\text{Tape Run}}$ inverted is also used to reset flip-flops H4-5 and F2-9.

Immediately after motion has started the control pcb issues an $\overline{\text{MTT Break Request}}$ to fetch the first character to be written on tape from the CPU. The CPU responds by sending an $\overline{\text{MTT Address Accepted}}$ signal to the data pcb at connector pin B9, and to the control pcb to reset the BRK REQ flip-flop. The $\overline{\text{MTT Address Accepted}}$ signal is inverted by H3-3 and is gated with Write Select, from connector pin B12, by G3-8 to reset the Data Register – B2, D2, F4, E4. The CPU then applies an $\overline{\text{MB Out to MTT Buffer}}$ signal to connector pin B23. The signal is inverted by G2-3 to enable NAND gates F3, D3, and B3. This allows the data from the CPU, available on BMB 00 to BMB 11 lines at connector pin group B18 to B26, to pass through these gates and direct set the Data Register. As soon as the register has been loaded its outputs apply the data to the Data Output Driver NAND gates, where it waits to be strobed out to the MTT.

When writing on 7-track tape, a 12-bit word must be divided into two 6-bit bytes. This means that for every 12-bit word of data, there are actually two 6-bit words written on tape. This leaves one track on the tape for the parity bit.

When tape motion is started flop H4-5 is reset by $\overline{\text{Tape Run}}$ via I3-8. The flop $\overline{\text{Q}}$ output enables gates H5-3 and I4-12. I4-12 is also enabled by a Write Select and $\overline{\text{WLG+WEOF}}$. Therefore the output of I4-12 is true (low). This is inverted by I3-3 to enable output drivers F5-4, E5-4, D5-4 and 10, and D4-4 and 10.

When the tape reaches speed the control pcb sends (Data) Clock pulses to the data pcb, connector pin B3. These pulses are applied to I5-6 pin 5. I5 was previously enabled by $\overline{\text{Tape Run}}$. The gate output, I5-6, drives the clock input of scaler I2, which divides the clock pulses by a factor of 16. The scaler output is shaped to a pulse by an RC network and gated with Write Select at H3-11. The output of H3-11 is inverted and applied to G3-6 pins 4 and 5. G3-6 has been enabled by the $\overline{\text{Write Data}}$ signal from the control pcb via connector pin B8 and gate G2-8. The output of G3-6 is the Write Clock, which, via I5-11, H5-6, H4-6, and I4-12, strobes the six most significant bits of data out to the MTT via the enabled output drivers. The Write Clock also resets scaler H2 via I3-11, and clocks flop H4-5 via I5-11 and H5-6. Flop H4-5 then toggles, thus disabling gates H5-3 and I4-12, and enabling gates H5-11 and I4-8. This disables the six most significant output drivers and enables the six least significant, i.e., gates F5-10, E5-10, B5-4 and 10, and B4-4 and 10. Scaler I2 continues to scale until a second Write Clock is produced as described previously. This Write Clock strobes the second byte of data out to the MTT, and is also applied to H5-8 pin 10 via I5-11. The output of H5-8 is the $\overline{\text{1 to BRK}}$ pulse which is applied to the control pcb to initiate a second Break Request. The second Write Clock is also used to toggle flop H4-5 again to disable the six least significant drivers and re-enable the six most significant drivers.

NOTE: The propagation delay through H5-6 and H4-5 is slow enough that H4-5 will not change states until a $\overline{\text{1 to BRK}}$ pulse has been produced by H5-8.

Each successive word of data is written as described above until the complete record has been written. The controller then writes LRCC on the tape then stops the tape motion.

WRITE LRCC

After the last byte has been written on tape the control pcb cancels the $\overline{\text{Write Data}}$ signal at connector pin B to disable gate G3-6 via G2-8, thus eliminating any further Write Clocks. Because there are no Write Clocks to reset scaler H2 it is allowed to continue scaling: H2-8 and I2-11 will then go hgih simultaneously. Consequently the output of H3-6 will go low, sending a Write Reset signal to the MTT via connector pin F. Write Reset automatically writes LRCC on the tape.

STOP SEQUENCE

H2 continues to scale until its last stage, H2-11, goes high. This is the 1 to Stop signal, and it is sent to the control pcb via connector pin B7 to stop the tape motion.

WRITE LONG GAP

The control pcb issues a $\overline{\text{WLG+WEOF}}$ signal to the data pcb via connector pin B6 to write a long gap on tape. This disables I4-8 and I4-12, thus disabling the data output drivers so that nothing can be written on the tape. The control pcb starts tape motion but does not issue any (Data) Clocks until the long gap has been written. After it has been written, clock pulses are sent to the data pcb and I2 and H2 begin to scale. During a Write Long Gap, $\overline{\text{Write Data}}$ is false (high) and WEOF is false (low) to disable G2-8 via G2-11. The output of G2-8 disables G3-6 to prevent the production of Write Clocks.

When the scalers have scaled to the end, so that H2-11 goes high, a 1 to Stop is issued to stop the tape motion.

PARITY GENERATION AND CHECKING

Parity is generated by the parity tree C4-8 (top left). It senses the Write Data lines and produces the correct parity bit for each byte of data applied to its inputs. C4-8 pin 12 can generate either even (high) or odd (low) parity.

Parity is checked by the parity tree D1-8. It operates in the same manner as the generator, but it senses the data from the MTT Read Data Lines. If it detects a parity error the signal, Parity Error, is applied to the control pcb via connector pin B24 for processing.

By definition the EOF code (17) must always be even parity. Therefore, the choice of odd parity is controlled by the signal $\overline{\text{WLG+WEOF}}$. For a normal data write sequence $\overline{\text{WLG+WEOF}}$ is high at connector pin B6, forcing I5-8 low, and C4-8 pin 12 and D1 pin 12 low. This sets the pcb to generate and check for odd parity. When writing an end of file, $\overline{\text{WLG+WEOF}}$ is low, causing C4-8 pin 12 and D1 pin 12 to generate and check for even parity. (This forcing of even parity prevents the detection of false parity errors when the EOF is read after a write operation. The PEC MTT is a Read after Write model.) When an EOF is detected during a read operation it is accompanied by a parity error if the data pcb is set to operate in odd parity.

WRITE END OF FILE

The control pcb issues two signals to the data pcb - WEOF and $\overline{\text{WLG+WEOF}}$ - to write a File Mark on tape. $\overline{\text{WLG+WEOF}}$ at connector pin B6 disables the data output drivers in the same manner as it does when writing a Long Gap. It also conditions the output data lines with the EOF code 17 via I5-8 and the C3 inverters (top left).

The WEOF signal at connector pin B15 releases the reset of flop F2-5, places a high level on the D input and enables gate G2-11 at pin 13. The control pcb sends clock pulses to the data pcb and I2 and H2 begin to scale. When the first Write Clock is produced at G3-6 it strobes the EOF level via I5-11, H5-6, H4-5, H5-11 and H4-9, out to the MTT at connector pin B14. The clock trailing edge clocks and sets flop F2-5. The $\overline{Q}$ output of F2-5 goes low, causing the output of G2-11 to go false (high) to disable G3-6 via G2-8 and prevent any further Write Clocks being issued.

I2 and H2 continue to scale to produce a Write Reset at connector pin F to put LRCC on tape and to produce a 1 to Stop to initiate a normal stop sequence.

READ DATA SEQUENCE

The control pcb starts tape motion and applies $\overline{\text{Tape Run}}$ to the data pcb at connector pin B5. When the start sequence has finished, the control pcb begins sending (Data) Clock pulses to the data pcb via connector pin B3. The MTT reads the first character on tape and applies it to the data pcb via a cable to the Read Data inputs at pin group N to A. The parity checker senses the data and checks for a parity error. The data is received by the E2 inverters and applied to the D inputs of the Data Register. The MTT also sends a Read Clock signal to the control pcb, which then applies a $\overline{\text{Read Clock}}$ level to the data pcb at connector pin B4.

$\overline{\text{RD RCL}}$ resets the scalers I2 and H2 via I5-3 and is applied to gates H5-3 and H5-11 via inverter G2-6. H5-3 is enabled at pin 2 by flop H4-5 $\overline{Q}$. Therefore the data is clocked into the most significant byte of the data register by the $\overline{\text{RD RCL}}$ via H5-3 and inverter G5-6. $\overline{\text{RD RCL}}$ also clocks flop H4-5 via I5-11 and H5-6. This causes H4-5 to set and enable gates H5-11 and H5-8. When the second character on tape is applied to the inputs of the Data Register, the $\overline{\text{RD RCL}}$ clocks the data into the least significant byte of the register and toggles H4-5 back to the reset condition to receive the next character from tape. Two 6-bit bytes from the tape have then been assembled into one 12-bit word in the Data Register and applied to the Output Drivers. The second $\overline{\text{RD RCL}}$ also clocks H5-8 to produce a 1 to BRK signal which is applied to the control pcb to initiate an $\overline{\text{MTT BRK REQ}}$ to the multiplexor. The multiplexor responds by sending a Data In pulse to the data pcb via connector pin B16, which then strobes the data out to the CPU via the Output Drivers.

RD RCL pulses to the data pcb terminate when the entire record has been read. I2 and H2 are allowed to scale through to the end to produce a 1 to Stop signal, at connector pin B7, which then initiates a normal stop sequence.

READ LONG GAP

When the controller begins a normal read sequence and no Read Clocks are applied to the control pcb, $\overline{\text{RD RCL}}$ pulses to the data pcb are inhibited. The absence of $\overline{\text{RD RCLs}}$ allows I2 and H2 to scale to the end and initiate a normal stop sequence.

READ EOF

The EOF code is recognized by gates C2-8 and E3-6. The inputs of C2-8 and E3-6 will all be true when the code 1717 has been assembled in the Data Register, causing their outputs to be true. These are inverted by G4-3 and E3-8 and applied to G4-6, causing its output to be treu to the D-input of flop H4-9.

When the $\overline{\text{RD RCL}}$ pulse clocks the least significant byte into the Data Register, via H5-11 and G5-8, H5-11 also clocks flops H4-9 and F2-9. This causes F2-9 to set and if the EOF code is present H4-9 will reset. The $\overline{Q}$ output of H4-9 goes high to send the EOF signal to the readcheck pcb.

The Q output of F2-9 enables gate G4-8. If another $\overline{\text{RD RCL}}$ arrives indicating that the EOF just detected was not a true EOF, then the output of G4-8 will go low (true) and set flop H4-9 to remove the EOF signal from the readcheck pcb.

The Magnetic Tape Data, 9-Track, pcb controls data transfers between the CPU and 9-track Magnetic Tape Transport. The lower portion of the logic diagram shows data control circuitry and the upper portion shows data handling circuitry.

The logic consists of the following main blocks:

1.	Data register	E2, E3
2.	CRCC register	C2-9, C3, C4
3.	CRCC Drivers	A3, B2-13, B3
4.	Data Drivers and Receivers	C1-6, C1-7, F2, A5, B5, A4, B2-1, B4
5.	Timing Circuits	I4, I5
6.	Parity Generator and Check	F4, F3
7.	End of File Detection	H3, H4

WRITE DATA SEQUENCE

When the MTT control pcb starts motion of the MTT it issues a $\overline{\text{Tape Run}}$ signal to the data pcb, connector pin B5. The signal is inverted and applied to gate I3-3 pin 2, it also enables gate I3-11 at pin 13. The output of I3-3 resets Timing Scaler I4 and is also inverted and applied to I3-6 pin 4, whose output resets scaler I5.

Immediately after motion has started, the control pcb issues an MTT Break Request to fetch from the CPU the first character to be written on tape. The CPU responds with an MTT Address Accepted signal which is applied to the control pcb to reset the Break Request flip-flop, and to connector pin B9 of the data pcb where it is applied to IOR gate H2-3 pin 1. The output of H2-3 is gated with Write Select, from connector pin B12, at F1-6 to reset the Data Register flip-flops. The CPU then applies an MB Out to MTT Data signal, to connector pin B23, which is inverted and gated with Write Select at H1-8. The output of H1-8 is inverted and used to enable NAND gates E4 and C5 to allow the data available on BMB 4 to BMB 11, connector group B28 to B26, to direct set the Data Register.

When the Data Register is loaded its outputs apply the data to the CRCC Generator Circuit, the Parity Generator circuit F4, and the Output Driver NAND gates A4 and B4. The parity bit generated by F4-8 is applied to the Parity Driver, B2-1 pin 3. The Output Drivers and the Parity Driver — A4, B4, B2-1 — are enabled by the $\overline{\text{Write Data}}$ signal from connector pin B8. The signal is routed via IOR gate H2-11 and applied to NAND gate H2-8 with the inverted WEOF signal from connector pin B15. Thus the driver gates have the complete data word available at their outputs.

When the tape reaches speed the control pcb sends (Data) Clock pulses to the data pcb connector pin B3. These pulses are applied to I3-11 pin 12, which was enabled by $\overline{\text{Tape Run}}$. The output of I3-11 drives the clock input of scaler I4. The scaler divides the clock pulses by a factor of 16 and this output is used to trigger the Monostable, I1. The 3 µs pulse output is gated with the Write Select, from connector pin B12, by H2-11 whose output is inverted and gated by I3-8 with the Write Data signal from H2-11. The output of I3-8 is applied to G5-6 pin 5, I3-6 pin 5, and H1-6 pin 5 to produce the 1 the Break signal at connector pin B11.

The output of G5-6 is gated by G5-8 with the $\overline{Q}$ output of flip-flop G2; G2 is held in the reset state except during a WLG or WEOF condition. Thus G5-8 is enabled and produces a $\overline{\text{Write Clock}}$ signal at connector pin J. The signal strobes the data available at the outputs of the driver gates — A4, B4, and B2-1 — into the MTT data electronics via the cable connected at pin group X to D (top left).

The output of I3-6 is used to reset scaler I5 every time the monostable, I1, initiates a $\overline{\text{Write Clock}}$ during a normal write data sequence.

The next word of data is requested by the trailing edge of the $\overline{\text{1 to BRK}}$ signal, at connector pin B11, which sets the BRK REQ flip-flop on the control pcb. The $\overline{\text{1 to BRK}}$ signal is produced at the same time as the $\overline{\text{Write Clock}}$ signal. The circuit then operates as previously described for each successive break request until the complete record has been written. The controller then writes LRCC and CRCC on the tape, then stops the tape motion.

WRITE CRCC

When the last Address Accepted pulse comes from the computer an $\overline{\text{MTT WC Overflow}}$ pulse is issued by the WC and CA pcb, 10442, to the MTT control pcb to inhibit any further Break Requests from the MTT. When the data pcb issues the 1 to BRK pulse, which corresponds to the last $\overline{\text{Write Clock}}$, the control pcb cancels the $\overline{\text{Write Data}}$ signal so that connector pin B8 goes high. This inhibits I3-8 via H2-11 and prevents the 3 µs pulse produced by I1 from enabling gate I3-8; thus any further 1 to BRK signals and the reset of scaler I5 are inhibited; I5 continues to scale.

Because $\overline{\text{Write Data}}$ is high, G3-6 pin 6 will be high to enable gates G4-6 and H2-6; F5-1 pin 2 will also be high and prevent clocking of the CRCC Register.

When scaler I4-11 goes low, I5-12 will go high and enable G4-6. When I4-11 next goes high, the monostable will produce a 3 µs pulse to be gated with Write Select by H1-11, inverted by G3-2 and applied to G4-6 pin 3. The output of G4-6 is then applied to H2-3 pin 2 whose output is gated by F1-6 with Write Select from connector pin B12 to reset the Data Register.

When scaler I5-8 goes high, four character times after the last data word was written, H2-6 output will go low and H5-12 pin 2 will be enabled. The low signal at the output of H2-6 is inverted by B1-9 and enables the CRCC Driver gates A3, B3, and B2-13. The CRC character available at the CRCC Register flop outputs is then applied, via the inverters B1 and C1 and the output drivers, to the write data lines to the MTT.

While I5-8 is still high I4-11 will go high, causing the monostable to produce a pulse which is applied to H5-12 pin 13 via H1-11 and G3-2. H5-12 pin 12 will go low, causing G5-6 to go high. This high is applied to G5-8 pin 9, which is enabled by G2-5 pin 6, and a $\overline{\text{Write Clock}}$ is produced at connector pin J to write the CRC character on tape.

When the 3 µs pulse terminates H5-12 pin 12 will return to the high state and clock the flip-flop G2-5. G2-5 pin 6 will go low and disable gate G5-8, thus inhibiting any further $\overline{\text{Write Clocks}}$.

WRITE LRCC

Scaler I5-11 will go high four character times after I5-8 goes high, or four character times after CRCC was written on tape. When I5-11 goes high, G5-3 pin 3 will go low to send a Write Reset signal to the MTT via connector pin F. The signal resets the Write amplifiers and the MTT automatically writes the correct LRC character on tape.

STOP SEQUENCE

When I5-11 goes low again the output of adder D4 will go high and clock flip-flop I2-9 to set the flip-flop, which then sends a 1 to Stop signal to the control pcb via connector pin B7 in initiate the stop sequence.

Flip-flop G2-5 will be reset to allow $\overline{\text{Write Clock}}$ pulses when the control pcb removes the Write Select signal.

WRITE LONG GAP

To write a long gap on tape the control pcb issues a $\overline{\text{WLG+WEOF}}$ signal to the data pcb via connector pin B6. This low signal is applied to G5-11 pin 12 and H5-12 pin 1. G5-11 will be high, forcing E5-8 pin 8 low to hold the CRCC Register reset for the time the long gap is being written. G5-11 pin 11 will also force E5-6 pin 6 low to hold the EOF detection flip-flops (H3 and H4) reset while writing a long gap. $\overline{\text{WLG+WEOF}}$ also holds the output of H5-12 high. This prevents a $\overline{\text{Write Clock}}$ from being produced through G5-6 and G5-8 when I5-8 goes high.

The control pcb inhibits clocks to the data pcb until the long gap has been written. When the clocks begin scalers I4 and I5 start to scale and tape motion is stopped by the normal Stop Sequence.

WRITE EOF

The control pcb sends a $\overline{\text{WLG+WEOF}}$ signal to the data pcb to write an EOF on tape. The $\overline{\text{WLG+WEOF}}$ signal conditions the data pcb in the same manner as it does when writing a long gap.

The WEOF signal at connector pin B15 releases the reset and conditions the D-input of flip-flop I2-5, and also enables NAND gate H1-3. Because flip-flop K2-5 is reset, pin 6 is high and H1-3 output will go low to H2-11 pin 12. The output of H2-11 enables I3-8 pin 9, and is also inverted by G3-6 and applied as a low to H2-6 pin 4 to disable the CRCC Driver gates – A3, B3, and B2-13.

WEOF is also inverted by C1-1. This low level is applied to H2-8 pin 9 to disable the Output Drivers – A4, B4, and B2-1. It is also applied to inverter E1-8 whose output is applied to inverters A2-1, A2-4, and A2-13 The outputs of these gates go low to place the EOF code 23 on the output data lines.

The control pcb inhibits clocks until a long gap has been written then issues them to the data pcb and I4 begins to scale. When I4-11 goes high the monostable I1 produces a pulse which is applied to H1-11, inverted, and applied to I3-8. The output of I3-8 clocks flip-flop I2-5 on the trailing edge. I2-5 pin 6 then goes low, forcing the output of H1-3 high. This causes H2-11 to go low and disable I3-8 to inhibit any further pulses from the monostable. The single pulse allowed to pass I3-8 enables G5-6 to produce a single $\overline{\text{Write Clock}}$ at G5-8 pin 8 and connector pin J.

This $\overline{\text{Write Clock}}$ strobes the first word of the EOF code to the MTT to be written on tape. I5 is then allowed to scale: when I5-11 goes high it enables G5-3. When I4-11 goes high it triggers the monostable which applies a pulse to G5-3 via H1-3 and G3-2. The output of G5-3 goes low and applies a $\overline{\text{Write Reset}}$ signal to the MTT via connector pin F. This $\overline{\text{Write Reset}}$ writes the second word of the EOF code on the tape.

When I5 finishes scaling and I5-11 goes low it sets flip-flop I2-9 and a normal stop sequence is initiated.

READ DATA SEQUENCE

The control pcb starts tape motion and sends the $\overline{\text{Tape Run}}$ signal to the data pcb as for the Write Data Sequence. When the start sequence is complete the control pcb sends clock pulses to the data pcb. The MTT reads the first character and sends the data to the data pcb via cable connector pin group S to K where it is received by inverters F2, C1-6, and C1-7. The inverted data is applied to the D inputs of the Data Register flip-flops and the inputs of the Parity Checker F3. The output of F3 is applied to flip-flop G2-9 pin 12. Simultaneously the MTT reads the character and sends a $\overline{\text{Read Clock}}$ signal to the control pcb and to the data pcb via cable connector pin H. The control pcb produces a $\overline{\text{Gated Read Clock}}$ which it sends to connector pin B4 of the data pcb. This signal is applied to H1-6 pin 4 to produce a $\overline{\text{1 to BRK}}$ pulse at connector pin B11: it also applied to inverter G1-13 pin 12. The output of G1-13 is applied to inverter E1-6 whose output clocks the data into the Data Register. The Data Register outputs then apply the data to the inputs of Data Driver gates A5 and B5 to await transfer to the CPU. The $\overline{\text{Read Clock}}$ signal at connector pin H clocks the Parity flip-flop G2-9. If there is a parity error G2-9 will set and send a $\overline{\text{Read Parity}}$ signal to the control pcb, via connector pin B24, to be processed.

The $\overline{1 \text{ to BRK}}$ pulse produces an $\overline{\text{MTT BRK REQ}}$ at the control pcb. This is sent to the multiplexor which responds with a Data to MB In signal at connector pin B16 to strobe the data out to the CPU via output Data Drivers A5 and B5.

When motion starts $\overline{\text{Tape Run}}$ releases scalers I4 and I5. When the start sequence has ended the control pcb sends clocks to the data pcb and I4 and I5 will scale. Each $\overline{\text{Gated Read Clock}}$ resets the scalers via I3-3, G1-1, and I3-6. When the record has been read the $\overline{\text{Gated Read Clock}}$ signals stop and I4 and I5 are allowed to scale through to initiate a normal stop sequence.

READ LONG GAP

The controller starts a normal read sequence. When no $\overline{\text{Read Clock}}$ signals reach the control pcb, no $\overline{\text{Gated Read Clock}}$ signals are produced to send to the data pcb. The absence of a $\overline{\text{Gated Read Clock}}$ for 16 word times causes the most significant bit of scaler I5 to set and produce a 1 to Stop signal. This indicates a blank detect condition to the control pcb which will then start a normal stop procedure.

READ EOF

An EOF is coded as two successive 23 octal characters. Gates F5 and G4-12, and G4-8 recognize the code of 23; G4-8 enables gate H5-6 and flip-flop H3-9 via inverter G3-9. The trailing edge of the first $\overline{\text{Gated Read Clock}}$ sets flip-flops H3-9 and H3-6. H3-9 enables H5-6 previously conditioned by G4-8 and $\overline{\text{WEOF}}$ on pins 5 and 3 respectively. H5-6 output puts a low level on the D input of H3-5. The Gated Clock leading edge clocks H4-12 to a set condition. The second $\overline{\text{Gated Read Clock}}$ toggles H4-12 to a reset condition and the Q output clocks H4-9 to a set state. Flip-flop H4-9 set condition indicates that two characters have been read. The trailing edge of the second $\overline{\text{Gated Read Clock}}$ resets H3-5. The output of H5-8 then goes low, and is inverted by G3-7, and applied to the control pcb via connector pin B14 to indicate an EOF has been received.

When H4-9 is set the $\overline{Q}$ output disables the K input of H4-12. H4-12 can now only be set, and not reset. If a third $\overline{\text{Gated Read Clock}}$ arrives it sets H4-12 and the $\overline{Q}$ output disables H5-8. This invalidates any EOF codes by removing the EOF signal. Any further clocks will have no effect.

The MTT motion stops in the normal manner.

CRCC GENERATION

The CRCC Register is originally reset so that its content is zero. The Q outputs of the CRCC Register are applied to one input of the full adders D1, D2, D3, D4, D5; the Q outputs of the Data Register are applied to another input. The Parity Generator output from F4 is applied to adder D5-9 pin 12 via F4-6 and G3-1. The outputs of the full adders are applied to the next most significant flip-flop in the CRCC Register. When the CRCC Register is clocked (at the same time as $\overline{\text{Write Clock}}$) the adders accomplish the add and shift portion of the CRCC generation. The output of adder D5-7 is fed back to an input of each of D1-9, D2-7, D2-9, and D3-7. This causes register flop Q outputs at C3-10, C3-7, C3-6, and C4-9 to be inverted if the parity bit, at flop C4-6 output, becomes a 1 when the register is shifted. Inverters B1 and C1 invert the contents of the CRCC Register, except flops C3-10 and C3-6, to write the CRC character on tape.

NOTE: A description of how CRCC is actually written on tape is contained in the Write Data Sequence portion of this description.

The 7-track MTT Readcheck and Status pcb operates in exactly the same manner as the 9-track pcb, 10246. The cyclic redundancy check character circuitry is not used on 7-track magnetic tape and is not included on this pcb.

The MTT Readcheck and Status pcb provides error detection during a read data sequence, including read after write, by enabling appropriate status bits to the CPU. Status bits are also generated to indicate to the CPU the current state of the MTT.

The pcb contains a longitudinal redundancy check character register (LRCC), the cyclic redundancy check character register (LRCC), the cyclic redundancy check character register (CRCC), and the status output gates.

LRCC

The parity bit and eight data bits are applied to the pcb via connector pin group B to L, left side. The inputs are applied via DTL receiver-inverters H1-2 to E1-6 to the J and K inputs of the LRCC register – J-K flip-flops H2-13 to A2-8. The Read Clock input to the pcb, via connector pin B32, is applied through gates A5-8, C2-6, and A1-6 to the C inputs of the register flops.

The flop resets are connected in common to power driver A3-8, which is pulsed by the output of monostable C5-6. The monostable is triggered by the Tape Run pulse at connector pin B8 and resets the register each time a Tape Run pulse occurs.

When the first data word occurs the register J-K inputs will be either high or low, depending upon whether the corresponding data bit is a 1 or 0. Any flop with a high input will toggle when a Read Clock arrives; any flop with a low input will remain in the same state. Thus a flop receiving an even number of ones will always be in the reset condition.

The number of ones on each track in NRZ magnetic tape recording is always even because of the LRCC written by the write amplifier reset strobe. Therefore if the LRCC is correct the register will be all reset at the end of each data transfer.

The $\overline{Q}$ outputs of all the J-K flops are applied to the multiple inputs of IOR gate C1-8. When a correct LRCC state exists all the $\overline{Q}$ outputs will be high, causing C1-8 to be low. This low level is applied to NAND gate J5-11 as a positive going pulse. IOT 6541 is applied to connector pin B3 at Read Status time to strobe the LRCC status to the CPU accumulator via J5-11 and connector pin B7.

During Reverse motion connector pin B9, Forward, will be high to D5-8 pin 9, which will make C2-6 pin 4 low to cause an inhibit state and prevent Read Clocks being applied to the register.

CRCC

CRCC Handling

Nine-track magnetic tapes are written with a Cyclic Redundancy Check Character (CRCC) at the end of each data block.

The CRCC is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only. When reading, it can also be used in conjunction with the VRC and LRCC checks for error correction, provided that the errors are confined to a single channel.

The character is generated in the CRCC register, which consists of nine flops, designated CP, and C0 to C7. (IBM use the designations P, parity, and 0 to 7, ie. 2^7 to 2^0).

With the register originally reset to zero the CRCC character is generated as follows (refer to the following figure and tables).

1. All data characters are added to the CRCC register without carry (each bit position n is exclusive ORed to C).
2. Between additions the CRCC register is shifted one position (CP to C0.....C7 to CP).
3. If a shift causes CP to become 1 the bits being shifted into C2, C3, C4, and C5 are inverted.
4. After the last character has been added the CRCC register content shifts again in accordance with steps 2 and 3.
5. Before writing the register contents onto tape the contents of all positions, except C2 and C4, are inverted. The parity CRCC is odd if the number of data characters within the block is even, and the parity is even if the number of characters within the block is odd. The CRCC may only contain all 0-bits if the number of data characters is odd.
6. Its value is such that the LRCC always has odd parity.

To check CRCC in a Forward command the CRCC register recalculates the CRCC. When the original CRCC is combined with the new CRCC, the result should be a match pattern of 111010111 in the CRCC register; Table 1b shows this function.

To check CRCC in a Reverse command, the significance of the data bits entering the CRCC register must be reversed; Table 1c shows this function.

The figure gives details of circuit implementation. The full adders can be used to provide the exclusive OR and inverse exclusive OR function by the setting of Ci to a 0 or a 1, for example:

ci	A	B	S	
0	0	0	0)	
0	0	1	1)	
0	1	0	1)	exclusive OR
0	1	1	0)	
1	0	0	1)	
1	0	1	0)	not exclusive
1	1	0	0)	OR/equivalence
1	1	1	1)	

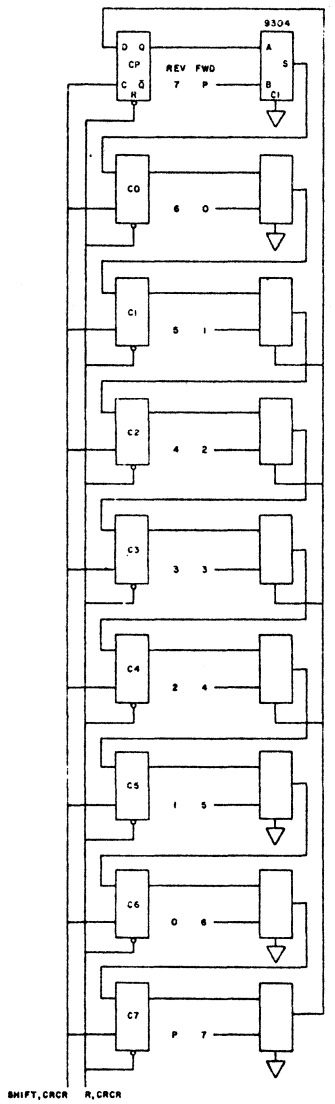


Table 1a: FORWARD CRCC GENERATION

IBM SIG		P	0	1	2	3	4	5	6	7	
BIT SIG		P	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
CP 1/P = 1		CP	C0	C1	$\overline{C2}$	$\overline{C3}$	$\overline{C4}$	$\overline{C5}$	C6	C7	
CRC TO TAPE		$\overline{CP}$	$\overline{C0}$	$\overline{C1}$	C2	$\overline{C3}$	C4	$\overline{C5}$	$\overline{C6}$	$\overline{C7}$	CRC PARITY
RESET		0	0	0	0	0	0	0	0	0	
CHAR 1		0	0	0	0	0	0	0	0	1	
ADD. SHIFT		1	0	0	1	1	1	1	0	0	
	CRC	(0	1	1	1	0	1	0	1	1)	EVEN
CHAR 2		0	0	0	0	0	0	0	1	0	
ADD. SHIFT		0	1	0	0	1	1	1	1	1	
	CRC	(1	0	1	0	0	1	0	0	0)	ODD
CHAR 3		0	0	0	0	0	0	1	0	0	
ADD. SHIFT		1	0	1	1	1	0	0	0	1	
	CRC	(0	1	0	1	0	0	1	1	0)	EVEN
CHAR 4		0	0	0	0	0	1	0	0	0	
ADD. SHIFT		1	1	0	0	0	0	0	0	0	
	CRC	0	0	1	0	1	0	1	1	1	ODD

Table 1b: FORWARD CRC CHECKING

CHAR 4		0	0	0	0	0	1	0	0	0	
ADD. SHIFT		1	1	0	0	0	0	0	0	0	
	CRC	(0	0	1	0	1	0	1	1	1)	ODD
CRC		0	0	1	0	1	0	1	1	1	
ADD. SHIFT		1	1	1	0	1	0	1	1	1	TEST FOR MATCH PATTERN

Table 1c: REVERSE CRC CHECKING

IBM SIG		7	6	5	4	3	2	1	0	P	
RESET		0	0	0	0	0	0	0	0	0	
CRC		1	1	1	0	1	0	1	0	0	
ADD. SHIFT		0	1	1	1	0	1	0	1	0	
	CRC	(1	0	0	1	1	1	1	0	1)	EVEN
CHAR 4		0	0	0	1	0	0	0	0	0	
ADD. SHIFT		0	0	1	1	0	0	1	0	1	
	CRC	(1	1	0	1	1	0	0	1	0)	ODD
CHAR 3		0	0	1	0	0	0	0	0	0	
ADD. SHIFT		1	0	0	1	0	1	1	1	0	
	CRC	(0	1	1	1	1	1	0	0	1)	EVEN
CHAR 2		0	1	0	0	0	0	0	0	0	
ADD. SHIFT		0	1	1	0	1	0	1	1	1	
	CRC	(1	0	0	0	0	0	0	0	0)	ODD
CHAR 1		1	0	0	0	0	0	0	0	0	
ADD. SHIFT		1	1	1	0	1	0	1	1	1	TEST FOR MATCH PATTERN

CRCC Check

The CRCC Register consists of the nine flops I4-5 to E4-9, CP to C7. The leading edge of the Tape Run signal at connector pin B8, via monostable C5-6 and power driver A3-6, sets the register to its zero state. This ensures that the register is reset before the first data character is received at the beginning of each data block. The Q output of each register flop is applied to the A input of its associated full adder flop, I3-7 to D3-7.

When the first data word is applied from the Read Data connector pins B to L to the B inputs of the adder flops via the receiver-inverters, H1-2 to E1-6, all of the A inputs will be low (the register was reset by Tape Run). Therefore the sum output of the adders will correspond to the applied data at the B inputs (e.g. if the data applied to H3-7 pin 3 is high then pin 7 will be high).

The first data word presented to the register is 1_8, refer to the figure. This will cause the B input of adder flop D3-7 pin 3 to go high; the B input was low from E4-9 because of the initial reset from Tape Run. Consequently the sum output at D3-7 pin 7 will be high and the $\overline{sum}$ output at pin 6 will be low. Pin 6 is fed back to pin 12 (ci) of H3-10 and G3-10. Pin 7 is fed back to pin 4 (ci) of H3-7 and G3-7 to cause inversion of bits 2^5, 2^4, 2^3, and 2^2 (refer to CRCC Handling).

The CRCC Register will perform an add-shift function for every data word applied to the pcb; the final word is the CRCC as originally written on the tape. When this word is exclusive ORed to the re-generated CRCC the result is a match pattern, refer to the figure. The pattern is checked by 10-input IOR gate H5-8. The gate inputs are individually derived from the Q outputs of the CRCC Register flops. Thus when a match pattern exists in the register all of the inputs to H5-8 will be high, causing pin 8 to go low as a wired OR with inverter D5-6 to CRCC Error flop D4-5 pin 2. The wired OR ensures that the CRCC Error flop can not be set during a Reverse motion.

It is possible for the tape CRCC character to be all zeros, therefore the facility to produce a phantom strobe has been provided for use when it has been determined that the CRCC is zero data. Under normal read data conditions, including read after write, the read data strobe, Read Clock, is applied via connector pin B32 to inverter B3-8 pin 9 and IOR gate A5-8 pin 9. Therefore Read Clocks appear at A5-8 for every word read off the tape. The positive-going clock pulses at B3-8 are applied to a retriggerable 150 μs Monostable 1, B4-7 pin 4. Thus the monostable will be continuously set while Read Clocks are being received. B4-7 $\overline{Q}$ will be low to flop C3-5 pin 3 during this time, causing it to remain reset.

If the read strobe is absent from B4-7 pin 4 for more than 200 μs, i.e., four character spaces, the monostable will not be retriggered. Consequently pin 7 will go high to clock flop C3-5, which in turn triggers the 150 μs Monostable 2, B4-10 whose Q output causes the D input of flop D4-9 to go high. If the CRCC is not zero data a Read Clock pulse will arrive at D4-9 pin 11 and set the flop. The Q output is connected to the direct set and latches the flop once it is set; the $\overline{Q}$ output also inhibits NAND gate A5-11 pin 12 to inhibit the phantom strobe, generated by B4-10, to allow the normal read data condition. If the CRCC was zero data D4-9 would not set, therefore NAND gate A5-11 would be enabled and the Read Clock strobe would pass through to clock the registers.

The phantom strobe is generated by the positive to negative transition of Monostable 2. Assuming that the input to inverter A5-6, pins 4 and 5, and NOR gate B5-10 pin 9 are logic high, the output of B5-10 will be low (because of pin 9). When B4-10 goes low B5-10 pin 9 will immediately follow the change, while the input to B5-10 pin 8 is slowed by the 680 pf capacitor. Thus at some time both inputs to the NOR gate are low for a pulse period with the pulse width depending upon the capacitor.

The trailing edge of the phantom strobe circuit output pulse clocks the CRCC Error flop D4-5, via inverter A5-3; the flop is cleared by IOT $\overline{6532}$ from connector pin B2.

The flop E4-5 ensures that the Record Longer than Word Count status does not give a false indication, due to the extra CRCC strobe.

TAPE TRANSPORT SELECTION

The four Transport Select flip-flops, J3 and J4, bottom left, provide capabilities for selecting one of up to four tape transports. The select bit is presented to the D inputs and IOT 6521 is presented to the C inputs of the four flops. The appropriate flop will set and its output will be buffered and inverted by its associated inverter, J1-3, J1-4, J1-10, or J1-11, and applied to the select line of the required MTT via connector pins S, R, T, and U.

If an MTT has not been selected and an attempt is made to issue tape commands a Set Illegal status will be generated, via exclusive OR gates J2 and connector pin B31. This status will also occur if more than one MTT is selected simultaneously.

J3-5 and J3-9 flop outputs are connected to exclusive OR gate J2-8; J4-5 and J4-9 outputs are connected to J2-3. The outputs of both gates are connected to exclusive OR gate J2-6. If none of the Select flops are set the inputs to J2-8 and J2-3 will be low, causing the outputs to be low to J2-6 to provide a Set Illegal condition. When an MTT is correctly selected a high level will appear at J2-6.

STATUS OUTPUT

The status outputs are provided by the 12 power NAND gates FG5-3 to J5-4 (top of illustration) which provide the following status information when enabled by IOT 6541 at connector pin B3:

Vertical Parity	EOF
Illegal Command	Busy
EOT	CRCC Error
BOT	LRCC Error
Record Longer than Word Count	Transport Not Ready
Record Shorter than Word Count	No Write Ring

The IOT generator decodes both positive and negative pulses, IOT 6501 to IOT 6554; the multiplexor transfers break requests from the drum and MTT to the CPU. Although mounted on the same pcb, the two units function independently of each other.

IOT GENERATOR

The IOT generator is detailed on the left portion of the illustration; apart from the Drum and MTT IOTs three other pulses are generated to control the software flag. The flag comprises R-S flop G2-3 and F5-6 (bottom centre).

Pulse IOT 6461 (Skip if Software flag is false) senses the status of the R-S flop through gate G5-4. The decoded pulse from NAND gate G2-11 is inverted and applied to G5-4 pin 5. The $\overline{Q}$ side of the R-S flop is applied to G5-4 pin 6. A Skip pulse is generated, at connector pin B9, if IOT 6461 is issued and the R-S flop is reset.

Pulse IOT $\overline{6462}$ (Reset Software flag) resets the R-S flop through gate G2-8. When the CPU is not running a B Run (1) level appears at connector pin A13 (bottom left) to reset the R-S flop F5-6 at pin 3.

Pulse IOT $\overline{6464}$ (set Software flag) sets the R-S flop through gates G2-6 and G2-3. If the R-S flop is true the output of G2-3 is inverted and goes low to connector pin A9 to create a Program Interrupt level.

A $\overline{\text{Clear Accumulator}}$ pulse will be generated (top left) if any one of nine instruction exist. The instructions are applied through IOR gates D5, E5, and G5 to connector pin B11.

The nine IOT instructions are: $\overline{6502}$, $\overline{6504}$, $\overline{6512}$, $\overline{6522}$, $\overline{6524}$, $\overline{6534}$, $\overline{6541}$, $\overline{6551}$, and $\overline{6552}$. Four of the output pulses ($\overline{6522}$, $\overline{6524}$, $\overline{6551}$, and $\overline{6552}$) are differentiated prior to the power drivers to shorten the pulse length from 600 to 400 ns.

MULTIPLEXOR

The multiplexor routes the break requests from the MTT or drum to the CPU, and handles the CPU responses in sequence. Neither of the breaks have priority. Initially either drum or MTT can take command of the data break and consequently block the break request from the other unit.

The $\overline{\text{MTT Break Request}}$ and $\overline{\text{Drum Break Request}}$ are applied to the pcb via connector pins B7 and A16 respectively (right side). The $\overline{\text{Drum Break Request}}$ is inverted and applied to NAND gate F1-8 pin 11, which is enabled if the MTT break request is not in progress. The $\overline{\text{Drum Break Request}}$ is also routed through C1-8, F2-6, E1-3, and C5-4 to pull down the CPU break request line via connector pin B25. F1-8 also will go low to inhibit the $\overline{\text{MTT Break Request}}$ at F1-12 pin 13 and enable D1-6 pin 2. D1-6 goes high to connector pin B21 to provide the Drum Address to DA (Data Address) pulse requesting the Current Address Register on the WC & CA pcb, 10442, to gate the correct address onto the ADR lines of the CPU.

When the break request has been issued to the CPU and the Drum Address has been applied to the ADR lines (on pcb 10442) the CPU issues an Address Accepted pulse to the pcb via connector pin A21. The pulse is inverted through E1-11 and applied as a high level to NAND gate C1-3 pin 2. C1-3 pin 1 is high because of the original break request. C1-3 goes low to D1-1 so that D1-6 will hold the Drum Address to DA level high. Therefore the R-S flop C1-3, D1-6 is controlled by Address Accepted (connector pin A21) once the drum break has been issued.

The pulse also appears at connector pin A32, Drum Address Accepted, for the duration. It cancels the original drum break request or the Drum Control pcb, 10282, and increments the word count and current address portions of pcb 10442. The pulse is also applied through B1-6 pin 4 to E5-3 pin 1; E5-3 pin 2 will be high for a read transfer only. E5-3 is enabled and H5-8 issues a strobe, Drum Data to MB In, via connector pin A36. The B1-6 positive pulse is also applied to B1-8 pin 12 to produce a pull-up pulse, MB Out to Drum Data, at connector pin A33. The pulse returns to a high level at the end of its duration and strobes the BMB line into the Derandomizer Write Register. The B1-6 positive pulse is also applied to C5-13 pin 11 to inhibit E5-3 if there is also a Drum Write input at connector pin B30. C5-13 also sets the Transfer Direction low to the CPU at connector pin B28.

The original Address Accepted pulse from the CPU is 400 ns wide; when it terminates C1-3 will go high. The Drum Break Request was cancelled earlier, therefore F1-8 is high to D1-6 pin 2, and cancels the Drum Address to DA and Drum Address Accepted levels at connector pins B21 and A32. The R-S flop B1, A1 remains set until a BTS 3 Delayed pulse appears at connector pin A30. BTS 3 from connector pin A37 is delayed by the A5 inverters for 100 ns for timing considerations.

Thus, a state exists where the break cycle has commenced at the CPU, the Address Accepted pulse has been timed out, and the data transfer, in or out, is due. BTS 3 Delayed goes low to A1-11 pin 12 to reset the R-S flop. B1-6 will go low and power driver B1-8 will provide a positive level change to connector pin A33 (MB Out to Drum Data) as explained previously. The positive edge transfers the data from the MBs to the Derandomizer pcb as the final operation in the drum break cycle.

The MTT Break Request is applied in a similar manner to the drum request, providing the drum is not transferring data. The MTT Break Request level at connector pin B7 is inverted to apply a high level to F1-12 pin 1 and inverter F2-7 pin 8. The inverter output is applied to E1-3 pin 2 (similar to the drum cycle) to put a Break Request to connector pin B25 via C5-4. NAND gate F1-12 functions as in the drum cycle — the MTT request must not be pre-empted by the drum request — and the drum request must not be in progress. If these conditions are met, F1-12 goes low to D1-8 pin 10; pin 8 goes high to connector pin A25, MTT Current Address to Data Address. As with the drum cycle the pulse goes to the Word Count Current Address pcb to put the current address into the ADR line of the CPU. An Address Accepted pulse is issued by the CPU when it recognizes the break request. The pulse is applied via connector pin A21 and E1-11 pin 12 to C1-11 pin 13; pin 12 is held high by D1-8 (similar to the drum address accepted circuit). Therefore pin 11 goes low to hold D1-9 low for the duration of the Address Accepted pulse and to set the MTT Data Transfer R-S flop C1, A1.

When the flop is set it signals, via C5-1 and connector pin B28, that the cycle is ready to accept data to or from the CPU. G5-13 pin 12 goes high when the flop sets; pin 11 is high during a read cycle and G5-13 generates a strobe, MTT Data to MB In, via H5-6 and connector pin A26. An MTT Write level, connector pin A27, places a high on A1-6 pin 5 to enable that gate and produce an MB Out to MTT Data level at connector pin B31 during a Write sequence. It also inhibits G5-13 via C5-1, which is low.

The output at C1-11 is also applied to connector pin A23 as the MTT Address Accepted pulse to cancel the MTT Break Request on the MTT Control pcb 10285. When the MTT Break Request terminates, the MTT Address to DA (connector pin A25), and MTT Address Accepted (connector pin A23) pulses terminate.

The BTS 3 Delayed pulse resets the MTT Data Transfer R-S flop C1, A1 and causes a positive output at A1-8. The transition at C1-6 goes low and is shaped into a 100 ns positive pulse by the A5 circuitry. During Write conditions this output pulse strobes the data to the MTT Data pcb via A1-6 and connector pin B31.

An R-C network between F1-12 and F1-8 pin 9 prevents parasitic oscillations.

The circuitry consists basically of four 12-bit binary counters, which control high speed data break transfers between the CPU and magnetic storage drum, and the CPU and magnetic tape transport. The pcb contains two similar circuits: one for the drum and one for the MTT. Each circuit consists of two presettable 12-bit binary counters: one for current address and one for word count. The drum circuitry only will be described.

WORD COUNT (WC)

The drum word count register, D1, F1, H1 counts the number of words transferred between the drum and the CPU. It is initially preset to a value that is the two's complement of the total number of words to be transferred. This value is supplied by the CPU BAC lines 00 to 11, connector pin group B40 to A4. The drum WC register consists of 4-bit binary counters D1, F1, and H1. The register is preset by IOT 6522 via connector pin A2 and inverter H5-12.

The drum word count register is incremented during each break cycle via the Drum Address Accepted pulse at connector pin B4 (lower left). This pulse is routed via F5-3 and gated by B Break (0) at F5-11 to prevent noise from incrementing the registers when a break cycle is not in progress. A pulse generator, consisting of G5-10, G5-6, and G5-4, produces a 150 ns pulse which is transmitted via F5-8 to clock the drum WC register. (It also clocks the drum CA register, consisting of D3, F3, and H3.)

When the most significant bit of the drum WC register changes from a one to a zero (i.e. overflow) a Drum WC Overflow pulse is produced at connector pin B37. This indicates to the Drum Control pcb that the desired number of words have been transferred.

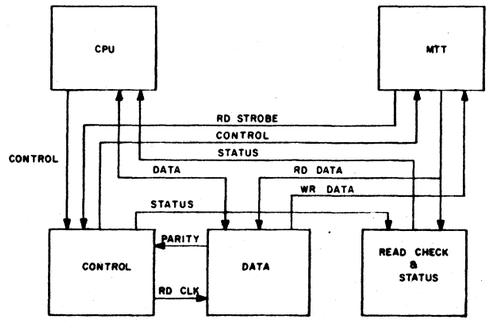
CURRENT ADDRESS (CA)

The Drum Current Address Register consists of 4-bit binary counters D3, F3, and H3. These are preset via IOT 6524 at connector pin B2. The CA register value indicates to the CPU which address in memory is to be used for data transfer. The 12-bits are capable of addressing 4096 memory locations. The drum Extended Memory Address Register consists of three flip-flops E5, D5, and C5. The flops are used to select one of the eight 4096 word memory fields which is to be used in the transfer. This register is loaded via IOT 6544 at connector pin A24 from accumulator bits 06, 07, and 08.

The value held in the drum CA and drum EMA registers is applied to open collector NAND gates E3, G3, I3, and C3. The 15-bit value is gated onto the Data Address bus lines by the Drum Address to DA pulse applied at connector pin A13 (top left).

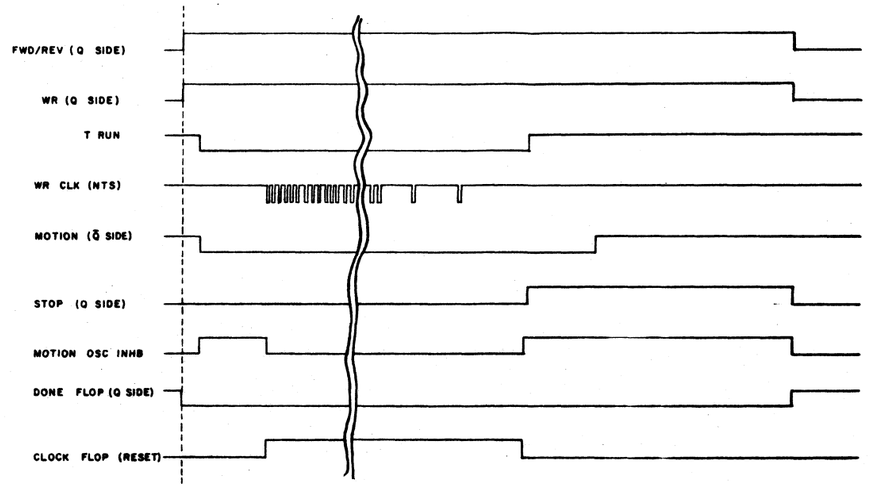
B RUN CONDITIONING

The $\overline{\text{B Run}}$ signal is taken directly from the CPU to connector pin A27 then through a noise suppression circuit consisting of an integrator and Schmitt trigger. This circuit is capable of rejecting high-going noise pulses up to 4 µs wide. The signal is inverted by paralleled power gates, B5-6 and B5-8, and fed to the CCL logic via connector pin A26.



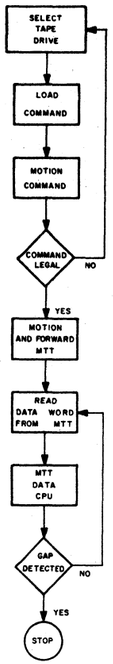
DATA CONTROL AND STATUS ROUTING

FIGURE 5-1



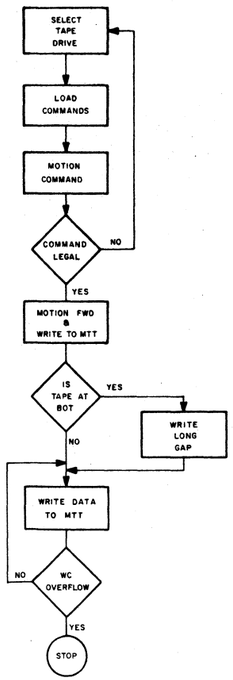
MTT WRITE CYCLE TIMING

FIGURE 5-5



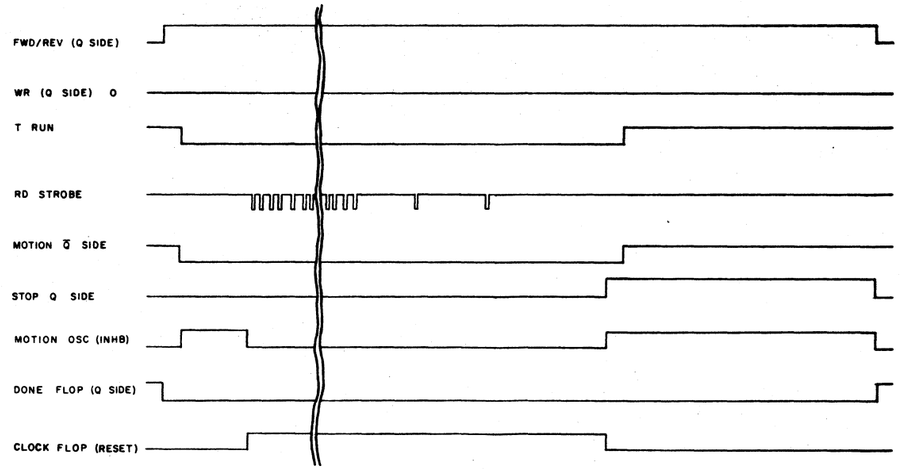
READ DATA FLOW

FIGURE 5-2



WRITE DATA FLOW

FIGURE 5-3



MTT READ CYCLE TIMING

FIGURE 5-4

rev	eco	description	date	by	chk	apprvd

used on | drawn

scale: 23 AUGUST 71 (date) | design apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

checked | final apprvl | material | finish

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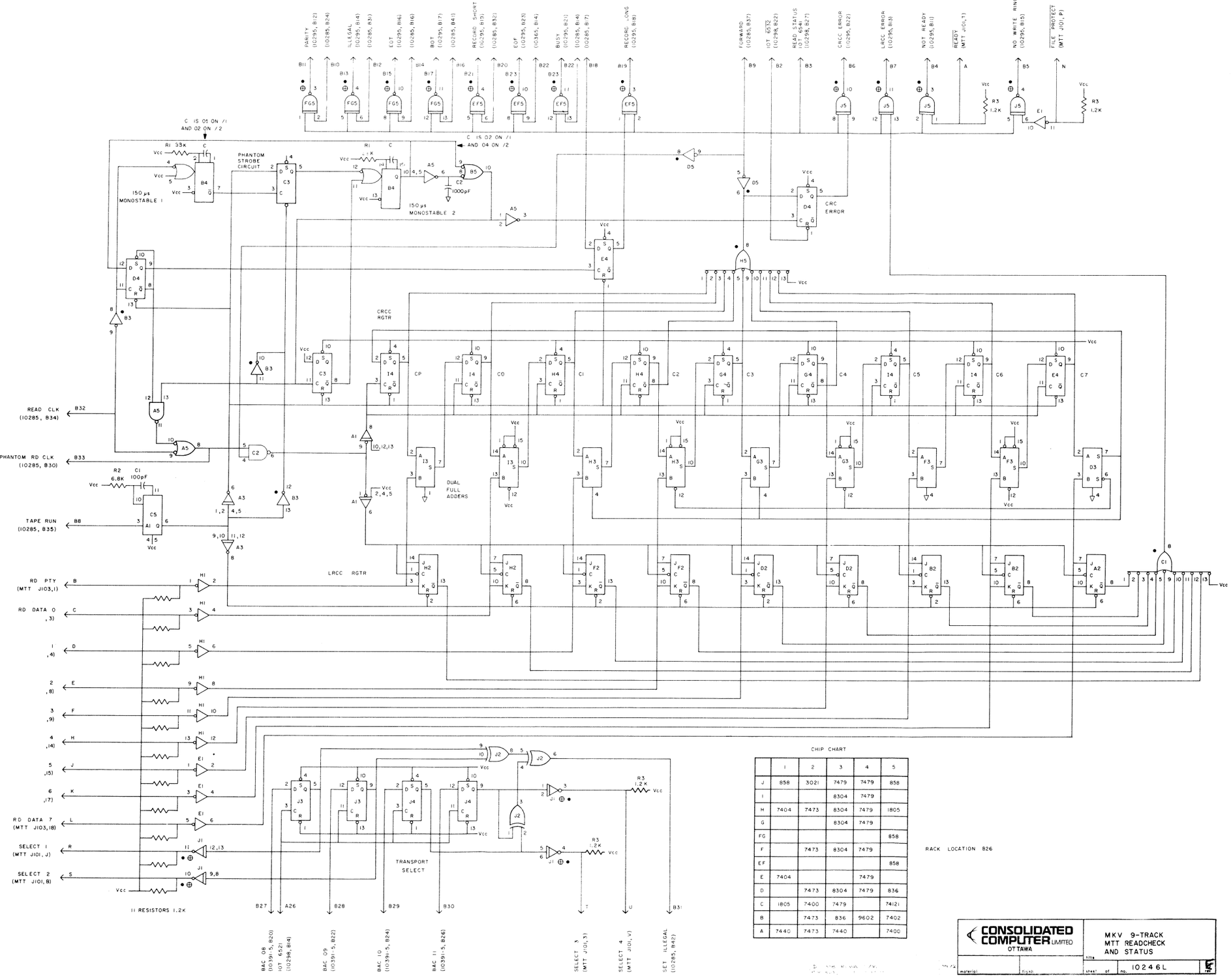
OTTAWA

title: MTT

sheet of | no.



CHIP CHART

	1	2	3	4	5
J	858	3021	7479	7479	858
I			8304	7479	
H	7404	7473	8304	7479	1805
G			8304	7479	
FG					858
F		7473	8304	7479	
EF					858
E	7404			7479	
D		7473	8304	7479	836
C	1805	7400	7479		74121
B		7473	836	9602	7402
A	7440	7473	7440		7400

RACK LOCATION B26

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MKV 9-TRACK MTT READCHECK AND STATUS

10246L

	5	4	3	2	1
A	836				
B	7430	7493	7479	7440	836
C	7420	7493	7479	7479	858
D	7410	7493	7400	7410	7400
E	7400	7493	836	7430	
F	7403	7479	7400	7479	858
G	7400	7400	7400	846	836
H	7479	7479	7479	7479	7402
I	7479	7479	7400	7400	8601

RD RCL ← B15
GATED READ CLOCK ← F ← B34
READ CLOCK ← B
FILE PROTECT ← D
EOT ← A
ILLEGAL ← B31
READY ← C
SET WRITE STATUS ← J
IOT G551 ← B38
IOT G552 ← B29
B RUN ← B19
BOT ← B41
RUN ← B35
LOAD POINT ← U
RWC ← S
(SFC) FOR ← T ← B37
(SRC) REV ← R
OFF LINE ← E
VCC ← A1, B1
GND ← L22
GND ← A43, B43

READ CLOCK PHANTOM STROBE → B30
PAR ERROR → B12
PARITY → B24
EOT → B16, B42
SET ILLEGAL → B14
BUSY
CLOCK → B40
WE oF + WLG → B13

B20 → IOT G534
B22 → SKIP BUS
B21 → IOT G531
B28 → INT REQ BUS
B18 → IOT G532
B19 → B RUN (0)
B17 → REC LONG
B2G → MTT ADD ACC
B33 → WRITE DATA
B31 → 1-BRK
B36 → MTT BRK REQUEST
B23 → WC O'FLO

BAC1 IOT G542 ← B5, B8
BAC 4 ← B25
BAC 5 ← B2
BAC 0 ← B4
WRITE SELECT ← B3
BAC 2 ← B7
BAC 3 ← B9
WE oF ← B10
IOT G542 ← B6
1 STOP ← B11
REC SHORT ← B32

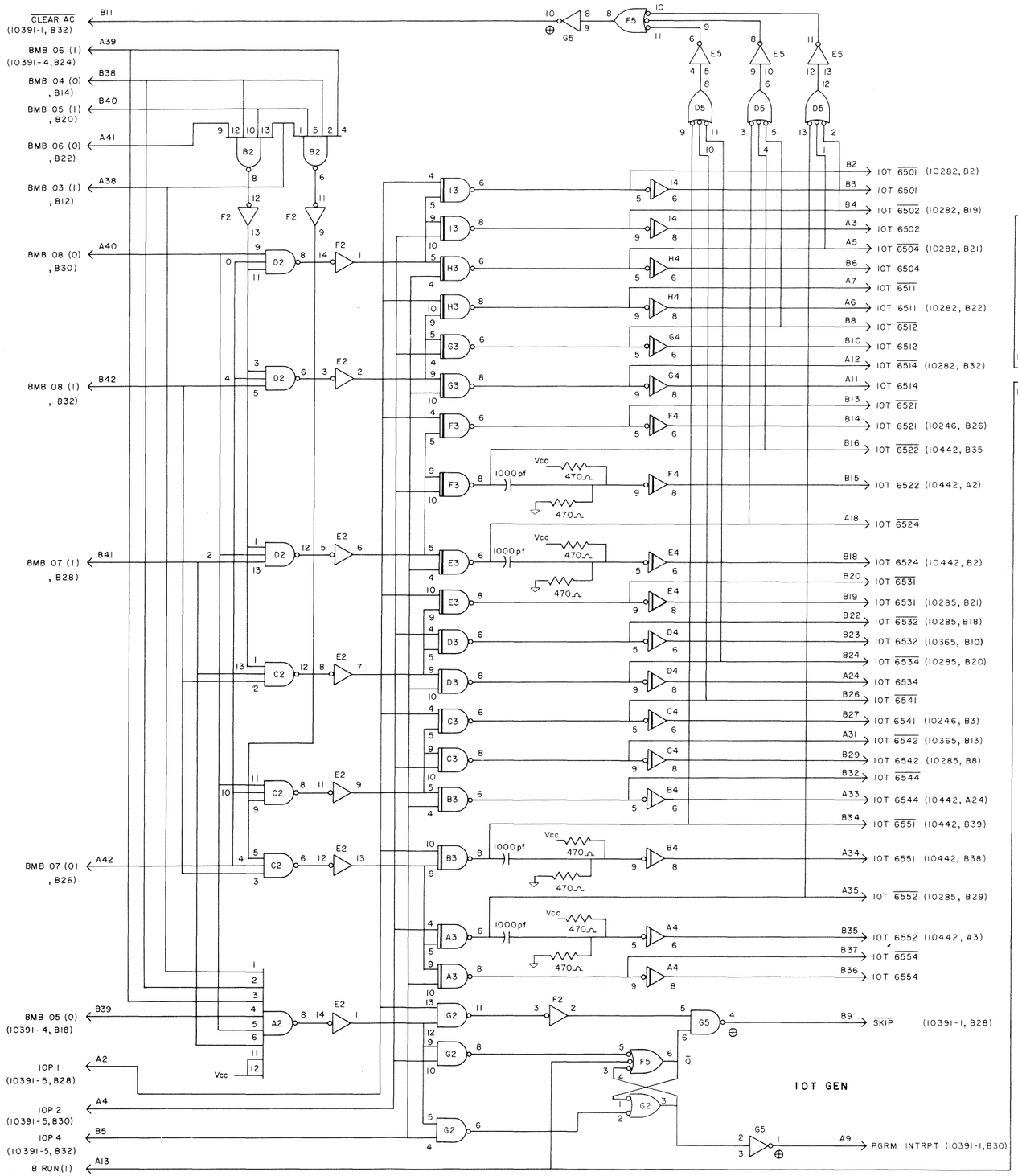
C7-C46 .01μf DECOUPLING CAPACITORS NOT SHOWN ON LOGIC

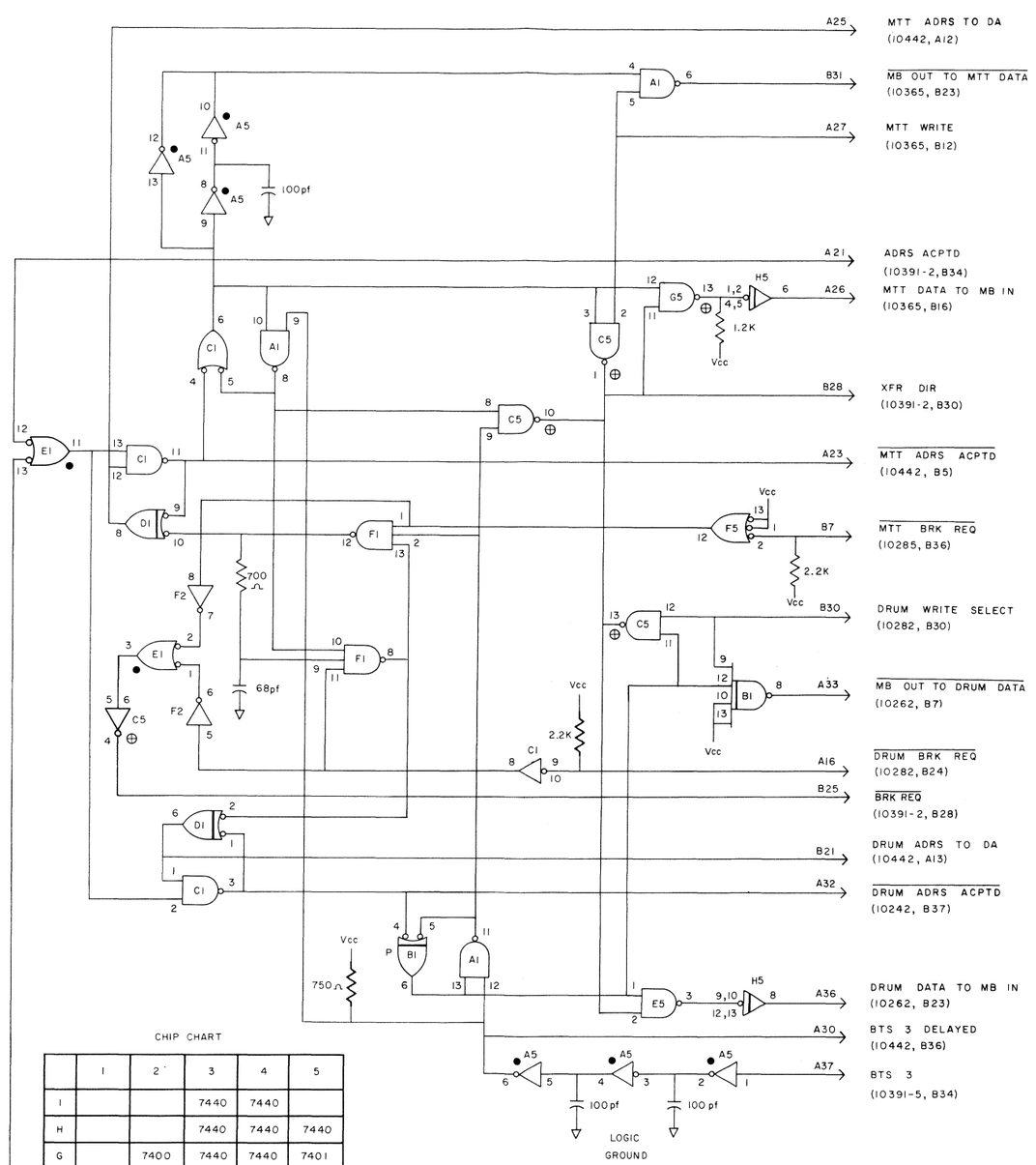
rev	eco	description	date	by	chk	apprvd
G	450	ECO KE 450 INCORP	25 SEPT 72	MJ		
F	399	RESISTOR ADDED, TRACK ADD.	14 SEPT 72	MJ		
E	300	Q1,2,4&5 CHANGED TO MPS 3704	26 MAY 72	MM		
D	252 254	REDRAWN, TRACK & TRANSISTOR REV.	19 NOV. 71	RK		

used on N.T.S. | scale | date 19 NOV. 71
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0°30'
drawn T.P. KINDS | design apprvl J. KAYE | checked | final apprvl J. KAYE
material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: PEC MAG TAPE CONTROL (556 BPI)
sheet 1 of 1 | no. D10285L/1 | G





CHIP CHART

	1	2	3	4	5
I			7440	7440	
H			7440	7440	7440
G		7400	7440	7440	7401
F	7410	475	7440	7440	7410
E	846	475	7440	7440	7400
D	7440	7410	7440	7440	7410
C	7400	7410	7440	7440	7401
B	7440	7420	7440	7440	
A	7400	7430	7440	7440	836

MULTIPLEXOR

RACK LOCATION A21

rev	eco	description	date	by	chk	apprvd
A	VE 1750	PRODUCTION RELEASE	15 JULY 72	LL		

used on | drawn R.M.
scale | date 3 SEPT 71 | design apprvl
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
checked
final apprvl VSD
material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: DRUM AND MTT MULTIPLEXOR IOT GENERATOR

sheet 1 of 1 | no. D10298L | rev

TRANSTEX IS 300-8-71

TRK 4 WRT PTY (MTT J102,L)
7 WRT DATA 7 ,V)
6 6 ,U)
5 5 ,T)
3 4 ,S)
9 3 ,R)
2 ,P)
8 1 ,N)
TRK 2 WRT DATA 0 (MTT J102,M)

(10391-3,B12) DATA 04 B29
DATA 05 ,B14 B34
DATA 06 ,B16 B20
DATA 07 ,B18 B27
DATA 08 ,B20 B38
DATA 09 ,B22 B41
DATA 10 ,B24 B37
(10391-3,B26) DATA 11 B42
(10298, A23) DATA TO MB IN B16

DATA DRIVERS
CRCC DRIVERS AND OUTPUT DRIVERS
CRCC REGISTER AND GENERATOR
DUAL FULL ADDERS PINS 1&8 TO Vcc
LOGIC GND
EIGHT RESISTORS 1.2K TO Vcc
DATA RCV
DATA RGTR
PARITY DRIVER
PARITY GEN
PARITY CHECK

TRK 2 RD DATA 0 (MTT J103,S)
8 1 ,A)
1 2 ,B)
9 3 ,J)
3 4 ,K)
5 5 ,L)
6 6 ,M)
7 RD DATA 7 ,N)
TRK 4 RD PTY 8 (MTT J103,T)

BMB 4 (10391-4, B16) B28
5 ,B20) B35
6 ,B24) B19
7 ,B28) B22
8 ,B32) B39
9 ,B34) B40
10 ,B36) B36
BMB 11 (10391-4, B38) B26
CLOCK (10285, B40) B3
TAPE RUN (10246, B8) B5
GATED RD CLK (10285, B15) B4

TIMING SCALERS
MONOSTABLE 3μs

B13 IOT G532 (10285, B6)
B24 (10285, B12) RD PTY
H RD CLK (MTT J103,2)
EOF DETECTION
B14 EOF (10246, B22)
RACK LOCATION B24

B15 WEOF (10285, B10)
B11 I TO BRK (10285, B39)
B12 WRT SEL (10285, B3)
B8 WRT DATA (10285, B33)
B7 I TO STOP (10285, B11)
J WRT CLK (MTT J102,A)
B23 MB TO MTT DATA (10298, B31)
B6 WLG+WEOF (10285, B13)
F WRT RESET (MTT J102,C)
B9 MTT ADRS ACPTD (10285, B26)

CHIP CHART

	1	2	3	4	5
J	74121	7479	7400	7493	7493
H	7400	7400	7479	7473	7410
G	475	7479	475	7410	7400
F	7440	475	4008	4008	7402
E	7440	4015	4015	7400	7440
D	8304	8304	8304	8304	8304
C	475	7479	4015	4015	7400
B	475	7401	7401	7401	7401
A		7401	7401	7401	7401

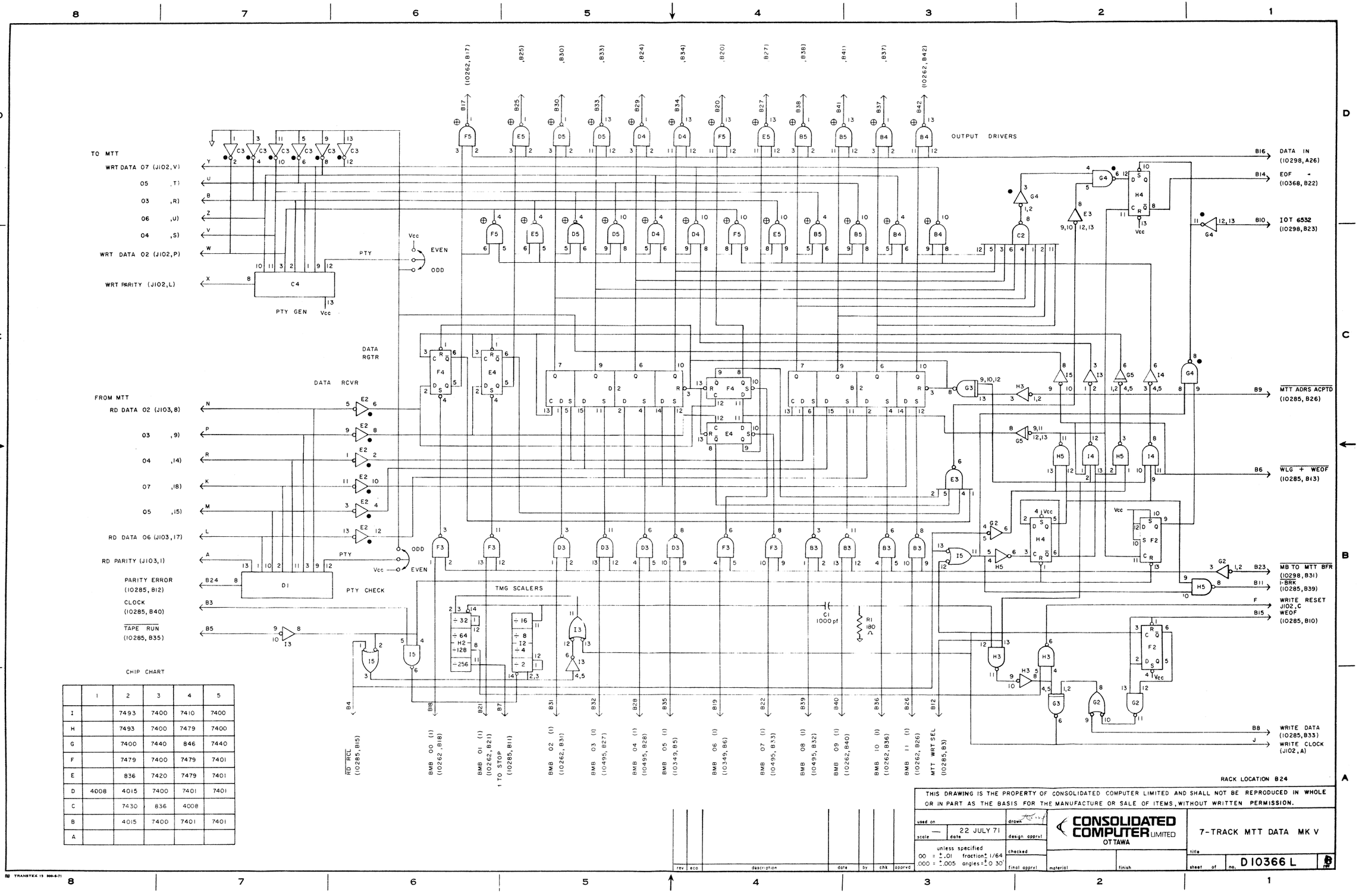
rev	description	date	by	chk	approved

used on | drawn | date
scale | design appvd
unless specified: .00 ± .01 fraction ± 1/64, .000 ± .005 angles ± 0° 30' | checked
material | finish | final appvl

CONSOLIDATED COMPUTER LIMITED OTTAWA

MK V 9-TRACK
MTT DATA

title
sheet of | no. 10365 L | rev B



CHIP CHART

	1	2	3	4	5
I		7493	7400	7410	7400
H		7493	7400	7479	7400
G		7400	7440	846	7440
F		7479	7400	7479	7401
E		836	7420	7479	7401
D	4008	4015	7400	7401	7401
C		7430	836	4008	
B		4015	7400	7401	7401
A					

rev	eco	description	date	by	chk	apprvd

used on — | scale — | date 22 JULY 71 | drawn | design apprvl | checked | final apprvl

unless specified
00 = ±.01 fraction ± 1/64
000 = ±.005 angles ± 0° 30'

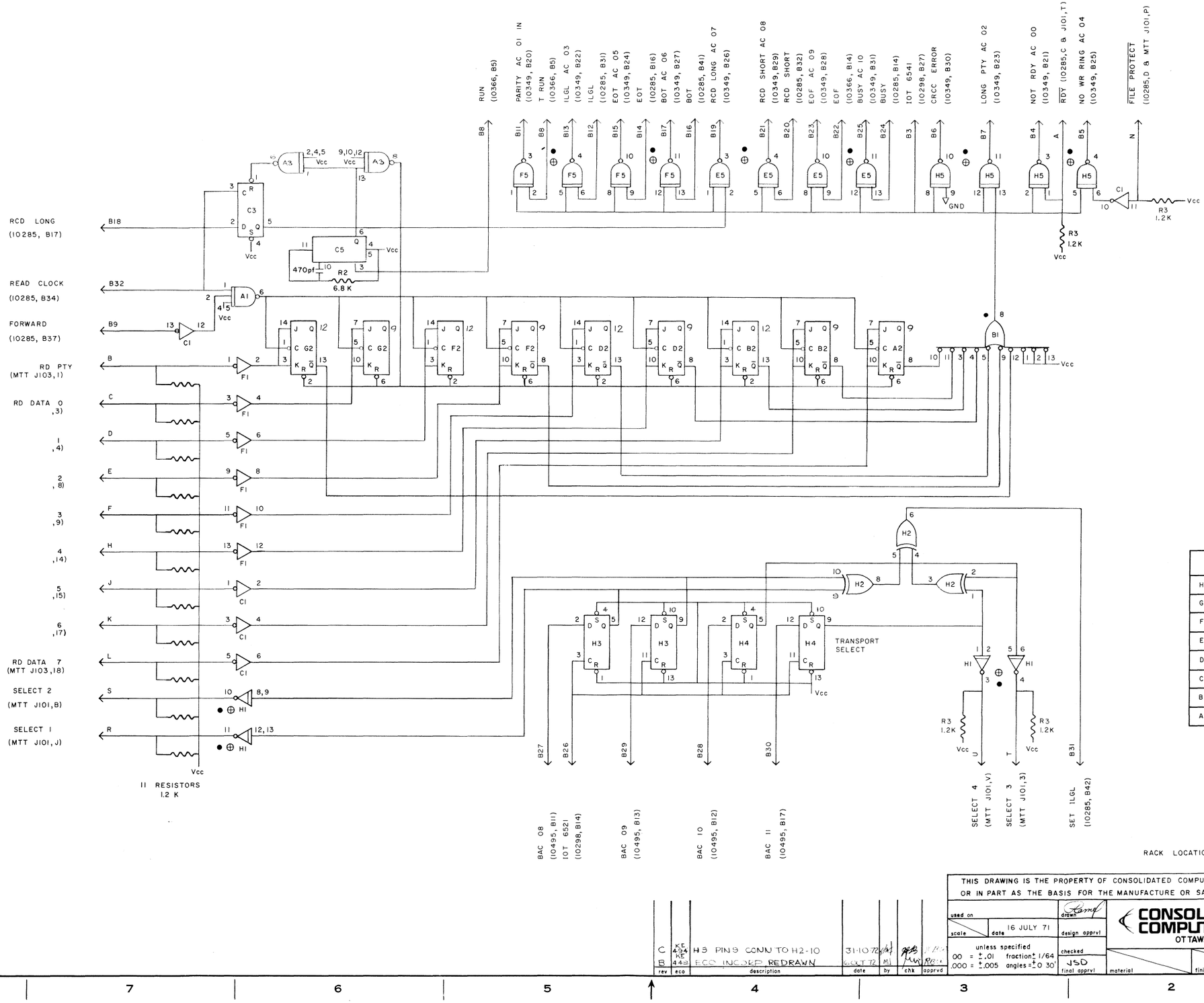
material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: 7-TRACK MTT DATA MK V

sheet of | no. D10366 L | rev B

TRANSTEX 15 800-6-71



CHIP CHART

	1	2	3	4	5
H	858	3021	7479	7479	858
G		7473			
F	7404	7473			858
E					858
D		7473			
C	7404		7479		74121
B	1805	7473			
A	7440	7473	7440		

RACK LOCATION B26

rev	eco	description	date	by	chk	apprvd
C	KE 484	H3 PIN 9 CONN TO H2-10	31-10-72	MJ		
B	KE 443	ECO INCDEP REDRAWN	6 OCT 72			

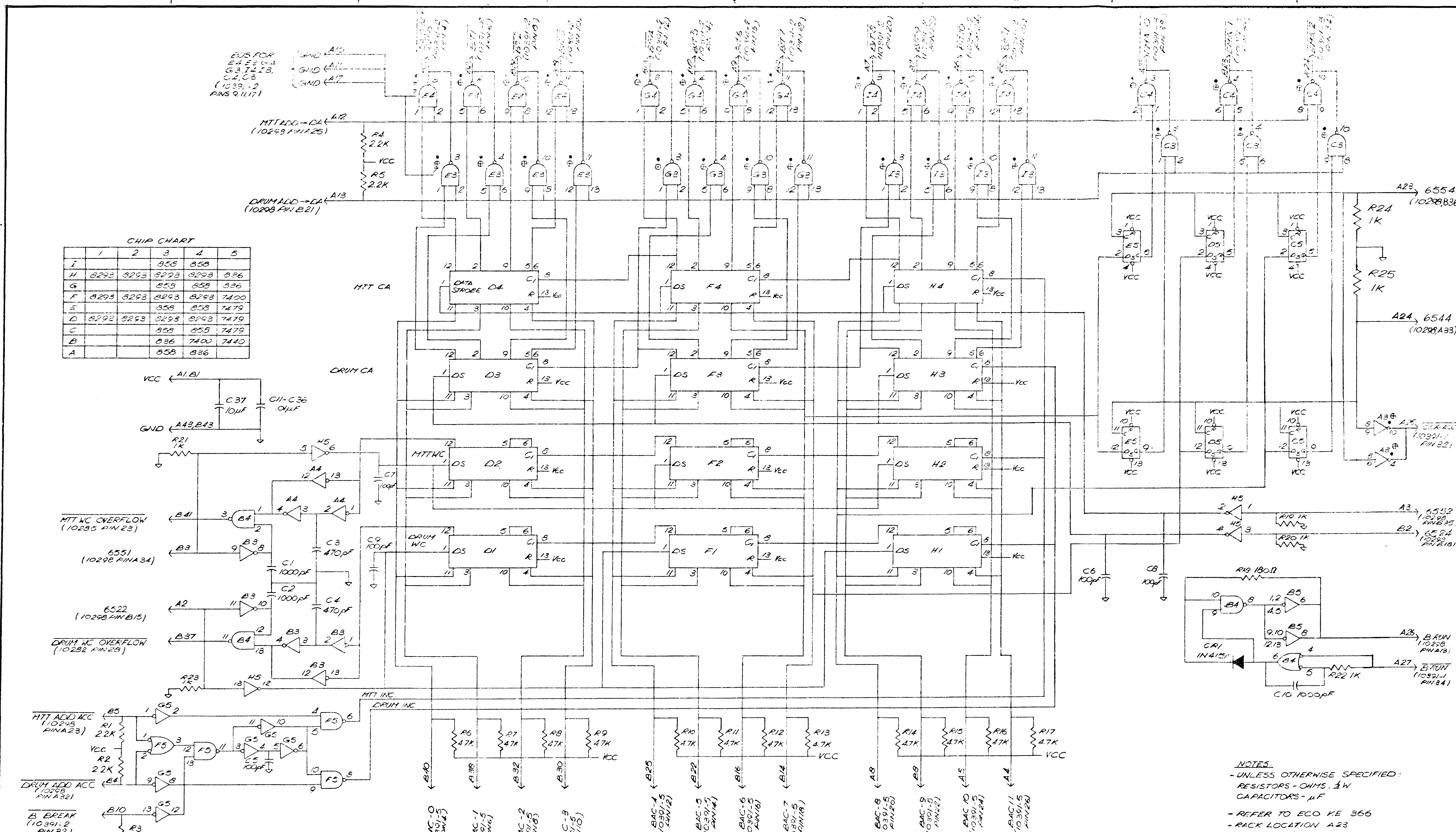
used on | drawn: Tomf
scale | date: 16 JULY 71 | design apprvl
unless specified: 00 = ±.01 fraction ± 1/64; 000 = ±.005 angles = ± 0 30' | checked | final apprvl: JSD
material | finish

CONSOLIDATED COMPUTER LIMITED OTTAWA

title: MTT READ CHECK 7-TRACK

sheet 1 of 1 | no. D10368 L | C rev

TRANSTEX 18 500-8-71



CHIP CHART

	1	2	3	4	5
I			856	858	
H	8293	8293	8293	8293	836
G			853	858	836
F	8293	8293	8293	8293	7400
E			856	858	7479
D	8293	8293	8293	8293	7479
C			858	855	7479
B			836	7400	7440
A			858	836	

NOTES:
- UNLESS OTHERWISE SPECIFIED:
  RESISTORS - OHMS, ¼W
  CAPACITORS - μF
- REFER TO ECO KE 366
- RACK LOCATION A23

eco	rev	description	date	by	chk	apprvd
KE 477	G	CORRECTION	6-10-72	DJ		
KE454	F	NO CHANGE	15-9-72	MN		
KE 438	E	REDRAWN (A3 ADDED)	28-8-72	MN	RAP	JWB

CONSOLIDATED COMPUTER LIMITED OTTAWA

date: 22 JUNE 1972 — drawn: MN — design apprvl: JWB — checked: RAP

unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0 30'

title: LOGIC WC & CA PCB

sheet 1 of 1 — no. B10442L G