Site Preparation

The customer will provide the furniture and proper operating environment for KEY-EDIT 50. Check the conditions noted in Table 1 and inform the customer about any problems. The site should be cleaned before delivery of the system.

Table 1

Temperature	15°C to 32°C	(59°F to 90°F)
Humidity	20% to 80%	relative humidity
Main AC	100 V ±10% 115 V ±10% 220 V ±10% 230 V ±10% 240 V ±10% 250 V ±10%	
Main AC Frequency		50 Hz +1%, -2% 60 Hz ± 1%

Cabinet Preparation

NOTE: Refer to the unpacking and installation procedures in the manufacturer's manual supplied with each peripheral.

1. Open all of the crates and check the contents against the KEY-EDIT system checklist.

2. Move the cabinets to the position shown in the Installation Plan. Place the cabinets as shown in SLB 11846 A.

3. Screw the levelling feet into the cabinet floors and bolt the cabinets together.

4. Install the AC Distribution Unit as shown in SLB 11846 A.
   CAUTION: This unit weights 100 lb (45.4 kg). It must be installed with two support rails underneath it.

5. Connect the external bus cables to the PDP/8-E processor. Refer to DEC PDP/8-E Small Computer Handbook (1971) page 10-17 for cable connections.

6. Install the processor on its slides as shown in SLB 11844 A.

7. Remove the logic rack faceplate and slide the rack out. Connect the external bus cables to the feedthrough pcbs (refer Figure 1).

8. Install the disc and disc power supply as shown in SLB 11845 A.

9. Release the disc read/write heads. Refer to 015 Disc Manual.

10. Install the magnetic tape transport (MTT) in the MTT cabinet. (Refer to the Cipher Model 100X Training Manual.)

11. Place the teletype as required and connect the ac and signal cables to the CPU. (Refer Figures 2 and 3.)

12. If a printer is included in the system, position it as required. Connect the ac cable to the AC Distribution Unit and the signal cable to the Line Printer Interface pcb. (Refer Figures 1, 2, 3, and SLB 11848 I.)

13. Place the Key-Data Terminals (KDT) as shown on the Installation Plan. Ensure that the ac power switch on the rear of each KDT is off and connect the ac mains. Some versions of KDTs have all of their controls on the operator faceplate. The ac switch on these is part of the volume control. Turn the control upward until the switch is heard. This ensures that the KDT is turned off.

14. Connect the signal cables to the connector on the back of each KDT and run the cables as required into the system. The normal entry of the system is through the floor of the CPU cabinet.

15. Connect the KDT cables to their respective VCU Terminal Control pcbs. (Refer to SLC 11722 A and SLB 11989 I.)

16. Install the VCU Terminal Control interconnect and insert the VCU DMA and VCU Terminal Control pcbs into rack B of the logic rack. (Refer SLB 11844 A.)

17. Connect the disc and MTT signal cables to their respective data pcbs as shown in Figures 1 and 3.

18. Slide the logic rack into the cabinet and replace the faceplate.

19. Install the ac cables as shown in Figure 2 and SLB 11848 I.

20. Connect the ground straps as shown in Figure 4. Each ground must be connected to bare metal by a star washer and bolt.

21. Ensure that the CPU power and ac circuit breakers on the distribution unit, disc, disc power supply, logic rack, and printer are turned off.

22. Ensure that the site ac mains are turned off.

23. Connect the ac mains to the AC Distribution Unit (refer Figure 2 and SLB 11848 I.
    CAUTION: The ac mains connection is:

Ground	(Earth)	Green/Yellow
Hot	(Line)	Brown
Neutral		Blue

24. Turn on the site ac mains.

25. Turn on the distribution unit breaker and depress the system ON switch. The fans in the upper rear of each cabinet should begin operating and the MTT should power up.

26. Turn on the logic rack regulator circuit breaker. Check that the voltage available at the regulator connector pin B33 is 5 V, ±0 V. (Refer to SLB 11806 W.)

27. Turn on the disc power supply ac circuit breaker. Check that the voltage available at the cable connector is correct.

28. Turn off the disc power supply and connect the dc cable to the disc. Then turn the disc and disc power supply circuit breakers on. The disc RDY lamp should light within two minutes.

29. Turn on the CPU power. Check the dc power supplies. Refer to the DEC PDP-8/E Maintenance Manual; Volume 1, Chapter 4. (DEC-8E-HR1B-D).

30. Using the Cipher Model 100X Training Manual, check the MTT mechanical and electrical adjustments.

31. Switch the TTY selector to LOCAL and check the printer operation by depressing all keys. Switch the TTY selector to LINE.

32. Turn on the printer ac circuit breaker and power it up.

33. Load the mini-loader given in the 100, 100 V, Phase 1 System Library and run the KEY-EDIT diagnostic. Leave the program running for at least an hour, preferably overnight.

34. Turn on all of the KDTs.

35. Ensure that all cables are clamped. Refer Figure 2 and SLB 11989 I.

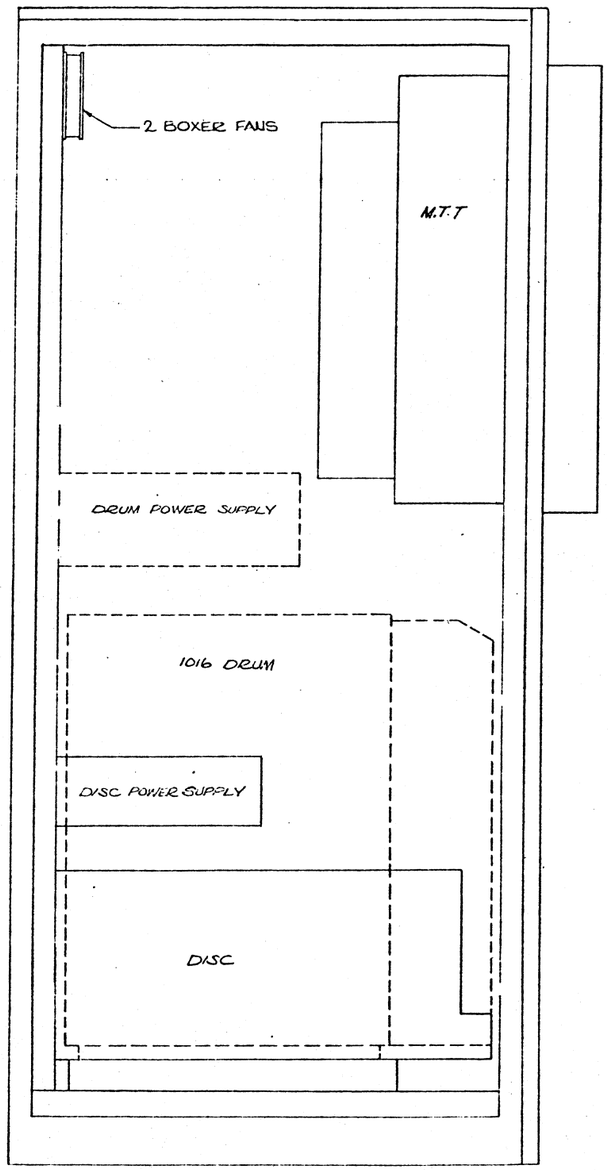
36. Perform a system cold-start as outlined in the KEY-EDIT 50 System Reference Manual.

37. Check the operation of each KDT and read a Peel tape onto the customer's EDP system.

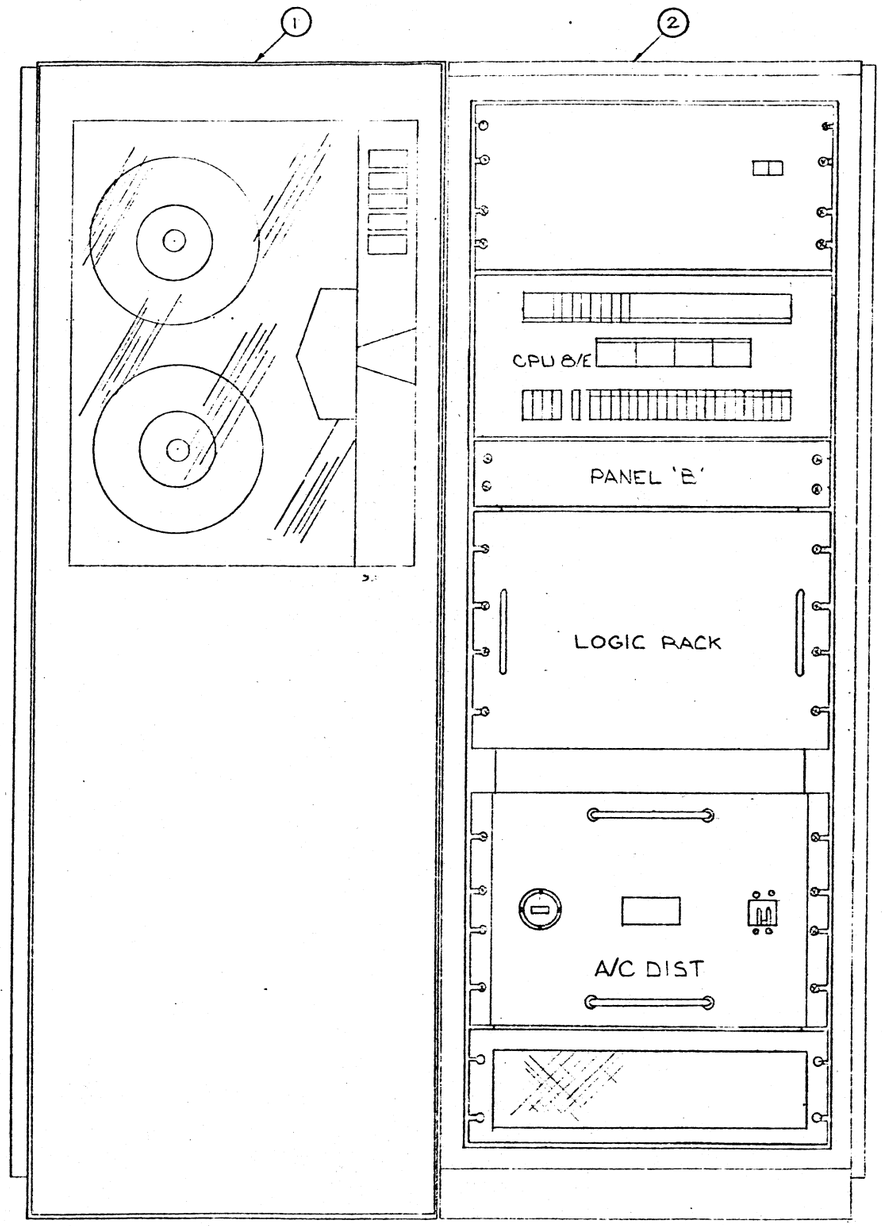
38. If the system is satisfactory, hang the doors and side panels and fit the vermin shields. (Refer Figure 5.)

39. Ensure that the system log and manual contain the system serial number.

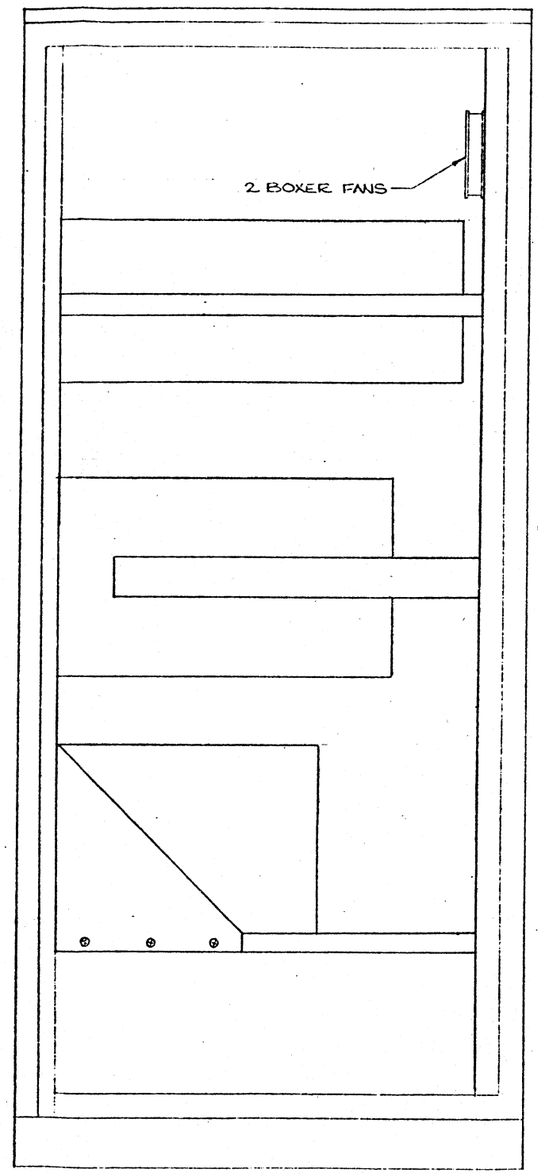
The system is ready for operation.



LEFT SIDE VIEW



FRONT VIEW



RIGHT SIDE VIEW

FOR P/L SEE SHT 2.

rev	eco	description	date	by	chk	approved
2	548	CABINET MODIFICATION	10 APR	DJ		
1		FOR P/L DEL				

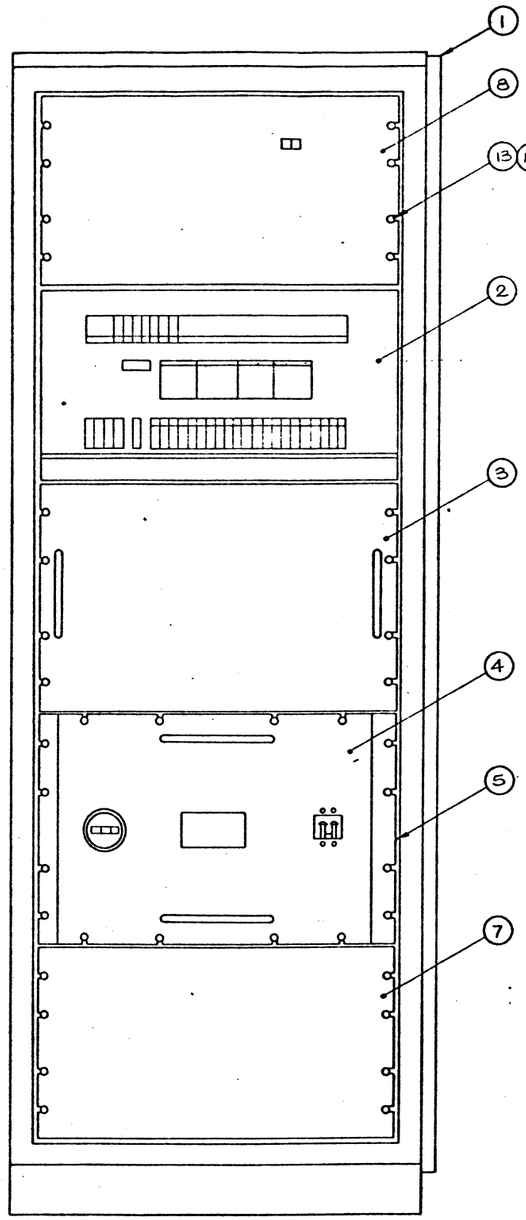
used on | drawn | scale | date | checked | final approval | material | finish

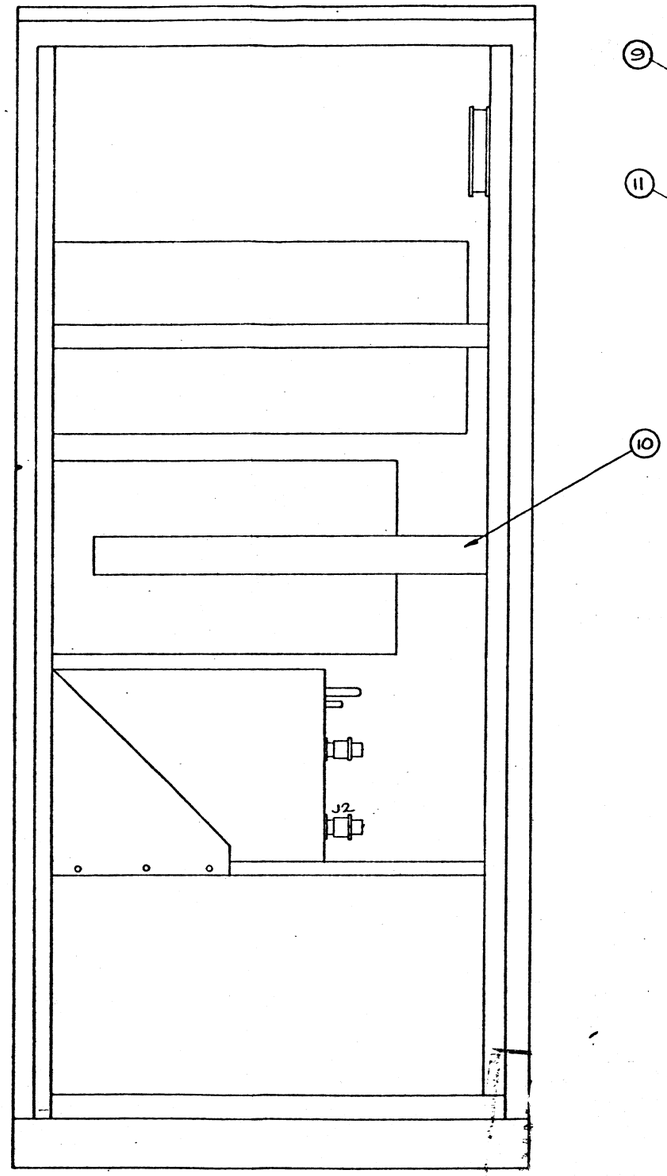
unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles ± 0 30'

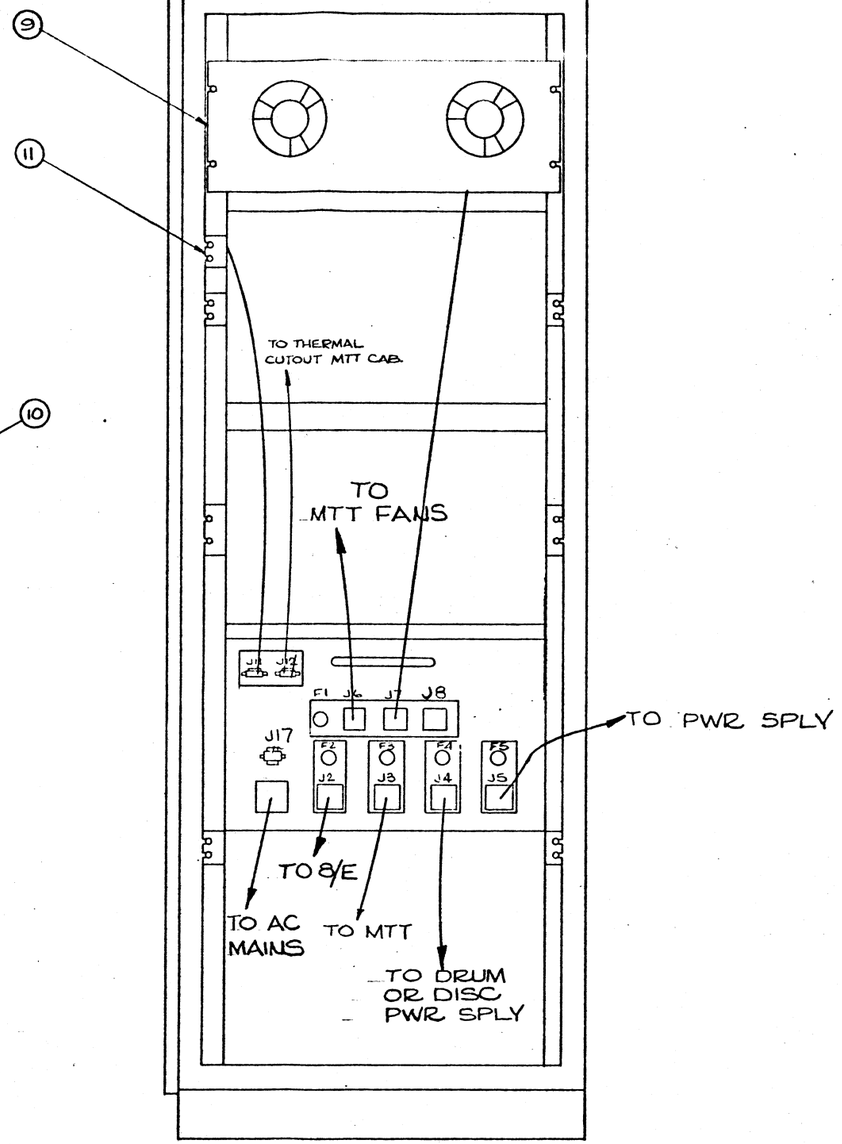
CONSOLIDATED COMPUTER INC. OTTAWA

title: CENTRAL CONTROL SECTION 117V SERIES L - PHASE 1

sheet 1 of 2 | no. SLB1184 rev 2







FOR P/L SEE SHTS 2 & 3

rev	eco	description	date	by	chk	approved
1		FOR PROD REL				

size C SLB11846A	drawn NJ
scale 1/4	date 15 DEC 72
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles ± 0 30'	design
	check
	final approval
material	finish

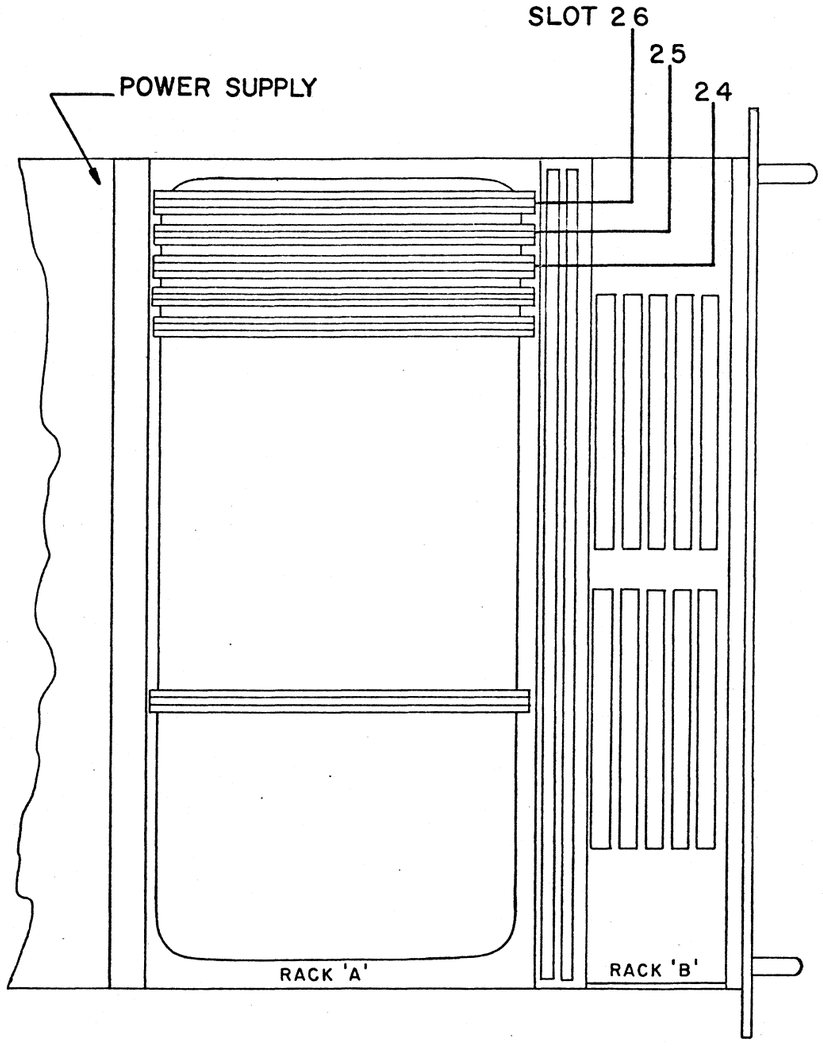
CONSOLIDATED COMPUTER INC. OTTAWA

FINAL ASSEMBLY
CPU CABINET
SERIES L - PHASE 1
117 VAC

title

sheet 1 of 3 | SLB11844A | 1 rev

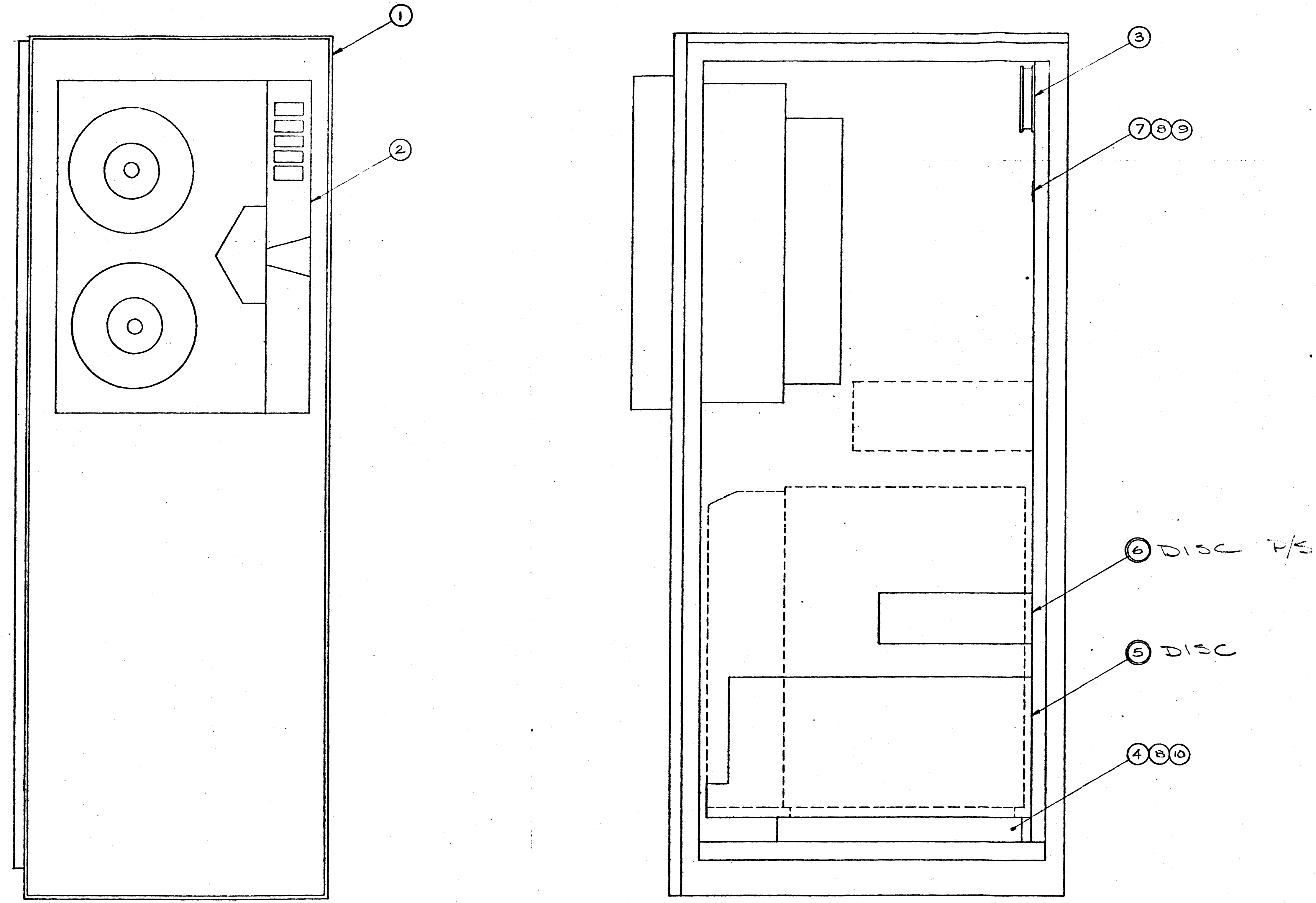
TRANSTEX 10 000-0-70



PCB	POSITION	RACK
POWER FAIL PROTECT	9	A
REAL TIME CLOCK	10	A
LINE PRINTER INTERFACE	12	A
FEEDTHRU (AC BUS)	14	A
FEEDTHRU (DB ADD)	15	A
FEEDTHRU (DB DATA)	16	A
FEEDTHRU (BMB BUS)	17	A
FEEDTHRU (BAC BUS)	18	A
MTT READ CHECK	19	A
MTT CONTROL	20	A
MTT DATA	21	A
DRUM MTT AND VCU MULTIPLEXOR	22	A
WC & CA	23	A
DISC CONTROL	24	A
DISC DATA	25	A
DERANDOMIZER	26	A
VCU DMA CONTROL	ANY	B
VCU TERMINAL CONTROL	ANY	B

LOGIC RACK PCB LOCATIONS

FIGURE 1.



FOR P/L SEE SHT 2

SLB11846A

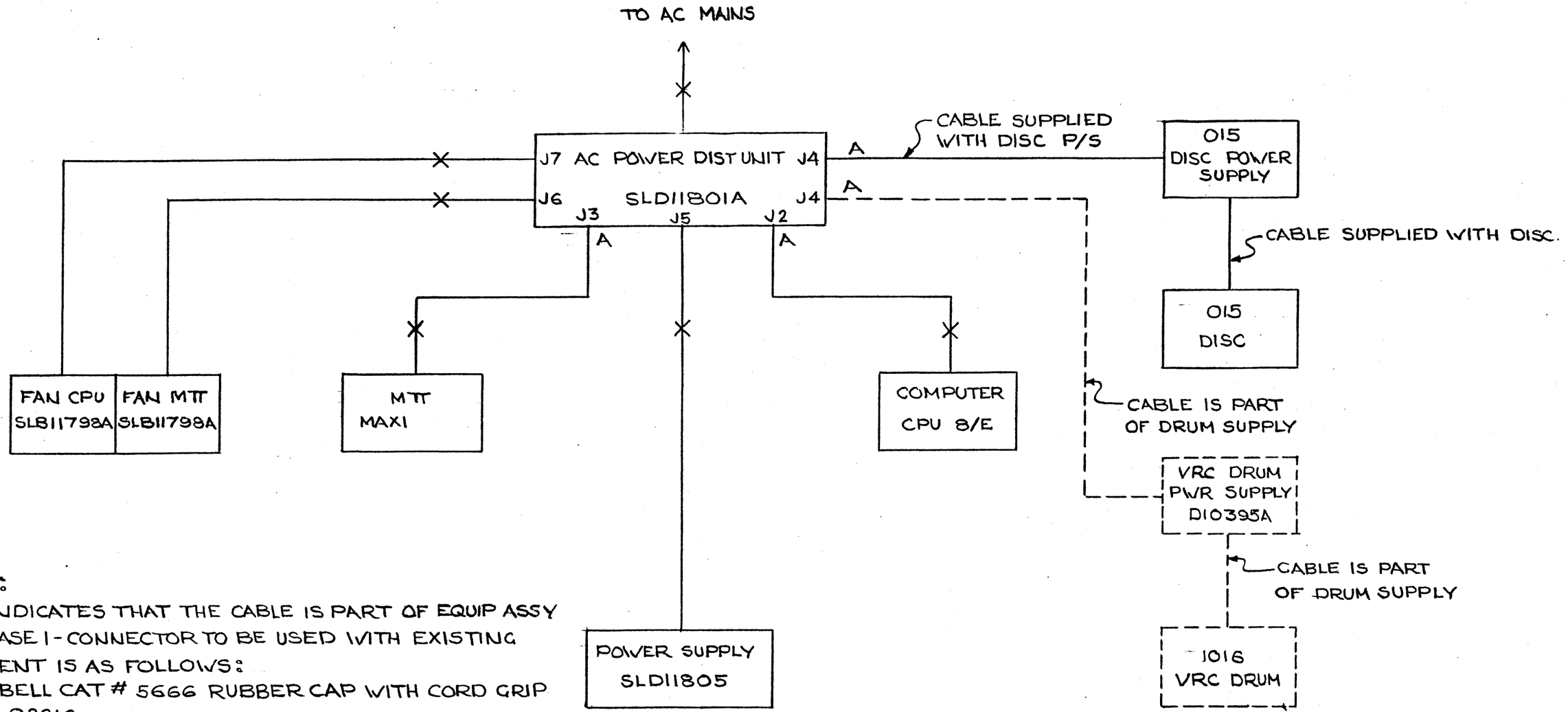
scale: 1/4 | date: DEC 72

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ±0 30

CONSOLIDATED COMPUTER INC.
OTTAWA

title: FINAL ASSEMBLY
MTT CABINET
SERIES L - PH 1
117VAC

sheet 1 of 2 no. SLB11845A rev 1



NOTES:

1 —X— INDICATES THAT THE CABLE IS PART OF EQUIP ASSY

2 FOR PHASE I - CONNECTOR TO BE USED WITH EXISTING EQUIPMENT IS AS FOLLOWS:
A - HUBBELL CAT # 5666 RUBBER CAP WITH CORD GRIP CCI No 92216

rev	eco	description	date	by	chk	apprvd
3	SL 149	CABLE LENGTHS DELETED	24 APR 73	GT		
2	SL 023	INFORMATION ADDED	18 APR 73	DJ		
1		PRE PROD REL	17 JAN 73			

used on: SERIES L PHASE I

scale | date: 12 JAN 73

unless specified
00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0 30'

drawn | design eng | checked | final apprvl

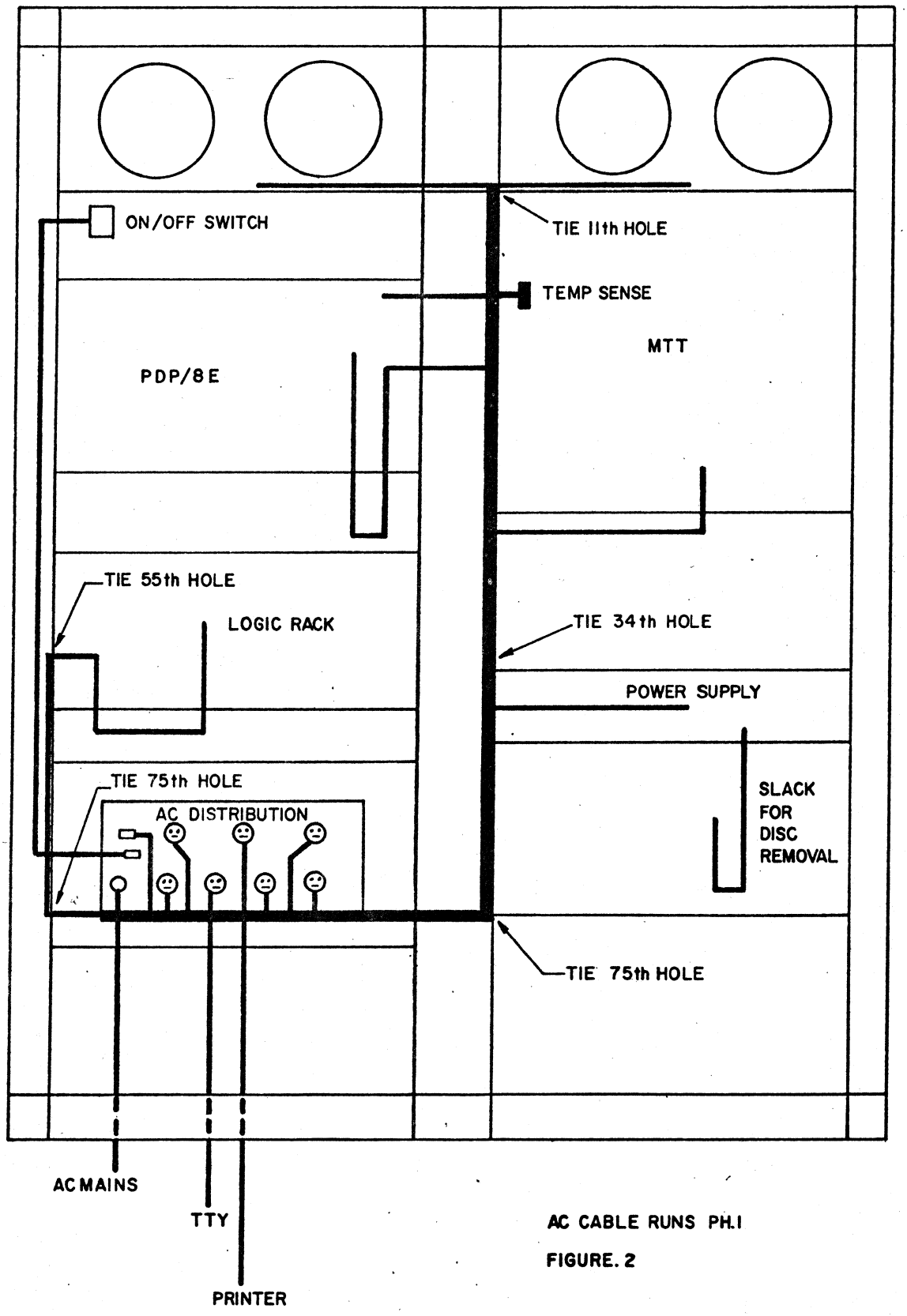
CONSOLIDATED COMPUTER INC. OTTAWA

material | finish

title: AC CABLES SERIES 50 PHASE I 220/240 V

sheet 1 of 1 | no. SLB11848 I | 3 rev

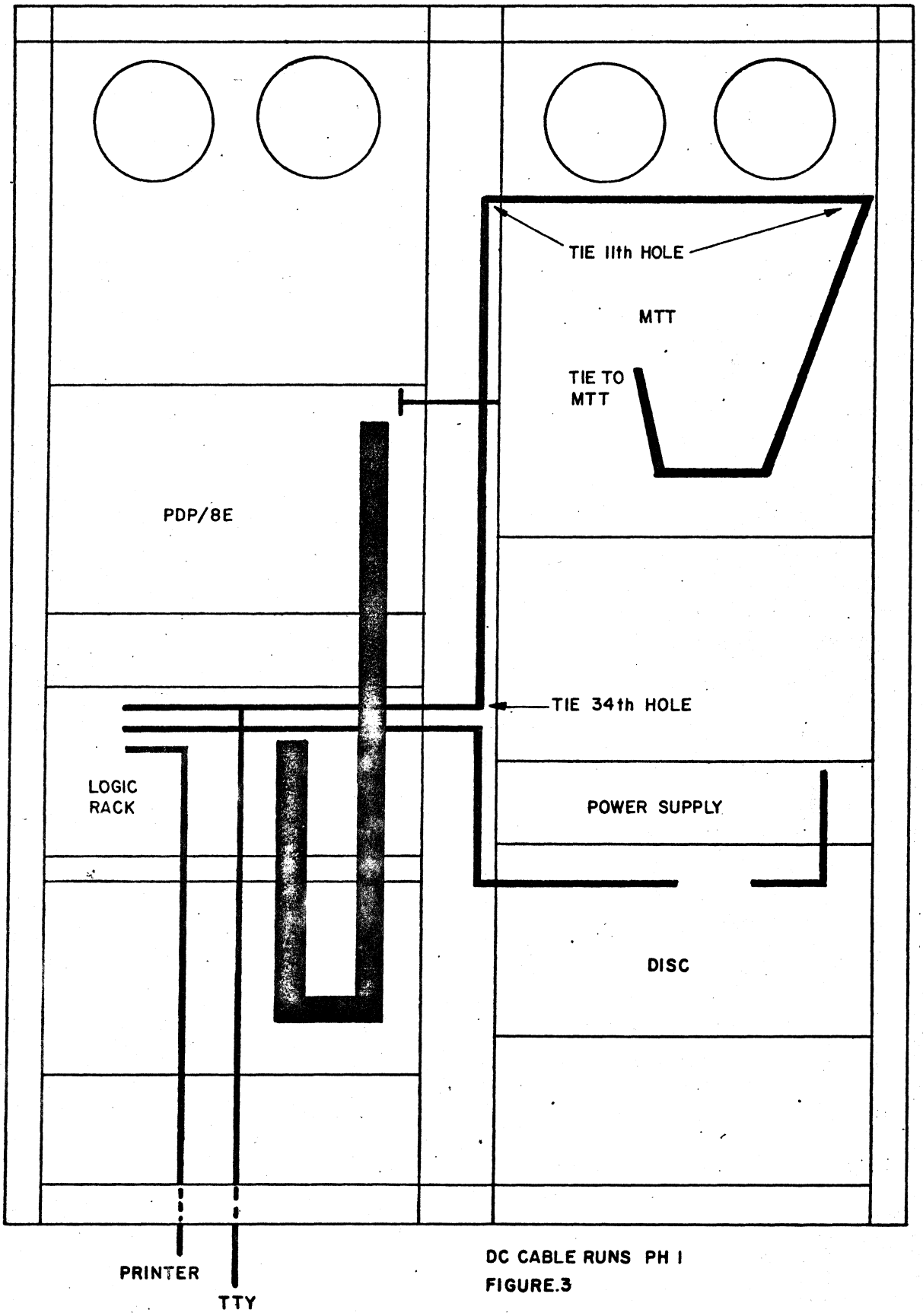
TRANSTEX 15 500-8-72



AC CABLE RUNS PH.I

FIGURE. 2

REAR VIEW



DC CABLE RUNS PH I
FIGURE.3

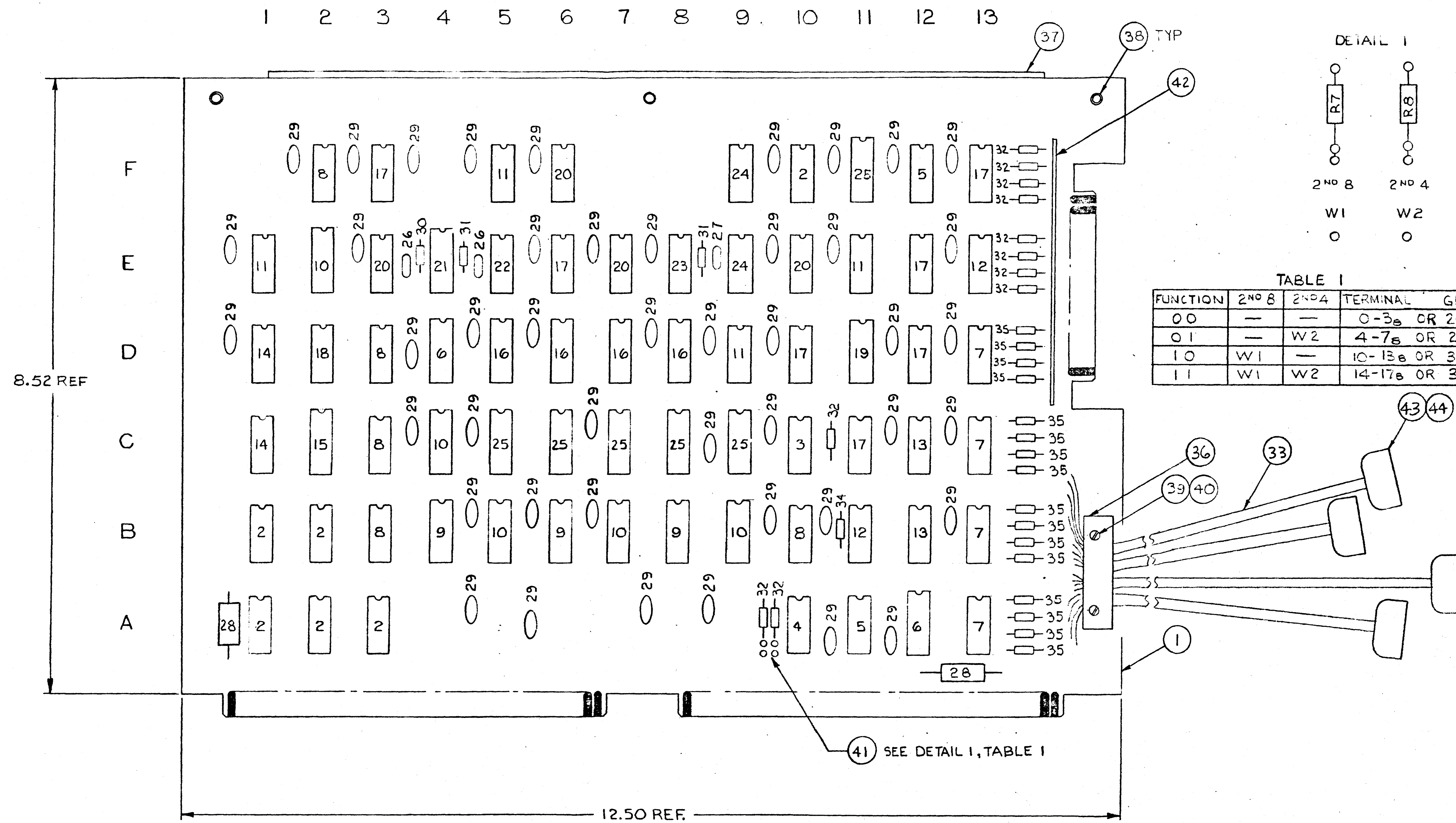


TABLE 1

FUNCTION	2ND 8	2ND 4	TERMINAL GROUP
00	—	—	$0\text{-}3_8$ OR $20\text{-}23_8$
01	—	W2	$4\text{-}7_8$ OR $24\text{-}27_8$
10	W1	—	$10\text{-}13_8$ OR $30\text{-}33_8$
11	W1	W2	$14\text{-}17_8$ OR $34\text{-}37_8$

NOTES: 1. RESISTORS R33 THRU R40 TO BE POSITIONED IN MOST SUITABLE LOCATION AT ASSEMBLY.

FOR PARTS LIST SEE SHEETS 2 AND 3

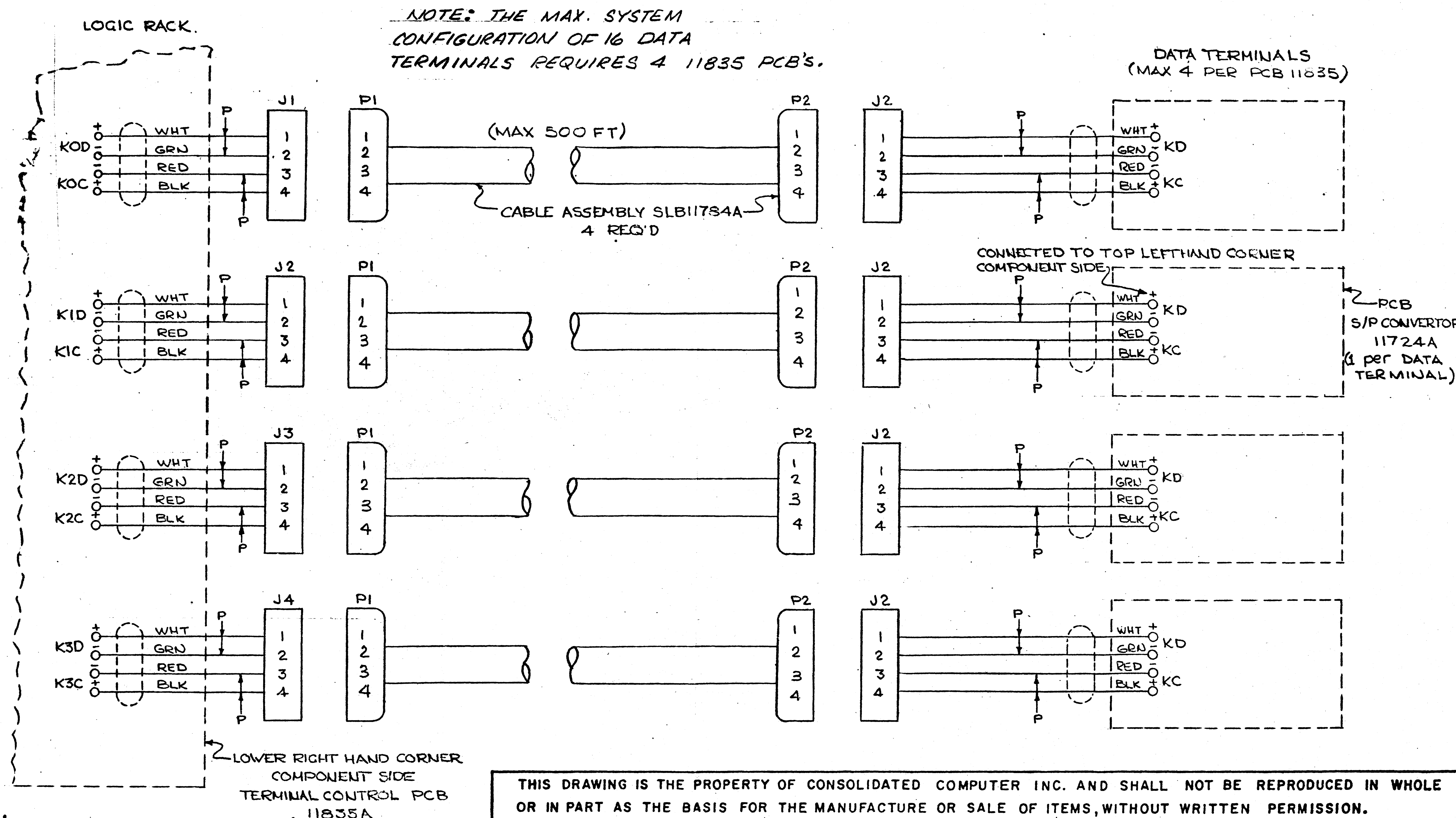
rev	eco	description	date	by	chk	apprvd
2	SL 384	TERM. GROUP COLUMN OF TABLE CHANGE	7 MAR 73			
1		PRE PRODUCTION				

used on: SLD11707A — drawn: DJ
scale: 1:1 — date: 15 DEC 72 — design eng: D WALSH
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0 30'
checked — final apprvl — material — finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: SERIES L-100V VCU TERMINAL CONTROL

sheet 1 of 3 — no. SLC11722A — rev 2

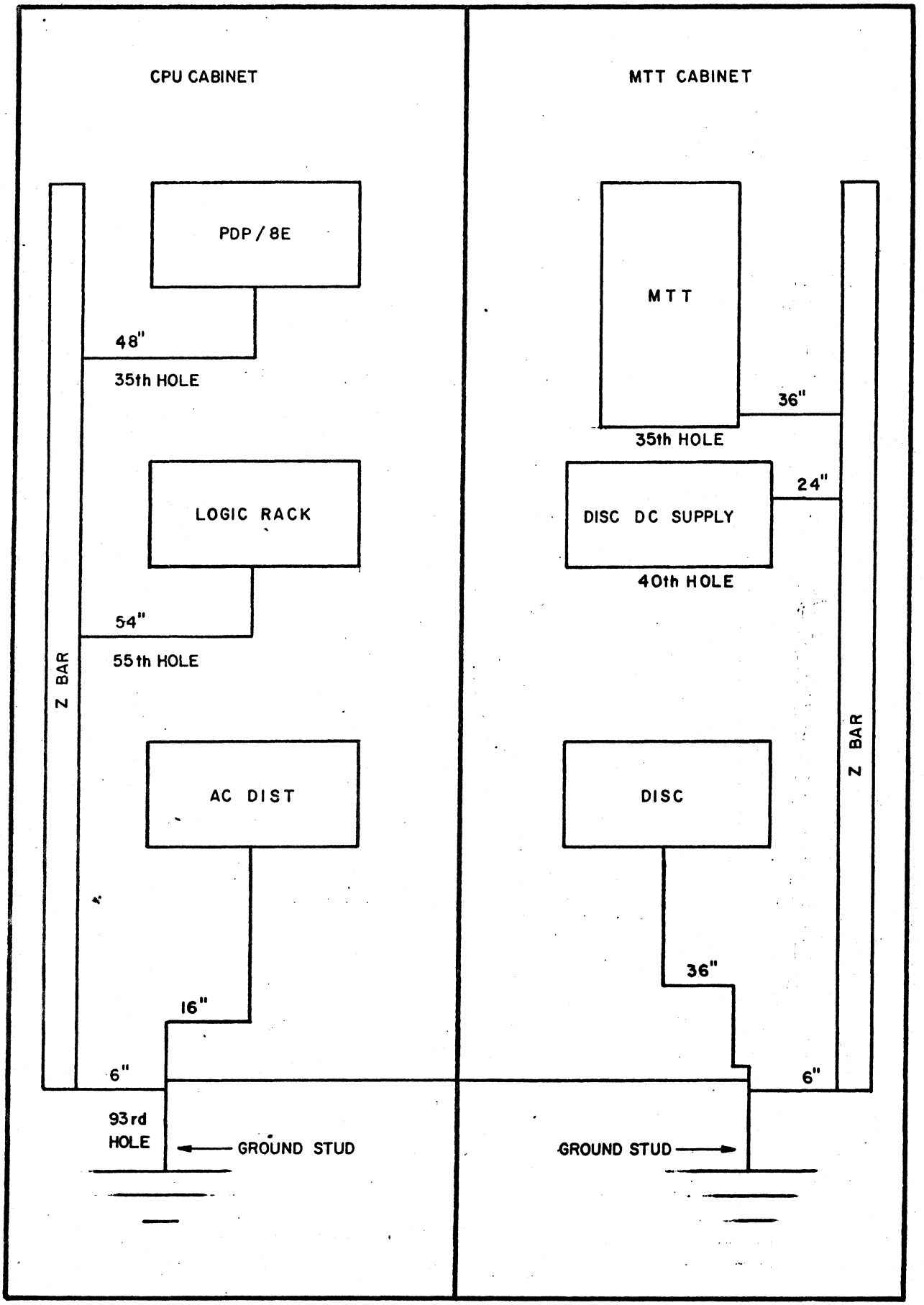


CONSOLIDATED COMPUTER INC. OTTAWA

used on	SERIES L PHASE I
scale	NTS
date	2 MAR 73
drawn	[signature]
design eng	D WALSH
checked	RL
final apprvl	
material	
finish	
title	CABLE INTERCONNECTIONS VCU TERMINAL CONTROL TO DATA TERMINAL SERIES L PHASE I
sheet	1 of 1
no.	SLB11989I
rev	1

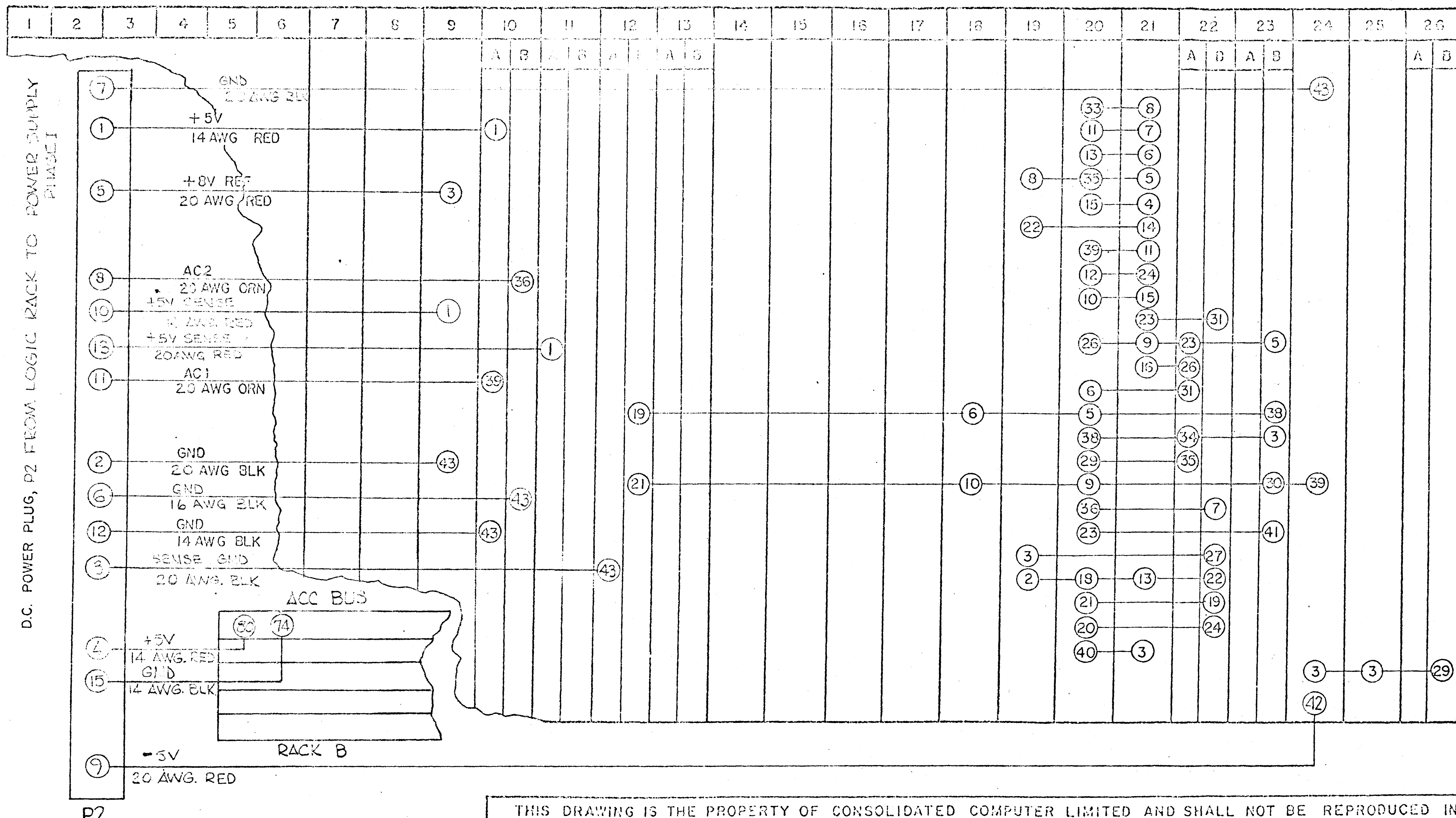
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0°30'

rev	eco	description	date	by	chk	apprvd
1	SL107	PRE PROD REL	15MAR73	VB	RL	DW



GROUND STRAP PH.I FIGURE 4

RACK A



rev	ecn	description	date	by	chk	apprvd
	SL 059	WIRES FROM P2 REVISED	12APR73	ΣL		
2	SL 058	P2-13 WAS P2-10. WIRE DESIG AC1 & AC2 INTERCHANGED	12 APR 73	ΣL		
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

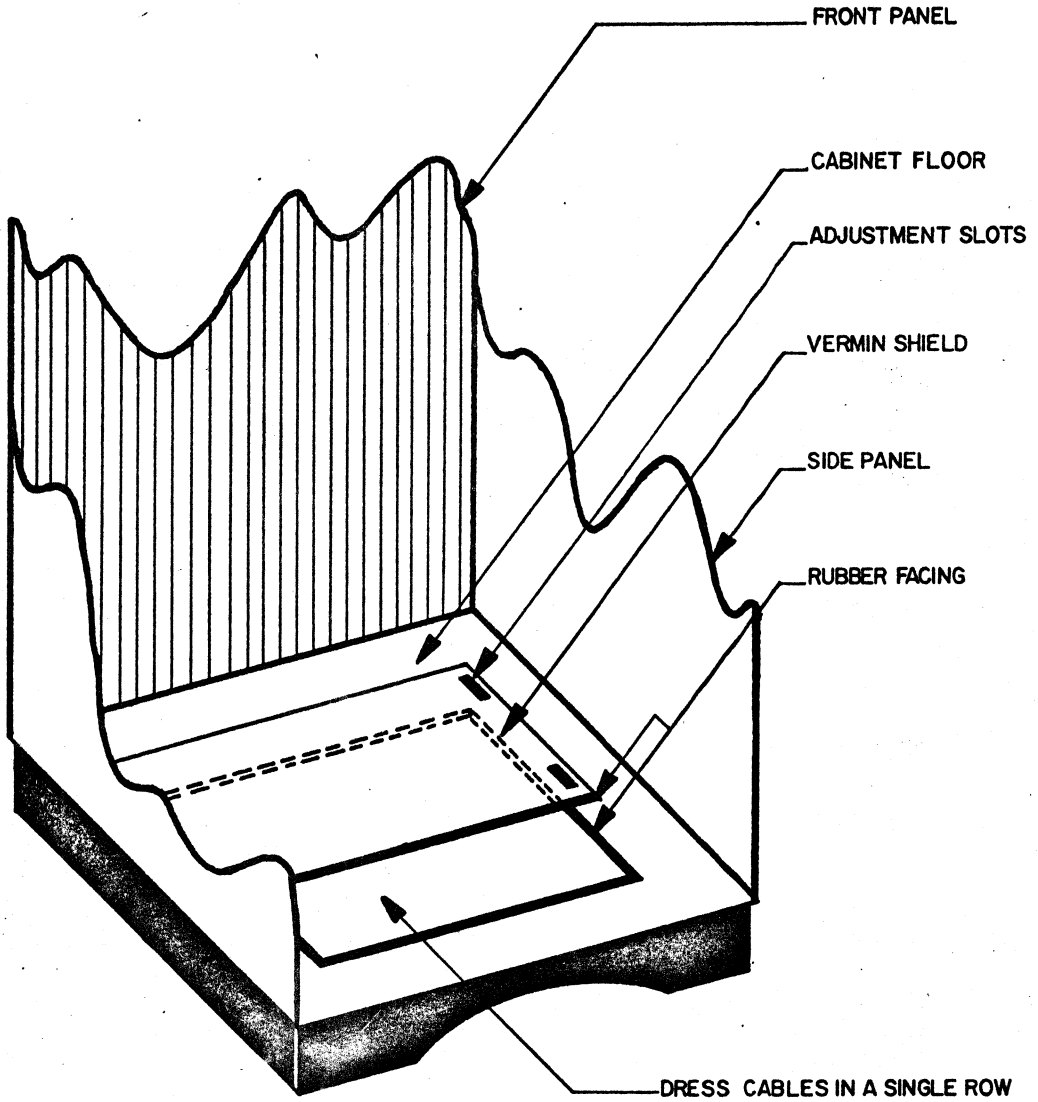
used on: SLD11806A & SLD11807A
drawn: R. Boyd
date: 3 JAN 73
design: ENG.

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

INC.
OTTAWA

title: BACK PLANE WIRING SERIES L-PHASE I LOGIC RACK

sheet 13 of 20 no. SLB11806W rev 5



VERMIN SHIELD

FIGURE 5

PRELIMINARY

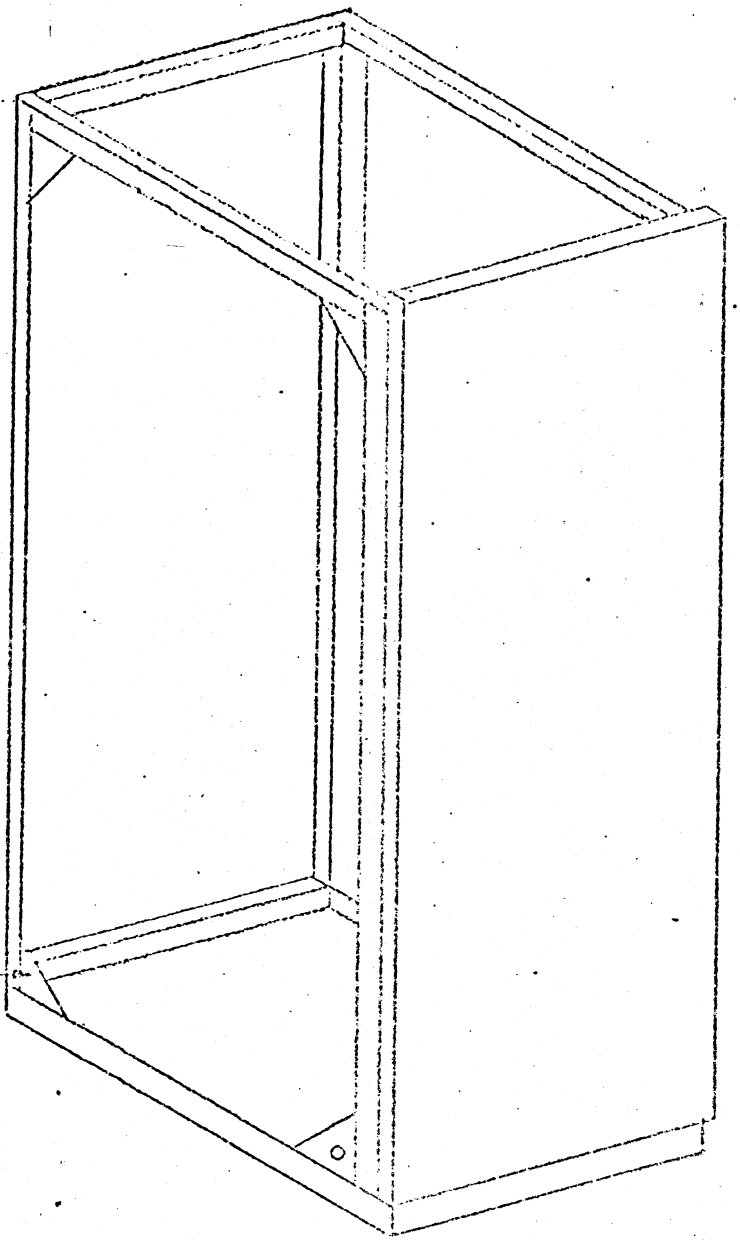


FIGURE 6

DESCRIPTION

The Power Fail Protect circuitry issues an interrupt to the CPU in the event of the temperature or supply voltage exceeding the specified limits, refer Figure 6-4-1.

Power Low

When the supply voltage is normal the Line Voltage Monitor provides 8 vdc to connector pin B3 of the Power Fail Protect pcb, 10185. The applied voltage varies directly with the line voltage.

The Zener diode, CR1, trip level of 4.3v is set by potentiometer R12 and is applied to the base of Q6. The transistor is normally on. Its collector is at ground level and holds Q7 off; therefore Q7 collector in normally high.

When the line voltage goes low CR1 ceases to conduct. Q6 base will go high and switch the transistor off. Its collector will go high (Vcc) to Q8 base. Q8 conducts, shorts R11, and alters the voltage divider ratio -- R11, R12, R13 -- to hold Q6 off until the line voltage rises about 2 volts above the detection trip level. This prevents alternate run and stop of the CPU if the supply voltage is marginal and fluctuating.

Q7 base goes high (when Q6 switches off) and its collector goes low to IOR gate IC2-12 pin 1. The high output from the gate is inverted to set R-S flip-flop IC3 at pin 9. IC3 output goes high, is inverted, and applied as an interrupt signal to the CPU via connector pin A42. The R-S flop is reset to $\overline{\text{B Run}}$ when the CPU stops.

IC3-8 is also inverted by IC4-4 and applied to NAND gate IC4-13 with IOT 6404, derived from the CPU via connector pin A38. The gate output is a $\overline{\text{Skip}}$ pulse that facilitates the status check of the Power Fail Protect circuit.

Power High

The Power High circuitry is basically the same as the Power Low but Q10 is normally on and its collector low.

If the power goes low Q9 switches on and Q10 switches off. The collector high level is inverted and initiates an interrupt to the CPU.

Temperature High

The Temperature High control is basically a bridge circuit. Two bridge arms contain thermistors (R29, R30); one contains a fixed resistor and the other a potentiometer (R5) for balance adjustment.

The bridge output is applied to a differential amplifier, Q1, Q2. When the operating temperature is normal Q1 is on, Q2 is off, and a high level is present at the base of Q3 (PNP).

Should the temperature rise the resistance of the thermistors will decrease until the bridge is unbalanced. Q1 will switch off, Q2 will switch on and apply a low voltage to Q3 base. Q3 will switch on and apply a high voltage to Q4 base; Q4 collector will then go low to initiate an interrupt via IC2-12 pin 2.

CALIBRATION

Refer Figure

1 Power Low.

1. Connect the monitor to a variable voltage ac power source (Variac).
2. Adjust the variable supply:

   117v systems, adjust to 105v
   220v systems, adjust to 198v
   240v systems, adjust to 216v

3. Connect a high impedance voltmeter (or oscilloscope) to the Power Low test point, connector pin 7.
4. Adjust the power low potentiometer, R12, clockwise until the meter indicates a 5v high level.
5. Adjust counterclockwise until the circuit trips and the meter indicates a low level.

2 Power High.

1. Connect the monitor to a variable voltage ac power source (Variac).
2. Adjust the variable supply:

   117v systems, adjust to 129v
   220v systems, adjust to 242v
   240v systems, adjust to 264v

3. Connect a high impedance voltmeter (or oscilloscope) to the Power High test point, connector pin 9.
4. Adjust the power high potentiometer, R22, counterclockwise until the meter indicates a 0v low level.
5. Adjust clockwise until the circuit trips and the meter indicates a high level.
6. Lower the variable supply voltage and check that the meter indicates a low level (0v).

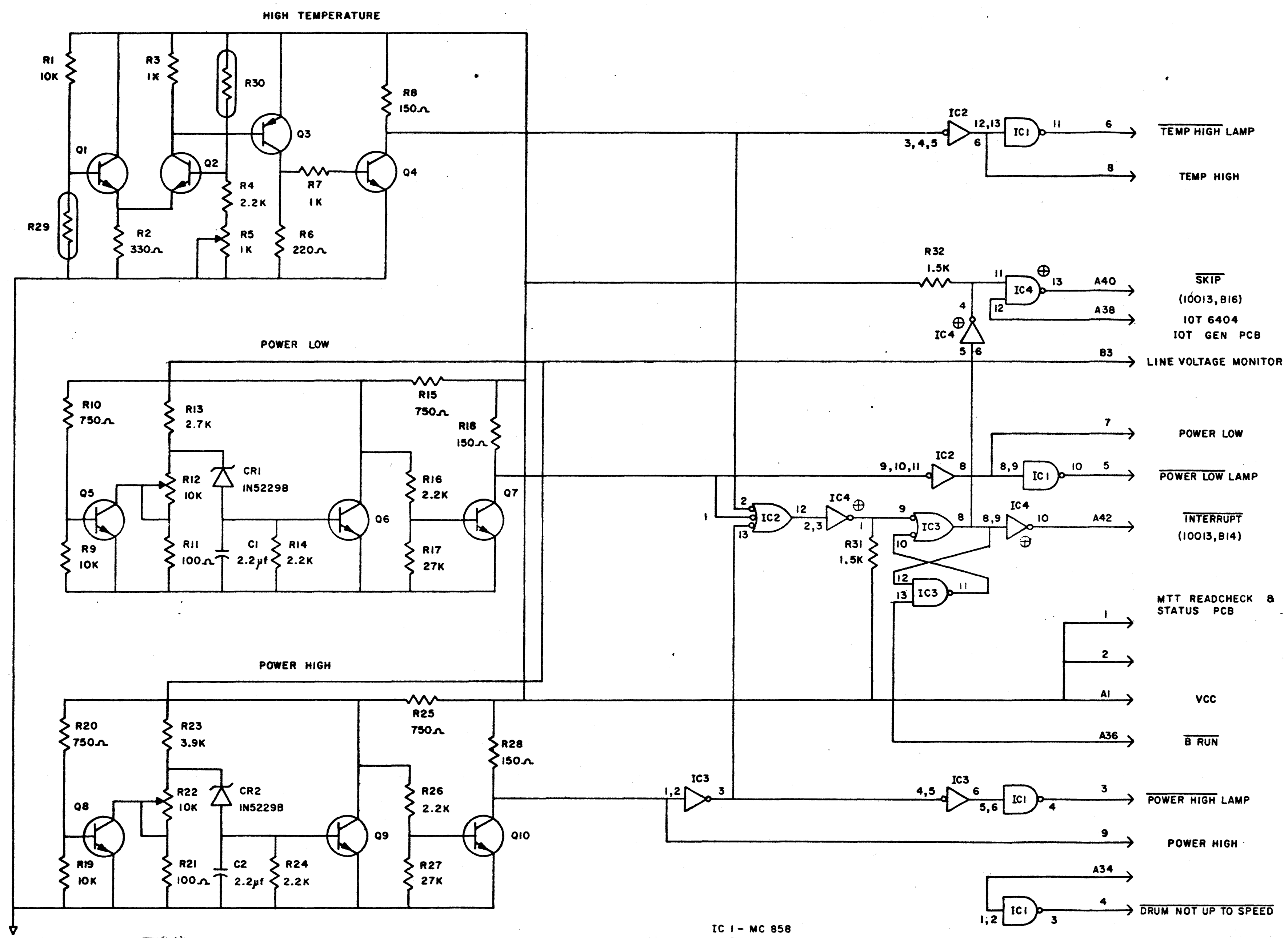
3 Temperature.

1. Connect a high impedance voltmeter to the temperature high test point, connector pin 8.
2. Raise the temperature of the thermistors to approximately 100F (39.5C). (Hold between thumb and forefinger).

CAUTION: Thermistors are brittle and will break easily.

3. Adjust the temperature high potentiometer, R5, until the meter indicates a 0v low level.
4. Check that the meter indicates a high level (5v) when the thermistors cool.

NOTE: The temperature detection circuit can only be adjusted accurately in a controlled environment, such as a heat chamber.



IC 1 - MC 858
IC 2 - MC 7410
IC 3 - MC 846
IC 4 - MC 7401
⊕ OPEN COLLECTOR

NOTE: ALL TRANSISTORS ARE MPS 3704
EXCEPT Q3, WHICH IS MPS 3702

FIGURE 6-4-1

RACK LOCATION A6

rev	eco	description	date	by	chk	approved
D	KE 444	ECO INCORP, REDRAWN	6 OCT 72	MJ		PEW
C	KE 191	REDRAWN WITHOUT REV				

date: 6 DEC 71

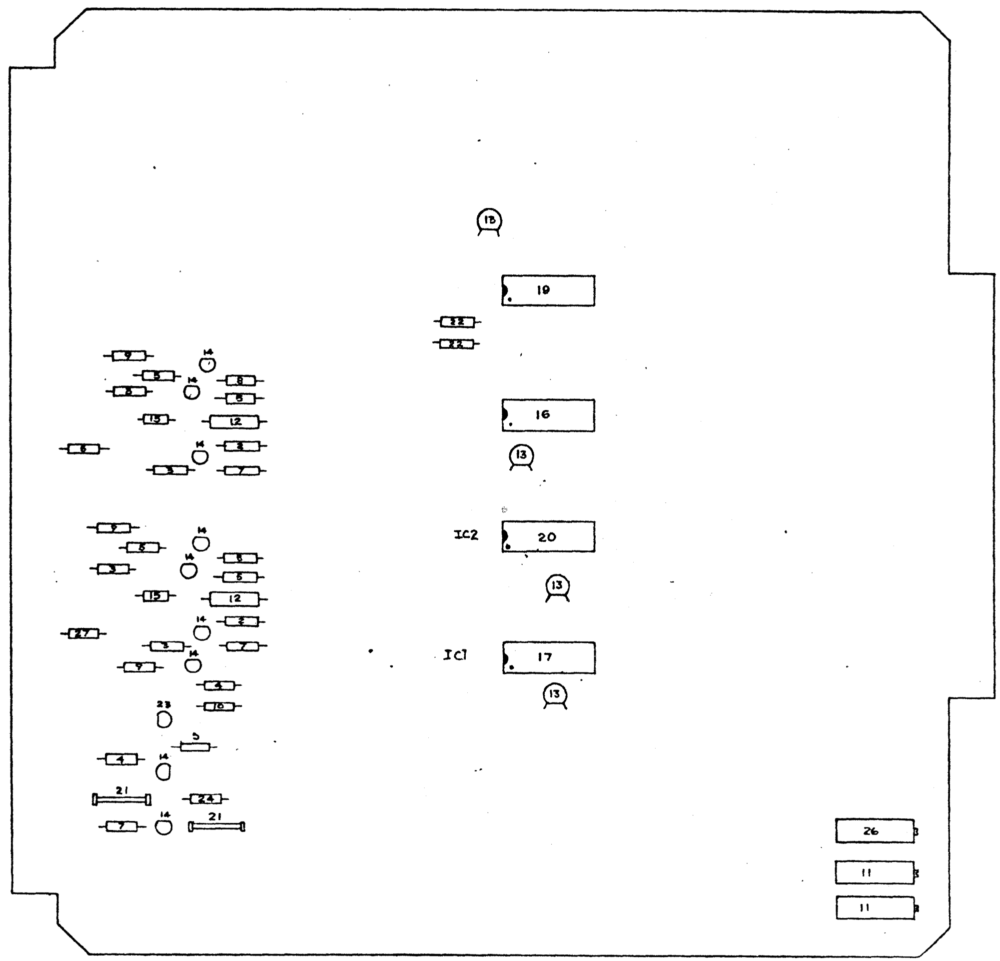
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

checked: JSO

CONSOLIDATED COMPUTER LIMITED
OTTAWA

POWER FAIL PROTECT
SCHEMATIC

sheet 1 of 1 no. D 10185 S



ECO KE 176
ECO KE 163
KE 148

C	RELEASED PER ECN KE 191	30 APR 71	J.F.F.
B3	PARTS LIST ONLY		P.M.
B2	ITEM 27 WAS ITEM 6		P.M.
B1	ITEM 5 WAS ITEM 2		P.B.
B	ITEM 22 WAS ITEM 11		
A	DRAWN		R.C.

D10152A — used on
unless specified: fractions ±1/64, .00 ± .01, .000 ± .005
drawn: R.C.

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

POWER FAIL PROTECT

D10153A

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R. CHARLEBOIS | DATE: 1970 8 APRIL | APPROVED BY:

TITLE: POWER FAIL PROTECT

SERIAL NO.

USED ON ASSEMBLY: D10152A | DRAWING REV. C

DATE ISSUED

ASSEMBLY NO. D10185A | SHT 1 OF 2

PRODUC

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO
1	10185P	B	1	P.C.B.		KE 147 - B
2	90480-39		2	RESISTOR 100Ω 1/4W	R11, R21.	KE 148 - B
3	90480-60		4	RESISTOR 750Ω 1/4W	R10, R15, R20, R25,	KE 163
4	90480-63		2	RESISTOR 1K 1/4W	R3, R7	KE 176
B1 5	90480-71		5	RESISTOR 2.2K 1/4W	R4, R14, R16, R24 R26	KE 191 (
6	90480-77		1	RESISTOR 3.9K 1/4W	, R23	
7	90480-87		3	RESISTOR 10K 1/4W	R1, R9, R19	
8	90480-97		2	RESISTOR 27K 1/4W	R17, R27	
9	90480-43		3	RESISTOR 150Ω 1/4W	R8, R18, R28.	
10	90480-47		1	RESISTOR 220Ω 1/4W	R6	
B2 11	90485		2	RESISTOR VARIABLE 10K DALE 2187	R12, R22	
B3 OR 11	91478		2	RESISTOR VARIABLE 10K BECKMAN	R12, R22	
12	90000		2	CAPACITOR 2.2 μF	C1, C2	
13	90119		4	CAPACITOR 0.01μF 50V	C	
C 14	90597		9	TRANSISTOR MPS 3704	Q1 TO Q10 (MOTOROLA)	
15	90216		2	DIODE IN5229B	CR1, CR2.	
16	90341		1	I.C. MC 84C P	IC3	
17	90323		1	I.C. MC 858 P	IC1	
19	90332		1	I.C. MC 7401	IC4	
20	90333		1	I.C. MC 7410	IC2	

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R.CHARLEBOIS | DATE: 1970 8 APRIL | APPROVED BY:

TITLE: POWER FAIL PROTECT

SERIAL NO.

USED ON ASSEMBLY: D10152A | DRAWING REV. "C

DATE ISSUED

ASSEMBLY NO. D10185A | SHT 2 OF 2

PRODL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O.N
21	90562		2	THERMISTOR 10K QB41J1	R29, R30,	
22	90480-67		2	RESISTOR 1.5K 1/4W	R31, R32	
23	90598		1	TRANSISTOR MPS 3702	Q3	
24	90480-51		1	RESISTOR 330Ω	R2	
B 25	-		"			
B1 26	90484		1	RESISTOR, VARIABLE 1K DALE 2187	R5	
27	90480-73		1	RESISTOR 2.7K 1/4 W	R13	
REF	C10185S			SCHEMATIC		

Feedthrough pcb B20 — 1. BMB TEST

```
Starting Address  2000   7604
                         3020
                         1020
                         5200
```

Monitor each BMB bit. There should be a pattern change as the corresponding Switch Register bit is changed.

Feedthrough pcb B21 — 2. BAC TEST

```
Starting Address  4000   7604
                         7000
                         7000
                         7200
                         7000
                         7000
                         5200
```

Monitor each BAC line. There should be a square wave as the corresponding Switch Register is set to a one.

Feedthrough pcb B21 — 3. IOP TEST

```
Starting Address  1000   6447
                         5200
```

Sync off IOP 1

Monitor IOP 1 at pin 28.
IOP 2 at pin 30.
IOP 4 at pin 32.

4. KEYSTATION

4.1 BASIC CHECKOUT ROUTINES

4.1.1 Read keyboard data into accumulator.

Toggle in on any page:

```
6401        SKIP NO KBD FLAG
5203        JMP +2
5200        JMP -2
6426        CLEAR AC, READ DATA, CLEAR FLAG
7000/7402   NOP/HLT
5200        JMP RESTART
```

4.1.2 Strobe data to keystation display.

Toggle in on any page:

```
7604        LAS    DISPLAY CODE
 641        SELECT ADDRESS
1206        TAD ADDRESS
6421        STROBE DATA
7000/7402   NOP/HLT
5200        JMP RESTART
7777
```

4.2 KEYSTATION IOT GENERATOR AND INTERRUPT CONTROL, pcb 10295

4.2.1 Use IOT and Clear Accumulator Test program listed in the Drum and MTT IOT Generator test, 4.1, to test the IOT pulses. The following IOTs should clear the accumulator:

6402
6411
6412
6414
6422

4.2.2 Keyboard Address Test:

Starting Address	7000	7200
		6402
		6402
		6402
		6402
		7100
		6401
		7120
		5200

Ground each keyboard priority flag input: the binary number of that keyboard should appear in the accumulator.
A correct skip is indicated by the link being reset when any of the keyboard priority inputs are grounded.

4.3 KEYSTATION OUTPUT CONTROL, pcb 11075

4.3.1

Starting Address	4000	7604
		6411
		6412
		6414
		5200

Monitor a square wave at each of the two output pins for each accumulator bit when the corresponding Switch Register bit is set to a one.
Also try setting each bit to a zero when all other bits are set to a one.
Observe the outputs from each of the three Select Function R-S flops. Each flop is set by one IOT and reset by the other two.

4.3.2 Keyboard Enable:

Starting Address	6000	7604
		6421
		7000
		5200

To test the first set of eight keyboards Switch Register bit 3 must be a one. For the second set of eight keyboards bit 2 must be a one. For the third set of eight keyboards bit 1 must be a one. For the fourth set of eight keyboards bit 0 must be a one.
Each of the eight keyboards corresponds to bits 4 to 11 of the Switch Register. A 4 microsecond pulse should be seen at the selected output.

4.4 INPUT AND PRIORITY RUNDOWN, pcb 10295

4.4.1 Read keyboard data into accumulator.

Starting Address 6000 6422
7000
5200

As each key on the keyboard is depressed its output code should appear in the accumulator.

4.4.2 Strobe data to keystation display.

Starting Address 7000 7604
6411
1206
6421
7000
5200
7777

Change location 7001 to 6411 to output data to keystation buffer A.

Change location 7001 to 6412 to output data to keystation buffer B.

Change location 7001 to 6414 to output data to keystation buffer C.

As the input codes are selected from the Switch Register the correct data should be displayed on the keyboard.

5. DRUM AND MTT IOT GENERATOR, pcb 10298

5.1 IOT and Clear Accumulator Test

Starting Address 6000 7604
3203
7240
7000
7000
7000
5200

Start program at 6000. Set up each IOT in the Switch Register and monitor the IOT pulses. The following IOTs should clear the accumulator:

6502	6541
6504	6542
6512	6551
6522	6552
6524	

5.2 Multiplexor Test

A Drum or MTT break request can be simulated by grounding the Drum Break request line (pin A16) or the MTT Break request line (pin B7).
Start the following program and then monitor the multiplexor signals:

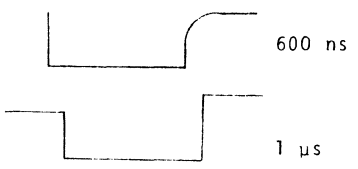
Starting Address 1000 7000
5200

5.2.1 Drum Break Request:

Ground pin A16 and monitor the following signals.

Trigger on Address Accepted, pin A21

MB Out to Drum Data, pin B33



Drum Data to MB In, pin A36 low

Drum Address Accepted, pin A32  600 ns

Drum Address to DA, pin B21 high

MTT Data to MB In, pin A26 low
MTT Address Accepted, pin A23 high
MB Out to MTT Data, pin B31 low

5.2.2 Magnetic Tape Break Request.

Remove ground from pin A16.
Ground pin B7.

Monitor the following signals:

Trigger on Address Accepted, pin A21  600 ns

MB Out to MTT Data, pin B31 

MTT Data to MB In, pin A26 low

MTT Address Accepted, pin A23  600 ns

MTT Address to DA, pin A25 high

Drum Data to MB In, pin A36 low
Drum Address Accepted, pin A32 high
MB Out to Drum Data, pin B33 high

5.2.3 Software Flag

Program	6462	6462
	6464	6464
	6461	6461
	JMP Program	5200
	HLT	7402

a. Remove all jumpers for the previous test.
b. Load address and start the above program.

This program halts if the software flag will not set. A square wave should be monitored at pin A9.

6. WORD COUNT AND CURRENT ADDRESS, pcb 10442

5.1

7000	7604
	6522
	7604
	6524
	7604
	6551
	7604
	6552
	6526
	6553
	5200

Monitor the output of each flip-flop for a square wave when the corresponding Switch Register bit is set to a one. All four flops for a particular bit should be toggling.

6.2 Increment Test:

```
6000   6554
       7000
       7000
       5200
```

Ground B Break line at pin B10.
Jumper IOT 6554, pin A23, to Drum Adrs Acptd, pin B4, to test drum word count and current address flip-flops. Then Jumper IOT 6554, pin A23, to MTT Adrs Acptd, pin B5, to test MTT word count and current address flip-flops.

Monitor the output of each flip-flop to see that it divides by 2 the previous flip-flop's output.

6.3 Extended Memory Address Test:

```
2000   7604
       6554
       7604
       6544
       5200
```

Monitor the Q output of the extended memory address flip-flops. As Switch Register bits 6, 7, and 8 are set to a one the corresponding flip-flop should also set.

7.1

```
2000    7300
   1    6501
   2    1221                                  TAD WC
   3    6522
   4    1224                                  TAD IF
   5    6544
   6    1222                                  TAD CA
   7    6524
  10    1223                                  TAD SECTOR
  11    6502
  12    7604                                  LOAD R/W & TRACK
  13    6504
  14    6511                        (1225)    TAD TIME
  15    5200   USE IF FLAG          (3226)    DCA WAIT
  16    5214   IS NOT WORKING       (2226)    ISZ WAIT
  17    7402                        (5216)
  20    7402                        (5200)
  21    7770                                  WC
  22    3000                                  CA
  23    0000                                  SECTOR
  24    0000                                  IF
  25    4000                                  TIME
2026    4000                                  WAIT
```

7.2 PROCEDURE

Load program into IF & DF 0. To use the program in another field location 2024 must be changed using bits 6, 7, and 8, to give octal address of the field the program is to run in.

1. Load data pattern into locations 3000 to 3007
2. Load address 2000
3. Set bit 0 to a one for write
4. Clear and continue
5. Halt
6. Clear contents of locations 3000 to 3007
7. Load address 2000
8. Set bit 0 to a zero for read
9. Clear and continue
10. Halt
11. Observe data pattern in locations 3000 to 3007

8.1

```
4000    1232                    TAD COUNT
   1    3231                    DCA WAIT 2
   2    7300
   3    1226                    TAD FIELD
   4    6554
   5    1225                    TAD TAPE
   6    6521
   7    7300
  10    6532
  11    1224                    TAD CA
  12    6552
  13    7604
  14    6542
  15    1227                    TAD WC
  16    6551
  17    6531    USE IF      2230    WAIT 1
  20    5200    FLAG NOT    5217
  21    5217    WORKING     2231    WAIT 2
  22    5217
  23    5200
  24    6000                    CA
  25      10                    TAPE
  26    0000                    FIELD
  27    7770                    WC
  30    0000                    WAIT 1
  31    7770                    WAIT 2
  32    7770                    COUNT
```

8.2 PROCEDURE

Load program into IF DF 0. To use the program in another field location 4026 must be changed using bits 6, 7, and 8 to give octal address of the field the program is to run in.

1. Load data pattern to be written into locations 6000 to 6007
2. Load address 4000
3. Set bit 0 to a one for Write
4. Clear and continue; after writing a few blocks of data set bit 4 to a one for a rewind command
5. Halt
6. Clear locations 6000 to 6007
7. Load address 4000
8. Set bit 0 to a zero for Read and bit 1 to a one for Forward motion
9. Clear and continue
10. Halt
11. Observe data pattern in locations 6000 to 6007

9.1 TEST PROGRAM

```
4000              6501            6501
4001              TAD CA          1236
4002              DCA FILL        3242
4003              TAD WC          1235
4004              DCA TALLY       3243
4005   AGAIN,     CLA OSR         7604    /Fill Buffer with
4006              DCA I FILL      3642    /data from SW
4007              152 FILL        2242
4010              152 TALLY       2243
4011              JMP AGAIN       5205
4012              TAD WC          1235    /WC = 7726
4013              6522            6522
4014              6544            6544    /FLD = 0
4015              CCL CLL         7300
4016              TAD CA          1236    /CA = 6000
4017              6524            6524
4020              CLA CLL         7300
4021              6502            6502    /SC = 0000
4022              TAD WTORRD      1237
4023              6504            6504    /Command = 4000
4024              TAD TIME        1240
4025              DCA WAIT        3241
4026   LNGWT,     6667            6667    /6511
4027              6667            6667    /5200
4030              6667            6667     5226
4031              6667            6667
4032              ISZ WAIT        2241
4033              Jmp LNGWT       5226
4034              Jmp BACK        5200
4035              WC, 7726
4036              CA, 6000
4037              WTORRD, 4000
4040              TIME, 4000
4041              WAIT, 4000
4042              FILL, 0000
4043              TALLY, 0000
```

9.2 PROGRAM OPERATION

This program will write from field zero start location 6000 a 52_8 word buffer containing a number specified from the switch register setting.

1. Toggle the test program into field 0
2. Load address 4000 and press Clear, then Start
3. The current contents of the switch register becomes drum data.

NOTE 1: If the drum flag is setting satisfactorily insert the following sense flag instructions.

Address		Contents
4026	6511	6511
4027	Jmp BACK	5200
4030	Jmp -2	5226

NOTE 2: To read change the following address

Address		Contents
4037	to	2000

NOTE 3: Throughout the test the letters CB denote control board, DB denotes data board, and BB denotes buffer or derandomizer board.

pcb 10282	CB - logic rack slot B23
pcb 10284	DB - logic rack slot B22
pcb 10262	BB - logic rack slot A26

9.3 Observe the following waveforms of the drum match circuitry on the control board.

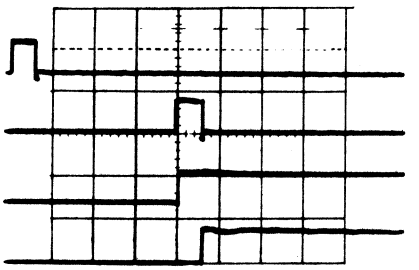
The figure shows the relationship between the Index Clock, Sector Clock, Drum Sync, and Match $\overline{\text{Sector Clock}}$.

Trigger Index Clock CB, pin J

Sector Clock CB, pin V

Drum Match D1-6

Match·$\overline{\text{SC}}$ CB, pin B36



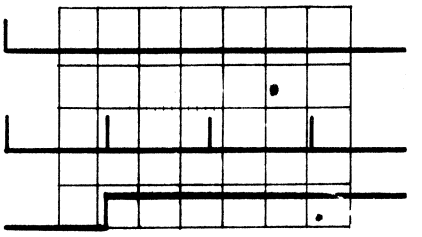
0.5 µs/cm

9.4 The figure shows the output of the Match circuit when sector one is chosen from the switch register.

Trigger Index Clock CB, pin J

Sector Clock CB, pin V

Match CB, E2-8
(Select Sector One)



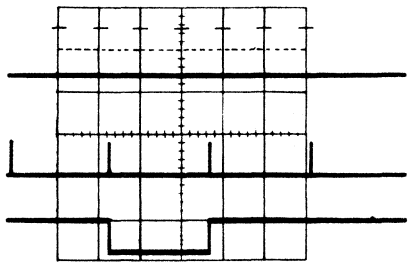
0.1 ms/cm

9.5 The figure shows the Match when Sector Two is chosen from the switch register. For each successive sector chosen the Match will move to the next sector pulse. A maximum of 100_8 sectors can be chosen in this manner.

Index Clock CB, pin J

Sector Clock CB, pin V

Match CB, E2-8
(Select Sector Two)



0.1 ms/cm

9.5.1 The following waveforms are shown with calibration settings and pertinent data.

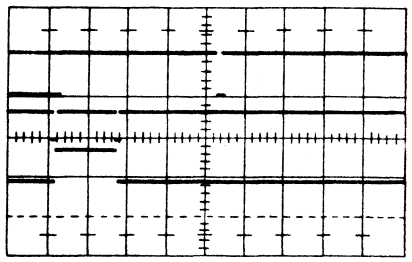
Waveform data:

calibration setting = .2 ms/cm
word count = 52_8
mode = write in field 0

Trigger on Index Clock CB G1-2

Break Request CB B24
40 Word CB B40

WC Overflow CB D2-6



When a data transfer is initiated to the drum, six words are transferred immediately to the derandomizer and the logic waits for an index clock. Upon selecting sector zero the derandomizer starts to empty and break requests are initiated for the remaining 44_8 12-bit words. Two 40 Word pulses are given: One for the first 50_8 word sector and the other to terminate the sector with only two words. Although only two words were written from memory the rest of the sector is filled with the last word taken from CPU memory.

9.5.2 Waveform data:

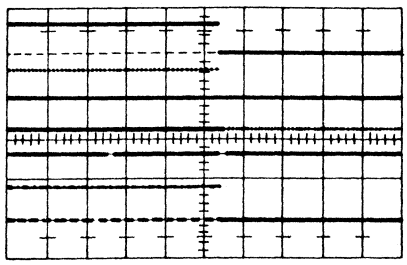
calibration setting = .1 ms/cm mode = write
word count = 52 data word = 5252

Trigger on Match·$\overline{SC}$ DB B13

Load data DB A4-1

Write data DB D5-12

CRC DB D4-10



Trigger on Match·$\overline{SC}$ and observe that Match stays up for two sectors when writing 52_8 words. The controller continues to write a whole sector even though only a portion of a sector is included in the word count. As explained for the previous group of waveforms the data to fill the sector is a repetition of the last word written, and the final CRC check word will be calculated on all data, not just words specified from memory.

Note that the CRC word for constant data will always be zero.

9.5.3 Waveform data:

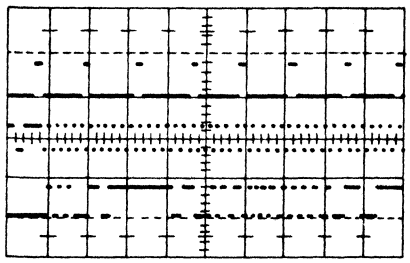
calibration setting = 5 µs/cm mode = write
word count = 52 data word = 5252

Trigger on Match·$\overline{SC}$ DB B13

Load data DB A4-1

Write data DB D5-12

CRC DB D4-10



This group of waveforms is exactly the same as the previous group, except that the time base is 5 µs/cm to show the load pulse every 12 bits, the data output for the data word 5252, and the CRC pulse train for that word.

9.5.4 Waveform data:

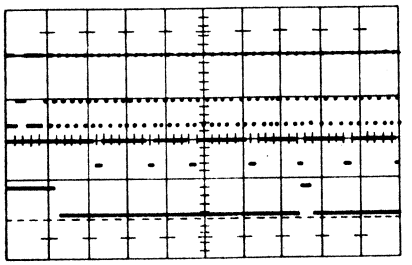
calibration setting = 5 μs/cm mode = read
word count = 52 data word = 5252

Trigger on Match•$\overline{SC}$ DB B13
Load Word DB A3-13

Read data DB A3-15

Read last BD B-29

Detect CRC E3-4



In the read mode data is received and strobed out of the shift register every 12 bits. At the same time Read Last commands are sent to the derandomizer to store the 12-bit word.

9.5.5 Waveform data:

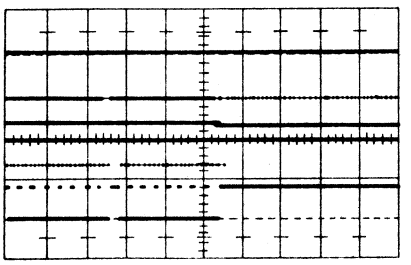
calibration setting = .1 ms/cm mode = read
word count = 52 data word = 5252

Trigger Match•$\overline{SC}$ DB B13
Load word DB A3-13

Read data DB A3-15

Read last DB B29

Detect CRC DB E3-4



This group of waveforms is exactly the same as the group in 9.5.4, except the time base is changed to .1 ms/cm to see the entire read for 52_8 words. The read process continues to the end of the sector even though only 52_8 words are transferred into memory.

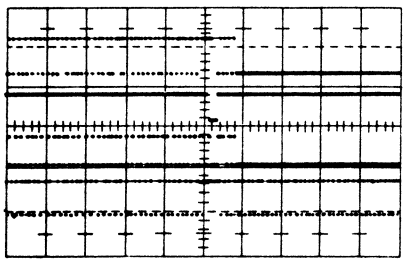
9.5.6 Waveform data, derandomizer read logic:

calibration setting = 50 μs/cm mode = read
word count = 52 data word = 5252

Trigger 1 Drum BRK REQ BB B14

40 Word BB B3

Drum Data BB In BB B13



The waveforms are of signals required to initiate a derandomizer read.

9.5.7 Waveform data, derandomizer write logic:

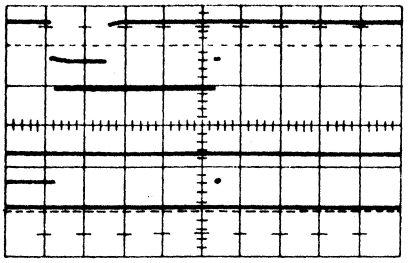
calibration setting	= .2 ms/cm	mode	= write
word count	= 52	data word	= 5252

Trigger 1 Drm BRK REQ BB B14

INHB Shut Down BB B6

BB Out Drum Data BB B7

Drum Wait Sync BB B29



The waveforms are signals required to initiate a derandomizer write.

NOTES: Due to the unsynchronized nature of read and write the internal waveforms become blurred and difficult to record.

If the computer break response is slow (greater than 4.7 µs) the input address can get ahead of the output address causing data to be out by six words.

9.6 FINAL CHECK

Load the latest diagnostic program to check all aspects of the drum logic.

10.1 TEST PROGRAM

TOGGLE THE FOLLOWING TEST PROGRAM

```
4000          CLA OSR        7604    /select MTT from SW
   1          6521           6521
   2          CLA MLT        7602
   3          6554           6554    /Set FLD = 0
   4  BACK,   TAD CA         1236
   5          DCA FILL       3242
   6          TAD WC         1240
   7          DCA TALLY      3243
  10  UP,     CLA OSR        7604    /Write contents of SW
  11          DCA I FILL     3642
  12          ISZ FILL       2242
  13          ISZ TALLY      2243
  14          JMP UP         5210
  15          6532           6532    /clear controller
  16          TAD CA         1236
  17          6552           6552    /set up current address
  20          TAD WTCOM      1237
  21          6542           6542    /set up write command
  22          TAD WC         1240
  23          6551           6551    /set up word count and
  24  WAIT,   6667           6667    /start motion/6531
  25          6667           6667                  Jmp Back
  26          6667           6667                  Jmp Wait
  27          6667           6667    /wait loop
  30          6667           6667
  31          6667           6667
  32          6667           6667
  33          ISZA           2241
  34          JMP WAIT       5224
  35          JMP BACK       5200    5204
  36  CA,                    6000
  37          WTCOM,         4000
4040  WC,                    7770
  41  A,                     0000
  42  FILL,                  0000
  43  TALLY                  0000
```

10.2 PROGRAM OPERATION

The test program will select an MTT from the switch register. Eight word blocks will be written from the contents of the switch register. A long wait loop is used instead of waiting for the flag. This enables cycling the control commands even though a fault prevents the flag from setting. Once the flag is setting properly the wait loop is replaced with the flag sensing IOT as shown below:

change address	to	contents
4024	6531	6531
4025	Jmp BACK	5204
4026	Jmp WAIT	5224

1. Toggle in the program instructions.
2. Load address 4000, set the Switch Register to the desired MTT (MTT 1 = 0010) and press Clear, Continue.
3. The program will halt. Set the Switch Register to equal the desired data and press Continue.
4. The program will write consecutive blocks taking the current contents off the switch register as data.

NOTE: To read consecutive blocks change address 4037 to 2000.

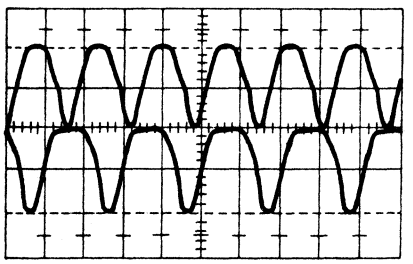
10.3 The following waveforms are shown with cablibration settings and pertinent data.

10.3.1 Waveform data:

calibration setting = 1 µs/cm

640 khz OSC CB A5-5

511.57 khz OSC CB A5-9



The oscillator waveforms are taken at the emitter follower output. The 511.57 khz oscillator will remain constant because it dictates the interrupted gap. The other oscillator's frequency will depend on the word density. The 640 khz oscillator is for 800 bpi.

10.3.2 Waveform data:

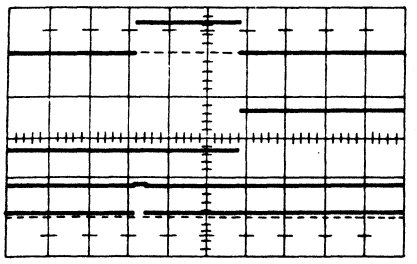
calibration setting	= 5 ms/cm	mode	= write
word count	= 10_8	data word	= 252

Trigger $\overline{6532}$ CB B18

Read permit CB C3-5

Run CB B35

Scaler CB B3-8



Read Permit illustrates a 16 ms start-up time. The blank period in the scaler output is the time taken for data to be transferred to tape. The Run waveform shows the end of the stop time.

10.3.3 Waveform data:

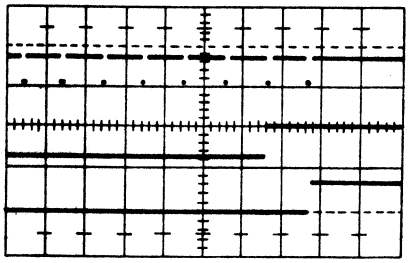
calibration setting = 50 µs/cm mode = write
word count = 10_8 data word = 252

Trigger Read Permit CB C3-5

Break request CB B39

WC Overflow flop CB F3-6

$\overline{\text{Write Data}}$ CB B33



These waveforms are triggered by read permit. The picture shows an eight word data block.

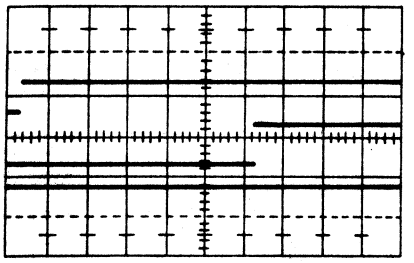
10.3.4 Waveform data:

calibration setting = 2 ms/cm mode = write
word count = 10_8 data word = 252

Trigger $\overline{\text{Write Data}}$ CB B33

Stop flop CB H4-9

Motion CB B35
Read Clock CB H4-3



This group of waveforms illustrate the shutdown sequence. The motion flop is reset about 13 ms after data is written onto tape. The read clocks shown are the Read after Write data.

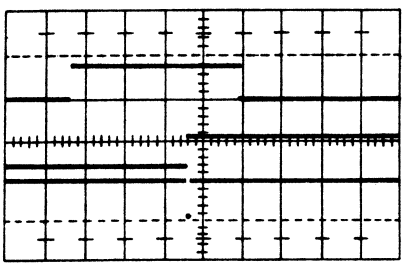
10.3.5 Waveform data:

calibration setting = 5 ms/cm mode = read
word count = 10_8 data data word = 252

Trigger on $\overline{6532}$ CB B18

Read Permit CB C3-5

$\underline{\text{Read Sync}}$ CB H4-5
$\overline{\text{Break Request}}$ CB B36



This group of waveforms illustrates the control timing for Read. The start-up time for read is 8 ms.

10.3.6 Waveform data:

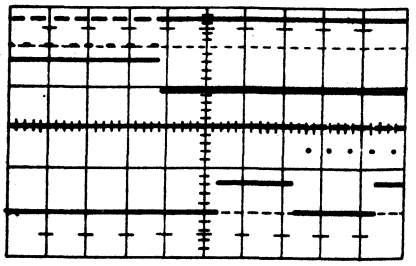
calibration setting = .1 ms/cm
word count = 10
mode = write
data word = 252

Trigger clock CRC DB F1-8

Strobe Data out DB B1-1

Strobe LRCC out DB B1-9

Strobe CRCC out DB G5-3



The waveforms shown are taken on the data pcb for a block of eight words and show the major data and CRC gating signals.

10.3.7 Waveform data:

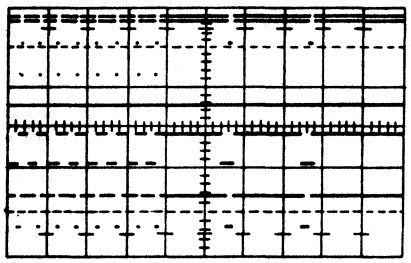
calibration setting = .1 ms/cm
word count = 10
mode = read
data word = 252

Trigger read clock DB B4

Data in DB B16

Read Parity DB G2-12

1 to BRK DB B-11



These waveforms show the major gating signals during Read.

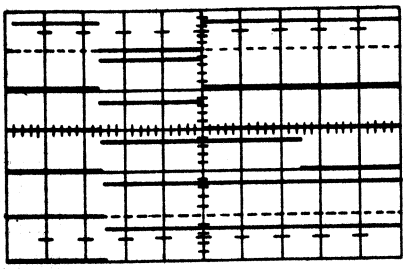
10.3.8 Waveform data:

calibration setting = 20 µs/cm
word count = .4
mode = write
data words = 6000 = 0
6001 = 7
6002 = 70
6003 = 370

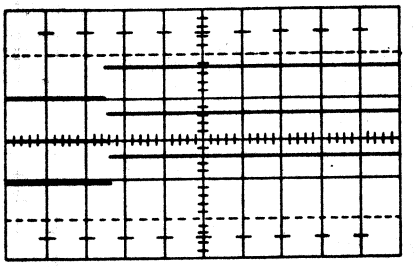
Test Program changes = 4011 = 7200

trigger CRC clock

DB C2-9



Data at C2-9
DB C3-9
DB C3-10
DB C3-7
DB C3-6
DB C4-9
DB C4-10
DB C4-7
DB C4-6



The waveforms show the output of the CRC generator flops as the data 0, 7, 70, 370 is read from memory.

10.3.9 Waveform data:

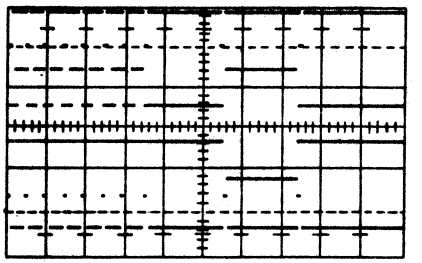
calibration setting = .1 ms/cm
word count = 10
mode = read
data word = 252

Trigger Read Clock RC B22

LRCC detect RC H5-8

CRCC detect RC H5-8

Strobe CRCC RC A1-8



These waveforms show the LRCC and CRCC detect signals when reading a block of eight data words (0252).

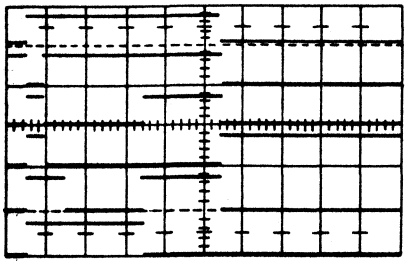
10.3.10 Waveform data:

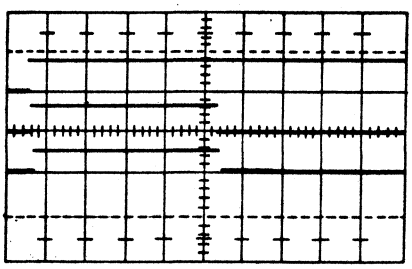
calibration setting = .1 ms/cm
word count = 4

mode = read
data words = same as for write
test program change = 4037 ⟶ 2000

Trigger read clock
RC B32

Data at I4-5
I4-9
H4-5
H4-9
G4-5
G4-9
F4-5
F4-9
E4-9





These waveforms show the hardware CRC calculation for the four data words 0, 7, 70, 370.

10.4 WRITE END OF FILE

Use the following program to test EOF

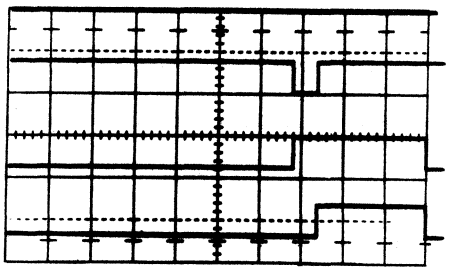
```
* 2000    6532      6532
  2001    TAD EOF   1207
  2002    6542      6542
  2003    6551      6551
  2004    6531      6531
  2005    Jmp BACK  5200
  2006    Jmp .-2   5204
  EOF,    400       400
```

Trigger WEOF CB B8

Read Permit CB H1-6

1 to Stop CB E4-9

Run CB A37



20 ms/cm

10.5 FINAL CHECK

Load latest diagnostic program to automatically check Write, Read, EOF, and Status.

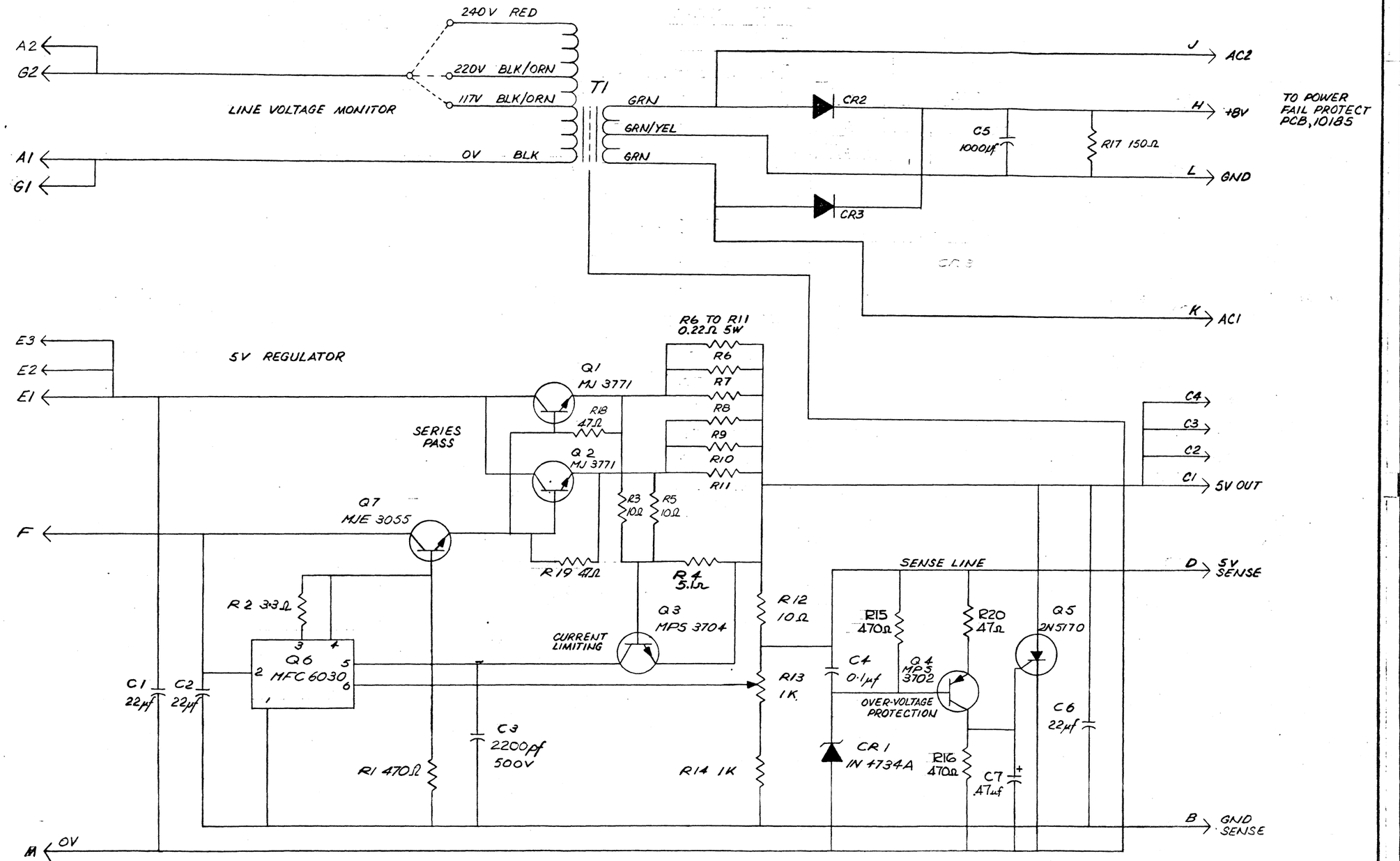


FIGURE 6-2-5

B	ECO KE 499 INCORP	8 Nov 72	LL	
A1	DREVO# 176 INCORP	23 FEB 72	WB	
A	ECO# KE 293 INCORP	10 JAN 72	RWL	
Ø1	DREVO# 256 INCORP	27 JULY 71	MI	

B11036P used on

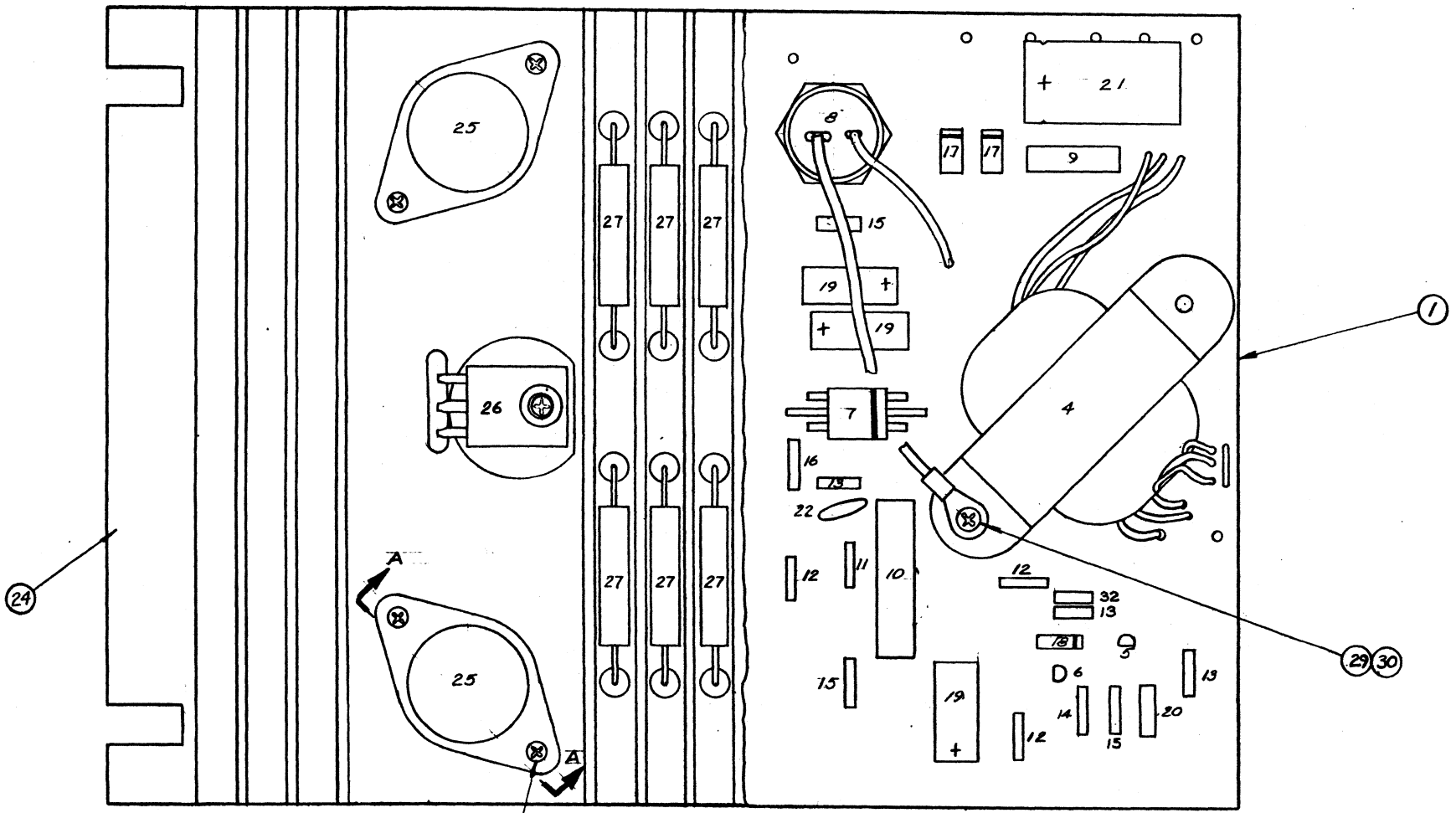
unless specified
fractions ±1/64
.00 = ±.01
.000 = ±.005
angles = ±0°30'

scale | 11 MARCH 71 date | M. N. drawn | design apprvl | checked | material

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

5V 20A REGULATOR PCB SCHEMATIC

title



SECTION 'AA'
TYP. 2 PLACES

NOTE:
1. HEAT SINK COMPOUND (WAKEFIELD P/N 122 CCL P/N 90890) REQ'D BETWEEN HEAT SINK AND EACH TRANSISTOR.
2. ITEM 26 (TRANSISTOR MJE3055) REQUIRES MICA INSULATOR WHICH IS SUPPLIED WITH TRANSISTOR.

rev	description	date	by	apprvd
A	ECO "KE 293 INCORP	10 JAN 72	RWL	
Ø3	DREVO "110 AL CHANGE	13 OCT 71	RAP	
Ø2	DREVO # 056 INCORP	27 JULY 71	MJ	
Ø1	DWG Nº CHANGE C11036A WAS C11035A	14 JUNE 71	JRB	

D11034A/1 used on A1/2 | 4:1 scale | 21 MAY date | R.M. drawn

unless specified: fractions ± 1/64; .00 = ± .01; .000 = ± .005; angles = ± 0°30'

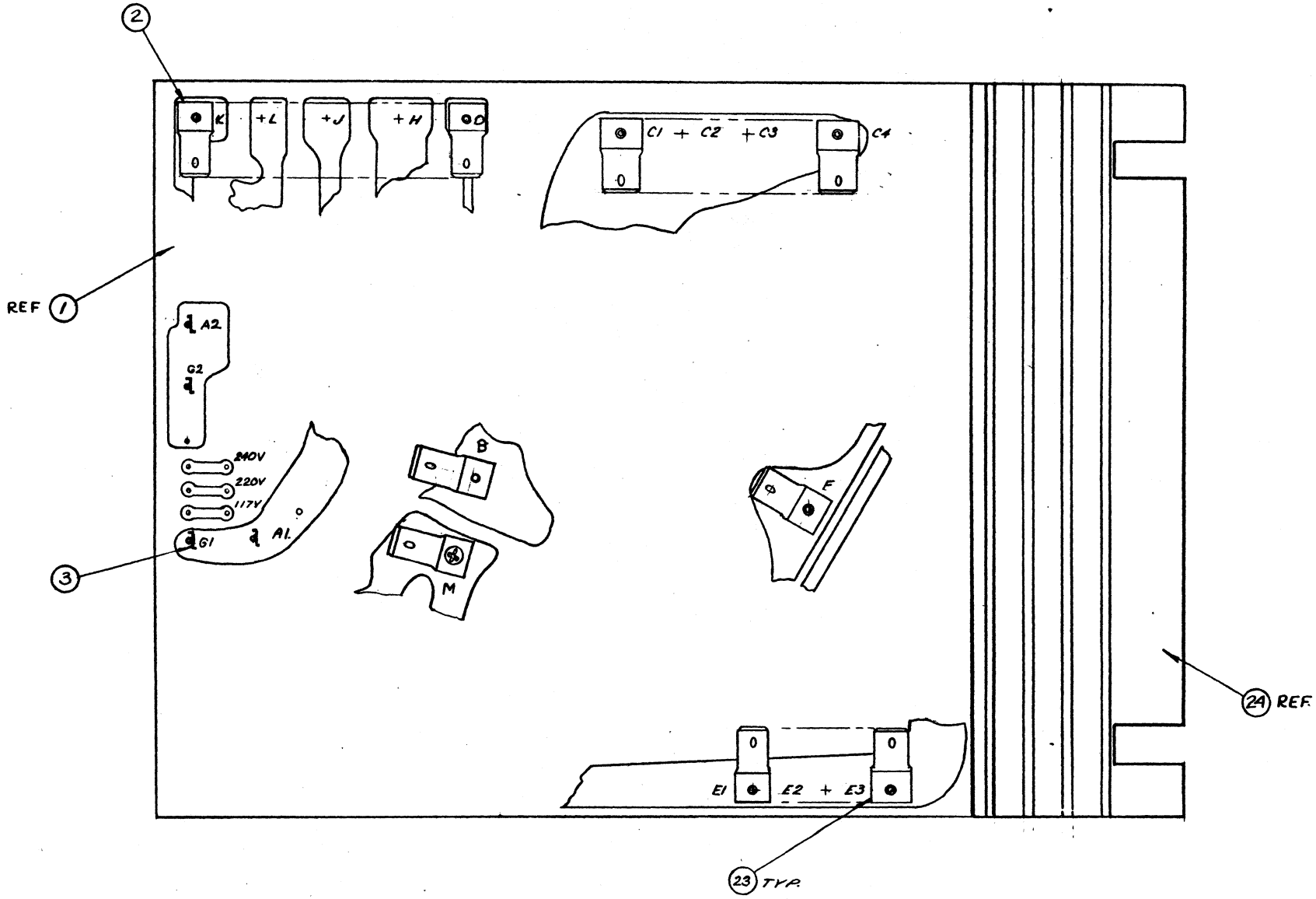
material | finish | W.B.S. Collis design apprvl | checked | final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

LOGIC RACK REGULATOR 5V-20A PCB ASSY

title

sheet 1 of 2 | no. C11036A | A rev



TRACK SIDE SHOWN.

rev	description	date	by	approvd
A	ECO *KE 293 INCORP	10JAN72	EWL	WG
Ø3	DREVO*110 P/L CHANGE	13 OCT 71	RAP	
Ø2	DREVO*056 INCORP	27JULY71	MJ	
Ø1	DWG No CHANGE	14 JUNE 71	JRB	

dwg no DWG34A 11/12 | scale 4:1 | date 20MAY71 | drawn R.M | design approvl | checked | final approvl

unless specified
fractions ± 1/64
.00 = ±.01
.000 = ±.005
angles = ± 0°30'
material
finish

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title: LOGIC RACK REGULATOR 5V-20A PCB. ASSY.

sheet 2 of 2 | no. C111036A | Δ

CON LIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R.M. | DATE: 21 MAY 71 | APPROVED BY:

TITLE: LOGIC RACK REGULATOR 5V-20A PCB ASSY.

SERIAL NO.

USED ON ASSEMBLY: D11034A 1/2

DRAWING REV. A

DATE ISSUED

ASSEMBLY NO. C11036A

SHT 1 OF 2

PRODUCT

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.
1	B11036P		1	LOGIC RACK REGULATOR P.C.B.		Ø2 (DREVO#
2	91757		15	TAB 250 FASTON	AMP 428 22-2	Ø3 (DRCVO# 11
3	91817		4	TAB 110 FASTON	AMP 61134-1	A (ECO# KE 29
4	91538		1	TRANSFORMER 95038 HAMMOND	T1	
5	90598		1	TRANSISTOR MPS 3702	Q4	
6	90597		1	TRANSISTOR MPS 3704	Q3	
7	91767		1	IC. MFC 6030	Q6	
8	91763		1	SEMICONDUCTOR 2N 5170	Q5	
9	90482-43		1	RESISTOR 150Ω 1W	R17	
10	90484		1	RESISTOR TRIMPOT 1K 1W	R13	
11	90480-63		1	RESISTOR 1K ¼W	R14	
12	90480-15		3	RESISTOR 10Ω ¼W	R3, R5, R12	
13	90480-55		3	RESISTOR 470Ω ¼W	R1 R15, R16	
14	90480-8		1	RESISTOR 5.1Ω ¼W	R4	
A 15	90480-31		3	RESISTOR 47Ω ¼W	R18, R19, R20	
16	90480-3		1	RESISTOR 3.3Ω ¼W	R2	
17	91161		2	DIODE IN4002	CR2, CR3	
18	91764		1	DIODE IN4734A	CR1	
19	90103		3	CAPACITOR 22 uf 35V	C1, C2, C6	
Ø3 20	91583		1	CAPACITOR 0.1 uf 50V	C4	
21	90099		1	CAPACITOR 1000 µf 25V	C5	
22	90098		1	CAPACITOR 2200 pf 500V	C3	
23	91902		14	EYELET 4/32 DIA x 6/32 LG BRASS	SPAENAUR E-46	

CONSOLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: R.M. | DATE: 27MAY71 | APPROVED BY:

TITLE: LOGIC RACK REGULATOR 5V-20A PCB ASSY.

SERIAL NO.

USED ON ASSEMBLY: 11 D11034A 12

DRAWING REV. A

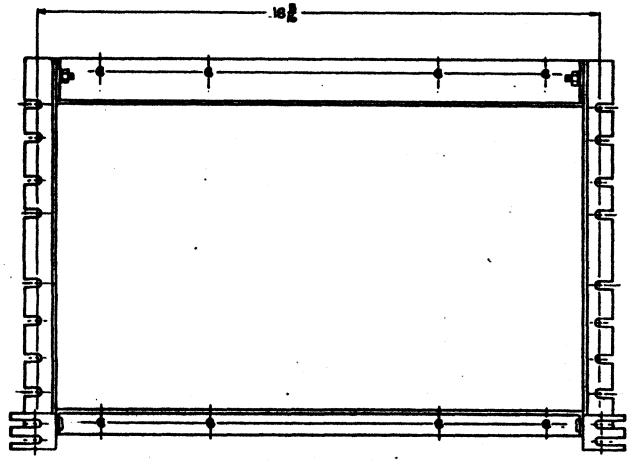
DATE ISSUED

ASSEMBLY NO. C11036A

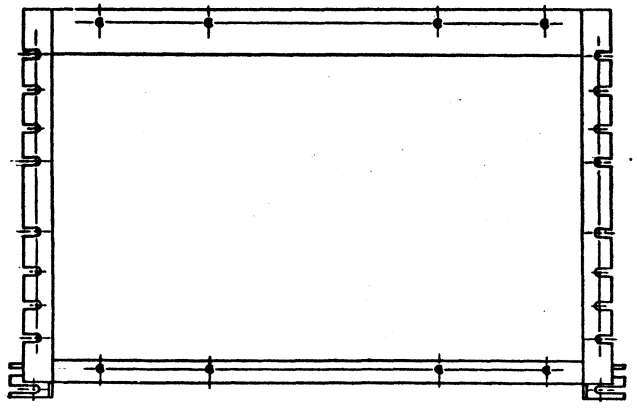
SHT 2 OF 2

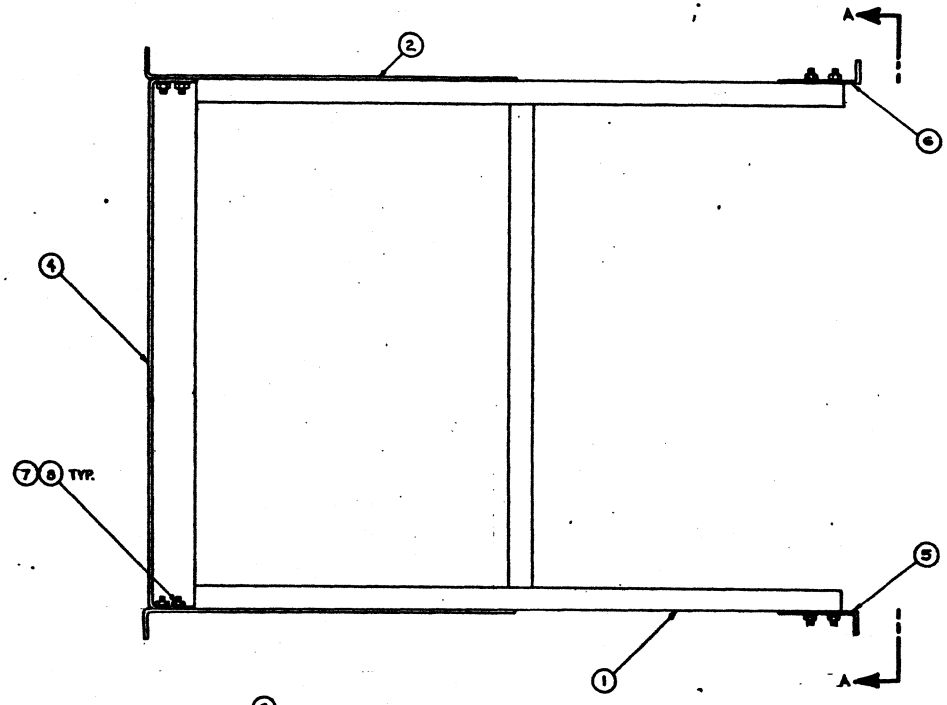
PRODUCT

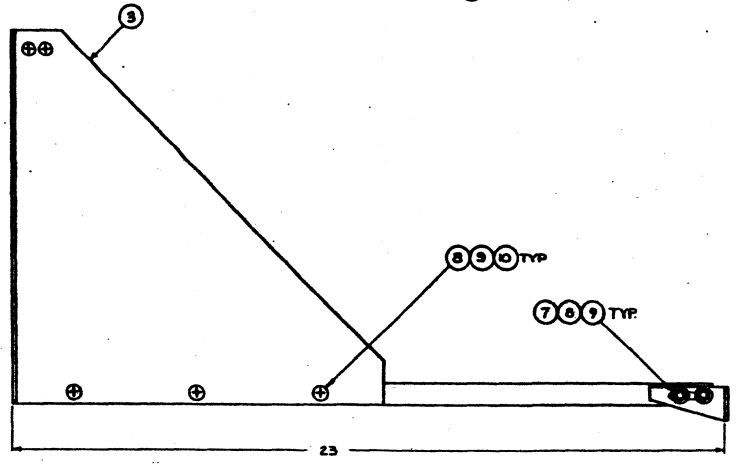
	ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO.
	24	C11035M		1	HEAT SINK		Ø2(DREVO#5
	25	91343		2	TRANSISTOR MJ3771	Q1, Q2	Ø3(DREJO #11
	26	90581		1	TRANSISTOR MJE 3055	Q7	A(ECO #KE29
	27	91818		6	RESISTOR 0.22Ω 4W	R6, R7, R8, R9 R10, R11	
	28	90043-27		5	SCREW 6-32 X 3/4" P.P.H.		
	29	91202		6	NUTS 6-32 KEP.		
	30	90043-24		1	SCREW 6-32 x 3/8" P.P.H.		
	31	BS10214M-3/16		4	SPACER 3/16" ID. X 3/16 LG.		
A	32	91678		1	CAPACITOR .47 μf 35 V	C7	
	REF	C11036S			SCHEMATIC		



VIEW A-A







	PRODUCTION RELEASE #E350	16 JULY 72	A.L.	A		
GP1	PICTORIAL CHANGE DREVO 167	2 JAN 72	RWL			
rev	description	date	by	approved		

used on	1/2	MAY 71	MJ
unless specified fractions ± 1/64, .00 ± .01, .000 ± .005, angles ± 0°30'	material		drawn
			design approval
			checked
finish			engineering approval

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

ASSEMBLY
AC POWER DISTRIBUTION RACK

title

sheet 1 of 1 | dwg D11085A | rev

C OLIDATED COMPUTER SERVICES LTD.

ASSEMBLY PARTS LIST

WORK AREA

COMPILED BY: MJ | DATE: 21 MAY 71 | APPROVED BY: [illegible]

TITLE: ASSEMBLY

AC POWER DISTRIBUTION RACK

SERIAL NO.

USED ON ASSEMBLY:

DRAWING REV. A

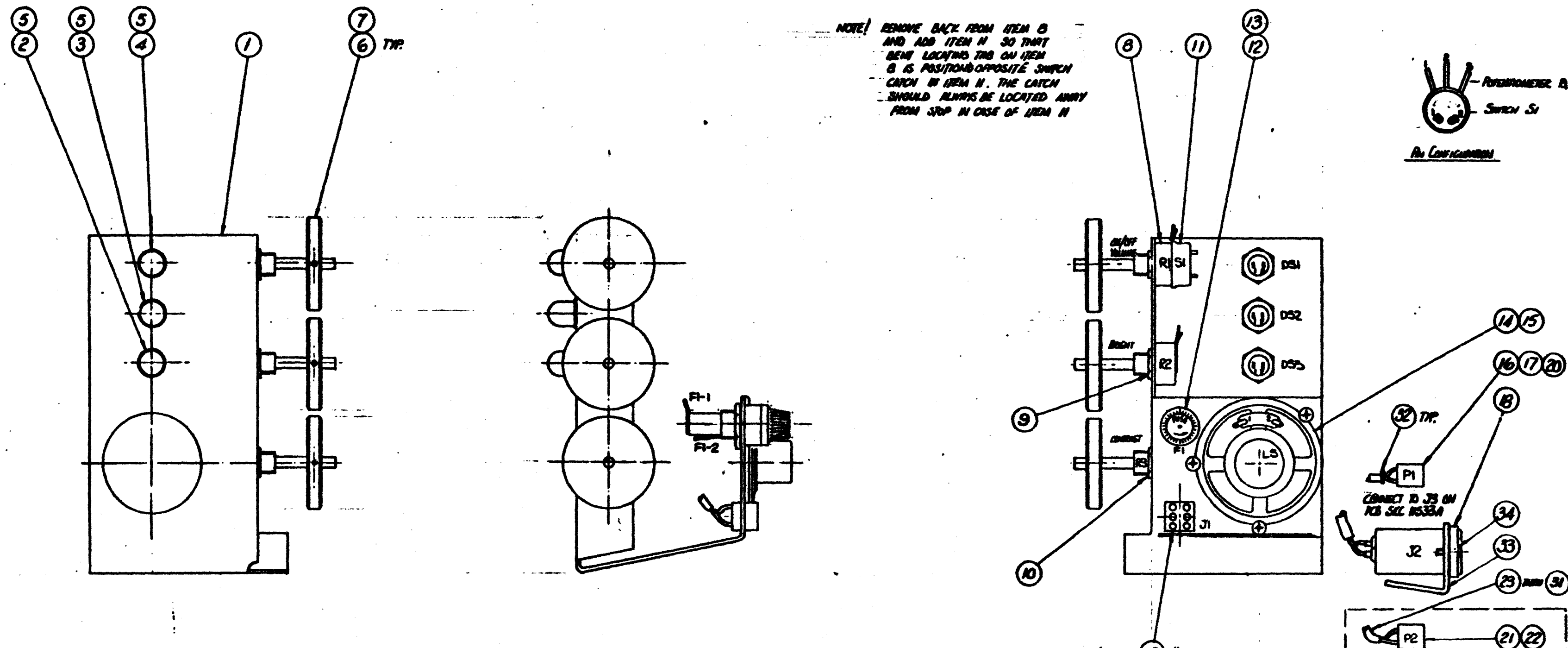
DATE ISSUED

ASSEMBLY NO. D11085A

SHT 1 OF 1

PRODUC

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	E.C.O. NO
1	C11085M		1	RACK BASE	2 SHTS	Ø1 DREVO
2	BS11057M/1		1	SIDE PANEL (LH)		A KE 35(
3	BS11057M/2		1	SIDE PANEL (RH)		
4	B11086M		1	FRONT TOP BRACE		
5	BS11060M/1		1	REAR BRACKET (RH)		
6	BS11060M/2		1	REAR BRACKET (LH)		
7	91301		14	NUT, KEP 10-32		
8	90043-47		4	SCREW, 10-32 X 1/2 LG. PPH		
9	90124		4	WASHER, FLAT NO. 10		
Ø1 10	90040-47		10	SCREW, 10-32 x 1/2 LG P.F.H 82° C'SK		



NOTE! REMOVE BACK FROM ITEM 8 AND ADD ITEM 11 SO THAT BENT LOCATING TAB ON ITEM 8 IS POSITIONED OPPOSITE SWITCH CATCH IN ITEM 11. THE CATCH SHOULD ALWAYS BE LOCATED AWAY FROM STOP IN CASE OF ITEM 11

* CONTACT TYPE F = FEMALE M = MALE

PIN №	1	2	3	4	5	6
P1	M	F	M	M	-	-
J1	M	M	M	F	F	F

VOLTAGE	JUMPER	LINE	NEUT
115	1-3 & 2-5	2	1
220	2-3	4	1
230	2-3	5	1
240	2-3	6	1

NOTE! REFER TO SKA 11570 W FOR WIRING DIAGRAM FOR PARTS LIST SEE SHEETS 1 & 2

rev	eco	description	date	by	chk	approved
4		NOTE ADDED PIN CHANGED ITEM 5	31 JAN 73			
3		ITEM 33 & 34 ADDED	27 DEC 72			
2		CONNECTOR I.D. CHANGED	13 DEC 72			
1		PRE PRODUCTION RELEASE				

used on SKD 11565 A
scale 1:1 date 12-OCT-72
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ±0 30'
drawn / design approval / checked / final approval / material / finish

CONSOLIDATED COMPUTER INC. OTTAWA

SUB ASSY - SWITCH MOUNTING BRACKET

sheet no. SKD 11570 A

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: JEB | DATE: 10 OCT 72 | APPROVED BY: [illegible]

USED ON ASSEMBLY: SKD 11565 A | DRAWING REV: 4

ASSEMBLY NO: SKD 11570 A | SHT 2 OF 3

TITLE: SUB ASSY SWITCH MOUNTING BRACKET SERIES 1000 DATA TERMINAL (BALL TYPE)

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS		QTY. REQ.	AVAIL
1	SKD 11570 M		1	SWITCH MOUNTING BRACKET				
2	92882		1	LAMP ASSY RED # 162 8430 0931 502	DIALCO	DS1		
3	92883		1	LAMP ASSY GREEN # 162 8430 0932 502	DIALCO	DS2		
4	92884		1	LAMP ASSY YELLOW # 162 8430 0933 502	DIALCO	DS3		
5	91311		3	LAMP 6V .04A · #345	CHICAGO MINI LAMP WORKS			
6	SKB 11625 M		3	THUMBWHEEL				
7	91935		3	SCREW 4-40 UNC x 1/4 LG SOCKET HEAD SET				
8	93126	*	1	POTENTIOMETER 500 Ω AUDIO TAPER		R1		
9	92887	*	1	POTENTIOMETER 100 K CARBON (NOT WIRE WOUND)		R2		
10	92889	*	1	POTENTIOMETER 500 Ω CARBON (")		R3		
11	92889		1	AD-A-SWITCH		S1		
12	90283		1	FUSE HOLDER				
13	90276		1	FUSE SLO BLO 115V 1 1/2 A		F1		
OR 13	90279		1	FUSE SLO BLO 230V 1/2 A		F1		
14	92902		1	SPEAKER 8 Ω P222	DAVCO			
15	90013-34		3	SCREW 8-32 x 1/4 PPH				
16	92892		1	RECEPTACAL # 1625-4R	MOLEX			
17	92894		4	FEMALE CONTACT # 1561	MOLEX	P1		
18	92890		1	LINE FILTER & CONNECTOR # IEF 115/230V	CORCOM	J2		
19	92897		1	RECEPTICAL # 1625 6R	MOLEX	J1		
20	92893		6	MALE CONTACT # 1560	MOLEX			
21	91974		1	HOUSING AMP 1-480276-0	MATE-N-LOK	P2		
22	92895		6	CONTACT AMP 61116-1	MATE-N-LOK			

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: JRB | DATE: 10 OCT 72 | APPROVED BY:

USED ON ASSEMBLY: SKD 11565 A | DRAWING REV: 4

ASSEMBLY NO: SKD 11570 A | SHT 3 OF 3

TITLE: SUB ASSY SWITCH MOUNTING BRACKET SERIES 1000 DATA TERMINAL (BALL TYPE)

QTY RUN

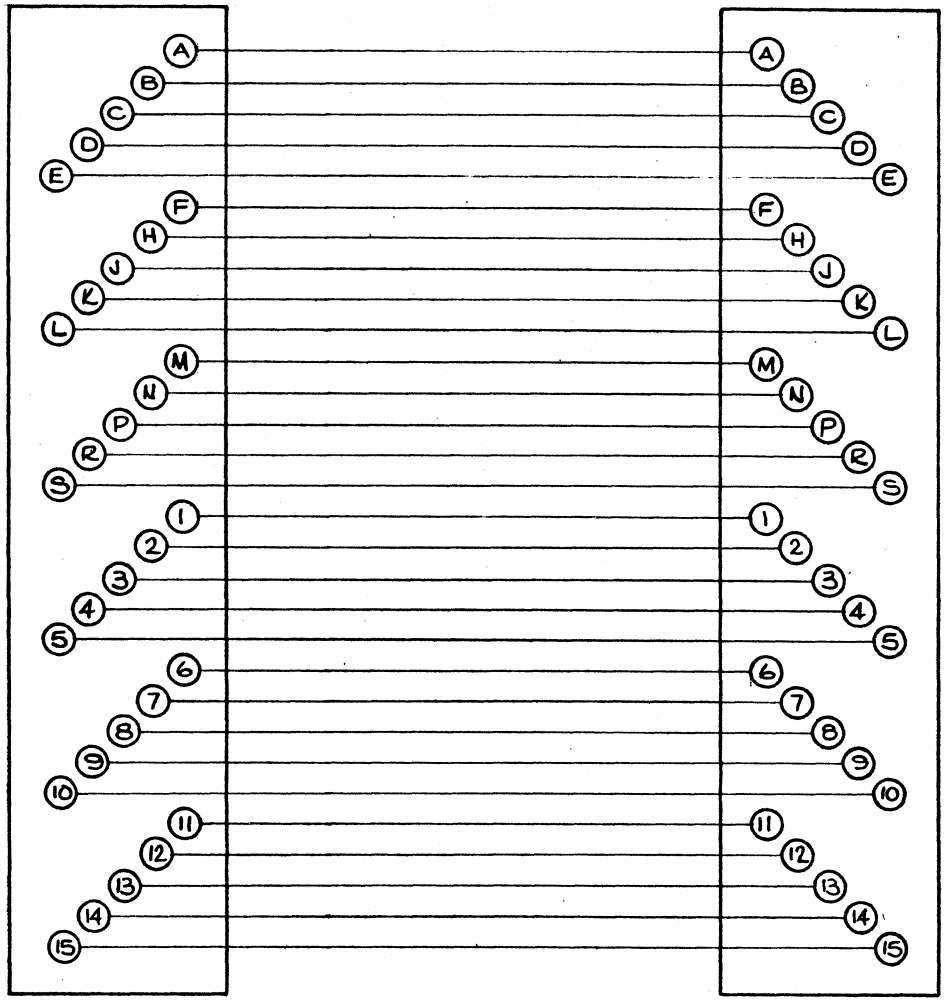
DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
23	90605-2		25"	WIRE 20 GA STRANDED RED			
24	90605-4		25"	YEL			
25	90605-1		25"	GRN			
26	90605-6		20"	BLU			
27	90605-5		5"	GRN			
28	90604-0		50	WIRE 18GA STRANDED BLK			
29	90604-9		40	WHI			
30	90604-5		12"	GRN			
31	90604-4		5"	YEL			
32	90195		10	CABLE TIE			
33	SKB 11696M		1	MOUNTING BRACKET			
34	90043-13		2	SCREW 4-40 UNC X 3/8 LG PPH			
REF	SKA 11570 W			WIRING			
*	93126			SPEC CONTROL DING REQ'D			
	92887			" " " "			
	92888			" " " "			

CONSOLIDATED COMPUTER LTD			TITLE WIRING - SUB ASSY SWITCH MOUNTING BRACKET SERIES 1000 DATA TERMINAL (BALL TYPE)	ASSY NO SKA 11570 W	REV 3
COMPILED BY JCS	DATE 21AUG72	APPR BY		USED ON SKD 11570A	SHT 1 OF 1

WIRE NO	WIRE SIZE	COLOR CODE	LGT	FROM	TO	SIGNAL	REMARKS	ECO	APP
1	20 GA	RED	14"	P1-1	LS1	5V		SK012	
2	20 GA	RED	6"	LS-1	DS3-1	5V		SK014	
3	20 GA	RED	2"	DS3-1	DS2-1	5V			
4	20 GA	RED	2"	DS2-1	DS1-1	5V			
5	20 GA	YEL	12"	P1-2	DS2-2	READY			
6	20 GA	BRN	12"	P1-3	DS3-2	ERROR			
7	20 GA	BLU	12"	P1-4	R1-2	TONE			
8	20 GA	BLU	6"	R1-3	LS-2	TONE			
9	20 GA	GRN	4"	DS1-2	GND	GND			
10	18 GA	WHI	39"	J2 - NEUTRAL	P2-1	NEUTRAL			
11	18 GA	BLK	12"	J2 - LINE	S1-1	LINE			
12	18 GA	GRN	12"	J2 - EARTH	CHASSIS GND	GND.			
13	18 GA	BLK	6"	S1-2	F1-1	LINE			
14	18 GA	BLK	30"	F1-2	P2-2,4,5 OR 6	LINE	SEE TABLE SKD 11570A		
15	18 GA	YEL	2"	P2-1	P2-3	115V	"		
16	18 GA	YEL	2"	P2-2	P2-5	115V	"		
17	20 GA	BRN	6"	R2-1	J1-1	BRIGHTNESS			
18	20 GA	YEL	6"	R2-3	J1-2	"			
19	20 GA	GRN	6"	R2-2	J1-3	"			
20	20 GA	GRN	6"	R3-1	J1-4	CONTRAST			
21	20 GA	YEL	6"	R3-2	J1-5	"			
22	20 GA	GRN	6"	R3-3	J1-6	"			
23	18 GA	YEL	2"	P2-2	P2-3	220, 230 OR 240 V	SEE TABLE SKD 11570A		



v	eco	description	date	by	chk	apprvd
		PRE-PROD. RELEASE	8 DEC 72	DJ		

used on: SLC 11731A
scale / date: 2 NOV 72
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

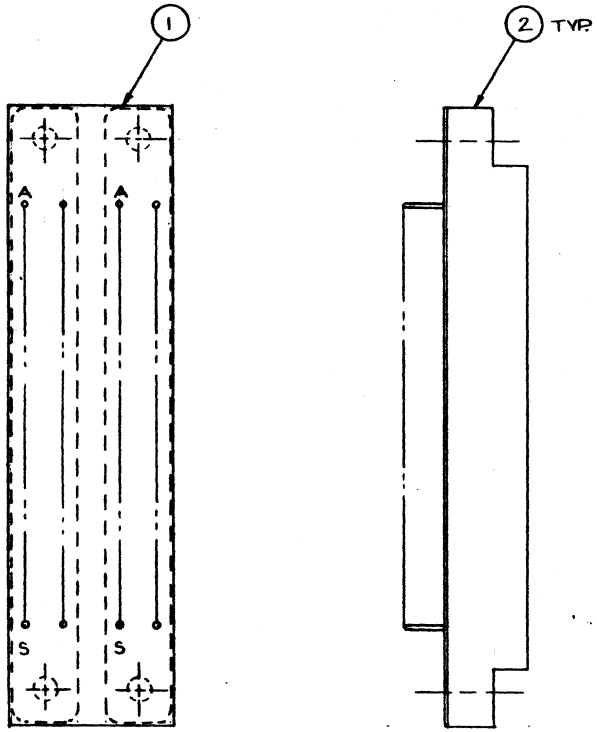
drawn: MJ
design apprvl: DJW
checked:
final apprvl:

CONSOLIDATED COMPUTER INC.
OTTAWA

material:
finish:

title: SCHEMATIC
SERIES-L-100V
INTERCONNECT-2

sheet 1 of 1
no. SLB 11731S
rev 1



FOR PARTS LIST SEE SHT 2

rev	eco	description	date	by	chk	approvd
1		PRE-PROD. RELEASE	8 DEC 72	DJ	MJ	

used on: SLD 11707A
scale: 2:1
date: 25 OCT 72
drawn: DJ
design apprvl: DJW
checked: MJ
final apprvl:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material:
finish:

CONSOLIDATED COMPUTER INC.
OTTAWA

title: PCB ASSEMBLY
SERIES L-100V
INTERCONNECT-2

sheet 1 of 2
no. SLC 11731A
rev 1

TRANSTEK 10 000-0-76

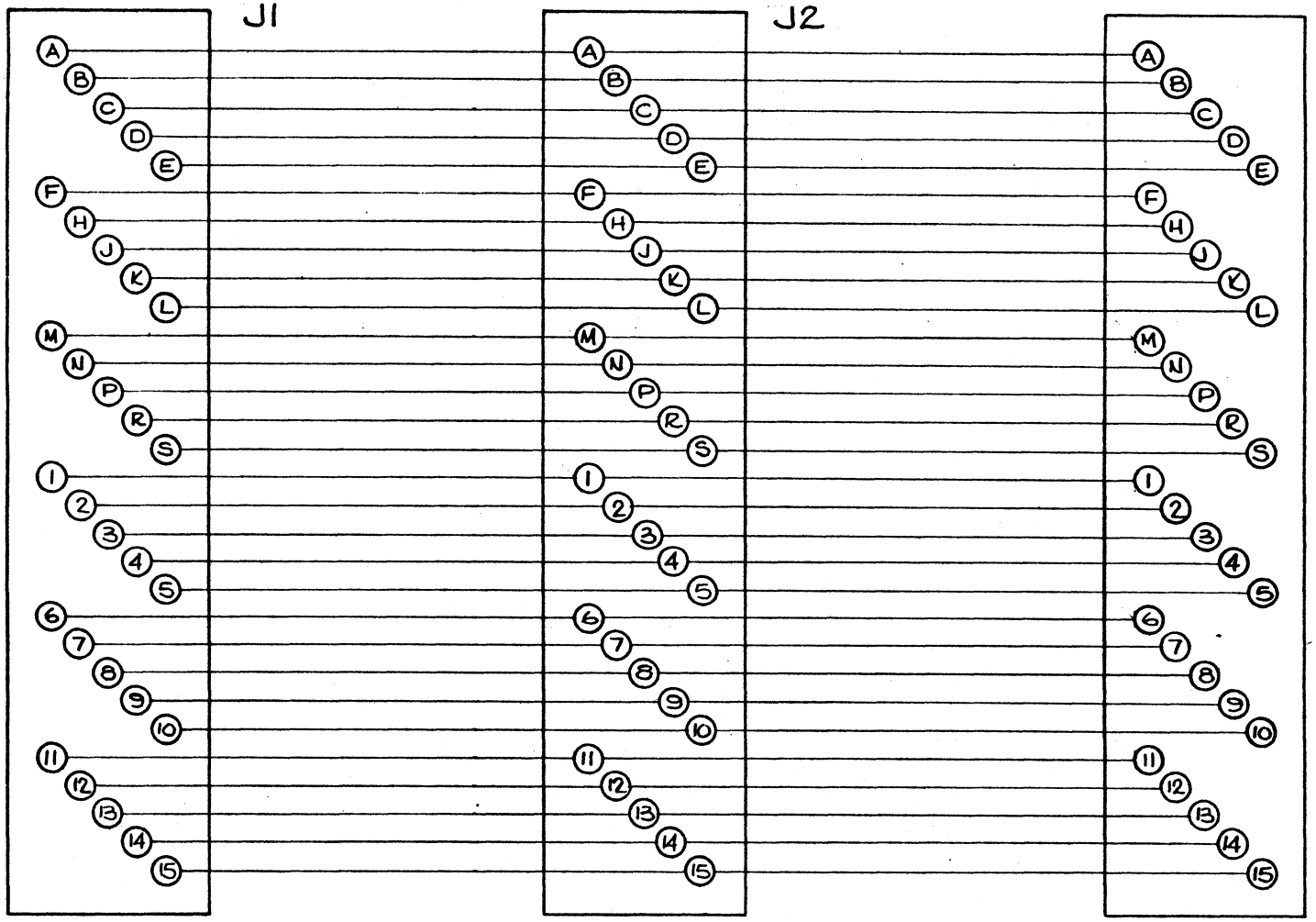
CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: DJ	DATE OCT 72	APPROVED BY MJ	QTY RUN
USED ON ASSEMBLY SLD11707A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLC11731A		SHT 2 OF 2	CONTROL

TITLE: PCB ASSY
SERIES L-100V
INTERCONNECT - 2
FOR ASSY SEE SHT 1

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLD11731P		1	PCB BLANK			
2	92811		2	CONNECTOR (ELCO)	6007-030-981-002		
REF	SLC11731M/1			BOARD OUTLINE			
REF	SLB11731S			SCHEMATIC			



ev	eco	description	date	by	chk	apprvd
		PRE-PROD RELEASE	8 DEC 72	DJ		

SLC 11732A — used on

2 NOV 72 — scale / date

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

MJ — drawn
DJW — design apprvl
checked
final apprvl

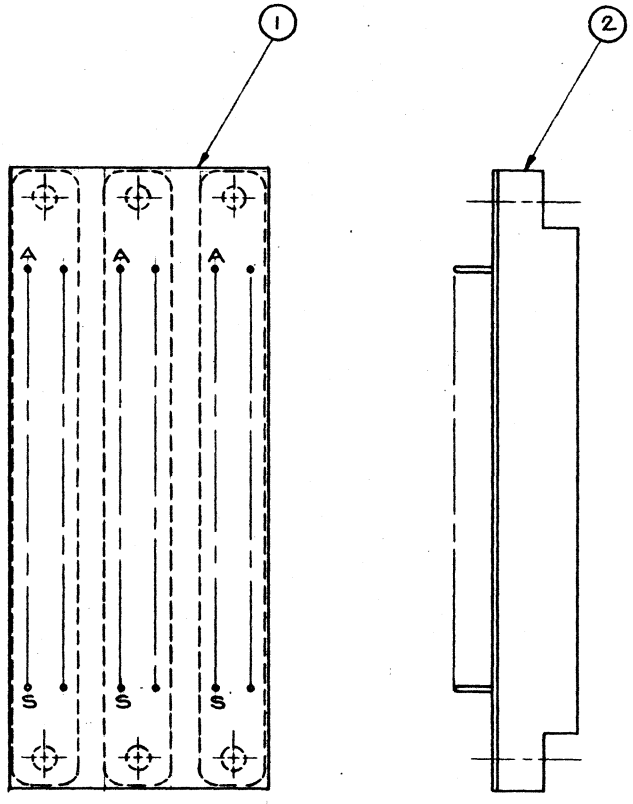
CONSOLIDATED COMPUTER INC.
OTTAWA

material
finish

SCHEMATIC
SERIES - L - 100V
INTERCONNECT-3

title

sheet 1 of 1
no. SLB11732S
1



FOR PARTS LIST SEE SHT 2

rev	eco	description	date	by	chk	apprvd
1		PRE PROD. RELEASE	8 DEC 72	DJ	MI	

used on: SLD 11707A
scale: 2:1
date: 25 OCT 72
drawn: DJ
design apprvl: DJW
checked: MI
final apprvl:

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: PCB ASSEMBLY SERIES L-100V INTERCONNECT-3

sheet 1 of 2
no. SLC 11732A
rev 1

TRANSTEX 10 000-0-72

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: D J | DATE: 25 OCT 72 | APPROVED BY: MJ

USED ON ASSEMBLY: SLD11707A | DRAWING REV: 1

ASSEMBLY NO: SLC11732A | SHT 2 OF 2

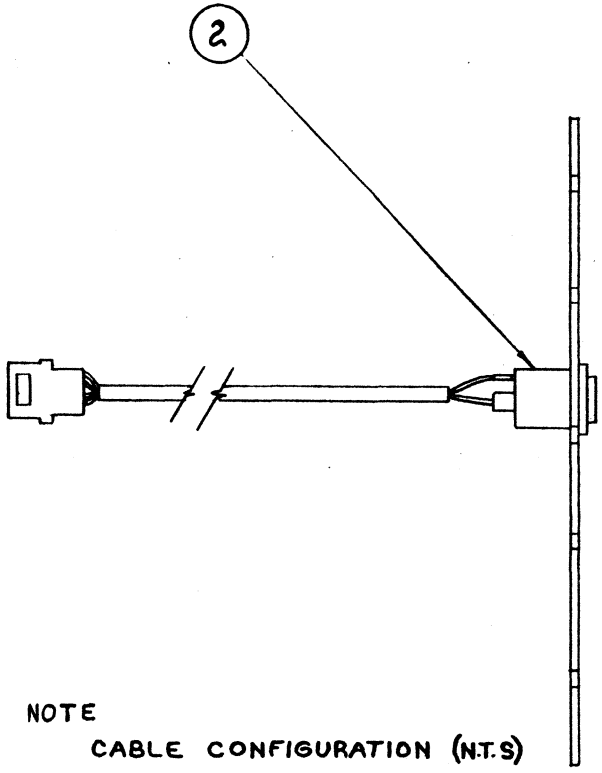
TITLE: PCB ASSY
SERIES L-100V
INTERCONNECT - 3
FOR ASSY SEE SHT 1

QTY RUN

DATE ISSUED

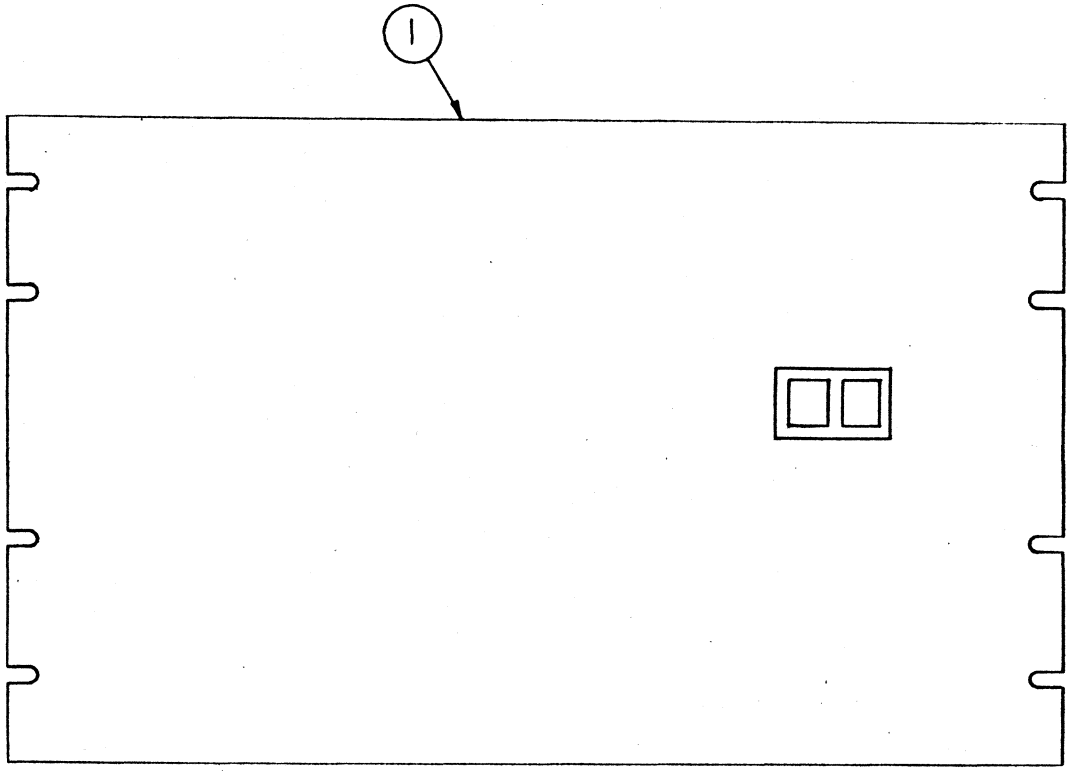
CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLD11732P		1	PCB BLANK			
2	92811		3	CONNECTOR (ELCO)	6007-030-981-002		
REF	SLC11731M/2			BOARD OUTLINE			
REF	SLB11732S			SCHEMATIC			



NOTE

CABLE CONFIGURATION (N.T.S)



FOR P/L SEE SHT 2

rev	description	date	by	apprvd
2	ECO SL007 INC.	16JAN73	MS	
1	PRODUCTION RELEASE	5-JAN-73	JB	

SLD11780A
SLB11786A
used on

unless specified
fractions ± 1/64
.00 = ±.01
.000 = ±.005
angles = ±0°30'

scale 1:2 | date 3 JAN 73

material | finish

drawn JB
design ENG
checked
final apprvl

CONSOLIDATED COMPUTER INC.
OTTAWA

material | finish

MAIN SWITCH PANEL ASSY
SERIES L-100V/PHASE 1
220/240V

title

sheet 1 of 2 | SL no. B 11783 A | 2 rev

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY:	DATE	APPROVED BY
JB	3 JAN 73	

TITLE: MAIN SWITCH PANEL ASSY
SERIES L-100V/ PHASE 1
220/240V
(FOR DWG SEE SHT 1)

USED ON ASSEMBLY: SLB11780A & SLB11786A

DRAWING REV: 2

ASSEMBLY NO: SLB11783A

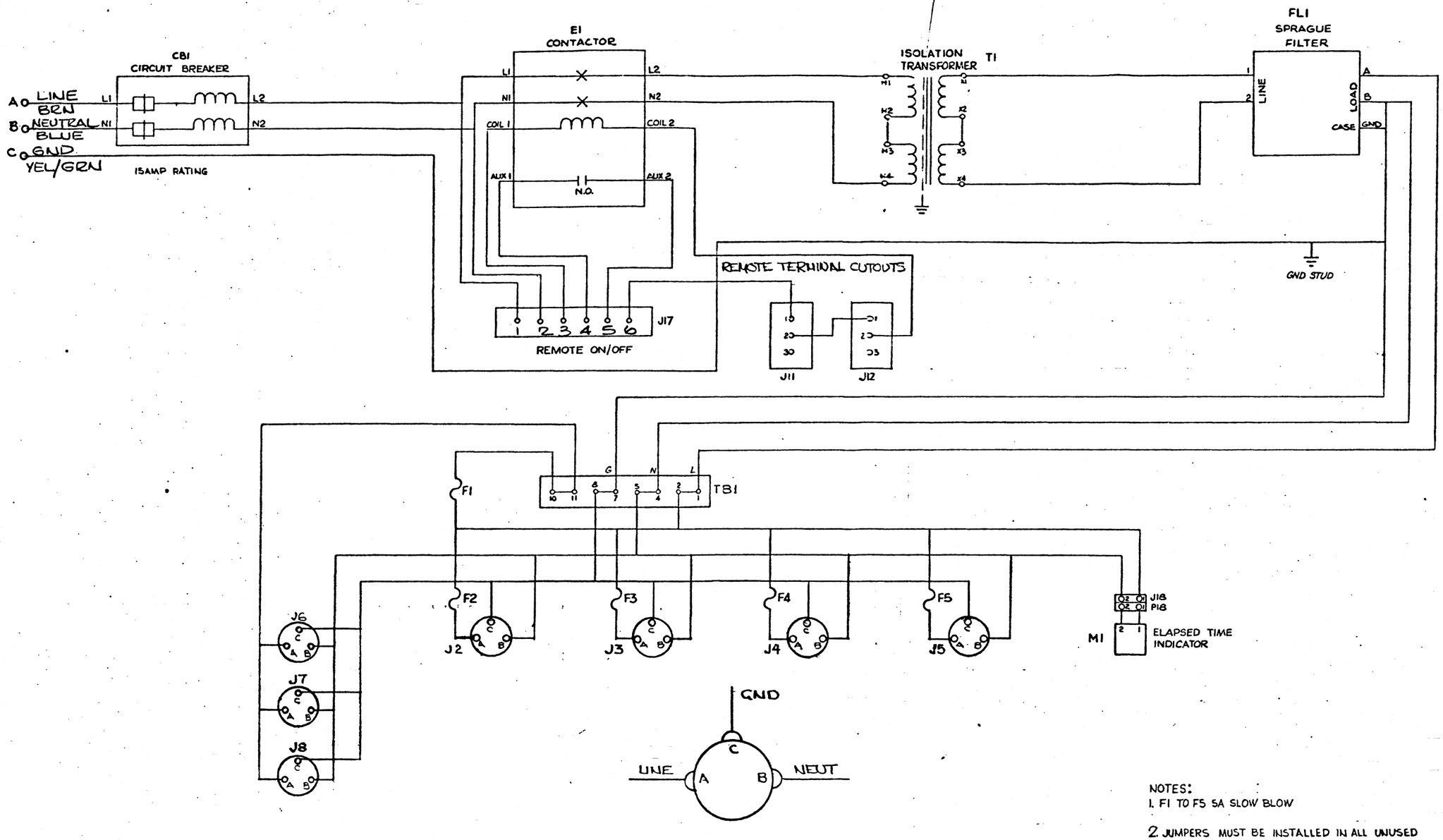
SHT 2 OF 2

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL	✓
1	SLCS11783M		1	MAIN SWITCH PANEL				
2	B11248A		1	CABLE ASSY PIT AC POWER UNIT				
				TO ON/OFF SWITCH	(SINGLE UNIT 220/240V)			



NOTES:
1. F1 TO F5 5A SLOW BLOW

2 JUMPERS MUST BE INSTALLED IN ALL UNUSED THERMAL CUTOUTS

FIGURE 6-1-2b

rev	description	by	date	chk	eng
1	PRE-PRODUCTION RELEASE	MJANTZ	FB		

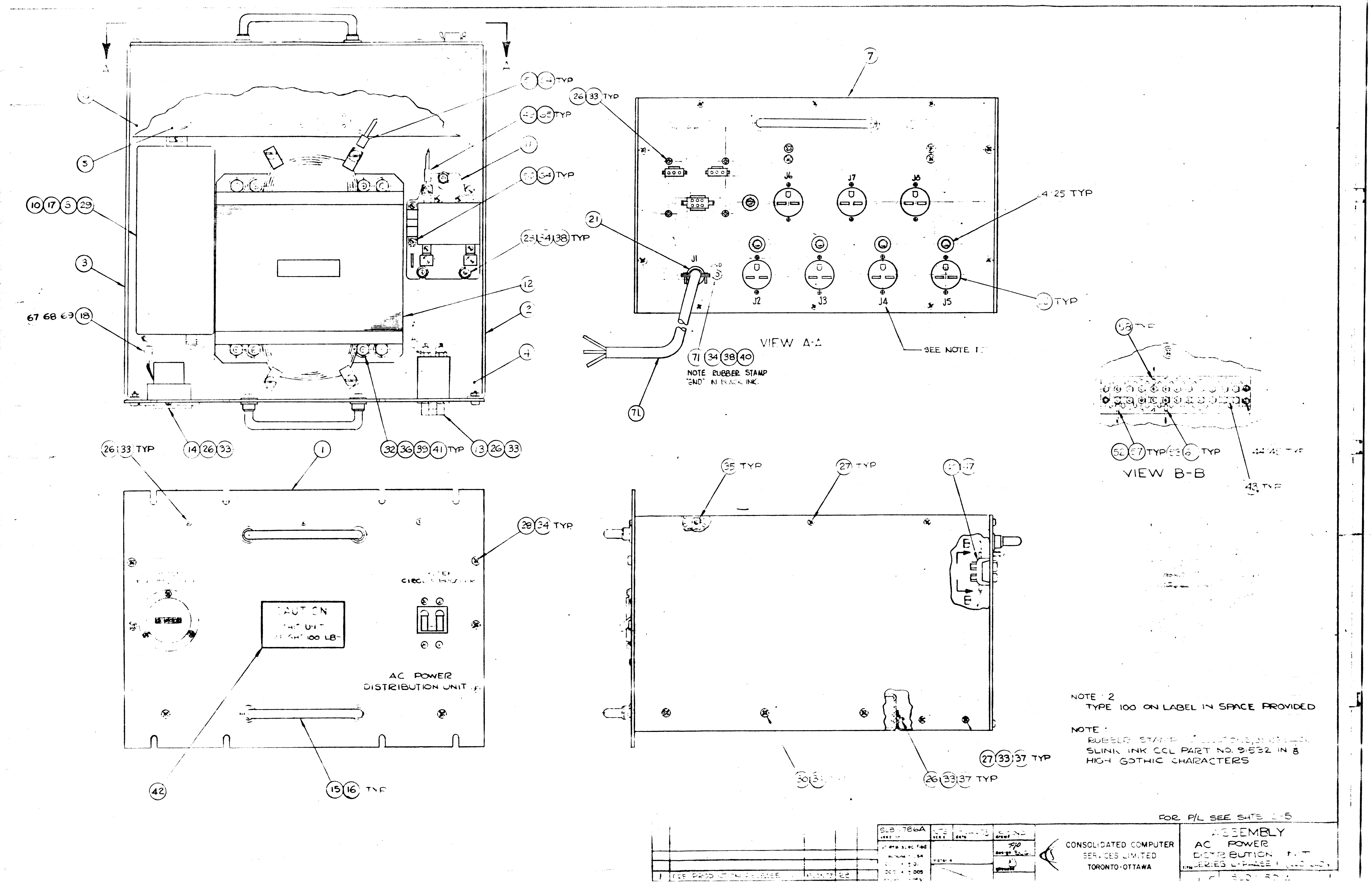
wood or	drawn KRD
scale —	date 8 JAN 79
design approv	710
checked	MJ
final approv	
material	finish

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

CONSOLIDATED COMPUTER LIMITED
OTTAWA

(225/240V)
SCHEMATIC
AC POWER DISTRIBUTION
SERIES — PHASE

size | sheet 1 of 1 | no. SL3118015 | rev 1


VIEW A-A
VIEW B-B
J1
J2
J3
J4
J5
J6
J7
J8
SEE NOTE 1
NOTE RUBBER STAMP "GND" IN BLACK INK.
CAUTION
THIS UNIT WEIGHT 100 LB
CIRCUIT BREAKER
AC POWER DISTRIBUTION UNIT
NOTE : 2
TYPE 100 ON LABEL IN SPACE PROVIDED
NOTE :
SLINK INK CCL PART NO. 91532 IN 8
HIGH GOTHIC CHARACTERS
FOR P/L SEE SHTS 2-5
SLB 1786A
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA
ASSEMBLY
AC POWER
DISTRIBUTION UNIT

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: MJ | DATE 19 JAN 73 | APPROVED BY

USED ON ASSEMBLY SLB11786A | DRAWING REV 1

ASSEMBLY NO SLD11801A | SHT 2 OF 5

TITLE: ASSEMBLY
AC POWER 220/240U
DISTRIBUTION UNIT (FOR DWG SEE SHT 1)
SERIES L - PHASE 1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	D11089M		1	FRONT PANEL			
2	D11090M/1		1	SIDE PANEL (RH)			
3	D11090M/2		1	SIDE PANEL (LH)			
4	D11092M		1	BASE			
5	D11093M		1	BOTTOM SCREEN			
6	D11094M		1	TOP SCREEN			
7	SLD11788M		1	REAR PANEL			
8	D11103MA		1	FILTER BOX & COVER			
9	SLB11790M		1	CONNECTOR PLATE			
10	91952		1	FILTER (SPRAGUE)	JN17-3715E		
11	91953		1	CONTACTOR (CUTLER HAMMER)	C10CN2A		
12	92061		1	TRANSFORMER (HAMMOND)	97536		
13	92119		1	CIRCUIT BREAKER (AIRPAX)	15A		
14	91586		1	ELAPSED TIME METER			
15	91949		3	HANDLE (HAMMOND)	C/W HARDWARE		
16	91921		6	FERRULE			
17	91956		1	OUTLET BOX CONNECTOR			
18	91937		1	CONNECTOR (AMP)	1-480319-0		
19	91939		2	CONNECTOR (AMP)	1-480304-0		
20	91940		1	CONNECTOR (AMP)	1-480273-0		
21	93214		1	CONNECTOR, TWO SCREW	THOMAS BETTS 3302		
22	93074		7	RECEPTACLE, 3 SOCKET	HUBBEL 5658		
23							

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: MJ	DATE 19 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLB11786A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLD11801A		SHT 3 OF 5	CONTROL

TITLE: ASSEMBLY AC POWER DISTRIBUTION UNIT 220/240V SERIES L - PHASE 1

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
24	90283		5	FUSE HOLDER			
25	92284		5	FUSE, 5 AMP SLO-BLO			
26	90043-24		37	SCREW, 6-32 x 3/8 LG PPH			
27	90043-25		10	SCREW, 6-32 x 1/2 LG, 100° CSK PFH			
28	90043-47		15	SCREW, 10-32 x 1/2 LG PPH			
29	90043-46		4	SCREW, 10-32 x 3/8 LG PPH			
30	90044-47		6	SCREW, 10-32 x 1/2 LG, 100° CSK PFH			
31							
32	91903		8	SCREW, CAP HEX HD 5/16-18 x 1 LG			
33	91202		35	NUT, KEP 6-32			
34	91301		23	NUT, KEP 10-32			
35	91574		12	NUT, CLIP FLOATING (ESNA)			
36	91904		8	NUT, HEX 5/16-18			
37	90122		7	WASHER, FLAT NO. 6			
38	90124		4	WASHER, FLAT NO. 10			
39	91905		8	WASHER, FLAT 5/16 DIA			
40	91448		1	WASHER, STAR NO. 10			
41	91368		8	WASHER, LOCK 5/16 DIA			
42	BS11069M		1	LABEL, WARNING			
43	91948		4	JUMPER, (CINCH JONES)	142J-1		
44	90043-37		4	SCREW, 8-32 x 5/8 LG PPH			
45	91493		4	NUT, KEP 8-32			
46	91957		1	TERMINAL BLOCK, (KULKA)	602C-2202-11		

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: M | DATE: 19 JAN 73 | APPROVED BY:

USED ON ASSEMBLY: SLB11786A | DRAWING REV: 1

ASSEMBLY NO: SLD11801A | SHT 4 OF 5

TITLE: ASSEMBLY AC POWER 220/240V DISTRIBUTION UNIT SERIES L - PHASE 1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
47	91947		1	MARKER STRIP (KULKA)	MS602-11XP-7E		
48	91114		11	TERMINAL RING			
49	91936		11	TERMINAL RING			
50	91110		3	TERMINAL RING			
51	91400		12	TERMINAL RING			
52	91924		18	TERMINAL RING			
53	90932		14	TERMINAL RING			
54	90600-0		80"	WIRE, 10 AWG BLK			
55	90600-9		56"	WIRE, 10 AWG WHT			
56	90600-5		54"	WIRE, 10 AWG GRN			
57	90601-0		46"	WIRE, 12 AWG BLK			
58	90601-9		35"	WIRE, 12 AWG WHT			
59	90601-5		29"	WIRE, 12 AWG GRN			
60	90603-0		22"	WIRE, 16 AWG BLK			
61	90603-9		31"	WIRE, 16 AWG WHT			
62	90603-5		16"	WIRE, 16 AWG GRN			
63	90604-0		31"	WIRE, 18 AWG BLK			
64	90604-2		53"	WIRE, 18 AWG RED			
65	90604-9		18"	WIRE, 18 AWG WHT			
66	90604-5		18"	WIRE, 18 AWG GRN			
67	91938		1	CONNECTOR, HOUSING (AMP)	1-480318-0		
68	91744		2	CONNECTOR PIN (AMP)	60620-1		
69	91745		26	CONNECTOR SOCKET (AMP)	60619-1		

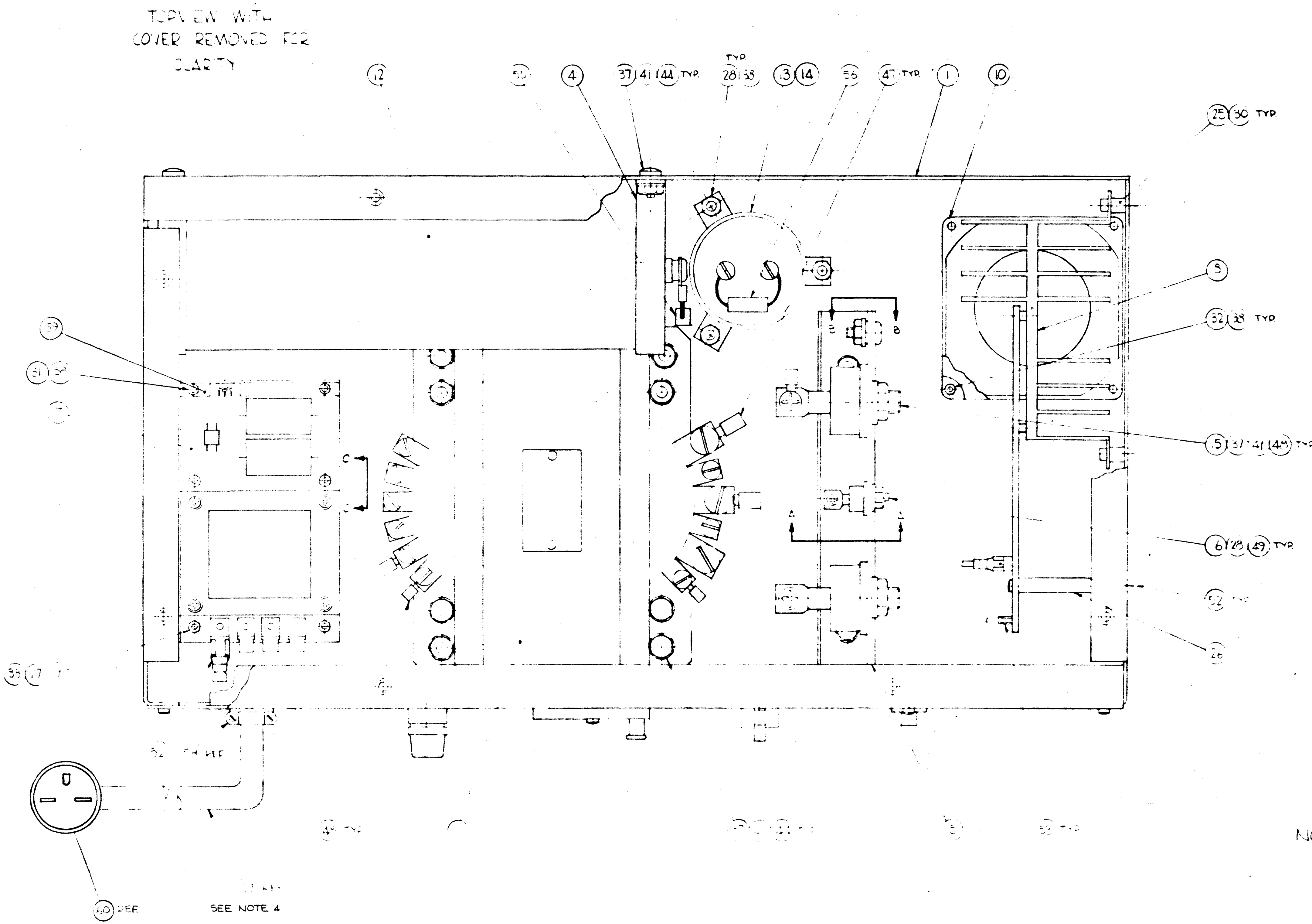
CONSOLIDATED COMPUTER INCORPORATED

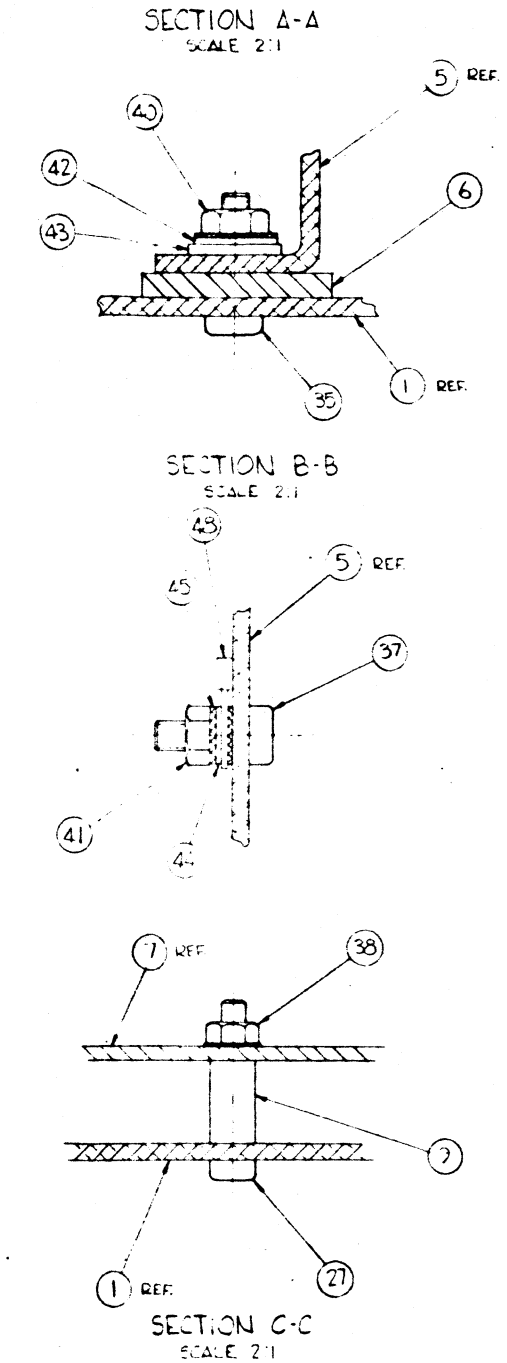
ASSEMBLY PARTS LIST

COMPILED BY: MJ	DATE 19 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLB11786A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLD11801A		SHT 5 OF 5	CONTROL

TITLE: ASSEMBLY AC POWER 220/240V DISTRIBUTION UNIT SERIES L-PHASE 1

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
70	90043-40		1	SCREW 10-32 x 3/4 LG PPH			
71	91369		*	CORD 3W EUROPEAN COLOR CODING	(REF. B11249A)		
			*	15'-0 MAX.			





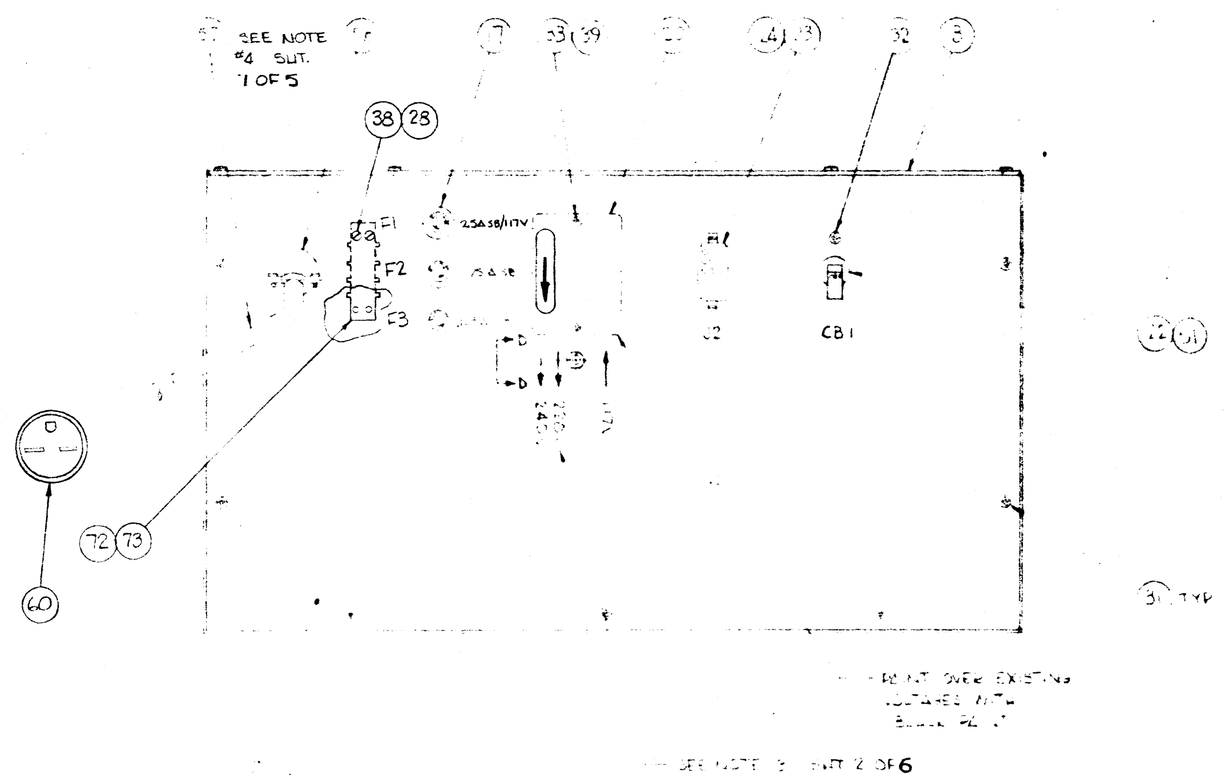
NOTE:

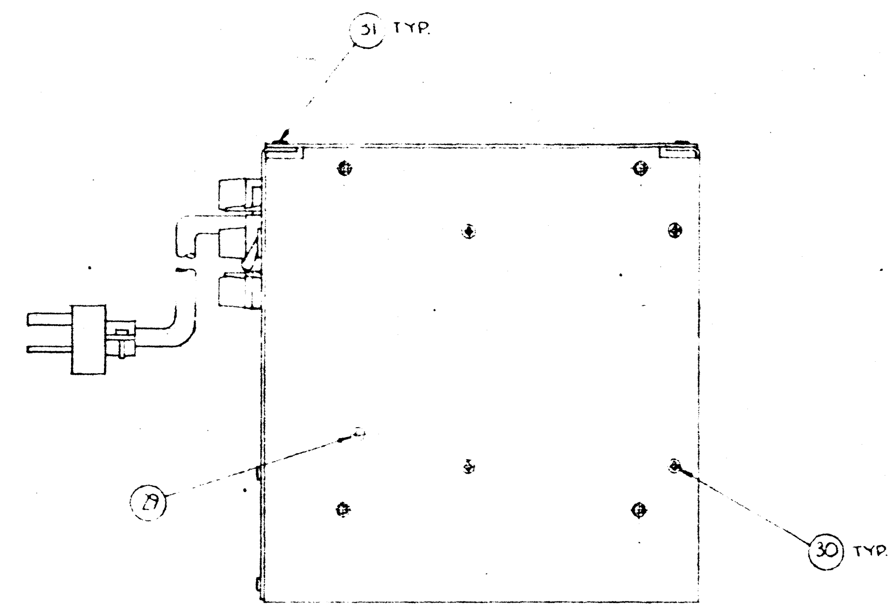
1. TORQUE ON ITEM 15 TO BE 25 LB. IN MIN. 30 LB. IN MAX
2. HEAT SINK COMPOUND ON ALL DIODES
3. CHARACTERS TO BE IN BLACK APPROXIMATE SIZE AND LOCATION SHOWN, USING LETRASET OR/AND RUBBER STAMPING
4. CABLE MUST PROTUDE OUT OF SUPPLY THE MIN. OF 4 FT.

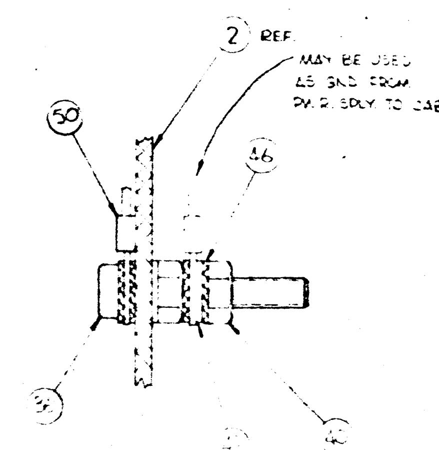
FOR PART LIST SEE SHT. 3 OF 6

ELD11807A (used on)	R. Boyd (drawn)	CONSOLIDATED COMPUTER INC. OTTAWA	ASSEMBLY SERIES L - PHASE I POWER SUPPLY (220/240 VAC) (title)
1-1 (scale) / 4 JAN 73 (date)	(design)		
unless specified ... fraction ± 1/64	(checked)		

FOR PRODUCTION RELEASE







SECTION D-D
SCALE 4:1

1	PRE-PRODUCTION RELEASE	4 JAN 73	RB

used on: SLD11807A	drawn: R. BOYD	CONSOLIDATED COMPUTER INC. OTTAWA	ASSEMBLY SERIES L - PHASE I POWER SUPPLY (220/240 VAC)
date: 4 JAN 73			
unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles ± 0°30'	checked		2 6 SLD11805A

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: R BOYD	DATE 4 JAN 72	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLD 11807A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLD 11805A		SHT 3 OF 6	CONTROL

TITLE: ASSEMBLY
SERIES L - PHASE I POWER SUPPLY
(220/240 VAC)
FOR DWG SEE SHT. 1 OF 6 & 2 OF 6

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLD 11808MA		1	BASE			
2	SLD11809M		1	REAR PANEL			
3	SLD11810M		1	COVER			
4	B11065M		2	CAPACITOR HOLDING BRACKET			
5	B11062M		1	HEAT SINK			
6	B11063M		1	INSULATION PAD			
7	C11766A		1	ASSY. POWER SUPPLY 5V 1A			
8	11[illegible]6A		1	PCB LOGIC RACK REGULATOR			
9	B910214M/½		4	SPACER			
10	91485		1	FAN	(SPRITE NO. SP2A3 220/240V)		
11	91762		1	TRANSFORMER (HAMMOND)	95622		
12	91765		1	CAPACITOR ELECTOLYTIC 260,000 uf	c/w HARDWARE		
13	91760		1	CAPACITOR ELECTOLYTIC 26000 uf	c/w HARDWARE		
13	91766		1	CAPACITOR ELECTOLYTIC 27000 uf	c/w HARDWARE		
14	91836		1	CAPACITOR CLAMP (MALLORY)	VR8		
15	11799		2	DIODE RECTIFIER MR 1810 SLR	c/w HARDWARE		
16	91755		2	DIODE RECTIFIER IN3208R	c/w HARDWARE		
17	90283		3	FUSE HOLDER	c/w HARDWARE		
18	91886		1	FUSE, 2.5 AMP. SLO BLO	F1		
19	90299		2	FUSE .125 AMP SLO BLO	F2, F3		
20	91759		1	VOLTAGE SELECTOR (McMURDO)	B 279002/A		
21							
—							

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY	DATE	APPROVED BY
R BOYD	4 JAN 73	

USED ON ASSEMBLY: SLD 11807A

DRAWING REV: 1

ASSEMBLY NO: SLD11805A

SHT 4 OF 6

TITLE: ASSEMBLY
SERIES L PHASE I, POWER SUPPLY
(220/240 VAC)

FOR DWG. SEE SHT 1 OF 6 & 2 OF 6

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
22	91746		1	BREAKER (AIRPAX)	AP6-6-1 REC 2-5-1-20?		
23	91743		1	HOUSING SOCKET MATE-N-LOK	AMP 1-480323-0		
24	93029		15	PIN CONTACT SOCKET MATE N-LOK	AMP 61117-1		
25	91758		4	NYLON SPACER			
26	91901		1	STANDOFF HEX $\frac{1}{4}$ X 1 $\frac{3}{4}$ LG X 6-32	NYLON		
27	90043-28		4	SCREW, 6-32 UNC X 1 LG. PPH.			
28	90043-25		9	SCREW, 6-32 UNC X $\frac{1}{4}$ LG PPH			
29	90040-24		1	SCREW. 6-32 UNC X $\frac{3}{8}$ LG X 100° PFH			
30	93182-1		4	SCREW, #8 SELF TAPPING X $\frac{3}{4}$ PPH	SPAX NAUR ST 532P		
31	90043-23		17	SCREW, 6-32 UNC X $\frac{3}{16}$ PPH			
32	90041-24		5	SCREW, 6-32 UNC X $\frac{3}{8}$ LG PPH			
33	90043-13		2	SCREW, 4-40 X $\frac{3}{8}$ LG. PPH			
34							
35	90043-37		2	SCREW, 8-32 UNC X $\frac{5}{8}$ PPH			
36	90043-39		1	SCREW, 8-32 X 1 LG PPH.			
37	90043-47		16	SCREW, 10-32 X $\frac{1}{2}$ PPH			
38	91202		17	NUT KEP 6-32			
39	90767		2	NUT KEP 4-40			
40	91493		4	NUT KEP 8-32			
41	91301		16	NUT KEP 10-32			
42	90123		4	WASHER FLAT NO. 10			
43	91652		2	WASHER, EXTRUDED FIBRE NO. 8	SPAE NAUR W-76 F		
44	90124		4	WASHER FLAT NO. 10			

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: R Boyd	DATE 3 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLD 11807A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLD11805A		SHT 5 OF 6	CONTROL

TITLE: ASSEMBLY
SERIES L - PHASE I, POWER SUPPLY
(220/240 VAC)
FOR DWG. SEE SHT 1 OF 6 & 2 OF 6

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
45	91443		4	WASHER, STAR NO 10	EXTERNAL TOOTH		
46	91510		3	WASHER, STAR NO 8	EXTERNAL TOOTH		
47	91400		3	TERMINAL RING ¼ DIA.			
48	91112		13	TERMINAL RING NO. 10			
49	91111		2	TERMINAL RING NO. 6			
50	90932		3	TERMINAL RING NO. 8			
51	91114			TERMINAL RING NO. 10			
52	11760		1M	RECEPTACLE 250 SERIES			
53	91316		4	RECEPTACLE 110 SERIES			
54	90191		15	CABLE TIES			
55	90433-26		1	RESISTOR 100Ω 5 WATT			
56	90483-31		1	RESISTOR 220Ω 5 WATT			
57	91588		5 FT	CABLE 3W 18 AWG.			
58	93214		1	CONNECTOR 2 SCREW ⅜ (THOMAS BETTS #3302)	C/W HARDWARE.		
59	B11483M		1	HEAT SINK			
60	92216		1	PLUG RUBBER CAP (HUBBELL #5666)	220/240 VAC		
61	90600-2			WIRE, 10 AWG. RED			
62	90603-2			WIRE, 16 AWG. RED			
63	90603-0			WIRE, 16 AWG. BLK.			
64	90603-6			WIRE, 16 AWG. BLU.			
65	90603-5			WIRE, 16 AWG GRN.			
66	90603-7			WIRE, 16 AWG. VIO.			
67	90603-9			WIRE, 16 AWG WHT.			

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: R Boyd	DATE 5 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLD11807A		DRAWING REV 1	DATE ISSUED
ASSEMBLY NO SLD11805A		SHT 6 OF 6	CONTROL

TITLE: ASSEMBLY
SERIES L- PHASE I, POWER SUPPLY
(220/240 VAC)
FOR DWG. SEE SHT. 1 OF 6 & 2 OF 6

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
68	90604-0			WIRE, 18 AWG. BLK			
69	90604-9			WIRE, 18 AWG. WHT.			
70	90605-2			WIRE, 20 AWG. RED			
71	90605-0			WIRE.. 20 AWG. BLK			
72	93211		1	TERMINAL BLOCK (KULKA)	(SERIES 600A)		
73	93212		1	MARKER STRIP	MS6004-3-XP		
REF.	SLD11805A			SCHEMATIC			
REF.	SLD11805W			WIRING			

RACK A

1	2	3	4	5	6	7	8	9	10 A	10 B	11 A	11 B	12 A	12 B	13 A	13 B	14	15	16	17	18	19	20	21	22 A	22 B	23 A	23 B	24	25	26 A	26 B
																		Out put of ALU														
																		1	2													
								10185 POWER FAIL PROTECT	10349 REAL TIME CLOCK				10495 LINE PRINTER INTERFACE 11214				10391-1 FEEDTHRU (AC BUS)	10391-2 FEEDTHRU (DB ADD)	10391-3 FEEDTHRU (DB DATA)	10391-4 FEEDTHRU (BMB BUS)	10391-5 FEEDTHRU (BAC BUS)	10368(7TK) MTT READ CHECK 10246(9TK) 10445(1600BPI) MTT STATUS	10285(7TK&9TK) 10444(1600CPI) MTT CONTROL	10366(7TK) 10365(9TK) 10443(1600BPI) MTT DATA	11730 DRUM MTT & VCU MULTIPLEXOR		10442 WC & CA		10282 11254 DRUM CONTROL DISC CONTROL	10284 11255 DRUM DATA DISC DATA	10262 DERANDOMIZER	

SHEETS 14 TO 28 'C SIZE'

rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

SLD11806A & SLD11807A used on | R. Boyd drawn | scale | 3 JAN 73 date | design ENG. | checked | unless specified .00 = ±.01 fractions ± 1/64 .000 = ±.005 angles = ±0 30' | tool approvl | material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

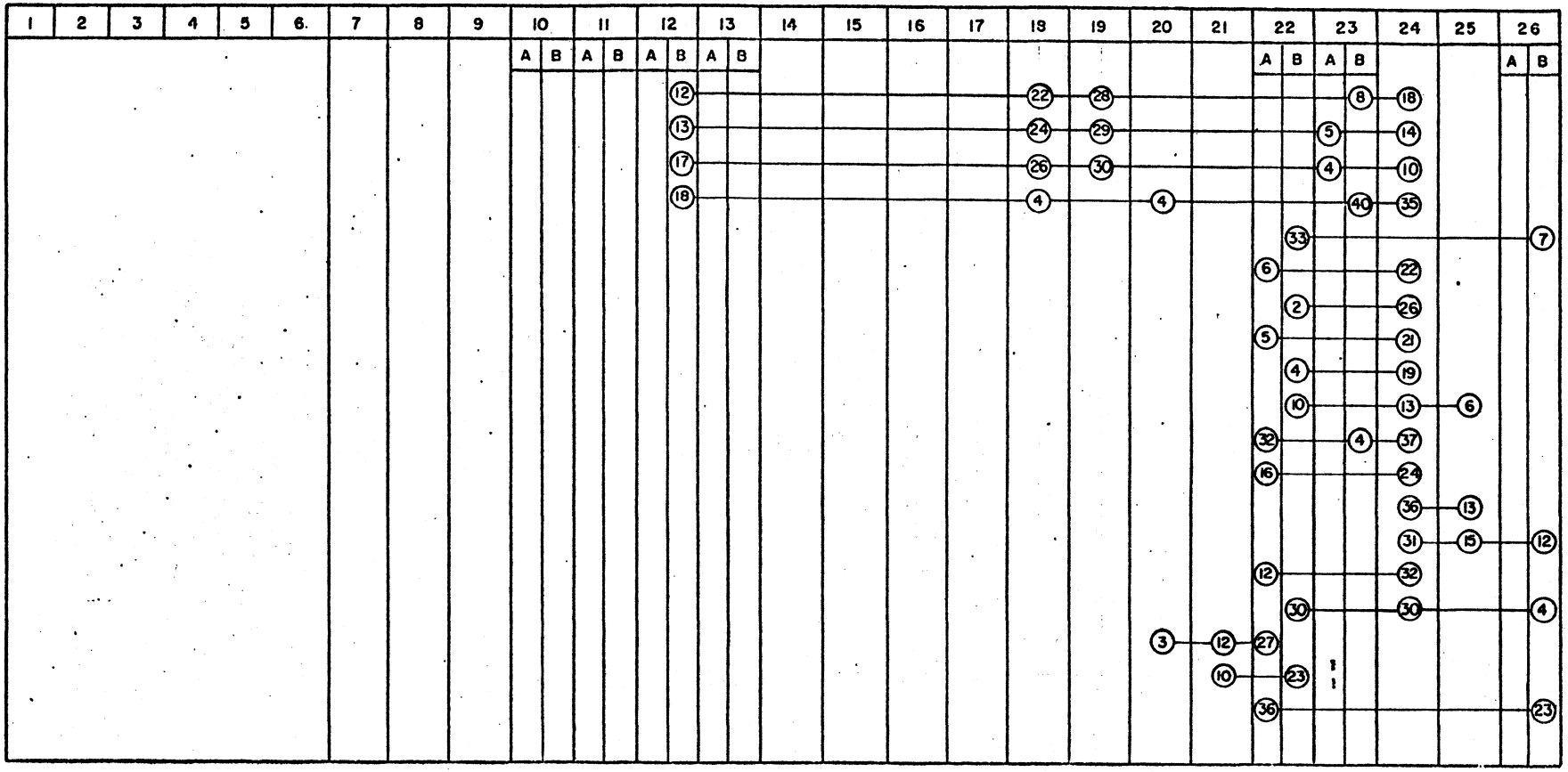
title | sheet 1 of 28 | no. SLD11806W | 1 rev

4 | 3 | 2 | 1

B

A

RACK A



rev	con	description	date	by	chk	approved
1		PRE PRODUCTION RELEASE	3JAN73	RB		

SLD11806A & SLD11807A — used on

3 JAN 73 — scale / date

R. BOYD — drawn

110 — design ENG

unless specified
00 = ±.01 fraction ± 1/64
000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

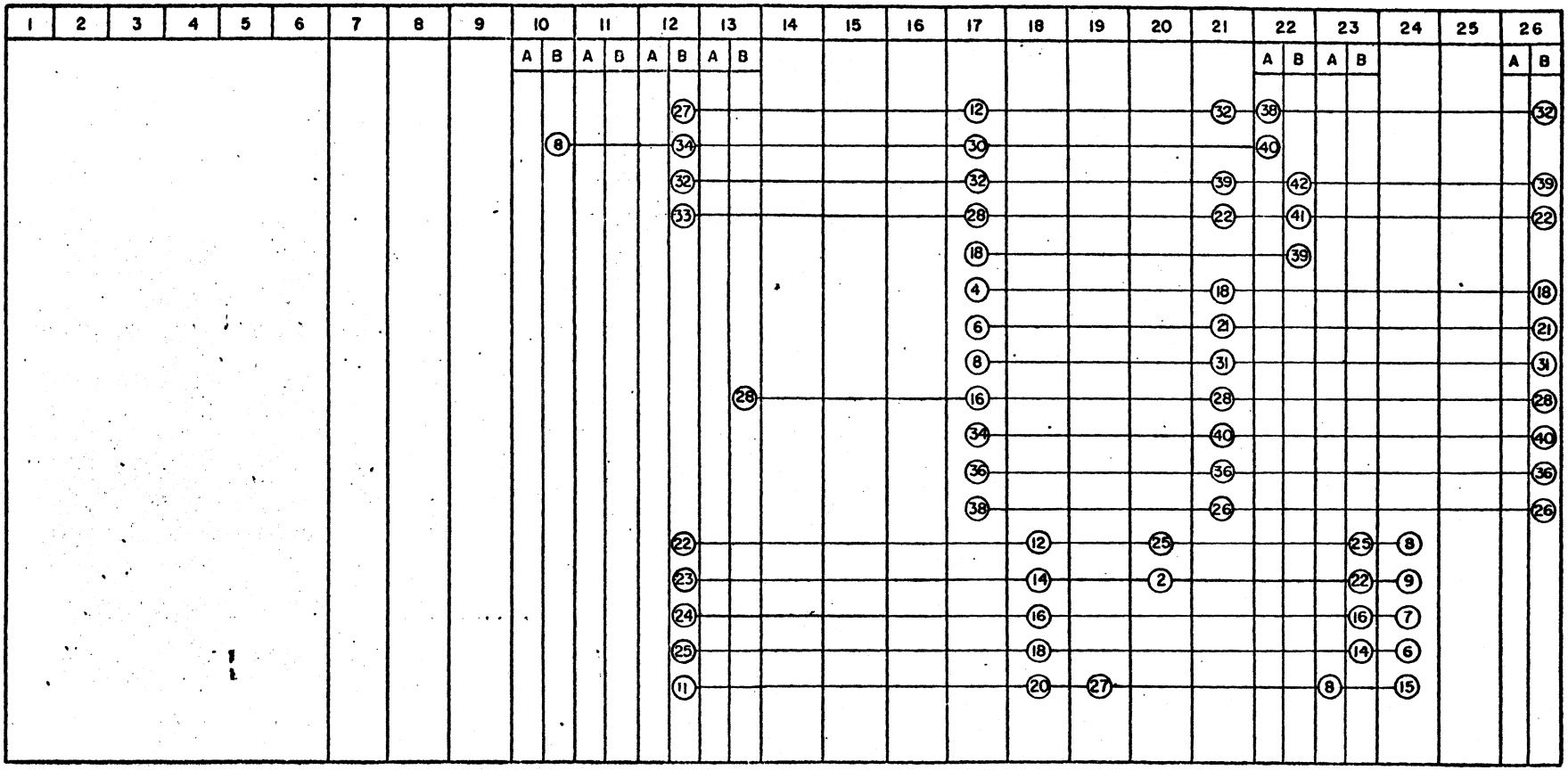
material / finish

BACK PLANE WIRING
SERIES L-PHASE I
LOGIC RACK

title

sheet 2 of 2 | no. SLB11806W | 1

RACK A



rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3JAN73	RB		

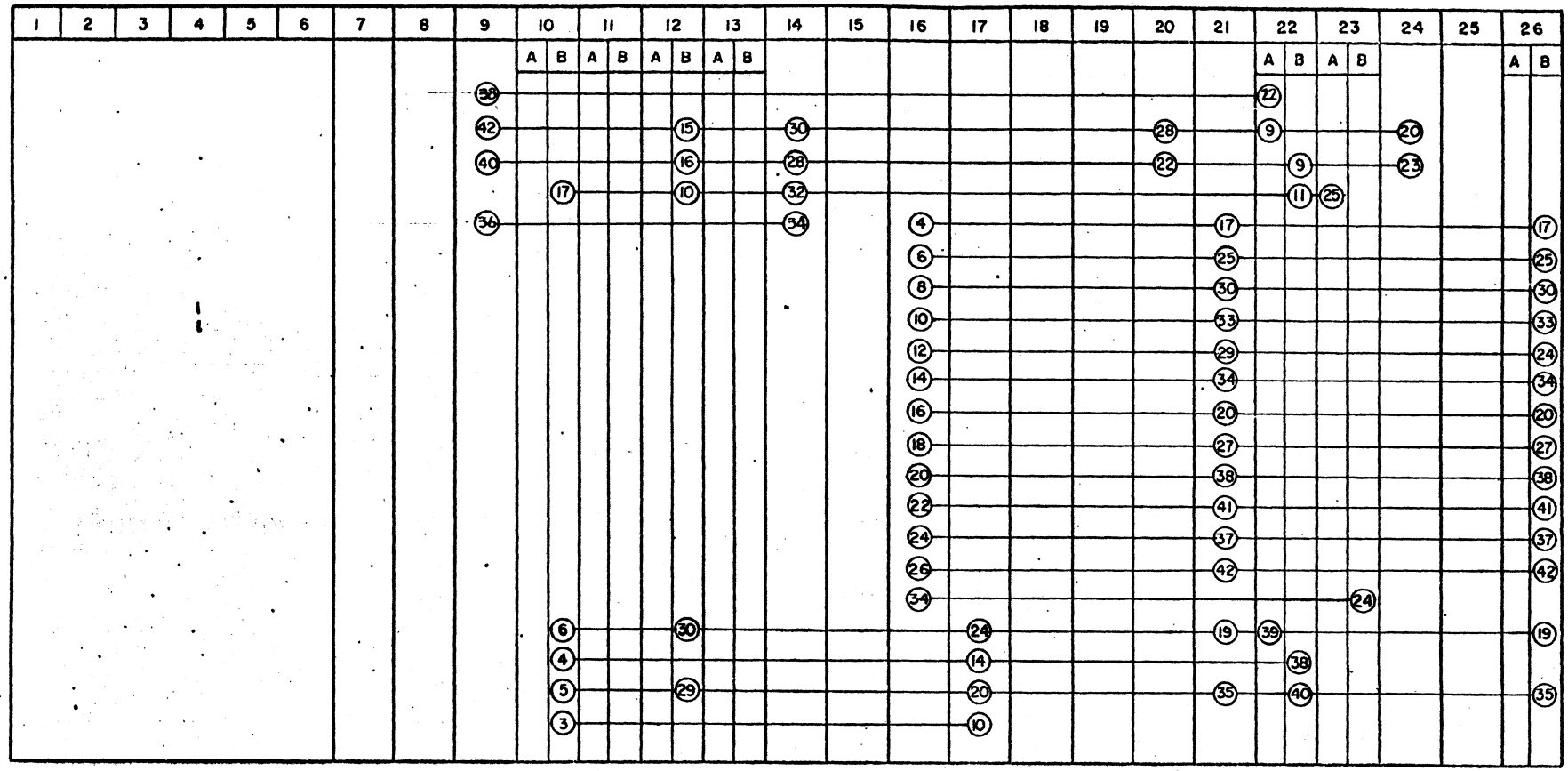
used on: SLD11806A & SLD11807A
scale:
date: 3 JAN 73
drawn: R. BOYD
design: ENG.
ch:
unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0 30'
1st appvl:
material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

sheet 3 of 20
no. SLB11806W
rev 1

RACK A



rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

used on: SLD11806A & SLD11807A
scale: | date: 3 JAN 73
drawn: R Boyd
design: ENG.
checked:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material | finish

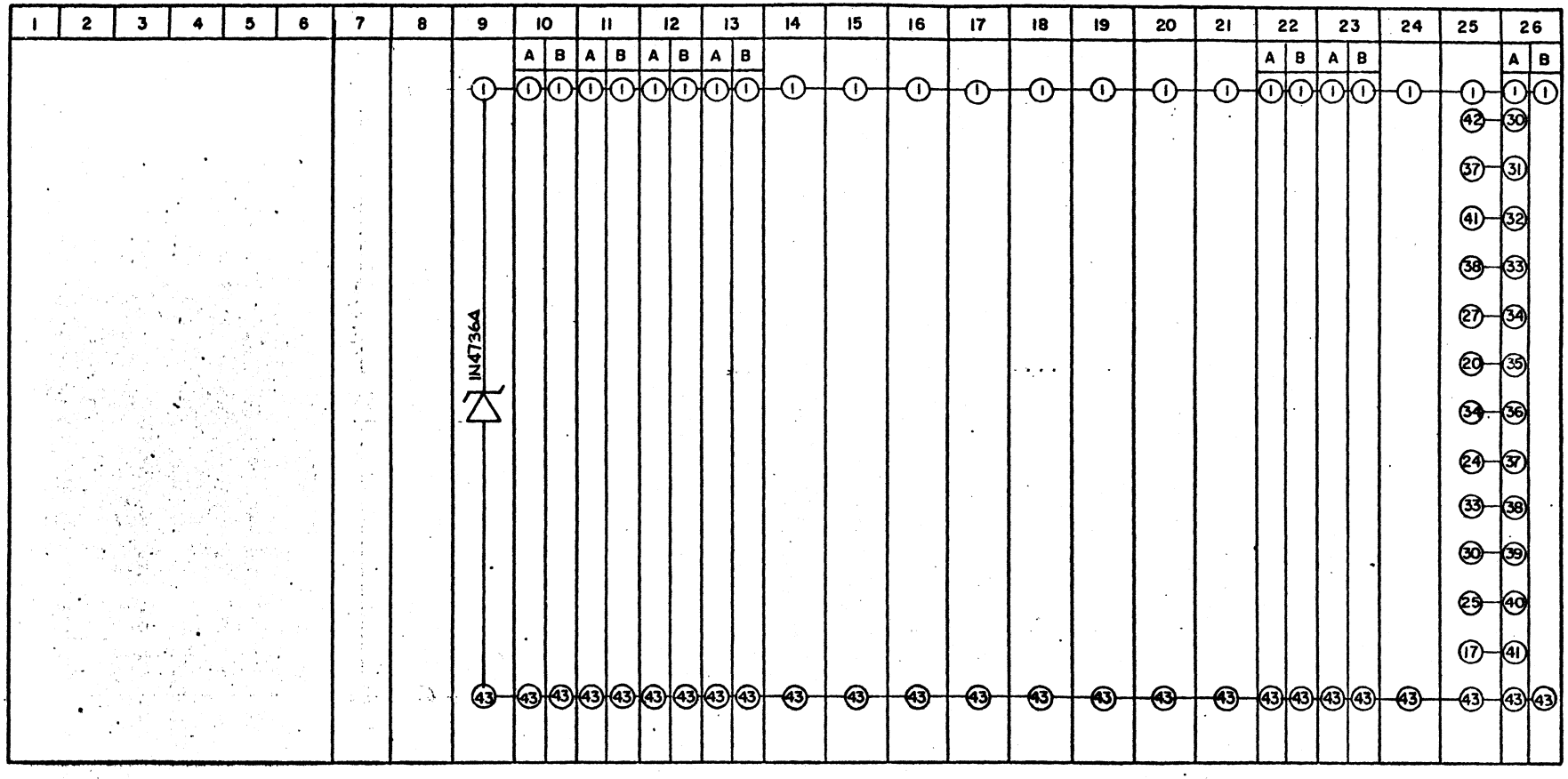
CONSOLIDATED COMPUTER INC.
OTTAWA

title: BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

SLD11806W

sheet 4 of 22 | rev 1

RACK A



eng	description	date	by	chk	approved
	PRE PRODUCTION RELEASE	3 JAN 73	RB		

used on	3LD11806A & 3LD11807A
scale	
date	3 JAN 73
drawn	R. Boyd
design	ENG
checked	
tipping	
material	
finish	

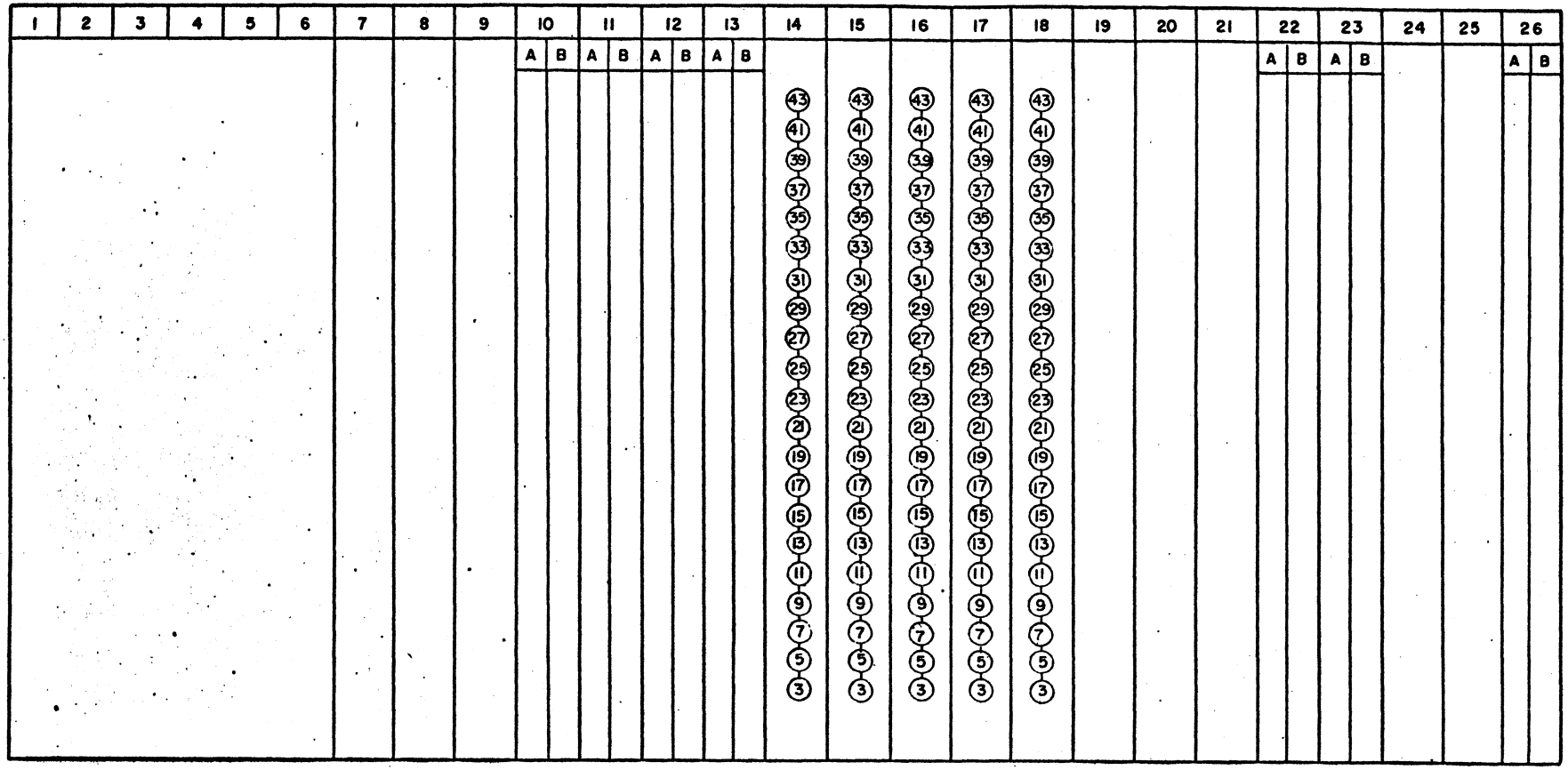
unless specified
00 = ±.01 fraction ± 1/64
000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER INC.
OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

sheet 5 of 29 | no. SLB11806W | rev 1

RACK A



rev	eco	description	date	by	chk	apprvd
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

used on: SLD11806A & SLD11807A
drawn: R. Boyd
scale: 3 JAN 73 (date)
design: ENG
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles = ± 0 30'
checked:
final apprvl:
material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L PHASE I LOGIC RACK

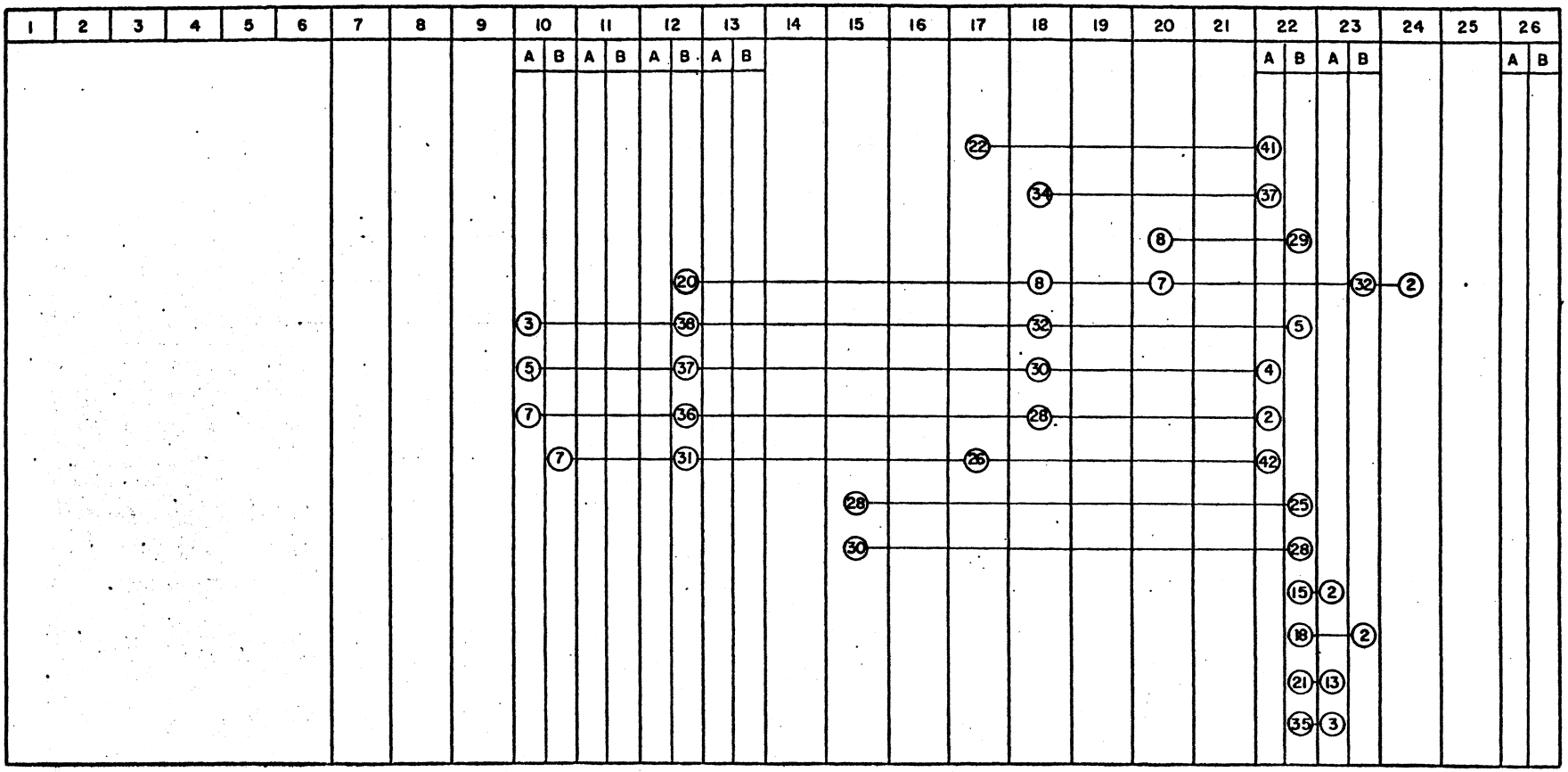
sheet 6 of 28 | no. SLB11806W | 1 rev

4 3 2 1

B

A

RACK A



1	PRE PRODUCTION RELEASE	5JAN73	RB	

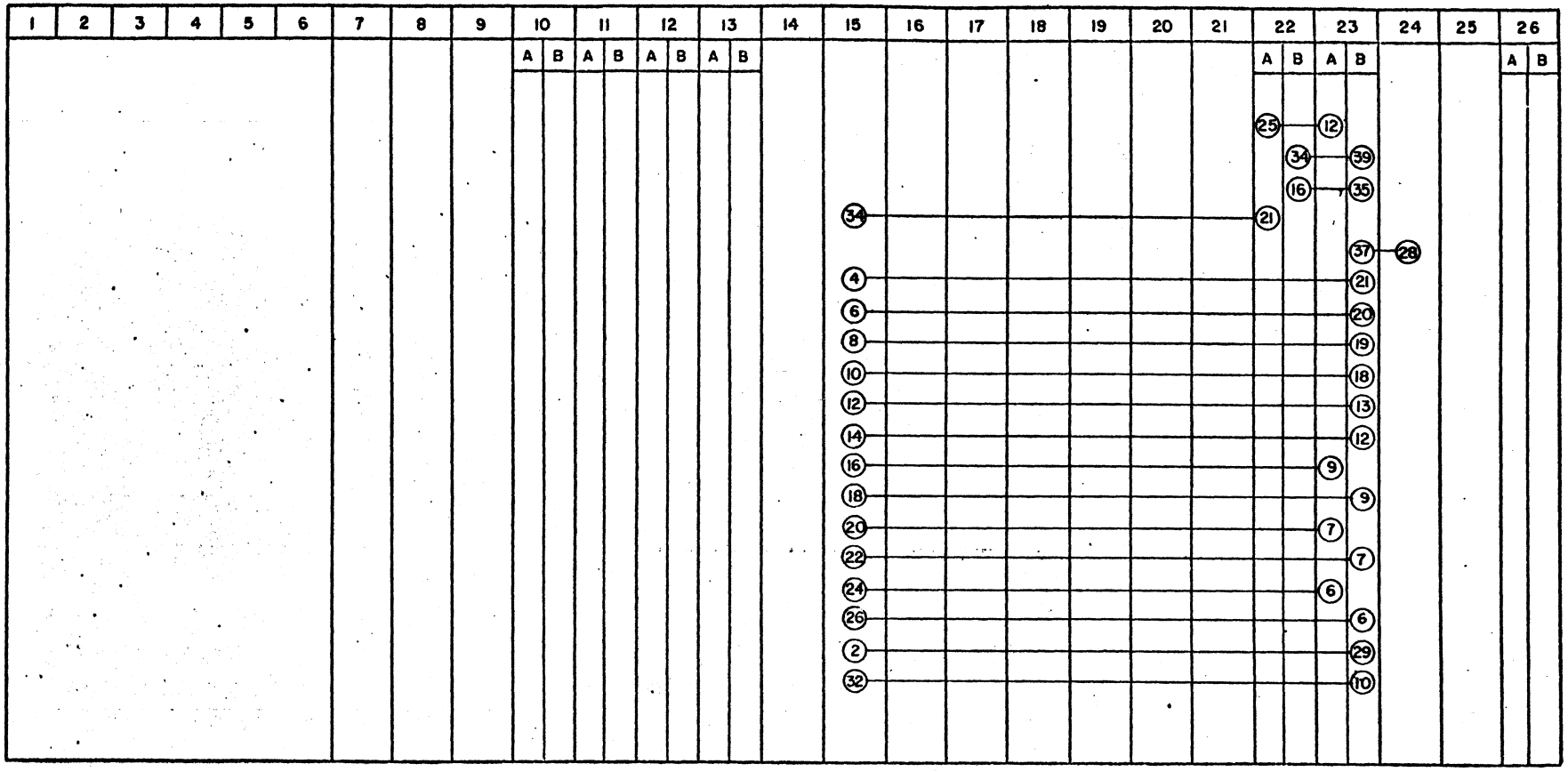
used on: SLD11806A & SLD11807A
drawn: R. BOYD
scale / date: 3 JAN 73
design ENG:
check:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material / finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L-PHASE I LOGIC RACK

SLB11806W | 1

RACK A



rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3 JAN 72	RB		

used on	SLD11806A & SLD11807A
drawn	R. Boyd
scale	
date	3 JAN 73
design ENG.	
checked	
material	
finish	

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

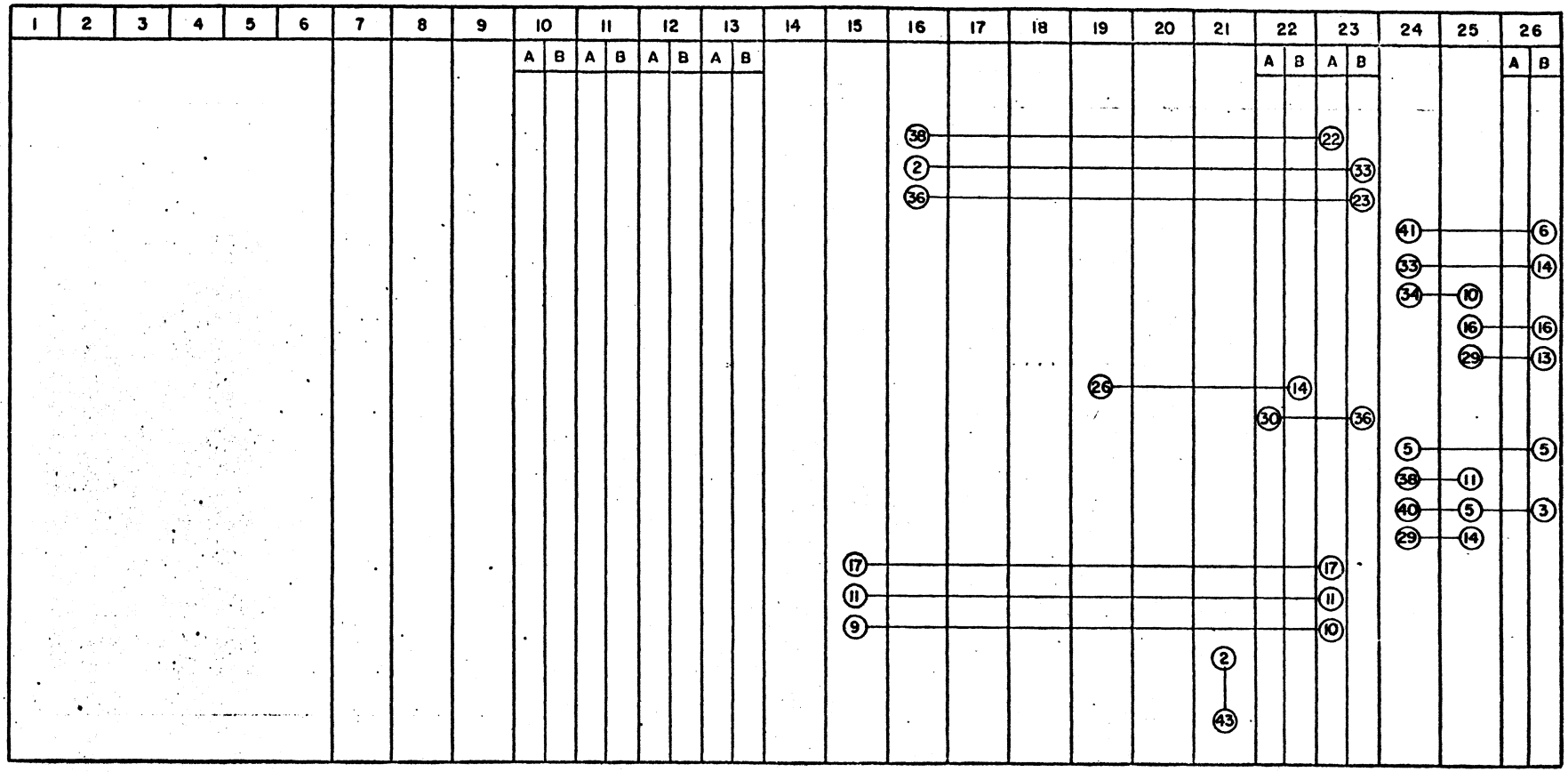
CONSOLIDATED COMPUTER INC.
OTTAWA

title: BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

sheet 8 of 28 | no. SLB11806W | rev 1

4 3 2 1

RACK A



B

A

rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

used on: SLD118064 & SLD118074

scale | date: 3 JAN 73

unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0 30'

drawn: R. BOYD

design: ENG

checked:

final accept:

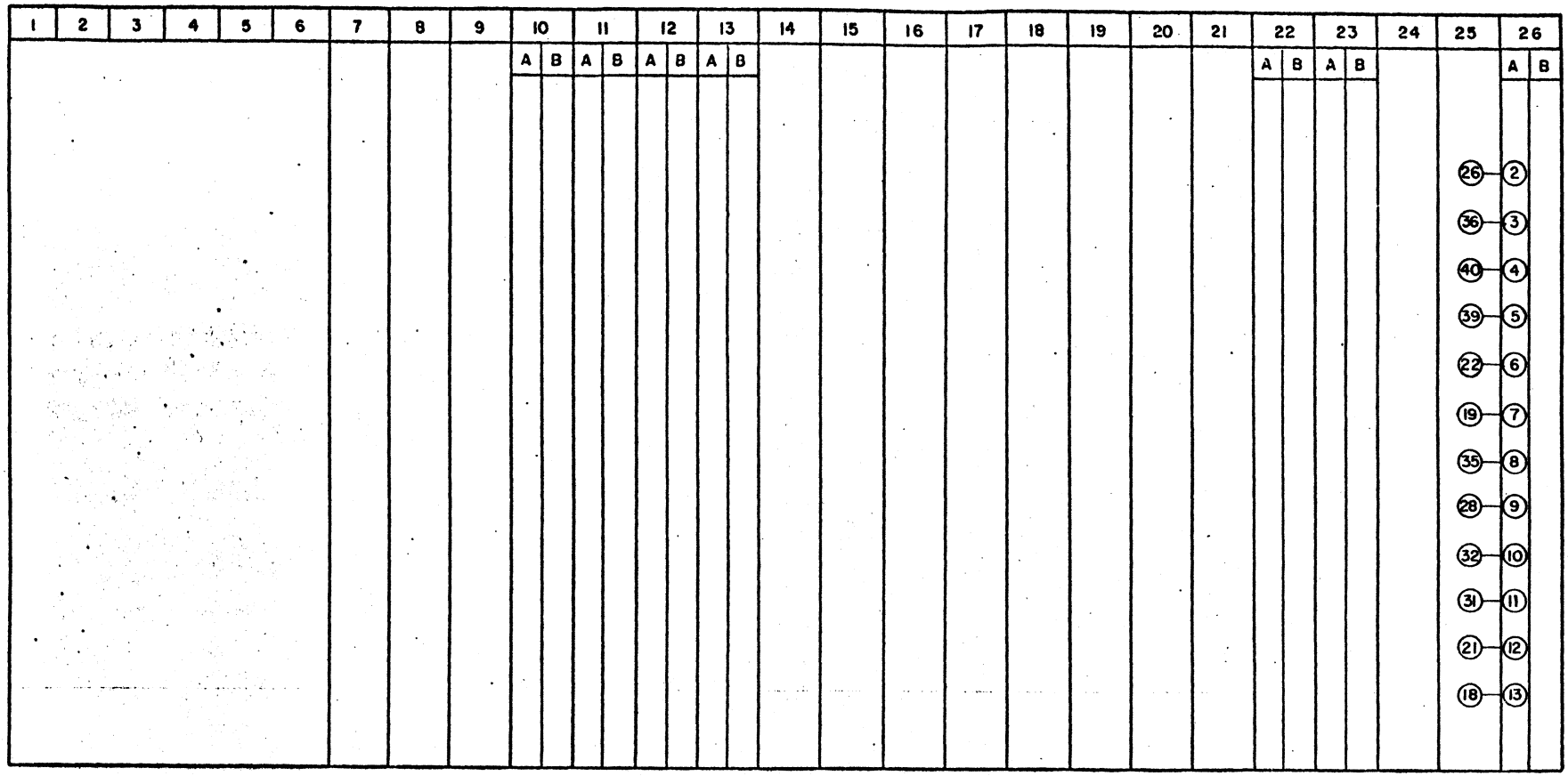
material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

sheet 9 of 28 | no. SLB11806W | rev 1

RACK A



	description	date	by	chk	apprvd
	PRE PRODUCTION RELEASE	3 JAN 73	RB		

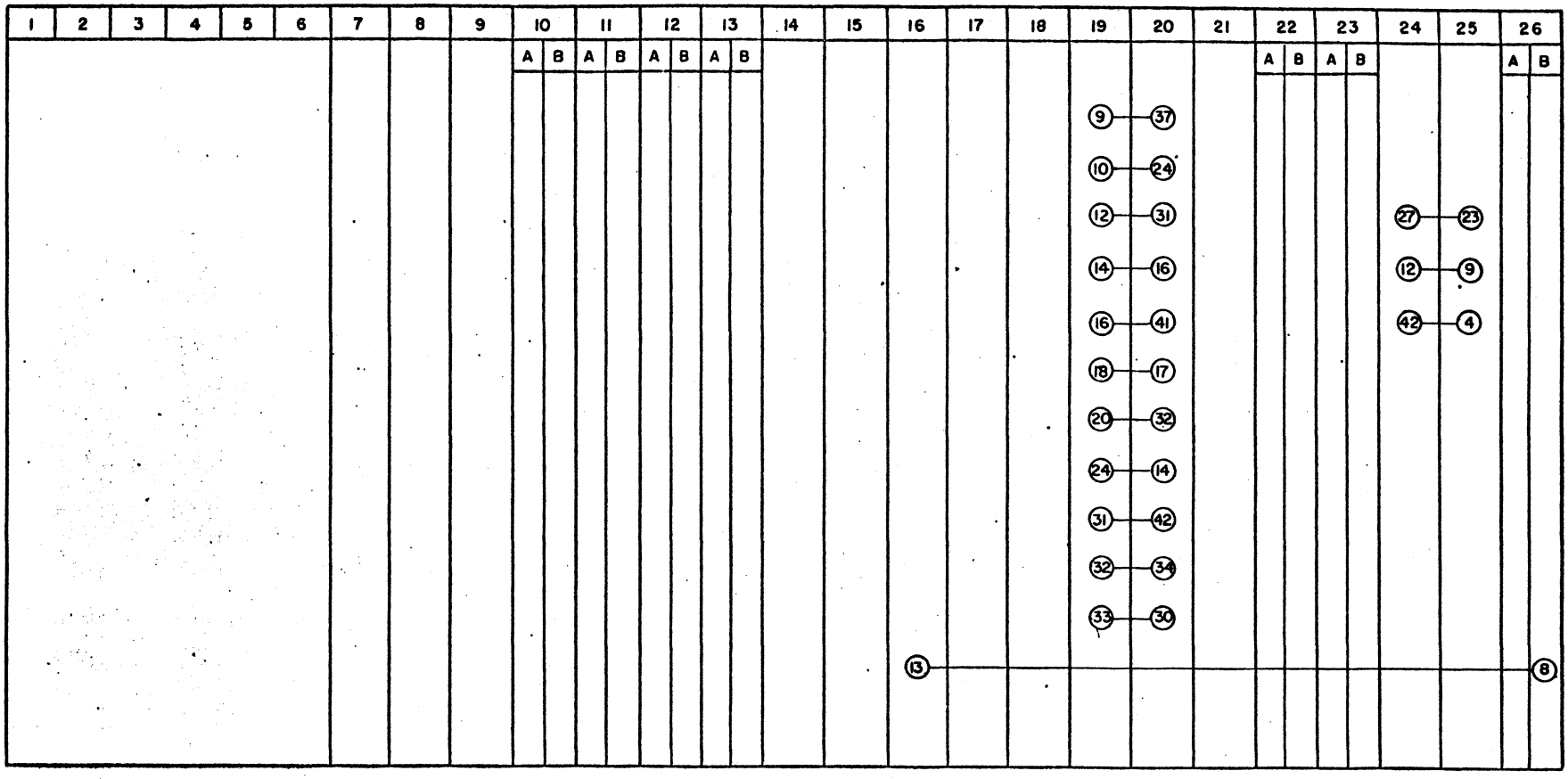
used on: SLD11806A & SLD11807A
drawn: R. Boyd
scale:
date: 3 JAN 73
design ENG:
chk:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
final apprvl:
material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

sheet 10 of 28 | no. SLB11806W | rev 1

RACK A



rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	3JAN73	RB		

SLD11806A & SLD11807A — used on
3 JAN 73 — date
R BOYD — drawn
ENG — design
unless specified
00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material
finish

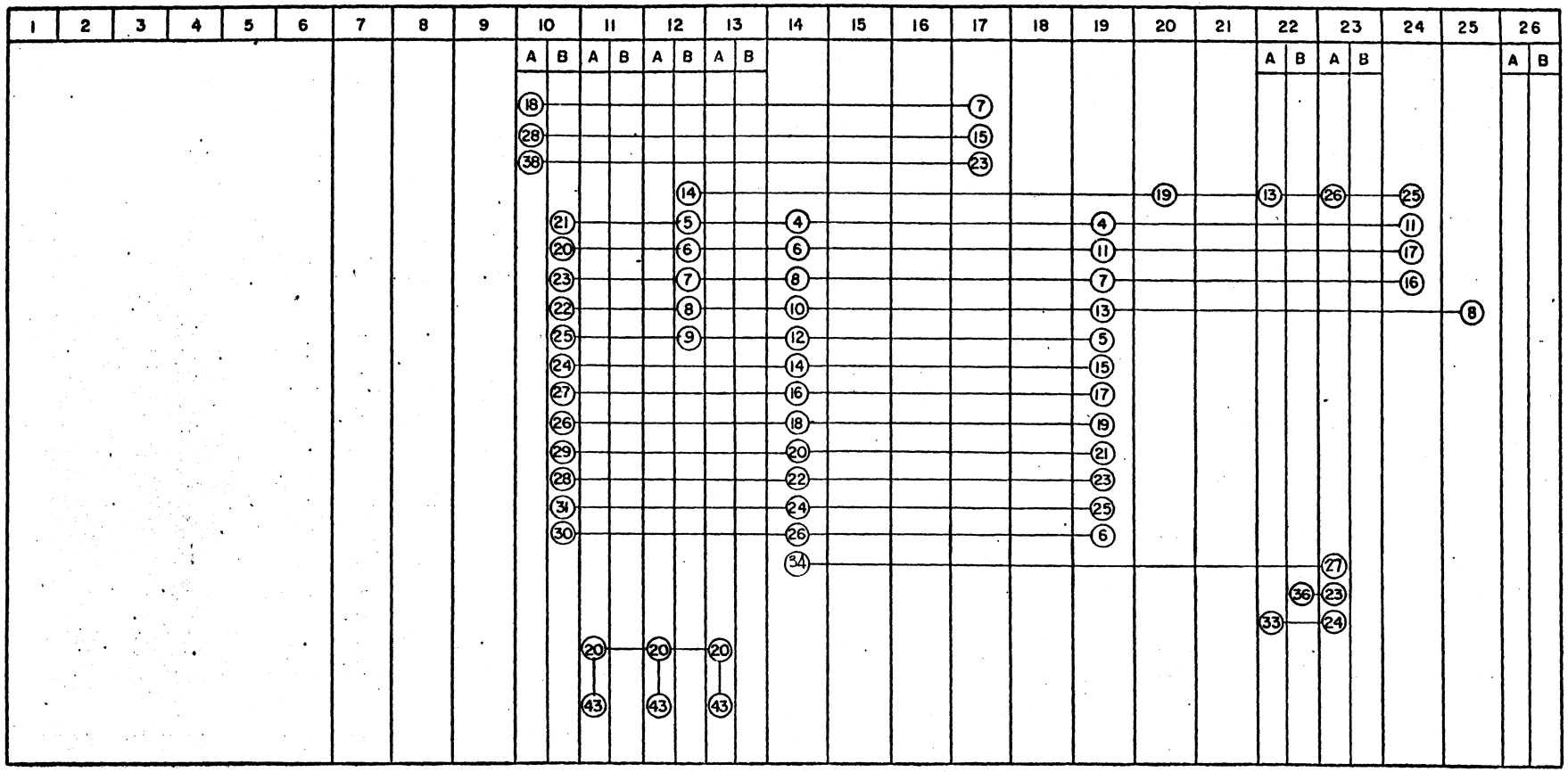
CONSOLIDATED COMPUTER INC.
OTTAWA

BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

title

sheet 11 of 28 — no. SLB11806W — 1

RACK A



rev	description	date	by	chkd	approved
1	PRE PRODUCTION RELEASE	3JAN73	RB		

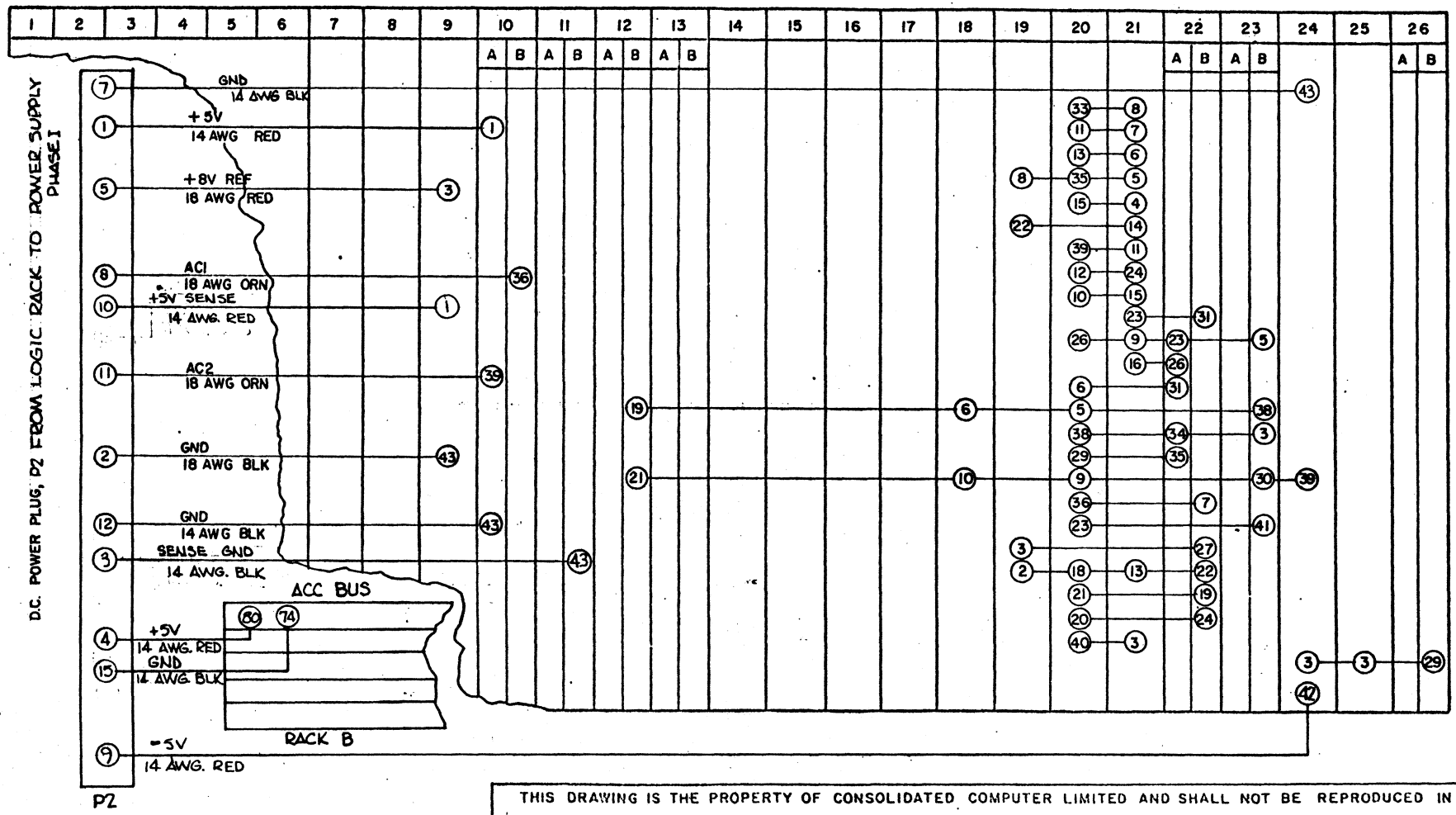
SLD11806A & SLD11807A — used on
3 JAN 73. — date
scale
R Boyd — drawn
design ENG
check
unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles = ± 0 30'
material
finish

CONSOLIDATED COMPUTER INC. OTTAWA

BACK PLANE WIRING
SERIES L-PHASE I
LOGIC RACK

title

sheet 12 of 20 — no. SLD11806W — 1



rev	description	date	by	chk	approved
1	PRE PRODUCTION RELEASE	3 JAN 73	RB		

SLD11806A & SLD11807A — used on

3 JAN 73 — scale / date

unless specified
.00 = ± .01 fraction ± 1/64
.000 = ± .005 angles ± 0 30'

R. Boyd — drawn

ENG. — design

finish — material

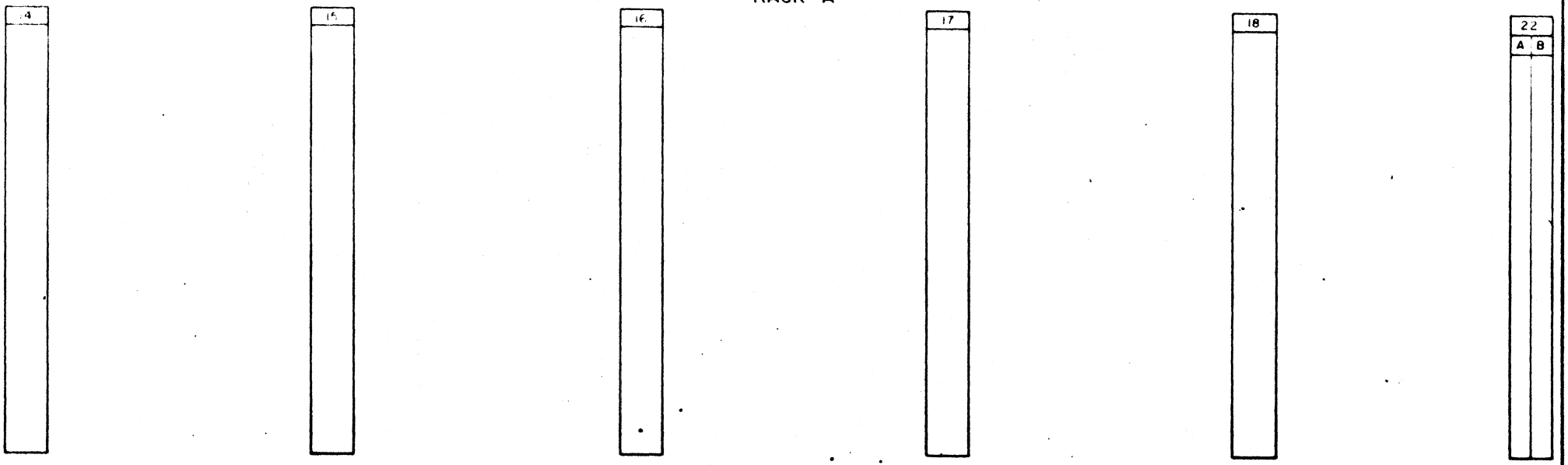
CONSOLIDATED COMPUTER INC. OTTAWA

BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

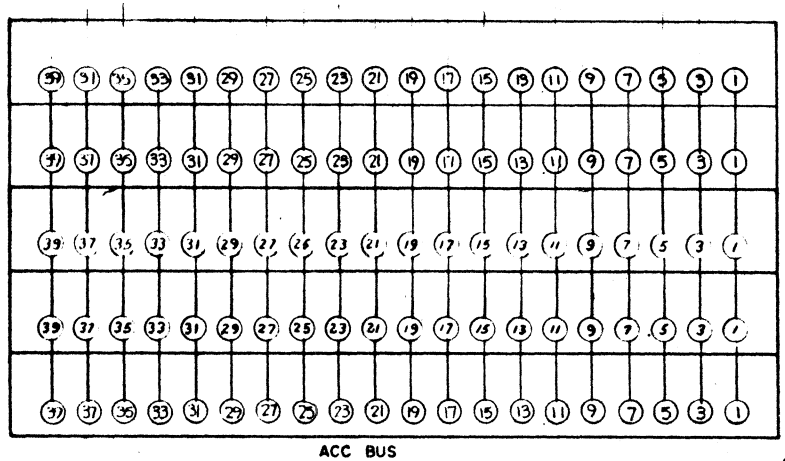
title

sheet 13 of 22 — SLB11806W — no.

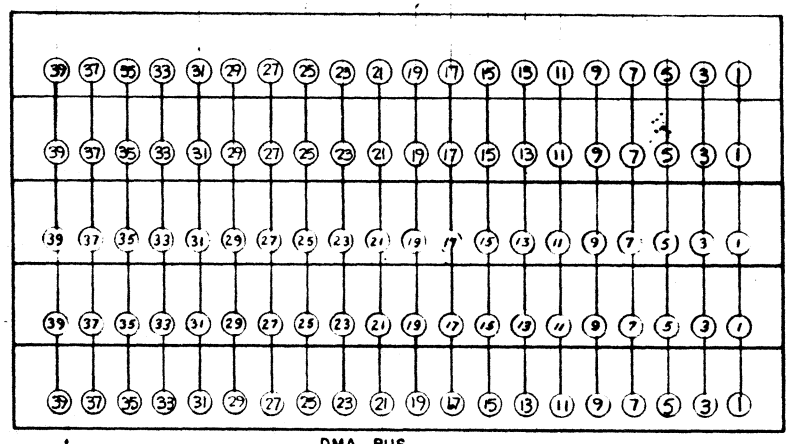
RACK A



CONNECTOR



ACC BUS



DMA BUS

RACK B

SHEETS 1 TO 13 "B SIZE"

rev	eco	description	date	by	chk	approved
1		PRE PRODUCTION RELEASE	2 JAN 73	RB		

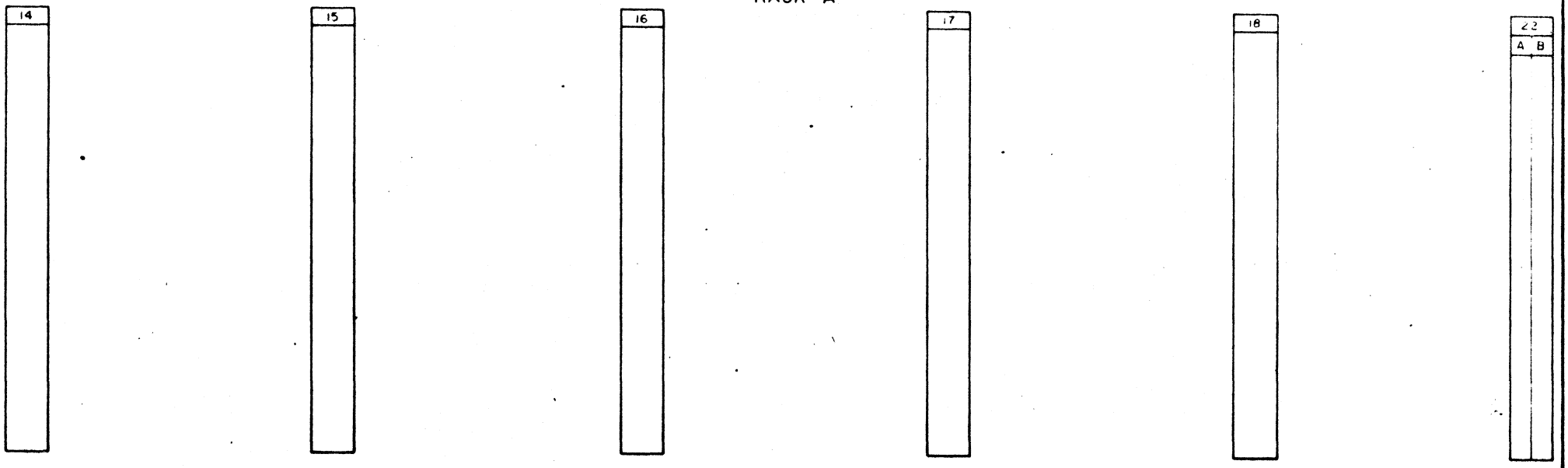
used on: SLD11806A & SLP1107A
scale:
date: 2 JAN 73
drawn: R. BOYD
design: BJG
checked:
unless specified: .00 = ±.01 fraction ± 1/64; .000 = ±.005 angles ± 0 30
final approval:
material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK
sheet: 14 of 28
no.: SLC 11806W
rev: 1

4 3 2 1

RACK A



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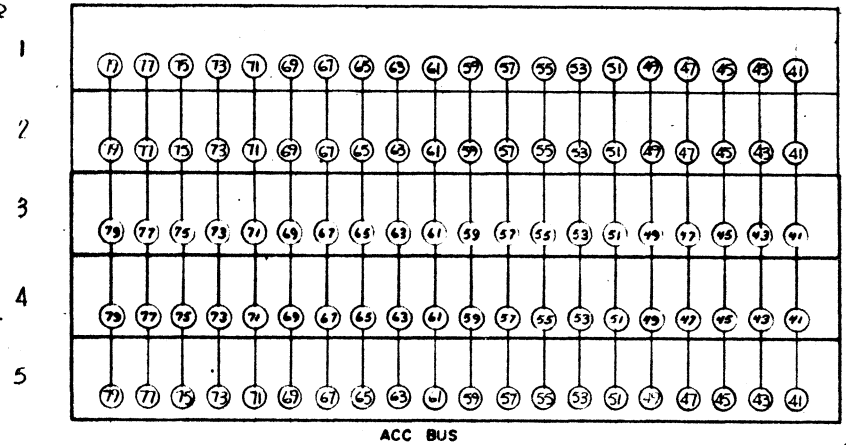

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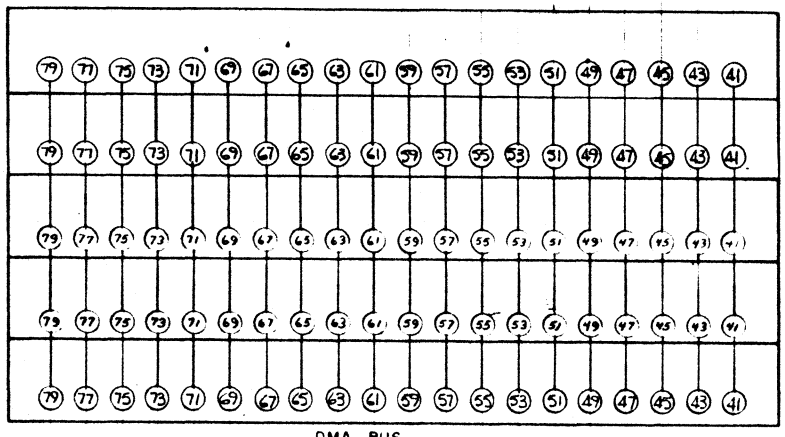


DMA BUS

RACK B

rev	eco	description	date	by	chk	approvd
1		PRE PRODUCTION RELEASE	2 JAN 73	RB		

SLD118064 & SLD118074 — used on
2 JAN 73 — date
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

K. Boyd — drawn
design ENG.
checked
other approval
material
finish

CONSOLIDATED COMPUTER INC. OTTAWA

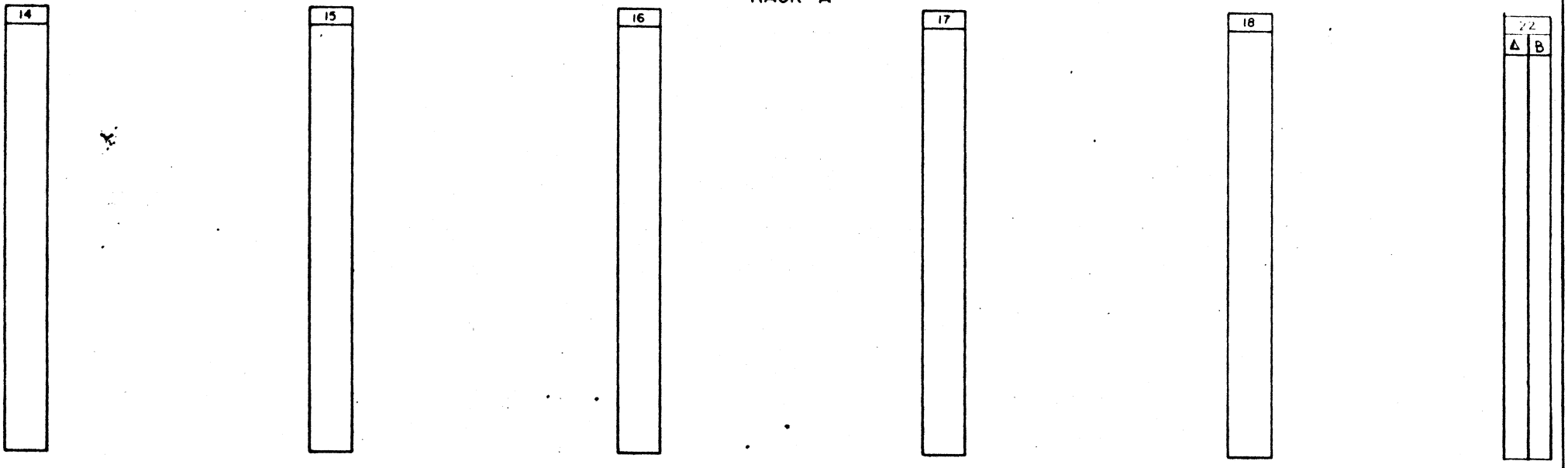
title: BACK PLANE WIRING SERIES L-PHASE I LOGIC RACK

sheet 15 of 28

no. SLC11806W

rev 1

RACK A



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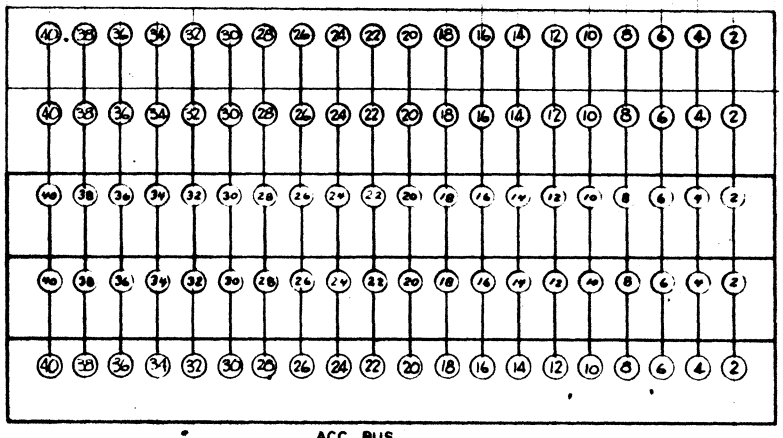

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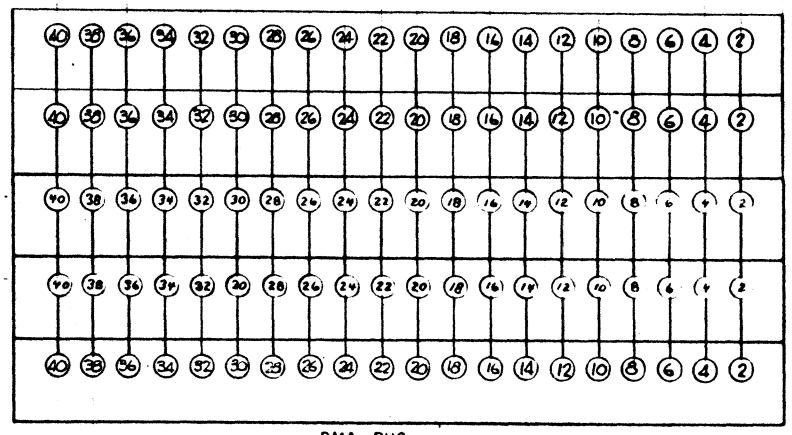


DMA BUS

RACK B

rev	eco	description	date	by	chk	apprvd
1		PRE PRODUCTION RELEASE	2 JAN 73	RB		

used on	SLD11806A & SLD11807A
scale	
date	2 JAN 73
drawn	R Boyd
engineering	
checked	
mfg. approval	
material	
finish	

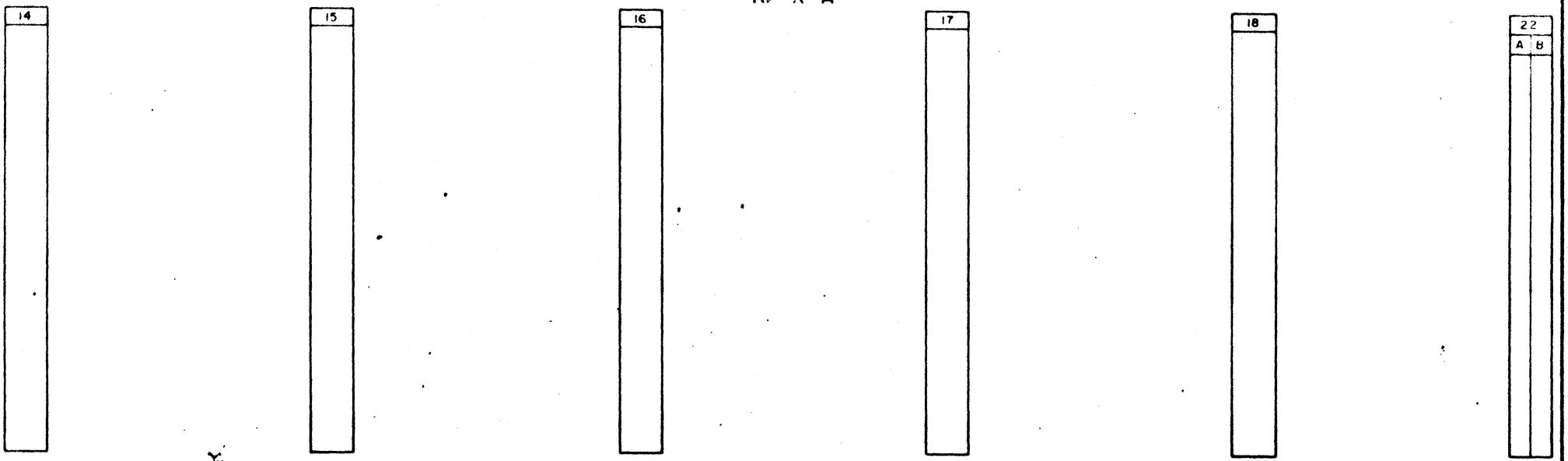
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

CONSOLIDATED COMPUTER INC.
OTTAWA

BACK PLANE WIRING
SERIES L-PHASE I
LOGIC RACK

title	sheet	of	no.	rev
	16	28	SLD11806W	1

RACK A



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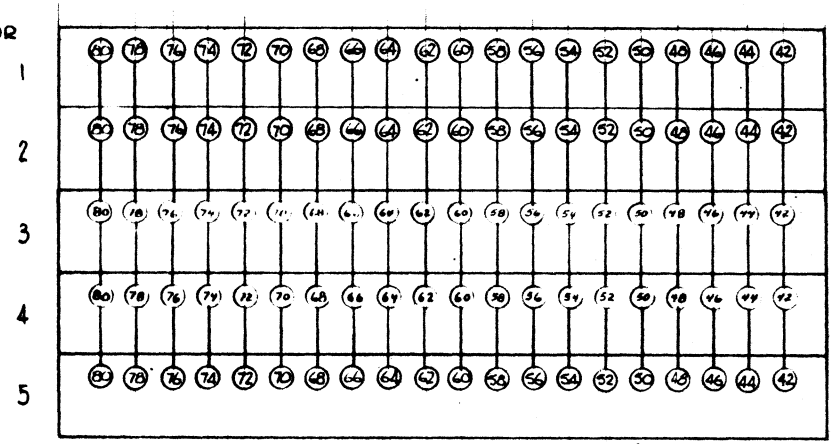

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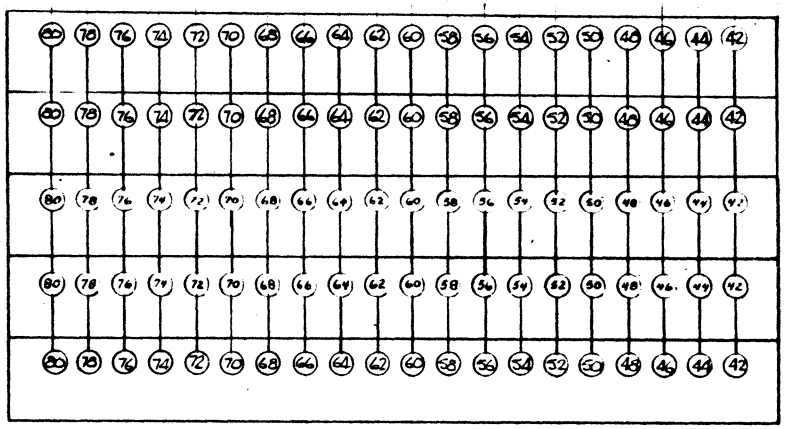


DMA BUS

RACK B

1	PRE PRODUCTION RELEASE	2 JAN 73	RB		

used on: SLD11806A & SLD11807A	R. BOYD drawn	CONSOLIDATED COMPUTER INC. OTTAWA
2 JAN. 73 date	ENG.	BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK
		title: 17 sheet 28 of no. SLC11806W rev 1

rev	eco	description	date	by	chk	approved
1		PRE PRODUCTION RELEASE	2 JAN 73	RB		

used on: SLD11806A & SLD11807A
scale:
date: 2 JAN 73
drawn: R. Boyd
design: ENG
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material:
finish:

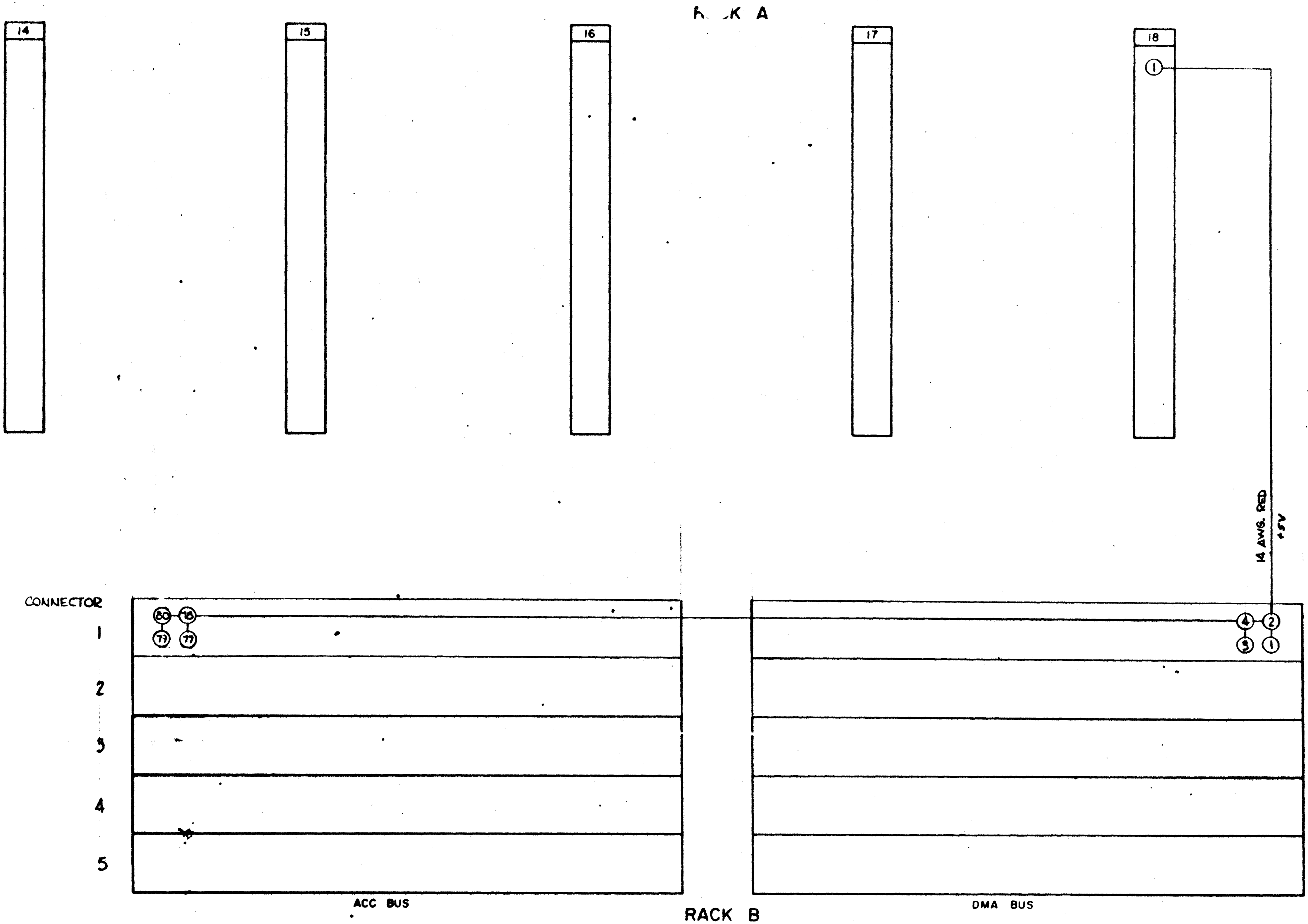
CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L - PHASE I - LOGIC RACK

sheet 18 of 28

no SLC11806W

rev 1



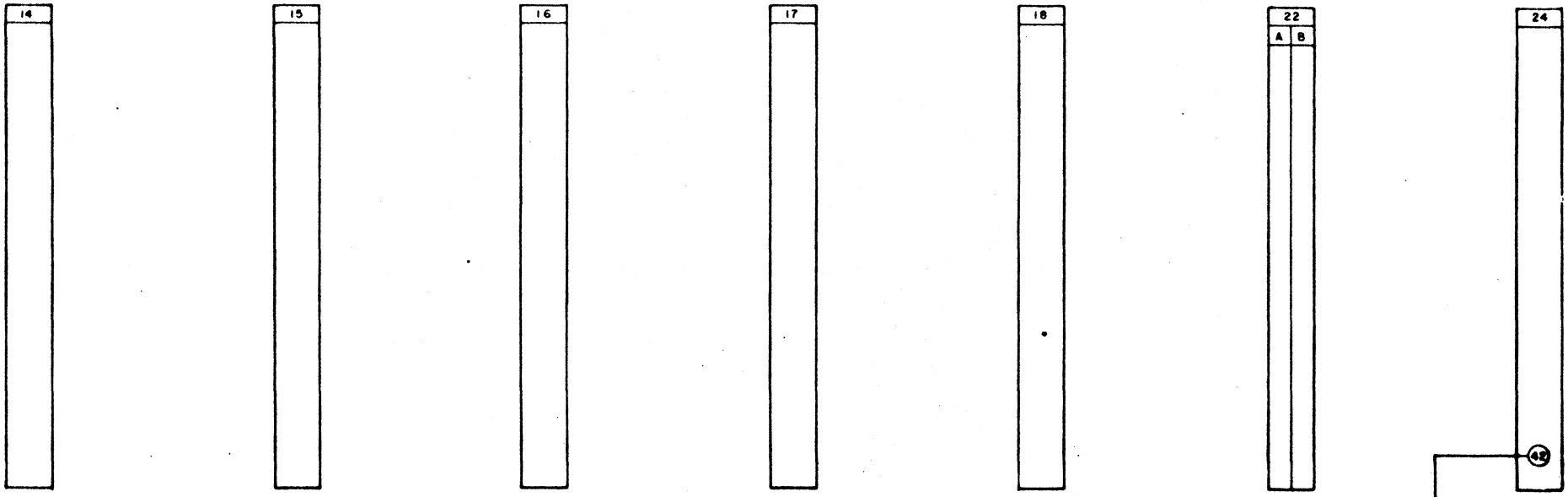
CONSOLIDATED COMPUTER INC.
OTTAWA

BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

used on	SLD11806A & SLD11807A
drawn	R. Boyd
date	2 JAN 73
sheet	19 of 28
no.	SLC11806W
rev	1

rev	eco	description	date	by	chk
1		PRE PRODUCTION RELEASE	2 JAN 73	RB.	

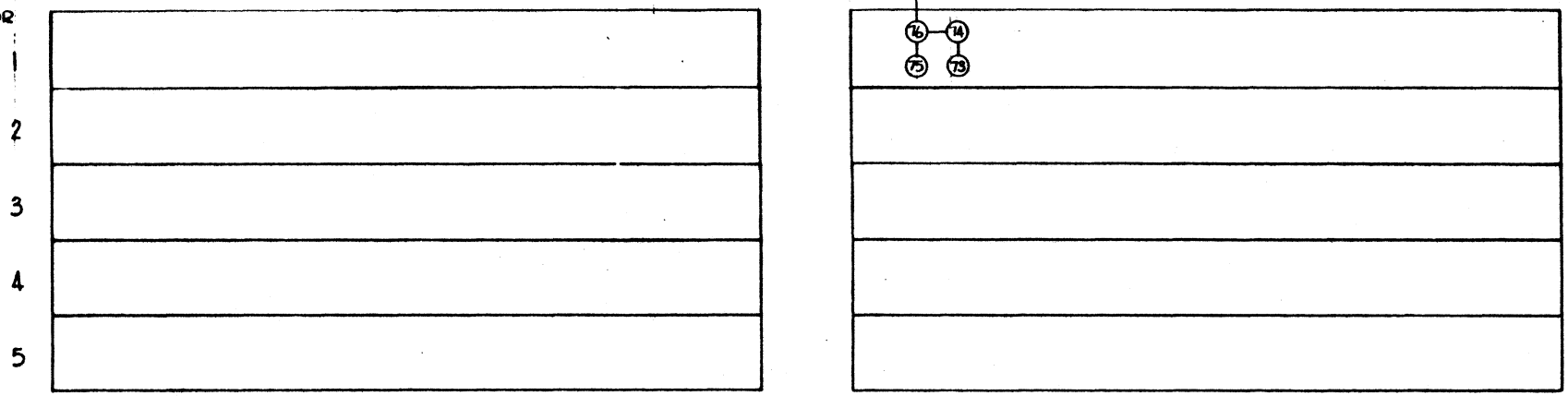
RACK A



14 AWG. RED

-5V

CONNECTOR



ACC BUS

DMA BUS

RACK B

rev	eco	description	date	by	chk	approv
1		PRE PRODUCTION RELEASE	2 JAN 73	RE		

SLD11806A & SLD11807A used on

2 JAN 73 date

R Boyd drawn

design ENG.

check

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

final approval

material

finish

CONSOLIDATED COMPUTER INC. OTTAWA

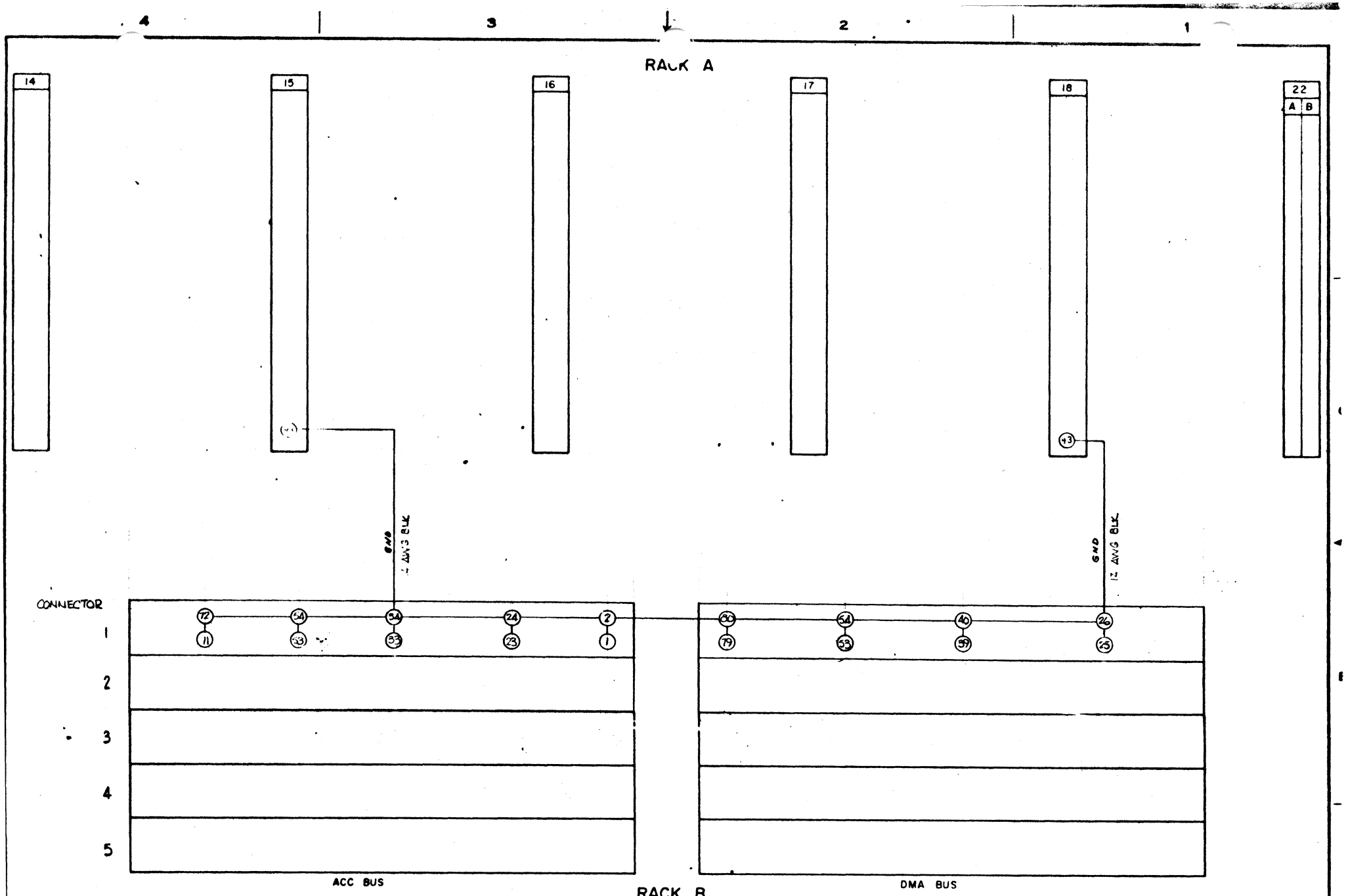
BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

title

sheet 20 of 28

no. SLCI1806W

rev 1



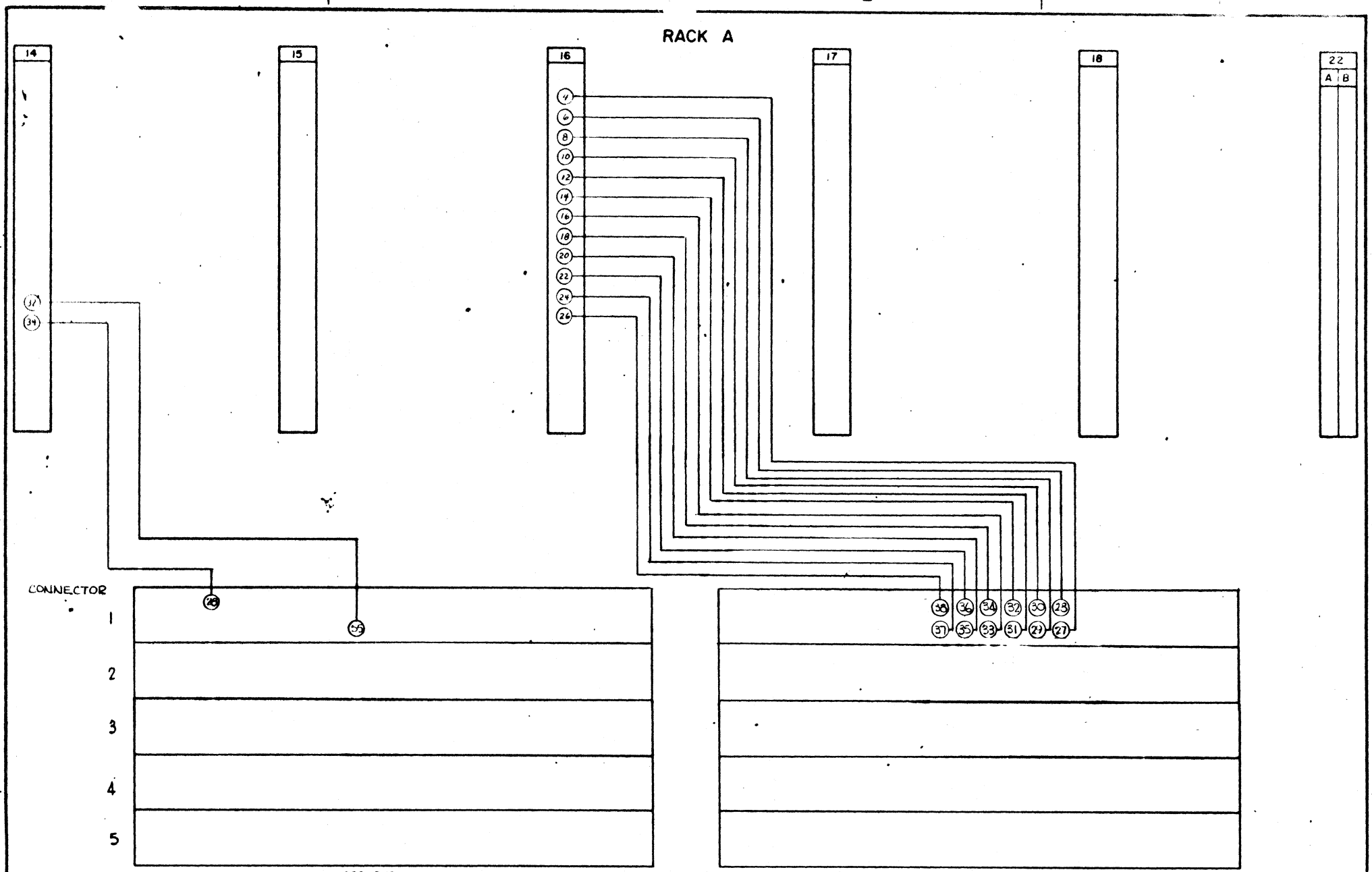
rev	eco	description	date	by	chk	approv
1		PRE PRODUCTION RELEASE	2 JAN 75	RB		

SLD118064 & SLD118074 — used on
2 JAN 73 — date
R Boyd — drawn
design ENG
unless specified
.00 = ±.01 fraction ± 64
.000 = ±.005 angles = ±0.5°
1st appvd
material
finish

CONSOLIDATED COMPUTER INC.
OTTAWA

BACK PLANE WIRING
SERIES 1- PHASE I
LOGIC RACK

title
21 sheet 28 of
no. SLC11806W
1 rev



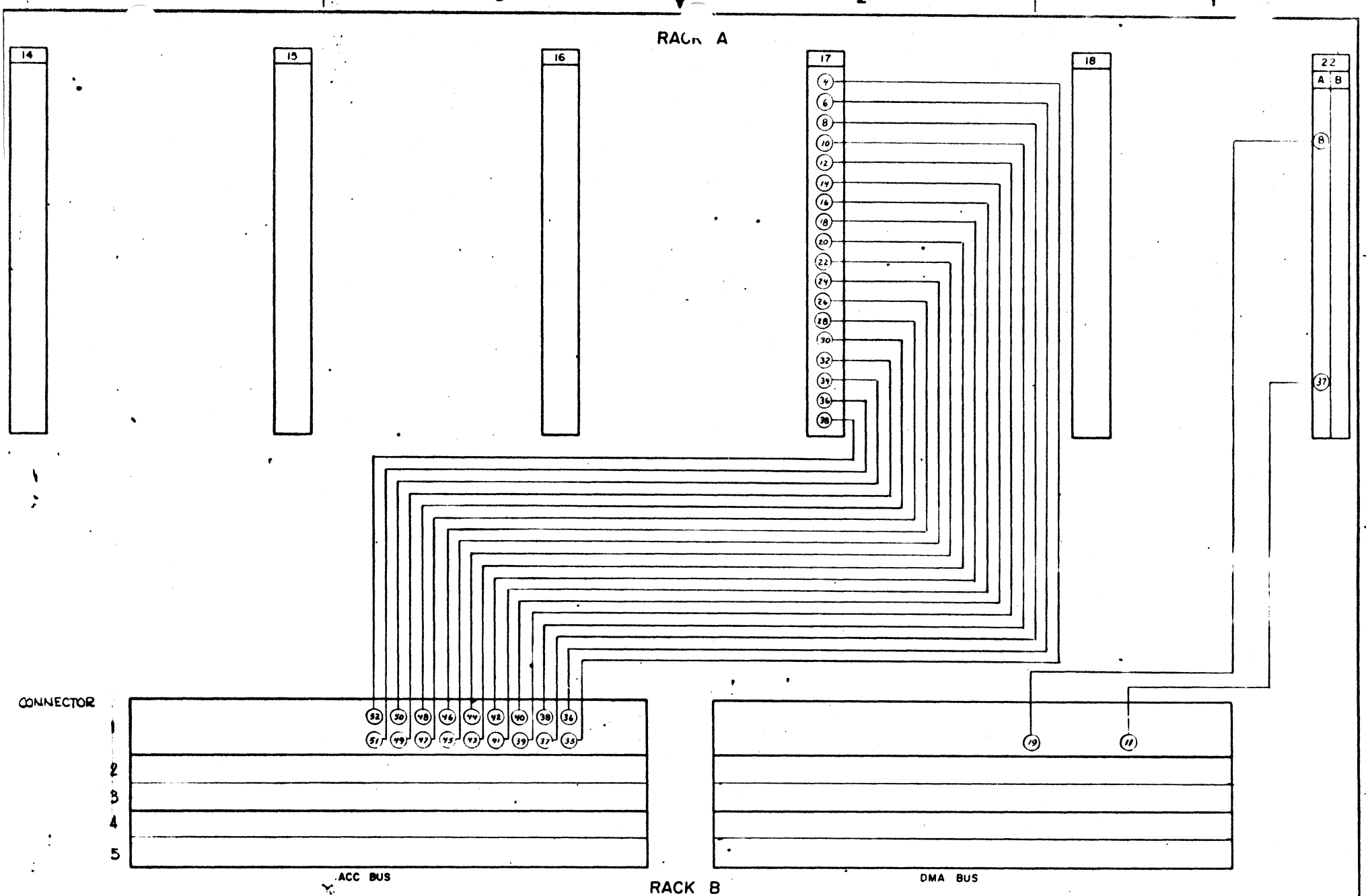
1	PRE PRODUCTION RELEASE	3 JAN 73	RB	

SLD11806A & SLD11807A — R BOYD — 3 JAN 73

CONSOLIDATED COMPUTER INC. OTTAWA

BACK PLANE WIRING SERIES L - PHASE I LOGIC RACK

22 28 — SLC11806W — 1



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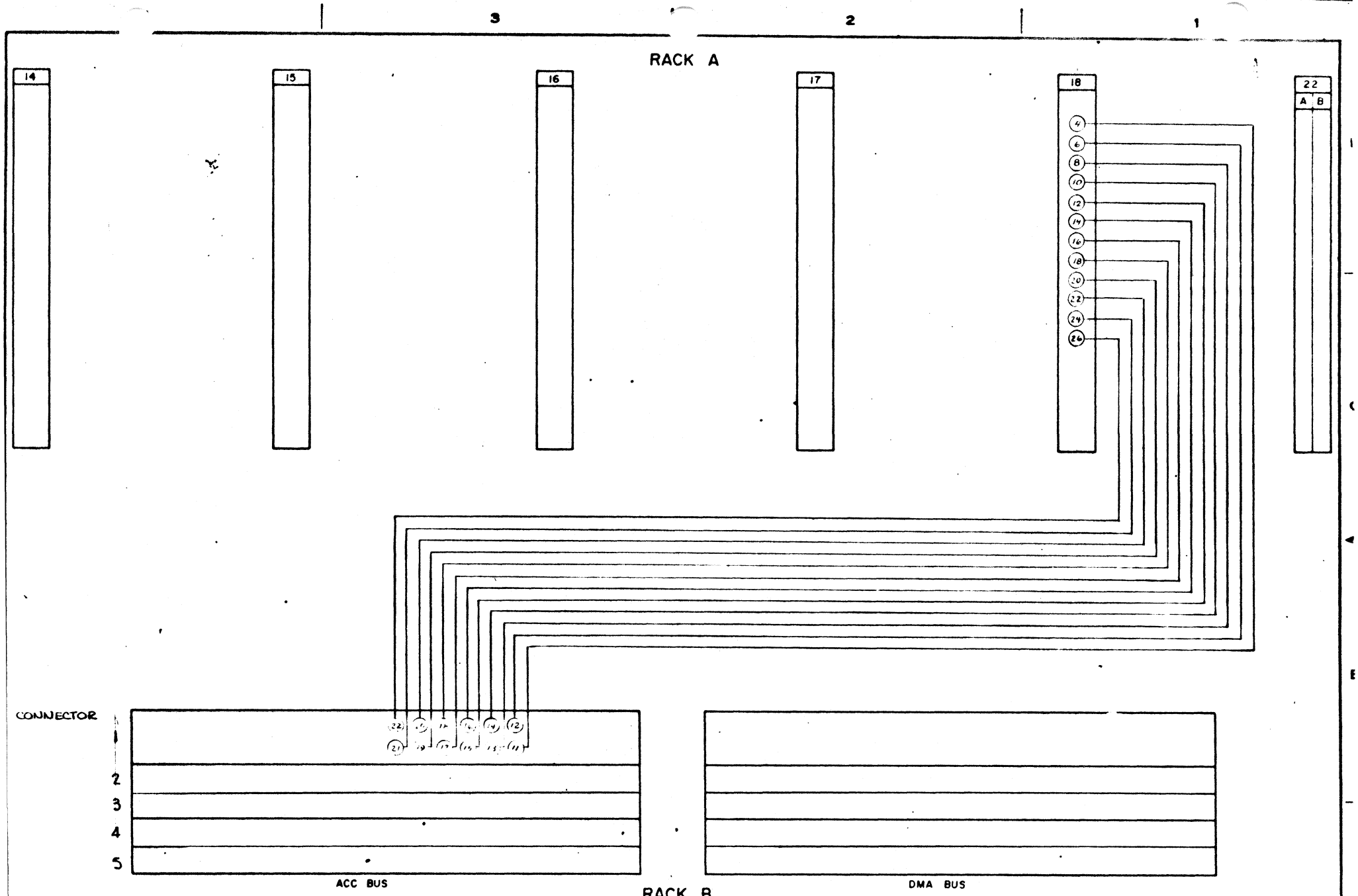
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

used on	SLD11806A & SLD11807A
drawn	R BOYD
scale	
date	3 JAN. 73
design F.N.S.	
unless specified .XX ± .01 fraction ± 1/64 .XXX ± .005 angles ± 0.5°	
ch	
approved	

CONSOLIDATED COMPUTER INC.
OTTAWA

BACK PLANE WIRING
SERIES -
LOGIC RACK

title			
sheet	of	SLC11806W	1
23	28		



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used on: SLD118064 & SLD118074 | drawn: R BOND | scale | date: 3 JAN 73 | design | check

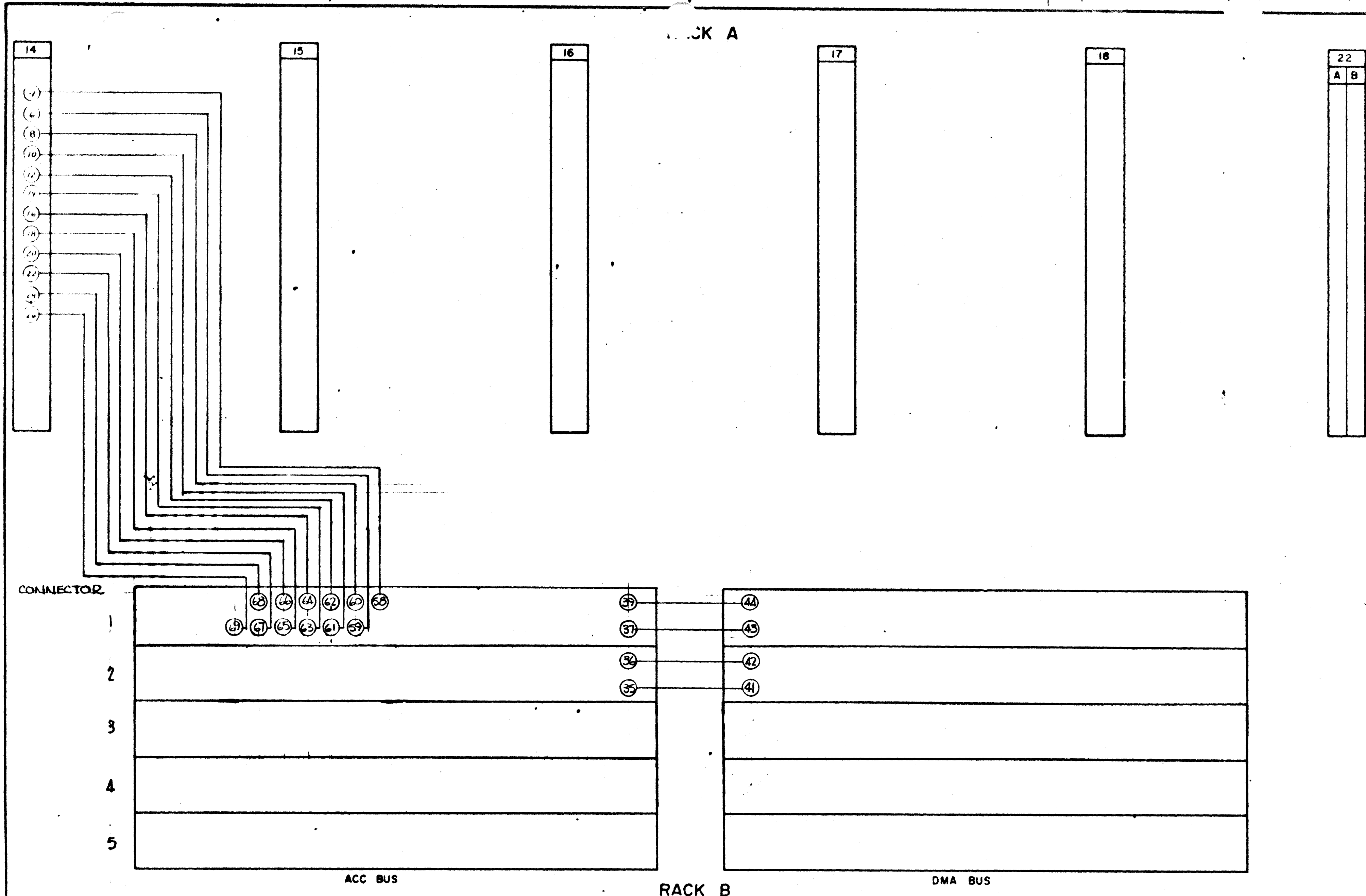
unless specified: 00 = ±.01 fraction ± 1/64; 000 = ±.005 angles = ± 0 30'

material | finish

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

sheet 24 of 28 | no SLC11506W | rev 1



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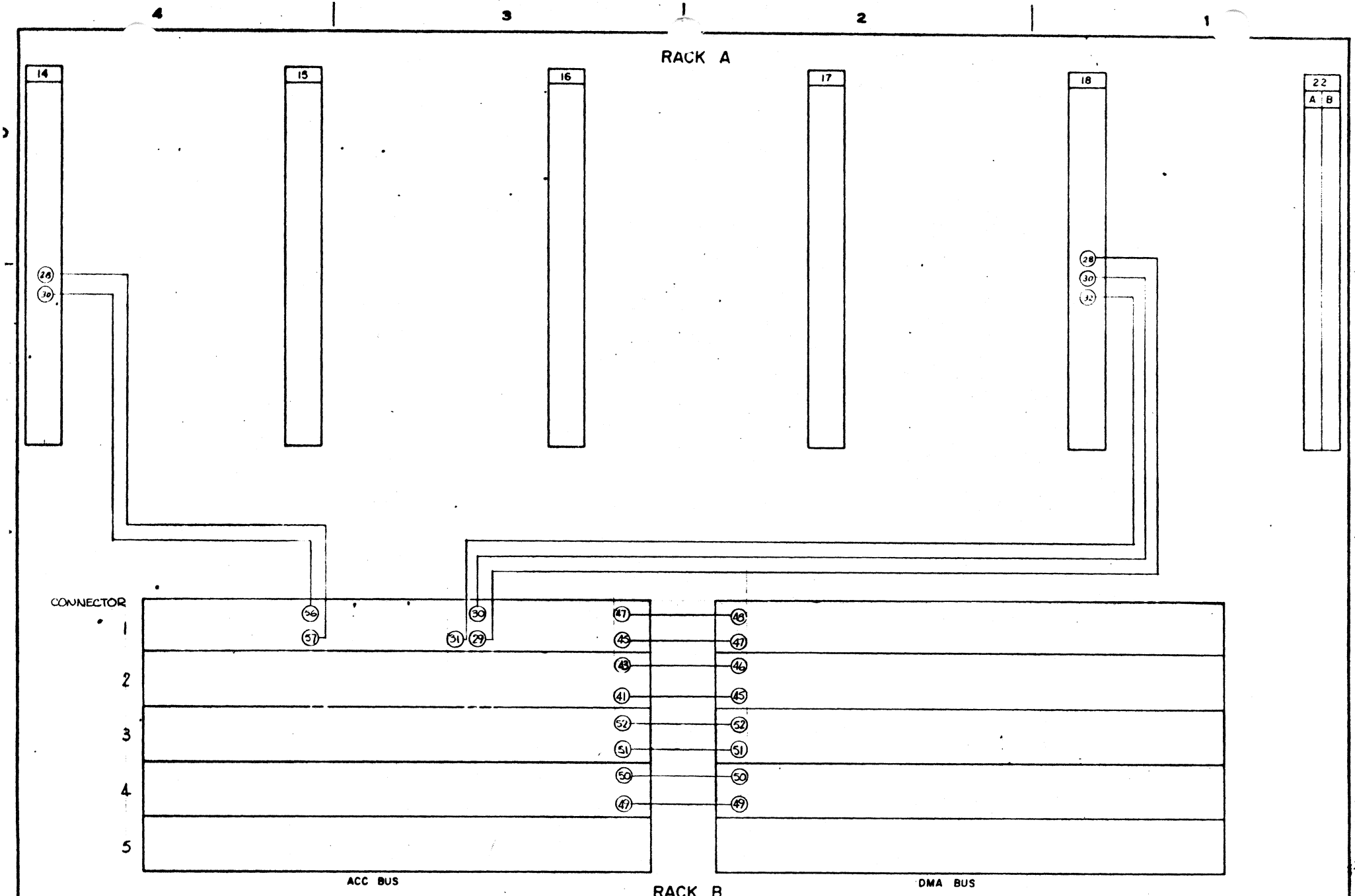
rev	description	date	by	chk	apprvd

used on: SLD11806A & SLD11807A
drawn: R BOYD
date: 3 JAN 73
unless specified

CONSOLIDATED COMPUTER INC. OTTAWA

title: BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK

sheet 25 of 28 — no. SLC11806W — rev 1



rev	eco	description	date	by	chk	unprvd
1		PRE PRODUCTION RELEASE	3 JAN 73	RB		

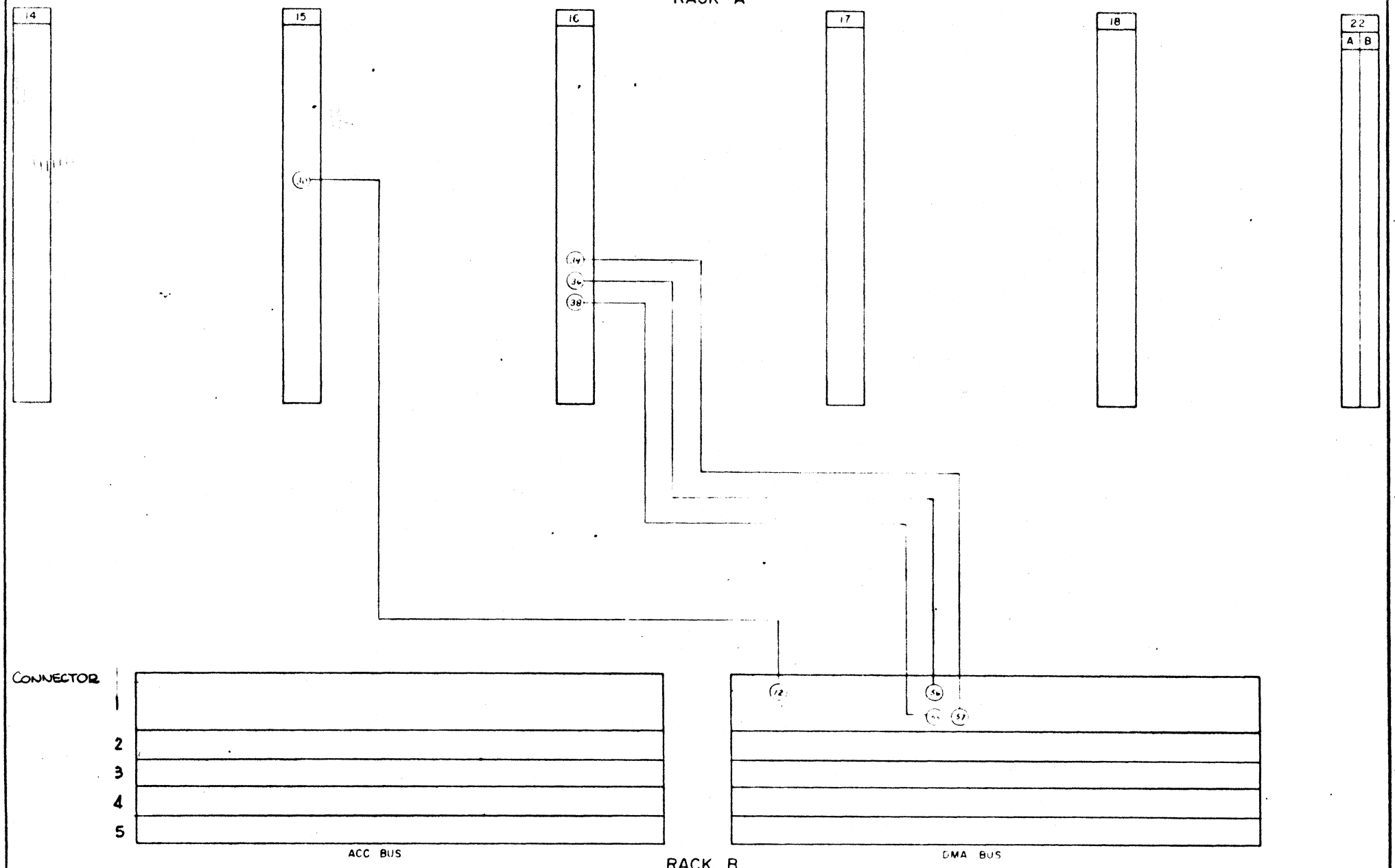
used on	SLD11806A & SLD11807A
scale	date 3 JAN 73
unless specified	.00 ± .01 fraction ± 64 .000 ± .005 angles ± 0 30
drawn	R. Boyd
des. appr.	ENG
chkd	
mfgr. approv.	
material	
finish	

CONSOLIDATED COMPUTER INC.
OTTAWA

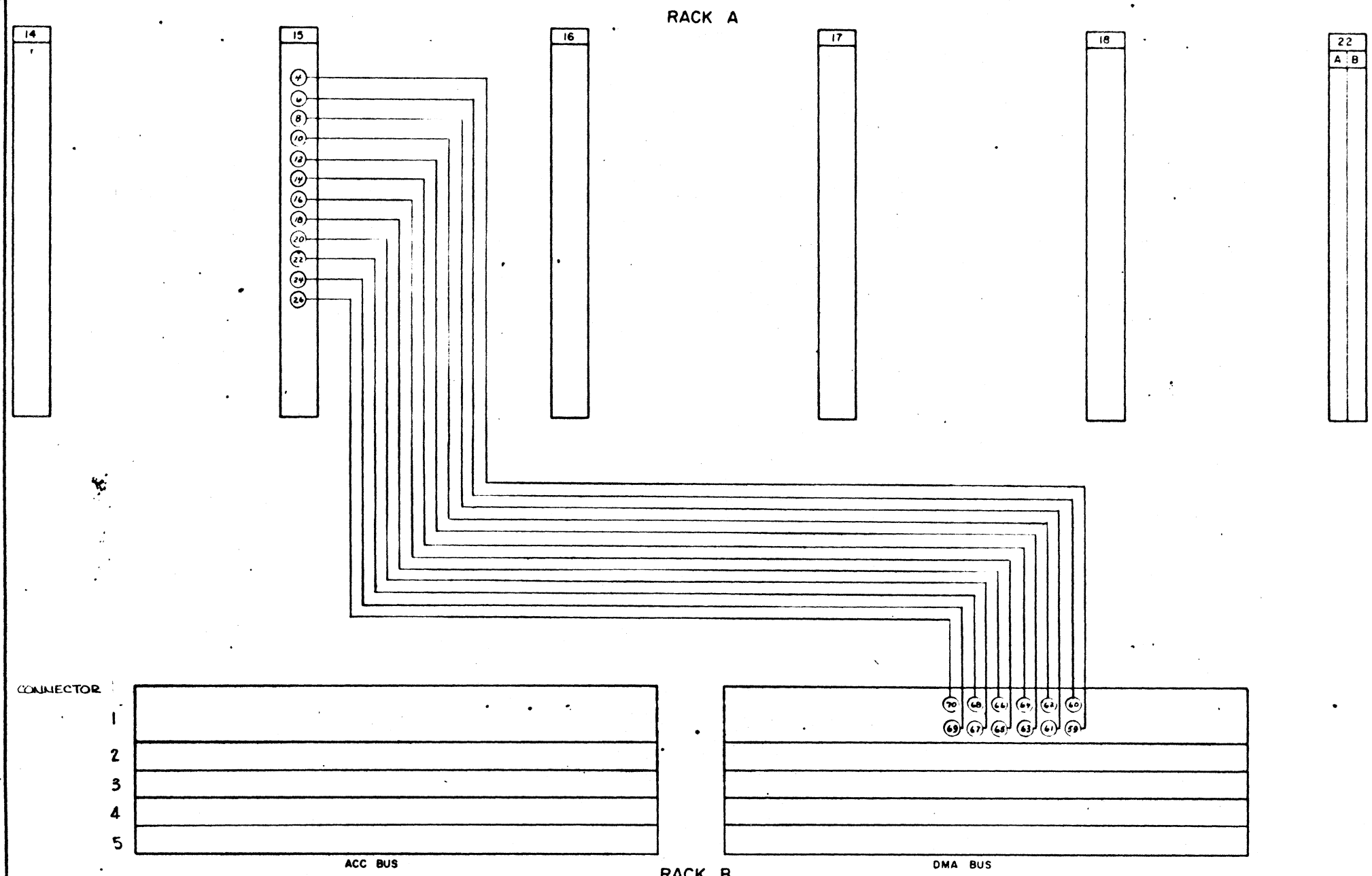
BACK PLANE WIRING
SERIES L- PHASE I
LOGIC RACK

title			
sheet 26 of 28	no SLC11806W	rev 1

86 TRANSFER IS Dwg. #



1	PRE PRODUCTION RELEASE	3 JAN 73 RB	SLD11806A & SLD11807A R BOYD	CONSOLIDATED COMPUTER INC. OTTAWA
			3 JAN 73	BACK PLANE WIRING SERIES L- PHASE I LOGIC RACK
			PROJ ENG	27 28 SLC11806W 1



rev	prod	description	date	by	chk	approved
1		PRE PRODUCTION RELEASE	8 JAN 73	PB		

SLD11806A & SLD11807A used on

scale

3 JAN 73 date

unless specified .00 ± .01 fraction ± 1/64 .000 ± .005 angles ± 0.5°

R. Boyd drawn

TPO design Engr.

check

finish

material

CONSOLIDATED COMPUTER INC. OTTAWA

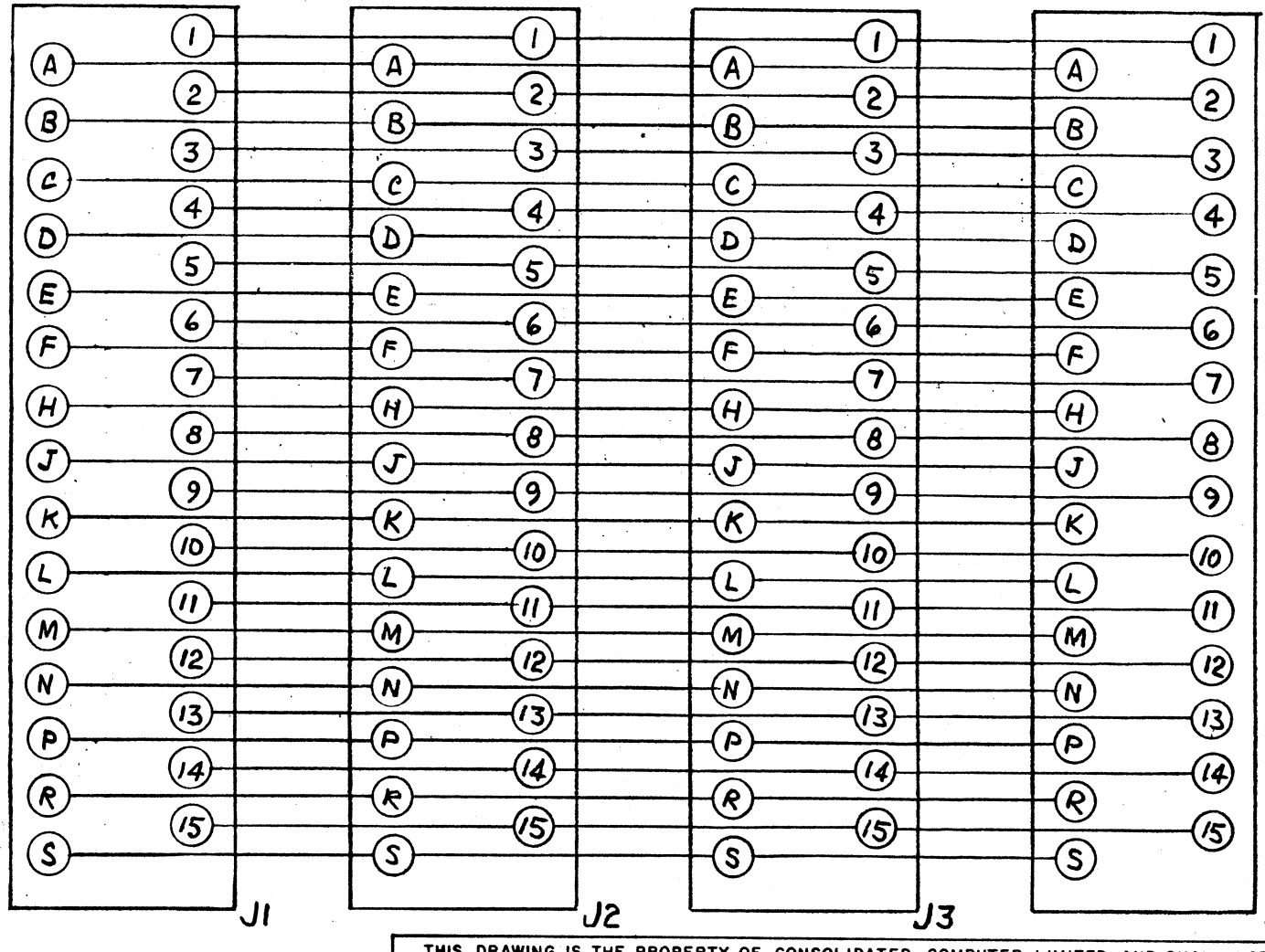
BACK PLANE WIRING SERIES L - PHASE I LOGIC RACK

title

28 28 sheet of

SLC11806W no.

1 rev



rev	eco	description	date	by	chk	apprvd
1		PRE-PROD RELEASE	17 JAN 73	GH		

used on SLC11819A

scale | date 16 JAN 73

drawn GH

design ENG DJW

checked

final apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

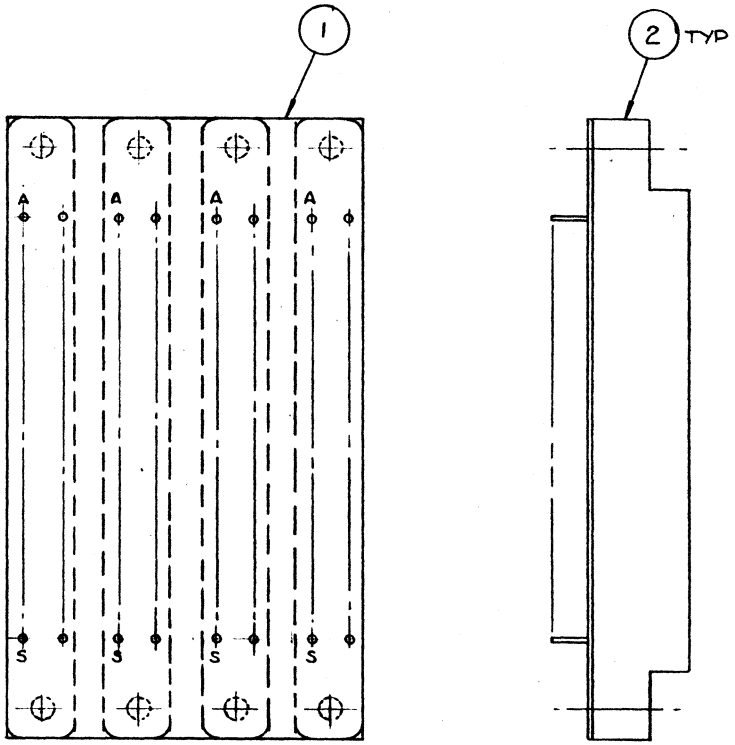
material | finish

CONSOLIDATED COMPUTER INC.
OTTAWA

SCHEMATIC
SERIES L-PHASE 1
INTERCONNECT 4

title

sheet 1 of 1 | no. SLB 11819 S



FOR PARTS LIST SEE SH 2

rev	eco	description	date	by	chk	approvd
1		PRE-PROD RELEASE	16JAN73	GH		

used on SLD11807A

drawn GH

scale 2/1 date 15 JAN 73

design ELEC DIW

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles ± 0 30'

checked

final apprvl

material

finish

CONSOLIDATED COMPUTER INC. OTTAWA

PCB ASSEMBLY
SERIES L - PHASE I
INTERCONNECT - 4

title

sheet 1 of 2 no. SLC11819A 1

TRANSTEX 10 800-0-73

CONSOLIDATED COMPUTER INCORPORATED

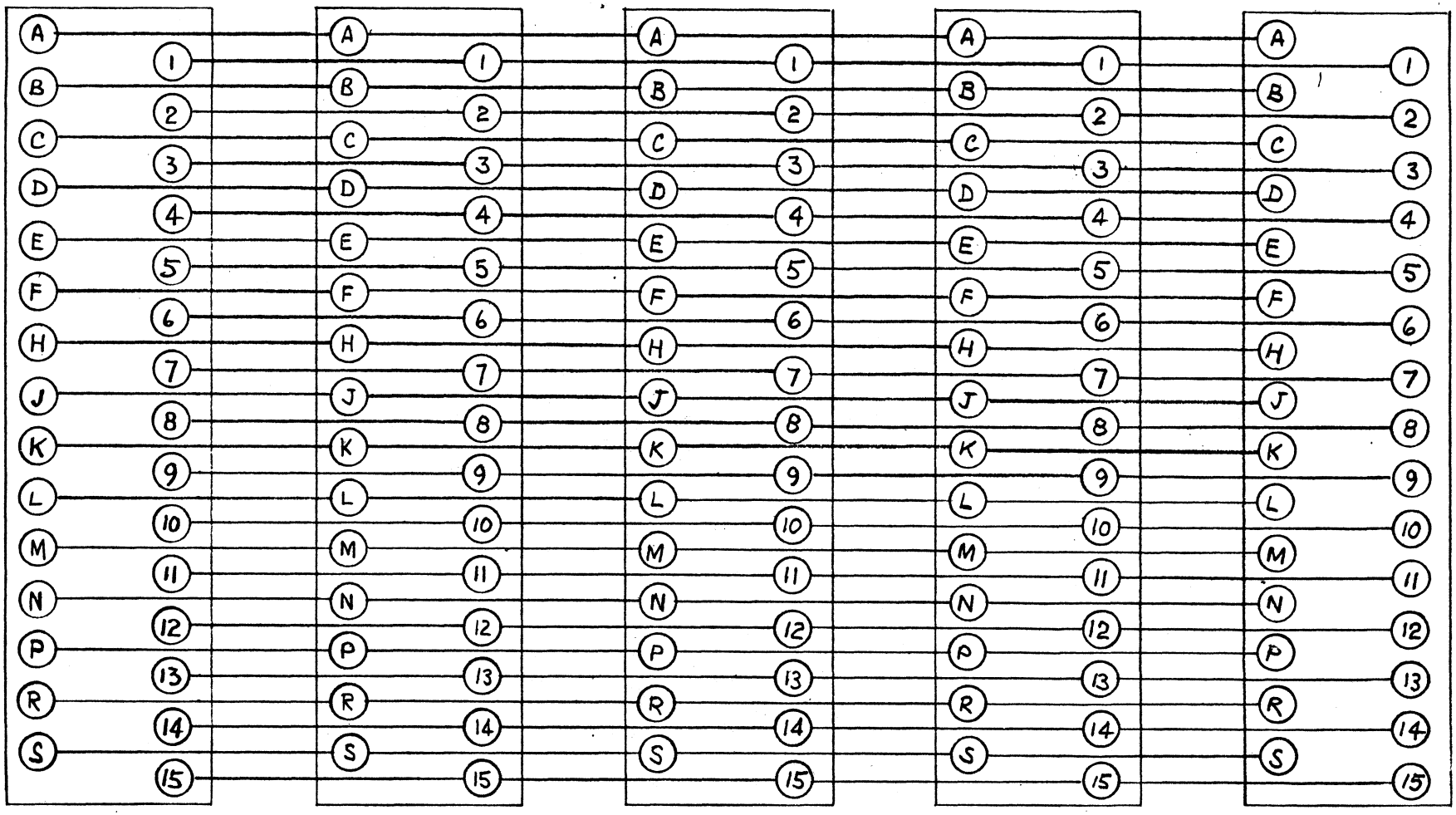
ASSEMBLY PARTS LIST

COMPILED BY: GH	DATE 16 JAN 73	APPROVED BY	QTY RUN
USED ON ASSEMBLY SLD11806A & SLD11807A		DRAWING REV 1	DATE ISSUE
ASSEMBLY NO SLC11819 A		SHT 2 OF 2	CONTRC

TITLE: PCB ASSEMBLY
SERIES L-PHASE I
INTERCONNECT 4

FOR ASSY SEE SH 1

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AV
1	SLD11819P		1	PCB BLANK			
2	92811		4	CONNECTOR (ELCO)	6007-030-981-002		
REF	SLC11819M/3			BOARD OUTLINE			
REF	SLB11819S			SCHEMATIC			



rev	eco	description	date	by	chk	apprvd
1		PRE PROD RELEASE	17 JAN 73	GH		

used on SLC11820 A | drawn GH | scale | date 16 JAN 73 | design ENG | checked | final apprvl

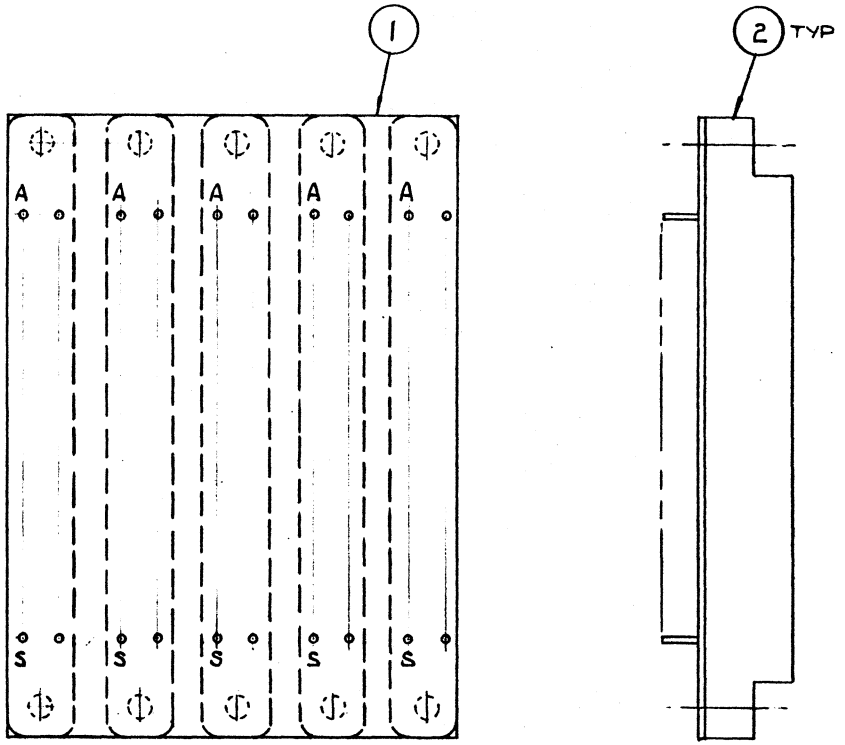
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

material | finish

CONSOLIDATED COMPUTER INC.
OTTAWA

title: SCHEMATIC SERIES L / PHASE I INTERCONNECT 5

sheet 1 of 1 | no. SLB 11820 S



FOR PARTS LIST SEE SH 2

rev	eco	description	date	by	chk	apprvd
1		PRE PROD RELEASE	16 JAN 73	GH		

used on SLD11806 A, SLD11807A
scale 2/1 date 15 JAN 73
drawn GH
design ENG
checked
final apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

material
finish

CONSOLIDATED COMPUTER INC.
OTTAWA

PCB ASSEMBLY
SERIES L - PHASE I
INTERCONNECT 5

title

sheet 1 of 2 no. SLC 11820 A 1 rev

CONSOLIDATED COMPUTER INCORPORATED

ASSEMBLY PARTS LIST

COMPILED BY: GH | DATE: 16 JAN 73 | APPROVED BY:

USED ON ASSEMBLY: SLD11806A & SLD11807A | DRAWING REV: 1

ASSEMBLY NO: SLC11820 A | SHT 2 OF 2

TITLE: PCB ASSEMBLY
SERIES L - PHASE I
INTERCONNECT 5
FOR ASSY SEE SH1

QTY RUN

DATE ISSUED

CONTROL

ITEM	PART NO.	RV	QTY	DESCRIPTION	REMARKS	QTY. REQ.	AVAIL
1	SLD11820P		1	PCB BLANK			
2	92811		5	CONNECTOR (ELCO)	6007-030-981-002		
REF	SLC11820M/4			BOARD OUTLINE			
REF	SLB11820 S			SCHEMATIC			

GENERAL

The Line Printer Interface is a Key-Edit Series 100 optional feature that permits a line printer to be used with the system in an off-line mode, or for dumping data.

The interface will operate with both 80 and 132 column line printers using any six, seven, or eight bit code set. Specifically, the printers are:

Centronics, Model 101—132 column 60/150 lines per minute
Data Products, Models 2310 and 2410—80 and 132 column 300 lines per minute

The interface consists of one pcb (11214) and a cable (11252) of 50 ft maximum length. Operating power is supplied by the 5 vdc logic rack supply.

A loop on the pcb indicates to the CPU that a printer interface pcb is installed in the logic rack.

IOT INSTRUCTIONS

6774 Skip On Serial Printer Interrupt.

If the serial printer is causing an interrupt to the CPU the program counter is incremented by one so that the next sequential instruction is skipped.

6761 Read Serial Printer Status.

The accumulator is cleared and the serial printer status word is read. The following bits are a binary one when the stated condition is true:

AC 00	Demand
AC 01	$\overline{\text{On Line}}$
AC 02	Illegal Command
AC 03, AC 04	Centronics Serial Printer Installed

AC 00 Demand is a signal from the serial printer indicating that it is ready to accept data. It goes false when a character is received, and goes true again when it is ready to accept another character. Demand will always be false if the printer is not on-line.

AC 01 On Line is a signal from the serial printer indicating that it is ready to print, i.e., the motor is up to speed, paper is not out, and the printer has been selected (switched on-line).

NOTE: the signal has been inverted so that $\overline{\text{On Line}}$ appears in the status word.

AC 02 Illegal Command is a signal that is true if the Illegal command flip-flop is set. This will occur if IOT 6751, Load Serial Printer Data, is issued when Demand is false, i.e.:

$$\text{Illegal Command} = \text{IOT 6751} \cdot (\overline{\text{Demand}})$$

No data is sent in this condition.

It is possible that the bad status causing the Illegal command flip-flop to be set could clear itself in the time between the issuing of IOT 6751 and the checking of the status word. The Illegal command flip-flop is cleared by IOT 6764, General Serial Printer Reset, or by B Run when the CPU is stopped.

AC 03, AC 04 Centronics Serial Printer Installed are bits which indicate that a Centronics serial printer interface pcb is installed and a cable is attached.

6771 Load Serial Printer Interrupt Mask.

This command loads the interrupt mask flip-flops and clears the accumulator. If the mask bit is a binary one an interrupt will be generated when the named condition is true. The flip-flops are cleared by IOT 6764, General Serial Printer Reset, or by B Run when the CPU is stopped. The interrupt mask bits are defined as follows:

AC 00	enable Demand interrupt
AC 01	enable $\overline{\text{On Line}}$ interrupt
AC 02	enable Illegal Command interrupt
AC 03	enable Printer Installed interrupt

NOTE: If mask bit AC 01 is a binary one an interrupt will be generated when the printer is off-line, i.e., $\overline{\text{On Line}}$ is true.

6764 General Serial Printer Reset.

This command will clear all interrupt mask flip-flops (thus all interrupts are cleared), data registers, and the Illegal command flip-flop.

6751 Load Serial Printer Data.

This command loads the serial printer Data Register from AC 05 through AC 11, sends a data strobe to the printer, and clears the accumulator.

AC 05	ID7	Seven-bit Centronics Serial Printer Code (See Table)
AC 06	ID6	
AC 07	ID5	
AC 08	ID4	
AC 09	ID3	ID7 most significant
AC 10	ID2	
AC 11	ID1	ID1 least significant

BEL	007	@	100
LF	012	A	101
VT	013	B	102
FF	014	C	103
CR	015	D	104
SO	016	E	105
Space	040	F	106
!	041	G	107
"	042	H	110
#	043	I	111
$	044	J	112
%	045	K	113
&	046	L	114
'	047	M	115
(	050	N	116
)	051	O	117
*	052	P	120
+	053	Q	121
,	054	R	122
-	055	S	123
.	056	T	124
/	057	U	125
0	060	V	126
1	061	W	127
2	062	X	130
3	063	Y	131
4	064	Z	132
5	065	[	133
6	066	\	134
7	067	]	135
8	070	^	136
9	071	DEL	177
:	072		
;	073		
<	074		
=	075		
>	076		
?	077		

NOTE: The codes are represented in terms of octal numbers and are a modified form of ASCII.

CONTROLLER DETAILS

The controller logic strobes code data from the CPU buffered accumulator to the line printer input buffer in parallel, one character at a time.

The interface contains five basic sections:

IOT Decoder	Interrupt Enable Register	Data Register
Status Outputs	Illegal Flop	

The illustrations contained at the end of this options section provide the Interface Flow Diagram, Write Sequence Diagram, Relative Timing, and the Logic Diagram.

IOT Decoder

The IOT Decoder decodes both positive and negative pulses from the CPU to produce IOT instructions 6751 to 6774.

Three IOP levels and several BMB outputs are generated by the CPU during the extended fetch cycle. The BMBs are applied to connector pin group B31 to B29 (left side) and decoded by NAND gates D5-6, D5-8, C5-6, and C5-8. IOPs 1, 2, and 4 are applied to connector pins B36, B37, and B38 respectively, and are gated through NAND gate group B3-8 to B5-11 with the BMB levels. The gate outputs are inverted or applied directly to connector pin group A34 to B35 as IOTs $\overline{6774}$ to $\overline{6751}$.

IOT First and Second Digits — All IOT commands are prefixed with the numeral 6, therefore the remaining three digits must be decoded. When BMBs 03, 04, and 05 are simultaneously high NAND gate D5-6 is enabled. Its low output is inverted and applied as a high level, Decode 7, to C5-8 pin 9, C5-6 pin 5, and D5-8 pin 9. Thus the first two digits of the IOT are now 67.

IOT Third Digit — The Decode 7 level, BMB 07 (0), BMB 08 (1), and BMB 06 (1) on pin 10 cause NAND gate D5-8 output to go low. The inverted output at D4-8 decodes the numeral 75. Similarly NAND gates C5-6 and C5-8 are enabled to decode numerals 76 and 77 respectively. Thus the IOT are now decoded to 675, 676, or 677.

IOT Fourth Digit — D4-8 output provides one input to the two-input NAND gates B5-11, B5-8, and B5-3. The other gate inputs are derived from IOP 1, IOP 2, and IOP 4 respectively. Thus the decoded output of B5-11 is 6751, B5-8 is 6752, and B5-3 is 6754. The other six IOTs are similarly decoded.

All the IOTs appear as a logical 1 state at the outputs of inverters A5 to C4.

IOTs 6751, 6761, and 6771 are inverted and applied to connector pin B10 as a CLR ACC signal.

Interrupt Enable Register

This register comprises four D-flops (F5 and E5). Four conditions of the line printer are monitored by this register:

Demand	(BAC 00)
$\overline{\text{On Line}}$	(BAC 01)
Illegal Command	(BAC 02)
Printer Installed	(BAC 03)

Interrupt Enable Bits.

If the Demand enable bit is present at connector pin B18, IOT 6771 will set the register flop F5-5. Consequently NAND gate G4-3 is enabled when Demand is true, causing H4-6 to go true. The high level output is inverted at E4-13 to produce an $\overline{\text{Interrupt}}$ level at connector pin B15. It is also gated through open collector DTL NAND gate G5-3 with IOT 6774, to create a $\overline{\text{Skip}}$ level at connector pin B16. The other three interrupt enable bits are strobed and gated similarly. The Interrupt Enable Register and the Illegal Flop are reset by B Run (0), or IOT $\overline{6764}$, via B3-11 and power inverter D3-6.

Interrupt Levels.

The Demand interrupt indicates that the printer is ready to accept another character. It goes low when data is received, and goes high when ready to accept more data.

The $\overline{\text{On Line}}$ interrupt indicates that the line printer is not ready to print, i.e., the motor is not up to speed, or there is not sufficient paper loaded.

An Illegal Command interrupt is generated if IOT 6751 is issued when either the $\overline{\text{On Line}}$ signal is high or the Demand signal is not high.

Status Outputs

Four status bits are provided as inputs to the CPU accumulator input buffer. All of the signals are unbuffered with the exception of AC 02, Illegal Command, as explained previously. They are:

AC 00	Demand
AC 01	$\overline{\text{On Line}}$
AC 02	Illegal Command
AC 03	Printer Installed

The status outputs originate from five open-collector DTL NAND gates formed by G5 and H5.

B Run (0) or IOT 6764 acts as a general reset and clear for the Illegal Flop and Data and Interrupt Enable Registers.

Installed Loop.

A status bit, AC 03, appears at connector pin B8 and provides an indication on the PDP-8 console when a Line Printer Interface pcb is properly installed and the cable connected. When these four interrupt enable levels are present in their high state the four D-flops are set high at F5-5, F5-9, E5-5, and E5-9. These levels are connected to the four G4 NAND gates to provide an Interrupt level at connector pin B15.

Illegal Flop.

The On Line signal is a combination of Select and Paper Empty from the printer. Select is a push button on the printer which is depressed to place the printer on-line; Paper Empty goes true when the sensor detects that paper has run out. Thus $\overline{\text{On-Line}} = \overline{\text{PE}} \cdot \text{SLCT}$

Select is received via connector pin V (top centre) by the Schmitt trigger receiver. R2 and C6 are line terminators. CR1 provides a higher threshold voltage at the input and R15 varies the output hysteresis. This output is applied to the input of NAND gate E2-11. Paper Empty, which is normally false, is received at connector pin X in the same manner as SLCT, inverted by E2-8, and fed to the other input of E2-11.

The DEMAND signal consists primarily of On Line and $\overline{\text{ACKNOWLEDGE}}$, which is a 4 ms pulse showing that the printer has received data and is ready for more. The trailing edge of the pulse will set flop F4-9, thus conditioning gate E2-3 pin 1. The On Line signal from E2-11 is inverted by E2-6 and enables E2-3 at pin 2. Thus $\overline{\text{DEMAND}}$ = On Line • ACKN

When jumper W2 is wired to C (bottom right) the output of E2-11 is inverted by H2-4 to condition H1-6. The output of E2-3 is applied through jumper W1 to enable H1-6, whose output will be low when the printer is ready to accept a character in its buffer. This output is connected to NAND gate H1-8 pin 9; IOT 6751 is connected to pin 10. Therefore if either the Demand or On-Line signal is not present when IOT 6751 strobes the gate, H1-8 is enabled low. This level appears at IOR gate H1-11. Pin 12 will go low only in the case of a detected parity error (which is an unused feature on this pcb). Therefore the Illegal Flop is set at F4-5, and in turn enables NAND gate G4-6, ultimately producing an interrupt to the CPU. Both the Demand and On-Line must be present before a character can be strobed into the printer.

Where a Data Products printer is installed the signals On Line and Demand are used; the jumpers W1 and W2 are wired accordingly. The signals are inverted by Q1 and Q2 and applied to H1-6, which functions as previously described.

Data Register

The Data Register comprises two quad-latch D-flops E3 and G3 (upper right). Input data from BAC 04 to BAC 11 is strobed into the register on the leading edge of IOT 6751. IOT 6751 is also delayed 60 ns by cascaded DTL inverters D1-2 and D1-4 before being gated, with the On-Line signal, through H4-8. The Data Strobe is generated on the trailing edge of IOT 6751 to ensure that the data is present at the printer before it is strobed into the line printer buffer. The strobe is generated when pin 12 of the one-shot, D2, goes high after its low excursion, resulting in a 1 μs pulse.

CHECKOUT PROCEDURE

Maintenance of the line printers should be conducted according to the instructions in the relevant manual.

The interface can be checked by the program listed overleaf; refer to Figure 02-3.

11018 - CABLE, DATA PRODUCTS LINE PRINTER

FROM	TO	FUNCTION
11214		
(or 10495) -A	CONN J1-E	Demand
B	y	On Line
S	j	$\overline{\text{Data Strobe}}$
T	u	Clear 6752
U	t	Latch 6754
L	p	Paper Instruction
K	B	ID1
J	F	ID2
H	L	ID3
F	R	ID4
E	V	ID5
D	Z	ID6
C	n	ID7
N	10495-P	Printer Installed Loop

11252-CABLE, CENTRONICS LINE PRINTER

FROM	TO	FUNCTION
11214-S	CONN J1- 1	$\overline{\text{Data Strobe}}$
W	10	$\overline{\text{ACKN}}$
X	12	Paper Empty
V	13	SLCT
K	2	Data 1 (ID1)
J	3	Data 2
H	4	Data 3
F	5	Data 4
E	6	Data 5
D	7	Data 6
C	8	Data 7
L	9	Data 8
P	11214-Y	Printer Installed Loop
N	-Y	

INSTALLATION PROCEDURE

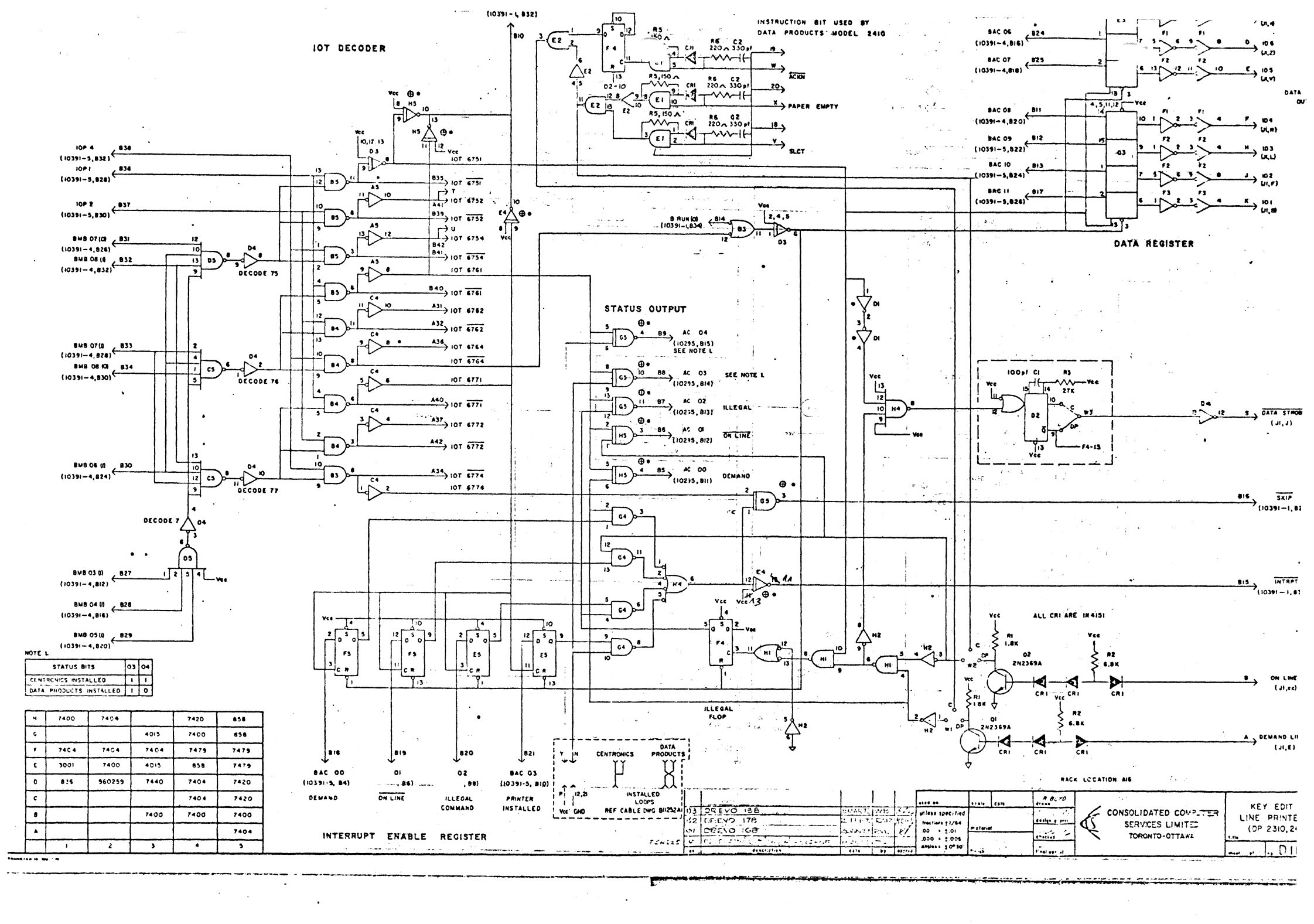
1. Plug the interface pcb into logic rack location A16.
2. Connect the interface cable from the pcb, through the bottom of the cabinet, to the line printer.
3. Plug the printer power cord into a 117 vac (or 220/240 vac) outlet.
4. Power up the printer
5. Run the test program

NOTE: When the printer is in operation do not de-select until printing is complete and print head has returned to its normal rest position.

Should de-selection take place while a 132 character line is being completed. the printer may continue to print out the last character. Should this occur, turn the printer ac switch off, and on again.

CHECKOUT PROGRAM LISTING
DATA PRODUCTS AND CENTRONICS PRINTERS

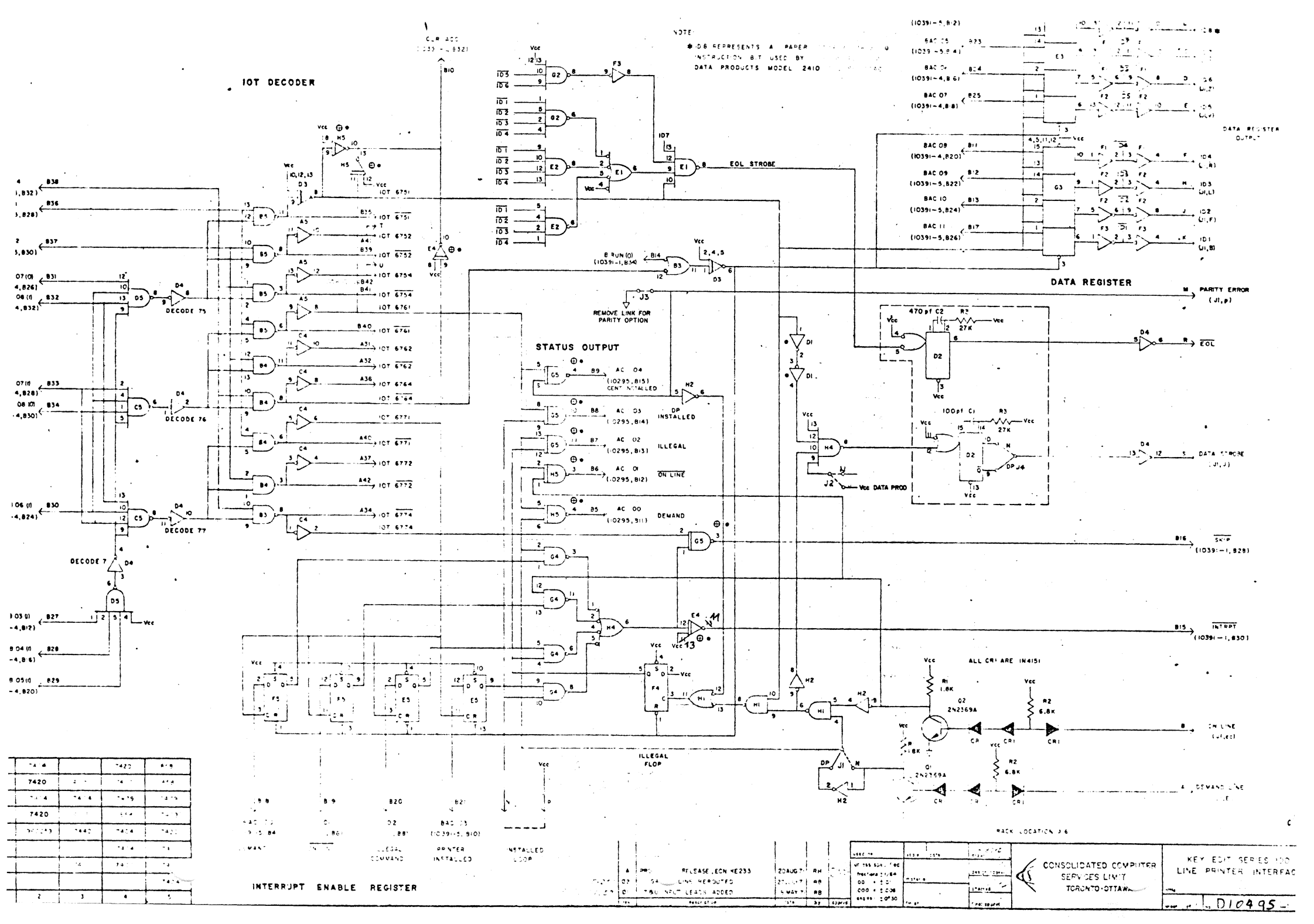
```
1000    6764    START,  RESET ALL
1001    7330            SET AC0
1002    6771            ENABLE INTERRUPT
1003    7300
1004    1050            TAD MAX
1005    3051            DCA COUNT
1006    4300            JMS DATA        /GET A CHARACTER
1007    4240            JMS PRINT       /STROBE TO PRINTER
1010    2051            ISZ COUNT       /NEXT COLUMN
1011    5206
1012    1052            TAD LINE FEED   /80 COL. DONE,DO LINE FEED
1013    4240            JMS PRINT       /STROBE TO PRINTER
1014    5200

0050    7660    MAX (80) (Insert 7574 for 132 column)
0051    0000    COUNT
0052    0012    LINE FEED (Insert 0015 for Centronics - Carriage Return)

                /PRINT ROUTINE
1040    0000
1041    6751            OUTPUT DATA
1042    6774            FLAG SET?
1043    5242            NO,JMP.-1
1044    7300            YES
1045    6761            CHECK STATUS
1046    0253            AND MASK
1047    7450            SKIP IF ANY ERRORS
1050    5640            NO STATUS ERROR,EXIT
1051    7402            STATUS ERROR,HLT
1052    5200            JMP START
1053    1200    MASK

                /DATA ROUTINE
1100    0000
1101    2053            INCREMENT CURRENT CHAR
1102    1053
1103    1054
1104    7630            IS IT > MAX CHAR ?
1105    5310            YES,RESET CURRENT CHAR
1106    1053            NO,GET IT
1107    5700
1110    1055            GET RESET VALUE
1111    3053            SET CURRENT CHAR
1112    5306

0053    0040    CURRENT CHAR
0054    7646    MAX CHAR
0055    0040    RESET VALUE
```

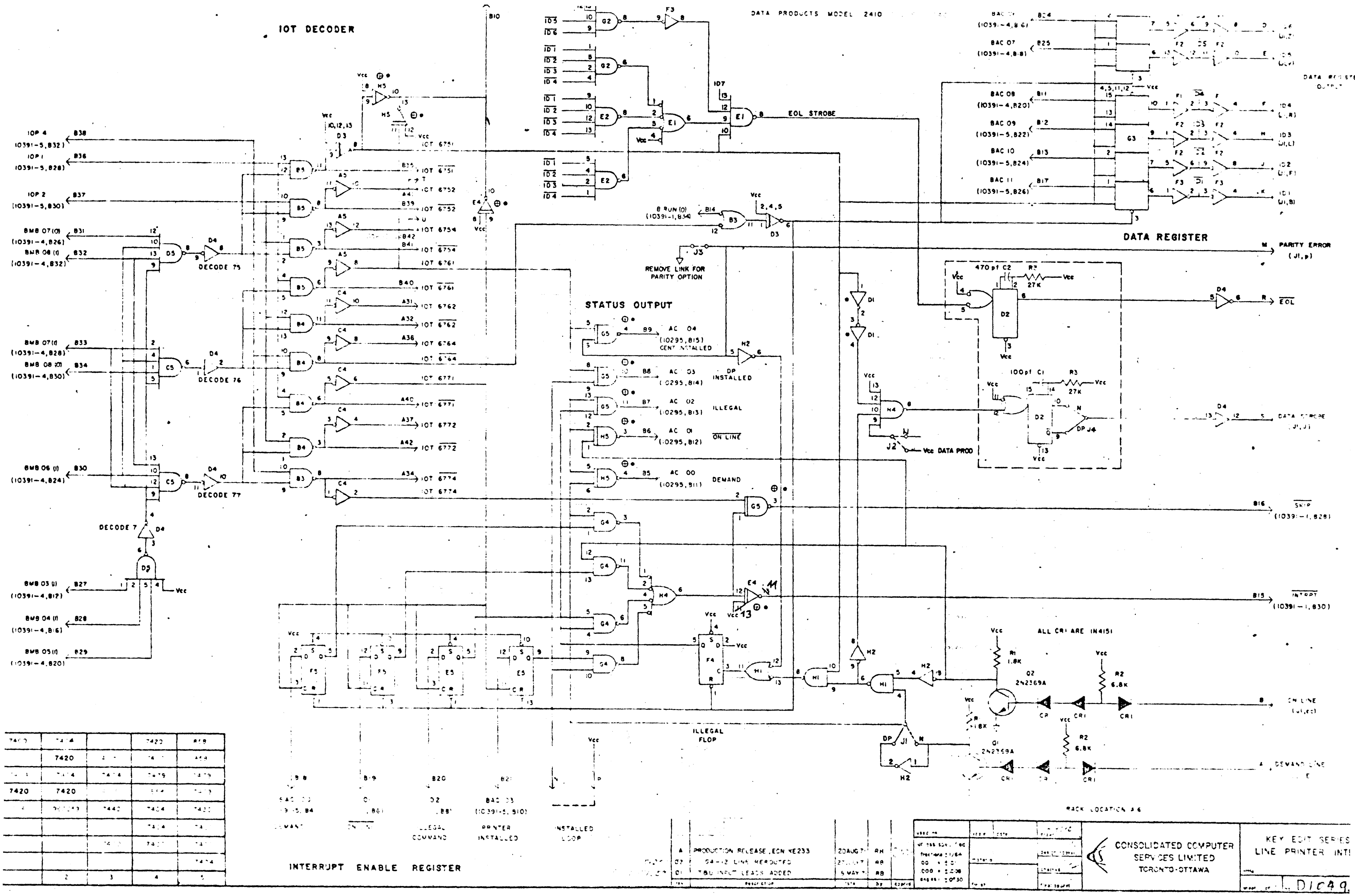


NOTE L

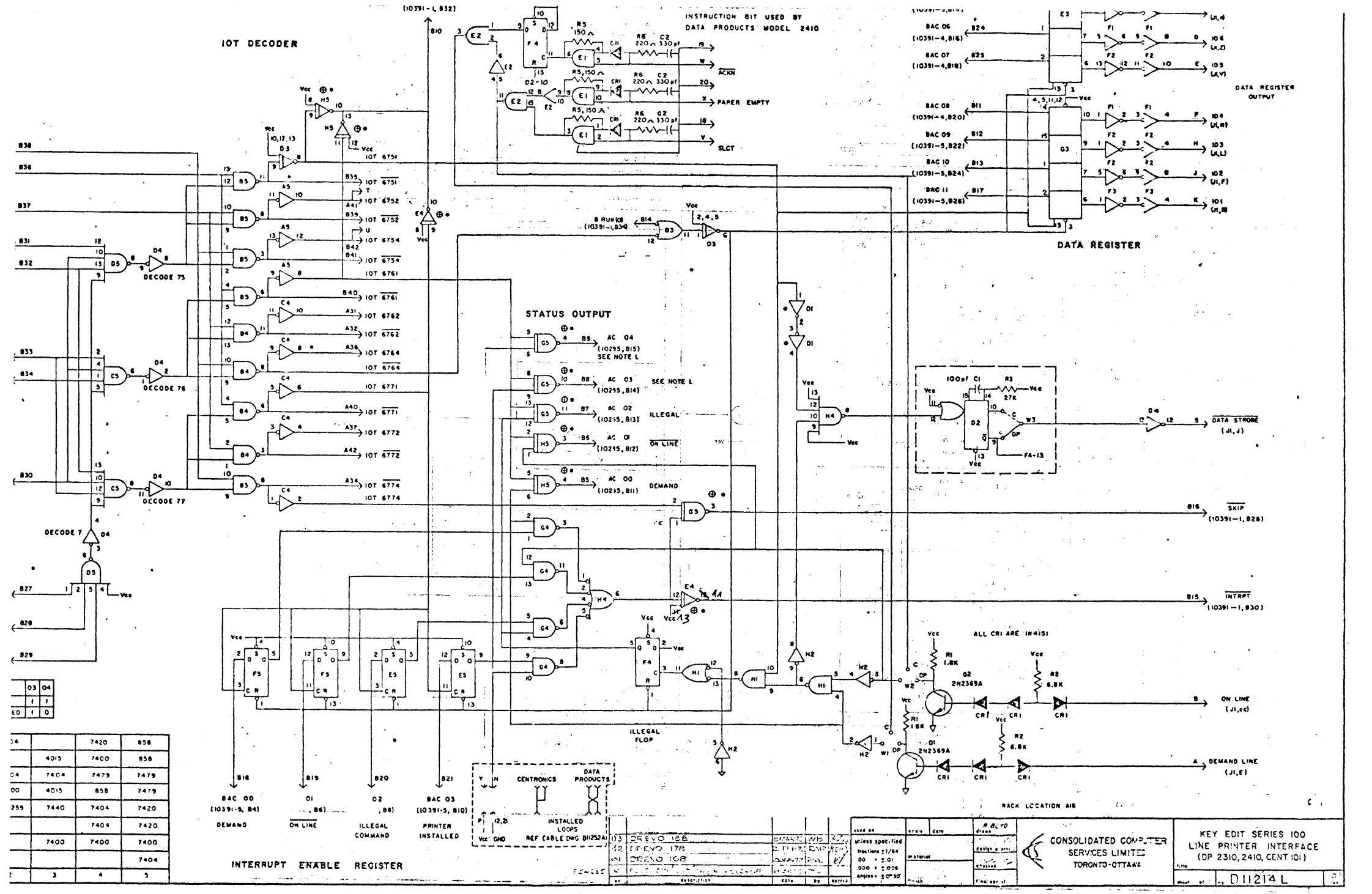
STATUS BITS	03	04
CENTRONICS INSTALLED	1	1
DATA PRODUCTS INSTALLED	1	0

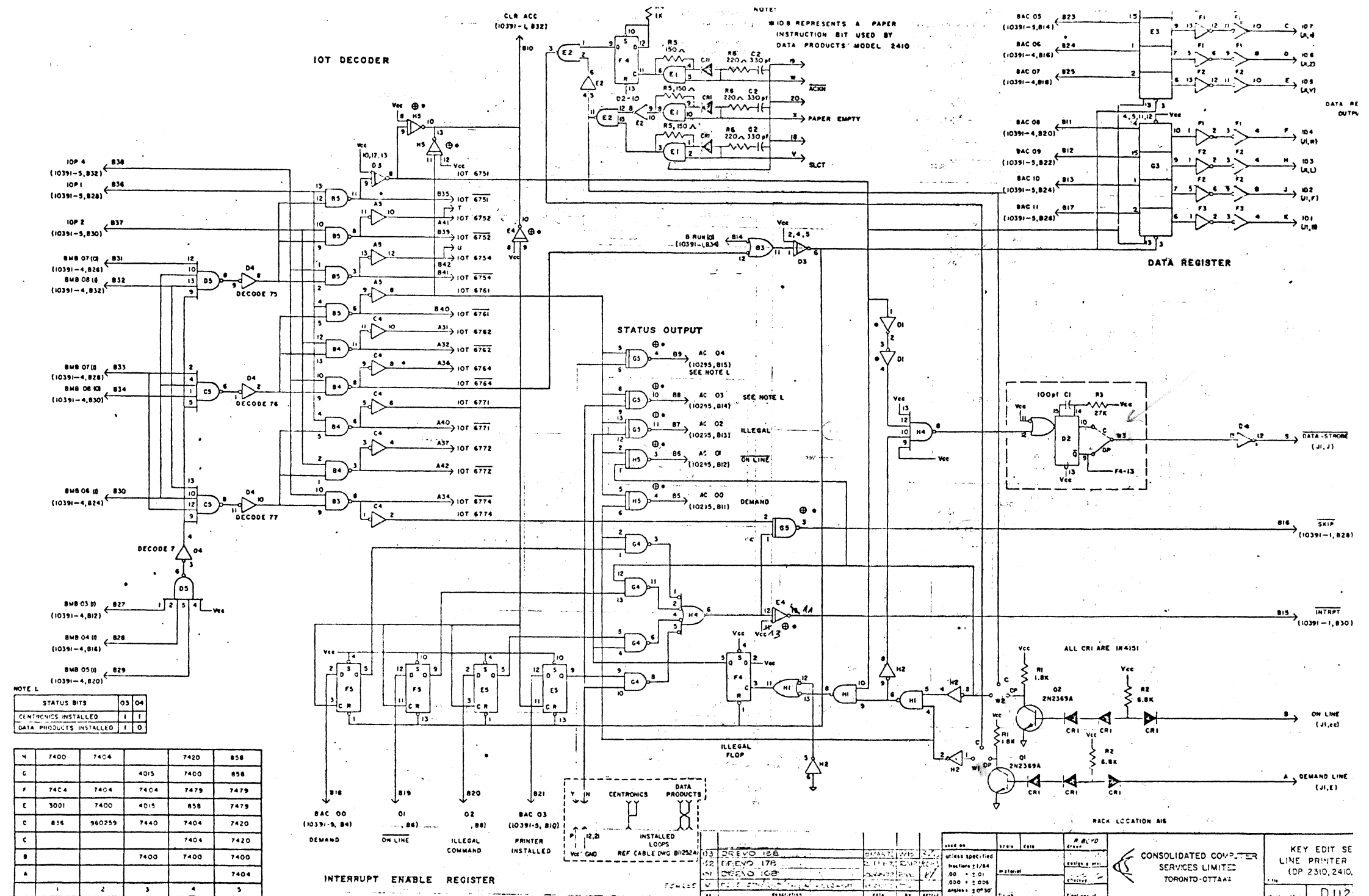
H	7400	7404		7420	858
G			4015	7400	858
F	7404	7404	7404	7479	7479
E	3001	7400	4015	858	7479
D	835	960259	7440	7404	7420
C				7404	7420
B			7400	7400	7400
A					7404
	1	2	3	4	5


IOT DECODER
NOTE
* D6 REPRESENTS A PAPER INSTRUCTION BIT USED BY DATA PRODUCTS MODEL 2410
DATA REGISTER
DATA REGISTER OUTPUT
STATUS OUTPUT
EOL STROBE
REMOVE LINK FOR PARITY OPTION
PARITY ERROR
EOL
DATA STROBE
DP INSTALLED
ILLEGAL
ON LINE
DEMAND
SKIP
INTRPT
ILLEGAL FLOP
ALL CR1 ARE IN4151
DECODE 75
DECODE 76
DECODE 77
DECODE 7
INTERRUPT ENABLE REGISTER
RACK LOCATION A 6
CONSOLIDATED COMPUTER SERVICES LIMITED TORONTO-OTTAWA
KEY EDIT SERIES 100 LINE PRINTER INTERFACE
D10495



IOT DECODER
DATA PRODUCTS MODEL 2410
STATUS OUTPUT
DATA REGISTER
INTERRUPT ENABLE REGISTER
EOL STROBE
DECODE 7
DECODE 75
DECODE 76
DECODE 77
REMOVE LINK FOR PARITY OPTION
PARITY ERROR (J1,p)
EOL
DATA STROBE
SKIP (10391-1,B28)
INTRPT (10391-1,B30)
ON LINE
DEMAND LINE
ALL CR1 ARE 1N4151
ILLEGAL FLOP
DATA REGISTER OUTPUT
DEMAND
ON LINE
ILLEGAL
DP INSTALLED
CENT INSTALLED
ILLEGAL COMMAND
PRINTER INSTALLED
INSTALLED LOOP
RACK LOCATION A6
A PRODUCTION RELEASE, ECN KE233 20AUG7 RH
D2 G4-12 LINE REROUTED RB
D1 TBU INPUT LEADS ADDED 5 MAY RB
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA
KEY EDIT SERIES
LINE PRINTER INT
D1C49


IOT DECODER
INSTRUCTION BIT USED BY DATA PRODUCTS MODEL 2410
PAPER EMPTY
SLCT
DATA REGISTER
DATA REGISTER OUTPUT
STATUS OUTPUT
DECODE 75
DECODE 76
DECODE 77
DECODE 7
AC 04 (10295, B15) SEE NOTE L
AC 03 (10295, B14) SEE NOTE L
AC 02 (10295, B13) ILLEGAL
AC 01 (10295, B12) ON LINE
AC 00 (10295, B11) DEMAND
SKIP (10391-1, B28)
INTRPT (10391-1, B30)
DATA STROBE (J1, J)
ON LINE (J1, cc)
DEMAND LINE (J1, E)
ALL CRI ARE IN4151
ILLEGAL FLOP
BAC 00 (10391-5, B4) DEMAND
01 ,B6) ON LINE
02 ,B8) ILLEGAL COMMAND
BAC 03 (10391-5, B10) PRINTER INSTALLED
CENTRONICS
DATA PRODUCTS
INSTALLED LOOPS
REF CABLE DWG B11252A
INTERRUPT ENABLE REGISTER
RACK LOCATION A16
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA
KEY EDIT SERIES 100
LINE PRINTER INTERFACE
(DP 2310, 2410, CENT 101)
D11214 L



NOTE L

STATUS BITS	03	04
CENTRONICS INSTALLED	1	1
DATA PRODUCTS INSTALLED	1	0

H	7400	7404		7420	858
G			4015	7400	858
F	7404	7404	7404	7479	7479
E	3001	7400	4015	858	7479
D	835	960259	7440	7404	7420
C				7404	7420
B			7400	7400	7400
A					7404
	1	2	3	4	5

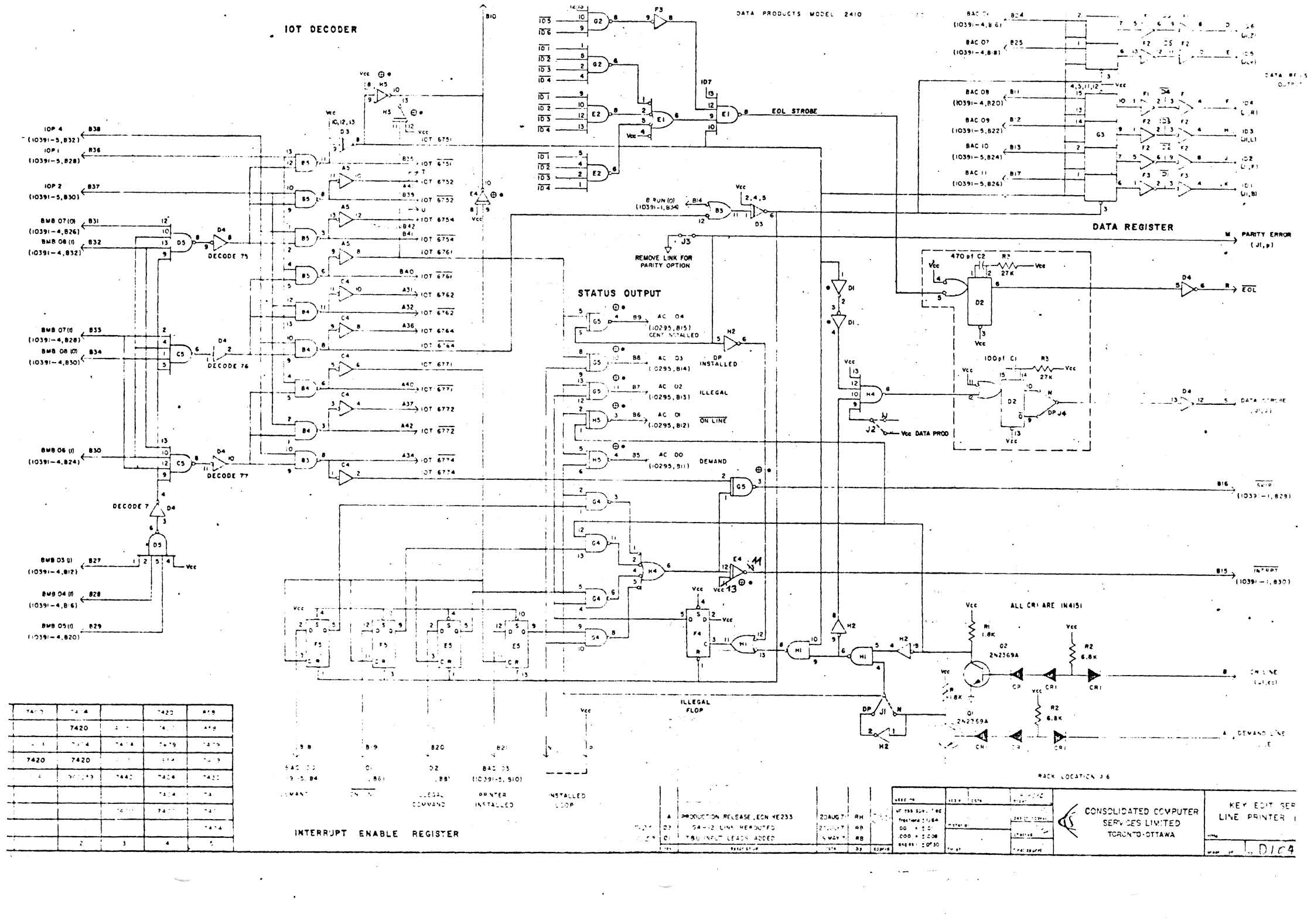
03	DREVO 16B			
02	DREVO 17B			
01	DREVO 16B			
00				
	description	date	by	correct

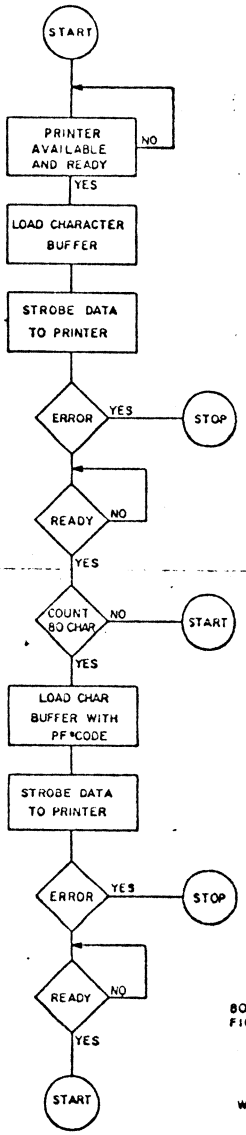
unless specified fractions ±1/64 .00 ± .01 .000 ± .005 angles ± 0°30'

CONSOLIDATED COMPUTER SERVICES LIMITED TORONTO-OTTAWA

KEY EDIT SE
LINE PRINTER
(DP 2310, 2410,

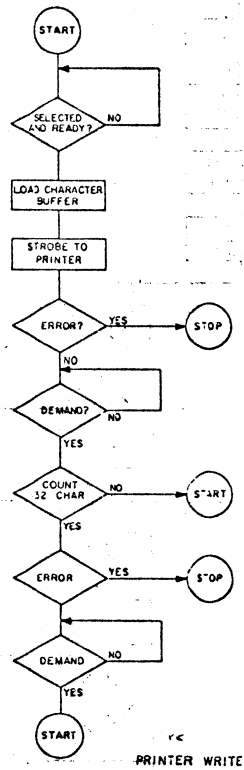
D112


IOT DECODER
DATA PRODUCTS MODEL 2410
DATA REGISTER
STATUS OUTPUT
INTERRUPT ENABLE REGISTER
DECODE 75
DECODE 76
DECODE 77
DECODE 7
EOL STROBE
REMOVE LINK FOR PARITY OPTION
PARITY ERROR
EOL
DATA STROBE
DP INSTALLED
ILLEGAL
ON LINE
DEMAND
PRINTER INSTALLED
ILLEGAL COMMAND
ILLEGAL FLOP
ALL CR1 ARE IN4151
RACK LOCATION 3-6
CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA
KEY EDIT SER
LINE PRINTER I
D1C4

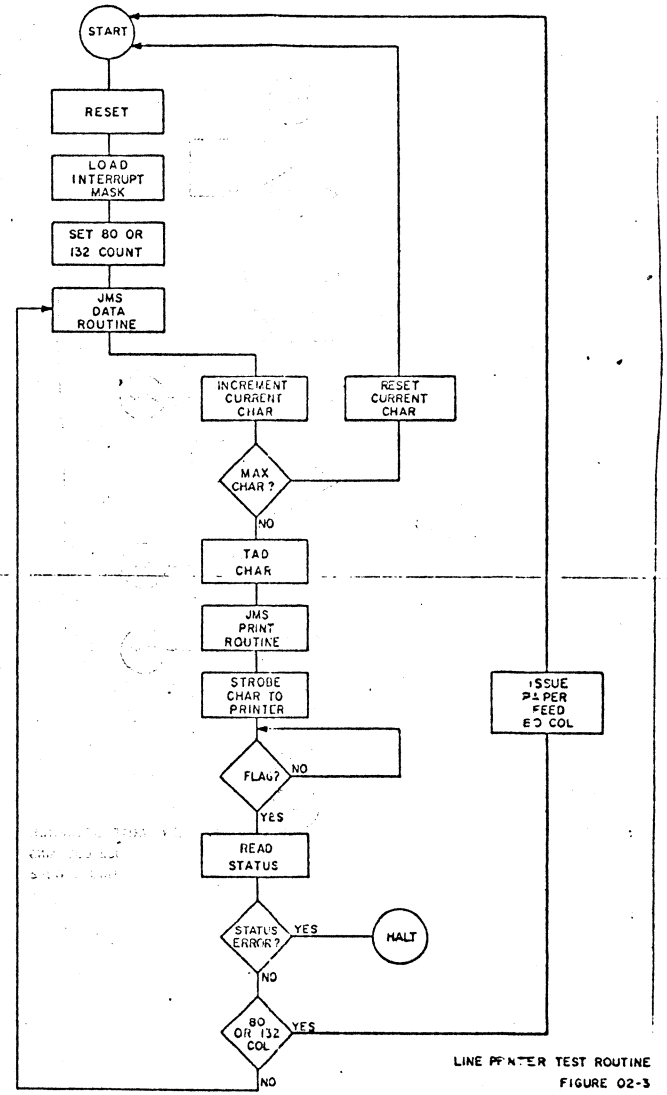


80 COLUMNS
FIGURE 02-1

LINE PRINTER
WRITE SEQUENCE
DIAGRAMS



PRINTER WRITE SEQUENCE
132 COLUMNS
FIGURE 02-2



LINE PRINTER TEST ROUTINE
FIGURE 02-3

CONSOLIDATED COMPUTER LIMITED
OTTAWA

CENTRONIC

APPENDIX D

PARALLEL INTERFACE SPECIFICATIONS

SYSTEM DESIGN SPECIFICATIONS

1.0 SCOPE

This specification covers interconnection requirements between Centronics Model 101 Line Printer and various processors.

2.0 SIGNAL LINE DESCRIPTION

Signals to Line Printer

Name	Description
DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7 DATA 8	Printer information levels, when positive represent binary ones, which form a character being transmitted to the Line Printer Information register, provided DATA 6 or DATA 7 is positive. If DATA 6 and DATA 7 are at ground level, then the code being transmitted, represents a functional operation to the Printer. DATA N must be stable, 0.5 μsec, prior to the leading edge of $\overline{\text{DSTB}}$ and must remain stable, 0.5 μsec, after the lagging edge of $\overline{\text{DSTB}}$. DATA 8 is terminated in the Model 101, but is used as a control bit in the Model 101A.

The first character transferred from the processor to the printer, will be the "most significant digit" (MSD) and shall be printed in the left-most column. Printer utilizes USASCII Transmission Code.

Name	Description
$\overline{\text{DSTB}}$	DATA STROBE, a 0.5 μsec pulse (min) used to clock the data from the processor to the printer logic.

Signals from Line Printer

$\overline{\text{ACKNLG}}$	Acknowledge, a 4 μsec pulse used to indicate the completion of the input of a character into memory or the end of a functional operation.
BUSY	BUSY, a level indicating to the processor that the printer is performing an operation.

PE	A level that is True when the printer is out of paper.
SLCT	A level that is True when the printer is selected.
SS	A level that is True when the Hardware Alarm is tripped.
OSCXT	A 100 KHz (nominal) internal clock.
$\overline{\text{PRIME}}$	A False pulse causes the printer to be primed. (101A ONLY).
$\overline{\text{FAULT}}$	A False level that indicates a Paper Empty, Hardware Alarm, Light Detection, or an unselected condition (101A ONLY).
LIGHT DETECTION	A True level that indicates the video lamp is inoperative (101A ONLY).

3.0 CABLE

The Centronics Model 101 Printer will be supplied with an Amphenol 57 series, 36 pin connector.

4.0 SIGNAL LINE CHARACTERISTICS

Definitions

Logical TRUE

A positive signal is defined as a Logical TRUE or a Logical one. A signal is positive if it is in the range of +2.4 volts to +5.0 volts.

A ground signal is defined as a Logical FALSE or a Logical zero. A signal is negative if it is in the range of +0.4 volt to 0.0 volt.

Level

A signal which is present for two or more clock times or whose pulse width is not critical is defined as a level, for example DATA N TRANSMISSION LINES.

Pulse

A signal whose width is critical is defined as a pulse and the width is specified, for example DATA STROBE PULSE. Pulse width is measured at the +2.4 volt for a true condition and +0.4 volt for a false condition.

Delay Time

Delay time is defined as the relationship between the specified signal at the receiving end of a cable and a reference signal in the receiving unit. It is measured at the +2.4 volt point for a Logical one and +0.4 volt for a false condition.

Switching Time

Switching time is defined as the rise or fall of a signal -- whichever is greater. It is specified between +0.4 volt and +2.4 volts. Unless specified otherwise in the following table, maximum switching time for signals is 0.2 μsec for input or 0.2 μsec for output.

Current Requirements

When a signal to the line printer is positive, the line printer input circuit requires no more than 0.320 ma at +2.4 volts. When a signal from the line printer is positive the driving circuit is capable of supplying a maximum current of 0.320 ma at +2.4 volts.

When a signal to the line printer is negative, the current required by the printer input circuits is 12 ma, current flow being positive to negative.

LINE TERMINATION

A line is terminated in the Line Printer by a 1000 Ohm resistor to +5.0 volt supply.

TIME RELATIONSHIP

The timing diagram enclosed shows the time relationship of the specified signals to and from the printer.

5.0 SIGNAL LINE CHARACTERISTICS TABLE

SIGNALS TO PRINTER				
Name	Printer Connector Pin No. Return No.	Min. Signal Width (μsec)	Max. Switch Time (μsec)	Max. Current From Processor At Positive Signal
DATA 1	Sig. 2 Ret. 20	1.5	0.2	0.320
DATA 2	Sig. 3 Ret. 21	1.5	0.2	0.320
DATA 3	Sig. 4 Ret. 22	1.5	0.2	0.320
DATA 4	Sig. 5 Ret. 23	1.5	0.2	0.320
DATA 5	Sig. 6 Ret. 24	1.5	0.2	0.320
DATA 6	Sig. 7 Ret. 25	1.5	0.2	0.320
DATA 7	Sig. 8 Ret. 26	1.5	0.2	0.320
DATA 8	Sig. 9 Ret. 27	1.5	0.2	0.320
$\overline{\text{DSTB}}$	Sig. 1 Ret. 19	0.5	0.2	0.320
SIGNALS FROM PRINTER				
ACKNLG	Sig. 10 Ret. 28	4	0.2	0.320
BUSY	Sig. 11 Ret. 29	Depends on function being performed. (Ref. Figs. 1, 2, and 3.)	0.2	0.320

6.0 PRIMARY POWER

The printer shall be independently connected to the primary power source and shall contain conversion, regulation, and sequencing equipment required for correct performance.

7.0 GROUNDING

Equipment Ground

The green wire (building ground) of the power cable for the printer shall be securely fastened to the frame. The white wire (neutral A.C.) shall not be grounded to the frame.

D.C. Ground

The shield wire of the interconnecting line, twisted pair shall be grounded to the D.C. ground. This connection shall be made as close as practical to the signal source and load.

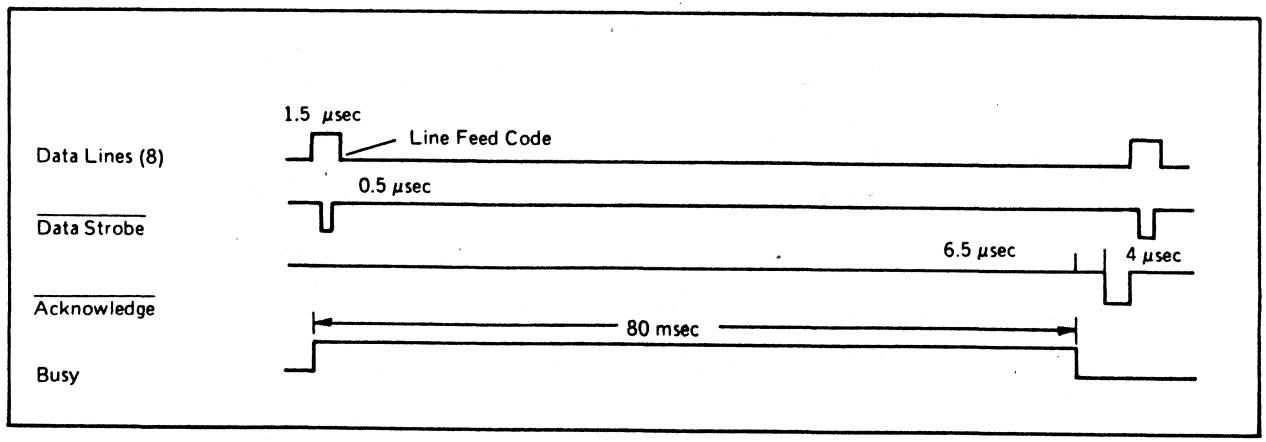


Figure D-1 LINE FEED

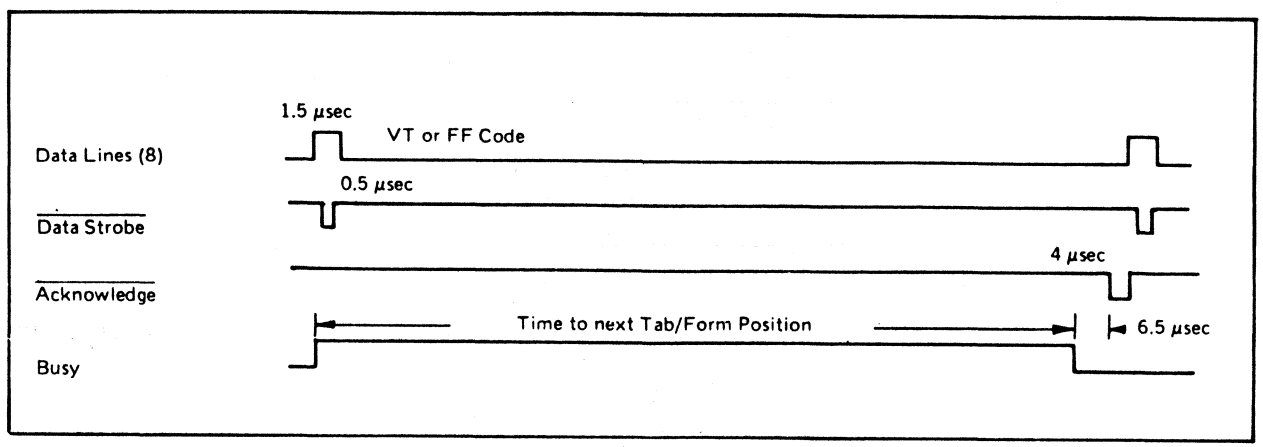


Figure D-2 VERTICAL TAB AND FORM FEED

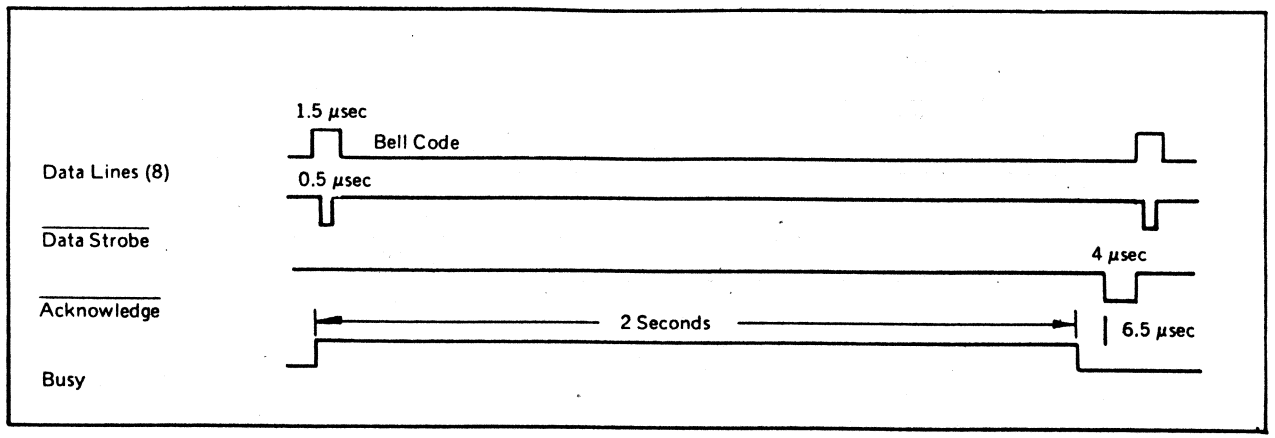


Figure D-3 BELL COMMAND

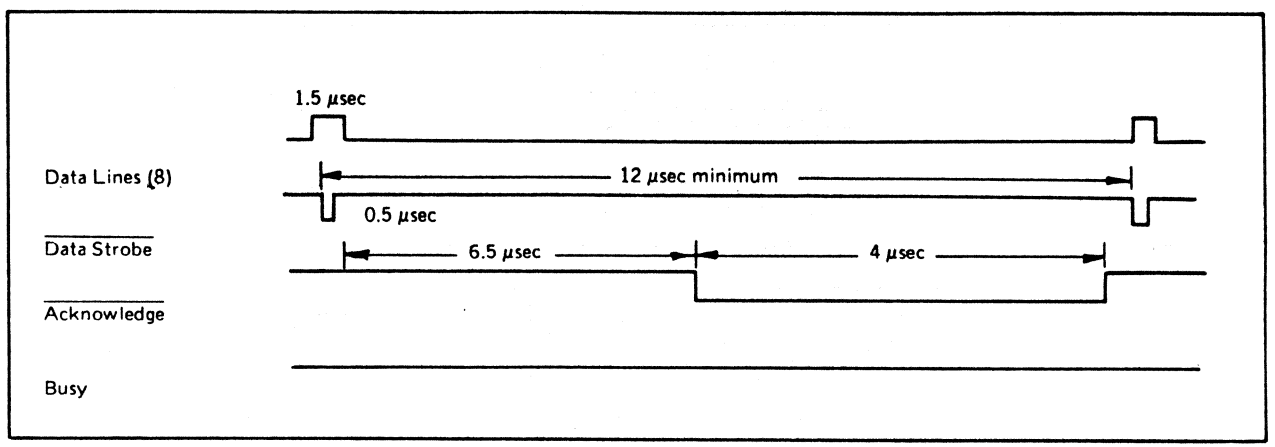


Figure D-4 PARALLEL DATA INPUT TIMING

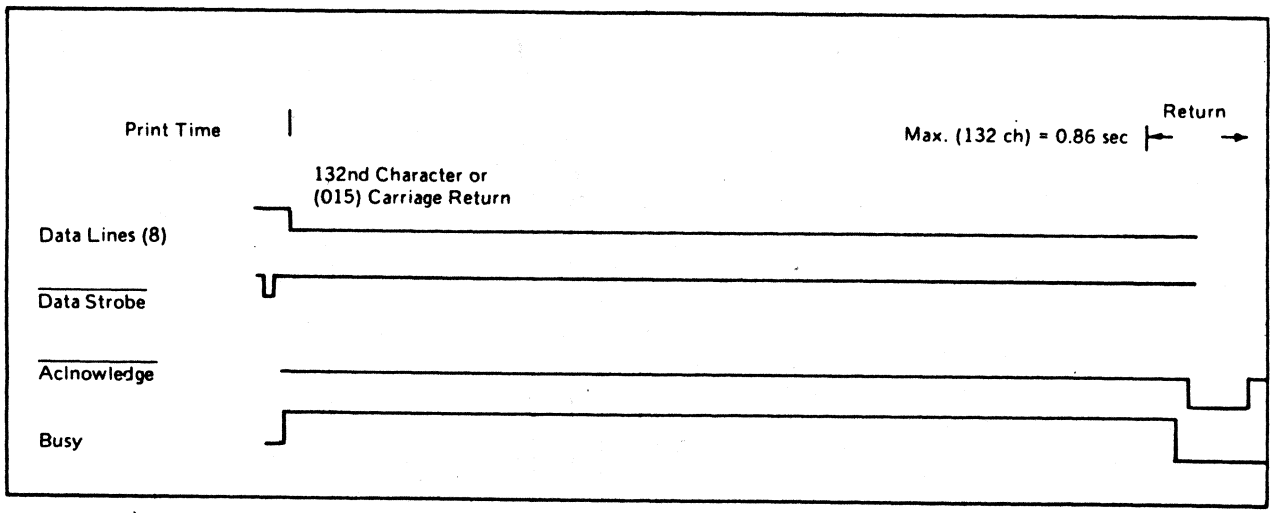


Figure D-5 PRINT TIMING

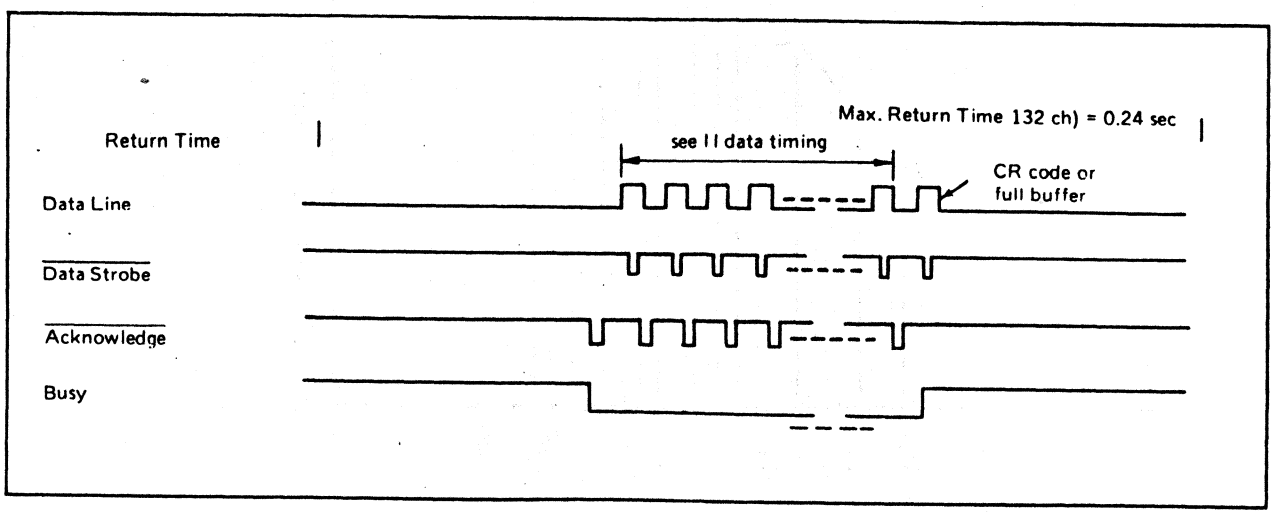


Figure D-6 RETURN TIMING

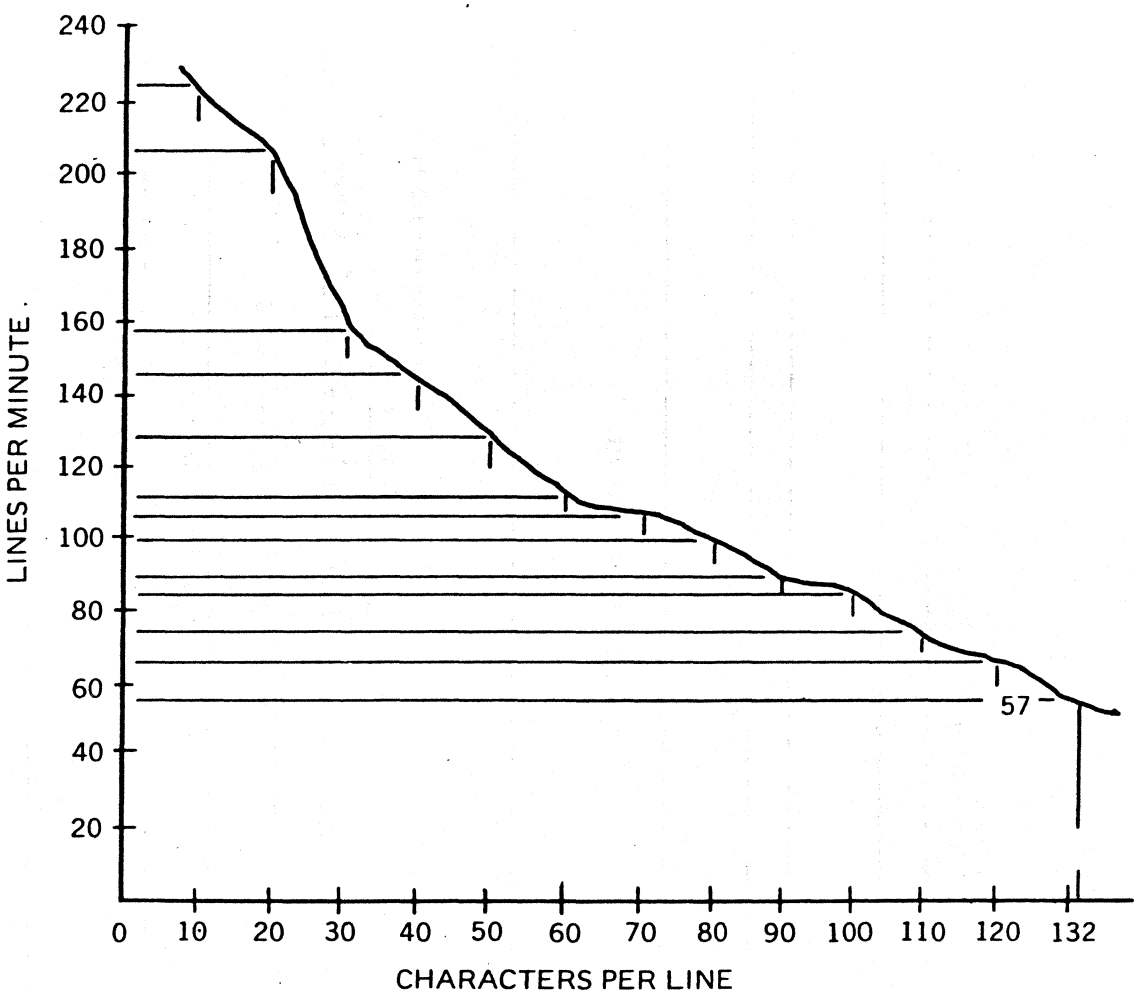


Figure D-7 CHARACTERS PER LINE versus LINES PER MINUTE

VOLTAGE TEST

5 volt	18
Ground	16

PARALLEL INPUT

		Pins	Ground
Data	1	2	20
	2	3	21
	3	4	22
	4	5	23
	5	6	24
	6	7	25
	7	8	26
	8	9	27
Strobe		1	19
Acknlg		10	28
Busy		11	29

PIN	SIGNAL	PIN	SIGNAL
1	DATA STROBE	19	TWISTED PAIR GND
2	DATA 1	20	TWISTED PAIR GND
3	DATA 2	21	TWISTED PAIR GND
4	DATA 3	22	TWISTED PAIR GND
5	DATA 4	23	TWISTED PAIR GND
6	DATA 5	24	TWISTED PAIR GND
7	DATA 6	25	TWISTED PAIR GND
8	DATA 7	26	TWISTED PAIR GND
9	DATA 8	27	TWISTED PAIR GND
10	ACKNLG	28	TWISTED PAIR GND
11	BUSY	29	TWISTED PAIR GND
12	PE	30	PRIME RET (101A ONLY)
13	SLCT	31	PRIME (101A ONLY)
14	SS	32	FAULT (101A ONLY)
15	OSCXT	33	LIGHT DETECTION (101A ONLY)
16	OV		
17	CHASSIS GND	34	
18	5V	35	
		36	

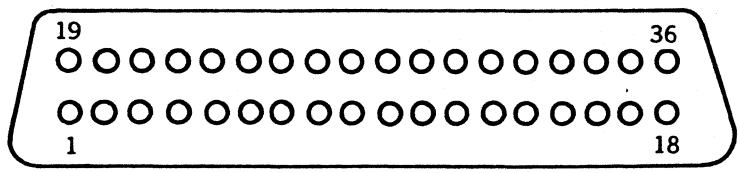
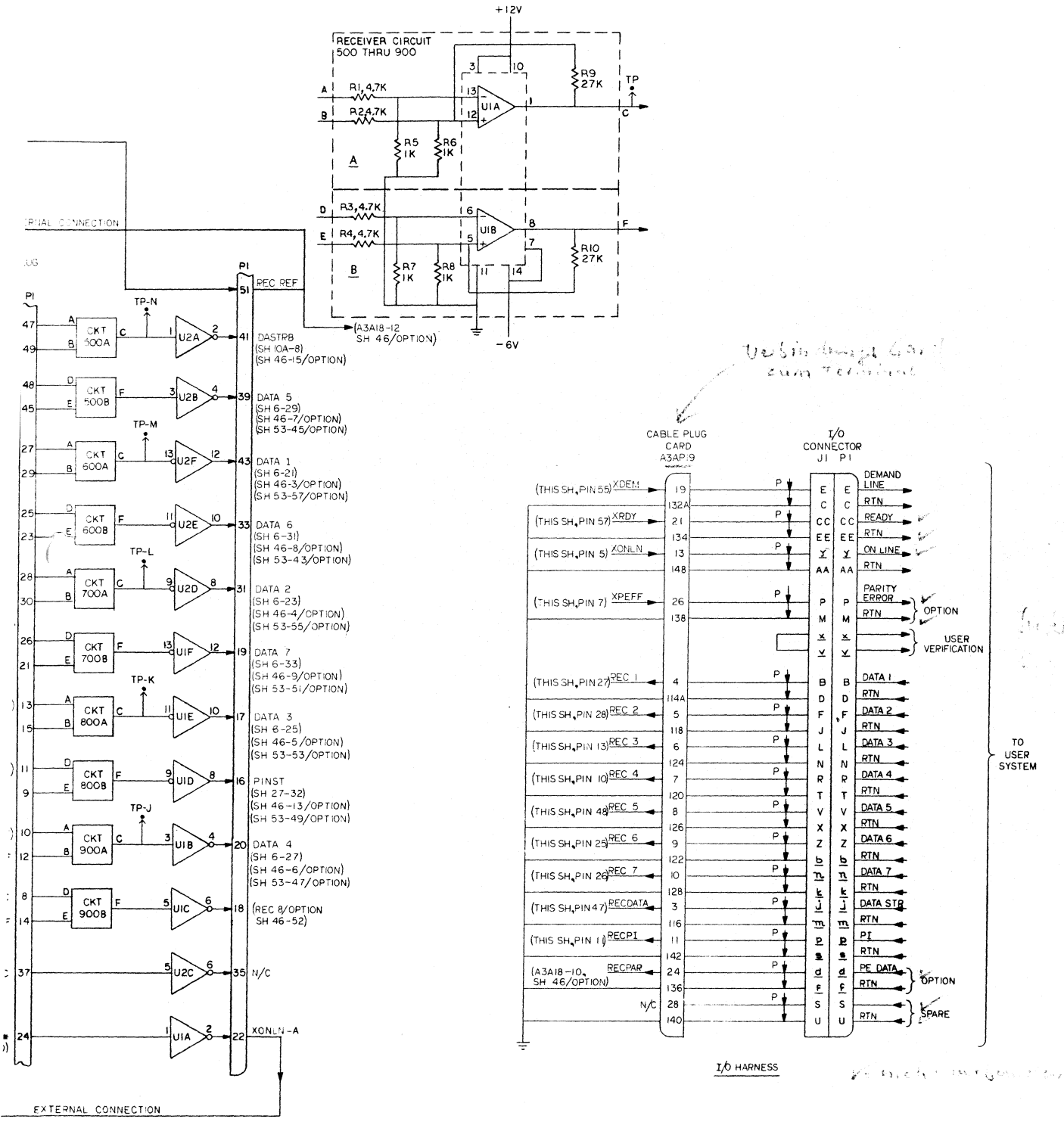


Figure D-8 ELECTRICAL CONNECTOR

DP 2410



LOGIC DIAGRAM SHEET 5
(A3A20 & A3AP19 — ALL MODELS)

data products			
TITLE: AL-25/AL-51 RECEIVER & POSITIVE DRIVER & I/O HARNESS			
SIZE: E	CODE IDENT NO.: 19790	DRAWING NO.: 232454	REV: C
SCALE: NONE	SHEET 1 OF 1		

DEL 2420 SH 9 13 DEM (A) OR SH 53-15
TION MODELS 2440/2470: SH 54-31 DEM B

GENERAL

The Real Time Clock is a Key-Edit optional feature that provides the system time information. It contains a 24-bit asynchronous binary counter which is incremented once a second: it has a maximum time of 2^{23} seconds, or nearly 200 days. The circuitry is contained on one pcb.

The time is read into the accumulator in two 12-bit words. The clock can be reset to zero at any time.

IOT INSTRUCTIONS

6141 Reset clock to zero

6142 Clear accumulator and read least significant byte.
AC 11 is least significant byte.

6144 Clear accumulator and read most significant byte.
AC 00 is most significant byte.

CONTROLLER DETAILS

Clock Generation and Counting

Refer to D10349L; the circuit consists of:

1. Clock Generation - D2, C2, B2, F2
2. IOT Decoding - I5, G2
3. Counter Register - B3, C3, D3, E3, F3, G3
4. Accumulator Gating - B5, C5, D5, E5, F5, G5

Two 6.3 vrms 50/60 hz signals 180^0 out of phase are applied to connector pins A39 and B36 from the line voltage monitor in the logic rack.

Zener diodes CR2 limit the input voltages to +3.9v and -0.6v to protect the logic components; the 470 ohm resistors, R2, limit the current.

The R-S flip-flop D2-8, D2-11 forms a wave-shaping circuit for the out of phase ac input; the circuit is highly immune to noise and line transients. Resistors R1 feed back the output of the flip-flop to the input gates — D2-3 and D2-6 — so that the circuit acts like a Schmitt Trigger. The silicon diodes, CR1, provide a hysteresis of approximately 0.6 volts.

The 4-bit universal counter, C2, can be wired by jumpers to divide either by 10 for 50 hz, or by 12 for 60 hz line frequency. For either frequency C2-9 will provide a 5 hz square wave signal. This output is divided by 5 at counter B2 to provide a 1 hz signal at B2-9 which is inverted and applied to R-S flip-flop F2-11, F2-9. F2-12 is normally high and permits the 1 hz signal to pass through to B3-14 of the Counter Register. The register is arranged in a binary counting sequence so that each circuit divides by 2^4 or 16_{10}. When the clock inputs to the circuits, pins 14, go low the output signals change state.

Data Transfer

The count, or time, stored in the register is gated into the accumulator in two words via the open collector NAND gates, B5 to G5. The least significant word, bits 2^0 to 2^{11} from circuits B3, C3, and D3, is gated by IOT 6142, IOP 2, at connector pin A5. The most significant word, bits 2^{12} to 2^{23} from circuits E3, F3, and G3, is gated by IOT 6414, IOP4, at connector pin A3.

IOR gate F2-6 output will go high during either IOT pulse and permit pin 11 of the F2-8, F2-11 flip-flop to go high if the clock line should change state. Since the register counters change state on the negative slope of the clock, at pins 14, they do not change state during the pulse.

The $\overline{\text{ACC Clear}}$ signal at connector pin B17 (top left) is held low during the IOT pulse time from F2-6 and inverter H2-4. This state causes the data to be jam-transferred into the accumulator.

IOT 6141 at connector pin A7 will reset the register B3 to G3, and the clock, B2 and C2.

CHECKOUT PROCEDURE

It is impractical to check all possible output times up to 200 days, so the following steps 1 to 7 will check the least significant bits and the generation circuitry and steps 8 to 14 will check the remaining possible times or codes. The latter check will require a temporary jumper on the logic rack back wiring.

1. Use the binary loader to load the checkout tape (CCL P/N 1080-914-15) into any field.
2. Ensure pcb 10349 is secure in slot A14.
3. Load address 4050 (of proper field) and start.
4. The accumulator should display the time, with the count increasing at one second intervals.
5. If the accumulator is not changing check all the inputs; connector pins B36, B39, etc.
6. If the accumulator is changing, halt the CPU, load address 4100, and start.
7. The accumulator should display changes at one second intervals.

   If the CPU halts at location 4125 the clock is probably wired for 60 hz operation in a 50 hz system. If it halts at 4132 it is probably wired for 50 hz in a 60 hz system.

NOTE: The following tests will fail if the 8/I CPU cycle time is not between 1.60 and 1.62 μs. The 8/E CPU is not affected; a change to the program caters to the timing difference.

8. Connect a temporary jumper between logic rack locations A14 pin B40 and B23 pin 26. This permits the clock to be advanced by IOT 6501.
9. Disconnect the line voltage monitor 117 vac line (by placing tape over the pcb connector pins A39 and B36).
10. Load address 4000 and start. The CPU should loop for about 3 minutes.
11. If the CPU halts at either 4012 or 4020 there is an error in the least significant word. Location 4040 contains the number that the time should have been.
12. If the CPU halts at 4032 there is an error in the most significant word (bit). Location 4040 contains the number that the time should have been.
13. If the CPU halts at 4035 the clock is functioning correctly.
14. Remove temporary jumper and restore 117 vac to line voltage monitor at end of test.

```
                    /              REAL TIME CLOCK CHECK OUT PROGRAM
                    *4000
4000  7000  START,  NOP                    CCL STOCK NO  1080-914-15
4001  7201          CLA IAC
4002  3236          DCA TIME
4003  3237          DCA COUNT
4004  6141          6141              /  RESET CLOCK
4005  6501  A,      6501              /  ADVANCE CLOCK
4006  6142          6142              /  READ LSW
4007  7041          CIA               /  NEGATE
4010  1236          TAD TIME          /  COMPARE TO TIME
4011  7440          SZA
4012  7402          HLT               /  ERROR LSW
4013  2236          ISZ TIME          /  OK
4014  5205          JMP A             /  ADVANCE
4015  6501          6501
4016  6142          6142
4017  7440          SZA               /  CHECK LSW = 0
4020  7402          HLT               /  ERROR LSW
4021  2236          ISZ TIME
4022  5226          JMP CHK2
4023  6501  B,      6501              /  ADVANCE CLOCK
4024  2237          ISZ COUNT         /  2**12
4025  5223          JMP B
4026  6144  CHK2,   6144
4027  7041          CIA
4030  1236          TAD TIME
4031  7440          SZA
4032  7402          HLT               /  ERROR MSW
4033  2236          ISZ TIME
4034  5223          JMP B
4035  7402          HLT               /  OK
4036  0000  TIME,    0000
4037  0000  COUNT,   0000
                    /
                    /
                    /
                    *4050
4050  6141  START3,  6141             /  RESET CLOCK
4051  6142          6142              /  READ LSW
4052  5251          JMP .-1           /  CHECK LOOP TO SEE
                    /                    IF CLOCK IS COUNTING
                    /

                    *4100
4100  7001  START2,  IAC
4101  3352          DCA EXPTM         /  EXPECTED TIME
4102  6141          6141
4103  7200  CYCLE,   CLA
4104  4336          JMS DELAY1        /  900 MSEC
4105  7200          CLA
4106  1357          TAD TA4           /  20 DEC = 24 OCT
4107  3360          DCA ST3           /  7753
4110  6142  F,      6142              /  READ LSW
4111  7041          CIA               /  NEGATE
4112  1352          TAD EXPTM
4113  7450          SNA               /  OK ?
4114  5326          JMP TIMES         /  YES
4115  7200          CLA               /  NO
4116  1356          TAD TA3           /  7777 - 4255
4117  3353          DCA CNTR          /  = 3522
4120  6142          6142              /  READ LSW
4121  2353          ISZ CNTR          /  (3.22 + 1.61)2070 ,  DEC
4122  5321          JMP .-1           /  10 MSEC
4123  2360          ISZ ST3
4124  5310          JMP F
4125  7402          HLT               /  CLOCK TOO SLOW
4126  1360  TIMES,   TAD ST3
4127  7041          CIA
4130  1357          TAD TA4
4131  7450          SNA               /  CLOCK TOO FAST ?
4132  7402          HLT               /  YES
4133  2352          ISZ EXPTM         /  NO
4134  5303          JMP CYCLE
4135  7402          HLT               /  RTC OF
4136  0000  DELAY1,  0000             /  900 MSEC
4137  1355          TAD TA2           /  90 DEC = 132 OCT
4140  3361          DCA ST2           /  7645
4141  7200  C,      CLA
4142  1356          TAD TA3           /  2070 DEC = 4026 OCT
4143  3353          DCA CNTR          /  3751
4144  6142          6142              /  READ LSW
4145  2353          ISZ CNTR          /  (3.0 + 1.5)2222 ,  DEC
4146  5345          JMP .-1           /  = 10 MSEC
4147  2354          ISZ ST2           /  X90 DEC
4150  5341          JMP C             /  = 900 MSEC
4151  5736          JMP I DELAY1
4152  0000  EXPTM,   0000
4153  0000  CNTR,    0000
4154  0000  ST2,     0000
4155  7645  TA2,     7645   ___  7636
4156  3751  TA3,     3751        3470   for 8/E
4157  7753  TA4,     7753   ___  7747
4160  0000  ST3,     0000
```

	1	2	3	4	5
I					7430
H		858			
G		846	7493		858
F		7400	7493		858
E		7440	7493		858
D		7400	7493		858
C		4023	7493		858
B		4023	7493		858
A					

TEST POINT 1 B40

ACC CLEAR (10391-1,32) B17

ACC GATING

AC 11 ,26) B30 — AC 10 ,24) B31 — AC 09 ,22) B28 — AC 08 ,20) B29 — AC 07 ,18) B26 — AC 06 ,16) B27 — AC 05 ,14) B24 — AC 04 ,12) B25 — AC 03 ,10) B22 — AC 02 ,8) B23 — AC 01 ,6) B20 — AC 00 (10391-1,4) B21

B5 · C5 · D5 · E5 · F5 · G5

2^0 2^4 2^8 2^{11} 2^{12} 2^{16} 2^{20} 2^{23}

COUNTER LSB

REGISTER MSB

R3 2K Vcc

B3 → BMB 3(0) (10391-4,10)
B4 → BMB 4(0) (10391-4,14)
B5 → BMB 5 (1) (10391-4,20)
B6 → BMB 6 (1) (10391-4,24)
B7 → BMB 7(0) (10391-4,26)
B8 → BMB 8 (0) (10391-4,30)

Vcc

IOT 14 DECODING

A7 → IOP 1 IOT 6141 RESET CLOCK (10391-5,28)
A5 → IOP 2 IOT 6142 LSB (10391-5,30)
A3 → IOP 4 IOT 6144 MSB (10391-5,32)

CLOCK GENERATION

÷5 B2 ÷10 OR/C2 ÷12 C2

50 HZ 60 HZ

R1 180Ω R2 470Ω CR1 IN4151 CR2 IN4730 (3.9V)

A39 → L1 (AC 2)

50/60 HZ J3 POWER PLUG

B36 → L2 (AC 1)

RACK LOCATION A14

rev	description	date	by	apprvd
01	DREVO 176	3MAR72	WB	

D10152A used on

unless specified
fractions ± 1/64
.00 ± ±.01
.000 ± ±.005
angles ± ±0°30'

scale — date

material

finish

R. BOYD drawn

design apprvl

checked

final apprvl

CONSOLIDATED COMPUTER SERVICES LIMITED
TORONTO-OTTAWA

title: REAL TIME CLOCK

sheet 1 of 1 no. D10349L 01

Replace Title Page with Revision 2 Title Page attached.

SECTION 2

Logic Drawings

D10295L, bottom right - amend Revision box (Ø) to read B.

D10300L - insert Revision B, attached, immediately after Revision A1 in the manual.

D10362L - remove Revision D, pages 1 and 2, and replace with Revision E, pages 1 and 2, attached.

D10482L, bottom right - amend Revision box (Ø) to read A.

D11075L, bottom right - amend Revision box (A) to read B.

SECTION 3

Page 3-9, "Write Data", para 5, line 3 - amend the sentence to read

"The trailing edge of pulse 11 conditions counter J4-5 pin 6; I5-3 goes true to I5-6 and I3-11 goes true to I2-6 to condition the register in a load mode."

Page 3-11, "READ DATA", para 6, 2.a - amend to read

"increment the counter via connector pin 6, I1-4, I1-6, F2-8, A2-3, A2-13, G4-8, and G3-8."

Page 3-11, "READ DATA", para 6, 2.b - amend to read

"issue clocks to the Shift Register via F2-8, A2-3, A2-13, and G2-8, pins 9 and 10..."

SECTION 3

Logic Drawings

D10282L, bottom right - amend Revision box (B) to read C.

D10284L - remove Revision A and replace with Revision D, attached.

SECTION 5

Remove page 5-21 and replace with Revision 2 page 5-21, attached.

Logic Drawings

D10246L, bottom right - amend Revision box (D) to read E.

D10285L - remove Revision C and replace with Revision G, attached.

D10298L - remove Revision Ø and replace with Revision B, attached.

D10366L, bottom right - amend Revision box (Ø1) to read B.

D10368L - remove Revision Ø and replace with Revision C, attached.

D10442L - remove and replace with B10442L, Revision G, attached.

SECTION 6

Replace Contents Page with Revision 2 Contents Page, attached.

Logic Drawings

D11155B - remove Revision Ø2 and replace with Revision B attached.

D11089S, bottom right - amend Revision box (Ø4) to read A.

D11240S, bottom right - amend Revision box (Ø) to read A.

D11197B - remove Revision Ø2 and replace with Revision A attached.

B11061S, bottom right - amend Revision box (Ø1) to read A.

B11034S, bottom right - amend Revision box (Ø1) to read A.

D10363S - remove Revision E and replace with Revision F attached.

D10283S, bottom right - amend Revision box (A) to read B.

D10185S, bottom right - amend Revision box (C) to read D.

SECTION 7

Logic Drawings

D11046I, bottom right - amend Figure No. (7-2) to read 7-3;
amend Revision box (Ø2) to read C.

B11154X - remove Revision Ø1 and replace with Revision A attached.

SECTION 8

Replace Contents Page with Revision 2 Contents Page attached.

Integrated Circuit Pin Numbering -1, box MC 858 - add at bottom of box the following statement:

'OFTEN USED WITH SEPARATE GND'.

Integrated Circuit Pin Numbering -1, box DM 1584 or MC 8820 - amend title of box to read

'MC 1584 or DM 8820'.

Integrated Circuit Pin Numbering -4, box MC 7493 - amend statement at bottom of box to read

'RESET IS HELD AT 0 FOR SHIFTING: AT 1 TO RESET COUNTER ....'

Integrated Circuit Pin Numbering -6, box MC 8602, O/S1 - delete the bar over the upper Q, and add a bar over the lower Q.

Integrated Circuit Pin Numbering -6, box MC 8602, O/S2 - delete the bar over the upper Q, and add a bar over the lower Q.

After Systems Test Programs, Part 13, Drum Analyser, insert Part 14, MTT Analyser, attached.

Wiring Diagram B11038W - remove sheets 1-2, 3-4, 5-6, 11-12, 23-24, 27-28, Revision B, and replace with sheets 1-2, 3-4, 5-6, 11-12, 23-24, Revision D, 27-28, Revision E, attached.

OPTIONS

Remove Options Contents Page and replace with Revision 2 Contents Page attached.

System No:
Change Inserted by:
Date:

Revision 1 May 72
CHANGE INSTRUCTIONS TO
KEY-EDIT TECHNICAL MANUAL
SERIES 100/100 MKV, 100/85 Mk1

PAGE CHANGES

TITLE PAGE Replace existing Title Page with Revision 1 Title Page attached.

SECTION 2 Replace existing page 2-10 with Revision 1 page attached.

D 10362 L. Replace Sheets 1 and 2 with Revision D sheets attached.

D 11075 L. Replace drawing with Revision A attached.

SECTION 3 Replace drawings 10282 L, 10284 L, and 10262 L with Revision B, A, and A, respectively

SECTION 5 Replace drawing 10246 L with Revision D attached.

SECTION 6 Replace existing page 6-1-1 with Revision 1 page attached.

Replace Figure 6-1-5 with Figures 6-1-5a and b attached (C11356S and C11355S).

Replace Figure 6-2-2 with Revision A attached.

After Figure 6-2-5 insert Figure 6-2-6a attached.

SECTION 8 Replace Contents page with Revision 1 page attached.

Before the Logic Rack Wiring diagrams, D11038W Sheet 1, insert the attached Drum Analyser consisting of contents page to program listing page 81 (30 sheets)

OPTIONS Replace Contents page with Revision 1 page attached.

MANUSCRIPT CHANGES

SECTION 2 D10300L. End of Record Beeper, junction of pin 14 and resistor (22K) goes to Vcc.

SECTION 6 Figure 6-1-4. Locate NEON LAMP OFF; draw a horizontal line from the right end of the resistor to the next vertical line (the LOAD line).

Above NEON LAMP ON delete NEUT.

Beneath drawing delete CABLE NO.

Figure 6-2-6 (after Figure 6-2-6a). Change figure number to 6-2-6b.

Delete ALSO 10395 above figure number.

Delete NOTE at bottom left, and all of 220/240 TERMINAL BOARD INTERCONNECTIONS table

Top left, change Cannon P/N for 1004S Drum to read PW06B-12-3-5; and for 1016 Drum to read PT06A-16-8S

Insert the System Number on the manual Title Page (where applicable)

Insert the System Number, the date, and your name on the change Title Sheet Retain this sheet at the back of the manual.