PART 2 MK 1 DATA TERMINAL

PART 2A MK 2 DATA TERMINAL

PART 2
KEY DATA TERMINAL

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ILLUSTRATIONS

KEY DATA TERMINAL

INTRODUCTION

Purpose

The Key Data Terminal (KDT) is the data entry station of the KEY-EDIT Series 50 system. The KDT consists of two functional units: a keyboard and a video display unit (VDU). The system receives data entered through the keyboard and transmits data to the operator via the VDU.

The KDT is interfaced to the system by the KDT Controller. Figure 2-1 illustrates the position of the KDT in the system. A maximum of 32 KDTs can be connected to the controller; eight on each of four VCU Terminal Control pcbs. However, current software requirements limit each system to a total of sixteen terminals.

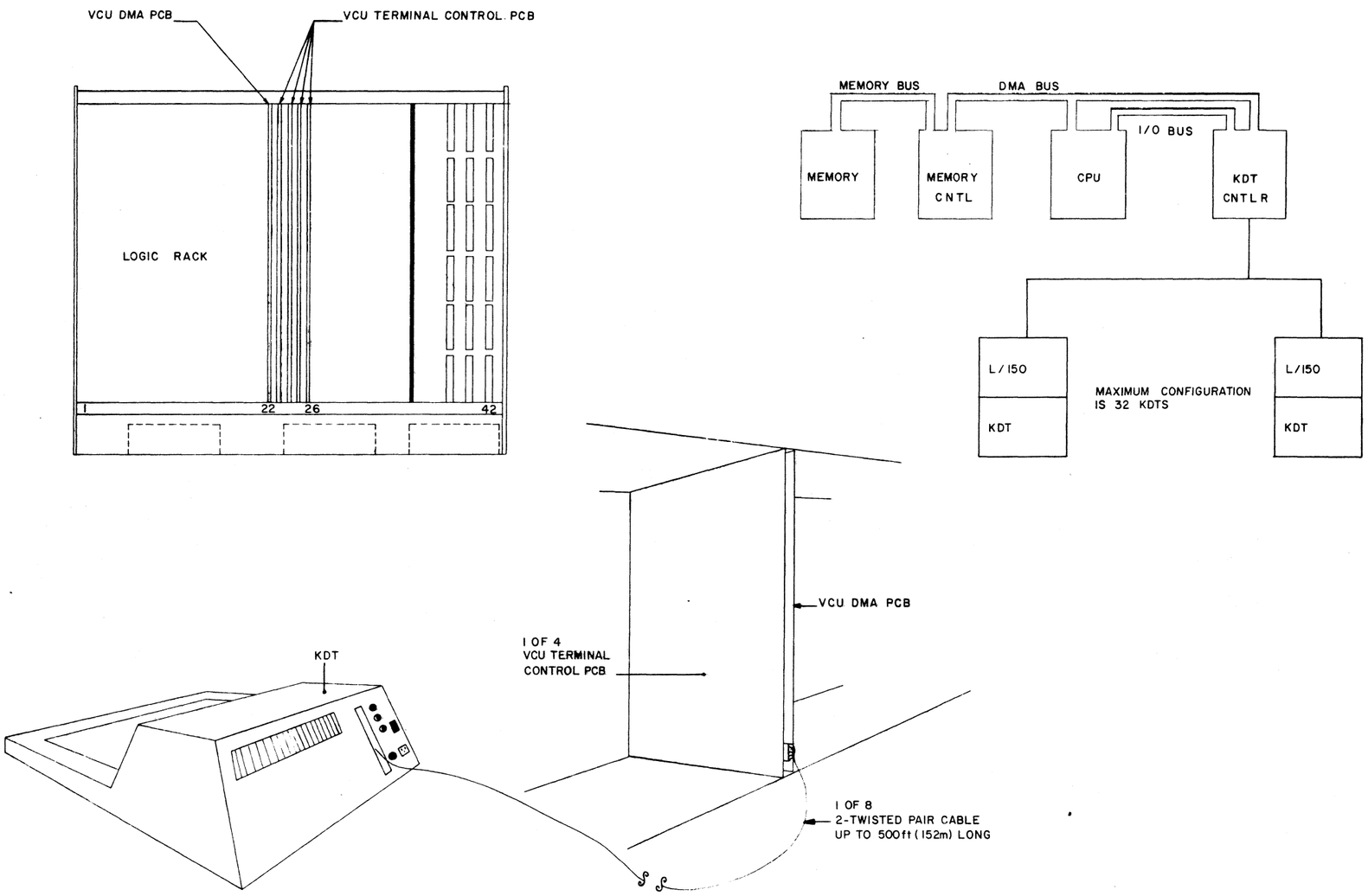


FIGURE 2-1
KDT CONFIGURATION

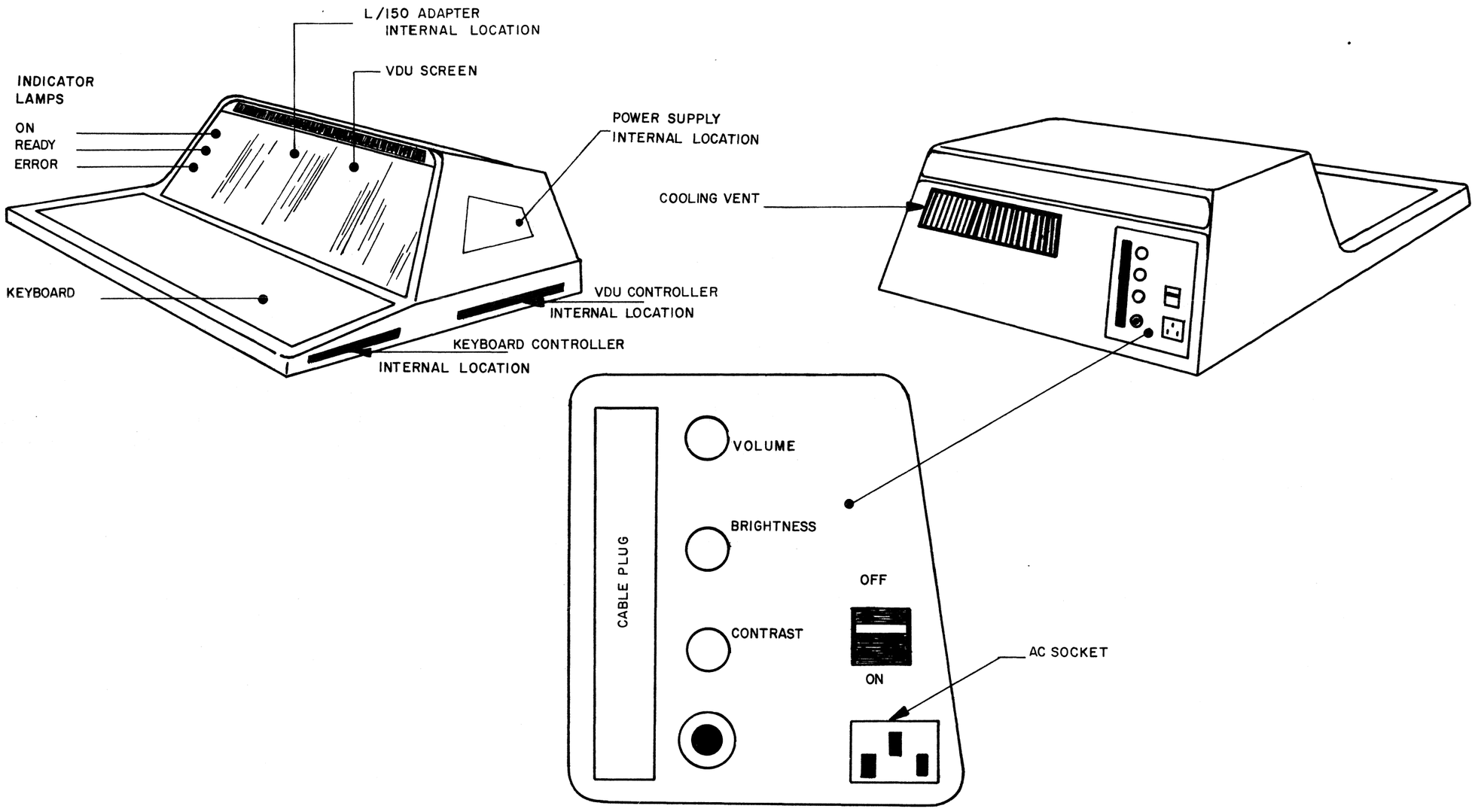


FIGURE 2-2
KEY DATA TERMINAL

CONFIGURATION

The KDT contains:

- Keyboard
- Video Display Unit (VDU)
- Keyboard Controller, SK 11840
- VDU Controller, SK 11535
- Power Supply, SK 11577
- L/150 Adapter

Figure 2-2 illustrates the major units and the KDT operator controls. These three controls adjust the volume of the signal tones, and the brightness and contrast of the Video Display Unit. The KDT status is displayed by three indicator lamps on the left side of the graphic display front panel.

FUNCTION

Figure 2-3 illustrates data flow between the major units in the KDT. Basically, the data entered by the operator from source documents is assembled into data words for transfer to the system by the Keyboard Controller. The VDU Controller accepts data from the system and displays it on the VDU screen, permitting the system to communicate with the operator. The L/150 Adapter converts parallel data from the KDT into serial data that can be accepted by the KDT Controller, and vice versa. (Refer to Part 3.)

POWER

All voltages required to operate the controller logic and the VDU are generated by a self-contained power supply, SK 11577. The required voltages are +15, +5, -9, and -12 V.

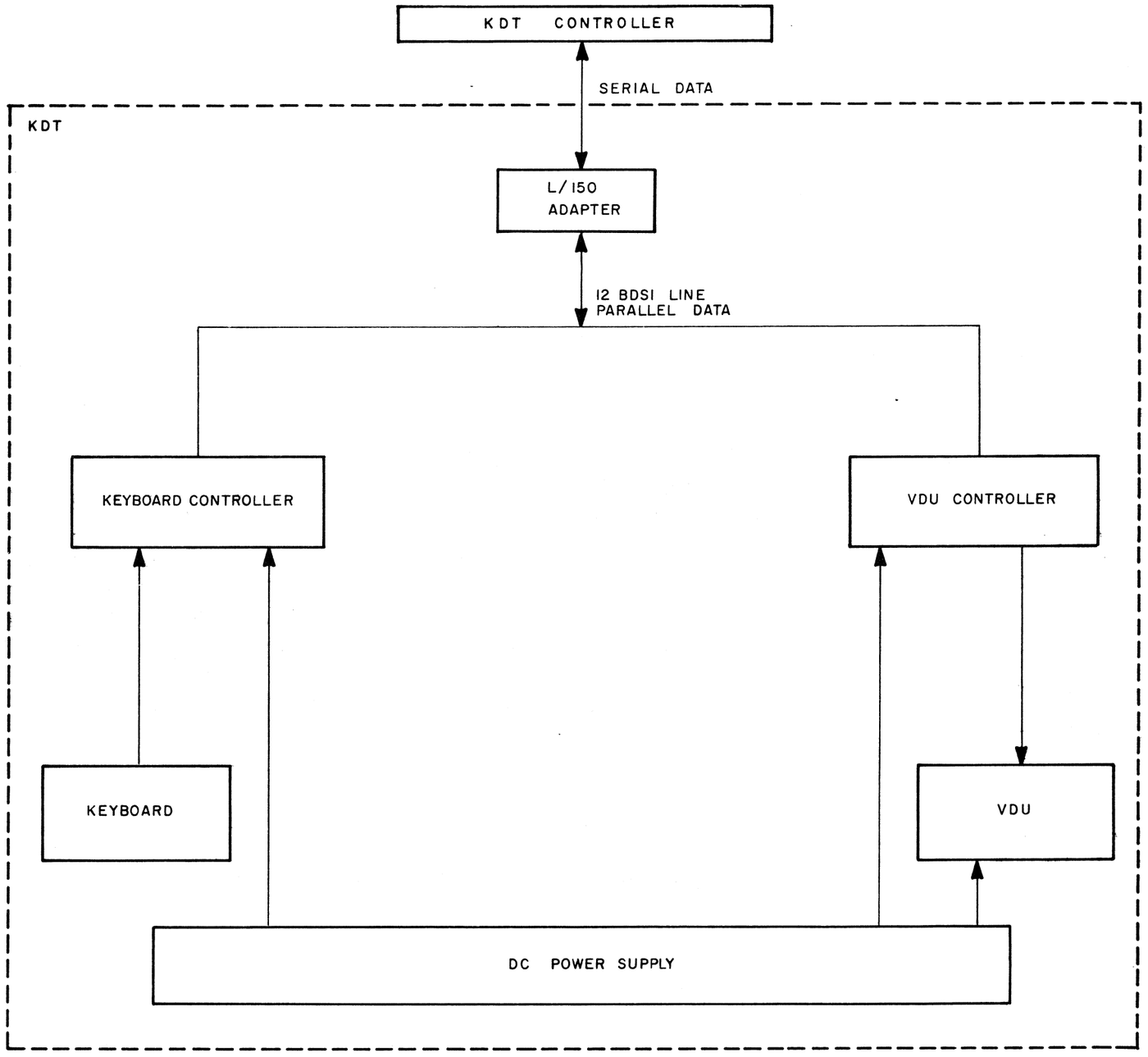
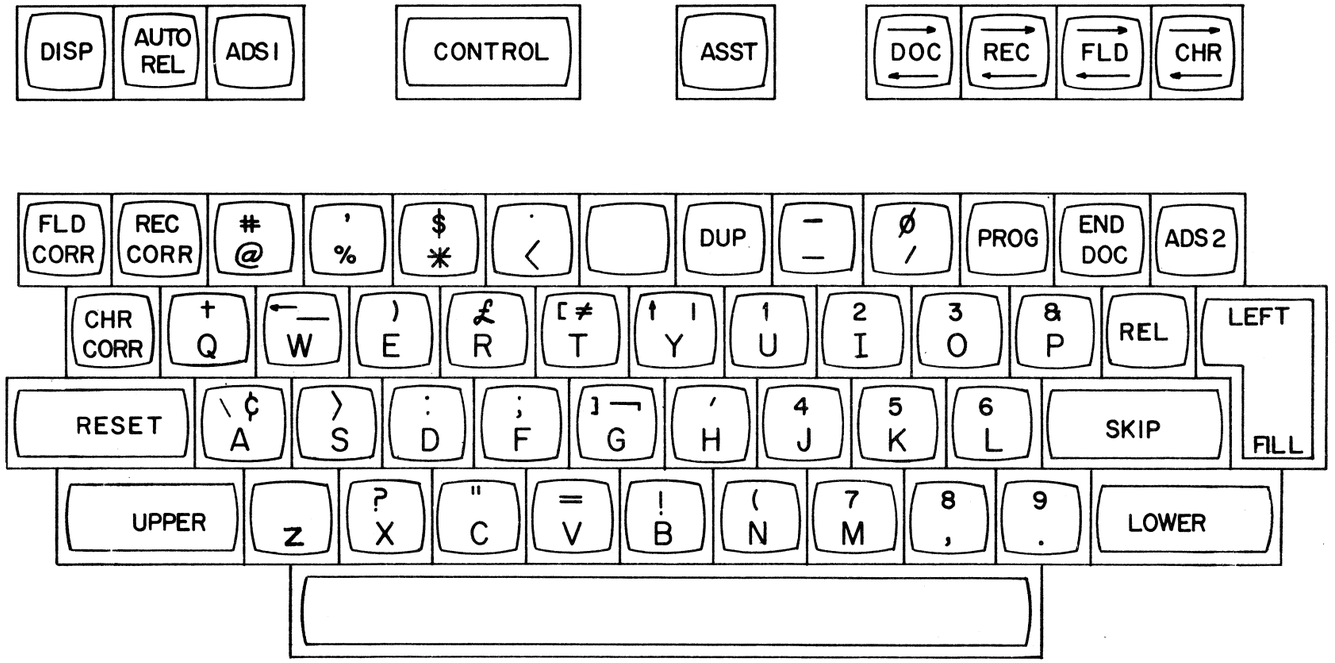


FIGURE 2-3
DATA FLOW



FOR NOTES SEE SHEET 4

rev	eco	description	date	by	chk	apprvd
3		SEE SH 1				
2		SEE SH 1				
1	35 173	PRE PROD RELEASE	16APR73	EL	GB	NJW

used on SLB13042A
drawn E.L
scale NTS
date 16 APR 73
design ENG D WALSH
checked
unless specified
00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
final apprvl
material
finish

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title: ASSEMBLY KEYBOARD DATA TERMINAL SERIES L PHASE I & II

sheet 3 of 6
no. SLC13046A
3 rev

TRANSTEX 15 500-8-72

KEYBOARD CONTROLLER

Introduction

The Keyboard Controller is a single pcb mounted in the KDT beneath the keyboard. The controller has three modes of operation:

- assembly of data words as the operator strikes keys, and transfer of data to a KDT controller
- acceptance of commands from the CPU
- error detection.

Operation

DATA TRANSFER

The KDT uses a scanning Keyboard Controller to encode data entered by the operator. The data generated is most accurately described as the address of the key that has been depressed. Figure 2-4 illustrates the addresses of each key position in the keyboard. Drawing 13046A illustrates keytop configuration. The system software uses these addresses in a look-up table to extract the required data word.

Each key on the keyboard is connected to a crosspoint in a diode matrix. A scanner in the controller compares the output of each crosspoint with the output of that crosspoint on the previous cycle. If the two signals are different, the scanner clock is stopped and another clock is enabled to produce KEYSTROBE (KSTB), the pulse that loads the Data Buffer with the crosspoint address and initiates a data transfer.

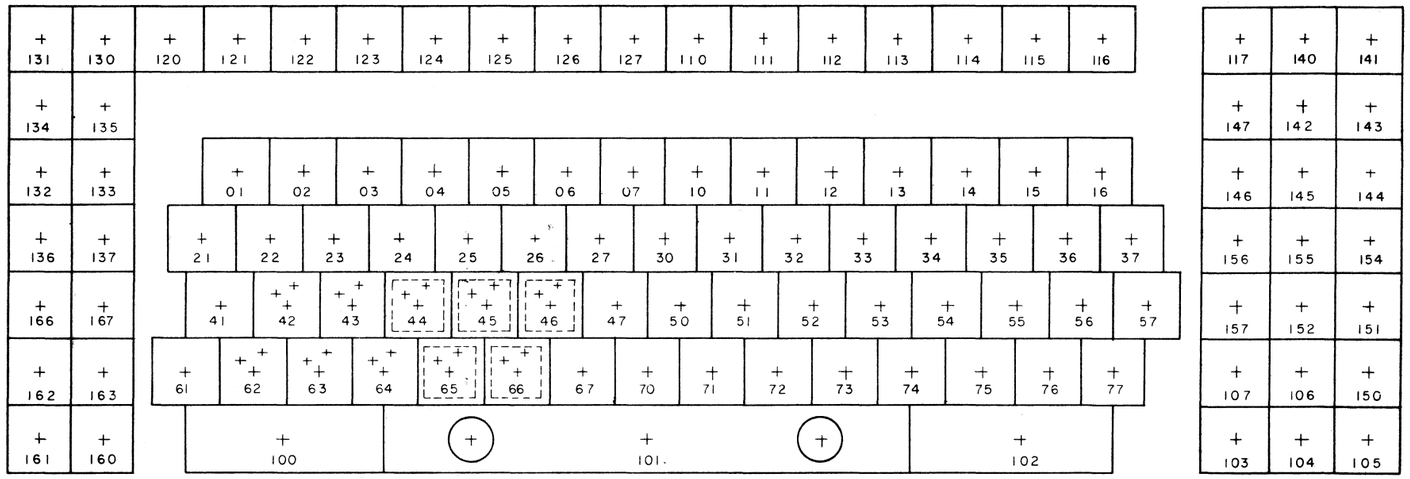


FIGURE 2-4
KEY CODES

A data transfer involves two signals that perform handshaking between the Keyboard Controller and the L/150 Adapter. These are DATA AVAILABLE (DAV-X) and DATA ACKNOWLEDGE (DAK-X). When KSTB pulses, a data word appears on the data lines DL00-X to DL07-X, and DAV-X enables. The L/150 responds to DAV-X with DAK-X and strobes the data into an input buffer. Figure 2-5 illustrates data transfer timing.

COMMAND MODE

The Keyboard Controller contains a command register that controls the keyboard mode of operation and generates the tones that signal errors.

When a command is transmitted to the keyboard, the lines used are six of the data lines, DAV-X, DAK-X, and the three command lines, COMMAND BIT (CMDB), COMMAND SET (CMDS) and COMMAND RESET (CMDR). The L/150 first uses the command lines to perform BUS BUSY (BBSY-X) handshaking. This ensures that a Keyboard Controller is connected to the L/150. The rest of the sequence is a DAV/DAK data transfer from the L/150 to the controller. Figure 2-6 illustrates the timing of a command transfer.

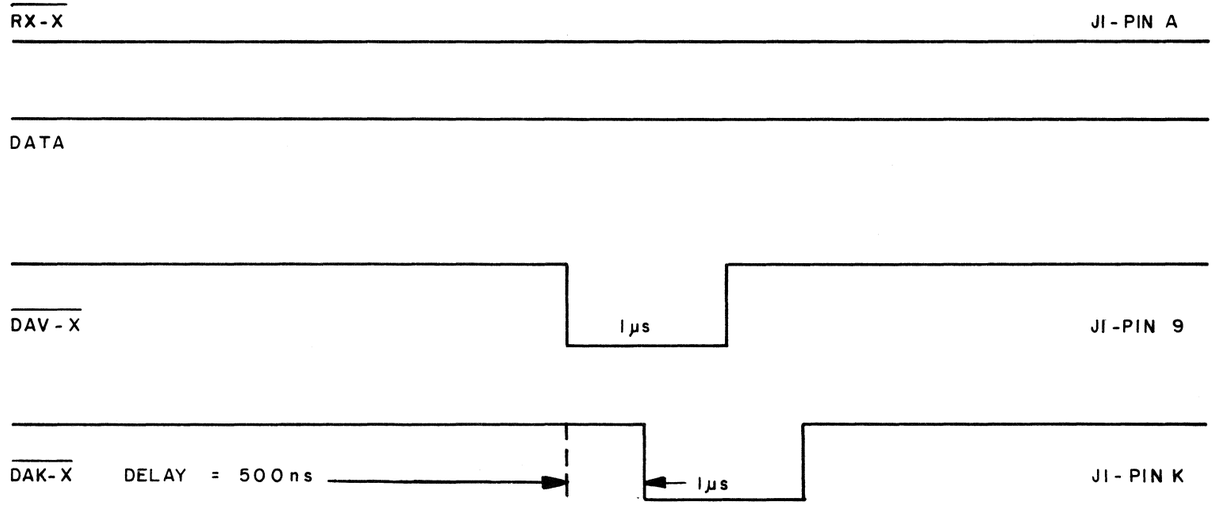


FIGURE 2-5
DATA TRANSFER TIMING

ERROR DETECTION

If the keyboard detects an error, data line DLI0 of the I2 BD SI is forced true, and on the next receive transfer (from the KDT to the system) the KDT Controller is notified of the error. This error can occur due to one of two reasons. Either two keys have been pressed/ released within I0 ms of each other; or new data has been presented to the keyboard Data Buffer before the previous data could be transferred to the KDT Controller. Either one of these errors causes a tone to sound and the red ERROR lamp on the front of the KDT to illuminate until reset by the system software.

While a Parity Option is available for the KDT, it does not affect the keyboard operation. Only commands are sent to the keyboard, and a Parity Check is made only on data. Therefore, the keyboard never generates the PARITY ERROR (PAE) signal; consequently, the PAE line is always false.

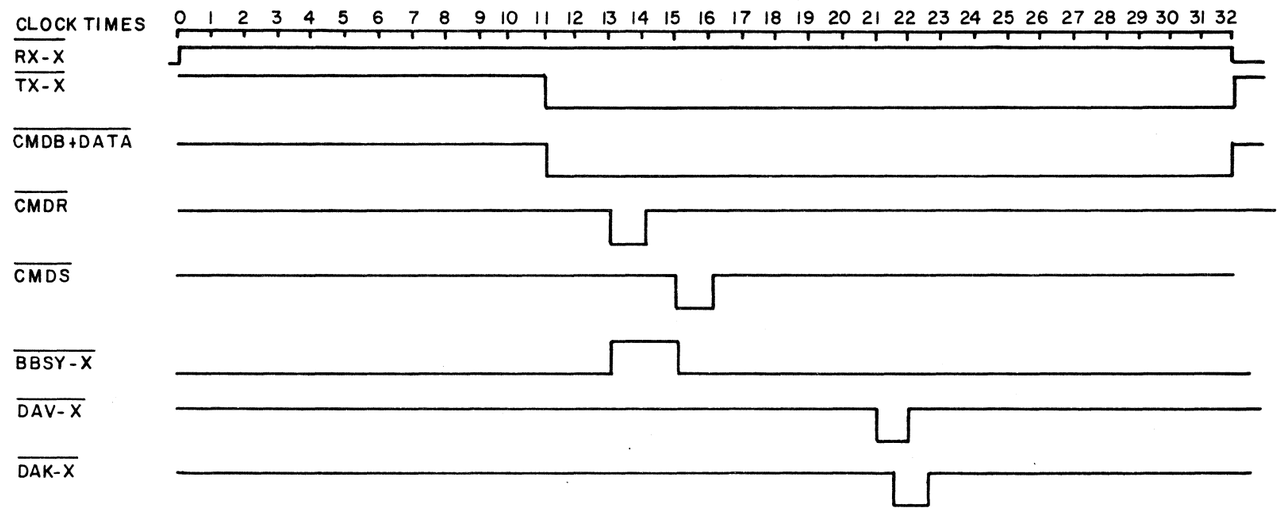


FIGURE 2-6

COMMAND TRANSFER TIMING

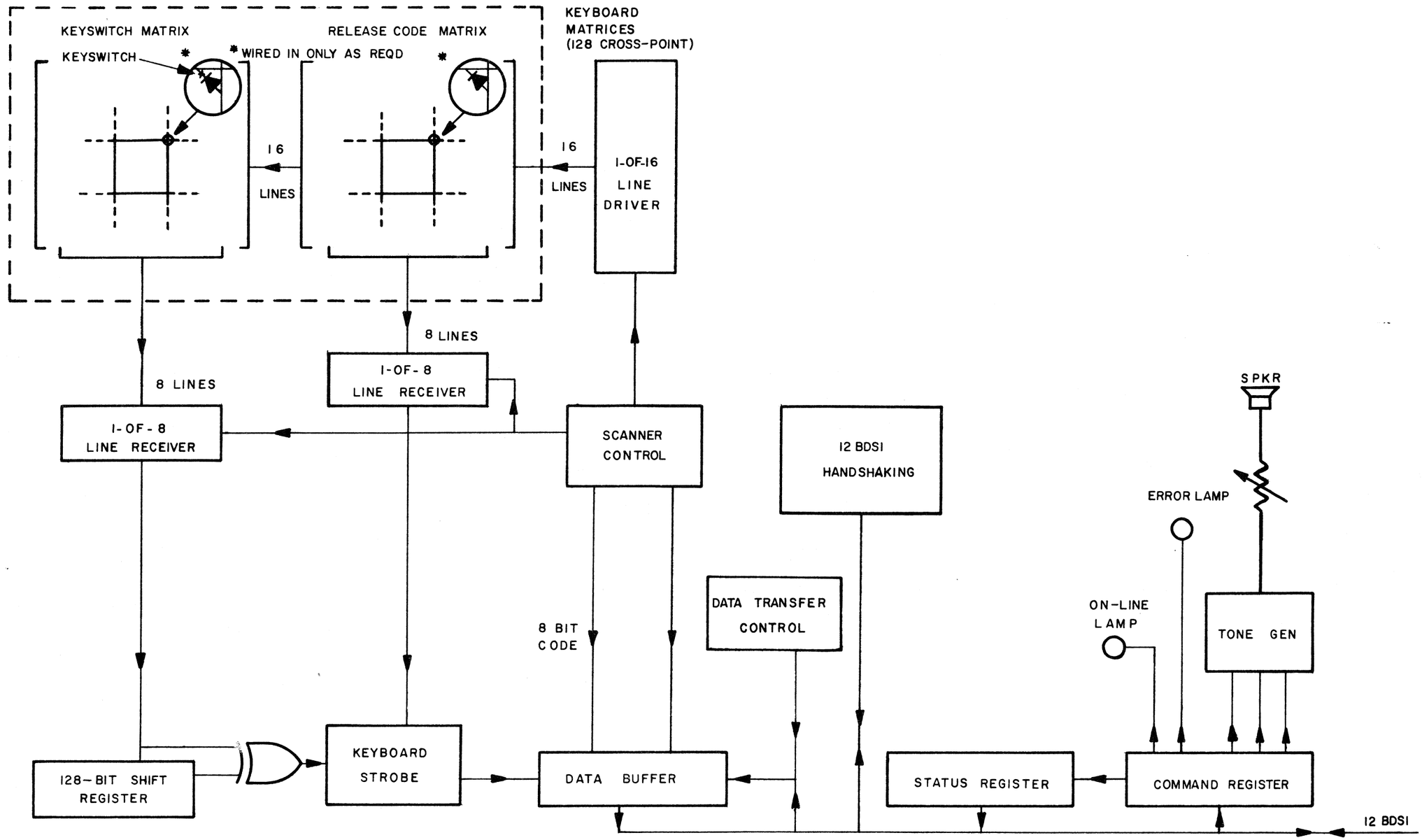


FIGURE 2-7
KEYBOARD CONTROLLER BLOCK DIAGRAM

Circuit Description

Figure 2-7 is a block representation of the Keyboard Controller circuitry. The function of each circuit of the controller is detailed in this section.

SCANNER CONTROL

The Scanner Control circuit conditions and generates the address of each crosspoint in the Keyboard Matrix once during every cycle of its 4-bit counters. If a key is depressed, the low level conditioned by the scanner control for that crosspoint will be used by the 128-bit Shift Register to stop the Scanner and enable the Keyboard Strobe circuit.

KEYBOARD MATRIX

A pair of diode matrices are used to stop the Scanner Control when a key is depressed or released. Every key position has a unique address, which is transferred to the CPU and used to extract a character from a table contained in core. Special characters can be specified if a diode is inserted in the release code matrix. Data bit 07 is added to these addresses so that they differ from an ordinary address generated by a key depression. (The diodes that generate release codes are installed to customer specifications.)

128-BIT SHIFT REGISTER

This circuit is used to stop the Scanner Control when a key is depressed or released. The Shift Register stores the output from each crosspoint as it is conditioned by the scanner. During the next scanner cycle the current and stored outputs of each crosspoint are compared. If any differ, a key has been depressed or released, and the address of that key may be transferred to the CPU. (The address is always transferred when a key is depressed. On release, the address is transferred only if a diode is installed in that section of the release code keyboard matrix.)

KEYBOARD STROBE

This circuit is enabled when the 128-bit Shift Register has stopped the Scanner Control. After 6 ms, a 1 ms pulse enables. This KEYSTROBE (KSTB) loads the data word into the Data Register and initiates a data transfer.

DATA BUFFER

The Data Buffer, or Register, contains the data word currently being transferred to the CPU. It is loaded by KSTB if the Full flop is reset.

DATA TRANSFER CONTROL

These circuits perform DATA AVAILABLE/DATA ACKNOWLEDGE (DAV/DAK) handshaking, sense errors, and control the Data Buffer and Status Register line drivers.

DAV/DAK handshaking is used to strobe data from the Data Buffer in the keyboard to the Data Buffer in the L/150. The timing is shown in Figure 2-5.

The Error flop is set if two KSTB pulses occur within one 10 ms time slot, or if the KDT Controller fails to respond to $\overline{DAV}$ with $\overline{DAK}$. KSTB sets the Full flop which conditions the Error flop. The next KSTB will set the Error flop unless DAK has reset the Full flop.

The Data Buffer and Status Register line drivers are controlled by the STATUS REGISTER (STR) flop, which is set by a command that requests status from the KDT. Normally it is reset, enabling the Data Buffer line drivers.

COMMAND REGISTER

This register controls the error indicators and controller mode of operation. In the command transmission mode, the command word is clocked into the Command Register by $\overline{\text{DAK-X}}$. The register is loaded by $\overline{\text{DAV}}$ if the $\overline{\text{TRANSMIT}}$ ($\overline{\text{TX}}$) signal is true. The bit assignment in the Command Register is illustrated in Figure 2-8. The bit functions are:

READY — When set, READY allows KSTB to load the Data Register and initiate DAV/DAK handshaking.

TONE 1, TONE 2 — TONE 1 and TONE 2 control the tone generator in the Keyboard Controller.

½ s — This bit sets a one-shot that disables the tone generators after a ½-second delay.

STATUS — STATUS determines which set of line drivers is connected to the 12 BD SI line. If the STATUS bit is set, the data drivers are disabled and the status word drivers are enabled for one DAV/DAK cycle.

ERROR — ERROR is set by the software if it detects an error in data received by the system. It enables the ERROR lamp, and is usually used with TONE 1 and TONE 2 to signal the operator.

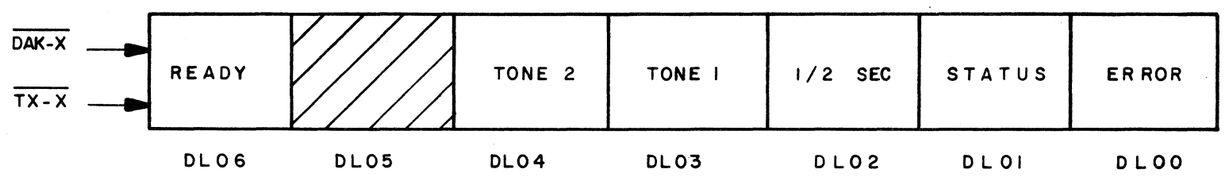


FIGURE 2-8

COMMAND REGISTER BIT ASSIGNMENT

STATUS REGISTER

If the command sets the STATUS bit, the controller disables the Data Register line drivers, and enables the Status Register line drivers. The status word is then received by the system in the same manner as is any other data word. The bit assignment in the Status Register is hard-wired to reflect the keytop configuration. This register is left unwired in KEY-EDIT 50 systems; a binary code of possibilities is illustrated in Figure 2-9.

12 BD SI HANDSHAKING

The 12 BD SI is a data transfer system that uses the same data lines for several devices. Each of these devices is assigned an address. This address is used to determine whether or not a particular controller connected to the 12 BD SI cable exists. Address bits DL09, 10, and 11 are used to condition the BBSY line before CMDR and CMDS reset to set BBSY.

TROUBLE ISOLATION

Figures 2-10 and 2-11 illustrate the sequence of events which occurs during a command transmission, and in the receive and error modes. Using these sequence diagrams, in conjunction with logic diagram 11840L, enables the Field Engineer to isolate any faults which occur in the Keyboard Controller. Use of the sequence diagrams is described in Part 1.

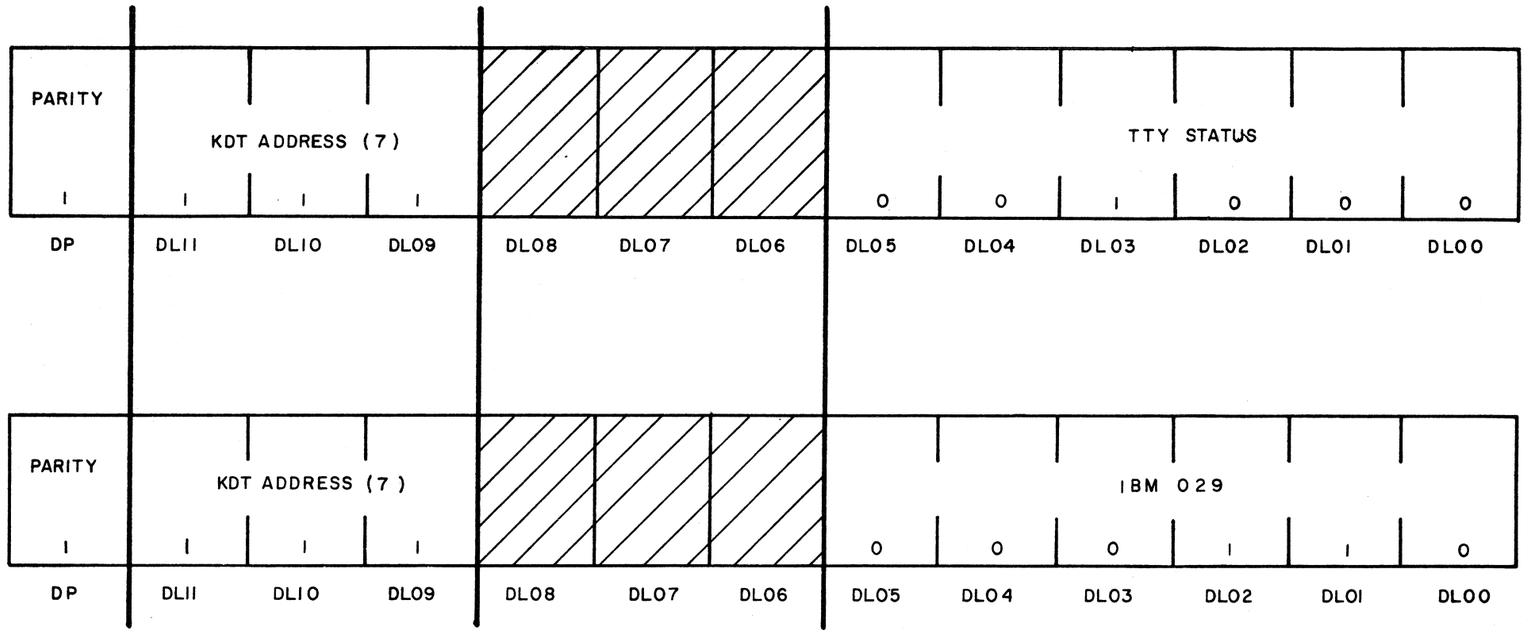


FIGURE 2-9

STATUS REGISTER BIT ASSIGNMENT

COMMAND TRANSMISSION

SOFTWARE DECISION TO SEND A COMMAND
THE KDT CNTRL ASSEMBLES A WORD
RECEIVE (RX 11840,2,2D,A12-13,J1-A) DISABLES
FULL • RX (11840,2,7B,B8-11) DISABLES TO PREVENT THE FULL FLOP ENABLING A RECEIVE CYCLE
AFTER A 20 μS DELAY COMMAND BIT AND DATA BIT ENABLE
TRANSMIT (TX, 11840,2,6A,A12-14,J1-C) ENABLES
COMMAND REGISTER BUFFERS (11840, 2, COL 5, A9-A10) ENABLE
AFTER 4 μS COMMAND RESET (CMDR, 11840, 2, 3B, A11-5, J1-D) ENABLES FOR 2 μS
BUS BUSY (BBSY, 11840, 2, 2B, C11-6, J1-7) DISABLES ONLY IF THE DATA CONTAINS THE PROPER DEVICE ADDRESS.
AFTER 4 μS COMMAND SET (CMDS,11840,2,3B,A11-12,J1-E) ENABLES FOR 2 μS
BBSY ENABLES

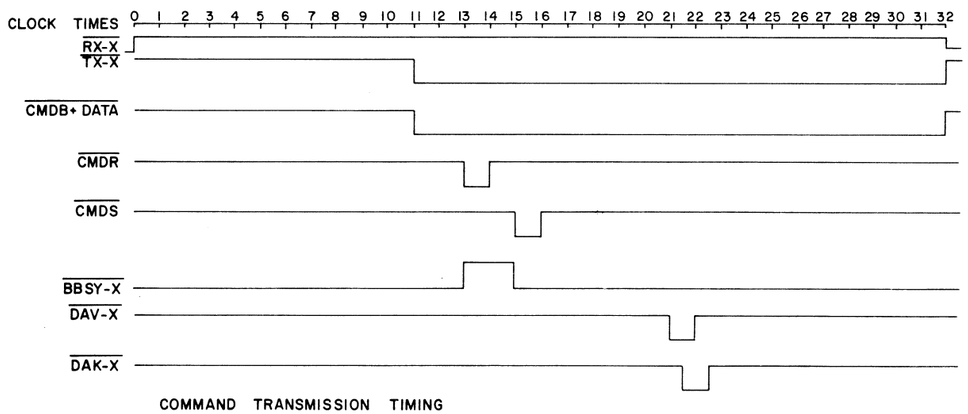
AFTER 12 μS DATA AVAILABLE ($\overline{\text{DAV-X}}$, 11840, 2, 6B,A10-7,J1-9) ENABLES
AFTER 500 ns THE COMMAND REGISTER (11840,2, COL 5, B9-D9) IS CLOCKED
DATA ACKNOWLEDGE ($\overline{\text{DAK-X}}$,11840,2, 4A ,A8-8,J1-K) ENABLES
AFTER 500 ns $\overline{\text{DAV-X}}$ DISABLES
AFTER 500 ns $\overline{\text{DAK-X}}$ DISABLES

IF THE COMMAND CONTAINED A REQUEST FOR KEYBOARD STATUS THE FLOW CONTINUES FROM THE TIME THAT THE COMMAND REGISTER IS CLOCKED

STAT FLOP (11840,2,5E,D9-5) SETS
STR FLOP (11840,2,7A,B7-5) SETS ONLY IF THE FULL FLOP IS RESET

STAT FLOP RESETS
STR.(TX,RDY)(11840,2,7A,D8-11) DISABLES THE KEY ADDRESS DRIVERS AND ENABLES DATA LINE 11 (11840,2,1C,A1-3,J1-6)
STR.(TX,RDY) ENABLES THE STATUS REGISTER DRIVERS

FULL FLOP (11840,2,7B,B7-9) SETS
DAVF FLOP (11840,2,7B,C8-8) SETS
DAV-X ENABLES
AFTER 500 ns $\overline{\text{DAK-X}}$ ENABLES
END OF DATA TRANSMISSION (EODT, 11840,2,7A,C4-2) ENABLES
STR FLOP RESETS
STATUS REGISTER DRIVERS DISABLE AND KEY ADDRESS DRIVERS ENABLE
AFTER 500 ns DAVF FLOP RESETS
FULL FLOP RESETS
AFTER 500 ns $\overline{\text{DAK-X}}$ DISABLES
EODT DISABLES



COMMAND TRANSMISSION TIMING

FIGURE 2-10
KEYBOARD CONTROLLER
COMMAND TRANSMISSION
SEQUENCE

DATA RECEIVE FLOW

KEY STROBE (KSTB, I1840, 2, 8B, B5-5) ENABLES FOR 1 MS
- ERROR FLOP (I1840,2,7B,B6-5) IS CLOCKED AND REMAINS RESET ONLY IF THE ERROR GATE (I1840,2,7B,C6-3) IS DISABLED
- DATA LATCHES (I1840,2, COL 8, A3-A4) ARE CLOCKED ONLY IF THE FULL FLOP (I1840,2,7B,B7-9) IS RESET
- FULL FLOP IS CLOCKED ONLY IF IT WAS RESET
- DAVF FLOP (I1840,2,7B,B8-8) IS SET ONLY IF THE RECEIVE GATE (I1840,2,7B,B8-11) IS ENABLED
- DLIO FLOP (I1840,2,6B,B6-9) IS CLOCKED AND REMAINS RESET ONLY IF THE ERROR FLOP IS RESET
- DATA AVAILABLE (DAV-X, I1840,2,6A,A8-6,J1-9) ENABLES
- AFTER 500 NS DATA ACKNOWLEDGE ($\overline{\text{DAK-X}}$, I1840,2,4A,C7-9,J1-K) ENABLES
- DAK GATE (I1840,2,8A,C7-14) ENABLES ONLY IF THE TRANSMIT GATE (I1840,2,6A,A12-14) IS DISABLED
- AFTER 500 NS THE FULL FLOP RESETS
- DAVF FLOP RESETS
- $\overline{\text{DAV-X}}$ DISABLES
- AFTER 500 NS $\overline{\text{DAK-X}}$ DISABLES — END

ERROR FLOWS

ASSUME THAT THE TERMINAL CONTROLLER IS IN THE TRANSMIT MODE WHEN THE KSTB ENABLES

KSTB ENABLES
- FULL FLOP SETS
- RECEIVE GATE IS HELD DISABLED
- ERROR GATE ENABLES
- KSTB ENABLES
- ERROR FLOP SETS
- AFTER SOME TIME $\overline{\text{RX}}$ ENABLES
- DAVF FLOP SETS
- DLIO FLOP SETS
- $\overline{\text{DLIO-X}}$ ENABLES
- $\overline{\text{DAV-X}}$ ENABLES
- AFTER 500 NS $\overline{\text{DAK-X}}$ ENABLES
- EODT ENABLES
- AFTER 500NS THE FULL FLOP RESETS
- DAVF FLOP RESETS
- $\overline{\text{DAV-X}}$ DISABLES
- THE DLIO FLOP WILL BE RESET WHEN THE NEXT DATA TRANSFER OCCURS — END

IF TWO KEYSTROKES OCCUR WITHIN IOMS THE CONTROLLER RESPONDS AS FOLLOWS:

KSTB ENABLES
- FULL FLOP (I1840,2,7B,B7-9) SETS
- NORMAL RECEIVE CYCLE FOLLOWS
- ERROR FLOP (I1840,7B,B6-5) IS CLOCKED AND REMAINS RESET
- IO MS TIMER (I1840,2,7B, B5-7) IS SET
- ERROR GATE (I1840,2,7B,E6-3) ENABLES
- WITHIN IOMS KSTB ENABLES
- ERROR FLOP (I1840,7B,B6-5) SETS
- TONE 2 FLOP (I1840,2,5C,B9-6) SETS
- ERROR LAMP FLOP (I1840,2,5B,D9-9) SETS
- FULL FLOP SETS
- DAVF FLOP (I1840,2,7B,B8-8) SETS
- DLIO FLOP (I1840,2,7B, B6-8) SETS
- DLIO-X (I1840,2,6B,A8-11,J1-11) ENABLES
- DATA AVAILABLE ($\overline{\text{DAV-X}}$, I1840,2,6B,A8-6,J2-9) ENABLES
- AFTER 500 NS DATA ACKNOWLEDGE (DAK-X, I1840,2,8A,C7-9,J1-K) ENABLES
- END OF DATA TRANSMISSION (EODT, I1840,2,7A,C7-3) FLOP
- ERROR FLOP RESET
- AFTER 500NS THE FULL FLOP RESETS
- DAVF FLOP RESETS
- $\overline{\text{DAV-X}}$ DISABLES
- AFTER 500 NS $\overline{\text{DAK-X}}$ DISABLES — END

ERROR DETECTION

PARITY ERRORS

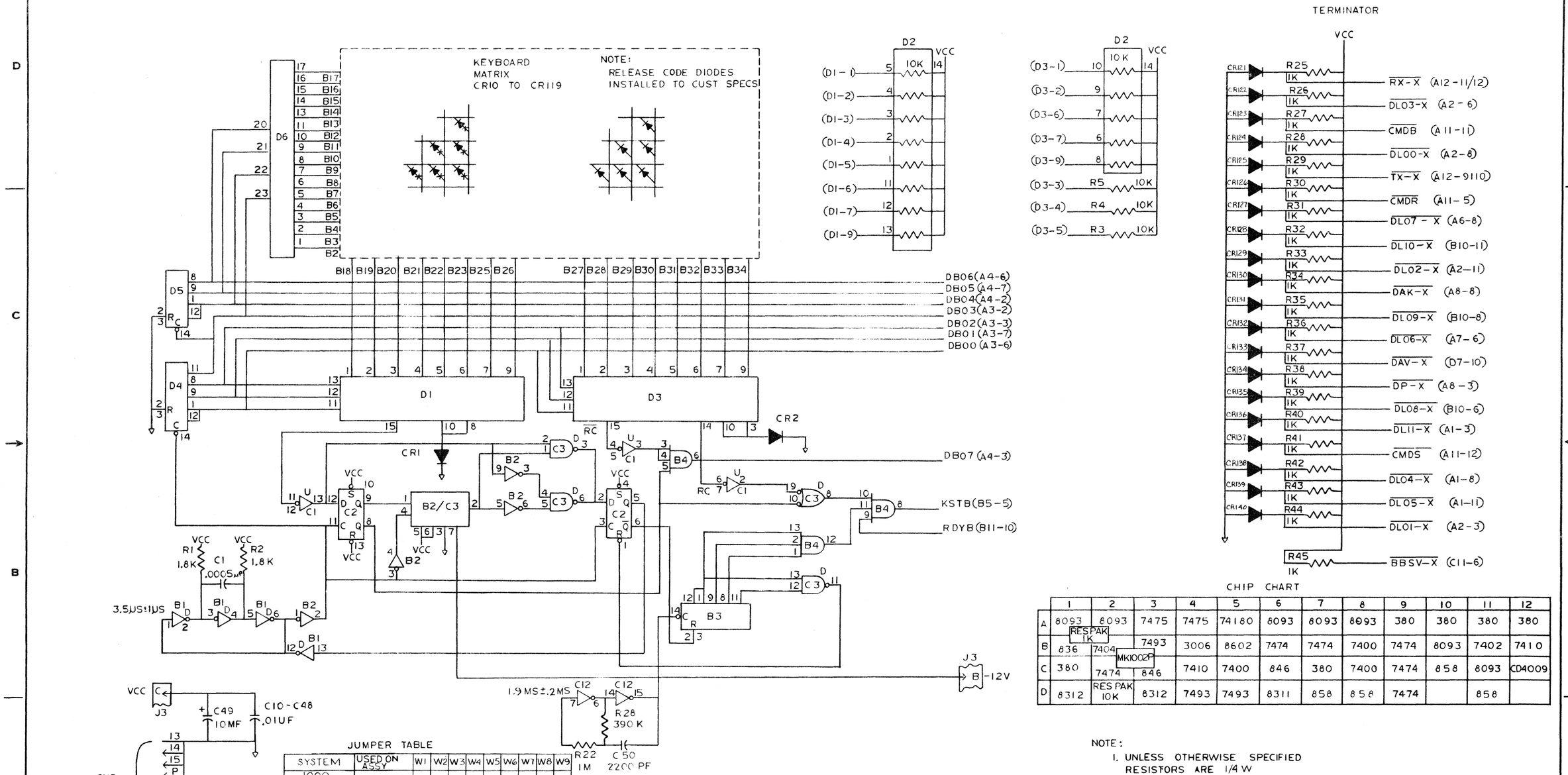
A PARITY BIT IS GENERATED BY THE KEYBOARD FOR BOTH DATA AND STATUS WORDS. THIS BIT IS USED BY THE TERMINAL CONTROLLER TO CHECK THE WORD PARITY. IF AN ERROR IS DETECTED THE SOFTWARE RESPONDS BY SENDING A COMMAND TO THE TERMINAL IN THE SAME MANNER AS ANY OTHER COMMAND.

KEYBOARD ERRORS

THE KEYBOARD CONTROLLER MUST ENSURE THAT THE PRESENT WORD IN THE DATA LATCH IS RECEIVED BY THE TERMINAL CONTROLLER BEFORE ANOTHER WORD IS GENERATED. THERE ARE TWO WAYS THAT THE KEYBOARD CONTROLLER CAN DETECT ERRORS. A TIMER IS USED TO LIMIT THE INTERVAL BETWEEN KEYSTROKES TO AT LEAST IO MS AND GATING IS USED TO ENSURE THAT THE TERMINAL CONTROLLER HAS RESPONDED TO ONE DATA AVAILABLE PULSE BEFORE ISSUING ANOTHER.

DATA LINE IO IS USED TO INDICATE TO THE TERMINAL CONTROLLER THAT THE KEYBOARD HAS DETECTED AN ERROR (REFER TO ERROR FLOWS)

FIGURE 2-11
KEYBOARD CONTROLLER
RECEIVE & ERROR
SEQUENCE



JUMPER TABLE

SYSTEM	USED ON ASSY	W1	W2	W3	W4	W5	W6	W7	W8	W9
1000 STD 029	SKD11753A		1		1			1		1
1000 TTY	SKD11752A						1			1
1000 TTY WITHOUT NUMERIC PAD	SKD13302A						1			1
50 PHASE I	SLB11821A								1	
50 PHASE I & II	SLC13046A								1	
50 PHASE II KATAKANA 029	SLC13149 A		1			1			1	
50 PHASE II KATAKANA ISO	SLC13143A		1					1	1	

CHIP CHART

	1	2	3	4	5	6	7	8	9	10	11	12
A	8093	8093	7475	7475	74180	8093	8093	8093	380	380	380	380
B	836	RES PAK 1K 7404	7493	3006	8602	7474	7474	7400	7474	8093	7402	7410
C	380	7474	MK1002P 846	7410	7400	846	380	7400	7474	858	8093	CD4009
D	8312	RES PAK 10K	8312	7493	7493	8311	858	858	7474		858	

NOTE:
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4 W DIODES ARE IN914

SK437	G	ECO INC	20MAR74	JB	W2	
SK305	F	ECO INC.	8NOV73	WB	WB	
-	E	REV E NOT USED.	-			
SK301	D	RE-DRAW	2 APR73	JB		
ECO	rev	eco	description	date	by	chk / apprvd

used on | drawn: RWT | scale | date: 18 JAN 73 | design eng: RJ | unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ±0°30' | checked: WB | final apprvl: GN | material | finish

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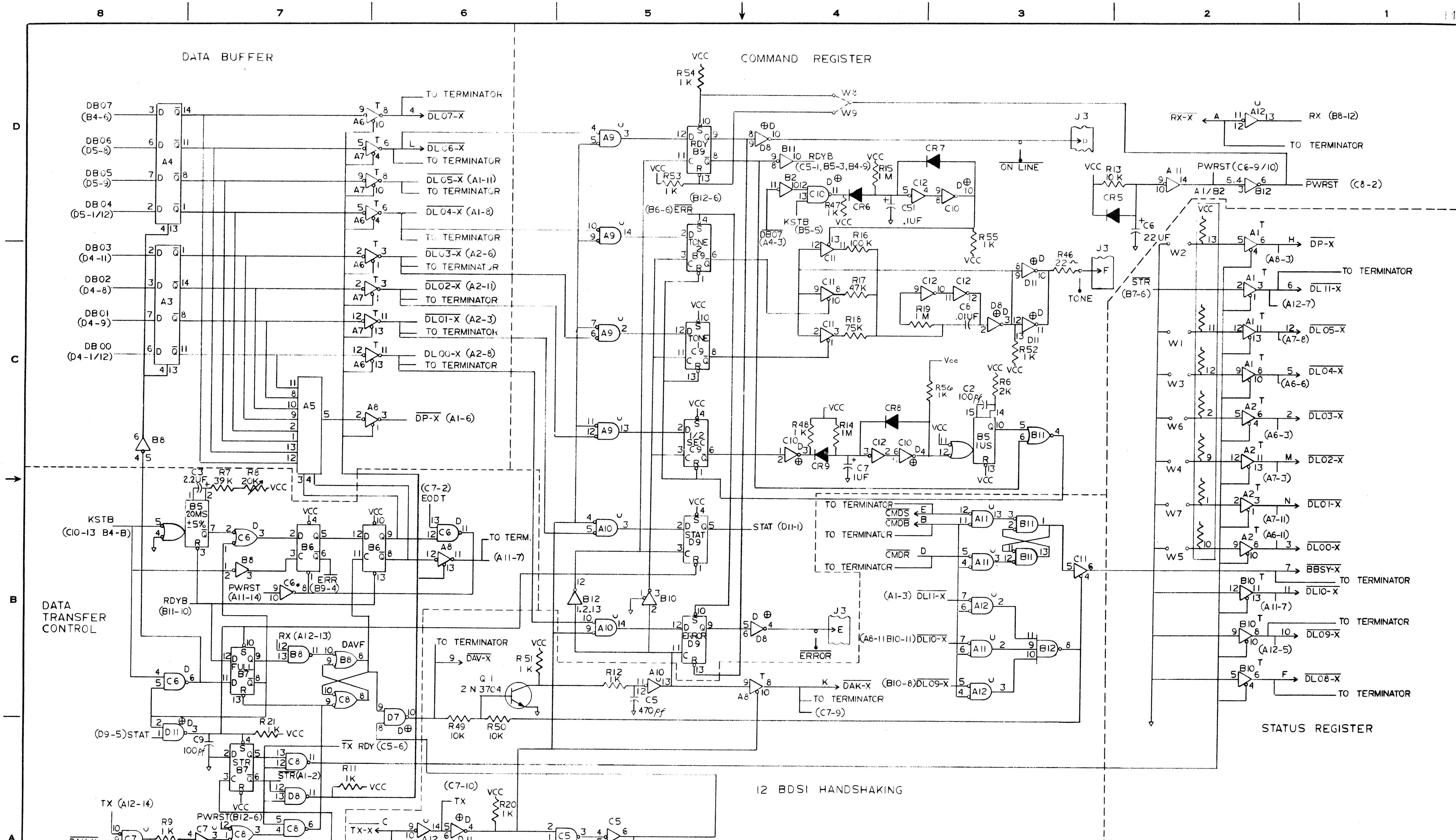
LOGIC DIAGRAM KEYBOARD DATA TERMINAL

title | sheet 1 of 2 | no. SKD11840L | rev G

TRANSTEX 19 800-2-73



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rev	eco	description	date	by	chk	apprvd
G	SK 437	ECO INC	20 MAR 74	B		
F	SK 205	ECO INC.				
E		REV E NOT USED				
D	SK 301	RE DRAW				

used on: | scale: | date: 18 JAN. 73 | drawn: R.W.T. | design eng: R.J. | checked: W.B. | final apprvl: G.N.

unless specified: .00 = ±.01, .000 = ±.005, fractions ± 1/64, angles ± 0°30'

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material | finish

title: LOGIC DIAGRAM KEYBOARD DATA TERMINAL

sheet 2 of 2 no. SKD11840L rev G

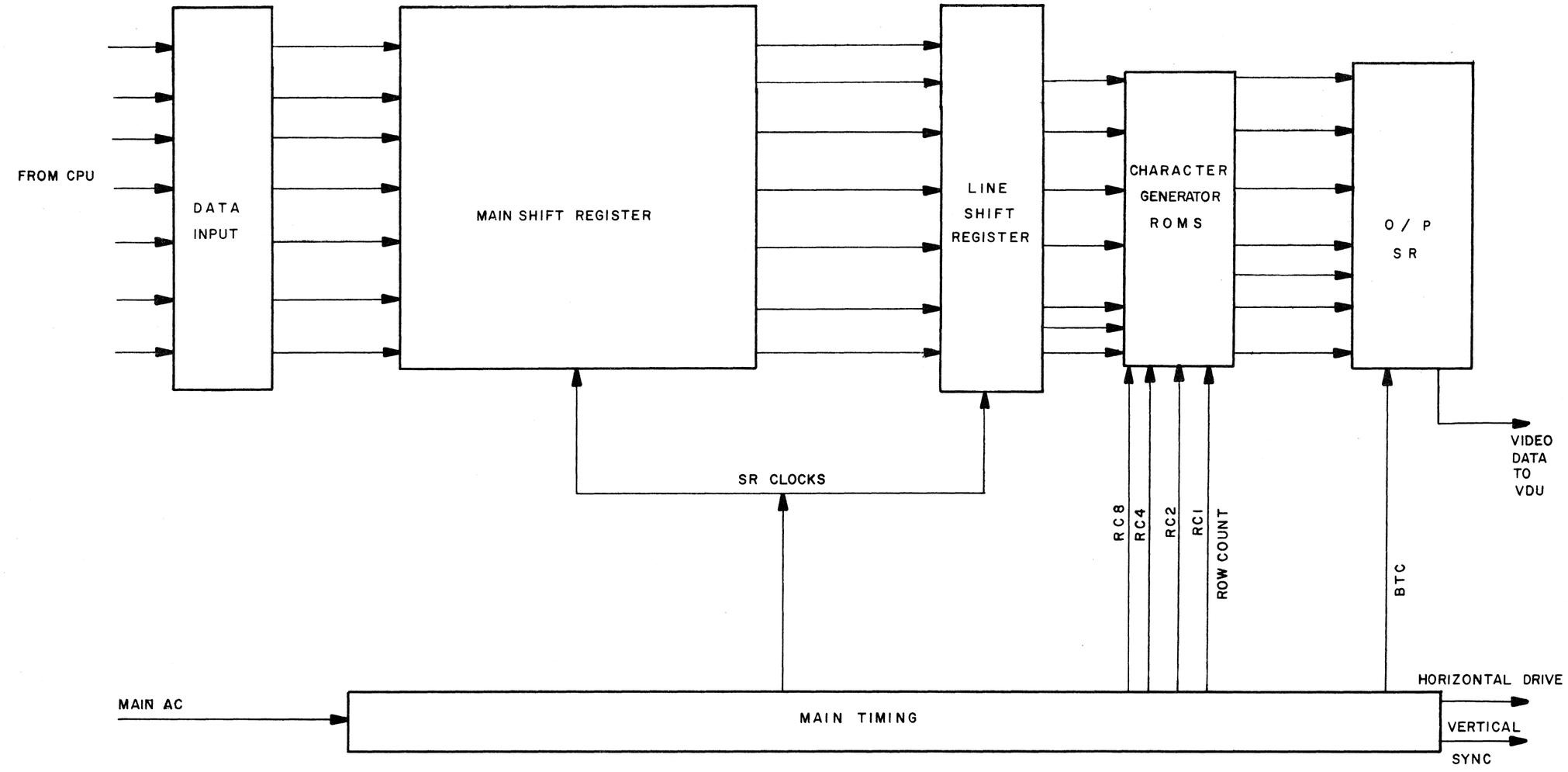


FIGURE 2-12
VDU FUNCTIONS

VDU CONTROLLER

INTRODUCTION

The VDU Controller is a single pcb mounted in the rear of the KDT beneath the VDU. The controller has two functions:

- providing the VDU with vertical and horizontal sweep timing pulses
- accepting data from the CPU and converting the information.

Refer to Figure 2-12.

OPERATIONS

TIMING CONTROL

The VDU requires a horizontal drive pulse and a vertical synchronization pulse to define its raster. These pulses are derived from the local mains frequency. The pulses used to define the positions of the dots that form a character are also derived from the mains frequency. Figure 2-13 shows the relationships between these timing pulses.

The master clock used by the VDU Controller is BIT TIME CLOCK (BTC). This is a train of 50 ms pulses at whatever frequency is required by the VDU to maintain its raster. Each BTC also defines a position in the 10 x 16 dot matrix used to form characters. Ten BIT TIME CLOCKS define one CHARACTER WIDTH TIME (CWT). Sixty CWTs form one ROW TIME (RT), defining the width of the display as sixty characters. The horizontal drive pulse is derived from CWT 12 and CWT 50.

Sixteen RTs define one CHARACTER LINE TIME (CLT), the height of each character on the display. Depending on the mains frequency, 15 or 19 CLTs are used to generate the vertical synchronization pulse and define the number of lines of characters on the VDU screen.

The BIT TIME CLOCK is also used to clock the Main and Line Shift Registers that store the data displayed on the VDU screen.

DATA CONVERSION

Data is written on the VDU screen by constructing each character from dots in a 10 x 16 dot matrix. These dots are written by turning the VDU CRT beam on and off. The VDU Controller supplies the bit patterns that form each character.

The VDU Controller accepts 12 BD SI command and data words from the L/150. Command words are used to determine the controller mode of operation. Data words are used as addresses in the Main Shift Register.

Any block of words transmitted to the VDU Controller contains both command and data words. A sequence to perform the loading of a data character into an address is as follows:

Command.....Load Address
Data.....Address
Command.....Load Data Same Address
Data.....Character Data

Once the data character is loaded into an address in the Main Shift Register, it is rotated through to the Line Shift Register by the Shift Register Timing.

The method of forming characters is dictated by the characteristics of the raster on the VDU screen. Since the raster is painted on the screen line by line, the characters are formed the same way. Each time the electron beam sweeps across the screen it paints one row of the 16 lines that define a character height. To produce the proper bit pattern for each row, the VDU controller must combine two pieces of information: the row, and the character being painted on the screen. The row number is counted by the Main Timing circuitry and applied to three Read Only Memories (ROM) as part of an address. The character data is contained in the Line Shift Register. This register is clocked so that the proper data for each character in a line is available sixteen times while the line of characters is formed. The character data is used as the rest of the ROM address to enable the proper bit patterns as each row of each character is painted on the VDU screen.

The data on the VDU screen must be continually refreshed. The Main Shift Register contains the data for all of the characters on the screen. This data is continuously rotated through the shift register. Each time a character line is completed, the Line Shift Register is loaded with the data for the next line. The Main Shift Register and the Line Shift Register are clocked with pulses that are based on BTC. This ensures that both registers and the raster remain synchronized, so that all of the characters will remain in place on the VDU screen.

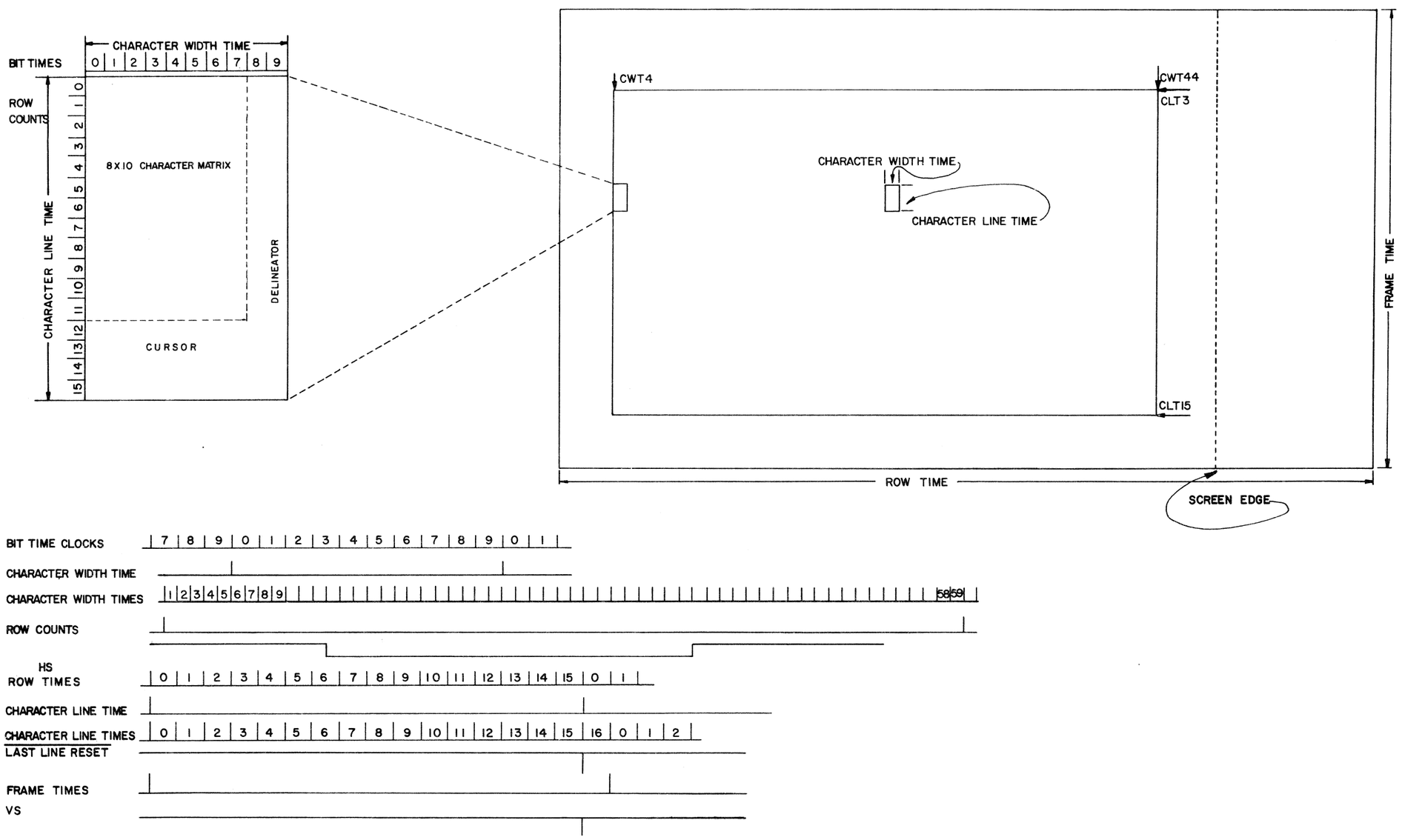


FIGURE 2-13
VDU CONTROLLER MAIN TIMING

CIRCUIT DESCRIPTION

Figure 2-15 is a block diagram of the VDU Controller. Each functional circuit of the controller is detailed in this section.

COMMAND REGISTER

The Command Register is loaded with commands from the L/150 to control the mode of operation. The register bit assignment is illustrated in Figure 2-14.

The bit functions are:

$\frac{\text{RDY}}{\text{RDY}}$ READY conditions a gate to allow the DAV/DAK cycle to load the Data Register.

$\frac{\text{SET}}{\text{SET}}$ This bit writes cursors and delineators if it is true, and clears cursors and delineators if it is false.

$\frac{\text{DATA}}{\text{DATA}}$ This bit indicates that the word following is a data word.

$\overline{\text{INC}}$ INCREMENT is used to load a string of data characters in order into the Main Shift Register.

$\frac{\text{DEL}}{\text{DEL}}$ The delineator is a vertical line which is written to the right of a character if this bit is set.

$\frac{\text{CUR}}{\text{CUR}}$ The cursor is a horizontal line written under a character at Row 13.

EOL END OF LINE is used to control cursors and delineators from the present address to the end of the present line.

$\frac{\text{ALL}}{\text{ALL}}$ This bit is used to apply the current command to all of the addresses in the Main Shift Register.

$\frac{\text{ON}/\overline{\text{OFF}}}{\text{ON}/\overline{\text{OFF}}}$ This bit holds the video, cursor, and delineator flops reset to blank the VDU screen.

READY	SET	ALL	DATA	INCREMENT	DEL	CUR	EOL	ON/OFF
DL08	DL07	DL06	DL05	DL04	DL03	DL02	DL01	DL00

FIGURE 2-14
COMMAND REGISTER BIT ASSIGNMENT

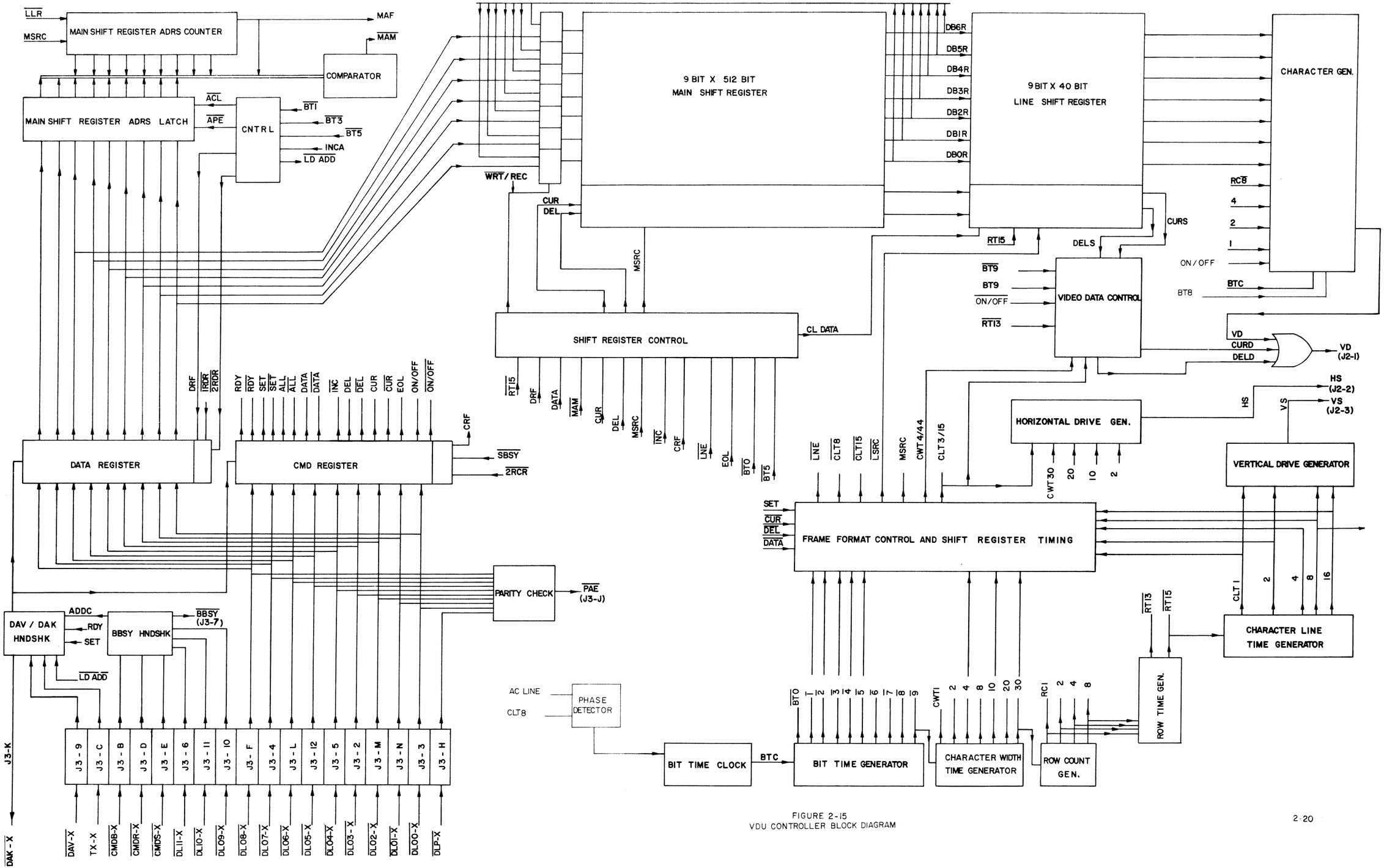


FIGURE 2-15
VDU CONTROLLER BLOCK DIAGRAM

The CR bits are used to form the following commands:

CODE	COMMAND
XX1	Display ON
XX0	Display OFF (Add with the codes below)
600	Load Address
440	Load Data Same Address
460	Load Data Increment Address
204	Set Cursor Same Address
224	Set Cursor Increment Address
210	Set Delineator Same Address
230	Set Delineator Increment Address
004	Clear Cursor Same Address
024	Clear Cursor Increment Address
010	Clear Delineator Same Address
030	Clear Delineator Increment Address
304	Set All Cursors
104	Clear All Cursors
310	Set All Delineators
110	Clear All Delineators
214	Set Cursor and Delineator Same Address
234	Set Cursor and Delineator Increment Address
014	Clear Cursor and Delineator Same Address
034	Clear Cursor and Delineator Increment Address
314	Set All Cursors and Delineators
114	Clear All Cursors and Delineators
140	Clear All Data
154	Clear All Data, Cursors and Delineators
000	Off Line
042	Clear Data to End of Line (EOL)
046	Clear Data and Cursors to EOL
052	Clear Data and Delineators to EOL
056	Clear Data Cursors and Delineators to EOL
206	Set Cursors to EOL
214	Set Delineators to EOL

CODE	COMMAND
216	Set Cursors and Delineators to EOL
006	Clear Cursors to EOL
012	Clear Delineators to EOL
016	Clear Cursors and Delineators to EOL
444	Load Data Clear Cursor Same Address
450	Load Data Clear Delineator Same Address
454	Load Data Clear Cursor and Delineator Same Address
644	Load Data Set Cursor Same Address
650	Load Data Set Delineator Same Address
654	Load Data Set Cursor and Delineator Same Address
464	Load Data Clear Cursor Increment Address
470	Load Data Clear Delineator Increment Address
474	Load Data Clear Cursor and Delineator Increment Address
664	Load Data Set Cursor Increment Address
670	Load Data Set Delineator Increment Address
674	Load Data Set Cursor and Delineator Increment Address.

12 BD SI HANDSHAKE

This circuitry provides the signals that respond to 12 BD SI BUS BUSY and DATA AVAILABLE/DATA ACKNOWLEDGE Handshaking, and generates a STROBE (STB) pulse to clock the Data and Command Registers.

12 BD SI LINE RECEIVERS

The 12 BD SI Line Receivers isolate the 12 BD SI cable from the VDU Controller.

DATA REGISTER

The Data Register latches each data word as it is provided by the 12 BD SI.

PARITY CHECK

The Parity Check circuit generates an output called PARITY ERROR (PAE) to provide the L/150 with a check on the parity of each word transferred through the 12 BD SI.

MEMORY ADDRESS MATCH

This circuit consists of three sections: a counter, a latch, and a comparator. The counter reflects the current Main Shift Register address. The latch contains the Main Shift Register address required. The comparator generates MEMORY ADDRESS MATCH ($\overline{\text{MAM}}$) when the latch and counter outputs are coincident.

CHARACTER GENERATOR

The Character Generator consists of a latch, three Read Only Memories (ROM), and a shift register. The latch contains part of the addressing that enables the ROMs to generate the character presently being displayed. The ROMs contain the bit patterns that generate characters. The shift register changes the parallel output of the ROMs to a serial bit pattern for use as video data. The character codes are shown in Appendix 2-2.

LINE SHIFT REGISTER

This register contains the forty data words for the current line. These words are loaded into the Character Generator Latch sixteen times during each CHARACTER LINE TIME.

MAIN SHIFT REGISTER

This register contains 480 data words. Forty of these words are loaded into the Line Shift Register to write a complete line of characters during each CLT.

DATA MULTIPLEXOR

The Data Multiplexor loads the Main Shift Register either from its own output (recirculate mode) or from the Data Register (upgrade mode).

SHIFT REGISTER CONTROL

This circuit clocks the Shift Register and controls the Data Multiplexor. The circuit also provides clear data, cursor, and delineator information to the Line Shift Register.

VIDEO DATA CONTROL

Controls the Video Data, Cursor Data, and Delineator Data flops to ensure that data is painted on the screen within the boundaries of CLT 3 - 15 and CWT 4 - 44.

BIT TIME CLOCK

The Bit Time Clock produces a train of 50 ns clock pulses synchronized with the local mains to provide the main timing pulses for the VDU Controller.

BIT TIME GENERATOR

This generator is clocked with the Bit Time Clock output to produce BIT TIME pulses, ten of which form one CHARACTER WIDTH TIME (CWT).

CHARACTER WIDTH TIME GENERATOR

This circuit generates timing pulses that define the width of one character on the screen. Sixty CWTs form one ROW TIME (RT).

ROW TIME GENERATOR

This circuit, clocked by CWT, generates timing pulses that define the row of the 10 x 16 character matrix to be written on the screen, and provide addressing data to the ROMs to enable the required bit pattern. Sixteen ROW TIMES form one CHARACTER LINE TIME (CLT).

CHARACTER LINE TIME GENERATOR

This circuitry, fed by the CWT Generator, generates the horizontal drive pulse used by the Video Display Unit.

FRAME FORMAT CONTROL AND SHIFT REGISTER TIMING

This circuit provides the clock pulses for the two memory shift registers and the Memory Address Match circuit. It defines the frame size in terms of character widths and character lines, and provides the LINE END ($\overline{\text{LNE}}$) signal.

ERROR DETECTION

The only error the VDU is capable of detecting is the data PARITY ERROR (PAE), if the Data Parity option is installed. If this option is not included in the system, the PAE line is tied to +5 V so that it is always false. With the option installed, the input (from the system to the KDT) signal DATA PARITY (DP) conditions the Parity Checking logic. This logic generates an overall even parity bit which is high false for a correct transfer. If a transfer is incorrect, the resultant even parity bit is low true, and generates the PAE signal true on the I2 BD SI line.

TROUBLE ISOLATION

Figures 2-16 and 2-17 illustrate the sequence of events which occurs during character generation and load address operations. Using these sequence diagrams, in conjunction with logic diagram 11535L, enables the Field Engineer to isolate any faults which occur in the VDU Controller. The format and use of the sequence diagrams is described in Part 1.

Character Generator Flow

The first data character is loaded by the Character Generator at Bit Time 0, Row Count 0, Character Width Time 4 of Character Line Time x where x is 3-15

The data character bits and the row count combine to address a bit pattern in the character generator ROMs.

At Bit Time 8 ($\overline{BT8}$, 11535,3,5C,L2-3) the bit pattern is loaded into a shift register (11535,2,2B,E1-9).

The Video Data Flop (11535,2,2B,E2-8) is reset

At Bit Time 9 the first bit of data is presented to the video display unit. Each Bit Time Clock presents another bit of data until ten have been sent. These bits make up the first row of the first character on the screen.

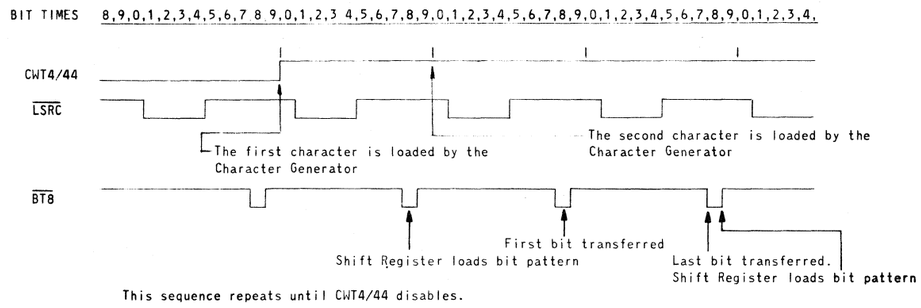
At $\overline{BT0}$ of Character Width Time 5, the second data character is loaded by the character generator and is transferred to the video display unit

This sequence of load and display repeats until Character Width Time 4/44 (CW 4/44, 11535,3,6B,D2-13) disables.

Line Shift Register Clock ($\overline{LSRC}$,11535,3,6B,D3-11) disables.

When the timing sequence returns to CWT4 $\overline{LSRC}$ enables and the next row of bit patterns is written on the video display screen.

During Row Time 15 ($\overline{RT15}$, 11535,3,2D,E5-17) the line Shift Register is loaded with forty data characters



This sequence repeats until CWT4/44 disables.

FIGURE 2-16
VDU CONTROLLER
CHARACTER GENERATOR FLOW
SEQUENCE

The flows show the loading of a data character into the Main Shift Register and then the generation of the bit pattern that writes the character on the video display screen.

The word sequence to load a data character is:

		CODE
Command	Load Address	4600
Data	Main Shift Reg. Address	000 to 479
Command	Load Data Same Address	4441
Data	Data Character for "A"	0101

In order to load a data address, both the Load Address and the Main Shift Register flows must be completed.

Load Address Flow

Terminal Controller assembles a word.

Transmit ($\overline{TX-X}$,11535, 1, 8B, F12-13, pin 12, J1-C) enables.

Command Bit ($\overline{CMDB}$, 11535, 1, 7B, E12-3, pin 5, J1-B) enables.

Data Bits ($\overline{DLO7-X}$ and $\overline{DLO1-X}$, 11535, 1, 8D, J1-4, F) enables.

After 4 usec Command Reset (CMDR, 11535,1,7B, F12-3, pin 5) enables for 2 usec.

Bus Busy ($\overline{BBSY}$, 11535, 1 D4, C13-11) disables.

After 4 usec Command Set ($\overline{CMDS}$, 11535, 1, 7B, F12-2, J1-E) enables for 2 usec.

$\overline{BBSY}$ enables.

After 12 usec Data Available ($\overline{DAV-X}$, 11535, 1, 8A, D13-3, J1-9) enables.

After 500 nsec STB (11535,1,6A, E11-4) enables.

Command Register (11535, 1, col.4) is clocked.

Ready (11535, 1, 4D, E10-10) enables

Set (11535, 1, 4D, E10-9) enables.

Load Address (LDADD, 11535, 3, 6A, E13-6) enables.

Data Acknowledge ($\overline{DAK-X}$, 11535, 1, 8A, C13-8, J1-K) enables.

After 500 nsec $\overline{DAV-X}$ disables

After 500 nsec DAK-X disables.

At this time the flow stops until the Data Register Full (DRF,11535, 1, 6B, C9-5) signal enables. This signal enables when the Data Register has been loaded with the required Main Sghft Register Address. The flow is:

Terminal controller assembles a data word.

Data lines enable

$\overline{DAV-X}$ enables

After 500 nsec STB enables.

The Data Register is clocked

$\overline{DAK-X}$ enables

DRF enables

At $\overline{BT1}$, Address Parallel Enable (APE, 11535, 3,5A, B7-8) enables

During $\overline{BT3}$ Address Clock ($\overline{ACL}$, 11535, 3, 5B, E7-1 enables

Memory Address Latch (11535, 1, 2B, C10 and B10) loads the address.

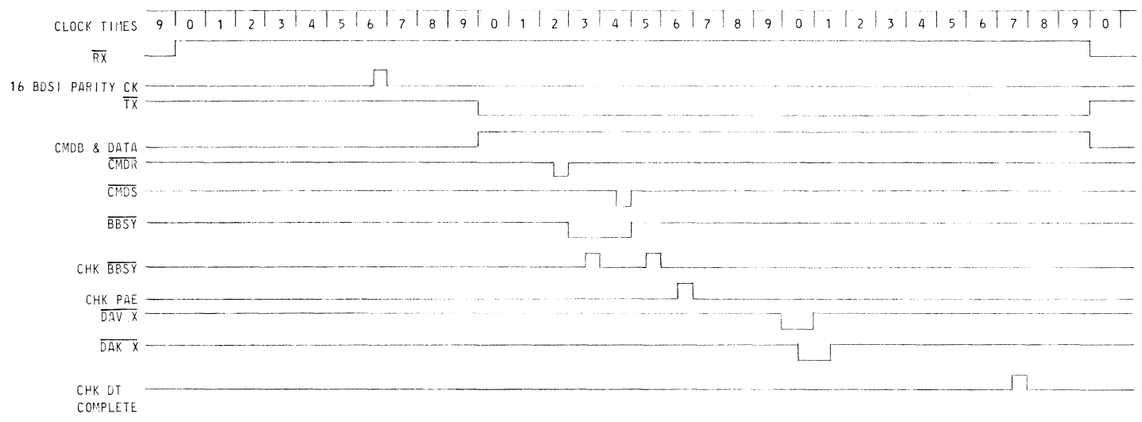
2 Reset Data Register ($\overline{2RDR}$, 11535, 3, 5A, D8-11) enables

DRF disables

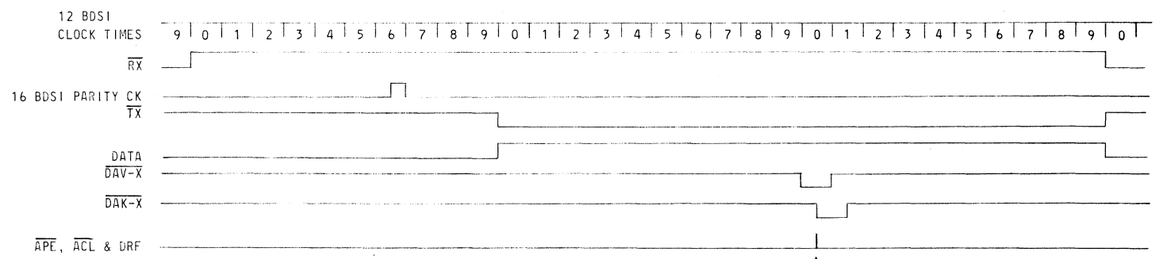
After 500 sec $\overline{DAV-X}$ disables

After 500 nsec $\overline{DAK-X}$ disables.

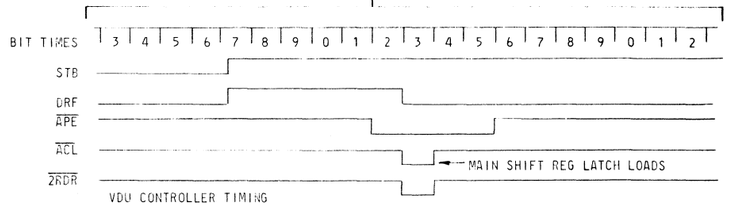
END



VDU CONTROLLER LOAD ADRS TIMING

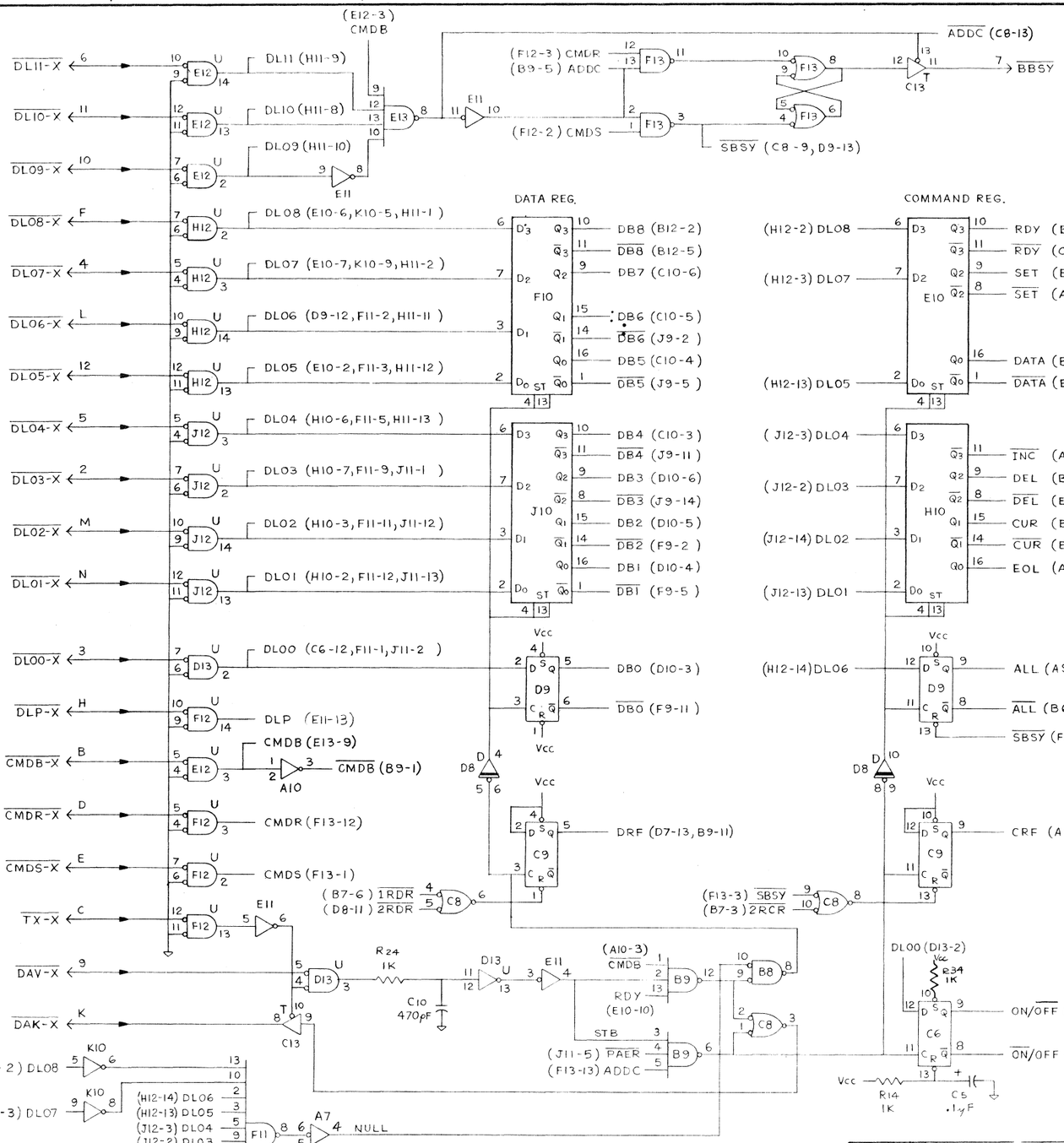


12 BDSI DATA WORD TRANSFER



VDU CONTROLLER TIMING

FIGURE 2-17
VDU CONTROLLER LOAD ADDRESS SEQUENCE



MAIN ADDRESS MATCH

CHIP CHART

	1	2	3	4	5	6	7	8	9	10	11	12	13
L	74164	3001	7479		4044		NOTE 2						
K	3001	7420	1805	8601	7404	9602	858	IM5013	7406	7404			
J	7400	7410	7479	7402	7479	2519	7402		8267	7475	74180	380	
H					7493	R 3K	R 4.7K	1403's	RIK	7475	74180	380	
F	IC SOCKET	IC SOCKET		IC SOCKET	8308	2519	7402	(QTY 5)	8267	7475	1805	380	7400
E	74165	7479	3001	7492	8311		7402	7451	7400	7475	7404	380	7420
D	7490	7402	7400	7490	7410	7404	7400	857	7479	93L16/ B316	7242	93L16/ B316	380
C	7493	9602	9602	7493	7420	7479	7479	3001	7479	93L16/ B316	7242	93L16/ B316	8093
B	7493	7479	7410	7420	7400	7479	7400	3003	7410	7242	7479	7400	
A	7493	7493	7404			7400	7402	7400	7410	7400			

F/H 7/8 CCI P/N 9467800 0

NOTES: 1-UNLESS OTHERWISE SPECIFIED
RESISTORS - OHMS, 1/4W
CAPACITORS - μF

2. ISOLATOR, OPTICALLY COUPLED (TYPICALLY 4N28) SEE COMPONENT I.D. DRAWING BS13277

REV	eco	description	date	by	chk'd	approvd
E	SK479	F/H 7/8 ADDED	7 MAR 74	JB		
D	SK410	ECO INC	7 MAR 74	JB		
C	SK427	NOTE 2 ADDED	7 MAR 74	CDB		
B	SK343	ECO INCORP	6 SEPT 73	JB		
A	SK102	PROD RELEASE	8 MAR 73	DJ		
1		PRE PROD REL	13 OCT 72	RC		

used on SKD11535A/3 | scale | date 3 AUGUST 72 | drawn R.C | design apprvl | checked | final apprvl | material | finish

unless specified .00 = ±.01 fraction ± 1/64 .000 = ±.005 angles = ± 0 30'

CONSOLIDATED COMPUTER LIMITED OTTAWA

LOGIC
VDU CONTROLLER
DATA TERMINAL
title (WITH PARITY)

sheet 1 of 3 | no. SKD11535 L/3 | E rev

MAIN SHIFT REGISTER UPDATE CONTROL

LINE SHIFT REGISTER & CHARACTER GENERATION

(AB-8) CL DATA

Vcc

-9V

-12V

(E10-16) DATA
(A6-12) MAM
(C9-5) DRF

(A3-6) RT15
(L2-11) $\overline{BT5}$

(L3-5) $\overline{BTO}$
(B6-3) BT05
(A9-5)

(B7-11) MSRC

(H10-11) $\overline{INC}$

INCA (E7-3)

(B7-11) MSRC

$\overline{2RCR}$ (C8-10)

(H10-15) CUR
(H10-9) DEL
(B9-10) MAM

MAM (A10-8)

CRF (C9-9)

BT05 (A6-3)

$\overline{ALL}$ (D9-8)

DEL (H10-9)

SET (E10-9)

(C2-9) $\overline{LNE}$

(H10-16) EOL
(A6-3) BT05

(E10-16) DATA
(E10-8) $\overline{SET}$
(D9-9) ALL

CL DATA (J7-6)

(D6-12) $\overline{MSRC}$

(B7-11) MSRC

(C6-9) $\overline{ON/OFF}$

F/H 7/8

(J7-4) DB6R
(F10-14) $\overline{DB6}$
(K5-10) DB5R
(F10-1) $\overline{DB5}$
(J7-13) DB4R
(J10-11) $\overline{DB4}$
(J7-10) DB3R
(J10-8) $\overline{DB3}$

(F7-4) DB2R
(J10-14) $\overline{DB2}$
(F7-1) DB1R
(J10-1) $\overline{DB1}$
(F7-13) DB0R
(D9-6) $\overline{DB0}$

DB6R (J9-1)
DB5R (J9-6)
DB4R (J9-10)
DB3R (J9-15)
DB2R (F9-1)
DB1R (F9-6)
DB0R (F9-10)

(D3-11) $\overline{LSRC}$
(E5-17) $\overline{RT15}$

CWT 4/44 (D2-13)

$\overline{BT9}$ (L3-9)

CURS (F5-11)

DELS (J5-5)

BT9 (L3-8)

CWT 5/45

$\overline{RT13}$ (E5-15)

$\overline{CURD}$ (J2-2)

$\overline{DELD}$ (J2-13)

K5 $\overline{BTO}$ (L1-2)

DELS (J3-12)

CWT 4/44 (J5-12)

$\overline{RC8}$ (K5-4)

CURS (J3-2)

(H5-8) RC4
(H5-9) RC2
(H5-1) RC1

(K5-12) BTC

RC4 (H5-8)

RC8 (H5-11)

$\overline{RC8}$ (F4-2/3)

$\overline{ON/OFF}$ (C6-8)

$\overline{CURD}$ (J2-6)

$\overline{DELD}$ (J2-8)

VD+CD (J1-10)

(L2-3) $\overline{BT8}$

CWT 4/44 (J5-12)

E	SK479	SEE SH 1					
D	SK410	SEE SH 1					
C	SK427	SEE SH 1					
B	SK343	ECO INCORP	6SEPT73	JB			
A	SK102	PROD RELEASE	8MAR73	DJ			
1		PRE PROD REL	13OCT72	RC			
REV	eco	description	date	by	chk	apprvd	

SKD11535A/3 — R.C. drawn

used on — 3 AUGUST 72 date — design apprvl

unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'

checked — final apprvl

material — finish

CONSOLIDATED COMPUTER LIMITED
OTTAWA

LOGIC
VDU CONTROLLER
DATA TERMINAL
(WITH PARITY)

sheet 2 of 3 — no. SKD11535L/3 — E

TRANSTEX 19 800-8-71

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

C

B

A

MAIN TIMING

CWT1
CWT2 (D5-10)
CWT4 (D3-4/5)
CWT8
CWT10 (D3-9, D5-11)
CWT20 (E3-9)
CWT30 (D3-10, E3-10, C3-5)

$\overline{RT13}$ (J1-4/5)
$\overline{RT15}$ (F6-4, B2-10, A3-5, C4-14, J6-4)

(C3-7)

(K5-3) RC8
(F1-22, K5-1) RC4
(F1-20) RC2
(F1-21) RC1

BT9 (J2-9)

50HZ	60HZ
W2	W4
W3	W1

(C5-2) CLT1
(C5-5) CLT2
(C5-13) CLT4
(C5-9) CLT8
(L5-3)

(E5-17) $\overline{RT15}$

(D6-5) $\overline{LSTL}$

$\overline{CLT16}$ (C5-4)

$\overline{LLR}$ (D12-1)

DISPLAY FORMAT

(D3-3) $\overline{CLT8}$
(D6-4) $\overline{CLT16}$
(C4-1) CLT1
(C4-9) CLT2
(C4-8) CLT4
(C4-11) CLT8

CLT 3/15 (J1-9)

CLT15 (B5-4)

$\overline{CLT8}$ (C5-1)

(D4-8) CWT4

(E4-8) CWT30
(E4-11) CWT10

CWT4/44
CWT4/44 (J5-12, J1-1)

(A3-6) RT15

$\overline{MSRC}$ (C7-11) (D12-2)

MSRC (B7-4) (B7-2) (D7-9) (D1-14)

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(KI-6) $\overline{BT3}$
(KI-8) $\overline{BT4}$

$\overline{LSRC}$ (F6-6)

VIDEO & SYNC OUTPUTS

(B5-8) CLT 3/15 VD+CD (J2-12)

(E4-8) CWT30
(E4-9) CWT20

(E4-11) CWT10
(D4-9) CWT2

(D5-6) $\overline{LSTL}$

GND
VD
HS
VS

R30 220Ω
R31 1K
R32, 1K

MAIN SHIFT REGISTER UPDATE SEQUENCE

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(L2-8) $\overline{BT6}$
(L2-6) $\overline{BT7}$

(A3-8) $\overline{RT15D}$
(B1-9) 512
(B1-8) 1024

(A3-12) $\overline{32}$
(B5-3) CLT15

(E5-17) $\overline{RT15}$

(KI-8) $\overline{BT4}$

RECYCLE COUNTER

$\overline{32}$ (B5-5)

512 (B4-12)
1024 (B4-13)

(E5-17) $\overline{RT15}$

(B8-3) INCA

MAF (B11-9)

RT15 (B8-12, B3-13)

$\overline{RT15D}$ (B4-10)

LINE END COUNTER

(B7-11) MSRC

$\overline{LNE}$ (A8-1)

(E10-9) SET
(H10-14) $\overline{CUR}$
(H10-8) $\overline{DEL}$
(E10-1) $\overline{DATA}$

$\overline{LD\ ADD}$ (F11-4)

DRF (C9-5)

$\overline{BT1}$ (KI-11)

(L2-11) $\overline{BT5}$

(KI-6) $\overline{BT3}$

$\overline{APE}$ (D10-9)

ACL (D10-2)

$\overline{2RDR}$ (C8-5)

BT0 (J4-9, K3-10)
BT1 (K3-2, K2-4, K2-10, E2-3)
BT2 (K3-3, K2-2, K2-13)
BT3 (K3-4, K2-1, E7-12)
BT4 (K3-1, K2-5, B2-11)
BT5 (B8-13, E2-4, K3-9)
BT6 (K3-12, K2-12)
BT7 (K3-13, K2-9)
BT8 (J1-12/13, K3-11, L3-12)

BTC (E2-11)

(J5-11) $\overline{BT9}$

$\overline{BT8}$ (L2-3)

(L1-2) $\overline{BT0}$
(K1-11) $\overline{BT1}$
(K1-3) $\overline{BT2}$
(K1-6) $\overline{BT3}$
(K1-8) $\overline{BT4}$
(L2-11) $\overline{BT5}$
(L2-8) $\overline{BT6}$
(L2-6) $\overline{BT7}$
(L2-3) $\overline{BT8}$

(K5-3) RC8
(F1-22, K5-1) RC4
(F1-20) RC2
(F1-21) RC1

(E4-8) CWT30

(H5-14)

(C5-2) CLT1
(C5-5) CLT2
(C5-13) CLT4
(C5-9) CLT8
(L5-3)

(E5-17) $\overline{RT15}$

(D6-5) $\overline{LSTL}$

$\overline{CLT16}$ (C5-4)

$\overline{LLR}$ (D12-1)

(B5-8) CLT 3/15 VD+CD (J2-12)

(E4-8) CWT30
(E4-9) CWT20

(E4-11) CWT10
(D4-9) CWT2

(D5-6) $\overline{LSTL}$

GND
VD
HS
VS

(B7-11) MSRC

$\overline{LNE}$ (A8-1)

(A3-6) RT15

$\overline{MSRC}$ (C7-11) (D12-2)

MSRC (B7-4) (B7-2) (D7-9) (D1-14)

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(KI-6) $\overline{BT3}$
(KI-8) $\overline{BT4}$

$\overline{LSRC}$ (F6-6)

(D4-8) CWT4

CWT4/44
CWT4/44 (J5-12, J1-1)

CLT15 (B5-4)

$\overline{CLT8}$ (C5-1)

(A3-8) $\overline{RT15D}$
(B1-9) 512
(B1-8) 1024

(A3-12) $\overline{32}$
(B5-3) CLT15

(E5-17) $\overline{RT15}$

(KI-8) $\overline{BT4}$

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(L2-8) $\overline{BT6}$
(L2-6) $\overline{BT7}$

(E10-9) SET
(H10-14) $\overline{CUR}$
(H10-8) $\overline{DEL}$
(E10-1) $\overline{DATA}$

$\overline{LD\ ADD}$ (F11-4)

DRF (C9-5)

$\overline{BT1}$ (KI-11)

(L2-11) $\overline{BT5}$

(KI-6) $\overline{BT3}$

$\overline{APE}$ (D10-9)

ACL (D10-2)

$\overline{2RDR}$ (C8-5)

(A3-6) RT15

$\overline{MSRC}$ (C7-11) (D12-2)

MSRC (B7-4) (B7-2) (D7-9) (D1-14)

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(KI-6) $\overline{BT3}$
(KI-8) $\overline{BT4}$

$\overline{LSRC}$ (F6-6)

(D4-8) CWT4

CWT4/44
CWT4/44 (J5-12, J1-1)

CLT15 (B5-4)

$\overline{CLT8}$ (C5-1)

(A3-8) $\overline{RT15D}$
(B1-9) 512
(B1-8) 1024

(A3-12) $\overline{32}$
(B5-3) CLT15

(E5-17) $\overline{RT15}$

(KI-8) $\overline{BT4}$

(KI-11) $\overline{BT1}$
(KI-3) $\overline{BT2}$
(L2-8) $\overline{BT6}$
(L2-6) $\overline{BT7}$

(E10-9) SET
(H10-14) $\overline{CUR}$
(H10-8) $\overline{DEL}$
(E10-1) $\overline{DATA}$

$\overline{LD\ ADD}$ (F11-4)

DRF (C9-5)

$\overline{BT1}$ (KI-11)

(L2-11) $\overline{BT5}$

(KI-6) $\overline{BT3}$

$\overline{APE}$ (D10-9)

ACL (D10-2)

$\overline{2RDR}$ (C8-5)

E	SK479	SEE SH1				
D	SK410	SEE SH1				
C	SK427	SEE SH1				
B	SK343	ECO INCORP	6 SEPT73	JB		
A	SK102	PROD RELEASE	8 MAR 73	DJ		
1		PRE PROD REL	15 OCT 72	RC	UR	
	eco	description	date	by	chk	approvd

used on SKD11535A/3 — RC drawn

scale — date 3 AUGUST 72 — design apprvl

unless specified
00 = ±.01 fraction ± 1/64
000 = ±.005 angles = ±0 30'

UR checked

final apprvl

material — finish

CONSOLIDATED COMPUTER LIMITED
OTTAWA

LOGIC
VDU CONTROLLER
DATA TERMINAL
(WITH PARITY)

sheet 3 of 3 — no. SKD11535L/3 — E rev

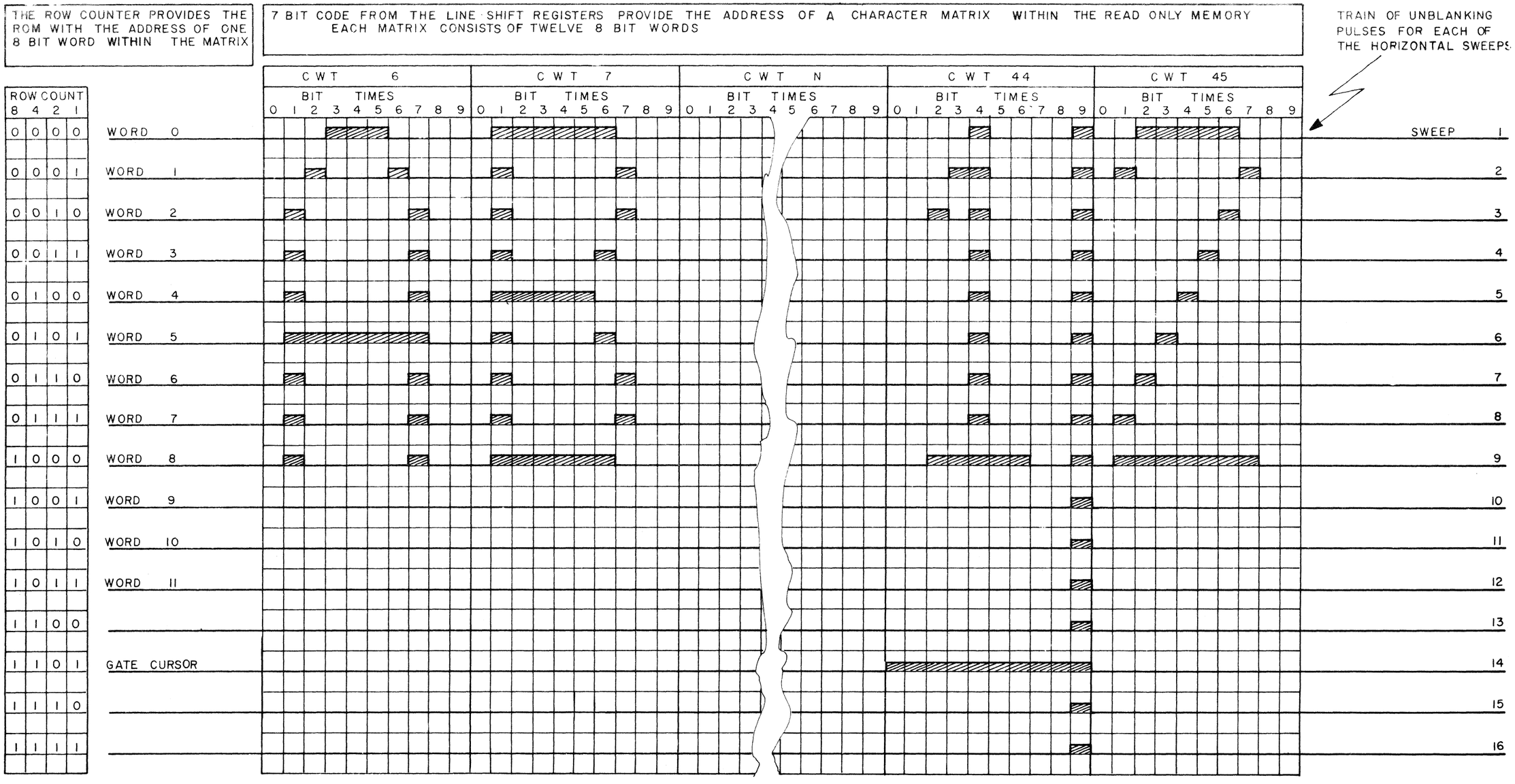


FIGURE 2-18
CHARACTER DISPLAY GENERATION

KDT ADJUSTMENTS

Keyboard Controller Adjustments

The multivibrator used in the error detection circuits must be adjusted to time out in 10 ms. The adjustment sequence is:

1. Remove the five screws securing the data terminal cover to the base.
2. Lift the cover and place it behind the terminal without disconnecting any cables.

   NOTE: Flop B9-9 must be forced set by grounding B9-10 before this adjustment can be made.

3. Turn the terminal on.
4. Adjust R8 until the pulse seen at B5-7 is 10 ms long. The pulse can be initiated by pressing any key on the keyboard.

VDU Controller Adjustment

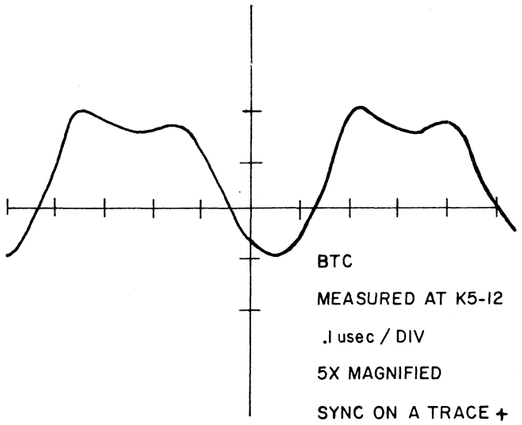
To adjust the Bit Time Clock frequency:

1. Remove the terminal cover and slide the keyboard and VDU controllers forward in order to allow access to R25 and R6 on the VDU Controller.
2. Turn the terminal on and adjust R25 until the voltage across R6 is 4.2 V. If a large change is made, allow the meter to settle before reading it.
3. Check that the raster is stable. If not, adjust R25 as necessary and check the voltage across R6.
4. The voltage across R6 should be 4.2 V ± 0.1 V in order to allow the phase-locked loop circuit the widest possible control range. Any major variation from this value indicates a possible problem in the main timing sequence.

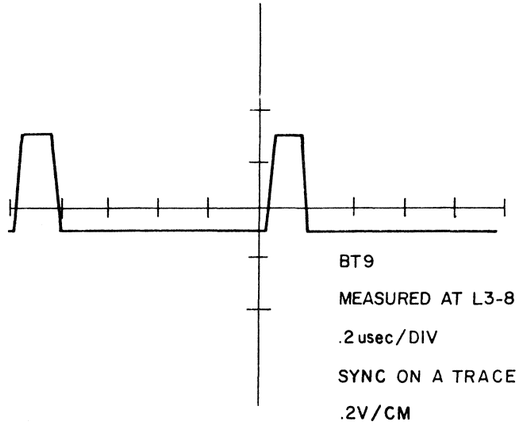
Each of the following major timing pulses (refer to Figures 2-18 and 2-19) should be checked:

NAME	LOCATION
Bit Time Clock	11535, 3, 6C, K5-12
BT9	11535, 3, 4D, L3-8
CWT30	11535, 3, 3D, E4-8
$\overline{\text{RT15}}$	11535, 3, 2D, C4-14
CLT8	11535, 3, 3C, C4-11

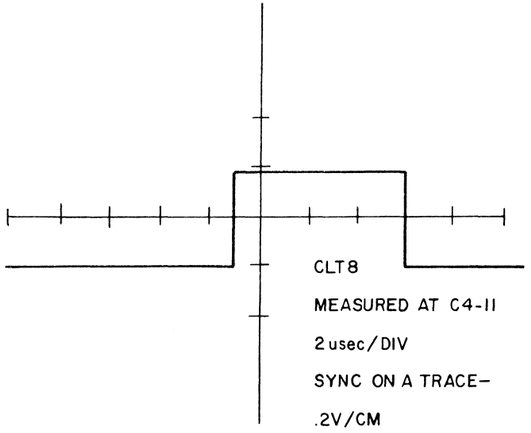
CAUTION: Do not ground the oscilloscope to the pcb if the terminal is connected to the system.



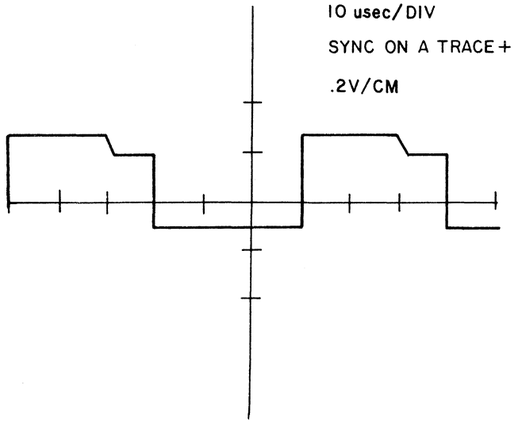
BTC
MEASURED AT K5-12
.1 usec / DIV
5X MAGNIFIED
SYNC ON A TRACE +
.2V/CM



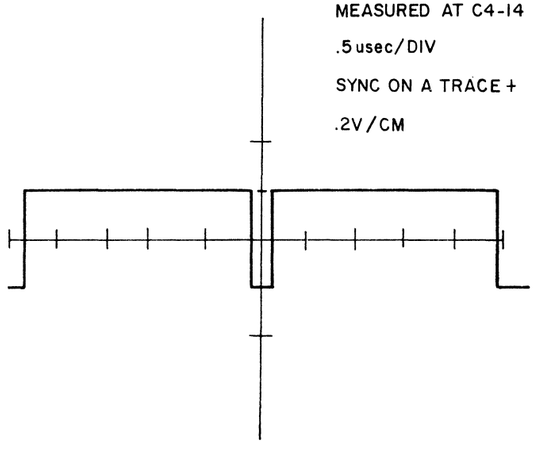
BT9
MEASURED AT L3-8
.2 usec/DIV
SYNC ON A TRACE +
.2V/CM



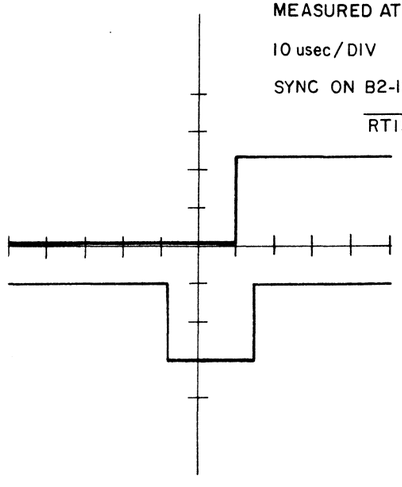
CLT8
MEASURED AT C4-11
2 usec/DIV
SYNC ON A TRACE–
.2V/CM



CWT 30
MEASURED AT E4-8
10 usec/DIV
SYNC ON A TRACE+
.2V/CM



$\overline{RT15}$
MEASURED AT C4-14
.5 usec/DIV
SYNC ON A TRACE +
.2V/CM



CWT4/44
MEASURED AT D2-13
10 usec/DIV
SYNC ON B2-10-
$\overline{RT15}$

FIGURE 2 - 19
VDU CONTROLLER MAJOR TIMING PULSES (SHEET 1 OF 2)

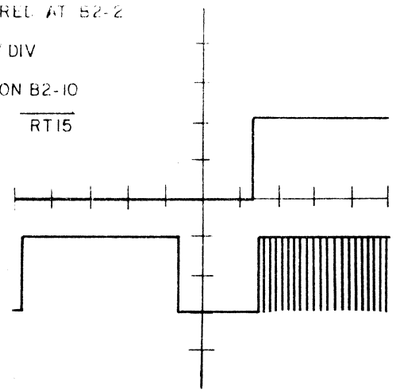
LSRC

MEASURED AT B2-2

5 usec / DIV

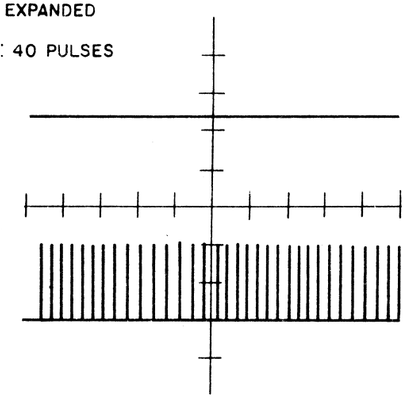
SYNC ON B2-10

$\overline{\text{RT15}}$



LSRC EXPANDED

NOTE: 40 PULSES



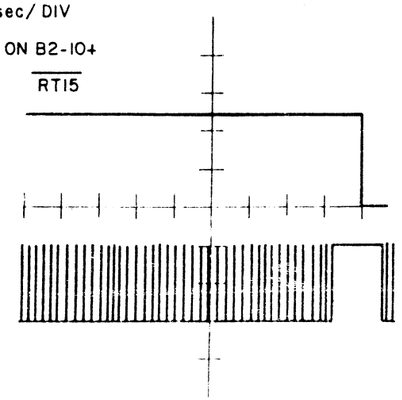
MSRC

MEASURED AT D6-12

100 usec / DIV

SYNC ON B2-10+

$\overline{\text{RT15}}$



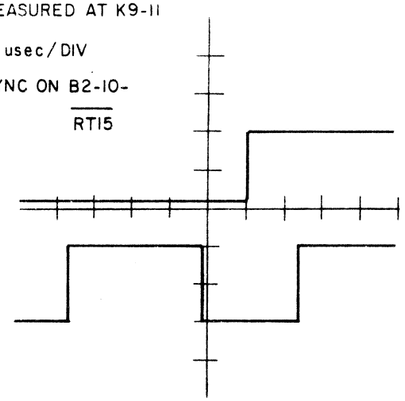
HS

MEASURED AT K9-11

10 usec / DIV

SYNC ON B2-10-

$\overline{\text{RT15}}$



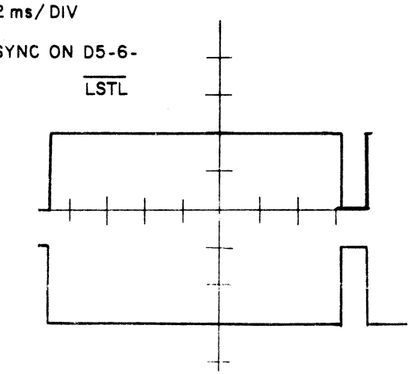
VS

MEASURED AT K9-9

2 ms / DIV

SYNC ON D5-6-

$\overline{\text{LSTL}}$

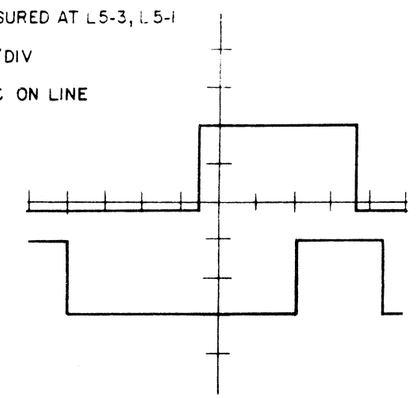


PHASE LOCK LOOP

MEASURED AT L5-3, L5-1

2 ms / DIV

SYNC ON LINE



CLT 3

MEASURED AT B5-8

2 ms / DIV

SYNC ON D5-6+

$\overline{\text{LSTL}}$

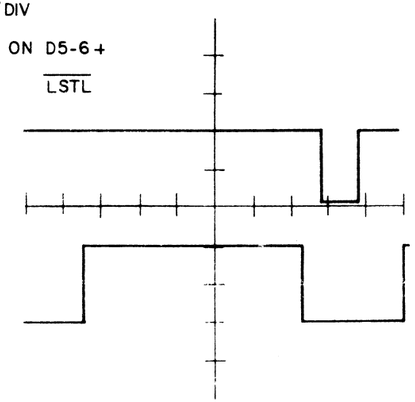


FIGURE 2-19
VDU CONTROLLER MAJOR TIMING PULSES (SHEET 2 OF 2)

KDT Power Supply Adjustments

The +15 V power supply can be adjusted for voltage and short circuit current output. Refer to Figure 2-20 and schematic drawing 13044S. The adjustment sequence is as follows:

CAUTION: Do not short circuit any power supply without adjusting R3 and R10 fully counter-clockwise.

Do not disconnect any power supply from the L/150 Adapter without disconnecting all power supplies. Damage to logic IC may occur if any supply is left connected.

1. Disconnect the cables at J6 and J7.
2. Adjust R5 until the voltage between J6, pin 1 and ground (J6-3) is 15 V.
3. Turn R3 fully counter-clockwise.
4. Adjust R3 until the short circuit current between J6, pin 1, and ground (J6-3) is 750 mA; use an ammeter with a resistance of less than 0.1 Ω (AVO Model 8 Mk IV is acceptable).
5. Reconnect the cables to J6 and J7 and check the supply output voltage.

The +5 V power supply adjustment sequence is as follows:

1. Disconnect the cables from J8 and J9.
2. Adjust R12 until the voltage between J9, pin 3, and ground (J9-1) is 5.20 ± .05 V.
3. Turn R10 fully counter-clockwise.
4. Adjust R10 until the short circuit current between J9, pin 3, and ground (J9-1) is 2 A; use an ammeter with a resistance of less than 0.1 Ω (AVO Model 8 Mk IV is acceptable).
5. Reconnect the cables to J8 and J9 and check the supply output voltage.

The -12 V and -5.5 V power supplies are not adjustable nor short circuit protected. The -12 V power supply output can be checked between J8-1 and J8-6, and the -5.5 V supply between J8-2 and J8-6.

SUPPLY	ADJUSTMENT	METER CONNECTIONS	LIMITS
+15 V	Voltage, R5	J6-1, J6-3	15 ± 0.1 V
	Short Circuit Current, R3	J6-1, J6-3 (GND)	750 ± 50 mA
+5 V	Voltage, R12	J9-3, J9-1	5.20 ± .05V
	Short Circuit Current, R10	J9-3, J9-1 (GND)	2 A ± 200 mA
-12 V	Voltage	J8-1, J8-6	-12 ±0.6 V
-5.5 V	Voltage	J8-2, J8-6	-5.5 ±0.5 V

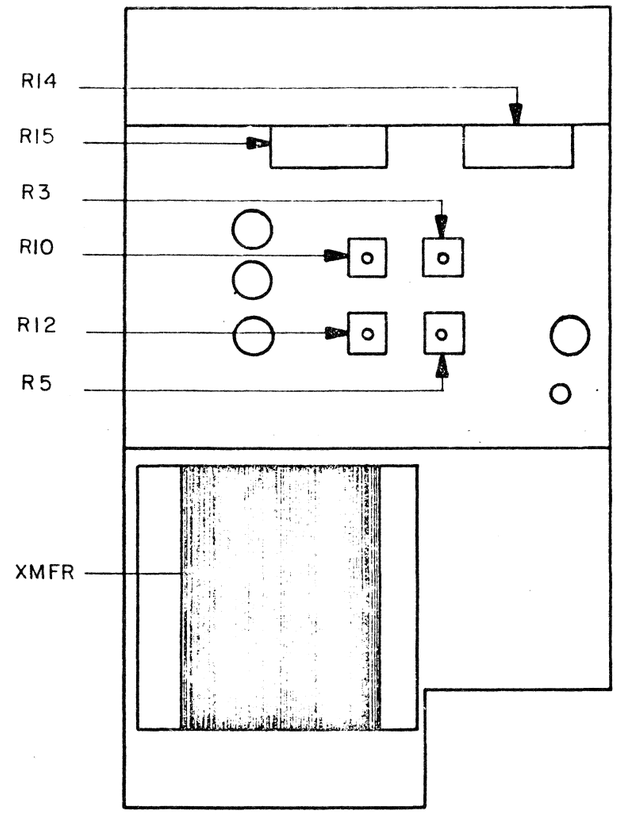
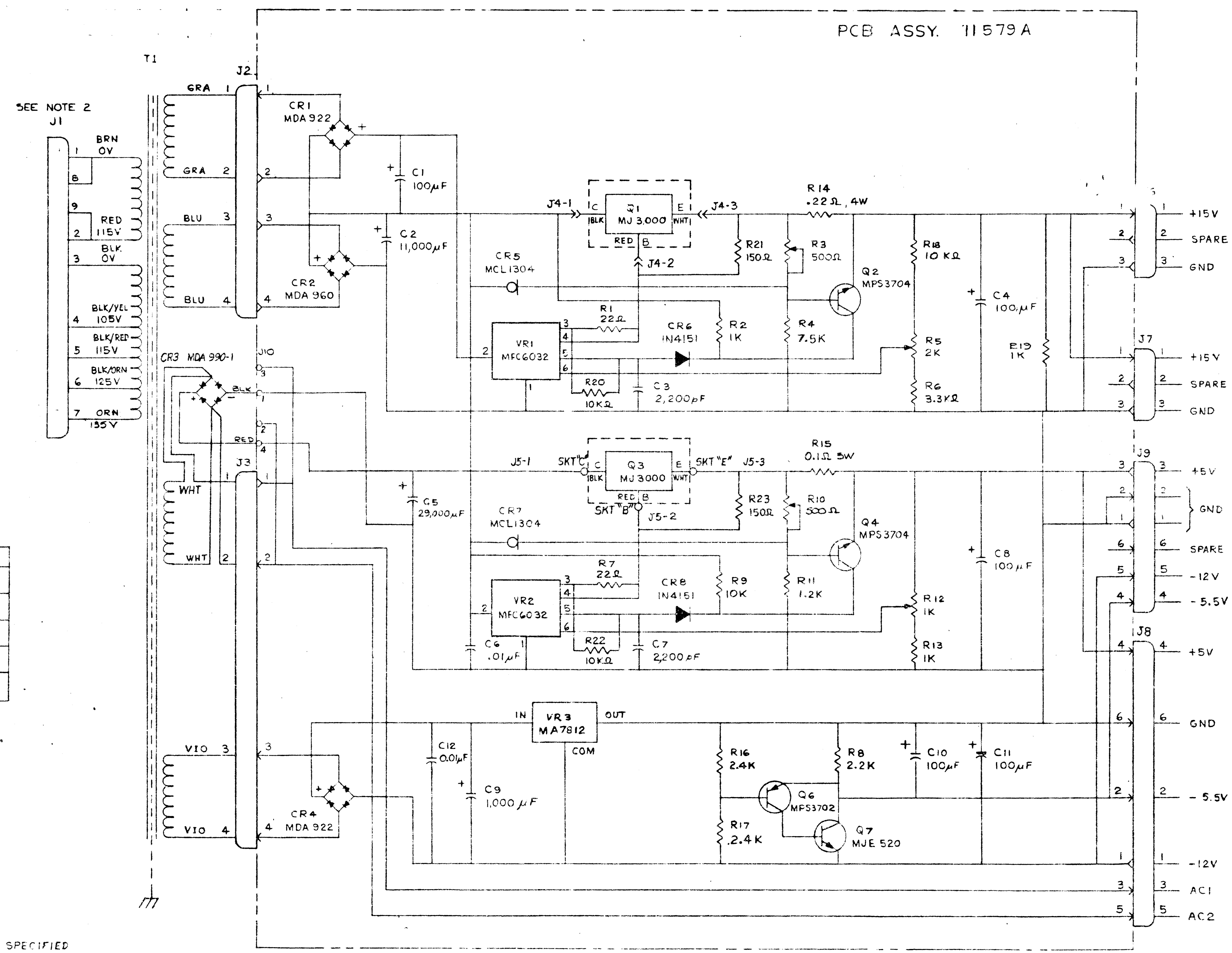


FIGURE 2-20
POWER SUPPLY ADJUSTMENTS



MATING CONNECTOR WIRING

VOLTAGE	JUMPER	L	N
115	3-8 & 5-9	2	1
220	2-3	4	1
230	2-3	5	1
240	2-3	6	1
250	2-3	7	1

NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR ARE IN OHMS 5% 1/4 W CAPACITOR ARE IN μF
2. SEE SHT 2 FOR ALTERNATE TRANSFORMER WIRE COLOURS.

SHEET 2 IS C SIZE

REV	ECO	description	date	by	chk	apprd
F	SK572	ECO INC	11 NOV 74	RC		
E	SK5??	ECO INC	7 ?? 74	RC		
D	SK512	ECO INC	3 MAY 74	CE		
C	SK465	ECO INC PK WAS 10K, J8-2 WAS -9V	5 MAY 74	DB		
B	?150	ECO INCORP	14 MAR 73	DJ		
A	SK122	PROD REL & ECO INCORP	17 APR 73	RAP		

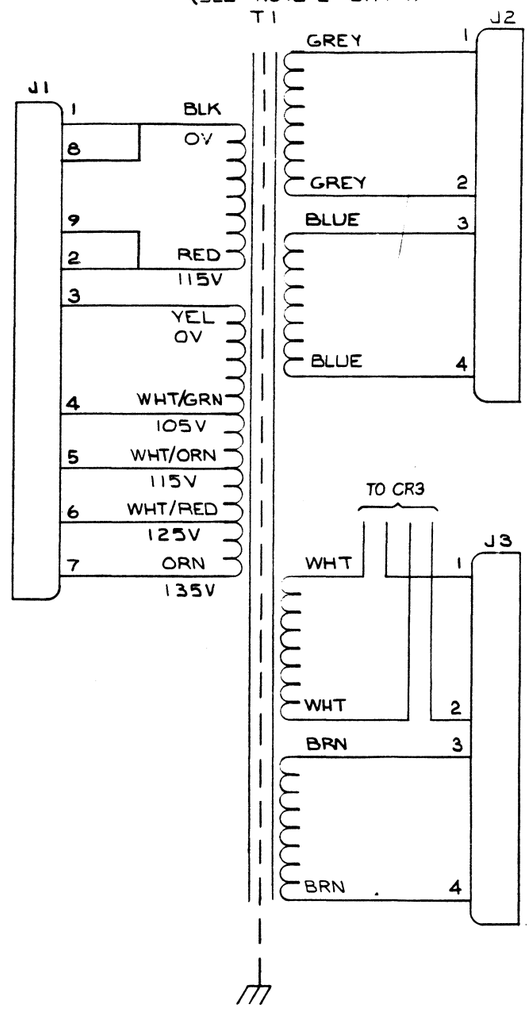
used on: SKD 3044A
drawn: RAP
date: 7 APR 73
design: ENG
unless specified .00 ± .01 fraction ± 1/64 .000 ± .005 angles ± 0 30'

CONSOLIDATED COMPUTER INC. OTTAWA

title: SCHEMATIC POWER SUPPLY DATA TERMINAL

SKD 13244E

ALTERNATE TRANSFORMER COLOR CODE
(SEE NOTE 2 SHT 1)



SHEET 1 IS 'D' SIZE

rev	eco	description	date	by	chk	apprvd
F	SK 572	SEE SH1	11NOV74	RC		
E	SK 573	SEE SH 1	7NOV 74	RC		
D	SK 512	SEE SH 1		DB		
C	SK 465	SEE SHEET 1	8MAY74	CDB		
B		SEE SHT 1	24MAY73	DJ		

used on: SKD13044A
scale: —
date: 24 MAY 73
drawn: DJ
design eng:
checked:
final apprvl:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0°30'
material:
finish:

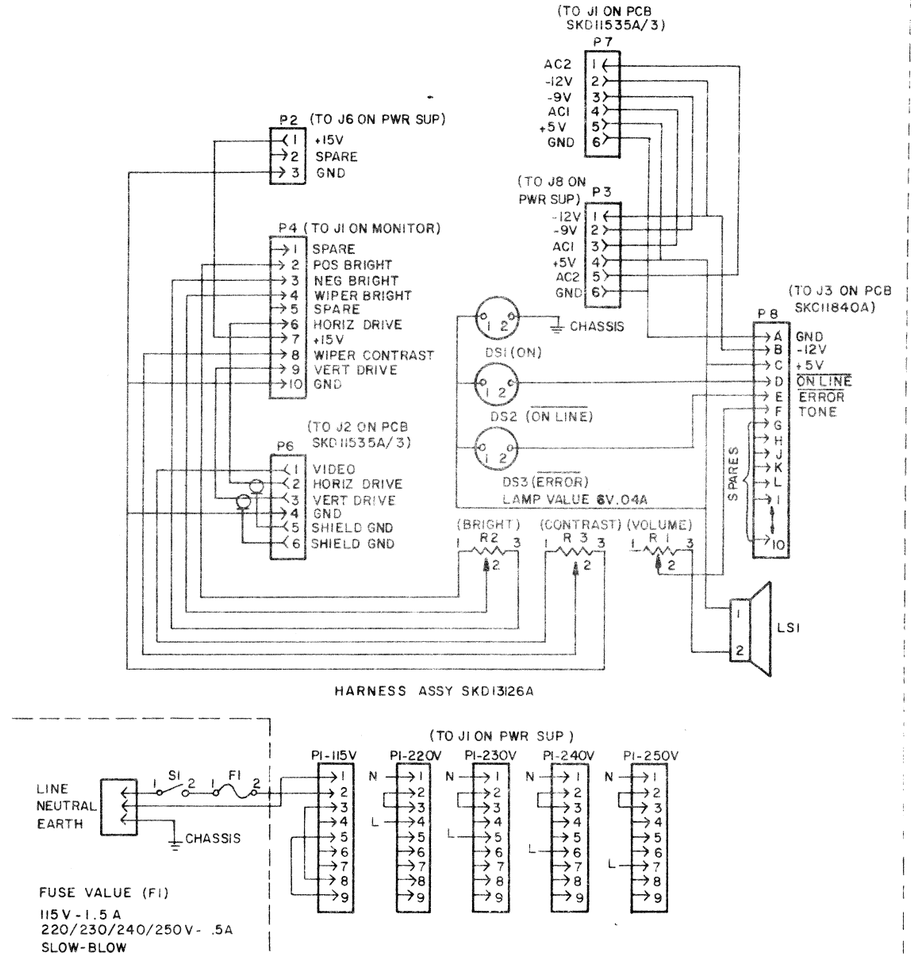
CONSOLIDATED COMPUTER INC.
OTTAWA

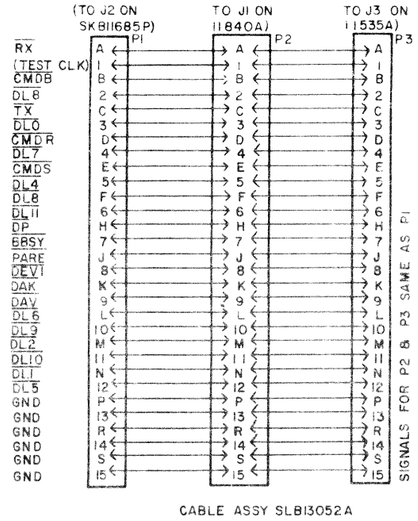
title: SCHEMATIC POWER SUPPLY DATA TERMINAL
sheet 2 of 2
no. SKD13044S
rev F

CABLE CONNECTIONS AND WIRING

The KDT cable connections are illustrated in drawing 130421. KDT wiring is illustrated in Figure 2-21. The following list details power supply wiring:

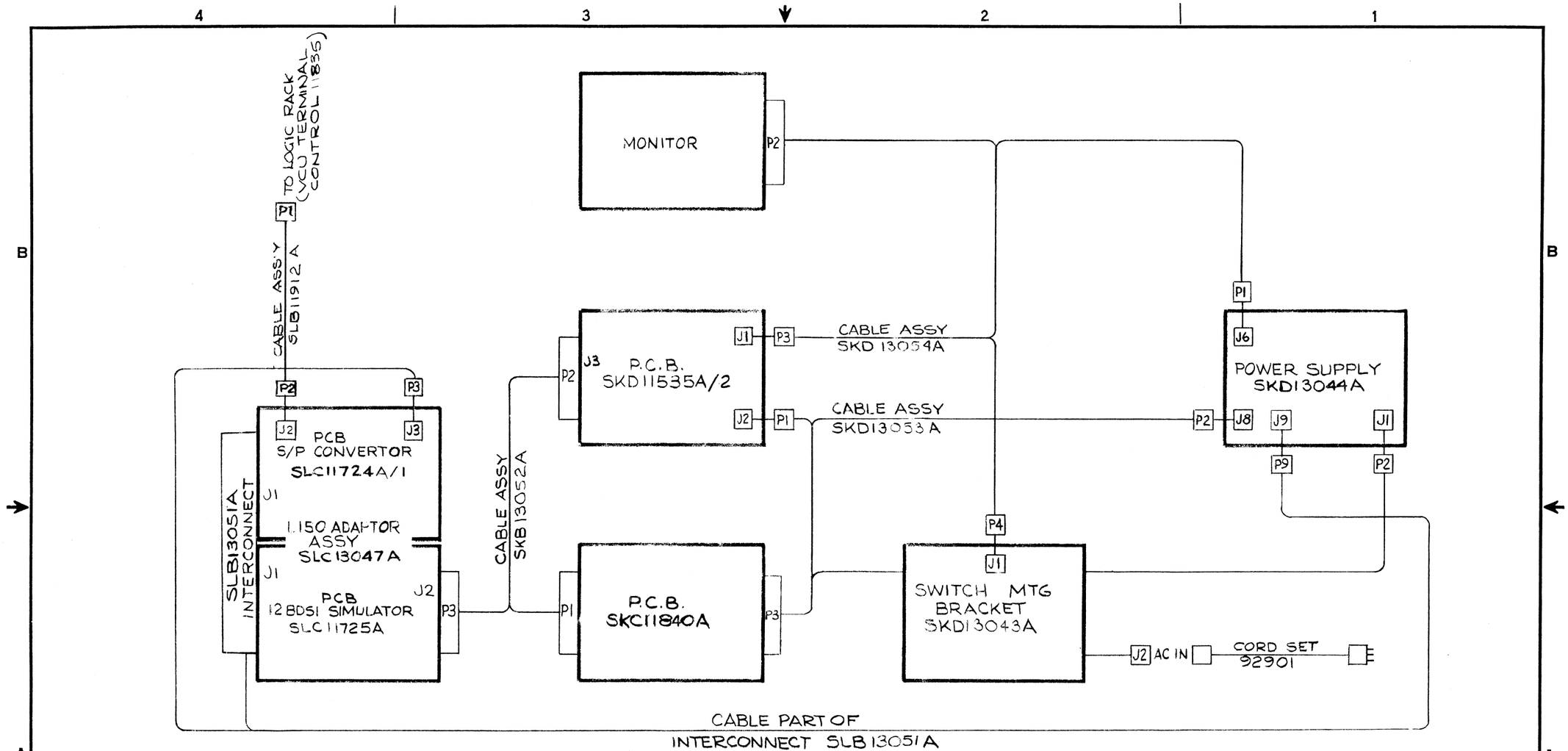
CONNECTOR		SIGNAL	COLOUR CODE
From	To		
T1	J1-1	0	BRN
T1	J1-2	115	RED
T1	J1-3	0	BLK
T1	J1-4	105	BLK/YEL
T1	J1-5	115	BLK/RED
T1	J1-6	125	BLK/ORN
T1	J2-1, F		GREY
T1	J2-2, M		GREY
T1	J1-3, M		BLUE
T1	J2-4, M		BLUE
T1	J3-1, M		WHT
T1	J3-2, F		WHT
T1	J3-3, F		VIO
T1	J3-4, F		VIO
Q1-C	J4-1, F		BLK
Q1-B	J4-1, F		BLK
Q1-E	J4-3, M		BLK
Q3-C	J5-1, F		BLK
Q3-B	J5-2, M		BLK
Q3-E	J5-3, F		BLK
T1	J1-7	135	ORN





CABLE ASSY SLBI3052A

FIGURE 2-21
DATA TERMINAL WIRING



rev	eco	description	date	by	chk	apprvd
2	SL 285	TITLE CHANGED	9 NOV 73	MJ		RJW
1	SL 123	PREPRODUCTION RELEASE	4 MAY 73	DJ		

used on: SLD13042A
scale: NONE
date: 4 MAY 73
drawn: DJ
design ENG: D WALSH
checked:
final apprvl:
unless specified
.00 = ±.01 fraction ± 1/64
.000 = ±.005 angles = ± 0 30'
material:
finish:

CONSOLIDATED COMPUTER INC. OTTAWA

title: DIAGRAM CABLE CONNECTIONS DATA TERMINAL SERIES L PHASE I & II

sheet 1 of 1
no. SLB13042 I
rev 2

TRANSTEX 15 500-8-72

KDT MAINTENANCE NOTES

Basic KDT maintenance procedures are described in Part 9 of this manual. However, two major items are detailed below.

To remove or install the Ball Brothers pcb:

1. Switch off ac power to KDT
2. Remove KDT power supply unit
3. Remove or install pcb.

CAUTION: Switch off the ac supply to the KDT before removing or installing the VCU Terminal Control pcb to KDT Terminal Control pcb to KDT cable, 12048.

Always allow at least 5 seconds discharge time before reinstating the supply.

APPENDIX 2-1

12 BD SI LINE

The 12 BD SI line assignment is as follows:

MNEMONIC	CONNECTOR J1	FUNCTION
$\overline{\text{CMDB-X}}$	B	The COMMAND BIT, if set, indicates that the data being transferred is a command word.
$\overline{\text{CMDR-X}}$	D	The COMMAND RESET bit resets the $\overline{\text{BBSY}}$ line.
$\overline{\text{CMDS-X}}$	E	COMMAND SET sets the $\overline{\text{BBSY}}$ line true.
$\overline{\text{BBSY-X}}$	F	The BUS BUSY line defines the status of the 12 BD SI line.
$\overline{\text{TX-X}}$	C	The TRANSMIT line indicates that the KDT is in the transmit mode (i.e., the system is sending data to the KDT).
$\overline{\text{RX-X}}$	A	The RECEIVE line indicates that the KDT is in the Receive mode (i.e., the KDT is sending data to the system).

MNEMONIC	CONNECTOR J1	FUNCTION
$\overline{\text{DAV-X}}$	9	The DATA AVAILABLE line indicates to the KDT Controller that data is available for transfer.
$\overline{\text{DAK-X}}$	K	The DATA ACKNOWLEDGE line indicates to the KDT Controller that data transfer is complete.
$\overline{\text{DP-X}}$	H	The DATA PARITY bit ensures that data parity is odd.
$\overline{\text{DL00-X}}$	3	If $\overline{\text{CMDB}}$ is low, $\overline{\text{DL00-08}}$ represent a command to the device and $\overline{\text{DL09-11}}$ address the devices on the 12 BD SI line. If $\overline{\text{CMDB}}$ is high, $\overline{\text{DL00-11}}$ represent data to the device.
$\overline{\text{DL01-X}}$	N	
$\overline{\text{DL02-X}}$	M	
$\overline{\text{DL03-X}}$	2	
$\overline{\text{DL04-X}}$	25	
$\overline{\text{DL05-X}}$	12	
$\overline{\text{DL06-X}}$	L	
$\overline{\text{DL07-X}}$	4	
$\overline{\text{DL08-X}}$	F	
$\overline{\text{DL09-X}}$	10	
$\overline{\text{DL10-X}}$	11	
$\overline{\text{DL11-X}}$	6	

APPENDIX 2-2

VDU Character Codes

	000	040	100	140
00	-0	BLANK	@	SPARE
01	-1	!	A	a
02	-2	"	B	b
03	-3	#	C	c
04	-4	$	D	d
05	-5	%	E	e
06	-6	&	F	f
07	-7	'	G	g
10	-8	(	H	h
11	-9	)	I	i
12	¢	*	J	j
13	Δ	+	K	k
14	∇	,	L	l
15	CR	-	M	m
16	_	.	N	n
17	SPARE	/	O	o
20	|	0	P	p
21	⌐	1	Q	q
22	□	2	R	r
23	▨	3	S	s
24	→	4	T	t
25	↓	5	U	u
26	↑	6	V	v
27	←	7	W	w
30	Å	8	X	x
31	Ä	9	Y	y
32	Ö	:	Z	z
33	£	;	[	½
34	..	<	\	10
35	S	=	]	11
36	┼	>	^	12
37	┼	?	—	NULL

VIDEO DISPLAY CHARACTER CODES - KATAKANA

	000	40	000	40	000	40		40	140	100	140	100	140	100
00	ア	SPACE	12 ¢	*	24 シ	4	36 ¥	)	50 ハ	H	62 ヤ	R	74 ン	/
01	イ	!	13 Δ	+	25 ↓	5	37 キ	?	51 ヒ	I	63 ユ	S	75 ゛	]
02	ウ	"	14 ∇	,	26 ↑	6	140 00 ツ	100 @	52 フ	J	64 ヨ	T	76 °	^
03	エ	#	15 CR	-	27 ←	7	01 テ	A	53 ヘ	K	65 ラ	U	77 NULL	—
04	オ	$	16 ー	.	30 ス	8	02 ト	B	54 ホ	L	66 リ	V		
05	カ	%	17 サ	/	31 セ	9	03 ナ	C	55 マ	M	67 ル	W		
06	キ	&	20 ｜	ø	32 ソ	:	04 ニ	D	56 ミ	N	70 レ	X		
07	ク	'	21 ⌐	!	33 タ	;	05 ヌ	E	57 ム	O	71 ロ	Y		
10	ケ	(	22 □	2	34 ‥	<	06 ネ	F	60 メ	P	72 ワ	Z		
11	コ	)	23 ■	3	35 チ	=	07 ノ	G	61 モ	Q	73 1/2	[		