PART 2A
MK 2 DATA TERMINAL

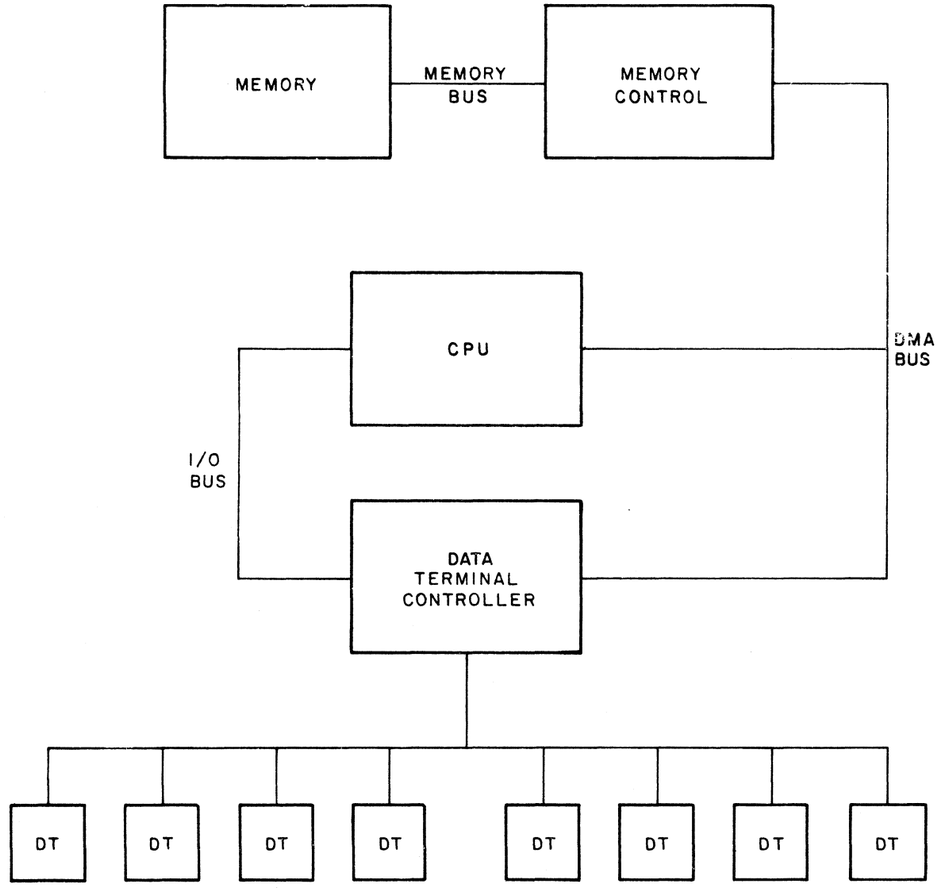
CONTENTS

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS

TABLES



NOTE: ONE DATA TERMINAL CONTROL PCB CONTROLS EIGHT DT (MAXIMUM OF FOUR CONTROL PCB)

FIGURE 2A-1
KE 50 DT CONFIGURATION

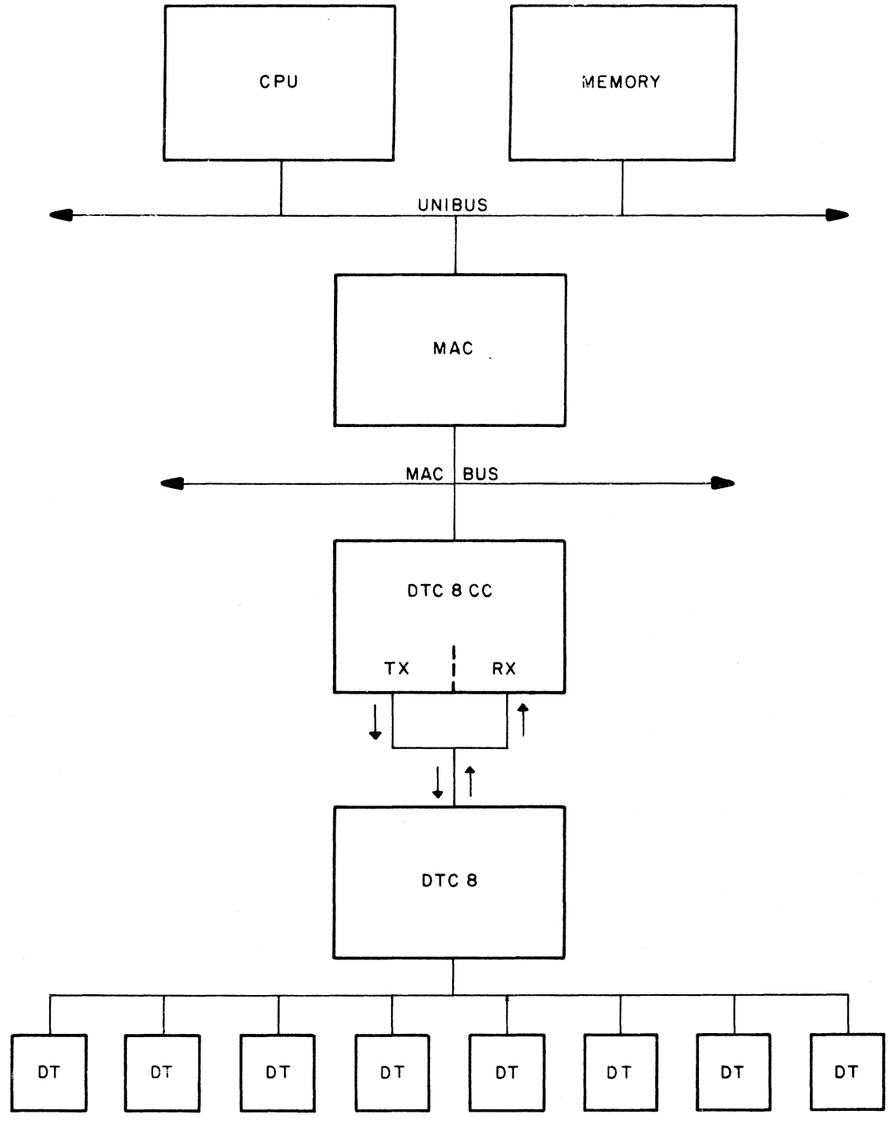


FIGURE 2A-2
KE 1000 DT CONFIGURATION

INTRODUCTION

The Data Terminal is used in both the KEY-EDIT 50 and the KEY-EDIT 1000 systems. For the purpose of this document, the following abbreviations apply:

- KEY-EDIT 50 is designated KE 50
- KEY-EDIT 1000 is designated KE 1000.

Each system uses a different interface for the terminal: the KE 50 uses a serial bit interface, and the KE 1000 uses a parallel bit interface. Thus, the data terminal has two interchangeable interface adapters.

This description assumes that the reader understands the respective interface of each system and the data terminal controller of that system. Figures 2A-1 and 2A-2 illustrate the relative position of the data terminal in the systems.

PURPOSE

The data terminal is the data entry and display station of the KEY-EDIT system, and comprises two independent devices: a Keyboard, and a Video Display Unit (VDU).

The Keyboard transfers data to memory via a 12 BD SI line, a DTC 8, a DTC 8 CC, and a MAC (KE 1000); or via a serial line and a Terminal Controller (KE 50). The VDU displays data messages sent to the data terminal by the software. These messages are explained in the KE 1000 Operator's Procedures Manual (1143) and the KE 50 Operator's Procedures Manual (5143).

CAPABILITIES

The data terminal is a self-contained unit that comprises a keyboard, a VDU, an interface, and a power supply. The capabilities of the data terminal are described in relation to these components.

KEYBOARD

The keyboard can have a maximum of 112 keys. The operation of the keyboard is controlled by its Command Register (CR). The software loads the Keyboard CR with a command word, causing the keyboard to perform any of the following operations:

- send status
- send data
- indicate operational status by tones and indicator lamps
- perform error checking.

When commanded by the program the keyboard sends a status word defining the keyboard address (7_8), and the keyboard style (i.e., 029, or teletype).

Once placed on-line by a command word, the keyboard transfers a word when a key is depressed, or when a key that has been assigned a release code is released. One bit of the word distinguishes between a word generated by key depression and a word generated by key release. In either case, the word contains the address of the key that was depressed or released.

The software uses the key address to find a character in a look-up table in memory. The base address of the table is determined by the keyboard status (i.e., the keyboard layout used). Thus, by generating a key address instead of character code, the keyboard can be adapted to any keyboard layout simply by altering the look-up table.

The keyboard indicates its operation status by using tones and indicator lamps. Figures 2A-3 and 2A-4 illustrate the data terminal indicators and controls.

When the terminal is powered up, the READY lamp (yellow) is lit. The ON-LINE lamp is lit when the keyboard is on-line. (When used with the KE 1000 system, the keyboard powers up off-line, and when used with the KE 50 system, the keyboard powers up on-line.) The ERROR lamp is lit when the keyboard detects an error or the software sets the error bit in the Command Register, and flashes to gain the operator's attention.

The keyboard can generate four tones. It generates a 50 ms, 430 Hz tone whenever a key is depressed. This tone is necessary because there is no mechanical noise (as in a keypunch) to inform the operator that she has operated a key.

The other three tones can be generated under control of the Command Register. The tones are:

- TONE 1 = 550 Hz
- TONE 2 = 830 Hz
- TONE 3 = 1320 Hz

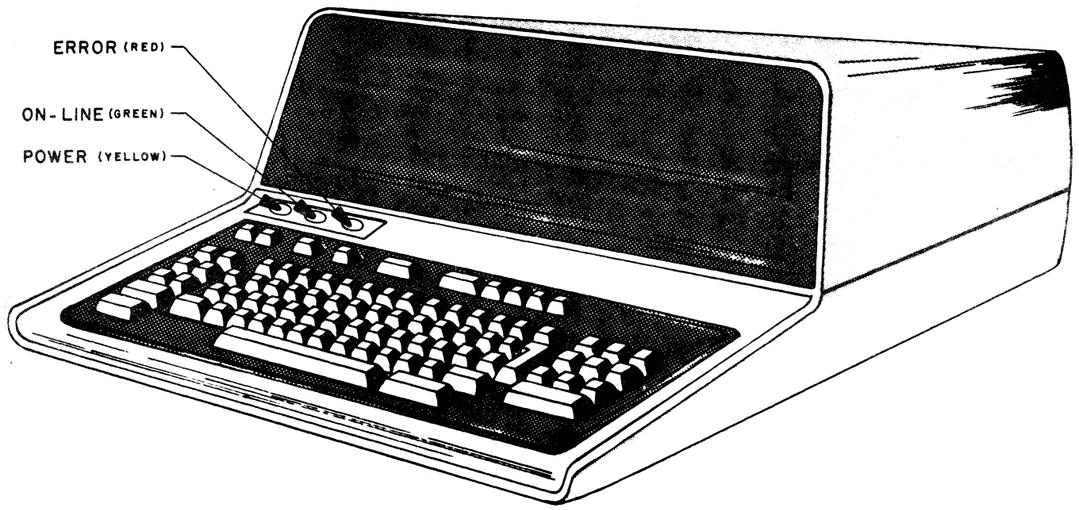


FIGURE 2A-3
DATA TERMINAL INDICATORS

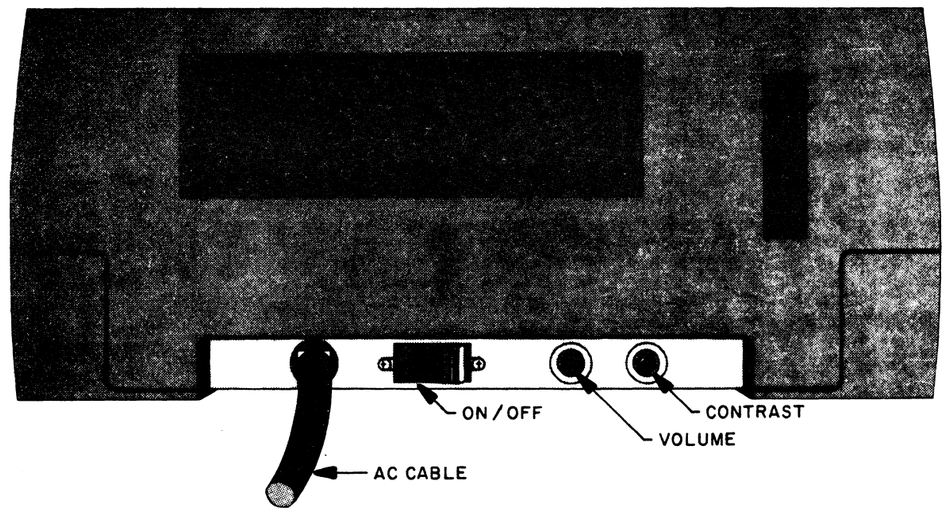
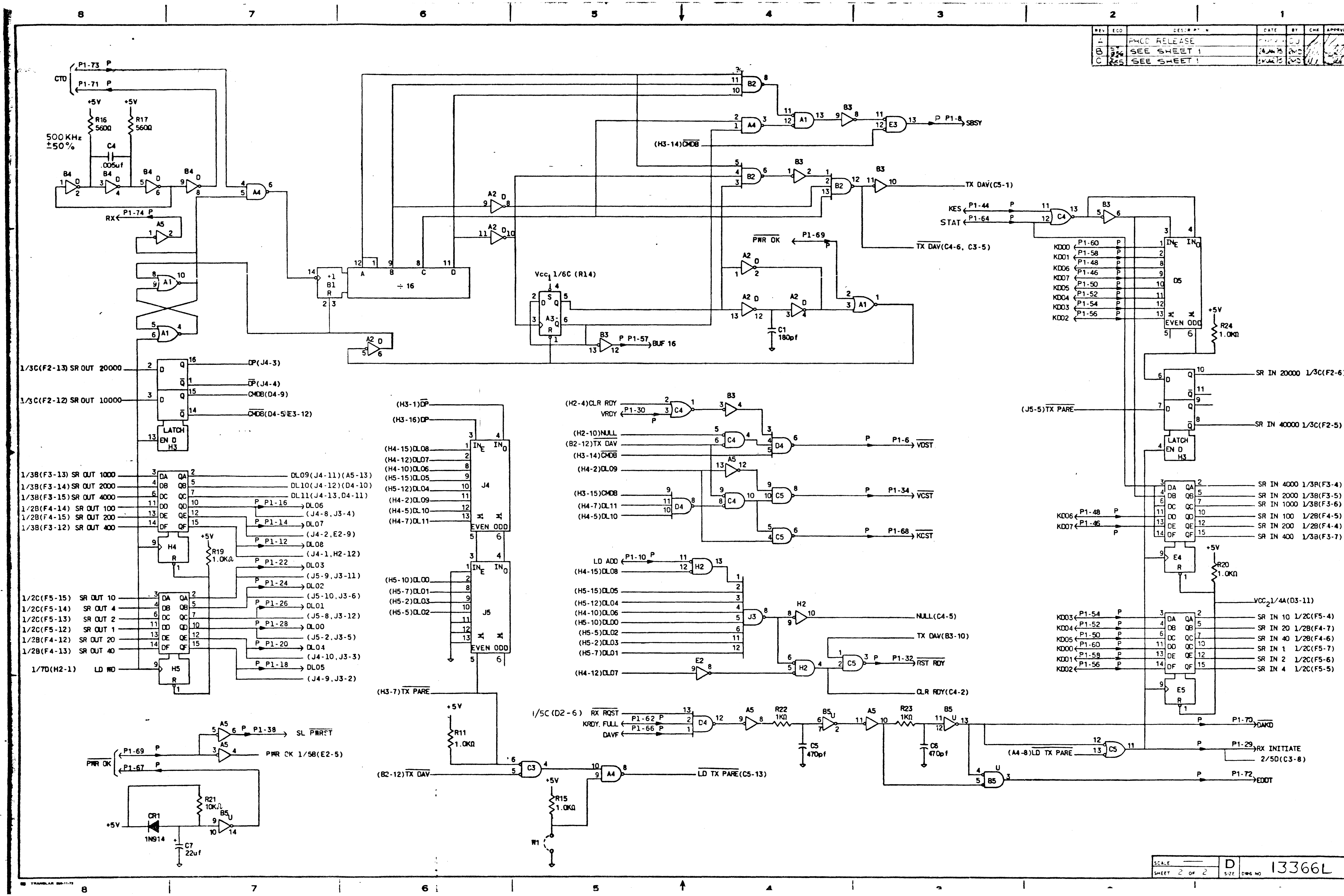


FIGURE 2A-4
DATA TERMINAL CONTROLS



A PHCO RELEASE
B SEE SHEET 1
C SEE SHEET 1
CTO
P1-73
P1-71
+5V
R16 560Ω
R17 560Ω
500 KHz ±50%
C4 .005uf
B4
A4
RX
P1-74
A5
A1
B1
÷ 16
B2
A4
A1
B3
E3
P1-8 SBSY
(H3-14) CMDB
TX DAV (C5-1)
TX DAV (C4-6, C3-5)
KES P1-44
STAT P1-64
C4
PWR OK P1-69
A2
A3
Vcc 1/6C (R14)
C1 180pf
P1-57 BUF 16
D5
EVEN ODD
R24 1.0KΩ
1/3C (F2-13) SR OUT 20000
1/3C (F2-12) SR OUT 10000
DP (J4-3)
DP (J4-4)
CMDB (D4-9)
CMDB (D4-5/E3-12)
LATCH EN D H3
1/3B (F3-13) SR OUT 1000
1/3B (F3-14) SR OUT 2000
1/3B (F3-15) SR OUT 4000
1/2B (F4-14) SR OUT 100
1/2B (F4-15) SR OUT 200
1/3B (F3-12) SR OUT 400
H4
R19 1.0KΩ
1/2C (F5-15) SR OUT 10
1/2C (F5-14) SR OUT 4
1/2C (F5-13) SR OUT 2
1/2C (F5-12) SR OUT 1
1/2B (F4-12) SR OUT 20
1/2B (F4-13) SR OUT 40
1/7D (H2-1) LD WD
H5
J4
J5
(H3-1) DP
(H3-16) DP
(H3-7) TX PARE
(B2-12) TX DAV
C3
R11 1.0KΩ
R15 1.0KΩ
W1
LD TX PARE (C5-13)
(H2-4) CLR RDY
VRDY P1-30
(H2-10) NULL
(B2-12) TX DAV
(H3-14) CMDB
(H4-2) DL09
(H3-15) CMDB
(H4-7) DL11
(H4-5) DL10
P1-6 VDST
P1-34 VCST
P1-68 KCST
LD ADD P1-10
(H4-15) DL08
J3
NULL (C4-5)
TX DAV (B3-10)
P1-32 RST RDY
CLR RDY (C4-2)
1/5C (D2-6) RX RQST
KRDY, FULL P1-62
DAVF P1-66
R22 1KΩ
R23 1KΩ
C5 470pf
C6 470pf
P1-70 DAKD
P1-29 RX INITIATE 2/5D (C3-8)
(A4-8) LD TX PARE
P1-72 EDDT
SR IN 20000 1/3C (F2-6)
(J5-5) TX PARE
SR IN 40000 1/3C (F2-5)
SR IN 4000 1/3B (F3-4)
SR IN 2000 1/3B (F3-5)
SR IN 1000 1/3B (F3-6)
SR IN 100 1/2B (F4-5)
SR IN 200 1/2B (F4-4)
SR IN 400 1/3B (F3-7)
E4
R20 1.0KΩ
VCC 2 1/4A (D3-11)
SR IN 10 1/2C (F5-4)
SR IN 20 1/2B (F4-7)
SR IN 40 1/2B (F4-6)
SR IN 1 1/2C (F5-7)
SR IN 2 1/2C (F5-6)
SR IN 4 1/2C (F5-5)
E5
SL PWRST P1-38
PWR OK 1/5B (E2-5)
PWR OK P1-69 P1-67
CR1 1N914
R21 10KΩ
C7 22uf
SHEET 2 OF 2
D
13366L

KEYBOARD

Command Initiation

When a program sends a command word to the Keyboard, the Interface pcb (L/150 or 12 BD SI) generates $\overline{\text{KCST}}$ and gates the command bits onto DL00 - DL06. The Keyboard Command Register logic is illustrated in Figure 2A-15.

The leading edge of $\overline{\text{KCST}}$ loads DL01 - DL04 and DL06 into the Keyboard CR, and the trailing edge loads in DL00 and DL05. Table 2A-2 defines the bit assignment of the Keyboard CR, and the function of each bit.

TABLE 2A-2

KEYBOARD COMMAND REGISTER

BIT	INPUT	MNEMONIC	FUNCTION
06	DL06	KRDY	KEYBOARD READY is set when the keyboard is to be placed on-line, enabling the keyboard to transfer a data word when a key is depressed, or a status word when the status bit is set.
05	DL05	FLASH	This bit is set in conjunction with the tone bits to cause an interrupted tone.
04 03	DL04 DL03	TONE 2 TONE 1	These bits control the tone generator, enabling it to generate one of three tones: TONE 1 = 550 Hz TONE 2 = 830 Hz TONE 3 = 1320 Hz (TONE 1 · TONE 2).
02	DL02	½ SECOND	This bit is set in conjunction with the tone bits to cause the tone to end after 0.5 second.
01	DL01	STATUS	When STATUS and KRDY are set, the keyboard transfers a status word. On completion of the transfer, STATUS is reset.
00	DL00	ERROR	The ERROR bit is set by the program when it detects an error in the data received from the keyboard. When ERROR is set, the error lamp flashes.

Command Execution

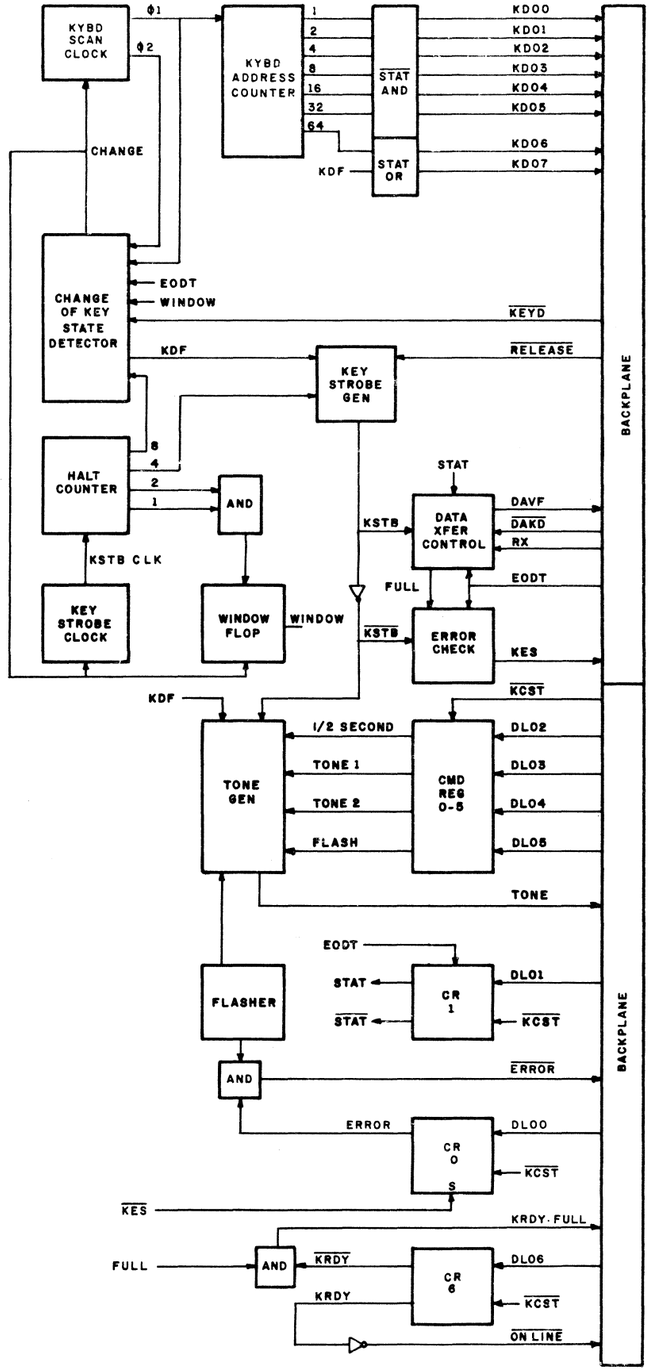
INTRODUCTION

The keyboard can execute four operations:

- data word transfer to the Terminal Controller or DTC 8 when a key is depressed (the data sent is actually the address of the depressed key)
- status word transfer, when the STATUS bit is set in the CR, to define the keyboard address (7_8) and the keyboard style (i.e., TTY or 029)
- tone generation
- indicator lamp illumination.

DATA TRANSFER

The keyswitches of the keyboard are connected at the crosspoints of a 15 by 8 line matrix on the Keyboard pcb. (The Keyboard pcb logic is shown on drawing 13132L.) The keyboard control logic addresses each key in sequence, stores the state of the key, and compares it to the previous state of the key. When a change is detected, the control logic initiates a data transfer if the change was caused by a depressed key, or if the change was caused by a released key that has been assigned a release code. Figure 2A-15 is a block diagram of the keyboard logic.



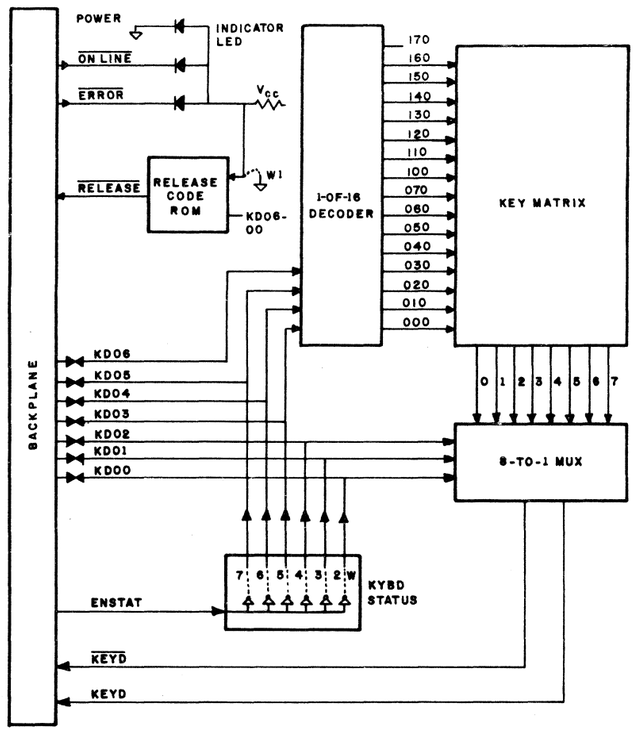


FIGURE 2A-15
KEYBOARD BLOCK DIAGRAM

11	10	09	08	07	06	05	04	03	02	01	00

DL11 STATUS INDICATOR
DL10-08 KYBD ADDRESS
DL07-06 NOT USED
DL05-00 KYBD STYLE CODE

FIGURE 2A-16
STATUS WORD

These tones are generated to inform the operator of various operational conditions. TONE 2 is also generated when the keyboard detects an error.

The keyboard detects two errors:

- a double keystroke error, which occurs when two keys are depressed within 8.5 ms of each other
- a data transfer error, which occurs when a key is depressed and a word is not transferred to the Data Terminal Controller within 4 ms.

When it detects either error, the keyboard flashes the ERROR lamp, generates TONE 2 (830 Hz), and sets an error bit in the next word transferred to memory.

VIDEO DISPLAY UNIT

The operation of the VDU is also controlled by its Command Register. The VDU CR is loaded by the program to turn it on-line or off-line and to control its operation when on-line.

The VDU can display a maximum of 480 characters (12 lines of 40 characters each). Each character can be cursored (underlined) and/or delineated (vertically lined). The VDU uses an 8 x 12 matrix to display each character (this large matrix allows the terminal to display many different alphabets, such as Japanese).

The VDU can be commanded to update:

- any single character on the screen
- any line of characters
- any partial line of characters (from any point on the line to the end of the line only)
- all characters on the screen.

INTERFACE

The Data Terminal can adapt to either of the KEY-EDIT systems (KE 50, KE 1000) by using one of two interface pcb.

The internal operation of the Data Terminal is compatible to the 12 BD SI interface; that is, a parallel bit interface. Therefore, when used in a KE 1000 system, the Data Terminal uses a 12 BD SI Interface pcb that allows the Data Terminal and the DTC 8 to communicate via a 12 BD SI interface cable, which may be up to 100 feet long.

If the Data Terminal is used on a KE 50 system, the Data Terminal uses an L/150 Adapter pcb that allows the Data Terminal and Video Control Unit (VCU) to communicate via a serial interface cable which may be up to 500 feet long. The L/150 Adapter must convert data and commands from serial to parallel and vice versa.

POWER

The Data Terminal has its own power supply that can operate on 100, 115, 220, 230 or 240 V ac, depending on the transformer used and how it is tapped. The power supply provides all the dc voltages required to operate the logic and the Cathode Ray Tube (CRT).

COMMAND SEQUENCE

There are three stages in a command sequence: Command Initiation, Command Execution, and Command Termination. A command is initiated when the program controlling that device loads a command word into the Keyboard or VDU Command Register. Command Execution is the operation performed by the device as a result of the Command Register loading. A command is terminated when:

- the device completes the required operation
- the program clears the command from the device CR.

The Data Terminal description is divided into four sections: Interface, Keyboard, VDU, and Power. The first section explains how data, status, and command words are transferred between the Data Terminal and the DTC 8 (KE 1000) or Terminal Controller (KE 50). The second section describes the operation of the Keyboard, and the third section describes the operation of the VDU. The fourth section describes the power supply.

INTERFACE

The Data Terminal uses one of two Interface pcb. In a KE 1000 system, it uses a 12 BD SI Interface pcb; an L/150 Adapter pcb is used in a KE 50 system.

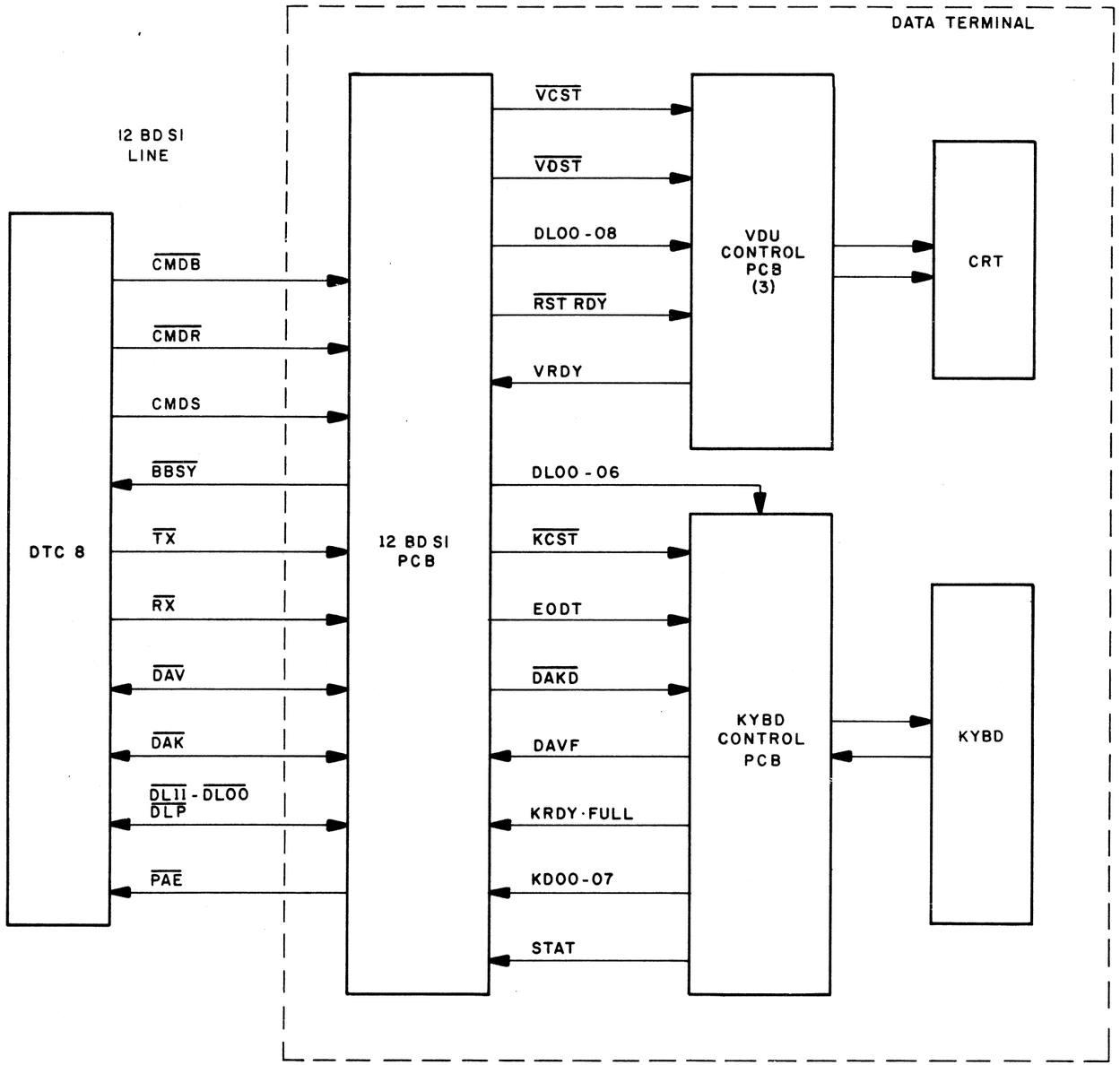
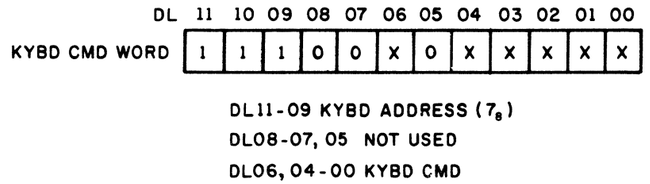
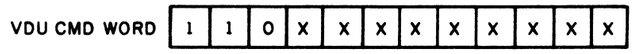


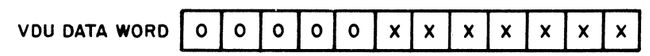
FIGURE 2A-5
12 BD SI DATA FLOW & CONTROL



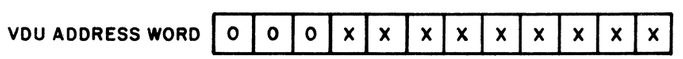
DL11-09 KYBD ADDRESS (7_8)
DL08-07, 05 NOT USED
DL06, 04-00 KYBD CMD



DL11-09 VDU ADDRESS (6_8)
DL08-00 VDU CMD



DL11-07 NOT USED
DL06-00 DATA



DL11-09 NOT USED
DL08-00 VDU ADDRESS

FIGURE 2A-6
12 BD SI TRANSMIT WORD STRUCTURE

12 BD SI Interface

In the KE 1000 system, the Data Terminal communicates with a Data Terminal Concentrator (DTC 8) via a 12-Bit Data Standard Interface (12 BD SI) cable. The cable has 11 control and 12 data lines. Table 2A-1 defines the function of each line.

12 BD SI PCB

FUNCTIONAL DESCRIPTION

The 12 BD SI PCB allows two-way word transfer between the Data Terminal and the DTC 8. Figure 2A-5 illustrates the data flow between the DTC 8, the Keyboard, and VDU.

The DTC 8 transmits words to either the Keyboard or the VDU, and receives words from the Keyboard only. When the DTC 8 transmits a word to the Data Terminal, the 12 BD SI pcb determines whether the word is a command for the Keyboard, a command for the VDU, or a data or address word for the VDU. Figure 2A-6 illustrates the four word structures.

When the DTC 8 transmits a command word to the Data Terminal, it asserts $\overline{\text{CMDB}}$ of the 12 BD SI line. $\overline{\text{CMDB}}$ enables the 12 BD SI pcb to decode $\overline{\text{DL11}}$ - $\overline{\text{DL09}}$. If $\overline{\text{DL11}}$ - $\overline{\text{DL09}}$ equal 7_8, the pcb generates KEYBOARD COMMAND STROBE (KCST) when the DTC 8 asserts $\overline{\text{DAV}}$. KCST loads $\overline{\text{DL00}}$ - $\overline{\text{DL06}}$ into the Keyboard CR. If $\overline{\text{DL11}}$ - $\overline{\text{DL09}}$ equal 6_8, the 12 BD SI pcb generates VIDEO COMMAND STROBE (VCST) to load $\overline{\text{DL01}}$ - $\overline{\text{DL08}}$ into the VDU CR.

TABLE 2A-1

12 BD SI CABLE

MNEMONIC	
$\overline{\text{TX}}$	The DTC 8 controls the $\overline{\text{TRANSMIT}}$ line; the line is asserted when the DTC 8 transmits a word to the Data Terminal.
$\overline{\text{RX}}$	The DTC 8 also controls the $\overline{\text{RECEIVE}}$ line. $\overline{\text{RX}}$ is false only when the DTC 8 is transmitting data on the 12 BD SI line. When $\overline{\text{RX}}$ is true, the Keyboard can initiate a word transfer to the DTC 8. NOTE: There is a period in the transmit sequence when both $\overline{\text{RX}}$ and $\overline{\text{TX}}$ are false. This time allows the Keyboard to complete a word transfer initiated when $\overline{\text{RX}}$ was true.
$\overline{\text{CMDB}}$	The DTC 8 asserts $\overline{\text{COMMAND BIT}}$ if it is transferring a command word for either the Keyboard or VDU. If $\overline{\text{CMDB}}$ is false, the word being transferred is a data or address word for the VDU.
$\overline{\text{CMDR}}$	The DTC 8 asserts $\overline{\text{COMMAND RESET}}$ to reset the $\overline{\text{BBSY}}$ flop in the Data Terminal.
$\overline{\text{CMDS}}$	The DTC 8 asserts $\overline{\text{COMMAND SET}}$ to set the $\overline{\text{BBSY}}$ flop in the Data Terminal when transferring a command word to the Data Terminal.
$\overline{\text{BBSY}}$	The DTC 8 checks the state of the $\overline{\text{BUS BUSY}}$ line after the $\overline{\text{CMDR}}$ and $\overline{\text{CMDS}}$ strobes. If $\overline{\text{BBSY}}$ is not in the correct state after each strobe, the DTC 8 terminates the transfer.
$\overline{\text{DAV}}$	$\overline{\text{DATA AVAILABLE}}$ is asserted by the DTC 8 to transfer data into the terminal. The terminal asserts $\overline{\text{DAV}}$ when it transfers data to the DTC 8.
$\overline{\text{DAK}}$	The device receiving data asserts $\overline{\text{DATA ACKNOWLEDGE}}$ to acknowledge the data. On receipt of $\overline{\text{DAK}}$, the transmitting device clears $\overline{\text{DAV}}$.
$\overline{\text{LINT}}$	$\overline{\text{LINE INTERRUPT}}$ allows a device to initiate an interrupt; however, it is not used by the Data Terminal.
$\overline{\text{DL00}}$ $\overline{\text{DL01}}$ $\overline{\text{DL02}}$ $\overline{\text{DL03}}$ $\overline{\text{DL04}}$ $\overline{\text{DL05}}$ $\overline{\text{DL06}}$ $\overline{\text{DL07}}$ $\overline{\text{DL08}}$ $\overline{\text{DL09}}$ $\overline{\text{DL10}}$ $\overline{\text{DL11}}$	If CMDB is true, $\overline{\text{DATA LINES 00}}$ - $\overline{11}$ represent a command word. $\overline{\text{DL11}}$ - $\overline{\text{DL09}}$ define the address of the device (7_8 = Keyboard, 6_8 = VDU). $\overline{\text{DL08}}$ - $\overline{\text{DL00}}$ define the command for that device. If $\overline{\text{CMDB}}$ is false, $\overline{\text{DL00}}$ - $\overline{\text{DL11}}$ represent a data (Keyboard or VDU), status (Keyboard), or address (VDU) word.
$\overline{\text{DLP}}$	$\overline{\text{DATA LINE PARITY}}$ is conditioned by the transmitting device (DTC 8 or Keyboard) to maintain odd data parity.
$\overline{\text{PAE}}$	When the DTC 8 transmits a word to the Data Terminal, the terminal checks word parity. If parity is incorrect (even), the Data Terminal asserts $\overline{\text{PARITY ERROR}}$, and the DTC 8 sets a parity error and terminates the transfer.

If the word transmitted is a data word, the 12 BD SI pcb generates VIDEO DATA STROBE (VDST), provided the VDU is on-line (VIDEO READY (VRDY) true). VDST loads $\overline{DL00}$ - $\overline{DL08}$ into the VDU Data Register.

The Keyboard can transfer a data, status, or error word to the DTC 8. Figure 2A-7 illustrates the three receive word structures. When the Keyboard has a word to transfer, it asserts KEYBOARD READY (KRDY) FULL and DAVF. If $\overline{TX}$ of the 12 BD SI line is false, the 12 BD SI pcb asserts $\overline{DAV}$ and gates the word onto the data lines $\overline{DL11}$ - $\overline{DL00}$. The DTC 8 responds by asserting $\overline{DAK}$ to terminate the transfer, and the 12 BD SI pcb generates END OF DATA TRANSFER (EODT) to clear KRDY · FULL.

DETAILED DESCRIPTION

Drawing 13133L illustrates the 12 BD SI Interface pcb logic. The pcb accepts words from the DTC 8 (transmit mode) or sends words to the DTC 8 (receive mode).

TRANSMIT MODE

Introduction

The transmit cycle of the DTC 8 has three periods, each serving a different purpose. Figure 2A-8 illustrates the transmit timing.

During the first period (T1) of the transmit cycle, the DTC 8 resets $\overline{RX}$ of the 12 BD SI line. This period allows the Keyboard to complete a word transfer initiated when $\overline{RX}$ was true.

During the second period (T2), the DTC 8 asserts $\overline{TX}$ and gates the word onto $\overline{DL11}$ - $\overline{DL00}$, and the 12 BD SI pcb checks data parity. If a parity error has occurred, the DTC 8 sets a parity error and terminates the transfer prematurely. When the DTC 8 transmits a command word, it performs a handshaking sequence with the 12 BD SI pcb by resetting and setting the $\overline{BBSY}$ flop with $\overline{CMDR}$ and $\overline{CMDS}$. The DTC 8 checks the state of $\overline{BBSY}$ after each strobe, and if it is not correct, the DTC 8 sets a data transfer error and terminates the transfer prematurely.

During the third period (T3) of the transmit cycle, the DTC 8 asserts $\overline{DAV}$, and the 12 BD SI pcb generates one of three strobes, $\overline{VCST}$, $\overline{BDST}$, or $\overline{KCST}$. $\overline{VCST}$ is generated to load $\overline{DL01}$ - $\overline{DL08}$ into the VDU CR when the word is a command for the VDU. $\overline{KCST}$ is generated if the word is a command for the Keyboard; $\overline{VDST}$ is generated if the word is data for the VDU.

The 12 BD SI pcb asserts $\overline{DAK}$ approximately 0.5 µs after $\overline{DAV}$ is asserted. $\overline{DAK}$ causes the DTC 8 to reset $\overline{DAV}$, terminating the transfer.

Command Word

When a command word is transmitted to the Data Terminal, the DTC 8 asserts $\overline{CMDB}$ during T2 and T3. $\overline{CMDB}$ enables gate A2-6 (drawing 13133L, sheet 1) to decode DL11 and DL10. If the command is for either the Keyboard or VDU, DL11 and DL10 are true and ADDRESS KEYBOARD + VDU (ADKV) is asserted. ADKV and $\overline{ADKV}$ enable the handshaking logic (F1-3, F1-2, F5-11) and the command strobe logic (C4-11, sheet 2).

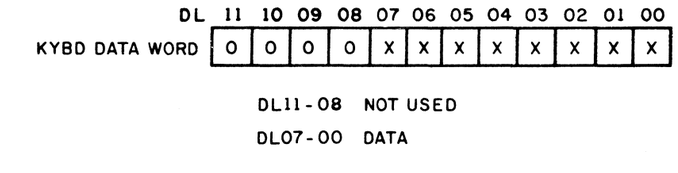


FIGURE 2A-7
12 BD SI RECEIVE WORD STRUCTURE

At $T2_2$, the DTC 8 asserts $\overline{CMDR}$ to reset the BBSY flop, F2-1, F2-4 (sheet 1). At $T2_3$, the DTC 8 checks $\overline{BBSY}$, and if it is not false, terminates the transfer immediately. If $\overline{BBSY}$ is false, the DTC 8 asserts $\overline{CMDS}$ at $T2_4$. $\overline{CMDS}$ sets the BBSY flop, and at $T2_5$ the DTC 8 checks $\overline{BBSY}$ again. If $\overline{BBSY}$ is not true, the DTC 8 terminates the transfer immediately. If $\overline{BBSY}$ is true, the DTC 8 checks $\overline{PAE}$ at $T2_6$. If it is true (incorrect parity), the DTC 8 terminates the transter immediately. The 12 BD SI pcb checks DL11 - DL00 and DLP in E3 and E4. If the parity is not odd, E4-6 goes high and $\overline{PAE}$ (A5-3) is asserted.

If the parity is correct, the DTC 8 asserts $\overline{DAV}$ to turn Q1 off, allowing DAVB at A3-10 (sheet 2) to go high and enable gate C4-11. This gate conditions the two command strobe gates, A4-11 and A4-10. If DL09 is true (DL11 - DL09 = 7_8), gate A4-11 is enabled to generate KCST and load the command word into the Keyboard CR. If DL09 is false (DL11 - DL09 = 6_8), gate A4-11 is enabled to generate $\overline{VCST}$ and load the command word into the VDU CR. Either strobe causes $\overline{DAK}$ (A5-11) to be asserted. $\overline{DAK}$ resets $\overline{DAV}$ in the DTC 8, which in turn clears the command strobe (KCST, VCST) and $\overline{DAK}$. If the DTC 8 does not receive $\overline{DAK}$ by $T3_7$, it terminates the transfer immediately. Normal transmission terminates at the end of T3, when DTC 8 resets $\overline{TX}$, clears the data from the line, and asserts $\overline{RX}$.

Data Word

The DTC 8 transmits a data word in the same way as a command word, except that $\overline{CMDB}$ is not asserted and therefore no handshaking sequence occurs during T2.

Parity is checked during T2 as it is for a command word transmission. If the parity is correct, the DTC 8 asserts $\overline{DAV}$ at T3 and $\overline{DAVB}$ goes high to condition gate A2-12. As $\overline{CMDB}$ is false, gate A2-12 is enabled if VRDY or RESET READY ENABLE (RST RDY E) is true, to generate $\overline{DAK}$ via gates A2-8 and A5-11. VDST is generated at A3-6 only if NULL + RST RDY is false. $\overline{NULL + RST\ RDY}$ enables gate B1-2 to assert VDST and load DL00 - DL08 into the VDU Data Register.

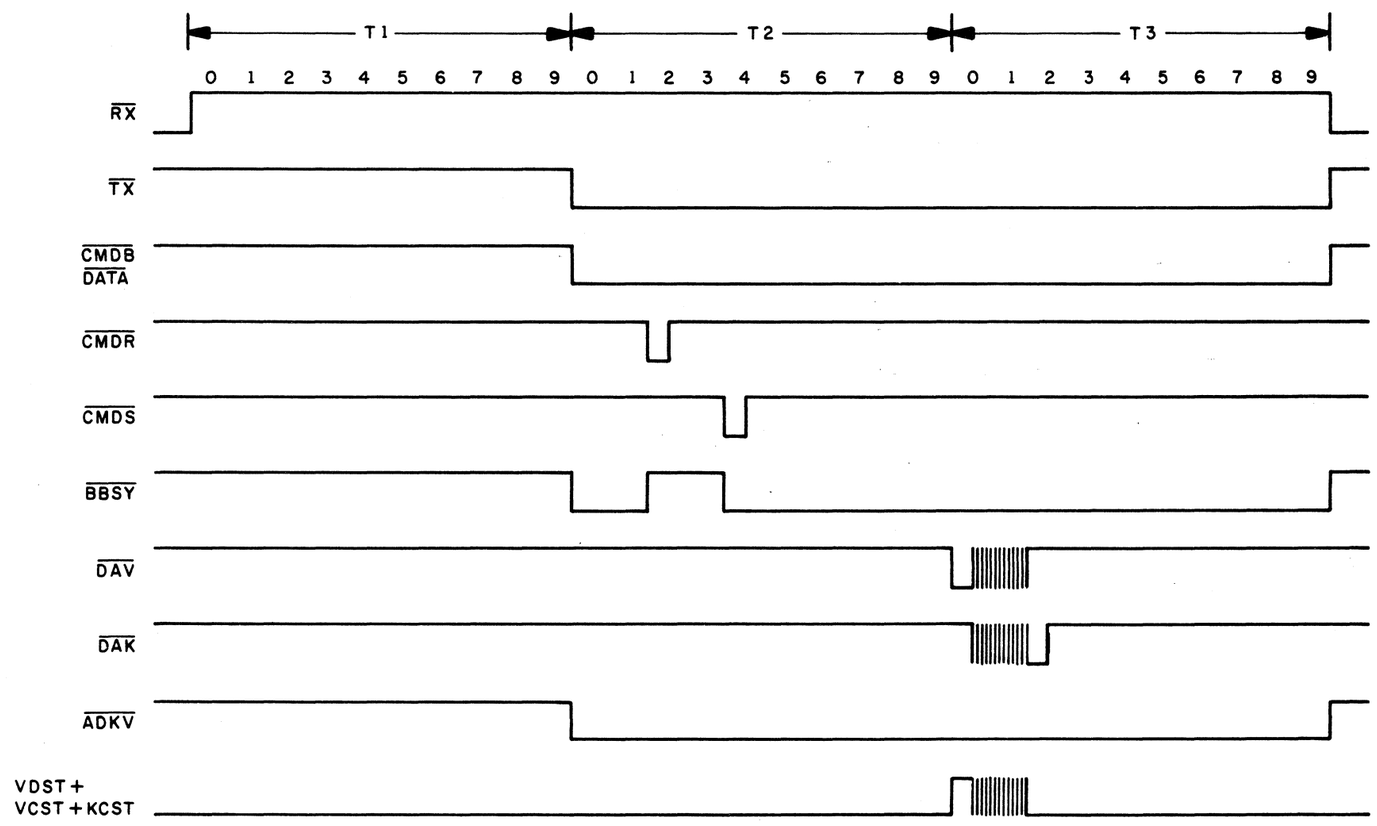


FIGURE 2A-8
12 BD SI TRANSMIT MODE TIMING

NULL + RST RDY (F2-10, sheet 1) is generated when a NULL character (DL00 - DL08 = 177_8) or a RST RDY character (DL00 - DL08 = 377_8) is sent to the VDU. In either case, VDST should not be generated, as $\overline{\text{RST RDY}}$ (C4-6) clears VRDY in the VDU CR, and NULL is used as a filler character and should not be sent to the VDU Data Register. However, if either character is sent, the 12 BD SI pcb must still assert $\overline{\text{DAK}}$. Normally, when NULL is sent to the VDU, VRDY is true to enable gate A2-12 via gates F3-13 and A3-12. If the character is RST RDY character, VRDY is reset; therefore, RST RDY E enables gate A2-12 to assert $\overline{\text{DAK}}$.

RECEIVE MODE

DATA TRANSFER

The Keyboard transfers a word to the DTC 8 when it is on-line and a key is depressed, or when the Keyboard is issued a send status command. Figure 2A-9 illustrates the receive mode timing.

When the Keyboard has a word to transfer, it asserts KRDY · FULL and DAVF (sheet 2) when $\overline{\text{RX}}$ is true. Provided $\overline{\text{TX}}$ is false, gate F5-10 is enabled and the signal TXB · KRDY · FULL is asserted. TXB · KRDY · FULL gates the word onto the 12 BD SI line ($\overline{\text{DL11}}$ - $\overline{\text{DL00}}$) and the parity logic examines DL11 - DL00 to create the parity bit, $\overline{\text{DLP}}$.

TXB · KRDY · FULL also enables gate F5-3, and after a delay of approximately 5 µs, gate F5-4 goes low to assert $\overline{\text{DAV}}$. On receipt of $\overline{\text{DAV}}$, the DTC 8 loads the word into the 12 BD SI line buffer and asserts $\overline{\text{DAK}}$ to acknowledge the transfer. When $\overline{\text{DAK}}$ becomes true, gate A1-13 is enabled and $\overline{\text{DAKD}}$ is asserted when capacitor C3 becomes fully charged. $\overline{\text{DAKD}}$ resets DAVF in the Keyboard, causing $\overline{\text{DAV}}$ to go false. When $\overline{\text{DAV}}$ goes false, the DTC 8 resets $\overline{\text{DAK}}$ and gate A1-13 goes low to assert END OF DATA TRANSFER (EODT) at A1-2. EODT remains true until capacitor C3 discharges and forces A1-3 high. EODT resets KRDY · FULL to end the transfer, and the 12 BD SI line is restored.

LINE DRIVER CONTROL

The line drivers (sheet 2) are enabled by TXB · KRDY · FULL. The drivers for $\overline{\text{DL07}}$ - $\overline{\text{DL00}}$ are controlled by KD07 - KD00 from the Keyboard logic. KD07 - KD00 may represent a key address (data), or the Keyboard status or error status words. Figure 2A-5 illustrates the three different word structures.

The drivers for $\overline{\text{DL11}}$ - $\overline{\text{DL08}}$ are controlled by STATUS (STAT) and KEYBOARD ERROR STROBE (KES). If the Keyboard is transferring the Keyboard status, it asserts STAT to force $\overline{\text{DL11}}$ - $\overline{\text{DL08}}$ true. If the Keyboard is transferring data, STAT and KES are false, and $\overline{\text{DL11}}$ - $\overline{\text{DL08}}$ are therefore false. If the Keyboard is transferring an error word, it asserts KES, forcing $\overline{\text{DL10}}$ true.

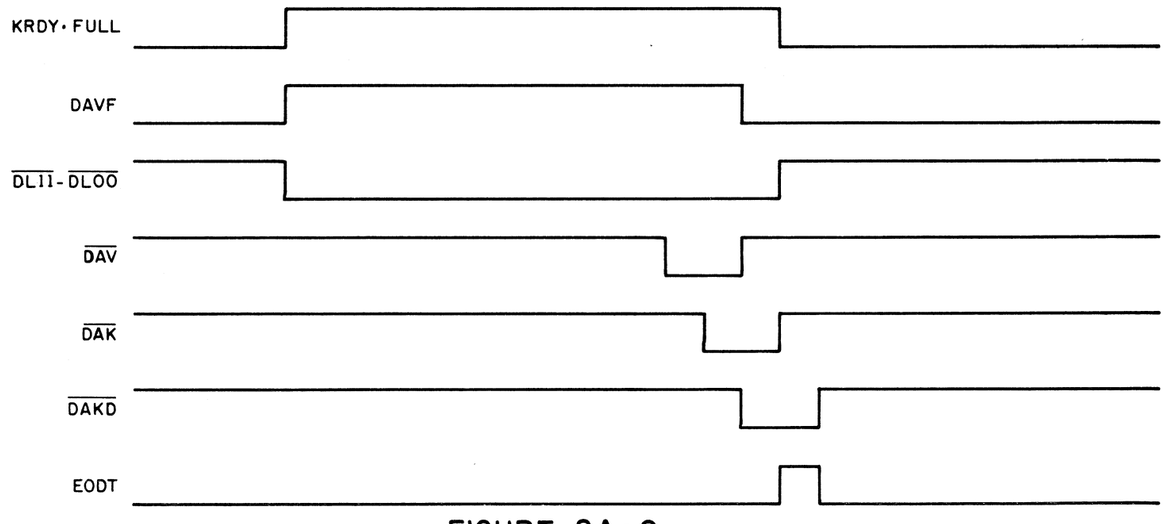
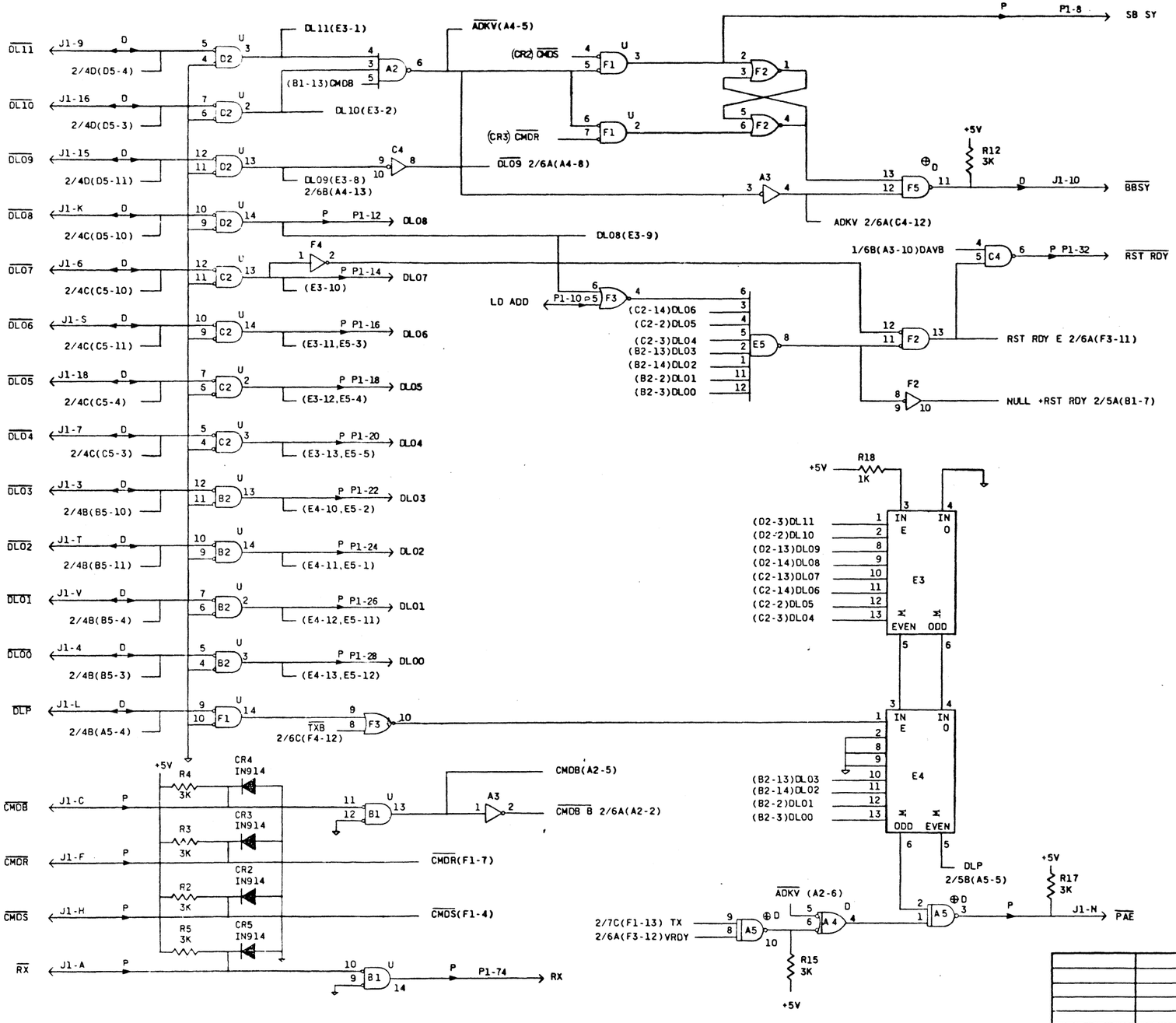


FIGURE 2A-9
12 BD SI RECEIVE MODE TIMING

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	21 OCT 74	DN		



CHIP CHART					
	1	2	3	4	5
F	380A	7402	7402	7404	858
E			74180	74180	7430
D		380A			858
C		380A		7400	858
B	380A	380A			858
A	380A	7410	7404	857	858

NOTE: C3 IS PROVIDED FOR ON PCB AS A RESISTOR PAK, BUT IS NOT USED

IC GND AND POWER TABLE		
+5V	GND	CHIP
14	7	A2,A3,A4,A5,B5,C5,D5
14	7	C4,E3,E4,E5,F2,F3,F4,F5
8	1	B1,B2,C2,D2,F1,A1

MISSING COMPONENTS

C17,C19,C20,C22

LAST COMPONENTS

R20,C26,CR21,Q1

UNLESS OTHERWISE NOTED

All resistors are 1/4w

Spare Gates -A3-8

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00± .01 ANGLES ± 0° 30' .000± .005	DR NORTON 21 OCT 74
			CHK CASSEMAN 21 OCT 74
		MATERIAL	DSGN GMT
			ENGRG GMT
			ORIGINALLY DESIGNED FOR ST
1B133A	ST	SPEC	APPD
NEXT ASSY	USED ON	FINISH	APPROVED
APPLICATION		SPEC	DWG CODE

CONSOLIDATED COMPUTER INC. OTTAWA CANADA

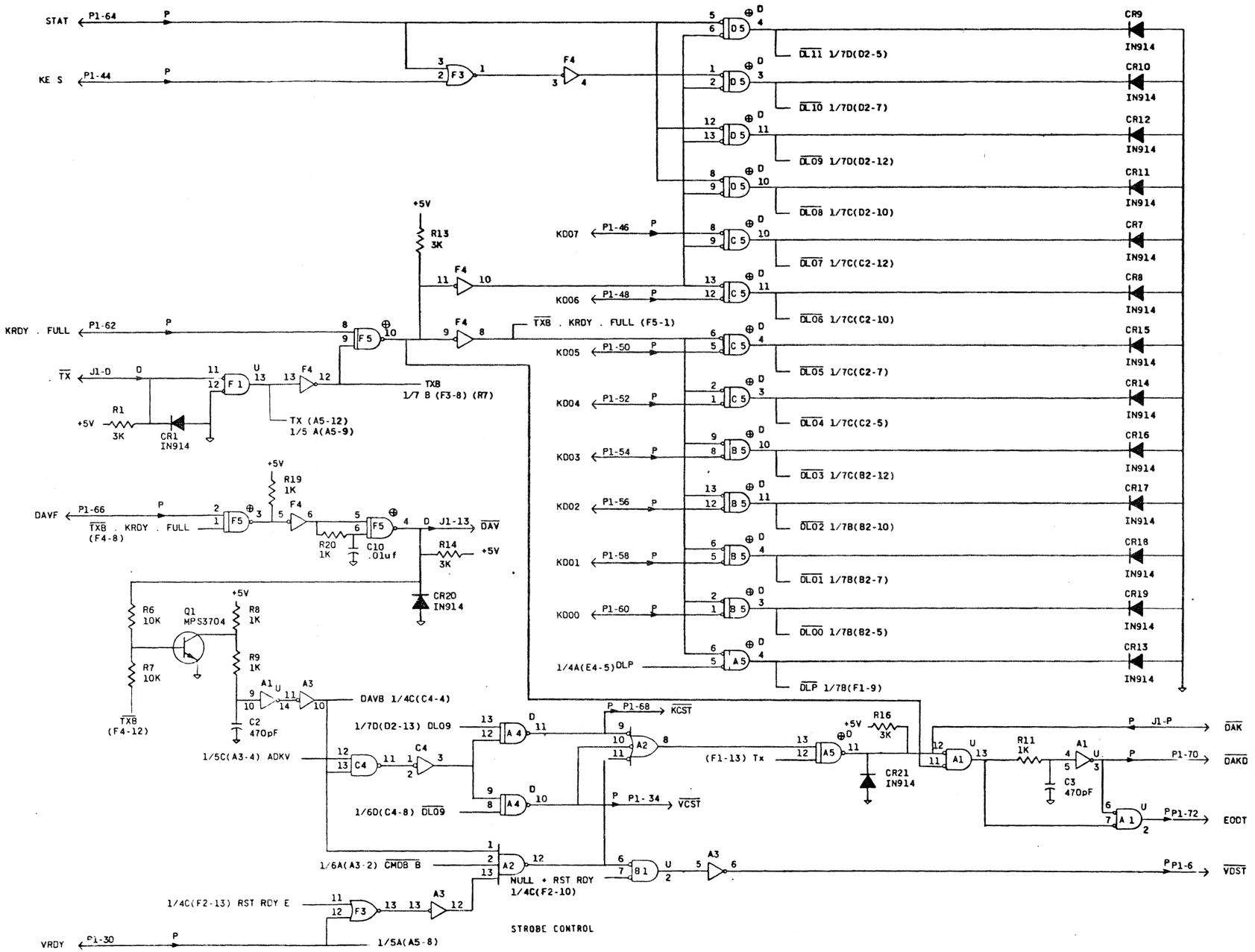
LOGIC DIAGRAM
12 BDSI

SCALE | SHEET 1 OF 2 | D SIZE | DWG NO 13133L

13133L B A

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	[illegible]	DN		

12 BDSI DATA LINE DRIVERS



SCALE	SHEET 2 OF 2	D SIZE	DWG NO. 13133L

L/150 ADAPTER

INTRODUCTION

In a KE 50 system, the Data Terminal communicates with the Terminal Controller via a serial bit interface cable. The cable has two pair of wires, one for bi-directional data transfer, and one to supply the clock pulses for data transfer. Figure 2A-10 illustrates the data flow between the Terminal Controller and the Data Terminal.

When the Terminal Controller transmits a word to the Data Terminal in serial format, the L/150 pcb uses the accompanying clock pulses to load the data into a shift register. When all 16 bits are loaded into the register, the L/150 determines the purpose of the word, which may be either a Keyboard command, a VDU command, or VDU data. Figure 2A-11 illustrates the three word structures for the incoming 16-bit word. The L/150 simulates a 12 BD SI transfer to either the Keyboard or VDU by asserting either $\overline{KCST}$ to load the word into the Keyboard CR, $\overline{VCST}$ to load the word into the VDU CR, or $\overline{VDST}$ to load the word into the VDU Data Register.

Figure 2A-12 illustrates the three receive word structures. When the Keyboard transfers data, error, or status words to the Terminal Controller, it performs the same type of transfer operation as it does for a 12 BD SI interface, except that the word is first stored in the L/150 pcb. The L/150 then generates a transfer request, and the Terminal Controller responds by placing the clock signal on the KC- and KC+ lines. The L/150 then shifts the data, one bit at a time, onto data lines KD+ and KD-, and it is loaded into the Terminal Controller.

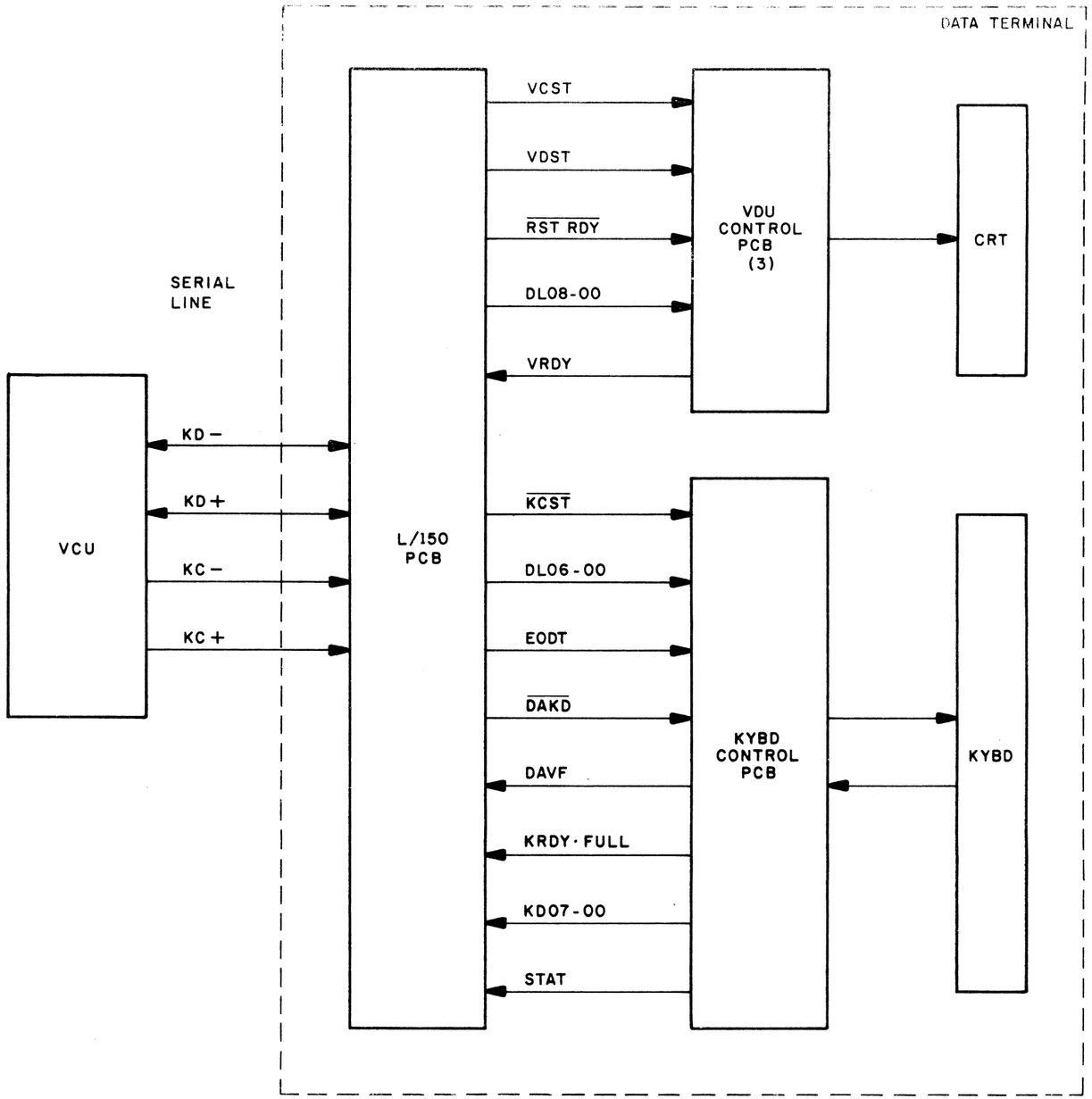
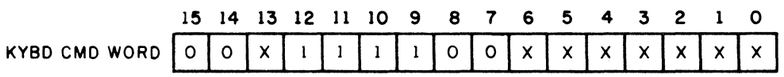
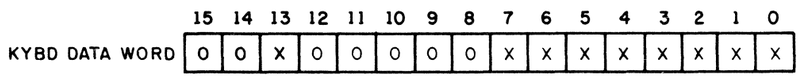
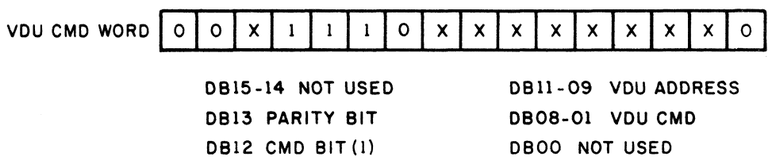
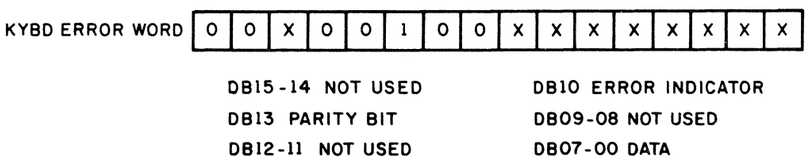


FIGURE 2A-10
L/150 DATA FLOW & CONTROL









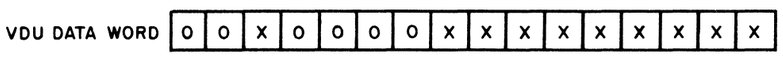


FIGURE 2A-11
L/150 TRANSMIT MODE WORDS

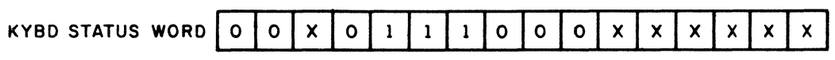


FIGURE 2A-12
L/150 RECEIVE MODE WORDS

DETAILED DESCRIPTION

The KE 50 Terminal Controller transmits 16-bit serial command or data words to the Data Terminal, and receives 16-bit data, status, or error words. Drawing 13366L illustrates the L/150 pcb logic.

TRANSMIT MODE

Figure 2A-13 illustrates the transmit timing. When the Terminal Controller has assembled a word, it begins transmission by generating a series of 17 clock pulses. The leading edge of the first clock pulse inhibits a Receive Request (RX RQST) by setting RS flop C1-3 to disable C2-13 (drawing 13366L, sheet 1).

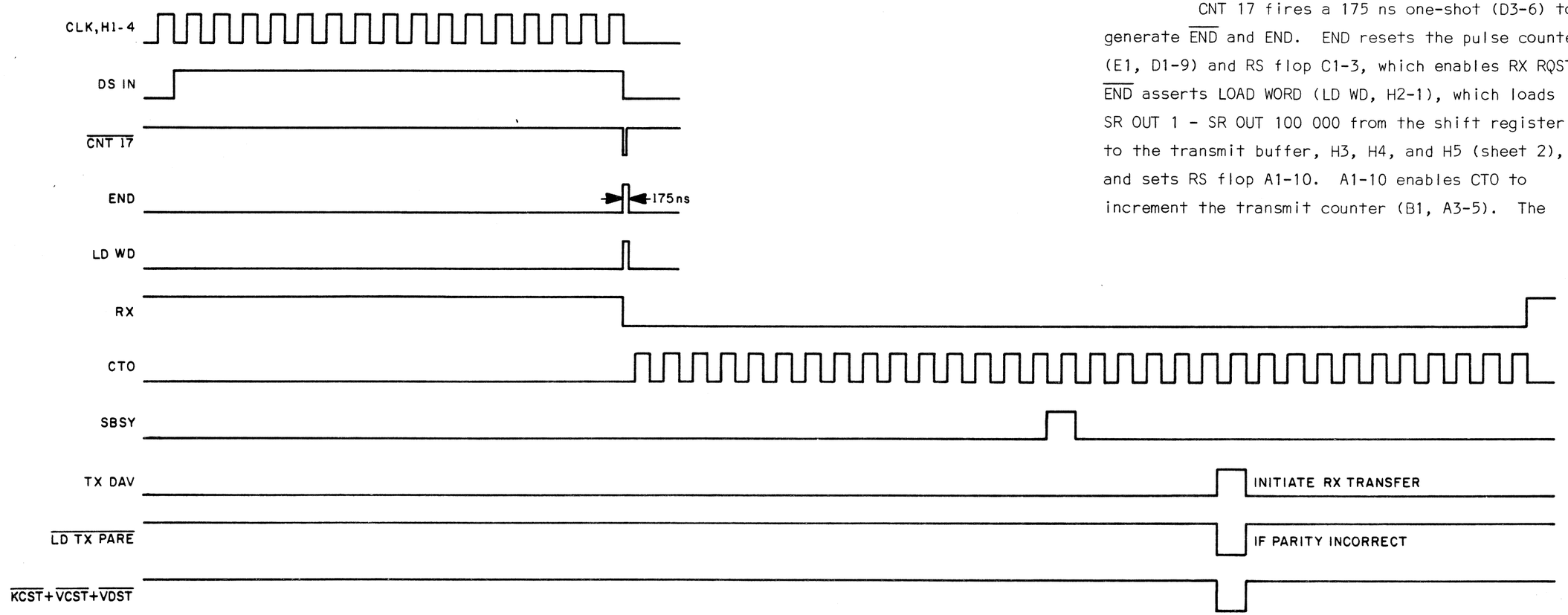
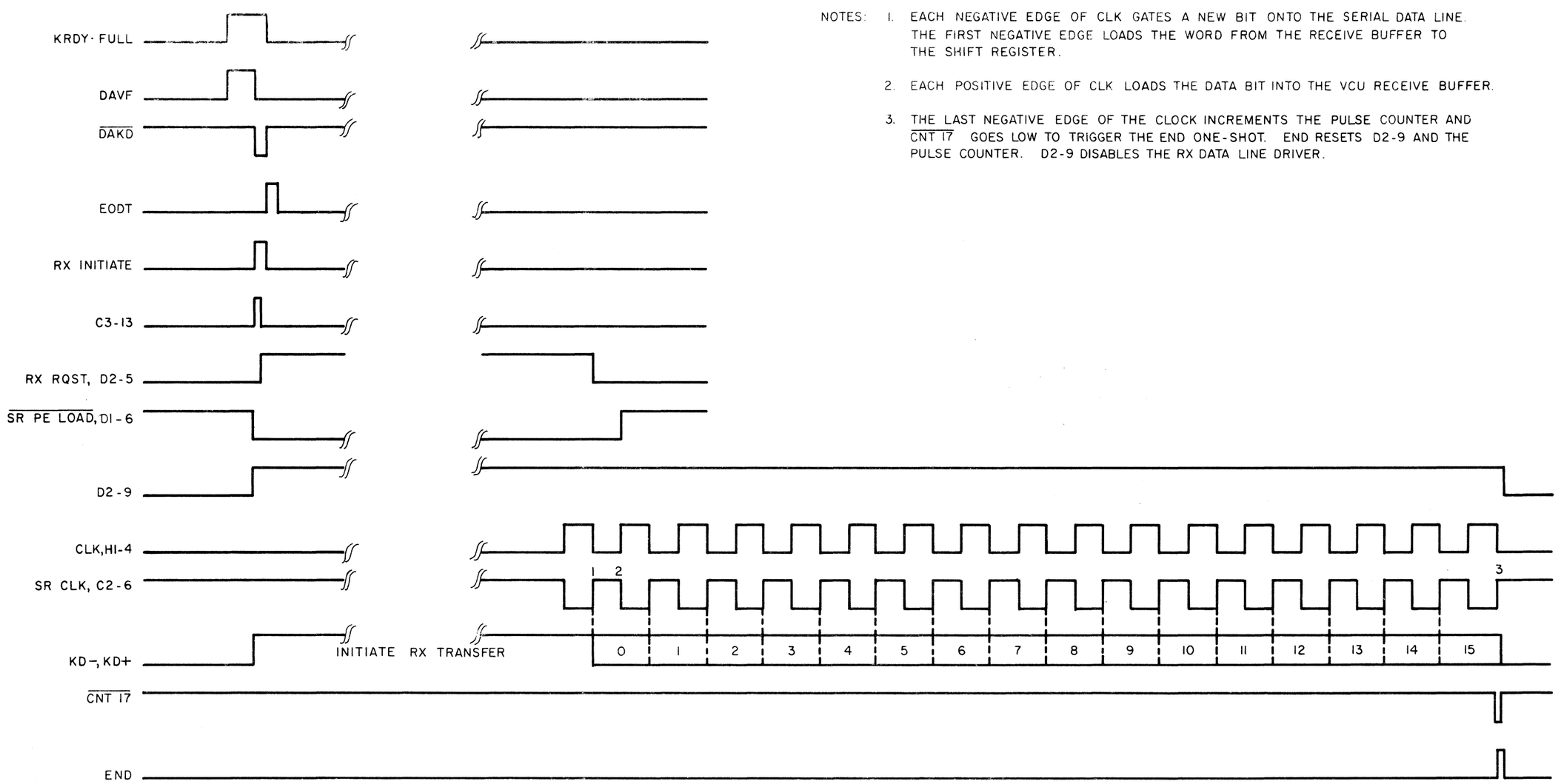


FIGURE 2A-13
L/150 TRANSMIT MODE TIMING

The trailing edge of the first clock pulse gates the least significant bit of the word onto the data line (KD+, KD-), and increments the clock pulse counter (E1, D1-9). The leading edge of the second clock pulse loads the first data bit, DATA SERIAL IN (DS IN), into the 16-bit shift register (F2, F3, F4, F5). This process continues until the leading edge of the 17th clock pulse loads the 16th (final) bit into the shift register, and the trailing edge increments the pulse counter to assert COUNT 17 (CNT 17).

$\overline{\text{CNT 17}}$ fires a 175 ns one-shot (D3-6) to generate $\overline{\text{END}}$ and END. END resets the pulse counter (E1, D1-9) and RS flop C1-3, which enables RX RQST. $\overline{\text{END}}$ asserts LOAD WORD (LD WD, H2-1), which loads SR OUT 1 - SR OUT 100 000 from the shift register to the transmit buffer, H3, H4, and H5 (sheet 2), and sets RS flop A1-10. A1-10 enables CTO to increment the transmit counter (B1, A3-5). The



NOTES:

1. EACH NEGATIVE EDGE OF CLK GATES A NEW BIT ONTO THE SERIAL DATA LINE. THE FIRST NEGATIVE EDGE LOADS THE WORD FROM THE RECEIVE BUFFER TO THE SHIFT REGISTER.
2. EACH POSITIVE EDGE OF CLK LOADS THE DATA BIT INTO THE VCU RECEIVE BUFFER.
3. THE LAST NEGATIVE EDGE OF THE CLOCK INCREMENTS THE PULSE COUNTER AND $\overline{\text{CNT 17}}$ GOES LOW TO TRIGGER THE END ONE-SHOT. END RESETS D2-9 AND THE PULSE COUNTER. D2-9 DISABLES THE RX DATA LINE DRIVER.

FIGURE 2A-14

L/150 RECEIVE MODE TIMING

outputs of this counter are used to generate the strobes to transfer the word to the Keyboard CR, the VDU CR, or the VDU Data Register. Flop A1-10 also forces RX false to prevent further data transfer from the Keyboard.

If CMDB is true (H3-15), the L/150 asserts SBSY (E3-13) during the 16th count time (1, 2, 4, and 8 true; 16 false). SBSY is used to clear CMD REGISTER FULL (CRF) on the VDU-2 pcb. During the 21st count time (1, 16, and 4 true; 2 and 8 false), TX DAV is asserted at B3-10 to enable the strobe logic and the parity logic. If the parity is incorrect ($\overline{\text{TX PARE}}$ low), TX DAV asserts $\overline{\text{LD TX PARE}}$, which asserts RX INITIATE to load TX PARE into the receive buffer (H3, E4, E5) and initiate a receive transfer.

The strobe logic may assert one of three strobes. If CMDB is true, the logic decodes DL11 - DL09. If DL11 - 09 equal 7_8, the logic asserts KCST (C5-6) when TX DAV goes true. If DL11 - 09 equal 6_8, the logic asserts $\overline{\text{VCST}}$ (C5-8). $\overline{\text{KCST}}$ loads SL06 - 00 into the Keyboard CR, and $\overline{\text{VCST}}$ loads DL08 - 01 into the VDU CR. If CMDB is false, the logic asserts $\overline{\text{VDST}}$ (D4-6) to load DL08 - DL00 into the VDU Data Register, provided:

- DL08 - DL00 $\neq 177_8$ (NULL character)
- DL08 - DL00 $\neq 377_8$ (RESET VDU CR)
- LOAD ADDRESS (LD ADD) is false.

If LD ADD is true, 177_8 or 377_8 may be a valid address.

At the end of the count of 32, the logic clears the transmit counter (B1, A3-5) and resets RS flop A1-10, allowing RX to go true, and inhibiting CTO from incrementing the counter.

RECEIVE MODE

Figure 2A-14 illustrates receive mode timing. The L/150 pcb initiates a receive mode transfer when:

- the Keyboard sends a data word
- the Keyboard sends a status word
- the Keyboard sends an error word
- the L/150 detects a parity error during a transmit sequence.

The Keyboard sends a word to the L/150 pcb by asserting KRDY · FULL and DAVF. If $\overline{\text{RX RQST}}$ is false, the logic asserts $\overline{\text{DAKD}}$, which asserts RX INITIATE and resets DAVF in the Keyboard. DAVF goes false to force $\overline{\text{DAKD}}$ false, and B5-3 (sheet 2) asserts EODT for the time capacitor C6 takes to discharge through R22. EODT resets KRDY · FULL in the Keyboard.

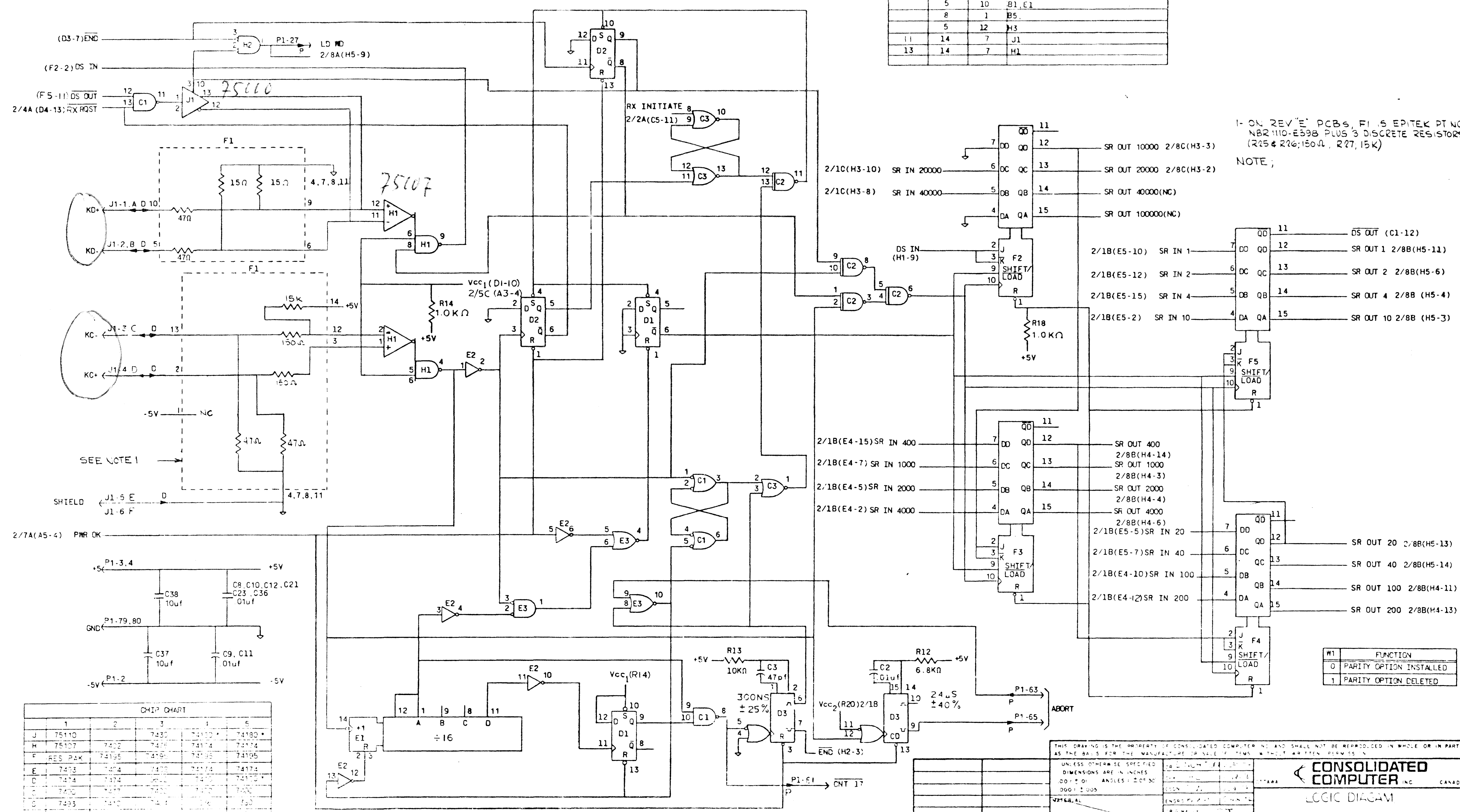
RX INITIATE, whether asserted by $\overline{\text{DAKD}}$ or $\overline{\text{LD TX PARE}}$, loads the receive buffer (H3, E4, E5) and sets the Receive Initiate flop, C3-13 (sheet 1). Provided the L/150 is not in a data transfer sequence (either RX or TX), gate C2-11 goes low to set:

- the RX REQUEST flop (D2-5), which forces a one bit onto the data lines (KD+, KD-) to initiate a receive transfer
- the shift register parallel load flop (D1-5)
- flop D1-9 to enable the clock pulse to the shift register via C2-8 and C2-6.

The Terminal Controller acknowledges the receive transfer request by supplying the clock pulses to shift the word onto the data lines, KD+ and KD-.

The first negative edge of CLK (H1-4) loads the word from the receive buffer (H3, E4, E5) to the shift register, as D1-6 has been set by RX INITIATE. D1-6 enables the shift register to be parallel-loaded. The first negative edge also resets RX RQST (D2-5), which enables the output of the shift register, $\overline{\text{DS OUT}}$, to control the data line driver via C1-11, and the first data bit is put on the data line. On the next (second) positive edge, the Terminal Controller loads the bit into the receive buffer. This edge also resets the parallel load flop, D1-5. Each of the next fifteen negative edges of CLK shifts a new bit onto the data line, and also increments the clock counter (E1, D1-9). On the 17th (final) negative edge $\overline{\text{CNT 17}}$ is asserted at C1-8 to trigger one-shot D3-6, which generates END and $\overline{\text{END}}$. END resets the clock counter via E3-10, and the trailing edge of $\overline{\text{END}}$ resets flop D2-9 to disable gate C2-8, ending the receive mode transfer.

NOTE: Once RX RQST (D2-5) is reset, another word can be stored in the receive buffer.



I.C. POWER, GROUND TABLE			
-5V	+5V	GROUND	CHIP DESIGNATION
	14	7	A1, A2, A3, A4, A5, B2, B3, B4 C1, C2, C3, C4, C5, D1, D2, D4 D5, E2, E3, J3, J4, J5, H2
1	14	4,7,8,11	F1
	16	8	D3, E4, E5, F2, F3, F4, F5, H4, H5
	5	10	B1, E1
	8	1	B5
	5	12	H3
11	14	7	J1
13	14	7	H1

CHIP CHART					
	1	2	3	4	5
J	75110		7430	74180 *	74180 *
H	75107	7402	7475	74174	74174
F	RES PAK	74195	74195	74195	74195
E	7493	7404	7402	74174	74174
D	7474	7474	[illegible]	7410	74180 *
C	7400	7427	7402	7400	7400
B	7493	7410	[illegible]	[illegible]	[illegible]
A	7402	[illegible]	7474	7400	7404

* IC REMOVED WHEN PARITY OPTION DELETED

W1	FUNCTION
0	PARITY OPTION INSTALLED
1	PARITY OPTION DELETED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00 = ±.01 ANGLES = ±0° 30' .000 = ±.005

CONSOLIDATED COMPUTER INC. OTTAWA CANADA

LOGIC DIAGAM

L150 ADAPTER

ORIGINALLY DESIGNED FOR ST

SIZE D DWG NO 13366L

The address counter is incremented by the scan clock (ϕ1), and its output is gated onto KD00 - KD06, provided STATUS is false. KD00 - KD06 address a keyswitch by enabling a decoder driver (KD03 - KD06) and a multiplexor (KD00 - KD02). The outputs of the multiplexor, KEYD and $\overline{\text{KEYD}}$, reflect the state of the addressed key. If the key is operated (depressed) the ground from the decoder line is shunted to the multiplexor input line and $\overline{\text{KEYD}}$ and KEYD are asserted. KD00 - KD06 also address a release code ROM. If a key has been assigned a release code, the ROM asserts $\overline{\text{RELEASE}}$ when that key is addressed.

$\overline{\text{KEYD}}$ is stored in the key state detector, which compares it to its state for the previous scan of this key. If a change is detected, CHANGE is asserted when ϕ2 is true. CHANGE halts the SCAN clock, enables the strobe clock, and sets WINDOW. If $\overline{\text{KEYD}}$ remains stable (no key bounce) while WINDOW is true, CHANGE remains true to keep the strobe clock running; otherwise, CHANGE goes false and the control logic returns to scanning the key switches. WINDOW is reset (if there is no key bounce) when the halt counter is incremented to 3. When the halt counter is incremented to 4, the logic generates $\overline{\text{KSTB}}$ if KDF or $\overline{\text{RELEASE}}$ is true. KDF is true if the change was caused by a depressed key; $\overline{\text{RELEASE}}$ is true if the change was caused by a released key that has a release code.

$\overline{\text{KSTB}}$ sets FULL if RX is true. RX is false only when a word is being transferred to the Data Terminal. If the keyboard is on-line (KRDY) and $\overline{\text{DAKD}}$ is false, the control logic asserts DAVF and KRDY · FULL to initiate a word transfer. The interface pcb performs the transfer, and asserts $\overline{\text{DAKD}}$ and EODT when the transfer is completed. $\overline{\text{DAKD}}$ resets DAVF, and EODT resets FULL, KRDY · FULL, and CHANGE. When CHANGE goes false, the strobe clock is disabled, the scan clock is enabled, and the control logic continues scanning the keyswitches.

ERROR DETECTION

The error logic can detect two error conditions, a double keystroke error, and a data transfer error. A double keystroke error occurs when $\overline{\text{KSTB}}$ is asserted within 8.5 ms of the trailing edge of the last $\overline{\text{KSTB}}$. A data transfer error occurs when KSTB is asserted to initiate a word transfer, but EODT is not asserted before the halt counter is incremented to an 8 count.

When either error is detected, KES is set. KES sets the ERROR and the TONE 2 bits in the CR, causing the error lamp to flash and an 830 Hz tone to sound. The tone may be interrupted if the FLASH bit is set in the CR.

KES also forces $\overline{\text{DL10}}$ true when the next word is transferred to the Terminal Controller or DTC 8, and is reset by the next EODT.

STATUS TRANSFER

When STATUS (STAT) is set in the CR, the keyboard sends a status word to the DTC 8 or Terminal Controller. Figure 2A-16 defines the significance of each bit of the status word.

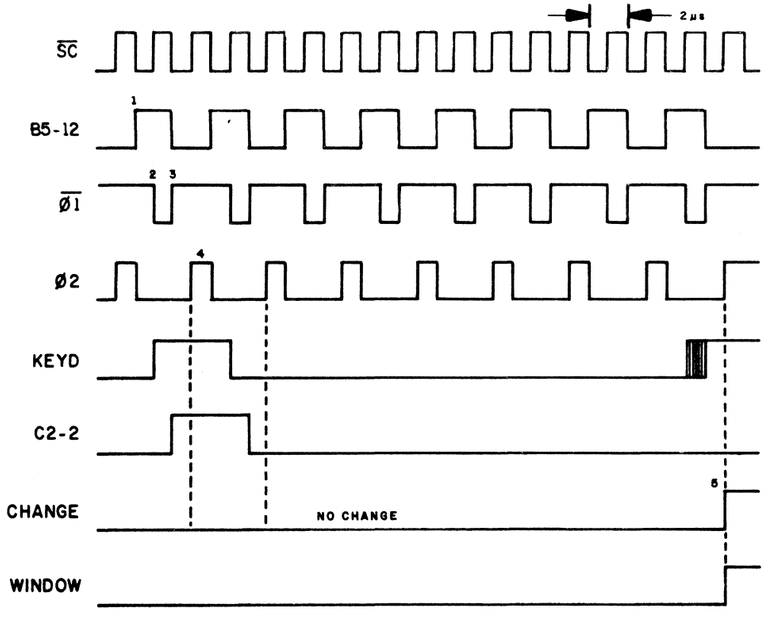
$\overline{\text{STAT}}$ inhibits the outputs of the address counter from KD00 - KD05, and STAT forces KD06 and KD07 false. $\overline{\text{STAT}}$ also asserts ENABLE STATUS (ENSTAT) and FULL. ENSTAT gates the keyboard status onto KD00 - KD05, and FULL asserts KRDY · FULL and DAVF to initiate a word transfer. When the transfer is completed, the interface pcb asserts EODT to reset STATUS and end the status transfer.

DETAILED DESCRIPTION

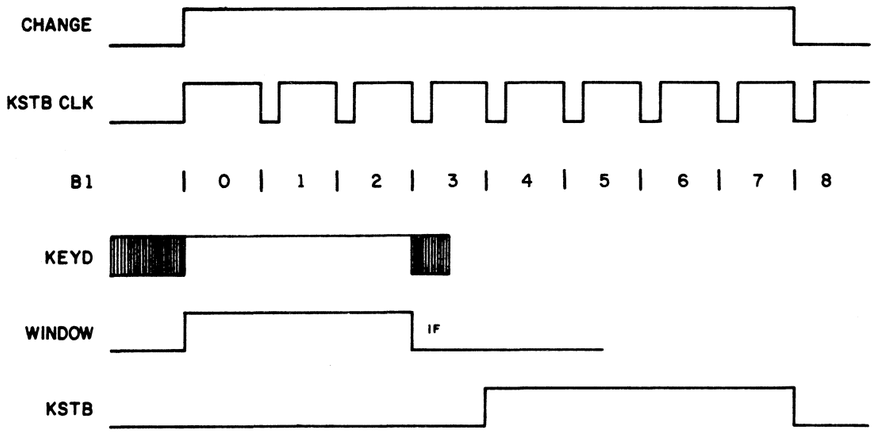
KEYBOARD SCANNING

Drawing 13131L illustrates the logic that scans the keyswitch matrix. Drawing 13132L illustrates the Keyboard pcb logic. The scanning sequence is controlled by a scan clock (D5, B5-12, D1-3, B3-10, sheet 2) which generates two pulses, $\overline{\phi 1}$ (D1-3) and ϕ2 (B3-10). Figure 2A-17 illustrates the scan clock timing.

The leading edge of $\overline{\phi 1}$ increments the address counter (B4, B5), whose outputs control KD00 - KD06 when STATUS is false. KD00 - KD06 address one of the keyswitches on the Keyboard pcb, and the trailing edge of $\overline{\phi 1}$ clocks the key state ($\overline{\text{KEYD}}$) into flop D4-5. The trailing edge of $\overline{\phi 1}$ also clocks C2, a 128-bit shift register, to load the state of the previously addressed key (D4-9) into the shift register. Thus, the output of the shift register (C2-2) represents state of the key when last addressed, and KDF (D4-5) represents its present state.

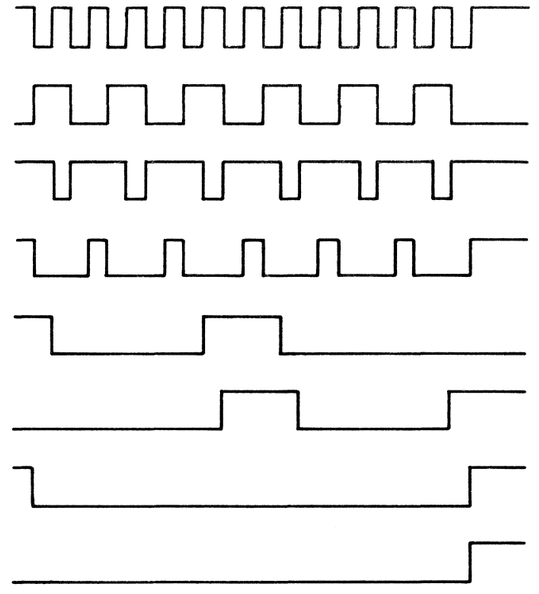


KEYBOARD SCAN KEY DEPRESSED

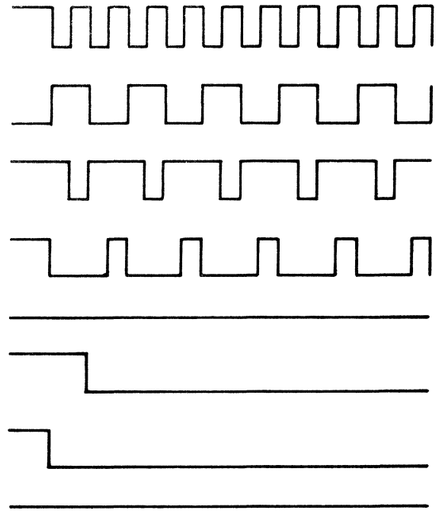


WINDOW TIMING DEPRESSED KEY

HALT CYCLE KEY DEPRESSED (FIGURE 2A-18)



HALT CYCLE KEY RELEASED (FIGURE 2A-19)



NOTES:
1. POSITIVE EDGE OF B5-12 CLOCKS STATE OF KDF INTO D4-9
2. LEADING EDGE OF Ø1 INCREMENTS KEYBOARD ADDRESS (KD0 - KD6)
3. TRAILING EDGE OF Ø1 CLOCKS STATE OF KEYD INTO KDF
   TRAILING EDGE OF Ø1 CLOCKS STATE OF D4-9 INTO SHIFT REGISTER
4. Ø2 TESTS OLD KEYD STATE-SHIFT REGISTER OUTPUT (C2-2) TO NEW STATE (KDF)-
   IF DIFFERENT, CHANGE IS ASSERTED TO HALT SCANNER CLOCK (SC)
   ($\overline{SC}$, $\overline{Ø1}$, Ø2 REMAIN HIGH, B5-12 REMAINS LOW).
5. CHANGE SETS WINDOW TO ALLOW BOUNCE TEST. IF THE STATUS OF KEYD CHANGES WHILE WINDOW IS TRUE, KDF IS RESET (CHANGE SET BECAUSE KEY DEPRESSED) OR SET (CHANGE SET BECAUSE KEY RELEASED) AND STATE OF KDF EQUALS STATE OF C2-2 TO FORCE CHANGE FALSE AND ENABLE THE SCANNER.

FIGURE 2A-17
SCAN CLOCK TIMING

If the states represented by KDF and the shift register output are the same, the scan clock continues to cycle and the next positive edge of B5-12 clocks KDF into flop D4-9. D4-9 is clocked into the shift register by the next trailing edge of $\overline{\phi 1}$.

NOTE: D4-9 is needed because the shift register is a CMOS IC that requires a longer set-up time.

If the states are different, neither gate D3-1 nor gate D3-4 become low, and gate E2-11 is enabled at pin 13. When $\phi 2$ goes high, E2-11 asserts CHANGE to begin a scan HALT cycle by:

- halting the SCAN clock at $\phi 2$
- setting WINDOW (A2-5)
- enabling the keystroke clock (A6).

During a halt cycle, the control logic determines whether the change of state was caused by a bouncing key, a depressed key, or a released key.

WINDOW (A2-6) enables gates B2-8 and B2-12, which check for key bounce. If the key bounces, $\overline{\text{KEYD}}$ changes state, and either gate B2-8 or B2-12 goes low. If the logic detects what seems to be a released key (KDF false, C2-2 true), but the key bounces, gate B2-8 sets KDF. If the logic detects a depressed key (KDF true, C2-2 false), but the key bounces, gate B2-12 resets KDF. Thus, KDF is restored to the same state as the shift register output (C2-2) when a bouncing key is detected. Where KDF and the shift register output are the same, either gate D3-1 or D3-4 goes low to reset CHANGE (D2-2), which disables the key strobe clock (A6), and enables the scan clock to end the halt cycle. The next positive edge of B5-12 clocks the state of KDF into flop D4-9, and the flop output is clocked into the shift register by the next trailing edge of $\overline{\phi 1}$. Thus the key state stored (KDF) is the same as that stored during the previous scan of this key.

If the key does not bounce while WINDOW is true, the key strobe clock increments the halt counter B1 to a count of 3 and resets WINDOW. When the counter is incremented to 4, B1-8 enables gates C5-13 and E2-8. These gates, with C1-3 and A4-12, determine:

- whether a key strobe should be generated
- whether the halt cycle should be ended.

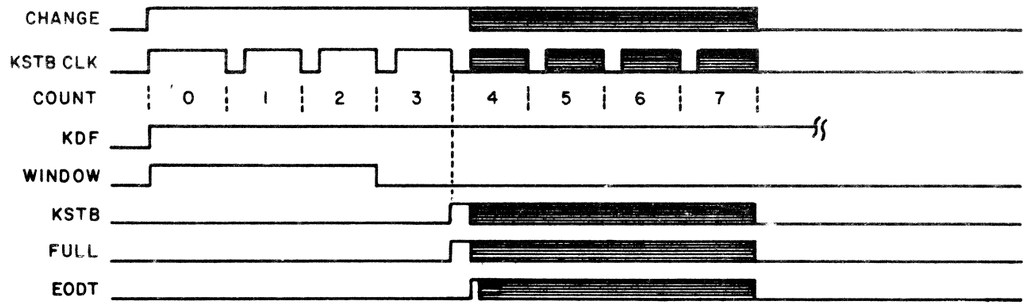
A keystrobe ($\overline{\text{KSTB}}$) is asserted by gate E2-8 if the halt occurred because a key that has a release code was released ($\overline{\text{RELEASED}}$ true) or a key was depressed (KDF true). $\overline{\text{KSTB}}$ initiates a word transfer and KD00 - KD07 are used on the interface pcb to form a word for transfer to the DTC 8 or Terminal Controller. KD00 - KD06 represent the key address, and KD07 (B3-4) is asserted only when the transfer is the result of a key that has a release code being released.

$\overline{\text{KSTB}}$ is not asserted if both $\overline{\text{RELEASE}}$ and KDF are false, which occurs when a key is released but has no release code. In this case, gate C5-13 goes low, forcing CHANGE false to end the halt cycle. Figure 2A-18 illustrates the timing when a depressed key is detected, and Figure 2A-19 illustrates the timing when a released key is detected.

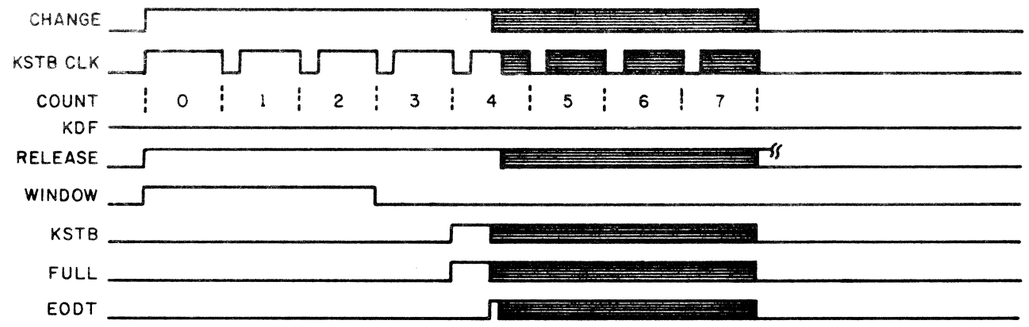
The keyboard transfers a word to the DTC 8 or Terminal Controller when $\overline{\text{KSTB}}$ is asserted or STATUS is set in the CR.

$\overline{\text{KSTB}}$ asserts FULL (D3-10) by setting flop A3-5, provided RX (B2-6, pin 3 and $\overline{\text{STATUS}}$ (B2-6, pin 4) are false. FULL asserts DAVF (A5-6) if $\overline{\text{DAKD}}$ is false, and asserts KRDY · FULL (B3-13, sheet 1) if the keyboard is on-line (KRDY true at F5-9).

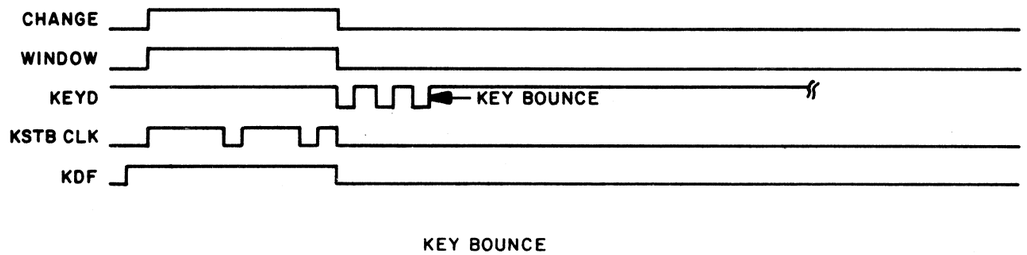
DAVF and KRDY · FULL cause the interface pcb to initiate a word transfer and send the data, KD00 - KD07, to the Terminal Controller or DTC 8. On completion of the transfer, the interface pcb asserts $\overline{\text{DAKD}}$ which resets DAVF. When DAVF goes false, the interface pcb resets DAKD and generates an END OF DATA TRANSFER (EODT) pulse. EODT resets flop A3-5, resetting FULL and KRDY · FULL. EODT also forces gate C5-10 low, which resets CHANGE (D2-2) and ends the halt cycle.



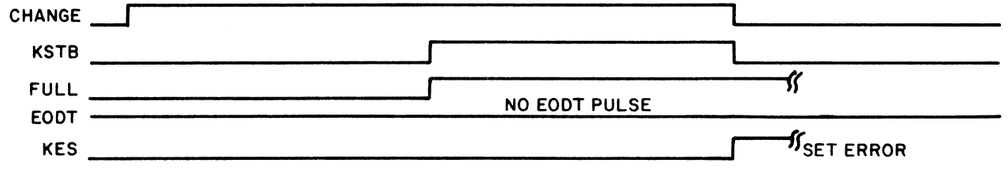
DATA TRANSFER



DATA TRANSFER

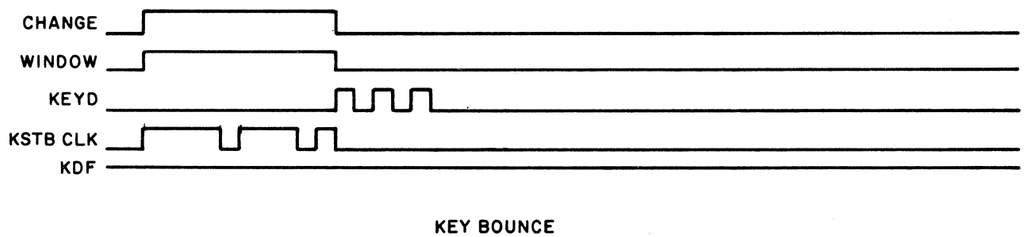


KEY BOUNCE

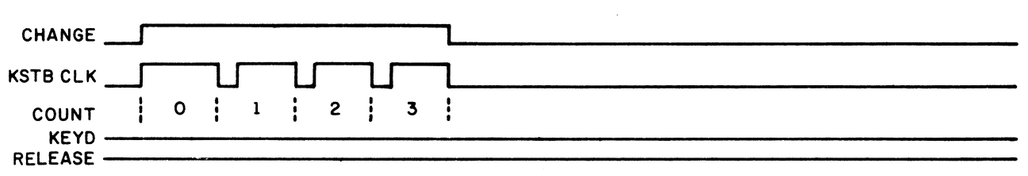


DATA TRANSFER ERROR

FIGURE 2A-18
DEPRESS HALT TIMING



KEY BOUNCE



NO RELEASE CODE

FIGURE 2A-19
RELEASE HALT TIMING

When the program examines the status of the keyboard, it sends a command word to the keyboard that sets KRDY (F5-9, sheet 1) and STATUS (E4-5). $\overline{\text{STAT}}$ inhibits the output of the key address counter (B4, B5, sheet 2) to KD00 - 05, and STAT forces KD06 (B3-1) and KD07 (B3-4) false. Thus, while the keyboard is transferring a status word, the scanning logic cannot address the keyswitch matrix.

STAT also asserts ENSTAT (D2-8) and FULL (D3-10). ENSTAT enables a six-bit keyboard status code onto KD00 - KD05. FULL asserts DAVF and KRDY · FULL to initiate a data transfer. On completion of the transfer, the Interface pcb asserts $\overline{\text{DAKD}}$ and then EODT. EODT resets STATUS (E4-5, sheet 1) to end the transfer, and the scanning logic is able to address the keyboard. The six keyboard code bits are hardwired on the Keyboard pcb at the time of its manufacture. This code defines the type of keyboard layout. Appendix 2A-1 illustrates the different keyboard layouts and their status code.

ERROR DETECTION

The error logic can detect two errors: a data transfer error, and a double keystroke error. A data transfer error is detected when $\overline{\text{KSTB}}$ is asserted to initiate a transfer and EODT is not asserted before the halt counter reaches a count of 8. At this time, $\overline{\text{KSTB}}$ goes false and sets KES (A2-9, sheet 2) as A3-5 is not reset by EODT.

A double keystroke error is detected when a $\overline{\text{KSTB}}$ pulse is asserted with 8.5 ms of the previous $\overline{\text{KSTB}}$. The trailing edge of $\overline{\text{KSTB}}$ triggers the 8.5 ms one-shot A1-9. If KSTB is asserted before the one-shot times out, KES is set.

KES sets TONE 2 (F5-5, sheet 1) and ERROR (E5-5) in the CR. TONE 2 enables the tone oscillator to generate an 830 Hz tone, and ERROR causes the ERROR lamp to flash.

TONE CONTROL

The tone oscillator (F1) generates a 430 Hz tone when the scanning logic detects a depressed key. KDF and $\overline{\text{KSTB}}$ (E2-3) trigger a 50 ms one-shot (F2-3). While the one-shot is active, it enables E1-2 to gate resistor R3 into the oscillator circuit, and a 430 Hz TONE (F3-4) is generated if KRDY is true.

The oscillator is also controlled by two bits of the Command Register, TONE 1 (E5-9) and TONE 2 (F5-5). These bits control gates E3-10 and E3-13. When E3-13 is high, it enables E1-3 to gate R5 into the oscillator circuit. Gate E3-10, when high, enables E1-9 to gate R2 into the oscillator circuit. Under the control of TONE 1 and TONE 2, the oscillator can generate three tones:

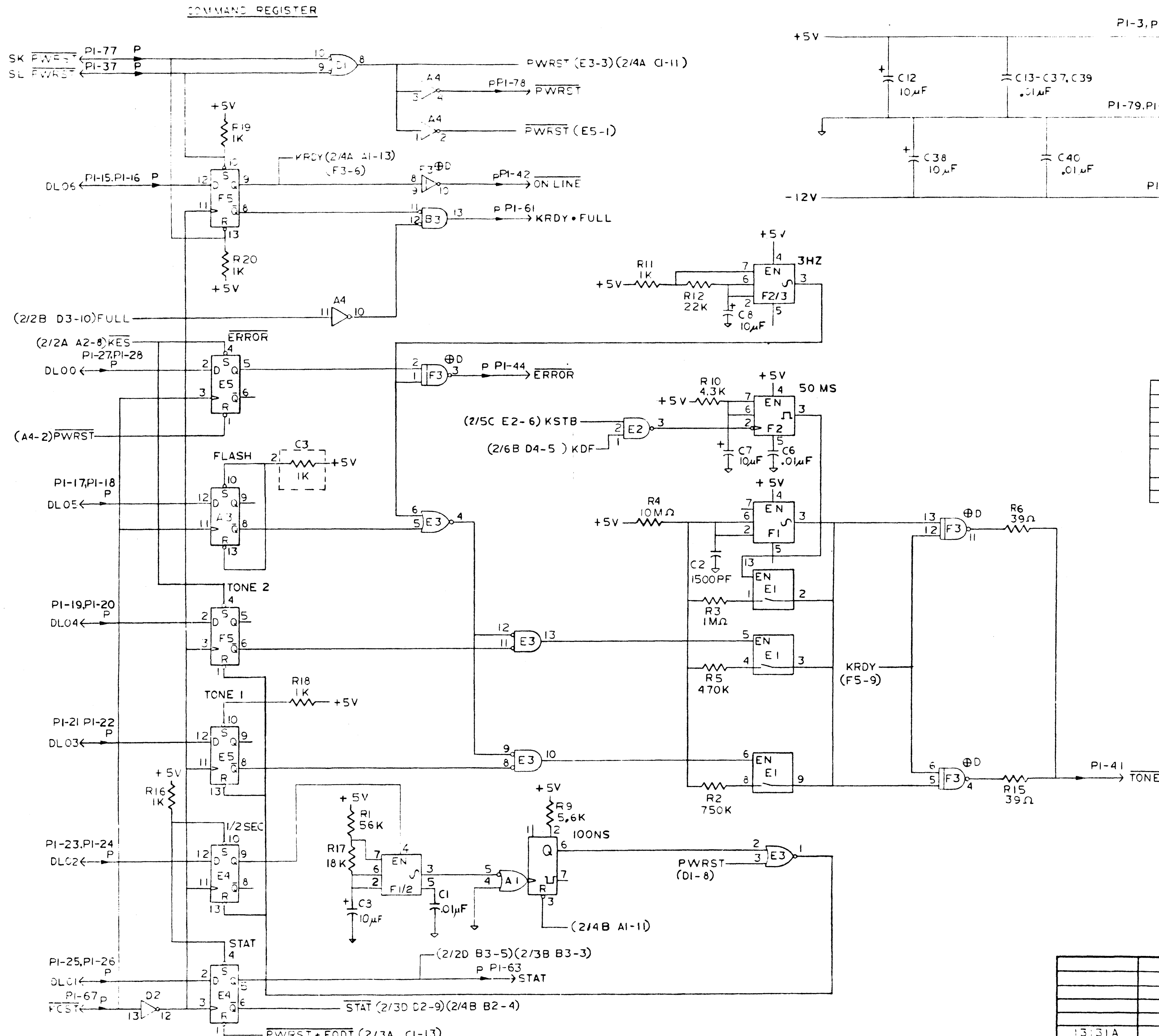
- TONE 1 = 550 Hz (R2)
- TONE 2 = 830 Hz (R5)
- TONE 3 = 1320 Hz (R5, R2).

The tone may be continuous, interrupted, or of $\frac{1}{2}$-second duration. If FLASH (A3-9) and $\frac{1}{2}$ SECOND (E4-9) are reset, the tone is continuous. If FLASH is set, the tone is interrupted by the output of the flash oscillator (F2/3). If $\frac{1}{2}$ SECOND is set, a $\frac{1}{2}$-second one-shot is triggered. When the one-shot times out, it fires a 100 ns one-shot (A1-6), which resets $\frac{1}{2}$ SECOND, TONE 1, and TONE 2.

INDICATORS

The keyboard has three indicator lamps: POWER ON, ON-LINE, and ERROR.

The POWER ON lamp (yellow) is lit when the Data Terminal is powered-up; that is, when Vcc and ground are applied to CR3 on the Keyboard pcb. The ON-LINE lamp (green) is lit when KRDY (F5-9) is set in the Keyboard CR. KRDY asserts $\overline{\text{ON LINE}}$, which grounds CR4. When the ERROR bit is set in the CR, gate F3-3 asserts $\overline{\text{ERROR}}$, whenever the output of the flash oscillator (F2/3) is high, to cause the error lamp to flash.



CHIP CHART						
	1	2	3	4	5	6
F	555 555	555 555	555		7474	
E	14016	7400	7432	7474	7474	
D	7400	7404	7401	7474	836	
C	380	1012	RES PAK	7401	7401	
B	7493	7410	7432	7493	7493	
A	5602	7474	7474	7404	7400	555

I.C. POWER AND GROUND TABLE			
-12V	+5V	GND	CHIP
	8	1	C1, F1, F1/2, F2, F2/3
	16	8	A1
	5	10	B1, F4, B5
	14	7	A2, A3, A4, A5, B2, B3, C4, C5, D1, D2, D3, D4, D5, E1, E2, E3, E4, E5, F3, F5
7	5&6	3	C2

MISSING COMPONENTS
R21 R24
C5

LAST COMPONENT
R25
C40

UNLESS OTHERWISE NOTED
ALL RESISTORS ARE 1/4W

SPARE GATES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
.00 = ±.01 ANGLES = ±0° 30'
.000 = ±.005

13131A | ST
NEXT ASSY | USED ON
APPLICATION

ORIGINALLY DESIGNED FOR ST

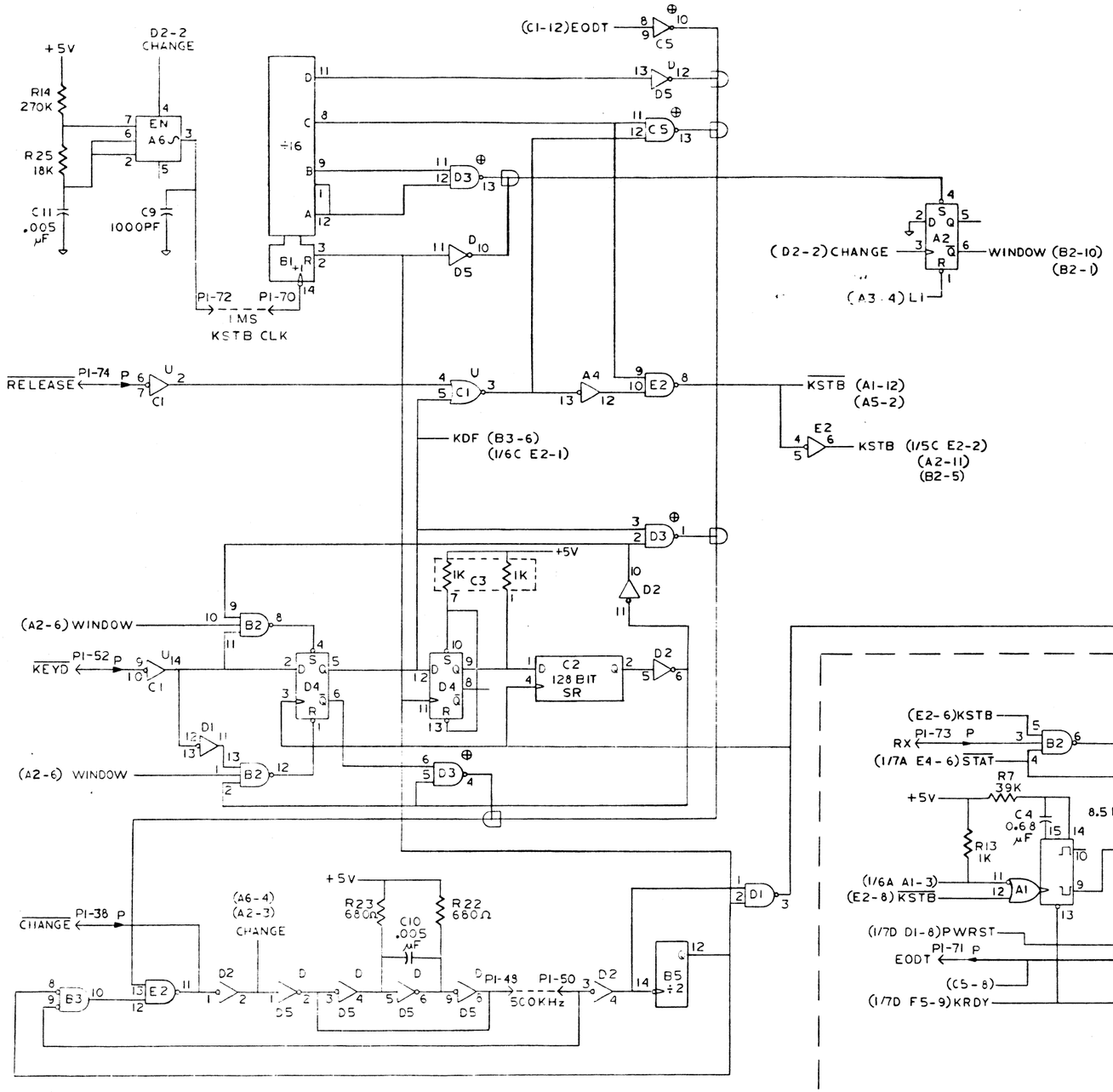
CONSOLIDATED COMPUTER INC.
OTTAWA CANADA

LOGIC DIAGRAM
KEYBOARD CONTROL

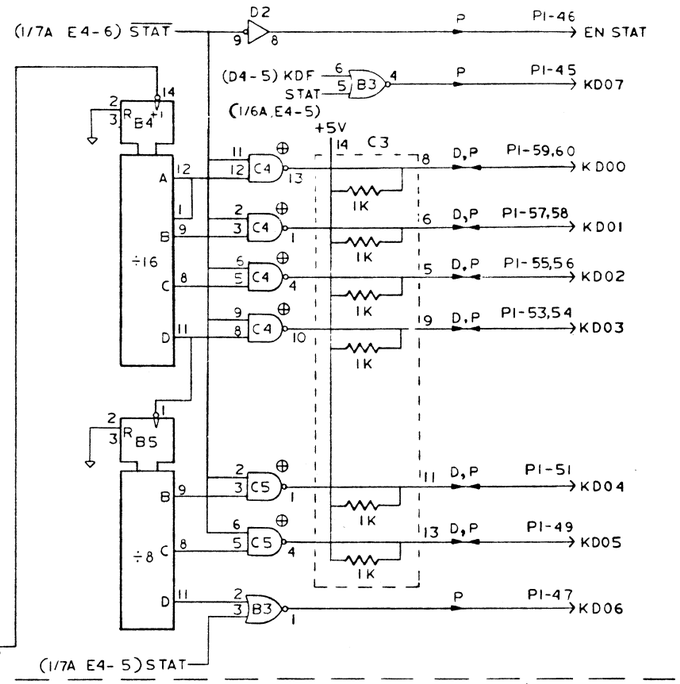
SHEET 1 OF 2 — SIZE D — DWG NO. 1313IL

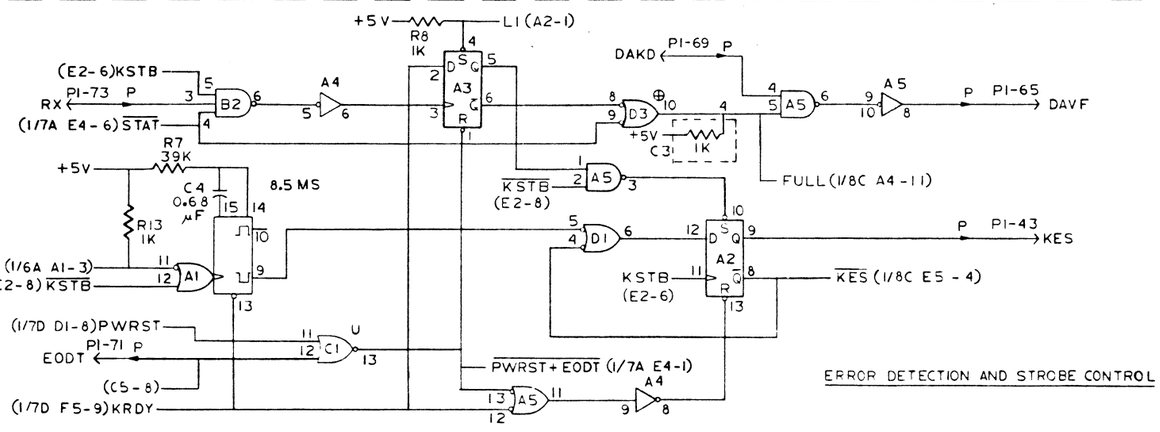
REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		SEE SH 1				
B		SEE SH 1				
C		SEE SHEET 1				

KEYBOARD SCANNER



KEYBOARD SCAN CLOCK

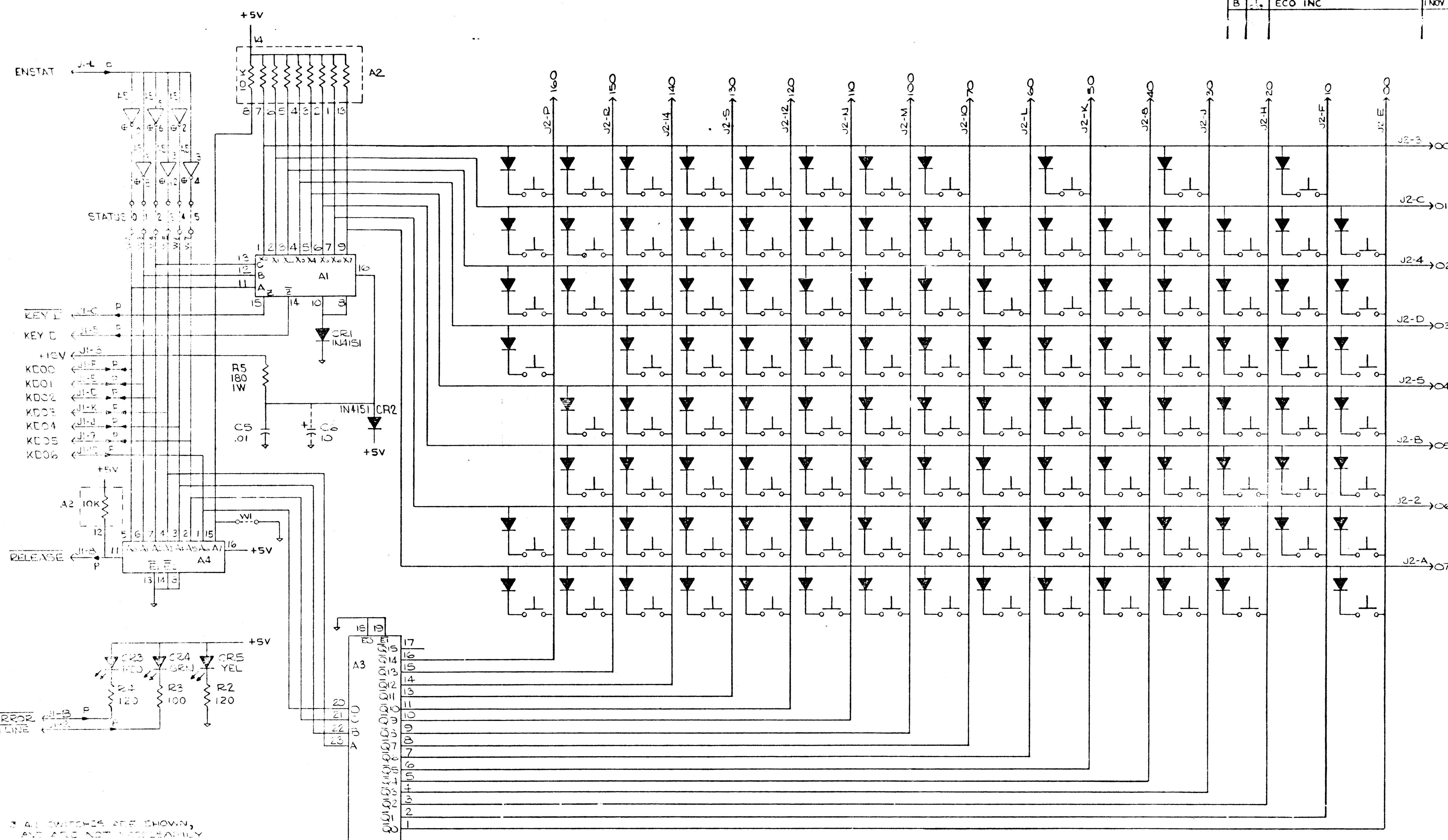




ERROR DETECTION AND STROBE CONTROL

SCALE	SIZE	DWG NO.
SHEET 2 OF 2	D	13131L

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PROD RELEASE				
B	1	ECO INC	1 NOV 79	MM		

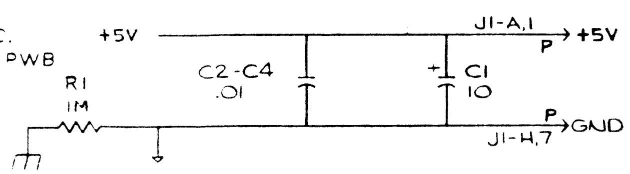


3. ALL SWITCHES ARE SHOWN, AND ARE NOT NECESSARILY INSTALLED IN ALL POSITIONS

2. C6 (10μF) IS PROVISIONAL AND IS NOT USED. MOUNTING HAS BEEN PROVIDED ON THE PWB

1. UNLESS OTHERWISE SPECIFIED:
RESISTORS – OHMS 1/4 WATT
CAPACITORS – μF

NOTES:



CHIP CHART

	1	2	3	4	5
A	8312	RES PAK	8311	HM1-7611-5	7405

13132A	ST
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00 ± .01 ANGLES ± 0° 30' .000 ± .005

MATERIAL

SPEC

FINISH

SPEC

APPROVED

DWG CODE

OTTAWA CONSOLIDATED COMPUTER INC. CANADA

LOGIC DIAGRAM KEYBOARD MARK II DATA TERMINAL

SCALE — SHEET 1 OF 1 SIZE D DWG NO 13132L

VIDEO DISPLAY UNIT

INTRODUCTION

The VDU comprises two elements: the control logic, and the video monitor. Figure 2A-20 is a block diagram of the VDU.

The control logic refreshes the display on the video screen using three signals:

- HORIZONTAL SYNC (HS), which controls the horizontal sweep of the CRT electron gun
- VERTICAL SYNC (VS), which controls the vertical sweep of the gun
- VIDEO DRIVE (VD), which turns the electron gun on or off to illuminate or darken the CRT display surface.

HS and VS are derivatives of the control timing and VD is derived from the timing and the display control logic. The display control logic stores enough information to control the display of the complete line (40 characters), and under timing control, it asserts VD to trace the required display on the screen display surface. When a complete line is displayed, a new line of information is loaded from the display storage.

The display storage logic can store enough information to display 12 lines (480 characters). The software can update this information by issuing commands and sending data. The storage control logic with the Command and Data Registers, controls the update process.

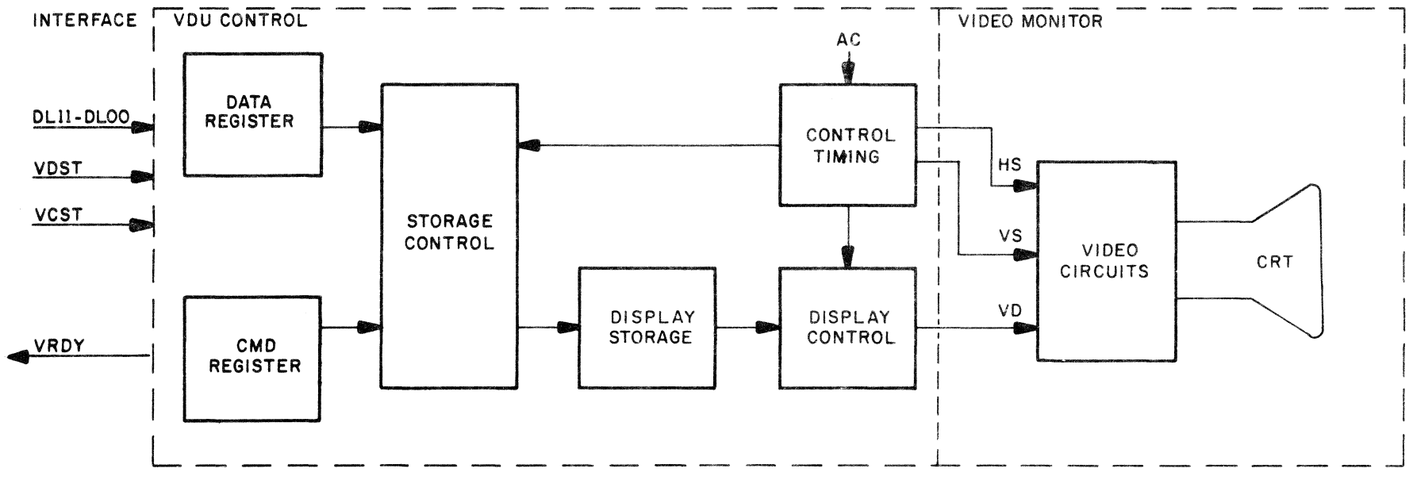


FIGURE 2A-20
VDU BLOCK DIAGRAM

VIDEO MONITOR

The VDU uses a Ball Brothers Video Monitor. Their Instruction Manual, CRT Data Displays, IM1003, explains monitor operation.

CONTROL TIMING

This timing controls the refresh sequence of the VDU. Figure 2A-21 illustrates the control timing and its relationship to the display area on the VDU screen.

The master clock generates BIT TIME CLOCK (BTC). BTC is a 50 ns pulse with a period of 102 ns. The period of BTC is controlled by a phase comparator which compares the timing to the ac line frequency. The circuit automatically adjusts BTC if it becomes too long or too short. As the Data Terminal can use 50 Hz or 60 Hz, the phase comparator circuit must be adjusted to the line frequency (R7, VDU-3, pcb 13136). The purpose of this circuit is to eliminate any swimming effect.

BTC clocks the bit time generator, which produces $\overline{\text{BIT TIMES}}$ ($\overline{\text{BT}}$) $\overline{0}$ - $\overline{\text{BT9}}$. The trailing edge of $\overline{\text{BT9}}$ clocks the character width time generator to produce CHARACTER WIDTH TIMES (CWT1, CWT2, CWT4, CWT8, CWT10, CWT20, and CWT30).

VD is disabled during CWT0 to CWT4 and CWT45 to CWT60. CWT0 to CWT4 provide a 5-character width space between the left edge of the screen and the left margin of the display area. CWT45 to CWT49 provide an identical spacing on the right of the screen. HS is asserted at CWT50 to enable the flyback action of the horizontal sweep. CWT50 - CWT60 allow the beam time to swing back to the

left edge of the screen. HS is synchronized to ≃ 16 kHz by an astable multivibrator circuit to prevent damage to the video monitor.

One ROW TIME (RT) comprises 60 CWT. The RT generator is clocked by the trailing edge of CWT30 (60th CWT), and produces sixteen row times, $\overline{RT0}$ - $\overline{RT15}$.

One CHARACTER LINE TIME comprises 16 row times. The leading edge of RT15 clocks the CLT generator to produce CLT1, CLT2, CLT4, CLT8, and CLT16. The VDU displays one line of 40 characters during each CLT. At the end of the refresh cycle (CLT16, 60 Hz, or CLT19, 50 Hz), the control times assert VS to enable the vertical flyback action. At the end of CLT16 or CLT19, $\overline{\text{LAST LINE RESET}}$ ($\overline{LLR}$) is generated to reset the CLT generator and CWT10, CWT20, and CWT30 of the CWT generator.

NOTE: The duration of VS depends on the line frequency used. If the source is 60 Hz ac, the vertical sweep is ≃ 16.6 ms. If the source is 50 Hz, the vertical sweep is 20 ms, slower than that of the 60 Hz source; therefore, to keep VS in sync with the line period, VS must be generated at a later time, CLT19.

During this time, the control logic can trace 16 character lines (CLT0 - CLT15). The 17th CLT (CLT16) allows time for the vertical fly back action.

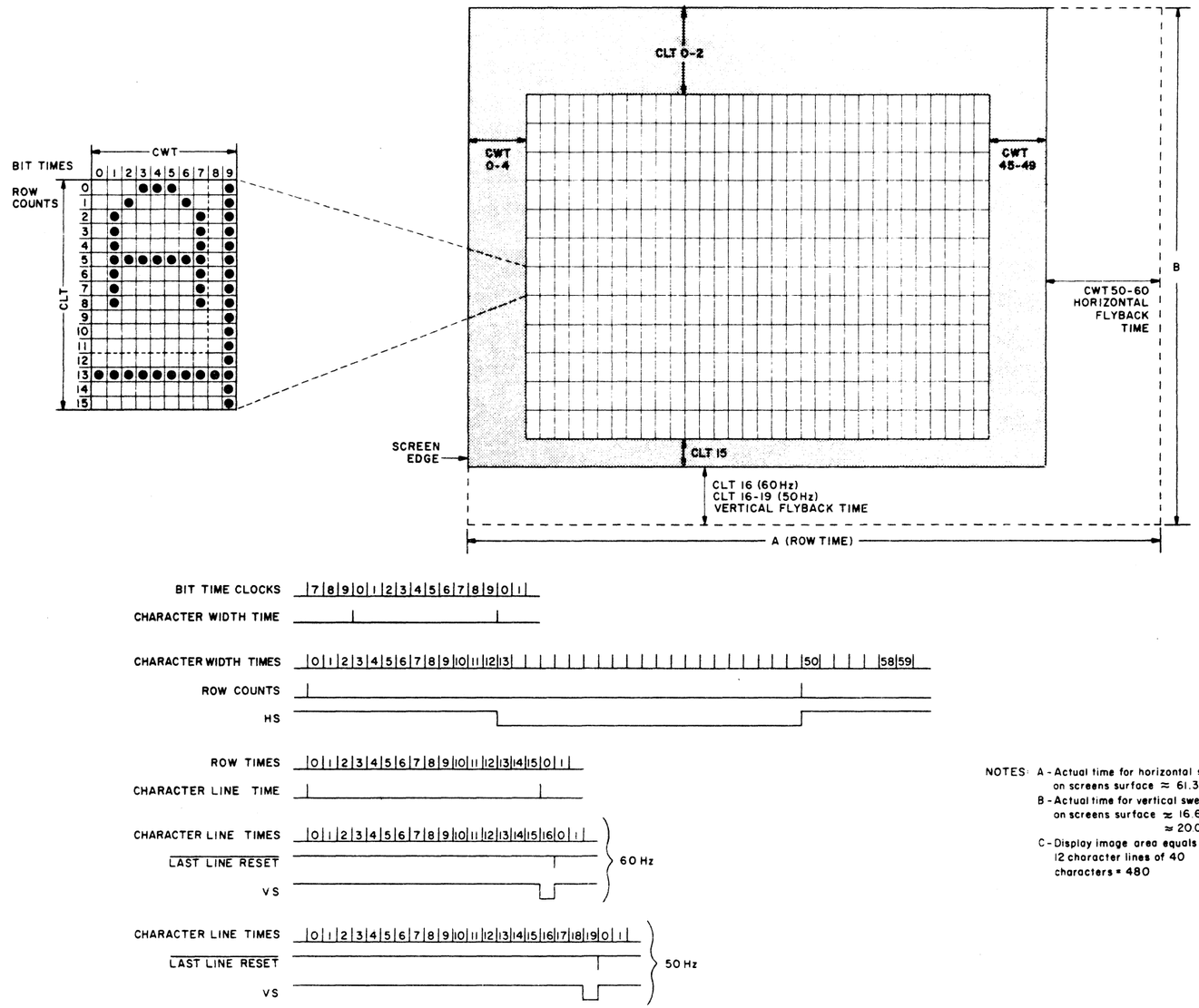


FIGURE 2A-21
VDU TIMING PULSES

VD is only enabled between CLT3 and CLT14, the 12 character display lines. CLT0 to CLT2 provide a space between the top of the screen and the first display line. CLT15 (60 Hz) or CLT15 to CLT18 (50 Hz) provides a space at the bottom of the screen. CLT16 (60 Hz) or CLT19 (50 Hz) allows time for the vertical fly back action.

DISPLAY FORMAT

The display area on the screen is bounded by the 6th and 45th CWT (CWT5 - CWT44) and by the 4th and 15th CLT (CLT3 - CLT14) to create a display area of 12 lines of 40 characters each (480 characters).

Each character is displayed in a 10 x 16 dot matrix on the screen (Figure 2A-21). A character, a cursor, and a delineator can be displayed within this matrix. The character is displayed within an 8 x 12 matrix (BT0 - BT7 x RT0 - RT11). The cursor is displayed in the 14th row (CLT13) and the delineator is displayed in the 10th column (BT9 of RT0 - RT15). Appendix 2A-2 illustrates the display of each character.

VIDEO DRIVE

The control logic asserts VD to illuminate an area on the screen. VD is controlled by the character generation logic and control timing. As the electron gun swings horizontally, the beam is turned on and off to trace the desired image on the screen. To trace a complete character line (40 characters), 16 horizontal sweeps are required. Figure 2A-22 is a block diagram of the logic that controls the electron gun.

The Main Shift Register (MSR) is a 9 x 512-bit register that stores all the data to be displayed on the screen. Seven bits control the character display (8 x 10 matrix), one controls the cursor display (row 14 of the 10 x 16 matrix), and one controls the delineator display (column 10 of the 10 x 16 matrix). Any location within the MSR can be updated under program control.

The Line Shift Register (LSR) is a 9 x 40-bit register that stores enough data to display one character line (40 characters). Forty characters are transferred from the MSR to the LSR during $\overline{RT15}$ of each character line time. Thus, the LSR must be loaded 12 times during a refresh cycle, once for each display line.

When RT15 is true, it disables the recirculation (internal) of the LSR, and enables the output of the MSR to be loaded into the LSR when $\overline{\text{LSR CLOCK}}$ ($\overline{LSRC}$) goes true. $\overline{LSRC}$ is asserted during BT1 - BT4 (≃408 ns) when CWT4/44 is true (CWT4/44 is true from the beginning of CWT4 to the beginning of CWT44). Thus $\overline{LSRC}$ is asserted 40 times during $\overline{RT15}$ to load 40 characters from the MSR.

As the data originates in the MSR, the MSR must also be shifted 40 times. $\overline{LSRC}$ asserts $\overline{\text{MAIN SHIFT REGISTER CLOCK}}$ ($\overline{MSRC}$) when RT13 and CLT3/15 are true. However, $\overline{MSRC}$ lags $\overline{LSRC}$ by 100 ns, enabling $\overline{LSRC}$ to load the LSR before the MSR is shift-loaded. $\overline{MSRC}$ normally loads the MSR

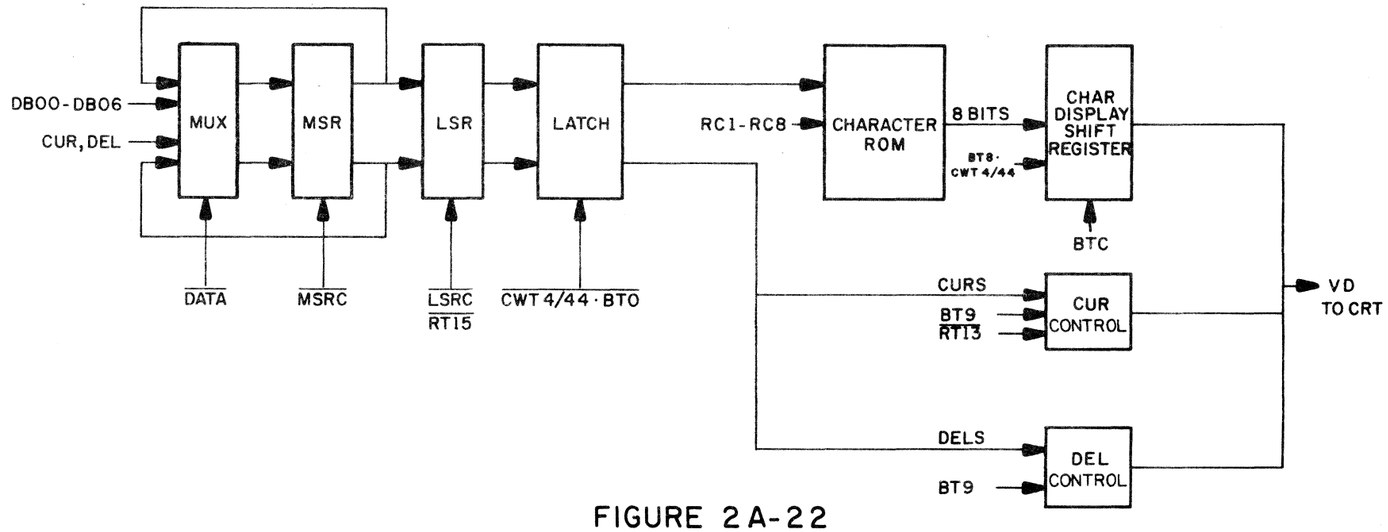


FIGURE 2A-22
VIDEO DRIVE CONTROL

output (DB6R - DB0R) back into the MSR to recirculate the whole display field. However, input to the MSR is controlled by a multiplexor, which selects under program control as the input source, the MSR output, or the VDU Data Register. The latter is the source when the program issues a command to the VDU to update the MSR, and transfers data to the Data Register (refer to COMMAND EXECUTION).

During $\overline{RT0}$ - $\overline{RT14}$ ($\overline{RT15}$ false), the LSR is allowed to recirculate, as its content controls the display of one character line (16 horizontal sweeps). LSR control of the display pattern during one character line time is described in Table 2A-3, in chronological order.

The cycle described in Table 3 repeats itself for each row time RT0 - RT13. As the row count increments, a different ROM location is addressed. After the 12th ROM time, the ROM and CSR are disabled. However, the delineator flop still controls VD at BT9 of these rows. During the 14th row time ($\overline{RT13}$), the output of the cursor control flop controls VD. If the flop is set, VD is enabled during BT0 - BT9 of the character width time to trace cursor line.

The LSR is not recirculated during RT15 as it is being loaded with new data from the MSR. Thus, the data that was recirculated during RT0 - RT14 is clocked into the LSR latch for the last time. At the next RT0, the new data in the LSR controls the display pattern for the next character line.

The MSR is shifted 40 times during RT15 of each character line time CLT3 - CLT14, for a total of 480 shifts. However, as the MSR contains 512 locations, the MSR update control logic must shift the MSR 32 times more to bring it back into position for the next refresh cycle of the screen.

During RT0 - RT14 of every character line time, the MSR update logic asserts $\overline{MSRC}$ 1536 times to recirculate the MSR three complete times. Recirculation is provided so that new data can be loaded into the MSR as fast as the VDU receives it from the DTC 8 or VCU (2 k words/second maximum). Each time the MSR is shifted, the MSR Address Register is incremented. When the MSR address matches the address in the VDU Address Register, the new data is loaded from the VDU Data Register (character codes) or the VDU Command Register (cursor, delineator), depending upon the command issued. Normally the MSR is loaded from its own output.

Data is transferred from the MSR to the LSR during CLT3 to CLT14 only. Therefore, during CLT15, the MSR update logic asserts $\overline{MSRC}$ 1568 times instead of the normal 1536 to bring the MSR back to its starting location (0) for the next refresh cycle.

TABLE 2A-3

DISPLAY PATTERN CONTROL

CHARACTER WIDTH TIME	BIT TIME	OPERATION
CWT4	BT0	The LSR output is loaded into the LSR latch. The upper seven bits, with the Row Counter outputs (RC1, RC2, RC4, RC8), address the character ROM.
	BT1 to BT4	$\overline{LSRC}$ is asserted to shift-load the LSR (recirculate).
	BT8	By this time, the content of the addressed ROM location is at the input of the Character Shift Register (CSR), and BT8 loads the data (8 bits) into the shift register.
	BT9	The trailing edge of BT9 loads the cursor and delineator bits from the LSR into the cursor and delineator control flops.
		NOTE: At this time all data to be displayed during CWT5 is stored. CWT5 is the first character to be displayed.
CWT5	BT0	1. New data is loaded from the LSR to the LSR Latch and the ROM is addressed. 2. The first bit is shifted out of the CSR. If the bit is a one, VD is asserted and the screen is illuminated.
	BT1 to BT4	1. $\overline{LSRC}$ is asserted to shift-load the LSR. 2. The next four bits of the CSR are shifted out to control VD.
	BT5 BT6 BT7	The last three bits of the CSR are shifted to control VD.
	BT9	If the delineator control flop is set, the delineator bit is lit for this CWT.
CWT6 CWT43		The same process as for CWT5 occurs.
CWT44	BT0 to BT7	The eight bits are shifted out of the CSR to control VD for the first 8 bit times.
	BT9	If the delineator flop is set, the delineator bit for the this CWT and row is lit.

COMMAND INITIATION

INTRODUCTION

The program issues commands to the VDU to update the information stored in the MSR. The Command Initiation sequence occurs in three stages.

Firstly, the program sends a command word to the VDU, which is loaded into the Command Register. This first command word initiates a Load Address operation in the VDU, enabling the VDU to load the next data word into the VDU Address Register.

Secondly, the program sends a data word to the VDU. The VDU accepts the word and loads it from the VDU Data Register (DR) into the Address Register (AR). This address defines a location within the MSR that is to be updated. The AR may be incremented by the VDU after the update, provided the command so specifies. This allows multiple updates, to the end of a character line, or of the whole display, by issuing a single command.

Lastly, the program sends another command word to the VDU, to determine how the VDU is to update the MSR. The AR content specifies the location in the MSR at which the update sequence is to begin.

Table 2A-4 defines the function of each bit in the CR. Table 2A-5 lists all the legal command words.

TABLE 2A-4

VDU COMMAND REGISTER

BIT	INPUT	MNEMONIC	FUNCTION
01	DL01	EOL	When set, END OF LINE inhibits the increment of the AR. It allows the VDU to update information in the VDU to the end of the character line which contains the address.
02	DL02	CUR	When CURSOR is set, the VDU inserts a cursor bit into the MSR location addressed by the AR.
03	DL03	DEL	When DELINEATOR is set, the VDU inserts a delineator bit into the MSR location addressed by the AR.
04	DL04	INC	When INCREMENT is set, the VDU increments the AR after the addressed location is updated. INC, with EOL, enables the VDU to update locations in the MSR to the end of the character line which contains the loaded address. INC, with ALL, allows the VDU to update all locations in the MSR. If INC is reset, the VDU only updates the MSR location addressed by the AR.
05	DL05	DATA	When DATA is set, the VDU loads the data, as it is received from the DTC 8, into the MSR location addressed by the AR.
06	DL06	ALL	When ALL is set, the VDU updates or clears all locations in the MSR.
07	DL07	SET	When SET is true, the VDU updates the location in the MSR addressed by the AR. When SET is false, the VDU clears the MSR location addressed by the AR.
08	DL08	VRDY	VDU READY must be set before the interface pcb can assert $\overline{\text{VDST}}$ to load data words into the Data Register.

TABLE 2A-5

VDU COMMANDS

CODE	COMMAND
600	LOAD ADDRESS preconditions the control logic so that it will load the next data word received into the Address Register. If more than one data word is sent, the last represents the address. The AR stores a 9-bit address, allowing 512 address locations; however, only 480 are displayed.
440	LOAD DATA, SAME ADDRESS preconditions the control logic to load the next data word received into the display storage location defined by the AR. If more than one data word is sent, only the last word is displayed.
460	LOAD DATA, INCREMENT ADDRESS preconditions the control logic to load the next data word received into the display storage location defined by the AR, and then increments the AR. One or more data words may be stored using this command.
204	SET CURSOR, SAME ADDRESS sets the cursor in the display location defined by the AR.
224	SET CURSOR, INCREMENT ADDRESS sets the cursor in the location defined by the AR, and then increments the AR.
004	CLEAR CURSOR, SAME ADDRESS clears the cursor in the location defined by the AR.
024	CLEAR CURSOR, INCREMENT ADDRESS clears the cursor in the location defined by the AR, and then increments the AR.
210	SET DELINEATOR, SAME ADDRESS sets the delineator in the location defined by the AR.
230	SET DELINEATOR, INCREMENT ADDRESS sets the delineator in the location defined by the AR, and then increments the AR.
010	CLEAR DELINEATOR, SAME ADDRESS clears the delineator from the location defined by the AR.
030	CLEAR DELINEATOR, INCREMENT ADDRESS clears the delineator from the location defined, and then increments the AR.
304	SET ALL CURSORS sets the cursor in all locations.
104	CLEAR ALL CURSORS clears the cursor in all locations.
310	SET ALL DELINEATORS clears the delineator in all locations.
110	CLEAR ALL DELINEATORS clears the delineator in all locations.
214	SET CURSOR AND DELINEATOR, SAME ADDRESS sets the cursor and delineator in the location defined by the AR.
234	SET CURSOR AND DELINEATOR, INCREMENT ADDRESS sets the cursor and delineator in the location defined and then increments the AR.
014	CLEAR CURSOR AND DELINEATOR, SAME ADDRESS clears the cursor and delineator from the location defined by the AR.
034	CLEAR CURSOR AND DELINEATOR, INCREMENT ADDRESS clears the cursor and delineator from the location defined and then increments the AR.
314	SET ALL CURSORS AND DELINEATORS sets the cursor and delineator in all locations.
114	CLEAR ALL CURSORS AND DELINEATORS clears the cursor and delineator in all locations.
450	LOAD DATA, CLEAR DELINEATOR, SAME ADDRESS clears the delineator from the addressed location, and loads the next data word received into that location.
454	LOAD DATA, CLEAR CURSOR AND DELINEATOR, SAME ADDRESS clears the cursor and delineator from the addressed location, and loads the next data word received into that location.
644	LOAD DATA, SET CURSOR, SAME ADDRESS sets the cursor in the addressed location, and loads the next data word received into that location.
650	LOAD DATA, SET DELINEATOR, SAME ADDRESS sets the delineator in the addressed location, and loads the next data word received into that same location.
654	LOAD DATA, SET CURSOR AND DELINEATOR, SAME ADDRESS sets the cursor and delineator in the addressed location, and loads the next data word received into that same location.
464	LOAD DATA, CLEAR CURSOR, INCREMENT ADDRESS clears the cursor in the addressed location, then increments the AR. The next data word is loaded into the newly addressed location, and then the AR is incremented again. (The AR is incremented each time a data word is loaded.)
470	LOAD DATA, CLEAR DELINEATOR, INCREMENT ADDRESS performs the same function as 464 except that the delineator is cleared first.
474	LOAD DATA, CLEAR CURSOR AND DELINEATOR, INCREMENT ADDRESS performs the same function as 464, except that both the cursor and delineator are cleared first.
664	LOAD DATA, SET CURSOR, INCREMENT ADDRESS sets the cursor first.
670	LOAD DATA, SET DELINEATOR, INCREMENT ADDRESS sets delineator first.
674	LOAD DATA, SET CURSOR AND DELINEATOR, INCREMENT ADDRESS sets the cursor and delineator first.
140	CLEAR ALL DATA clears the character display from all locations. Delineators and Cursors are unaffected.
000	OFF LINE turns the VDU off-line, and the VDU ignores all data transmissions.
154	CLEAR ALL DATA, CURSOR AND DELINEATORS clears the characters, cursors, and delineators from all locations.
444	LOAD DATA, CLEAR CURSOR, SAME ADDRESS clears the cursor in the location defined by the AR, and loads the next data word received into the same location.
	The END OF LINE commands operates on all locations between the location defined by the AR and the last location in that particular line.
042	CLEAR DATA TO END OF LINE (EOL)
046	CLEAR DATA AND CURSORS TO EOL
052	CLEAR DATA AND DELINEATORS TO EOL
056	CLEAR DATA, CURSORS AND DELINEATORS TO EOL
206	SET CURSORS TO EOL
214	SET DELINEATORS TO EOL
216	SET CURSORS AND DELINEATORS TO EOL
006	CLEAR CURSORS TO EOL
014	CLEAR DELINEATORS TO EOL
016	CLEAR CURSORS AND DELINEATORS TO EOL

NOTES

COMMAND REGISTER LOAD

The VDU is loaded by $\overline{\text{VCST}}$, which is generated by the interface pcb when a command word is sent to the VDU. Figure 2A-23 illustrates the Command Register logic.

The leading edge of $\overline{\text{VCST}}$ loads DL05 and DL07 into the CR and its trailing edge loads in DL01, DL02, DL03, DL04, DL06, and DL08. The trailing edge of $\overline{\text{VCST}}$ also sets COMMAND REGISTER FULL (CRF).

DATA REGISTER LOAD

The Data Register (DR) may be loaded under two conditions:

1. A word is loaded into the DR after the CR is loaded with a load address command word. In this case, the VDU transfers the word from the DR to the AR in the MSR address match logic. The address defines the MSR location to be updated.

2. A word is loaded into the DR after the CR is loaded with a command that requires update of the data bits of the MSR location (DATA . VRDY set in CR). The MSR is a 9 x 512-bit register; seven of these bits control the display pattern, one controls cursor display, and one controls the delineator display. The cursor and delineator bits are loaded from the CR.

Figure 2A-24 illustrates the Data Register logic. The DR is loaded by $\overline{\text{VDST}}$, which is asserted by the interface pcb when the DTC 8 or VCU sends a data word to the VDU and VRDY is set in the CR.

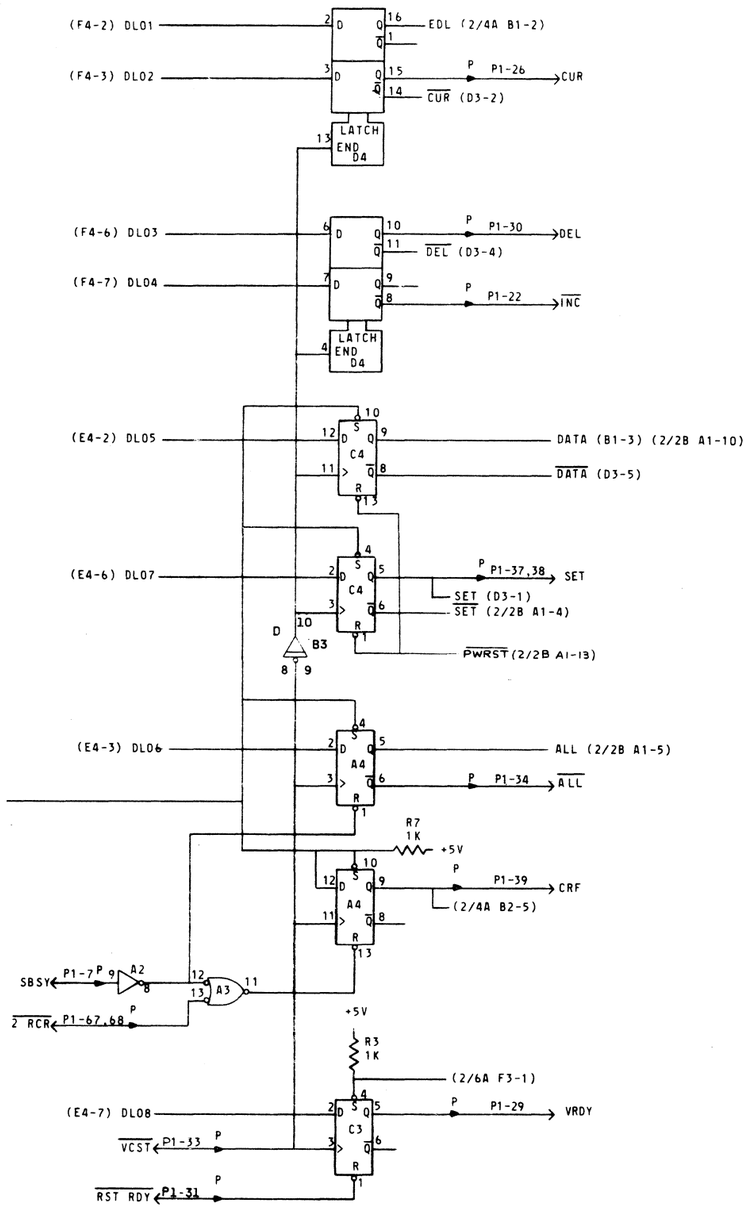


FIGURE 2A-23
VDU CR LOGIC

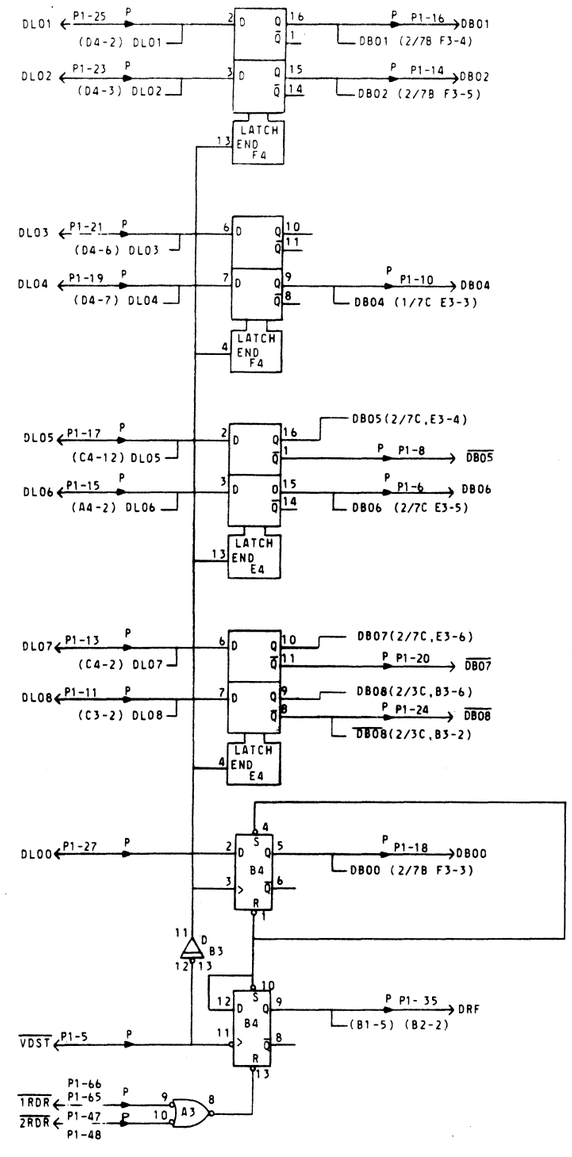


FIGURE 2A-24
DATA REGISTER LOGIC

The leading edge of $\overline{\text{VDST}}$ loads DL00 into the DR, and the trailing edge of $\overline{\text{VDST}}$ latches in DL01 - DL08. The trailing edge of $\overline{\text{VDST}}$ also sets DATA REGISTER FULL (DRF).

ADDRESS REGISTER LOAD

When the program is to update the MSR, it must load the VDU AR to define the location(s) to update. The AR may be incremented (INC set) after the addressed MSR location is updated. This allows the program to update more than one location in the MSR by issuing a single command.

The AR is loaded when the CR is loaded with a load address command word (RDY, SET true; DATA, DEL, CUR false) and the DR is full (DRF set). Figure 2A-25 illustrates the logic used to load the AR.

When SET is true and $\overline{\text{CUR}}$, $\overline{\text{DEL}}$, and $\overline{\text{DATA}}$ are false in the CR, (LD ADD) LOAD ADDRESS is asserted at A2-12. When the program loads the DR (DRF true), $\overline{\text{LD ADD}}$. $\overline{\text{DRF}}$ is asserted. At the next BT1, flop E4-5 is reset to assert $\overline{\text{ADDRESS PARALLEL ENABLE}}$ ($\overline{\text{APE}}$), enabling gate E5-6 at the next BT3. As $\overline{\text{APE}}$ enables the parallel load of the AR, $\overline{\text{ADDRESS CLOCK}}$ ($\overline{\text{ACL}}$) is asserted to load DB00 - DB07 from the DR into the AR. Flop E4-5 is set by the next BT5, and $\overline{\text{APE}}$ is reset and $\overline{\text{ACL}}$ disabled.

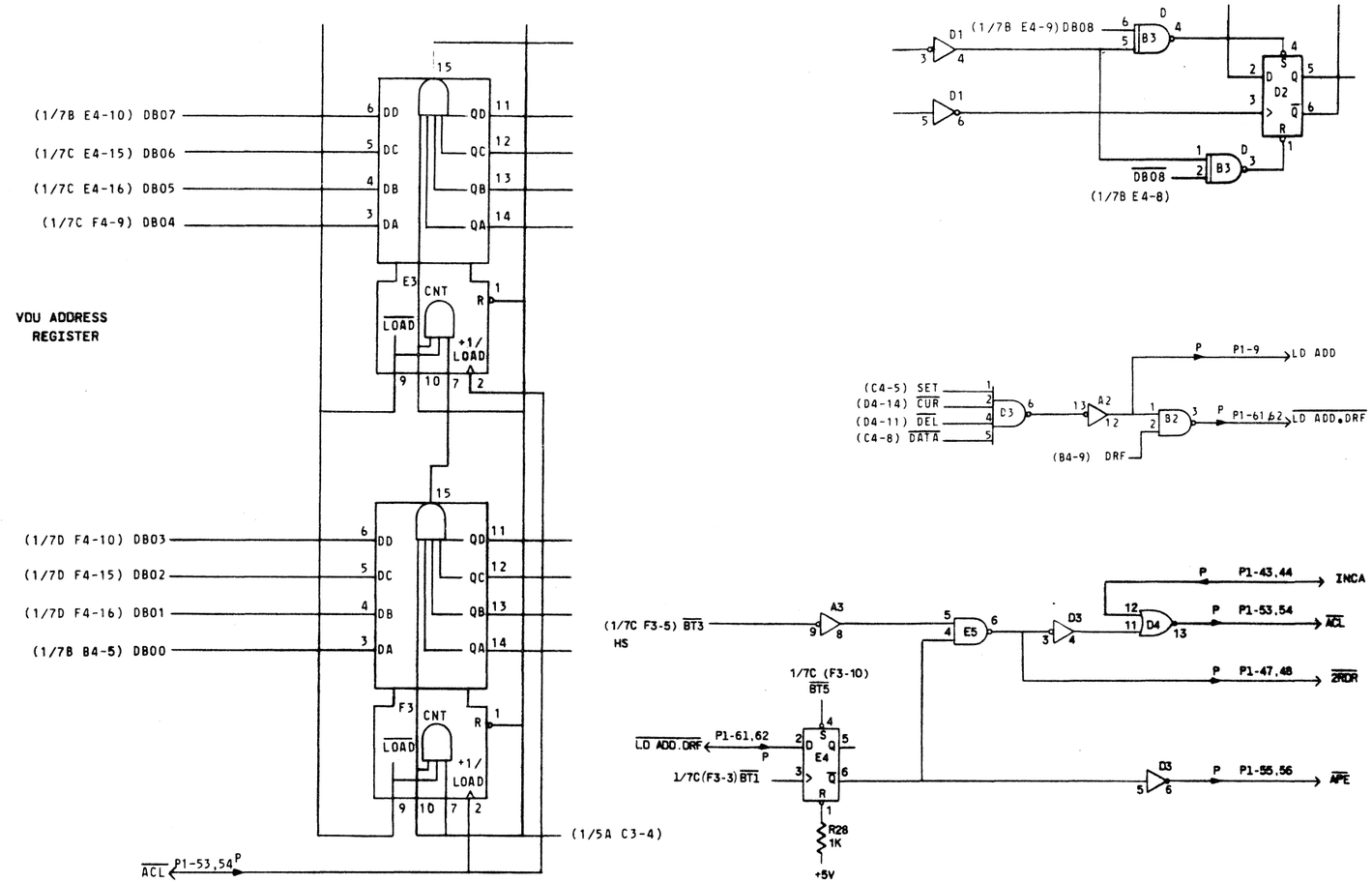


FIGURE 2A-25
ADDRESS REGISTER LOGIC

COMMAND EXECUTION

INTRODUCTION

Command Execution is the process of updating the MSR. During the update process, data bits are loaded from the DR and cursor and delineator bits are loaded from the CR. Figure 2A-26 is a block diagram of the MSR update control logic.

Input to the MSR is controlled by two multiplexors. One multiplexor switches the input to the character bits of the MSR from the MSR output (DB0R - DB6R) to the DR (DB00 - DB06). The other multiplexor switches input to the cursor and delineator bits from the MSR output to the CR output.

Each time the MSR is shift-loaded ($\overline{MSRC}$), the MSR AR in the Main Address Match logic is incremented. This register records the MSR location to be loaded next. The VDU AR, loaded during command initiation, is compared to the MSR AR. When they are equal, the Main Address Match logic asserts MAIN ADDRESS MATCH (MAM). MAM enables the multiplexor control logic. If the data bits are to be updated, the content of the DR is loaded into the MSR via the multiplexor. If the cursor and/or delineator are to be updated, the cursor and/or delineator bits are loaded from the CR to the MSR.

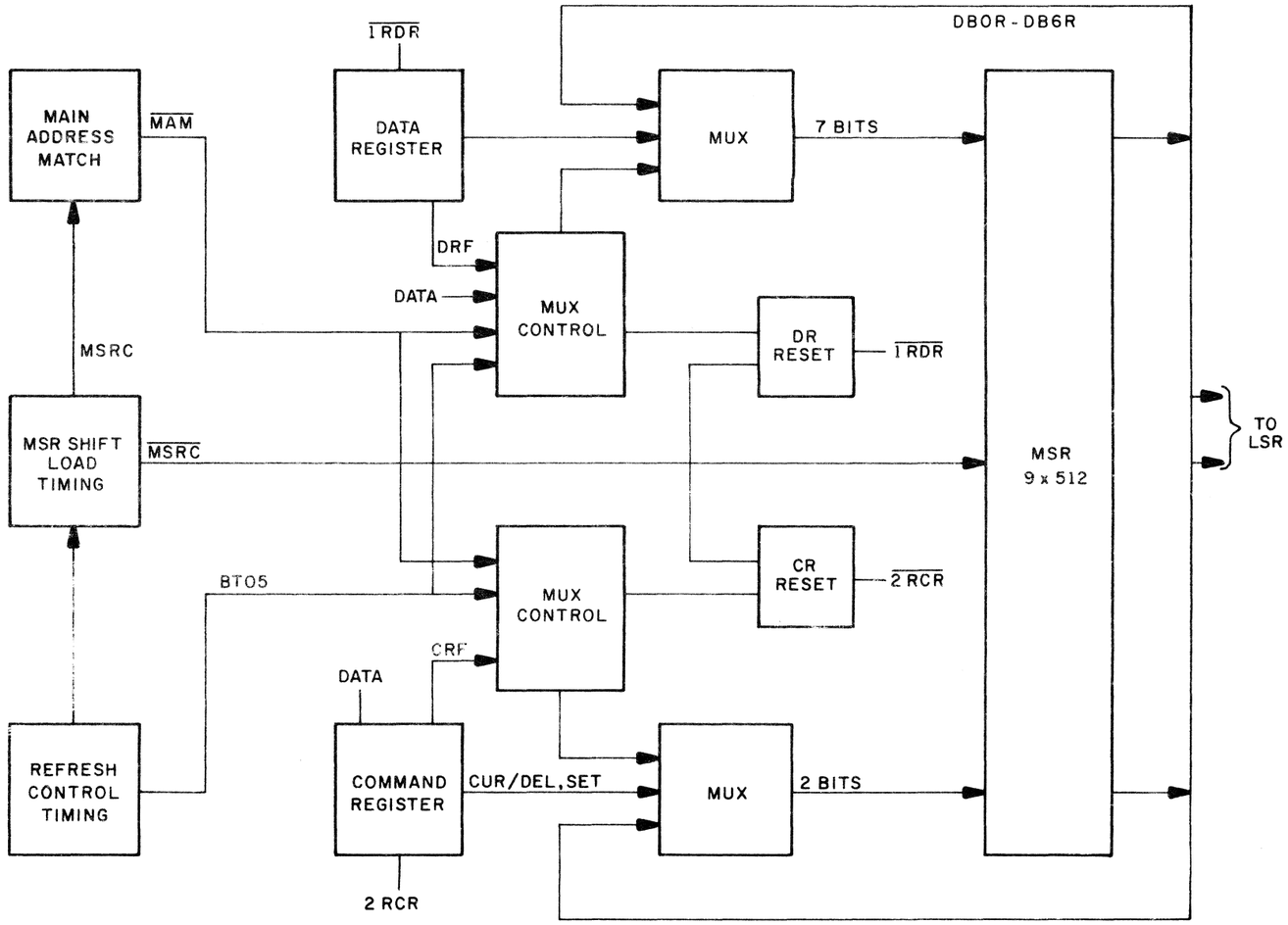


FIGURE 2A-26
MSR CONTROL

The update sequence is described under the following headings:

- MSR Load Timing
- Main Address Match
- Load Data
- Clear Data
- Set Cursor/Delineator
- Clear Cursor/Delineator.

MSR LOAD TIMING

The MSR is shift-loaded by MSRC. During row times RT0 - RT14 of each character line time CLT0 - CLT15, MSRC is generated 1536 times to recirculate the MSR three times (3 x 512 = 1536). The timing is such that the MSR is recirculated once in 0.35 ms. The MSR must be recirculated at this speed because the VDU must be able to update the MSR as fast as the VCU or DTC 8 can transfer data to the VDU. The DTC 8 has the highest transfer rate: 2 k words/second, or one word every 0.5 ms. Thus any location in the MSR can be updated in less time (0.35 ms) than it takes the DTC 8 to transfer a word (0.5 ms).

$\overline{\text{MSRC}}$ is also asserted, when LSRC is asserted, to transfer 40 characters from the MSR to the LSR during RT15 of CLT3 to CLT14. The LSR is reloaded 12 times during a refresh cycle; therefore, the MSR is shifted 480 (12 x 40) times. As the VDU only uses 480 of the 512 MSR locations, the MSR must be shifted 32 more times (480 + 32 = 512) to bring it back to its starting location for the next refresh cycle. This is done during CLT15 because no data has to be transferred from the MSR to the LSR for the rest of the refresh cycle. During RT0 - RT14 of CLT15, $\overline{\text{MSRC}}$ is asserted 1568 times, instead of 1536 to shift the MSR the required 32 times. Drawing 13136L (sheet 1) illustrates the MSR timing logic.

When $\overline{\text{RT15}}$ goes false, the next $\overline{\text{BT4}}$ clocks flop H3-9 reset to enable pin 10 of gate H1-8. Pin 9 of H1-8 is enabled when gate H1-12 is high ($\overline{1024}$ + $\overline{512}$ + RT + CLT15 · $\overline{32}$). H1-8 goes low to assert MSRC at D1-11 whenever $\overline{\text{BT1-2}}$ or $\overline{\text{BT6-7}}$ are true, and the counter (J1, J2, J3) is incremented. When the counter equals a count of 1536 (1024 · 512), gate H1-12 goes low to disable H1-8 and prevent more MSRC pulses, provided it is during CLT0 - CLT14. If $\overline{\text{CLT15}}$ is true, H1-12 does not go low until the counter reaches a count of 1536 (1024 · 515 · 32). RT15 resets the counter, and also disables gate H1-8 by setting flop H3-9. MSRC is also asserted by $\overline{\text{LSRC}}$ (D1-8) if CLT3/15 and RT15 are true.

MAIN ADDRESS MATCH

The Main Address Match logic indirectly controls the input to the MSR. Drawing 13134L (sheet 2) illustrates the address match logic.

One register (F3, E3, D2-5) is loaded during Command Initiation; when $\overline{\text{APE}}$ is true, $\overline{\text{ACL}}$ loads DB00 - DB08 into the register. The other register (F1, E1, D2-9) is incremented by $\overline{\text{MSRC}}$ and records the MSR location that may be loaded next. The outputs of both registers are compared, and if they are equal, MAIN ADDRESS MATCH (MAM) is asserted (D1-12). MAM enables the MSR multiplexor control logic. If the MSR location is to be updated, the multiplexor switches the input to the MSR from the MSR output to the Data Register output, DB00 - DB06, (character bits) or the Command Register output (DEL/CUR).

LOAD DATA

When the program is to update the character bits in an MSR location(s), it loads a command word into the VDU CR that sets DATA, SET, and KRDY. If more than one location is to be updated, it also sets INC. Drawing 13135L (sheet 1) illustrates the logic used to update the MSR.

The logic asserts $\overline{\text{DLD DATA}}$ (drawing 13134L, sheet 1, B1-6) when:

- DATA is set in the CR
- the DR is full (DRF set)
- the address match logic asserts MAM.

This signal causes $\overline{\text{DATA}}$ to be set at B5-5 when BT05 becomes true (BT05 = BT0 + BT5 · RT15). DATA gates DB00 - DB06 through the multiplexor to the MSR input, and the next MSRC pulse (BT1-2 + BT6-7) loads it into the MSR. MSRC also asserts $\overline{\text{1 RESET DATA REGISTER}}$ ($\overline{\text{1RDR}}$, B4-8) to reset DRF (drawing 13134, sheet 1). $\overline{\text{1RDR}}$ asserts INCREMENT ADDRESS (INCA, D2-6) if INC is set in the CR. INCA asserts $\overline{\text{ACL}}$ which increments the Address Register in the VCU, and the next time DRF and MAM are true, the update sequence is repeated.

CLEAR DATA

The program can clear the character bit in:

- a single MSR location
- all MSR locations
- all MSR locations that form one character line.

To clear data, the program must set DATA and clear SET in the VDU CR. If ALL is also set, the VDU clears the character bits in all MSR locations. If EOL is set, the VDU clears the character bits from the addressed MSR location to the last MSR location in that character line.

When DATA and ALL are set and SET is reset, CLEAR DATA (CL DATA) is asserted (drawing 13134L, sheet 2, A1-12). CL DATA forces all the multiplexor outputs low, and the MSRC pulses clock all zeros into the MSR. However, to display a blank on the screen the ROM must be addressed by code 040, not 000. The MSR inputs (DB0R - DB04R, DB6R) are all affirmative, except one, $\overline{\text{DB5R}}$. This low input to data bit 5 of the MSR represents a one, rather than a zero, as are the others. The LSR output inverts bit 5 so that the character ROM is addressed by 040_8.

To clear one character line or part of that line, the program sets DATA and EOL and resets SET. CRF and MAM assert $\overline{\text{CLD DATA}}$ (drawing 13134L, sheet 2) to enable pin 1 of gate B1-12. Pin 2 is enabled by EOL, and when BT05 goes true, $\overline{\text{LNEF}}$ is set. $\overline{\text{LNEF}}$, DATA, and $\overline{\text{SET}}$ force A1-8 low and CL DATA is asserted. Each succeeding MSRC pulse loads a blank character (040_8) into the MSR. At the end of the character line, the line counter asserts $\overline{\text{LNE}}$ (drawing 13136L, sheet 1, H5-7) to clear $\overline{\text{LNEF}}$ and therefore CL DATA.

SET CURSOR/DELINEATOR

When the program is to set the cursor and/or delineator bit in a single MSR location, it sets CUR and/or DEL and SET in the VDU CR. When the address match logic asserts MAM, $\overline{\text{CLD DATA}}$ is asserted and the next BT05 pulse clocks flop E5-9 reset to enable gates C2-3 and C2-11. If CUR or DEL is false, gates C2-3 and C2-11 remain high, allowing the MSR output back to its input (recirculation). However, if CUR or DEL is set, gate C2-3 or C2-11 becomes low to disable the recirculation and enable the set gates (C3-6, C3-8). As SET is true, the next MSRC pulse loads a cursor and/or delineator bit. Because B5-8 is high, MSRC also asserts $\overline{\text{2RCR}}$, which clears CRF and disables CLD DATA. The next BT05 pulse clocks flop B5-9 set again, and gates C2-3 and C2-11 are disabled.

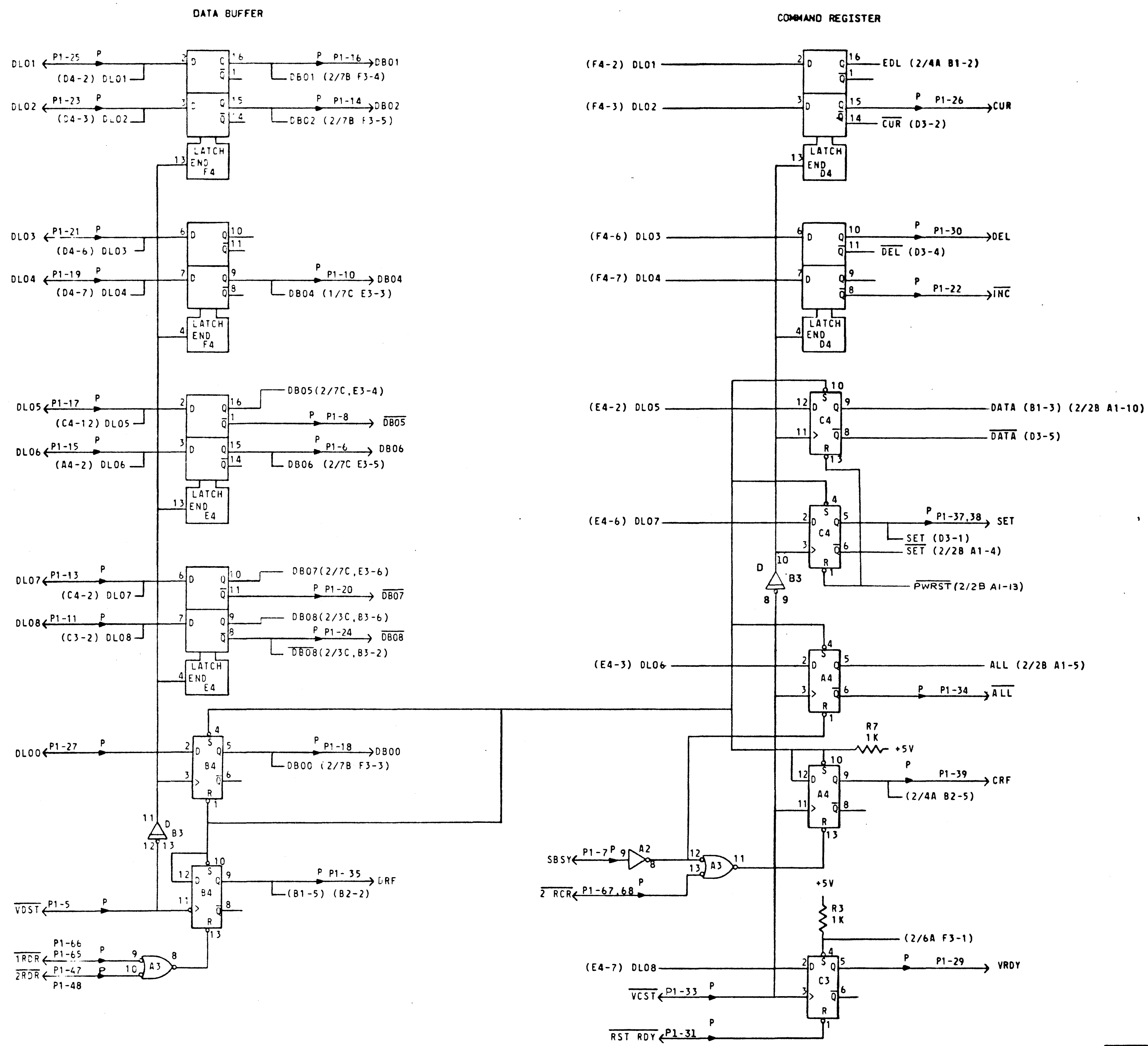
When the program is to set the cursor and/or delineator bits in all MSR locations, it sets ALL with SET and CUR and/or DEL. $\overline{\text{ALL}}$ resets flop B5-9 to enable gates C2-3 and C2-11, and each succeeding MSRC pulse loads a cursor and/or delineator bit into the MSR.

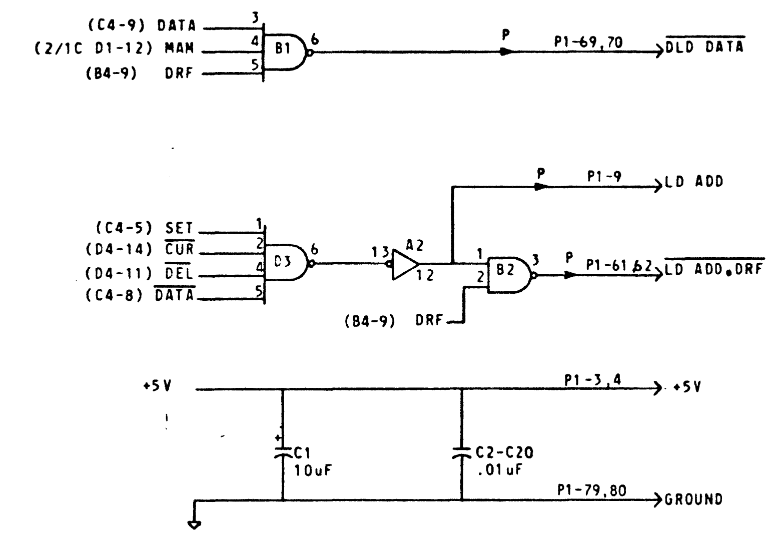
When the program is to load a cursor and/or delineator bit into the MSR locations of a character line or part of that line, it sets EOL with SET and CUR and/or DEL. When $\overline{\text{CLD DATA}}$ is asserted, the next BT05 pulse sets $\overline{\text{LNEF}}$. LNEF enables gates C2-3 and C2-11, and each succeeding MSRC pulse loads a cursor and/or delineator bit into the MSR. $\overline{\text{LNEF}}$ is reset when the location that ends the character line is addressed and loaded ($\overline{\text{LNE}}$).

CLEAR CURSOR/DELINEATOR

The program clears cursor and/or delineator bits in the same manner as it sets them. The only difference is that SET is not set in the CR, causing MSRC to clear the cursor and/or delineator bit in the desired MSR locations.

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	21 OCT 74	DN		
B	ST31	ECO INC		WC		
C	ST 260	ECO INC				





CHIP CHART				
	1	2	3	4
F	93L16	7486	93L16	7475
E	93L16	7486	93L16	7475
D	7404	7474	7420	7475
C	7402		7474	7474
B	7410	7400	857	7474
A	7410	7404	3001	7474

IC POWER AND GND CHART		
GND	+5V	
7	14	A1,A2,A3,A4,B1,B2,B3,B4,C1,C3,C4,D1,D2 D3,E2,F2
8	16	E1,E3,F1,F3
12	5	E4,F4,D4

MISSING COMPONENTS
R1,R2,R4,R5,R6

LAST COMPONENT
R7,C20

UNLESS OTHERWISE NOTED
All resistors are 1/4W
Spare Gates A2-2,4,6,, A3-3,6

NEXT ASSY.	USED ON
13134A	ST
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00 = ± .01 ANGLES = ± 0° 30' .000 = ± .005

MATERIAL
SPEC
FINISH
SPEC

DR NORTON 21 OCT 74
CHK CASSELMAN 30 OCT 74
DSGN GHT
ENGRG GHT
ORIGINALLY DESIGNED FOR ST
APPROVED
APPROVED
DWG CODE

OTTAWA CONSOLIDATED COMPUTER INC. CANADA

LOGIC DIAGRAM VDU-1

SCALE —— SHEET 1 OF 2 | SIZE D | DWG NO 13134L

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	21 OCT 74	DN		
B	ST31	SEE SH 1	30 OCT 74	WS		
C	ST CER	ECO ING	20 FEB 75	RD		

MEM ADDRESS REGISTER

VDU ADDRESS REGISTER

(1/7B E4-10) DB07
(1/7C E4-15) DB06
(1/7C E4-16) DB05
(1/7C F4-9) DB04
(1/7D F4-10) DB03
(1/7D F4-15) DB02
(1/7D F4-16) DB01
(1/7B B4-5) DB00

LLP P1-49,50
MSRC P1-51,52
APE P1-55,56
SCL P1-53,54

(1/5A C3-4)

(1/7B E4-9) DB08
DB08 (1/7B E4-8)

P P1-63,64 → MAF

MAM (B2-4) (1/3D B1-4)

LINE P1-57 P1-58

P P1-40 → LNEF

(1/5B A4-5) ALL
(1/5C C4-9) DATA
(1/5C C4-6) SET

P P1-73,74 → CL DATA

BTOS P1-59 P1-60
(1/5D D4-16) EDL

PWRST P1-77,78
PWRST 1/5C (C4-1)

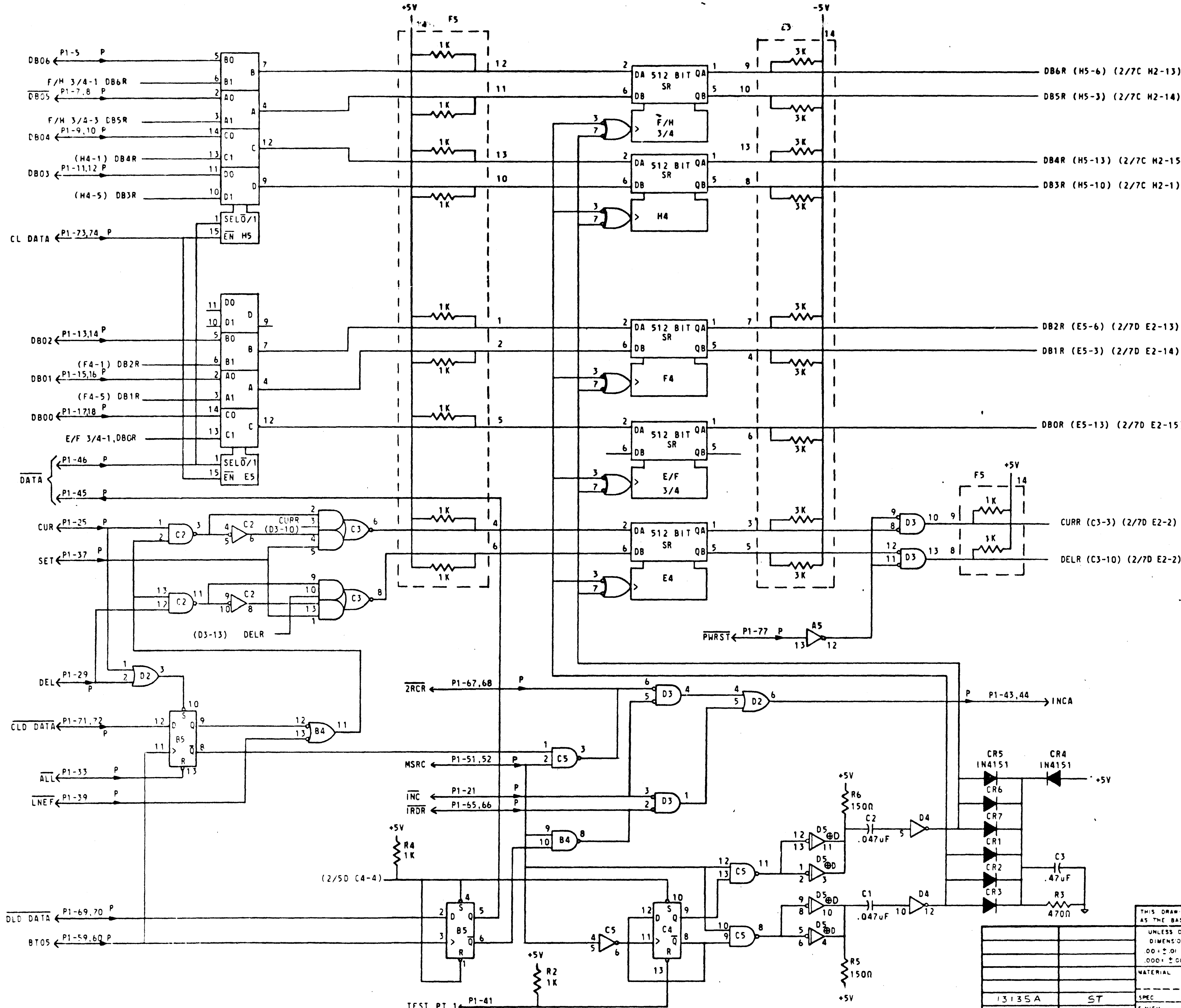
(D1-12) MAM
(1/5B A4-9) CRF

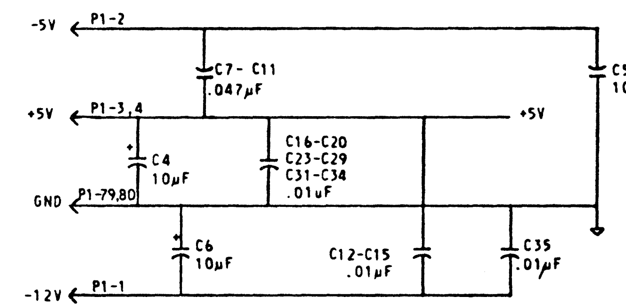
P P1-71,72 → CLD DATA

13134L

SCALE	SHEET 2 OF 2	D SIZE	DWG NO 13134L

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		PRODUCTION RELEASE	21 OCT 74	DN		





CHIP CHART

	1	2	3	4	5
H	8308	2519	1403	1403	9322
F	(3514)	RES PAK	1403	1403	RES PAK
E	SEE TABLE	2519	RES PAK	1403	9322
D	(3514)	3003	7402	5013	858
C	SEE TABLE	7400	7451	7474	7400
B	(3514)	74165	3001	7400	7474
A	SEE TABLE	7474	7474	7410	7404

ROM VARIANT TABLE

	A/B1	C/D1	E/F1
13135A-01	FSL30336 TYPE C	FSL30335 TYPE B	FSL30334 TYPE A
13135A-02	FSL30598 TYPE C	FSL30597 TYPE B	FSL30596 TYPE A

I.C. POWER & GROUND TABLE

-5V	-12V	+5V	GROUND	
		14	7	A2,A3,A4,A5, B3,B4,B5, C2,C3,C4,C5 D2,D3,D5
	1	24	12	A/B1,C/D1,E/F1
		16	8	B2,H5,E5
	7	14		D4
	5	16		E2,H2
8			4	E/F 3/4,F/H 3/4,F4,H4

MISSING COMPONENTS

C21,C22,C30

LAST NUMBER USED FOR COMPONENTS

R6,C35,CR7

UNLESS OTHERWISE NOTED

ALL RESISTORS ARE 1/4 W

NEXT ASSY.	USED ON
13135A	ST

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00 ± .01 ANGLES ± 0° 30' .000 ± .005

MATERIAL

SPEC

FINISH

SPEC

DR NORTON 18 JUNE 73
CHK CASSELMAN
DSGN GHT
ENGRG GHT 18 JUNE 73
ORIGINALLY DESIGNED FOR ST
APPROVED
APPROVED

CONSOLIDATED COMPUTER INC. OTTAWA CANADA

LOGIC DIAGRAM VDU-2

SCALE — SHEET 1 OF 2 SIZE D DWG NO 13135L

REV.	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	2-6-74	DN		

(1/5C F4-1) DB2R
(1/5C F4-5) DB1R
(1/5C E/F 3/4-1) DB0R
(1/4B D3-10) CURR
(1/4B D3-13) DELR
RT15 ← P1-20,19 P
(1/5D F/H 3/4 -1 DB6R
(1/5D F/H 3/4 -3 DB5R
(1/5D H4-1) DB4R
(1/5D H4-5) DB3R
P1-23,24 P → LSRC
F2
-12V
+5V
R1 1K
E2 40 BIT SR
H2 40 BIT SR
RECIRC/LOAD
3K
(1/5A B5-4)
CWT4/44. BTD ← 26 P
DELS (A3-2)
CURS (A3-12)
LATCH END H1 R
A5
(B4-5)
CWT4/44 ← P1-22 P
BT9 ← P1-6 P
(H1-11) CURS
(C4-5) DELS
A2
A3
A4
P P1-40 → RT13
P P1-42 → VD+CD
RC1 ← P1-34 P
RC2 ← P1-31,32 P
RC4 ← P1-30 P
BTC ← P1-38 P
RC8 ← P1-27,28 P
BT8 ← P1-35,36 P
(A2-2)CWT4/44
B4
B3
ROM
A0 A1 A2 A3 A4 A5 A6 A7 A8
O0 O1 O2 O3 O4 O5 O6 O7
E/F1 EN
C/D1 EN
A/B1 EN
8 BIT SR B2
SER IN
SH/LS
DA DB DC DD DE DF DG DH
QH QH

SCALE	SIZE	DWG NO.
SHEET 2 OF 2	D	13135L

13135L

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		ENGINEERING RELEASE		DN		
B	7302	ECO INCOR				

CHIP CHART					
	1	2	3	4	5
J	7493	7493	7493	7490	7493
H	7410		7474	7493	9602
F	7420	1805	74164		1800
E	7474		7474	7474	7400
D	7400		7404	7402	7406
C	7492	8602	7400		555
B	7490	7420			
A	7402	7493	7404	7486	8601

I.C. GND AND POWER TABLE		
+5V	GND	CHIP
16	8	C2,H5
5	10	A2,B1,C1,J1,J2,J3,J4,J5,H4
14	7	A3,A4,B2,C3,D1,D3,D4,D5,E1,E3,E4,E5,F1,F2,F3,
		F5,H1,H3,A1
8	1	C5
	7	A5

MISSING COMPONENTS

R14,R31,C12,C15,C16,C18-20,C30,C32,C34, C37,C43-46

LAST COMPONENT

R34,C47,Q3,CR1

UNLESS OTHERWISE NOTED

All resistors are 1/4W

Spare Gates A3-10,A3-2,A1-3 ,D5-4,D5-10,D5-12,E1-5,A1-13

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .XX ± .01 ANGLES ± 30' .XXX ± .005	DR NORTON	28 Aug 74	CONSOLIDATED COMPUTER INC. OTTAWA CANADA
	CH CASSELMAN	29 Aug 74	
	ESSN SMT	29 Aug 74	LOGIC DIAGRAM VDU-3
MATERIAL	ENGRG SMT	29 Aug 74	
	ORIGINALLY DESIGNED FOR ST		
SPEC			SCALE
FINISH		DWG CODE	SHEET 1 OF 2
SPEC	APPROVED		SIZE D DWG NO 13136L
13136A ST			
NEXT ASSY USED ON			
APPLICATION			

13136L

8 7 6 5 4 3 2 1

D C B A

CHARACTER WIDTH TIME COUNTER

CHARACTER LINE TIME COUNTER

CHARACTER ROW TIME COUNTER

50HZ LINK (OPEN CIRCUIT FOR 60HZ)

J1-78

R34 1K +5

1/7B(E3-10)

(D1-10) 1/6A

(1/6C H3-6)BT0

(A3-13)$\overline{RT13}$

$\overline{CLT8}$

CLT2 4

CLT1 1

CLT4 5

CLT8 1/5D(A4-1)

CLT 3-15 (1/6B H1-4)

(1/6C F2-13) LOGIC 1

$\overline{RT15}$ A3-13

CLT15 1/3B(D4-9)

P1-14 P

BT9

P1-15

P1-41,42 VD+CD

P1-45,46 VD

TEST 4

+5V R32 220Ω

+5V R27 27K

C6 100pF 1us±30%

P1-15

P1-49,50 $\overline{LLR}$

LOGIC 1 C2-13

R26 1K +5V

R29 1K

D5 P1-60,70 V5

P1-21,22 CWT4/44

P1-25,26 $\overline{CWT4/44.BT0}$

P1-75 +15V

R17 2.7K

R18 330Ω

R19 1K

R20 1.5K

R21 3K

C38 .047uF

C7 10uF 25V

Q2 MSP3702

Q3 MPS3702

R30 200Ω HORIZ. FREQ

CR1 1N914

C39 100pF

R22 390K

R23 680Ω

R24 560Ω

R25 3.3K

P1-67,68 HS

HORIZONTAL OSCILLATOR

TEST 2

P1-9

P1-10

H4

+5V R12 15K

TEST 3

P1-18

P1-17

50-200ns

C2-3 LOGIC 1

P1-39,40 $\overline{RT13}$

RC1 P1-33,34

RC2 P1-31,32

RC4 P1-29,30

RC8 P1-27,28

P1-26 $\overline{RT15}$ P1-19

$\overline{RT15}$ (E5-12) (E1-11) (A2-14) (H3-10)

RT15 1/5B(H1-3) 1/38(D4-2)

(1/7C F3-5) $\overline{BT3}$

P1-43,44 INCA

P1-53,54 $\overline{ACL}$

P1-47,48 $\overline{2RDR}$

P1-55,56 $\overline{APE}$

1/7C (F3-10) $\overline{BT5}$

P1-61,62 $\overline{LD\ ADD.DRF}$

1/7C(F3-3)$\overline{BT1}$

R28 1K +5V

1/7C(F3-10) $\overline{BT5}$

$\overline{RT15}$ A3-13

1/7D(F3-8)$\overline{BT0}$

P1-59,60 BT05

SCALE	SHEET 2 OF 2	SIZE D	DWG NO 13136L

CONFIGURATION

The Data Terminal comprises:

- one Keyboard pcb, 13132A
- one Keyboard Control pcb, STC13131A
- one CRT (Ball Brothers)
- three VDU Control pcb: VDU-1, 13134A; VDU-2, 13135A; VDU-3, 13136A
- one Interface pcb: L/150, 13366A; or 12 BD SI, 13133A.
- one power supply, 13351.

Figure 2A-27 illustrates the cabling between the individual components.

POWER

INTRODUCTION

The power supply, 13351, produces all the voltages required to operate the Data Terminal: +15 V, +5 V, -12 V, -5 V, and an ac reference voltage of approximately 3 V peak-to-peak. The +5 V, -5 V, and -12 V supplies are used to power the terminal logic circuits. The +15 V supply is used in the video monitor to produce all the voltages required to operate the CRT and its associated circuits (i.e., +250 V, CRT, B+). The 3 V reference signal is used by the VDU timing to ensure that BTC has the correct period. This reference signal has a frequency twice that of the line frequency.

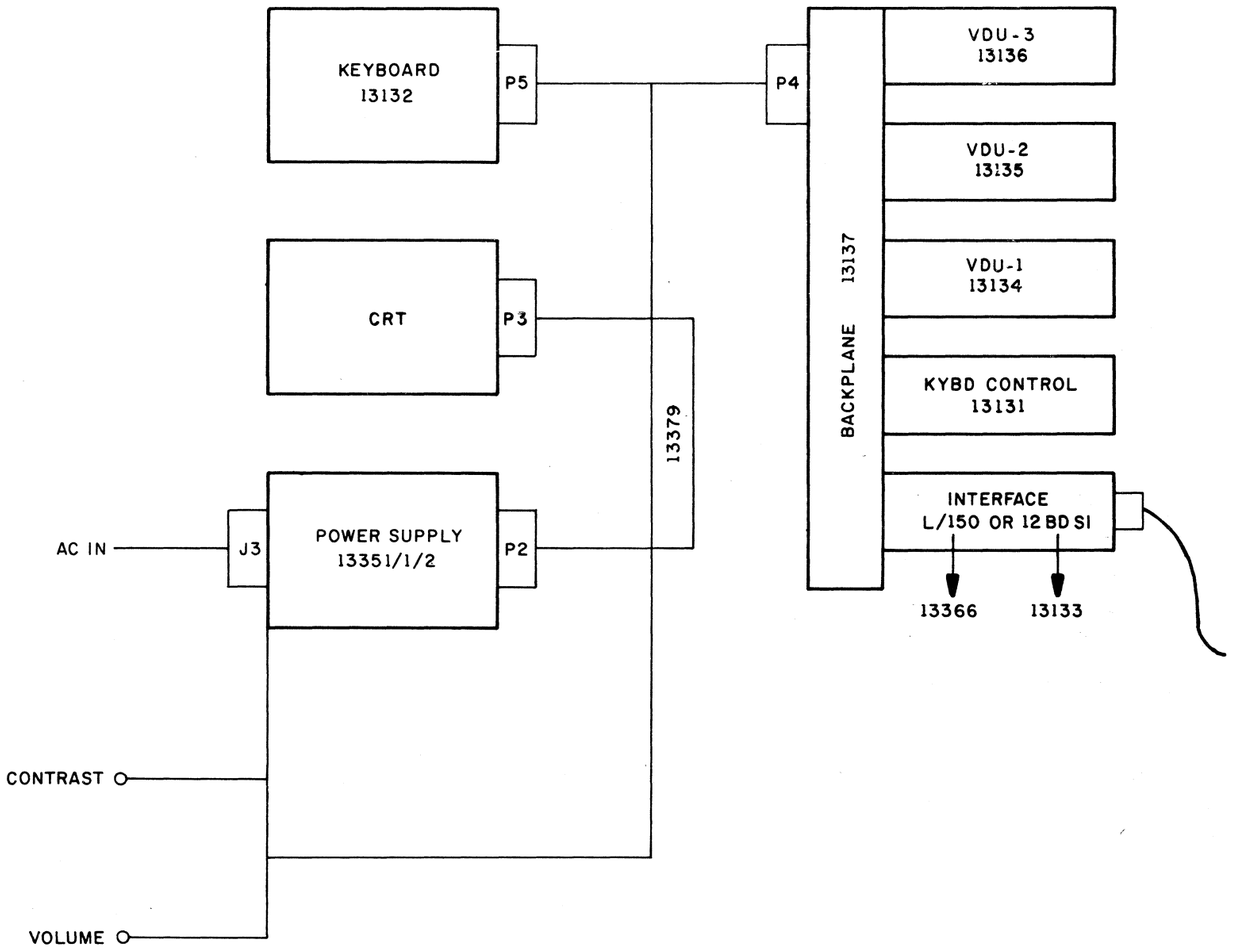


FIGURE 2A-27
DT INTERNAL CABLING

There are two versions of the power supply: 13351/1 or 13351/2. The only difference between the two is the type of transformer used. The 13351/1 power supply uses a transformer with a primary winding that can be tapped for use with 115, 220, 230, or 240 V ac line sources. Drawing 13351S/1 illustrates how the primary cable can be wired for the various input voltages. The 13351/2 power supply has a transformer that uses only 100 V ac line sources in the primary (refer to drawing 13351S/2).

+15 V Regulation

The output of rectifiers CR1 and CR2 are used by the +15 V regulator circuit. CR2 supplies ≃ 21.5 V to the series pass element Q1, which reduces the +21.5 V to +15 V under the control of VR1. The CR1 output is added to the CR2 output (via C1 and C2) to supply VR1 with +25.5 V. VR1 drives Q1 via a current sensing resistor (R1) which limits the maximum current VR1 supplies to Q1. The feedback loop is completed via a potentiometer down loop (R18, etc.) that incorporates a voltage setting potentiometer, R5.

Re-entrant (fold-back) current limiting is provided. A voltage developed by the output current across R14, plus a bias voltage (which is a function of output voltage due to R4), biases Q2. Should this voltage be sufficient to turn Q2 on (≃ 0.6 V), a secondary feed back loop is established via CR6, overriding the voltage control loop. Potentiometer R3 allows compensation for component tolerances. R3 is adjusted to allow a maximum output load current of 0.75 A and a short circuit current of 0.25 A. Figure 2A-28. illustrates how adjustments affect the regulator's characteristics.

+5 V Regulation

The +5 V regulator operates in the same way as does the +15 V regulator. CR3 supplies +10 V to the series pass element Q3, which reduces the +10 V to +5 V under the control of VR2. VR2 is supplied with +21.5 V from CR2. VR2 drives Q4 so that the output voltage is +5 V, the maximum load current is 4.5 A, and the short circuit current is 1.2 A. R12 adjusts the voltage and R10 adjusts the current.

-12 V, -5 V Regulation

NOTE: This regulator is not overload protected as are the +5 V and +15 V regulators.

CR4 supplies -17.5 V to regulator VR3. VR3 reduces the -17.5 V to -12 V. The -12 V is further reduced to -5 V by Q6, Q7, R16, R17, and R22. R22 adjusts the -5 V output.

AC Reference

The ac reference is derived by a simple resistor network (R20, R21, R23). Its frequency is twice that of the line frequency. Figure 2A-29 illustrates a typical wave form.

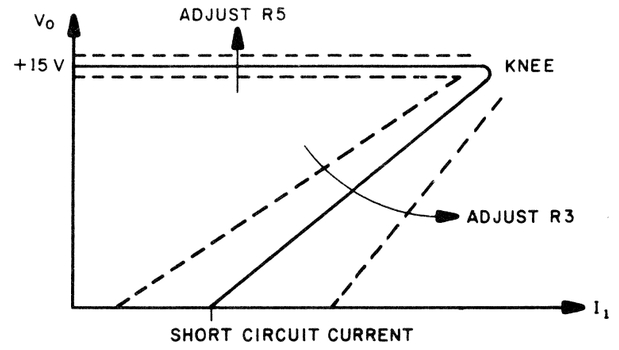


FIGURE 2A-28
+15 V REGULATOR OUTPUT CHARACTER

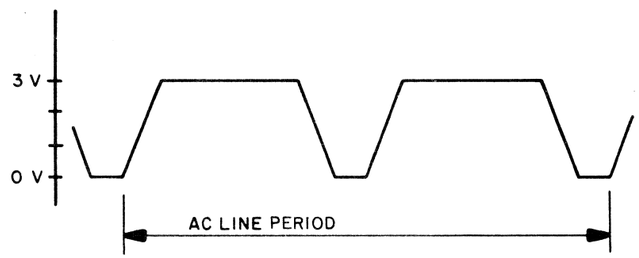


FIGURE 2A-29
AC REFERENCE WAVE FORM

GROUNDING

All power supply outputs share a common ground. This ground is connected to the chassis (earth) via a 1000 ohm resistor, R24.

ELECTRICAL CHARACTERISTICS

INPUT

The input mains voltage may deviate from the stated nominal (100, 115, 220, 230, 240) by ±10%. Under full load and maximum mains input voltage conditions, the maximum VA input will not exceed 12 VA (excluding the power-up transient).

OUTPUT

Characteristics of the dc output are given in Table 2A-6.

POWER ADJUSTMENTS

EQUIPMENT

1. DVM, 0.20 V ±10 MV accuracy.
2. Ammeter, dc current 0 - +10 A 0 - +1 A, accuracy of ±5%, V drop across Ammeter not to exceed ½ V at full scale (e.g., AVO Model 8).

CAUTION: Do not connect or disconnect any cable or component without turning the terminal power off.

TEST POINTS

Figure 2A-30 illustrates the component layout of the power pcb, 13351, and the recommended probe test points.

+15 V ADJUSTMENT

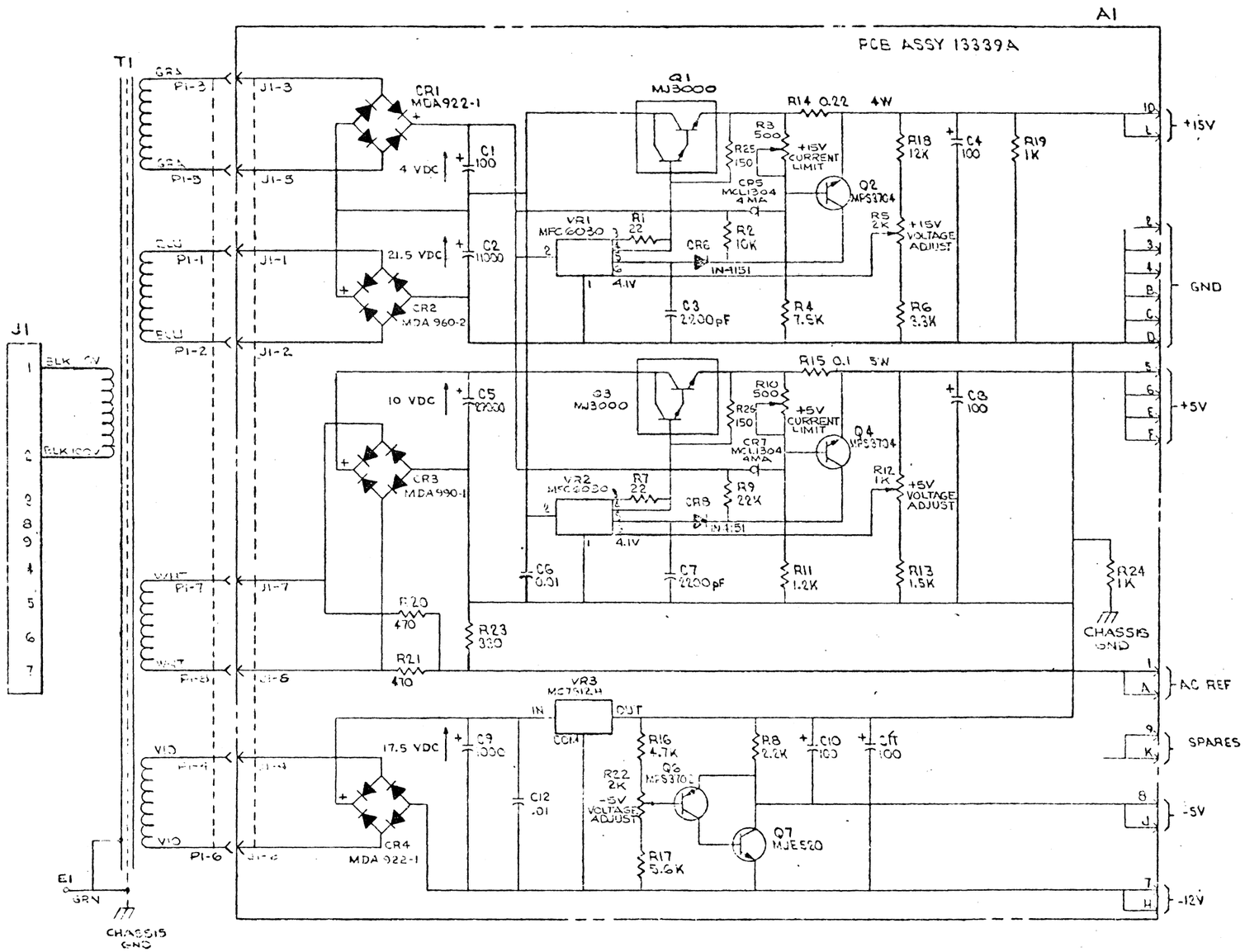
1. Connect DVM probes to the +15 V and GND test points.
2. If the reading lies between +14.5 V and 15.5 V, advance to current check (step 7).
3. Disconnect output connector, P2.
4. Adjust R5 until the DVM reading lies between +14.8 V and 15.2 V.
5. Reconnect P2.
6. Repeat step 2.
7. Disconnect the DVM, and connect an ammeter to the +15 V and GND test points.
8. If the ammeter reading lies between 0.5 A and 0.9 A, the adjustment is complete.
9. Adjust R3 until the ammeter reading lies between 0.65 A and 0.75 A; ignore slow drift.

TABLE 2A-6

DC OUTPUT CHARACTERISTICS

OUTPUT	CHARACTERISTIC	MINIMUM	TYPE	MAXIMUM	UNITS	NOTE
+15 V	Voltage	14.4		15.6	V	2
	Knee Current	1.5			A	
	Short Current	0.5		0.9	A	
	Temperature Coefficient (voltage)			0.3	%/°C	
+5 V	Voltage	5.04		5.16	V	2
	Knee Current	4.0			A	
	Short Circuit Current	0.5		1.5	A	
	Temperature Coefficient			0.03	%/°C	
-5 V	Voltage	4.75		5.25	V	2
	Load Current	0.13			A	
	Temperature Coefficient			0.05	%/°C	
	Load Regulation		70		mV	3
-12 V	Voltage	11.4		12.6	V	2
	Load Current	0.13			A	

NOTES:
1. All characteristics measured at 25°C ambient temperature.
2. Voltage measured at 95% minimum knee or load current.
3. Load regulation is defined as reduction in output voltage when load current is increased from 5% to 95% of mininum knee or load current.



2. COLOR CODE FOR T1 ACCORDING TO CCI SPEC 93247
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE IN OHMS 5% 1/4W, CAPACITORS ARE IN μF

NOTE:

C	ECO INC		
B	ECO INC		

CONSOLIDATED COMPUTER INC. SYLMA

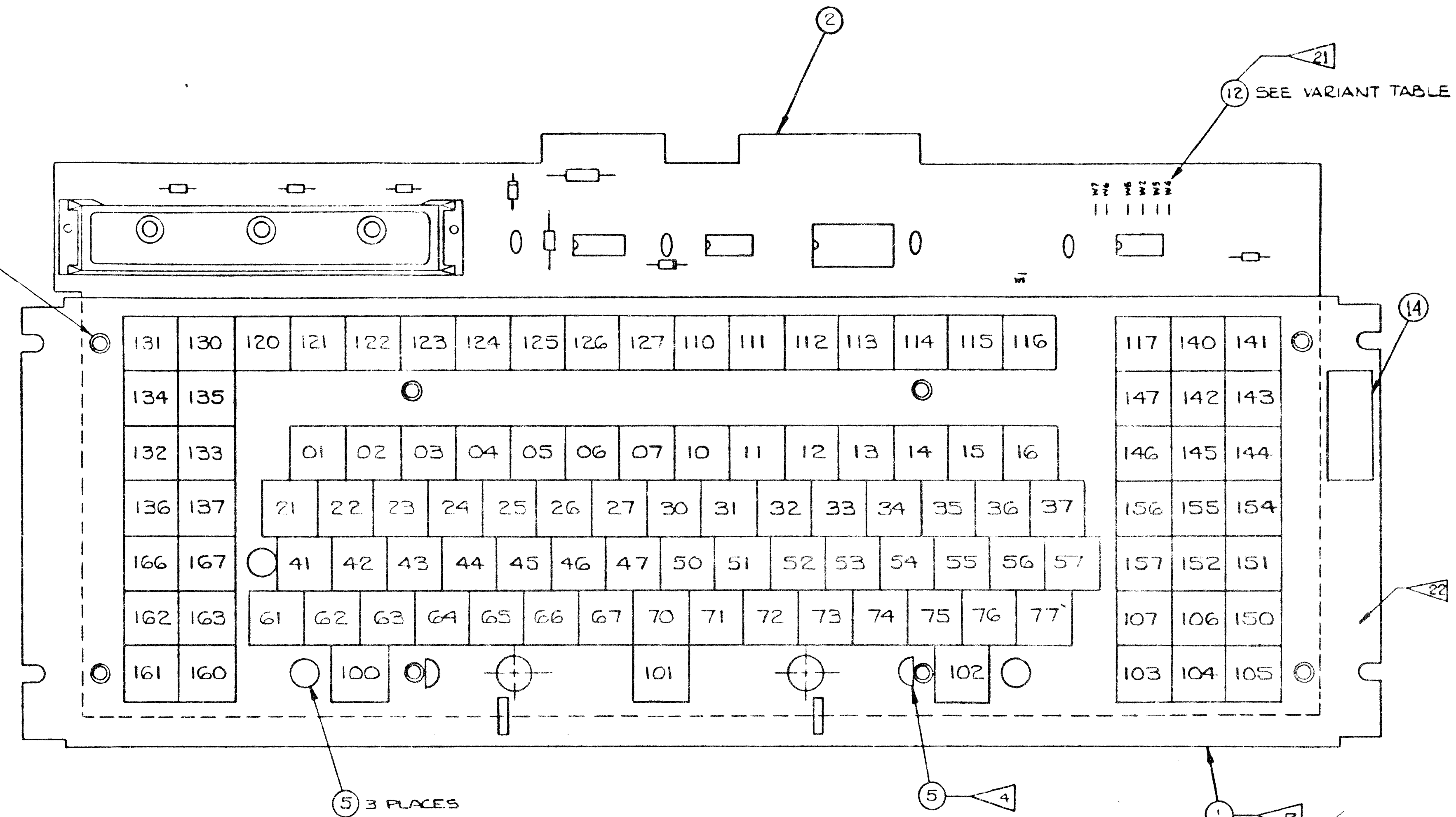
SCHEMATIC DIAGRAM, POWER SUPPLY, 100VAC MK II DATA TERMINAL

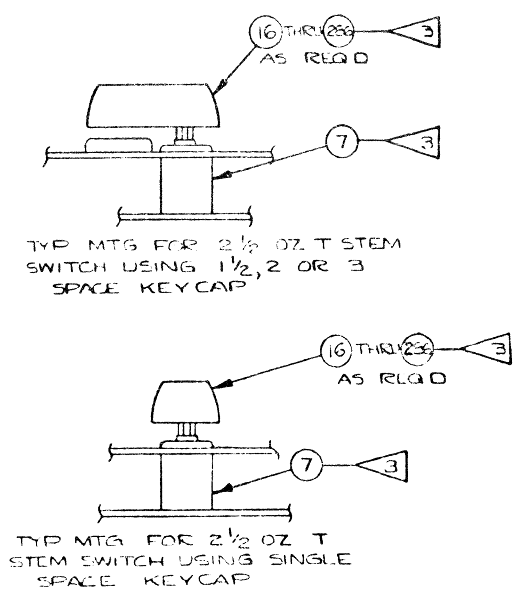
D13351S/2 C

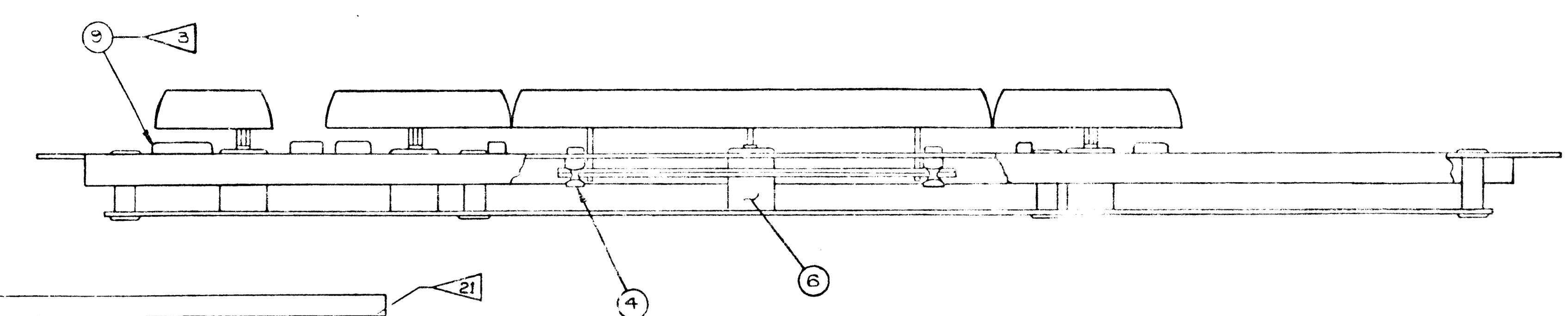
APPENDIX 2A-1

KEYBOARD STYLE LAYOUTS AND KEY CODES

A		PROD. RELEASE			
B		ECO INC			
C		ECO INC			







22. MARK IDENTIFICATION IN ACCORDANCE WITH CCI SPEC 70001

21. INSTALL WIRE LINKS WHERE INDICATED BY '1' IN VARIANT TABLE

20., 19. SEE SH 11

18., 17. SEE SH 10

16., 15. SEE SH 9

14., 13. SEE SH 8

12., 11. SEE SH 7

10., 9. SEE SH 6

8., 7. SEE SH 5

6., 5. SEE SH 4

4. ½ ITEM 5 USED IN 2 PLACES WHERE ITEM 3 (RIVET) INTERFERES. PLACE CUT SIDE AS CLOSE TO RIVET AS POSSIBLE

3. SEE SH 2 & 3 FOR KEYCAP KEY SWITCH AND BUMPER PLUG MTG POSITION TABLE

2. KEYCAPS & SWITCHES DELETED ON TOP VIEW TO ENABLE VIEWING OF SWITCH MTG POSITIONS

1. SEE SHEETS 12 THRU 25 FOR P/L

NOTES:

▷— REF SYMBOL

VARIANT TABLE

DWG NO.	VARIANT DESCRIPTION	WIRE LINKS W1	W2	W3	W4	W5	W6	W7
13383A-01	KATAKANA STANDARD 029 KEYBOARD	1		1	1	1	1	1
[illegible]	KATAKANA STANDARD [illegible] KEYBOARD		1		1	1	1	1
[illegible]	[illegible] KEYBOARD	1	1	1	1	1	1	1
[illegible]	[illegible] KEYBOARD		1			1	1	1
[illegible]	[illegible] KEYBOARD		1	1	1		1	1
[illegible]	[illegible] KEYBOARD [illegible] NUMERIC PAD		1	1	1		1	1
[illegible]	[illegible] NUMERIC PAD	1	1	1	1	1	1	1
[illegible]	[illegible] 029 NUMERIC PAD	1	1	1	1	1	1	1

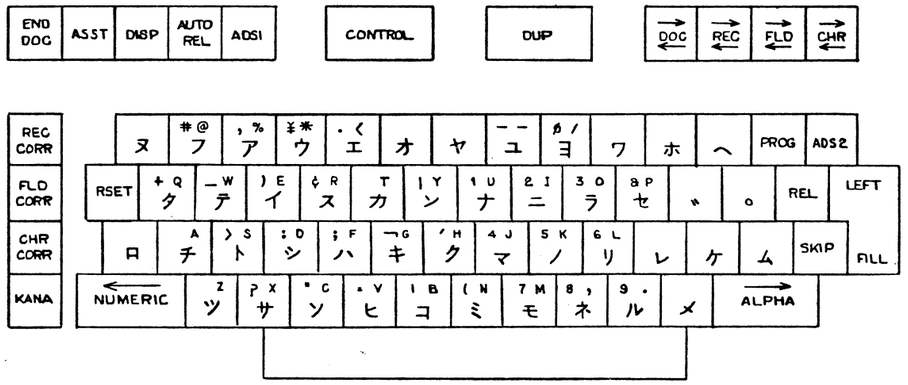
13689A — NEXT ASSY — APPLICATION

CONSOLIDATED COMPUTER INC. — OTTAWA — CANADA

KEYBOARD ASSEMBLY
MK II DATA TERMINAL

SHEET 1 OF 25 — SIZE D — DWG NO 13383A

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	6 MAY 74	RAP		
B		SEE SH 1				
		SEE SH 1				



6. STATUS CODE 01

5. THE FOLLOWING KEYS GENERATE RELEASE CODES
   KANA
   NUMERIC
   ALPHA

NOTES:

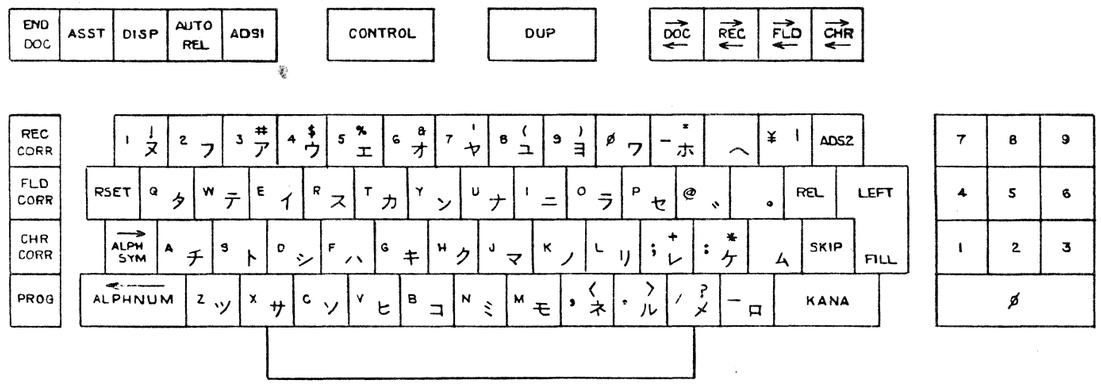
CONFIGURATION FOR
KATAKANA STANDARD 029 13383A-01

SCALE 1:1	D	DWG NO 13383A
SHEET 4 OF 25	SIZE	

13383A REV B

8 7 6 5 4 3 2 1

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		PRODUCTION RELEASE	16 MAY 78	RAP		
B		SEE SH 1				
C		SEE SH 1				



8. STATUS CODE 02

7. THE FOLLOWING KEYS GENERATE RELEASE CODES

KANA
ALPH NUM
ALPH SYM

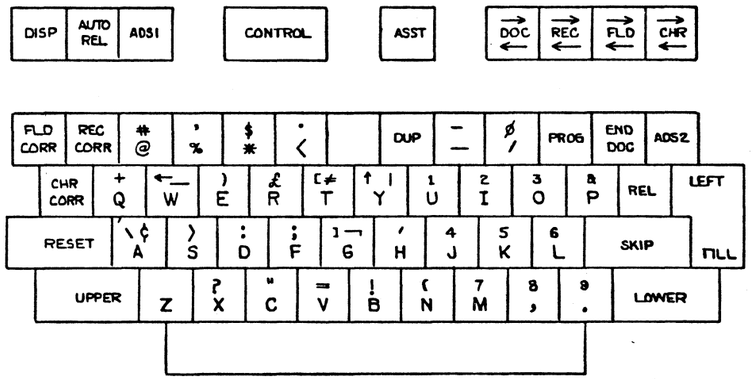
NOTES:

CONFIGURATION FOR
KATAKANA STANDARD ISO . 13383A-02

SCALE 1:1	D	13383A
SHEET 5 OF 25	SIZE	DWG NO

[13383A] B

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		PRODUCTION RELEASE	16 MAY 74	KAP		
B		SEE SH 1				
C		SEE SH 1				



10. STATUS CODE DD

9. THE FOLLOWING KEYS GENERATE RELEASE CODES
   UPPER
   LOWER

NOTES:

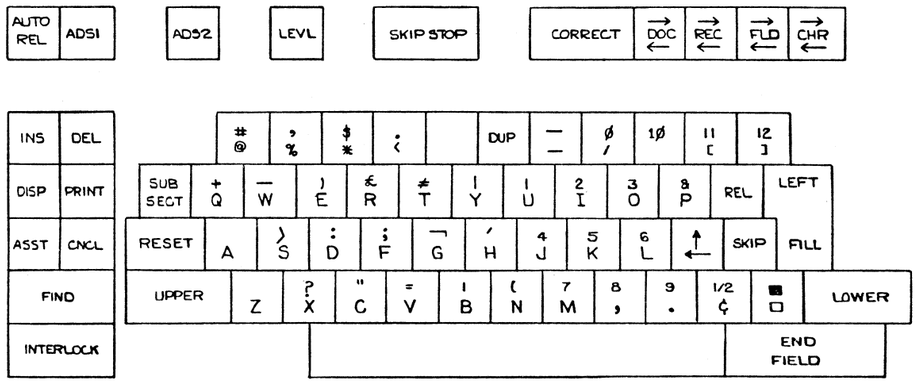
CONFIGURATION FOR
SERIES L PHASE I & II 13383A-03

SCALE 1:1	D	DWG NO. 13383A
SHEET 6 OF 25	SIZE	

13383A-1 B

A

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		PRODUCTION RELEASE	16 MAY 74	R.P.		
B		SEE SH 1				
C		SEE SH 1				



12. STATUS CODE 06

11. THE FOLLOWING KEYS GENERATE RELEASE CODES

LEVL	INTERLOCK
SKIP STOP	UPPER
CORRECT	LOWER
DOC	
INS	
DEL	
DISP	
FIND	

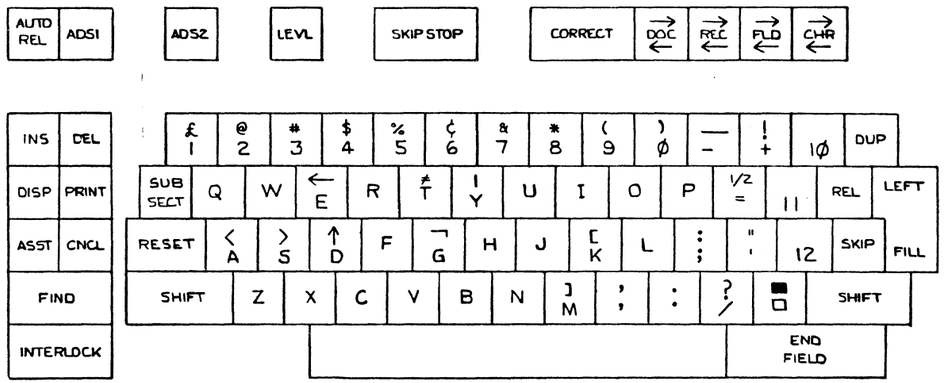
NOTES:

CONFIGURATION FOR STANDARD 029 13383A-04

SCALE 1:1	D	13383A
SHEET 7 OF 25	SIZE	DRG NO

[13383A]

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPROVED
A		PRODUCTION RELEASE	16 MAY 74	RAP	[illegible]	[illegible]
B		SEE SH 1				
C		SEE SH 1				



14. STATUS CODE 10

13. THE FOLLOWING KEYS GENERATE RELEASE CODES

LEVL	INTERLOCK
SKIP STOP	SHIFT (2 KEYS)
CORRECT	
REC	
INS	
DEL	
DISP	
FIND	

NOTES:

CONFIGURATION FOR
STANDARD TELETYPEWRITER 13383A-05

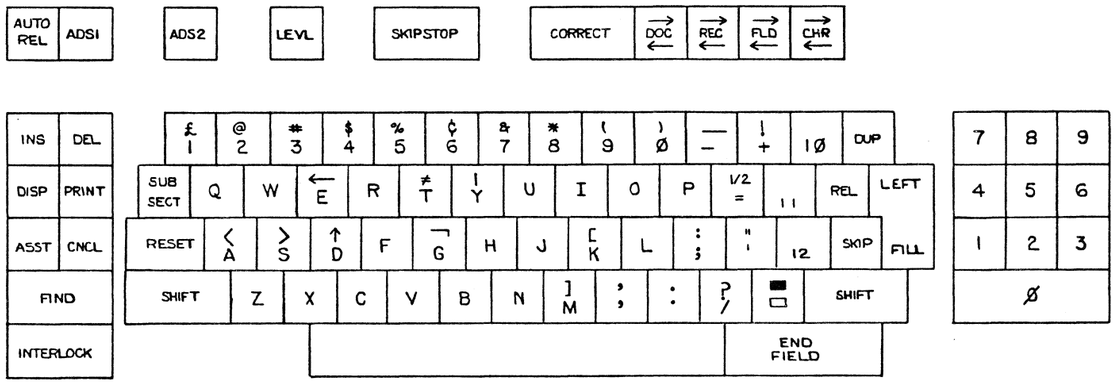
SCALE 1:1	D	13383A
SHEET 8 OF 25	SIZE	DWG NO.

13383A B

8 7 6 5 4 3 2 1

D C A

REV.	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
A		PRODUCTION RELEASE	16 MAY 74	ZAP	MH	[illegible]
B		SEE SH 1				
C		SEE SH 1				



16. STATUS CODE 10

15. THE FOLLOWING KEYS GENERATE RELEASE CODES

- LEVL
- SKIP STOP
- CORRECT
- REC
- INS
- DEL
- DISP
- FIND
- INTERLOCK
- SHIFT (2 KEYS)

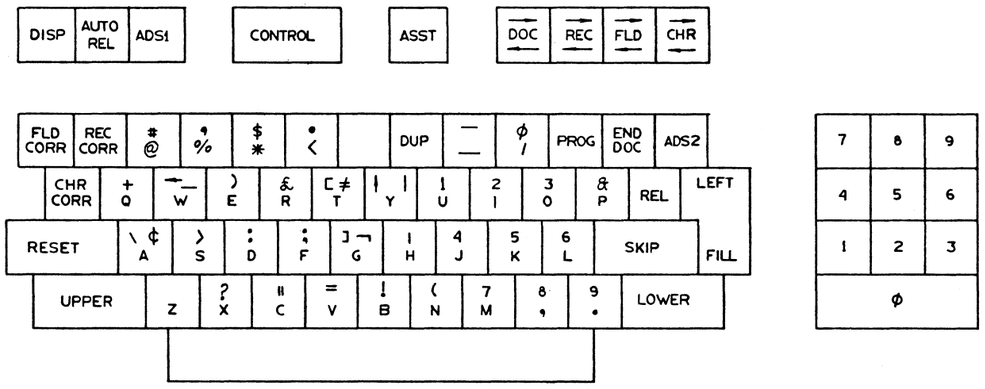
NOTES:

CONFIGURATION FOR
STANDARD TELETYPEWRITER WITH NUMERIC PAD 13383A-06

SCALE 1:1	D	DWG NO. 13383A
SHEET 3 OF 25	SIZE	

[13383A]

REV	ECO	DESCRIPTION	DATE	BY	CHK	APPRVD
B	[illegible]	ECO INC, THIS SHEET ADDED	10 DEC 74	[illegible]	[illegible]	[illegible]
C		SEE SH 1				



18. STATUS CODE 00

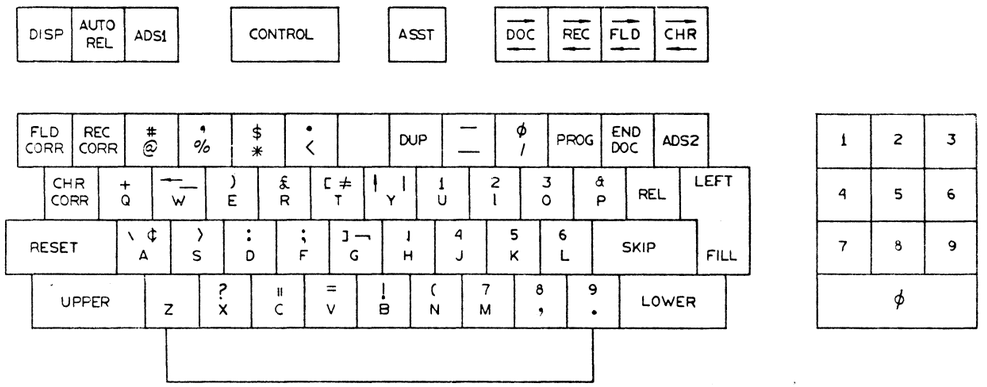
17. THE FOLLOWING KEYS GENERATE RELEASE CODES:
    UPPER
    LOWER

NOTES
CONFIGURATION FOR
SERIES L- PHASE I & II
WITH ISO NUMERIC PAD

13383 A-07

SCALE	SHEET 10 OF 25	SIZE D	DWG NO. 13383 A

13383 A B



20 STATUS CODE 00

19 THE FOLLOWING KEYS GENERATE RELEASE CODES

UPPER

LOWER

NOTES

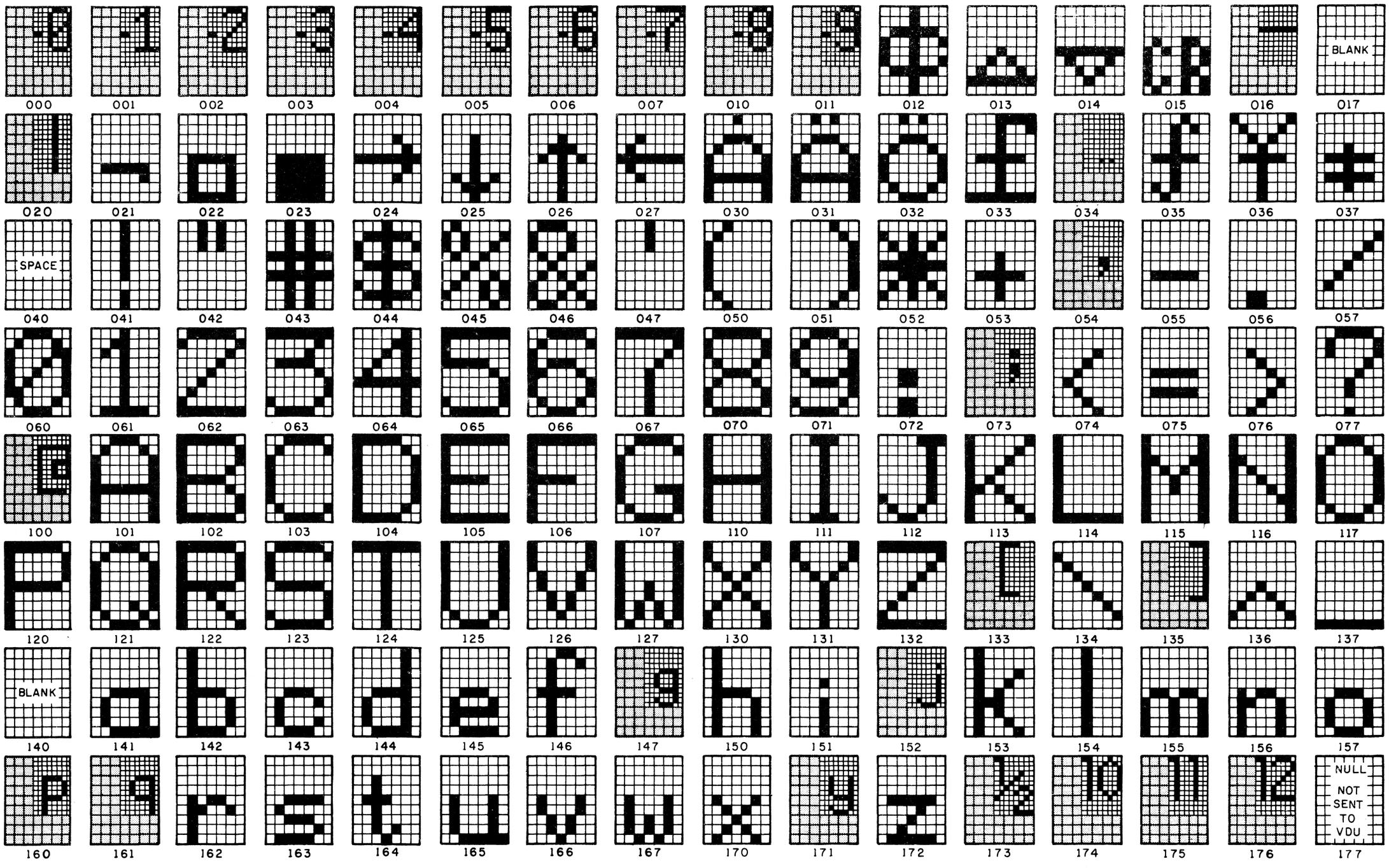
CONFIGURATION FOR SERIES L- PHASE I & II WITH 029 NUMERIC PAD

13383 A-08

13383 A

APPENDIX 2A-2

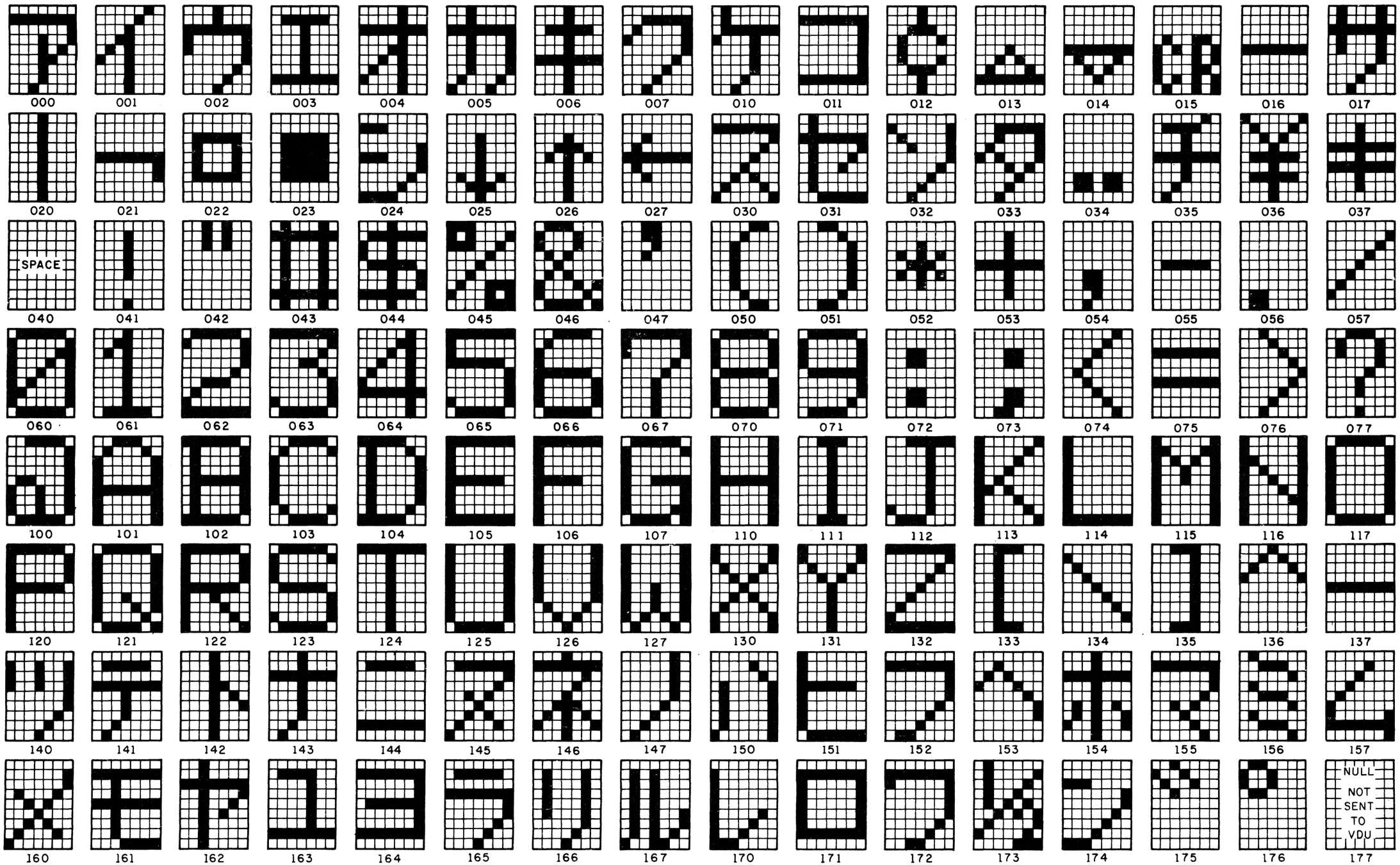
VDU CHARACTER FORMATS



5180

STANDARD ALPA-NUMERIC DISPLAY CODES

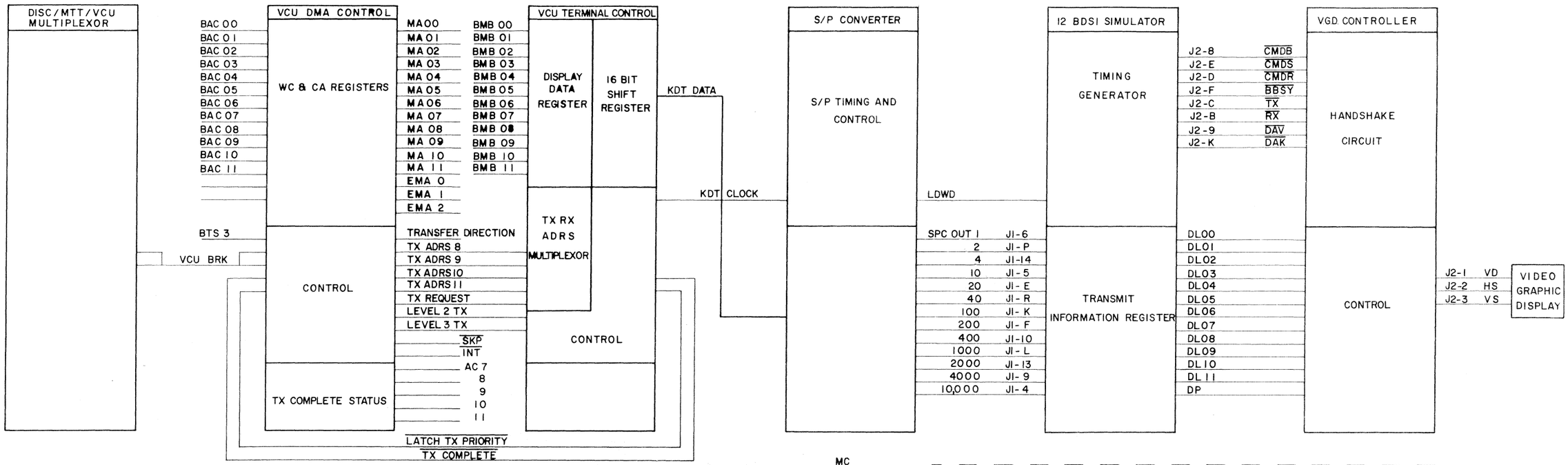
2A-64
REV 2

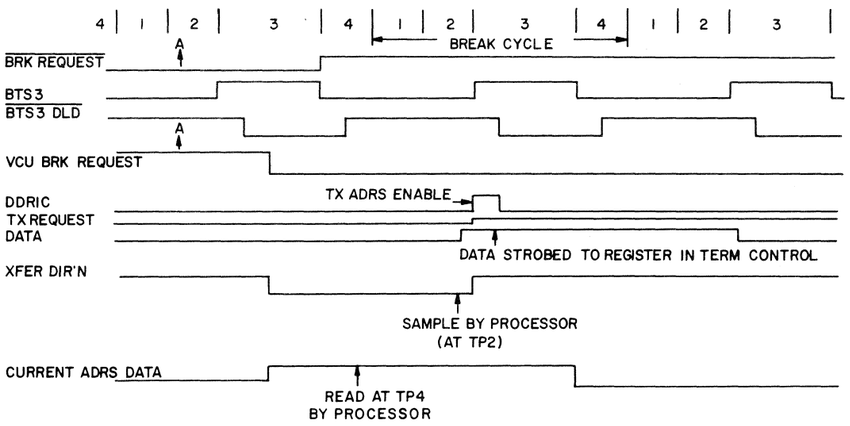


5180

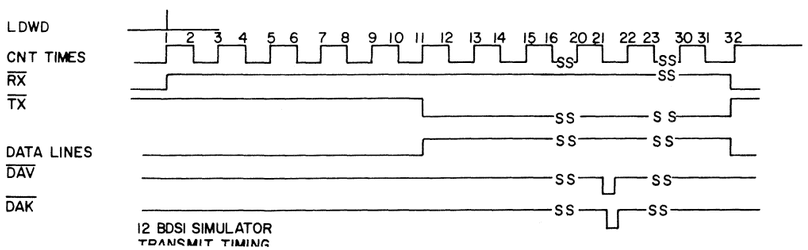
2A-65
REV 2

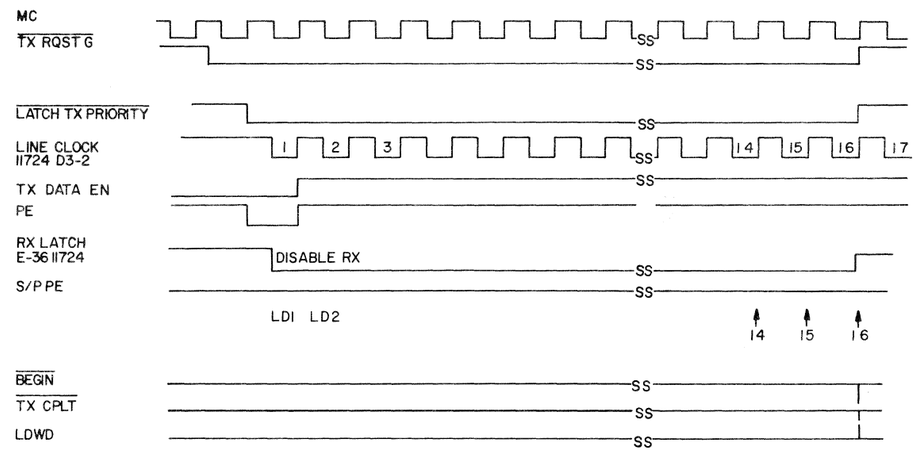
KATAKANA DISPLAY CODES



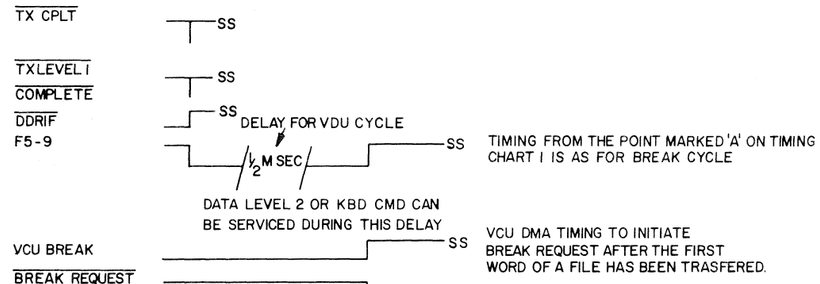


TRANSMIT BREAK CYCLE TIMING





TERMINAL CONTROL & S/P CONVERTER TRANSMIT TIMING



VIDEO KEYSTATION SUBSYSTEM
DATA TRANSMIT MODE
FIGURE 2-8B

KEY IS DEPRESSED

$\overline{DAV}$ (11725,C1,SIDE 9) ENABLES LOW

500 nSEC DELAY-$\overline{DAK}$ (11725,C1, SIDE K) ENABLES LOW

RX INITIATE (11725,A6,D3-8) ENABLES HIGH RX INITIATE FLOP (11724,D3,B2-14) SETS

DATA STROBED INTO RX INFORMATION REGISTER

500 nSEC DELAY-$\overline{DAV}$ DISABLES

500 nSEC DELAY $\overline{DAK}$ DISABLES

RX INITIATE DISABLES

RX/TX FLOP (11724,D5,F2-5) SETS ONLY IF RX LATCH (11724,C4,E3-6) IS RESET

SHIFT REGISTER CLOCK ENABLES (11724,D6,D2-11)

RX INITIATE FLOP RESETS

A11 TRANSMIT MODE SIGNALS DISABLE

KYSTN DATA DRIVER ENABLES

RX RQST (11835,1,C2,A11-5) ENABLES HIGH

RX RQST FLOP (11835,3,B4,E10-9) SETS WITH THE LEADING EDGE OF $\overline{MC}$ (11835,3,C2,E4-9) ONLY IF TX RQST FLOP IS SET.

SELECT LINE (11835,3,4C,E10-5) IS HIGH

$\overline{LATCH\ RX\ PRIORITY}$ (11835,3,4C,F10-4) ENABLES LOW

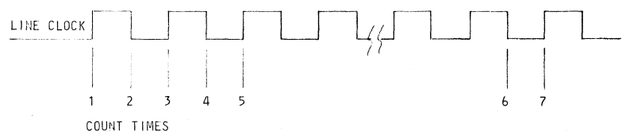
THE OUTPUT OF THE PRIORITY CHIP (11835,1,C2,A11) REFLECTS THE HIGHEST PRIORITY KYBD REQUESTING AN INTRPT. THE OUTPUT PARTIALLY ENABLES THE RELEVANT CLOCK & DATA LINES.

RX ADRS BITS (11835,3,D4,E12-4) ENABLE.

RX LATCH SETS

ABORT (11724,B2,C2-10) BEGINS TIMING OUT

THE RISING EDGE OF THE LINE CLOCK IS USED TO CLOCK THE VCU TERMINAL CONTROL SHIFT REGISTER. THE FALLING EDGE IS USED TO CLOCK THE S/P CONVERTER SHIFT REGISTER. THE SEQUENCE IS AS FOLLOWS.



AT COUNT TIME 1: THE LINE CLOCK ENABLES & THE VCU TERMINAL CONTROL LOADS WHATEVER DATA THE KYSTN DATA LINE HAPPENS TO PRESENT.

AT COUNT TIME 2: THE S/P CONVERTER PRESENTS THE FIRST BIT OF DATA ON THE KYSTN DATA LINE.

AT COUNT TIME 3: THE VCU TERMINAL CONTROL LOADS THE FIRST BIT OF DATA INTO THE 16 BIT SHIFT REGISTER.

AT COUNT TIME 4: THE S/P CONVERTER PRESENTS THE 2nd BIT OF DATA ON THE KEYSTATION DATA LINE.

AT COUNT TIME 5: THE VCU TERMINAL CONTROL LOADS THE 2nd BIT OF DATA INTO THE 16 BIT SHIFT REGISTER.
THIS SEQUENCE CONTINUES UNTIL 16 BITS OF DATA HAVE BEEN TRANSFERED TO THE VCU TERMINAL CONTROL.

AT COUNT TIME 6: S/P BIT 17 DECODER (11724,B2,E3-11) ENABLES LOW

$\overline{RESET}$ (11724,B2,C2-7) ENABLES LOW FOR 200 nSEC

BIT CNTR (11724,B4,F3-11) RESETS.

16 TH BIT FLOP (11724,B3,E2-5) RESETS

ABORT RESETS

RX LATCH RESETS

COUNT TIME 7

VCU TERMINAL CONTROL BIT 17 DECODER (11835,3,A2,F5-8) ENABLES LOW

$\overline{BEGIN}$ (11835,3,A3,E6-2) ENABLES LOW FOR 200 nSEC

RX RQST FLOP RESETS

SR MODE FLOP RESETS

LD RX INFO (11835,3,B2,E9-3) ENABLES HIGH FOR 200 NSEC

RX DATA REG (11835,4,B4, E2 & C4) ARE LOADED.

$\overline{INT}$ (11835,4,B3,B1-11) ENABLES LOW.

END

WHEN $\overline{INT}$ ENABLES THE CPU RESPONDS WITH IOT COMMANDS TO READ THE ADRS AND DATA FROM THE KYBD.

IN ORDER TO LOCATE A SIGNAL NAMED IN THE FLOW FIND THE FIRST PLACE IT IS USED. THEN USE THE DIAGRAM TO DECODE THE LOCATOR.

RX RQST FLOP (11835, 3, B4, E10-9)

- CHIP LOCATION & OUTPUT PIN
- LOCATION ON LOGIC DIAGRAM
- LOGIC DIAGRAM PAGE
- LOGIC DIAGRAM & PCB NUMBER

THE LOGIC DIAGRAM PAGE NUMBER IS ONLY INCLUDED FOR MULTIPLE PAGE LOGIC DIAGRAMS.

SERIES 50 PHASE I

KEYSTATION SUBSYSTEM
RECEIVE
FLOW
FIGURE 2-9A