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PRINTED CIRCUITS

CONTROL DATA INSTITUTE CONTROL DATA CORPORATION

1604 SERIES PRINTED CIRCUITS

FOR TRAINING PURPOSES ONLY

CONTROL DATA INSTITUTE
CONTROL DATA CORPORATION

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This manual was prepared for training purposes and does not contain all the card types used in Control Data computers.

For a complete listing of printed circuit cards, refer to Printed Circuits Manual, Volumes I & II, publications number 60042900.

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CONTENTS

THEORY OF CONTROL DATA LOGIC

The basic logic building block is a single inverter transistor circuit, represented on logic diagrams by a rectangle. This circuit uses the 180° phase shift of a grounded emitter amplifier to produce an inversion between input and output. Two circuits may be connected to form a bi-stable flip-flop.

The voltage levels used in the logic are -3v and -0.5v, representing "1" and "0" respectively. The single inverter circuit inverts these signals; a -3v input becomes a -0.5v output, and vice versa.

Control Data logic circuits are mounted on 2 1/2 by 2 1/8 inch printed circuit cards (figure 1). Each card is equipped with a 15-pin male connector for plugging into the equipment chassis.

The logic cards used are Single Inverter, Double Inverter, and Flip-Flop, designated 10 series, 20 series, and 30 series, respectively. On most cards the second digit denotes the number of inputs to each circuit.

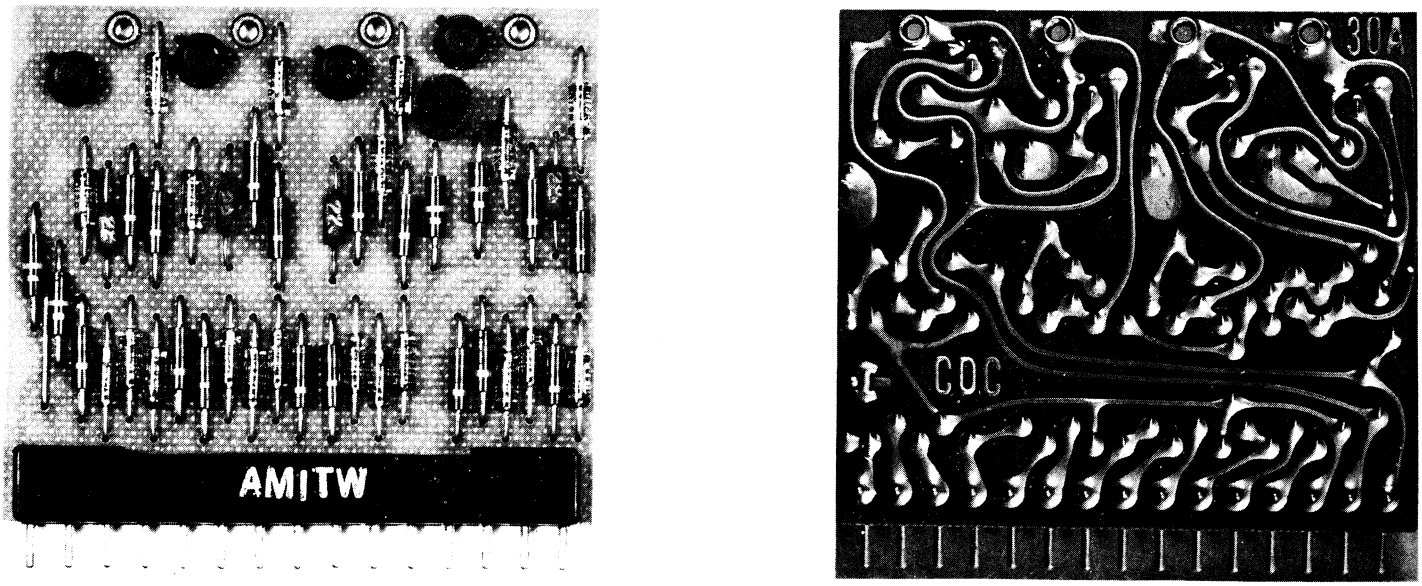


Figure 1. Control Data Printed Circuit Card

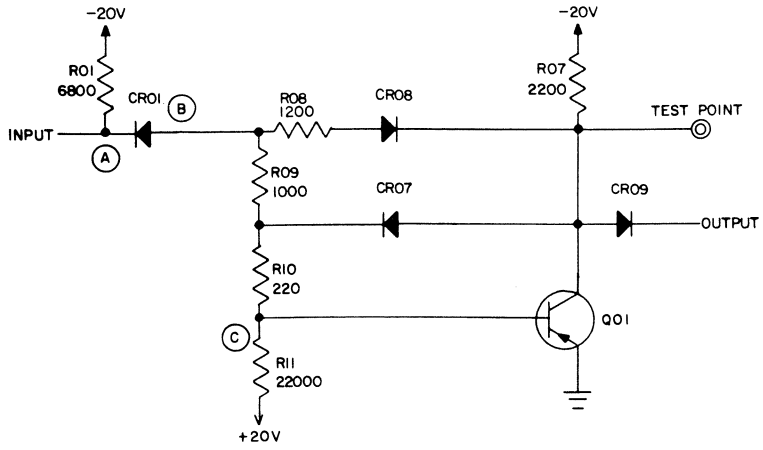
For example, a 14 card is a single inverter with 4 inputs. A 22 card contains two separate inverter circuits, each having two inputs. A 31 card contains two inverter circuits connected to form a flip-flop, each circuit having one input.

In numbering components and designating circuit locations, a diode might be numbered CR12A or CR12B; a location might be written D26A or D26B where D refers to the chassis row, 26 to the connector number, and A or B to the circuit.

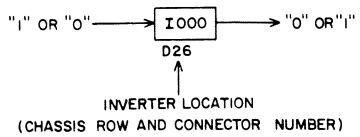
ANALYSIS OF SINGLE INVERTER

In the standard inverter circuit shown in figure 2, transistor Q01 is connected as an amplifier. The collector circuit of the transistor has two feedback loops which prevent the transistor from being driven to cutoff or saturation. Switching from one state to the other is accomplished in 10 to 80 nanoseconds.

SCHEMATIC DIAGRAM OF STANDARD INVERTER



CONVENTIONAL INVERTER SYMBOL



NOTE:
IF CARD CONTAINS TWO INVERTER CIRCUITS, THE ABOVE LOCATION WILL BE WRITTEN EITHER D26A OR D26B.

Figure 2. Standard Inverter Circuit

An input signal is applied through isolation diode CR01 to a voltage divider network composed of resistors R07, R08, R09, R10, and R11. An input signal of -0.5v (point A) results in -1.5v at point B and +0.8v at the base of Q01 (point C) so that Q01 does not conduct. CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter.

An open input circuit has the same effect as a -3v signal; point A is biased at -3v and CR01 conducts. Thus, a voltage of -1.1v appears at the base of Q01, causing it to conduct.

Transistor Q01 provides minimum beta* current gain of 25. The collector current of Q01 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output lines.

Diodes CR07 and CR08 form the feedback loops which prevent transistor Q01 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors.

When the transistor approaches cutoff, the collector approaches -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R08, R09, and R10. The base of Q01 is always held at a sufficiently negative voltage to permit some minimum conduction of Q01.

When the transistor approaches saturation, the collector approaches 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.

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* The beta current gain is the ratio of collector current to base current.

FLIP-FLOP (FF)

A FF is two single inverter circuits interconnected as shown in figure 3. (Each rectangle represents a single inverter.) One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a set input that is "1". It is placed in the "0" (cleared) state by a clear input that is "1". (Set and clear inputs are never "1" at the same time.)

The storage capability of a FF means that it remains in a state that is indicative of the last "1" input received. Specifically, if a "1" pulse is present at the set input, then the output of inverter K000 (figure 3) becomes "0". This output is applied as an input to K001 and the output becomes "1". The output of K001 is fed back to K000. When the set input returns to "0", the feedback connection between K000 and K001 permits the storage of the state to which the "1" pulse on the set input forced the FF. If the clear input later receives a "1" pulse, the output of K001 becomes "0", and the feedback input to K000 is "0". K000 furnishes a "1" output which is returned to K001 to replace the "1" pulse at the clear input.

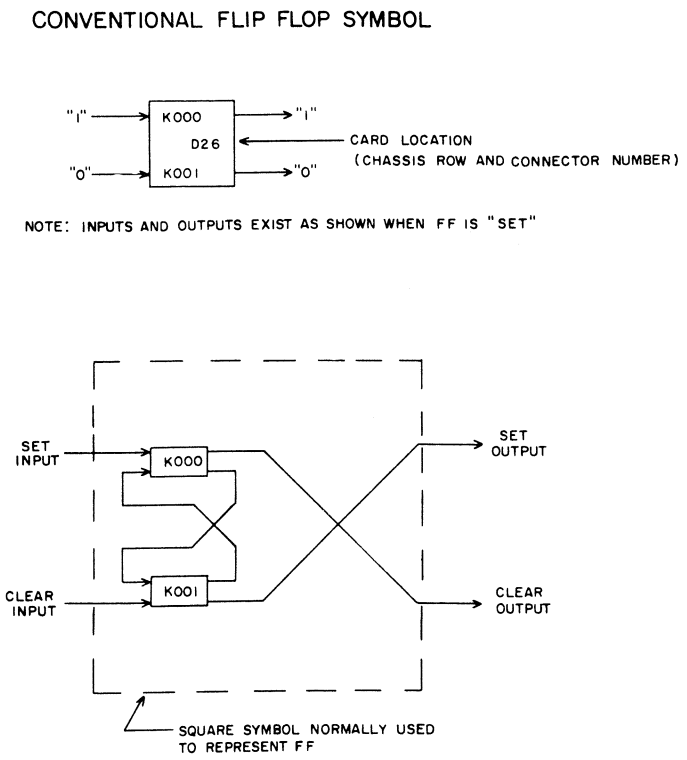


Figure 3. Interconnection of Inverters to Form a FF

When the FF is set, K001 has a "1" output, and K000 has a "0" output. When the FF is cleared, K001 has a "0" output, and K000 has a "1" output.

The conventional square symbol for a FF is used in figure 3 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

AND CIRCUIT

A three-input AND circuit is shown in figure 4. The AND gate requires all inputs to be "1". If any are "0", a "1" on another input will not be sensed.

If the transistors on cards A, B, and C are not conducting, their output diodes are biased in the reverse direction, and the resulting output signals are interpreted as being at the logical "1" level. The circuit on card D places a negative voltage on the base of the transistor so that it conducts.

If the transistor on card A, B, or C is conducting, its collector goes to approximately ground potential. Its output diode is biased in the forward direction from the -20v source on card D, and the transistor on card D is held in the nonconducting state.

OR CIRCUIT

A three-input OR circuit is shown in figure 5. An OR gate allows a "1" signal on any input to be sensed, although a "0" signal may simultaneously appear on another input. The input lines are separated by diodes; a -3v signal will not be nullified by a -0.5v signal on another input line.

If the transistor on card A, B, or C is not conducting so that the card has a "1" output, the input circuit on card D will apply a negative voltage to the base of the transistor on card D, causing it to conduct.

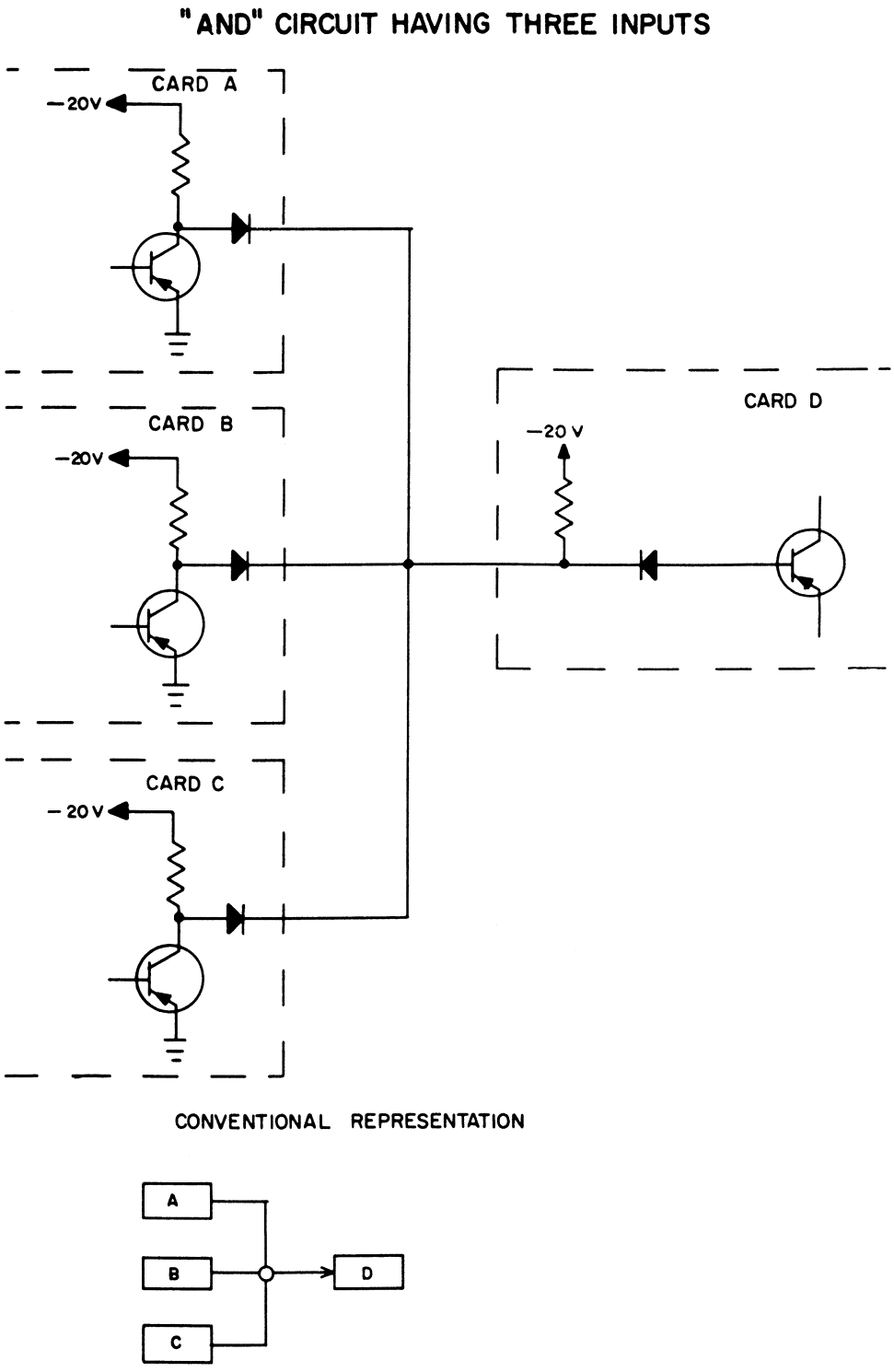


Figure 4. AND Circuit

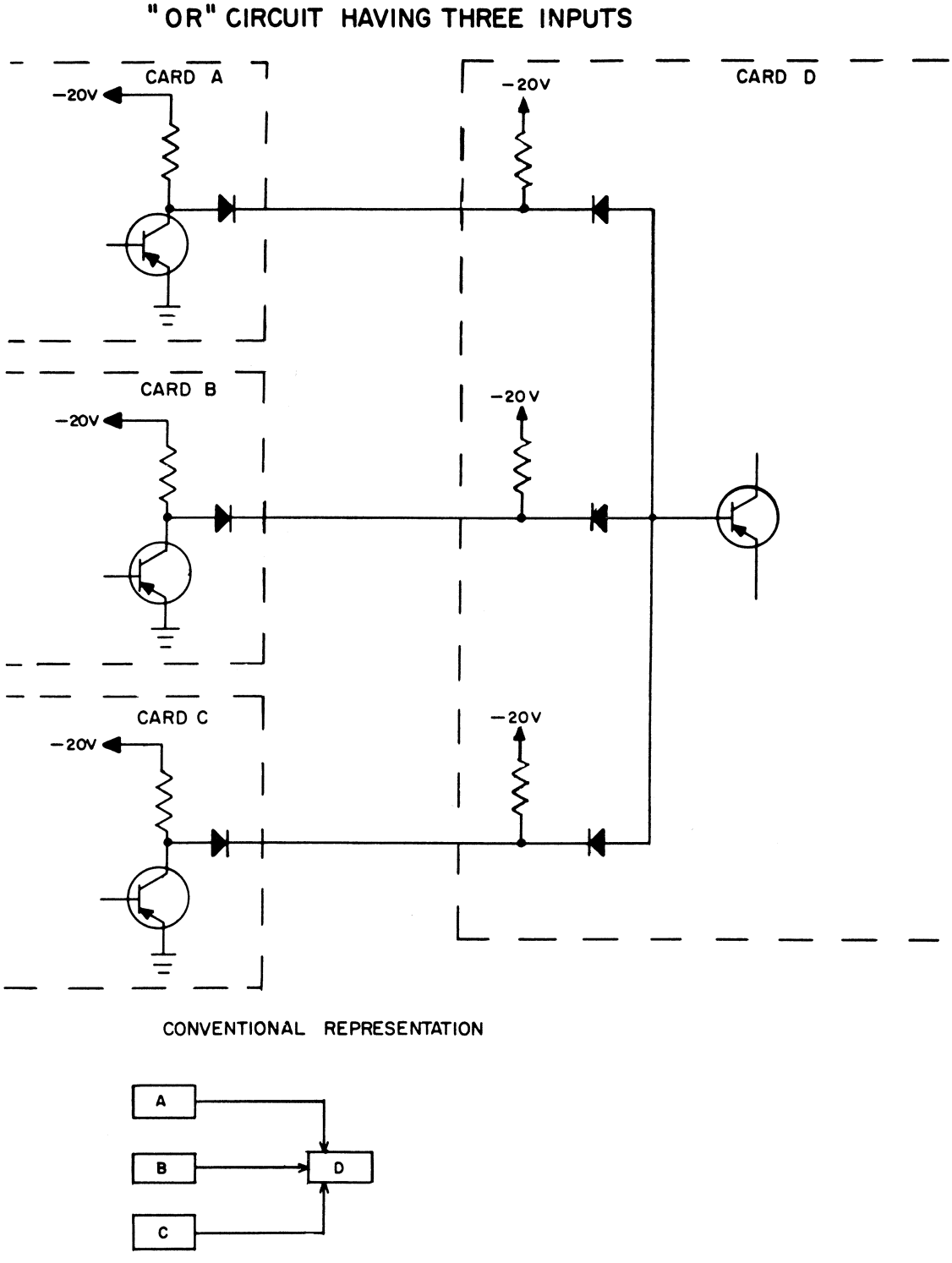


Figure 5. OR Circuit

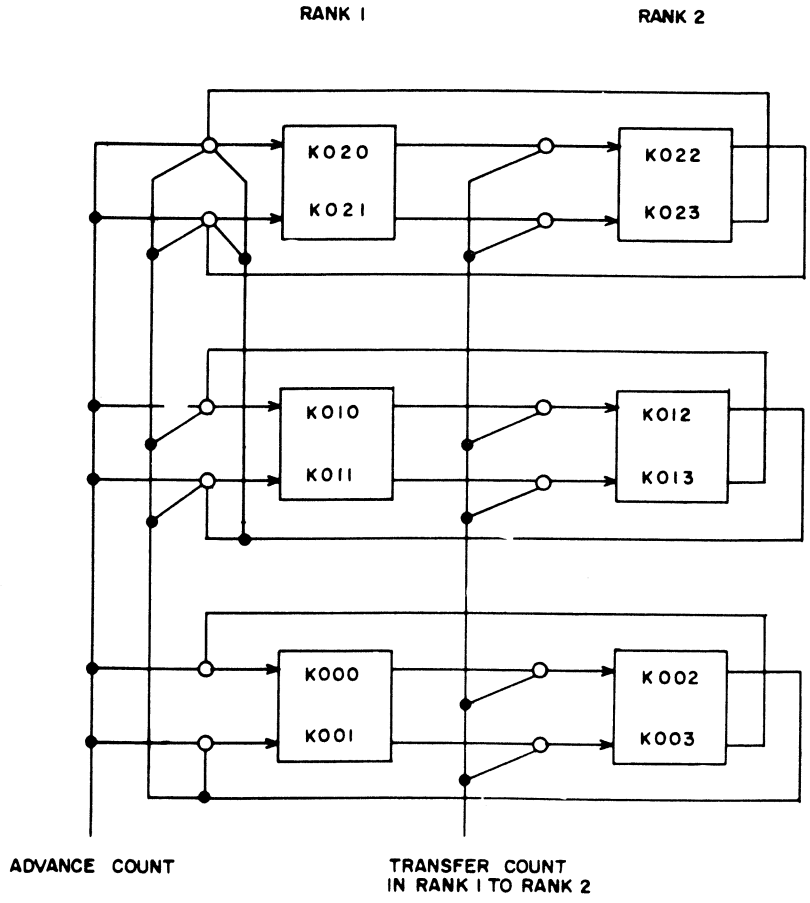
BASIC THREE-STAGE COUNTER

A counter is essentially a double rank register which increases or decreases the quantity stored, an increment at a time. The three-stage counter circuit shown in figure 6 is additive from binary 000 through 111.

A count is stored in two steps:

1) A "1" input on the advance line consecutively sets a FF in rank 1. When all three are set, the next input clears them.

2) A "1" input on the transfer line causes the FF's in rank 2 to assume the same state as the corresponding FF's in rank 1.



SET FF = 1
CLEAR FF = 0

MAXIMUM COUNT = BINARY 111, OCTAL 7
MAXIMUM COUNT REACHED WHEN ALL FF'S
IN RANK 1 ARE SET

Figure 6. Three-Stage Counter

To analyze the operation of the counter, assume that both ranks are initially cleared; the count stored is zero. The first advance command finds the AND gate to K000 enabled and therefore enters the count 001 (octal 1) into rank 1. This partially enables the AND gate to K002. The transfer command enters the count 001 into rank 2. The next advance command finds the AND gate to K001 and K010 enabled and enters the count 010 (octal 2) into rank 1. The operation continues as shown in table 1, until the count reaches 111 (octal 7), which is the highest possible count in a three-stage counter. A command sequence returns both ranks to count 000.

TABLE 1. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

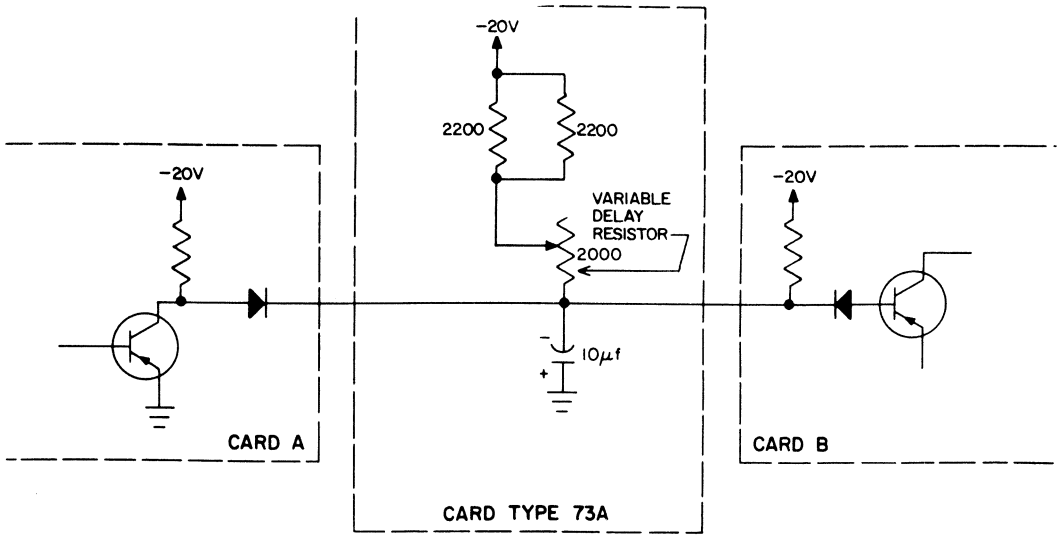
Command	Qty Stored	Rank 1			Rank 2		
	(Octal)	K02-	K01-	K00-	K02-	K01-	K00-
Initial Conditions	0	0	0	0	0	0	0
Advance	1	0	0	1	0	0	0
Transfer		0	0	1	0	0	1
Advance	2	0	1	0	0	0	1
Transfer		0	1	0	0	1	0
Advance	3	0	1	1	0	1	0
Transfer		0	1	1	0	1	1
Advance	4	1	0	0	0	1	1
Transfer		1	0	0	1	0	0
Advance	5	1	0	1	1	0	0
Transfer		1	0	1	1	0	1
Advance	6	1	1	0	1	0	1
Transfer		1	1	0	1	1	0
Advance	7	1	1	1	1	1	0
Transfer		1	1	1	1	1	1
Advance	0 (or 8)	0	0	0	0	0	0
Transfer		0	0	0	0	0	0

DELAY CIRCUIT

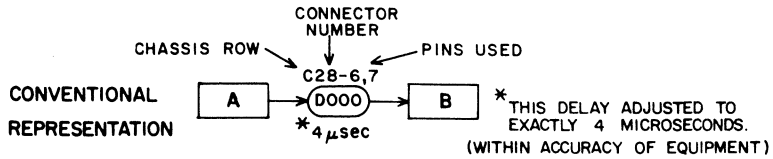
Placing a capacitor from the signal line to ground forms a delay circuit. The delay time is the time required to charge the capacitor when a -3v "1" signal appears on the line.

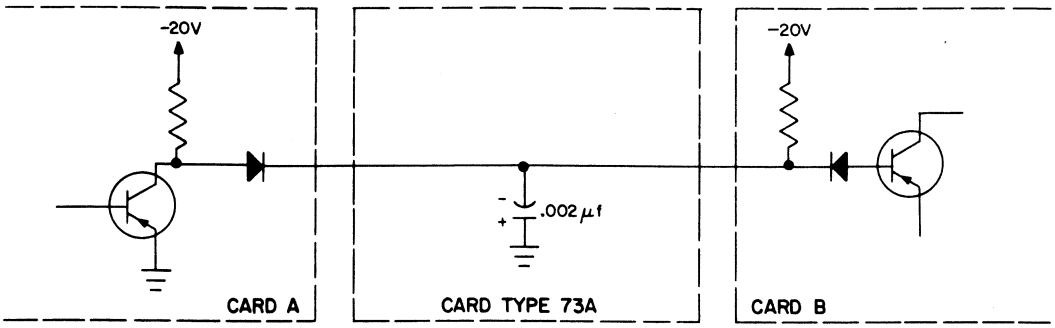
A delay is used to postpone the time at which a "1" signal is sensed by the input circuit of a card. It will have negligible effect on a "0" signal.

During the time that the transistor on card A is conducting, its collector will be at almost ground potential (figure 7). The voltage across the delay capacitor will not be more than 0.5v and will contain very little charge.



TYPICAL ADJUSTABLE DELAY INSTALLATION





TYPICAL NON-CRITICAL DELAY INSTALLATION

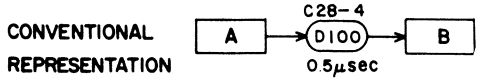
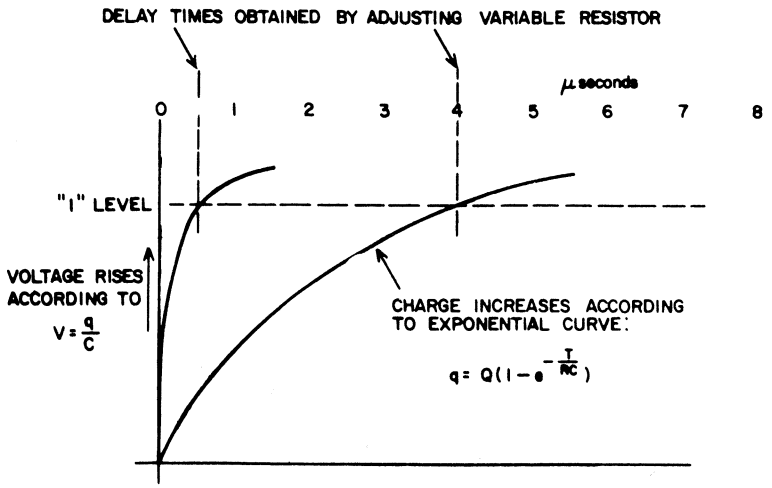


Figure 7. Typical Delay Circuits

When the output of card A switches to "1" and its transistor stops conducting, the input circuitry on card B attempts to bias the input line at the -3v level. Initially this voltage is absorbed by the uncharged delay capacitor, which gradually obtains a charge as shown in figure 8. In the case of an adjustable delay, the capacitor also receives charging current from the circuit on the 73A card.

The size of the capacitor and the rate at which it receives charging current govern the delay time. For a long delay, use a large capacitor. To increase or decrease the delay time, increase or decrease the series resistance between the capacitor and the source of charging current.



NOTE:

SYMBOL	REFERS TO:	UNITS
T	TIME	SECONDS
q	PARTIAL CAPACITOR CHARGE	COULOMBS
Q	FINAL CAPACITOR CHARGE	COULOMBS
R	SERIES RESISTANCE	OHMS
C	CAPACITANCE	FARADS
V	APPLIED POTENTIAL	VOLTS
e	NATURAL LOGARITHM BASE	PURE NUMBER 2.718, APPROX.

Figure 8. Relationship of Delay Time and Capacitor Charge Time

PULSE FORMING NETWORKS

Many circuits contain pulse forming networks, consisting of two inverters and a capacitive delay to reshape a steady "1" signal into a short "1" pulse. The leading edge network produces a pulse upon receipt of a "1" signal; the trailing edge network produces a pulse when the "1" signal ends (figure 9).

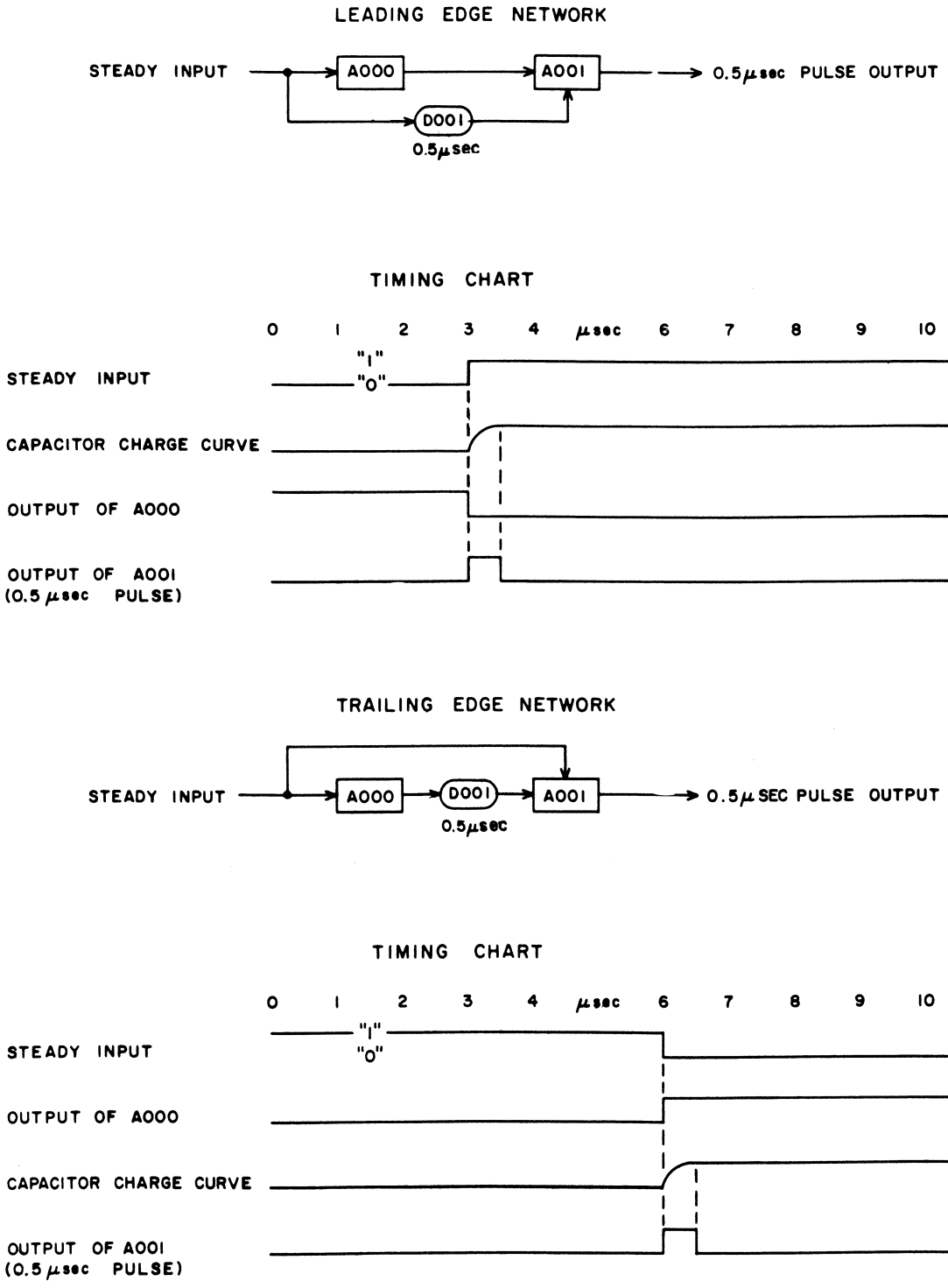


Figure 9. Pulse-Forming Networks

When a "1" input is received by a leading edge network, double inversion produces a "1" output. When the capacitor is sufficiently charged, a "1" is sent directly into A001 through an OR gate, and the output of inverter A001 switches to "0".

In the case of a trailing edge network, the steady input signal is fed directly into both inverters. When this signal goes to "0", the output of both inverters switches to "1". The "1" output of A000 does not reach A001 until the capacitor has charged sufficiently. The "1" enters A001 through an OR gate, and its output switches to "0".

TIMING CHAIN PULSE GENERATOR

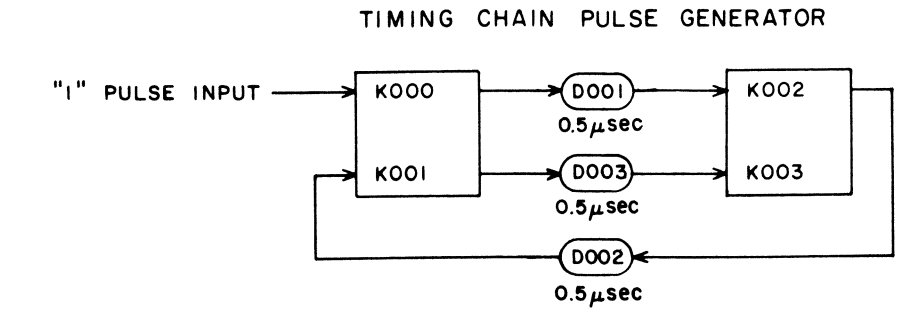
A convenient method of obtaining a series of four sequential pulses using two FF's and three delays is shown in figure 10.

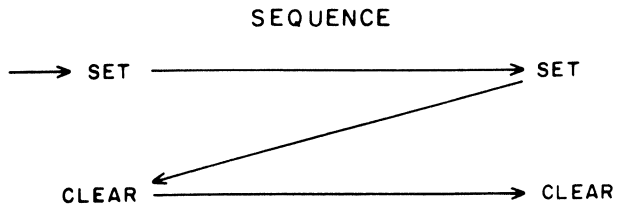
The two FF's exhibit four distinct sets of conditions at different time intervals. Initially both are in the clear state. A "1" pulse input to K000 sets K000/001, so that K001 has a "1" output. After a brief delay, this signal sets K002/003. K003 sends a "1" through a delay to K001; K000/001 is cleared. K000 sends a "1" through the third delay to K003; K002/003 is also cleared.

These four sets of conditions and the times at which they occur are:

	K000/001	K002/003
Time 0	Clear	Clear
Time 1	Set	Clear
Time 2	Set	Set
Time 3	Clear	Set
Time 0 (or 4)	Clear	Clear

The lengths of these time intervals are dependent upon the capacitive delays. In the example shown, all of the times are 0.5 usec. These may be varied.





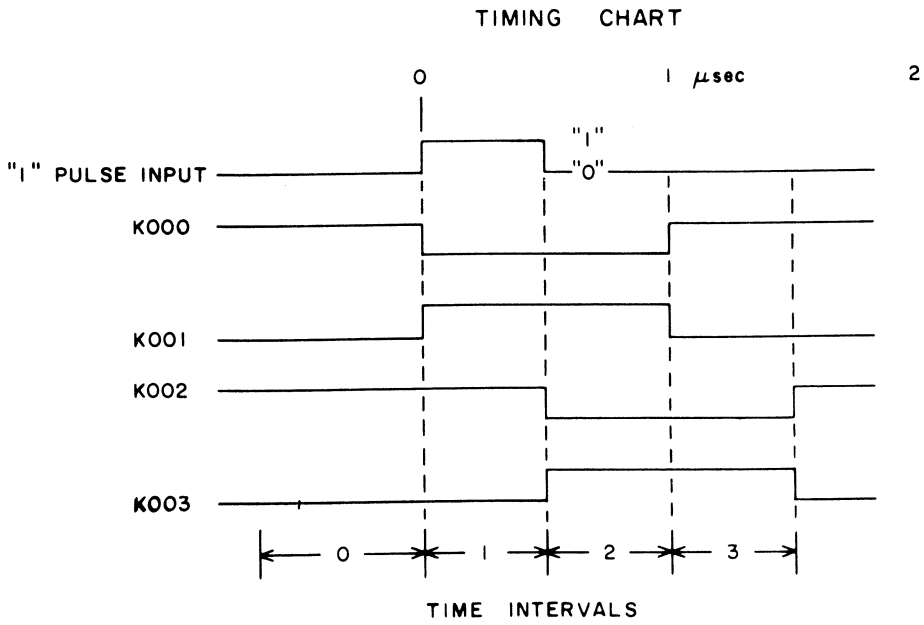


Figure 10. Pulse Generator Networks

OUTPUT/INPUT CARDS, L--- AND M--- SERIES

The output/input cards adapt the relatively low level logic voltages to the relatively high level voltages necessary for cable transmission. Card types 62 and 61, which perform this adaptation, contain three separate circuits per card, A, B, and C (figure 11).

These cards are similar to a standard inverter card in that they contain a common emitter transistor circuit. However, although these cards produce a 180° electrical phase shift, they do not function as logical inverters. Instead, they are used in pairs so that the total phase shift is 360° and the initial and final voltage levels are identical (figure 11).

Another similarity between an M--- card and a standard inverter is the fact that the card circuitry biases the transistors in their conduction state if an open circuit occurs on the card input. Thus an M--- card can be made to have a -0.5v "0" or a -3v "1" output by opening and closing a switch connecting its input to ground.

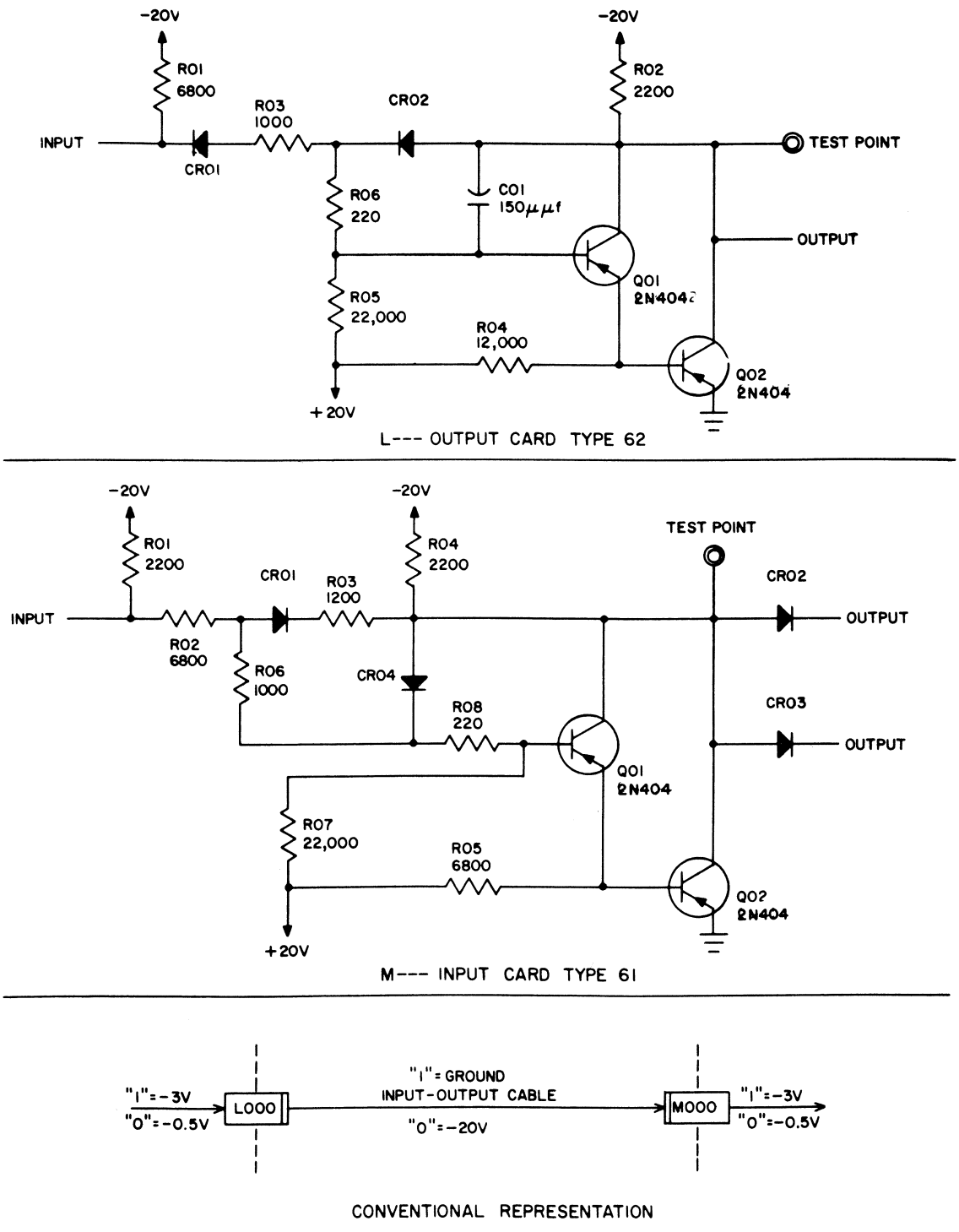
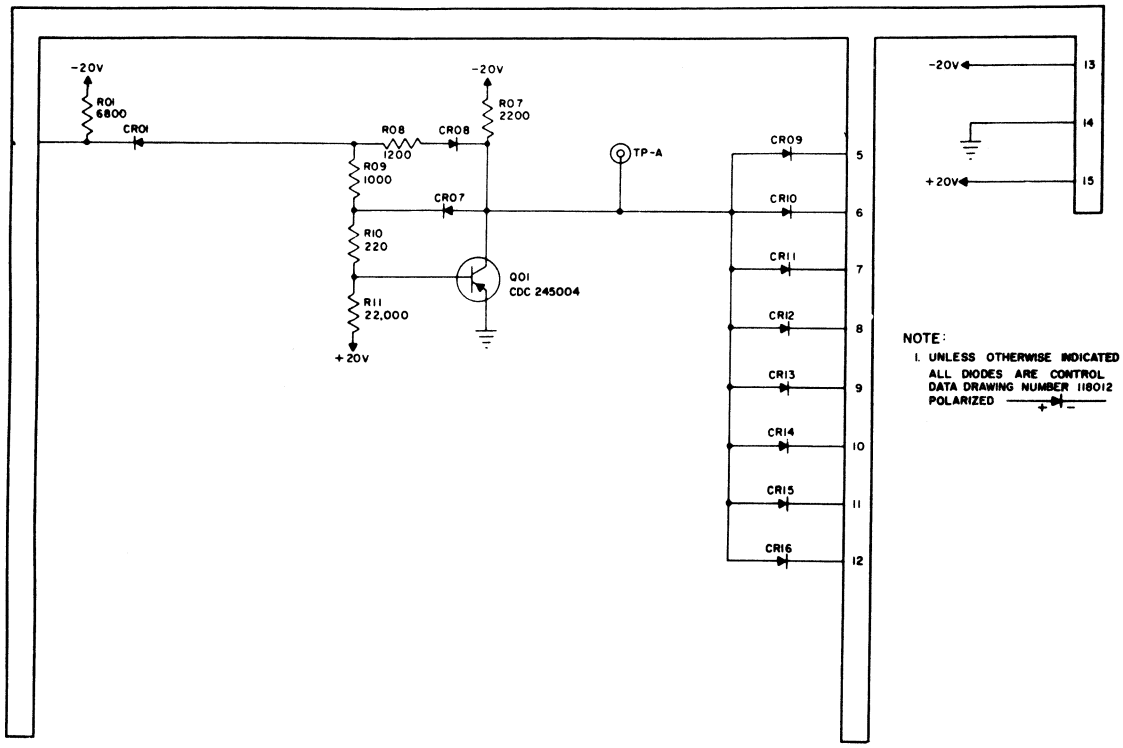
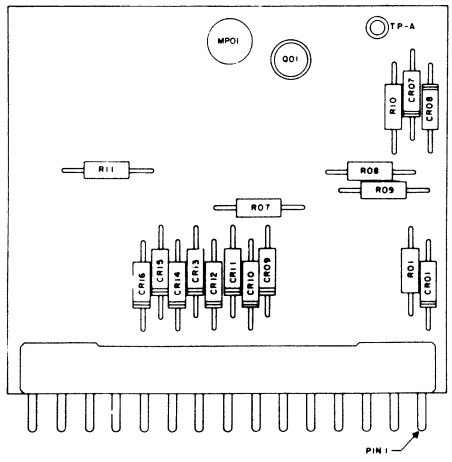


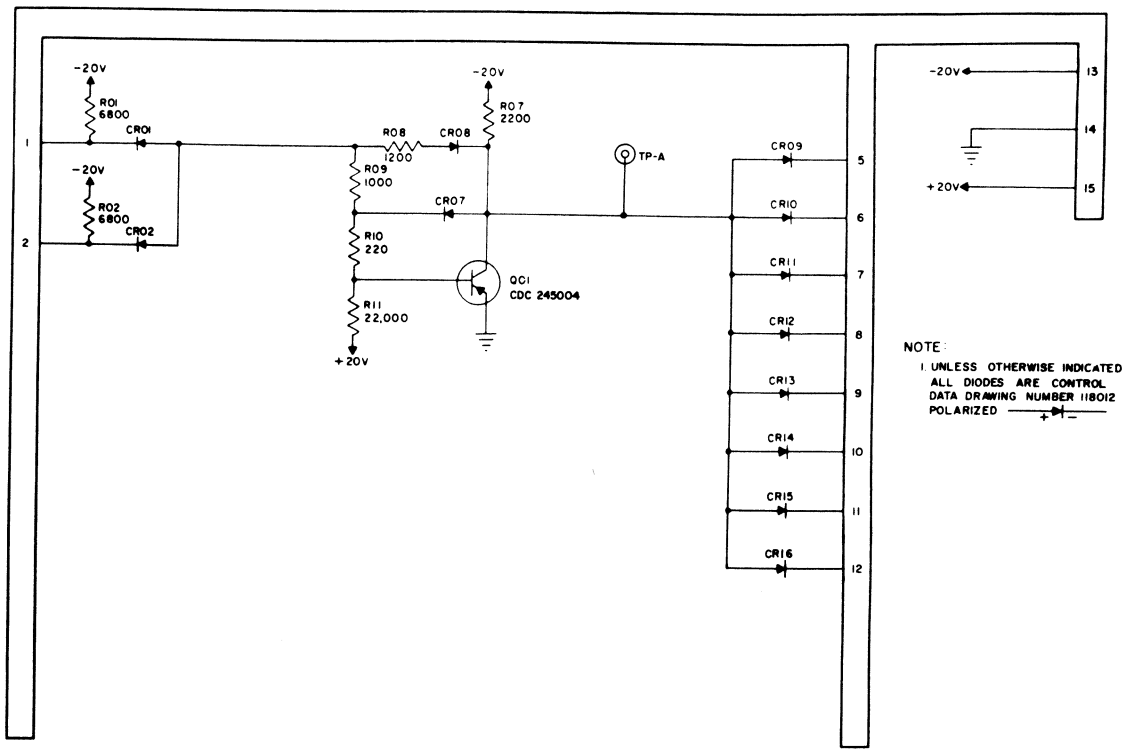
Figure 11. Input/Output Circuits

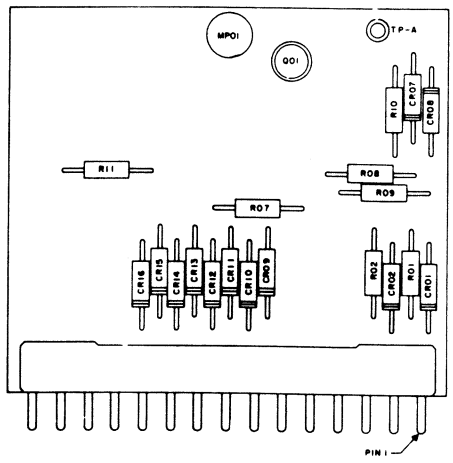
SINGLE INVERTER
11A



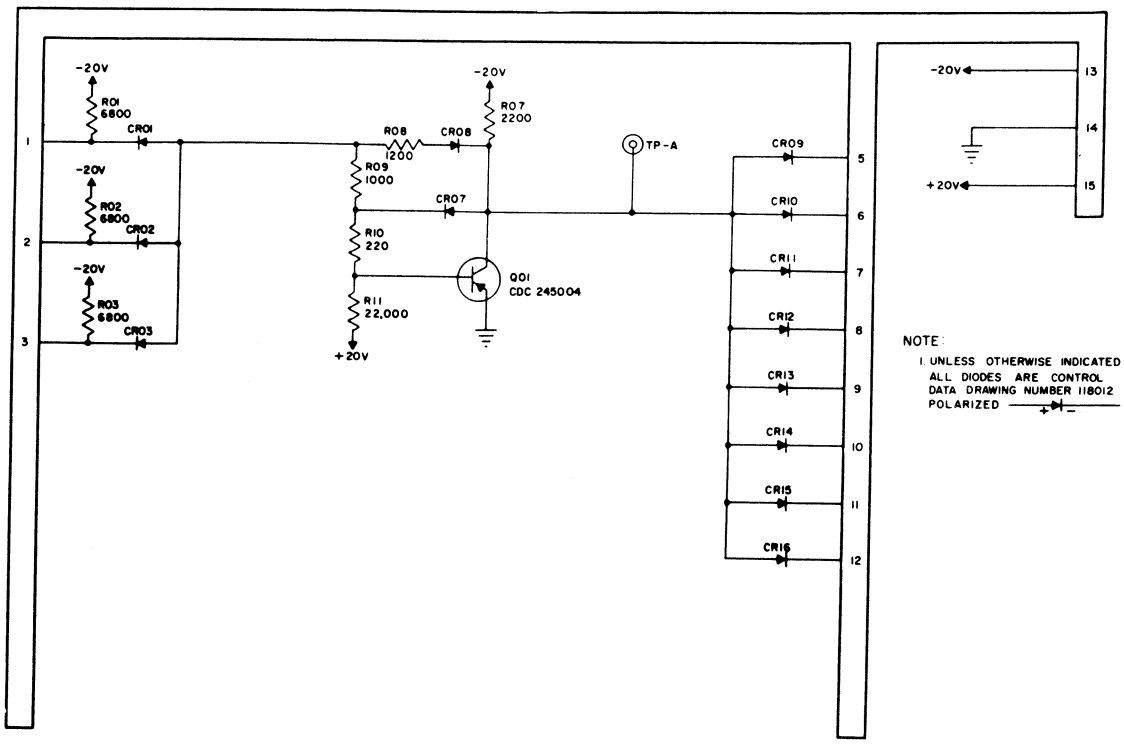


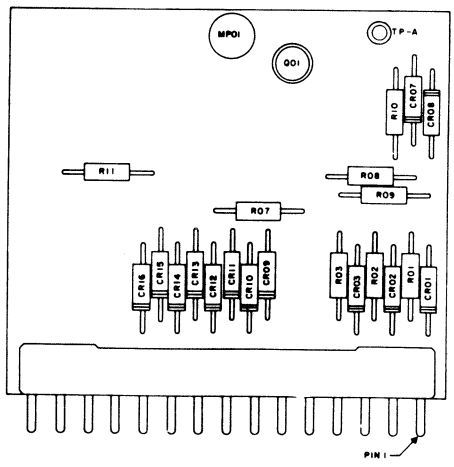
SINGLE INVERTER
12A



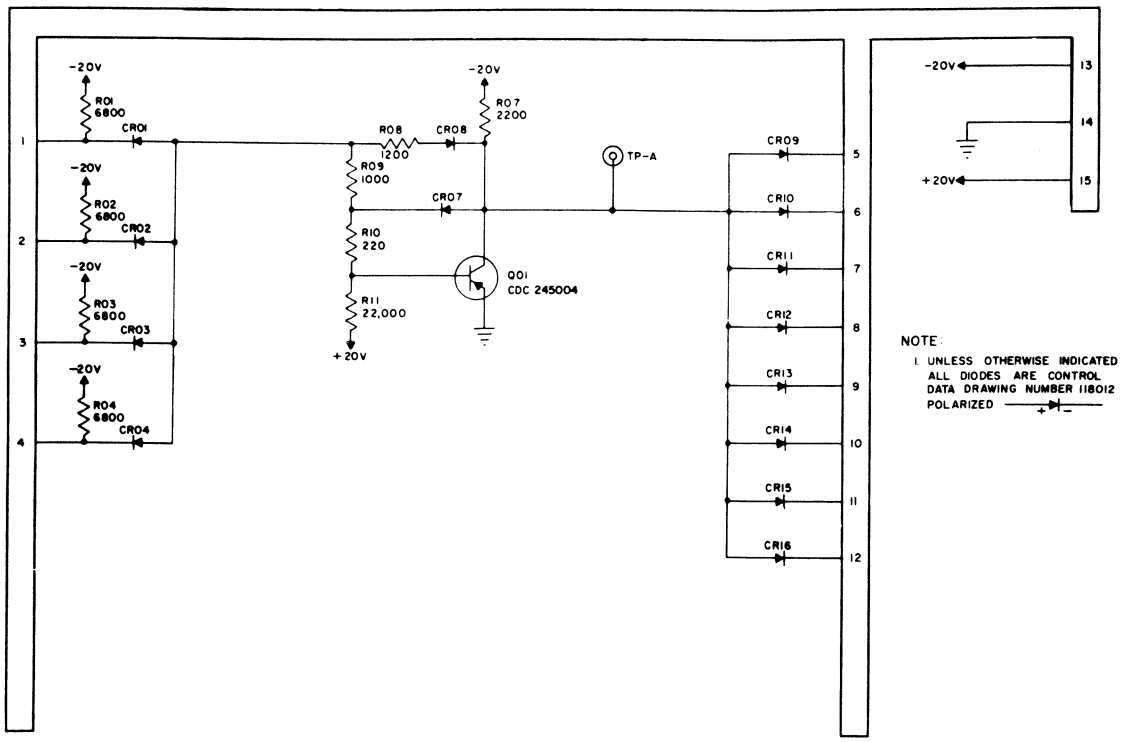


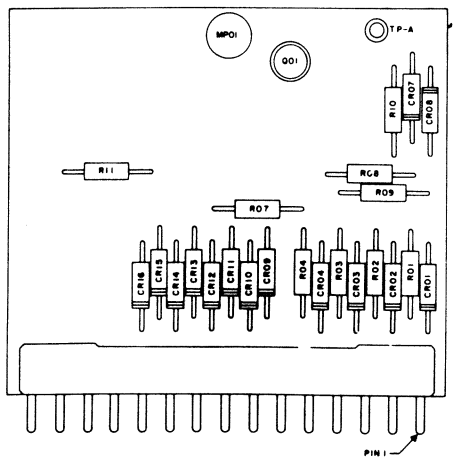
SINGLE INVERTER
13A





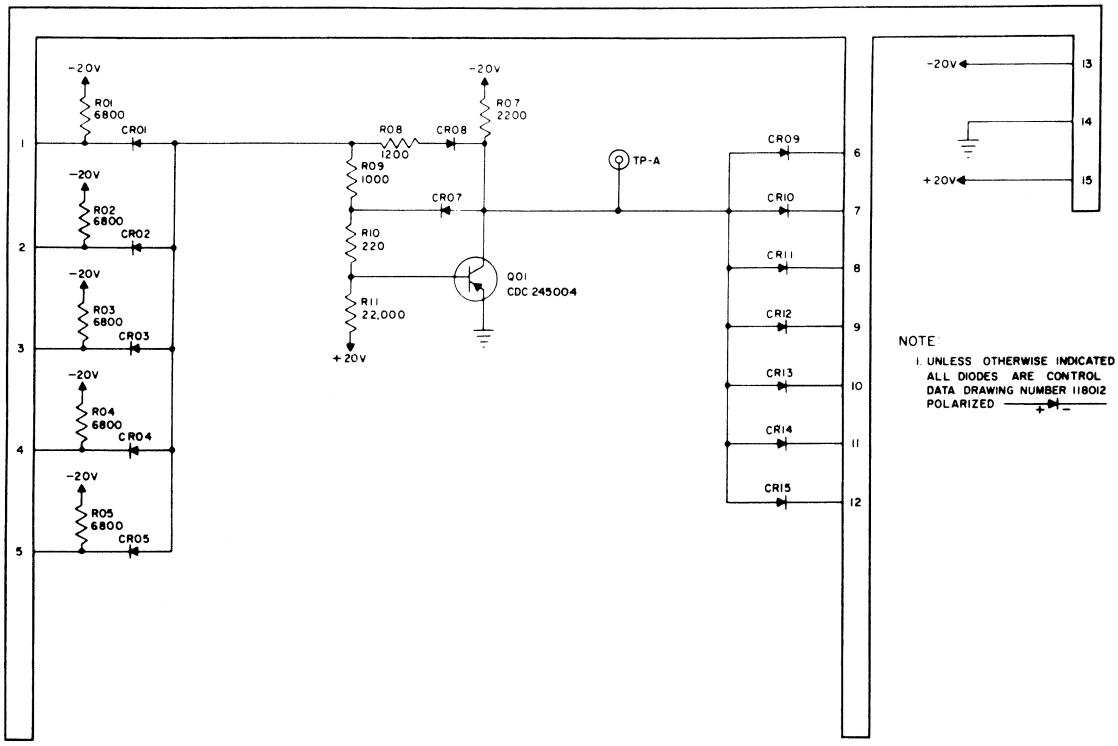
SINGLE INVERTER
14A

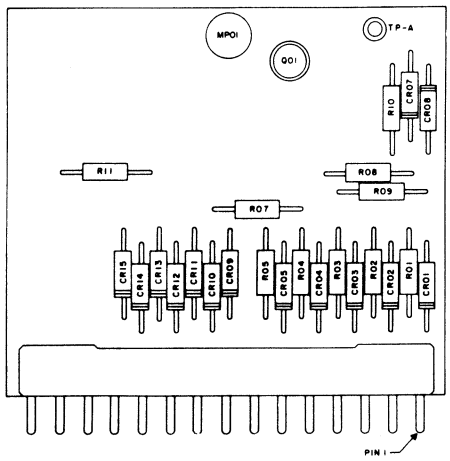




SINGLE INVERTER

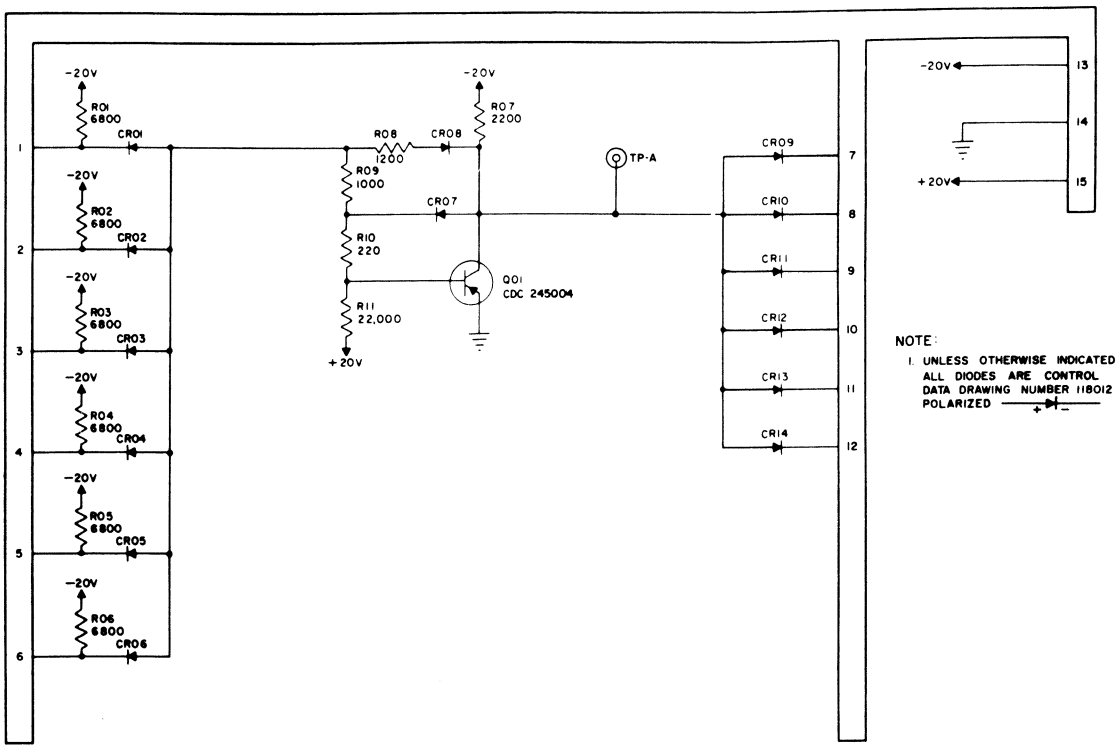
15A

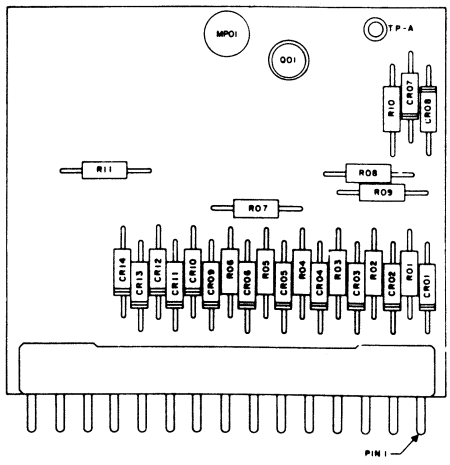




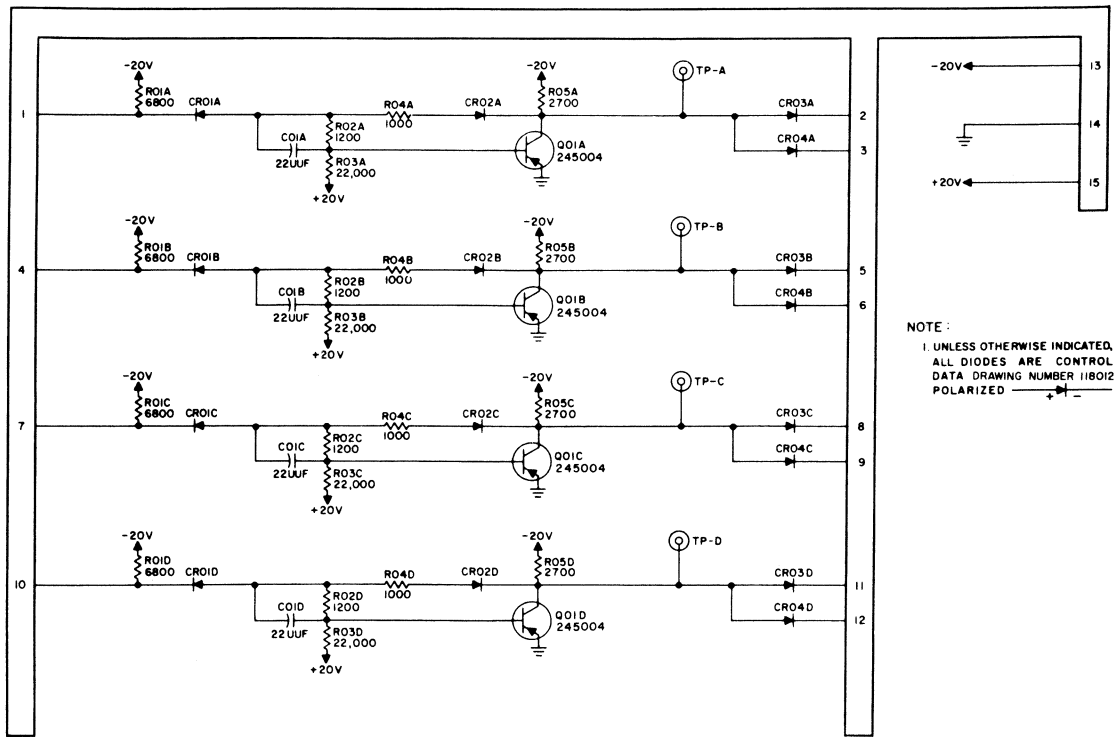
SINGLE INVERTER

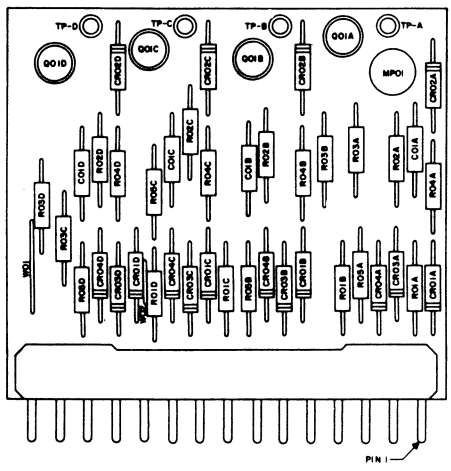
16A



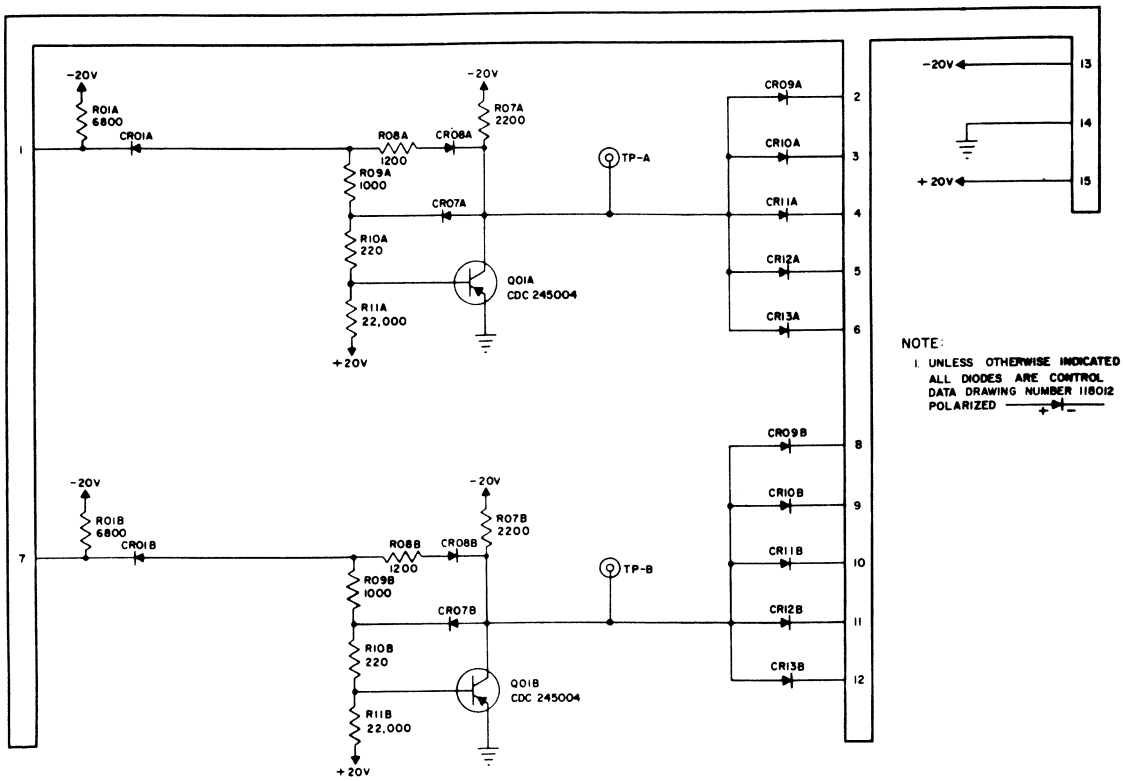


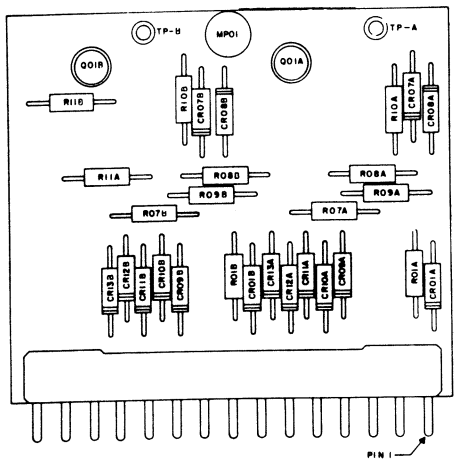
QUADRUPLE INVERTER
20A





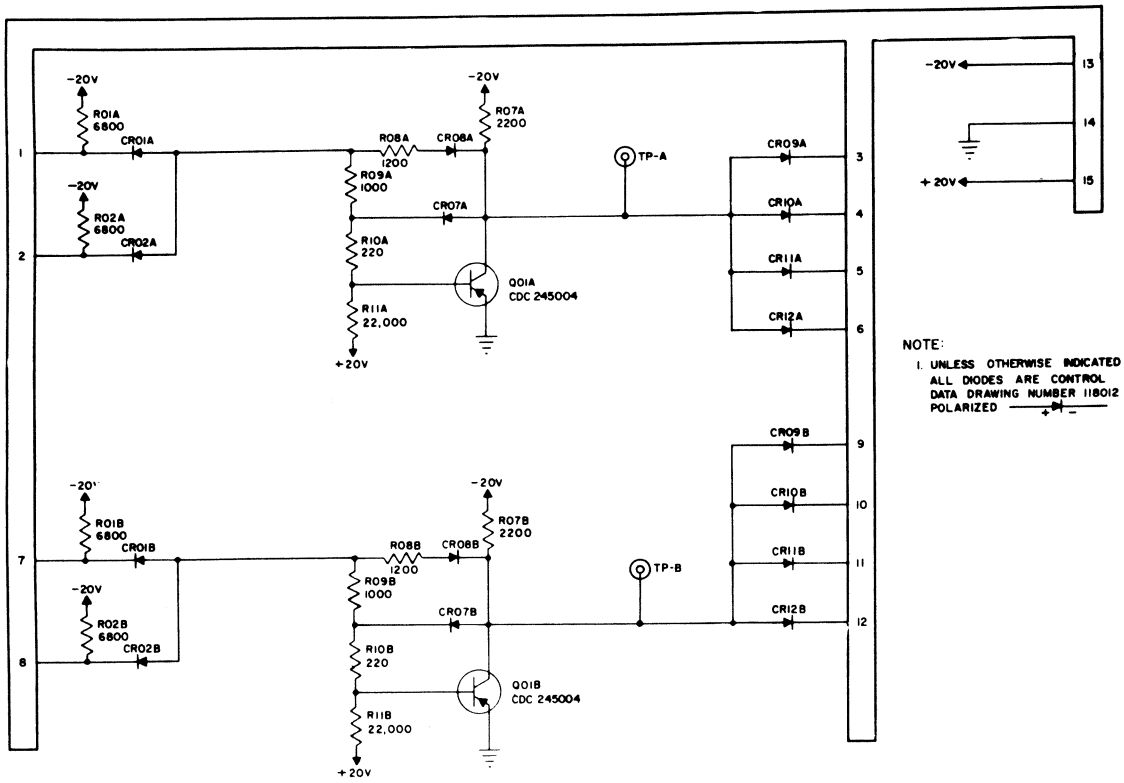
DOUBLE INVERTER
21A

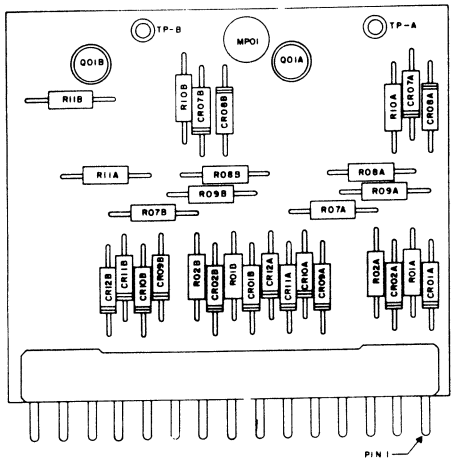




DOUBLE INVERTER

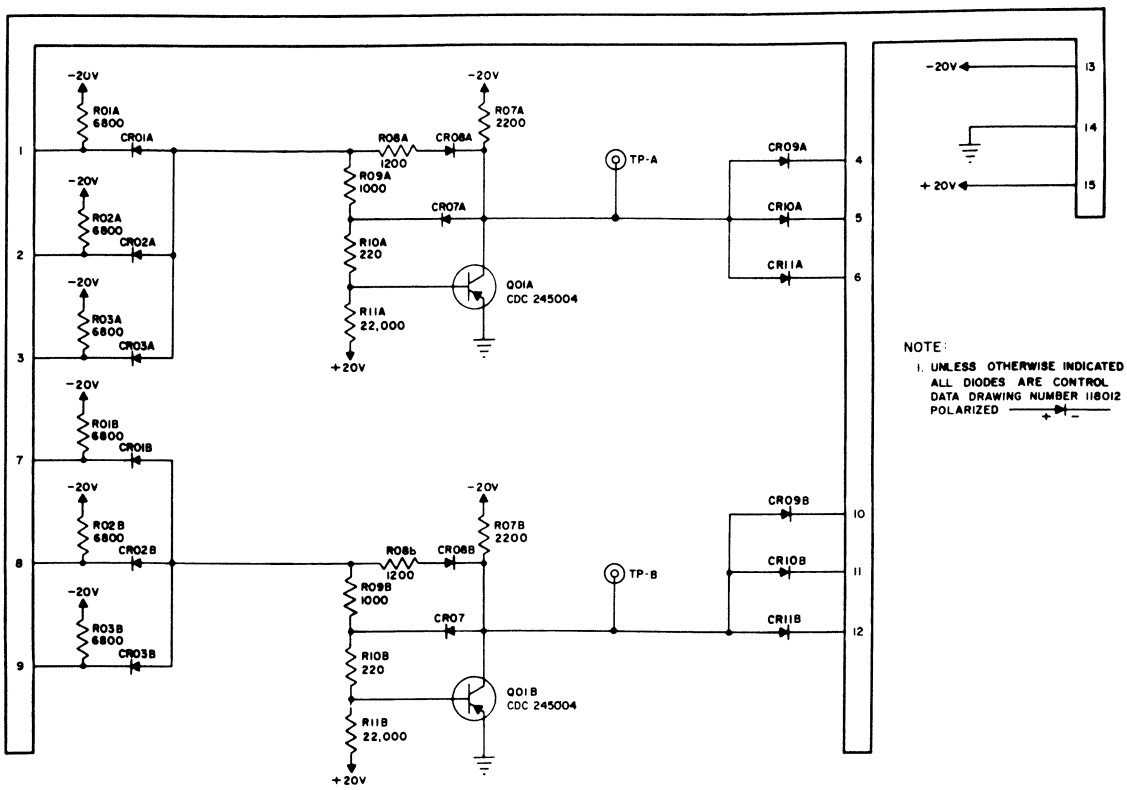
22A

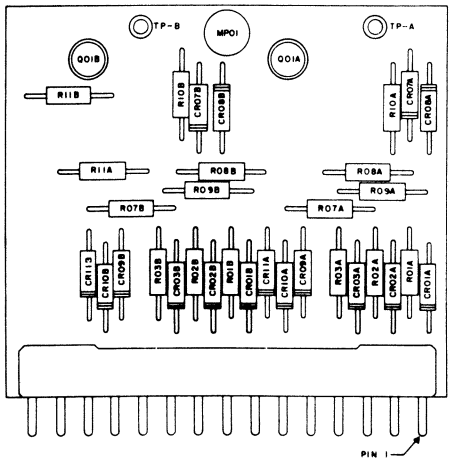




DOUBLE INVERTER

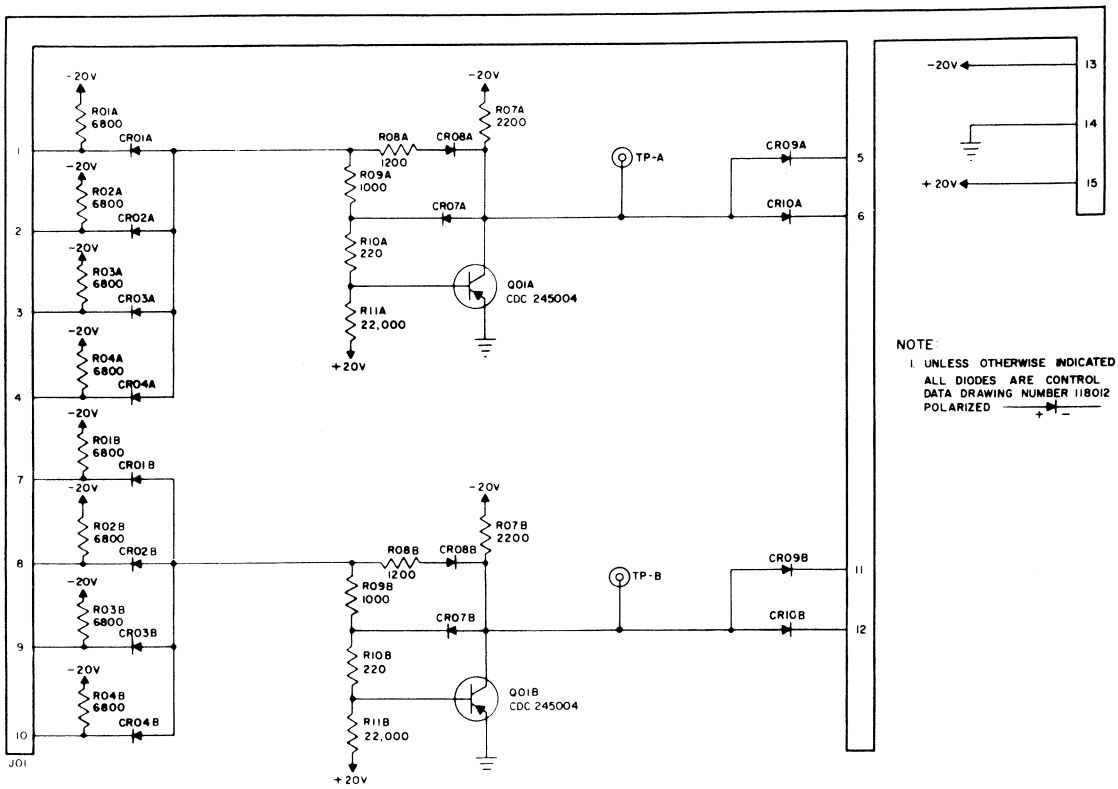
23A

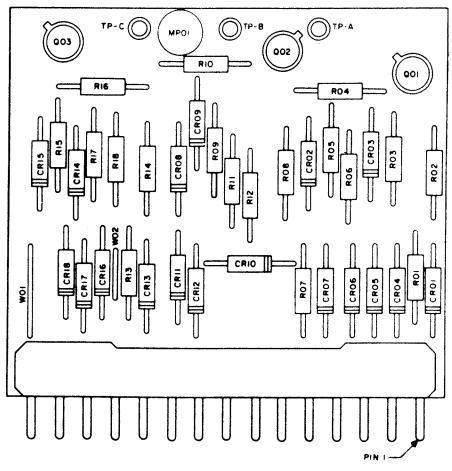




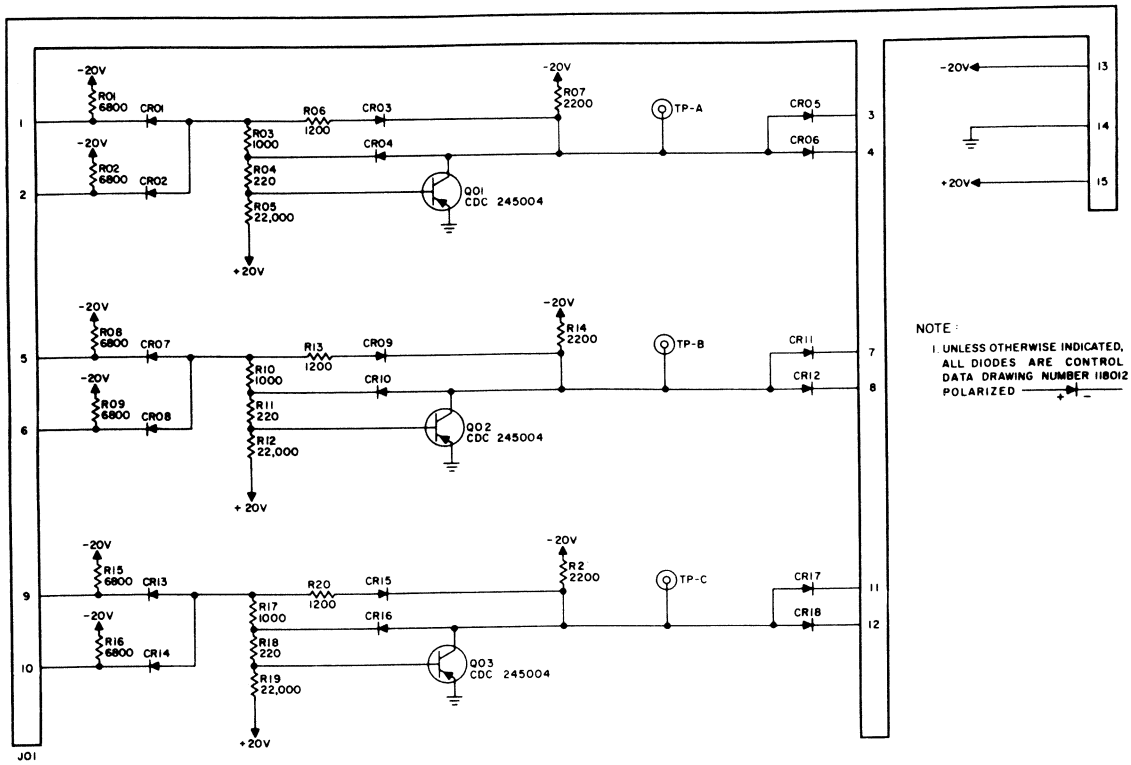
DOUBLE INVERTER

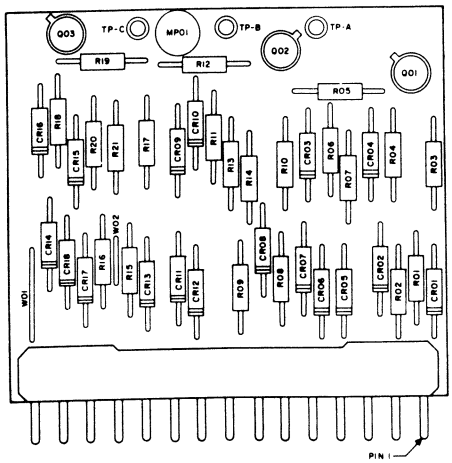
24A





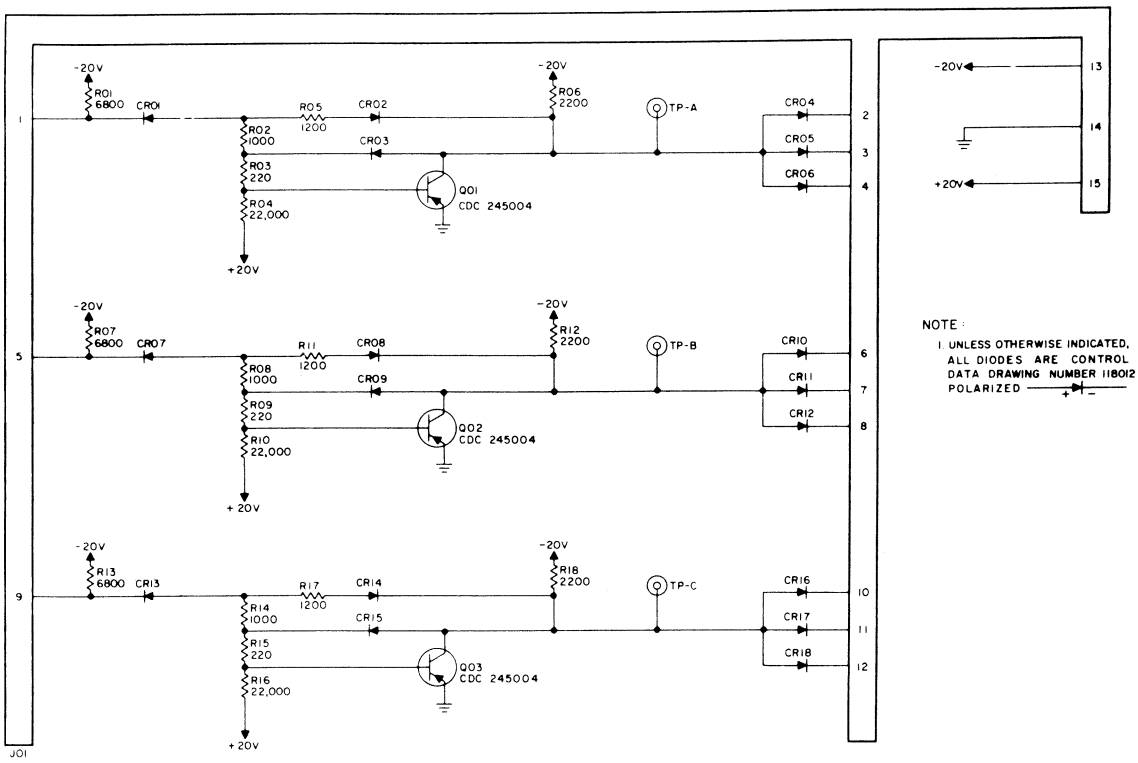
TRIPLE INVERTER
28A

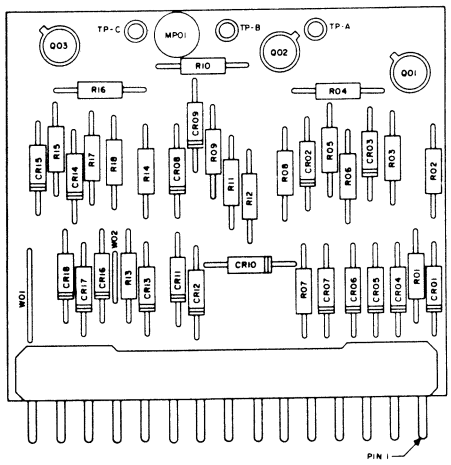




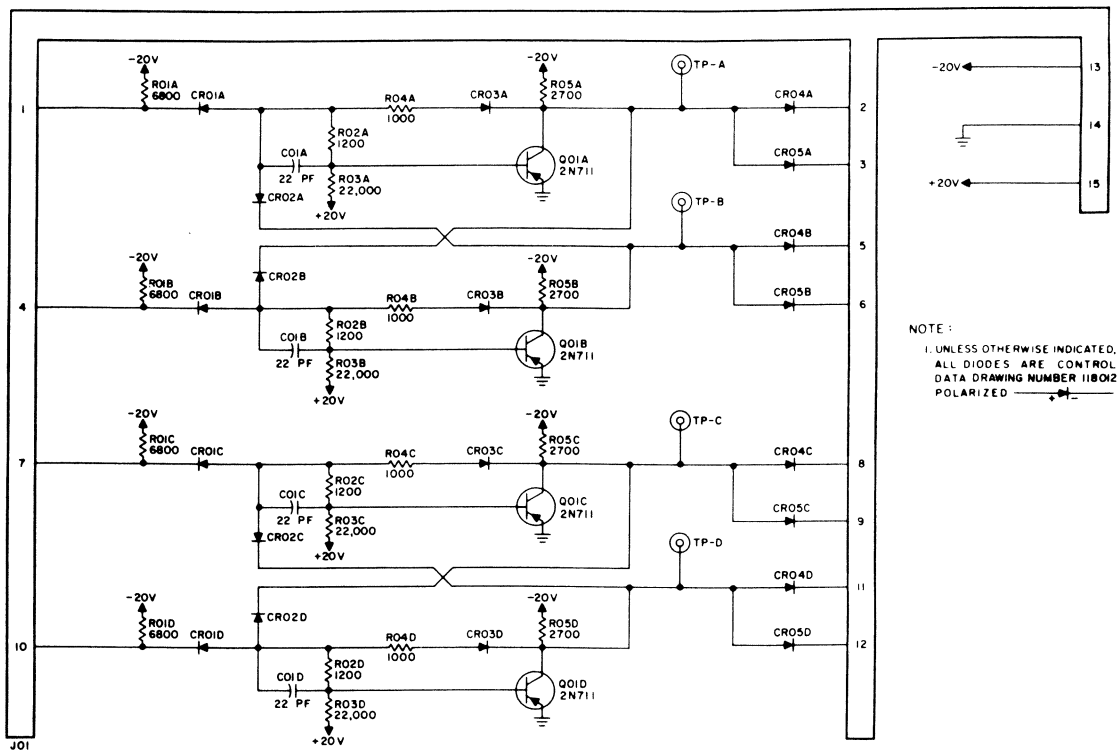
TRIPLE INVERTER

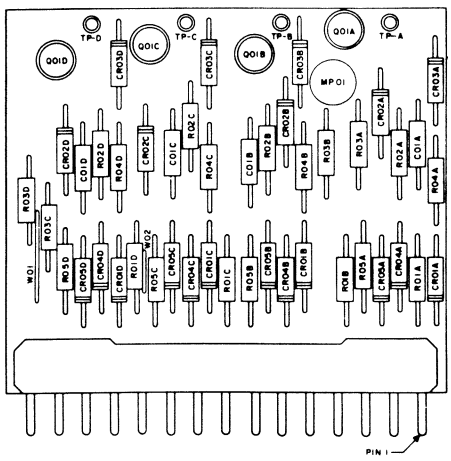
29A



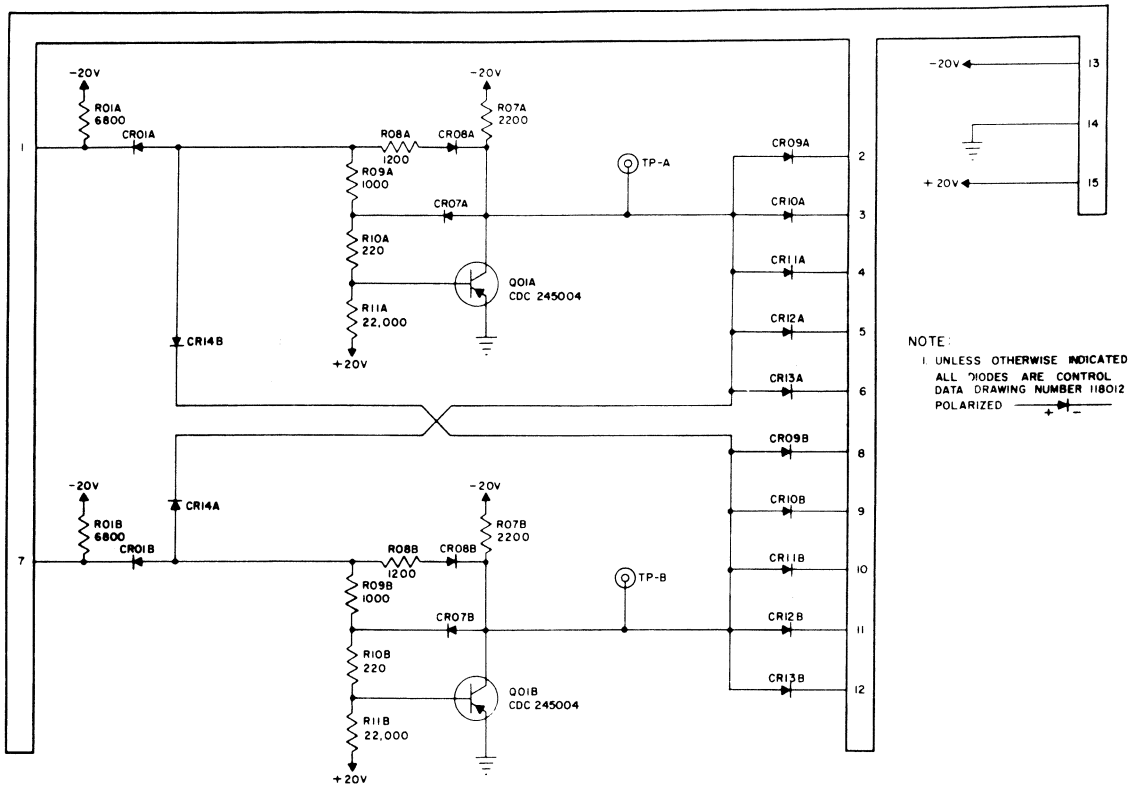


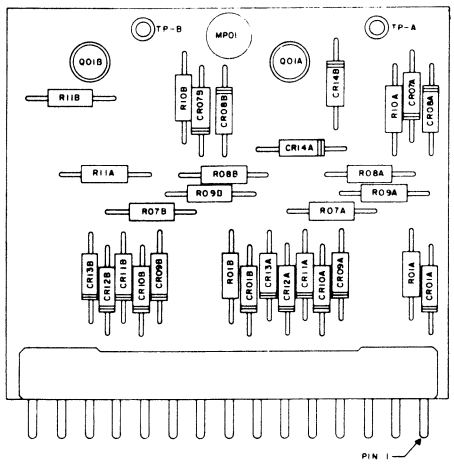
DOUBLE FLIP-FLOP
30A



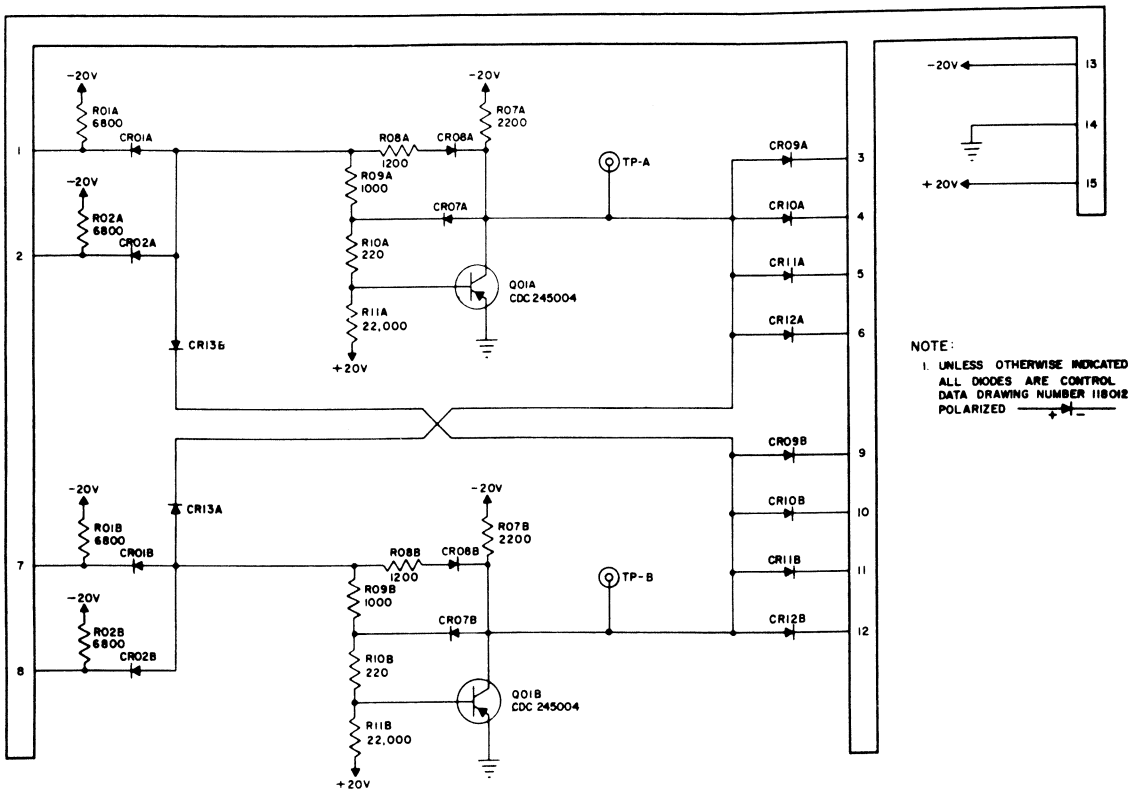


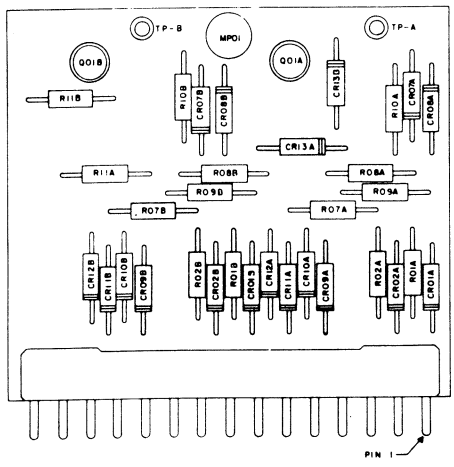
FLIP-FLOP
31A



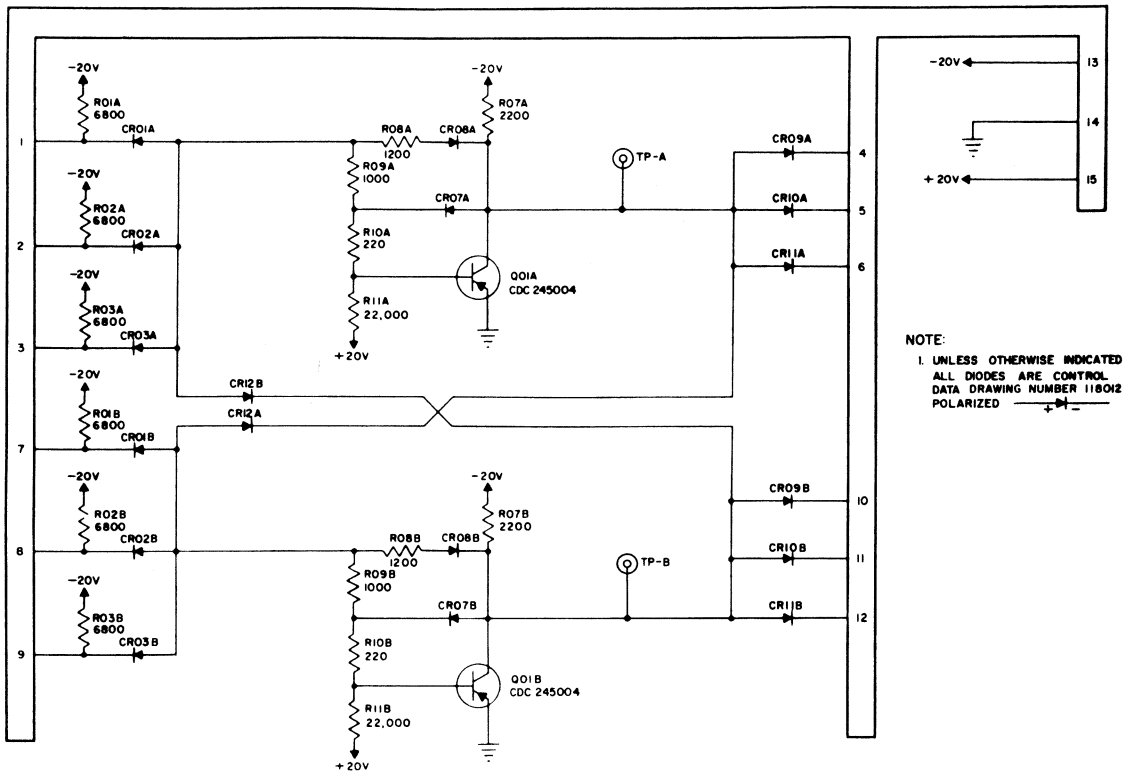


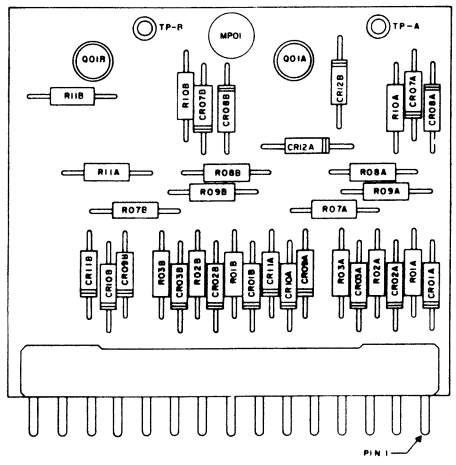
FLIP-FLOP
32A



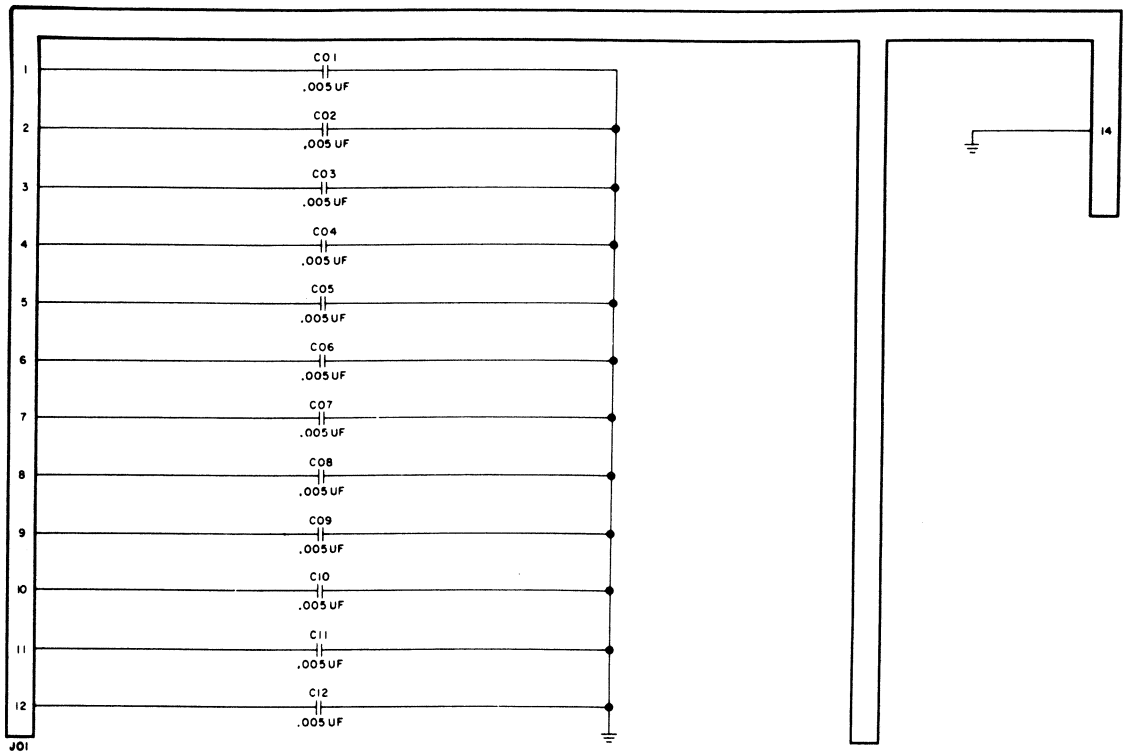


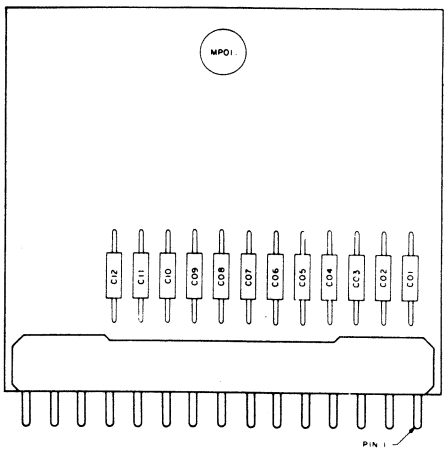
FLIP-FLOP
33A



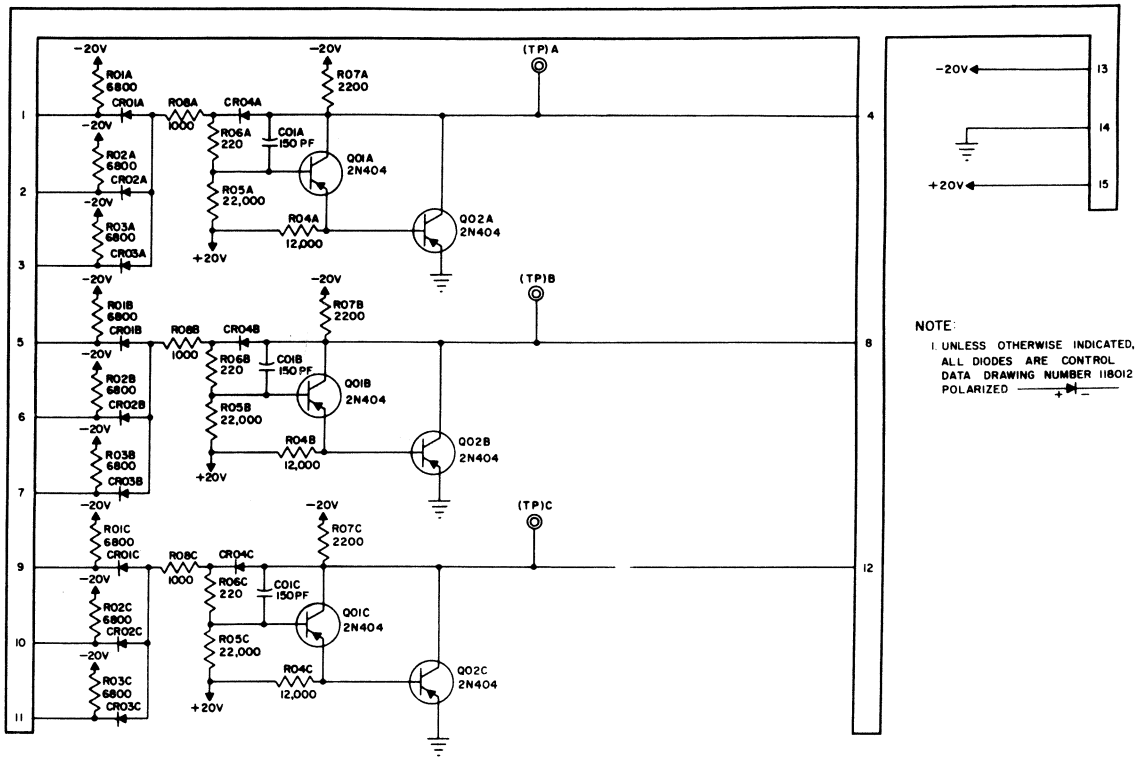


CAPACITOR
50A





OUTPUT
60A


-20V
R01A 6800
CR01A
R08A 1000
CR04A
R07A 2200
(TP)A
R06A 220
C01A 150 PF
Q01A 2N404
R05A 22,000
R04A 12,000
Q02A 2N404
+20V
R02A 6800
CR02A
R03A 6800
CR03A
R01B 6800
CR01B
R08B 1000
CR04B
R07B 2200
(TP)B
R06B 220
C01B 150 PF
Q01B 2N404
R05B 22,000
R04B 12,000
Q02B 2N404
R02B 6800
CR02B
R03B 6800
CR03B
R01C 6800
CR01C
R08C 1000
CR04C
R07C 2200
(TP)C
R06C 220
C01C 150PF
Q01C 2N404
R05C 22,000
R04C 12,000
Q02C 2N404
R02C 6800
CR02C
R03C 6800
CR03C
1
2
3
4
5
6
7
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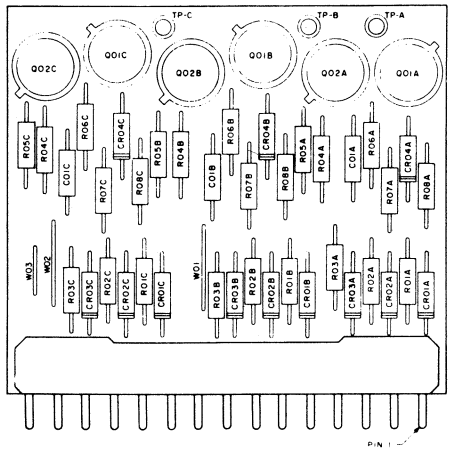
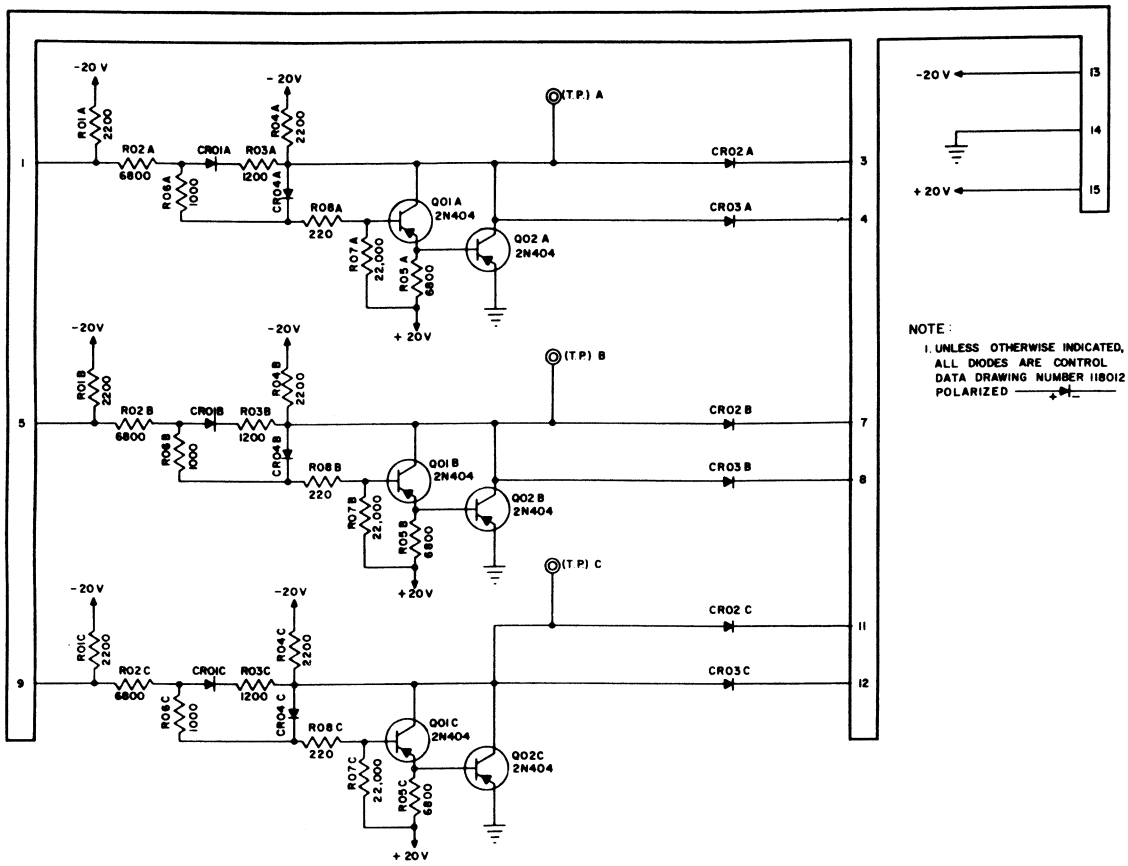
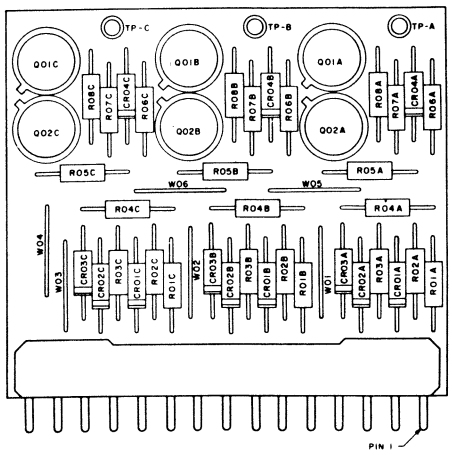
9
10
11
12
13
14
15
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012
POLARIZED

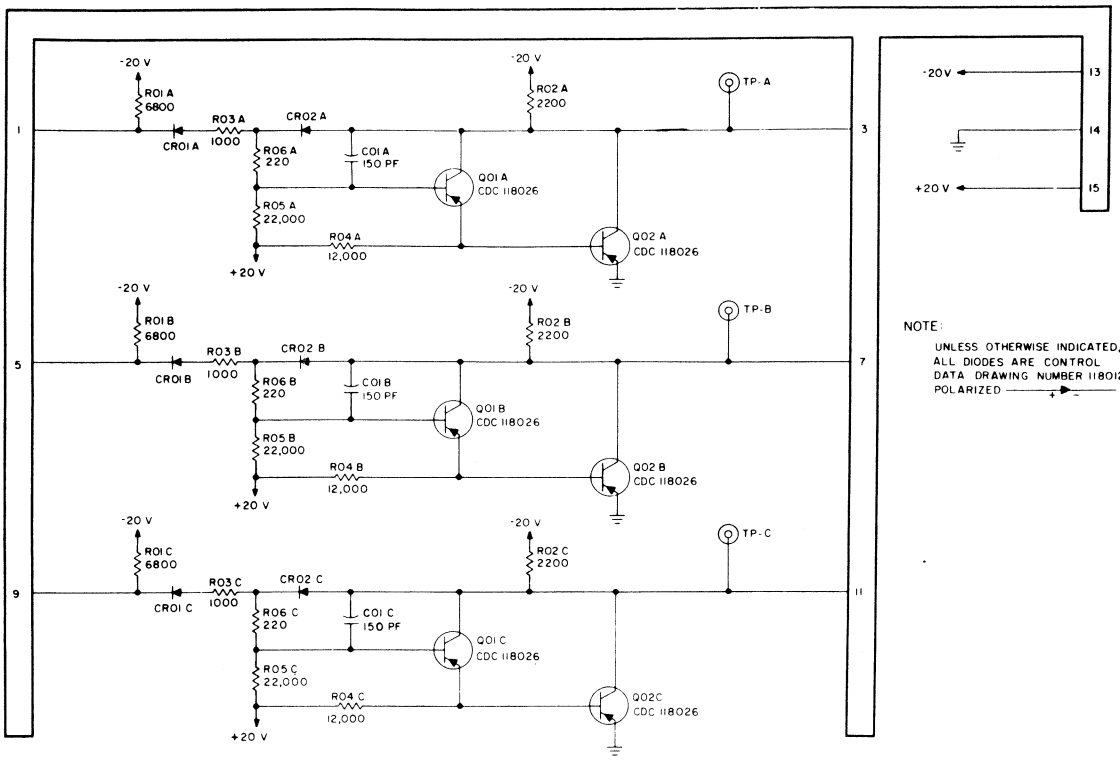

TP-C
TP-B
TP-A
Q02C
Q01C
Q02B
Q01B
Q02A
Q01A
W03
W02
W01
PIN 1

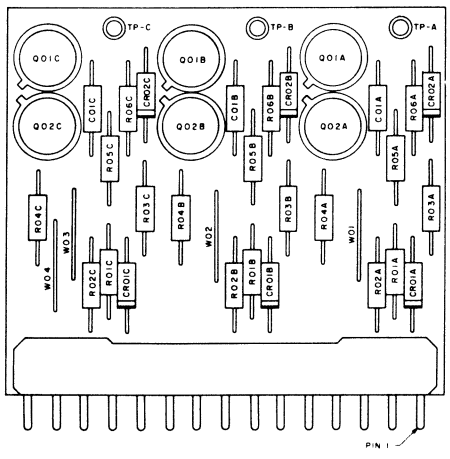
INPUT
61

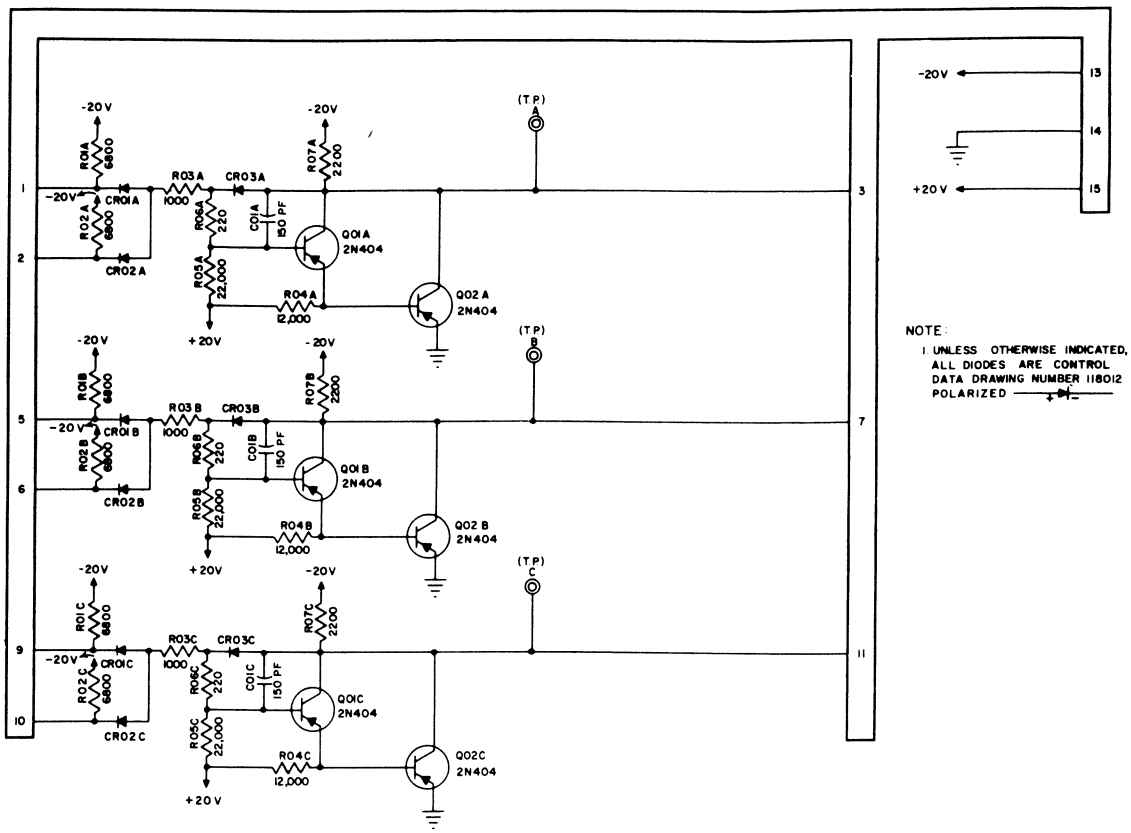

-20 V
-20V
(T.P.) A
R01A 2200
R02A 6800
CR01A
R03A 1200
R04A 2200
R06A 1000
CR04A
R08A 220
Q01A 2N404
Q02A 2N404
R07A 22,000
R05A 6800
+20V
CR02A
CR03A
1
3
4
(T.P.) B
R01B 2200
R02B 6800
CR01B
R03B 1200
R04B 2200
R06B 1000
CR04B
R08B 220
Q01B 2N404
Q02B 2N404
R07B 22,000
R05B 6800
CR02B
CR03B
5
7
8
(T.P.) C
R01C 2200
R02C 6800
CR01C
R03C 1200
R04C 2200
R06C 1000
CR04C
R08C 220
Q01C 2N404
Q02C 2N404
R07C 22,000
R05C 6800
CR02C
CR03C
9
11
12
-20 V
13
14
+20 V
15
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED


TP-C
TP-B
TP-A
Q01C
Q01B
Q01A
Q02C
Q02B
Q02A
R08C
R07C
CR04C
R06C
R08B
R07B
CR04B
R06B
R08A
R07A
CR04A
R06A
R05C
R05B
R05A
W06
W05
R04C
R04B
R04A
W04
W03
W02
W01
CR02C
CR03C
R03C
CR01C
R02C
R01C
CR03B
CR02B
R03B
CR01B
R02B
R01B
CR02A
CR03A
R03A
CR01A
R02A
R01A
PIN 1

OUTPUT
62


-20 V
R01 A
6800
R03 A
1000
CR01 A
CR02 A
R06 A
220
C01 A
150 PF
Q01 A
CDC 118026
R05 A
22,000
R04 A
12,000
+20 V
R02 A
2200
TP-A
Q02 A
CDC 118026
R01 B
6800
R03 B
1000
CR01 B
CR02 B
R06 B
220
C01 B
150 PF
Q01 B
CDC 118026
R05 B
22,000
R04 B
12,000
R02 B
2200
TP-B
Q02 B
CDC 118026
R01 C
6800
R03 C
1000
CR01 C
CR02 C
R06 C
220
C01 C
150 PF
Q01 C
CDC 118026
R05 C
22,000
R04 C
12,000
R02 C
2200
TP-C
Q02C
CDC 118026
1
3
5
7
9
11
-20V
13
14
+20 V
15
NOTE:
UNLESS OTHERWISE INDICATED,
ALL DIODES ARE CONTROL
DATA DRAWING NUMBER 118012
POLARIZED


TP-C
TP-B
TP-A
Q01C
Q01B
Q01A
Q02C
Q02B
Q02A
C01C
C01B
C01A
R06C
R06B
R06A
CR02C
CR02B
CR02A
R05C
R05B
R05A
R04C
R03C
R04B
R03B
R04A
R03A
W03
W02
W01
W04
R02C
R01C
CR01C
R02B
R01B
CR01B
R02A
R01A
CR01A
PIN 1


-20V
+20V
(T.P) A
(T.P) B
(T.P) C
R01A 6800
R02A 6800
CR01A
CR02A
R03A 1000
CR03A
R05A 22,000
R06A 220
C01A 150 PF
R04A 12,000
R07A 2200
Q01A 2N404
Q02A 2N404
R01B 6800
R02B 6800
CR01B
CR02B
R03B 1000
CR03B
R05B 22,000
R06B 220
C01B 150 PF
R04B 12,000
R07B 2200
Q01B 2N404
Q02B 2N404
R01C 6800
R02C 6800
CR01C
CR02C
R03C 1000
CR03C
R05C 22,000
R06C 220
C01C 150 PF
R04C 12,000
R07C 2200
Q01C 2N404
Q02C 2N404
1
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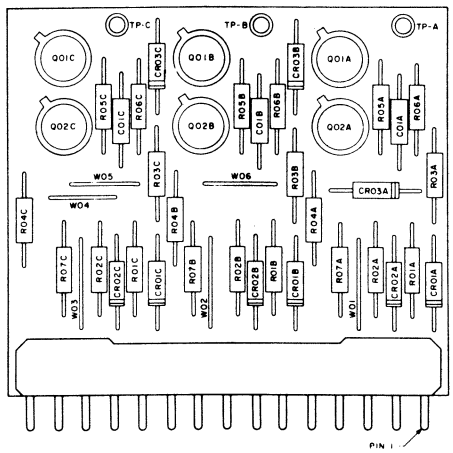
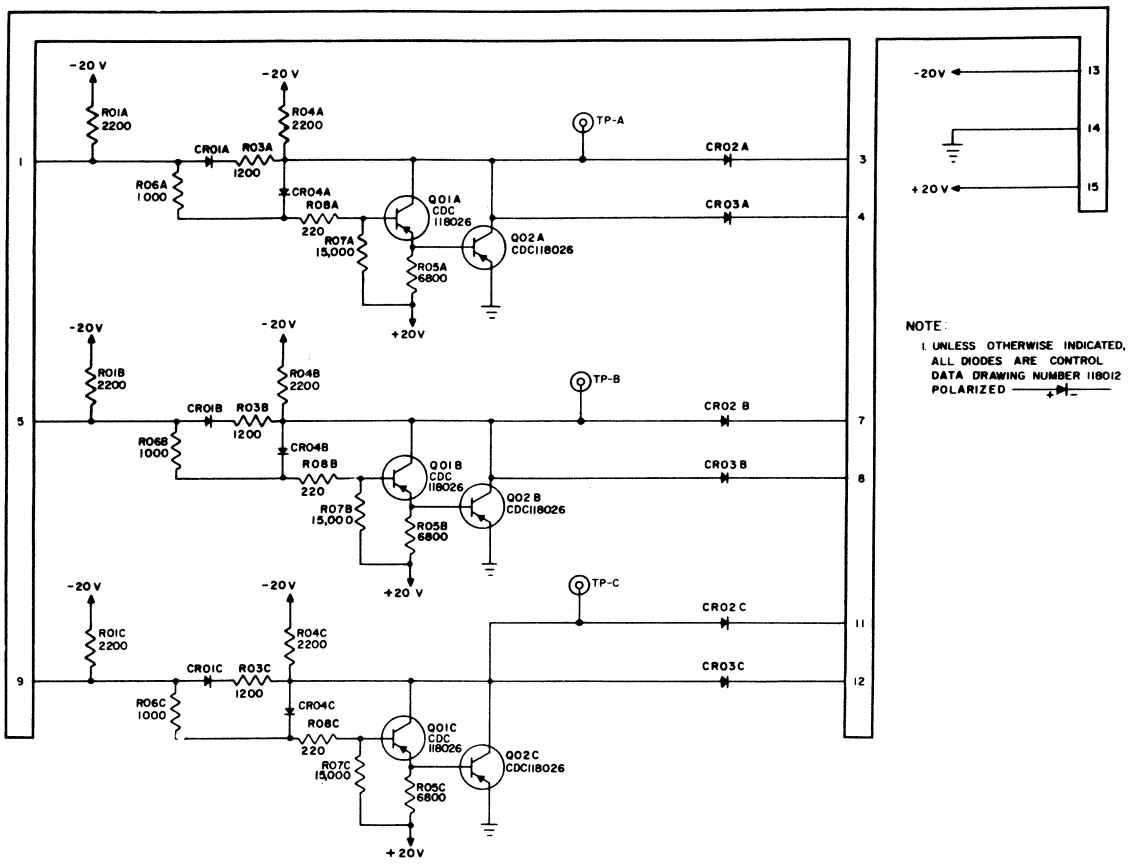
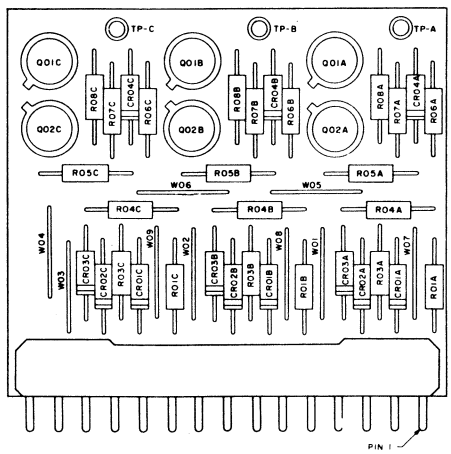
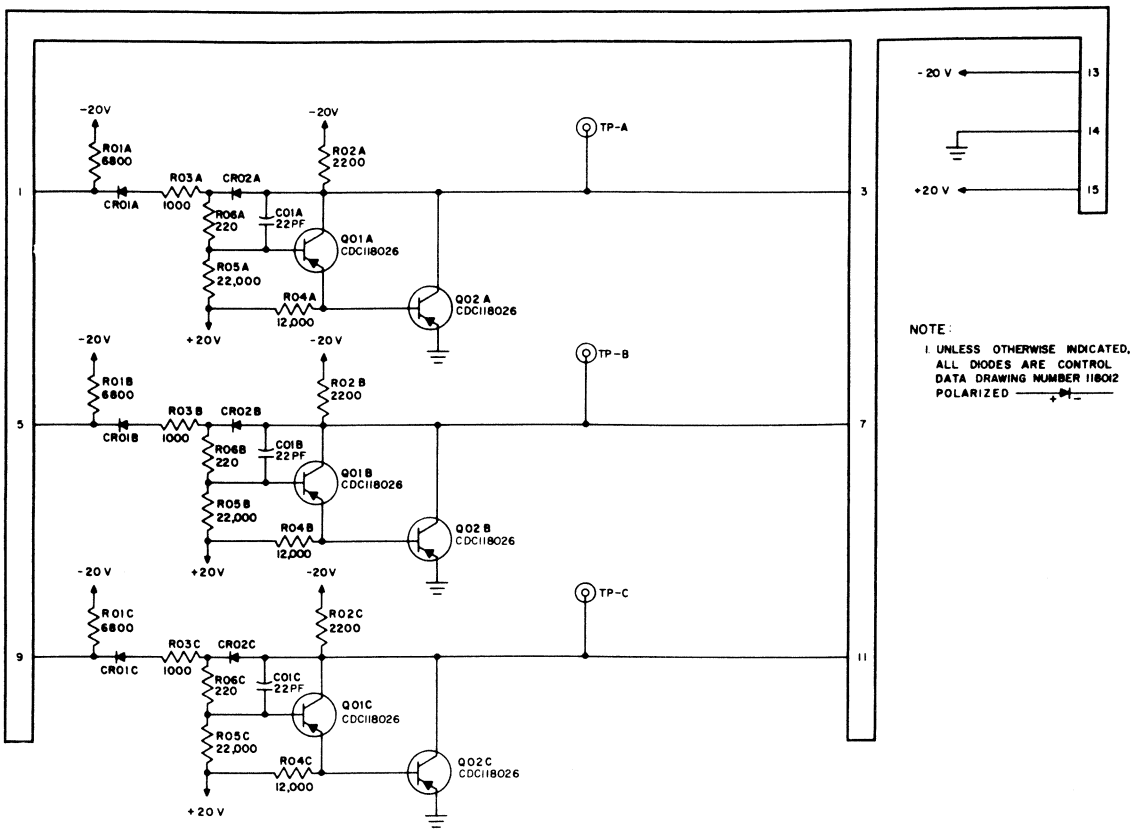
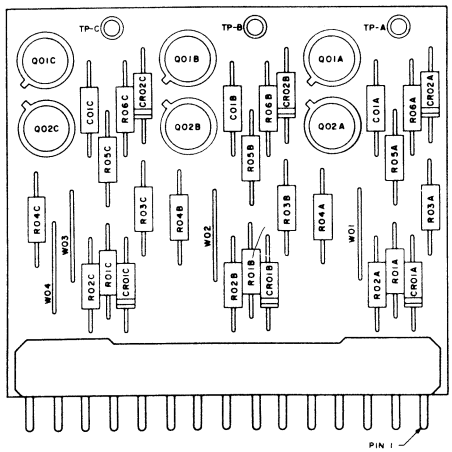
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED


TP-C
TP-B
TP-A
Q01C
Q02C
Q01B
Q02B
Q01A
Q02A
CR03C
CR03B
CR03A
R03C
R03B
R03A
R05C
R05B
R05A
C01C
C01B
C01A
R06C
R06B
R06A
W04
W05
W06
R04C
R04B
R04A
R07C
R07B
R07A
R02C
R02B
R02A
R01C
R01B
R01A
CR02C
CR02B
CR02A
CR01C
CR01B
CR01A
W03
W02
W01
PIN 1

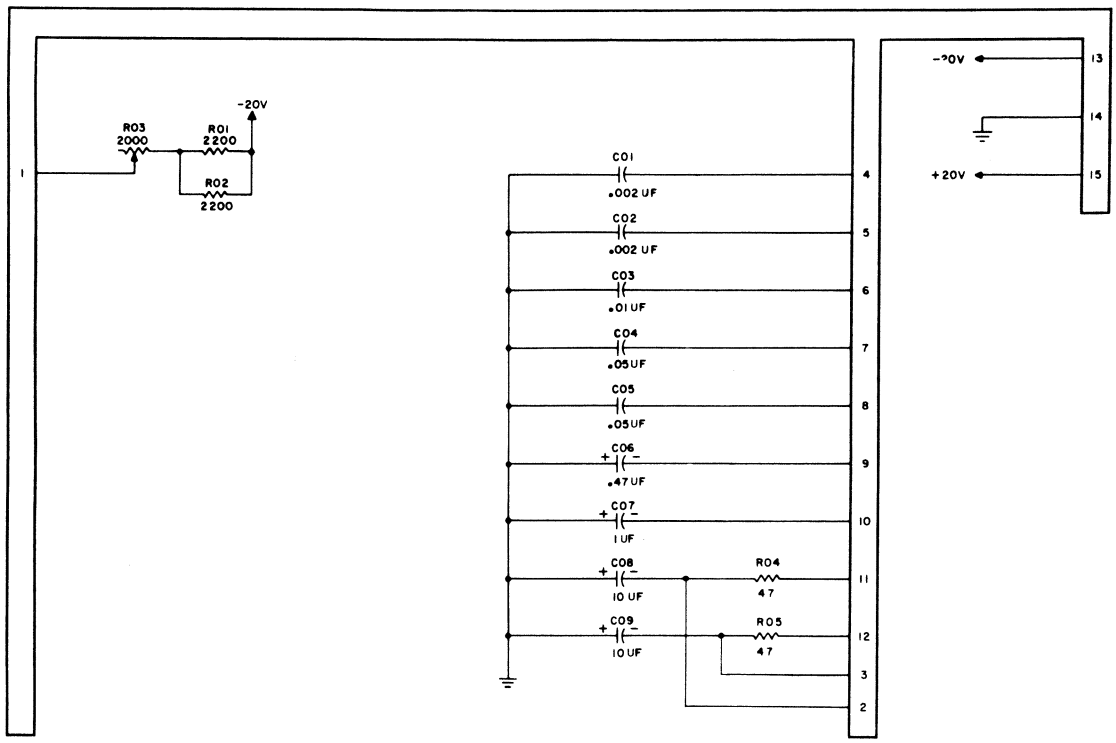

-20 V
R01A 2200
R04A 2200
CR01A
R03A 1200
R06A 1000
CR04A
R08A 220
R07A 15,000
R05A 6800
Q01A CDC 118026
Q02A CDC118026
+20V
TP-A
CR02A
CR03A
1
3
4
-20V
13
14
+20V
15
R01B 2200
R04B 2200
CR01B
R03B 1200
R06B 1000
CR04B
R08B 220
R07B 15,000
R05B 6800
Q01B CDC 118026
Q02B CDC118026
+20 V
TP-B
CR02 B
CR03 B
5
7
8
R01C 2200
R04C 2200
CR01C
R03C 1200
R06C 1000
CR04C
R08C 220
R07C 15,000
R05C 6800
Q01C CDC 118026
Q02C CDC118026
TP-C
CR02 C
CR03C
9
11
12
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED

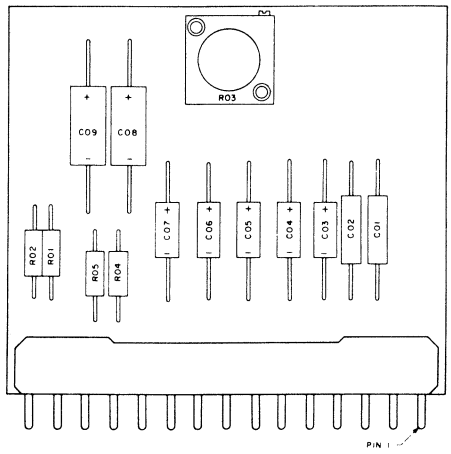

TP-C
TP-B
TP-A
Q01C
Q01B
Q01A
Q02C
Q02B
Q02A
R08C
R07C
CR04C
R06C
R08B
R07B
CR04B
R06B
R08A
R07A
CR04A
R06A
R05C
R05B
R05A
W06
W05
R04C
R04B
R04A
W04
W03
W09
W02
W08
W01
W07
CR03C
CR02C
R03C
CR01C
R01C
CR03B
CR02B
R03B
CR01B
R01B
CR03A
CR02A
R03A
CR01A
R01A
PIN 1


-20V
R01A 6800
CR01A
R03A 1000
CR02A
R06A 220
C01A 22PF
Q01A CDC118026
R05A 22,000
R04A 12,000
+20V
R02A 2200
TP-A
Q02A CDC118026
R01B 6800
CR01B
R03B 1000
CR02B
R06B 220
C01B 22PF
Q01B CDC118026
R05B 22,000
R04B 12,000
R02B 2200
TP-B
Q02B CDC118026
R01C 6800
CR01C
R03C 1000
CR02C
R06C 220
C01C 22PF
Q01C CDC118026
R05C 22,000
R04C 12,000
R02C 2200
TP-C
Q02C CDC118026
1
3
5
7
9
11
-20 V
+20 V
13
14
15
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED

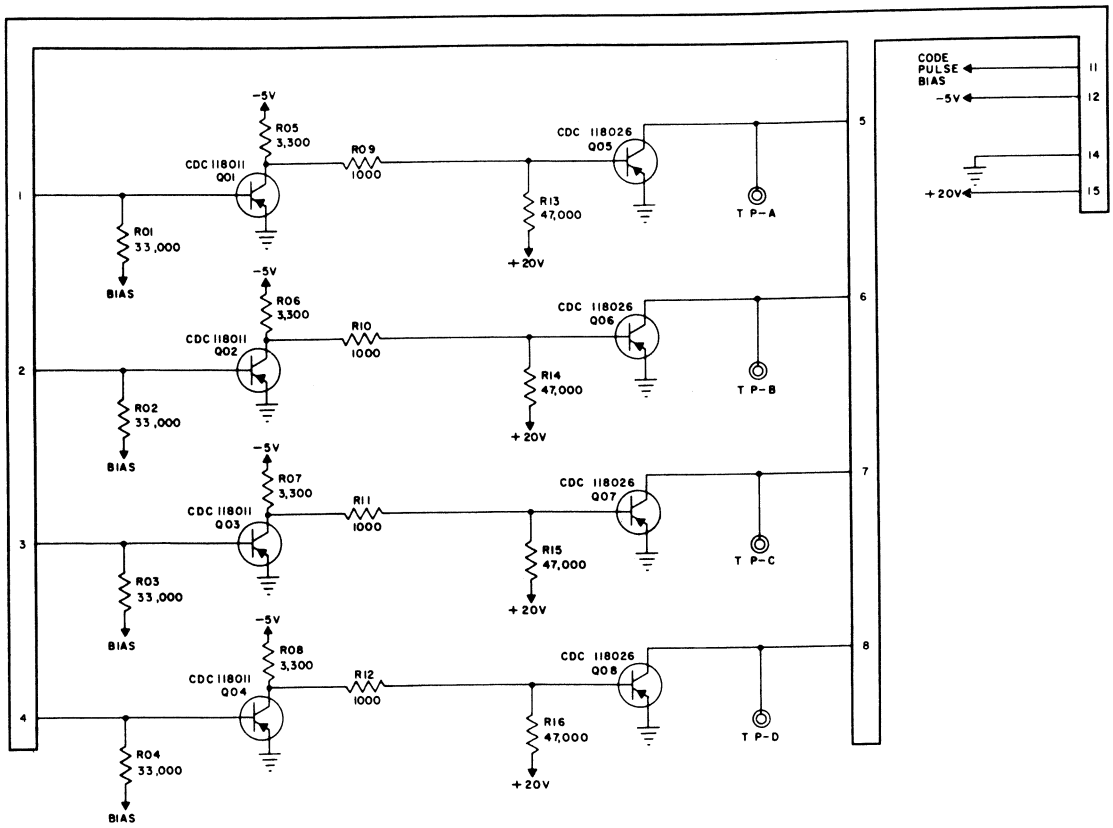

TP-C
TP-B
TP-A
Q01C
Q02C
Q01B
Q02B
Q01A
Q02A
C01C
R06C
CR02C
R05C
R04C
R03C
R02C
R01C
CR01C
W04
W03
C01B
R06B
CR02B
R05B
R04B
R03B
R02B
R01B
CR01B
W02
C01A
R06A
CR02A
R05A
R04A
R03A
R02A
R01A
CR01A
W01
PIN 1

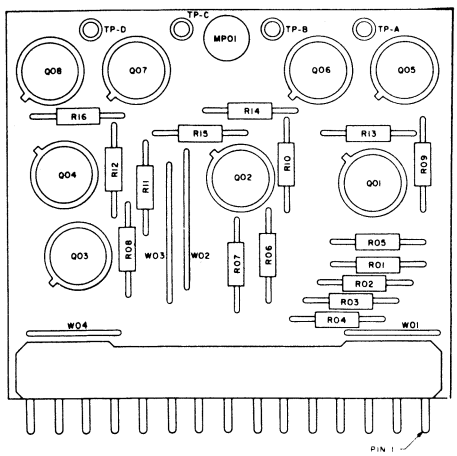
VARIABLE DELAY
73A





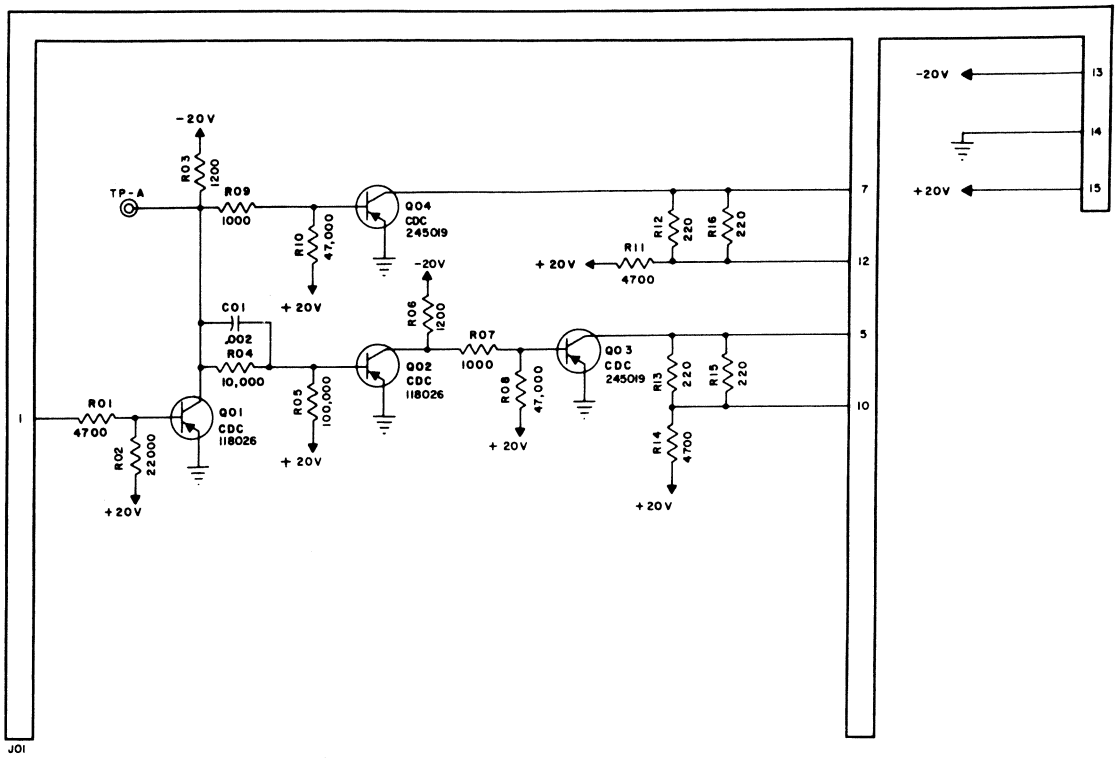
READ LEVEL AMPLIFIER
75B

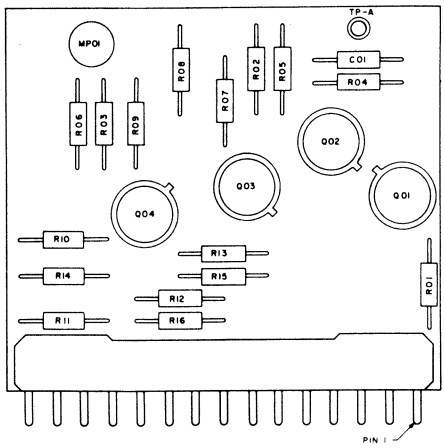




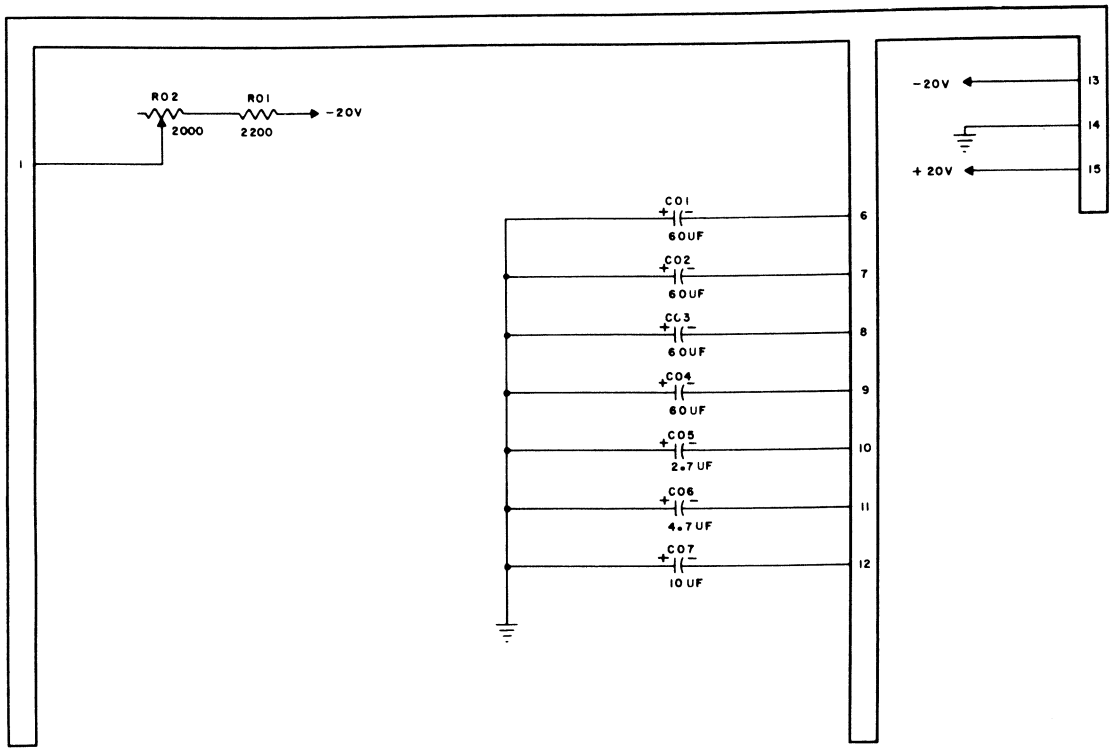
READER BRAKE

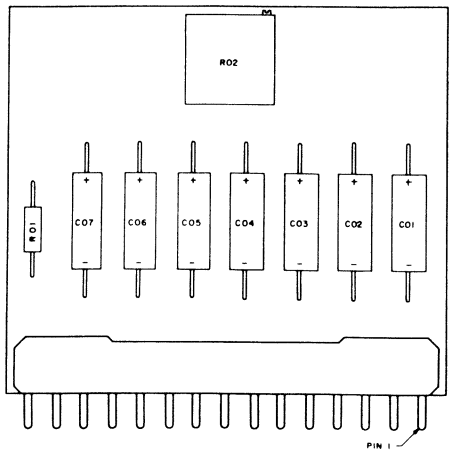
76B



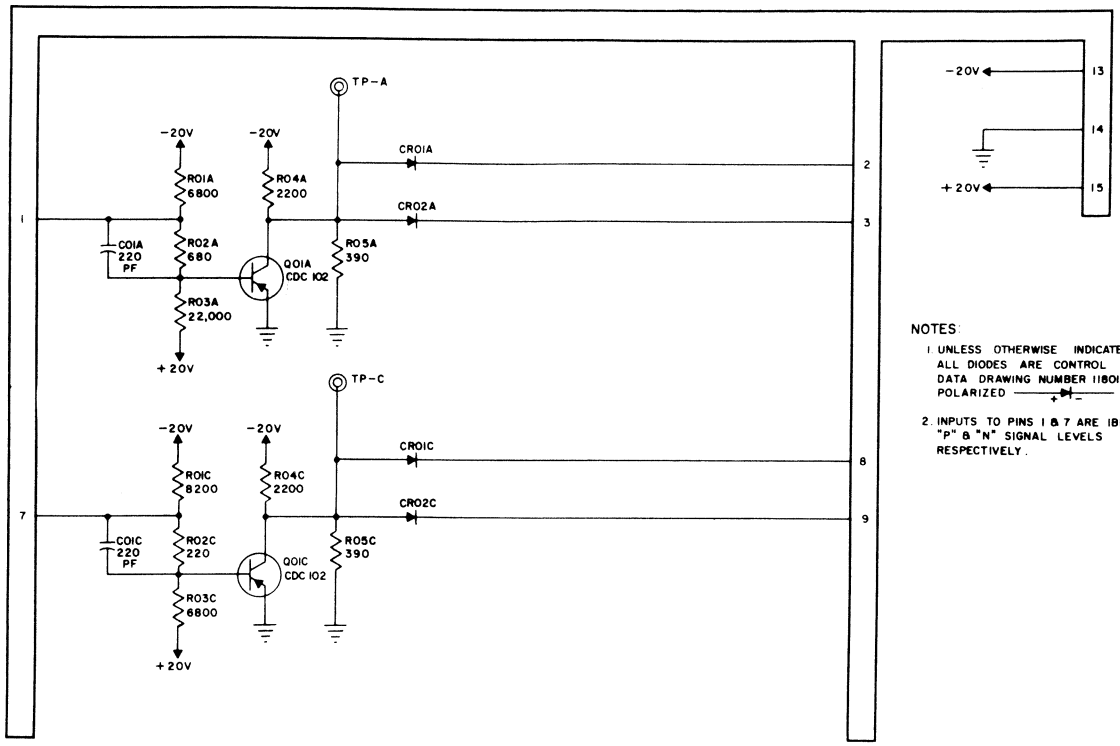


VARIABLE DELAY
77





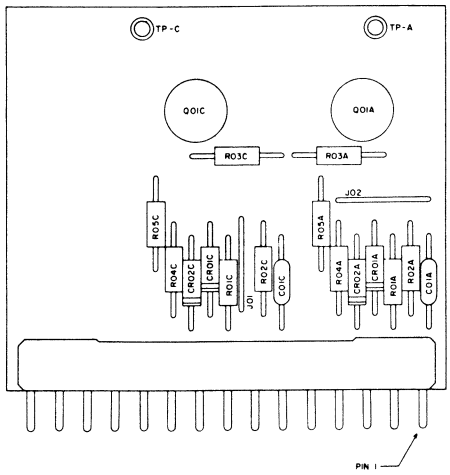
OUTPUT
78



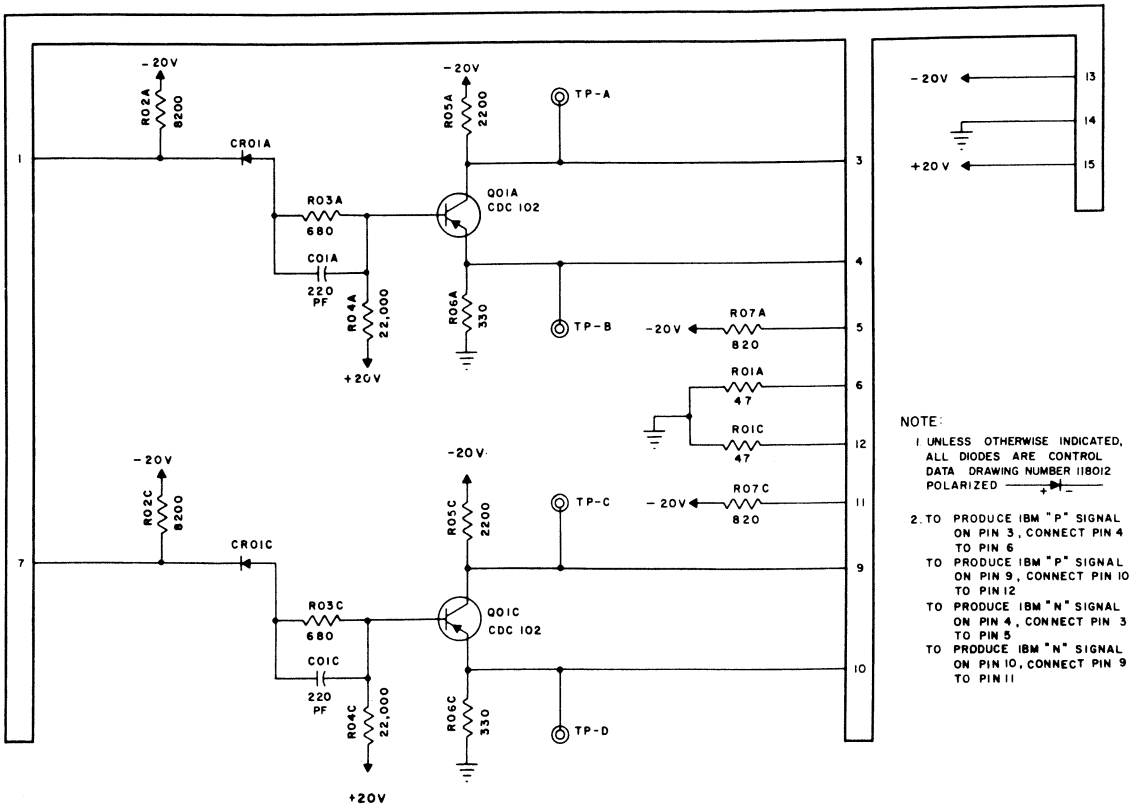
NOTES:

1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED

2. INPUTS TO PINS 1 & 7 ARE IBM "P" & "N" SIGNAL LEVELS RESPECTIVELY.



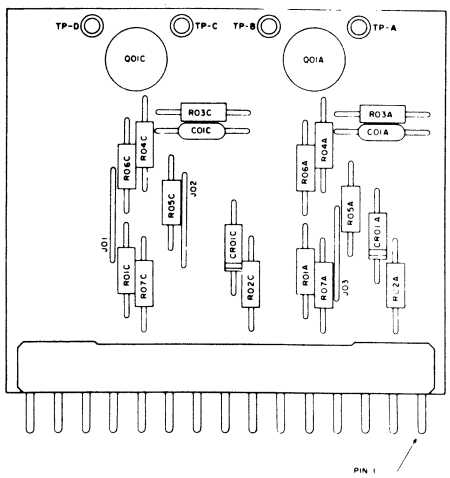
OUTPUT
79A



NOTE:

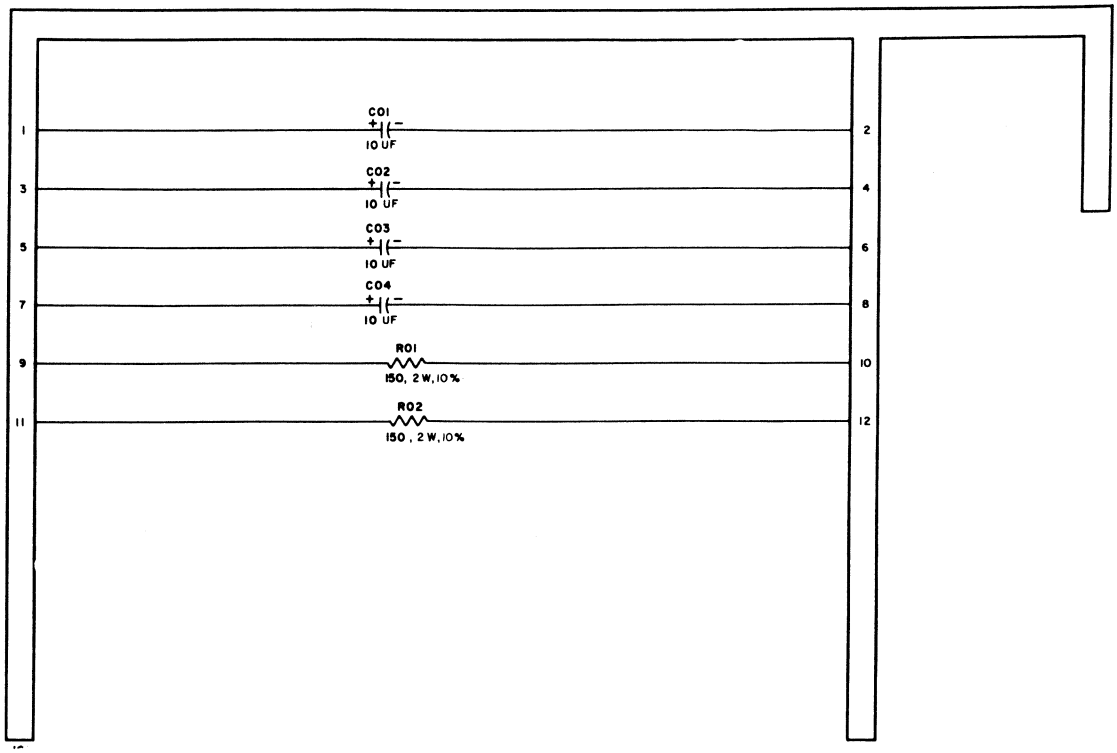
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED +|−

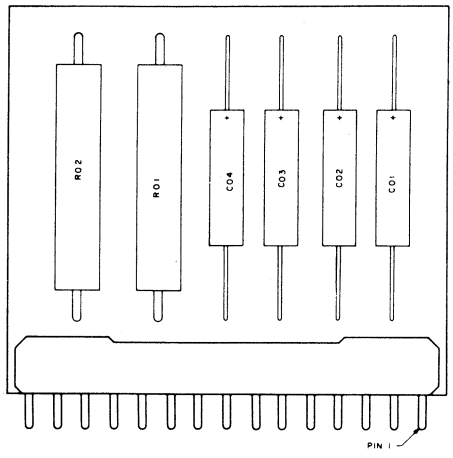
2. TO PRODUCE IBM "P" SIGNAL ON PIN 3, CONNECT PIN 4 TO PIN 6
   TO PRODUCE IBM "P" SIGNAL ON PIN 9, CONNECT PIN 10 TO PIN 12
   TO PRODUCE IBM "N" SIGNAL ON PIN 4, CONNECT PIN 3 TO PIN 5
   TO PRODUCE IBM "N" SIGNAL ON PIN 10, CONNECT PIN 9 TO PIN 11



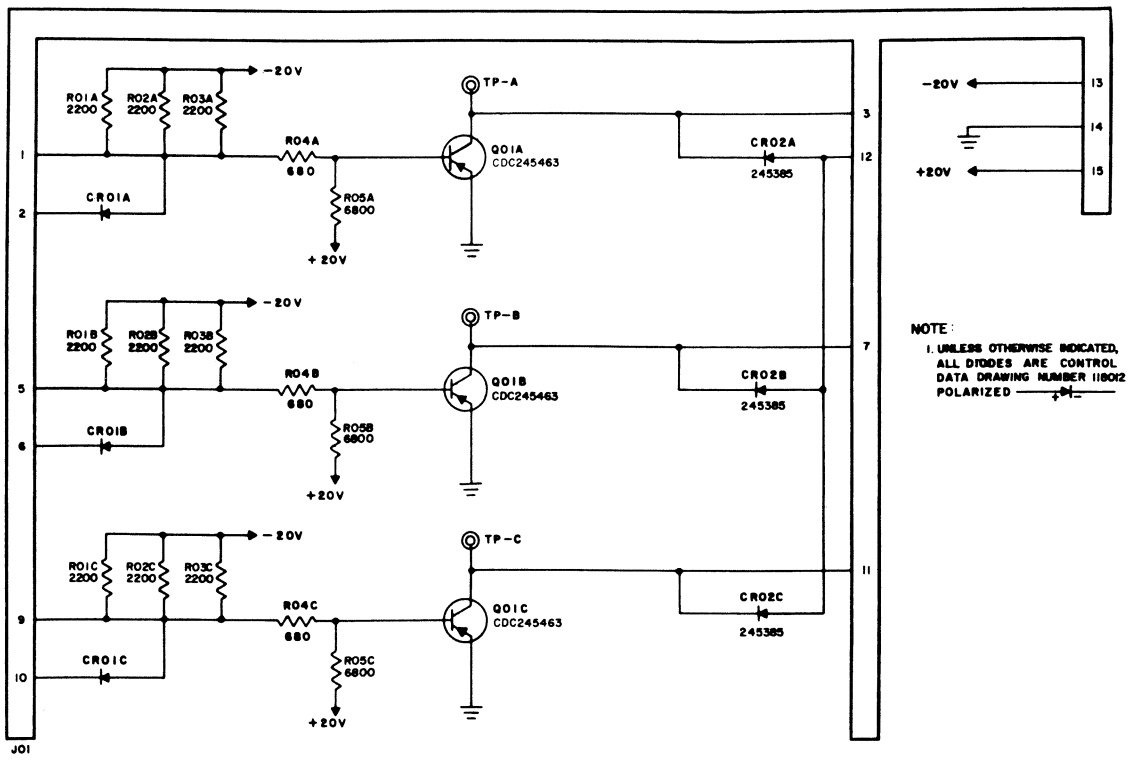
VARIABLE DELAY

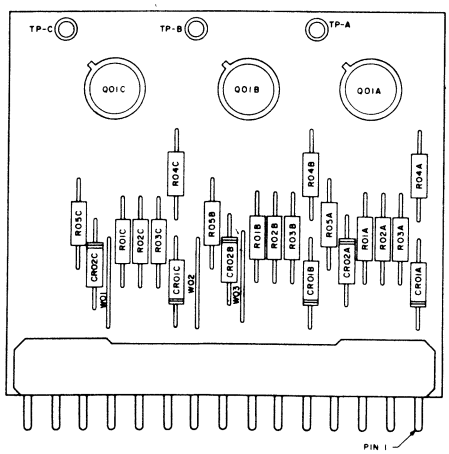
82



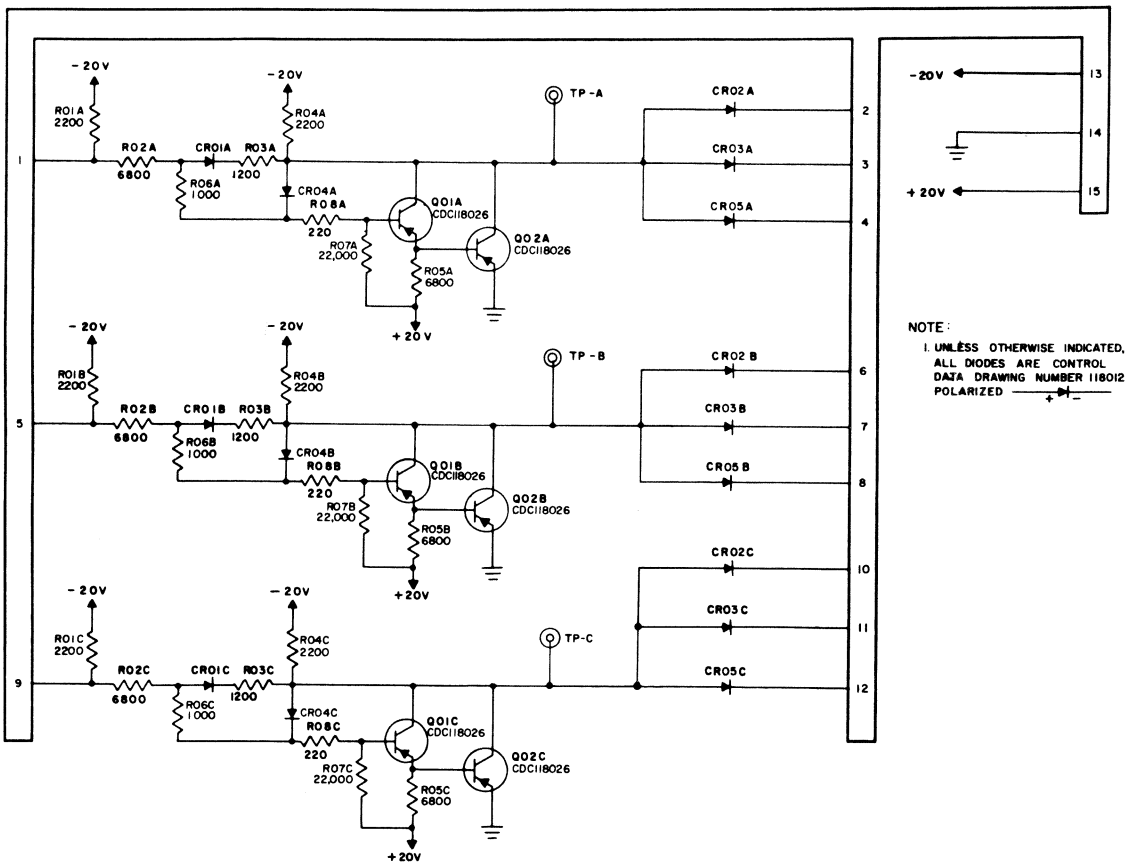


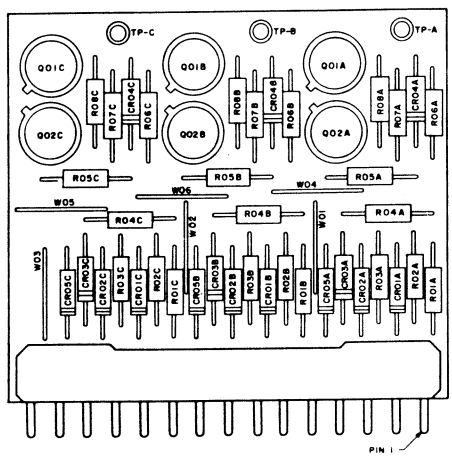
MAGNET PULLER
85A



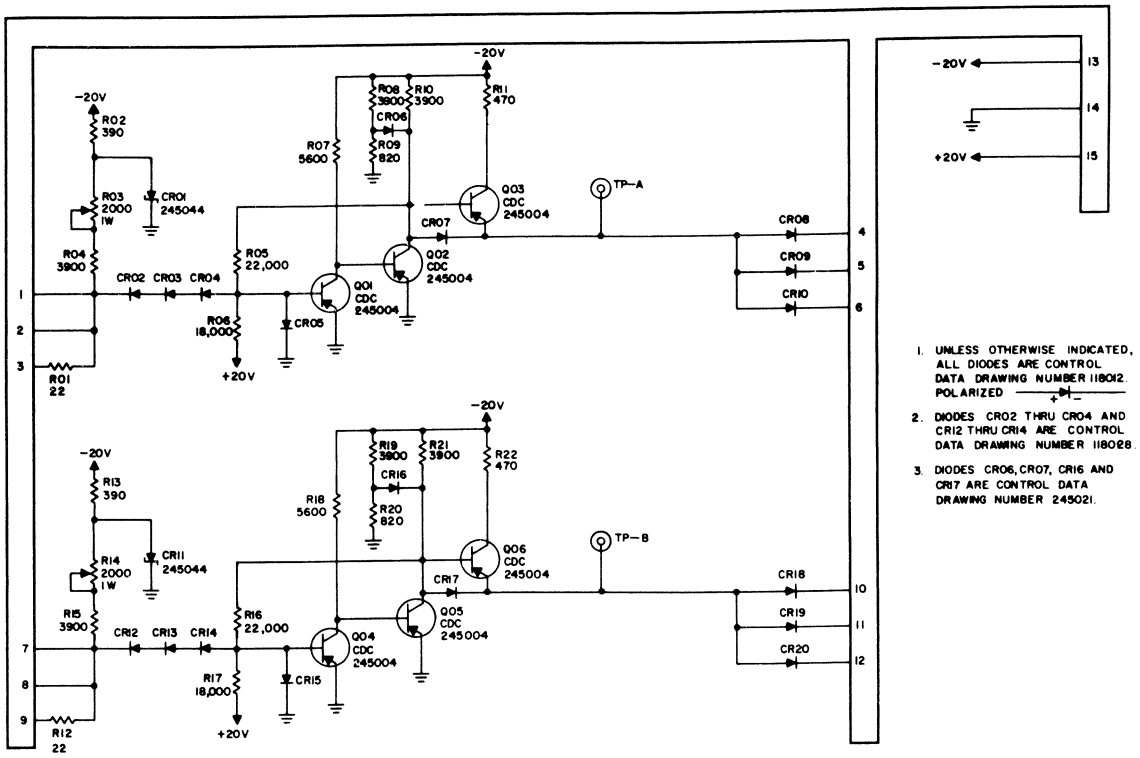


INPUT
87

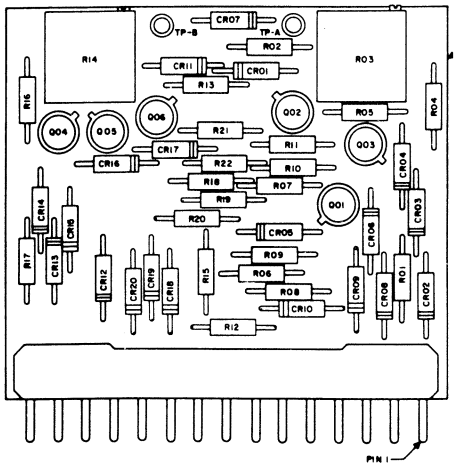

-20V
R01A 2200
R02A 6800
CR01A
R03A 1200
R04A 2200
R06A 1000
CR04A
R08A 220
R07A 22,000
R05A 6800
+20V
Q01A CDC118026
Q02A CDC118026
TP-A
CR02A
CR03A
CR05A
R01B 2200
R02B 6800
CR01B
R03B 1200
R04B 2200
R06B 1000
CR04B
R08B 220
R07B 22,000
R05B 6800
Q01B CDC118026
Q02B CDC118026
TP-B
CR02B
CR03B
CR05B
R01C 2200
R02C 6800
CR01C
R03C 1200
R04C 2200
R06C 1000
CR04C
R08C 220
R07C 22,000
R05C 6800
Q01C CDC118026
Q02C CDC118026
TP-C
CR02C
CR03C
CR05C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED


TP-C
TP-B
TP-A
Q01C
Q02C
Q01B
Q02B
Q01A
Q02A
R08C
R07C
CR04C
R06C
R08B
R07B
CR04B
R06B
R08A
R07A
CR04A
R06A
R05C
R05B
R05A
W06
W05
W04
R04C
R04B
R04A
W02
W01
W03
CR05C
CR03C
CR02C
R03C
CR01C
R02C
R01C
CR05B
CR03B
CR02B
R03B
CR01B
R02B
R01B
CR05A
CR03A
CR02A
R03A
CR01A
R02A
R01A
PIN 1

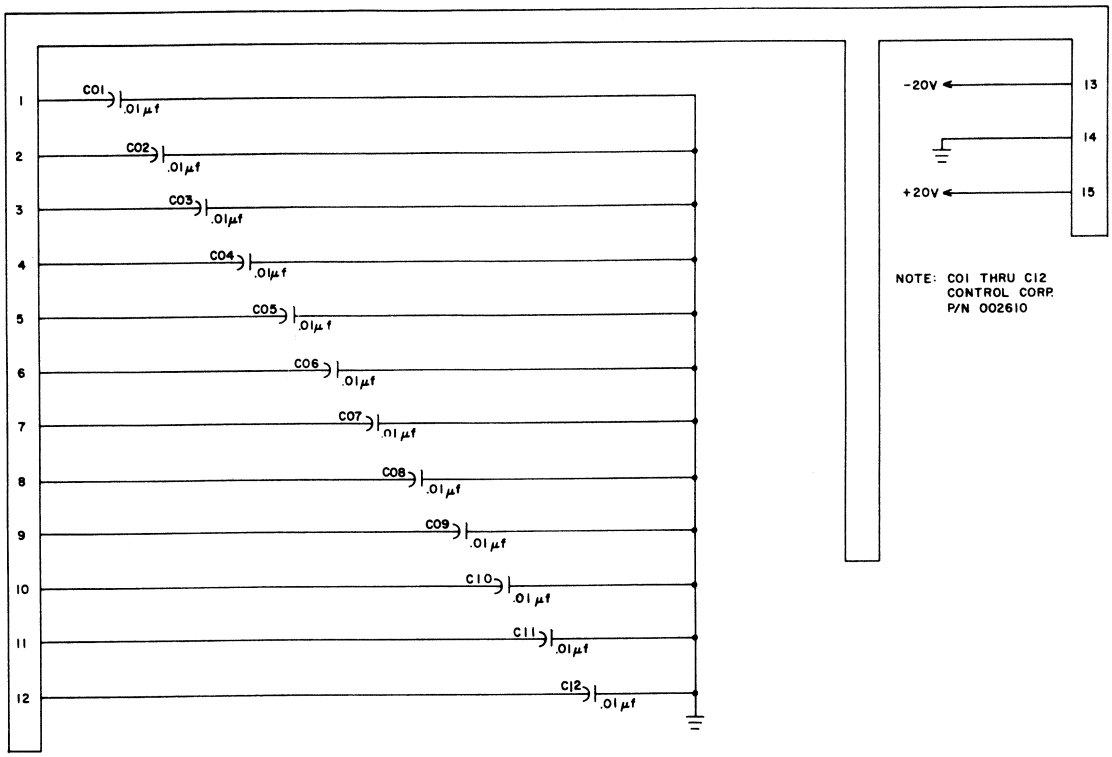
DELAY
97A

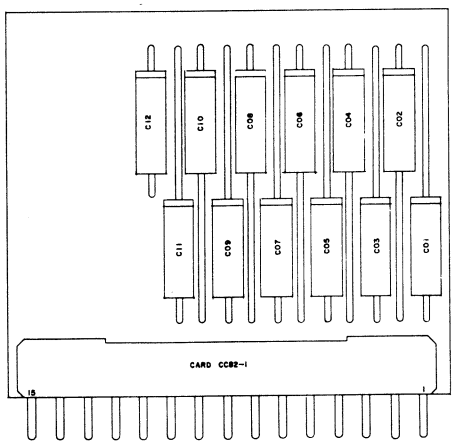


1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012. POLARIZED
2. DIODES CR02 THRU CR04 AND CR12 THRU CR14 ARE CONTROL DATA DRAWING NUMBER 118028.
3. DIODES CR06, CR07, CR16 AND CR17 ARE CONTROL DATA DRAWING NUMBER 245021.

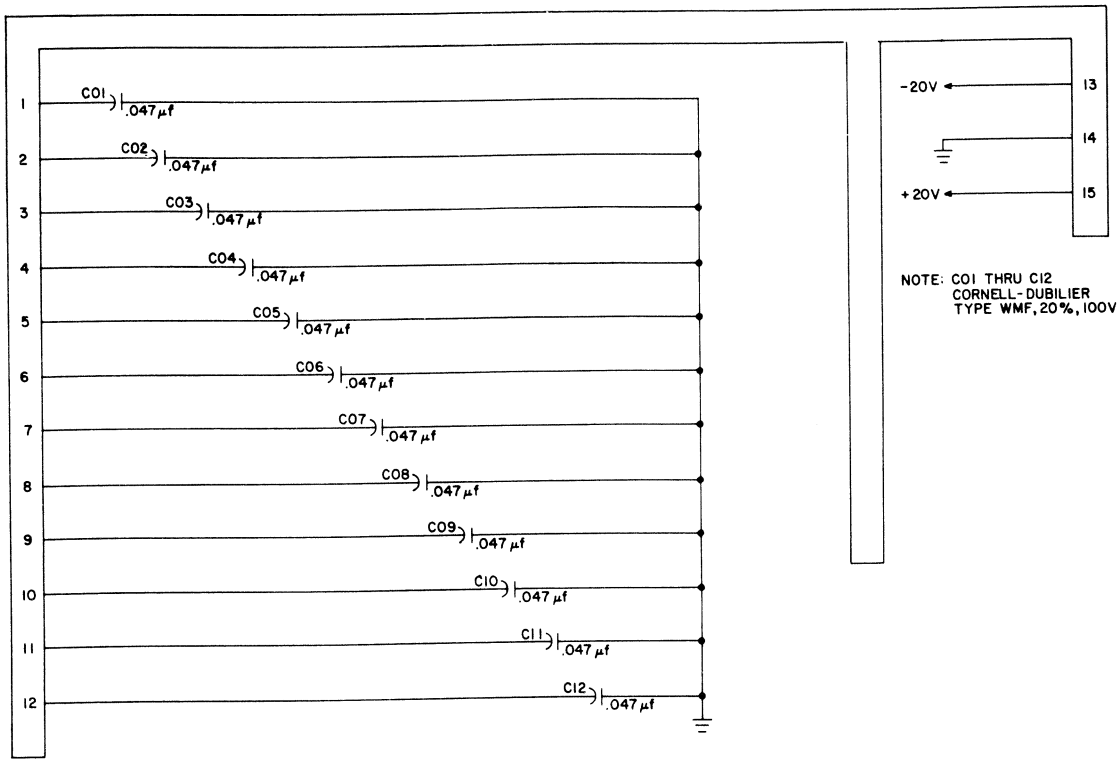


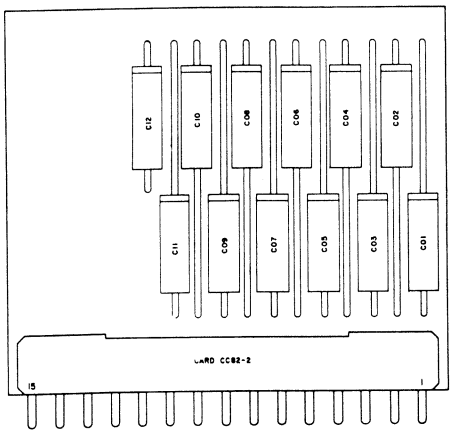
CAPACITOR
CC82-1



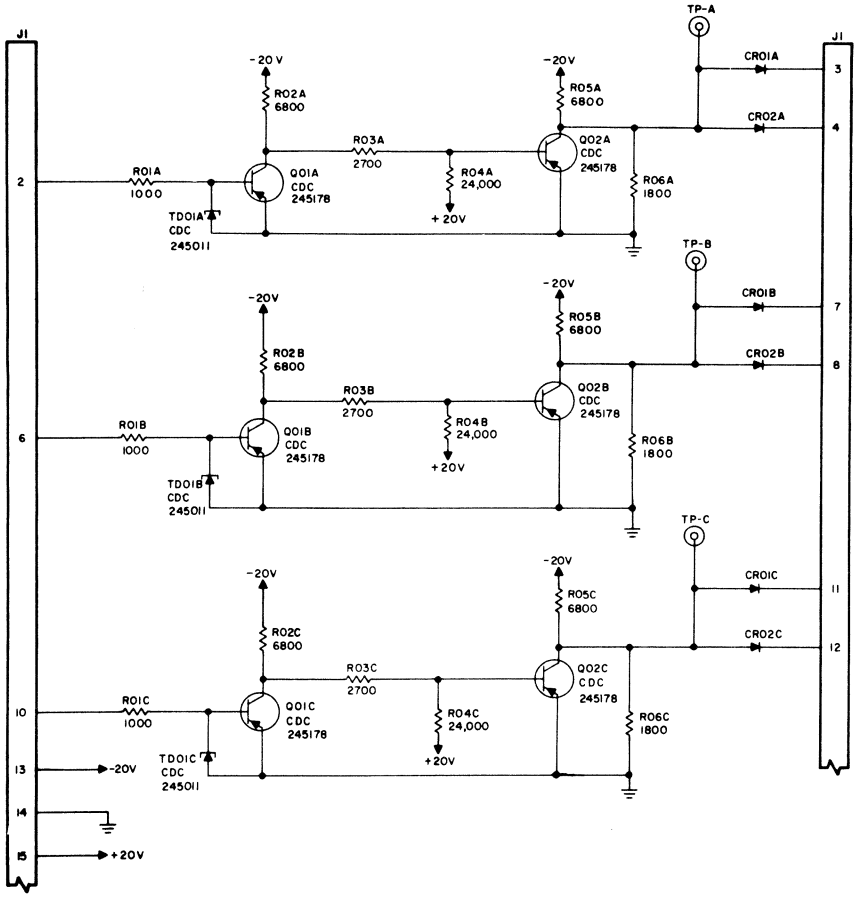


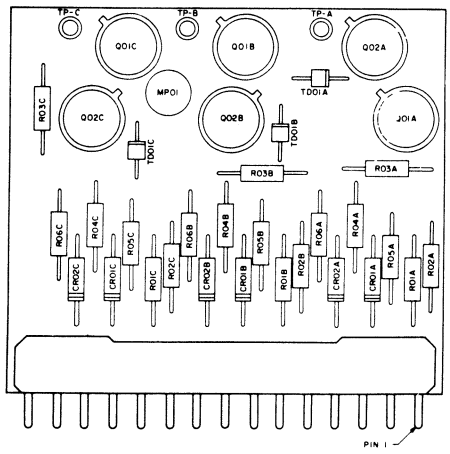
CAPACITOR
CC82-2



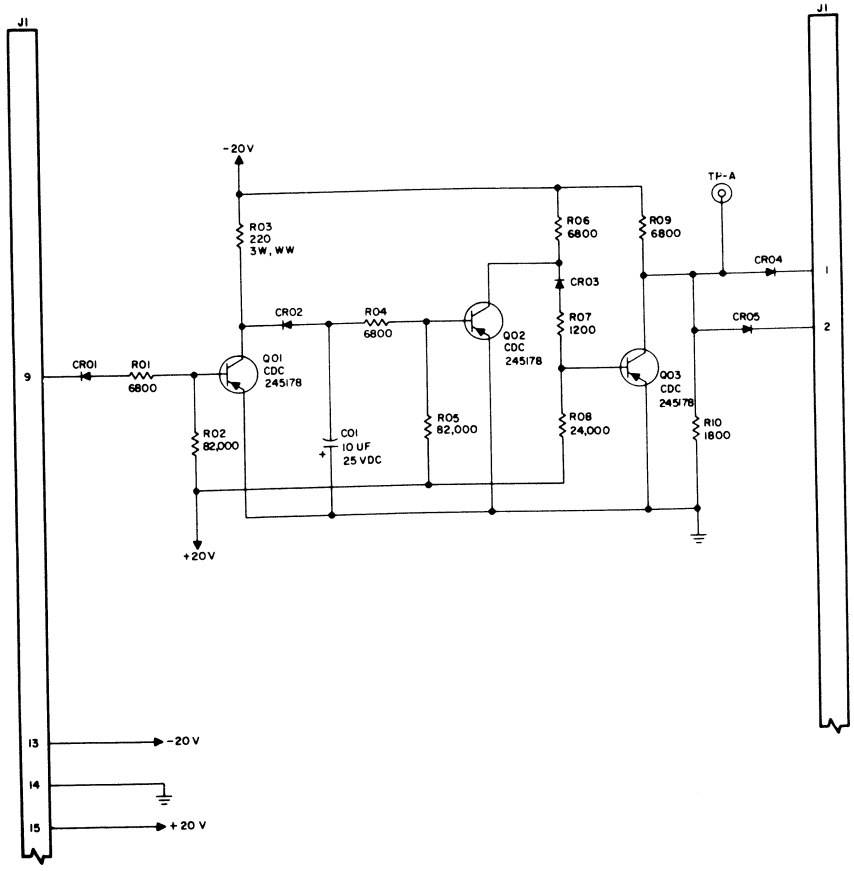


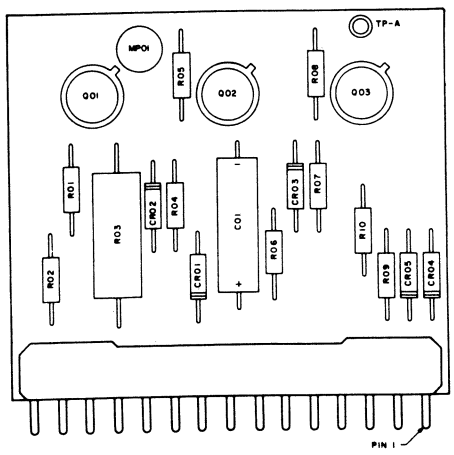
PULSE SHAPER
P93B



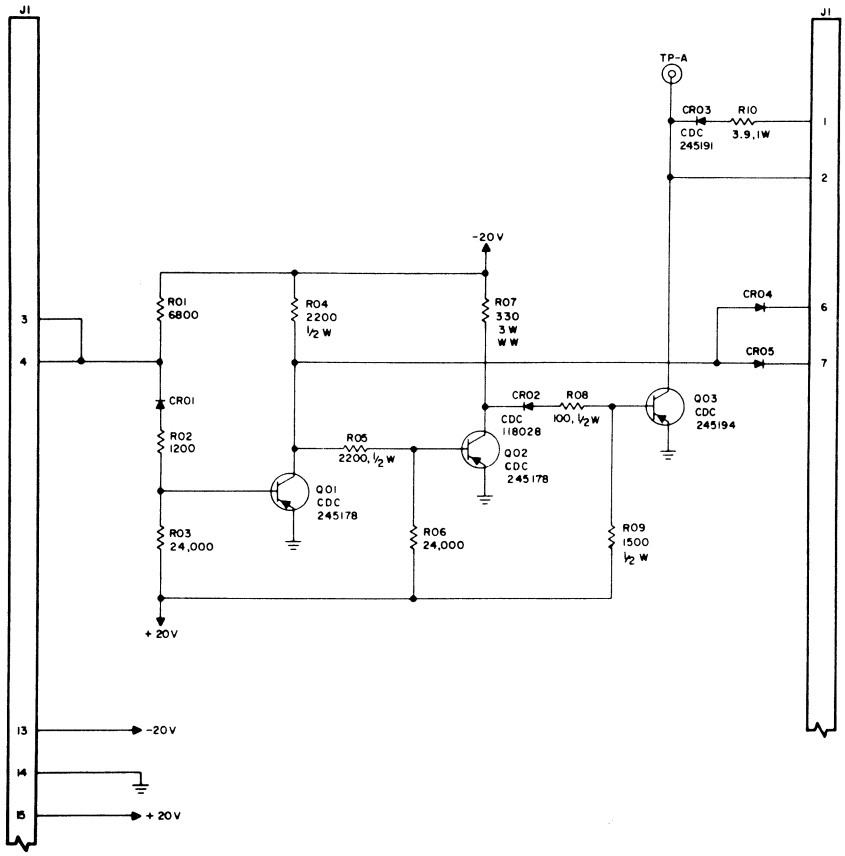


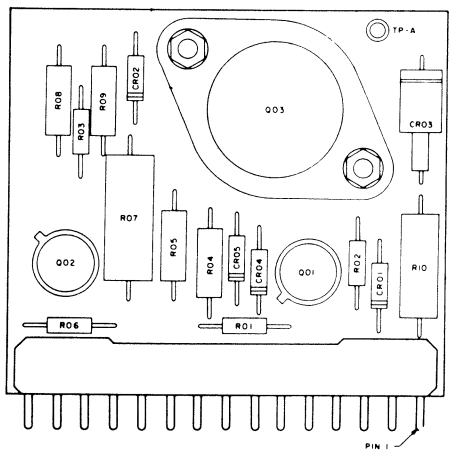
RIBBON ADVANCE
P94A





RIBBON DRIVE & HOLD
P96A





BRAKE CLUTCH ONE SHOT
P99