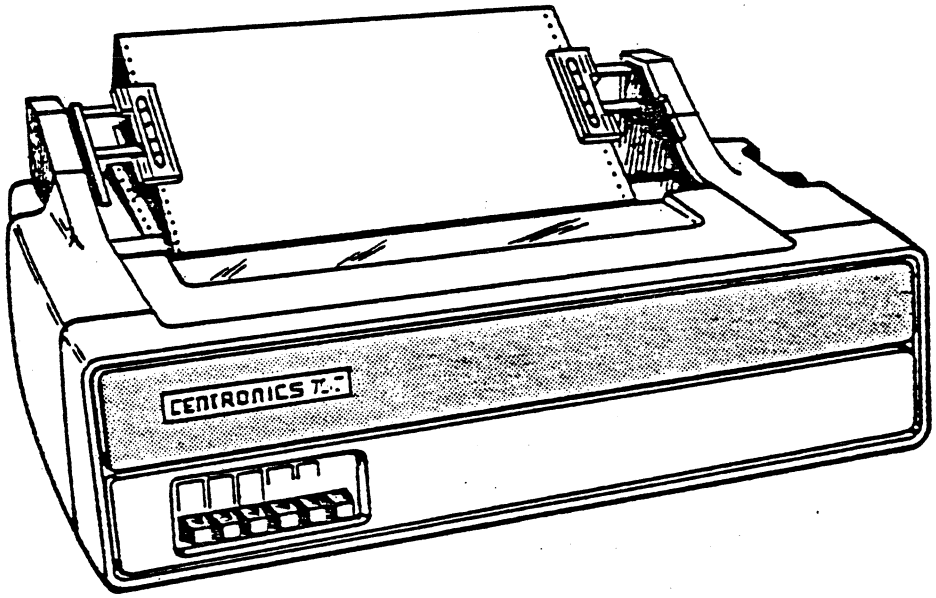
1A

TECHNICAL MANUAL

MODEL 704 PRINTER



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SECTION I
INTRODUCTION

1.1 MANUALS

This technical manual is part of a series providing complete documentation for the Model 704. The three manual series, with part numbers, is listed below.

TITLE	PART NO.
Technical Manual	37400700
Operator's Manual	37400701
Illustrated Parts Breakdown Manual	37400702

1.2 GENERAL DESCRIPTION (Figure 1-1)

The Model 704 is a 132-column, dot matrix printer with an intergrated RS-232C asynchronous interface and a 9-foot EIA input cable. The printer uses microprocessor technology and prints bidirectionally. Maximum throughput is achieved with the bidirectional print head which seeks the shortest path to the next line of data when printing successive lines of data. Print speed is 180 characters-per-second for the standard 7x7 dot matrix. Stepper motors control print head and paper movement. A six key control panel and DIP switches are used for operator control. The logic board contains circuitry for receiving serial data from a data set or modem. The RS-232C interface portion of the logic provides serial-to-parallel data conversion, buffers each data character and generates interrupts to synchronize the microprocessor with the serial data communications link.

The remainder of the logic consists of a 256 character input buffer, a 132 character print buffer and PROM's for firmware storage and character generation. Print mechanism control circuits provide the final output to the print head and stepper motors for carriage motion and paper movement.

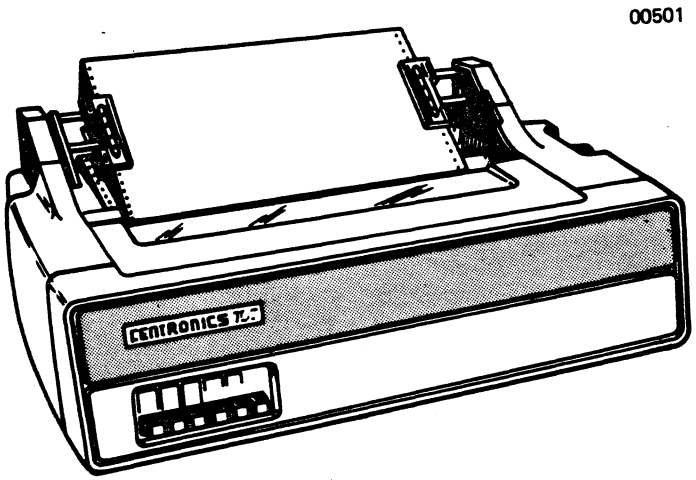

Figure 1-1. MODEL 704 PRINTER

1.3 PHYSICAL DESCRIPTION (Figure 1-2)

The printer is completely self-contained, including the printer mechanism with micoprocessor electronics and integral power supplies. Optional features are available to adapt the printer to specific needs.

The printer covers include several plastic covers and one sheet metal cover. The top cover, the two side covers, and the front cover are plastic, and the rear cover is sheet metal. The front cover has an opening for the control panel in the lower left corner.

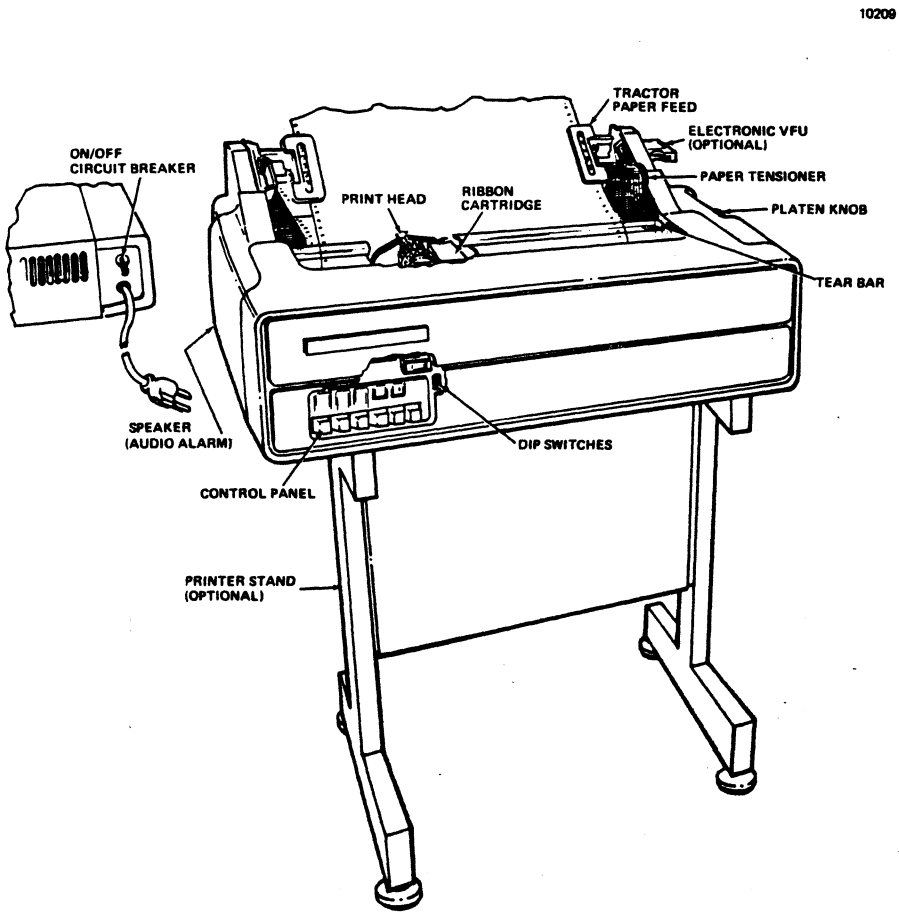

Figure 1-2. MAJOR ASSEMBLIES

The printer consists of three major units: the print mechanism, the electronics, and the paper handling mechanism.

1.3.1 PRINT MECHANISM

The print mechanism consists of the carriage assembly, drive mechanism and print head. The drive contains a stepper motor which drives a continuous belt that transports the print head and carriage assembly back and forth along the platen.

1.3.2 ELECTRONICS

Printer control is provided by the electronics which consists of the input power transformer, DC power supply, video amplifier, logic card, and power driver board. The logic card contains the RS-232C serial interface, microprocessor, firmware, control logic, and power supply regulators. The power driver board is located in front of the printer behind the front cover. It provides the drive signals for the print head solenoids and stepper motors. The video amplifier receives pulses from a timing fence to synchronize the head firing.

1.3.3 PAPER HANDLING MECHANISM

The paper handling mechanism is a tractor feed unit accommodating fan-fold forms up to 17.3 inch wide with a 13.2 inch maximum print width.

The printer has a rear paper feed and a bottom paper feed. Both can handle up to six-part forms at a slew rate of 15 inches per second (ips). The standard vertical line spacing is 6 lines per inch (lpi) with 8 lpi optional.

1.4 PRINTER OPERATION (Figure 1-3, 1-4)

Figure 1-3 is a basic block diagram of the printer, and Figure 1-4 is a pictorial diagram illustrating the particular printer components and how they relate to the main logic board.

The printer uses a microprocessor that controls printer operations. Under program control, the microprocessor, located on the logic board, controls the receiving of serial data via the I/O controller chip and monitors the control panel. Also, the microprocessor initiates movement of the print head carriage and paper, and monitors feedback from the limit switches, video system, optional electronic vertical format unit (EVFU), and the paper empty switch to effect proper execution of these motion commands. It maintains a record of the position of the print head at all times, provides printer status information to the attached devices, and performs other "housekeeping" functions.

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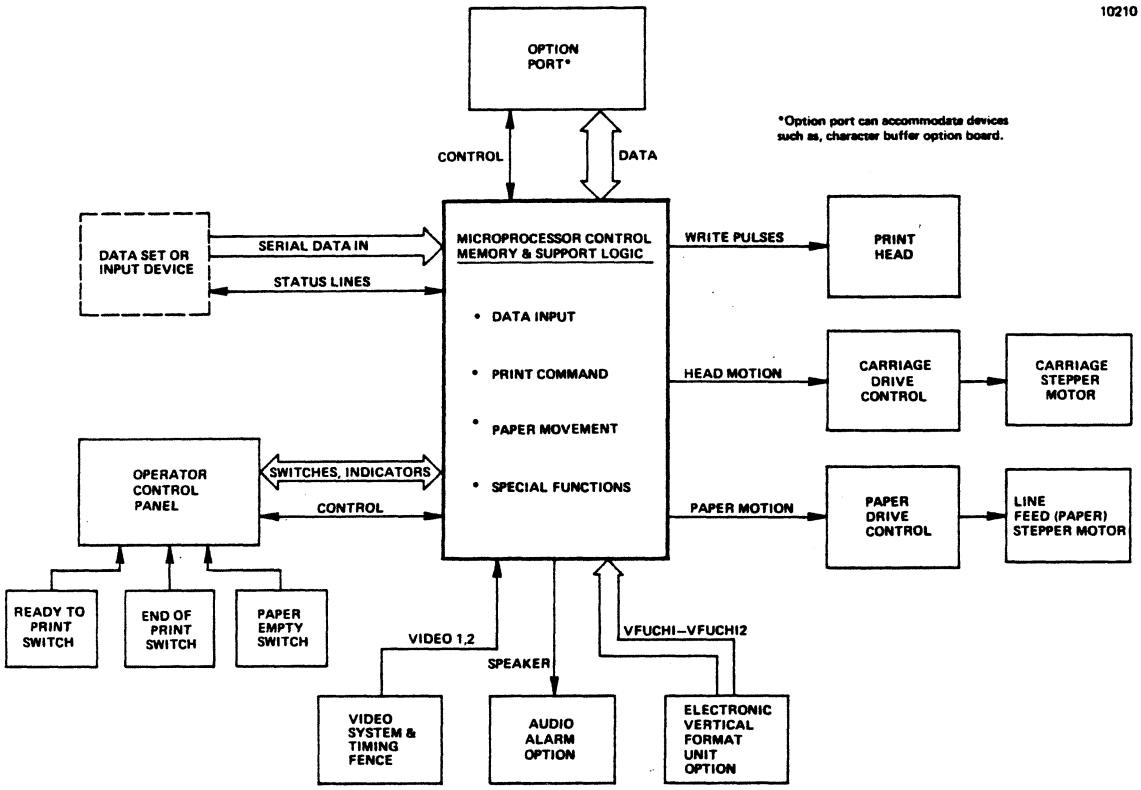

Figure 1-3. PRINTER BASIC BLOCK DIAGRAM

Basically, all printer functions can be grouped into one of three categories: (1) character printing, (2) paper motion, and (3) auxiliary functions such as automatic motor control, audio alarm, etc.

1.4.1 CHARACTER PRINTING (Figure 1-5)

In the printer, characters are printed by selectively activating the print wires aligned in a vertical column in the print head. As the head moves across the paper, the appropriate print wires are momentarily activated, driving them against the ribbon, paper and platen to form the specified dot pattern.

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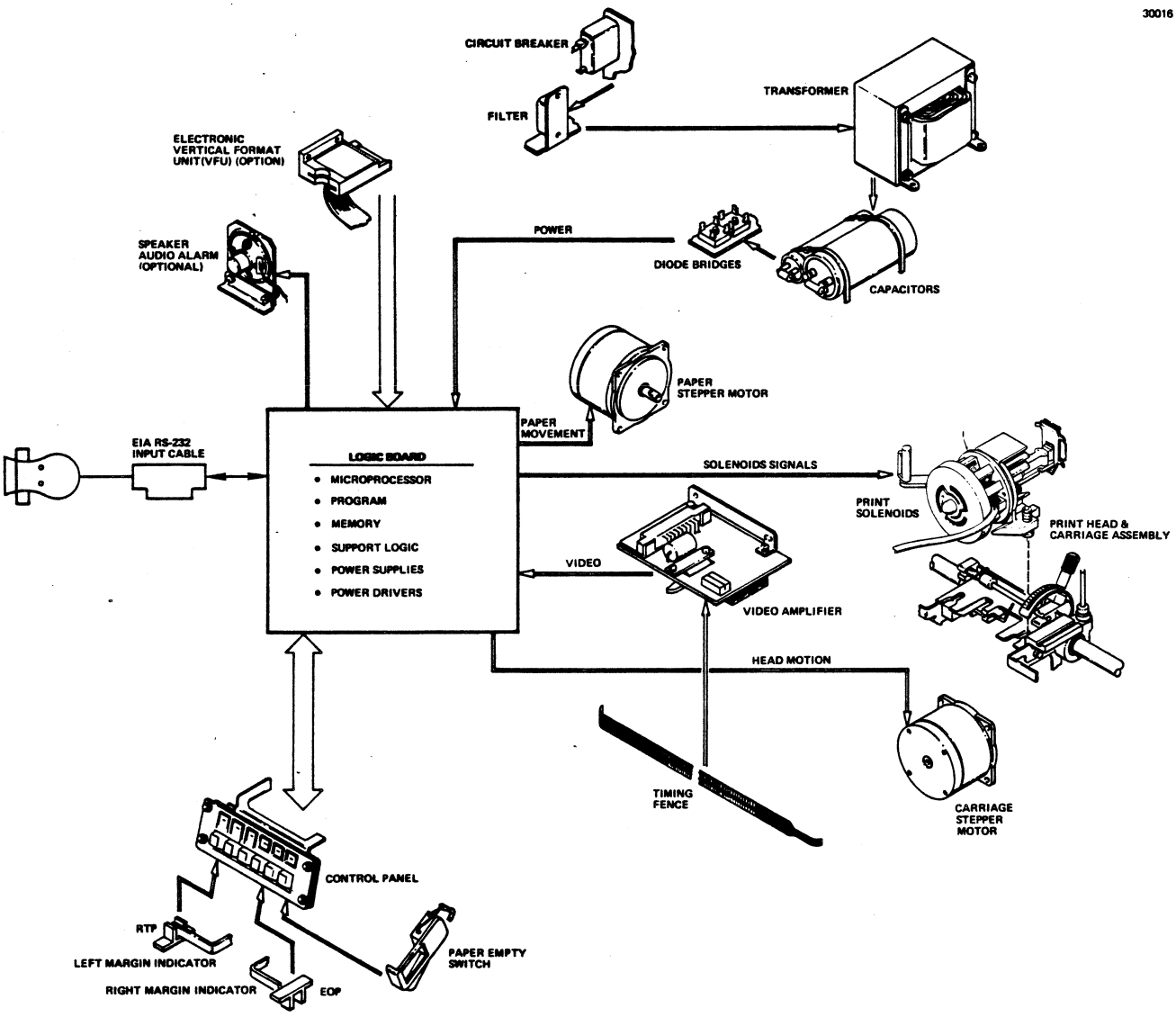

Figure 1-4. PRINTER PICTORIAL DIAGRAM

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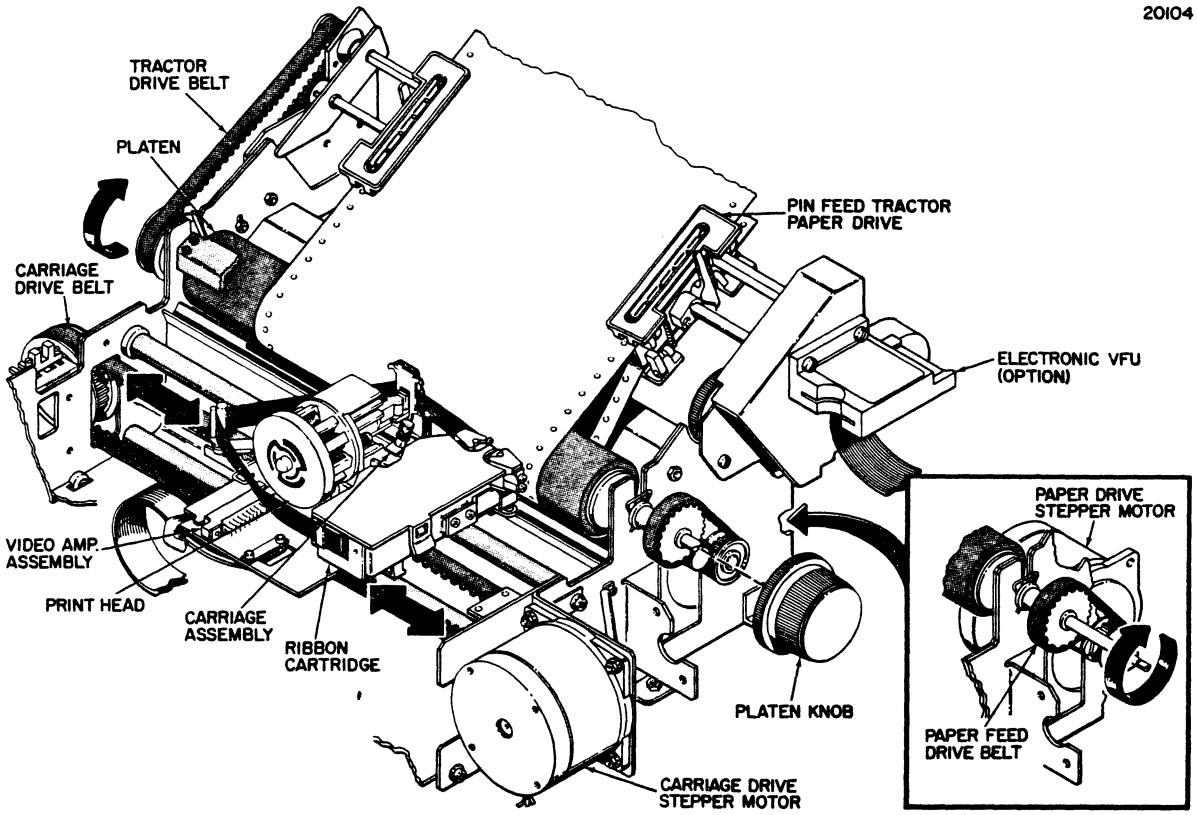

Figure 1-5. CHARACTER PRINTING/PAPER MOTION

The print commands to the print wires are developed by programmable read-only memories (PROM's). To extract print information, the microprocessor addresses a PROM memory location for each column within a character.

As shown in Figure 1-5, the print head is attached to the carriage assembly, which in turn is attached to a rotating carriage drive belt. The carriage is driven in the forward direction or in the reverse direction by the carriage stepper motor which rotates the belt clockwise (forward direction) or counterclockwise (reverse direction).

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1.4.2 PAPER MOTION (Figure 1-5)

Paper can be moved manually by pushing in and rotating the platen knob, or automatically by any of three paper motion commands: line feed, vertical tab and form feed.

Torque from the paper stepper motor is applied to the tractor drive gears. Paper is advanced one line by momentarily activating the paper stepper motor, which turns the drive gears to advance paper by one line. When using the tractor unit with the electronic vertical format option, vertical tab and form feed operations are accomplished by activating the paper stepper motor until the amount of paper movement programmed into the microprocessor has been completed.

The electronic vertical format option allows vertical tab, form feed and bottom of form operations to be controlled electronically by data memory. The memory can be loaded either locally through a hand-fed paper tape reader or remotely by downstream loading on the data lines. The paper tape must be pulled through the reader by the operator each time the printer is powered-up or when a format change is required. The memory holds the "tape image" which is electronically "rotated" as paper is advanced.

If the electronic vertical format option is not used, then a vertical tab operation moves paper 1 inch (6 line feeds) and a form feed operation moves paper 11 inches or 12 inches, as prescribed by the customer. This feature is preset in the option PROM, and also determines forms control if the electronic vertical format option is installed but memory is not loaded.

1.4.3 SPECIAL FUNCTIONS

As a standard feature, the printer contains an automatic motor control which turns off the carriage and paper stepper motors when no data is received. The motors are then automatically turned on whenever a print or paper motion command is received.

Also as a standard feature, the printer has a self-test capability which is activated by depressing the OVERRIDE switch while the printer is deselected. The printer automatically prints out both character sets and the hexadecimal equivalent for each of the 32, 8-bit locations in the option PROM.

An optional audio alarm is available for alerting the operator of a special condition. An audible tone from a speaker is sounded by software command (bell code - 07_{16}) or by a paper empty condition.

In addition to printable character codes, the printer also recognizes certain special control codes. Refer to the operators manual for a list of these control codes and the actions performed upon receiving these codes.

1.5 SPECIFICATIONS SUMMARY

EIA DATA INPUT

Baud Rate	110,150,300,1200,2400,4800,9600 (switch selectable)
Data Format	1 start bit, 7 data bits, 1 parity bit, and 1 or 2 stop bits. This data word must contain 10 or 11 bits.
Input Code	96 character ASCII
Buffers	One line print buffer and 256 character input buffer.
Line Protocol (Buffer Full Indication)	X-On/X-Off or Reverse Channel or Data Terminal Ready (switch selectable)

PRINTING

Printing Method	Impact, character by character, bidirectional
Dot Matrix	Standard - 7x7 dot matrix (7 pins high), 7x9 or 9x9 dot matrix (9 pins high)
Print Format	10 characters per inch
Number of Copies	Prints original and up to five carbon copies
Character Set	Standard: 96 character ASCII Optional: 96 character sets
Print Speed	180 cps (7x7 dot matrix) 165 cps (9x7 or 9x9 dot matrix)

PAPER ADVANCE

Vertical Format	6 lines per inch
Paper Entry	Rear and Bottom Feed
Auto Line Feed	Automatic line feed on carriage return (DIP switch selectable)
Paper Feed	Rear or Bottom Tractor Feed 17.3 inches (439 mm) maximum paper width 13.2 inches (335 mm) maximum print width

CONTROLS AND INDICATORS

Switches	Standard: Power, Select, LF, Override and TOF Optional: Double LF, 6/8 LPI
Indicators	Standard: Power, Select and Alert Optional: Audio Alarm
Manual Controls	Forms Thickness, Paper Advance, Paper Tensioner

PYHSICAL/ENVIRONMENTAL/ELECTRICAL

Height	8.0 inches (203 mm)
Depth	19.5 inches (495 mm)
Width	24.5 inches (622 mm)
Weight	60 lbs (27Kg) (without stand)
Temperature	Operating: 40° to 100°F (44° to 38°C) Storage: -35° to 130°F (-37° to 55°C)
Humidity	Operating: 20% to 90% (No Condensation) Storage: 5% to 95% (No Condensation)
Input Voltage	60 Hz; 115VAC, +10%/-15% of nominal 50 Hz; 230VAC, +10%/-15% of nominal

SECTION 2
INSTALLATION/SET-UP

2.1 INTRODUCTION

This section contains installation, floor planning and set-up procedures. All other operating notes and procedures are contained in the Model 704 Operator's Manual.

2.2 FLOOR PLANNING

Space requirements may be determined from Figure 2-1.

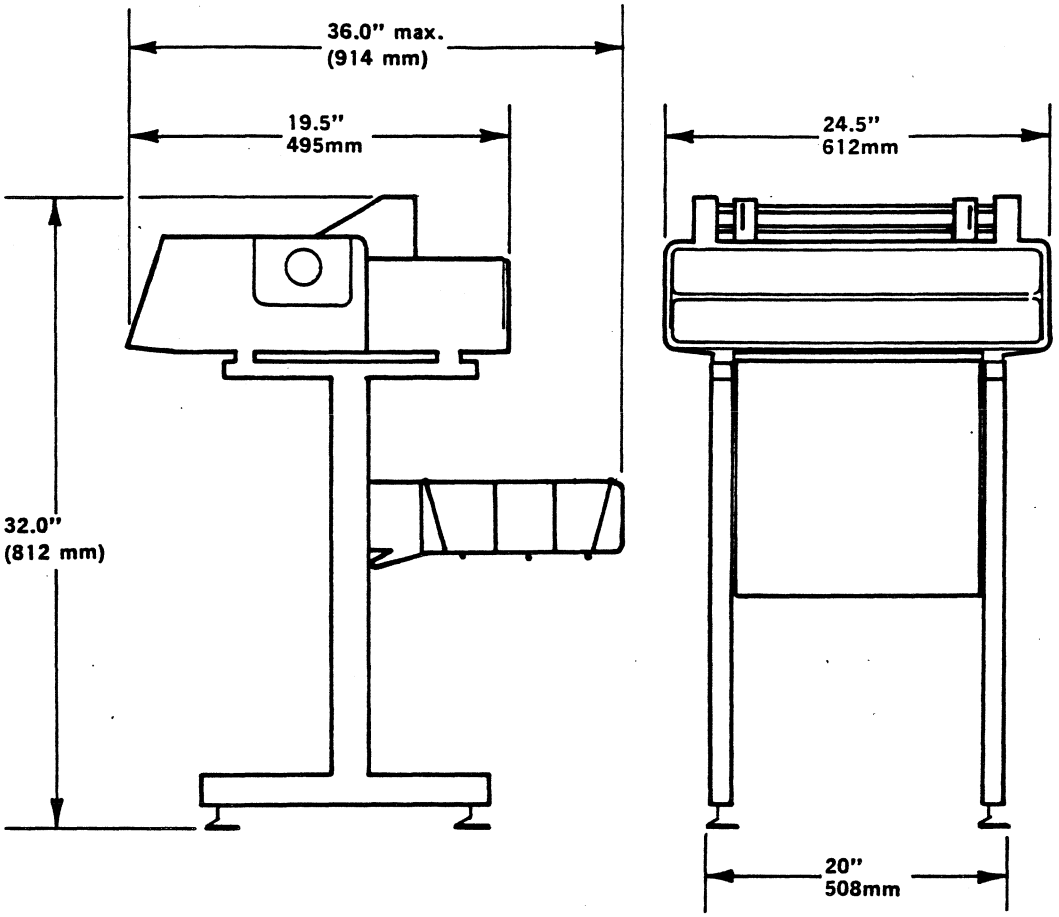

Figure 2-1. PRINTER OUTLINE DRAWING

WEIGHT

Printer 60 lbs (27Kg)
Stand 25 lbs (11.4Kg)

TEMPERATURE

Operating: 40° to 100°F
(4° to 37°C)

Storage: -40° to -160°F
(-37° to 54°C)

ELECTRICAL REQUIREMENTS

50/60 Hz, 115/230 VAC; +10%/-15% of nominal tappable transformer (100, 110, 115, 120, 200, 220, 230, 240 VAC)

Power Cord: 12 feet long

HUMIDITY

Operating: 20% to 90% (no condensation)

Storage: 5% to 95% (no condensation)

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2.3 SET-UP PROCEDURES (Figure 2-2)

1. Note any discrepancies in general printer appearance.

2. Remove the top plastic cover and manually move the print head from the left to right. ENSURE THE OPTICS BLOCK OF THE VIDEO AMPLIFIER DOES NOT CONTACT TIMING FENCE. Timing fence may be damaged by improper alignment of optics block.

3. Manually move the print head from left to right and ENSURE CARRIAGE ARMS DO NOT CONTACT THE READY TO PRINT AND END OF PRINT SWITCHES.

4. Loosen and move penetration control knob backwards, (away from platen) as far as possible and insert paper into printer as described in the LOADING PAPER section of the OPERATOR'S MANUAL.

5. Adjust print head penetration for optimum print quality as follows:

   SINGLE PART FORMS:

   A) Loosen and move penetration control knob as far forward as possible.

   B) Tighten penetration control knob.

   MULTI-PART FORMS:

   A) While manually moving print head across the page, increase penetration by moving knob forward until smudging occurs.

   B) Back knob off just enough to prevent smudging.

   C) Tighten penetration control knob.

6. Plug printer into appropriate AC outlet. ALWAYS USE A 3-WIRE GROUNDED OUTLET.

7. Set power switch on rear of printer to the ON position.

8. Ensure SELECT lamp on operator's panel is extinguished.

9. Depress Top of Form switch on operator's panel and rotate platen knob to adjust paper to top of form position.

10. Ensure power switch on rear of printer is OFF and connect printer to input device via interface connector.

11. Set power switch to ON position and depress SELECT switch to enable printer to receive data.

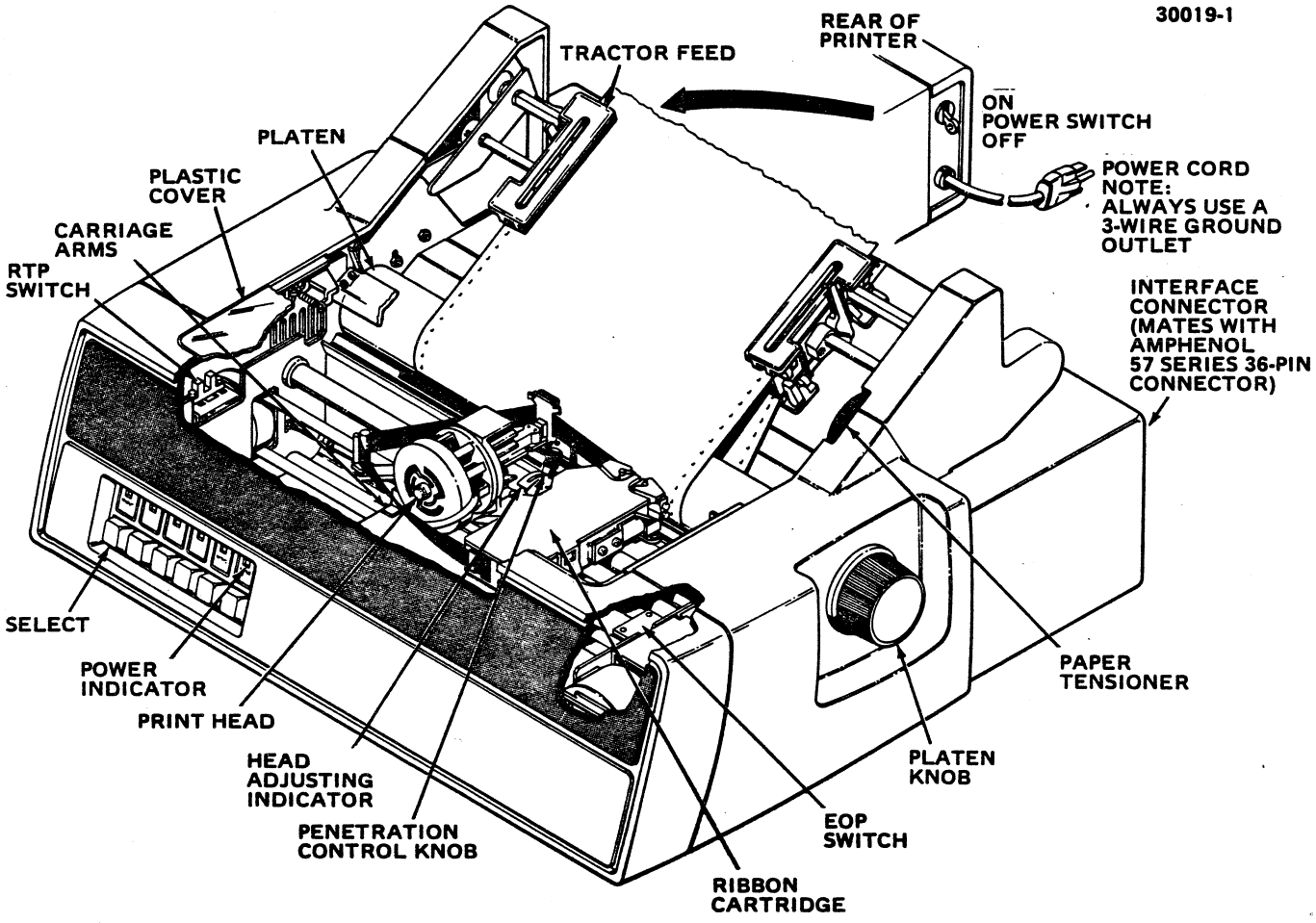

Figure 2-2. SET-UP PROCEDURES

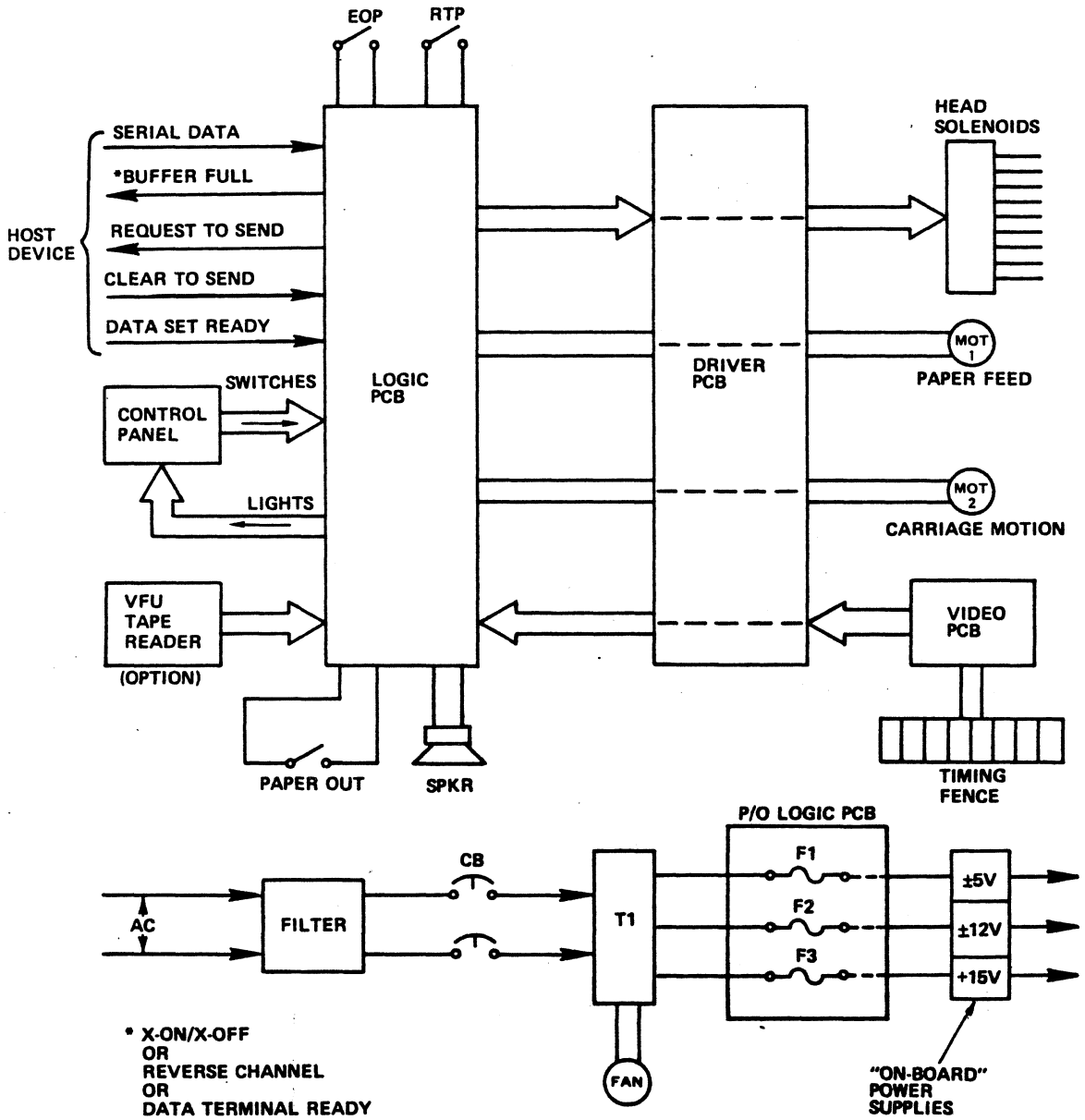

Figure 3-1. OVERALL BLOCK DIAGRAM

SECTION 3
THEORY OF OPERATION

3.1 OVERALL OPERATION

3.1.1 INPUT/OUTPUT SIGNALS (Figure 3-1)

Input/output paths and associated hardware devices are shown in Figure 3-1. Three pc boards control all printer operations. The video PCB receives and shapes the timing pulses from the timing fence. These pulses synchronize the firing of the print head solenoids with the carriage position. The driver PCB provides the current source for the solenoids and the paper feed and carriage drive motors. All input/output data is processed by the logic PCB. It receives the serial input data from the host device and responds within one of three operator selectable ways to define the buffer status. All printer operations are controlled by the logic PCB using end-of-print (EOP) and ready-to-print (RTP) signals provided by right and left margin photo-detectors in conjunction with the input data, video amplifier, timing pulses, and external commands from the control panel switches.

3.1.2 MICROPROCESSOR CONTROL

The printer electronics uses an interrupt driven microprocessor with a bus oriented structure. Memory reference instructions (MRI's) provide direct processor control for all input/output functions other than interrupts. Software detection of the 132nd input character or a control character initiates the printing of each line of data. After each column of dots is formed, a video interrupt (VIDINT) is generated from the timing fence to step the program logic to the next sequential dot column. When the interrupts have been serviced (software or VIDINT), the microprocessor polls the control panel and the optional VFU repeatedly while the electronics continues to load the next line of input data. The polled devices are serviced via MRI's as required until the software flags the beginning of another printed line with the accompanying VIDINT signals. This asynchronous operation keeps the loading of input data independent of the microprocessor routines. As soon as one line is accumulated, the microprocessor switches to printing that line by operating the print mechanism. Asynchronous operations may occur during the print cycle because of the relative timing between the mechanical operations of the printer and the electronic operations of the microprocessor. For example, the time between VIDINT pulses (adjacent print columns) is approximately 500 microseconds. One cycle of the microprocessor requires 500 nanoseconds. Thus, as many as 1000 microprocessor instructions may be executed "in between" the printing of each column of dots.

3.1.3 MEMORY ORGANIZATION

The printer electronics uses approximately 15K memory locations distributed among fifteen logic devices. The 15K, 8 bit locations are divided into 1K "slices" and allocated as shown in Figure 3-2, a memory map.

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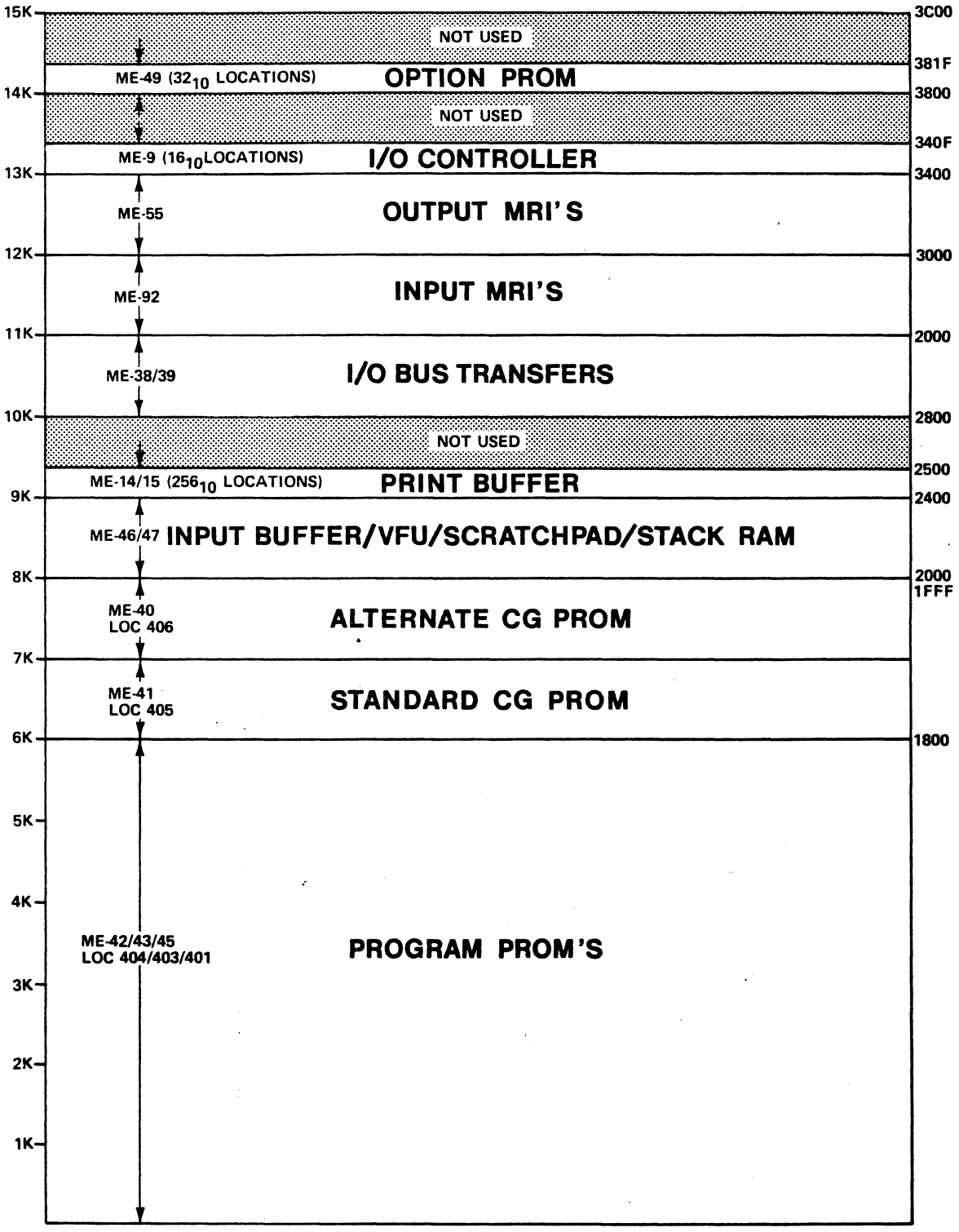

Figure 3-2. MEMORY MAP (Sheet 1 of 2)

The firmware program occupies the first 6K locations. The standard character generator firmware occupies the next 1K and the alternate character generataor the last 1K of the first half of memory. These 8K locations are contained in four 2K PROM's (ME 42/43/45) and two 1K PROM's (ME 40/41).

A scratchpad memory, which also stores VFU data and the stack RAM, occupies the next 1K locations provided by two 1K x 4 bit RAM's ME-46 and 47. These RAM's also contain the 256 character input buffer which provides temporarty storage for the de-serialized characters.

The first 256 locations above 9K (2400-24FF hex) are for the print buffer RAM (ME-14/15). This is a one line buffer for the received data from the input buffer. The rest of the 9K to 10K slice of memory is not used.

Locations 10K to 13K (2800-3400 hex) are reserved for I/O data manipulation and instructions, although only a small portion of each 1K slice is required.

The I/O controller (ME-9) for the MPU contains 16 locations in addresses 3400 to 340F hex. ME-9 contains a one character receiver buffer and a one character transmitter buffer to serialize and de-serialize data. The rest of the 13K to 14K slice is not used.

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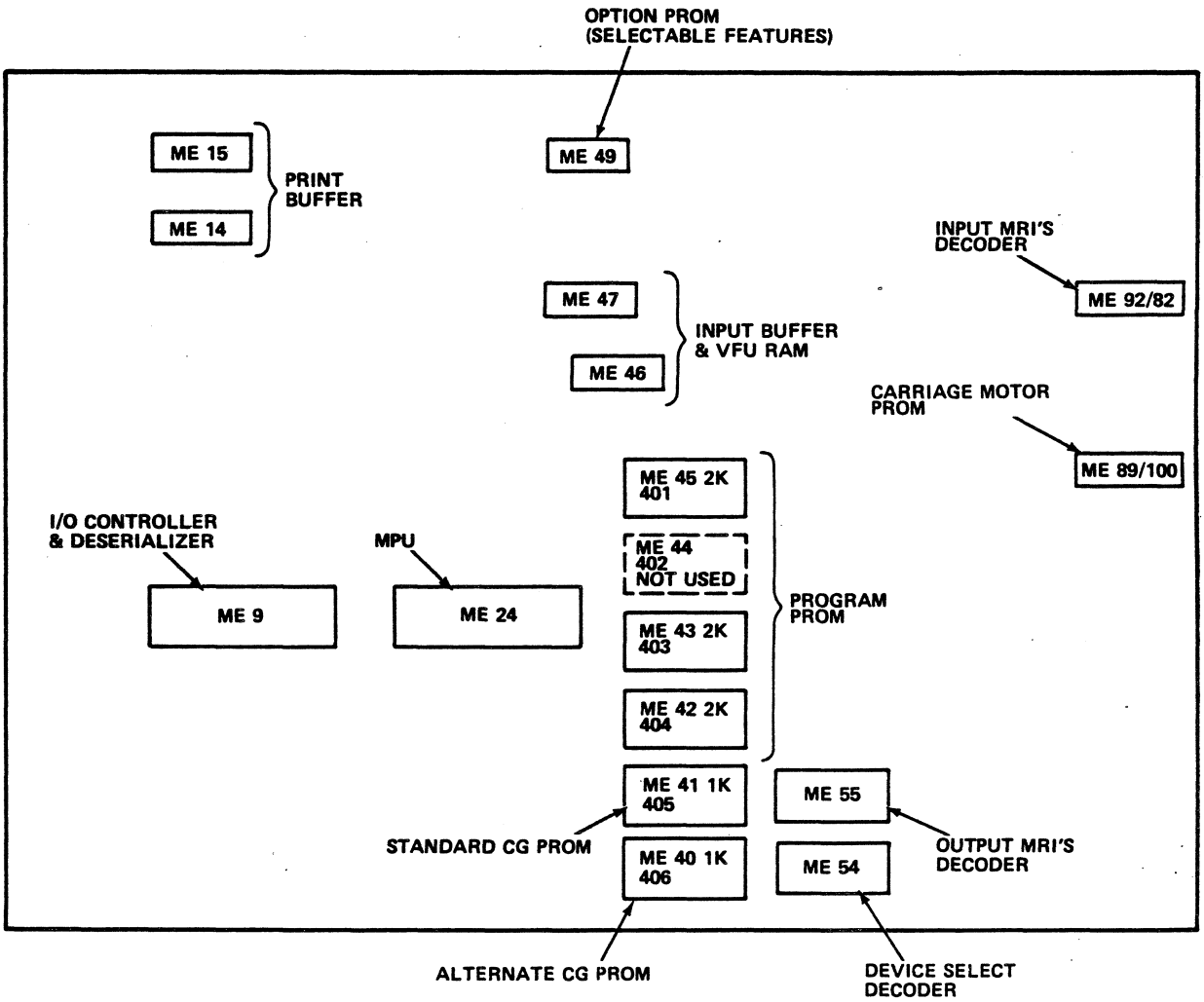

25 Figure 3-2. MEMORY MAP (CHIP LOCATIONS) (Sheet 2 of 2)

The first 32 locations above 14K are used by the option PROM (ME-49). The rest of 16K memory space is not used.

All memory devices are addressed from the MPU using a 16 bit address bus. Only the first 14 bits are used to address 15K locations. The address decoding scheme and a description of the input and output memory reference instructions are provided in paragraph 3-7.

3.2 MICROPROCESSOR (MPU)

The 8080A is an 8-bit parallel, microprocessor unit (MPU) contained on a single 40-pin, LSI chip (Figure 3-3). It transfers data and internal state information over an 8-bit, bidirectional data bus. Memory and input/output device addresses are transmitted over a separate 16-bit address bus. Six timing and control outputs (SYNC, DBIN, WAIT, WR(N), HLDA and INTE) are generated by the 8080A, while four power inputs (+12V, +5V, -5V, and GND) and two clock inputs (Ø1 and Ø2) are received. Instructions are located in ROM memory, from where they are fetched and executed sequentially. There are over 100 separate instructions possible.

3.2.1 ARCHITECTURE

The MPU contains the following:

- o Instruction register
- o Program counter
- o Memory address register
- o Stack pointer
- o Arithmetic and logic unit
- o Bidirectional, 3-state data bus buffer
- o Other registers and logic elements

Figure 3-4 shows the functional blocks within the MPU.

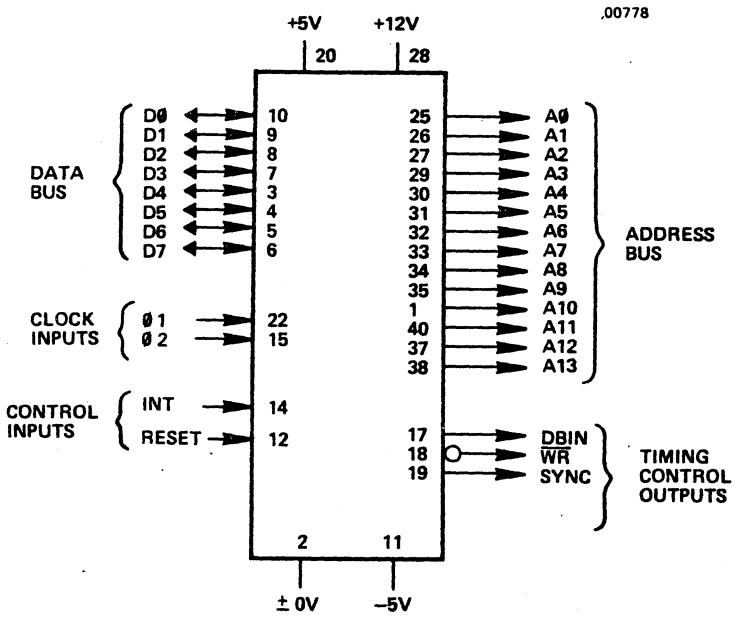

Figure 3-3. 8080A MICROPROCESSOR PIN DESIGNATIONS

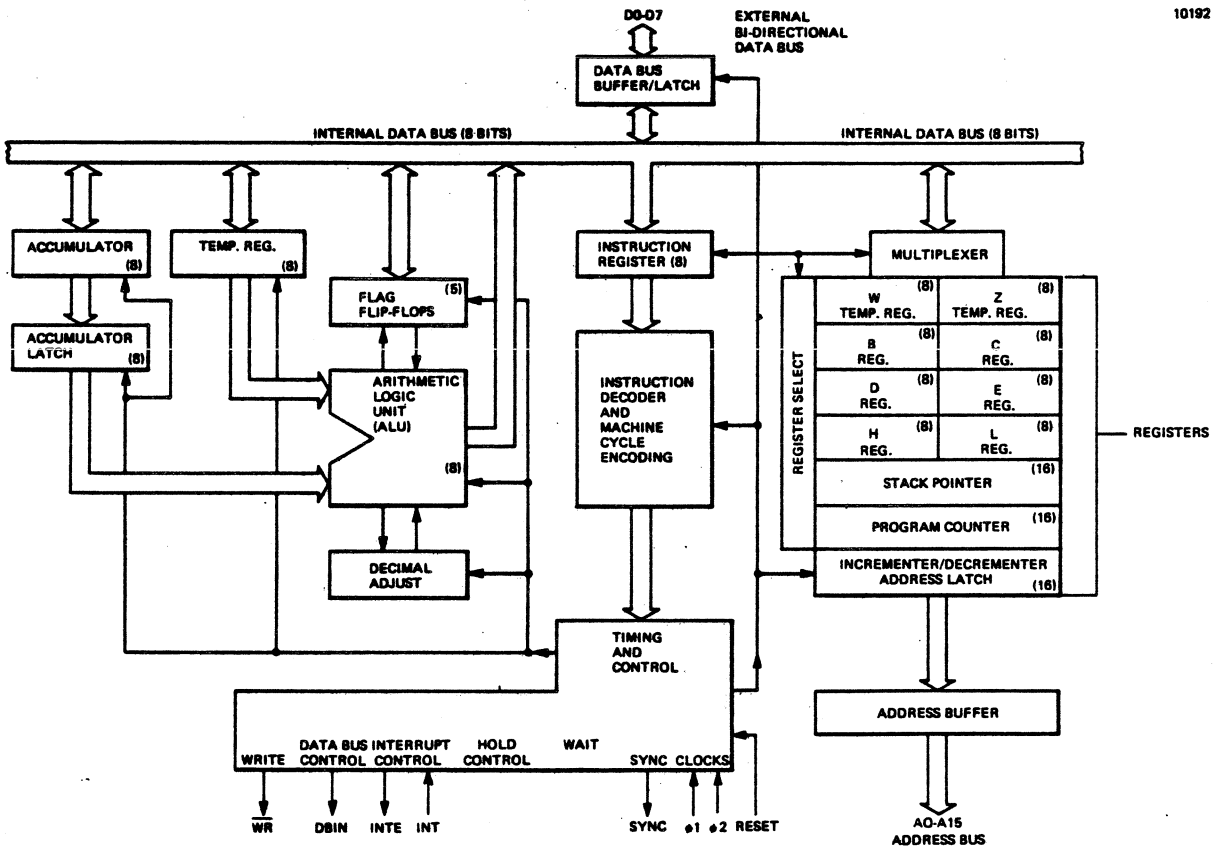

Figure 3-4. MPU BLOCK DIAGRAM

The instruction register holds the 8-bit instruction code. The program counter maintains the memory address of the current program instruction and is incremented automatically during every instruction fetch. The memory address register, referred to as the H, L register pair, is made up to two 8-bit registers and is used to address memory during read and write memory instructions. The stack pointer maintains the address of the next available main program instruction while an interrupt subroutine is being executed. The arithmetic and logic unit (ALU) performs the computational and logical operations. The remaining elements internal to the MPU perform the input and output operations over the data bus.

The data bus isolates the internal bus from the external data bus (D0-D7). In the input mode, the contents of the internal bus are loaded into a latch that drives the data bus output buffers. During the input mode, data from the external data bus is transferred directly to the internal bus.

3.2.2 TIMING

Timing is developed from a 12MHz oscillator that is divided to produce a two phase oscillator with a frequency of 2MHz. Clock signals Ø1 and Ø2 are converted from TTL levels to MOS levels before going to the MPU. Paragraph 3.4 covers system timing in detail.

3.2.3 BASIC MPU OPERATION

Operation of the MPU is divided into time periods called "cycles" and "states." There are two types of cycles: instruction cycles and machine cycles. The material that follows is summarized in the timing chart in Figure 3-5.

3.2.3.1 Instruction Cycle

An instruction cycle includes both the fetching of the instruction from memory and the execution of the instruction. Each instruction can be either one, two, or three 8-bit bytes in length. Multiple byte instructions are stored in successive memory locations.

3.2.3.2 Machine Cycle

A machine cycle is required each time an I/O device or the memory is accessed. Each instruction cycle can contain from one to five machine cycles. There are ten different types of machine cycles possible, as follows:

1. Instruction Fetch
2. Memory Read
3. Memory Write
4. Stack Read
5. Stack Write
6. Input
7. Output
8. Interrupt Acknowledge
9. Halt Acknowledge (not used)
10. Interrupt Acknowledge while in Halt (not used)

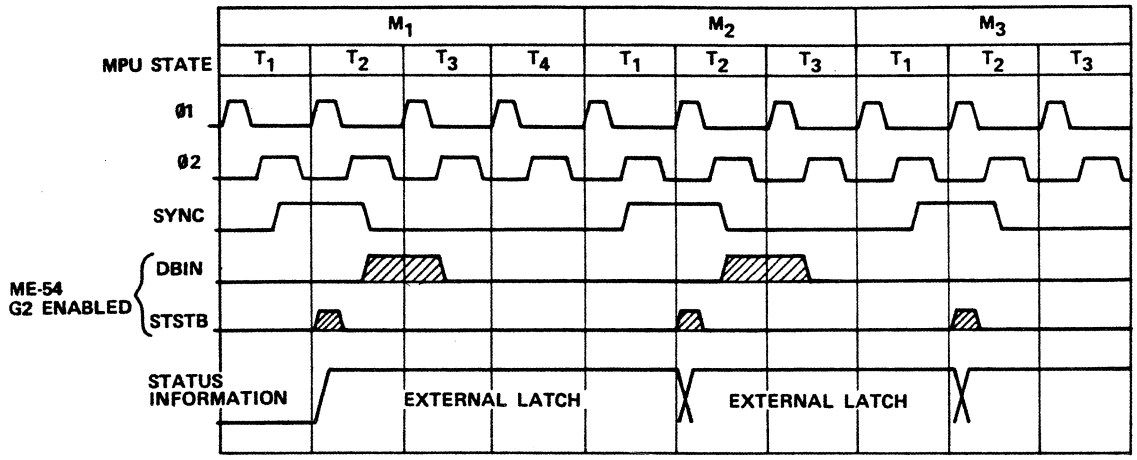

Figure 3-5. TYPICAL OUTPUT INSTRUCTION CYCLE TIMING

3.2.3.3 States

A state is defined as the time interval (500 ns) from leading edge to leading edge of the Ø1 clock. There are six possible states, identified as T1 through T5 and TW (representing "wait"). All machine cycles include T1, T2, and T3. T4 and T5 are omitted during the execution of the instructions not requiring them. The six states are defined as follows:

T1 - During state 1, either a memory address or an I/O device address is placed onto the memory address bus. Also, the MPU places bits of status information on the data bus which identify the type of machine cycle being performed. Following the rising edge of Ø2, the SYNC signal is produced by the MPU, which identifies the beginning of a machine cyle. Refer to Figure 3-5.

T2 - During state 2, the MPU monitors its RDY input. If it is high, the MPU goes on to state 3. If it is low, the MPU goes on the "wait" state. In the printer, the RDY input is tied high. This causes T3 to always follow T2.

During machine cycles that bring data into the MPU (Instruction Fetch, Memory Read, Stack Read, Input and Interrupt Acknowledge), the Data Bus In signal (DBIN), is developed at Ø2 during T2. DBIN remains high through T2 and into T3. This signal is used by the logic board to provide input data to the MPU.

TW - The wait state provides the MPU delay required for proper memory access. It is not used by the printer.

T3 - during T3 the data or instruction byte is actually transferred between the MPU and memory or an I/O device. The source and destination of the byte is determined by the type of machine cycle being performed. For example, during an instruction fetch cycle, the source of data (instruction byte) is the memory location addressed during state 1; the destination is the MPU. During an output machine cycle, the source is the MPU and the destination is the I/O device selected (addressed) in state 1.

T4 and T5 - These two states are used only when required for manipulation of data within the MPU.

3.2.3.4 System Logic Control

At the beginning of each machine cycle, the MPU issues "status" information on the data bus that indicates the type of cycle about to be performed. The status information provided by the MPU, and the system control signals developed for each of the ten types of machine cycles, are shown in Figure 3-6.

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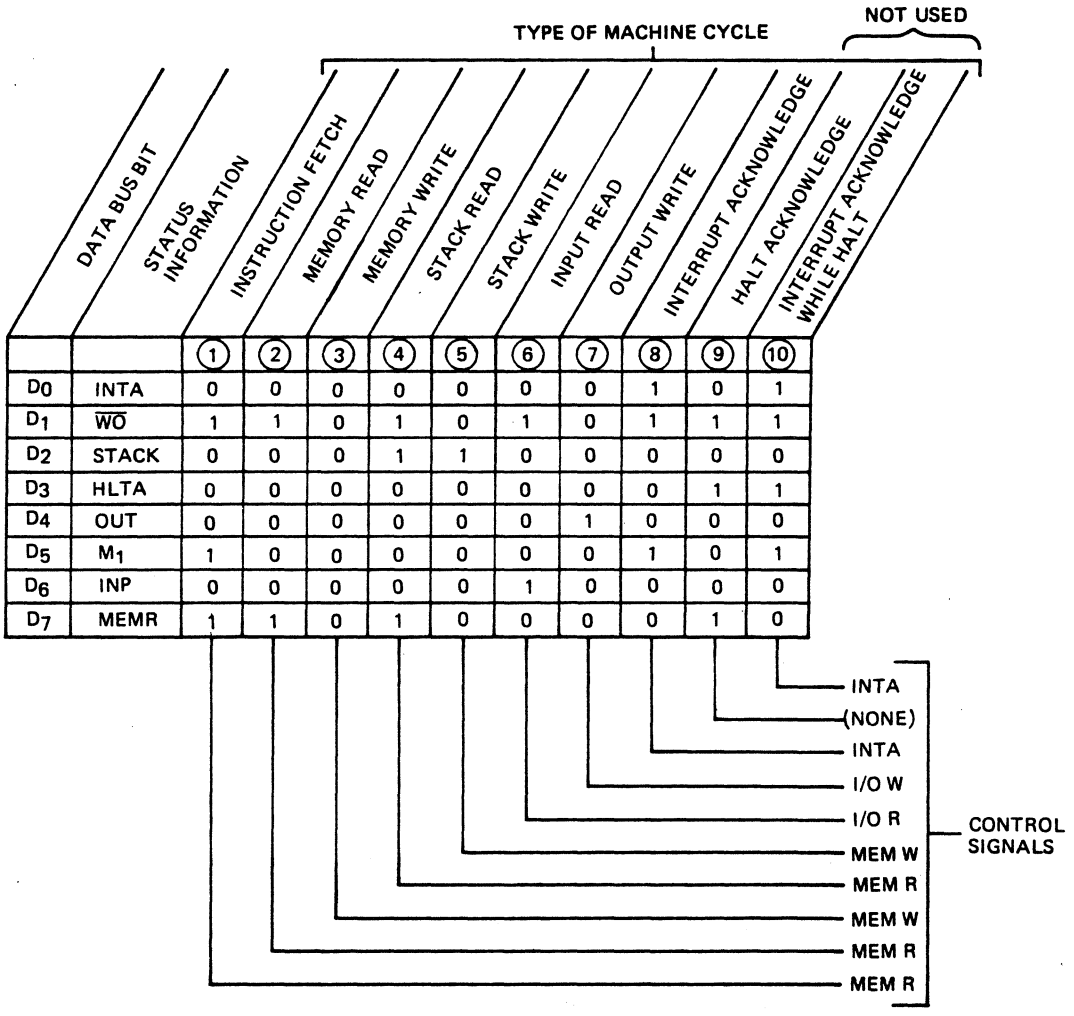

		1	2	3	4	5	6	7	8	9	10
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

Figure 3-6. MPU STATUS WORD

3.2.3.5 Addressing

The 16 address lines contain the binary address of the device currently being accessed. These lines allow the MPU to address 65,536 different addresses although the logic board uses only the first 15,336 addresses. All 16 lines are buffered by ME32/2 and ME33/2 to provide drive for all devices connected to the address bus.

3.2.3.6 Data Buses

Data transfer in and out of the MPU is accomplished via the 8-bit bidirectional data bus (DBUSB0 - DBUSB7). A detailed description of bus operation is contained in paragraph 3.3.

3.2.3.7 Control Lines

These lines control handshaking between the MPU and the remaining logic. The reset line (ME24-12/2) ensures that on power up, the MPU starts executing at location zero with all internal registers and flags reset. C26, R16, and ME84 create a positive reset pulse lasting between 40-60 milliseconds. The HOLD line (ME24-13/2) is not used and is permanently disabled to signal ground. The READY line (ME24-23/2) is held high. The interrupt line (INT) indicates to the MPU that an external event requires immediate attention. The MPU completes the current instruction and then services the interrupt.

When the MPU performs a read function via its data bus, the DBIN (ME24-17/2) signal is activated. This signal, combined with the addresses, activates the enable line for the required device, thus placing data on the data bus. The RAM and PROM's are activated by DBIN. When the MPU performs a write function via the data bus, the WRITE (ME24-18/2) signal is activated. This signal, combined with the correct addresses, activates the required device's input enable line, thus permitting the device to accept the data. The output SYNC signal (ME24-19/2) permits the logic to gate the status word from the data bus to the host device.

3.2.4 MICROPROCESSOR PROGAM

The microprocessor program is a series of coded instructions that provides the machine with its decision-making capability. Memory mapping I/O is used to treat all input and output actions as memory reference instructions (MRI's). Refer to the overall memory map in Figure 3-2 for the allocations.

After the printer has been initialized, the program progresses into the main loop. The main program loop periodically branches off into subroutines which perform specific operations. Flow charts of the major subroutine and interrupt routines are located at the end of this section. A list of the routines follows:

	Name	Mnemonic
1.	Print Routine	PRINT
2.	Video Interrupt Routine (With Print Only)	VIDINT
3.	Carriage Drive Interrupt Routine	CRMT
4.	Paper Drive Interrupt Routine	STMT
5.	Control Character Interrupt Routine	CONCHR
6.	VFU Paper Tape Load Routine	VFUCH
7.	Self-Test Routine	SELFTEST

3.3 BUS STRUCTURE

3.3.1 GENERAL DESCRIPTION (Figure 3-7)

Two, 8 bit data buses and a 16 bit address bus transfer all data in and out of memory and control the print mechanism. Figure 3-7 shows a simplified diagram of the two data buses. The address bus is shown in detail with the two data buses in Figure 7-1.

The two data buses in Figure 3-7 are designated the I/O bus and the memory bus. As shown, the input devices and output devices connect to the I/O bus via a transceiver. This bi-directional device is switched on and off by the microprocessor (MPU) to either send or receive data to or from the I/O bus and to or from the memory bus. Input devices consist of video pulses from the timing fences, the control panel switches, the ready-to-print switch (RTP) and the end-of-print switch (EOP). Output devices include the control panel lights and the print mechanism which consists of three devices:

1. Carriage Stepper Motor
2. Paper Stepper Motor
3. Print Head Solenoids

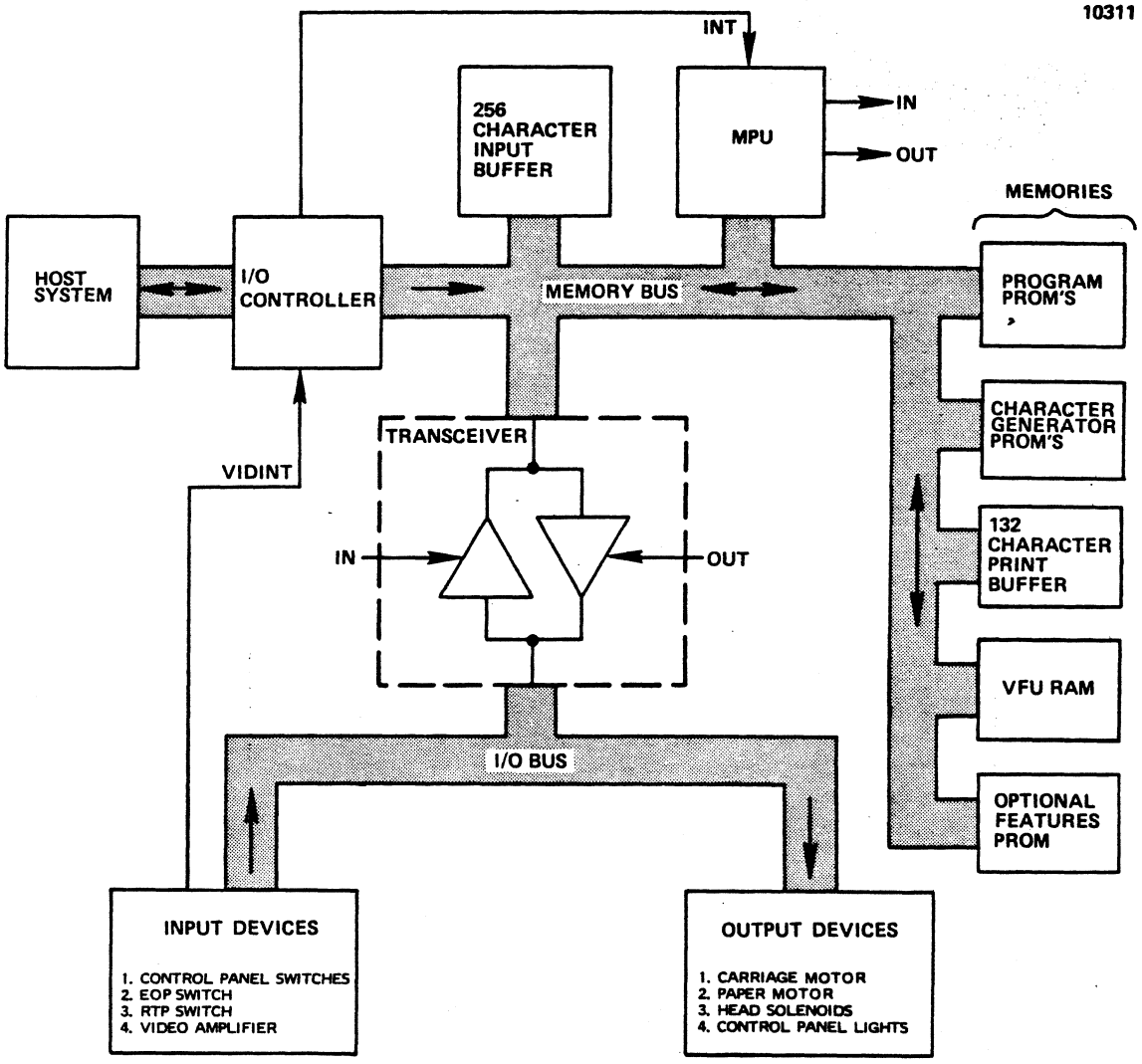

Figure 3-7. BUS STRUCTURE BLOCK DIAGRAM

Serial data characters are loaded from the I/O controller to the input buffer independent of the operation of the MPU and the printer mechanism. When a complete line of data is received or the maximum line length is reached the data characters are transferred to the print buffer. Data characters are then processed in between any other printer operations on a time sharing basis until the print buffer is empty.

The memory bus transfers data characters from the print buffer to the MPU, one character at a time. The MPU then accesses the corresponding locations in the character generator PROM's to obtain the matrix of dots, one column at a time. The transceiver gates the column code to the head solenoids via the memory bus and the I/O bus.

The memory bus also connects the program PROM's to the MPU and two other memory devices: (1) The vertical format unit RAM provides electronic storage for forms handling, (2) The optional features PROM may be used to control character responses and other user-orineted features.

NOTE
THE INPUT BUFFER IS PHYSICALLY PART OF THE VFU RAM.

3.3.2 DETAILED DESCRIPTION (Figure 7-1)

Figure 7-1 shows the bus structure in detail with all associated logic chips. The chips are identified by an abbreviated reference designation and the sheet number of the schematic that shows the entire chip. For example, the MPU is chip number ME-24 and is shown on Sheet 2 of the detailed schematic. It is abbreviated as 24/2 on the functional schematic. The abbreviated numbers are used on all functional schematics for easy cross reference to the schematic.

The 16 bit address bus (bits BADB01-15) originates in the MPU and is used by the following chips:

1.	Print Buffer	ME-14/15
2.	I/O Controller	ME-9
3.	Program PROM's	ME-42/43 and 45
4.	Character Generator PROM's	ME-40/41
5.	Optional Features PROM	ME-49
6.	Input Buffer/VFU RAM	ME-46/47
7.	Device Select Decoder	ME-54
8.	Output MRI Decoder	ME-55
9.	Input MRI Decoder	ME-92

Data on the I/O bus (bits BUFDB0-7) originates or terminates in the following devices:

1. Decoder ME-37
2. Video Amplifier Board
3. VFU Reader
4. Printer Mechanism
5. Control Panel

The I/O bus is connected to the memory bus (bits DBUSB0-7) and vice-versa via transceiver ME-38/39. The memory bus (bits DBUSB0-7) is a bi-directional bus as is the I/O bus. It sends and receives data to and from the print buffer, I/O controller, MPU and VFU/scratchpad RAM. The program PROM's, character generator PROM's and optional features PROM place data on the bus for manipulation by the MPU.

All activity on the bus is under program control of the MPU. Firmware instructions stored in program PROM's ME-42/43/45 are transferred to the MPU over the memory bus. The MPU executes the instructions by controlling the bits on the address bus to select the appropriate device via decoder ME-54 or by placing a memory reference instruction (MRI) on the address bus for decoding by the input MRI decoder ME-92 or the output MRI decoder ME-55, depending on the instruction.

3.3.3 INPUT DATA TRANSFERS

Data flow within the bus structure may be separated into communications with the devices on the I/O bus and receiving serial input data. I/O bus transfers are between the MPU and:

1. Video Amplifier
2. VFU Reader
3. Printer Mechanism
4. Control Panel

Input data characters are received from the host by the I/O controller (ME-9) in RS-232 serial format. The controller de-serializes the bits one character at a time, and temporarily stores one assembled character in its receiver buffer. It flags the MPU (ME-14) when each character is ready to be transferred. The character is then gated onto the memory bus and stored by the MPU in the input buffer (ME-46/47).

This process continues until the carriage return code (CR) at the end of the line is received. The CR causes the MPU to transfer the line from the input buffer to the print buffer (ME-14/15). The print mechanism immediately begins to print that line. The input buffer is then free to receive additional characters or lines of characters from the I/O controller independent of the print buffer and print mechanism operation.

3.3.4 I/O BUS TRANSFERS

Periodically, as part of the main program, the MPU scans the devices on the I/O bus for servicing. Multiplexers ME-60/61/71/72 are four input devices which connect the VFU reader to the I/O bus. (Only two inputs are used).

The VFU data consists of two 8 bit bytes. The MPU activates $\overline{\text{SELP10}}$ and toggles address bit BAD00 and BAD01 to gate each byte onto the I/O bus through transceiver ME38/39 and onto the memory bus DBUSB0-7. The MPU samples bit 14 which is high if a tape is loaded in the VFU reader. This bit corresponds to the VFU load switch signal (VFULSW). Bit 13 comes from the feed hole in the tape and provides a strobe pulse (VFUSTB) on the bit 13 line as the tape is pulled through the reader. Bits 15 and 16 are not used. The 12 channel VFU uses the lower 12 bits. If bit 14 (VFULSW) is low, the MPU executes the firmware program to load the VFU data into the VFU RAM ME-46/47. Otherwise, the MPU continues on to poll the next I/O device.

NOTE

THE $\overline{\text{VFULSW}}$ SIGNAL COMES FROM AN OPTICAL PICKUP IN THE VFU READER THAT SENSES THE PRESENCE OF THE TAPE. AFTER THE TAPE HAS BEEN PULLED THROUGH THE READER, ALWAYS REMOVE IT TO PREVENT CONSTANT ACTIVATION OF $\overline{\text{VFULSW}}$ WHICH MAY CAUSE THE PRINTER TO "HANG-UP."

Data transfers to and from the control panel are gated through transceiver ME77/78. The $\overline{\text{SELP11}}$ signal from device select decoder ME-54 and the READ pulse from the MPU, enable the transceiver. The control panel keyboard bus bits KBB 00-07 are connected to the I/O bus. The MPU addresses the input MRI decoder so as to generate an enable switch output pulse ($\overline{\text{ENSWOP}}$). This pulse samples the following:

X-ON/X-OFF	(DIP 2-5)	- Bit 0
EOP	(Left Margin)	- Bit 2
RTP	(Right Margin)	- Bit 3
DTR	(DIP 1-1)	- Bit 4
REV CHAN	(DIP 1-2)	- Bit 5
LF AFTER CR	(DIP 1-3)	- Bit 6
EIA/CL	(DIP 2-6)	- Bit 7

Bits Ø and 2 through 7 are set accordingly. The MPU addresses the input MRI decoder again to generate an enable serial output pulse ($\overline{\text{ENSERO}}$). It samples the following:

BAUD RATE 1	(DIP 1-6)	- Bit 0
BAUD RATE 2	(DIP 1-7)	- Bit 1
BAUD RATE 3	(DIP 1-8)	- Bit 2
REV CHAN POLARITY	(DIP 1-4)	- Bit 3
PARITY 1	(DIP 2-1)	- Bit 4
PARITY 2	(DIP 2-2)	- Bit 5
DATA BITS	(DIP 2-3)	- Bit 6
STOP BITS	(DIP 2-4)	- Bit 7

The MPU addresses the input MRI decoder again to generate an enable switch panel 2 pulse ($\overline{\text{ENSPN2}}$). This pulse samples the following front panel switch settings:

Select	(SW2)	- Bit 0
TOF	(SW3)	- Bit 1
Line Feed	(SW1)	- Bit 2
Double Line Feed	(SW5)	- Bit 3
Override	(SW4)	- Bit 6
6/8	(SW6)	- Bit 7

This three byte control panel word is acted upon as required by the MPU and is also used to light the appropriate LED's on the control panel. To output data, the MPU addresses the output MRI decoder ME-55 which sends an indicator clock pulse (INDCLK) to a latch in the control panel. The latch stores bits of the KBB00-07 word to light or extinguish the following LED indicators:

Power	(CR1)	- Bit 0
Select	(CR2)	- Bit 1
Alert	(CR3)	- Bit 2
Ready	(CR4)	- Bit 3
Alt. Char.	(CR5)	- Bit 4
On Line	(CR6)	- Bit 5

The video amplifier board is used only when the carriage is moving. During carriage motion, the dual timing fence and optics assembly generate electrical pulses to synchronize the firing of the print head solenoids with the carriage position. These pulses are sensed, shaped and amplified by the video amplifier board. The timing fence consists of a top and bottom fence. Each has alternating clear and opaque lines on them. They are aligned horizontally so that the corresponding electrical pulses are 90° out of phase. This technique provides twice the resolution of one timing fence. In addition, the direction of carriage motion is indicated by the relative phase relationship of the two video signals. Paragraph 3.10 provides a detailed description of the video.

Each edge of the two video signals corresponds to a dot column position for the printed character. Edge detector circuit ME-66/83/85 generates a video interrupt pulse (VIDINT) and sends it to the I/O controller for each edge of the video pulse. VIDINT causes an INT to the MPU telling it that the print mechanism is in position to fire the solenoids corresponding to the next character dot column. The MPU addresses either the standard character generator PROM ME-41 or the alternate character generator PROM ME-40 to obtain the code for the next column of dots.

Additional head position circuits are connected to the I/O bus to allow the MPU to determine the head's instantaneous position at all times. This information is used with the bi-directional firmware to calculate the shortest print path for the next line. If the carriage is moving to the right, multiplexer ME-82 connects the edge detector output to the "cout up" input of head position counter ME-93/94/95. The counter is reset initially by RTP. For right to left motion, the "count down" input is used. The counter provides a 12-bit binary word that divides the printed line into 4096 increments. This provides absolute values at all times. The 12 bit head position word (HDPS00-11) requires two bytes from the MPU. The input MRI decoder is addressed to generate a column 0 through 7 (COLOT7) pulse. This gates bits 0-7 to bus driver ME-79/80 and onto the I/O bus. The second byte (bits 8-11) is accessed by a column 8 through 11 pulse (CO8T11). The HDPS00-11 bits are compared with the print buffer address bits by the MPU. Basically, the print buffer address contains the position of the last character on the next line just before it is printed. By subtraction, the MPU determines which way the head should move to reach the correct position in the shortest time. It controls the REVESE signal to up/down counter ME-90 which determines the direction of carriage motion.

The printer mechanism operation is controlled by four latches and a PROM. The latches store control bits from the I/O bus which send the following signals to the power driver board and onto the printer mechanism:

$\overline{\text{SMT01-04}}$	Four phase inputs to stepper motor for paper motion.
$\overline{\text{CRMT01-04}}$	Same as above except for carriage stepper motor.
$\overline{\text{STMTSL}}$	Stepper motor slew control causes an initial high current flow to overcome inertia of paper motion stepper motor.
$\overline{\text{CRMTSL}}$	Same as above except for carriage motor.
$\overline{\text{CG1-CG9}}$	Character generator output signals that drive the nine head solenoids to fire each column of dots.
Motor Control	Enable signal for power driver board circuits.

The MPU gates the appropriate control bits from the memory bus onto the I/O bus and addresses the output MRI decoder ME-55 to generate the clock pulses necessary to load the bits into the four latches. Latch ME-67 stores the STMT01-04 signals and is loaded by the stepper motor clock (STMTCL). The output latch pulse (OUTLAT) clocks latch ME-68 which stores bits for STMTSL and CRMSTL to the power driver board and the reverse (REVESE) signal to the carriage motor counter ME-90. Enable output 1 (ENBOP1) clocks latch ME-70/81/91 to store the nine bits for CG1-CG9. The MOTOR CONTROL bit is stored in latch ME-69 by enable output 2 (ENBOP2). This latch also stores the SPEAK bit which turns on the paper empty alarm.

When the print cycle is started, the MPU addresses output MRI decoder ME-55 to generate the clock pulse necessary to generate a slew carriage control (SLEWCR) stored in ME-68. For each print column a pulse increments up/down counter ME-90. It counts from 0-7 during forward carriage motion and from 7-0 during reverse. The 3 bit counter output addresses carriage motor PROM ME-89. It contains the correct phase relationships for the four carriage motor signals (CRMT01-04) which drive the carriage to the next print column.

$\overline{\text{ENABLE}}$ output 3 (ENBOP3) is not used.

3.4 SYSTEM TIMING (Figures 3-8 and 3-9)

Basic timing is established by a crystal-controlled 12 MHz oscillator consisting of inverter ME-10 and crystal Y1. As shown in Figure 3-8, the 12 MHz pulses increment divide-by-six counter ME-11 (1, 2 and 3). The 1Q, 2Q and 3Q outputs are ANDed by ME-22 to gate flip-flop 4D on for 83 microseconds once every six clock pulses. This provides Ø1 and Ø2 pulses at a 500 nanosecond rate with the pulse width and relative timing shown in Figure 3-8. The Ø1 and Ø2 pulses are used by the microprocessor to establish each 500 nanosecond machine cycle. A 010 fault detector circuit prevents the counter from shutting off in the event it initially comes on in an illegal condition with 1D and 3D reset and 2D set (010). If this occurs, ME-96 clears all three flip-flops to 000 and the counter runs normally.

The 2 MHz Ø2 pulse train is divided-by-two to generate 1 MHz Ø2BY2 pulses. Two successive Ø2BY2 pulses are used to generate a 1 microsecond external interrupt pulse (EXTINT) to the I/O Controller when a line of data is ready to be printed. As shown in Figure 3-9, the Ø2 pulses are also divided-by-4, 8, and 16. The Ø2BY8, 250 kHz pulses provide a 4 microsecond acknowledge pulse (ACKNLG) to the sender after each input character is received. The 125 kHz OSCXT pulses are available for external clocking applications.

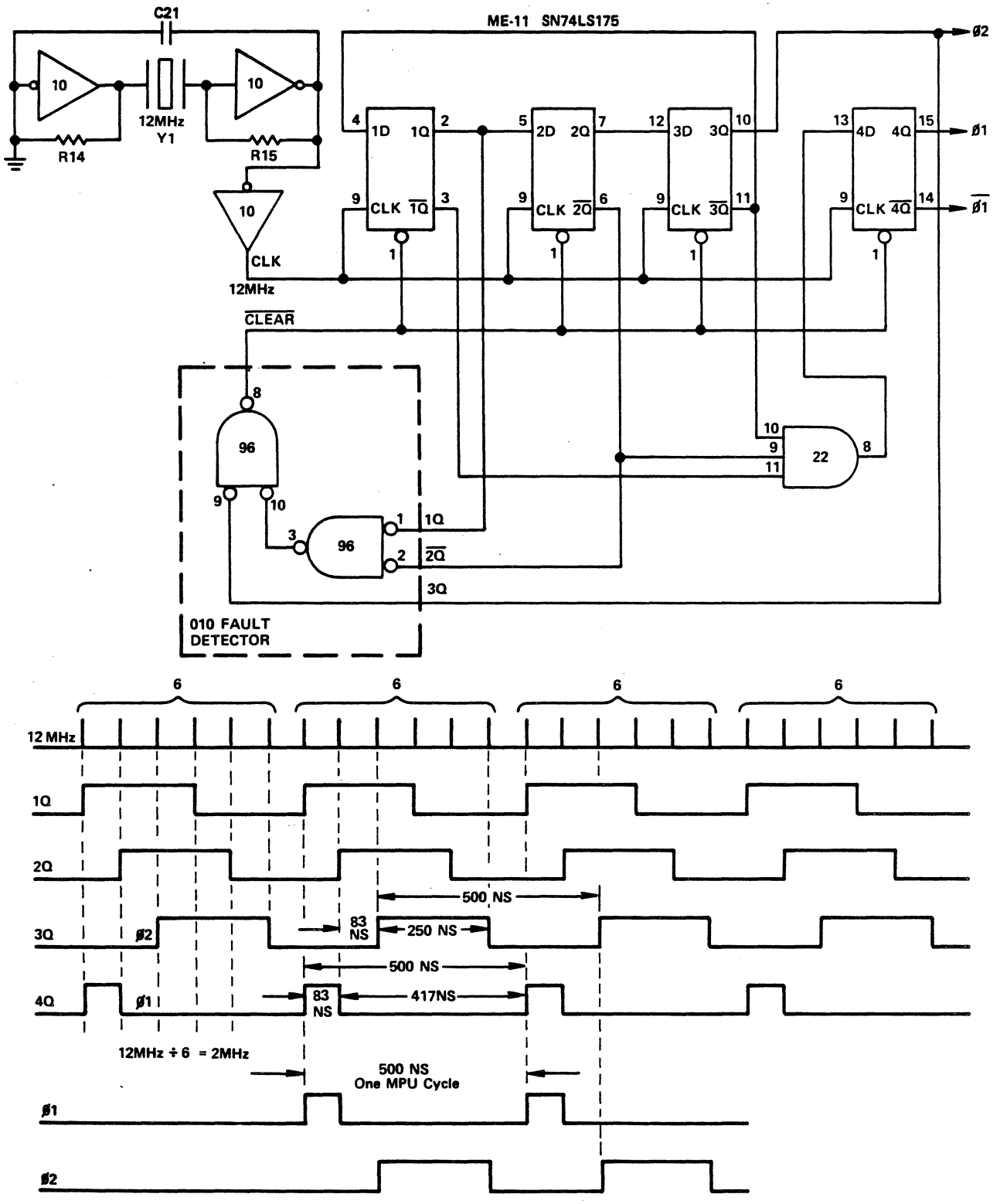

Figure 3-8. ø1/ø2 MPU TIMING CIRCUIT

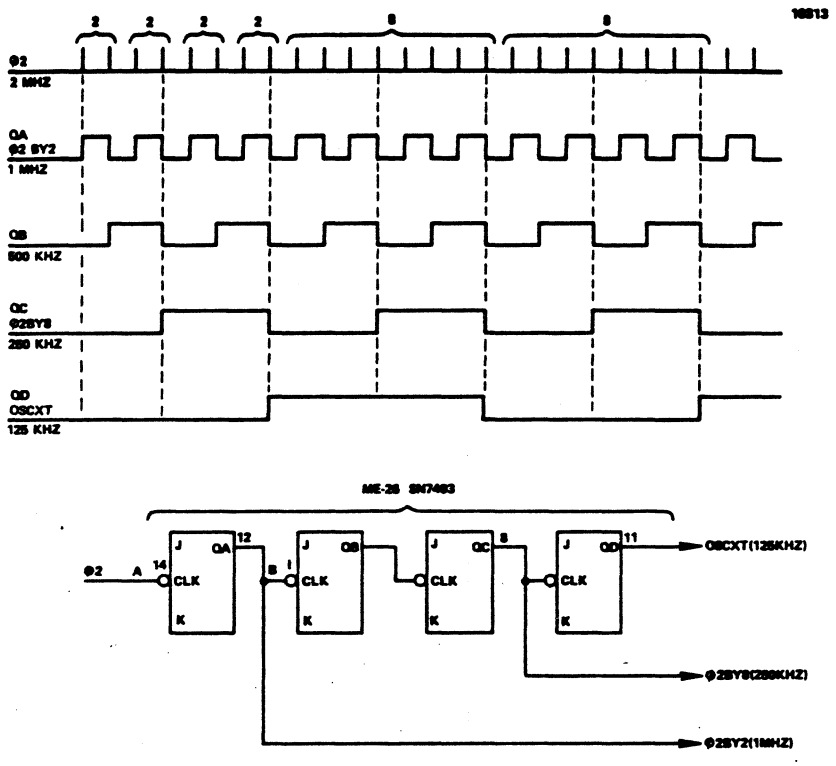

Figure 3-9. Ø2BY2/Ø2BY8 TIMING CIRCUIT

3.5 SERIAL COMMUNICATIONS (Figure 7-2)

3.5.1 INPUT DATA

Asynchronous, 10 or 11 bit serial ASCII characters are de-serialized by the communications portion of I/O Controller ME-9. When the RCV input to ME-9 goes low, the controller automatically shifts in the following data bits until it assembles one character in its receiver buffer. At that time it sets bit 3 of the I/O status word appearing on memory bus bits D_0-D_7 (OBUSØ-7). The next time the MPU polls the I/O Controller to read the status word, the RCV BUFFER LOADED flag (bit 3) is set. Status is ready by placing a 0011 code on the BADØØ-BADØ3 address lines. With bit 3 set, the MPU generates a command on the address lines to read the reciever buffer character onto the memory bus. This command is 0000. The MPU then loads the 8 bit character into the 256 character input buffer ME-46/47 and increments a software counter to keep track of the buffer contents. The I/O Controller is then free to de-serialize the next input character.

The I/O Controller can also tell the MPU that a charater has been assembled by generating an interrupt (INT) signal and simultaneously setting bits 3 and 4 (DBUSB3 and DBUSB4) on the memory bus. This tells the MPU that the interrupt was generated because the receiver buffer is full with one de-serialized character. In either case (INT or status word), the input character is loaded into the input buffer.

The rate at which input data is de-serialized is set by DIP switches behind the front panel. The MPU reads the status of the DIP switches and sends a "load rate register" word to the I/O contoller via the bi-directional memory bus (DBUSBØ-DBUSB7). This word is read into the I/O Controller by sending a 0101 "load rate register" command on the address bus.

00788

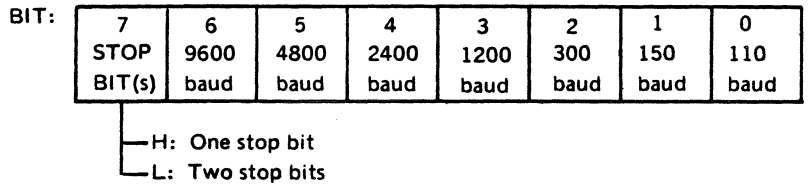

Figure 3-10. DATA BUS ASSIGNMENTS (BAUD RATE COMMANDS)

To receive data, the data set ready (DSREDY) and carrier detected (CARDET) input lines must both be active (EIA +12V nominal). They are applied to the I/O Controller via EIA-to-TTL converter ME-3 and 4 on the external input Ø and 3 lines (XIØ and XI3). The MPU gates the external inputs through the I/O contoller by issuing a "read external inputs" command on the address bus with a 0001 code. The two active external inputs appear on the data bus bits D_0 and D_3 and DBUSBØ and DBUS3 to the MPU. As long as both bits are set, de-serialization by the I/O Contoller is enabled.

When the input buffer accumulates 132 character or receives a control code, it transfers the data to the print buffer, ME-14 and 15, unless the print mechanism is busy printing a previous line. The print buffer contents are then accessed by the MPU one character at a time until the line of data is printed or the control code is acted upon.

3.5.2 OUTPUT DATA

Buffer full or empty status is transmitted by the I/O Contoller to the host in one of three ways as selected by the DIP switches on the operator panel. This status information tells the host to cease transmitting when the 256 character input buffer approaches a full condition to prevent the loss of data. The three methods are summarized below:

Table 3-1 Buffer Full Indication

PROTOCOL	BUFFER STATUS		OUTPUT LINE
	Full (224 chars.)	Empty (132 chars.)	
X-ON/X-OFF	Transmit DC3	Transmit DC1	XMTDAT (BA)
DATA TERMINAL READY	-12V	+12V	DATRDY (CD)
(*)REVERSE CHANNEL	-12V	+12V	XMTRCH (SA)
(*)REVERSE CHANNEL	+12V	-12V	XMTRCH (SA)

(*) Polarity is DIP switch selectable.

On buffer full, the X-ON/X-OFF protocol causes the I/O Controller to transmit the ASCII code for a DC3 in serial form over the XMTDAT line. Baud rate and bit structure are the same as those selected for the input serial data. DC3 is transmitted once and then the XMT line from the I/O Controller returns high. The MPU places the ASCII code for DC3 on the memory bus lines and issues a "load transmitter buffer" command (0110) on the address lines. The I/O Controller then serializes the DC3 character at the selected baud rate and bit structure. The clear to send line (CLRTOS-CB) must be high to enable serial transmission. When 132 characters remain in the buffer, the I/O Controller transmits the ASCII character for a DC1 once. This tells the host to resume inputting to the printer. If the X-ON/X-OFF protocol is not selected, the XMT line remains high.

The DATA TERMINAL READY protocol simply causes the DATRDY (CD) line to stay at +12 volts when the buffer contains 132 or fewer characters. It switches to -12 volts when the buffer has 224 characters and remains at -12 volts until the buffer has been reduced to 132 characters. If this prorocol is not selected the DATRDY line is held at +12 Volts.

REVERSE CHANNEL protocol is similar to DATA TERMINAL READY except it uses the XMTRCH(SA) line and the polarity is DIP switch selectable to have either +12 volts or -12 volts indicate the full or empty status.

If this protocol is not selected, the XMTRCH(SA) line is held at the polarity corresponding to a buffer empty condition.

3.6 CONTROL CHARACTERS

3.6.1 FIRMWARE RESPONSE

The firmware contains programmed responses for the standard 128 ASCII character set to detect special functions such as escape sequences and expanded character codes, as well as normal, printable character responses.

The following characters are action type control codes and are the only ones stored in the input buffer.

DC1	Select
LF	Line Feed
VT	Vertical Tab
FF	Form Feed
CR	Carriage Return
DC3	Deselect
DEL	Delete
GS	STVFULD (Start VFU Load)
RS	SPVFULD (Stop VFU Load)
US	VFUCOM (VFU Command)
ESC	Escape
SO	Expand Full Line

After the MPU executes the action control code, it prints any characters remaining in the print buffer. All other codes are listed below:

NUL	Null	STX	Start of Text
BS	Backspace	ETX	End of Test
HT	Horizontal Tab	EOT	End of Transmission
SI	Shift In	ENQ	Enquiry
DLE	Data Link Escape	ACK	Acknowledge
DC2	Device Code 2	NAK	Negative ACK
DC4	Device Code 4	SYN	Synchronous Idle
SUB	Substitute	ETB	EOT Block
FS	Forward Space	CAN	Cancel
SOH	Start of Header	EM	End of Medium

Until the printer is selected, either locally from the control panel or remotely by the host, no action occurs. Receipt of a DC1 code selects the printer.

Receipt of the SO expand code causes all the following characters to be printed double width. The expand character code sets a flag in the software so that all characters are printed double width until a DEL code or end-of-print command is received.

The printer may be switched between the standard character set and the alternate character set by software control of bit 8. Bit 8 reset enables the standard characters and bit 8 set enables the alternate characters.

The ESC code followed by a hex 33 (ASCII 3) sets bit 8. A hex 34 (ASCII 4) following an ESC code resets bit 8. Receipt of an ESC code sets a software flag. The next character either sets or resets a bit 8 flag depending on whether an ASCII 3 or 4 is received. The condition of this flag tells the MPU which character set to select. Either set bit 8 or reset bit 8 goes high depending upon whether an ASCII 3 or 4 is received. This sets or resets a bit 8 flag that tells the MPU which character set to select.

Receipt of a BELL code causes the $\overline{\text{SPEAK}}$ line to enable ME-5 which triggers 2-second timer ME-27. The timer enables the BEL SPK output of 2.5 kHz oscillator ME-17 which drives the speaker via Q7 and Q8. The BEL SPK output is enabled from the MPU via the BUFDB0-3 lines and latch ME-69 which generate $\overline{\text{SPEAK}}$.

3.6.2 CONTROL CODES

3.6.2.1 Line Feed Code (Octal 012)

If the printer is in the select mode, receipt of the line feed code causes immediate advance of one line.

3.6.2.2 Carriage Return Code (Octal 015)

If the printer is in the select mode and printable characters have been received, receipt of the carriage return code causes immediate printing.

3.6.2.3 DC1 Code (Octal 021)

Receipt of this code allows the printer to be selected remotely, independent of the operator control panel.

3.6.2.4 DC3 Code (Octal 023)

Receipt of this code allows the printer to be deselected remotely, independent of the operator control panel.

3.6.2.5 Vertical Tab (VT) (Octal 013)

If the vertical tab code is received while the printer is selected, the code is processed. The vertical tab will not be processed when the printer is deselected.

If VFU data is loaded in memory, receipt of VT code causes paper to advance to the next sequential vertical tab location.

If VFU data is not loaded in memory, receipt of a VT code causes paper to advance to a pre-set default VT location. Default VT locations are located in every sixth line from the top of form setting.

3.6.2.6 FF Code (Octal 014)

If the form feed code is received while the printer is selected, the code is processed. The form feed will not be processed when the printer is deselected.

If VFU data is loaded in memory, receipt of FF code causes the paper to advance to the next sequential form feed (top of form) location.

If VFU data is not loaded in memory, receipt of an FF code causes paper to advance to a pre-set default FF location. Default FF locations occur in 66 line increments. (72 line increments with 12" TOF option).

When the 6/8 LPI feature is used with an 8 LPI setting, default locations remain set for 6 LPI increments rather than advancing to the next 8 LPI TOF location.

3.6.2.7 DEL Code (Octal 177)

If the DEL code is received when the printer is in the select mode, the printer logic resets to zero.

3.6.2.8 SO Code (Octal 016)

If the printer is selected and receives the "SO" code, it prints characters as expanded characters. This mode is cancelled by a DEL code, an end of print command, or an input prime command.

A maximum of 66 elongated characters may be printed on one line (one half the print buffer size).

3.6.2.9 BEL Code (Octal 007)

Receipt of this code with the printer in the select mode causes the optional speaker to sound a tone for approximately 2 seconds.

3.7 MRI AND DEVICE SELECT DECODING (Figure 7-3)

3.7.1 DEVICE SELECT

The device select decoder may be enabled by $\overline{\text{MEMENA}}$ or BADB13 pulses each time the MPU performs an instruction. The MPU addresses bus places a 4 bit word on the device decoder input (ME-54) which corresponds to one of the 16 possible output device select lines ($\overline{\text{SELPØØ}}$ to $\overline{\text{SELP15}}$). The 16 select lines correspond to the 16 "slices" of memory shown in the memory map in Figure 3-2 and in the following table of address bits (Table 3-3). Bits BADB14 and BADB15 are always low since addresses above 16K are not used. The MPU controls bit BADB10 through BADB13 to select one particular 1K "slice" of memory corresponding to a specific memory device. Lower order addresses within the selected 1K range are sent directly to the device (e.g., program PROM, print buffer, etc.) and are controlled by bits BADB00 through BADB09.

Figure 7-3 is a functional schematic of the device select logic. It also shows the relative timing associated with memory selection. A status strobe pulse ($\overline{\text{STASTB}}$) is generated by ME-18 at the beginning of every T2 state. The data bus bits contain the status of the machine instruction about to be performed at that time. STASTB also clocks flip-flops ME-30 and ME-64 which may be used to enable the G2 input to 1 of 16 decoder ME-54. BUFDB0 is low unless an interrupt acknowledge instruction follows. In that case ME-54 is inhibited by INT ACK. If a memory read instruction follows, BUFDB7 is high. This activates the memory enable line ($\overline{\text{MEMENA}}$) and ME-54 G2 via ME-63 and ME-62, respectively. $\overline{\text{MEMENA}}$ is used for the lower 8K of memory which accesses the program PROM's and the character generator PROM's. The upper 8K is selected by bit BADB13 high as shown in Table 3-2. This bit is inverted by ME-84 and enables G2 via ME-63 in place of $\overline{\text{MEMENA}}$. The G1 input to ME-54 is held active low by BADB14 and BADB15 low.

TABLE 3-3 MEMORY ADDRESS BITS

Address Range	BADB 15	14	8K 13	4K 12	2K 11	1K 10	9	8	7	6	5	6	4	3	2	1	0	Select Line (SEL)	Memory Device	Chip No.
0K-1K	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	P00	Program PROM	ME-43
1K-2K	0	0	0	0	0	1												P01	Program PROM	ME-43
2K-3K	0	0	0	0	1	0												P02	Program PROM	ME-45
3K-4K	0	0	0	0	1	1												P03	Program PROM	ME-45
4K-5K	0	0	0	1	0	0				0 - 8K								P04	Program PROM	ME-42
5K-6K	0	0	0	1	0	1												P05	Program PROM	ME-42
6K-7K	0	0	0	1	1	0												P06	Standard C. G.	ME-41
7K-8K	0	0	0	1	1	1												P07	Alternate C. G.	ME-40
8K-9K	0	0	1	0	0	0												P08	Input Buffer & VFU RAM	ME-46/47
9K-10K	0	0	1	0	0	1												P09	Print Buffer	ME-14/15
10K-11K	0	0	1	0	1	0												P10	I/O Transfers	ME-38/39
11K-12K	0	0	1	0	1	1				8K - 16K								P11	Input MRI's	ME-92
12K-13K	0	0	1	1	0	0												P12	Output MRI's	ME-55
13K-14K	0	0	1	1	0	1												P13	I/O Controller	ME-9
14K-15K	0	0	1	1	1	0												P14	Option Prom	ME-49
15K-16K	0	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	P15	Not Used	

3.7.2 MRI DECODING

Input MRI's are decoded in a similar manner by ME-92. These decoded instructions gate input data onto the I/O bus from the control panel or the video amplifier when SELP11 and ENDBIN are active. The four input MRI's are as follows:

1. $\overline{\text{COLOT7}}$. Enables bus driver ME-78/79 to gate bits 0 through 7 of the two byte head position word (HDPS00-11) onto the I/O bus.

2. $\overline{\text{C08T11}}$. Same as above except it gates bits 8 through 11 (second byte of word).

3. $\overline{\text{ENSPN2}}$. Enable switch panel signal reads in position of six front panel switches (SW1 thru SW6).

4. $\overline{\text{ENSWOP}}$. Enable switch outputs from external switches for RTP and EOP and the LF after CR DIP switch.

Output MRI's are decoded by ME-55 when $\overline{\text{WRITE}}$, $\overline{\text{ENDBIN}}$ and $\overline{\text{SELP12}}$ are low. The ten MRI's are as follows:

1. $\overline{\text{ENBOP1}}$. Enable output 1 gates the I/O bus bits into latch ME-70/81/91. These bits control the print head solenoids using character generator signals CGI-9. One address bit (BADB08) is used with the 8 data bits (BUFDB0-7) to provide 9 bits of information.

2. $\overline{\text{ENBOP2}}$. Enable output 2 gates selected I/O bits into latch ME-69 to provide a MOTOR CONTROL signal to enable the carriage motion and paper feed stepper motors.

3. $\overline{\text{ENBOP3}}$. (Not Used)

4. $\overline{\text{RTP}}$. The ready-to-print signal originates at the left margin photo detector in the print mechanism and indicates that the printer is ready to print the next line. It is gated through the control panel onto the I/O bus, the memory bus and into the MPU. The MPU sets a software flag which ultimately causes the output address lines into decoder ME-55 to generate the $\overline{\text{RTP}}$ signal. From the decoder, $\overline{\text{RTP}}$ resets head position counter ME-93/94/95 in preparation for counting the next line.

5. $\overline{\text{OUTLAT}}$. The output latch MRI gates the I/O bus bits into latch ME-68. The three bits stored in this latch are the stepper motor slew command ($\overline{\text{STMSL}}$), the carriage motor slew ($\overline{\text{CRMTSL}}$) and the reverse signal. The slew commands increase stepper motor speed under MPU control. When the bi-directional head is moved quickly to a different position without printing, the $\overline{\text{CRMTSL}}$ slew command is used. Similarly for paper handling functions such as moving forms, the $\overline{\text{STMSL}}$ slew command is used.

6. $\overline{\text{STMTCL}}$. The stepper motor clock pulses load control bits into latch ME-67. These bits determine the sequence of the $\overline{\text{STMT01-04}}$ drive signals to the paper motion stepper motor.

7. $\overline{\text{CARPUL}}$. The carriage pulses clock up/down counter ME-90 when the motor is initially turned on or when it is turned off. These pulses cause the stepper motor to "ramp up" to normal operation quickly or to "ramp down" to a stop. They overcome the inherent inertia of the motor before the "auto-index" circuits slew the motor.

8. $\overline{\text{INDCLK}}$. The indicator clock pulses a latch in the control panel which stores control bits from the I/O bus to turn the front panel LED indicators on and off.

9. $\overline{\text{CPUACK}}$. (Not Used).

10. $\overline{\text{PRIME C}}$. (Not Used).

3.8 CONTROL PANEL/MPU COMMUNICATIONS (Figure 7-4)

As part of the main program, the MPU periodically samples the status of the control panel switches. It also changes the LED's as necessary. A three-byte input word contains the status of the switches while a single output byte controls the indicators.

Input MRI decoder ME-92 generates an $\overline{\text{ENSPN2}}$ pulse which strobes the status of switches 1 through 6 onto the keyboard bus (KBB00-07). The decoder is enabled by SELP11 while the address bus provides the MRI bits for $\overline{\text{ENSPN2}}$. The first byte of switch status is gated onto the I/O bus (BUFDB0-7) through transceiver ME-77/78 by the keyboard data enable signal ($\overline{\text{KBDENA}}$). It is gated from the I/O bus onto the memory bus (DBUS) and to the MPU through transceiver ME-38/39 by the external input signal ($\overline{\text{EXINPT}}$).

$\overline{\text{KBDENA}}$ and $\overline{\text{EXINPT}}$ are activated during $\overline{\text{ENDBIN}}$ while $\overline{\text{SELP11}}$ is active either by making address bit BAD02 low or BAD14 high. Either method enables ME-88 which drives $\overline{\text{KBDENA}}$ low and $\overline{\text{EXINPT}}$ goes low via ME-87.

The second byte is initiated when the input MRI decoder generates an enable switch output pulse ($\overline{\text{ENSWOP}}$). This pulse strobes ME-2, 3, 4 and 5 on the control panel pc board which places status bits on the keyboard bus for the EOP and RTP signals and for one section of DIP switch 1 and from sections of DIP switch 2. This byte is gated to the MPU in the same way as the first byte as shown in Figure 3-11.

The third byte is gated by the enable serial output pulse ($\overline{\text{ENSERO}}$). Baud rate selection in three bit binary and parity selection on two bit binary (odd, even or none) are placed on the keyboard bus along with bits for selection of 7 or 8 data bits and 1 or 2 stop bits.

LED's CR1 through CR6 are controlled by bits of the output data word. Figure 3-12 shows the bit assignment for the output word and the three byte input word described above. To activate an LED or turn it off, the MPU addresses device selects decoder ME-54 to activate SELP12 during the WRITE pulse time. Address bits 00-03 activate the MRI for the indicator clock pulse (IND CLK) from output MRI decoder ME-55. At the same time, the MPU gates the output data word onto the memory bus, through transceivers ME-38/39 and ME-77/78 to the I/O bus and to latch ME-1 on the control panel pc board. IND CLK strobes the word into the latch which turns the corresponding LED's on or off. Both transceivers are enabled to output data (write) when ENDBIN goes high.

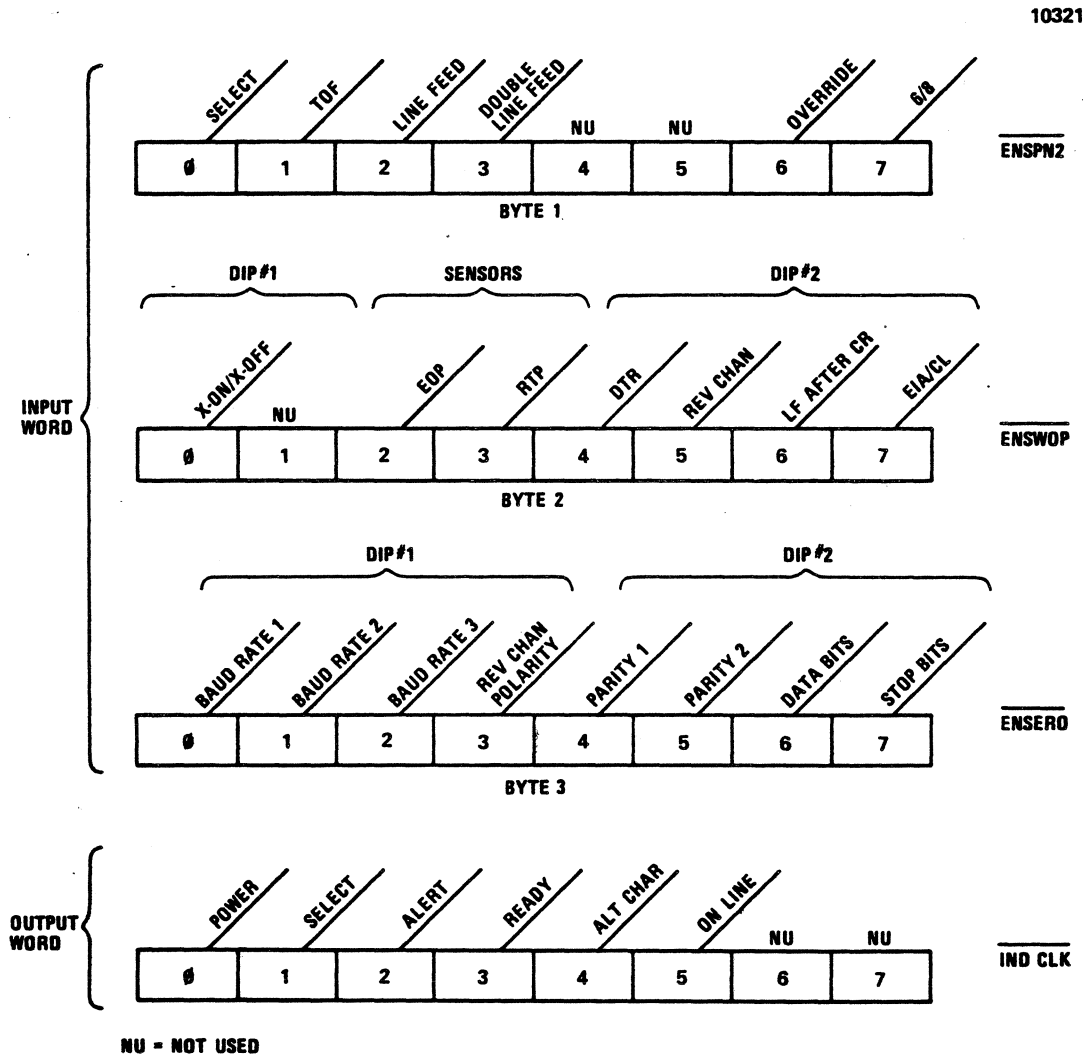

Figure 3-11. CONTROL PANEL STATUS WORD

3.9 VFU READER/MPU COMMUNICATIONS (Figure 7-5)

VFU data is read into the VFU RAM by the MPU whenever the $\overline{\text{VFU LSW}}$ bit is low. The VFU load switch bit ($\overline{\text{VFU LSW}}$) is the highest order bit in the 14 bit VFU word. As the MPU polls the I/O devices, it enables multiplexer ME-60/61/71/72 periodically to gate the VFU word onto the I/O bus and then to the MPU via the memory bus.

The 8-bit multiplexer is enabled by SELP10 and $\overline{\text{WRITE}}$ or $\overline{\text{ENDBIN}}$ being active. The resulting low from ME-61 (S10BIN) turns on gate inputs G1 and G2. S10BIN also enables transceiver ME-38/39 via ME-5 to gate I/O data onto the memory bus (BUFDB to DBUSB).

Address bits BAD00 and BAD01 are latched into ME-32/33 and control the A and B inputs to the multiplexer to select the lower 8 bits of the VFU word and then the upper 8 bits. With the A and B inputs both high, the upper bits are connected through the multiplexer via the four 1C3 and four 2C3 inputs to the I/O bus. If the tape is in the reader, bit 13 is low ($\overline{\text{VFU LSW}}$) and the MPU executes the program to load the 12 bit words into the VFU RAM on each VFU strobe pulse (VFU STB) generated by the tape feed hole. The MPU alternately loads bits 1-8 and then 9-14 (15 and 16 are not used) into the allocated RAM addresses until bit 13 goes high, indicating the end of data. This occurs when the tape is removed from the reader.

Each 8 bit byte is loaded into the MPU and then written into the VFU RAM ME-40/47. The BAD00-09 lines address the next sequential address allocated to VFU data while the $\overline{\text{WRITE}}$ pulse stores the data word appearing on the memory bus (DBUSB0-7) when the "chip select" line (CS) is enabled by SELP08 and $\overline{\text{WRIBIN}}$. Data is read from the RAM when $\overline{\text{WRITE}}$ is high and CS is enabled by $\overline{\text{ENDBIN}}$ and SELP08.

The downstream loading option allows the vertical spacing on forms to be changed remotely by software loading of the VFU memory via the interface. The sequence for downstream loading is initiated by sending a "Start Load" code ($1D_{16}$) followed by two bytes per line, and terminated by a "Stop Load" code ($1E_{16}$). Refer to the operator's manual for the complete data format used to downstream load via the interface.

3.10 PRINTER MECHANISM OPERATION (Figure 7-6)

Operation of the printer mechanism consists of turning on the stepper motor to move the carriage/head assembly across the page while simultaneously firing the head solenoids as required to form the dots for each column of the dot matrix character. In addition, the mechanism turns on the other stepper motor to move the paper up one or more lines. Printer operation is initiated upon detection of a control character in the input buffer. It ends when the end-of-print switch (EOP) is activated or the last character in the print buffer is printed.

3.10.1 CARRIAGE MOTOR OPERATION

Figure 7-2, the input data functional shows the details of how the MPU controls the address and data lines to read each character from the print buffer cnto the memory and bus and the I/O bus. The MPU puts the carriage motor in operation and then lets it run until the end of the line is reached. This frees the MPU from controlling each step.

Figure 7-6 shows the details of carriage motor operation.

The four-phase carriage stepper motor is controlled by PROM ME-89 which contains the correct phase relationships in 8 sequential addresses to create 0.9^{o} steps or 400 steps per revolution. Each step corresponds to one dot column. The PROM addresses are accessed by up/down counter ME-90. It counts up during left to right motion (REVESE is low) and counts down for right to left motion.

Initially, the carriage stepper motor is "ramped up" by a series of carriage pulses (CARPUL) to overcome the motor inertia. The MPU places bits on the address bus for the CARPUL, selects MRI output decoder ME-55 with SELP12 and then activates the decoder with each WRITE and ENDBIN pulse (WRBIN). The CARPUL pulses clock the up/down counter ME-90 via ME-63 until the motor reaches 10 ips.

During the "ramp up" operation, the slew carriage signal (SLEWCR) from latch ME68 is low. This keeps one-shot ME-73 and flip-flop ME-81 reset. The MPU controls both stepper motors using the output latch pulse (OUTLAT) from output MRI decoder ME-55, the address bus bits and the I/O bus bits. SLEWCR allows the auto-increment circuit (ME-73 and ME-81) to control the carriage stepper while REVESE determines its direction. The stepper motor slew signals (STMSL and CRMSL) enable the stepper drivers on the power driver board (see para. 3.12).

After the last $\overline{\text{CARPUL}}$, the MPU sets the SLEWCR bit high, releasing the auto-increment circuit (ME-73 and ME-81). The next 0.5 us Ø2 pulse sets ME-81. The clock input to the counter goes low and ME-66 is enabled. The next Ø2 pulse fires 500 us one-shot ME-73 and its $\overline{Q}$ output goes low. On the third Ø2 pulse ME-83 resets and its high $\overline{Q}$ output in conjunction with CARPUL high clocks the counter. ME66 is gated off until the one-shot times out 500 microseconds later. At that time the sequence repeats with Ø2 setting ME-81, re-triggering the one-shot and then re-setting ME-81. This auto-increment circuit continues to pulse the carriage stepper motor every 500 us until the MPU resets the SLEWCR bit at the end of the line.

3.10.2 VIDINT GENERATION

The video interrupt pulses (VIDINT) enable the logic board to determine print head position for registration of the printed characters and to calculate the shortest print path at the end of each line. Components of the video system consists of a dual timing fence, a video amplifier and a flexible cable. Since the amplifier is attached to the carriage/lead assembly, the flexible cable is used to connect the video signals to the logic via the power driver board. The timing fence is positioned between an optical pick-up and an LED. The print head moves the pick-up and LED along the fence. This generates a series of electrical pulses which are detected by the video amplifier and sent to the logic pc board.

The timing fence is a clear, thin strip of mylar with alternately transparent and opaque slots (See Figure 3-12). An upper and lower fence are photographically etched onto the strip with the fences displaced 90° from each other. This provides twice the pick density of a single fence since each edge of the slots from both fences establishes a dot column.

00466

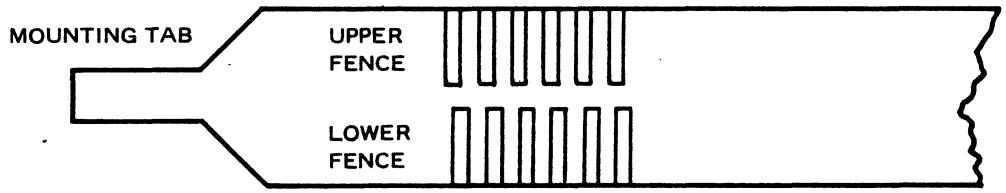

Figure 3-12. EXPLODED SECTION OF TIMING FENCE

As the print head moves over the timing fence, the transparent and opaque areas of the fence cause corresponding electrical signals to be generated by the two optical pick-ups. Each pick-up consists of an optical block that houses an LED and a phototransistor. The resulting video signals are detected, compared against an adjustable reference voltage and then sent to the logic board to generate the VIDINT pulses. Figure 3-13 shows the video amplifier and optical pick-ups.

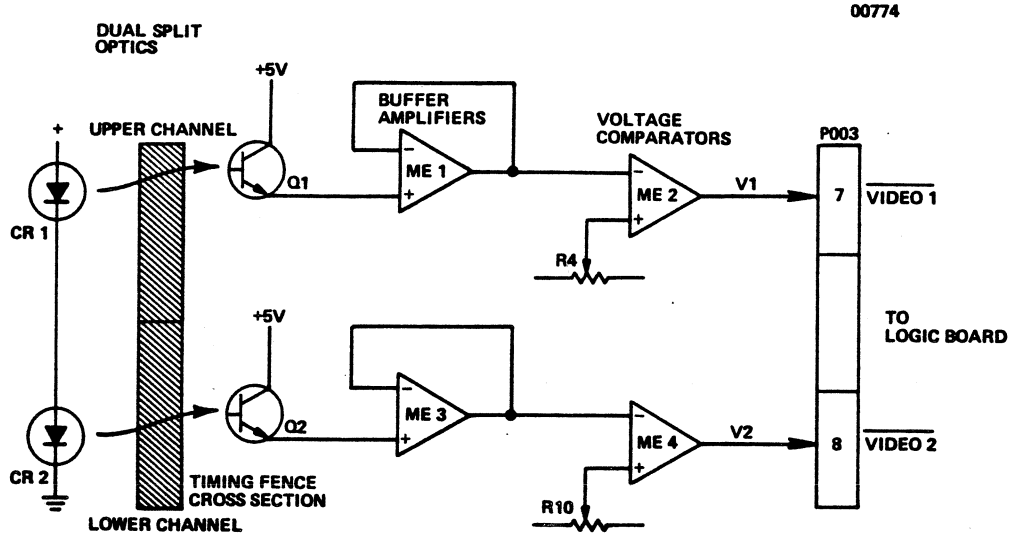

Figure 3-13. VIDEO AMPLIFIER SIMPLIFIED SCHEMATIC

Figure 3-14 shows the logic and timing for detecting each edge of the VIDEO 1 and VIDEO 2 pulses from the video amplifier. The top timing diagram gives overall relationships. Each video pulse train occurs at 500 Hz. The square wave pulses are on for 1 millisecond and off for 1 millisecond. The logic shown generates a VIDINT pulse for the leading and trailing edge of each video pulse. VIDINT occurs at 2 kHz because of the 90° phase relationship between the two video signals. Count up or count down pulses are also generated for forward and reverse head motion. These pulses go to the up/down head position counter which generates the 12 bit head position word (HDPS00-11). This word is used by the MPU to determine the direction to move the head before printing the next line.

As shown in Figure 3-14, the edge detector consists of four D flip-flops, a dual 4-to-1 multiplexer and associated logic gates. The MUX gates one of the four inputs (1C0-1C3) to the output, pin 1Y and one of the other four inputs (2C0-2C3) to 2Y. Both sections of the dual MUX are enabled during each VIDINT pulse by Ø1 via ME-75. This keeps the 1G and 2G inputs active for 0.5 microseconds. Note that the MUX is used only for the head position counter inputs (CD or CU). VIDINT is generated independent of the MUX.

D flip-flops ME-83D and 83A with exclusive or gate ME-66 detect each edge of VIDEO 1. On the negative-going edge, ME-83D sets with the next Ø2 pulse. ME-83A sets on the second Ø2 pulse. Before ME-83A sets, both inputs to ME-85 are high and VIDINT goes high for 0.5 microseconds. When VIDEO 1 goes positive, ME-83D resets on the next Ø2 pulse. At that time, the 4Q and 1Q outputs are both low and another VIDINT pulse is generated. The next Ø2 pulse drives 1Q high and ends VIDINT.

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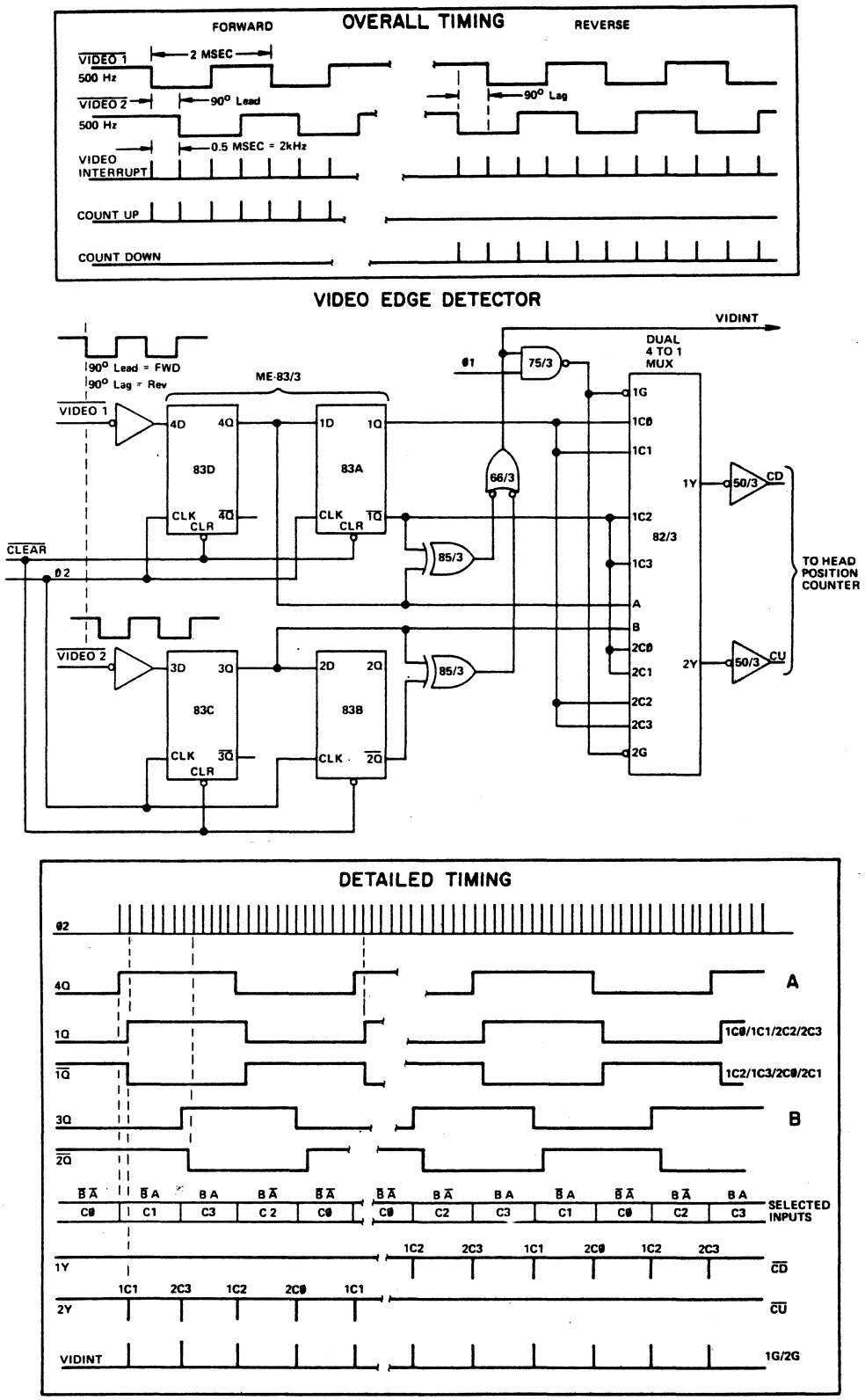


Figure 3-14. VIDEO EDGE DETECTOR CIRCUIT/TIMING

Flip-flops ME-83C and 83B operate in a similar manner to generate VIDINT pulses for each edge of the VIDEO 2 pulses.

Either CU or CD pulses are generated simultaneously with the VIDINT pulses depending on the phase relationship of the input video pulses. If VIDEO 1 leads VIDEO 2, CU pulses are generated for forward carriage motion. For reverse motion, VIDEO 2 leads VIDEO 1 and CD pulses are generated.

The A ($\overline{\text{VIDEO 1}}$) and B ($\overline{\text{VIDEO 2}}$) inputs to MUX ME-82 select one of the four input lines C0-C3. Since both "G" inputs (1G and 2G) are tied together, two lines are actually selected (i.e., corresponding inputs of both halves such as 1C0 and 2C0 or 1C1 & 2C1, etc.). An inspection of the timing diagram or Table 3-4 shows that either the 1Q or $\overline{1Q}$ output of ME-83A is high for two successive edges of video. These two outputs are connected to the MUX to provide a high input at the correct time for the CU or CD pulses.

The 1Q output is high during count down when the A & B inputs to the MUX select 0 or 1 and during count up when 2 or 3 is selected. The $\overline{1Q}$ is the complement of 1Q, therefore it is high for 2 & 3 during count down or 0 & 1 for count up.

Table 3-4. CU/CD BIT CONTROL (MUX ME-82)

COUNT UP (CU)

B	A	1Q	$\overline{1Q}$	2Y	DECODED COUNT
0	0	0	1	$\overline{1Q}$	2C0
0	1	0(1)*	1(0)*	$\overline{1Q}$	2C1
1	1	1	0	$\overline{1Q}$	2C3
1	0	1(0)*	0(1)*	$\overline{1Q}$	2C2

COUNT DOWN (CD)

B	A	1Q	$\overline{1Q}$	1Y	DECODED COUNT
1	0	0	1	$\overline{1Q}$	1C2
1	1	0(1)*	1(0)*	$\overline{1Q}$	1C3
0	1	1	0	$\overline{1Q}$	1C1
0	0	1(0)*	0(1)*	$\overline{1Q}$	1C0

*occurs 0.5 us after AB changes

3.10.3 CHARACTER GENERATION (Figure 7-6)

Each VIDINT pulse causes I/O controller ME-9 to send an INT pulse to the MPU when the controller is enabled by SELP13 on its chip enable input (CE). The MPU reads the next character from the print buffer, places it on the address bus and selects either the standard character generator PROM (ME-41) or the alternate PROM (ME-42) with SELP04 or SELP05. PROM selection depends on which character set bit has been set in the option PROM. The selected PROM places the bits for the first column of dots on the memory bus.

The MPU addresses output MRI decoder ME-55 to generate an $\overline{\text{ENBOP1}}$ pulse which clocks the character bits into latch ME-70/81/91. The CG1-CG9 lines from the latch turn on the corresponding drivers on the power driver board which energize the print head solenoids via lines L1-L9. Each time an $\overline{\text{ENBOP1}}$ pulse clocks the character bit latch, it fires re-triggerable, one-shot ME-73. When the one shot runs down in approximately 500 microseconds, it clears the character bits from the latch which de-energizes the head solenoids. The MPU then increments the PROM address by one to read out the next column of dots and the process repeats until the last column is printed.

Each vertical column represents one 8 bit word from the PROM. Wherever a "1" is programmed causes the corresponding solenoid to fire and form the dots on the page. Intercharacter spacing is provided by programming all zeroes in the word. The majority of the characters in the 9x7 or 9x9 matrices are formed by bits 1-8. Bit 9 is used only for underlining and for descending characters such as "p, q, z," etc. When the ninth bit is used, the MPU accesses the PROM twice. The first byte reads bit 1-8 while the second byte reads bit 9. Since the I/O bus has only 8 bits, the MPU uses address bit BAD08 as the ninth data bit when necessary.

3.11 MISCELLANEOUS OPERATIONS (Figure 3-15)

In addition to paper movement and character printing, the printer also performs the following: Audio Alarm (optional), Paper Out and Motor Control.

3.11.1 AUDIO ALARM

Receipt of a bell code (07_{16}) or detection of a paper-out condition causes the generation of the tone signal for the speaker if the optional audio alarm feature is installed. The software controlled BELL code or the SPEAK signal triggers timer ME-27 which enables 2.5 kHz ocsillator ME-17 for approximately 2 seconds.

3.11.2 PAPER OUT

A paper-out condition in the printer is detected by the paper-out switch located in the path of the paper. With paper in the printer, the switch is held open. After the last page passes over the switch, the switch closes, causing the microprocessor to deselect the printer, generate a speaker signal and light the ALERT lamp on the control panel.

To allow the printer to print the last form, the operator can press the OVERRIDE switch and then depress the select switch on the control panel. This overrides the paper-out condition as long as the switch is held depressed.

3.11.3 MOTOR CONTROL

The motor control feature automatically turns the stepper motors off when the printer has not received a print or paper movement command. If no print or paper movement command is received, the coil drive circuits, which provide the current to the motors, are deactivated. The coil drive circuits are reactivated by the next print or paper movement command.

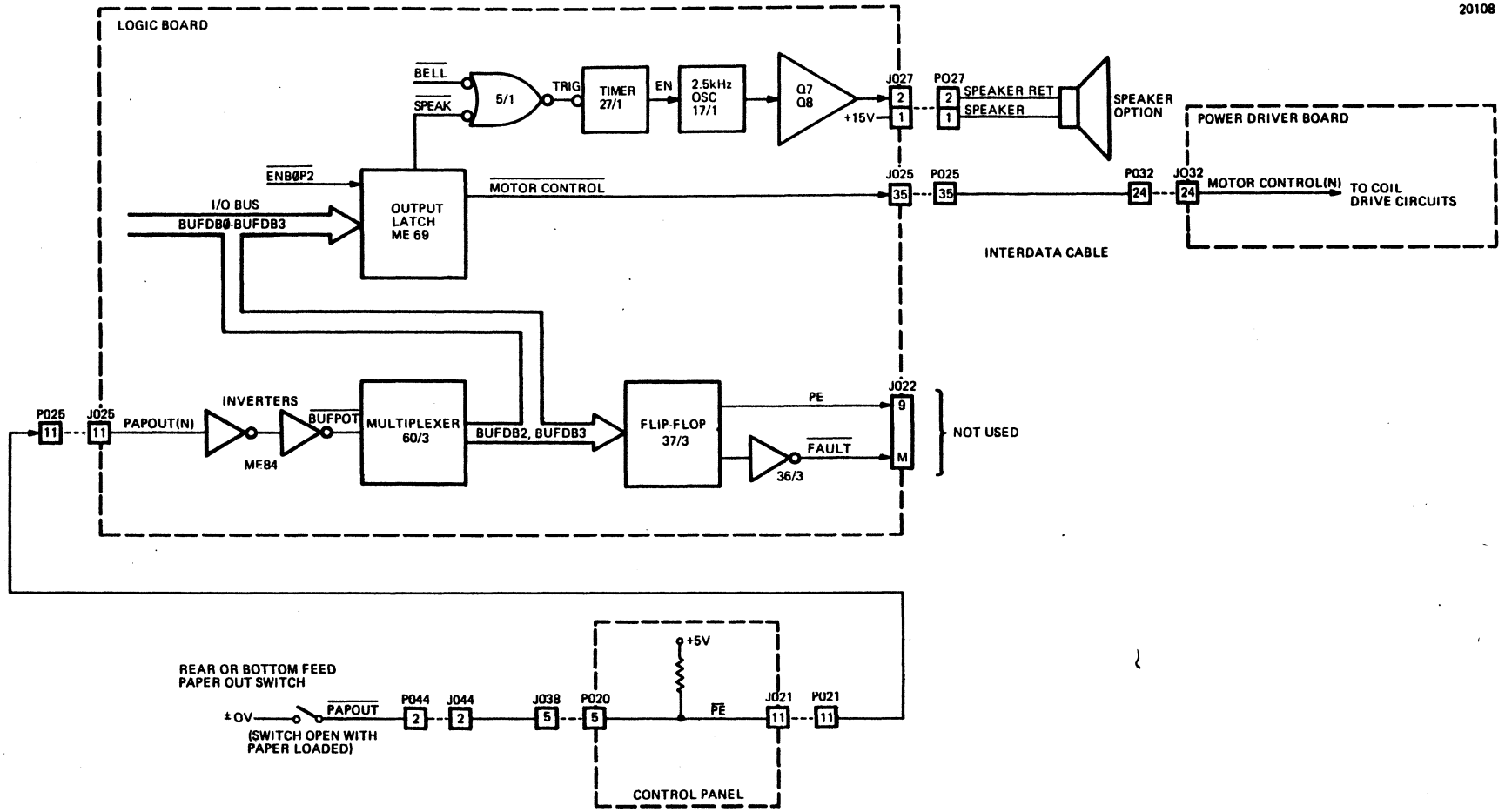


Figure 3-15. MISCELLANEOUS OPERATIONS

3.12 STEPPER MOTOR OPERATION

Two stepper motors are used in the printer, one to drive the paper feed mechanism and the other to drive the print head carriage. Both motors are identical, with motor specifications as shown below:

MOTOR SPECIFICATIONS

Voltage:	1.8 VDC
Current:	4.5 amps/phase
Resistance Per Phase:	0.4 ohms
Phase:	4
Excitation:	2 phase
Temperature Rise:	80 degrees
Insulation Class:	B
Inductance:	1.4 MH/phase
Dynamic Torque:	10 kg - cm
Holding Torque:	11 kg - cm
Response Freq.:	3000 PPS
Step Angle:	1.8 degrees
Rotor Inertia:	560 g - cm^2
Rotation:	bi-directional
Weight:	1400 g

The electronic drive circuitry for the motors is located on the power driver board behind the front cover. Basically, the stepper motor translates electrical pulses sent from the drive circuitry into precisely accurate mechanical movements. Each incoming pulse rotates the motor drive shaft through a specific angular rotation. This angle or displacement per step is repeated with each succeeding pulse sent from the drive circuitry. Stepper motors are used as opposed to servo-mechanisms with position feedback because the rotation of the stepper motor shaft is in fixed, repeatable, known increments.

Stepper motor operation is related to basic permanent magnet theory where "likes" repel and "unlikes" attract. If, for instance, the stator windings (A, B, C, D in Figure 3-16A) are energized so that polarities appear as shown, then the direction of the rotor is counterclockwise. The rotor aligns itself between the "average" south pole and the "average" north pole, as shown in Figure 3-16B.

To allow better single step resolution, more stator poles are added and teeth are machined on each stator pole and also on the rotor. The number of teeth on the rotor and stator is dependent upon the step angle required each time the polarity of the winding is changed. The stepper motor has a basic 1.8^{o} step angle movement, giving 200 full steps per revolution. An electronic half-stepping mode of operation is used in the printer, resulting in a 0.9^{o}, 400 step per revolution motor. This electronic half-stepping results in the rotor moving half its normal distance per step. The advantages are finer resolution and smoother motor operation.

Figure 3-17 is a schematic diagram of the driver circuit for one winding.

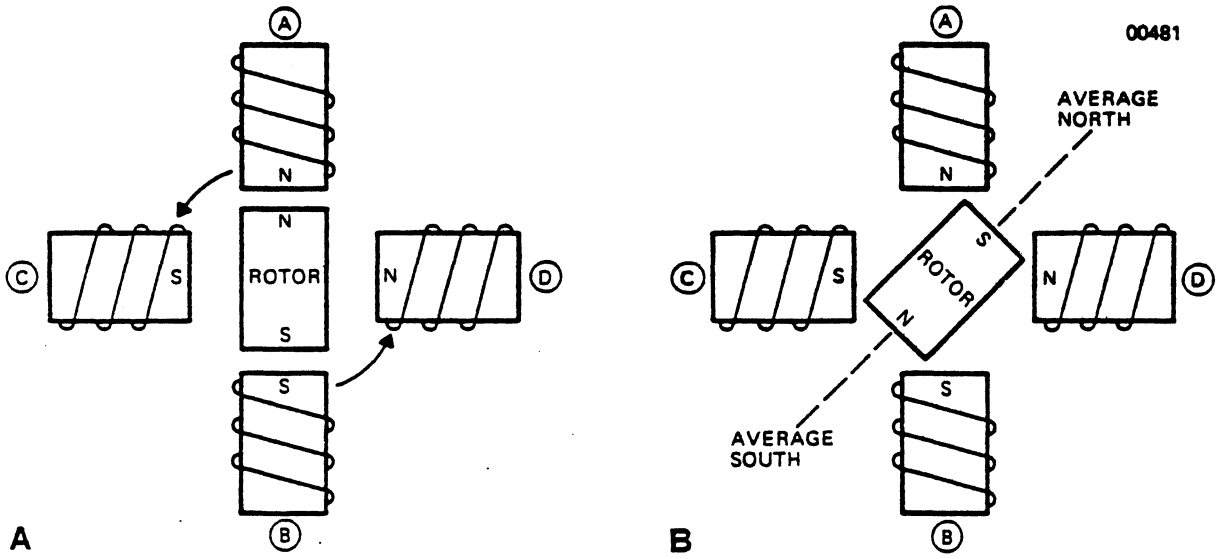


Figure 3-16. BASIC STEPPING MOTOR OPERATION

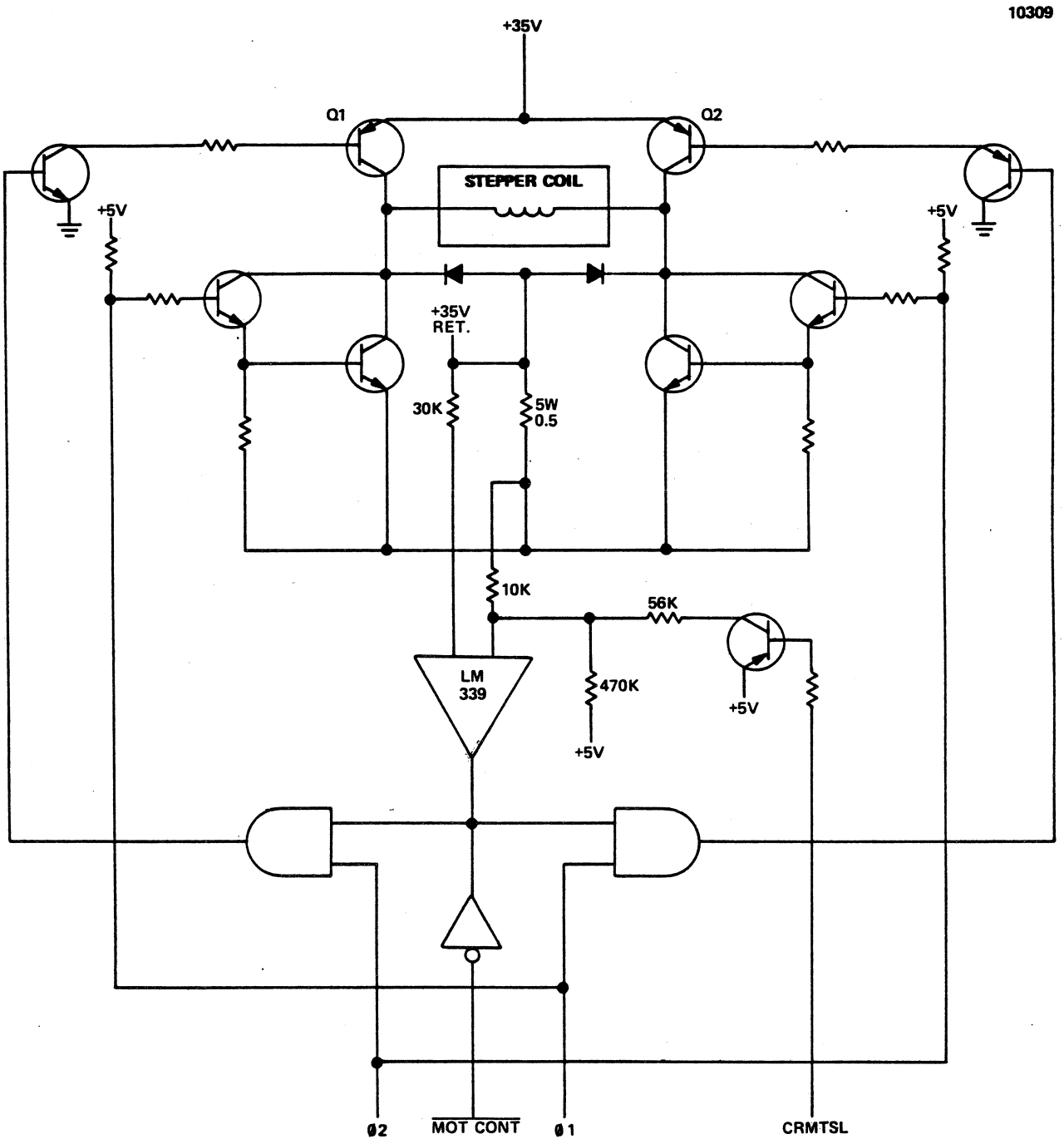


Figure 3-17. STEPPER MOTOR DRIVE CIRCUIT (TWO PHASE WINDING SHOWN)

3.13 POWER DISTRIBUTION (Figure 3-18)

The power supply provides six output voltages:

Regulated	Unregulated
+5 VDC	+35 VDC
-5 VDC	+15 VDC
+12 VDC	
-12 VDC	

The standard power input to the printer is 115 VAC, 60 Hz. Power enters the rear of the printer through a three-conductor power cord, an on/off circuit breaker and a line filter. From the line filter, power goes through the wire harness to the multitap power transformer and to the cooling fan. The wire harness to the transformer is connected to different points on the terminal block for each input voltage option.

The power transformer distributes the power at lower voltages for use in the logic circuits and head driver circuits. The secondary windings of the transformer develop the following voltages: 12 VAC, 36 VAC center-tapped and 27.5 VAC. The 12 VAC and 27.5 VAC voltages are connected to diode bridges to generate +15 VDC and +35 VDC, respectively. The +15 VDC is filtered and sent to the main logic board where it is fused and regulated to +5 VDC. The +35 VDC is filtered and sent to the main logic board where it is fused and sent unregulated directly to the print head via the ribbon cable and video amplifier board. The unregulated +35 VDC is also sent to the paper and carriage stepper motors. The 36 VAC is sent directly to the main logic board where it is rectified, fused and regulated to +12 VDC, -12 VDC, and -5 VDC.

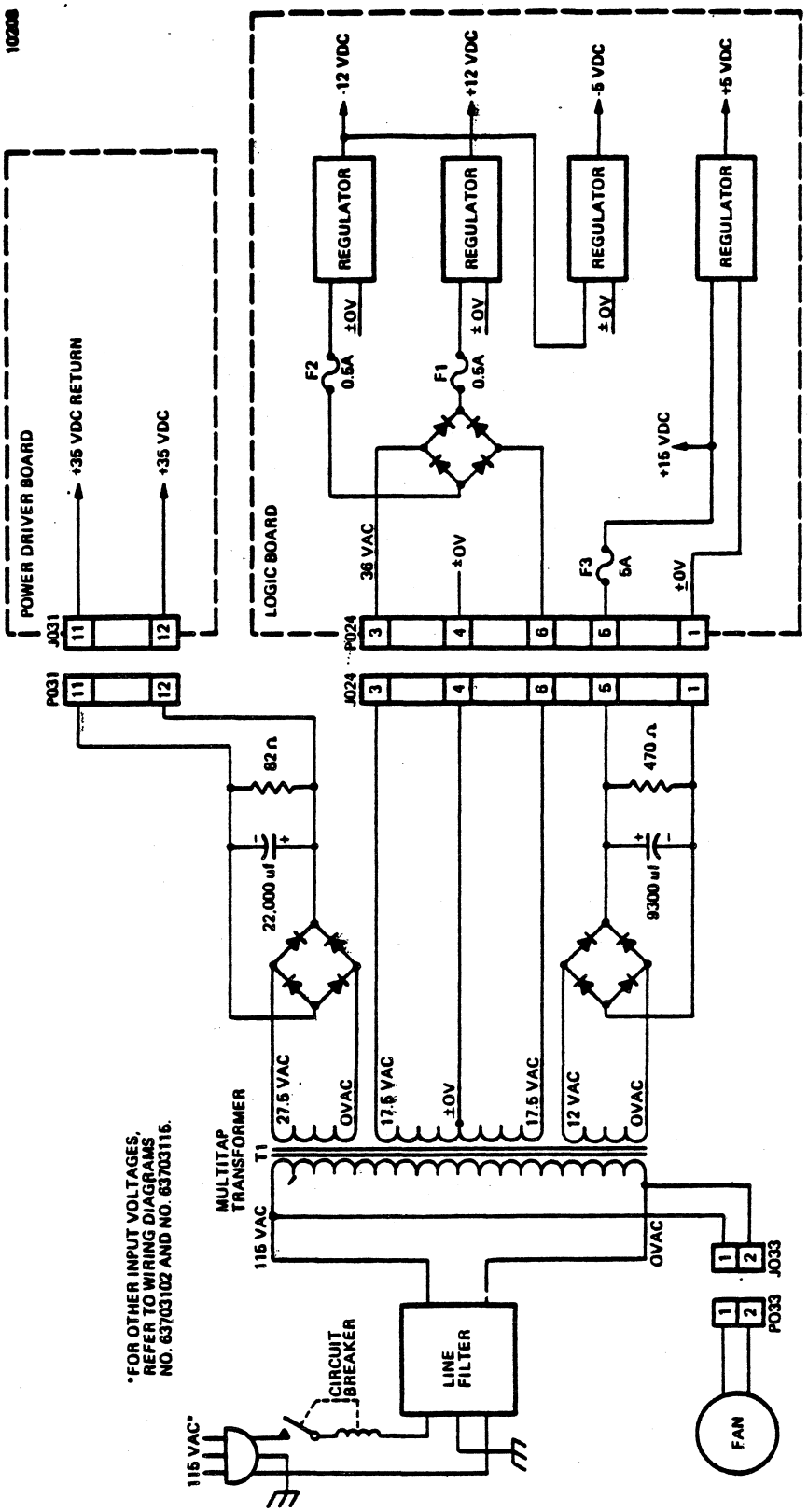


Figure 3-18. POWER DISTRIBUTION DIAGRAM

INIT

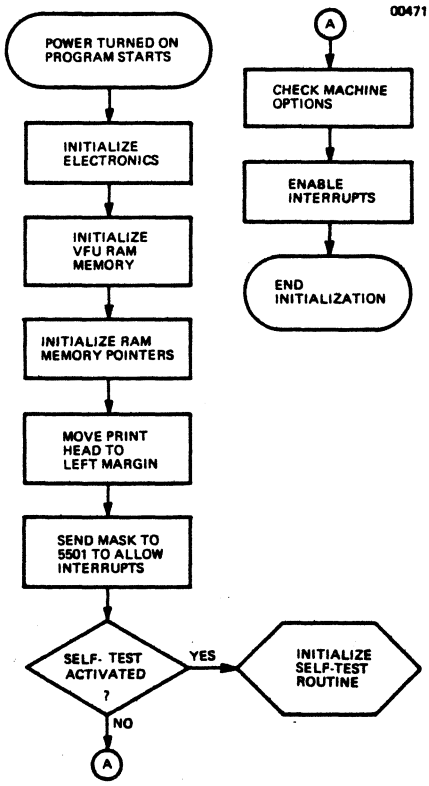


Figure 3-19. PRINTER INITIALIZATION FLOW CHART

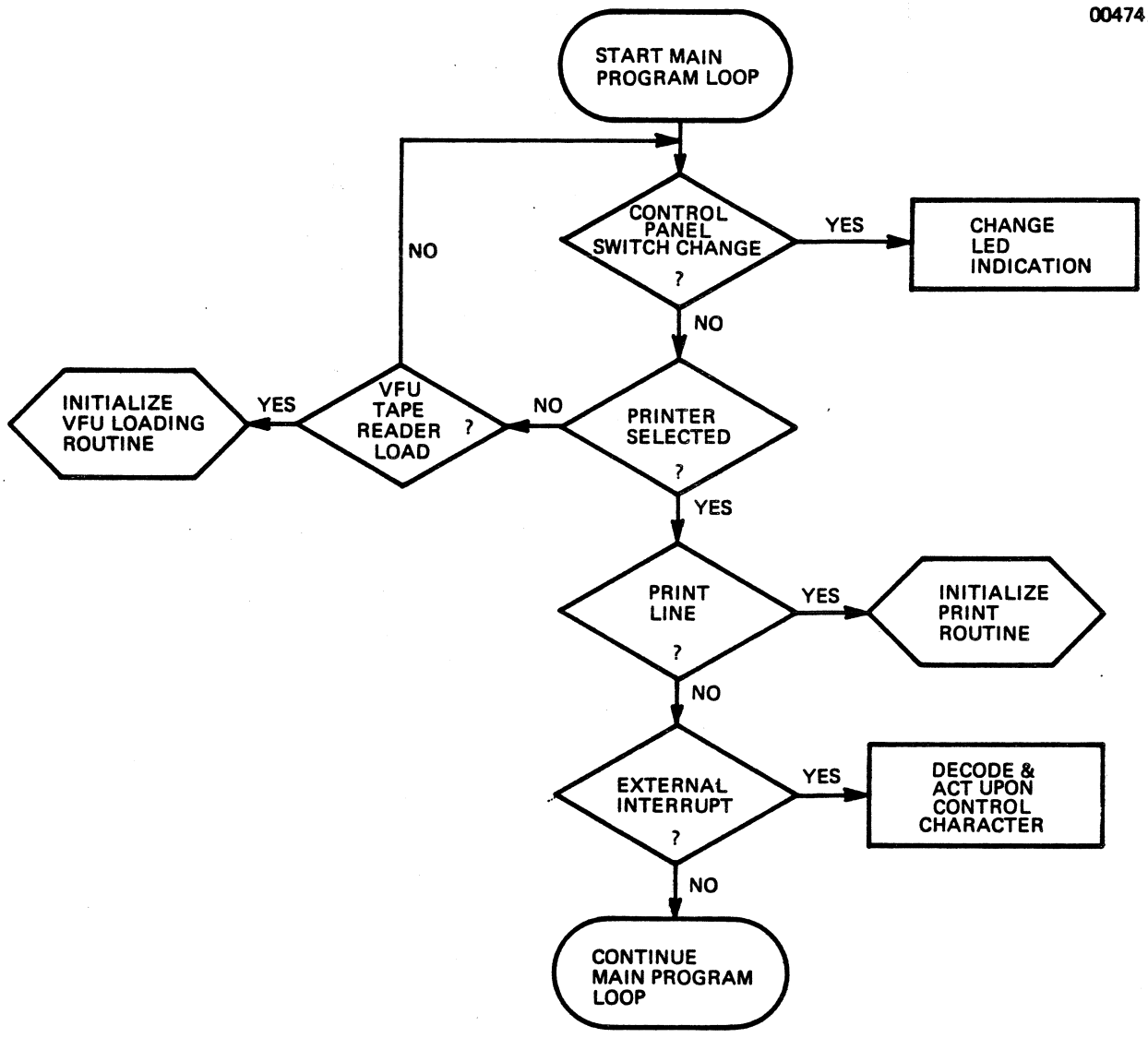


Figure 3-20. MAIN PROGRAM (MONITORING) LOOP, FLOW CHART

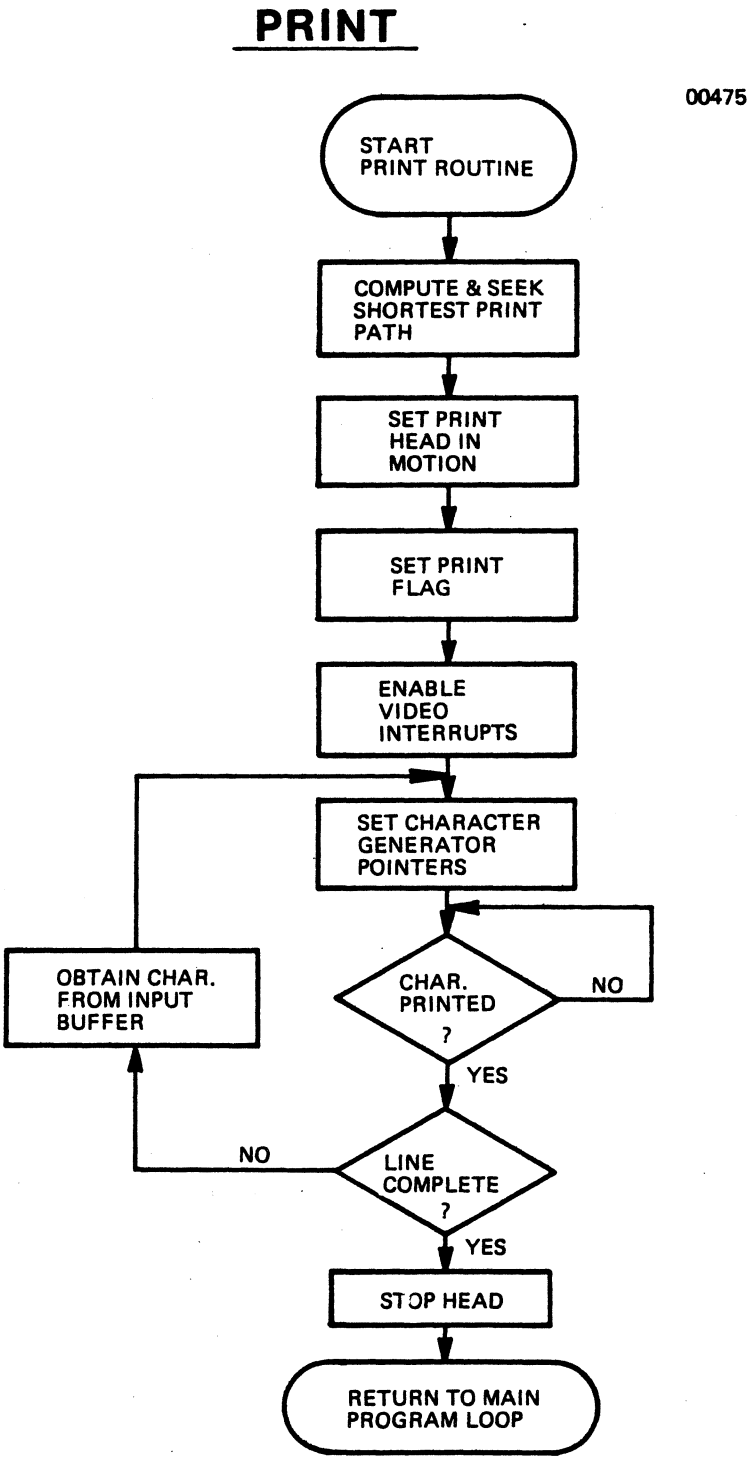


Figure 3-21. PRINT ROUTINE FLOW CHART

VIDINT

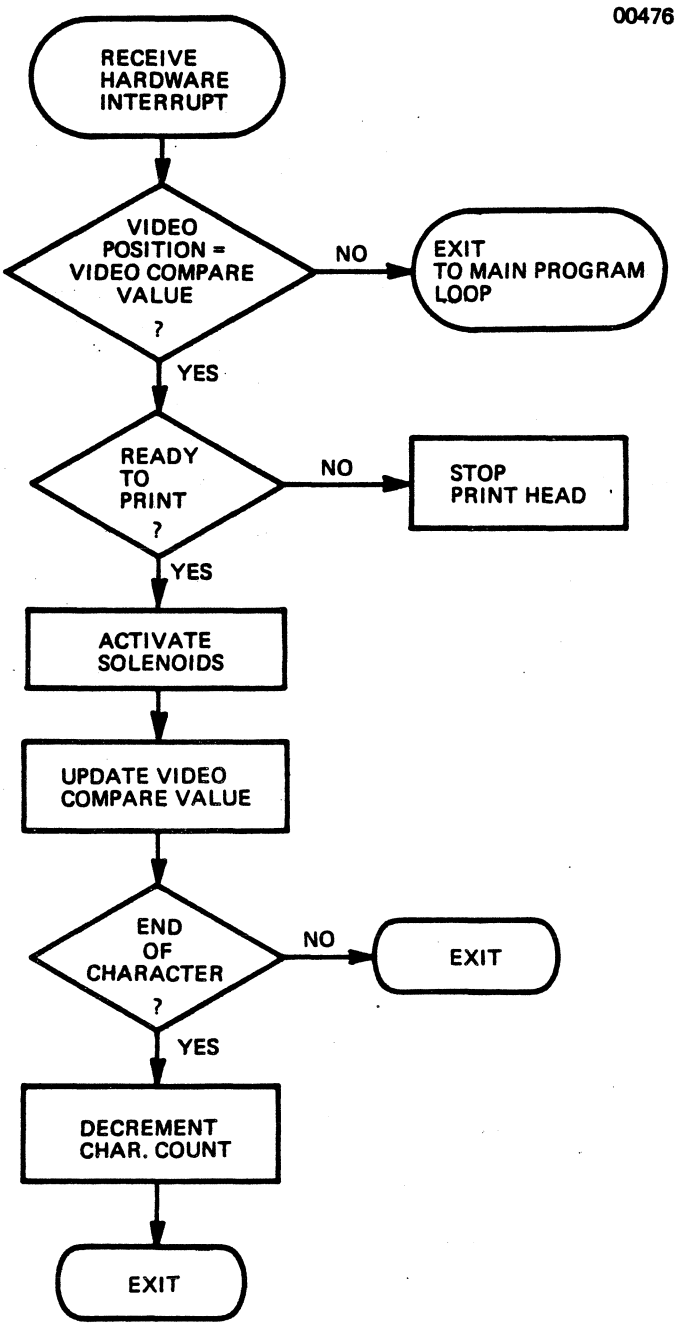


Figure 3-22. VIDEO INTERRUPT ROUTINE (WITH PRINT ONLY), FLOW CHART

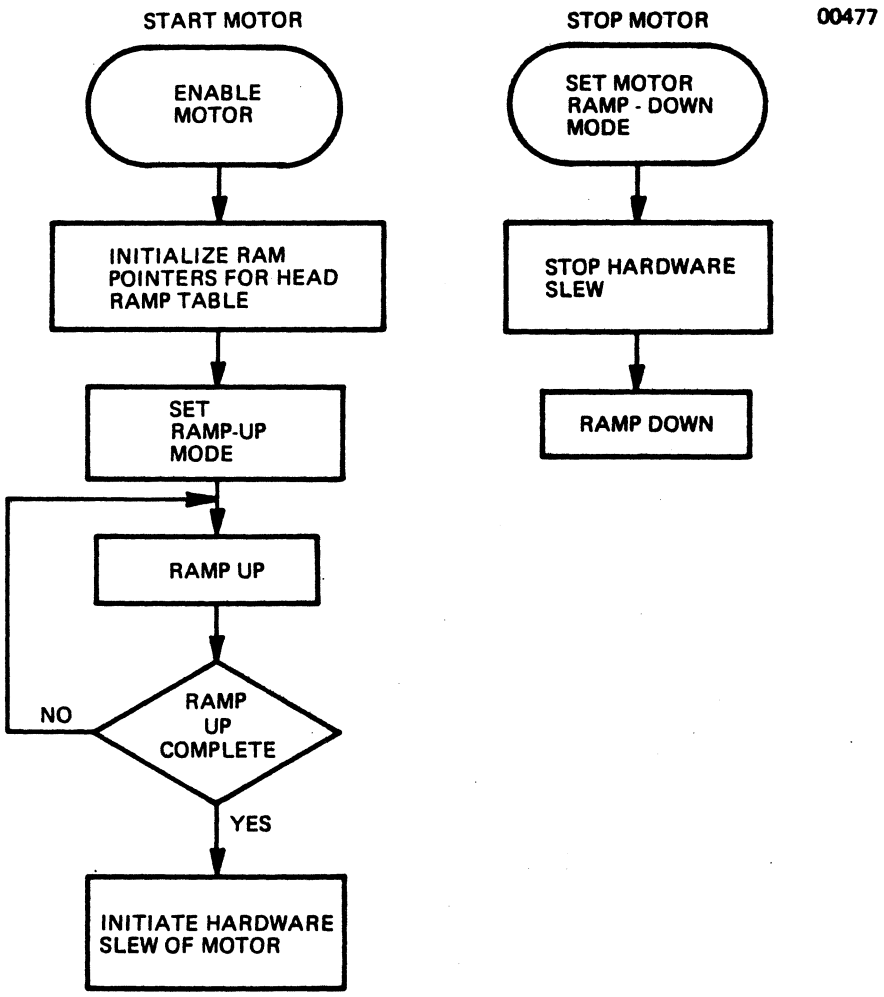


Figure 3-23. CARRIAGE DRIVE INTERRUPT ROUTINE, FLOW CHART

STMT

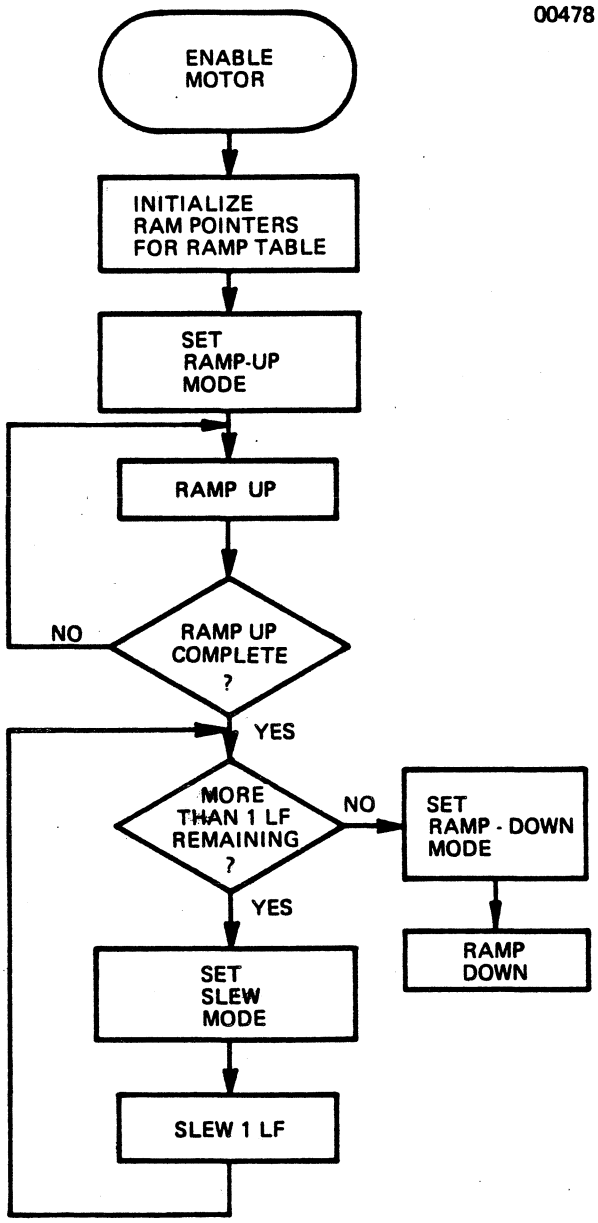


Figure 3-24. PAPER DRIVE INTERRUPT ROUTINE, FLOW CHART

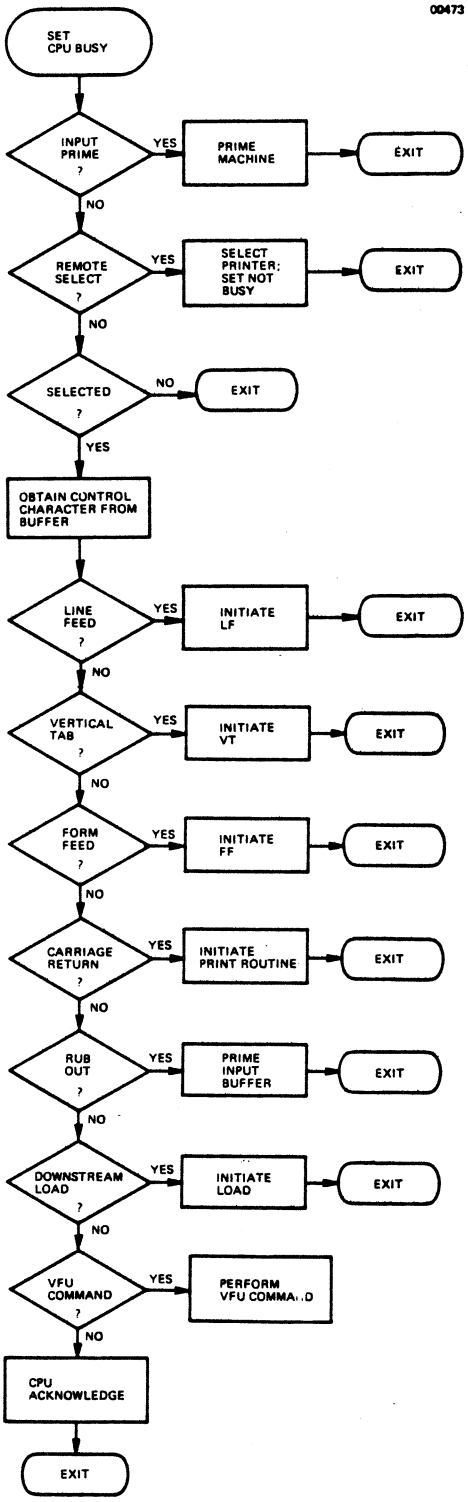


Figure 3-25. CONTROL CHARACTER INTERRUPT ROUTINE, FLOW CHART

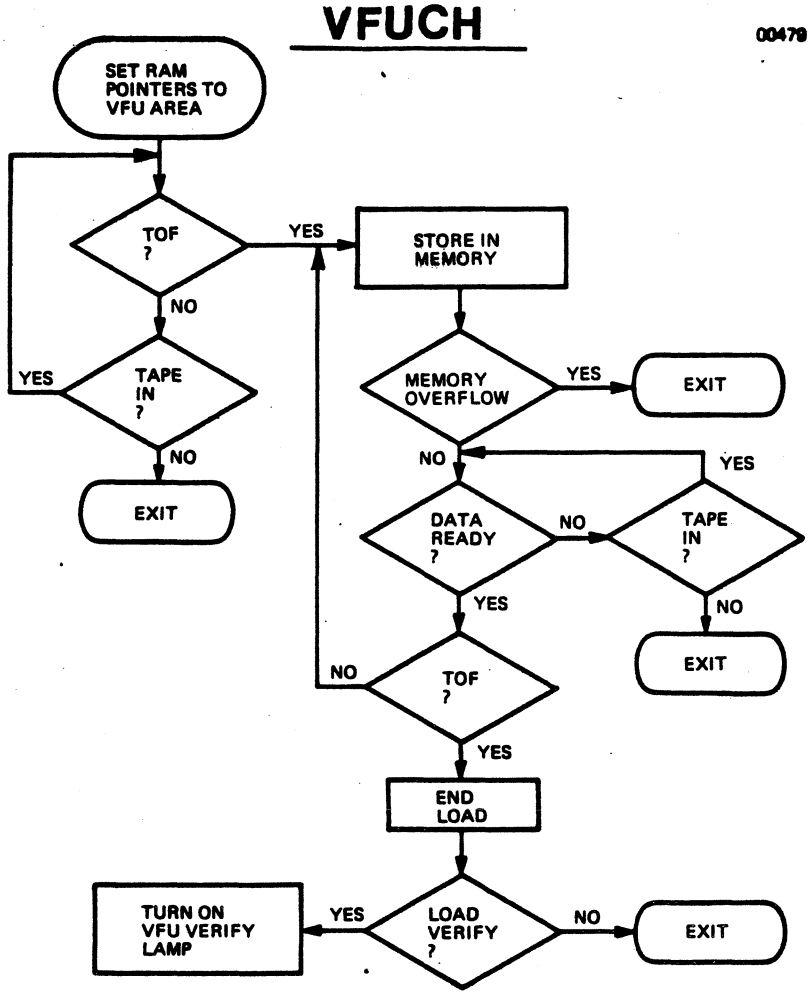


Figure 3-26. VFU PAPER TAPE LOAD ROUTINE, FLOW CHART

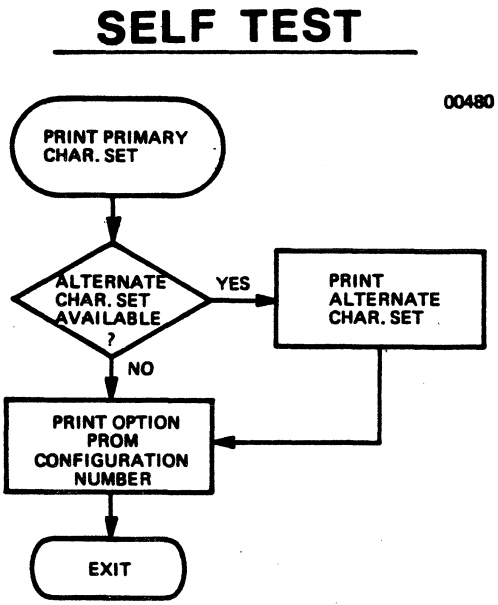


Figure 3-27. SELF-TEST ROUTINE, FLOW CHART

SECTION 4

MAINTENANCE

4.1 INTRODUCTION

This section contains maintenance information on the printer. The section is organized as follows:

4.2 PRINTER MARKING AND CONFIGURATION
4.3 RECOMMENDED PREVENTIVE MAINTENANCE
4.4 TROUBLESHOOTING GUIDE
4.5 RECOMMENDED TOOLS

CAUTION

TO ENSURE YOUR OWN PERSONAL SAFETY AND AVOID POTENTIAL DAMAGE TO THE PRINTER, OBSERVE ALL WARNING AND CAUTION LABELS. ALWAYS KEEP HANDS AND CLOTHING AWAY FROM ALL MOVING PARTS (BELTS, CARRIAGE, ETC.) WHILE PRINTER IS OPERATING.

4.2 PRINTER MARKING AND CONFIGURATION

This section provides information on printer marking/location of certain components in the printer and the configuration of the logic board assembly.

4.2.1 CENTRONICS NAMEPLATE (Figure 4-1)

The nameplate is located in the back of the printer on the electronic module cover and contains the following information.

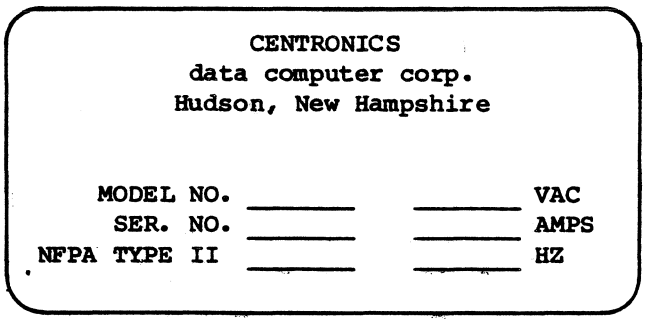


Figure 4-1. CENTRONICS NAMEPLATE

In the event of a field conversion of the operating voltage, amperage and frequency, it is recommended the nameplate be changed to reflect the conversion.

4.2.2 FUSE MARKING AND LOCATION

There are three fuses in the printer located on the logic board assembly. The fuses are marked F1-.5A, F2-.5A and F3-5.0A. If replacement of the fuses is necessary ensure the same type rated fuse is installed.

4.2.3 LOGIC BOARD MARKING AND CONFIGURATION

The logic board assembly is located in the electronic module assembly and is marked with three sets of dash numbers to define printer configuration. The following drawing and tables detail the meaning and location of the dash numbers.

10319

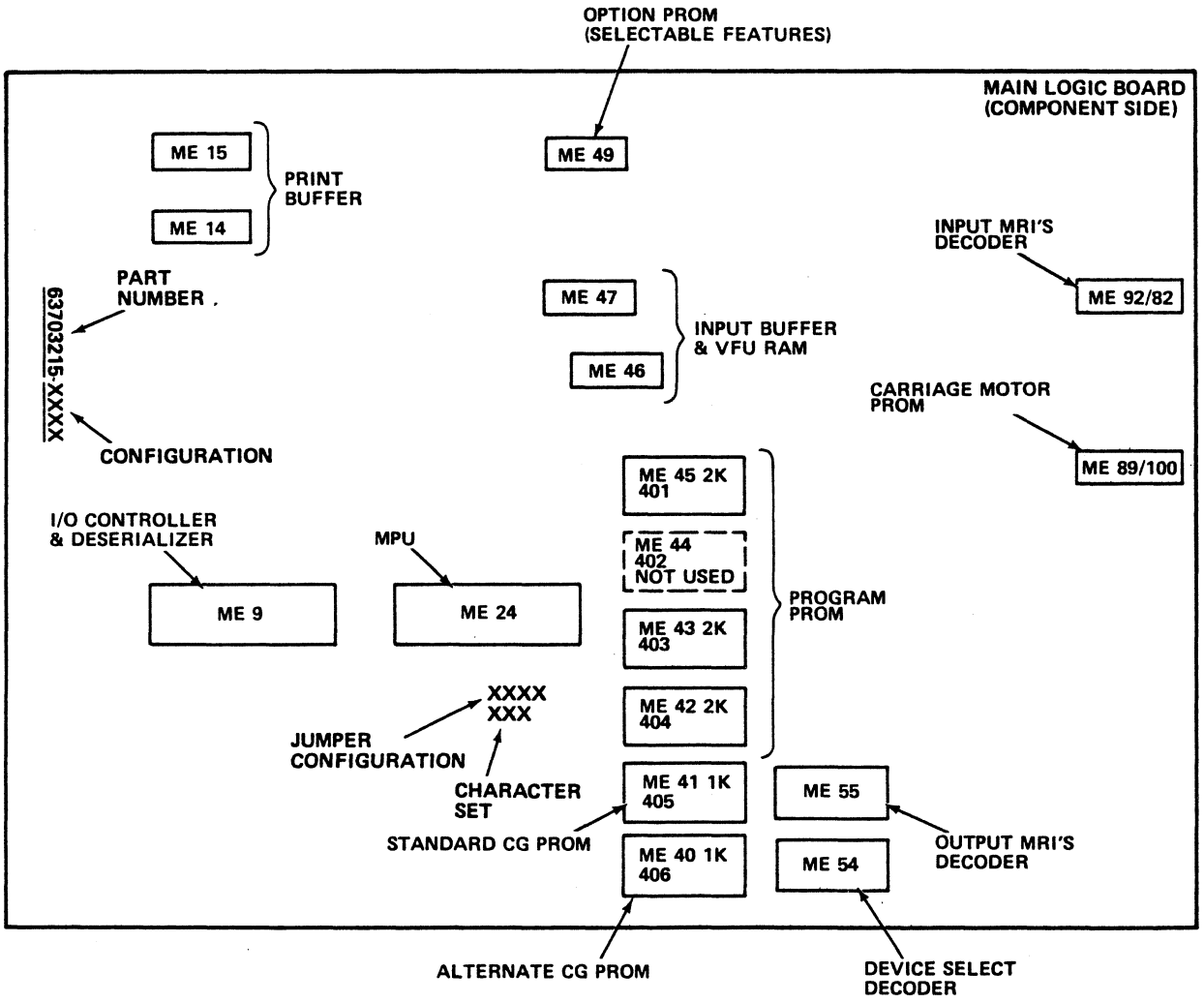
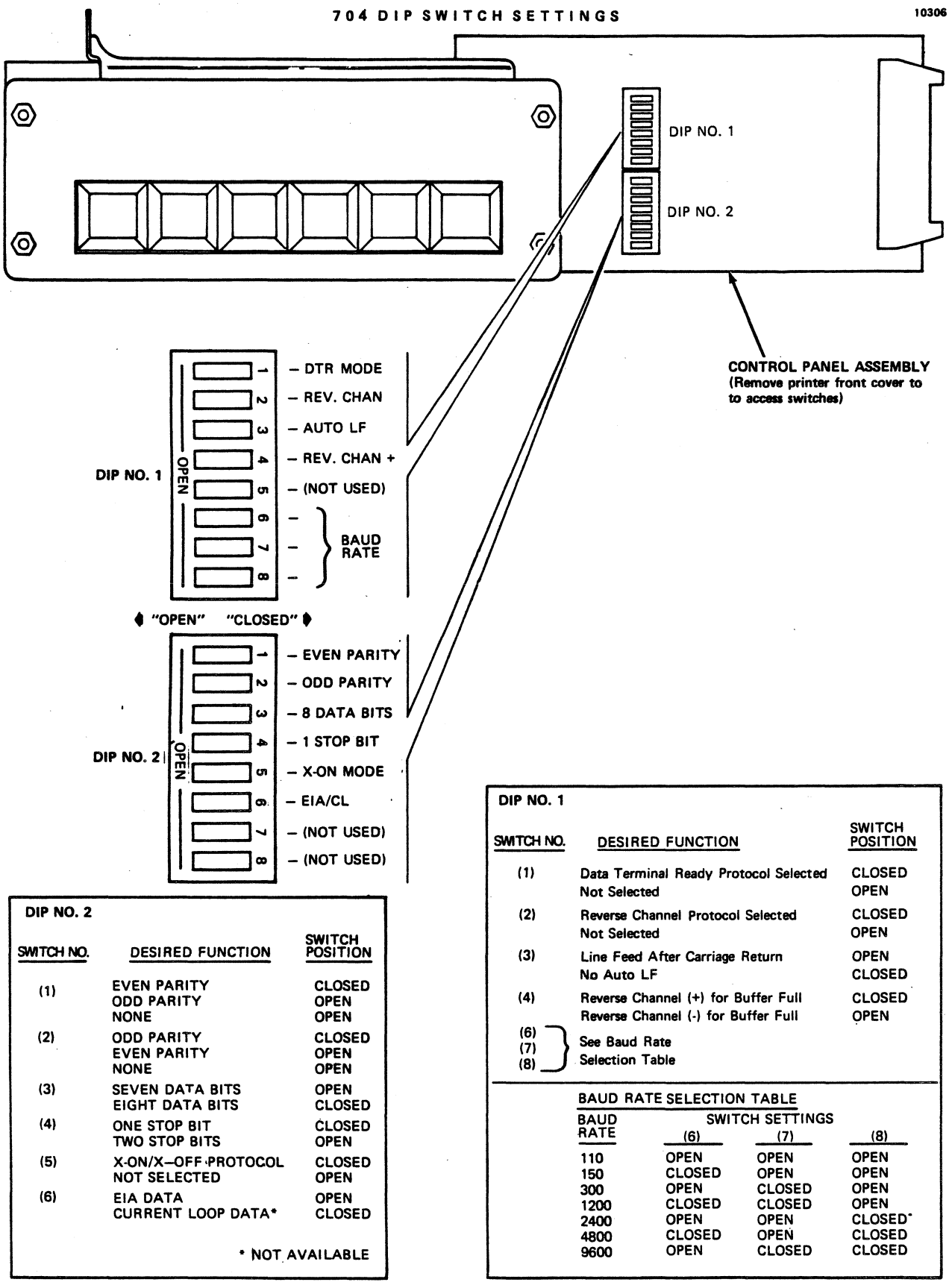


Figure 4-2. LOGIC BOARD MARKING

4.2.4 DIP SWITCH SETTINGS, CONTROL PANEL

The printer has switch selectable baud rate, parity, stop bits, auto LF and control line protocol. The two DIP switches for these functions are located under the front cover on the control panel PC board. The figure and tables below detail the switch settings for the functions.



DIP NO. 2

SWITCH NO.	DESIRED FUNCTION	SWITCH POSITION
(1)	EVEN PARITY	CLOSED
	ODD PARITY	OPEN
	NONE	OPEN
(2)	ODD PARITY	CLOSED
	EVEN PARITY	OPEN
	NONE	OPEN
(3)	SEVEN DATA BITS	OPEN
	EIGHT DATA BITS	CLOSED
(4)	ONE STOP BIT	CLOSED
	TWO STOP BITS	OPEN
(5)	X-ON/X-OFF PROTOCOL	CLOSED
	NOT SELECTED	OPEN
(6)	EIA DATA	OPEN
	CURRENT LOOP DATA*	CLOSED

* NOT AVAILABLE

DIP NO. 1

SWITCH NO.	DESIRED FUNCTION	SWITCH POSITION
(1)	Data Terminal Ready Protocol Selected	CLOSED
	Not Selected	OPEN
(2)	Reverse Channel Protocol Selected	CLOSED
	Not Selected	OPEN
(3)	Line Feed After Carriage Return	OPEN
	No Auto LF	CLOSED
(4)	Reverse Channel (+) for Buffer Full	CLOSED
	Reverse Channel (-) for Buffer Full	OPEN
(6) (7) (8)	See Baud Rate Selection Table	

BAUD RATE SELECTION TABLE

BAUD RATE	SWITCH SETTINGS (6)	(7)	(8)
110	OPEN	OPEN	OPEN
150	CLOSED	OPEN	OPEN
300	OPEN	CLOSED	OPEN
1200	CLOSED	CLOSED	OPEN
2400	OPEN	OPEN	CLOSED*
4800	CLOSED	OPEN	CLOSED
9600	OPEN	CLOSED	CLOSED

Figure 4-3. DIP SWITCH SETTINGS, CONTROL PANEL

TABLE 4-1 ELECTRONIC OPTION

J10 **	J11	J12	J13	OPTION	PLATFORM CODE ("C" ARTWORK AND ABOVE ONLY) X1	X3	X4	X5	X6	X7	X8
4	0	0	0	ROM/CDCC VFU LOAD	-	-	-	-	14	04	14
	1			INVERTED DATA STROBE	-	-	-	-	-	-	-
	16			ESCAPE CONTROL OF BIT 8	-	-	-	-	-	-	-
		4		CDCC VFU LOAD (STD)		*					
		1		NON GATED STROBE	-	-	-	-	-	-	-
			1	12 CPI	SEE TABLE 3 FOR ADJUSTMENTS						
			2	15 CPI	SEE TABLE 3 FOR ADJUSTMENTS						
1	0	0	0	1K PROM/CDCC VFU LOAD	-	-	-	-	14	16	30
2	0	0	0	2K PROM/CDCC VFU LOAD	-	-	-	-	05	21	21
0	0	0	0	Identifies boards shipped prior to release of Rev. C (and above) artwork. No longer to be marked on logics.	NA	NA	NA	NA	NA	NA	NA

SUM OF BINARY NUMBERS
EQUALS JUMPER OPTION CODE

SUM OF NUMBERS
SELECTED EQUALS X2

Select one set dependent on type firmware used.

*** X2 is not used

** = J10 Value 1, 2 or 4 marked on board only to identify type firmware installed in manufacturing. J10 Value "0" will not be marked on boards, but will always be part of an extended number on PNDB or Spares Orders.

* Does not change standard platform value.

- Indicates unused platform.

TABLE 4-2 PLATFORM CONFIGURATION

PLATFORM LOCATION	GROUP	OCTAL CODE	BINARY CODE	PLATFORM FROM	PIN TO	SIGNAL FUNCTION	REMARKS
X3	I	20	0	1	15	HALF DUPLEX	
			1	1	16	FULL DUPLEX	
	II	10	0	14	2	INT SUPPLY	
			1	14	3	EXT SUPPLY	
	III	4	0	4	12	CURRENT LOOP DATA	
			1	4	13	EIA DATA	
	IV	2	0	11	5	HALF DUPLEX	
			1	11	6	FULL DUPLEX	
X3	V	1	0	7	9	EXT SUPPLY	
			1	7	10	INT SUPPLY	

TABLE 4-2 PLATFORM CONFIGURATION

PLATFORM LOCATION	GROUP	OCTAL CODE	BINARY CODE	PLATFORM FROM	PIN TO	SIGNAL FUNCTION	REMARKS
X6	I	20	0	1	16	1K PROM MEM #5	
			1	1	16	2K PROM MEM #5	
	II	10	0	14	2	2K PROM MEM #4	
			1	14	3	1K PROM MEM #4	
	III	4	0	4	12	2K PROM MEM #5	
			1	4	13	1K PROM MEM #5	
	IV	2	0	11	5	1K PROM MEM #5	
			1	11	6	2K PROM MEM #5	
X6	V	1	0	7	9	1K PROM MEM #3	
			1	7	10	2K PROM MEM #3	
X7	I	20	0	1	15	1K PROM MEM #4	
			1	1	16	2K PROM MEM #4	
	II	10	0	14	2	2K PROM OR TI 4K ROM MEM #1	
			1	14	3	1K PROM MEM #1	
	III	4	0	4	12	2K PROM MEM #3	
			1	4	13	1K PROM MEM #3	
	IV	2	0	11	5	2K PROM OR TI 4K ROM MEM #1	
			1	11	6	1K PROM MEM #1	
X7	V	1	0	7	9	1K PROM MEM #3	
			1	7	10	2K PROM MEM #3	

TABLE 4-2 PLATFORM CONFIGURATION

PLATFORM LOCATION	GROUP	OCTAL CODE	BINARY CODE	PLATFORM FROM	PIN TO	SIGNAL FUNCTION	REMARKS
X8	I	20	0	1	15	4K PROM MEM #1	
			1	1	16	1K OR 2K PROM MEM #1	
	II	10	0	14	2	2K PROM MEM #4	
			1	14	3	1K PROM MEM #4	
	III	4	0	4	12	1K PROM, OR 2K PROM MEM #1	
			1	4	13	T1 4K ROM MEM #1	
	IV	2	0	11	5	NOT USED	
			1	11	6	NOT USED	
X8	V	1	0	7	9	1K PROM OR TI 4K ROM MEM #1	
			1	7	10	2K PROM MEM #1	

TABLE 4-3 PRINT HEAD SPEED

MODEL	DENSITY	CHAR MATRIX	TIME u SEC ME89-10
704	10 CPI	7x7	430-440
		7X9, 5x7, 9x7, 9x9	470-480
	12 CPI	7x7	520-530
		7x9, 5x7, 9x7, 9x9	565-575
	15 CPI	7x7	650-660
		7x9, 5x7, 9x7, 9x9	710-720

TABLE 4-4 TIMING FENCES/DENSITY			
MODEL	DENSITY	CHAR MATRIX	TIME FENCE PART #
704	10 CPI	7x7, 7x9	63703159-3001
		5x7, 9x7, 9x9	63701127-3001
	12 CPI	7x7, 7x9	63703159-3002
		5x7, 9x7, 9x9	63701127-3002
	15 CPI	7x7, 7x9	63703159-3003
		5x7, 9x7, 9x9	63701127-3003

TABLE 4-5
PROM CONFIGURATION TABLE

	X6(1)	X6(2)	X6(3)	X7(1)	X7(2)	X7(3)	X8(1)	X8(2)
MEMORY LOCATION #1								
1K (8708)					12		20	
INTEL 2K (2716)					00		21	
4K (4732)					00		04	
MEMORY LOCATION #3								
1K (8708)			00			04		
INTEL 2K (2716)			01			01		
MEMORY LOCATION #4								
1K (8708)		10		00				10
INTEL 2K (2716)		00		20				00
MEMORY LOCATION #5								
1K (8708)	04							
INTEL 2K (2716)	22							

NOTE 1: X6, X7 and X8 are additive in the horizontal direction. The following examples will explain the procedures for obtainting the octal platform dash condition.

EX #1 ALL 1K PROMS		EX #2 ALL INTEL 2K PROMS			
X6(1) = 04		X6(1) = 22		MEM #1 = 4K	
X6(2) = 10	X6=14	X6(2) = 00	X6=23	MEM #4 = 2K	
X6(3) = 00		X6(3) = 01		MEM #5 = 1K	
X7(1) = 00		X7(1) = 20		X6(1) = 04	
X7(2) = 12	X7=16	X7(2) = 00	X7=21	X6(2) = 00	X6=04
X7(3) = 04		X7(3) = 01		X6(3) = --	
X8(1) = 20	X8=30	X8(1) = 21	X8=21	X7(1) = 20	
X8(2) = 10		X8(2) = 00		X7(2) = 00	X7=20
				X7(3) = --	
				X8(1) = 04	X8=04

TABLE 4-6

RECOMMENDED PREVENTIVE MAINTENANCE

The recommended preventive maintenance (P.M.) schedule, if followed closely and accomplished at the intervals noted, will ensure maximum operating efficiency and maximum mean time between failures. The recommended cleaning materials, lubricants and tools for the P.M. are as follows:

A. CLEANING MATERIALS	MEDIUM BRISTLE CLEANING BRUSH, TWO SOFT CLEAN CLOTHS, MILD DETERGENT
B. LUBRICANTS	RHEOLUBE NO. 723MS CDCC SPEC. NO. 30050004-0001
C. TOOLS	REFER TO SECTION 4.5 OF THE MAINTENANCE SECTION

NOTE: WHEN PERFORMING THE PREVENTIVE MAINTENANCE (P.M.) BE VISUALLY ALERT FOR POSSIBLE PROBLEMS. LOOK FOR LOOSE WIRES AND PINS, NEED FOR LUBRICATION, LOOSE HARDWARE, CHAFING OF CABLES AND BADLY WORN PARTS. DO ONLY THE SCHEDULED P.M. ON A PRINTER THAT IS OPERATING PROPERLY.

ASSEMBLY	FREQUENCY	CLEAN	INSPECT
Cover Assemblies	As required	Clean all cover assemblies using a mild detergent, as required.	
Character Printing Assemblies	6 Months	Clean print area of all paper dust, dirt, etc. (Use vacuum cleaner, if available).	
Print Head Assembly	Each Ribbon Change	Using a soft clean cloth, wipe the front of the print head of all dried ink.	
Ribbon Cartridge Assembly	Each Ribbon Change		Inspect cartridge for proper ribbon tracking.

TABLE 4-6

RECOMMENDED PREVENTIVE MAINTENANCE

ASSEMBLY	FREQUENCY	CLEAN	INSPECT
Timing Fence Assembly	6 Months	Using a soft clean cloth, wipe both sides of timing fence. CAUTION NEVER USE AN ORGANIC SOLVENT AS THIS WILL DAMAGE TIMING FENCE.	Inspect for scratches in the encoder lines and for proper mechanical alignment of timing fence.
Stepper Motor Assembly, Carriage Drive	6 Months		Inspect for proper tension of main drive belt.
Stepper Motor Assembly, Paper Drive	6 Months		Inspect for proper tension of paper feed timing belt
Platen Assembly	6 Months	Clean platen assembly using a mild detergent.	
Column Scale Tear Bar Assembly	6 Months	Clean column scale/ tear bar using a mild detergent.	
Frame Assemblies	6 Months	Clean the upper and lower guide bars usinng a soft clean cloth.	

NOTE: AFTER PERFORMING THE PREVENTIVE MAINTENANCE OPERATE PRINTER TO ENSURE GOOD, CLEAN PRINT QUALITY.

TABLE 4-7

TROUBLESHOOTING GUIDE

MALFUNCTION	SYMPTOM	CAUSES
A. POWER FAILURE	1. TOTAL	1. Damaged power cord. 2. Open 5V supply fuse.
	2. INTERMITTENT/PARTIAL	1. Defective logic board. 2. Improper A.C. line voltage.
B. IMPROPER PRINTING	1. HEAD MOVES, BUT NO PRINT/ POOR REGISTRATION OR ERRATIC PRINT.	1. Improper print head position. 2. Dirty fingerboard connector from print head. 3. Dirty or defective timing fence. 4. Improper alignment of optical pickup assembly. 5. Defective video amplifier. 6. Defective ribbon cable. 7. Defective logic board.
	2. MISSING DOTS, POOR OR INTERMITTENT PIN REGISTRATION ALL CHARACTERS	1. Improper print head position. 2. Dirty fingerboard connector from print head. 3. Dirty or defective timing fence. 4. Defective logic board. 5. Defective ribbon cable. 6. Defective video amplifier.
	3. MISSING OR EXTRA DOTS CERTAIN CHARACTERS ONLY	1. Defective ROM. 2. Defective P.C. runs in character generator.
	4. LINE ACROSS PAGE	1. Improper print head penetration. 2. Defective print wires. 3. Defective ribbon cable. 4. Defective video amplifier.

TABLE 4-7

TROUBLESHOOTING GUIDE

MALFUNCTION	SYMPTOM	CAUSES
C. DRIVE FAILURE	1. ERRATIC CARRIAGE MOVEMENT	1. Improper carriage drive belt tension. 2. Dirty carriage guide bars. 3. Defective idle pulley, drive pulley and drive belt.
	2. CARRIAGE STICKS OR BINDS	1. Optics block contacting timing fence. 2. Improper carriage drive belt tension. 3. Head penetration too tight.
	3. CARRIAGE MOVES FORWARD, BUT DOES NOT RETURN	1. Defective EOP switch. 2. Defective logic board. 3. Missing video amplifier signal $\overline{V1}$ or $\overline{V2}$.
	4. CARRIAGE DOES NOT MOVE FORWARD	1. Defective RTP switch. 2. Defective stepper motor. 3. Defective logic board. 4. Inappropriate input data.
D. RIBBON FEED FAILURE	1. NO RIBBON FEED	1. Ribbon twisted or jammed. 2. Ribbon cartridge pinch rollers open.
	2. NO RIBBON FEED DURING FORWARD/REVERSE CARRIAGE MOTION	1. Ribbon feed mono-filament line broken. 2. Ribbon drive gears not meshed with ribbon cartridge gears.
E. PAPER MOVEMENT FAILURE	1. PAPER SKEW OR JAM	1. Print head too close to paper. 2. Improper pin feed sprocket alignment. 3. Improper tractor drive belt adjustment. 4. Paper pan friction against forms.

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CENTRONICS
data computer corporation
Hudson, New Hampshire 03051
Telephone (603) 883-0111

CENTRONICS TOOL KIT
(63002399-6001)

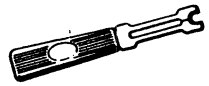
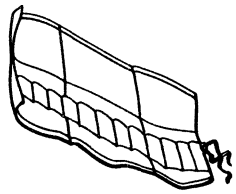
	UNIVERSAL HANDLE	30600002-3001		"T" HANDLE HEX KEY • 3/32-Inch • 5/32-Inch	 30600002-3017 30600002-3018
	EXTENSION • 4-Inch	30600002-3002		HEX KEY • 1/16-Inch • .050-Inch • 1.5mm • 2.0mm • 2.5mm • 3.0mm	 30600002-3025 30600002-3024 30600002-3020 30600002-3021 30600002-3022 30600002-3023
	NUT DRIVER • 4mm • 5.5mm • 7mm • 8mm • 10mm	 30600002-3003 30600002-3004 30600002-3005 30600002-3006 30600002-3007		WRENCH • SPANNER	 63003105-3001
	PHILLIPS INSERT • METRIC NO.1 • METRIC NO.2	 30600002-3030 30600002-3031		SNAP RING HOLDER • 4mm • 5mm	 30600002-3033 30600002-3034
	SCREWDRIVER • SLOTTED HEAD	30600002-3008		SPRING HOOK	30600002-3032
	PLIERS • NEEDLE NOSE	30600002-3010		BOX WRENCH • 17/19mm	 30600002-3035
	OPEN END WRENCH • 5x5.5mm • 6x7mm	 30600002-3011 30600002-3012		TOOL POUCH	30600002-3019
	COMBINATION OPEN END, BOX WRENCH • 8mm • 10mm	 30600002-3013 30600002-3014			

Figure 4-4. RECOMMENDED TOOLS

SECTION 5
ADJUSTMENTS

5.1 INTRODUCTION

This section contains adjustment procedures on the following printer assemblies:

5.2 CHARACTER PRINTING
5.3 PAPER MOTION
5.4 ELECTRICAL

Adjustment procedures should be performed whenever an affected printer assembly is replaced or to correct an improper operation. Check the adjustment parameters before performing the adjustment to ensure it is necessary.

5.2 CHARACTER PRINTING ADJUSTMENTS

5.2.1 PENETRATION ADJUSTMENT, PRINT HEAD ASSEMBLY (Figure 5-1)

A. Loosen penetration control knob.

B. Move penetration control knob away from platen.

C. Loosen hardware securing the adjusting stop plate.

D. Insert a 0.177 mm (0.007 in.) feeler guage between front of print head and platen.

E. Move penetration control knob and adjusting stop plate forward until 0.177 mm (0.007 in.) gap is met.

F. Tighten adjsting stop plate hardware and penetration control knob.

NOTE: IF REPLACING PRINT HEAD ASSEMBLY AND 0.177 IN. (0.007 in.) GAP IS NOT MET, LOOSEN ADJUSTING STOP PLATE HARDWARE AND ADJUST PER STEPS D THROUGH F ABOVE.

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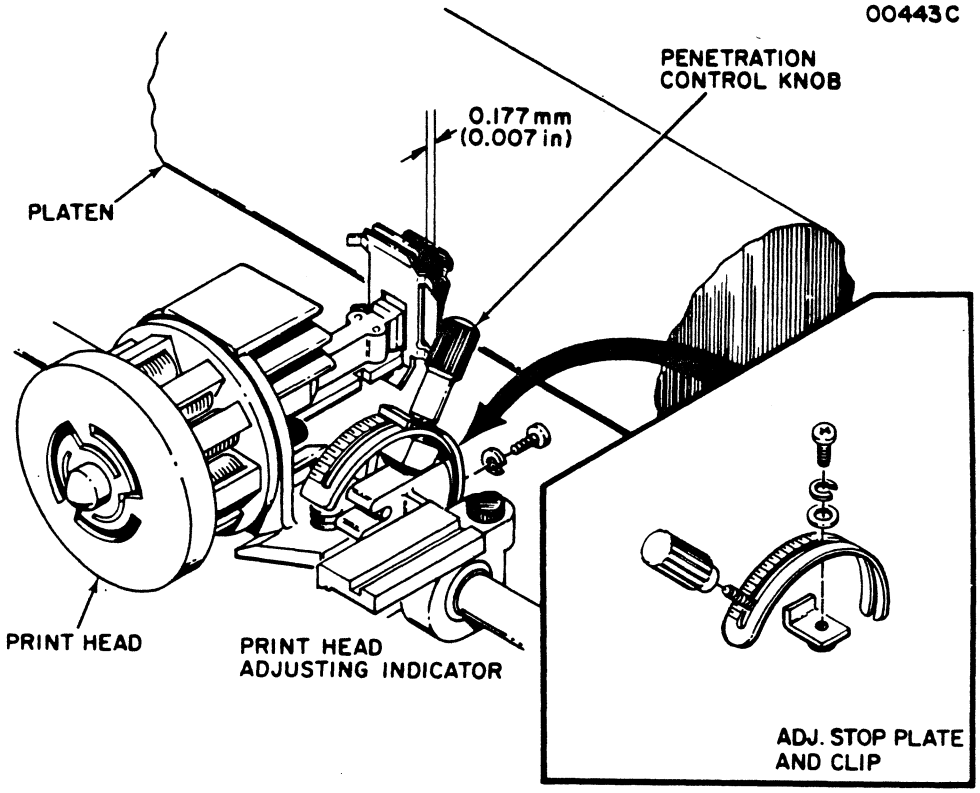

Figure 5-1. PENETRATION ADJUSTMENT, PRINT HEAD ASSEMBLY

5.2.2 TIMING FENCE ADJUSTMENT (Figure 5-2)

A. Loosen four socket head screws and move fence left or right so that first window of fence is located 106 mm (4.2 in.) from left frame.

B. Tighten four socket head screws securing fence.

C. Move video amplifier left to right and ensure optics block on underside of video amplifier does not contact fence. If optics block should contact fence refer to paragraph 5.4.1.A for adjustment.

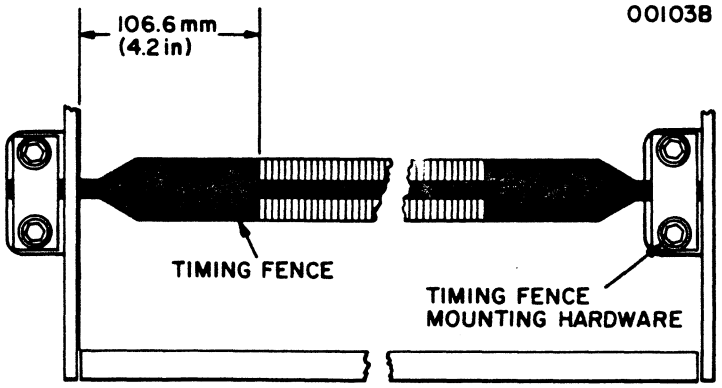

Figure 5-2. TIMING FENCE ADJUSTMENT

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5.2.3 CARRIAGE ACTUATOR ARMS ADJUSTMENT (Figure 5-3)

A. Bend ready to print (RTP) switch actuator arm parallel to and 59 mm (2.3 in.) from center of upper guide bar.

B. Bend end of print (EOP) switch actuator arm parallel to and 55 mm (2.1 in.) from center of upper guide bar.

C. After actuator arms have been adjusted, slowly move carriage assembly from left to right insuring arms do not contact the RTP and EOP optics switches.

D. If actuator arm should contact switch, loosen two optical switch mounting screws and position switch so that actuator arm is centered in slot of switch.

E. Tighten optical switch mounting screws, if necessary.

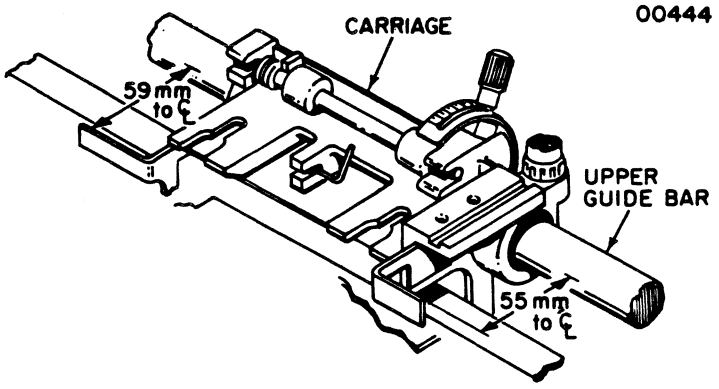

Figure 5-3. CARRIAGE ACTUATOR ARMS ADJUSTMENT

5.2.4 MAIN DRIVE BELT ADJUSTMENT (Figure 5-4)

A. With the carriage assembly in the left most position, adjust belt tension by turning clockwise (tighten) or counterclockwise (loosen) two adjusting screws on idle pulley assembly so that deflection at center of belt is 8 to 9 mm (9/16 in.) when a 300 gram (11 oz.) load is applied at the center of the belt.

NOTE: IT IS BEST TO USE A WIDE LOAD DISTRIBUTED 64 MM TO 74 MM (2-1/2 in. TO 3 in.) OVER THE BELT.

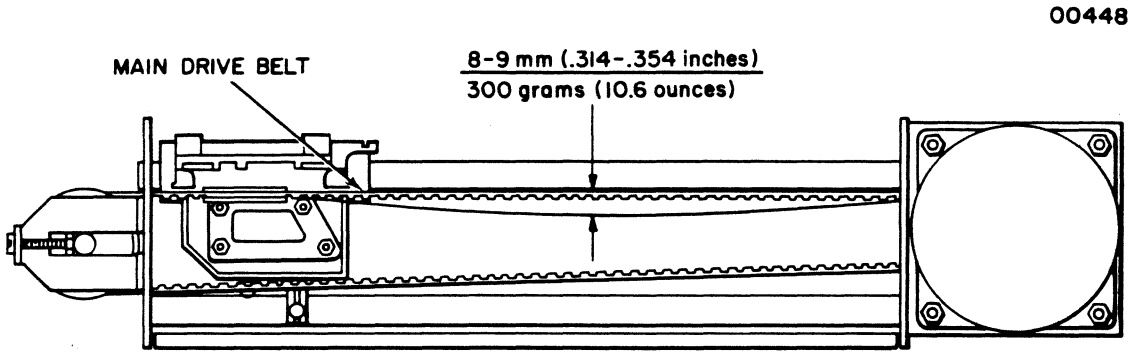

Figure 5-4. MAIN DRIVE BELT ADJUSTMENT

5.3 PAPER MOTION ADJUSTMENTS

5.3.1 PAPER FEED TIMING BELT ADJUSTMENT (Figure 5-5)

A. At a point equidistant from the line feed pulley and paper feed pulley adjust tension of belt by moving tension roller underneath belt up or down for a deflection of 4 to 5 mm (9/32 in.) when a 300 gram (11 oz.) load is applied.

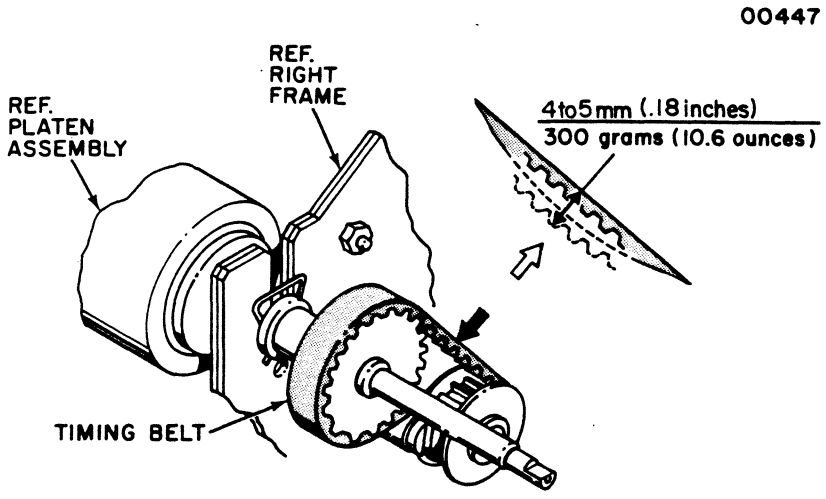

Figure 5-5 PAPER FEED TIMING BELT ADJUSTMENT

5.3.2 PLATEN ADJUSTMENT (Figure 5-6)

A. Operate printer and ensure print quality is uniform for the full line of characters printed. If print quality is not uniform (light to dark), the platen assembly is not parallel to the travel of the carriage. Adjust per steps B and C.

B. On left end of platen, loosen bolt and rotate adjusting plate and eccentric bushing slightly. Repeat steps A and B as required.

C. Tighten mounting hardware.

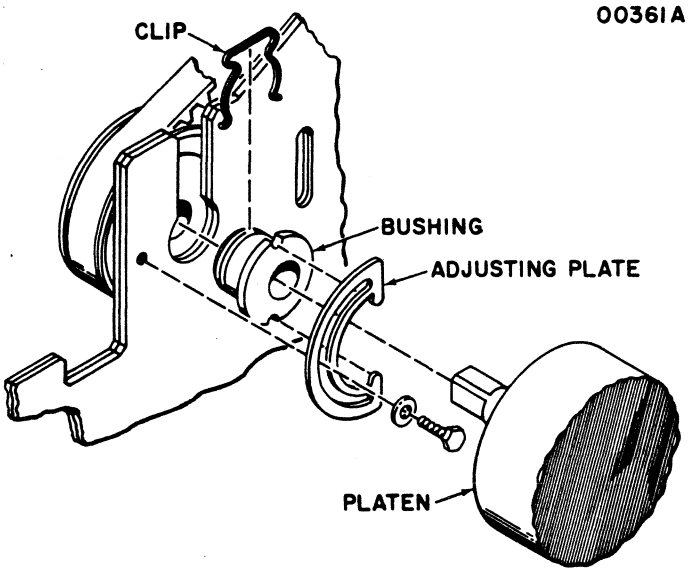

Figure 5-6. PLATEN ADJUSTMENT

5.3.3 TRACTOR DRIVE TIMING BELT TENSION (Figure 5-7)

A. Using adjustable tensioner on left side of frame, adjust belt tension so that deflection is 5 to 6 mm (1/4 in.) when a load of 300 grams (10.6 ounces) is applied at the middle of the belt.

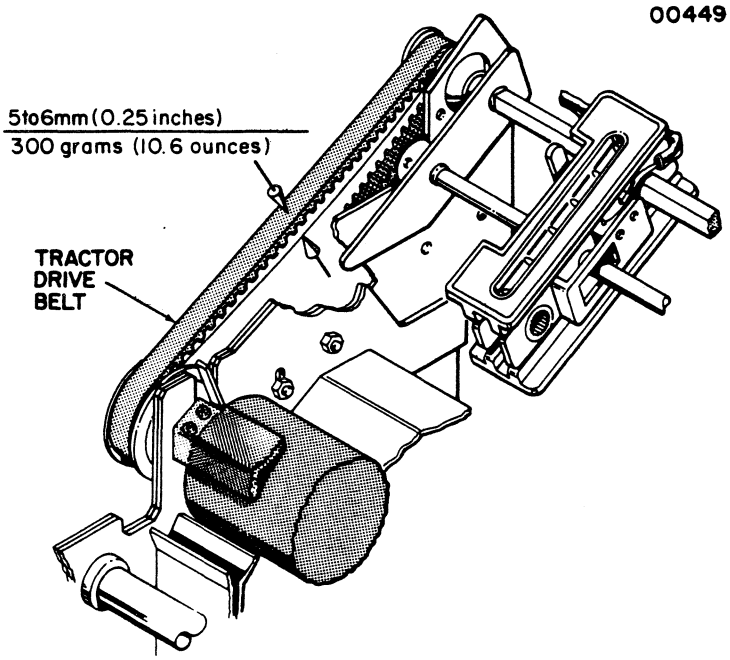

Figure 5-7. TRACTOR DRIVE TIMING BELT TENSION

5.3.4 PAPER TENSION ADJUSTMENT (Figure 5-8)

A. Adjust pin feed tractors, by turning eccentric knob on right side of tractor drive assembly, so plane of paper travel (top side of tractor unit) is tangent to the platen.

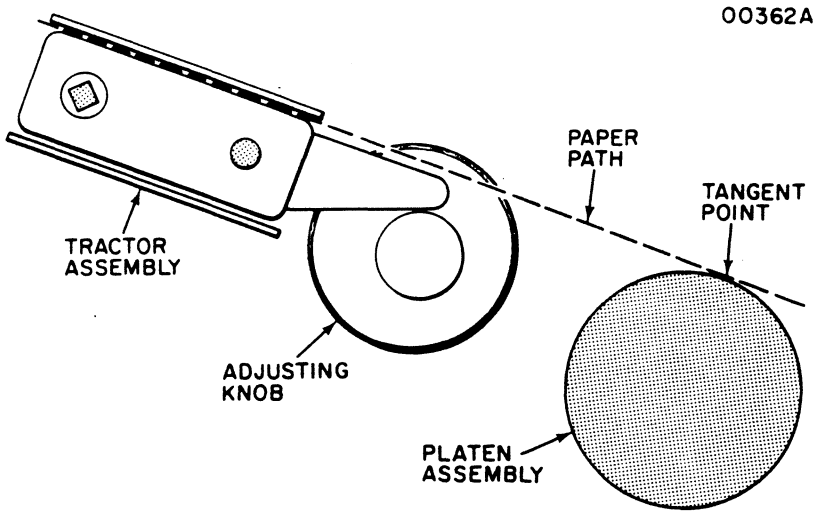

Figure 5-8. PAPER TENSION ADJUSTMENT

5.4 ELECTRICAL ADJUSTMENTS

5.4.1 VIDEO AMPLIFIER ADJUSTMENTS

NOTE: THE VIDEO AMPLIFIER CONTAINS AN OPTICAL PICKUP ASSEMBLY WHICH MUST BE ADJUSTED. STEPS A AND B DETAIL THE MECHANICAL ALIGNMENT OF THE PICKUP ASSEMBLY WHILE STEP C OUTLINES THE ELECTRICAL ADJUSTMENT.

A. Optical Pickup/Timing Fence Alignment (Figure 5-9)

1. Loosen hardware attaching the video amplifier to the carriage.

2. If required, loosen optical pickup mounting hardware and center pickup assembly over timing fence. Tighten optical pickup mounting hardware.

3. By moving the video amplifier up or down, align bottom of optical pickup assembly until it is parallel with bottom of timing fence.

4. Tighten video amplifier mounting hardware.

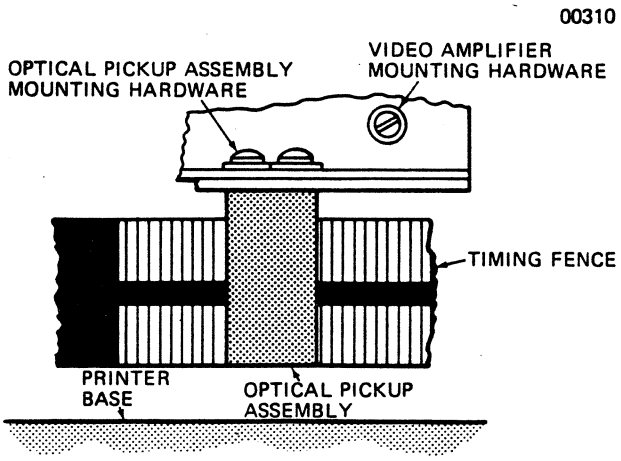

Figure 5-9. OPTICAL PICKUP/TIMING FENCE ALIGNMENT

B. Optical Pickup, Vertical Alignment (Figure 5-10)

1. Sight along the right edge of optical pickup assembly, and ensure that it is parallel with the encoder lines. If not, loosen video amplifier mounting hardware and adjust.

2. Sight along bottom edge of optical pickup assembly, and check parallelism with bottom edge of timing fence.

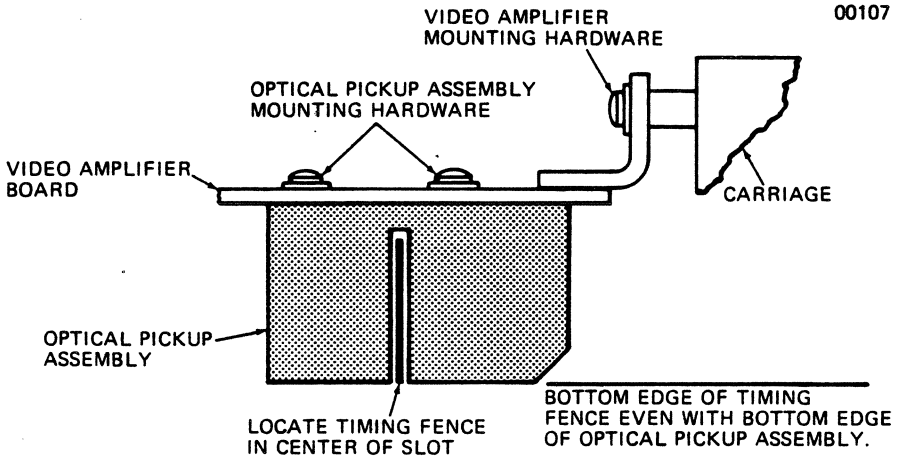

Figure 5-10. OPTICAL PICKUP, VERTICAL ALIGNMENT

C. Electrical Adjustment of Video Amplifier (Figure 5-11).

NOTE: THE VIDEO AMPLIFIER GENERATES THE TIMING SIGNALS USED FOR HORIZONTAL CHARACTER REGISTRATION. THE BI-DIRECTIONAL PRINTER REQUIRES A DUAL CHANNEL VIDEO AMPLIFIER. THE VIDEO NO. 1 (V1) AND VIDEO NO. 2 ($\overline{V2}$) SIGNALS ARE GENERATED AND AMPLIFIED BY THE VIDEO AMPLIFIER AS THE OPTICS BLOCK MOVES ACROSS THE TIMING FENCE. THE LOGIC BOARD DETERMINES THE FORWARD AND REVERSE DIRECTION OF THE PRINT HEAD BY COMPARING THE LEADING AND TRAILING EDGES OF ONE VIDEO CHANNEL SIGNAL WITH THE OTHER VIDEO CHANNEL SIGNAL. BOTH CHANNEL OUTPUTS, $\overline{V1}$ AND $\overline{V2}$, ARE ADJUSTED FOR A 50% DUTY CYCLE AND A CONSTANT 90° PHASE SHIFT BETWEEN CHANNELS. THE DUTY CYCLE AND PHASE ADJUSTMENTS ARE PERFORMED SEPARATELY AS FOLLOWS:

Duty Cycle Adjustment

1. Ensure that optics block on underside of video amplifier is centered over timing fence.

2. While manually moving carriage to the right and left, monitor and record the voltage level at E1 on the power driver board.

NOTE: VOLTAGE VARIES AS OPTICS BLOCK PASSES OVER LIGHT AND OPAQUE LINES ON TIMING FENCE. RECORD HIGHEST VOLTAGE OBSERVED.

3. Monitor and record voltage level at E2 on the power driver board.

4. By adjusting resistor R4 on the video amplifier, set voltage level to one-half the level recorded at E1. This reference voltage set-up approximates the proper video output duty cycle.

5. Monitor $\overline{V1}$ at E1 and check the duty cycle while the print head is moving at a constant speed. If duty cycle is not 50%, stop the print head, adjust R4 slightly, start print head motion and recheck duty cycle. Repeat until 50% duty cycle is achieved.

6. To adjust duty cycle of V2, repeat steps 1 through 5 while monitoring voltage at E2 and adjusting resistor R10 on the video amplifier.

Phase Shift Adjustment

1. Simultaneously monitor $\overline{V1}$ and E1 and $\overline{V2}$ at E2 on power driver board while print head is moving at a constant speed.

2. Check phase relationships between $\overline{V1}$ and $\overline{V2}$ as carriage moves in both forward and reverse directions. The phase difference between $\overline{V1}$ and $\overline{V2}$ should be a constant 90° over the entire travel of the carriage (i.e. width C equals 90° when it equals 1/4 width D). If phase adjustment is required, proceed to step 3.

3. Stop carriage, turn power off, and manually move carriage to the EOP switch.

4. Loosen, approximately one turn, the left side video amplifier mounting screw.

5. Move left side of board up until bottom of slotted mounting hole touches mounting screw.

6. Turn power on, start moving carriage and recheck phase adjustment.

7. If further adjustment is required, turn power off, move left side of board down slightly and recheck phase.

8. Repeat steps 6 and 7 until phase adjustment of $\overline{V1}$ and $\overline{V2}$ is correct.

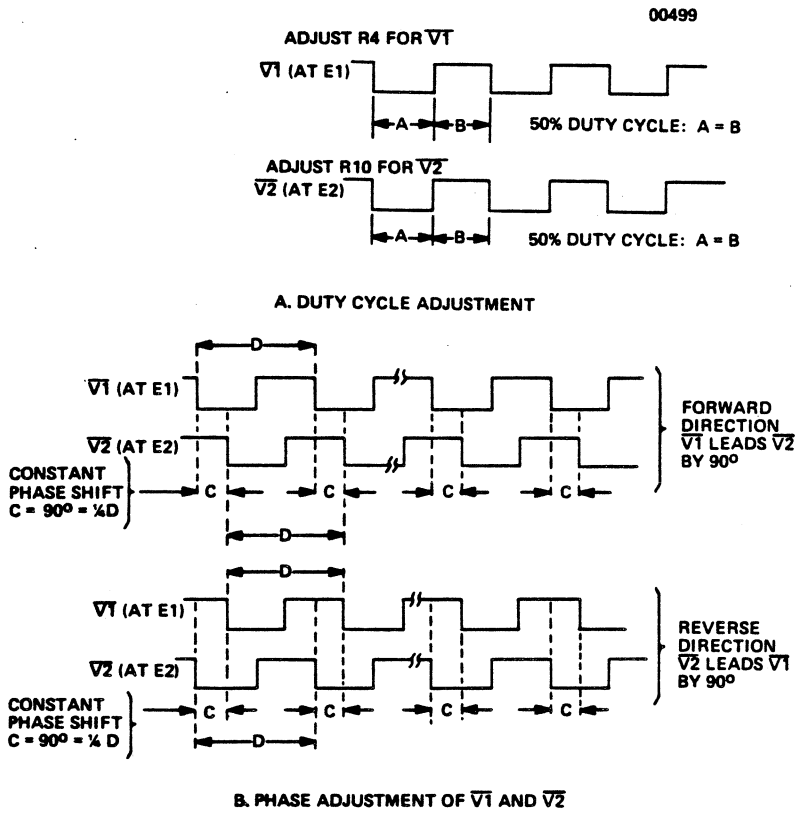

Figure 5-11. DUTY CYCLE AND PHASE ADJUSTMENT OF VIDEO AMPLIFIER

5.4.2 LOGIC BOARD ADJUSTMENTS

The following electrical adjustments may be required on the main logic board.

FUNCTION	SIGNAL NAME	ELEMENT/PIN	ADJUSTING RESISTOR	PULSE WIDTH
+5 Volts	+5V out	Test Point-TP4	R4	Adjust to +5V level
Print Head Speed	-	ME89-10	R40	See Table 4-3
Printer Strobe	PRTSTB	ME73-6	R50	425-450 usec

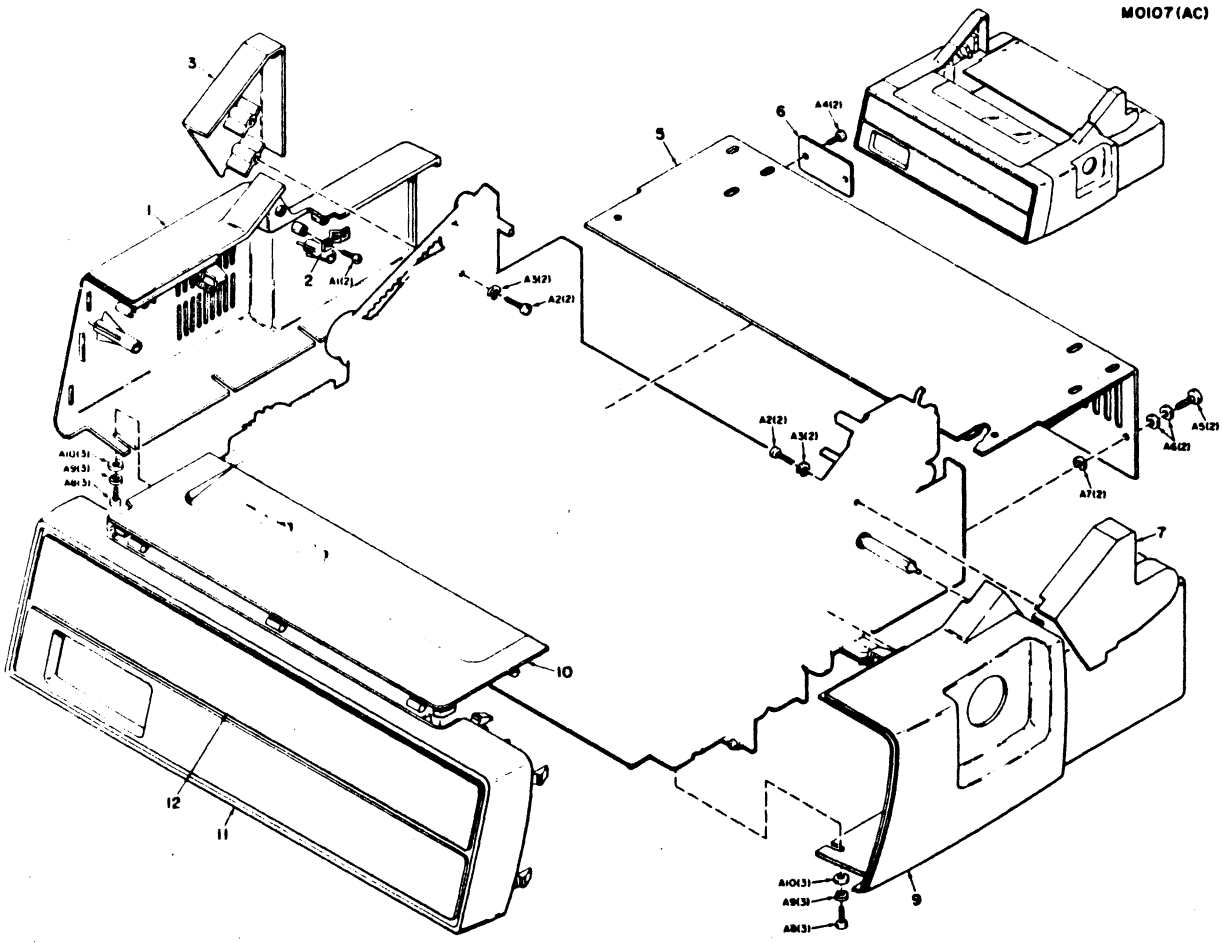

Figure 6-1. REMOVAL/REPLACEMENT, COVER ASSEMBLIES

SECTION 6

REMOVAL/REPLACEMENT

6.1 INTRODUCTION

This section details the removal/replacement procedures for the recommended spare parts in the printer. The section is organized as follows:

PARAGRAPH	DESCRIPTION	KIT/ASSEMBLY PART NUMBER
6.2	COVER ASSEMBLIES* (SEE NOTE 1)	-
6.3	PRINT HEAD ASSEMBLY	62001136-5002
6.4	POWER DRIVER BOARD ASSEMBLY	63703180-4002
6.5	TIMING FENCE ASSEMBLY	63703159-6XXX
6.6	VIDEO AMPLIFIER ASSEMBLY	63703164-4003
6.7	RIBBON CARTRIDGE ASSEMBLY	63700289-6001
6.8	CARRIAGE ASSEMBLY	81700217-5001
6.9	STEPPER MOTOR ASSEMBLY, CARRIAGE DRIVE	-
6.10	STEPPER MOTOR ASSEMBLY, PAPER DRIVE	-
6.11	PLATEN ASSEMBLY	81700228-5001
6.12	VERTICAL FORMAT UNIT	63703173-6001
6.13	TRACTOR DRIVE ASSEMBLY	81700243-5001
6.14	PIN FEED TRACTORS, LEFT/RIGHT	81700249-5001/81700247-5001
6.15	PRIMARY VOLTAGE ASSEMBLY	-
6.16	CAPACITOR ASSEMBLIES	63703190-6001
6.17	FAN ASSEMBLY	63703161-6001
6.18	LOGIC BOARD ASSEMBLY	63703216-4XXX
6.19	CONTROL PANEL ASSEMBLY	63761113-6000

6.2 COVER ASSEMBLIES (Figure 6-1)

TOOLS REQUIRED: Phillips and Slotted Head Screwdrivers

A. Clear Cover (10)

Lift cover to release tension on clamping springs and remove.

B. Cover, Front (11)

Unsnap six front cover clips from left and right covers and remove.

*NOTE 1: THE COVER ASSEMBLIES ARE NOT RECOMMENDED SPARE PARTS, AND ARE DETAILED FOR REFERENCE PURPOSES ONLY.

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C. Cover Assembly, Left (1)

Remove three screws, lockwashers and flatwashers attaching cover to printer base.

D. Cover Assembly, Right (9)

Remove three screws, lockwashers and flatwashers attaching cover to printer base.

E. Cover, Electronic Module (5)

Remove two snap rings, screws and four flatwashers mounting cover to electronic module frame.

F. Cover, Tractor Drive, Left (3)

Remove two screws and flatwashers mounting cover to left side frame.

G. Cover Tractor Drive, Right (7)

Remove two screws and flatwashers mounting cover to right side frame.

6.3 PRINT HEAD ASSEMBLY (Figure 6-2)

TOOLS REQUIRED: None

A. Remove clear cover from printer.

B. Remove ribbon from print head ribbon guides.

C. Remove fingerboard P037 on print head cable from connector J037.

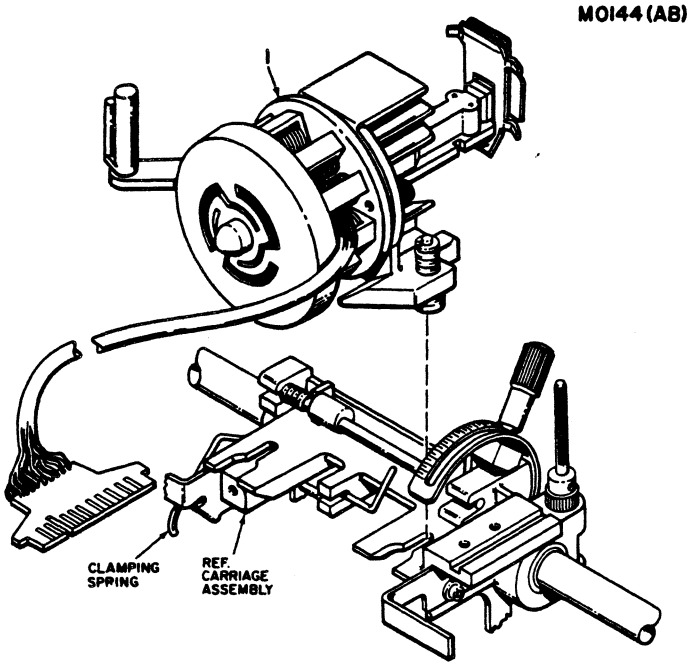
D. Release clamping spring tension, on left side off carriage assembly, by pulling spring up and over spring retainer.

E. Remove the print head assembly (1) by sliding off carriage assembly towards the front of the printer.

F. To install print head reverse steps A through E.

NOTE: WHEN INSTALLING THE PRINT HEAD ASSEMBLY, ENSURE THE CLAMPING SPRING CATCHES THE LIP UNDERNEATH THE PRINT HEAD THEN PULL SPRING UP AND OVER SPRING RETAINER.

G. Refer to paragraph 5.2.1, Section 5, for adjustments on the print head assembly.



ITEM	PART NUMBER	DESCRIPTION
1	62001136-5002	Print Head Assembly

Figure 6-2. REMOVAL/REPLACEMENT, PRINT HEAD ASSEMBLY

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6.4 POWER DRIVER BOARD ASSEMBLY (Figure 6-3)

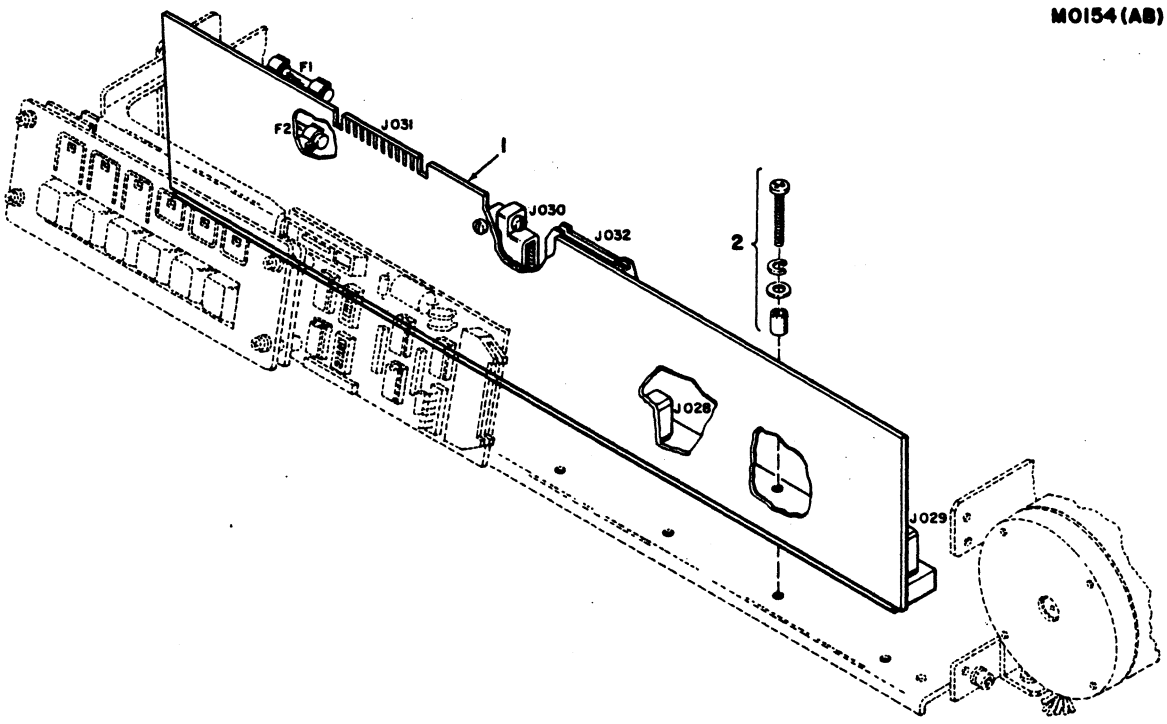
TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove clear and front covers from printer.

B. Disconnect all connectors from power driver board assembly.

C. Remove five mounting screws, lockwashers, flatwashers and spacers (2); and remove power driver board assembly.

D. To install power driver board reverse steps A through C.



ITEM	PART NUMBER	DESCRIPTION
1	63703180-4002	Power Driver Board Assembly
2	34000351-2021	Screw, M3 x 16 mm Lg, Pan Hd Phillips
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3
	36614403-2050	Spacer, .18 Lg x .25 Dia

Figure 6-3. REMOVAL/REPLACEMENT, POWER DRIVER BOARD ASSEMBLY

6.5 TIMING FENCE ASSEMBLY (Figure 6-4)

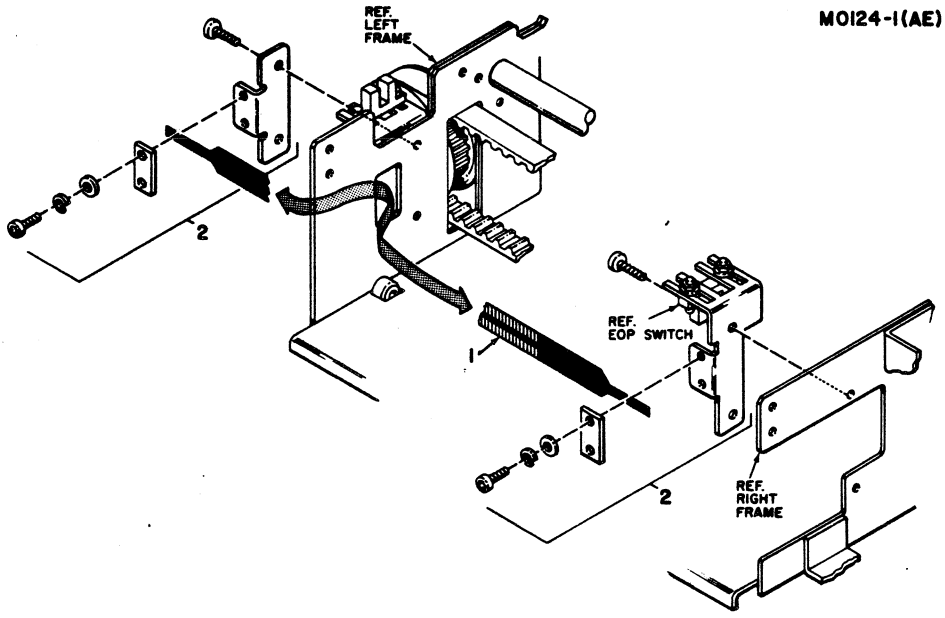
TOOLS REQUIRED: 3 mm Hex Key

A. Remove clear and front covers from printer.

B. Loosen four hex head screws (2) and remove fence (1A, 1B, 1C) from printer.

C. To install timing fence, reverse steps A and B.

D. Refer to paragraph 5.2.2, Section 5, for adjustments on the timing fence.



ITEM	PART NUMBER	DESCRIPTION
1A	63703159-3001	Timing Fence, 10 CPI, 7x7
1B	63703159-3002	Timing Fence, 12 CPI, 7x7
1C	63703159-3003	Timing Fence, 15 CPI, 7x7
2	81700193-2001	Bracket, Left
	81700181-2001	Clamp, Timing Fence
	34000355-2010	Screw, M3 x 8 mm Lg, Socket Head
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3
	81700192-2001	Bracket, Right

Figure 6-4. REMOVAL/REPLACEMENT, TIMING FENCE ASSEMBLY

6.6 VIDEO AMPLIFIER ASSEMBLY (Figure 6-5)

TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove clear and front covers from printer.

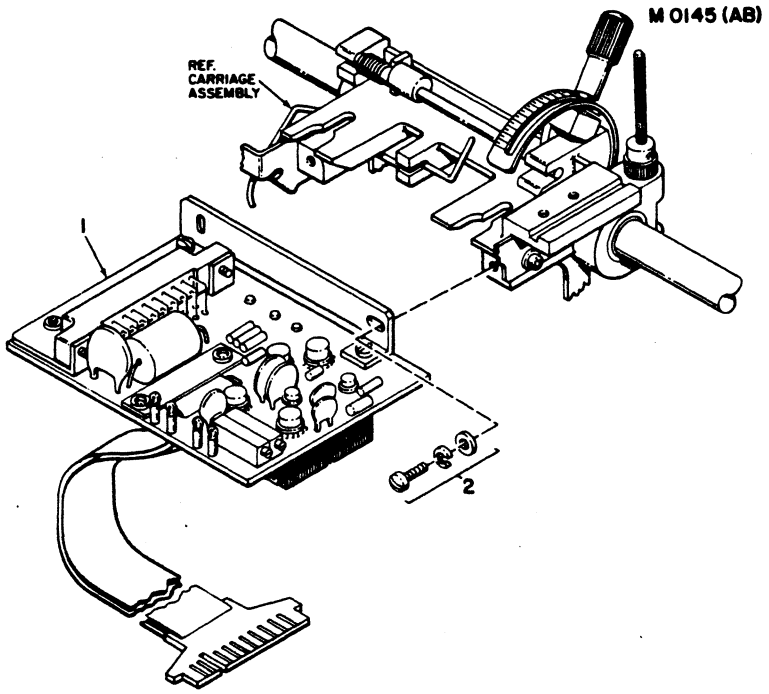
B. Remove print head cable fingerboard P037 from connector J037 on video amplifier.

C. Remove connector J036 of video amplifier cable from connector P036 on power driver board.

D. Remove two screws, lockwashers and flatwashers (2) mounting video amplifier to carriage, and remove video amplifier (1).

E. To install video amplifier, reverse steps A through D.

F. Refer to paragraph 5.4.1, Section 5, for adjustment procedures on video amplifier.



ITEM	PART NUMBER	DESCRIPTION
1	63703164-4003	Video Amplifier Assembly
2	34000351-2019	Screw, M3 x 10 mm Lg, Pan Hd Phillips
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3

Figure 6-5. REMOVAL/REPLACEMENT, VIDEO AMPLIFIER ASSEMBLY

6.7 RIBBON CARTRIDGE ASSEMBLY (Figure 6-6)

TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove clear cover from printer.

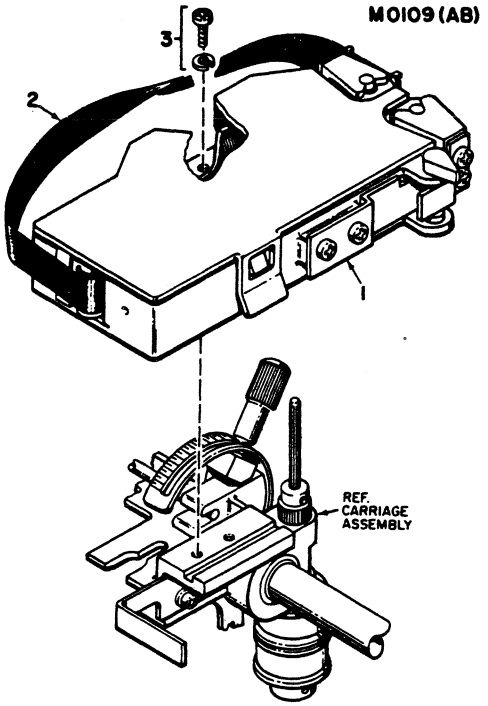
B. Remove print ribbon (2) from print head ribbon guides.

C. Remove two screws and lockwashers (3) mounting ribbon cartridge (1).

D. Remove ribbon cartridge (1) from printer.

E. To install ribbon cartridge, reverse steps A through D.

F. Refer to the OPERATOR'S MANUAL for ribbon replacement procedures.



ITEM	PART NUMBER	DESCRIPTION
1	535020001-5001	Ribbon Cartridge Assembly
2	-	Ribbon, Black*
3	34000351-2018	Screw, M3 x 8 mm Lg., Pan Hd. Phillips
	34000455-2004	Washer, Split Lock, M3

*Refer to the OPERATOR'S MANUAL for ribbon ordering purposes.

Figure 6-6. REMOVAL/REPLACEMENT, RIBBON CARTRIDGE ASSEMBLY

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6.8 LIGHTWEIGHT CARRIAGE ASSEMBLY (Figure 6-7)

TOOLS REQUIRED: Slotted and Phillips Head Screwdriver

A. Remove top, front, left and right covers per paragraphs 6.2.

B. Remove the print head assembly, power driver board assembly, timing fence, video amplifier and ribbon cartridge assembly per paragraphs 6.3, 6.4, 6.5, 6.6 and 6.7 respectively.

C. Loosen carriage drive belt (1) by loosening two locknuts (2) and turning, counterclockwise, two adjusting screws (3) on idle pulley assembly.

D. Remove the retaining ring (4) from the left end of the upper guide bar (5).

E. Remove screw (6), bolt (7), lockwasher (8) and guide bar support (9) mounting upper guide bar to right side frame.

F. Loosen locknut and screw (10) attaching bottom of carriage (11) to bottom guide bar (12).

G. Remove upper (13) and lower (14) ribbon drive wires from ribbon drive pulleys.

H. Remove the two screws and lockwashers (15) clamping the carriage drive belt to the carriage assembly.

I. While supporting the carriage, slide the upper guide bar to the right and through the carriage assembly and remove carriage.

NOTE: RETAIN THE RUBBER O-RING (16) REMOVED FROM THE LEFT END OF THE UPPER GUIDE BAR.

J. To replace the carriage assembly, reverse steps A through I.

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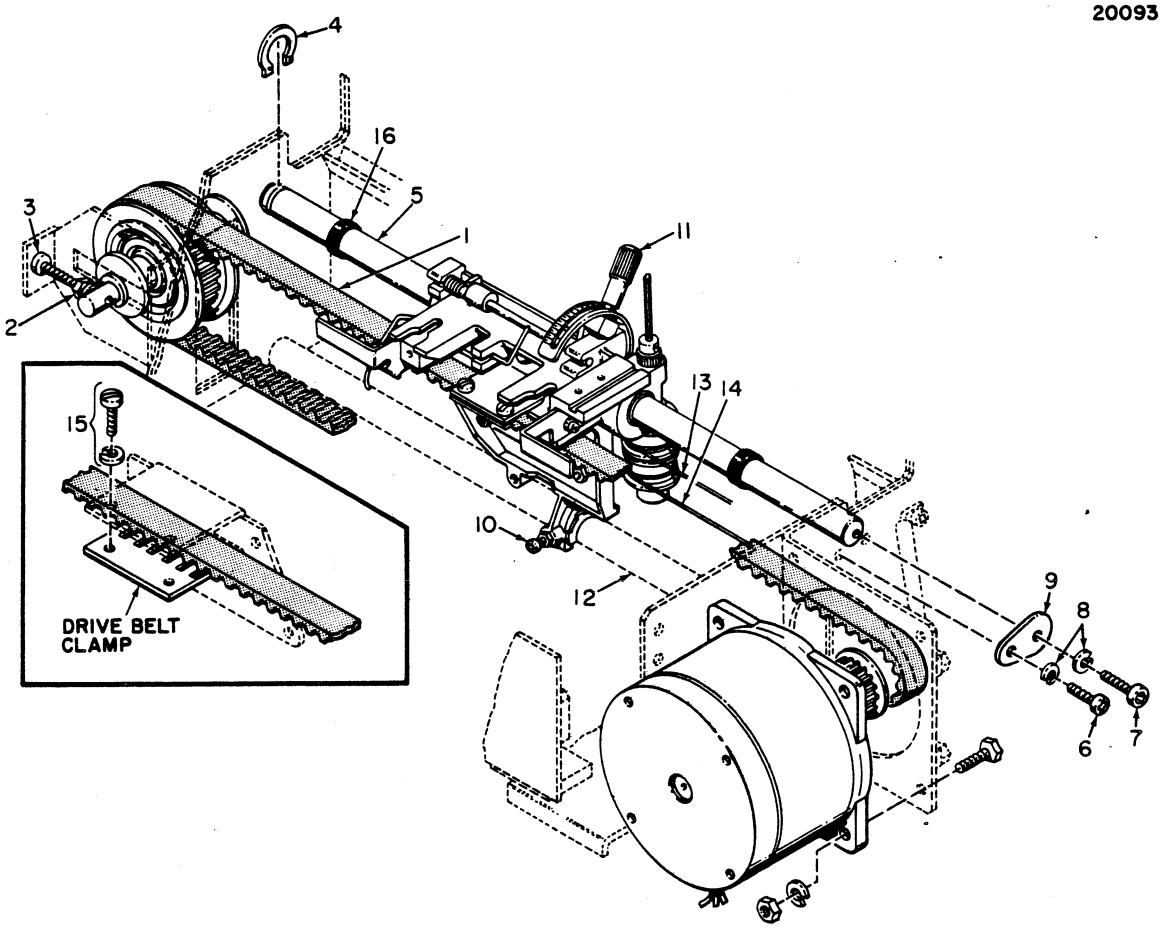

ITEM	PART NUMBER	DESCRIPTION
1	36400034-2001	Carriage Drive Belt
2	-	Locknuts
3	-	Adjusting Screws
4	-	Retaining Ring
5	-	Upper Guide Bar
6	-	Screw
7	-	Bolt
8	-	Lockwasher
9	-	Guide Bar Support
10	-	Locknut and Screw
11	81700217-5001	Carriage
12	-	Bottom Guide Bar
13	-	Upper Ribbon Drive Wire
14	-	Lower Ribbon Drive Wire
15	-	Screw and Lockwasher
16	-	Ribbon O-Ring

Figure 6-7. REMOVAL/REPLACEMENT, CARRIAGE ASSEMBLY

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6.9 STEPPER MOTOR ASSEMBLY, CARRIAGE DRIVE (Figure 6-8)

TOOLS REQUIRED: M5 Nut Driver, Phillips Head Screwdriver

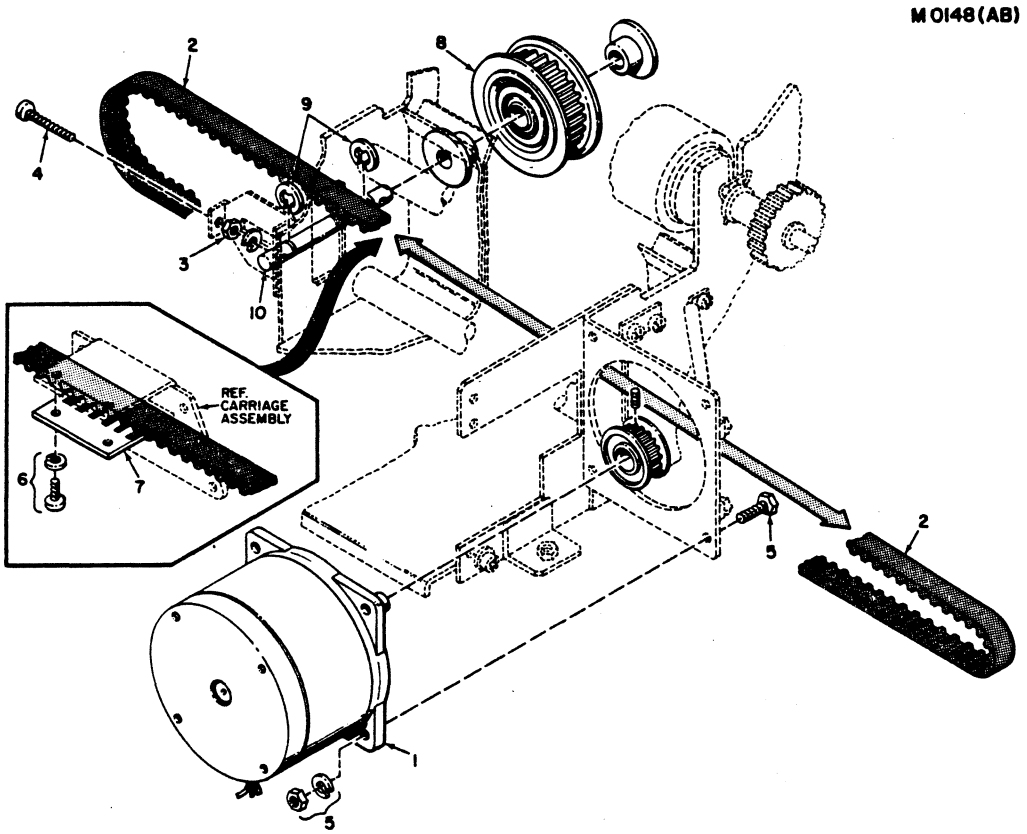
A. Remove top, front, left and right covers per paragraph 6.2.

B. Disconnect connector P028 on stepper drive motor (1) from connector J028 on power driver board assembly.

C. Loosen tension on main drive belt (2) by loosening two locknuts (3) and turning, counterclockwise, two adjusting screws (4) on idle pulley assembly.

D. Remove four mounting bolts and lockwashers (5), and remove stepper drive motor (1) from printer.

E. Remove main drive belt (2) from carriage assembly by removing two screws, lockwashers (6) and main drive belt holder (7).



ITEM	PART NUMBER	DESCRIPTION
1	30420003-1002	Stepper Drive Motor
2	36400034-2001	Main Drive Belt
3	34000661-2004	Nut, Hex, M3
4	34000660-2043	Adjusting Screw
5	34000664-20391	Bolt, M5 x 14 mm Lg.
	34000662-2007	Washer, Split Lock, M5

ITEM	PART NUMBER	DESCRIPTION
6	34000664-2017	Screw, M3 x 6 mm Lg.
	34000662-2006	Washer, Split Lock, M3
7	81700195-2001	Main Drive Belt Holder
8	81700198-5001	Idle Pulley
9	33100001-2008	Snap Ring
10	81700201-2001	Idle Pulley Shaft

Figure 6-8. REMOVAL/REPLACEMENT, STEPPER MOTOR ASSEMBLY, CARRIAGE DRIVE

F. Remove main drive belt and idle pulley (8) by removing two snap rings (9), adjusting screws (4) and slide idle pulley shaft (10) through idle pulley.

G. To install items in the carriage drive stepper motor, reverse steps A through E.

6.10 STEPPER MOTOR ASSEMBLY, PAPER DRIVE (Figure 6-9)

TOOLS REQUIRED: M5 Nut Driver

A. Remove left cover and electronic module cover per paragraph 6.2.

B. Disconnect two pin connector P029 from connector J029.

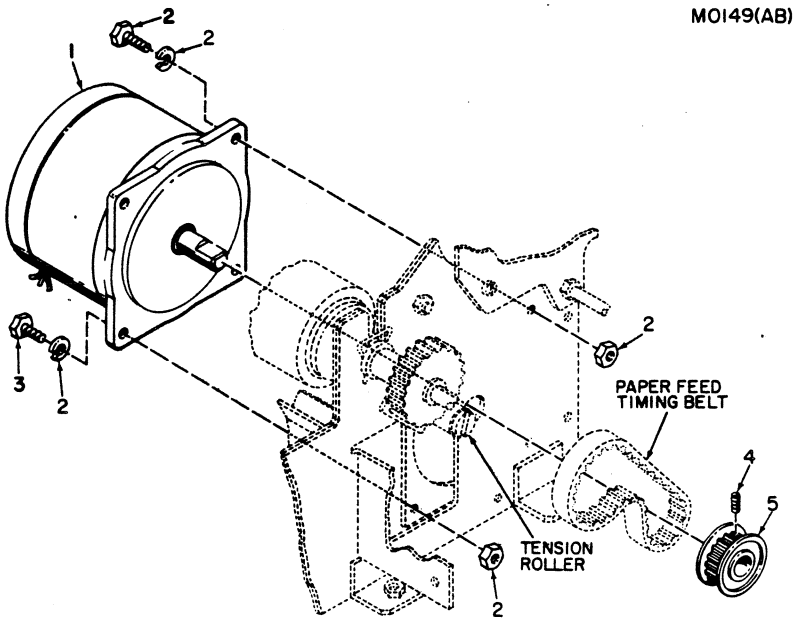
C. Loosen tension on paper feed timing belt by loosening screw mounting tension roller to right side frame.

D. Remove line feed pulley (5) by loosening set-screws (4) and sliding pulley off stepper motor shaft.

E. Remove mounting screws and lockwashers (2), and remove stepper motor assembly (1) from printer.

F. To install the stepper motor assembly, reverse steps A through E.

G. Refer to paragraph 5.3.1, Section 5, for adjustments on the paper drive stepper motor assembly.



ITEM	PART NUMBER	DESCRIPTION
1	30420003-1002	Stepper Motor Assembly, Paper Drive
2	34000664-2049 34000662-2007	Screw, M5 x 8 mm Lg., Hex Hd. Slotted Washer, Split Lock, M5
3	535323001-2001	Screw, M5 x 10 mm Lg., Hex Hd. Slotted
4	34000656-2033	Set-Screw, M4 x 6 mm Lg.
5	81700204-5001	Line Feed Pulley

Figure 6-9. REMOVAL/REPLACEMENT, STEPPER MOTOR ASSEMBLY, PAPER DRIVE

6.11 PLATEN ASSEMBLY (Figure 6-10)

TOOLS REQUIRED: M5 Hex Key, Flat Blade Screwdriver, M4 Open End Wrench

A. Remove top, front, left and right covers per paragraph 6.2.

B. Loosen tension on paper feed timing belt by loosening screw mounting tension roller to right side frame.

C. Slip the paper feed timing belt off paper feed pulleys.

D. Loosen two set-screws (1) mounting the tractor drive pulley (2) to left end of platen and remove pulley.

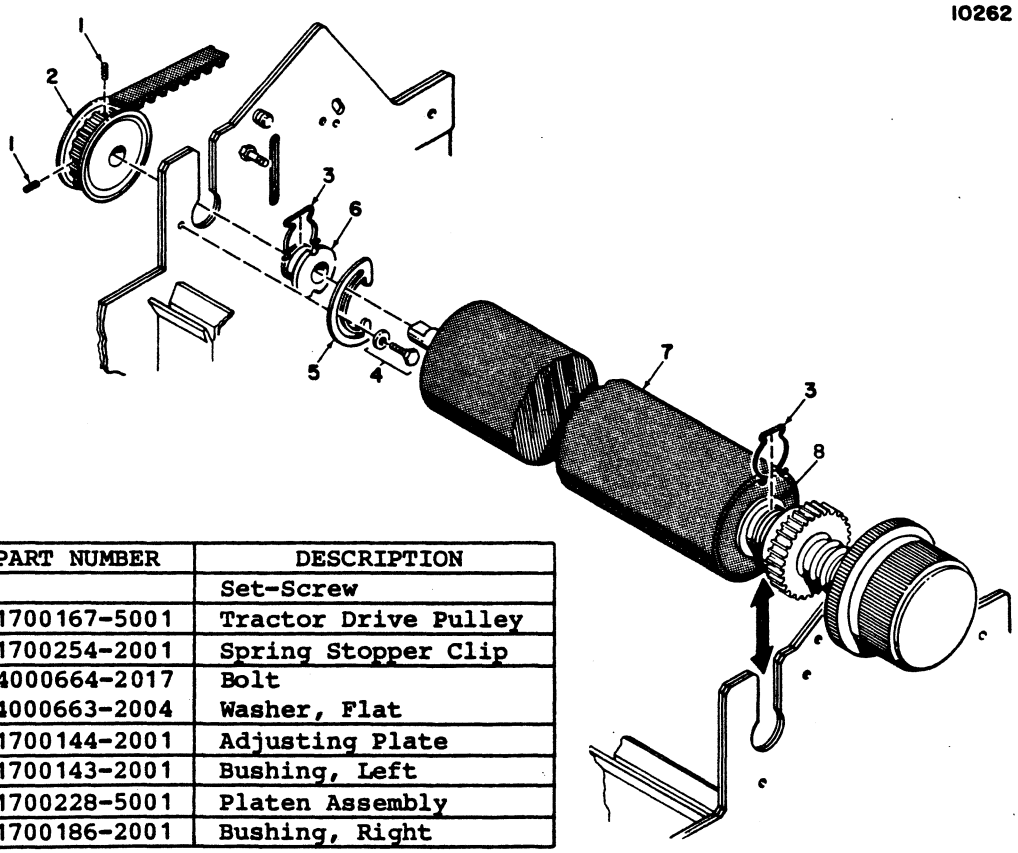
E. Remove two stop collar springs (3) from each end of platen.

F. Loosen bolt and lockwasher (4) mounting adjusting plate (5), and remove adjusting plate from left bushing (6) mounting slots.

G. Slide two brass bushings (6, 8) towards the center of printer, and lift platen assembly (7) from printer.

H. To install platen assembly, reverse steps A through G.

I. Refer to paragraph 5.3.2, Section 5, for adjustments on platen assembly.



ITEM	PART NUMBER	DESCRIPTION
1		Set-Screw
2	81700167-5001	Tractor Drive Pulley
3	81700254-2001	Spring Stopper Clip
4	34000664-2017 34000663-2004	Bolt Washer, Flat
5	81700144-2001	Adjusting Plate
6	81700143-2001	Bushing, Left
7	81700228-5001	Platen Assembly
8	81700186-2001	Bushing, Right

Figure 6-10. REMOVAL/REPLACEMENT, PLATEN ASSEMBLY

6.12 VERTICAL FORMAT UNIT (Figure 6-11)

TOOLS REQUIRED: Phillips Head Screwdriver

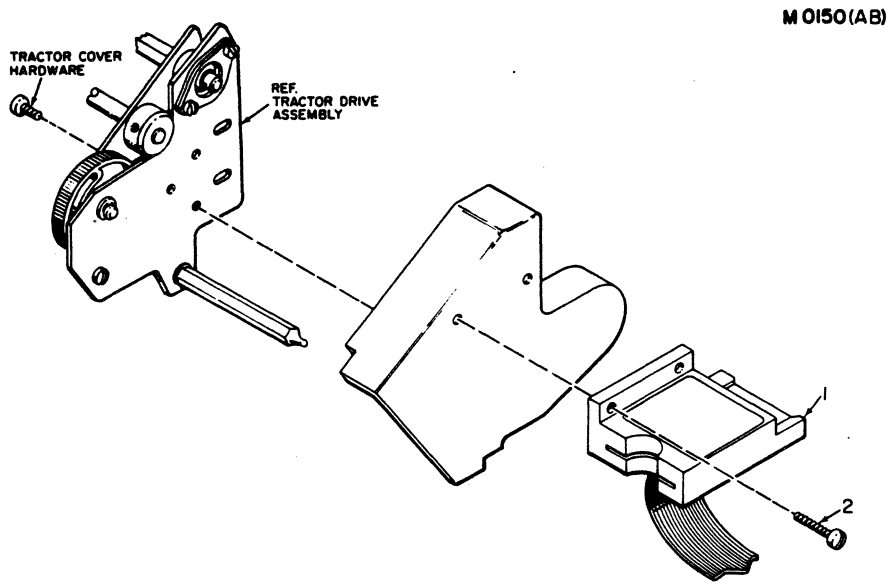
A. Remove electronic module cover from printer per paragraph 6.2.

B. Disconnect connector P012 of vertical format unit from connector J012.

C. Remove mounting screws (2), and remove vertical format unit (1) from printer.

D. Remove modified right tractor drive cover hardware, and remove spacer (3) and cover (4) from printer.

E. To install vertical format unit, reverse steps A through D.



ITEM	PART NUMBER	DESCRIPTION
1	63703172-4001	Tape Reader Assembly, 2 Channel
2	34000665-2002	Screw, M4 x 10 mm Lg, Pan Hd. Phillips, Self Tapping

Figure 6-11. REMOVAL/REPLACEMENT, VERTICAL FORMAT UNIT

6.13 TRACTOR DRIVE ASSEMBLY (Figure 6-12)
TOOLS REQUIRED: Phillips Head Screwdriver, M4 Open End Wrench

A. Remove left/right covers and left/right tractor drive cover per paragraph 6.2.

B. Disconnect two pin connector P044 of paper empty switch (1) from connector J044.

C. Remove left (2) and right (3) stud screws, four flatwashers (4) and nuts (5) attaching complete tractor drive assembly (7) to left and right side frames.

D. Remove two screws, lockwashers and flatwashers (6) mounting complete tractor drive assembly (7) to left and right side frames and remove tractor drive assembly.

E. To install the complete tractor drive assembly reverse steps.

F. Refer to paragraphs 5.3.3 and 5.3.4, Section 5, for adjustment procedures on tractor drive assembly.

6.14 PIN FEED TRACTORS, LEFT/RIGHT (Figure 6-12)
TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove left and right tractor drive covers per paragraph 6.2.

B. Disconnect P044 of paper empty switch (1) from connector J044.

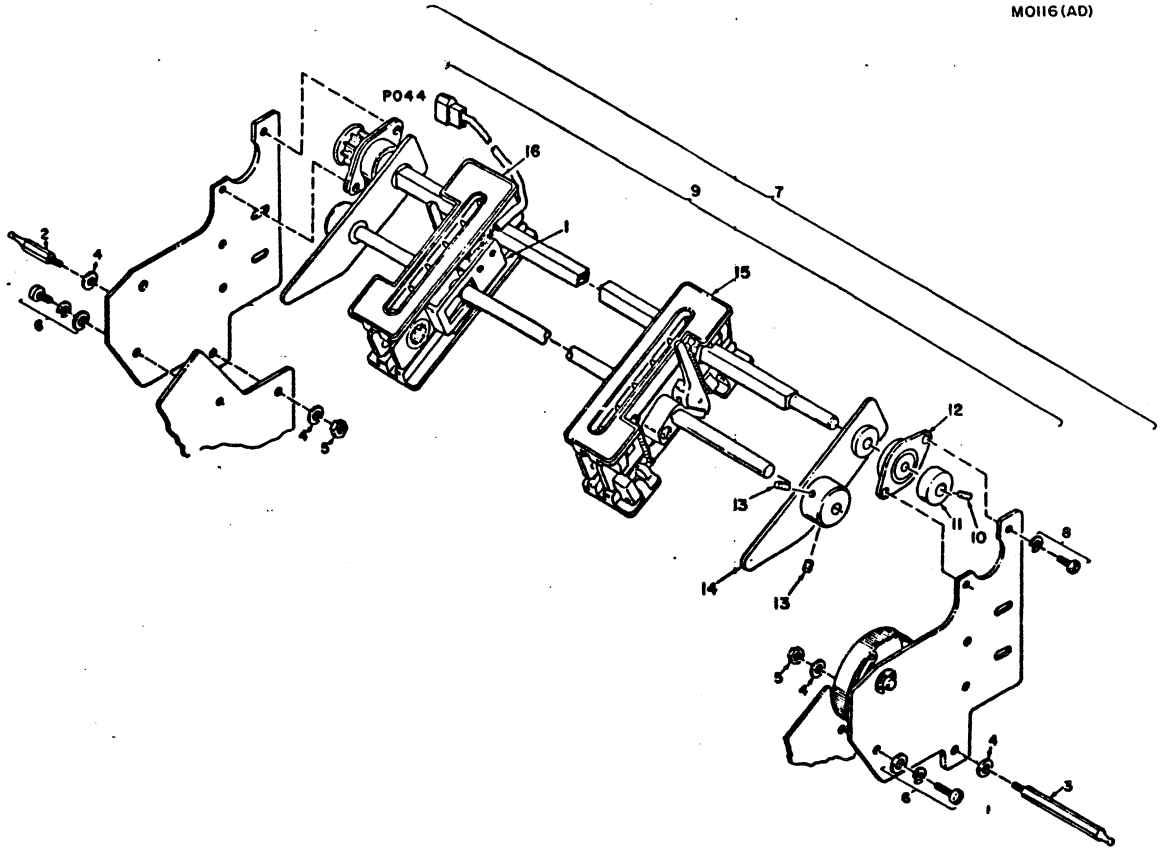
C. Remove four screws and lockwashers (8) monting sub tractor drive assembly (9) to left and right side frames and remove sub tractor drive assembly from printer.

D. On right side of sub tractor driver assembly loosen set-screw (10) mounting collar (11) and bushing (12) and remove collar and bushing.

E. Loosen set-screw (13) mounting right support plate (14) and remove right support plate (14).

F. Slide the right (15) and left (16) pin feed tractors off the drive shaft and support bar of the sub tractor drive assembly.

G. To install pin feed tractors, reverse steps A through F.



ITEM	PART NUMBER	DESCRIPTION
1	81700606-6001	Paper Empty Switch
2	81700044-2001	Stud Screw (Cover L-Rear)
3	81700044-2002	Stud Screw (Cover R-Rear)
4	34000663-2006	Washer, Flat, M4
5	34000661-2006	Nut, Hex, M4
6	34000351-2038 34000455-2006 34000452-2006	Screw, M4 x 10 mm Lg., Pan Hd Phillips Washer, Split Lock, M4 Washer, Flat, M4
7	81700243-5001	Tractor Drive Assembly
8	34000664-2037 34000662-2006	Screw, M4 x 6 mm Lg, Pan Hd. Phillips Washer, Split Lock, M4
9	-	Sub Tractor Drive Assembly
10	34000656-2013	Set-Screw M3 x 3 mm Lg
11	81700303-2001	Bushing
12	34000656-2031	Set-Screw
13	81700155-2001	Collar
14	81700053-2001	Right Support Plate
15	81700247-5001	Pin Feed Tractor, Right
16	81700249-5001	Pin Feed Tractor, Left

Figure 6-12. REMOVAL/REPLACEMENT, TRACTOR DRIVE ASSEMBLY PIN FEED TRACTORS, LEFT/RIGHT

6.15 PRIMARY VOLTAGE ASSEMBLY (Figure 6-13)

TOOLS REQUIRED: Phillips and Slotted Head Screwdriver

A. Remove electronic module cover from printer per paragraph 6.2.

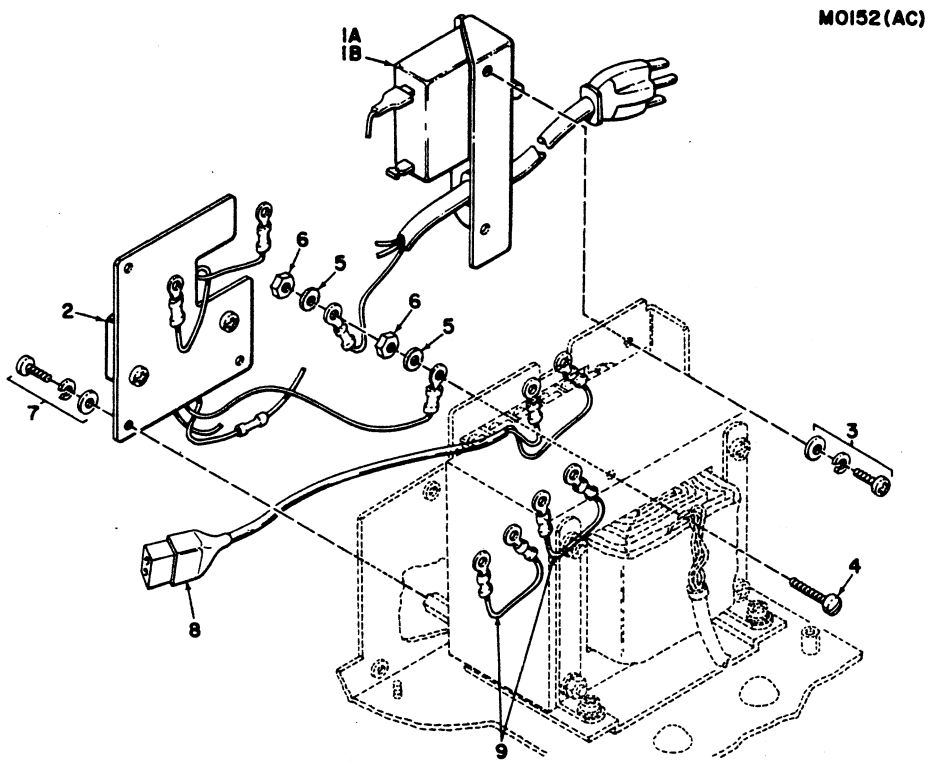
B. Disconnect all wires from the power bracket assembly (1A, 1B), and line filter assembly (2).

C. Remove two screws, lockwashers and flatwashers (3) mounting power bracket assembly.

D. Remove screw (4), two external tooth lockwashers (5) and nuts (6) connecting ground wire of AC power cord, and remove power bracket assembly.

E. Remove three mounting screws, lockwashers and flatwashers (7), and remove line filter assembly (2).

F. To install items of primary voltage assembly, reverse steps A through E.



ITEM	PART NUMBER	DESCRIPTION
1A	63703115-5001	Power Bracket Assembly, 115 VAC
1B	63703115-5002	Power Bracket Assembly, 230 VAC
2	63703144-5001	Line Filter Assembly
3	34000351-2038	Screw, M4 x 10 mm Lg., Pan Hd Phillips
	34000455-2006	Washer, Split Lock, M4
	34000452-2006	Washer, Flat, M4
4	34000351-2040	Screw, M4 x 16 mm Lg., Pan Hd Phillips
5	34000451-2056	Washer, Split Lock, External Tooth, M4
6	34000652-2006	Nut, Hex, M4
7	34000351-2037	Screw, M4 x 8 mm Lg., Pan Hd Phillips
	34000455-2006	Washer, Split Lock, M4
	34000452-2006	Washer, Flat, M4
8	63761184-4001	Cable Assembly, Adapter
9	63779114-4001	Jumper Wires, Transformer

Figure 6-13. REMOVAL/REPLACEMENT, PRIMARY VOLTAGE ASSEMBLY

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6.16 CAPACITOR/DIODE BRIDGE ASSEMBLY (Figure 6-14)

TOOLS REQUIRED: Slotted Head Screwdriver, M3 Nut Driver

A. Remove electronic module cover per paragraph 6.2.

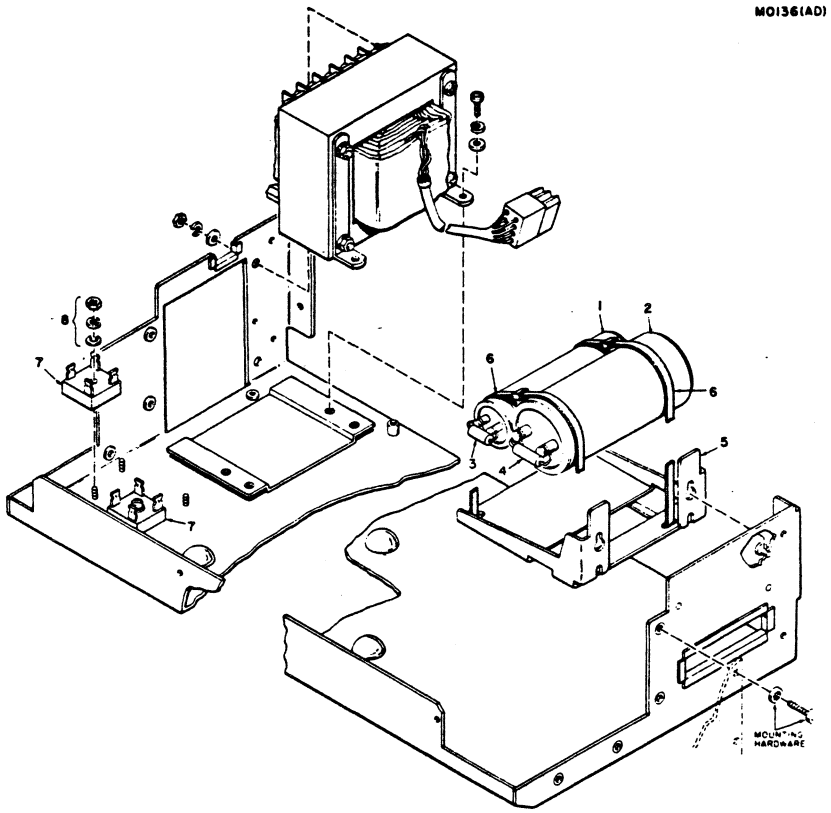
B. Remove the four screws connecting the four wires to the leads of the capacitor assemblies (1, 2).

C. Cut the two cable straps (6) mounting the capacitor assemblies to support bracket (5), and remove capacitor assemblies.

D. Remove the eight faston connectors from the two diode bridges (7).

E. Remove the two mounting nuts, lockwashers and flatwashers (8), and remove diode bridges from printer.

F. To install capacitor/diode assemblies, reverse steps A through E and add new cable straps around capacitors.



ITEM	PART NUMBER	DESCRIPTION
1	22938000-1001	Capacitor, 9300 uf, 50V, -10% +100%
2	22259001-1001	Capacitor, 25,000 uf, 50V, -10% +75%
3	63010138-5001	Resistor, Assembly, 470 Ohm
4	63010138-5002	Resistor, Assembly, 82 Ohm
5	63703155-2002	Capacitor Support Bracket
6	39690010-2011	Cable Strap
7	38125021-1002	Rectifier Bridge
8	34000652-2004	Nut, Hex, M3
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3

Figure 6-14. REMOVAL/REPLACEMENT, CAPACITOR/DIODE BRIDGE ASSEMBLY

6.17 FAN ASSEMBLY (Figure 6-15)

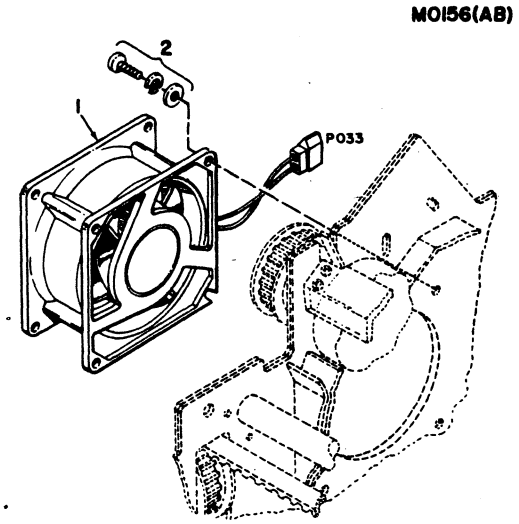
TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove electronic module cover from printer paragraph 6.2.

B. Disconnect two pin connectors P033 of fan assembly (1) from connector J033.

C. Remove the four mounting screws, lockwashers and flatwashers (2), and remove fan assembly from printer.

D. To install fan assembly, reverse steps A through C.



ITEM	PART NUMBER	DESCRIPTION
1	63703160-4001	Fan Assembly
2	34000355-2010	Screw, M3 x 10 mm Lg., Socket Head
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3

Figure 6-15. REMOVAL/REPLACEMENT, FAN ASSEMBLY

6.18 LOGIC BOARD ASSEMBLY (Figure 6-16)

TOOLS REQUIRED: Phillips and Slotted Head Screwdrivers

A. Remove electronic module cover from printer paragraph 6.2.

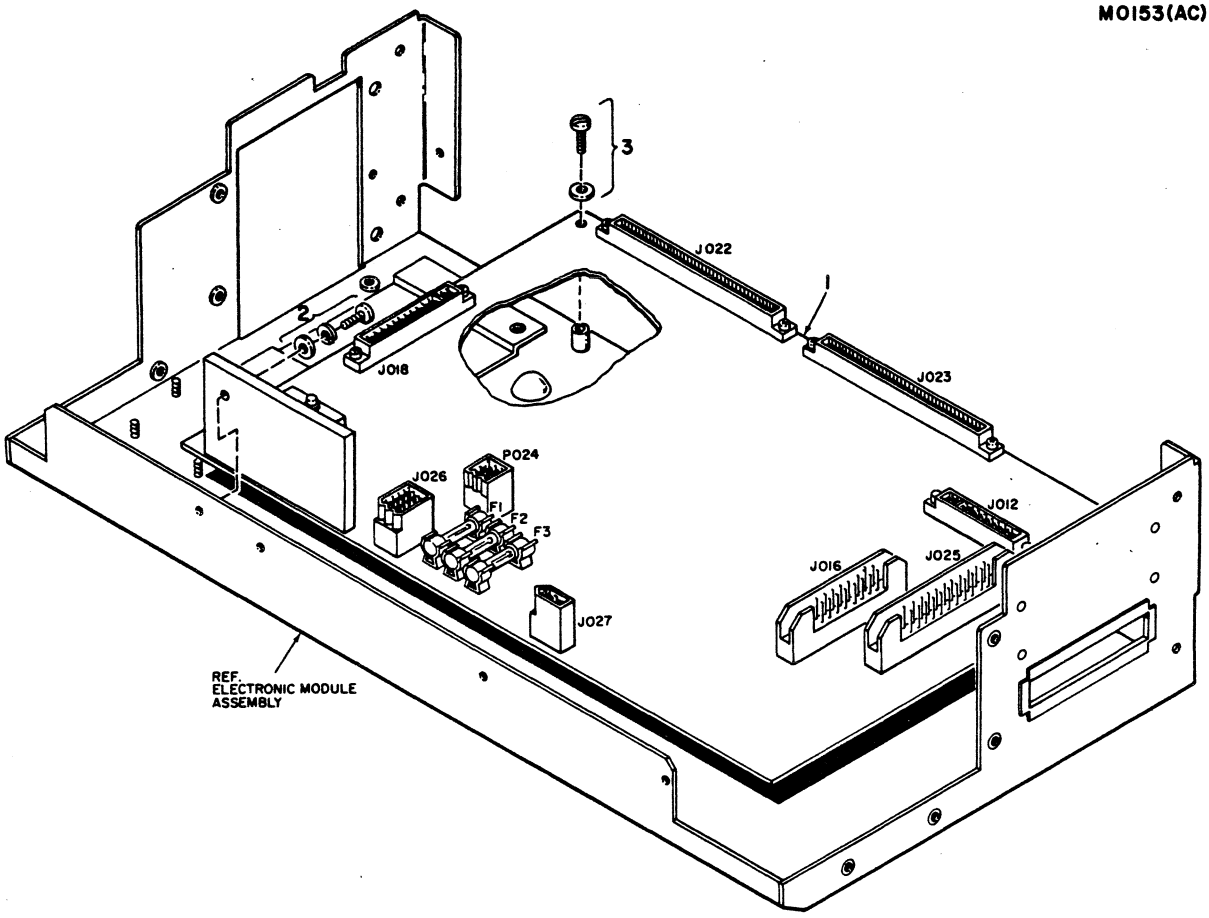
B. Disconnect all connectors and wires from logic board (1).

C. Remove screw, lockwasher and flatwasher (2) mounting front of logic board to electronic module frame.

D. Remove two screws, and flatwashers (3) mounting rear of logic board to module frame and remove board.

E. To install logic board assembly, reverse steps A through D.

F. Refer to paragraph 5.4.2, Section 5, for adjustment procedures on the logic board assembly.



ITEM	PART NUMBER	DESCRIPTION
1A	63703216-4002	Logic Board Assembly, RS232
1B	63703216-4280	Logic Board Assembly, RS232 Expanded Buffer
2	34000351-2020	Screw, M3 x 12 mm Lg., Pan Hd Phillips
	34000455-2004	Washer, Split Lock, M3
	34000452-2004	Washer, Flat, M3
3	33724117-2010	Screw, #6 x .312 Lg. Pan Hd. Phillips,
	34922084-2001	Washer, Flat, #6, Nylon

Figure 6-16. REMOVAL/REPLACEMENT, LOGIC BOARD ASSEMBLY

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6.19 CONTROL PANEL ASSEMBLY (Figure 6-17)

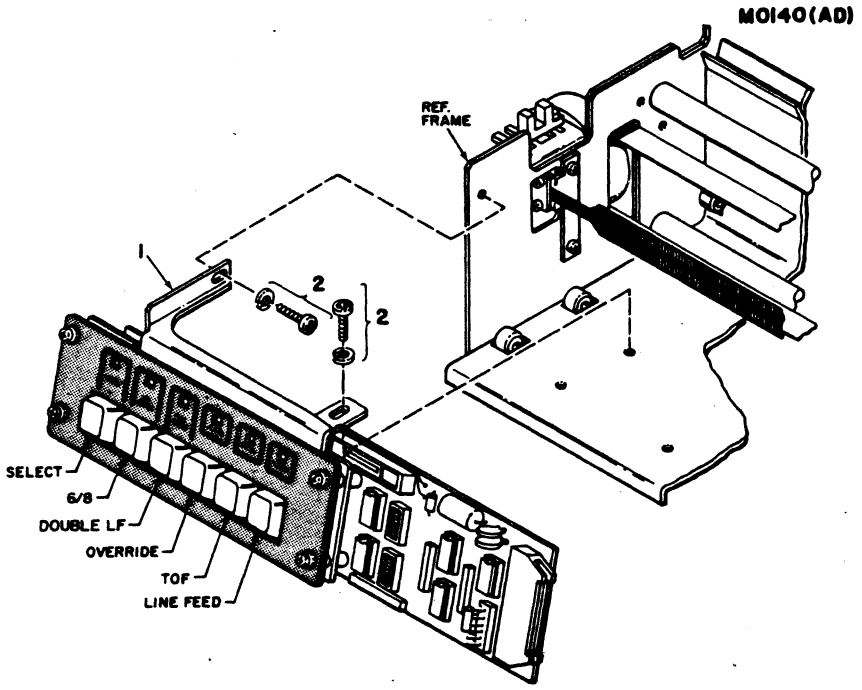
TOOLS REQUIRED: Phillips Head Screwdriver

A. Remove top and front covers from printer.

B. Remove connectors J038 and P021 from connectors P038 and J021 on the control panel assembly (1).

C. Remove three screws, lockwashers and flatwashers (2) mounting control panel (1) to printer base and left frame; and remove control panel (1) from printer.

D. To install the control panel assembly, reverse steps A through C.



ITEM	PART NUMBER	DESCRIPTION
1	63761114-4003	P.C. Board Assembly, Control Panel
2	34000657-2025	Screw, M5 x 10 mm Lg., Hex Hd Socket
	34000451-2057	Washer, Split Lock, Ext Tooth, M5

Figure 6-17. REMOVAL/REPLACEMENT, CONTROL PANEL ASSEMBLY

SECTION 7
ELECTRICAL DRAWINGS

The following pages contain functional, schematic, wiring and assembly diagrams for the printer. A list of the drawings follows:

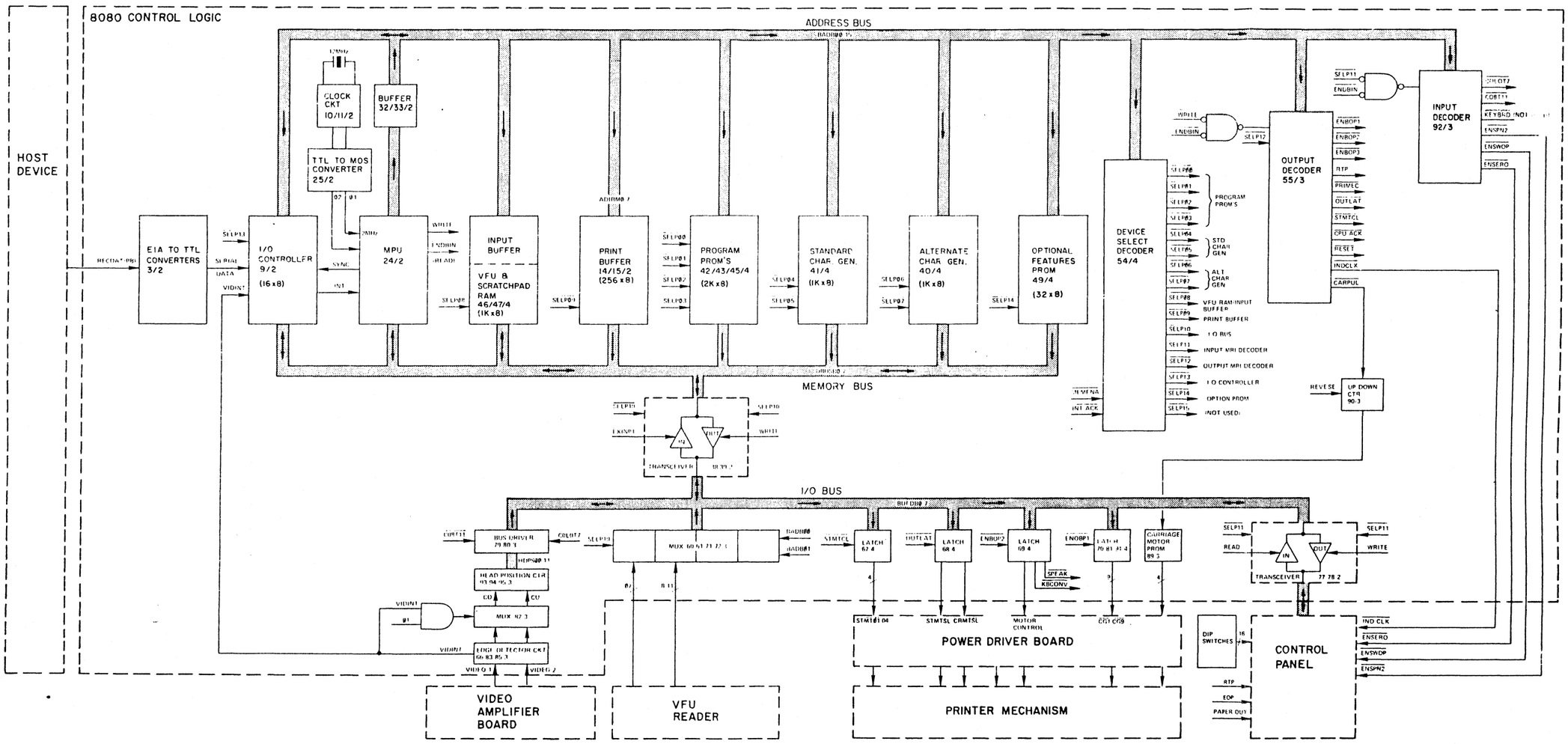


Figure 7-1. DATA/IO/ADDRESS BUS FUNCTIONAL SCHEMATIC

(19)

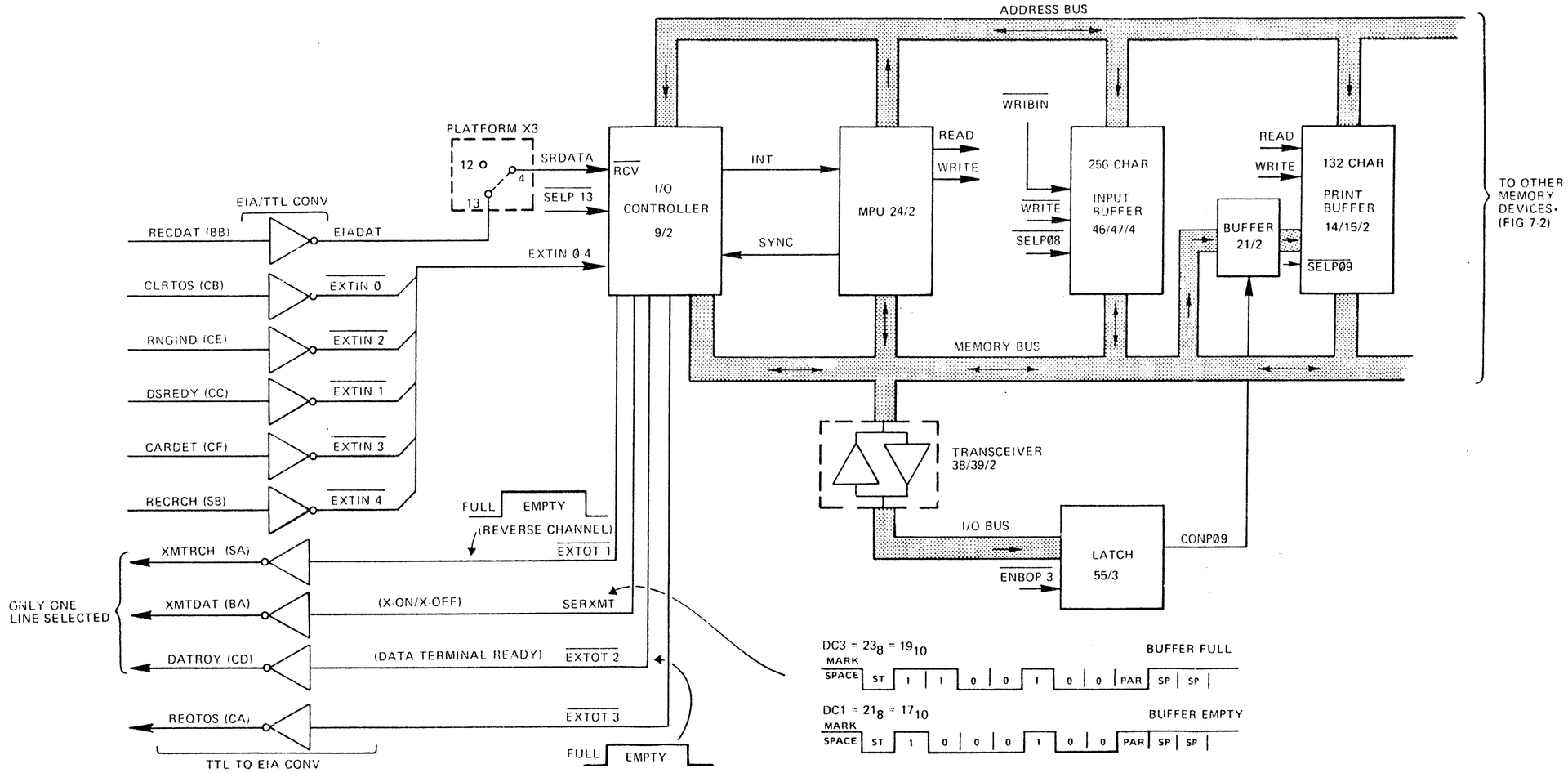


Figure 7-2. INPUT DATA FUNCTIONAL SCHEMATIC

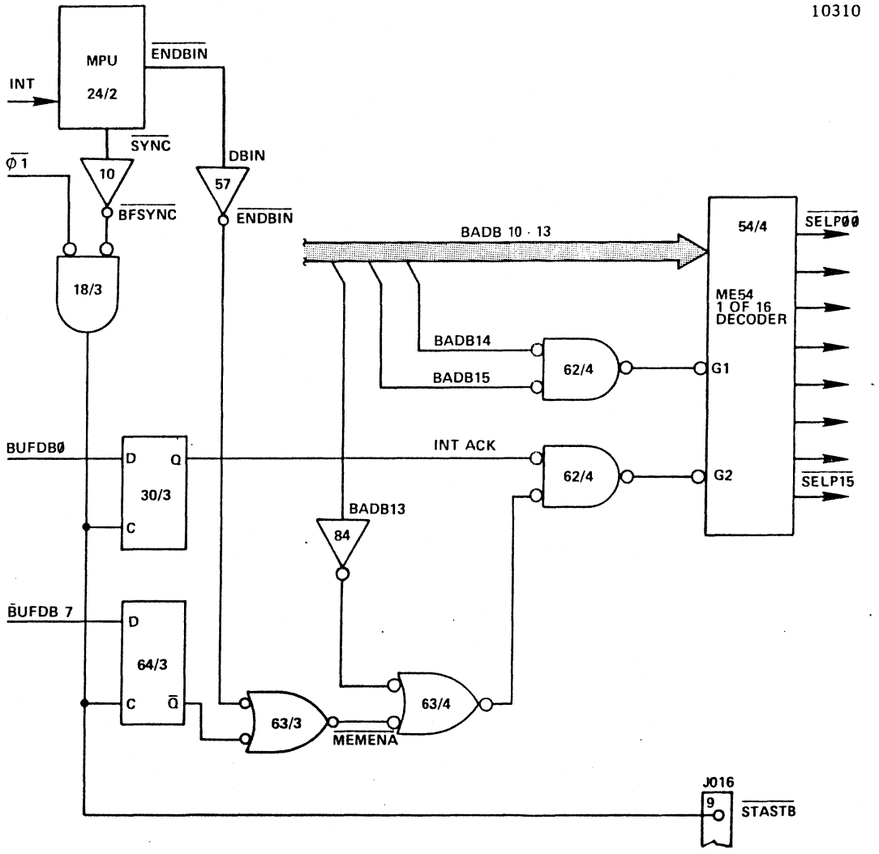


Figure 7-3. DEVICE SELECT FUNCTIONAL SCHEMATIC

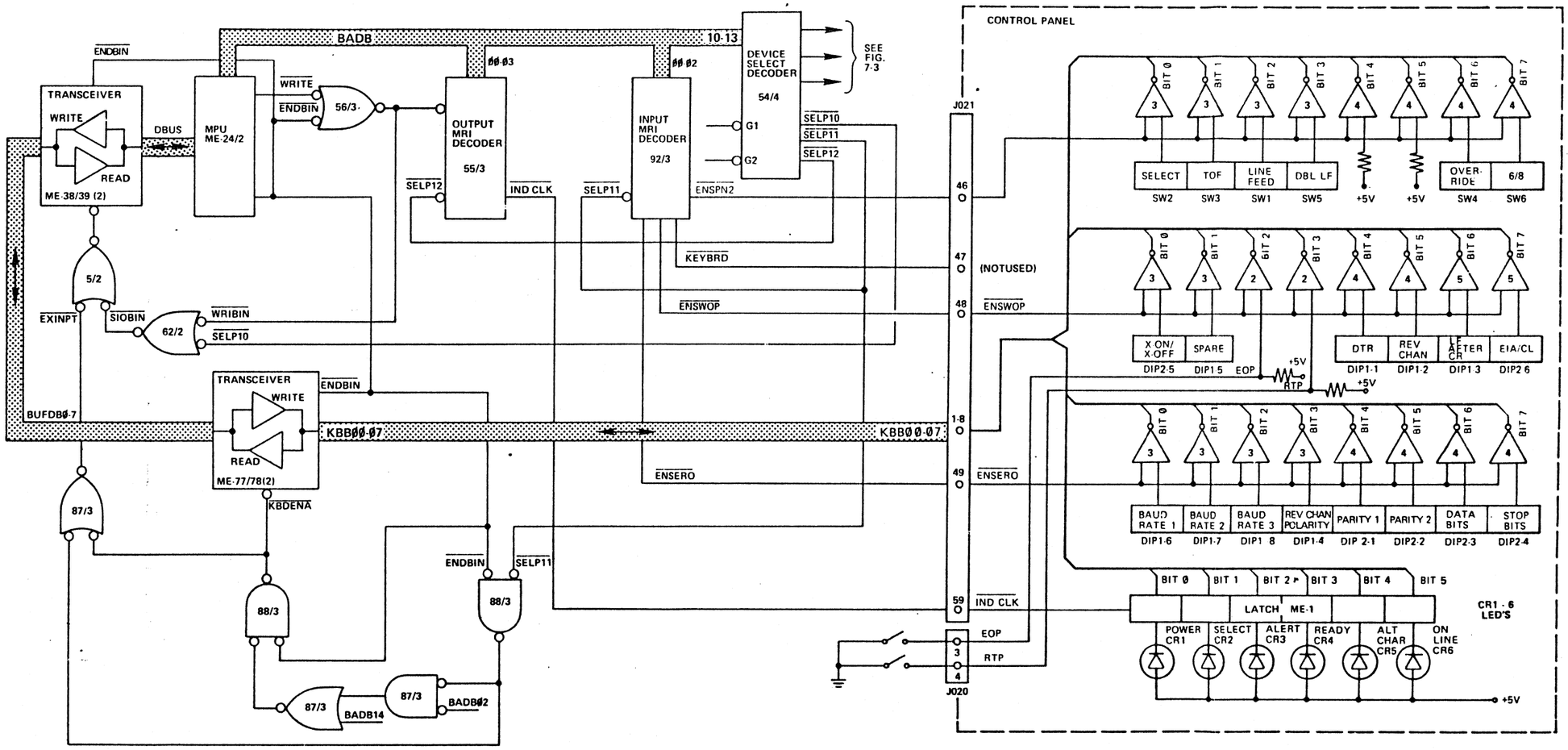


Figure 7-4. CONTROL PANEL/MPU FUNCTIONAL SCHEMATIC

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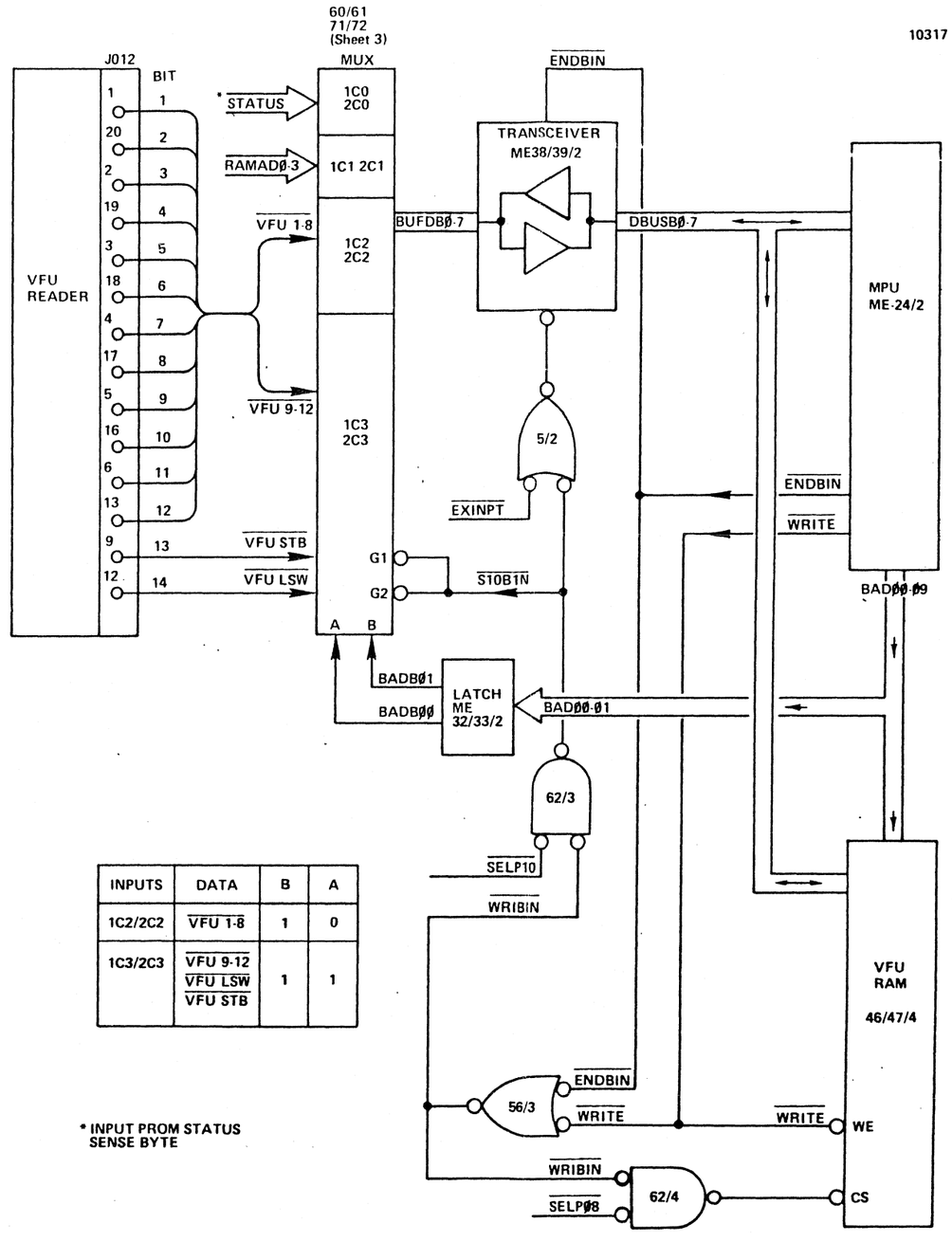

INPUTS	DATA	B	A
1C2/2C2	$\overline{\text{VFU 1-8}}$	1	0
1C3/2C3	$\overline{\text{VFU 9-12}}$ $\overline{\text{VFU LSW}}$ $\overline{\text{VFU STB}}$	1	1

* INPUT FROM STATUS SENSE BYTE

Figure 7-5. VFU READER/MPU FUNCTIONAL SCHEMATIC

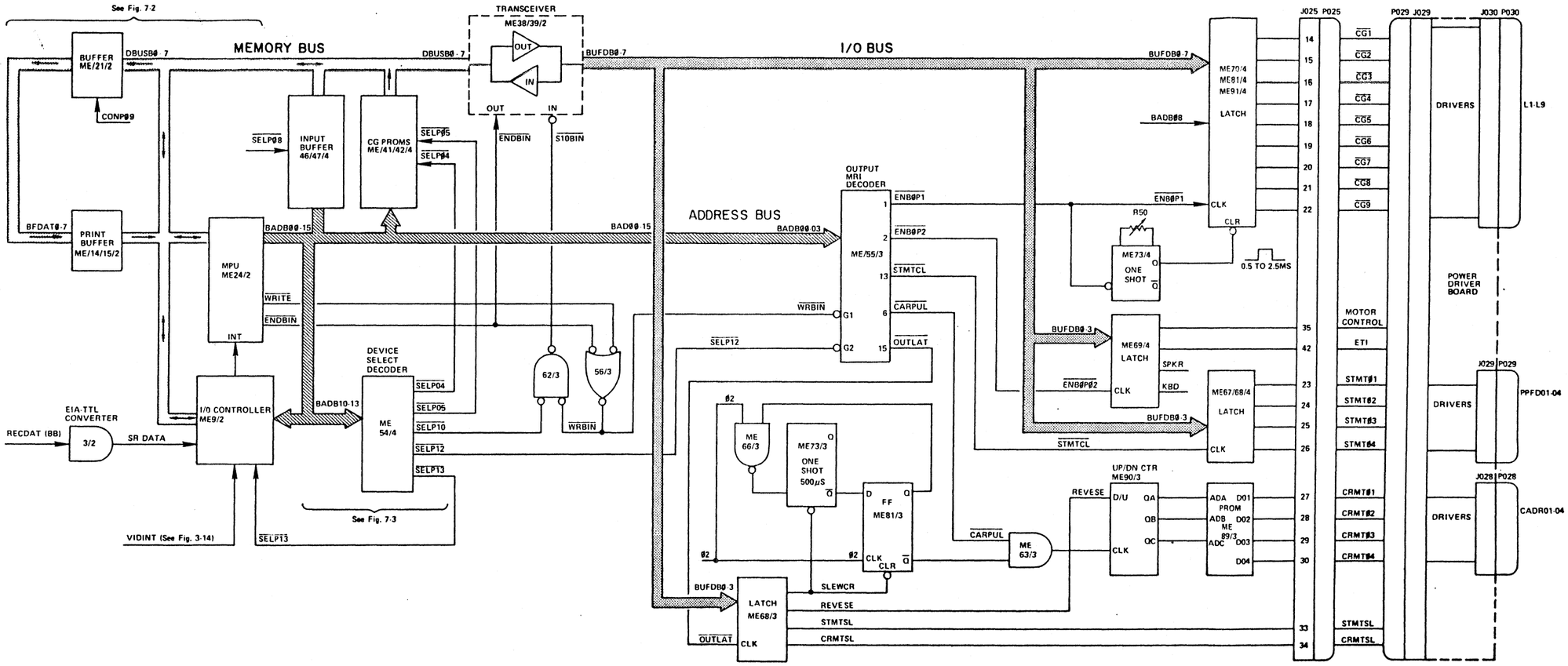

Figure 7-6. CG/STM/CRM/MPU FUNCTIONAL SCHEMATIC

7-13/7-14

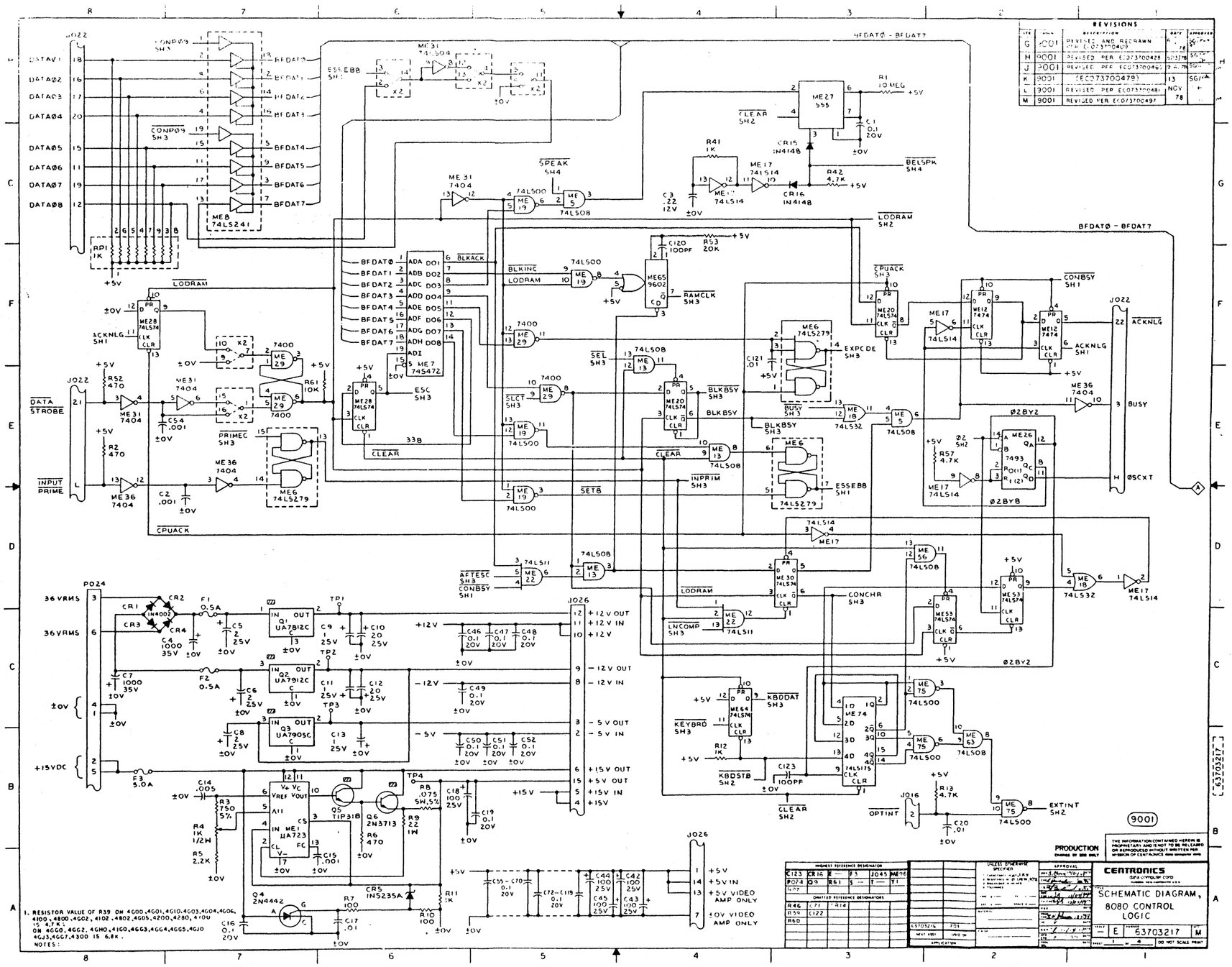

Figure 7-7. LOGIC BOARD SCHEMATIC DIAGRAM (Sheet 1 of 4)

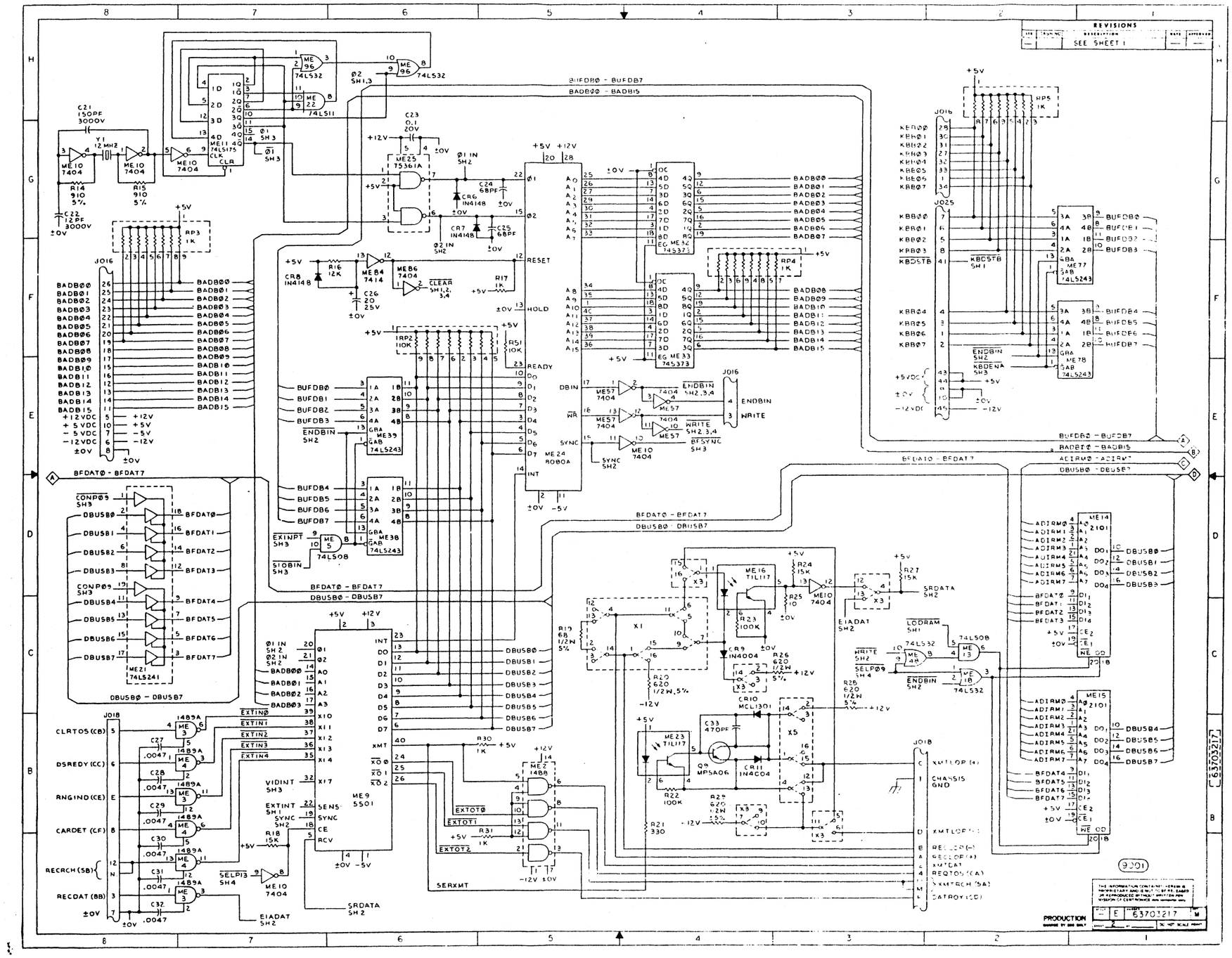

Figure 7-7. LOGIC BOARD SCHEMATIC DIAGRAM (Sheet 2 of 4)

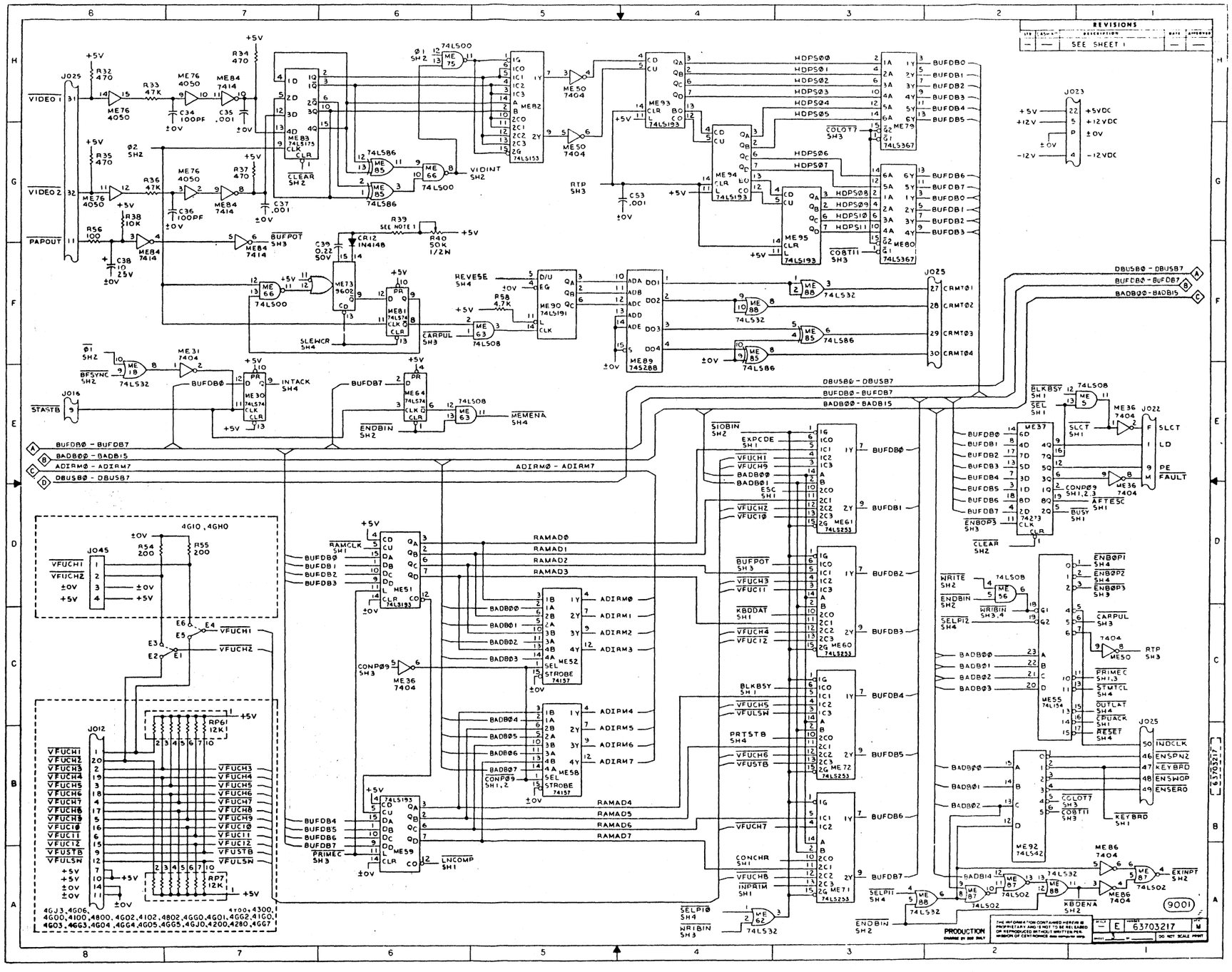

Figure 7-7. LOGIC BOARD SCHEMATIC DIAGRAM (Sheet 3 of 4)

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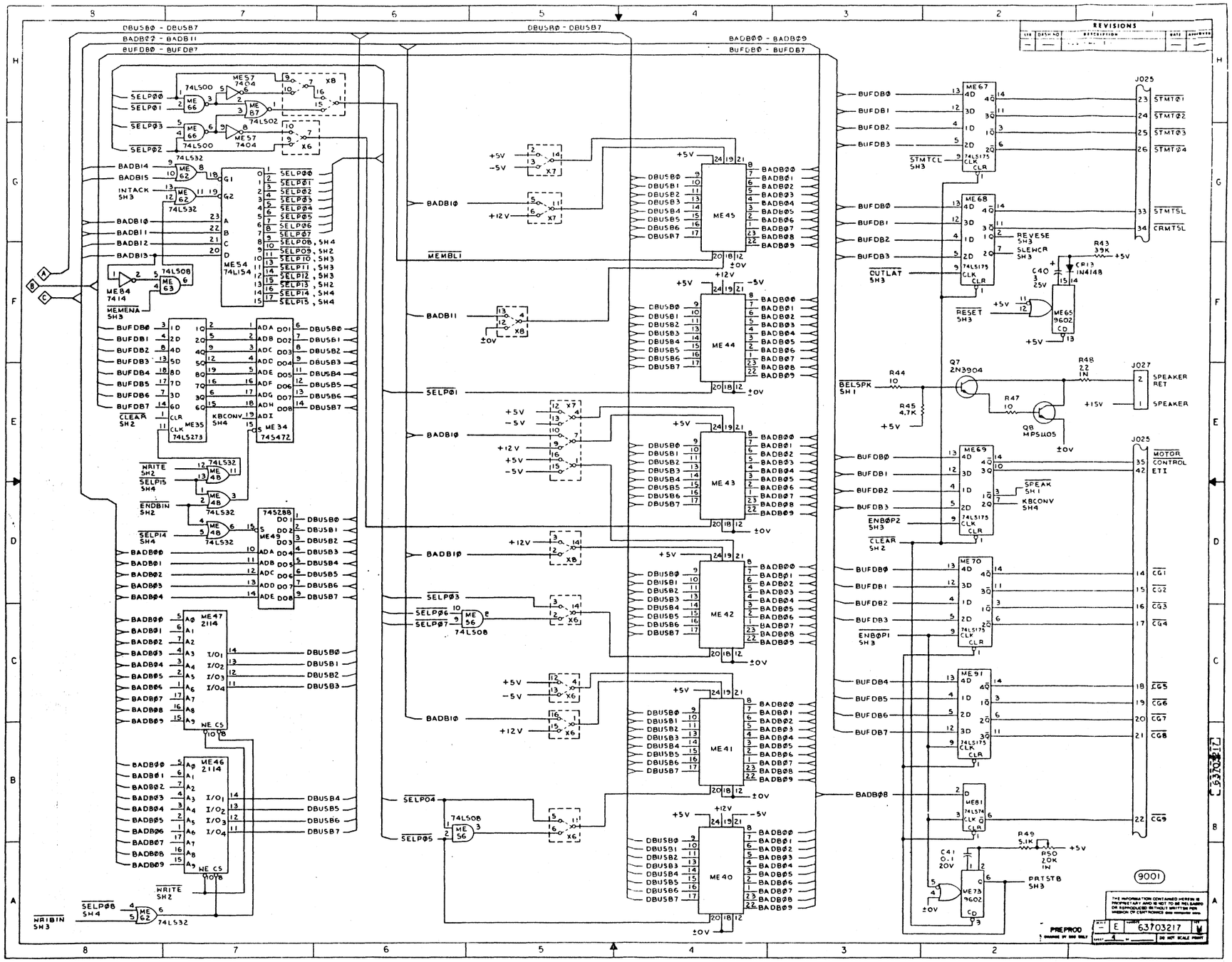

Figure 7-7. LOGIC BOARD SCHEMATIC DIAGRAM (Sheet 4 of 4)

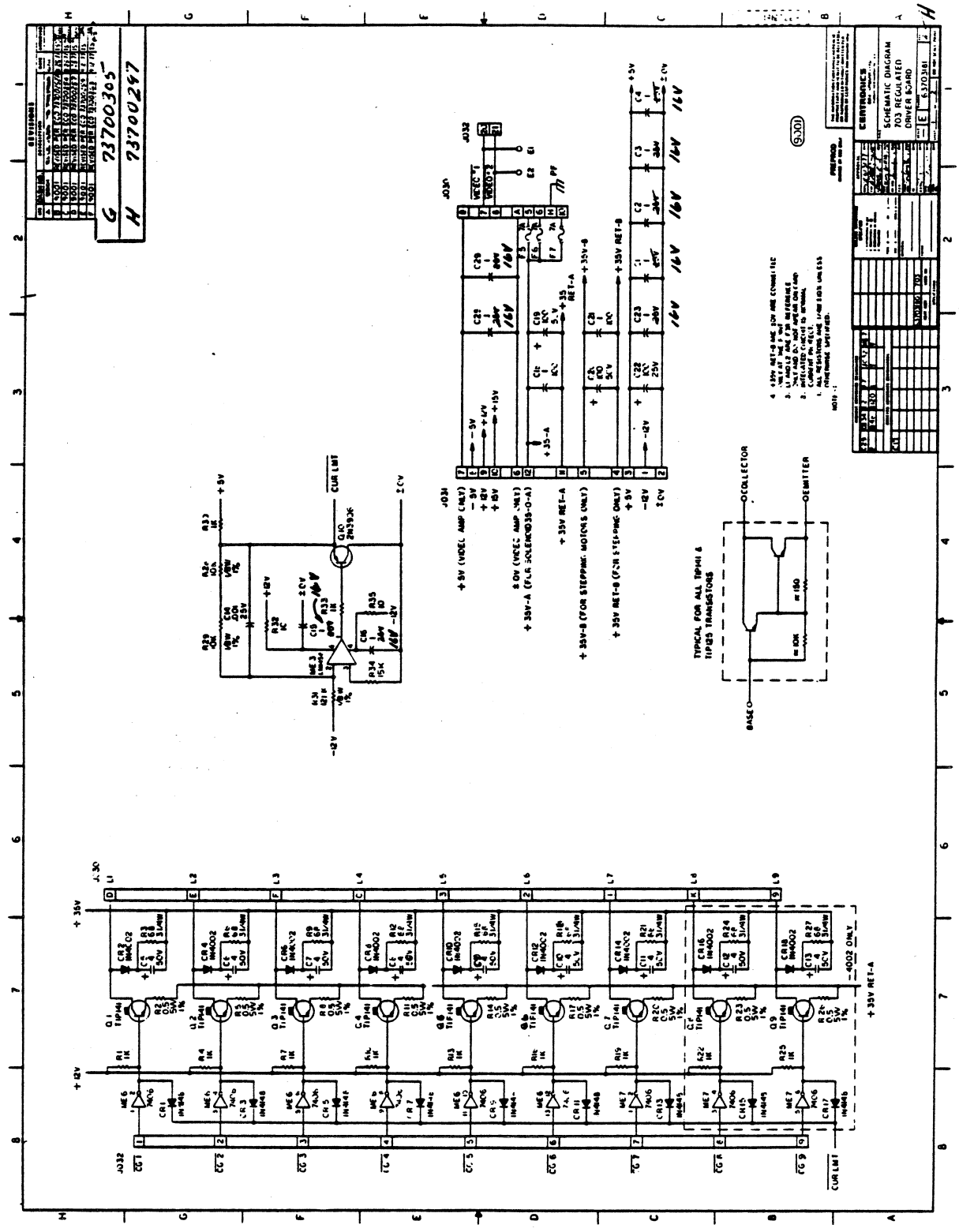

Figure 7-8. POWER DRIVER BOARD SCHEMATIC DIAGRAM (Sheet 1 of 2)

135

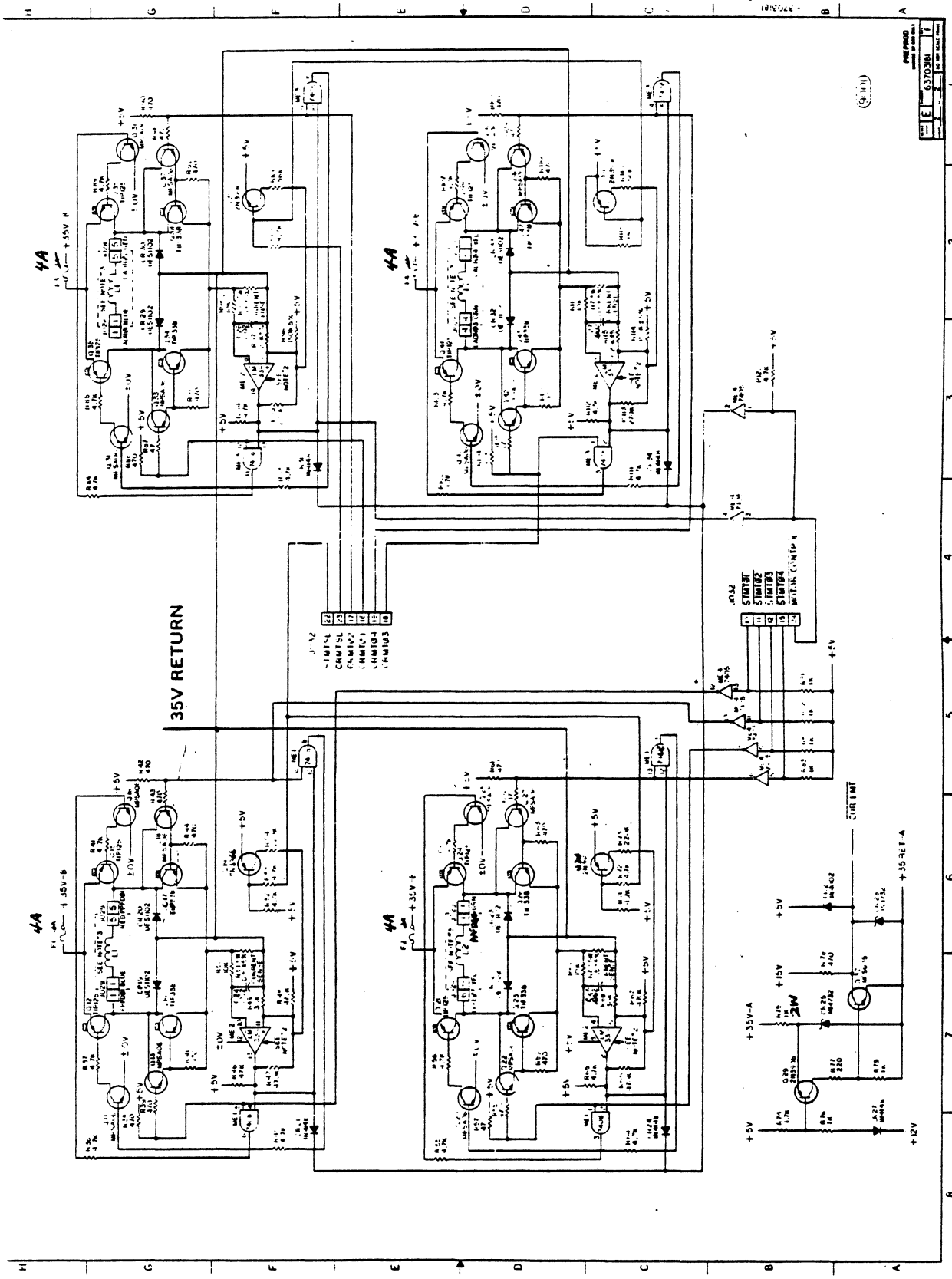

Figure 7-8. POWER DRIVER BOARD SCHEMATIC DIAGRAM (Sheet 2 of 2)

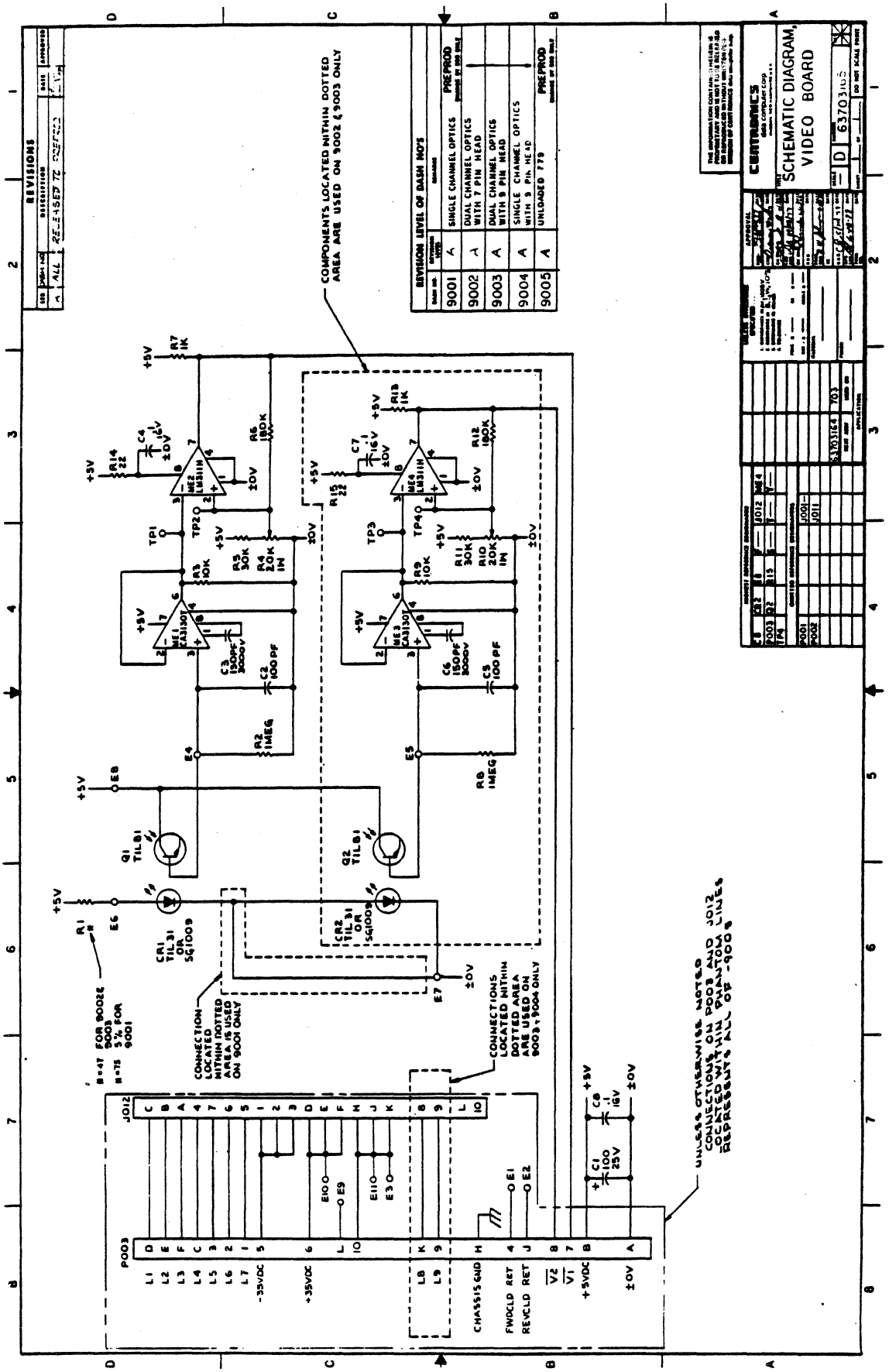

Figure 7-9. VIDEO AMPLIFIER BOARD SCHEMATIC DIAGRAM

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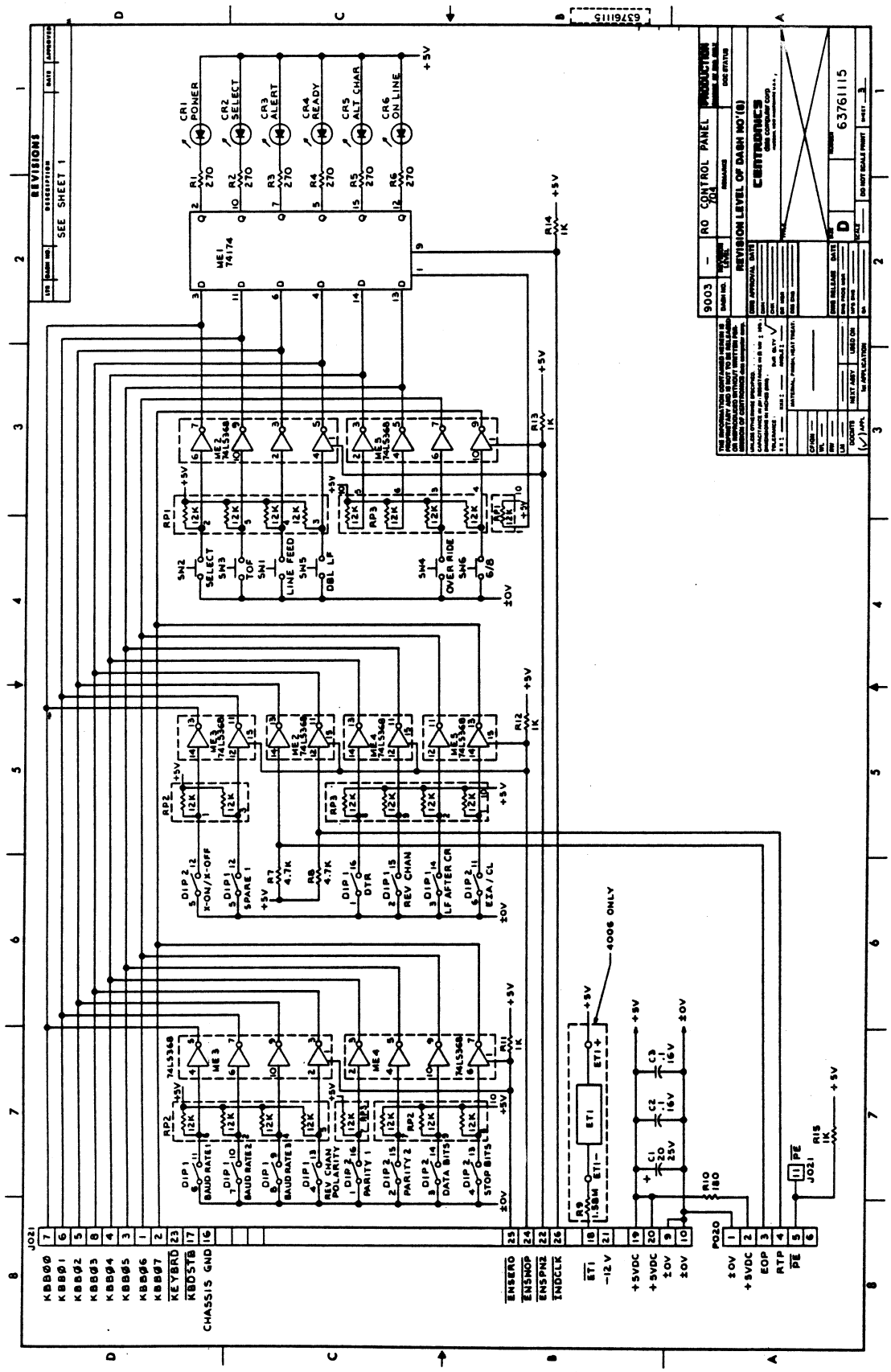

Figure 7-10. CONTROL PANEL BOARD SCHEMATIC DIAGRAM

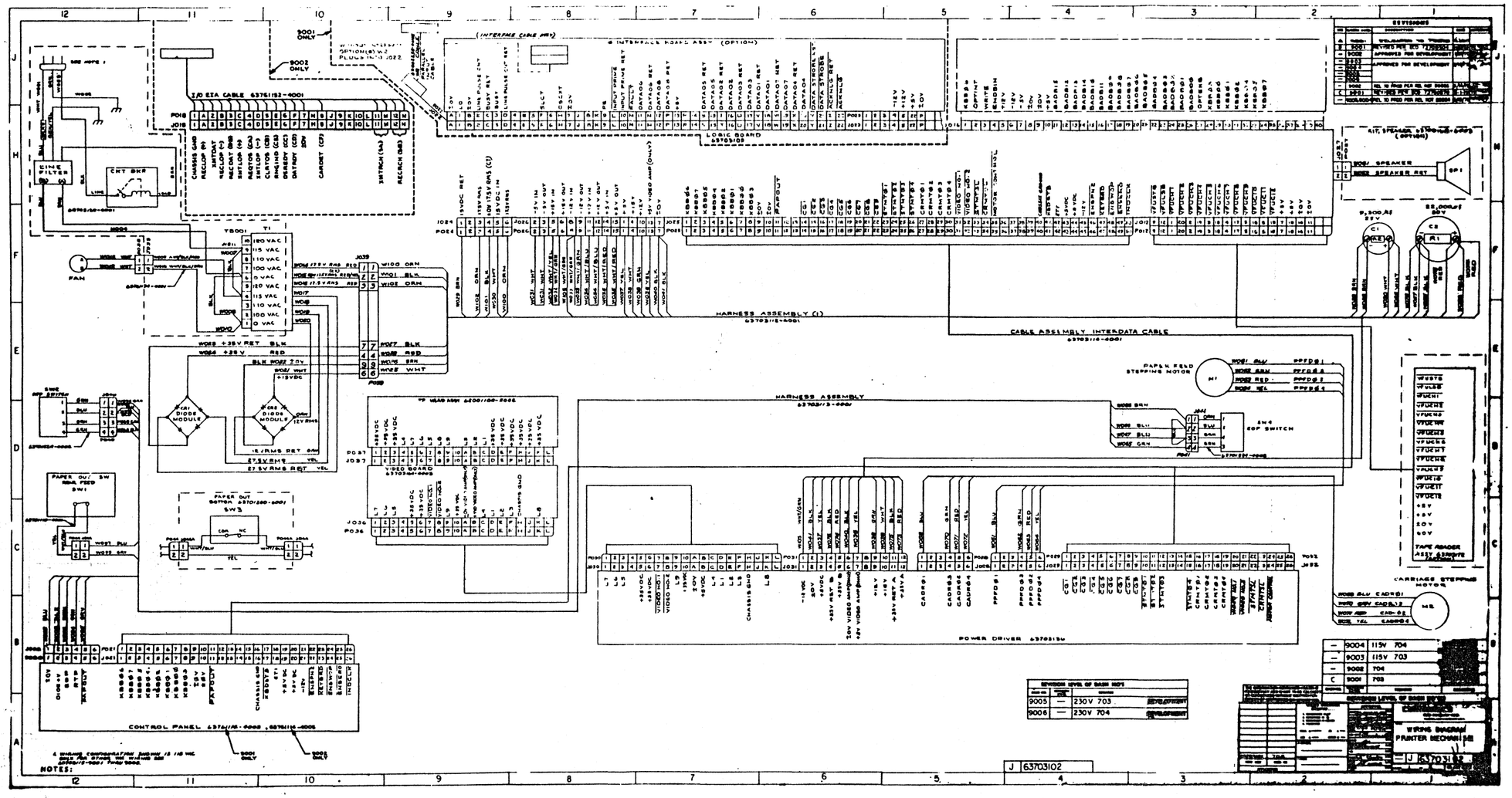

Figure 7-11. INTERCONNECTING WIRING DIAGRAM

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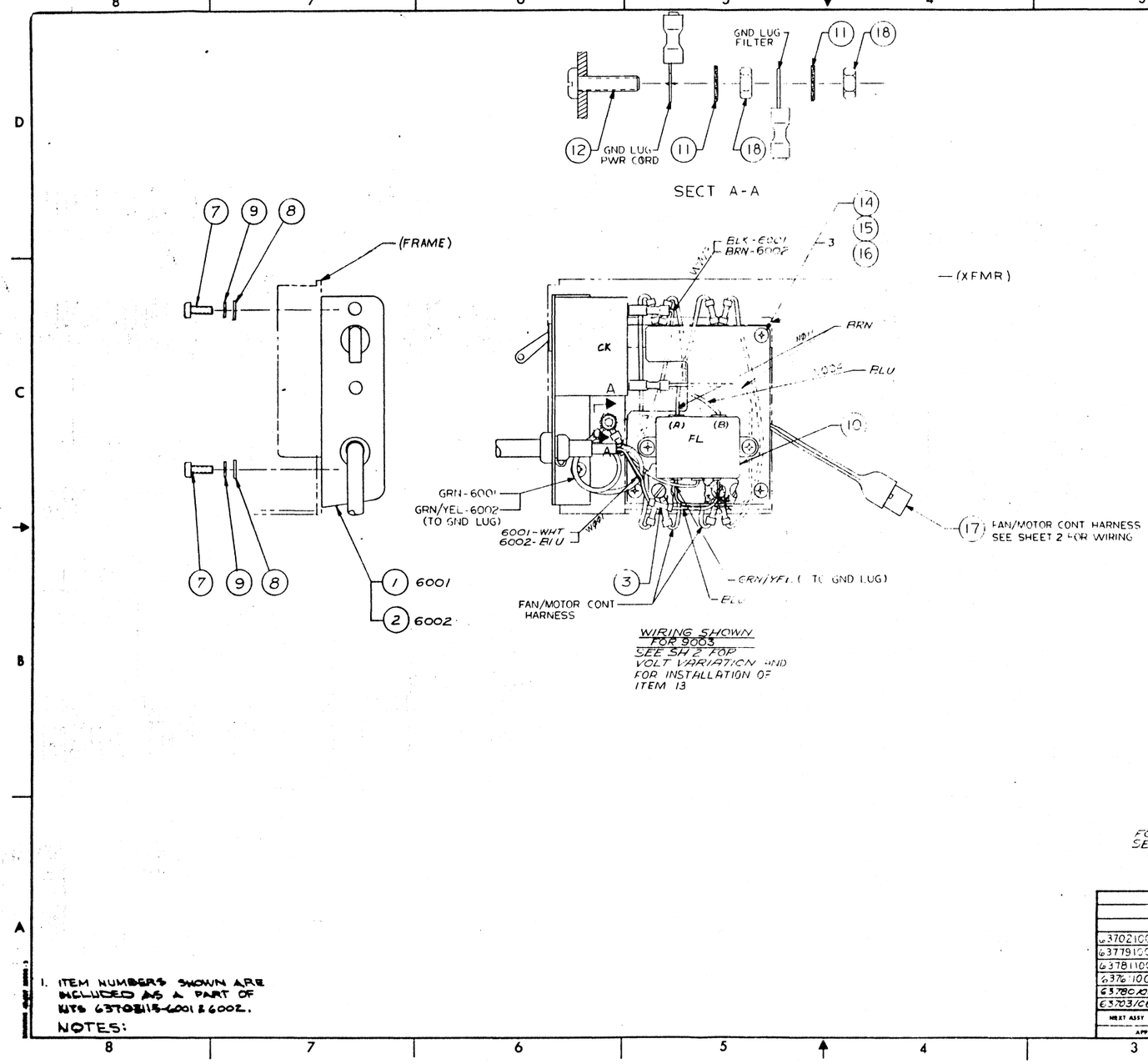

Figure 7-12. PRIMARY VOLTAGE WIRING DIAGRAM (Sheet 1 of 2)

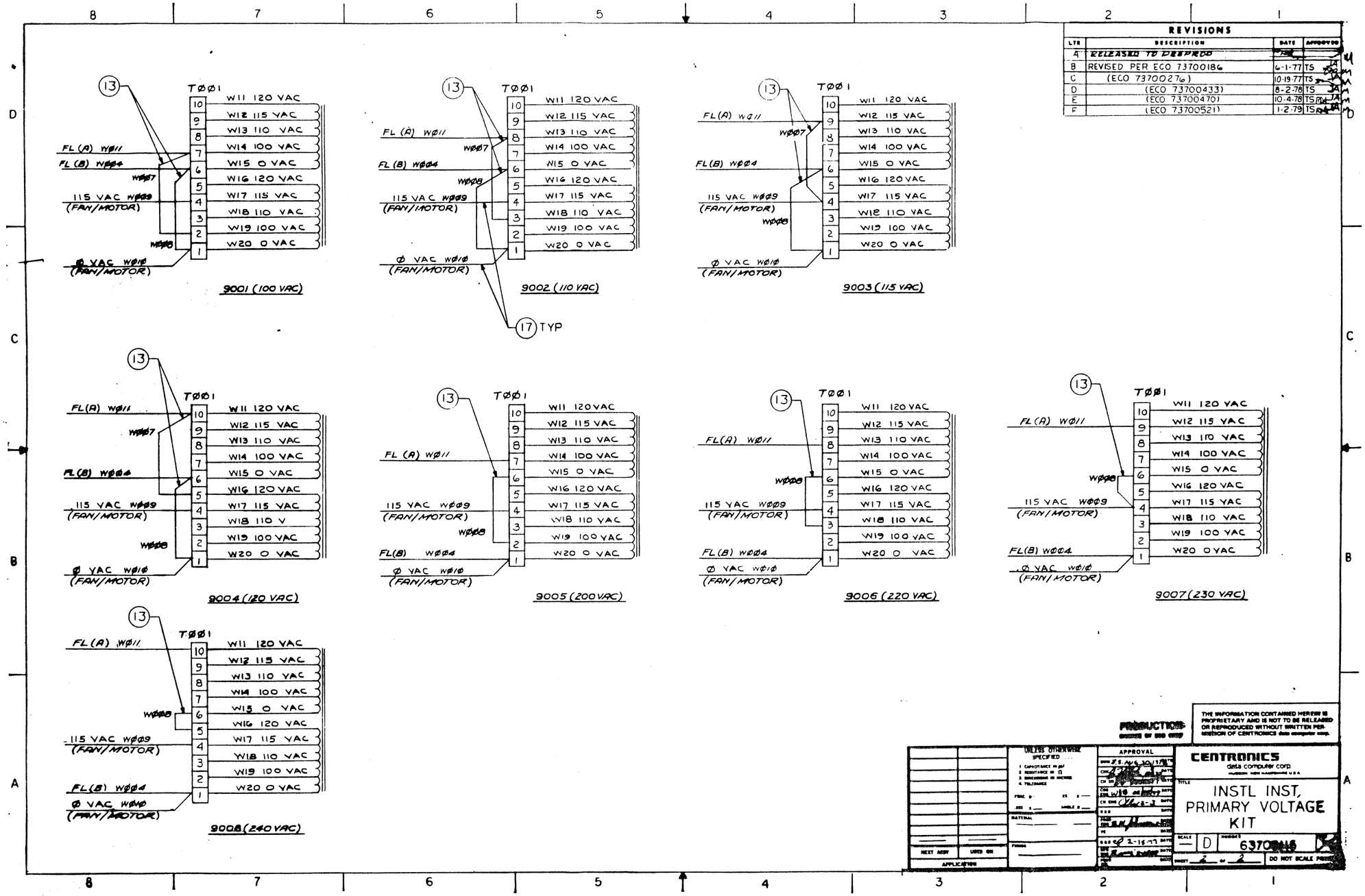

Figure 7-12. PRIMARY VOLTAGE WIRING DIAGRAM
(Sheet 2 of 2)

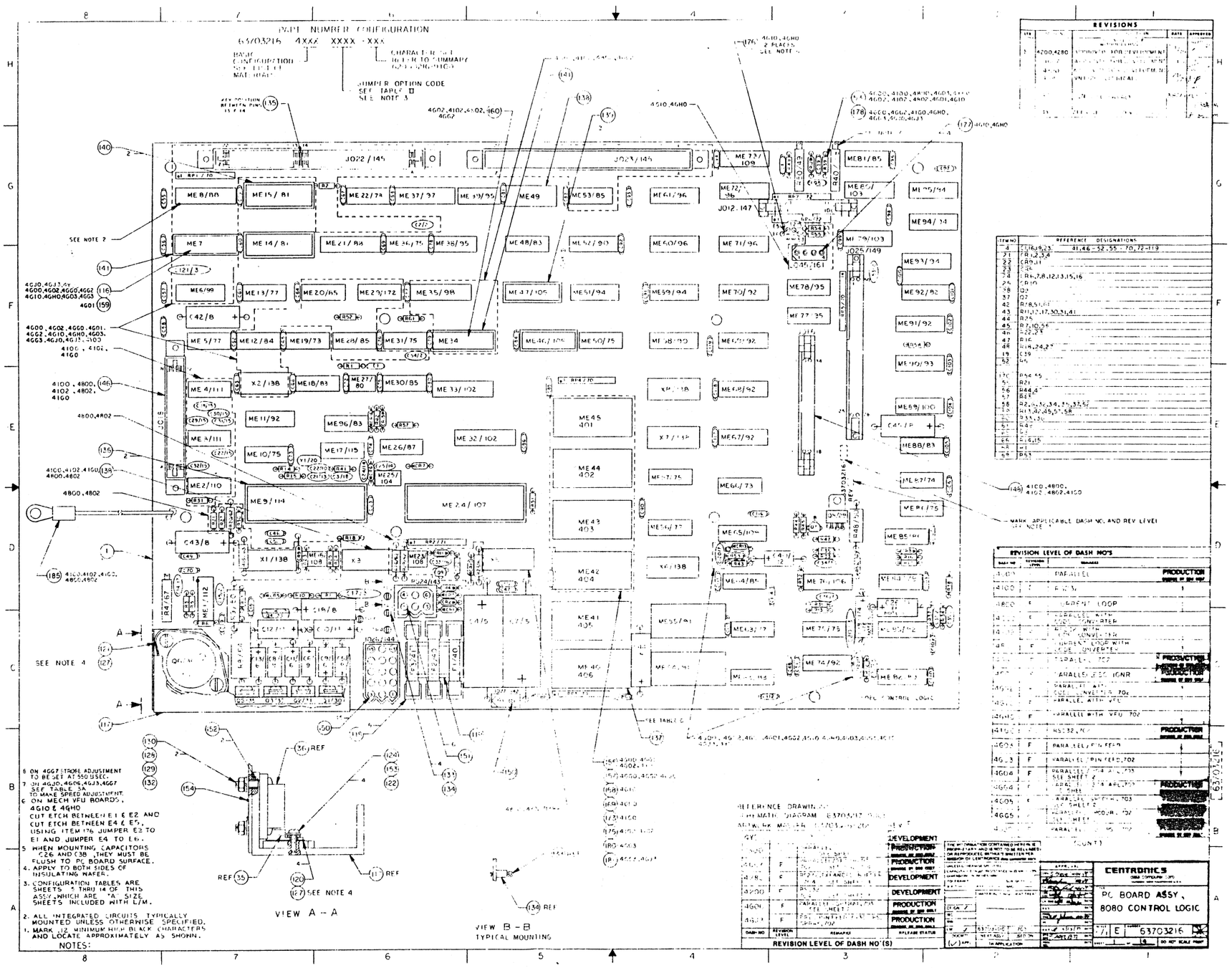

Figure 7-13. LOGIC BOARD ASSEMBLY DIAGRAM (Sheet 1 of 2)

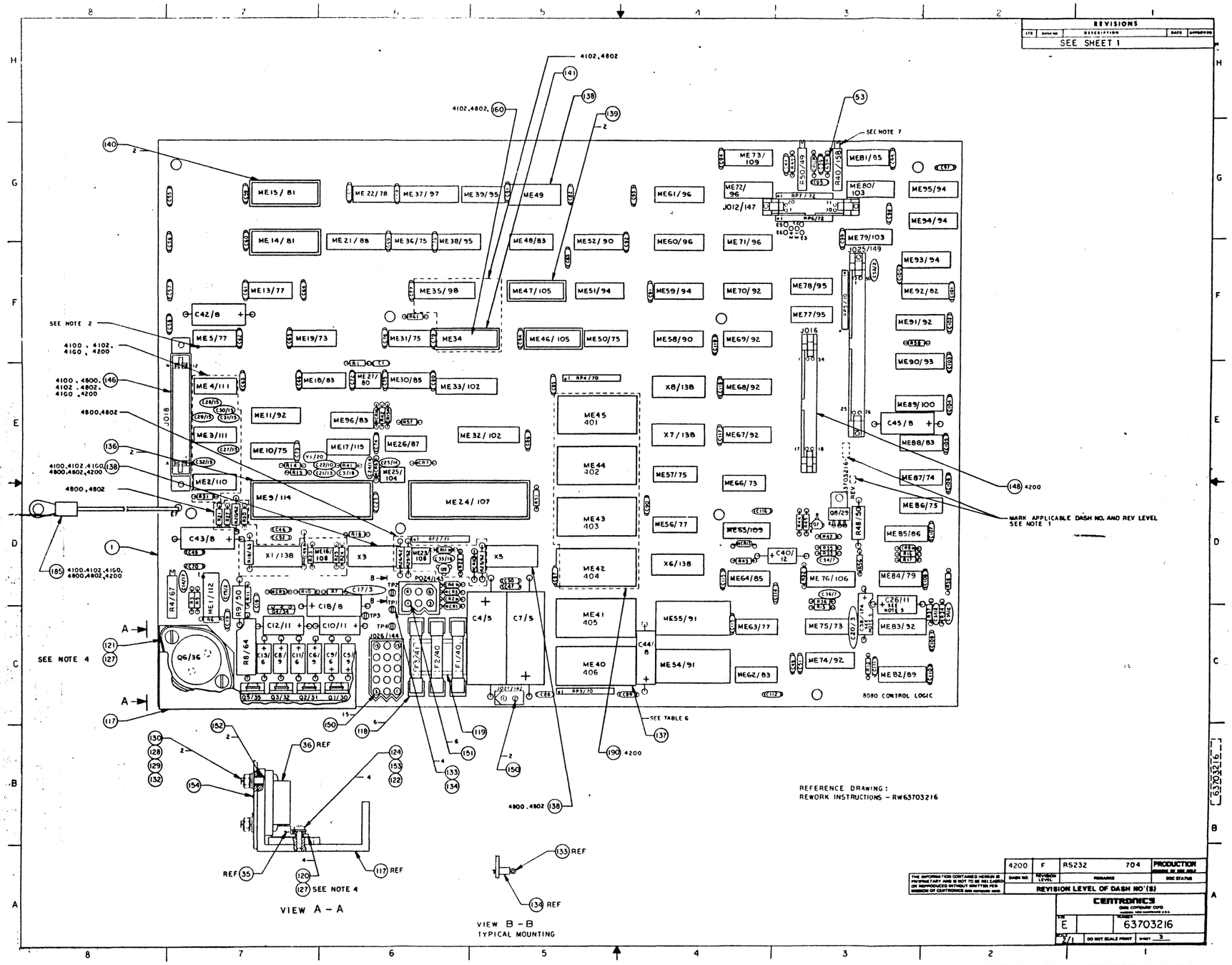

Figure 7-13. LOGIC BOARD ASSEMBLY DIAGRAM (Sheet 2 of 2)

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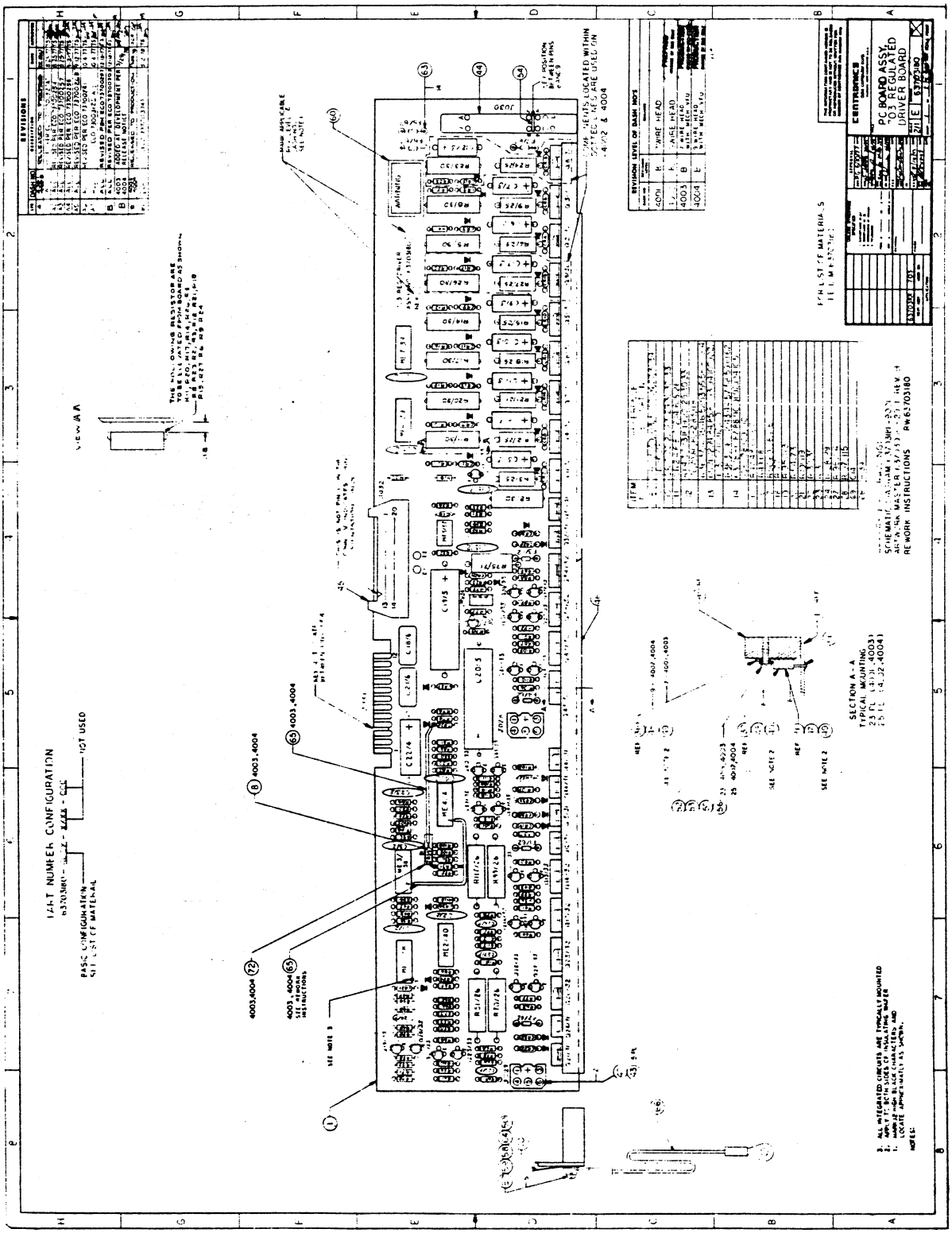


Figure 7-14. POWER DRIVER BOARD ASSEMBLY DIAGRAM

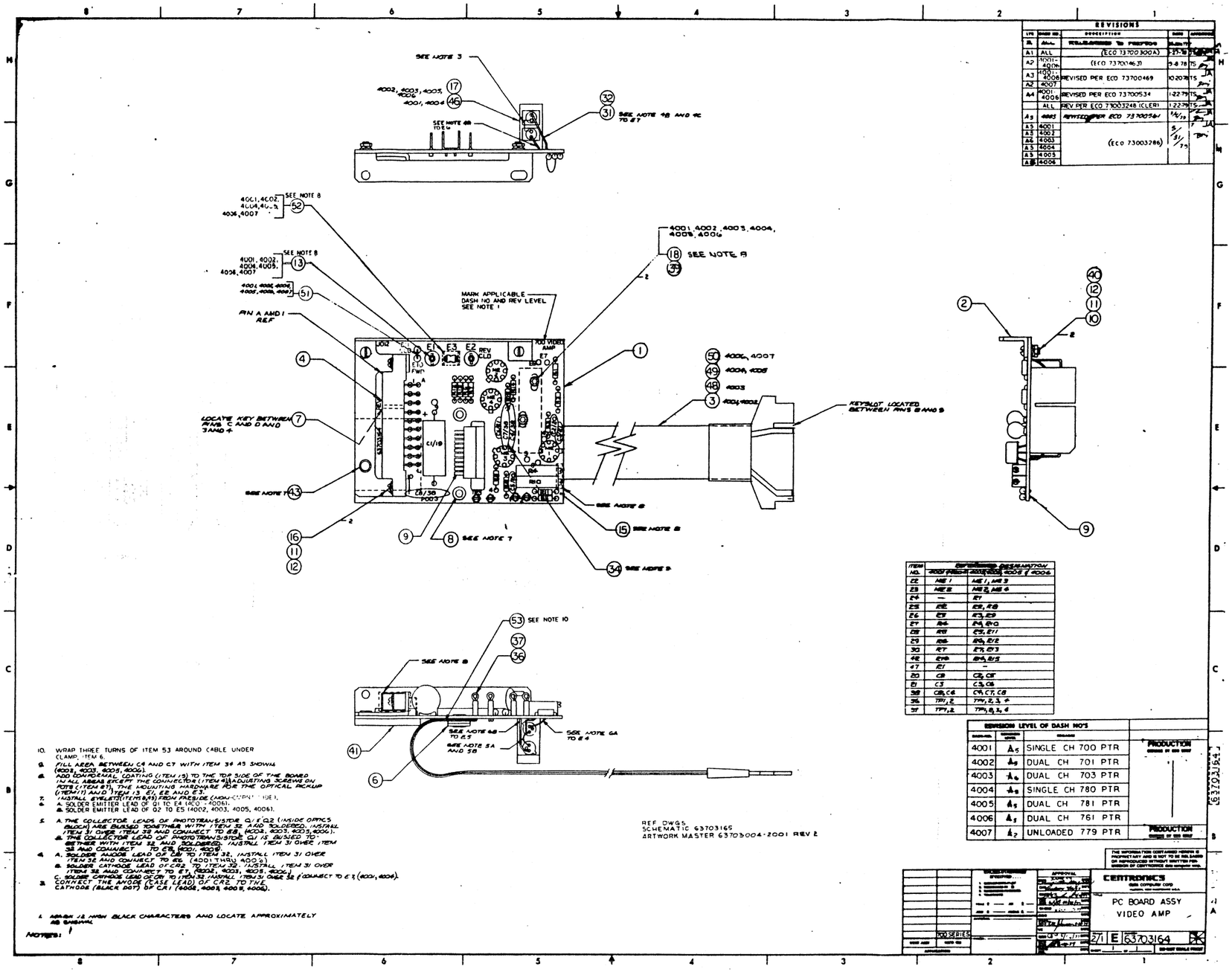


Figure 7-15. VIDEO AMPLIFIER BOARD ASSEMBLY DIAGRAM

145

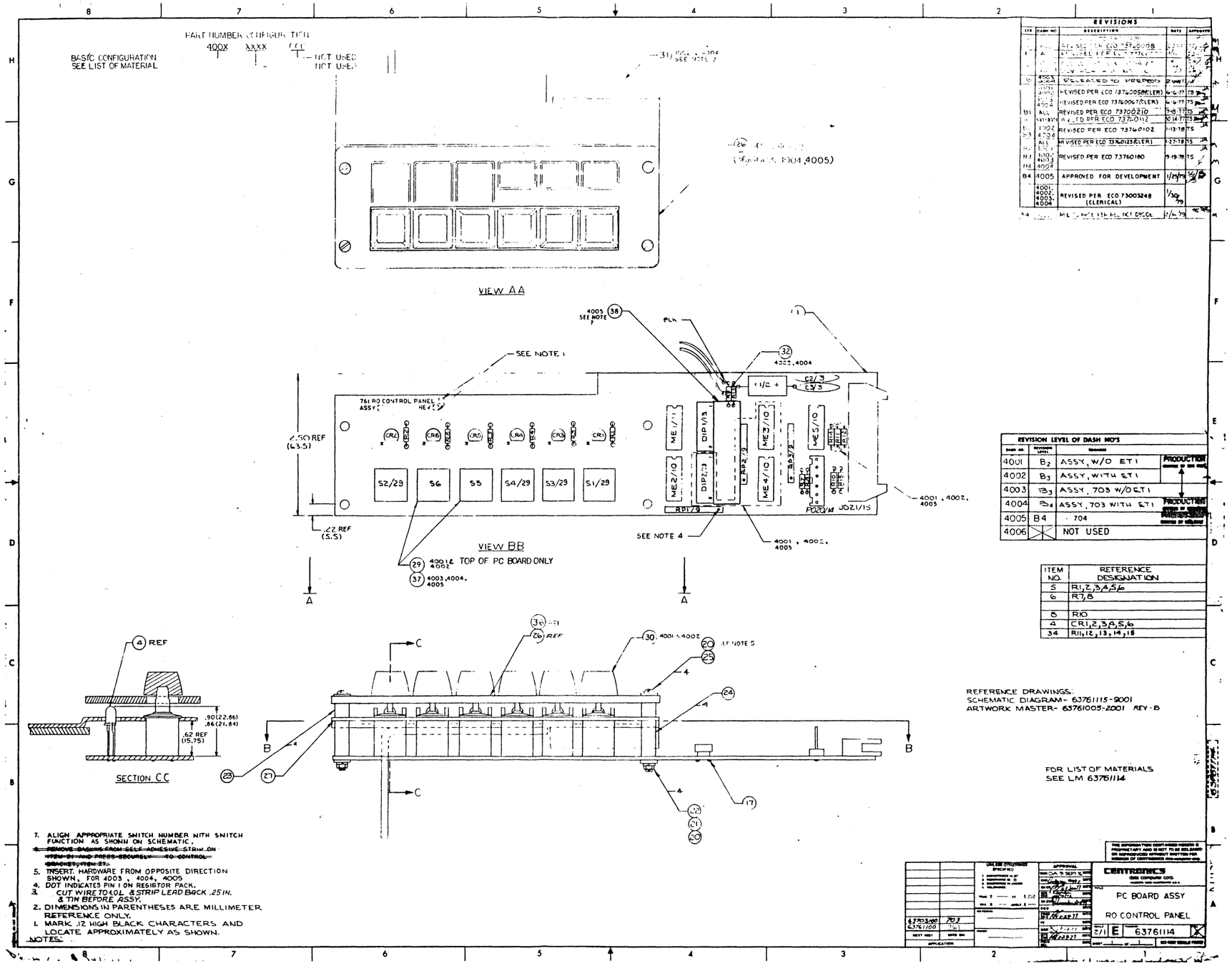
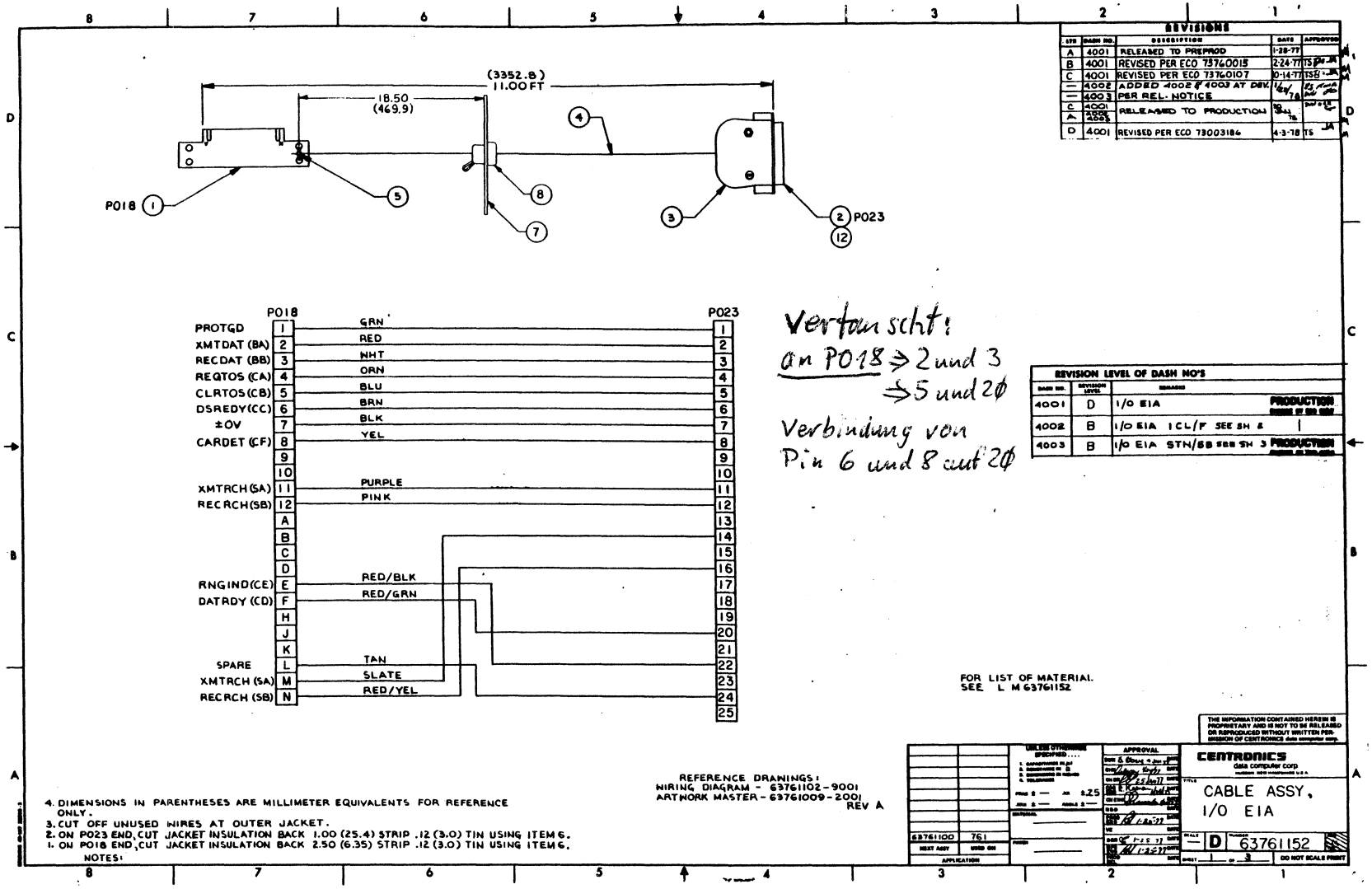


Figure 7-16. CONTROL PANEL ASSEMBLY DIAGRAM



LIST OF MATERIALS
CABLE ASSY, I/O EIA

63761152-4001
REV LEVEL D

ITEM	PART NO	DESCRIPTION	UM	QTY
1	63761009-2001	PC BD AW FINGER BD 12POS	EA	1.0000
2	31340018-1002	CONN PLUG 25POSN PIN CRP REM	EA	1.0000
3	31240432-1001	HOOD ASSY D CONN	EA	1.0000
4	39660030-0011	CABLE RND 15/C 22AWG GRA JKT	FT	11.0000
5	39695231-2001	STRAP CABLE ADJ LKG .625BDL	EA	1.0000
6	30070000-0001	SOLDER 60/40 .032D WIRE	RL	A/R
7	63004100-2001	PLATE ADAPTER INTERFACE	EA	1.0000
8	36150000-2002	BUSHING STRAIN RELIEF .290DIA	EA	1.0000
12	31240060-1001	CONTACT CONN CRP PIN 30-20AWG	EA	15.0000
999	63761010-9001	PC BD DD FINGER BD 12POS	EA	A/R
999	63761102-9001	WIRING DIAG, 761	EA	A/R

- Figure 7-17. I/O EIA CABLE ASSEMBLY DIAGRAM

APPENDIX
SIGNAL GLOSSARY

This signal listing is keyed directly to the Main Logic Schematic No. 63703217 (schematic includes four sheets). All signal mnemonics contained on the schematic are listed alphabetically with their source and destinations.

The following method is used to identify the signal source and destination locations: ME57 -4/2 signifies element ME57, pin 4 located on sheet 2 of the schematic.

The notation (N) after a signal mnemonic is used to indicate the "not" or inverse function of the signal. For example, WRITE(N) is the "not" function of the WRITE signal. The (N) notation is equivalent to the bar appearing over a signal as shown on the schematics.

SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
ACKNLG(N)	Not used.	-	-
ADIRMO-ADIRM7	Address Input RAM Memory 0 to 7 - address lines for 256 character input buffer.	-	-
AFTESC(N)	Not used.	-	-
BADB00-BADB15	Buffered address lines (unidirectional) that identify a particular memory location or I/O port.	ME32 ME33	Memory and I/O ports
BELSPK	Bell speaker signal generated by either MPU or bell code and used to sound speaker.	CR15,CR16	Q7/4
BFDAT0-BFDAT7	Buffered input parallel data lines.	ME8	ME7,X2, ME21,ME14, ME15
BFSYNC(N)	Buffered sync pulse indicating the beginning of a machine cycle.	ME10-10/2	ME18-9/3
BLKBSY(N)	Not used.	-	-
BLKINC(N)	Not used.	-	-
BUFDB0 - BUFDB7	Buffered data lines from data bus to control panel and option port.	-	-
BUFPOT(N)	Buffered paper-out signal.	ME84-6/3	ME60-6/3
BUSY (Status Line)	Not used.	-	-
CARDET(CF)	Carrier detected signal input indicates data set is receiving a valid carrier. Normally, +12 volts when active; -12 volts when off. Enables printer receive circuits in conjunction with DSREDY(CC).	Data Set	EIA Level Shifter ME4/2
CARPUL(N)	Carriage pulse generated by MPU to ramp up and ramp down the carriage stepper motor.	ME56-6/3	ME64-1/3
CG1(N) - CG9(N)	Signals used to energize the print head solenoids.	ME70 ME91 ME81	J025
CLEAR(N)	Clear signal used to clear various logic elements during power up.	ME53-2/2	Sheets 1, 3, 4
CLRTOS(CB)	Clear to send signal input indicates data is ready to receive serial data from printer. Used only with X-ON/ X-OFF protocol where serial transmission of DC3 or DC1 code indicates buffer full/empty status.	Data Set	EIA Level Shifter ME3/2
COLOT7	Columns 0 to 7 - signal used to gate head position bits 0 to 7 onto data bus.	ME92-5/3	ME79-15, 1/3 ME81-15/3
CONBSY(N)	Not used.	-	-
CONCHR	Not used.	-	-
CONCHR(N)	Not used.	-	-
CONPO9	Control character 09 signal switches input buffer to MPU.	ME37-2/3	ME8-1, 19/1 ME21-1, 19/2

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SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
CO8T11	Columns 8 to 11 signal used to gate head position bits 8 to 11 onto data bus.	ME92-6/3	ME81-1/3
CPUACK(N)	Not used.	-	-
CRMTSL(N)	Carriage stepper motor slew control.	ME68-11/4	J025-34/4
CRMTO1-CRMTO4	Carriage motor phases 1 to 4 used to drive carriage stepper motor.	ME91	J025
DATA STROBE (N)	Not used.	-	-
DATRDY(CD)	Data terminal ready output signal used to indicate buffer full when at -12 volts or empty when at +12 volts (DIP switch selectable).	TTL Level Shifter ME2/2	Data Set
DATA01-DATA08	Not used.	-	-
DBUSBO-DBUSB7	Bi-directional data bus lines on which data can flow between the MPU and memory or I/O port.	-	-
DSREDY(CC)	Data set ready signal input enables printer receive circuits in conjunction with CARDET (CF) (+12 volts on, -12 volts off).	Data Set	EIA Level Shifter ME4/2
EIADAT	Serial input data after conversion from EIA levels (±12 volts) to TTL levels (+5 volts and gnd).	EIA Level Shifter ME3/2	Jumper Platform X3/2
ENBOP1(N)-ENBOP3(N)	Enable signals P1 to P3 - used to clock CG lines and motor control. (ENBOP3 not used).	ME56	ME70 ME91 ME81 ME73 ME69 ME37
ENDBIN	Enable DBIN signal indicating that the data bus is in an input (high) or an output (low) mode.	ME57-4/2	J016-4/2
ENSERO(N)	Enable serial output signal for DIP switch 1 and 2 (1/2 of each).	ME92-4/3	J025-49/3
ENSPN2(N)	Enable signal for control panel switch inputs.	ME92-1/3	J025-46/3
ENSWOP(N)	Enable signal for RTP, EOP and DIP switches.	ME92-3/3	J025-48/3
ESC	Not used.	-	-
ESSEB8	Not used.	-	-
EXINPT(N)	Not used.	-	-
EXPCDE	Expanded code signal indicating printer received 0E16 code.	ME6-4/1	ME62-6/3
EXTINT	External interrupt signal to I/O controller 5501 (ME9) which in turn generates an interrupt to the MPU. When an optional interrupt (OPTINT) is present,	ME75-8/1	ME9-22/2

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SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
EXINTØ(N)	CLRTOS signal after EIA to TTL level conversion. (External input to I/O controller).	EIA Level Shifter ME3/2	ME9/2
EXINT1(N)	DSREDY signal after EIA to TTL level conversion.	EIA Level Shifter ME4/2	ME9/2
EXINT2(N)	Not used.	-	-
EXINT3(N)	CARDET signal after EIA to TTL level conversion.	EIA Level Shifter ME4/2	ME9/2
EXINT4(N)	Not used.	-	-
EXTOTØ(N)	REQTOS signal before TTL to EIA level conversion (External output of I/O contoller).	ME9/2	TTL Level Shifter ME2/2
EXTOT1(N)	XMTRCH signal before TTL to EIA level conversion.	ME9/2	TTL Level Shifter ME2/2
EXTOT2(N)	DATRDY signal before TTL to EIA level conversion.	ME9/2	TTL Level Shifter ME2/2
EXTOT3(N)	Not used.	-	-
FAULT(N)	Not used.	-	-
HDPSOO-HDPS11	Head position bits which give absolute head position at all times.	ME93 ME94 ME95	ME79 ME81
INDCLK(N)	Indicator clock used to clock control panel latch.	ME56-5/3	J025-50/3
INPRIM(N)	Not used.	-	-
INTACK	Not used.	-	-
KBB00-KBB07	Data lines to/from control panel (J025) or to option port (J016).	-	-
KBDENA(N)	Keyboard Data Enable - enables signal to data bus.	ME88-11/3	
LD	Not used.	-	-
LNCOMP(N)	Not used.	-	-
LODRAM(N)	Not used.	-	-
MEMBL1(N)	Memory enable line for PROM #1.	X8-1/4	X8-2, 6/4
MEMENA(N)	Memory enable signal used to enable all memory devices.	ME64-11/3	ME63-4/4
MOTOR CONTROL(N)	Motor control signal used to turn the stepper motors on and off.	ME69-14/4	J025-35/4
OPTINT(N)	Option interrupt signal which ..s from option board and causes interrupt to the MPU.	J016-2/1	ME75-10/1
OUTLAT(N)	Output latch signal.	ME56-15/3	ME68-9/4
PAPOUT(N)	Not used.	-	-
PE	Not used.	-	-
PRIMEC(N)	Not used.	-	-

SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
RAMAD0-RAMAD7	Not used.	-	-
RAMCCK(N)	Not used.	-	-
RECDAT(BB)	Input EIA serial receive data line from data set.	Data Set	EIA Level Shifter ME3/2
REQTOS(CA)	Request to send output line from printer to data set held active at +12 volts by	TTL Level Shift -	Data Set
REVESE	Reverse signal controls direction of carriage movement.	ME68-2/4	ME90-5/3
RTP	Ready-to-print signal generated by MPU after it detects the head is over the RTP switch.	ME50-8/3	ME93-14/3 ME94-14/3 ME95-14/3
SEL(N)	Not used.	-	-
SELP00-SELP15	Memory mapping address signals.	ME54	-
SET8(N)	Not used.	-	-
SERXMT	Output serial transmit data (X-ON/X-OFF protocol only) before TTL to EIA conversion.	ME9/2	TTL Level Shifter ME2/2
SLCT	Not used.	-	-
SLEWCR	Slew carriage signal controlling speed of carriage.	ME68-7/4	ME74-13/3 ME81-13/3
SPEAK(N)	Signal generated by MPU and used to produce a speaker signal tone.	ME69-3/4	ME5-1/1
SPEAKER	+15V supplied to the speaker.	J026-5, 4/1	J027-1/4
SPEAKER RET	Speaker return signal used to drive the speaker (alarm)	Q8/4	J027-2/4
SRDATA	Serial EIADAT after being jumpered through platform X3. (RCV input to I/O controller.	Platform X3	ME9/2
STASTB(N)	Status strobe for MPU status word clocking.	ME31-2/3	ME30-11/3 J016-9/3 ME64-3/3
STMTSL(N)	Paper stepper motor slew control.	ME68-14/4	J025-33/4
STMTO1(N)-STMTO4(N)	Paper motor phases 1 to 4 - used to drive paper stepper motor.	ME67/4	J025/4
SYNC	Synchronizing signal issued by the MPU indicating the beginning of a machine cycle.	ME24-19/2	ME10-11/2 ME9-19/2
S1OBIN(N)	ANDed $\overline{\text{SELP10}}$ and $\overline{\text{WRIBIN}}$.	ME62-3/3	ME61-1, 15/3 ME60-1, 15/3 ME72-1, 15/3 ME71-1, 15/3 ME5-10/2

SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
VFUCH1(N)- VFUCH12(N)	VFU inputs from paper tape reader.	J012/3	ME62 ME60 ME73
VFULSW(N)	VFU load switch signal which senses paper in VFU.	J012-12/3	ME73-3/3
VFUSTB(N)	VFU strobe from paper tape reader.	J012-9/3	ME73-13/3
VIDEO1(N)	Video output from channel 1 of the video amplifier	J025-31/3	ME76-14/3
VIDEO2(N)	Video output from channel 2 of the video amplifier.	J025-32/3	ME76-11/3
VIDINT	Video interrupt generated from video input pulses.	ME67-8/3	ME75-13/3 ME9-32/3
WRIBIN(N)	WRITE(N) and ENDBIN(N) "anded" together = Read.	ME57-6/3	ME56-18/3 ME62-5/4
WRITE	MPU write command indicates write operation on the data bus to memory or to an I/O port.	ME57-12/2	J016-3/2
XMTDAT(BA)	SERXMT data after TTL to EIA conversion.	TTL Level Shifter ME2/2	Data Set
XMTRCH(SA)	Transmit reverse channel line used for buffer status signal. DIP switch selectable polarity of ±12 volts for full or empty condition.	TTL Level Shifter ME2/2	Data Set
Ø1 IN	Phase 1 input clock to MPU.	ME25-7/2	ME24-22/2 ME9-20/2
Ø2 IN	Phase 2 input clock to MPU.	ME26-6/2	ME24-15/2 ME9-21/2
Ø2BY2	Phase 2 by 2 clock.	ME26-12/1	ME26-1/1 ME74-9/1
Ø2BY8	Phase 2 by 8 clock	ME26-8/1	ME17-5/1 ME12-3/1
36 VRMS	AC voltage from multitap transformer used to generate +12VDC, -12VDC, -5VDC.	P024-3, 6/1	CR1,CR2, CR3,CR4
+OV	Signal ground.	P024-4, 1/1	-
+15VDC	DC voltage used to generate +5VDC and the unregulated +15VDC.	P024-2, 5/1	F3
+12V	Regulated +12VDC generated from 36 VRMS and used to drive the logic.	TP1/1	J026-12/1
-12V	-12VDC is generated and used in the same manner as +12VDC.	TP2/1	J026-9/1
-5V	Regulated -5VDC generated by -12VDC and used to drive the logic.	TP3/1	J026-3/1
+15VDC	Unregulated +15VDC generates the +5VDC, drives the clamp circuit on the power driver board and the speaker circuit on main logic board.	P024-2, 5/1	J026-6/1

SIGNAL NAME	DESCRIPTION	SOURCE	DESTINATION
+5V	Regulated +5VDC generated by +15VDC and used to drive the logic.	TP4/1	J026-15/1
+5V VIDEO AMP ONLY	Separate +5VDC provided for video amplifier to eliminate noise.	TP4/1	J026-13/1
+OV VIDEO AMP ONLY	Separate signal ground provided for video amplifier.	P024/-4, 1/1	J026-7/1