SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1501/1530

TP-1780FN

Dec.14,1973		1

SUBJECT 1501: Release of 1K Memory Test.

MACHINES AFFECTED: All 1501's.

PROBLEM: The system 4 memory test programs which have been available, C4T memory test and the Automatic System Test memory test, did not completely test the first 1,000 bytes of memory.

Memories having faults in the first 1K appeared good using these memories tests and yet, application programs were not funcioning properly.

Using the new 1K memory test FN 5722 in addition to the C4T memory test, should be a complete test for either a 4,8, or 16K memories.

DESCRIPTION: The 1K memory test program is a four record program. The special boot-strap record uses a minimum of program instructions to load the next 3 program records into octal locations P14-000, P14-200, and P15-000. The section 1 index registers are used, and the address stack locations are shifted such that all of P00 is tested.

To make additional copies of this Program:

A. Load C4T Program.
B. Select '2',copy.
C. Load 1K memory test program tape onto Drive 2.
D. Load a write enabled scratch tape on Drive 1.
E. Depress the Start Key,
F. After a tape error indication, more copies can be made by depressing the Reset switch and following steps D and E.

SYSTEM REQUIREMENTS: 4K 15Ø1

Source listing included in 1500 Manual.

SINGER

BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1501/1530

TP-1780FN

Dec. 14,1973		2

SUBJECT: Malfunction in Processor which is not detected by the Processor Diagnostics Test.

MACHINES AFFECTED: All 1501's

ACTION REQUIRED: Information only.

INFORMATION: The I2 cycle is skipped during many instructions. If a malfunction occurs in the processor board and the I2 cycle is not skipped, the automatic system test (Processor Diagnostics) will not detect it. However, it can be detected later in the automatic system test when the tape speed is checked. It will result in the normal 10 I.P.S. change to about 12 I.P.S. The problem may be verified and corrected by installing another processor Bd. The tape speed should then return to within the correct specifications.

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1501/1530

TP-1780FN

Dec.14,1973		3

SUBJECT: 1501 Improvement Cogar P.S. Part No. 9009295-23.

MACHINES AFFECTED: 1501's with Cogar P.S.

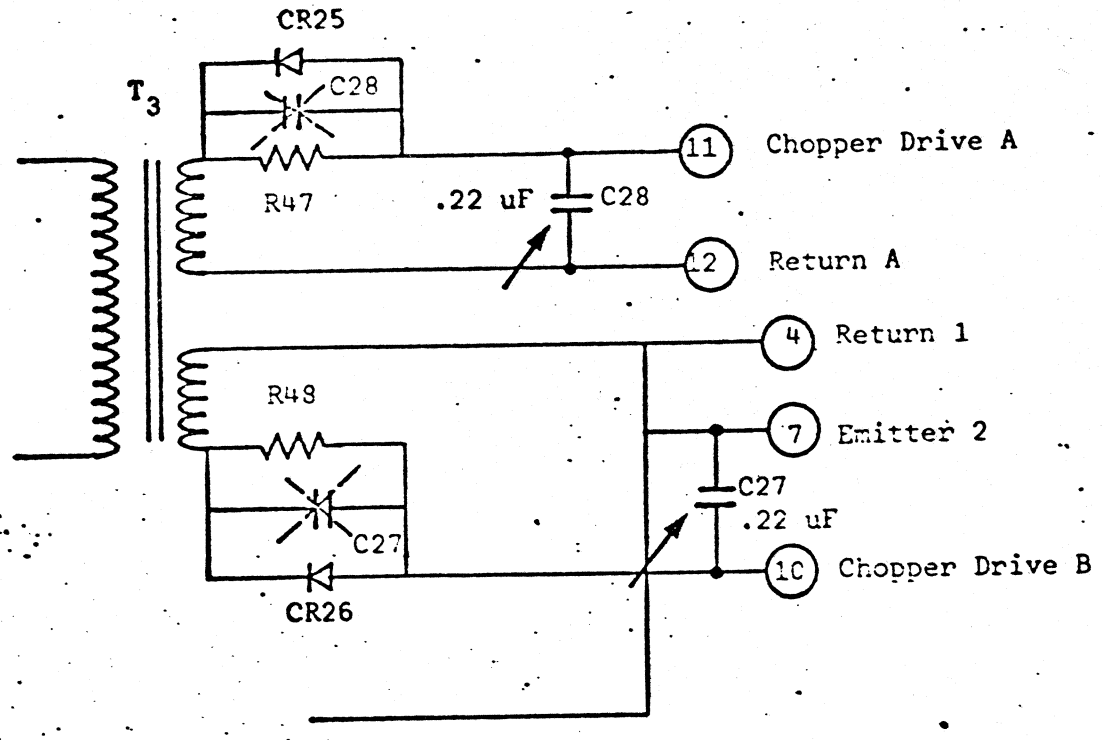
REASON: To improve Power Supply Efficiency and reliability of choppers and chopper drivers, P.C. Board Assy: power supply primary has been changed.

CORRECTIVE PROCEDURE:

1) Remove capacitors C27 + C28.

2) Add .22 uF 50 V cap. from pin 11 to 12 on Primary Board
.22 uF 50 V cap. from pin 7 to 10 on Primary Board.

3) Update Schematics.



Dec. 14, 1973		4

SUBJECT: Implementation of "Texas Instrument: (T.I.) Memory Board into the 1501 System replacing the 'COGAR' memory board.

MACHINES AFFECTED: All new 1501 Systems shipped from Cogar Corp. will have the T.I. memory installed. System serial numbers for these new 1501 Systems will start at 10,000. Processor Boards must be updated to at least revision 9 and CRT/I/O - Board to at least revision 8.

REASON: Information only.

APLICABLE TEST SOFTWARE:

'MØ9' Automatic System Test = FN-5676
Tests first 4K, one pass only.

'C4T' Selectable memory test = FN-5666
Tests either 4K, 8K or 16K continuously

1k Memory Test = FN-5722

Test first 1k completely. Needed because 'MØ9' & 'C4T' Memory tests do not test the first 1k completely.

'T12' Memory Tester

For special memory tester (not yet released)

TIME REQUIREMENT - PROCESSOR BOARD -

		Hrs.	Min.
Rev.	0 - 1	1	-
	1 - 2		15
	3 - 4		05
	5 - 6	1	15
	6 - 7		30
	7 - 8		20
	8 - 9	1	15
	Total	4	40
	Check out time		40
		5 Hrs.	20 Min.

000

TIME REQUIREMENT - C R T / I/O BOARD -

	Hrs.	Min.
Rev. 0 - 1	2	50
1 - 2		20
2 - 3		15
3 - 5		20
5 - 6		20
6 - 7		15
7 - 8	1	-
Total	5	20
Check-out-time	-	40
	6 hours	

CRT/I/O-Boards (Rev.8)

Revision-level of logic-drawings:

Sheet 1	CRT/I/O/-Assy	rev. 8
" 1	CRT/I/O	" 5
" 2	"	" 6
" 3	"	" 3
" 4	"	" 3
" 5	"	" 3
" 6	"	" 6
" 7	"	" 5
" 8	"	" 3
" 9	"	" 3
" 10	"	" 3

Rev. Level 3 does not effect the logic.

(Exception:sheet 10 of the CRT/I/O-logic).

Processor-Board (Rev. 9)

Revision level of logic-drawings:

Sheet	1	proc. Assy	rev. 9
"	1	proc.	" 6
"	2	"	" 6
"	3	"	" 3
"	4	"	" 3
"	5	"	" 3
"	6	"	" 3
"	7	"	" 4
"	8	"	" 3
"	9	"	" 6

REPLACEMENT OF COGAR MEMORIES WITH T.I. MEMORIES

System Requirements

The T.I. memory board requires different Bias voltage levels than the Cogar memory board.

Cogar Memory Voltages	T.I. Memory Voltages
+5	+5
GND	GND
-6	+20
+10	+17.5
	+12

To obtain these voltages the Cogar power Supply must be replaced with an ACME power supply set for these new voltages.

In Addition:

A. The processor board, into which the T.I. Memory Board will be inserted, must be at revision 9 , or higher, and must have a different address jumper plug.

B. The Tape/Crt/Io Bd used in the system must be at revision 8, or higher.

C. A jumper wire must be put on the wire module between wire module pins 1B55 to 2B12.

PROCEDURE FOR REPLACING A COGAR MEMORY WITH A T.I. MEMORY

A. Remove the Cogar memory/processor boards from the 1501 system.

B. Remove the Cogar Memory boards from the processor bd.

C. Check the revision level of the processor board. If the revision level is Rev 8 or lower, bring the P.C. board up to Rev 9 using the attached processor board rework instructions.

D. Change the address jumper plug, to SBM P/N 9012099-17, and install as shown in the attached jumper plug illustration.

E. Insert the T.I. memory board into the processor board chip side up.

F. Check the revision level of the Tape/Crt/Io Board. If the revision level is Rev 7 or lower, bring the P.C. board up to Rev 8 using the attached Tape/Crt/Io board rework instructions.

G. Insert the T.I. memory with processor bd. and the Tape/Crt/Io bd into the system.

H. Put a jumper wire on pins 1B55 to 2B12 of the wired module. See the attached illustration of the wired module.

I. Replace the Cogar Power Supply with the ACME power supply per attached procedure.

J. Adjust the ACME Power Supply voltages per the attached procedure.

K. Remove the Memory/Processor bd. from the System. Insert an extender bd. into the system and plug the processor bd. into the extender bd. The processor bd. should be properly supported in a horizonal position.

L. Set up the memory timing adjustments per the attached procedure.

M. Remove the extender bd. from the system. Insert the T.I. memory with processor.

N. Use available Software Tests to evaluate the Memory.

PROCESSOR BOARD
REVISION HISTORY

Change Rev	Bare Bd Rev	ECD	Reason
Rev #1	Rev #2	S-647	Change to Rev# 2 with necessary rework.
#2	#2	S-647	To allow increase range in memory clock pulse and to give the PI board access to the N-HSC-STALL.
#3	#2		Plastic Mem Board securing screws changed to steel.
#4	#2	S-791	Jumper wire from IC, C22-pin 13 to connector Pin B61.
#5	#2		Changed vendor on capacitor.
#6	#3	S-864	Rev 3 bare bd. with necessary rework; to eliminate program load on power on and to allow the use of the T.I. Memory.
#7	#3	S-915	To improve the memory timing margins for the T.I. Memory.
#8	#3	S-923	To improve the time margin for gating the MDR with the T.I. memory.
#9	#3	S-930	Required for T.I. Memory

SUB-ASSEMBLY Processor SHT 1 OF 1

DATE OF CHANGE RELEASE 5/18/73 ECD NO. S-647

REVISION CHANGE LEVEL: FROM 0 TO 1

REASON FOR CHANGE

Changed from Rev 1 bare board to Rev 2. This rework is needed due to artwork errors.

CHANGE DESCRIPTION

1) Lift G19-4, Jumper to H22-11
2) Lift L8-2; Jumper to L6-2
3) Jumper A4-11 to B1-1
4) Jumper K11-3 to B10-1
5) Jumper connector pin A73 to feed-thru next to A8-16
6) Jumper G7-9 to F7-2
7) Cut top layer run going to H2 - 6. Jumper the run to H2-11
8) Cut run from K4-16 to R22
9) Cut run from K2-16 to R25
10) Lift K4-16, Jumper to the cathode of CR4
11) Lift K2-16, Jumper to the cathode of CR3
12) Lift K18-12,H16-2, H11-3, H15-2 and jumper together
13) Lift C7, Lift K4-1 and K4-2. Connect C7 to K4-1 and K4-2. Connect R24 from feed-thru next to K3-1 to K4-2.
14) Jumper D7-13 to E12/13 - 14 (Not Required on Rev 2 Bare Bds.)
15) Jumper B2-12 to feed-thru below B2-12
16) Jumper A19-7 to D6-2
17) Jumper B14-9 to feed-thru beside B13-8

SUB-ASSEMBLY Processor SHT 1 OF 1

DATE OF CHANGE RELEASE 5/18/73 ECD S-647

REVISION CHANGE LEVEL: FROM 1 TO 2

REASON FOR CHANGE

1. To allow mem clk to be adjustable for memories requiring a 210 - 230 nsec. pulse (See service letter change Cogar Memory Timing).

2. To give the PI board access to the N-HSC-STALL.

CHANGE DESCRIPTION

1. The following rework must be applied to all proc. P.C. assemblies with rev. #2 bare boards.

   A. Capacitor C5 & C7 become a 33pf cap.

   B. Resistor R19 & R24 become a 5K1 res.

2. Jumper connector pin 2B61 to package Pin C22-13

Note: The signal N-HSC-Stall is a signal created on a special board: PI Board (Parallel IO-Board) and is not used for Singer.

SUB-ASSEMBLY Processor SHT 1 OF 1

DATE OF CHANGE RELEASE 2/1/73 ECD NO. S-791

REVISION CHANGE LEVEL: FROM 3 TO 4

REASON FOR CHANGE

This change is manditory for P.I.M. Installation and inventory Control Compatability of Processor Board.

CHANGE DESCRIPTION

1) Place a Jumper Wire from IC Package C22 Pin 13 to Connector Pin B61.

Note:
(included in revision 2 to 3)

Int. S.L. No. 4

ASM ASSEMBLY PROCESSOR SHT 1 OF 1

DATE OF CHANGE RELEASE 5/23/73 ECD NO. S-864

REVISION CHANGE LEVEL: FROM 5 TO 6

REASON FOR CHANGE

Changed to Rev #3 bare board to inhibit program load when power is turned on and to allow use of T.I. Memory.

CHANGE DESCRIPTION

1) Cut Jumper near capacitor (C1) between G22 and F22. (Not required for Rev 2 Bare Bds.)
2) Lift Pins 2 and 6 on I.C. D22A.
3) Place Jumper from D22A-2 (Leg) to D22A-6 (Leg).
4) Place Jumper from D22A-2 (Leg) to G17-14 (Leg).
5) Cut heavy run leading to R27. (Not required for Rev 2 Bare Bds).
6) Place Jumper from other side of R27 to Mem.Conn.Pin 88 (Same Run Cut in Step 5).
7) Lift I.C. Leg G17-3.
8) Lift I.C. Leg E22-2.
9) Place Jumper From E21-3 (leg) to G17-3 (leg).
10) Place Jumper from E22-2 (leg) to E22-1.
11) Place a jumper from E22-1 to E22-8.
12) Lift Legs 1,2, and 3 on I.C. K8.
13) Place a jumper from L10 Pin 3 to K8 Pin 2 (Pad).
14) Place a Jumper from L10 Pin 4 to K8 Pin 1 (Pad).
15) Place a Jumper from L10 Pin 6 to K8 Pin 3 (Pad).
16) Place a Jumper from L10 Pin 5 to G17 Pin 2.
17) Lift I.C. Legs 4,5,and 6 on E21.
18) Place a Jumper from E22 Pin 10 to Connector Pin B07.
19) Place a Jumper from E22 Pin 11 to E21 Pin 5 (Pad).
20) Place a Jumper from E22 Pin 9 to E21 Pin 4 (Pad).
21) Lift I.C. Leg 13 on E21. Tie to VCC (+5V). (D21-14).

SUB-ASSEMBLY Processor SHT 1 of 1

DATE OF CHANGE RELEASE 8/13/73 ECD NO. S-915

REVISION CHANGE LEVEL: FROM 6 TO 7

REASON FOR CHANGE

The following rework is required on all boards to improve the memory timing margins for T.I. memory.

CHANGE DESCRIPTION

1) Lift I.C. leg H3 pin 1.

2) Lift I.C. leg E18 pin 10.

3) Lift I.C. legs G9 pins 2 & 12.

4) Place a jumper from M22 pin 4 to G9 Pin 2,G9 Pin 12, & M20 Pin 3 (legs)

5) Place a jumper from M20 pin 4 to H3 Pin 1, & E18 Pin 10. (legs)

SUB-ASSEMBLY Processor SHT 1 OF 1

DATE OF CHANGE RELEASE 8/24/73 ECD NO. S-923

REVISION CHANGE LEVEL: FROM 7 TO 8

REASON FOR CHANGE

To delay negative going edge of P-CL-0 by the overlap duration of P-TE. This edge gates MDR signals in the tape and I/O. P-TE is the clock for MDR.

CHANGE DESCRIPTION

1) Cut the run leading to connector pin A79.

2) Place a jumper from connector pin A79 to G11 pin 11.

3) Place a jumper from connector pin C05 to G11 pin 12.

4) Place a jumper from E20 pin 2 to G11 pin 13.

SUB-ASSEMBLY Processor SHT 1 OF 2

DATE OF CHANGE RELEASE 9/12/73 ECD NO. S-930

REVISION CHANGE LEVEL: FROM 8 TO 9

REASON FOR CHANGE

T.I. Memory Compatibility

CHANGE DESCRIPTION

1) Jumper G20-2 to Pin 2B12.

2) Cut Run to Pin 2 A78 to Component Side. (For Rev 2 Bare Bds-Cut Run from Pin 2 A78 to Feed Thru)

3) Jumper Pin 2 A78 to K17-5.

4) Jumper E20-1 to K17-6.

5) Jumper K17-4 to F14-13.

6) Cut the 2 Runs on the bottom layer at Mem. Conn. Pins 86 and 87. (Not required for Rev 2 Bare Bds.)

7) Jumper F19-13 to M9-9.

8) Jumper F19-12 to M9-10.

9) Jumper F19-9 to M9-11.

10) Jumper M9-8 to M22-11.

11) Jumper M22-10 to Mem. Conn. Pin 86.

12) Jumper F20-4 to K13-1.

13) Jumper F20-1 to K13-2.

14) Jumper F20-2 to K13-13.

15) Jumper K13-12 to M18-9.

16) Jumper M18-8 to Mem. Conn. Pin 87.

17) Lift E21-12.

18) Jumper E19-14 to L15-6.

19) Jumper L15-9 to L17-7.

20) Jumper E21-3 to L15-12 and L15-7.

SUB -ASSEMBLY Processor SHT 2 OF 2

DATE OF CHANGE RELEASE 9/12/73 ECD NO. S-930

REVISION CHANGE LEVEL: FROM 8 TO 9

CHANGE DESCRIPTION (continued)

21) Jumper D22-3 to L15-8.

22) Jumper L15-11 to L17-11.

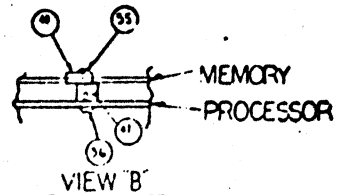
13) Jumper L17-10 to E21-12.

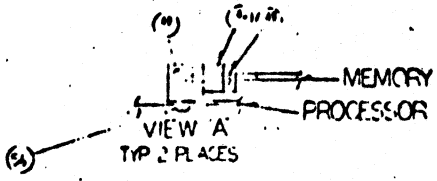
For revision 2 bare-boards:

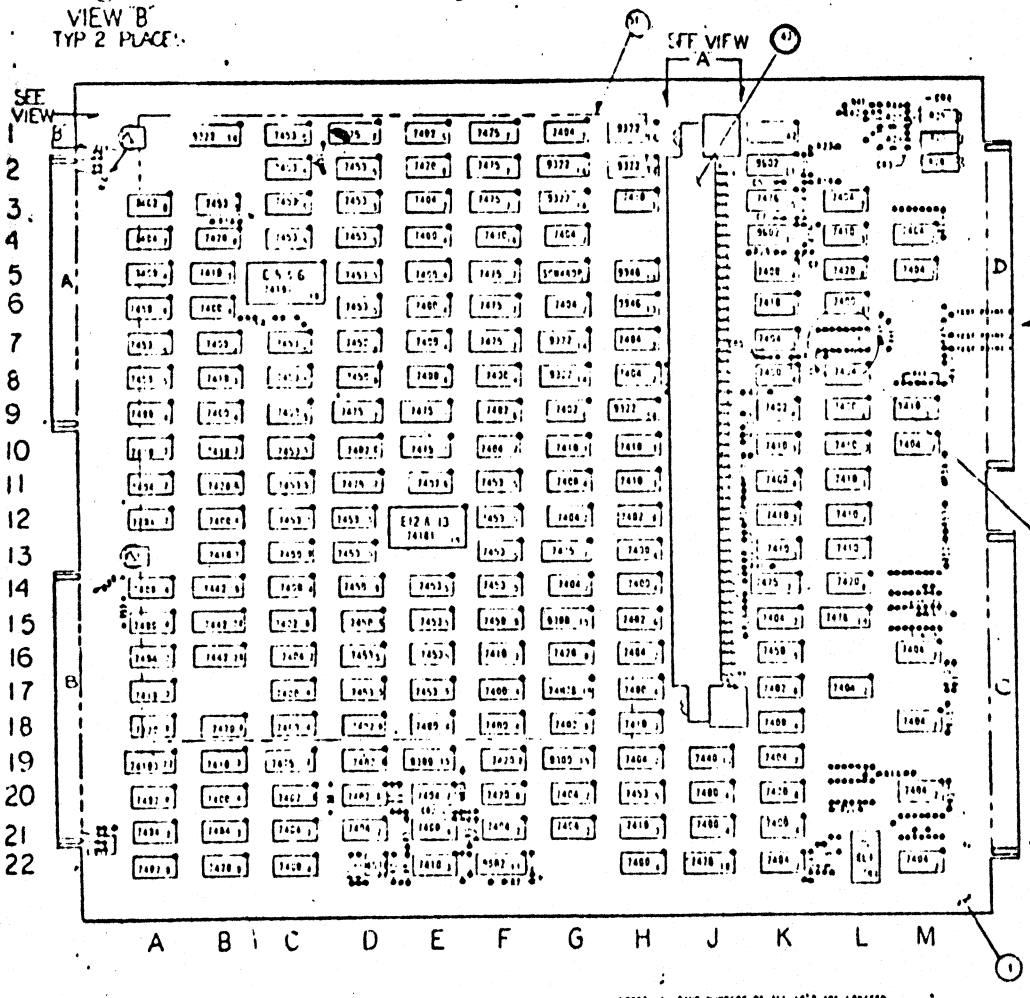
24) Jumper H 21-4 to Mem. Connector Pin 89

25) Jumper G 17-2 to B o7 Connector Pin

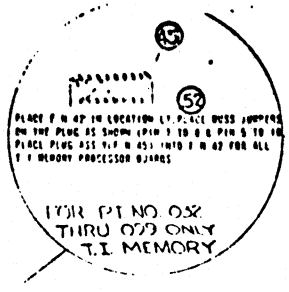
26) Jumper G 17-1 to Ground



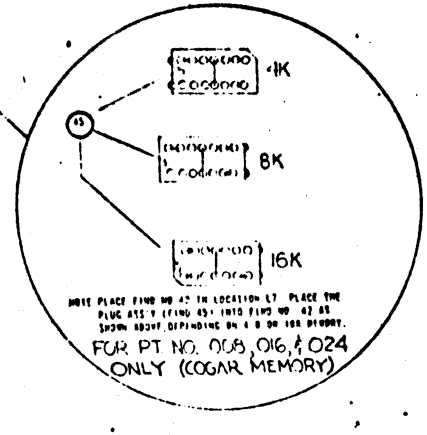




NOTES. 1. FIND NUMBERS OF ALL IC'S ARE LOCATED ON THE IC'S AT THE RIGHT SIDE.
2. FOR OTHER FIND NUMBERS SEE LIST AT TOP RIGHT OF THIS PAGE
3. PIN NO 1 ON ALL IC'S ARE IN LINE WITH THE EXCEPTION OF B5 B6 C5 C6 D12 D13, E12 AND E13



FIND NO.	DESCRIPTION	LOCATION
23	RES. 1K	B1,B2,B3,B4,B5,B6,B10,B13,B14,B15,B16,B20,B21,B22,B23, B24,B25,B26,B27,B28,B30,B40,B41,B42,B43,B44,B45,B46,B47, B48,B49,B50,B51,B52,B53,B54,B55,B56,M8,,B47,B58,B26,B27
24	RES. 10K	B7
25	RES. 200 OHM	B9
26	RES. 1 49 100 OHM	B10 B11
27	RES. 2K	B12 B29
28	RES 510 OHM	B17
29	RES. 3K3	B22,
30	RES 150 OHM	B28
31	RES 8K2	B29
32	RES 100 OHM 1 W	B31 B32
33	RES 1K8 POT	B33 B33,B35
35	CAP .500 PF.	C3
36	CAP .330 PF.	C4,C5
37	CAP .22 PF.	C6
38	CAP .100 PF.	C8 C9
39	DIODE 1N5148	CR2,CR5
40	DIODE 5 1V ZENER	CR3 C04
44	CAP .68 MFD	C10 C11
53	CAP .33 PF.	C5,C7
54	RES 5K1	B18 B24



*PLACE BUSS WIRE AS SHOWN ON EACH TEST POINT.

COGAR NO	DESCRIPTION
00 0	4K COGAR MEMORY
01-0	8K COGAR MEMORY
02-0	16K COGAR MEMORY
03-0	4K T I 9 BANK
04-0	8K T I BANK
05-0	24K T I BANK
06-0	32K T I BANK
07-0	48K T I BANK
08-0	64K T I BANK
09-0	96K T I BANK

S-930	SEE REWORK INST.	JW	9
S-923	SEE REWORK INST	JW	8
S-915	ADD DIODE CR3 THRU 008 SEE REWORK INST.	JW	7
S-864	REMARK FOR REV J BARE BDS		6
			4
			1

See reverse

TAPE/CRT/IO

REVISION HISTORY

LEVEL	BARE BD. REV.	CHANGE DOC.	BRIEF CHANGE DESCRIPTION
REV # 1	# 3	ECD S-647	
# 2	# 3	ECD S-647	Eliminates Bad Start Pattern
# 3	# 3	ECD S-647	Allows C4DE Operation with Additional wire in wired module
# 4		Does not exist	
# 5	# 4	ECD S-870	Rev # 4 bare bd and necessary rework; added resistors R93 thru R105 due to artwork errors
# 6	# 4	ECD S-900	Changed B6 and B9 to 74195
# 7	# 4	ECD S-922	To allow time to insure that the MDR is valid. A revision 7 T/C/I has to be used with the T.I. memory.
#7	#5	S-930A	Bare Board Change.
#8	#6	S-930	Required for T.I. memory.

SUB-ASSEMBLY TAPE/CRT/IO Bd 8-Layer SHT 1 OF 3

DATE OF CHANGE RELEASE 3/29/72 ECD NO S-647

REVISION CHANGE LEVEL: FROM - TO 1

REASON FOR CHANGE

The following rework must be applied to all Tape/CRT/IO P.C. assemblies with Rev. 2 bare boards.

CHANGE DESCRIPTION

1. a. Place a 7420 I.C. in spare location D8.
   b. Lift I.C. pin D4-6
   c. Place following jumpers on designated I.C. pins :

E7-6	to	D8-4
D4-10	to	D8-1
D3-8	to	D8-2
D6-11	to	D8-5
D8-6	to	E7-5
D7-7	to	D8-7
D7-14	to	D8-14

2. Jumper connector pin C59 to connector pin D55.

3. Lift E15-pin 11 and C11 pin 6 - wire same.

4. Lift C4 pin 3 and C2/3 pin 19 - wire same.

5. Lift D4 pin 1, D2 pin 4, and C2/3 pin 3 - wire same.

6. Lift E12 pin 1, E13 pin 2 - wire same.

7. Lift A22 pin 1 - wire to Con. B-78.

8. Lift J7 pin 7 - wire J7-7 to J6-7.

9 Lift K13-9, K13-11 - April 21, 1972
Jumper K13-8 to K13-9 PAD
Jumper K13-11 to L12-2

10. Lift Cathode of Q1 April 21,1972
Lift C9-10
Lift R113
Jumper R113 Pads
Jumper 51 Ohm res, from cathode to GND,
Jumper Cathode to F3-13,
Jumper F3-12 to C9-10

SUB-ASSEMBLY TAPE/CRT/IO Bd 8-Layer SHT 2 OF 3

DATE OF CHANGE RELEASE 3/29/72 ECD NO. S-647

REVISION CHANGE LEVEL: FROM - TO 1

REASON FOR CHANGE

The following rework must be applied to all Tape/CRT/IO P.C. assemblies with Rev. 2 bare boards.

CHANGE DESCRIPTION

11. Lift Package Pin B10-11
    Jumper B13-1 to B1-1
    Jumper C7-4 to B1-2
    Jumper C7-3 to B1-13
    Jumper B1-12 to D12-5

12. Lift package pin E18-2
    Jumper lifted pin E18-2 to E18-4

13. Place a SN7474 package in position F 15
    Lift B12-1,2
    Lift B13-5
    Jumper B10-3 to F15-4,13
    Jumper B1-12 to F15-2
    Jumper F12-7 to F15-3
    Jumper F12-6 to F15-11
    Jumper F14-8 to F15-10
    Jumper F15-6 to F15-12
    Jumper F15-9 to B12-2 pin
    Jumper F15-8 to B13-5 pin
    Jumper B12-4 to B12-1 pin
    Jumper F15-7 to GND
    Jumper F15-14 to +5
    Jumper F15-1 to +5

14. Jumper N2-1 to N2-2

*NOTE : When Rev. #3 bare boards are used, this rework will no longer be needed.

REASONS:

1. Two potential turn-on problems exists if the high speed F/F comes up set.
   A. A false sprocket may be generated
   B. Runaway circuit may latch.

2. PWR-ON switches of the C4E and Multi-Deck must be ordered.

SUB-ASSEMBLY TAPE/CRT/IO Bd 8-Layer SHT 3 OF 3

DATE OF CHANGE RELEASE 3/29/72 ECD NO. S-647

REVISION CHANGE LEVEL: FROM - TO 1

REASON FOR CHANGE

The following rework must be applied to all Tape/CRT/IO P.C. assemblies with Rev. 2 bare boards.

REASONS:

3. thru 8. - Artwork Errors

9. A race condition exists in I/O logic which can generate a false I/O sprocket when the C4E is in a slave mode in the C4E to C4E program.

10. A condition exists where the runaway P.U.T. will remain latched (runaway on first block of Prg. Load) and the program load switch will not clear. This fix makes the P.U.T. output a pulse.

11. The WR-CK-DROP F/F may come up set which would give a worst-case read condition. This would be detrimental in reading a marginal first record in a program load.

12. To allow use of CRT units with slow switching transistors.

13. Implementation of a crap-in-the-gap detector to detect crap during a write operation.

14. Artwork Error

SUB-ASSEMBLY TAPE/CRT/IO Bd 8-Layer SHT 1 OF 1

DATE OF CHANGE RELEASE 8/28/72 ECD No. S-647

REVISION CHANGE LEVEL: 1 TO 2

REASON FOR CHANGE

1. GND MISSING ON C6
2. Eliminates writing wrong start pattern by blocking noise into shift register.

CHANGE DESCRIPTION

1. Add jumper from bottom of Cap, C6 to GND (2nd res. across from C6, a 1K).

2. Drill feed-thru above B9-1. Add 1K res. at F22A between pins 5 & 8.
   Add jumpers F22A-7 to F11-1
   F22A-6 to F6-11
   F22A-5 to B7/8-22

SUB-ASSEMBLY TAPE/CRT/IO Bd 8-Layer SHT 1 OF 1

DATE OF CHANGE RELEASE 9/7/72 ECD NO. S-647

REVISION CHANGE LEVEL: FROM 2 TO 3

REASON FOR CHANGE

Allows one backboard jumper wire from 1B57 to GND to change a C4E machine to a C4DE.

CHANGE DESCRIPTION

1. Lift A5-7 Pin

2. Lift A13-7 Pin

3. Jumpers - B13-5 to E22-9
   Conn. Pin B57 to E22-10
   E22-8 to A5-7 Pin
   B12-2 to A13-7 Pin

4. Insert a 1K res. from E22-10 to E22-14 (+5)

SUB-ASSEMBLY Tape/CRT/IO Bd 8-Layer SHT 1 OF 1

DATE OF CHANGE RELEASE 5/31/73 ECD No. S-870

REVISION CHANGE LEVEL: FROM 3 TO 5

REASON FOR CHANGE

The following Rework must be applied to all Assemblies using Rev. 4 Bare Boards:
These are Artwork Errors.

CHANGE DESCRIPTION

1. Lift (K) Leg on Q1.
2. Cut run leading to R113 on solder side.
3. Place a Jumper from Q1 (K-Leg) to the left Leg of R113.
4. Place a Jumper from A9 Pin 15 to A11 Pin 4.
5. Place a Jumper from D8 Pin 6 to N3 Pins 6 and 7.

NOTE: This rework will no longer be required when Rev. 5 Bare Boards are available.

SUB-ASSEMBLY TAPE/CRT/IO SHT 1 OF 1

DATE OF CHANGE RELEASE 7/23/73 ECD NO. S-900

REVISION CHANGE LEVEL: FROM 5 TO 6

REASON FOR CHANGE

The I.C. used for the accumulator was loaded above rated specifications.

CHANGE DESCRIPTION

B6 and B9 from 9300 to 74195.

SUB-ASSEMBLY TAPE/CRT/IO SHT 1 OF 1

DATE OF CHANGE RELEASE 8/23/73 ECD NO. S-922

REVISION CHANGE LEVEL: FROM 6 TO 7

REASON FOR CHANGE

The following rework is required to allow time to insure MDR is valid:

CHANGE DESCRIPTION

1) Lift I.C. leg J7 pin 3.
2) Place a jumper from C4 pin 1 to F1 pin 9.
3) Place a jumper from D16 pin 11 to F1 pin 10.
4) Place a jumper from F1 pin 8 to J7 pin 3 (leg).

NOTES: 1) This rework will no longer be required when rev. 6 bare boards are available.

2) E.C.D. S-900 brought this assy. to rev. 6. Since rev.6 has not been incorporated yet: rev. 7 should be incorporated with E.C.D. S-900 when the parts are available.
No rev. 6 assemblies will appear in the field.

SUB-ASSEMBLY Tape/Crt/Io Board SHT 1 OF 1

DATE OF CHANGE RELEASE 9/12/73 ECD NO. S-930

REVISION CHANGE LEVEL: FROM 7 TO 8

REASON FOR CHANGE

T.I. Memory Compatibility

CHANGE DESCRIPTION

Insert an I.C., type 7486 into F16 position.

1) Lift C19-13.
2) Lift B20-1.
3) Jumper C19-6 to C19-13.
4) Jumper C19-12 to E22-13.
5) Jumper C16-3 to E22-12.
6) Jumper E22-11 to E13-3.
7) Jumper E13-4 to F16-1.
8) Jumper B19-12 to F16-2.
9) Jumper F16-3 to B20-1.
10) Lift C15-5.
11) Lift C15-10.
12) Lift D17-12.
13) Jumper D17-13 to D17-12 (Pad),
14) Jumper Pin 1B55 to K19-9.
15) Jumper C5-13 to K19-10.
16) Jumper K19-8 to C15-5 and C15-10.
17) Place R106 (Resistor 5K1) between K19 Pin 9 and +5V. (K19 Pin 14).
18) Jumper F16-14 to F17-14.
19) Jumper F16-7 to F17-7.

PLACEMENT PROCEDURE
OR THE ACME POWER SUPPLY

Materials Reguired:

A. Tools

1-regular screwdriver, blade 1/4"
1-long nose pliers
1-1/4" nut driver - Xcelite R# 146
1-medium size phillips head screwdrive #1

B. Replacement Parts Required
1 Dual ACME - Power Supply 220 V, P/N 9011813-35

Procedure:

A. Turn the A.C. Power switch off and remove the line cord from the A.C. outlet.

B. Remove the four cabinet top screw fasteners. Close the tape drive access door and lift the cabinet top straight up, while grasping its bottom side edges and pulling slightly outwards.

C. Remove the two green ground wires, using the Phillips screwdriver.

D. Remove the four mounting screws, using the 1/4" nut driver.

E. If this is a Cogar power supply, having a silver colored case and 4 black fuse holders on its top, extract the 8 D.C. voltage wires from the D.C. terminal block. If this is an ACME Power Supply, marked' ACME Electric Corporation' on its top, disconnect the D.C. voltage connector from the power supply.

F. Tilt power supply, such that the A.C. input wires can be removed from the power supply. Extract the power supply from the system.

G. If the extracted power supply was the Cogar type, install the ACME power supply with the D.C. voltage wire cable attached to the power supply. Otherwise, remove the D.C. voltage wire cable from the ACME power supply and return it with the defective power supply.

H. Attach the A.C. wires to pins 2 and 5 on the A.C. terminal block of the ACMEpower supply.

I. After re-assembly adjust the D.C. voltages per the standard adjustment procedure for the ACME power supply.

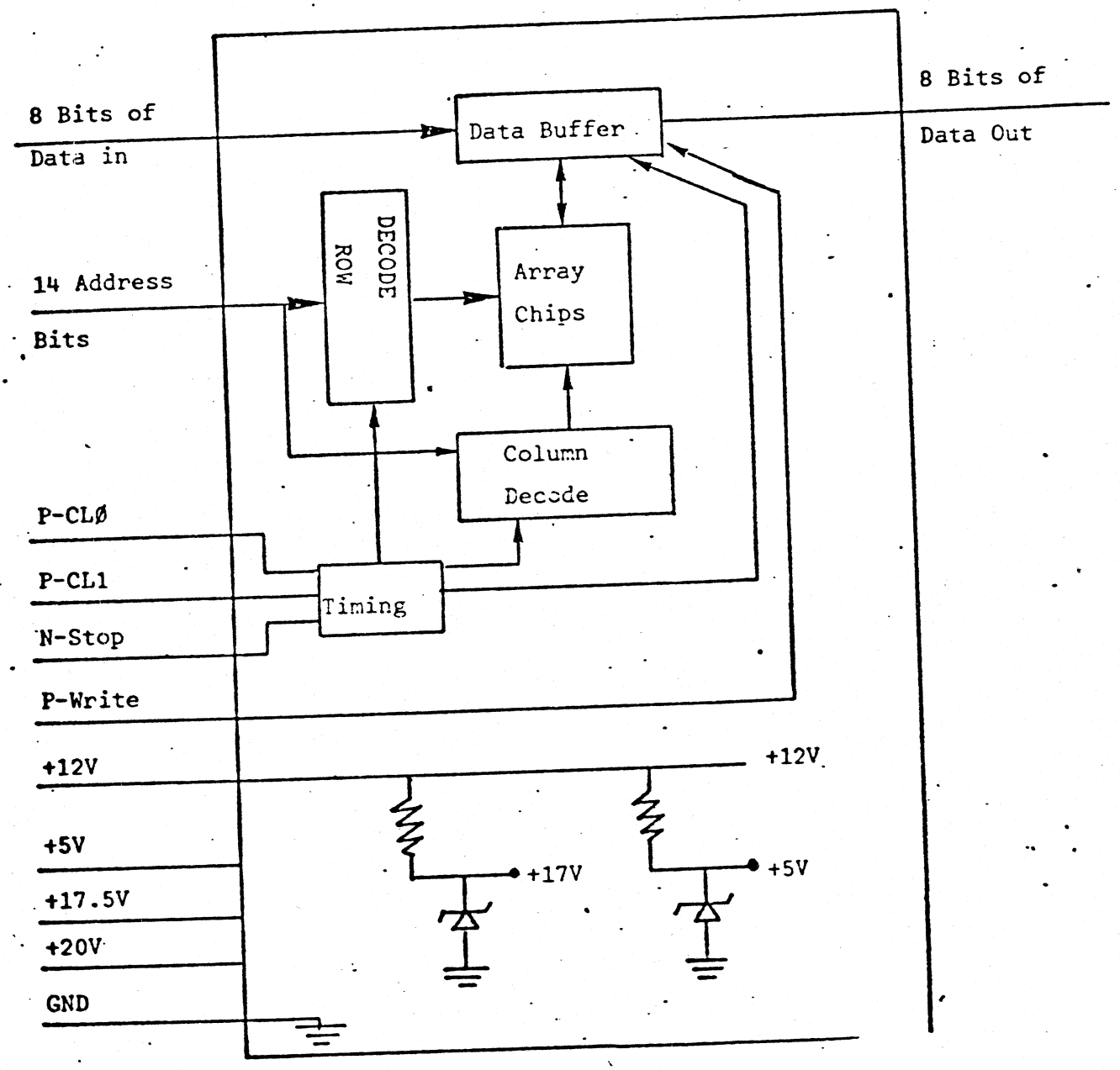
*Terminal Jumpers are different for different A.C. Voltages

Voltage	Jumper	AC input wires
90-110	1&2, 5&6	
104-129	2&3, 4&5	2-5
208-258	3&4	7=Ground

THEORY OF OPERATION OF THE MEMORY BOARD

The Memory Board may contain up to 8K by 1 bits of storage and electronic circuits necessary to provide appropriate timing pulses, address decoding, and input/output data buffers, which are TTl compatible logic levels.

MEMORY BOARD



e memory array chips (TMS 4062 JL) are high speed, dynamic random access elements. Their individual organization is 1024 bits X1. The memory system design allows them to be interconnected to provide a total capability of 8192 bits X 8 bits. This is accomplished by the design of the addressing matrix.

Each bit is stored in the array in a four transistor cell. During a read operation, the cell is internally gated to a pair of output lines on the chip. A "1" bit, or a "0" bit appears as a voltage difference which is detected (75370) by sensing a differential current. During a write operation, the same pair of lines are used to force the state of the memory cell.

For the lowest memory size configuration, 1K x 1 bits, row A on the memory board would have all 8 array chips present. Refer to the enclosed memory board illustration. For a memory of 2K x 1 bits, both rows A and B would have all 8 array chips. This pattern follows for all eight possible memory sizes.

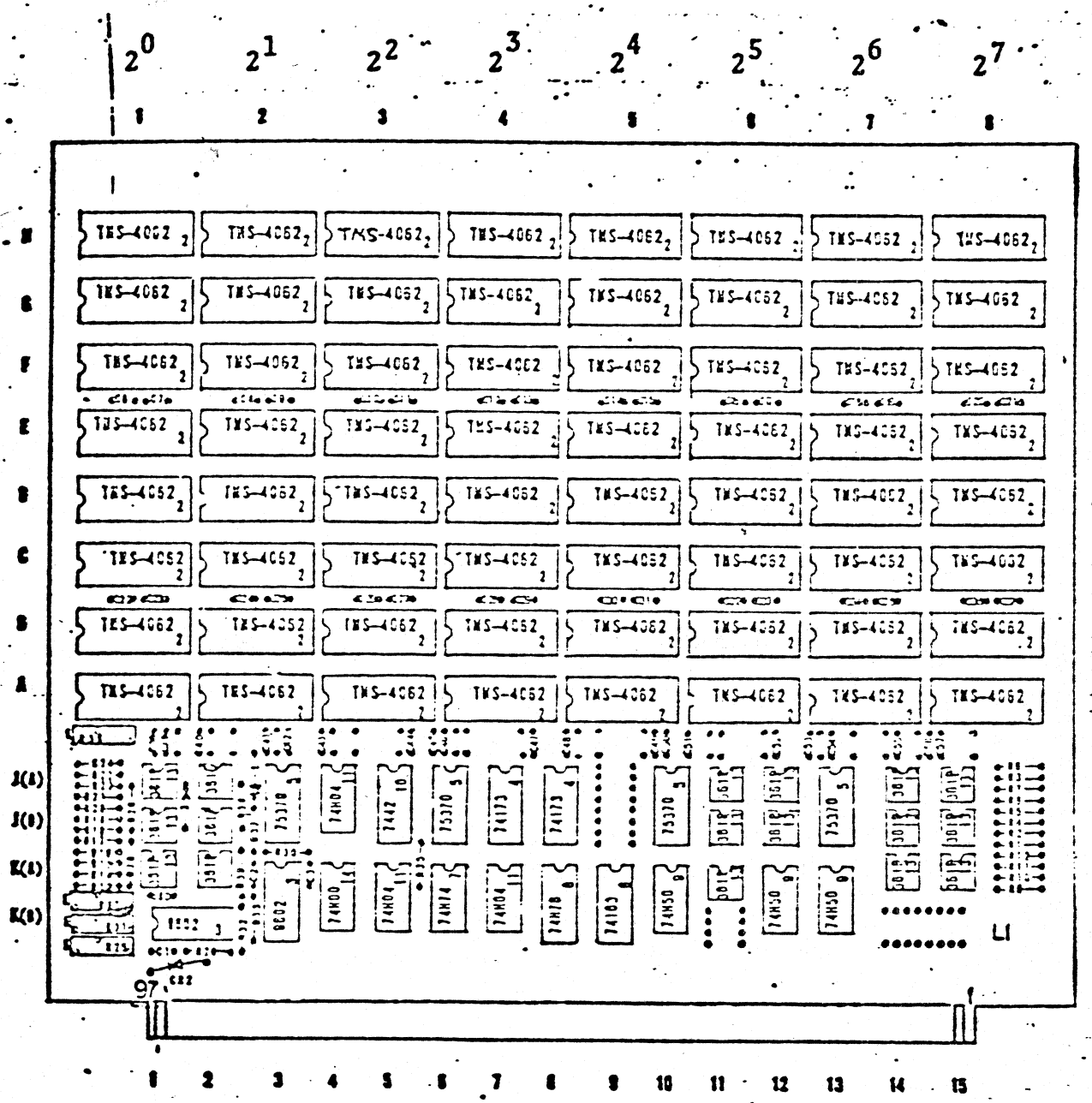
The Read Sensors/Write Drivers perform the dual function of differential current sensing during read,and voltage switching during write. The mode is selected by the signal "write".

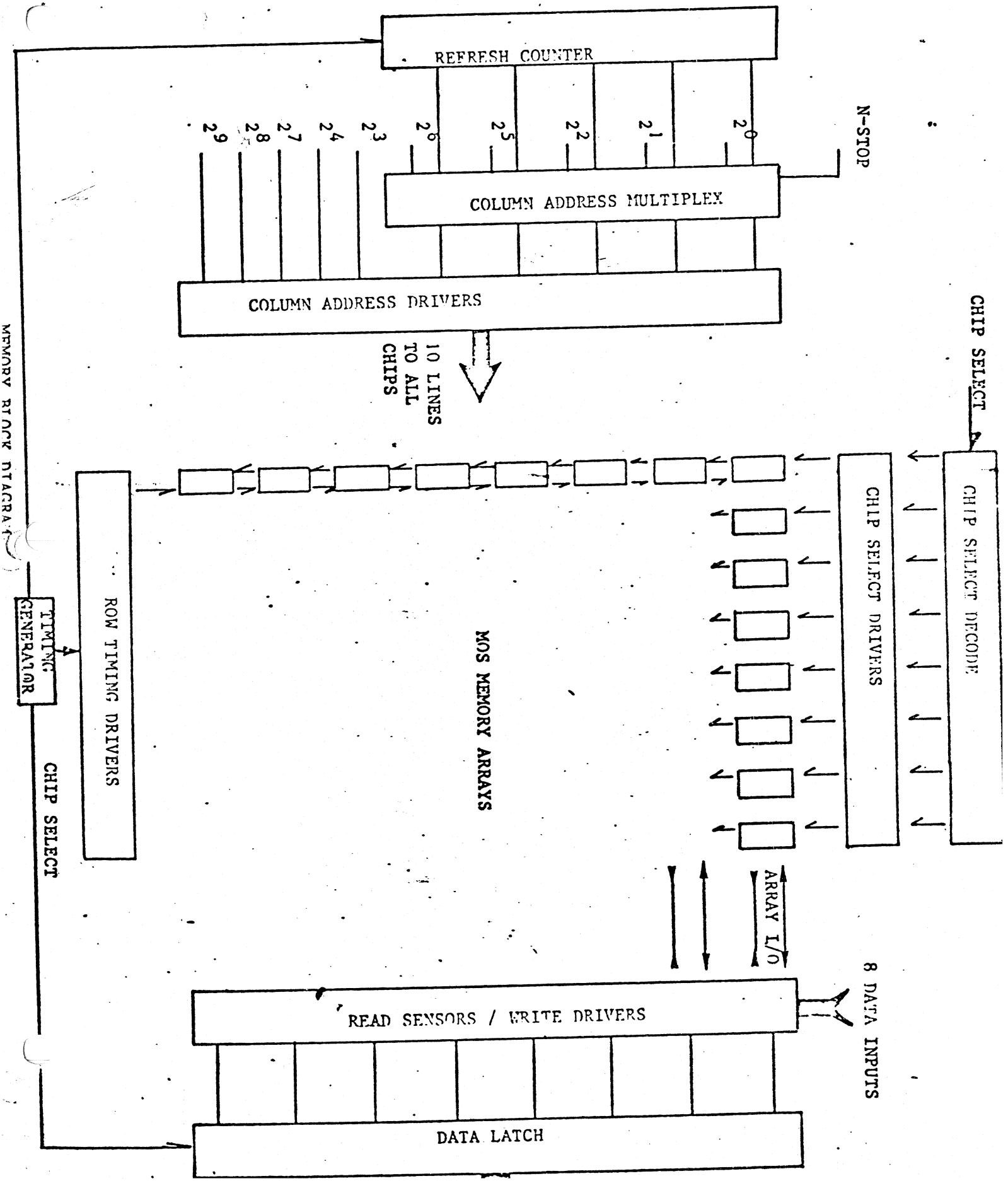
The Data latch simply captures the data from the sense amplifiers at the end of the read cycle. It is disabled during the write operation and when a memory address outside the range of the 8K PC is addressed. This is accomplished by the 2^{13} address line.

refresh counter is provided in the assembly. It is only used when a maintenance console is attached to the processor, and the console is in a cycle mode. The signal that controls this is "stop. Normal refresh is provided by other PC assemblies.

The timing generator establishes all clocked required for operation, and derives this timing from signals produced in the processor clock.

MEMORY BOARD ILLUSTRATION




REFRESH COUNTER
2^9 2^8 2^7 2^4 2^3 2^6 2^5 2^2 2^1 2^0
N-STOP
COLUMN ADDRESS MULTIPLEX
COLUMN ADDRESS DRIVERS
10 LINES TO ALL CHIPS
CHIP SELECT
CHIP SELECT DECODE
CHIP SELECT DRIVERS
MOS MEMORY ARRAYS
ROW TIMING DRIVERS
TIMING GENERATOR
CHIP SELECT
ARRAY I/O
8 DATA INPUTS
READ SENSORS / WRITE DRIVERS
DATA LATCH
MEMORY BLOCK DIAGRAM

MEMORY TIMING

The memory timing is developed on the board using one shots which are triggered by P-CL0 and P-CL1 from the processor board. Four variable resistors on the memory board are used to adjust the memory timing signals, for which an adjustment procedure is given on the appendix. The three timing signals created are:

N-Reset, used to pre-condition the row and column decode circuits within each memory array chip to accept a new address.

N-Clock, used to dump the '1' or '0' state of the selected bit position, and used to refresh (strengthen) the stored level.

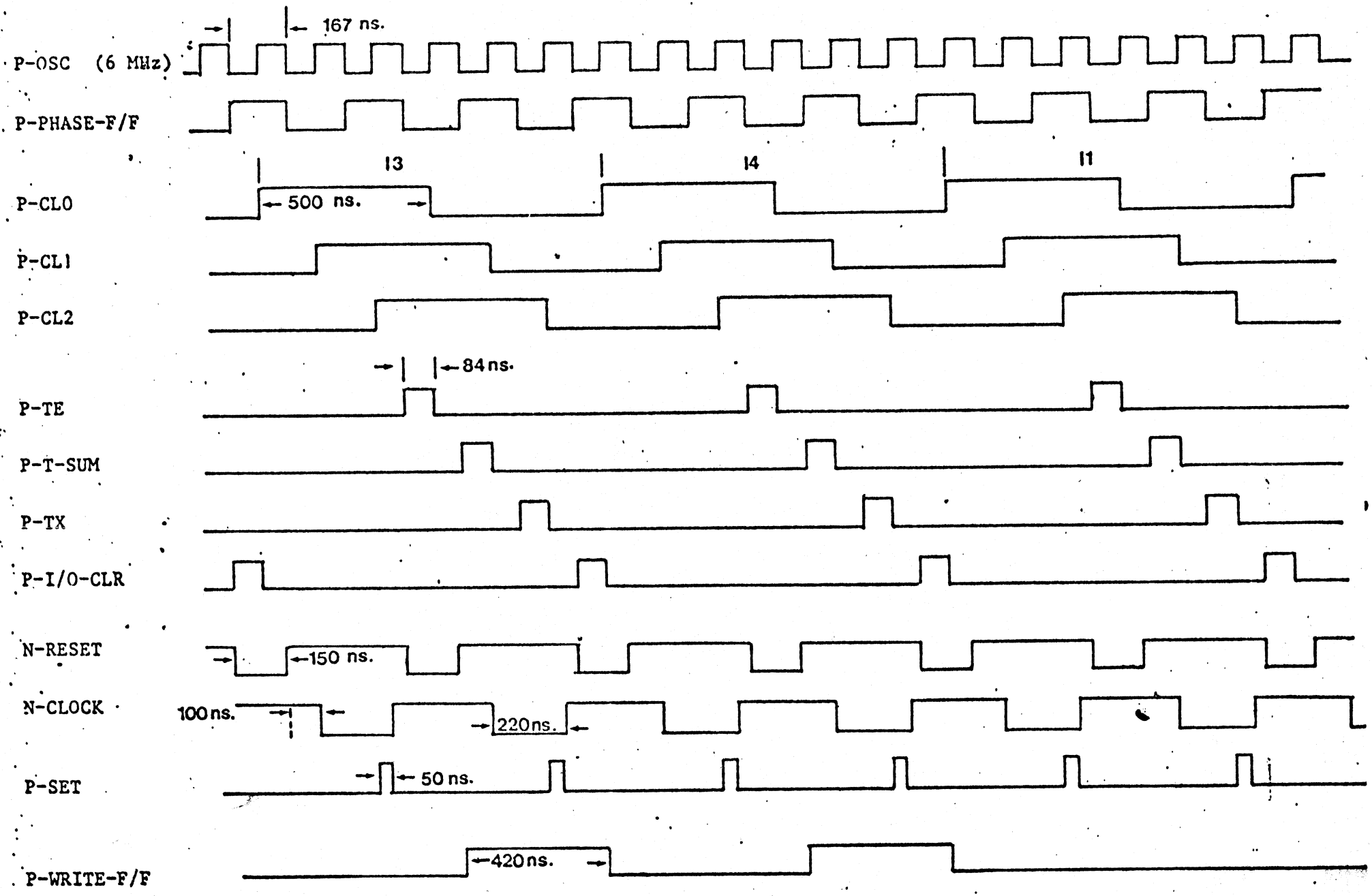
P-Set, used to load the data output of the memory into a storage register (Data Latch).

Signal N-Reset is developed at K2 pin 6* and feeds directly through the TTL to MOS drivers (SN75361A) into the memory chips. The output of the drivers swing between +17.5v to GND.

Signal N-Clock is developed at K3 pin 7 and, also feeds directly through the TTL to MOS drivers (SN75361A) into the memory chips.

Signal P-Set is developed at K3 pin 9 and is derived from signals N-Reset and N-Clock. P-Set allows a parallel load into the Output Data Latches, J7 and J8.

* All Component Locations are given on T.I.Memory Schematic, 007-002244-002.



PROCESSOR TIMING

MEMORY ARRAY OPERATION

Description

The TMS 4062 JC is a high-speed, 1024-word by 1-bit, dynamic random-access memory, fabricated through P-channel, metal-gate MOS processing. The devices are designed for use in low-cost, high-performance memory applications.

High performance at low power dissipation is achieved with a four transistor storage cell and unique support circuitry. Low-capacitance inputs minimize driver-circuit power requirements, simpify TTL-to-MOS conversion, and reduce over all system costs.

The memory is fully decoded and its differential outputs can be wired OR. The Chip-Select input allows the selection of individual components in arrays with greater than 1K words.

Information stored in the memory is nondestructively read, but since the memory is dynamic it must be refreshed periodically. Refreshing of the total memory requires 32 cycles every 2 milliseconds. The chip need not be selected during refresh.

The TMS 4062 JC is a 22 pin, hermetically sealed, ceramic dual-in-line package.

Operation

The storage element in the TMS 4062 JC is the four-transistor cell shown in Figure 1. The transistors connected at A and B are not part of the cell, they are within the 75370 chips. Actual operation of the cell is straightforward. It is selected by taking the clock input low and is a dc stable flip-flop at that time. When the clock is high the cell does not conduct and information is stored on one of the parasitic capacitors C_1 and C_2.

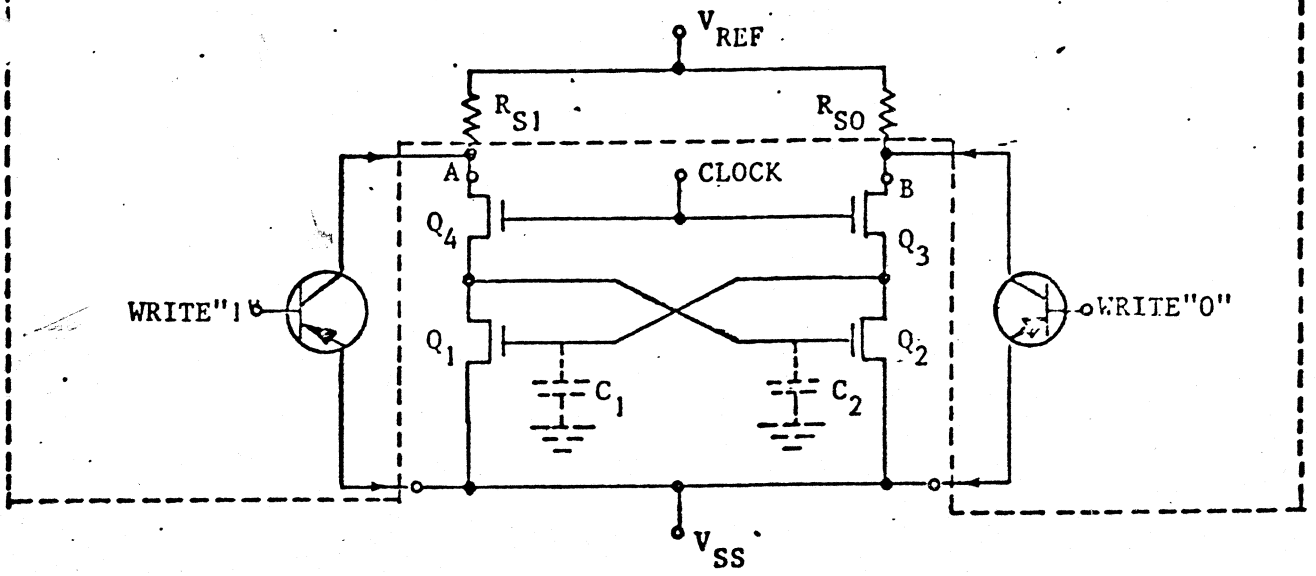
Writing data in the cell is simply executed a pair of switches such as the transistor attached at A and B. These transistors are within the 75370 chips. If the wire 1 transistor is turned on, it will force A to close to V_{SS}. This shuts off any conduction that may have been occuring in Q_2. At the same time the capacitor, C_1, will be charged and Q_1 will be charged and Q_1 will begin to conduct current. When the cell is selected for a subsequent Read operation, current will exist in the Q_1, Q_4, and R_{S1} side of the cell, and a differential amplifier between A and B would sense the voltage difference and detect the presence of a High state.

To understand how the cell is integrated into a 1024 array, consider the block diagram in Figure 2. The Reset input when in the Low state performs two functions, which are: 1) to precharge the device and 2) to turn off all the address inverters. On the TMS 4062 the address inputs are the drain of an MOS device and because they are off during the reset and clock periods, very low input capacitances are seen.

After the Reset input is taken High, there is a period required for the row and column decoders to function. This is the TDD time in the timing diagrams. The clock and chip-select periods occur next, with the clock input gating the row decoder while the chip-select input enables the column decoders. Information from the selected cell is then transferred to the I/O lines, which are also gated by the chip select input via FET switches. After the output data has been sensed, the clock and chip select are returned to the positive state and the device is ready for the next cycle.

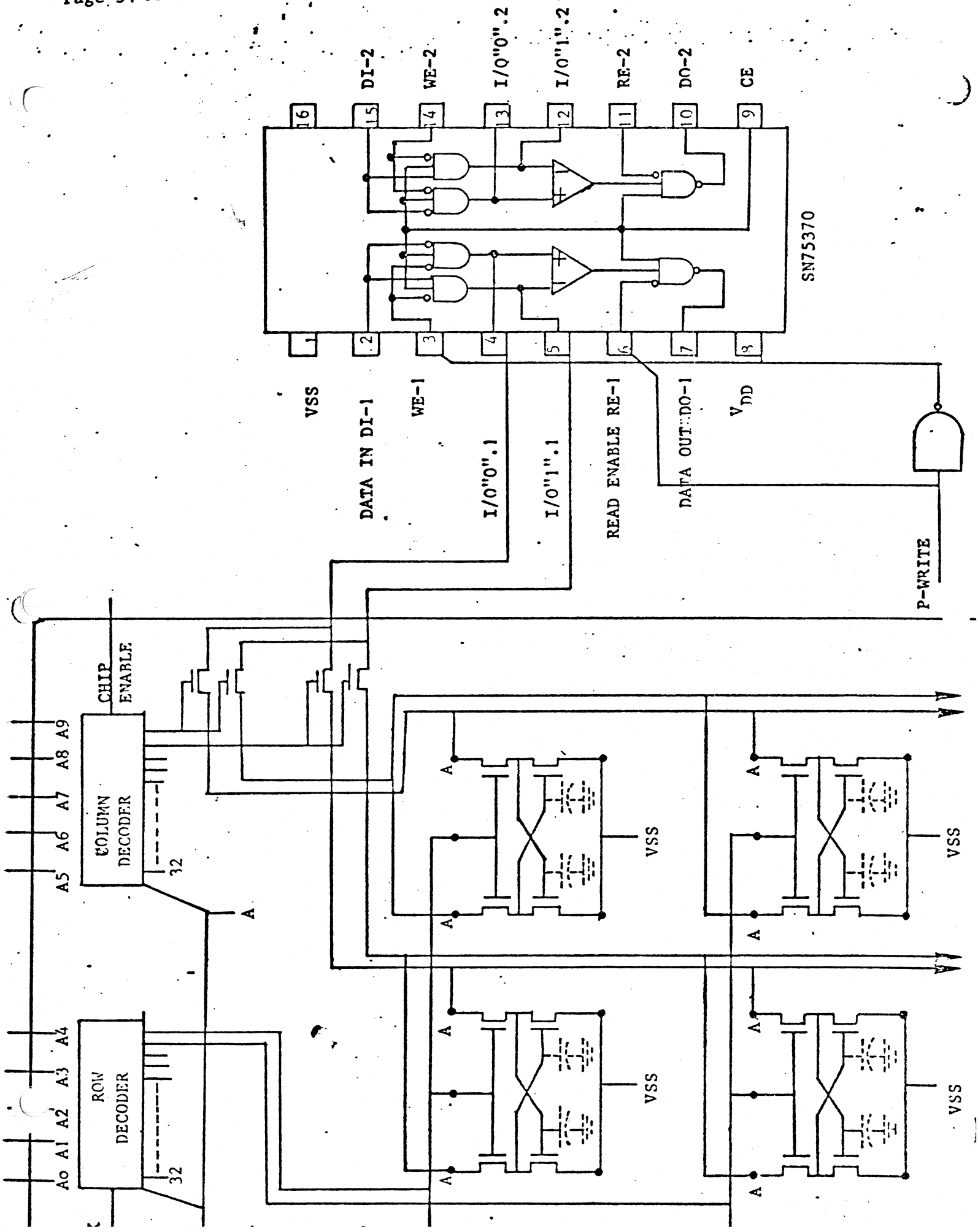
In the TMS 4062 the row-decode outputs is tied to the clock input of each cell. Thus any time a row is selected, all 32 cells are in a stable state. This selection will refresh those 32 cells, regardless of the state of the chip-select input. To refresh the 1024 bits, all32 rows must be selected. This is accomplished by exercising all 32 combinations of the A_0, A_1, A_2 addresses. Clock must be exercised to refresh-chip se-

Components within I.C. SN75370



One Bit Cell in
TMS 4062JL

Points A and B are gated to the Read Sensor/Write Driver (SN75370) only when its column position is selected.
Points A and B are pré-charged by the reset signal (not shown) to enable a refresh with the next clock. Thus refreshing is possible without VRef from the SN75370.


DI-2
WE-2
I/O"0".2
I/O"1".2
RE-2
DO-2
CE
16
15
14
13
12
11
10
9
SN75370
1
2
3
4
5
6
7
8
VSS
DATA IN DI-1
WE-1
I/O"0".1
I/O"1".1
READ ENABLE RE-1
DATA OUT DO-1
V_{DD}
P-WRITE
CHIP ENABLE
A9
A8
A7
A6
A5
COLUMN DECODER
32
A4
A3
A2
A1
A0
ROW DECODER
32
A
VSS

ADJUSTMENT PROCEDURE FOR THE ACME POWER SUPPLY (T.I. MEMORY)

Materials Required:

A. Tools

1-regular screwdriver, blade 1/4

B. Replacement Parts Required

1-Voltage meter, Simpson Model 260 or equivalent

Procedure:

A. Turn the A.C. Power Switch off.

B. Remove the four cabinet top screw fasteners. Close the tape drive access door and lift the cabinet top straight up, while grasping its bottom side edges and pulling slightly outwards.

C. Refer to attached drawing. Verify that the terminal block (TB2) connections are as shown in the drawing. Turn the system on and allow 15 minutes of warm up before making any adjustments.

D. All D.C. voltage measurements will be made at the D.C. terminal block behind the CRT unit. The voltage levels should be as follows:

T.B. Ref	Wire Color	Setting
+12	Red	+12.0V
-12	White/Red	-12.0V
+5	Orange	+5.1V
+10	Yellow	+17.5V
-7	White/Yellow	+20.0V

E. Set R10 (the +17.5V fine adjustment) in the midpoint of its swing Adjust R11 (the +17.5V course adjustment) until the voltage is approximately +17.5v at the D.C. terminal block. Adjust R10 until the voltag is exactly +17.5.

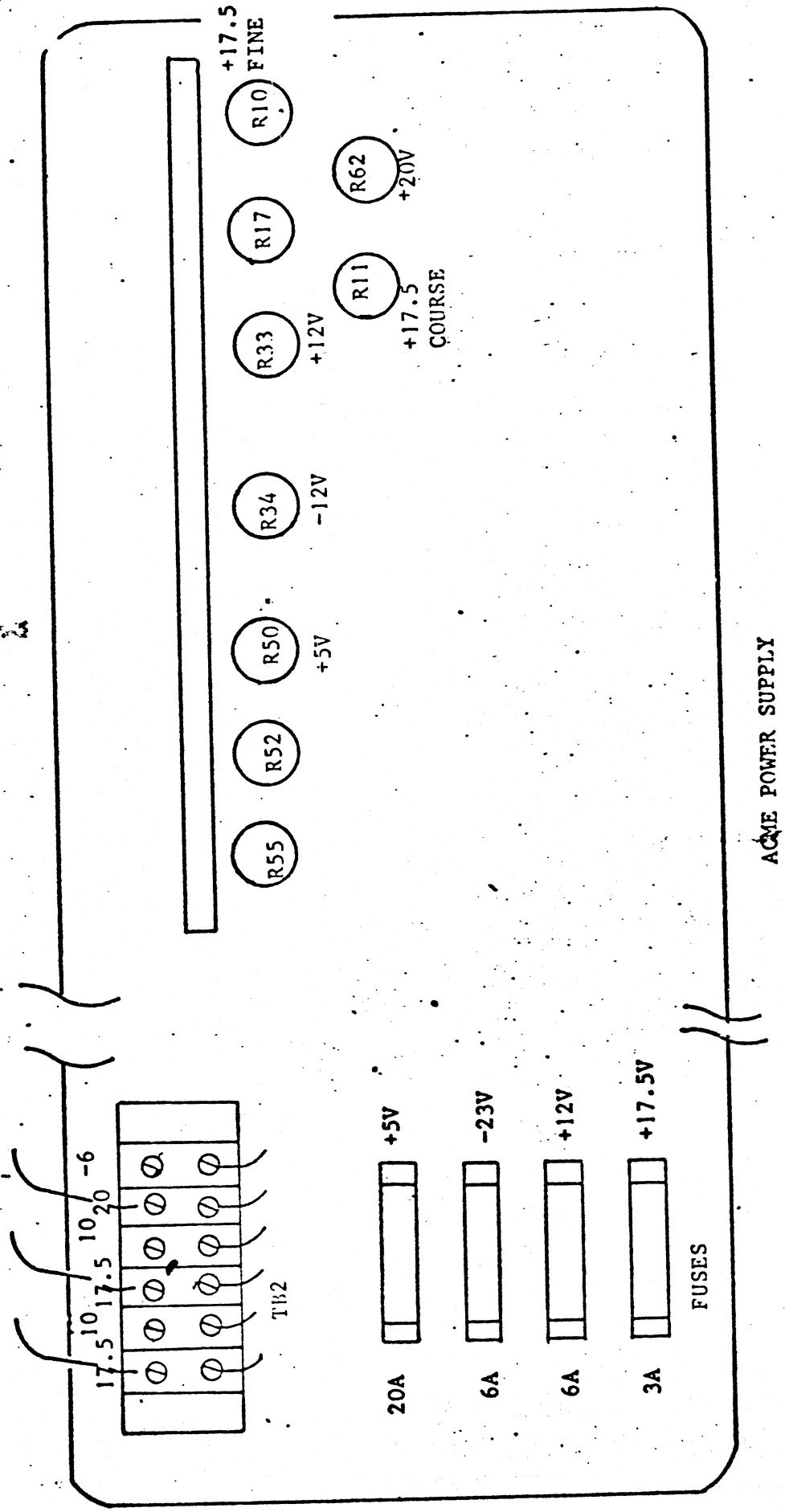
F. Adjust R62 to obtain +20.0 volts at the terminal block. (T.B.)

G. Adjust R50 to obtain +5.1 volts at the T.B.

H. Adjust R33 to obtain +12.0 volts at the T.B.

I. Adjust R34 to obtain -12.0 volts at the T.B.

J. Turn the A.C. Power Switch off. Put the system cabinet top onto the system and install the cabinet screws.


+17.5 FINE
R10
R62
+20V
R17
R11
+17.5 COURSE
R33
+12V
R34
-12V
R50
+5V
R52
R55
ACME POWER SUPPLY
-6
20
10
17.5
10
17.5
TB2
+5V
-23V
+12V
+17.5V
20A
6A
6A
3A
FUSES

ACME POWER SUPPLY CONVERSION

A. Replacing TI Memory with COGAR Memory

1. Move Power Supply Terminal Board No. 2 (TB2) leads from +17.5 to +10V (2 places) and from +20V to -6V positions. This is explained by moving the wires of the terminal board up one position. This is on the tape deck side of the power supply; TB2-1 to 2, TB2-3 to 4 and TB2-5 to 6.

2. Add jumper buss wires across R7, R13 and R14 on the P.C. card Assembly. These are located below the R33 adjustment pot.

3. Reset the +10 Volt output with pots R10 and R11. Set R10 to mid-range and adjust the output using R11. This is to allow the R10 pot to be used for the fine adjustment in the future.

4. Reset the +10 Volt over voltage with pot R17. The +10V over voltage should be set to 10.8 Volts.

5. Reset the -6 Volt output with pot R55.

B. Replacing COGAR Memory with TI Memory

1. Move TB2 leads from +10V to 17.5V (2 places) and from -6V to +20V positions. This is explained by moving TB2-2 to TB2-1, TB2-4 to TB2-3, and TB2-6 to TB2-5.

2. Remove jumpers across R7, R13, and R14 on the P.C. card assembly. These are located below the R33 adjustment pot.

3. Reset the +17.5V output with pots R10 and R11. Set R10 to mid-range and adjust the output using R11. This is to allow the R10 pot to be used for the fine adjustment in the future.

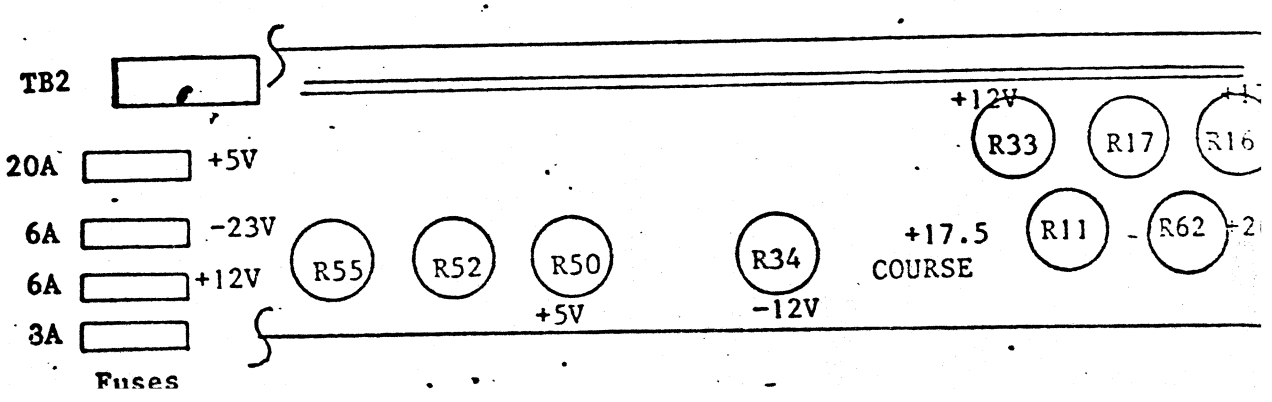
4. Reset the 17.5V over voltage with pot R17. The +17.5V over voltage should be set to 19 volts.

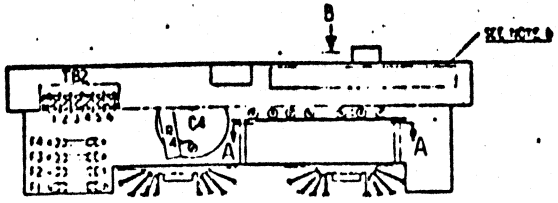
5. Reset the +20 volt output using pot R62.

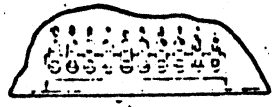
C. Notes

1. ACME supplies are normally shipped from the factory with a TI memory and adjusted as in paragraph B.

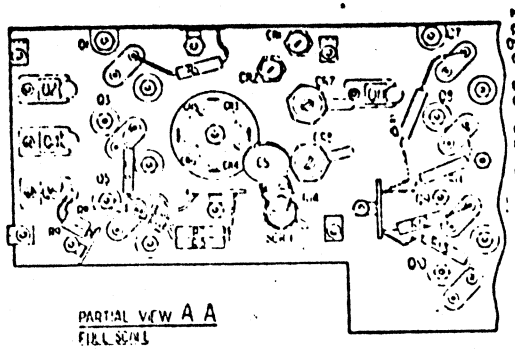
2. Top view of ACME power supply showing pot location:



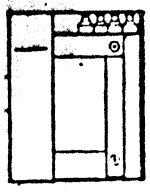


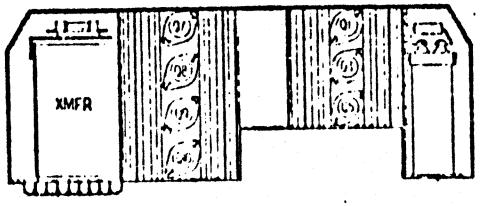


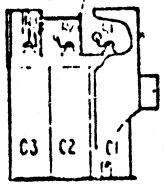
PARTIAL VIEW A A
FULL SCALE

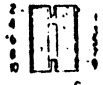


PARTIAL VIEW A A
FULL SCALE

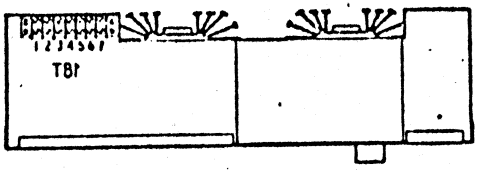


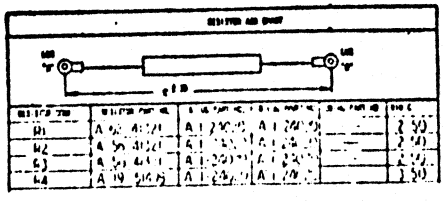




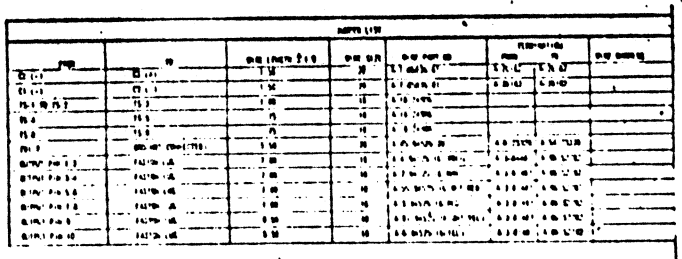


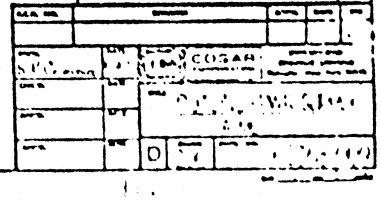
VIEW C
FULL SCALE

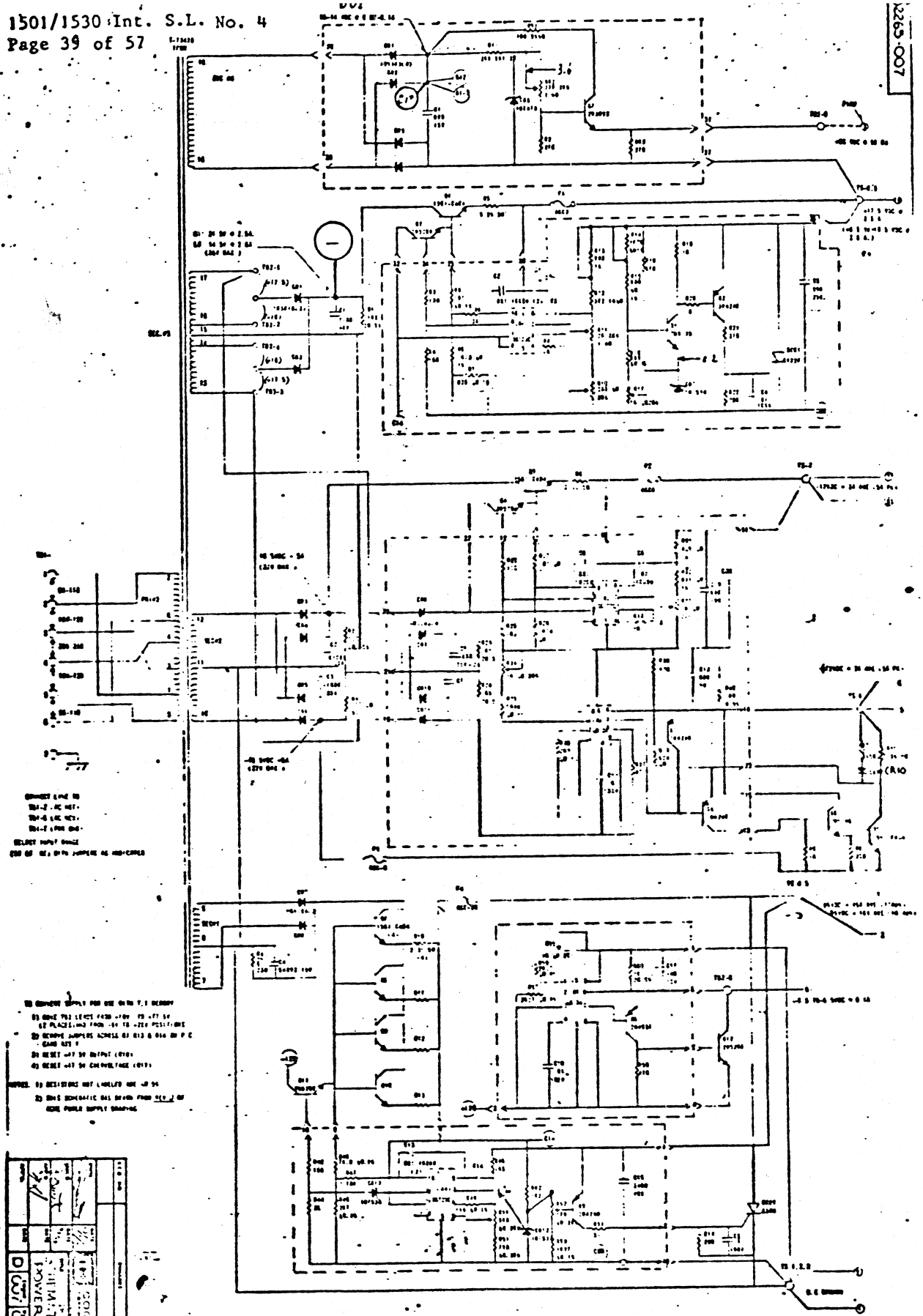




MAGNETIC CONNECTION	
LEAD	TERMINATION
(S1) P1S	TB1-5
(S1) P1F	TB1-3
(S1) P2S	TB1-4
(S1) P2F	TB1-2



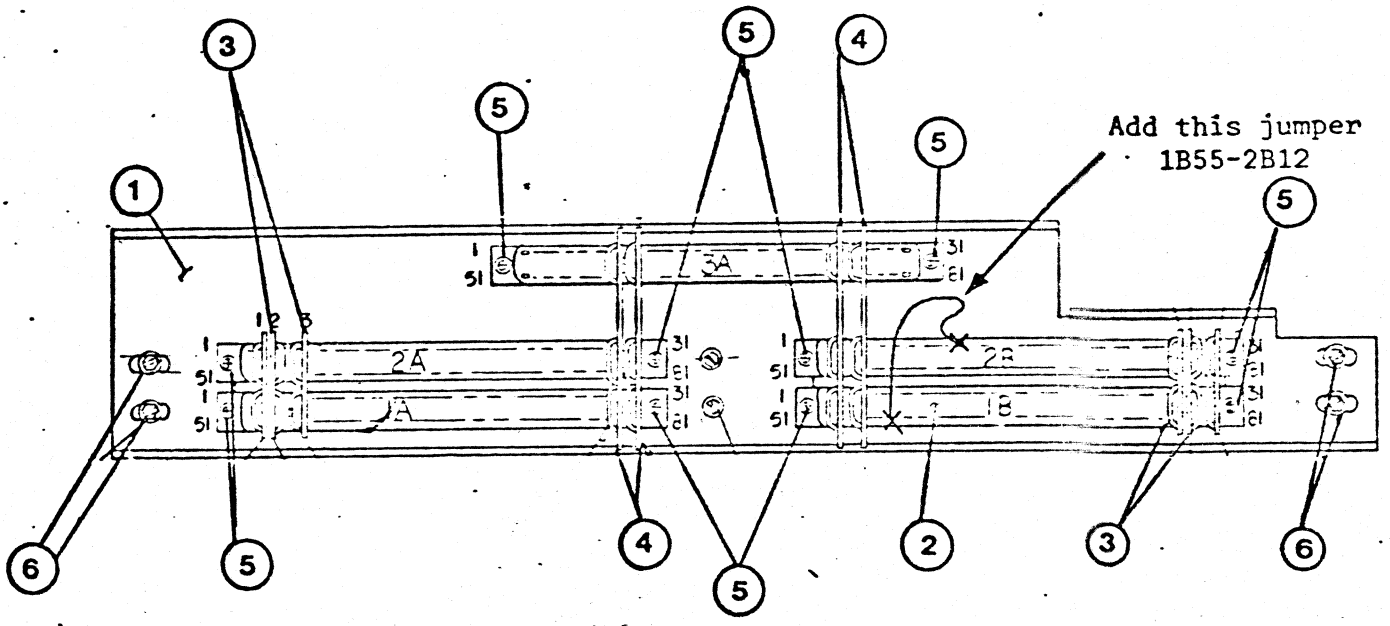




D	007	002265-007	SCHEMATIC - ACME POWER SUPPLY

DRAWING 29

WIRED MODULE



(7) YELLOW WIRE-WRAPPED WIRE

If Rev.8 TC1
Rev.9 Processor

T.I. MEMORY SET-UP PROCEDURE

Voltages are to be adjusted to nominal values at the Array Chip as follows:

V_{SS} (Pin 2)	=	17.5 V	
V_{SX} (Pin 1)	=	20.0 V	
V_{REF} (Pin 9)	=	7.5 V	(Not Adjustable)
V_{DD} (Pin 21)	=	0 V	(Not Adjustable)

Nominal listed values for VSS and VSX are recommended by the manufacturers, and for best memory performance, should be adhered to. At VSX max and VSS min, reliability is very bad. Otherwise, through-out the limit spread, all memories should run.

Voltage Limits

VSX			VSS		
MAX	NOM	MIN	MAX	NOM	MIN
22	20	18	20	17.5	17

Using a 50 MHz or better Dual Trace Oscilloscope, the timing pulses should be set s follows at the 50% point:

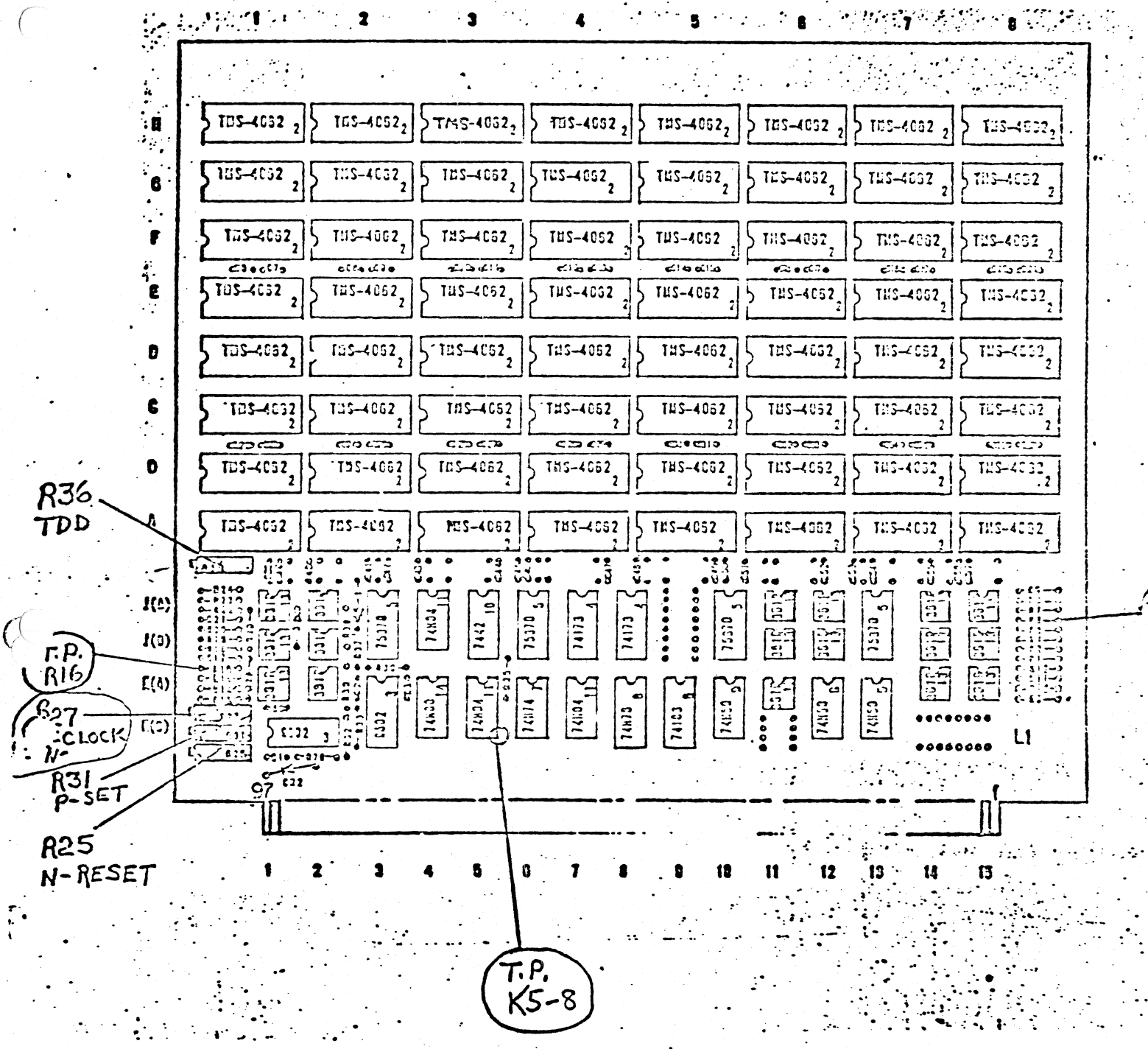
Attach Probe "A" to either end of R8. Sync on N-Reset and adjust R25 for a pulse width of 150 nsec. Set time base at 100 nsec.:Div.

Attach Probe "B" to R16 (N-CLOCK). Put time base on 100 nsec./ Div. and adjust R36 for a 100 nsec. delay (TTD) between the + Going Edge of N-RESET and the - Going of N-CLOCK.

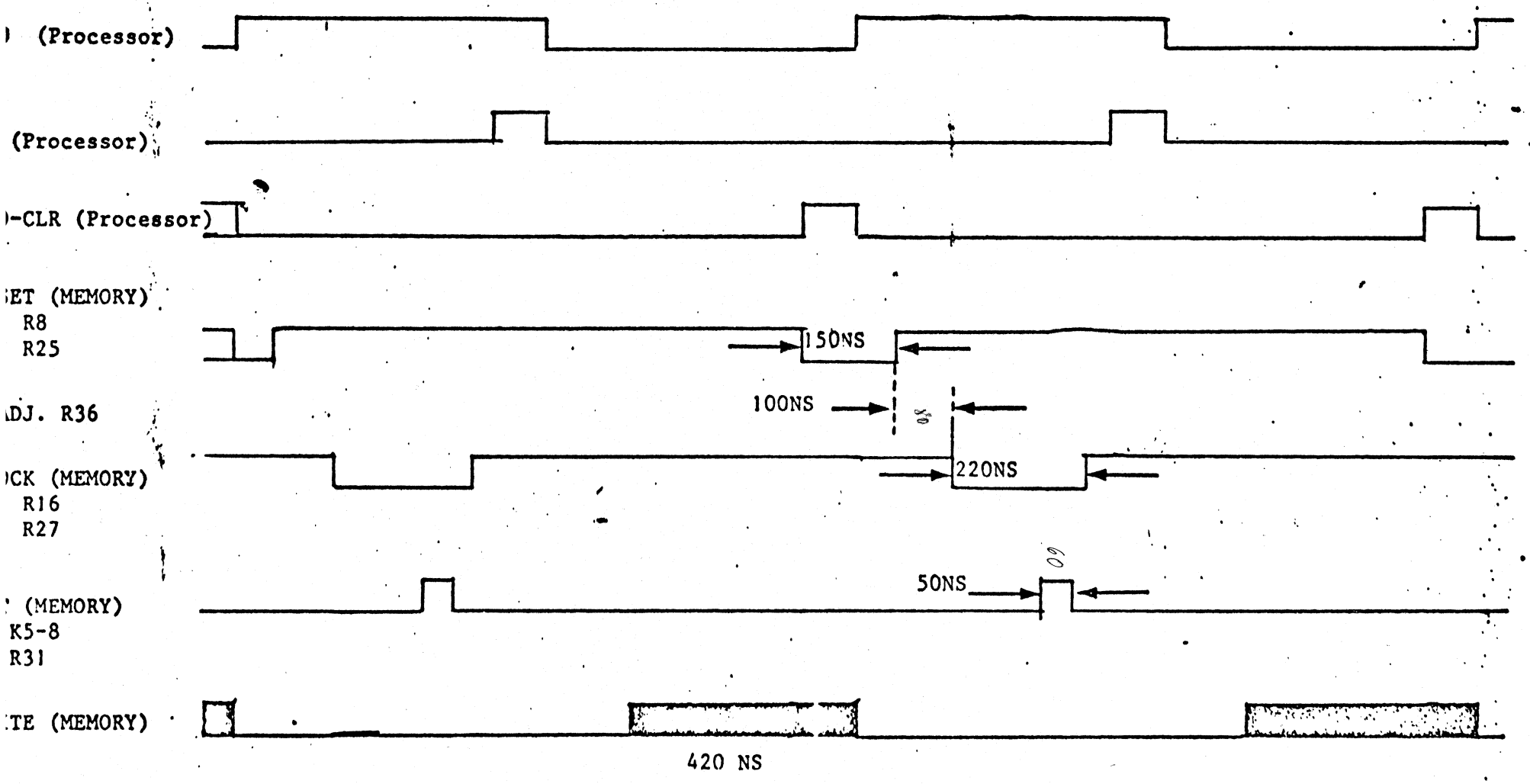
Adjust R27 for an N-CLOCK Pulse width of 210 nsec.

Attach Probe "B" to K5-8 (P-SET). Adjust R31 for a Pulse Width of 50 nsec.

T.I. MEMORY BOARD (REVI)



T.I. MEMORY TIMING



TP-1780FN

Dec.14,1973		5

SUBJECT: 1501 Field Repair of Cogar Power Supply.

SYMPTOM: This procedure will be followed when any or all of the following Power Supply symptoms occur:

1. All outputs are low
2. Adjusting pots does not increase output voltage
3. Q15 and Q16 are 2N6123 or when other troubles occur in the power supply and Q15 and Q16 are noted to be of the 2N6123 type.

MACHINES AFFECTED: All 1501's with Cogar Power Supply.

INSTRUCTIONS: To replace Q15 and Q16 which were found to be frequently defective in the power supply. If Q15 and Q16 are of the 2B6123 type, they should be replaced with MJE4923. (SBM P/N 9012094-37).

With the cover off of the System, Q15 and Q16 can be checked without removing the cover from the power supply. Lift the lower edge of the cover about 1/2" (at the end of the power supply which has the blue or red wired A.C. voltage selector plug). The transistor at the bottom of P.C. Board is Q16 (See Figure 1). If this transistor is black in colour, smaller than the MJE4923, and the screw that holds it in place does not pass through the transistor, it is of the 2N6123 type and should be replaced.

A. Remove the power supply from the System following the standard procedure for its replacement.

B. Remove the power supply cover using a small Phillips screwdriver and a 1/4" nut driver.

C. Q15 and Q16 are located on the primary board in the lower right hand corner of the power supply. (See Item A and B on Figure 2).

D. Remove the primary board from the power supply by using a medium Phillips screwdriver to remove the screws (Item C and D) in upper left and right corners of board.

E. Next remove the plastic screw (Item E) from the primary board. Note that there is a paper card used to insulate the back of the primary board, and that a plastic washer is inserted between the mounting post and the paper card.

F. Next remove the plug-in connector (Item F) from the primary board

G. Remove Q15 and Q16 from the primary board (Items A and B), by first clipping the leads, and removing the securing screws and nuts. After removing Q15 and Q16, heat and remove the transistor leads.

H. Remove the solder from the lead holes and discard the old mounting hardware.

I. Apply heatsink compoung (approximately 1/32 inch thick) on the back of the MJE4923's and mount them on board, using the supplied hardware and solder (Figure 1).

NOTE: When securing the new Q15 and Q16, the bottom of the transistors should be uniformly flat against the compound and surface of the primary board, to facilitate good thermo conductivity.

J. Re-assemble by following these procedures in the reverse order, starting at Procedure F.

Parts Required: Cogar P/N 057-000776-013.
Singer P/N 9012094-37.

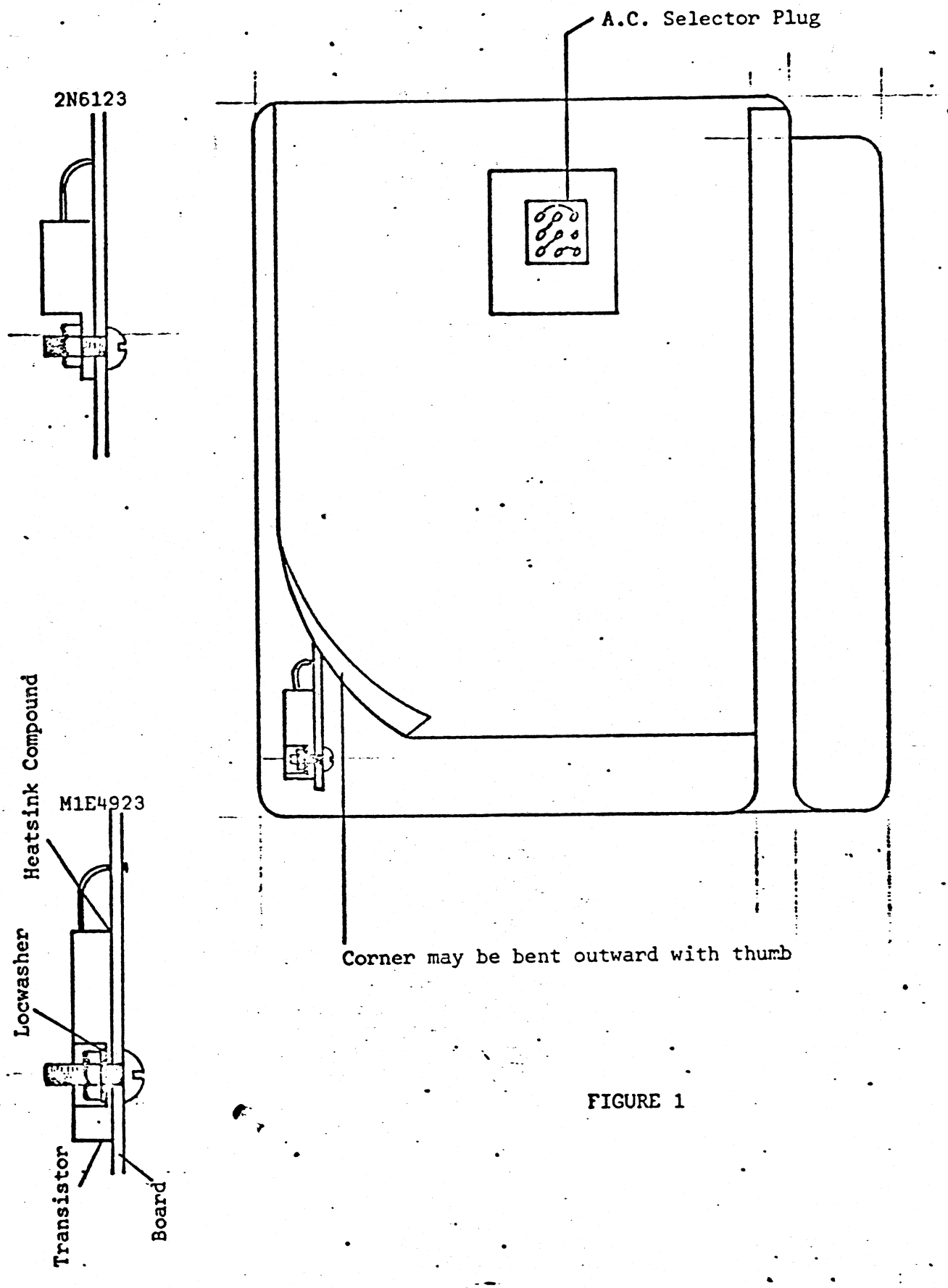

A.C. Selector Plug
2N6123
Heatsink Compound
M1E4923
Locwasher
Transistor
Board
Corner may be bent outward with thumb

FIGURE 1

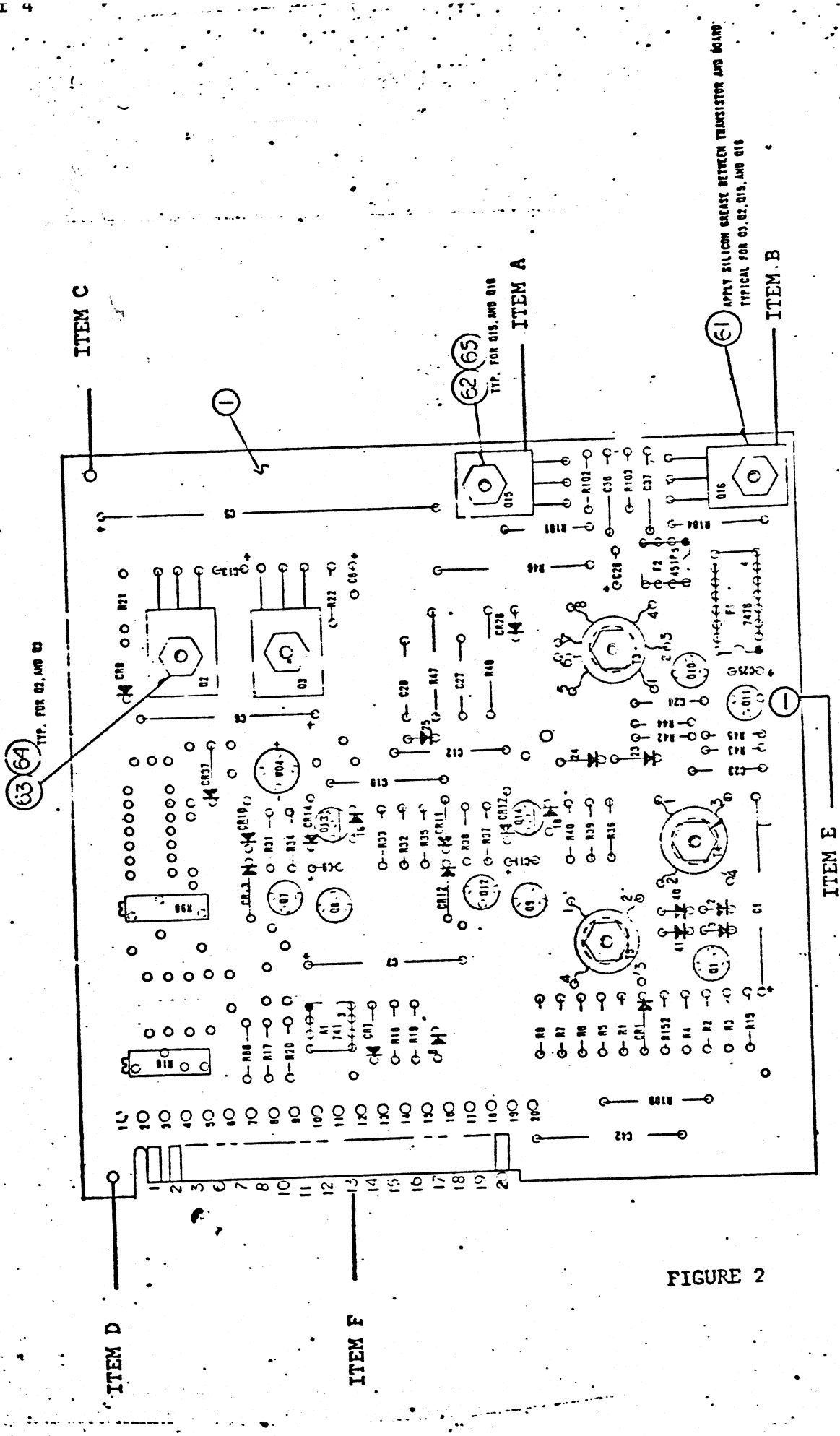

ITEM C
ITEM A
ITEM B
ITEM D
ITEM F
ITEM E
APPLY SILICON GREASE BETWEEN TRANSISTOR AND BOARD TYPICAL FOR Q3, Q2, Q15, AND Q16
TYP. FOR Q15, AND Q16
TYP. FOR Q2, AND Q3
NOTES. 1) FIND NUMBERS FOR EACH IC ARE LOCATED ON THE IC IN THE LOWER RIGHT HAND SIDE.
2) ALL OTHER FIND NUMBERS ARE SHOWN ON THE LIST AT THE RIGHT.

FIGURE 2

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1501/1530

TP-1780FN

Dec.14,1973		6

SUBJECT: New Adjustment Cogar Memory Timing.

MACHINES AFFECTED: All 1501's with Cogar Memory.

ACTION REQUIRED: In case of problems perform new adjustment.

INFORMATION: For improved reliability of the Cogar Memory, a change in the memory timing is required. The clock width should now be set for 230 NS rather than 240 NS.
This adjustment change is only valid for the 240 NS boards.
How to identify the 210 NS and 240 NS boards is described in another Service Letter.

MEMORY ADJUSTMENT

The Processor PCBA shows the controls and test points on the Processor Card used for proper adjustment of the memory cycle time. These controls affect:

1. The leading edge of the CLOCK pulse, from which all other timing pulses are referenced.

2. The positioning of the leading edge of the SET pulse in relation to the CLOCK pulse.

3. The width of the SET pulse.

Positioning and width of the SET pulse in relation to the CLOCK pulse is critical, since the SET pulse generates: (a) a reset signal for the output latches, and (b) a strobe signal for entering new information into the output registers.

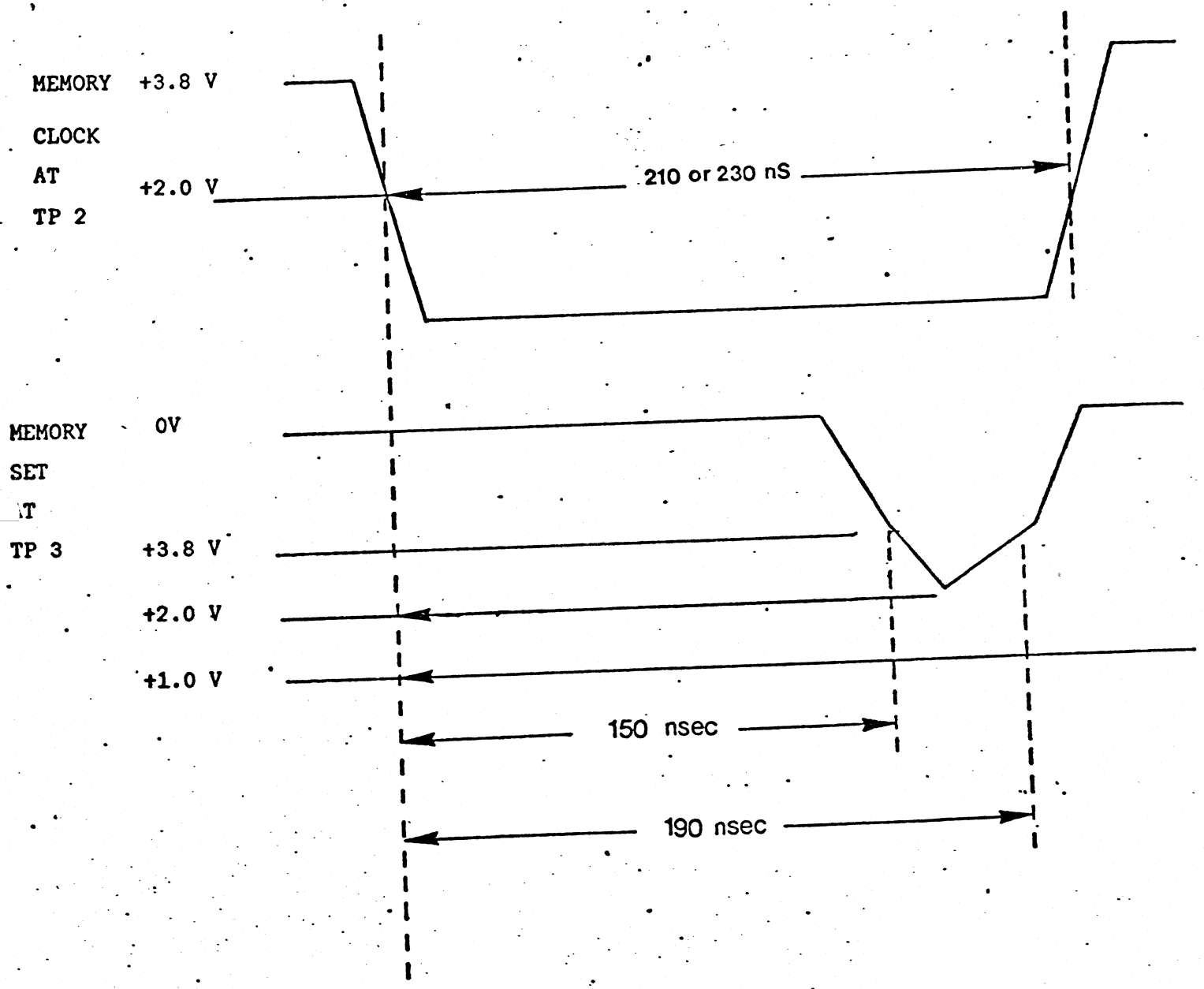
Access to the controls and test points on the Processor Card is accomplished by removing the card from the unit, placing the extender card in its location within the unit and mating the processor card to the extender card. Figure 1 is a timing diagram showing the timing of the CLOCK pulse and the SET pulse. Using the high impendance probes and Tektronix 453 (or equivalent) oscilloscope, proceed as follows to adjust the memory cycle:

1. Synchronize Channel A to TP2 on the processor board. With the Channel B probe at TP3, adjust R20 to obtain a negative-going clock pulse of the appropriate width.

2. Adjust R23 to position the leading edge of the Channel B SET pulse to occur 150 nsec after the occurance of the CLOCK (Channel A) pulse.

3. Adjust R25 to position the trailing edges of the CLOCK (Channel

MEMORY TIMING



TP-1780FN

Dec.14,1973		7

SUBJECT: 1501 Cogar Memory Identification

MACHINES AFFECTED: All 1500's with Cogar Memory

REASON: Information only

The Cogar Memory P.C. Boards are easily identified by the green square modules, with the name Cogar imprinted upon them, which are mounted upon the P.C. Board.

Three different memory capacities are possible; 4K, 8K, or 16K bytes.

A 16K memory must have 10 or 11 full columns, and the modules must be type 5300034. Refer to figure 1.

An 8K memory may have either:

A. 10 or 11 full columns, and the modules are not type 5300034. See figure 2.

B. 6 full columns and the modules are partly type 5300034. See figure 3.

A 4K memory may have two different array chip configurations, and may have two different memory timing requirements.

Array chip configurations:

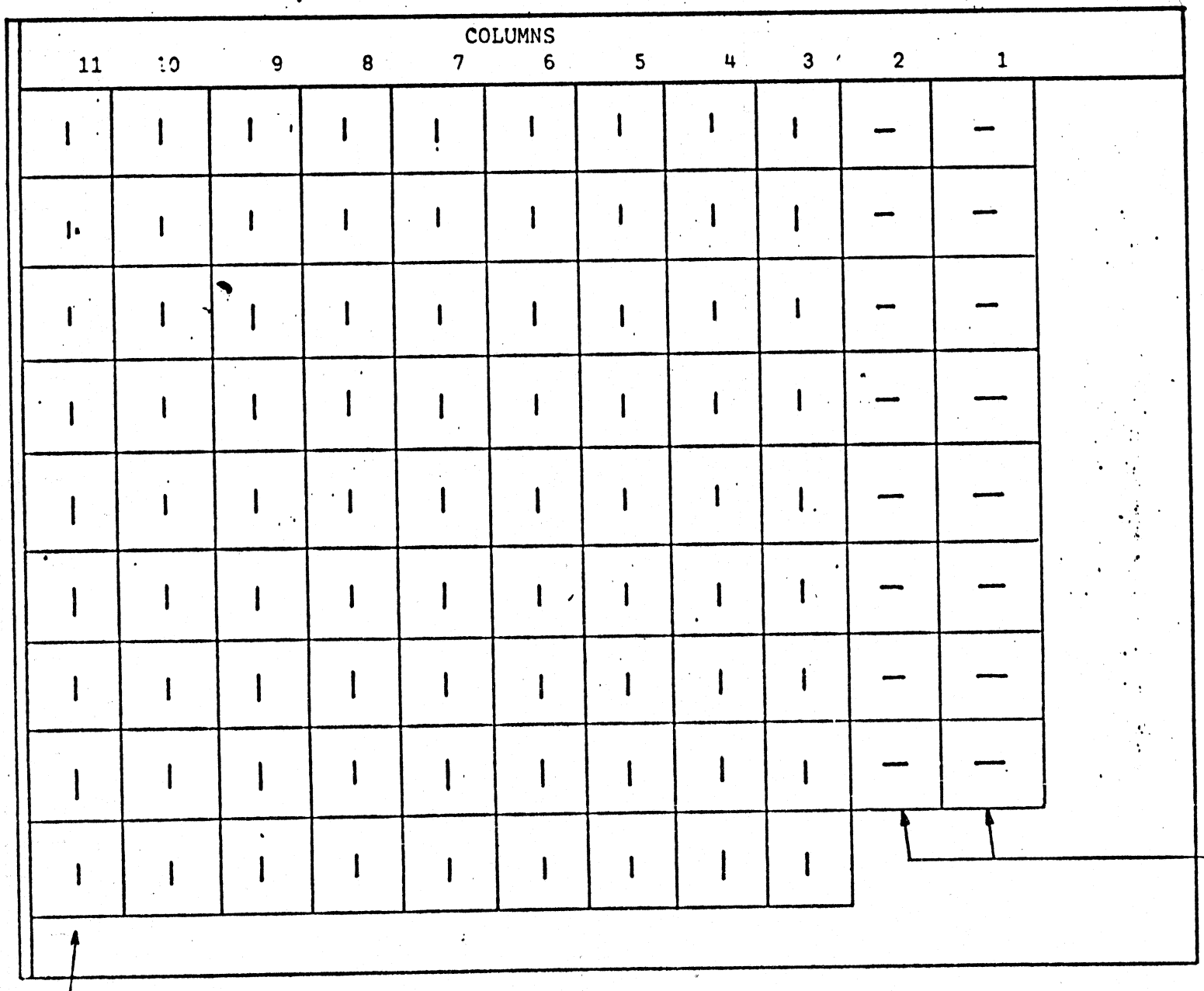
A. 6 full columns and the modules are not type 5300034. See figure 4.

B. 6 columns, with 5 modules, partly type 5300034. See figure 5.

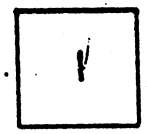
Different memory timing: Usually the memory clock timing requirement is shown with a tag on each memory. See figure 6. However, the timing requirement may be determined if a tag is not present by:

A. A 240 NS memory requires many more I.C.'s mounted. See Figure 6.

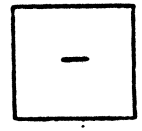
B. A 210 NS memory requires fewer I.C.'s mounted. See figure 5.



16 K
FIGURE 1



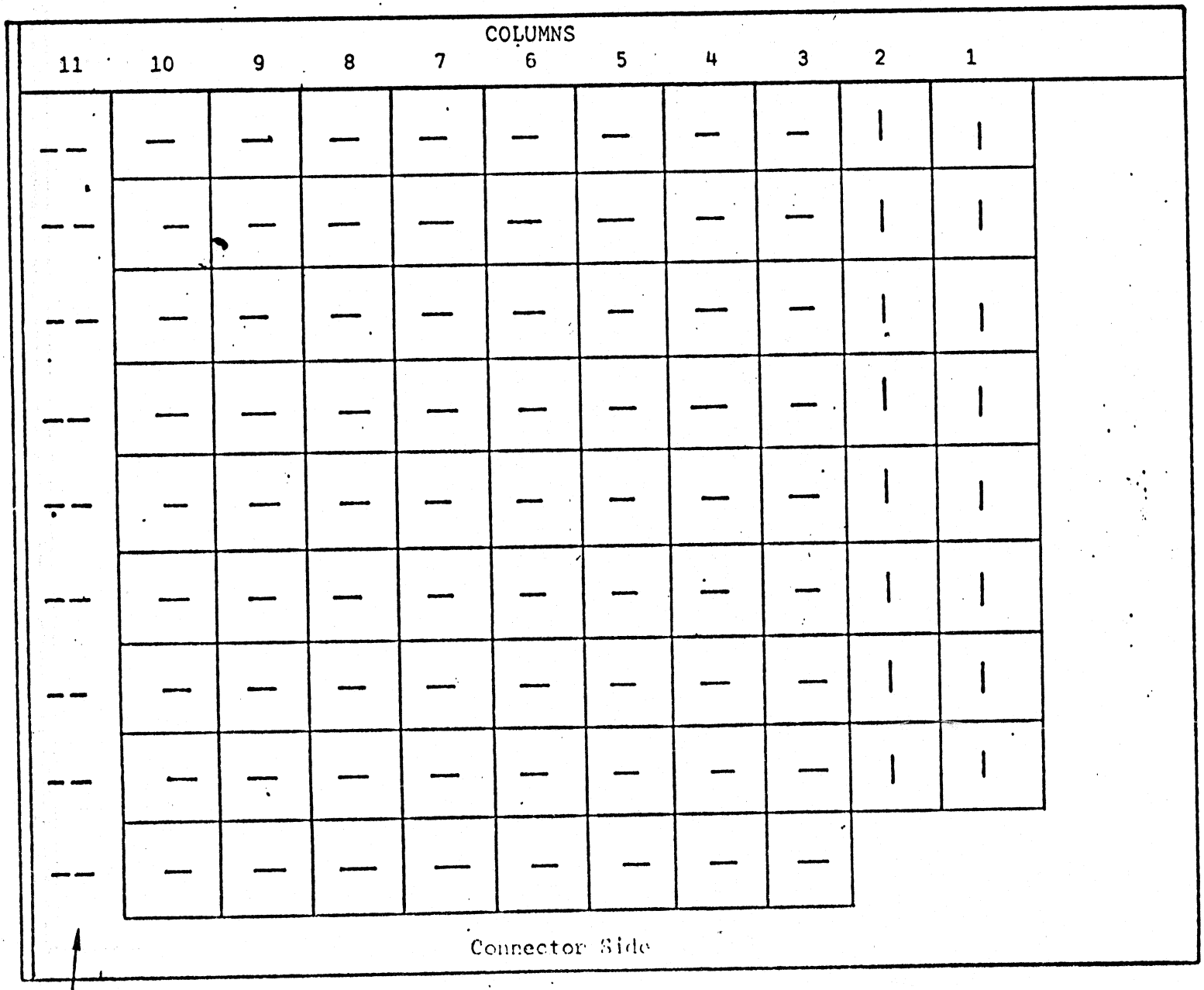
COGAR
5300034



COGAR
5300060

These modules do not hav
to be Type 5300034

umn Bay
ng



COGAR 5310184

COGAR 5300060

8K (Partial Chips)
FIGURE 2

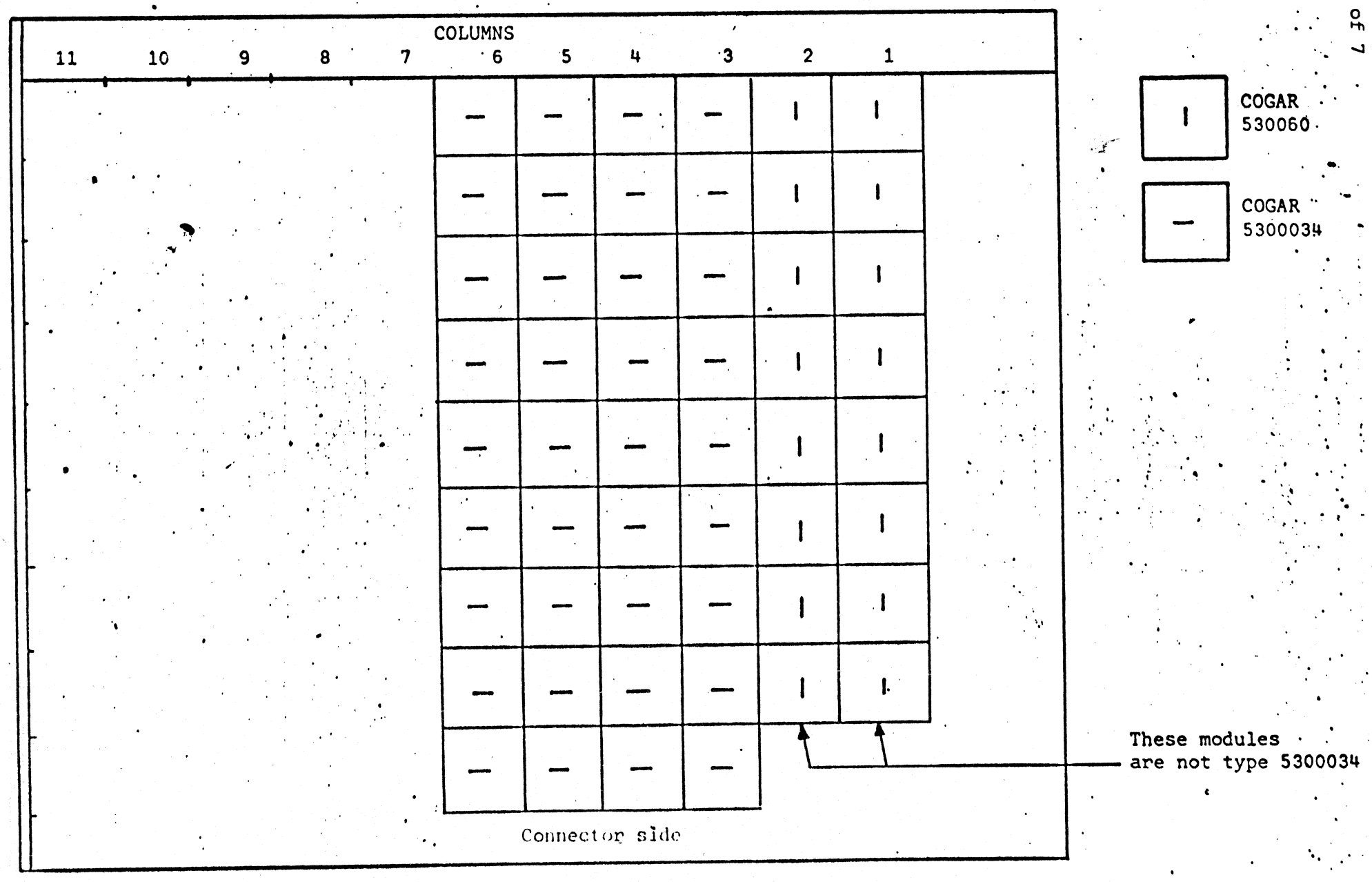
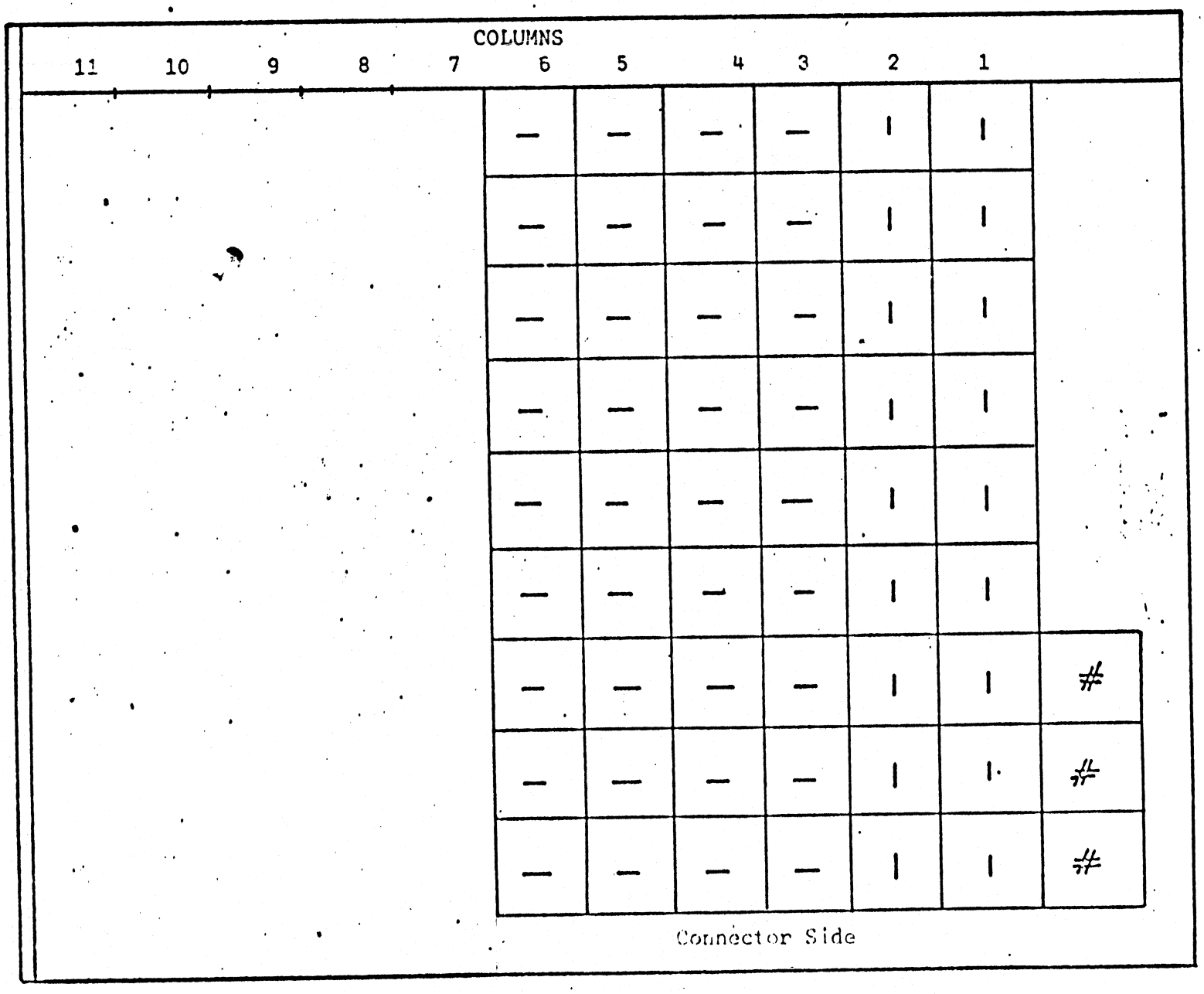
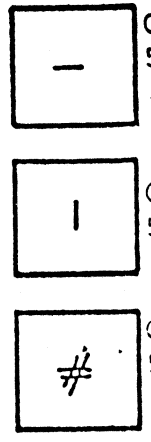


FIGURE 3
8K (Full Chips)





4K (Partial Chips)
FIGURE 4

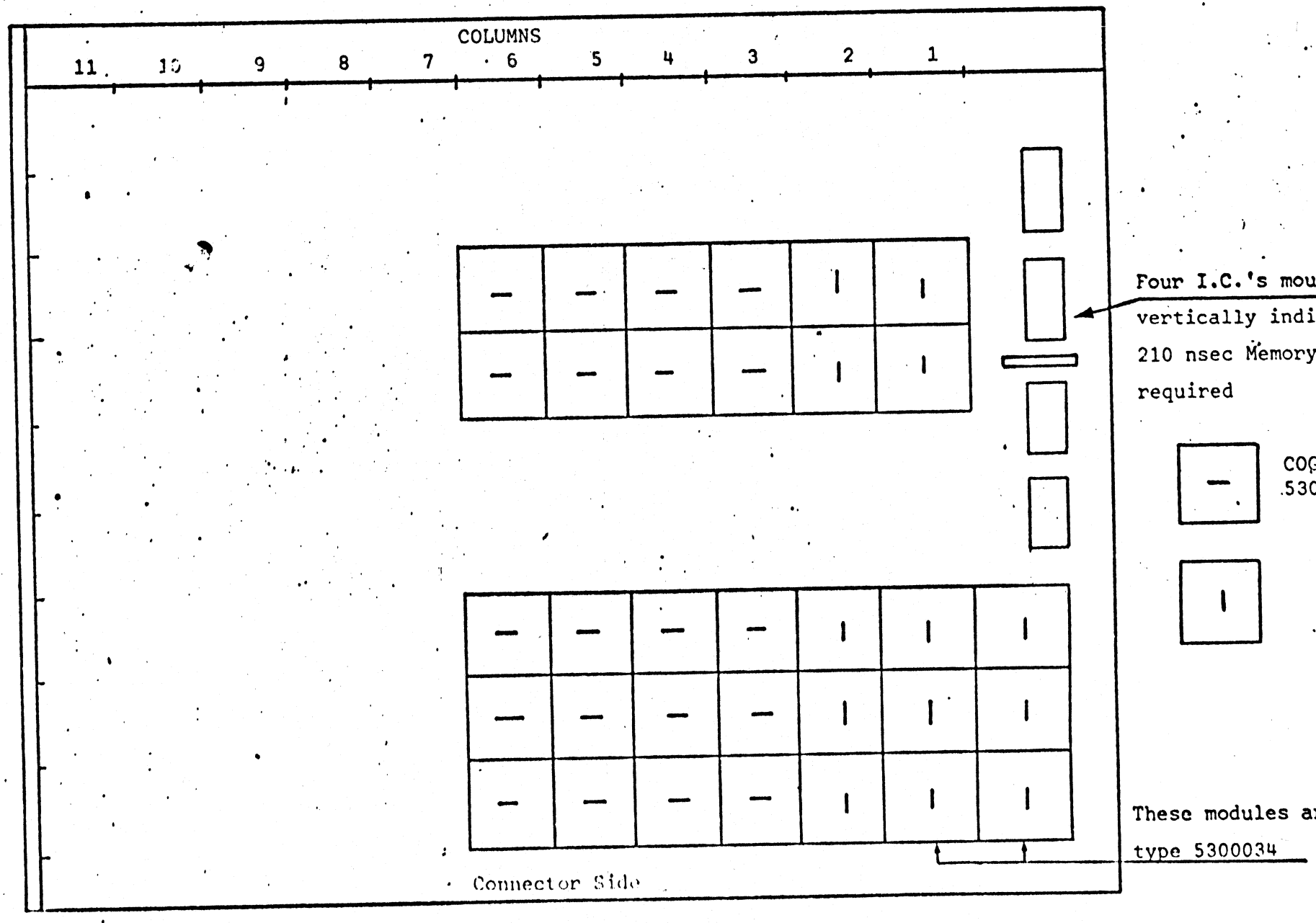
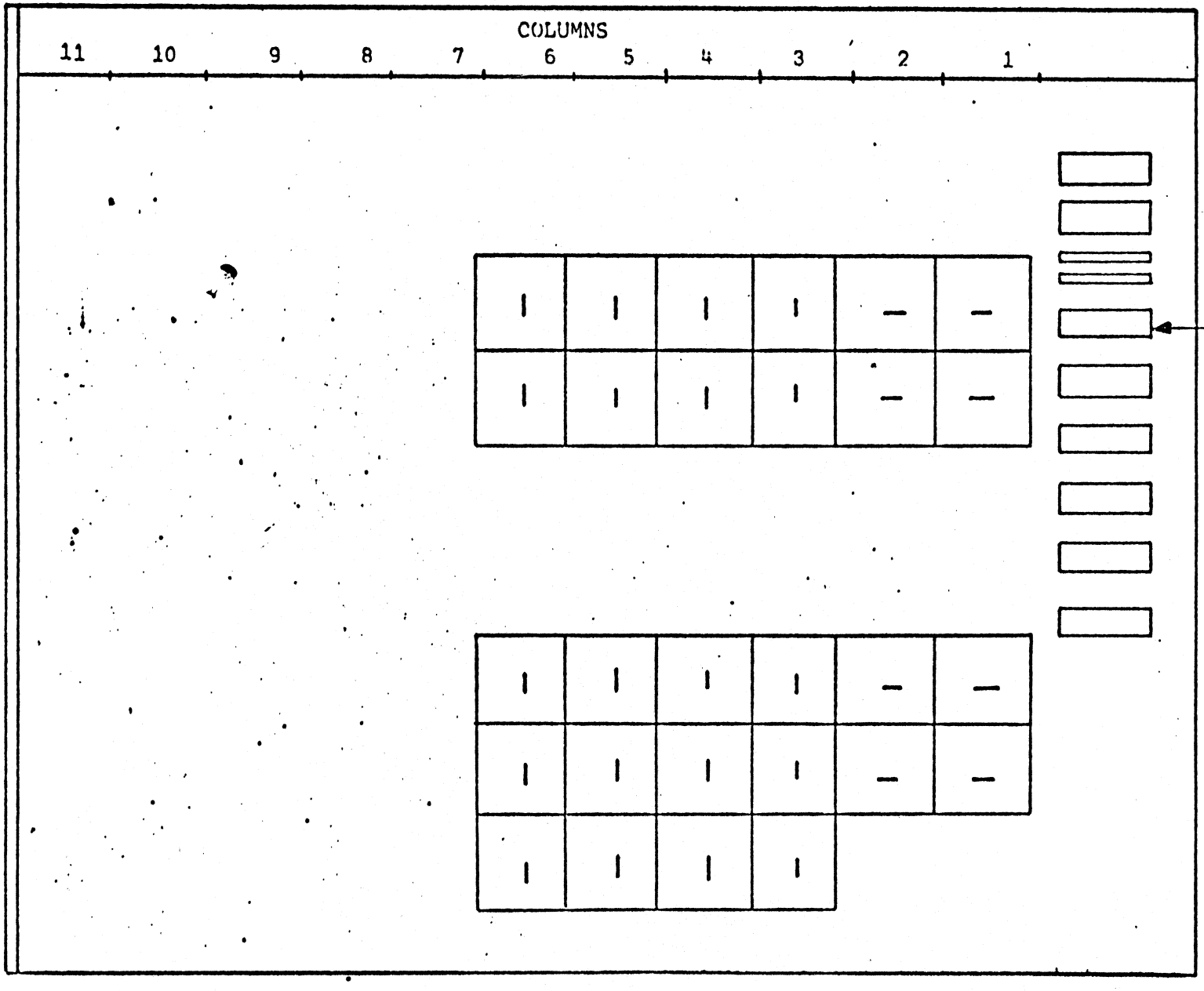


FIGURE 5
4K (Full Chips) 210 NS



COGAR 5300034

COGAR 5300060

Many I.C.'s mounted horizontally indicates a 240 nSec memory clock is required.

4K (Full Chips) 240 NS
FIGURE 6

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INTERNATIONAL SERVICE LETTER

1500 DATA COMMUNICATION

TP-1783FN

Febr. 15,1974		1 Rev. 1

Subject: 1535 BSC Communication Signal Data Rate and Ground Connections.

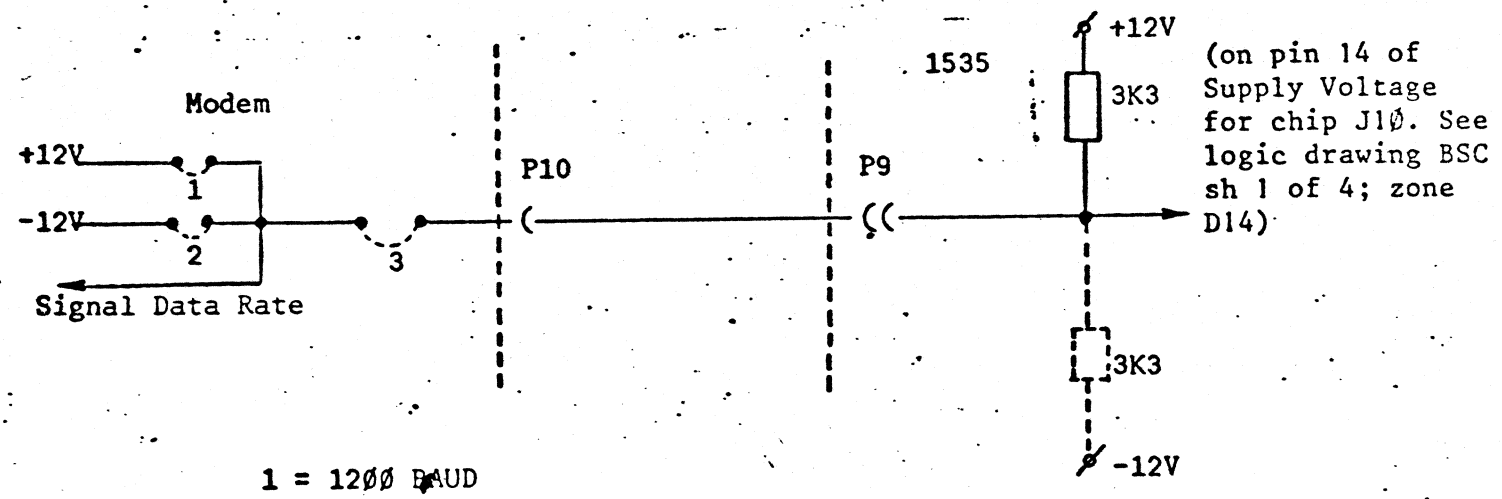
Machines affected: All 1535's

Action required: Information only.

Information: To establish normal communication possibilities the following actions must be taken:

a) Interconnection logic-ground/signal-ground.
Reference is made to dwg.no. Assy Cable Communications 006-002012-003. Interconnection between the signals frame-gnd and sig-gnd. must be made on either the 1535 BSC-Board or in the modem.

b) Signal Data Rate.
Reference is made to above-mentioned dwg. This signal should be connected to +12V for 1200 BAUD and to -12V for 600 BAUD. This connection can be strapped in the modem. If the modem must be used for different BAUD-rates the connection to +12V or -12 -12V through a 3K3 resistor is made on the BSC-Board.
See connector P9-09 on schematic.
In revision 8 Boards and higher the 3K3 resistor is connected to +12V (=1200 BAUD). Reposition if required.



1 = 12ØØ BAUD
2 = 6ØØ BAUD
3 = connection must be made in 1535 through 3K3 resistor.

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 DATA COMMUNICATION

TP-1783FN

Dec. 14,1973		1

SUBJECT: 1535 BSC Communication Signal Data Rate and Ground Connections.

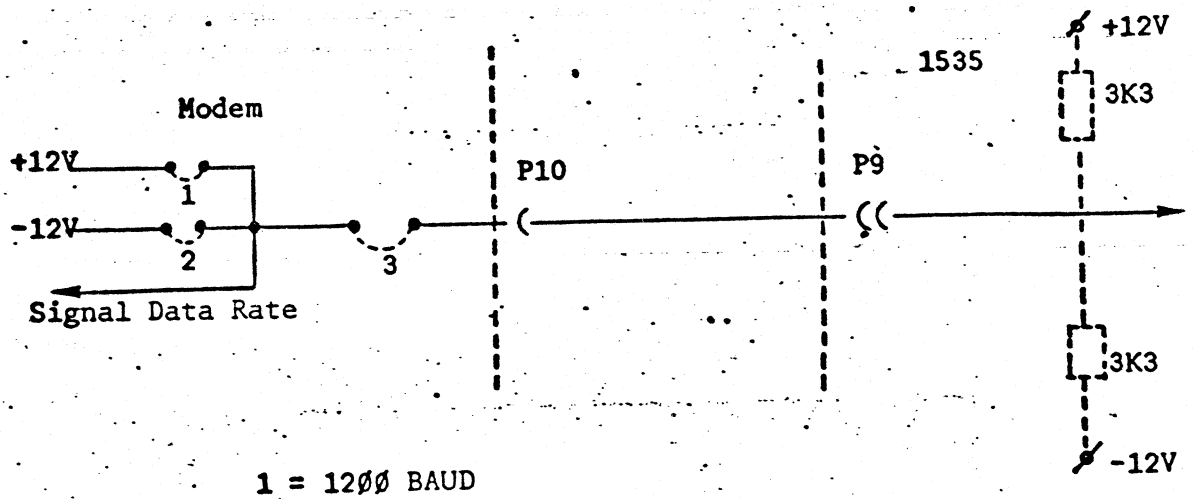
MACHINES AFFECTED: All 1535's

ACTION REQUIRED: Information only

INFORMATION: To establish normal communication possibilities the following actions must be taken:

a) Interconnection logic-ground/signal-ground.
Reference is made to dwg.no. Assy Cable Communications ØØ6-ØØ2Ø12-ØØ3. Interconnection between the signals frame-gnd and sig-gnd. must be made on either the 1535 BSC-Board or in the modem.

b) Signal Data Rate.
Reference is made to above-mentioned dwg. This signal should be connected to +12V for 12ØØ BAUD and to -12V for 6ØØ BAUD. This connection can be strapped in the modem. If the modem must be used in different ways the connection to +12V or -12V through a 3K3 resistor is made on the BSC-Board.
See connector P9-Ø9 on schematic. The +12V and -12V are not labelled in the schematic (Measure at chip 111).



1 = 12ØØ BAUD
2 = 6ØØ BAUD
3 = connection must be made in 1535 through 3K3 resistor.

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 DATA COMMUNICATION

TP-1783FN

Dec.14,1973		2

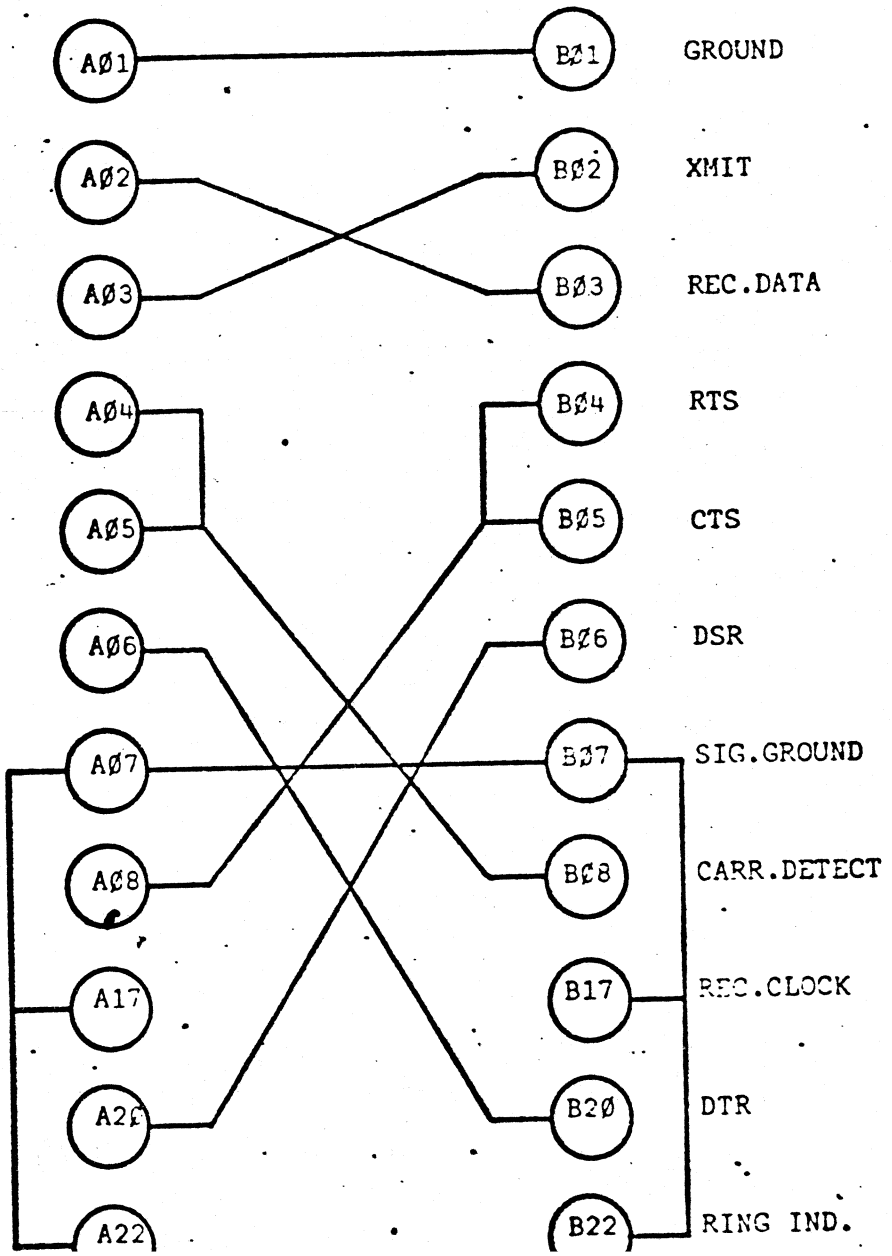
SUBJECT: 1535 Back to Back test possibility

MACHINES AFFECTED: See Subject

REASON Information only

INFORMATION: All test programs using the internal clock can be used when the wire connection is made as shown in figure 1.

CONNECTOR DATA COMM. 1501/1535



SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 DATA COMMUNICATION

TP-1783FN

Dec. 14,1973		3

SUBJECT: Patching 2024 modem for use with 1535.

MACHINES AFFECTED: All 1535's

ACTION REQUIRED: Information only.

INFORMATION: Following is a complete list of jumpers which must be patched in the 2024 modem setting up 201-A configuration for use with 1535 communication adapter. Only jumpers listed should be installed. Remove all other jumpers.

CORRECTIVE PROCEDURE:

-201-A modification, 2000 bit per second	Transmit-83PS A1, A2, A3, A4, A5, A6, AB	Receive 83PR A1, A2, A3, B3, B4, R, X, Z
-150 millisecond delay clear to send	G	-
-600 ohm termination	J.V.	K
-Auto answer-1001-A data coupler	L.P.	-
-No call abort	S	-
-Carrier control by request to send	K1	-
-Receive data squelch-120 millisecond	-	FF,M
-Carrier lamp off during receive carrier	-	H
-No local copy	M1	GG
-Spare lock-up	-	ZZ
-No half-rate	-	-
-No forced clear to send	-	-
-No special clock	-	S1
-No equalizer	-	P

Note 1: Normal patching level is -10DB-1 to 2, 3 to 4, 5 to 6. If this does not work, patch for two (2) DB below marked on DAA.

Example: DAA= -7, should patch for DAA=-9.

Note 2: Pins 14 and 24 MUST be opened in the modem on the 25 pin connector.

PARTS/TOOLS: System tool kit.

Dec.14,1973		3

SUBJECT: Field Replacement of Tachometers

PURPOSE: This procedure will be followed to replace malfunctioning tachometers. To determine if a tachometer is bad, check for the following symptoms:

A. Electrical Symptom - Deck will not run at slow speed, only high speed is possible. Or in forward and reverse: speed is not constant.

B. Mechanical Symptom - Turning of capstan (Fig. 1, A) does not turn tachometer shaft (Fig. 1, B).

PARTS REQUIRED: Replacement Tachometer Assembly Cogar (P/N 300-001700-004)
Singer (P/N 9012173-53)

PROCEDURE:

A. Turn the Tape Deck upside-down. The tachometer(Fig. 1, C) is mounted on the Drive Motor (Fig. 1, D).

B. Unsolder the red wire and the black wire at TB-1 (Fig. 1, E). The red wire connects to the blue wire on TB-1 and the black wire connects to the blue/white wire.

C. Next, unsolder the blue wire (fig. 1, F) and the blue/white wire (Fig. 1, G) on the Drive Motor.

D. On the Coupler, located in between the tachometer and Drive Motor (Fig. 1, H), four Allen Head Screws can be seen. They are arranged in pairs which are at right angles to each other. Loosen the lower pair (the pair closest to the Drive Motor).

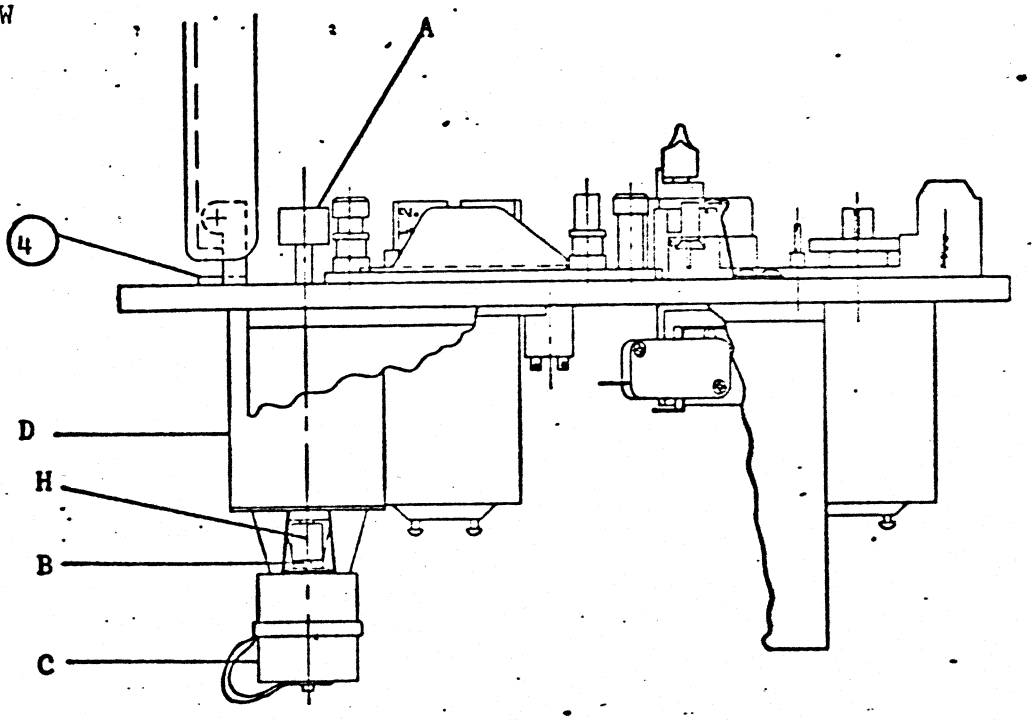
E. Using the Medium Phillips Screwdriver, remove the 3 screws (Item I) holding the plastic mounting bracket to the Drive Motor. You will now be able to remove the tachometer, Coupler, and mounting bracket as one unit by lifting upwards.

F. The new tachometer may be installed by following these procedures in reverse order.

NOTE: The new tachometers will have a protective cover over the terminals on the tach. This cover should not be removed until the deck is being installed in a System. Tach coupler should be carefully positioned upon the motor and tach shafts.Set screws should be equally torqued when tightened. If excessive tach wobble is noticed after assembly, re-positioning the coupler and/or re-setting the set screws should reduce this wobble.

G. Use Aut. Sys. Test to evaluate Tape Deck Speed.

SIDE VIEW



BOTTOM VIEW

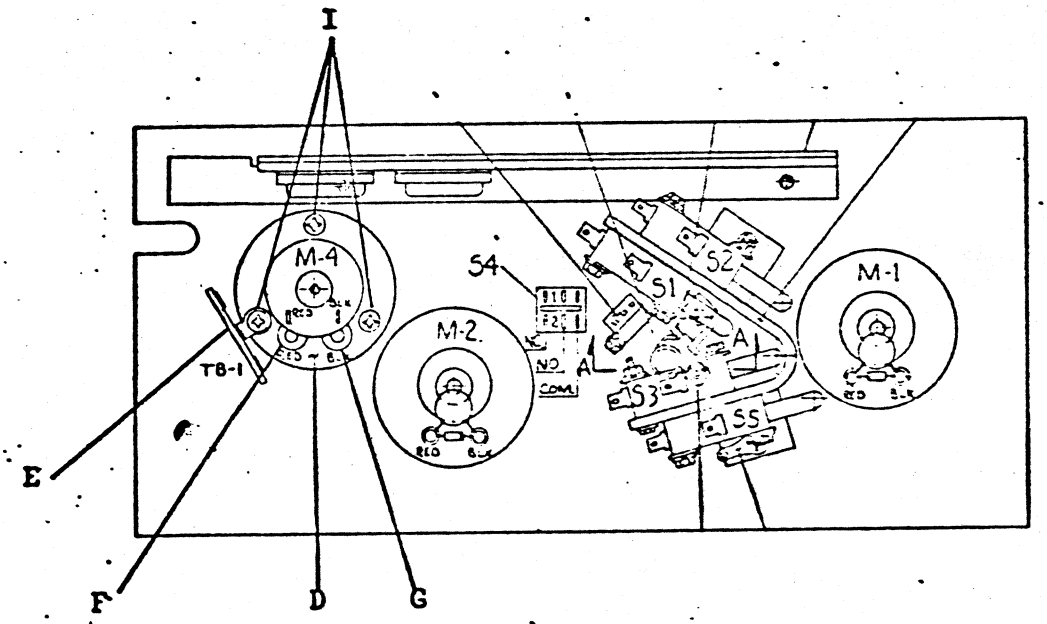


FIGURE 1

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INTERNATIONAL SERVICE LETTER

1500 GENERAL

TP-1779FN

Dec.14,1973		5

SUBJECT: Interchangeability of high- and low- power motor on mini tape deck.

MACHINES AFFECTED: All Mini Tape Decks.

ACTION REQUIRED: Information only.

INFORMATION: Two different Tape Decks exist: High and Low Power. The High Power Deck can be identified by looking at the spring connected to the carrier-lock mechanism. If this is a long one: High Power Deck. Several Assy's are not interchangeable.
One may find in one machine one Low Power Deck and one High Power Deck, or 2 High Power Decks or 2 Low Power Decks! The Low Power Deck is the latest version.

Below follows a table in which the sub-assy's of Hi/Lo-Power Decks are identified for the interchangeability-diagram.

High Power Deck		Low Power Deck		
A	Supply Motor (labelled by Cogar	E	Supply Motor = 4Ø Ohm	(labelled by sticker
B	Take-up Motor P/N ØØØØ9ØØ1)	F	Take-up Motor = 7Ø Ohm	
C	Servo Motor + Tacho	G	Servo Motor + Tacho	
D	Motion Cntl.Bd.	H	Motion Cntl.Bd.	

Interchangeability Diagram

In this diagram one can find the possible configuration for one type of deck.

	High Power	Low Power
Supply Motor	A or B	E
Take-up Motor	A or B	F
Servo Motor + Tacho	C or G	C or G
Motion Cntl.Bd.	D	H

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 GENERAL

TP-1779FN

Dec.14,1973		1

SUBJECT: Speed Adjustment on Low Power Tape Decks.

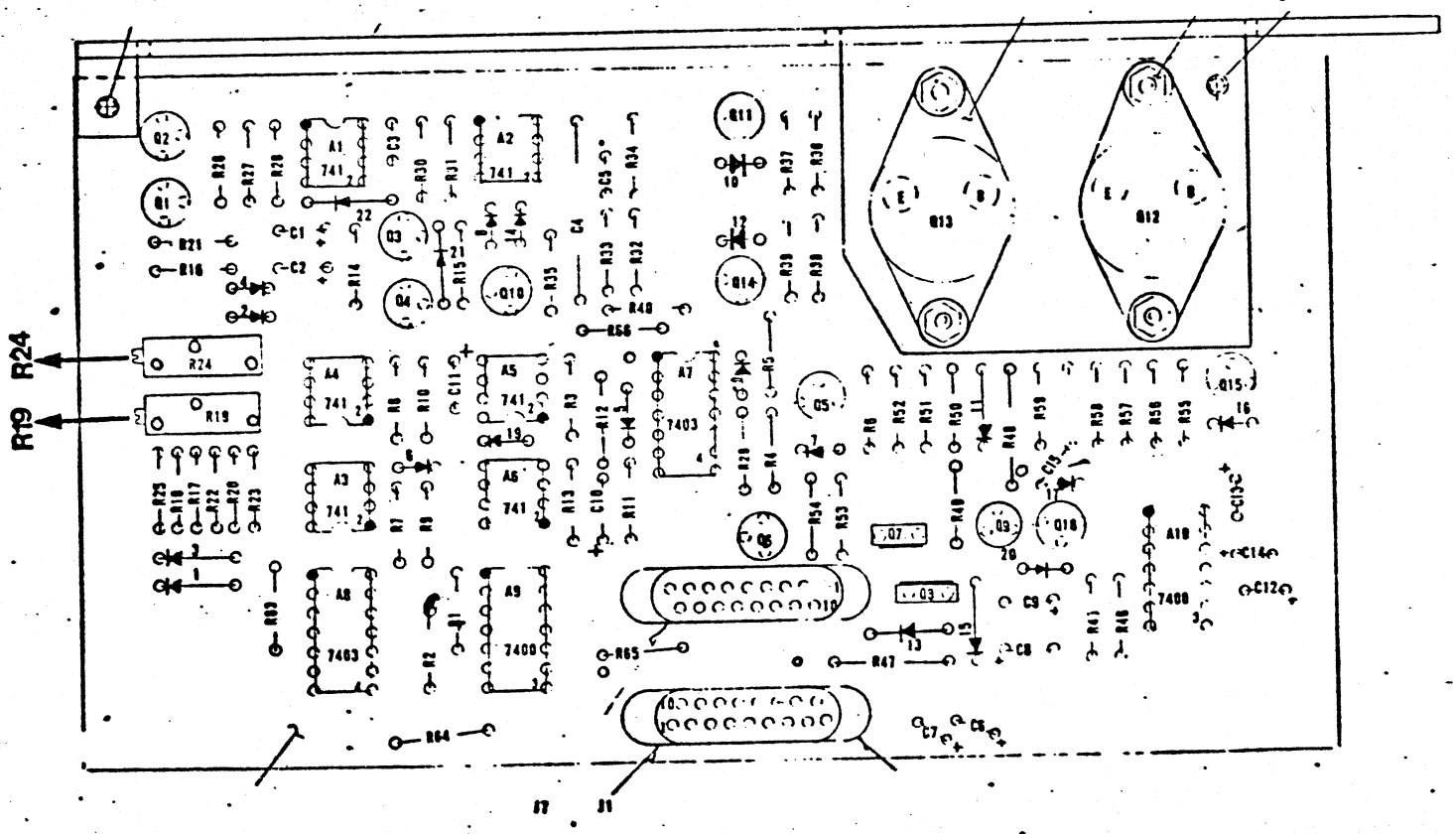
MACHINES AFFECTED: All 1500 Systems with Low Power Tape Decks.

REASON: Due to the new design of the Motion Control Board for the low power decks, the speed adjustment procedure has been changed.

To adjust the forward speed R19 (The Lower POT) is used.
To increase the forward speed, turn R19 clockwise. To decrease the forward speed, turn R19 counterclockwise.

To adjust the reverse speed R24 (The Upper POT) is used.
To increase the reverse speed, turn R24 counterclockwise.
To decrease the reverse speed turn R24 clockwise.

Use Aut. Sys. Test to evaluate Tape Deck Speed.



SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 GENERAL

TP-1779FN

Dec. 14,1973		2

SUBJECT: 15ØØ-Software problems High Power and Low Power Decks

MACHINES AFFECTED: All 15ØØ Models with cartridge tape drives.

ACTION REQUIRED: Information only.

INFORMATION: Due to the fact that a difference exists in start/stop-times for High- and Low Power decks, the Mini Read Write routine should provide a 100 mS start delay and 100 mS stop delay. With this value both types of decks can be controlled.
Application software written in the past might have a correct operation on high-power-deck but incorrect operation on low-power-deck.
The C_4T and Aut. Sys. Test contain the correct mini-routine.

TP-1779FN

Dec.14,1973		4

SUBJECT: Low Power Tape Drive Start/Stop Times.

MACHINES AFFECTED: All 1500 Systems with Low Power Tape Drives.

ACTION REQUIRED: Information only.

INFORMATION: If a Tape Drive passes all the available test software (automatic systems test, and the C4T tape diagnostic Program), but tape errors occur during either:

A. Rewriting a record in place
B. High speed search operation.

The fault may be incorrect start/stop times.

The start/stop times for the Tape drive may be observed by following this procedure.

A. Set Channel A probe at the positive leg of C1. See attached illustration. Set channel A volts/Div to .2 volts.

B. Set time base to 5 MS

C. Trigger scope at A8 pin 1.

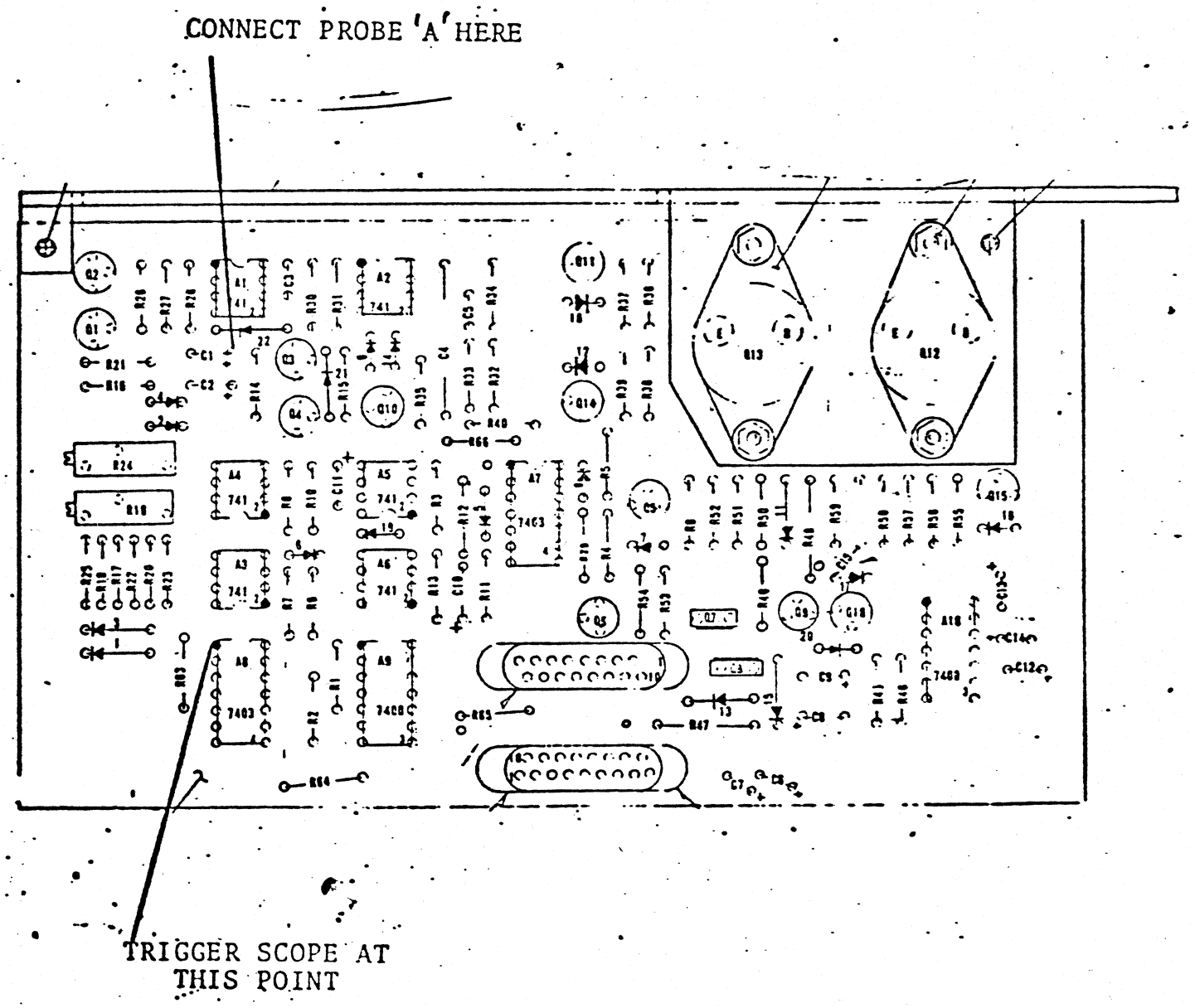
D. Load C4T Program and select 4, ADM
Depress "A" 02000
Key in the following program at the corresponding addresses.

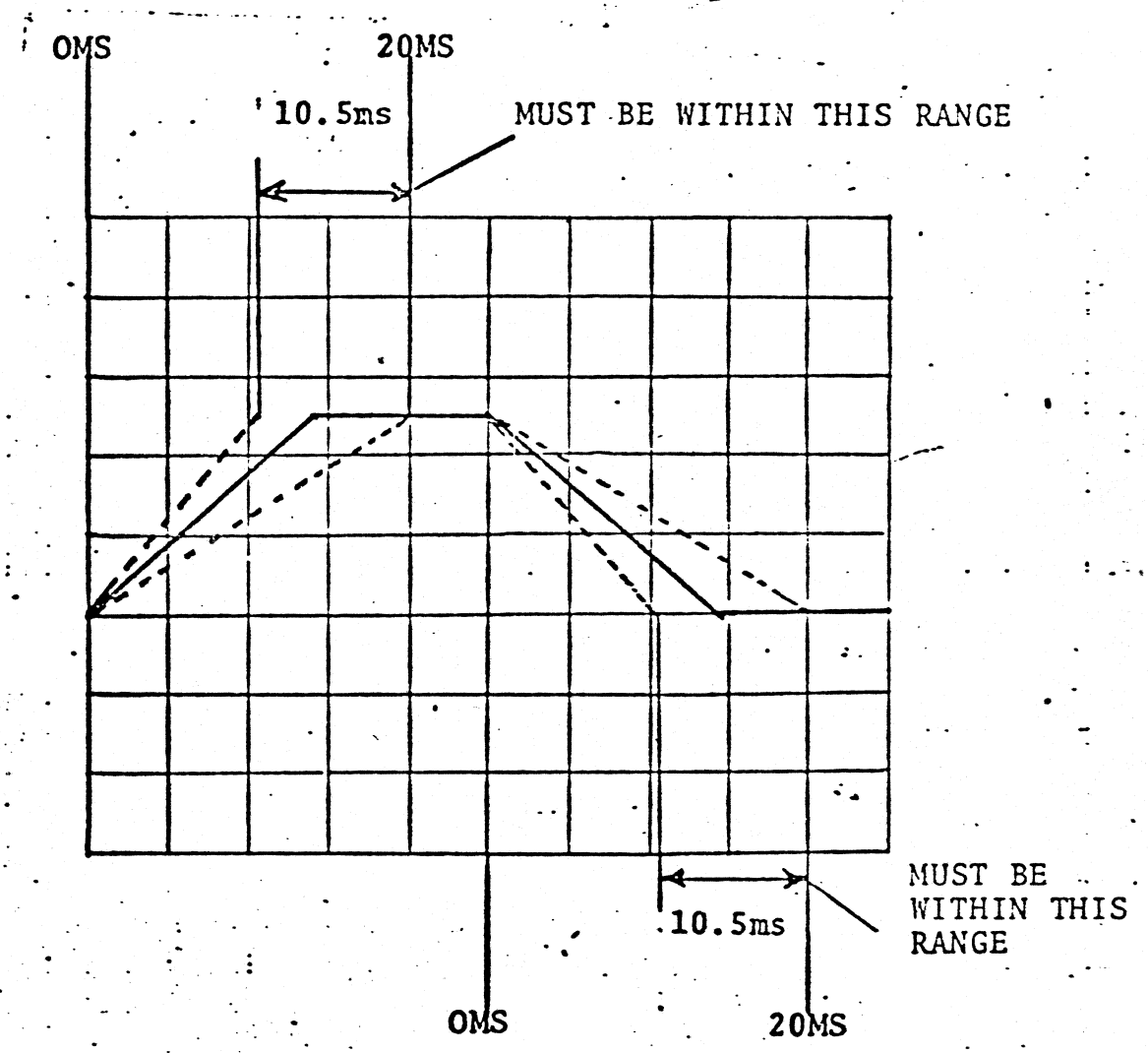
Address	Instruction
P02 000	172-001
" 002	122-012
004	171-005
006	122-012
010	102-000
012	201-011
014	261-001
016	341-000
020	102-035
022	122-034
024	200-000
026	260-001
030	015-000
032	102-026
034	140-000

Load scratch tape
Depress "X"
When the tape nears the end depress the rewind button.

E. The ramp wave form observed on the scope must comply

e ramp time may be altered, if out of spec., by changing the value of C1 or C2.





TIME BASE 5ms/DIV
AMPLITUDE SCALE .2 VOLTS/DIV

FIGURE 1

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1501/1530

TP-1780FN

Jan. 15,1974		8

SUBJECT: 1501 Downward Compatibility of New TCI or Processor Boards.

REASON: Information only.

In T.I. Memory Systems:

Processor Board must be Rev.9 or higher.
T/C/I Board must be Rev 8 or higher.
Jumper 1B55 to 2B12. (Rev 7 wired moduled)

In Cogar Memory Systems:

If processor board is at Rev 8 or less the T/C/I board must supply P-Call-Zone at pin 1B60, ie. Rev 7 or below T/C/I boards must be used. If Processor board is at Rev 9 or above the T/C/I board must supply N-Call-Zone at pin 1B60, ie. Rev 8 or higher. In addition a jumper must be added to 1B55 from 2B12.

When replacing either a T/C/I or Processor board, the revision of both must be checked, and the rules stated above must be followed.

The jumper from 1B55 to 2B12 may be installed in any system, T.I. or Cogar, regardless of Rev. levels.

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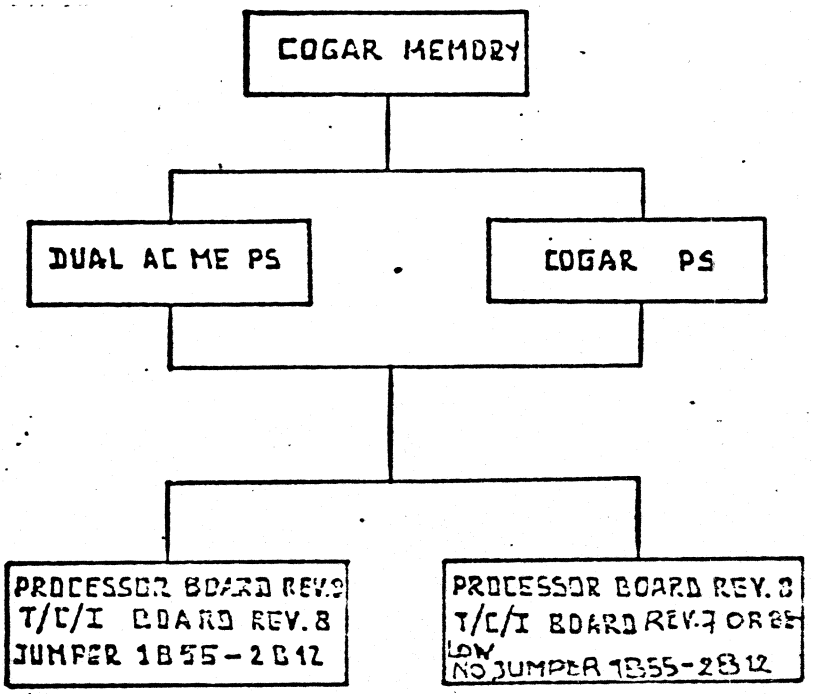

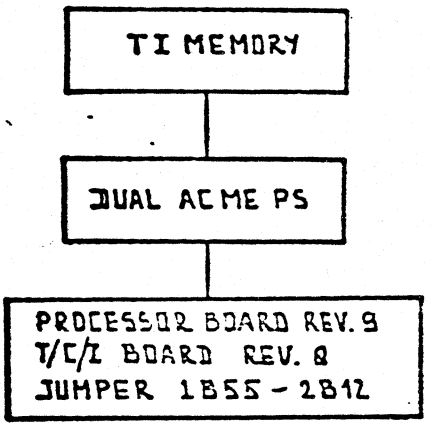

NOTE: P.S. Voltages must be checked for different Memories.
Jumper on Processor Board must be checked for different Memories.

SINGER
BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 TAPE DRIVES

TP-1781FN

Jan. 15,1974		1

SUBJECT: Release of 1511 7 Track Test Program

SYMPTOM: None

MACHINES AFFECTED: All 1501's

REASON: Release Test Program for 1511 7 Track Tape Drives

INSTRUCTIONS: The operator instructions are identical to those mentioned in the PEC I/O Test program in the C_4T Test Library and are therefor not included. Only exception: Delete CRC Transmit Check = Control Minus Key. Reason: no CRC or 7 Track Drives.
Source listing included in 1500 Manual.
Program available under FN-5734.

To make additional copies a copy function is included in the program.

PARTS AFFECTED: None

PARTS REQUIRED: Test Tape FN-5734

TIME REQUIRED: None.

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INTERNATIONAL SERVICE LETTER

1500 GENERAL

TP-1779FN

Jan. 15,1974		6

SUBJECT: Proper creation of test tape for C_4T program Tape Diagnostic.

SYMPTOM: Error message in "Tape Diagnostic" (C_4T).

MACHINES AFFECTED: 1500 Cassette Tape Drives only (as only these drives can be tested with abovementioned program.

INSTRUCTIONS: In order to run the "Tape-Diagnostic" program in the C_4T test library, a Test Tape must be created.
This test tape can be created using the: "Create Test Tape" function of C_4T.
Writing can occur with 1,1 inch IRG (no special selection required) or with 0,5 inch IRG (selected by control @, see operator instructions).
If this last writing is not selected, an error message will appear at the end of the Tape Diagnostic pass indicating 6Ø RS (Reverse Search) errors.
So always use the 0,5 inch IRG writing feature when preparing a Test Tape for the C_4T Tape Diagnostic Program.

PARTS AFFECTED: None

PARTS REQUIRED: None

TIME REQUIRED: None

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INTERNATIONAL SERVICE LETTER

1500 GENERAL

TP-1779FN

Jan. 15,1974		7

Subject: Alignment of Cartridge Locator, Supply Reel and Take-up Reel.

Symptom: Adjustment

Machines affected: All cartridge Tape Drives

Instructions:

1. Raise cartridge loader to vertical position.
2. Remove locking handle.
3. Loosen the six screws holding in place the cartridge locator.
4. Insert the cartridge alignment tool over the supply shaft head.
   NOTE: About 5/1000" play will be noticed between the supply shaft head and the cartridge alignment tool.
5. The cartridge should be positioned so that the supply reel is able to turn freely inside of it.
6. Tighten down the six screws that hold the cartridge locator and and replace the locking handle.
7. If it is necessary to replace the supply shaft head or take-up reel, their position on the shaft should be set with the master cartridge.
8. The base of the supply shaft head should be flush against the base of the cartridge alignment tool when it is seated properly in the cartridge locator.
9. The outside diameter of the take-up reel should be at the proper height so that it aligns with the slot in the cartridge alignment tool.

Parts affected: None

Special tools: Cartridge Alignment Tool FN5674.

Time required: 15 minutes.

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BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 TAPE DRIVES

TP-1781FN

Feb.1.1974.		3

Subject: Odd/Even Parity on 1511.

Symptom: n/a

Machines Affected: All 1511's.

Reason: Change when required.

Instructions: The 1511 Converter Board provides odd Parity.
When even parity is required, the software program must be altered and the following hardware changes on the Converter Board must be made.

Remove connections: D16-1 to D5-8
H16-9 to G10-2

Connect: D16-1 to D16-5
H16-6 to G10-12.

Parts Affected: n/a

Parts Required: n/a

Time Required: ½ hour.

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BUSINESS MACHINES

INTERNATIONAL SERVICE LETTER

1500 PRINTERS

TP-1782FN

Febr. 15,1974		3

Subject: 1525/1526 Power Supply.

Symptom: Intermittent Errors.

Machines affected: All 1525/1526 Printers.

Reason: Change as on fail basis.

Instructions: See schematic 1525/1526 Power Supply.
The output of the non-adjustable Power Supply is controlled by the operational Amplifier U1. The reference input of U1 is controlled by the 5.1V zener diode CR-3. When the zener voltage is not exactly 5.1V the output voltage might be incorrect resulting in intermittent Errors. Change 5.1V zener diode if necessary.

NOTE: If CR3 is open, the reference input to U1 goes positive. This results in an increased 5V supply output which might damage components. The overvoltage protection SCR1 does not fire, because the transistor Q1 will not conduct as result of a high positive potential (+ 10V) on its base and the increased 5V supply (+ 6.5V).

Parts required: Zener diode 5.1V, 2%, 1/4W.

Time required: 15 minutes.

TP-1782FN

Dec.14,1973		1

SUBJECT: Release of Test Program for 1525 or 1526 with the Cogar Motion Control Electronics.

REASON: 1525/1526 Information only.

INFORMATION:
1. For source listing see TPA-1114FN
2. The Test Program Description
3. Part no. Test Program FN-5723.

A. OBJECTIVE

This program is designed to exercise the Model 1525 (132 Column) and the Model 1526 (80 Column) as a Line Printer and a Character Printer.

When the program is loaded, the operator may select one of four tests or Print in Increment Mode. The following will be displayed:

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"1525/1526 PRINTER TEST"
1) SHIFTING PATTERN.
2) ONE CHARACTER SHIFT.
3) RIGHT MARGIN TEST.
4) LINE FEED TEST.
5) RUN ALL TEST (1,2,3, & 4).
6) INCREMENT PRINT.
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B. OPERATION

When Selection 1, 2, 3, 4, or 5 is made, the display will change asking the operator to select either 132 characters or 80 characters to print.
When the selection is made, the test will begin.

1) Shifting Pattern - All printable characters are printed (A thru Z, etc.) then shifted to the right one place. This will be repeated causing a shifting pattern.

2) One Character Print - One character will be printed per line. Starting with "+" then "0" etc. and each character will be shifted to the right one place. The test will start over when the Top of Form is reached.

3) Right Margin Test - To check the right margin function a line of 255 "A"'s are printed. An automatic CR should take place after 132 characters (Model 1525) have been printed.

The remaining characters are printed on the next line. The next print will be all "B"'s then all "C"'s, etc. until all C4 characters have been printed. Then the pattern starts over again.

4. Line Feed Test - To exercise the line feed mechanism a line is printed then indexed. It is repeated with 2 indexes and 3 etc. until 10 has been reached, then the test will start over. The number of lines under the test will be printed along with a test pattern.

5. Run All Test - This selection will run All Test (1, 2, 3, & 4) in order. Each test will run for 66 lines (1 Form). When all tests have been run it will repeat.

6. Increment Print - This test allows the operator to operate the printer in character mode. Each time a key is depressed on the SYSTEM 4 it will be printed. All characters on the keyboard are printable except the CONTROL character. The Control Keys which are operative in this mode and will be displayed during this selection.

C. CONTROL KEYS

1. Control Keys for Selection 1 thru 5

   a. Any Key = Start or Stop
   b. HOM Key = Return to Test Selection and clears printer errors.

2. Control Keys for Increment Mode

   a. LEFT ZERO = Carriage Return
   b. REL = Line Feed
   c. PRG/SEL = Display Status
   d. BKSP FIELD= Left Margin (CR without LF)
   e. ERROR = Clears Printer and displays Status
   f. HOM = Returns to test selection and clears printer errors.

D. ERROR DISPLAY

1. If an error occurs during printing it will be displayed on the CRT and an error tone activated. By depressing any key the operator will return to the test selection and the Printer will be cleared.

2. The following are the errors which may occur:

   a. I/O ERROR = Error in the Serial I/O
   b. ADDRESS ERROR = Printer can not be addressed
   c. Out of paper or interlock switch on.
   d. OVERRUN = Character underflow has occurred.