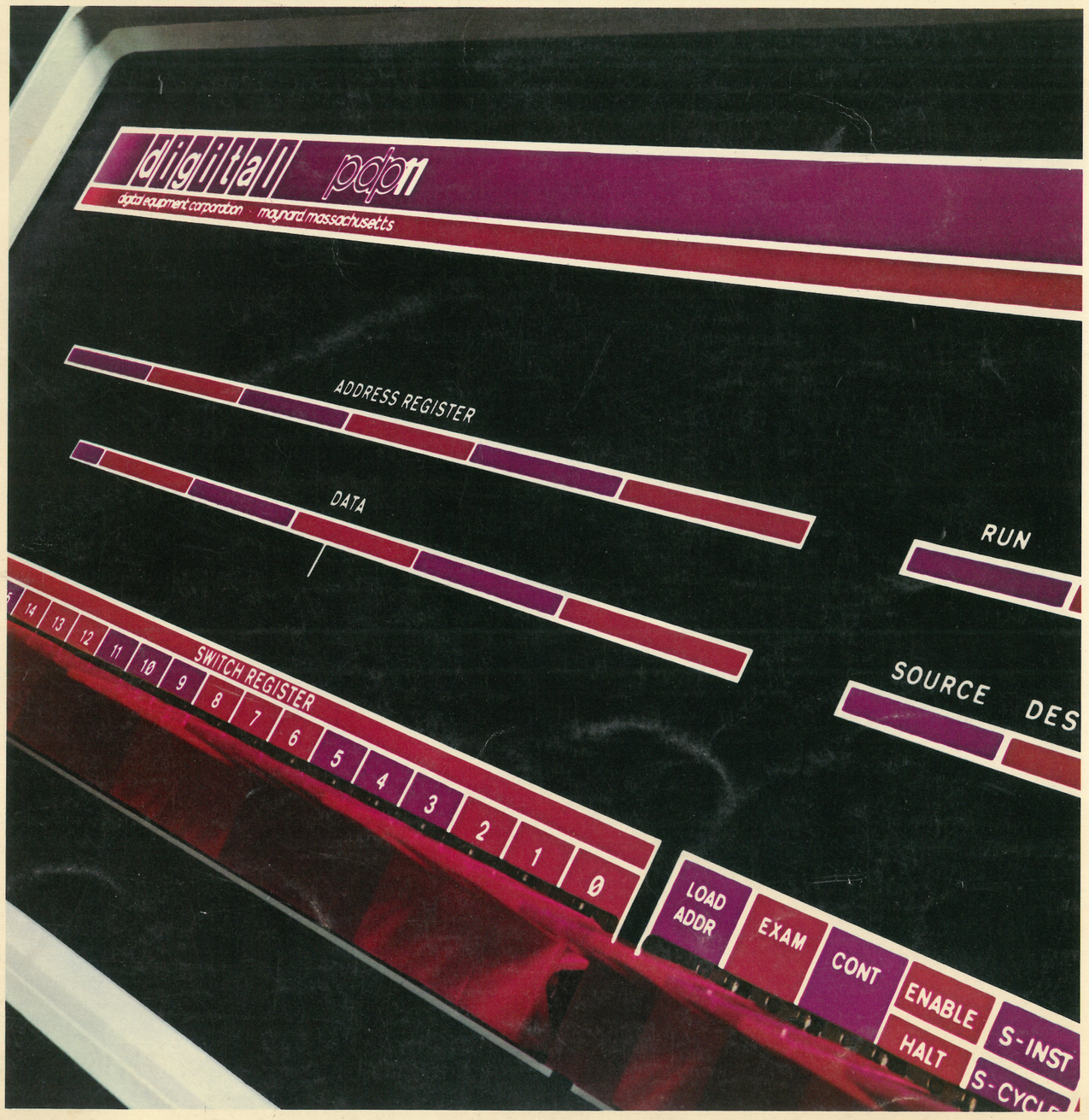

pdp11

PC-11 High Speed Paper Tape Reader/Punch manual

digital

DEC-11-HPCA-D

PDP-11
PC11 HIGH-SPEED READER/PUNCH AND CONTROL MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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FOREWORD

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the PC11 High-Speed Paper-Tape Reader/Punch and Control. This manual is directed at the reader who is familiar with basic digital computer theory. Consequently, this manual contains both general and detailed descriptions of the PC11 Reader/Punch and Control.

Control signals and data are transferred between the PC11 Reader/Punch Control and the Unibus(TM); however, this manual does not cover the operation of the Unibus. A detailed description of the Unibus is presented in the *Unibus Interface Manual* (DEC-11-HIAA-D).

The PC11 Reader/Punch Control is basically an interface between the bus and the PC05 High-Speed Paper-Tape Reader/Punch; however, this manual does not discuss operation of the PC05 unit. For a detailed discussion of the operation and maintenance of the PC05 High-Speed Paper-Tape Reader/Punch consult the *PC05 High-Speed Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HGHA-D).

A complete set of engineering logic drawings is provided with each PC11 Reader/Punch and Control. In addition, a set of reduced drawings is included in this manual. If any discrepancies exist between the drawings in this manual and the drawings supplied with the unit, the drawings furnished with the PC11 Reader/Punch Control take precedence.

This manual is divided into five chapters:

a. introduction
b. installation
c. operation and programming
d. detailed description
e. maintenance

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The following publications provide additional information about the PDP-11 System and the PC05 Reader/Punch:

Document Title	Number	Information
Unibus Interface Manual	DEC-11-HIAB-D	This manual describes the Unibus and bus operations; also various circuits of the M105 and M782 Modules are described.
PDP-11/20 System Manual	DEC-11-HR1A-D	A description of the overall system and of the instruction set.
PDP-11/20 Conventions Manual	DEC-11-HR6A-D	This manual provides a glossary, list of signal names in the processor, and pin assignments.
H720 Power Supply and Mounting Box Manual	DEC-11-HR5A-D	This manual depicts the physical construction and locations of parts, and a description of the power supply.
Paper-Tape Software Programming Handbook	DEC-11-GGPA-D	This manual describes the use of devices in the operating environment, and programming instructions.
PC05 High-Speed Paper-Tape Reader/Punch Maintenance Manual	DEC-00-HGHA-D	A description of the operating controls, physical construction, and logic of the PC05 device used in the PC11.

CHAPTER 1
INTRODUCTION

The PC11 Reader/Punch and Control comprises a PC05 High-Speed Paper-Tape Reader/Punch, a PC11 Control, and two connecting cables.

The PC05 High-Speed Paper-Tape Reader/Punch can be controlled by any PDP-11 System through a PC11 Reader/Punch Control. The PC05 serves as an input device (from eight-channel perforated paper tape) and an output device (to the same medium) for the system.

The PC11 Reader/Punch Control directs the operation of the PC05 Reader/Punch, which can be operated for single data transfers or for continuous data transfer. The PC11 controls the parallel transfer of an eight-bit byte between the Unibus and the PC05.

A PC11 Reader/Punch Control consists of three integrated circuit modules mounted on one-fourth of a system unit (slots 13 or 14 in the KA11 Processor or slots 1, 2, 3, or 4 in a DD11-A Peripheral Mounting Panel). Thus, four PC11 Reader/Punch Controls can be mounted in the space of a single system unit.

Two variations of the PC11 device are available from Digital Equipment Corporation (DEC). The PC11-A is designed for operation at 50 Hz power. The PR11 is a reader without a punch; it uses equipment identical to the reader portion of the PC11. When a 240V power supply provides power to any of these devices, an H722 Step-Down Transformer must be connected to the PC05 power supply.

1.1 FUNCTIONAL DESCRIPTION

The PC11 Control operates one PC05 High-Speed Paper-Tape Reader/Punch. The PC05 combines a photoelectric paper-tape reader and an electromechanical paper-tape punch in a 10-1/2 in. high frame that mounts in a standard 19-in. rack.

The paper-tape reader comprises: *a)* a light source, *b)* a set of photodiodes to translate the presence or absence of holes (in the tape) to logic levels representing 1s and 0s, *c)* a tape transport mechanism to move and position the paper tape between the light source and the read head, and *d)* bins to hold and collect the tape that passes through the reader. In addition to transferring an eight-bit byte from the paper tape to the PC11 Control, the reader can inform the PC11 Control of the reader's status. The specific indications of reader status are presented in Paragraph 3.1.

The paper-tape punch comprises: *a)* a punch drive motor, *b)* a punch mechanism that translates logic levels representing 1s and 0s to the presence or absence of holes in the tape, and *c)* a mechanism to advance the tape and position it under the punch mechanism. A supply of fan-folded paper tape is loaded into the PC05, and the tape, which is output by the punch, is collected in a bin accessible from the front of the PC05. The punch also provides signals to the PC11 Control to indicate its status; these signals are described in Paragraph 3.1.

Any information read or punched by the PC05 Reader/Punch is parallel transferred through the PC11 Control. One data path is used for input from the reader, and one path is used for output to the punch. The PC11 Reader/Punch Control enables the processor to determine the status of the PC05 device, to initiate device operations, and to control the use of the bus interrupt logic by the PC11.

When an address is placed on the Unibus, the PC11 Control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses assigned to the PC11 is selected, the PC11 Control determines whether an input or an output operation should be performed.

The PC11 Reader/Punch Control consists of four functional parts (see Figure 1-1): the address selection logic, the interrupt control, the punch control, and the reader control (four device register addresses that are divided into the two controls). The device register addresses are determined by the location of jumpers on the M105 Address Selection Module. These addresses are four sequential word addresses, assigned in ascending order to the device registers. The names, mnemonics, functions, and normally assigned addresses for the four registers are shown in Table 1-1.

An input operation from the reader is initiated when the processor transmits a command to the Paper-Tape Reader Status (PRS) register. The reader encodes and transmits one byte of data from a frame on the paper tape and then advances the tape. If the tape is in motion, the reader waits until the next frame of tape is in position over the read head, reads that frame, and advances the tape. In the reader, the transmitted word is stored in a buffer that can be read through the Paper-Tape Reader Buffer (PRB) register. A flag is then set, signalling the processor that a byte of data is available. When signalled, the processor may test the PRS to determine if this bit is set, or may enable interrupts from the reader, or service the reader between the execution of other instructions. When the new data is available in the PRB, the processor executes an instruction that moves the contents of the PRB to another bus location. The PRB is not cleared until the processor initiates another read operation.

An output operation is initiated when the processor transfers a byte to the Paper-Tape Punch Buffer (PPB) register. The punch mechanism waits until the punch rotor is synchronized with the punch head; it then punches the character and begins moving the tape forward to position it for the next punch operation. The processor can test the Paper-Tape Punch Status (PPS) register to determine if the current punch operation has been completed, or an interrupt service routine can be used.

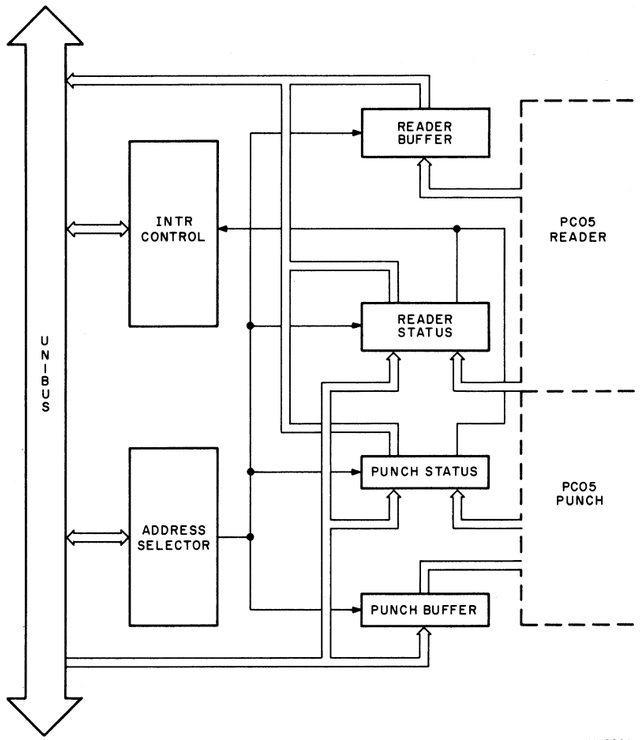

Figure 1-1 Simplified Block Diagram

Table 1-1
PC11 Device Registers

Name	Address	Mnemonic	Function
Paper-Tape Reader Status Register	777550	PRS	Provides indications of reader status, controls interrupts by the reader, and initiates reading.
Paper-Tape Reader Buffer Register	777552	PRB	Read-only register that gates data from the reader. Information is in low byte.
Paper-Tape Punch Status Register	777554	PPS	Provides indications of the punch device status and controls interrupts by the punch.
Paper-Tape Punch Buffer Register	777556	PPB	Write-only gating to the punch. Punching begins when the buffer in the punch is loaded.

1.2 SPECIFICATIONS

The physical structure, environmental specifications, and power supply requirements of the PC11 are presented in the following paragraphs. Corresponding specifications for the PC05 High-Speed Paper-Tape Reader/Punch are located in the *PC05 Maintenance Manual* (DEC-00-HGHA-D).

1.2.1 Physical Description

The PC11 Reader/Punch and Control is a small peripheral control device for the PDP-11. The PC11 consists of three integrated circuit modules that occupy four module slots in one row of the KA11 Processor (row 13 or row 14), or any one row of a DD11-A Peripheral Mounting Panel. All three modules are 8-1/2 in. in length. The modules are: *a)* the M105 Address Selector Module (single-height), *b)* M782 Interrupt Control Module (single-height), and *c)* M781 Reader/Punch Control Module (double-height). For information on the pin assignments of these modules, consult the *Unibus Interface Manual* (DEC-11-HIAB-D). Two BC08F-6 cables connect the M781 Module to the PC05 Reader/Punch (only one cable is needed for a PR11).

1.2.2 Environmental Specifications

The PC11 environmental requirements are as follows:

	Operating	Nonoperating
Temperature:	55° – 100°F ambient	30° – 130°F ambient
Humidity (noncondensing):	20% – 95% ambient	5% – 95% ambient

1.2.3 Power Requirements

The PC11 Control logic draws all necessary power from the H720 Power Supply, located in the mounting box. The power required is approximately 1A at +5V.

CHAPTER 2
INSTALLATION

This chapter contains the procedures necessary for installing the PC11 Control. The installation procedure is a function of the system configuration and the address and priority assignments, which dicate the presence or absence of jumpers. When a configuration has been selected, the user must assign and implement addresses, interrupt vectors, and priorities. After the hardware modifications required for the selected values have been completed and the physical components of the system have connected, the installation can be verified by testing the new hardware and the system.

2.1 CONFIGURATIONS

The PC11 Control is available in one standard configuration that includes a PC05C Reader/Punch. The PR11 Reader Control is a similar configuration to the PC11; however, it requires only one BC08F cable. This configuration is used to control a PC05R Paper-Tape Reader.

2.2 CABLING AND TERMINATIONS

The PC11 module set fits into slots in a system unit. These slots are, in turn, connected to the Unibus signal paths by back-panel wiring. Signals are transmitted from the PC11 to the PC05 through two BC08F cables that plug into two connectors on one side of the M781 Reader/Punch Control Module. The BC08F cable is a Flexprint® cable terminated by *a)* an M903 Connector Module that plugs into the PC05 and *b)* an M925 right-angle Flexprint Connector Module that plugs into the M781 Module. The reader signal cable plugs into the connector closest to the pins of the M781 Module; the punch signal cable plugs into a connector head near the handle of the module.

2.3 ADDRESS AND PRIORITY ASSIGNMENTS

Each PC11 uses four device register addresses, two interrupt vector addresses, and two bus priority level assignments. There are certain constraints, however: *a)* the device register addresses must be four contiguous word addresses with least significant digits ranging from 0 to 6; *b)* the two interrupt vectors must be directed to contiguous vector addresses differing only in the least significant digit; *c)* and the two interrupt priorities (bus priority level assignments), one for the punch and one for the reader, must be on the same major priority level. Consequently, only three hardware assignments are required.

The device register addresses are assigned by the M105 Address Selector Module. The M105 Module that is supplied with the PC11 is preset by jumpers to respond to addresses between 777550 and 777557. A different series of addresses can be selected by changing the jumper arrangement, but care must be taken to use addresses not assigned to other devices in the system. Any change from DEC-assigned addresses requires reprogramming, before the DEC-supplied system programs and diagnostic programs will operate with the system. The order in which addresses are assigned to the device registers is presented in Paragraph 3.1.

The two interrupt vectors are: the reader interrupt vector, and the punch interrupt vector. The reader interrupt vector is normally assigned the value of 70 by jumpers on the M782 Interrupt Control Module. The punch interrupt vector, which differs only in address bit 2, has the value 74. These values can be changed by modifying the jumper arrangement. The same cautions listed for the device register addresses must be adhered to for the interrupt vector addresses.

The bus major priority level is determined by a request and grant jumper that plugs into a receptacle on the M781 Module. The M781 Module is normally supplied with a jumper that connects the BR4 priority level to the M782 Module; however, this jumper may be replaced with one that selects a higher priority level if desired. The reader has a higher priority level than the punch if both request service simultaneously, because the bus grant signal must pass through the reader interrupt logic before reaching the punch interrupt logic.

2.4 POWER CONNECTIONS

The PC11 Control draws all electrical power from the system unit in which it is mounted. Power is supplied to the system by the H720 Power Supply, located in the mounting box. This power supply is described in the *H720 Power Supply and Mounting Box Manual* (DEC-11-HR5A-D). The PC05 Reader/Punch includes an integral power supply that is connected to the system power supply; status signals from the PC05 to the PC11 include signals that indicate whether the power supply is connected to the main voltage.

2.5 INSTALLATION VERIFICATION

When all system components have been connected and adjusted, the installation can be verified by running the PC11 High-Speed Reader and Punch Diagnostic Test (MAINDEC-11-D2BB-D).

NOTE

The DEC-supplied test will operate only with the standard address and interrupt vector assignments.

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CHAPTER 3
OPERATION AND PROGRAMMING

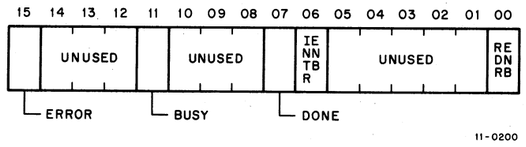
This chapter describes the operation and programming of the PC11 Reader/Punch and Control. The PC11 Control responds to processor commands through operations that are initiated and controlled by bits in the device registers. The device registers are presented in Paragraph 3.1. Technical details in the application of these registers are described in Paragraphs 3.2 through 3.4. Paragraph 3.5 provides examples for programming the device, and Paragraph 3.6 describes the program modifications required to restructure the system.

The PC05 Reader/Punch has manual power controls and manual feed switches, located on the front panel, for operation of the tape advance feature of both the reader and punch. All other operations of the PC05 are program-controlled.

3.1 DEVICE REGISTERS

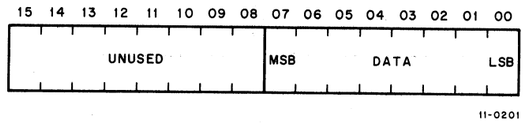
The PC11 comprises four device registers (the PR11 uses only the first two device registers, which are assigned to the read function). These registers are described in order of ascending addresses. The descriptions that follow include: *a)* the normally assigned address, *b)* the mnemonic suggested for use with the PAL-11 assembly program to address the register, and *c)* a bit assignment map illustrating the use of each register.

Name: Paper-Tape Reader Status Register
Mnemonic: PRS
Address: 777550



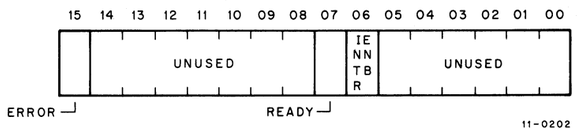
Bit	Name	Function
00	Reader Enable (RDR ENB)	Write-Only. Always reads as a 0. If a 1 is output to this bit, a read cycle is started, BUSY is set, DONE is cleared, and the PRB is cleared.
06	Reader Interrupt Enable (RDR INTR ENB)	Read/Write. When this bit is set, DONE or ERROR becoming set causes an interrupt.
07	DONE	Read-Only. This bit is set when a new data byte is available and cleared when RDR ENB is set, or the PRB is read. If RDR INTR ENB is set, an interrupt occurs.
11	BUSY	Read-Only. This bit indicates that the reader is completing an operation. BUSY is set when RDR ENB is set, and cleared when the present operation is complete (DONE is set).
15	ERROR	Read-Only. This bit is set to indicate that one of the following conditions has occurred: *a)* reader out of tape, *b)* reader off-line, *c)* no power to reader. This bit causes an interrupt if RDR INTR ENB is set. If the error condition has not been cleared manually, and an attempt to set RDR ENB is made, an immediate interrupt occurs, and no operation is initiated.

Name: Paper-Tape Reader Buffer Register
Mnemonic: PRB
Address: 777552



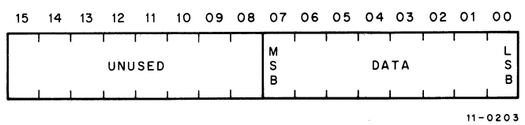
Bit	Name	Function
07-00	Data (07:00)	This register transfers eight bits of data from the PC05 reader to the Unibus. The register is read-only; it responds to DATO operations, but the contents of the register are unchanged. The most significant bit of register is bit 07, and the least significant bit is bit 00. (For more information on the bit assignments in the PC05, PC11, and PDP-11 Systems, refer to Appendix A.)

Name: Paper-Tape Punch Status Register
Mnemonic: PPS
Address: 777554



Bit	Name	Function
06	Punch Interrupt Enable (PUN INTR ENB)	Read/Write. When this bit is set, either READY or ERROR can cause an interrupt.
07	READY	Read-Only. This bit signifies that the punch can accept a byte for transfer to the paper tape. This bit is set when the current operation is completed, and cleared when the PPB is loaded. This bit causes an interrupt if PUN INTR ENB is set.
15	ERROR	Read-Only. This bit indicates that one of the following conditions has occurred: *a)* punch out of tape, *b)* no power to punch. If PUN INTR ENB is set, this bit causes an interrupt. If an attempt to punch a character is made before the error condition has been manually corrected, an immediate interrupt can occur.

Name: Paper-Tape Punch Buffer Register
Mnemonic: PPB
Address: 777556



Bit	Name	Function
07-00	Data (07:00)	Write-Only. Loading a byte into the PPB register clears READY in the PPS register and begins a new cycle of punch operation. The previous contents of the PPB register (which cannot be read to the bus) are replaced with the new data from the bus. Refer to Appendix A for information on the bit assignments in the PC05, PC11, and PDP-11.

3.2 ADDRESSES

The standard addresses for the PC11 device registers are listed in Paragraphs 1.1 and 3.1. The addresses assigned to these registers must be four contiguous word addresses, with bits 17–13 all 1s and bits 12–3 identical for all four addresses. Consequently, the addresses must be in the form n, n+2, n+4, and n+6, where n is divisible by eight and is in the range 760000 to 777770.

The addresses selected must not be assigned to any other device on the Unibus. Certain addresses in this range are assigned to internal storage within the KA11 Processor; these addresses, which must not be assigned to any device, are listed in the *Unibus Interface Manual.*

The address assignments for the PC11 must maintain the device register sequence of the standard assignments. This sequence is shown in Table 3-1.

Table 3-1
Sequence of Standard Assignments

Device Register Mnemonic	Relative Address
PRS	N
PRB	N+2
PPS	N+4
PPB	N+6

3.3 TIMING CONSIDERATIONS

The timing of PC11 Control Operations is dictated by a cycle of operations in the PC05, which is dependent on the direction of the data transfers. For each data transfer, the PC05 Reader/Punch executes a cycle of operations that includes positioning the paper tape, conducting an internal data transfer, and participating in a data transfer with the Unibus (through the PC11 Control).

3.3.1 Reader Timing

When the RDR ENB bit of the PRS register is set for a previously inactive reader (BUSY=0), the PC11 clears the DONE bit of the PRS register and sets the BUSY bit. The frame of the paper tape currently over the read head is transmitted to a buffer register in the PC05, and the PC05 begins moving the paper tape to position the next frame over the read head. When the buffer is loaded, the DONE bit of the PRS register is set, signifying that a byte is ready to transfer. The BUSY bit is cleared. When the PRB is read (addressed), the DONE bit is cleared.

The processor can transfer the contents of the PRB register as soon as the DONE bit becomes set. If the processor sets the RDR ENB bit again, the DONE bit is cleared again, and the PC11 Control is ready to begin another reader cycle as soon as the paper tape is repositioned. The programmer does not have to test the BUSY bit or wait until it is clear before beginning another cycle.

When the reader is started from idle, the first character is read immediately, and the tape is advanced. This tape advance is controlled by the reader clock in the PC05. The reader clock produces pulses that: *1)* control the stepping motor that advances the tape, *2)* strobe the data into the reader buffer, *3)* set the reader flag when new data is available, and *4)* determine when to stop the movement of the paper tape. During continuous operation, the clock maintains a character rate of 300 character/second by running on a 3.33 ms cycle. This speed is maintained as long as the PC11 receives another read command within 1/2 cycle (1.67 ms) after the DONE bit of the PRS is set. If no further read operations are requested, the reader stops the tape.

A late read command is not executed until the reader has come to a stop, then the tape motion is started again. The starting motion is slower than the continuous motion because it must accelerate the tape from a standstill. The reader clock is controlled by an acceleration circuit that extends the first few clock periods while the tape is reaching proper operating speed. Therefore, when the tape is moved in a start-stop fashion (because the read commands are not frequent enough to maintain continuous motion), the reader operates at a slower rate. The maximum speed for single-character operation (which occurs whenever the read commands are more than 1.67 ms apart) is approximately 25 characters per second.

The PC11 operating speed will affect the total time necessary to complete a data transfer program; however, it does not change the instruction sequence. The programming necessary to control a PC11 is independent of the operating speed.

3.3.2 Punch Timing

The PC05 Punch operates at a fixed cycle time of 20 ms, resulting in a punching rate of 50 characters per second. If the punch is idle, and a punch command is received (the PPB is loaded): *1)* the punch motor is turned on, *2)* the punch mechanism accelerates up to speed while a one-second timer delays punching, *3)* the punch unit punches the data into the tape and advances the tape one frame, and *4)* the PC05 signals that it is ready to begin another operation.

A second timer keeps the punch running for three seconds after the last punch command is executed (the timer restarts after each punch command). When the punch motor is running, any punch command received within 10 ms after the READY bit of the PPS is set is executed during the next punch cycle. Punch commands that are delayed more than 10 ms after READY is set are delayed until the following punch cycle (an extra delay of 20 ms).

The timing considerations for the punch affect only the throughput of the PC11, not the programming. The instructions required to operate the PC11 Reader/Punch and Control are independent of the effective speed of operation.

3.4 DATA FORMATS

The paper tape processed by the PC11 Reader/Punch and Control is 1-in. wide, eight-channel tape. Each byte of data is punched into one frame that consists of eight data positions arranged in a line perpendicular to the length of the tape. A hole punched in a data position represents a 1, and a 0 is represented by the absence of a hole.

The data positions are numbered from 0 to 7, with 0 the least significant bit and 7 the most significant bit. The feed hole, which is punched for every frame, is positioned between channels two and three (a channel is composed of one data position in successive frames of tape, i.e., a row of holes and unpunched positions extending the length of the tape). Figure 3-1 illustrates the tape format.

3.5 PROGRAMMING EXAMPLES

The PC11 Control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch, and either device can be under direct program control or can operate without direct supervision through the use of interrupts, to maintain continuous operation.

The examples provided in this section illustrate four types of programs that can be used with the PC11. These programs include: *a)* direct control of the reader, *b)* interrupt control of the reader, *c)* direct control of the punch, and *d)* interrupt control of the punch.

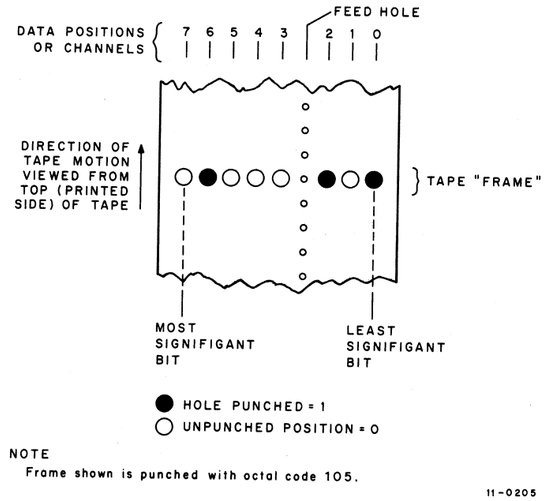


Figure 3-1 Paper-Tape Format

3.5.1 Program Control of the Reader

The sequence of instructions that follows reads one byte from the paper tape and deposits it in general register 0. If a reader error is sensed, the program branches to an error routine, which may type out a message and then wait for operator intervention.

```
        .
        .
READ:   INC     PRS
LOOP:   TST     PRS             ;SET RDR ENB
        BMI     ERR             ;LOOK FOR ERROR
        TSTB    PRS             ;BRANCH ON ERROR=1
        BPL     LOOP            ;LOOK FOR DONE
        MOV     PRB,    R0      ;WAIT IF DONE=0
        .                       ;READ CHARACTER
        .
```

A shorter form of the test loop is possible, as shown below:

```
        .
        .
READ:   INC     PRS
LOOP:   BIT     #100200,PRS     ;TEST BITS 15 and 7
        BEQ     LOOP            ;WAIT IF NO BITS SET
        BMI     ERR             ;ERROR IF BIT 15 SET
        MOV     PRB,    R0      ;IF BIT THAT IS SET IS
        .                       ;NOT BIT 15, MUST BE
        .                       ;BIT 7
```

3.5.2 Reader Interrupt Service

The PDP-11 System can combine PC11 operations with other processing by using the interrupt mode of device operation. When a device operation has been initiated, the PC11 continues without supervision until the operation is complete (or an error occurs); the remainder of the PDP-11 System is free to perform other operations. When the PC11 Control requires further service, the processor is notified by an interrupt.

Each device that is operated in an interrupt mode must be initialized by commands from the processor. An interrupt service routine and an interrupt vector (at the address corresponding to the vector address selected by the jumpers on the M782 Module) must be provided.

The program that follows can be used to read a block of 128 characters from the paper tape to a buffer.

```
START:    MOV     #-200,    R0          ;INITIALIZE COUNTER
          MOV     #101,     PRS         ;SET INTR ENB AND RDR ENB
HANG:     BR      HANG                  ;HANG UP HERE UNTIL BLOCK
                                        ;IS READ
                  .
                  .
70:       RDRINT                        ;VECTOR TO INTERRUPT ROUTINE
72:       200     .                     ;SETS STATUS TO PRIORITY 4
                  .
RDRINT:   TST     PRS                   ;TEST FOR ERROR
          BMI     ERR                   ;TYPE OUT MESSAGE IF ERROR
          MOVB,   PRB,      BUFEND(R0)  ;FILL BUFFER STARTING AT
                                        ;BUFEND-200 (OCTAL)
          INC     R0                    ;COUNT ONE BYTE AND MOVE POINTER
          BEQ     OUT                   ;WHEN COUNT IS ZERO, EXIT LOOP
          INC     PRS                   ;ENABLE READER AGAIN
          RTI                           ;RETURN FROM INTERRUPT
OUT:      ADD     #4,       SP          ;UNSTACK INTERRUPT PC AND PS
          CLR     PRS                   ;INHIBIT FURTHER INTERRUPTS
          JMP     HANG+2                ;CONTINUE MAIN PROGRAM
```

NOTE

The position of the buffer used by this program is specified by the end of the buffer, not the beginning. The indexed address uses the negative counter values to access bytes at decreasing distances from this base address.

Two operations performed by this program require caution. When a program accesses the same or contiguous locations, the program operating speed increases if the locations are addressed through a register. If this is done, either no other use can be made of this register or: *a)* the interrupt service routine must stack the former contents of the register, *b)* the counter must be moved from a temporary storage location to the register, *c)* the register must be used, and *d)* the storage operations reversed. In this example, where the processor does not do any other processing, no conflicts with the use of the register occur.

A second caution refers to the terminating exit from the service routine. When the exit does not occur through an RTI instruction, the main program PC (*Program Counter*) and PS (*Processor Status*) words that are stacked by the interrupt must be removed from the stack. The ADD instruction at OUT performs this operation. If this operation is not performed, the values stacked by other operations previous to the interrupt are not properly accessible.

3.5.3 Punch Programmed Service

The sequence of instructions that follows transfers one byte from register 0 to the paper tape. When controlling the punch, the READY bit of the PPS register is checked before the transfer; when controlling the reader, the DONE bit of the PRS register is checked after a command.

```
                  .
                  .
PUNCH:    BIT     #100200,  PPS         ;CHECK PUNCH STATUS
          BEQ     PUNCH                 ;IF NOT READY OR ERROR, WAIT
          BMI     ERROR                 ;PROCESS ERROR IF ANY
          MOV     R0,       PPB         ;OUTPUT CHARACTER
                  .
                  .
```

3.5.4 Punch Interrupt Service

This interrupt service routine outputs 8-bit codes to the paper tape, unless they are ASCII representations of the formatting characters Line Feed, Rubout, or Form Feed. Line Feeds and Rubouts are ignored (not punched), and the program stops punching when the character read from the buffer is a Form Feed. The Form Feed is not punched. The program transfers the contents of a buffer: *a)* starting at a preselected address to paper tape, *b)* stopping automatically when it reads an end-of-buffer character, and *c)* performing simple character editing.

The interrupt service routine is called into operation when the following sequence of instructions is encountered in the main program:

```
                  .
                  .
R0 = %0                                 ;REGISTER ZERO
SP = %6                                 ;REGISTER SIX
PC = %7                                 ;REGISTER SEVEN
PS = 177776                             ;PROCESSOR STATUS WORD
CLR       PUNDON                        ;CLEAR SOFTWARE FLAG
MOV       #BUFFER   POINTER             ;SET UP BUFFER POINTER
MOV       #100,     PPS                 ;SET PUNCH INTR ENB
                  .
                  .
                  .
```

This instruction sequence sets up the system by initializing the service routine and enabling interrupts from the punch.

If the punch is idle, an interrupt occurs immediately; otherwise, the first interrupt is delayed until the current operation is completed. The software flag is used by the main program to provide a check on the progress of the output. This occurs in the following manner: The main program continues with other processing until the use of the punch is required, or further processing is dependent on completion of the output. At this point the sequence of instructions shown below is executed:

```
LOOP:     TST     PUNDON                ;CHECK SOFTWARE FLAG
          BPL     LOOP
```

If the interrupt service routine has not set the flag, the processor stays in this wait loop, allowing interrupts for further output operations, until the routine signals that it is finished.

In this example, the interrupt routine to service the punch requires the following sequence of instructions:

```
                .
                .
                .
74:     PCHINT                          ;VECTOR TO ROUTINE
76:     200                             ;NEW STATUS WORD

                .
                .
PCHINT: MOV     R0          -(SP)       ;SAVE REGISTER ZERO
        MOV     POINTER,    R0          ;SETUP REGISTER
        TST     PPS                     ;CHECK NO ERRORS
        BMI     ERROR                   ;IF ERROR, EXIT WITH LAST
                                        ;BUFFER POSITION IN R0
RETEST: CMPB    (R0),       #212        ;LINE FEED?
        BNE     TEST2                   ;NO, CONTINUE
        INC     R0                      ;YES, IGNORE CHARACTER,
        BR      RETEST                  ;AND TEST NEXT CHAR.
TEST2:  CMPB    (R0),       #377        ;RUBOUT?
        BNE     TEST3                   ;NO, CONTINUE
        INC     R0                      ;YES, IGNORE
        BR      RETEST
TEST3:  CMPB    (R0),       #214        ;FORM FEED?
        BEQ     OUT                     ;YES, EXIT
        MOVB    (R0)+,      PPB         ;NO, OUTPUT CHARACTER
        MOV     R0,         POINTER     ;SAVE REGISTER
        MOV     (SP)+,      R0          ;UNSTACK PREVIOUS CONTENTS
        RTI                             ;NORMAL RETURN
OUT:    MOV     (SP)+,      R0          ;RESTORE TO PREVIOUS STATUS
        COM     PUNDON                  ;SET SOFTWARE FLAG
        RTI
POINTER: 0
PUNDON:  0
```

3.6 RESTRUCTURING THE SYSTEM

When a PC11 device changes address, or multiple PC11 devices are included in a system, the system software must be changed to reflect the changes in the device. Similar changes are required whenever the interrupt vector address or the priority level of a PC11 device changes.

Many of the systems programs, provided for use with the PC11, address the device registers indirectly through pointer locations. These locations can be changed to represent the new values of the device register addresses. Where the program addresses the device registers directly (through symbolic names that have been assigned the values of the addresses), the program can be reassembled with new values assigned to the symbolic names.

When the interrupt vectors are changed, the new addresses can be easily patched into the program, because only four bytes are affected.

NOTE

Be certain not to assign the interrupt vectors to any locations that may be required for other devices.

Any changes in the bus priority level are reflected by changes in the processor priority level stored in the second word of the interrupt vector. Normally, this processor priority is the same as the bus priority assigned to the PC11. (Hardware changes involved in reconfiguring a PC11 System are described in Paragraph 2.3.)

CHAPTER 4
DETAILED DESCRIPTION

The PC11 Control logic can be divided into three functional sections: *a)* the selection logic, *b)* the interrupt logic, and *c)* the data transfer logic. The data transfer logic can be further divided in two parts, relating to input and output transfers.

Figure 4-1 is a detailed block diagram of the logic in the PC11 Control. The print set contains the circuit schematics for this logic. The selection logic (which determines the register participating in a data transfer and the direction of the transfer) comprises the M105 Address Selection Module and parts of the M781 Module. The interrupt control logic comprises the M782 Interrupt Control Module, the interrupt enable logic on the M781 Module, and the priority selection chip on the M781 Module. The data transfer logic comprises the gating, timing, and condition sensing logic of the M781 Module.

4.1 SELECTION LOGIC

When the address information transmitted on the A-lines (Address Lines) of the bus matches the address encoded by the jumpers in the M105 Module, the module produces one of four register selection signals (indicating that one of the registers is being referenced); the module also produces one or more (of three) data direction signals, indicating the type of Unibus data transfers being performed. A detailed description of the logic on the M105 Module (and also of the M782 Interrupt Control Module) is contained in the *Unibus Interface Manual* (DEC-11-HIAB-D).

4.1.1 Gating Logic

The register selection signals and the data direction signals are combined by logic on the M781 Module to determine the data transfer that takes place (refer to Table 4-1). In some cases, no action takes place other than the transmission of SSYN by the M105 Module. A DATO to the PRB register or a DATI to the PPB register has no effect on the M781 Module, and no data transfer takes place between the M781 Module and the Unibus.

4.1.2 Bus Receivers and Drivers

The M781 Module has one set of eight bus receivers that connect the inputs of the four device registers to Unibus lines D (07:00). Each register is gated separately. The PRS and PPS registers each include one flip-flop that can be loaded from line D06 to store the Interrupt Enable for the corresponding device. The PRS register also requires a gate to transmit RDR ENB from line D00 to the reader. All other bits of these registers are read-only and do not receive information from the bus.

Table 4-1
Data Transfer Functions for
Gating Signals

Gating Structure	Function
SELECT 0 · IN	Gates PRS to bus.
SELECT 0 · OUT LOW	Gates bus to PRS (loads RDR INT ENB and RDR ENB).
SELECT 2 · IN	Gates PRB to bus.
SELECT 4 · IN	Gates PPS to bus.
SELECT 4 · OUT LOW	Gates bus to PPS (loads PUN INT ENB).
SELECT 6 · OUT LOW	Gates bus to PPB (produces IOP4 that loads punch buffer).

The PRB register is also read-only and does not accept information from the bus. The PPB register, however, is write-only; information from the bus is gated to a buffer in the punch, along with a signal to start a punch operation.

Each register that can supply data to the Unibus has a separate transmission system. The PRS and PPS registers each have bus drivers that transmit the status bits for the two devices; only bit 0 of the PRS is not transmitted to the bus. The PRB register requires eight bus drivers to gate a byte of data from the buffer register in the reader to the bus. The PPB register does not transmit data to the bus.

4.2 INTERRUPT CONTROL LOGIC

The PC11 Control can initiate an interrupt service routine by executing an interrupt bus operation. This occurs when one of two interrupt control sections in the M782 Module has both an interrupt and an interrupt enable signal asserted. The interrupt enable signal is supplied by a flip-flop in the status register; the interrupt signal can be asserted by one of a number of conditions.

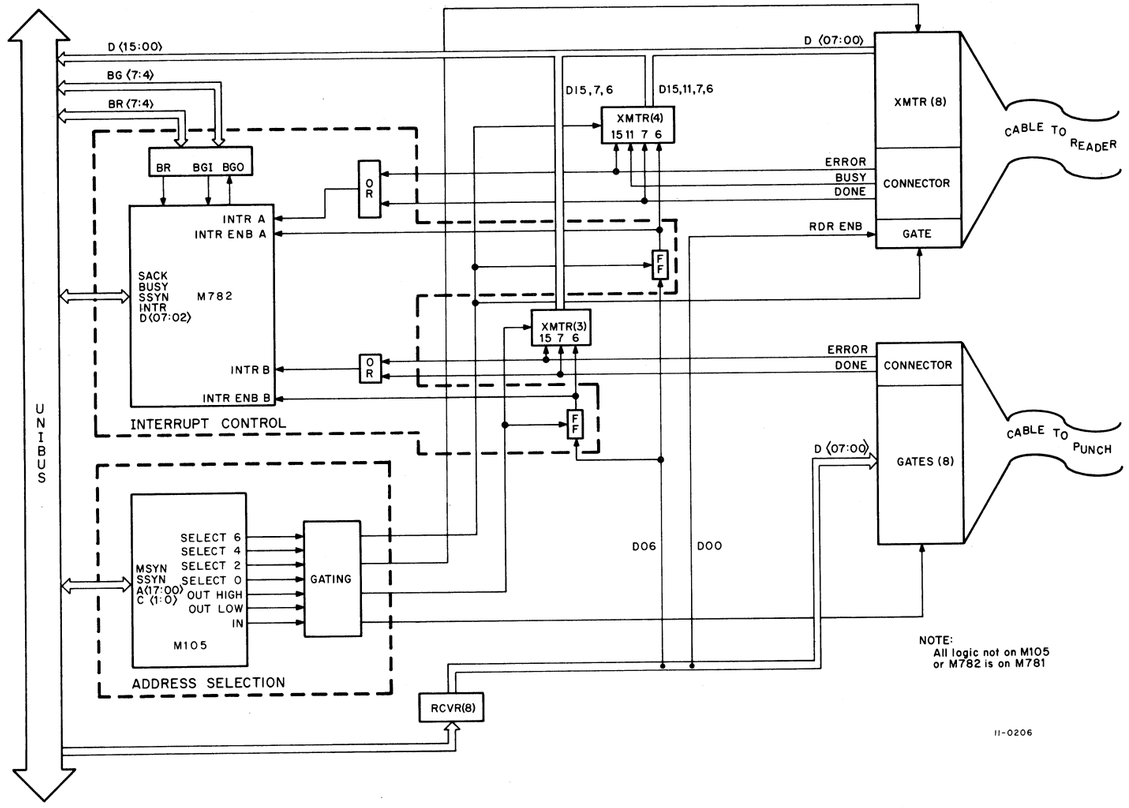


Figure 4-1 Detailed Block Diagram

If bit 6 of the PRS is set, an interrupt enable signal is provided to the Master Control A Section of the M782 Module. When either RDR DONE or RDR ERROR is asserted in the PRS, the corresponding signal generates an interrupt signal to the Master Control. This control initiates a bus request on a priority level selected by a jumper insert on the M781 Module. When the device receives bus control, the M782 Module asserts an interrupt and a vector address.

If the interrupt enable signal is cleared before the bus request is honored, no interrupt occurs. Similarly, if the condition that caused the interrupt is removed before the bus request results in a bus grant, no interrupt occurs.

Bit 6 of the PPB register provides an interrupt enable signal to the Master Control B. When either PUN READY or the punch error signal is set in the PPB, an interrupt sequence begins that is identical to that for a reader interrupt; however, the interrupt vector address that is transmitted is different. For a punch interrupt, the vector address is higher (bit 2 is set) than the address for a reader interrupt.

4.3 OUTPUT LOGIC

The PC05 Reader/Punch contains internal data buffering and provides complete control of one timing cycle. The only output logic required of the PC11 Control is the gating logic between the Unibus and the punch and reader connectors. This gating logic controls when a byte of data is sent to the punch, when a start signal is sent to the punch, or when a start signal is sent to the reader.

4.4 INPUT LOGIC

The input logic is involved in transfers that transmit data to the Unibus. The M781 Module provides gating that controls the transmission of: *a)* a byte of data from the reader, or *b)* status information from one of two status and control registers onto the Unibus.

CHAPTER 5
MAINTENANCE

This chapter covers the equipments and techniques necessary to maintain the PC11 High-Speed Paper-Tape Reader/Punch and Control. The *PC05 Maintenance Manual* (DEC-00-HGHA-D) provides information on the maintenance of the PC05 Reader/Punch. This chapter also lists the equipments and programs useful in determing the operating status of the system and describes some basic techniques for isolating and repairing faults in the PC11 hardware.

5.1 TEST EQUIPMENT AND PROGRAMS

Table 5-1 lists a variety of tools useful in testing and repairing the PC11 Control. The PC11 Control consists of only three modules; consequently, it is possible to correct faulty operation by swapping modules, and no tools are actually necessary to repair the control. Fault isolation and checking for marginal conditions is much easier in the PC11 because of this design.

Table 5-1
Test Equipment and Tools

Equipment	Item	Type
Test Equipment	Oscilloscope	Tektronix Model 453 (or equivalent)
	Volt-Ohmmeter	Triplett Model 630 (or equivalent)
Devices	Extender Board	One W984A double-extender board
		Two single-extender boards (a W984 board divided in half)
	Maintenance Module Set	One W130 One W131
	IC Test Clip	
	Pin probe tip	Tektronix #30
	Pointed-tip solder iron	Rated at less than 40W
	Package of solder wick	Used for removal of solder on printed circuit boards.
Tools	Screw drivers Allen wrench set Needle-nose pliers Wire strippers	
	Paper-Tape Gauge	DEC Part No. 18-09211

The maintenance philosophy for the PC11 Reader/Punch and Control is based on system checkout using test programs. The diagnostic programs, supplied by DEC, can be used to verify correct operation of the equipment or to indicate possible sources of malfunction. These maintenance programs are as follows:

MAINDEC-11-D2BB-D	PC11 High-Speed Reader and Punch Test Instructions
MAINDEC-11-D2BB-PB	PC11 High-Speed Reader and Punch Test Program

5.2 PREVENTIVE MAINTENANCE

Improper operation of the PC11 Reader/Punch can be caused by a dirty reader or by an unlubricated punch. The reader photocells should be examined for dirt each time a tape is loaded into the reader and should be cleaned with a nonabrasive cleaning agent at regular intervals. The paper-tape punch should be lubricated regularly, and the paper tape output should be compared to the standard (as represented by the paper-tape gauge, Part Number 18-09211, available from DEC) for hole spacing. Make certain that the holes are properly shaped; poorly shaped holes may indicate a worn punch block that needs replacement.

In addition to these maintenance procedures, the system should be fully checked at regular intervals by running the MAINDEC programs to verify correct operation and to identify marginal conditions. Many apparent operating errors are caused by incorrect or improperly operating programs; these errors can be identified by using the diagnostic programs to determine that the errors are not caused by the hardware.

5.3 CORRECTIVE MAINTENANCE

When it has been verified that the PC11 Reader/Punch and Control is not operating correctly, the fault must be isolated and corrected. Often the nature of the errors encountered when running the diagnostic programs indicate the type of fault, or the possible locations of faulty components. However, further testing may be required to determine the exact problem.

APPENDIX A
SIGNAL CORRELATIONS

The following tables provide signal correlations between the PC11 and PC05 devices.

Table A-1
Reader Data Signals

Comment	PC05	PC11	Unibus
Least significant bit (LSB), nearest back of reader	RD1	I/O BUS IN 11	BUS D 00
	RD2	I/O BUS IN 10	BUS D 01
	RD3	I/O BUS IN 09	BUS D 02
	RD4	I/O BUS IN 08	BUS D 03
	RD5	I/O BUS IN 07	BUS D 04
	RD6	I/O BUS IN 06	BUS D 05
	RD7	I/O BUS IN 05	BUS D 06
Most significant bit (MSB), at front of reader	RD8	I/O BUS IN 04	BUS D 07

Table A-2
Punch Data Signals

Comment	Unibus	PC11	PC05	Punch
LSB, right-side of reader; tape is upside down	BUS D 00	BD 00	(AC11 (1))	PB 7
	BUS D 01	BD 01	(AC10 (1))	PB 6
	BUS D 02	BD 02	(AC09 (1))	PB 5
	BUS D 03	BD 03	(AC08 (1))	PB 4
	BUS D 04	BD 04	(AC07 (1))	PB 3
	BUS D 05	BD 05	(AC06 (1))	PB 2
	BUS D 06	BD 06	(AC05 (1))	PB 1
MSB, left-side of reader	BUS D 07	BD 07	(AC04 (1))	PB 0

Table A-3
Reader Control Signals

PC05 Name	PC11 Name	Function
IOP 1 (1)	Not used	Not used
IOP 2 (1)	SELECT 2 * IN	PRB selected
IOP 4 (1)	SELECT 0 * OUT * BD 00	Read command
I/O BUS SKIP	Not used	Not used
I/O BUS INTR	DONE	BUS D 07 (done)
RDR RUN (0)	BUSY	BUS D 11 (busy)
RDR OUTAPE	RDR ERR	BUS D 15 (error)
QUALIFY		Always set
RDR INITIALIZE	B INIT	BUS INIT

Table A-4
Punch Control Signals

PC05 Name	PC11 Name	Function
IOP 1 (1)	Not used	Not used
IOP 2 (1)	Not used	Not used
IOP 4 (1)	SELECT 6 * IN	PPB selected
PUN ACTIVE	PUN READY	BUS D 07 (done)
PUN OUTAPE	ERROR	BUS D 15 (error)
PUN QUALIFY		Always set
I/O BUS SKIP	Not used	Not used
I/O BUS INTR	Not used	Not used
PUN INITIALIZE	B INIT	BUS INIT

APPENDIX B
ENGINEERING DRAWINGS

ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each PC11 System. Each manual in the basic series contains a complete set of reduced engineering drawings of the component described in the manual. The general logic symbols used on these drawings are described in the *DEC Logic Handbook*, 1970. Specific symbols as well as special ICs and circuits are discussed in the *KA11 Processor Manual*.

If any discrepancy exists between the reduced drawings in the manuals and the drawings supplied with the system, the drawings furnished with the system take precedence.

TERMINOLOGY

The final manual in the basic series, *PDP-11 Conventions*, includes a list of terminology and abbreviations used throughout the basic series as well as a glossary.

Table B-1
Engineering Drawings

Drawing	Sheets	Page
A-PL-PC11-0-0	1	B-2
D-CS-M781-0-1	3	B-3, -4, -5
D-BS-PC11-0-2	1	B-6
D-MU-PC11-0-MU	1	B-7
D-AR-PC11-0-4	1	B-8

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY P. MARCOTTE DATE 4/2/70	CHECKED AL PFYFFER DATE 4/14/70	SECTION 1
ENG RE Jones DATE 5/4/70	PROD Thomas Ward DATE 5/5/70	ISSUED SECT. 1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION PC11-Ø-Ø(60HZ)	PC11-A-Ø(50HZ)
1	A-PL-DD11-A-Ø	PERIPHERAL MOUNTING PANEL	1	1 (IF REQUIRED)
2	A-PL-PC11-Ø-MU	MODULE UTILIZATION	1	1
3	C-SC-1209[illegible]-Ø-Ø1	MODULE HOLDER	A/R	A/R
4.	D-UA-BCØ8F-6-Ø	BCØ8F CABLE 6FT.	2	2
5	D-UA-PCØ5-C-Ø	PCØ5-C, PUNCH, READER, DRIVER	1	
6	D-UA-PCØ5-CA-Ø	PCØ5-CA, PUNCH, READER, DRIVER		1
REF	D-AR-PC11-Ø-4	OPTION ARRANGEMENT	1	

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
LS PAPER TAPE RDR & PUNCH	SHEET 1 OF 1	A	PL	PC11-Ø-Ø		
		DIST.				

DEC FORM NO.
DRA 110

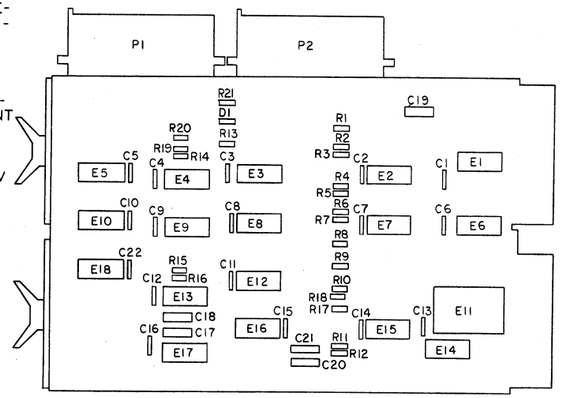
PARTS REFERENCE

ITEM NO	DRAWING REFERENCE	DESCRIPTION		PART NUMBER	QUANTITY
1	E1,E3,E4,E6,E13	DEC 8881	I.C.	1909705	5
2	E2,E7,E12,E15,E17,E18 E14	DEC 7400	I.C.	1905575	7
3	E5,E8,E10,E16	DEC 380	I.C.	1909485	4
4	E9	DEC 7474	I.C.	1905547	1
5	E11	I.C. SOCKET		1209838	1
6	C1-C16,C22	.01 MFD 100V 20%	CAP.	1001610	17
7	C17,C18,C19	6.8 MFD 35V 20%	CAP.	1000057	3
8	C20,C21	680 PFD 500V 10%	CAP.	1005726	2
9	R1,R11,R12,R14,R16,R18,R19,R20	1000 1/4W 5%	RES.	1300365	8
10	R2-R10	470 1/4W 5%	RES.	1300316	9
11	R13,R15	100 1/4W 5%	RES.	1300229	2
12	R17	220 1/4W 5%	RES.	1300271	1
13	P1,P2	H807 36 PIN CONN		7003512	2
14	E11 INSERT STANDARD	PRIORITY JUMPER LEVEL #4		5408776	1
	E11 INSERT OPTIONAL	PRIORITY JUMPER LEVEL #5		5408778	0
	E11 INSERT OPTIONAL	PRIORITY JUMPER LEVEL #6		5408780	0
	E11 INSERT OPTIONAL	PRIORITY JUMPER LEVEL #7		5408782	0
	D1	D664 DIODE		1100114	1
	R21	4.7K 1/4W 5%		1300447	1

NOTES:

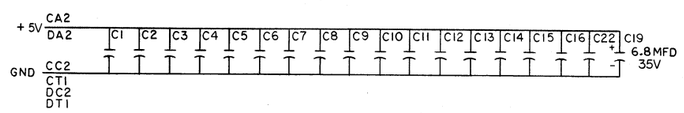
1. PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE OPTION. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT RIGHT.
2. DETAILS ON COMPONENTS ARE NOTED IN THE PARTS REFERENCE, PLACEMENT IS NOTED IN THE COMPONENT PLACEMENT DIAGRAM. CAPACITORS WITHOUT NOTED VALUES ARE .01 MFD.
3. GND AND 5V ARE USUALLY PIN 7 AND PIN 14, RESPECTIVELY THE EXCEPTION IS IC TYPE DEC 380, GND IS ON PIN 1 AND 5V IS ON PIN 8.
4. SEE MU FOR ACTUAL SLOT LOCATION.

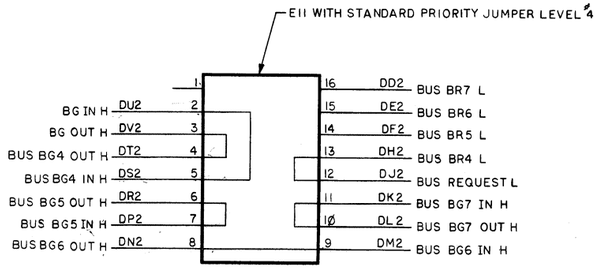
COMPONENT PLACEMENT



PIN NOMENCLATURE

MODULE	OPTION
A	C
B	D





REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP11

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —11—

FINISH —11—

		DATE
DRN		10-2-70
CHK'D		11/20/70
ENG		12/11/70
PROJ ENG		12/15/70
PROD.		DATE

NEXT HIGHER ASSY: A-ML-PCII-Ø

SCALE NONE

SHEET 1 OF 3

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PCII CONTROL

SIZE D | CODE CS | NUMBER M781-Ø-1 | REV A

ETCH REV B

DIST

P2 (READER CONNECTOR)

T1 F1 C1 A1 C2 F2 U2

P2 (READER CONNECTOR)

M1 P1 S1 V2 T2 S2 P2 M2 E1 D2 H1 H2 B1 E2

I/O BUS 11 L
I/O BUS 10 L
I/O BUS 09 L
I/O BUS 08 L
I/O BUS 07 L
I/O BUS 06 L
I/O BUS 05 L
I/O BUS 04 L
I/O BUS INT L
(IOP 1 (1) H)
RDR OUTAPE H
IOP 4 (1)
RDR RUN (1) L
IOP 2 (1) H

+5V R6 470
+5V R8 470
+5V R7 470
+5V R9 470
+5V R5 470
+5V R4 470
+5V R3 470
+5V R2 470
+5V R10 470
+5V R17 220
+5V R16 1K
R15 100
+5V R18 1K
+5V R11 1K
C18 6.8 MFD
C21 680 PFD

E7 7400 · E6 8881 · CS2 · BUS D00 L
E7 7400 · E6 8881 · CR2 · BUS D01 L
E7 7400 · E6 8881 · CU2 · BUS D02 L
E7 7400 · E6 8881 · CT2 · BUS D03 L
E2 7400 · E1 8881 · CN2 · BUS D04 L
E2 7400 · E1 8881 · CP2 · BUS D05 L
E2 7400 · E1 8881 · CV2 · BUS D06 L
E2 7400 · E1 8881 · CM2 · BUS D07 L

SELECT 2 H (PRB) DJ1 · E14 7400
BD00 H · E14 7400 · E14 7400
OUT LOW H DD1 · E15 7400 · E15 7400
BUS INIT L DL1
SELECT 0 H (PRS) DF1 · E15 7400
IN H DH1 · E15 7400
E16 380 · E12 7400
BD06 H · E9 RDR INT ENB 7474

RDR DONE H · E8 380 · E8 380 · DN1 · RDR INT H
E12 7400 · E3 8881 · CD2 · BUS D15 L
E16 380 · RDR ERR H
E12 7400 · E3 8881 · CH1 · BUS D11 L
RDR BUSY H · E3 8881
DM1 · RDR INT ENB H

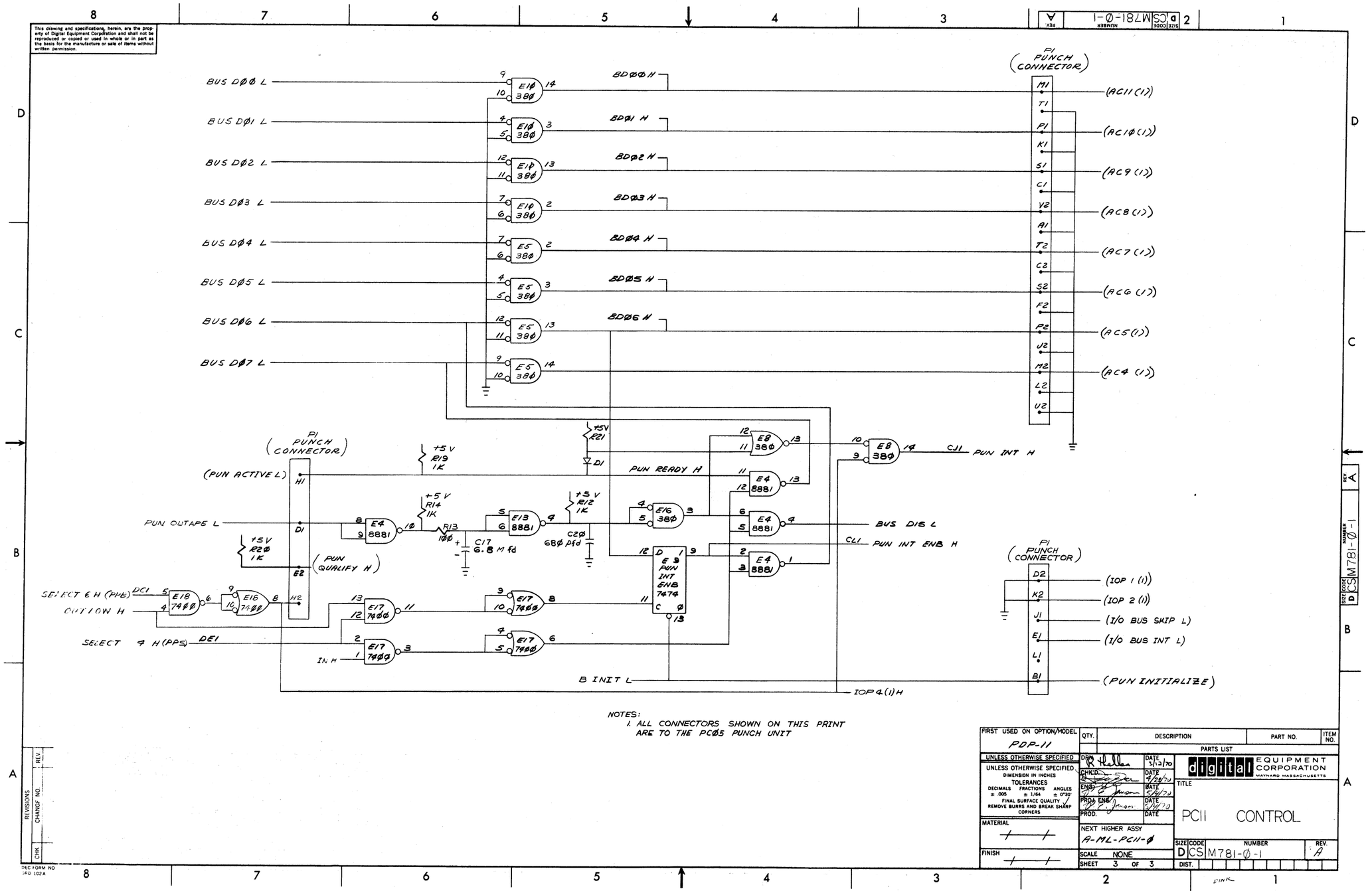
P2 (READER CONNECTOR)
+5V R1 1K
E2 (QUALIFY H)
J1 (I/O BUS SKIP L)
D1 B INIT L (RDR INITIALIZE L)
L1 (RDR INITIALIZE H)

NOTES:
1. ALL CONNECTORS SHOWN ON THIS PRINT ARE TO THE PC05 READER UNIT.

REVISIONS | REV | CHANGE NO | CHK

FIRST USED ON OPTION/MODEL: PDP-11	QTY.	DESCRIPTION	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED	PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS	DRN M Hellen DATE 3/12/70 · CHK'D DATE 6/23/70 · ENG DATE 3/6/70 · PROJ ENG DATE 3/11/70 · PROD. DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
MATERIAL —	NEXT HIGHER ASSY A-ML-PC11-0	TITLE PC11 CONTROL	
FINISH —	SCALE NONE · SHEET 2 OF 3	SIZE D · CODE CS · NUMBER M781-0-1 · REV. A · DIST.	

DEC FORM NO 3RD 102A



NOTES:
1. ALL CONNECTORS SHOWN ON THIS PRINT ARE TO THE PCØ5 PUNCH UNIT

FIRST USED ON OPTION/MODEL: PDP-11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN	K Hallen	DATE 3/13/70
CHK'D		DATE 4/28/70
ENG		DATE 5/4/70
PROJ ENG		DATE 5/11/70
PROD.		DATE

NEXT HIGHER ASSY: A-ML-PC11-Ø

SCALE: NONE

SHEET 3 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

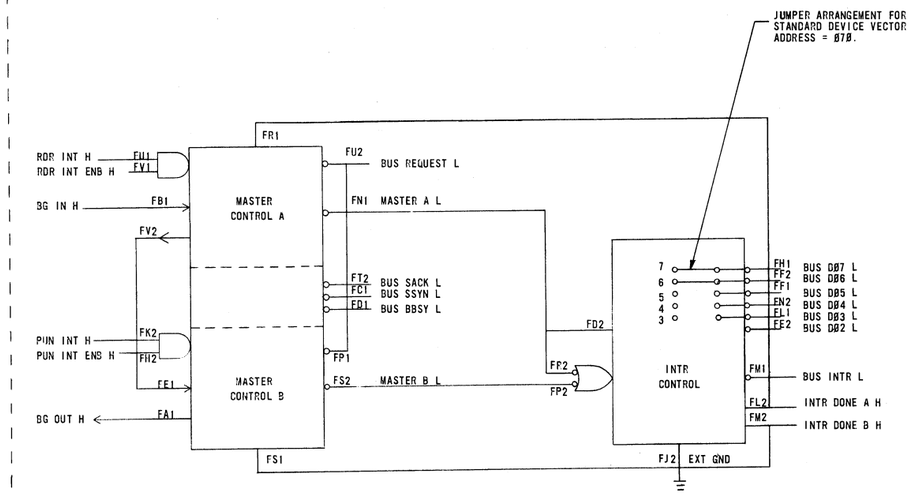
TITLE: PC11 CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M781-Ø-1	A

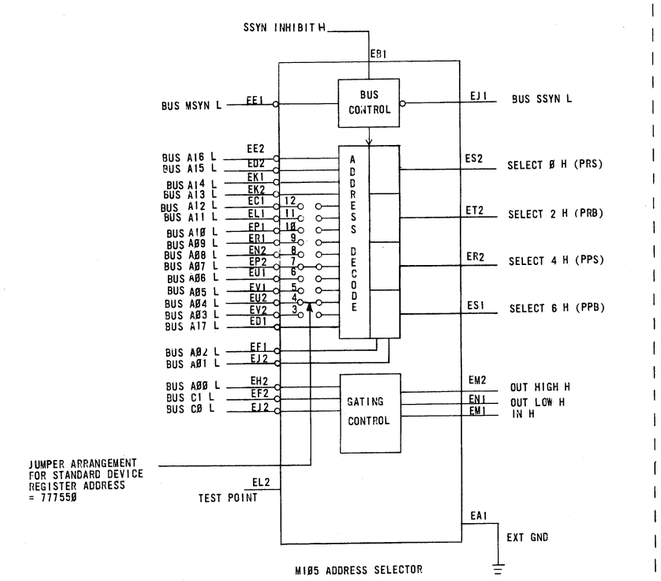
DIST.

REVISIONS	REV	CHANGE NO	CHK

DEC FORM NO 340 102A



M782 INTERRUPT CONTROL



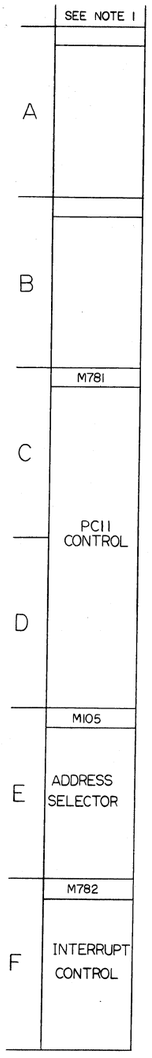
M105 ADDRESS SELECTOR

FIRST USED ON OPTION/MODEL: PDP11	QTY.	DESCRIPTION	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED		PARTS LIST	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DRN.	DATE 4-2-70	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHK'D.	DATE 4/14/70	TITLE: DEVICE CONTROL
	ENG.	DATE 5/4/70	
	PROJ. ENG.	DATE 5/4/70	
MATERIAL	PROD.	DATE 5/5/70	
	NEXT HIGHER ASSY: A-ML-PC11-0		SIZE D / CODE BS / NUMBER PC11-0-2 / REV.
FINISH	SCALE: NONE		DIST.
	SHEET 1 OF 1		

REVISIONS: REV | CHANGE NO | CHK

DEC FORM NO DRD 1024

NOTES:
SLOT 13 OR 14 IN THE KA11 PROCESSOR OR,
SLOT 1,2,3 OR 4, IN THE DD11-A.



REVISIONS	REV.
CHANGE NO.	
CHK.	

DEC FORM NO. DRD 100

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL
PDP 11

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—/—

FINISH —/—/—

DRN	R. Hellen	DATE 5/13/70
CHK'D.		DATE 7/29/70
ENG.		DATE 5/14/70
PROJ. ENG.		DATE 5/14/70
PROD.		DATE 5/15/70

NEXT HIGHER ASSY
A-ML-PC11-Ø

SCALE NONE
SHEET 1 OF 1

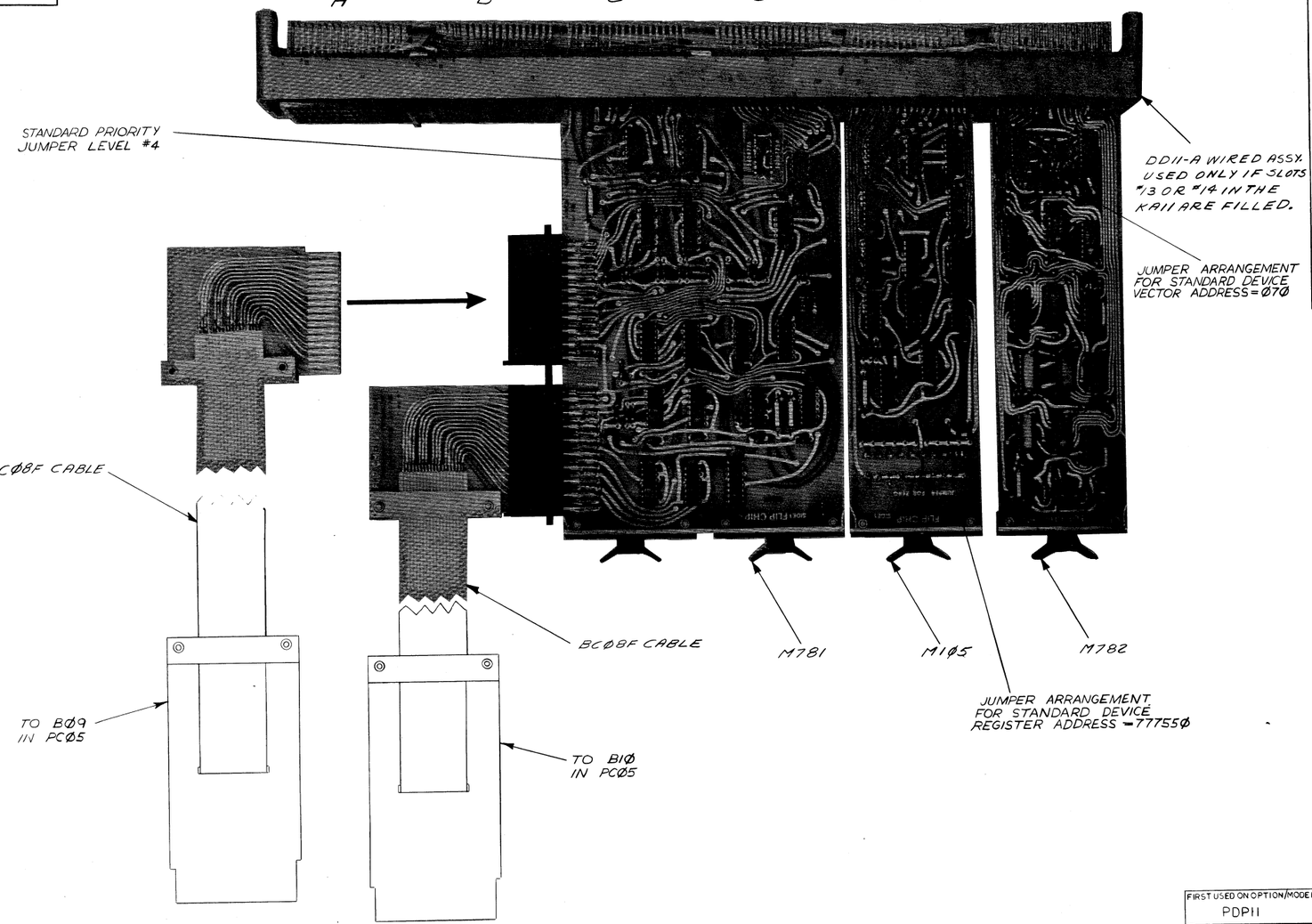
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
MODULE
UTILIZATION

SIZE	CODE	NUMBER	REV.
D	MU	PC11-Ø-MU	

DIST.

NOTES:
1. FOR CORRECT SLOT USAGE SEE D-MU-PC11-Ø-MU.



REVISIONS	REV.
CHANGE NO.	
CHK	

DEC FORM NO. TYPE

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN	M. Morrill	DATE 5.4.70
CHK	[illegible]	DATE 9/28/70
ENG	[illegible]	DATE 5/4/70
PROJ ENG	[illegible]	DATE 5/4/70
PROD	[illegible]	DATE 5/5/70

NEXT HIGHER ASSY: A-ML-PC11-0

SCALE 1/1

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: OPTION ARRANGEMENT

SIZE	CODE	NUMBER	REV.
D	AR	PC11-Ø-4	

DIST.

READER'S COMMENTS

PDP-11 PC11 HIGH-SPEED READER/PUNCH AND CONTROL DEC-11-HPCA-D

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How can this manual be improved? _____

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