dietz 621

Zentraleinheit

Technische Unterlagen

dietz 621

Zentraleinheit

Technische Unterlagen

5.75

Schutzgebühr DM 25,00

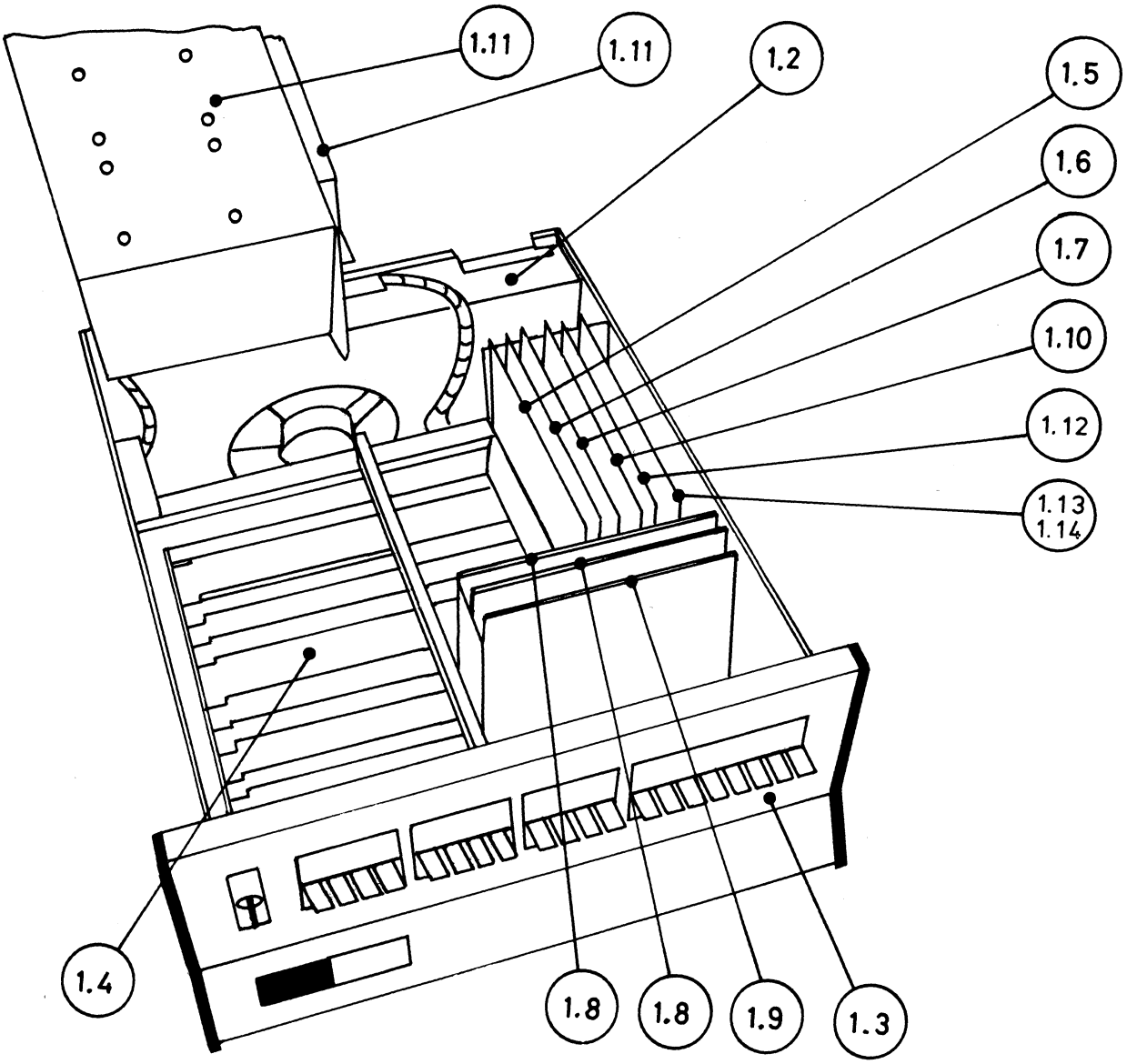
Heinrich Dietz
433 Mülheim a.d. Ruhr
Solinger Str. 9
Tel. (0213 3) 485024
Telex 856770

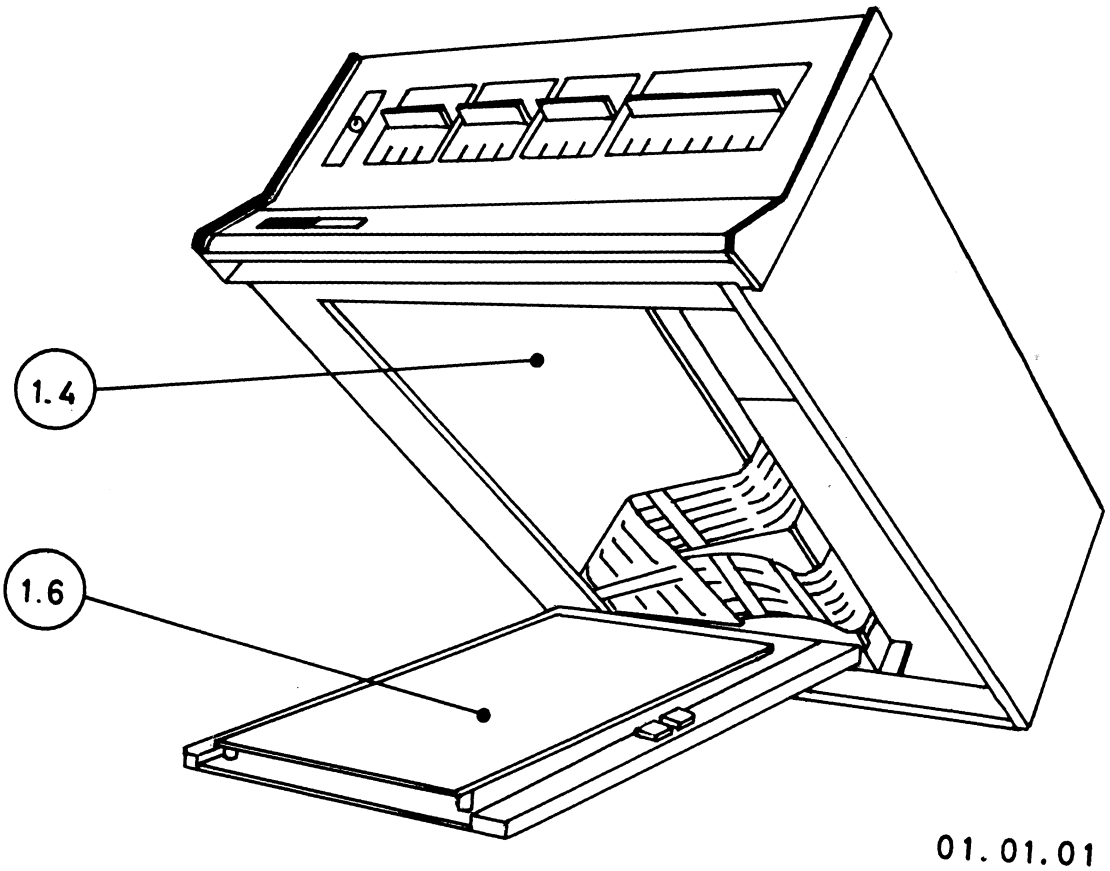
DIETZ Computer SYSTEME

TECHNISCHE UNTERLAGEN

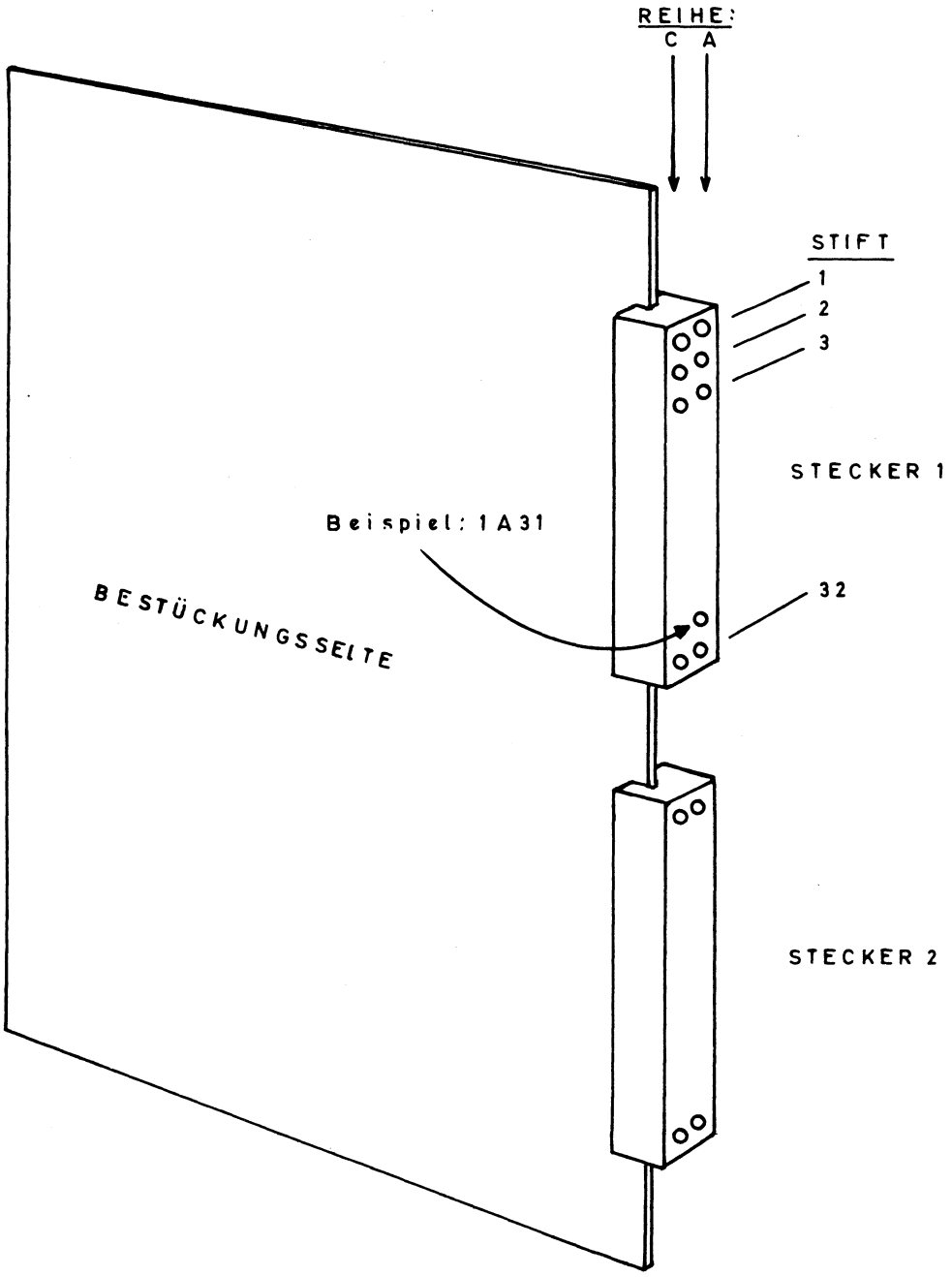
MC 6 - Zentraleinheit

INHALTSVERZEICHNIS





01.01.01



Zählweise der Stifte gültig für alle steckbaren Baugruppen

Jedem Rechner wird bei Auslieferung ein ausgefülltes Formblatt GERÄTESPEZIFIKATION beigelegt. Dieses Formblatt gibt Auskunft über den Rechnerausbau. Dabei sind folgende Ausbauten und Modifikationen möglich.

Lfd.Nr.	Benennung	Stand.	Option	Modifikation
1	Gehäuse verdrahtet	x		ohne
2	MINCAL 621 CPU	x		Programmstart auf 4000
			x	Programmstart auf 2000
		x		Rückmeldung des Interface II auf Level Ø
			x	Rückmeldung des Interface II auf Level 1 oder 2 usw. bis 15
3	Stromversorgung	x		ohne Batteriepufferung
			x	Umschaltung für interne Batteriepufferung
			x	Umschaltung für externe Batteriepufferung
4	Batterie - Element		x	
5	Bedienungskonsole	x		als Blindplatte ohne Elektronik
			x	Type 621 600 mit Locher/Leser/TTY - Bootstrap
			x	Type 621 600 mit DIETZdisk - Bootstrap
6	Ram-Baustein 303	x		0,25 K
			x	aufstockbar in Stufen von 0,25 bis 2 K (0-2 K)
7	Ram-Baustein 302		x	aufstockbar in Stufen von 0,25 bis 2 K (2-4 K)
8	Speicheranschluß-satz	x		4 K Kernspeicheranschluß
			x	8/16 K Kernspeicheranschluß
			x	32 K Kernspeicheranschluß
9	Speicher	x		4 K Kernspeicher
			x	8 K Kernspeicher
			x	16 K Kernspeicher
			x	32 K Kernspeicher
			x	1 K Reprom aufstockbar in Stufen von 1 K bis 8 K
10	Kernspeicheranpassung	x		ohne
11	Mikroschrittlogik	x		ohne
12	Ebenenlogik	x		Programmierung auf 8 Ebenen / 16 Ebenen
		x		Programmierung auf 16/32/64/128/256 byt Ebene
		x		Programmierung CNP-Ebene auf 1 oder 2 usw. bis 15
13	Echtzeituhr		x	Taktzeitprogrammierbar auf 100 µsek. o. 1 msek o. 10 msek o. 100 msek o. 1 Sek.
14	BUS - Anschluß	x		621 611 ohne Kabelabgang
			x	621 611 mit Gegenstecker für Speichererweiterung
			x	621 611 mit Gegenstecker für Universial-Interf. Einsch.
			x	621 611 mit Gegenstecker für Controller
15	Interface I		x	jedes Einkarteninterface ist einsetzbar
			x	Rückmeldung auf Ebene Ø Ø
16	Interface II		x	jedes Einkarteninterface ist einsetzbar
				Rückmeldung auf Ebene Ø Ø oder Ø 1 usw. bis 15
17	Netzkabel	x		ohne

Auftrags Nr	Serien-Nr	Starttermin	Ausstellungsdatum	Endtermin
67289		15 8 73	03 10 73	

MINCAL 62 Computer	Anlage Abt. 3	Ausgestellt Datum 14.8.73 Name HER	Blatt-Nr.	Blatt-Za
Kunde Müller	Gerätespezifikation		DFÜ	

Lfd. Nr.	Stück	Benennung	V-Bez	Typen-Nr		
1	1	Gehäuse verdrahtet				
2	1	MINCAL 621 CPU	MC 621	621 602	C	
3	1	Stromversorgung Typ: II	CSV_2	621 3		339
4	1	Batterie-Element Typ: II	CBP/			
5	1	Bedienungskonsole	CBK	621 600	C	
6	1	RAM-Baustein Platz 303	RAM/	621 6393	C	
7		RAM-Baustein Platz 302	RAM/	621		
8	1	Speicher-Anschlußsatz		621 080		
9	1	Speicher Kbytes: 16K	KS 16			601 173
10	1	Kernspeicheranpassungskarte		621 603	H	
11	1	Mikroschrittlogik		621 602	C	
12	1	Ebenenlogik Ebenen: 16	CPE	621 607	C	
13		Echtzeituhr	CCL	621 610	C	
14	1	BUS-Anschluß	BUS-			
15	1	Interface I TTY		602 000	E	
16	1	Interface II LO-LE		602 005	E	
17	1	Netzkabel	KANE-2,5	600 025		
18						
19						
20						
21						
22						

Bemerkungen allg.

23	64	byte Pool je Ebene
24	0F	Nr. der CNP-Ebene
25	00	Nr. der Interface-2-Ebene
26	10	ms Taktzeit Rechneruhr
27		Anschluß für externe Batterie
28		

Bemerkungen für Prüffeld

Exemplar:	F1	C4	P1	F33					Unt P4	01.01.04

RECHNER-STAND

STAND MINCAL 621 AM: 03.10.73 Komm.-Nr.: 67289 Kunde Müller

Benennung	Nr. der Leiterplatte	Index	GEÄNDERT AUF						
			D1 20.12.73 Ke	E4 3.4.74 Ga	H8 5.6.74 Ro				
CPU	621602	C							
K.Sp.Anp.K.	621603	K							
Schr.Spr.Logik	621602	C							
Ebenen-Logik	621607	C	621643 E 1.10.73 Ro	F1 3.4.74 Ga					
TTY-Interfaces	602000	E							
LO/LE-Interfaces	602005	E							
RAM Pl.303	621639 3	C							
RAM Pl.302									
Rechner Uhr	621610	C							
Bed.Konsole	621600	C							
SV Einschub	621 3/339								

MUSTER

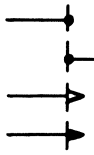
ACHTUNG !!!!!!!!!

Das zugehörige Formular muß im Rechner bleiben.

Sonstige Änderungen: Leiser Lüfter eingebaut 3.4.74 Ga

01.01.05

1/ Allgemeine Angaben



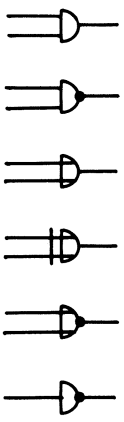
Invert. am Eingang

Invert am Ausgang

Dyn. Eingang Wirkung bei Übergang von 0 auf 1

Dyn. Eing. Wir k. b. Überg. v. 1 auf 0.

2/ Schaltkreisbeispiele



AND [UND]

NAND [$\overline{\text{UND}}$]

OR [ODER]

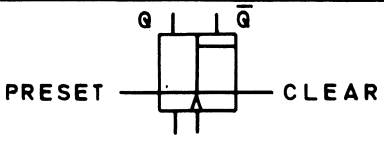
EXCLUSIVE OR [EXKLUSIV-ODER]

NOR [$\overline{\text{ODER}}$]

INVERTER [NEGATION]

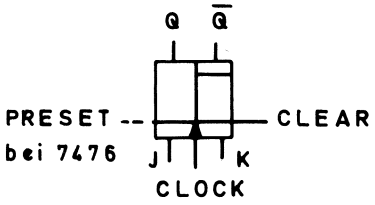
z. B. SN7486

z. B. SN7474



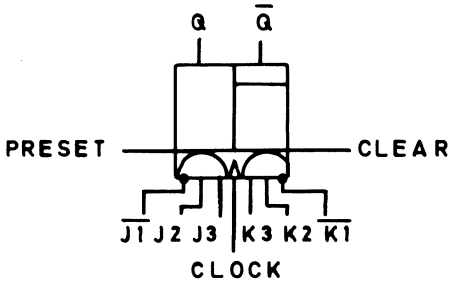
D-FLIP-FLOP

z. B. SN7473
SN7476
SN74107



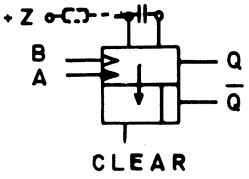
J-K-MASTER-SLAVE-FLIP-FLOP

z. B. SN7470



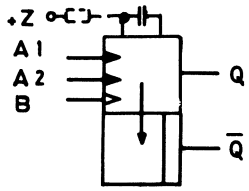
J-K-FLIP-FLOP

z. B. SN74123

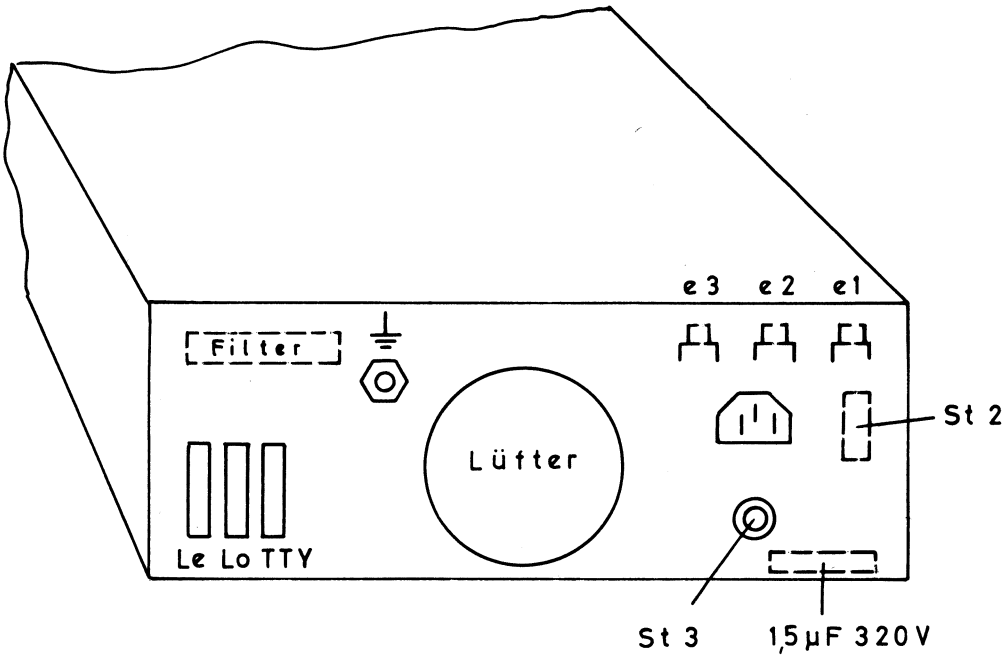


MONOFLOP

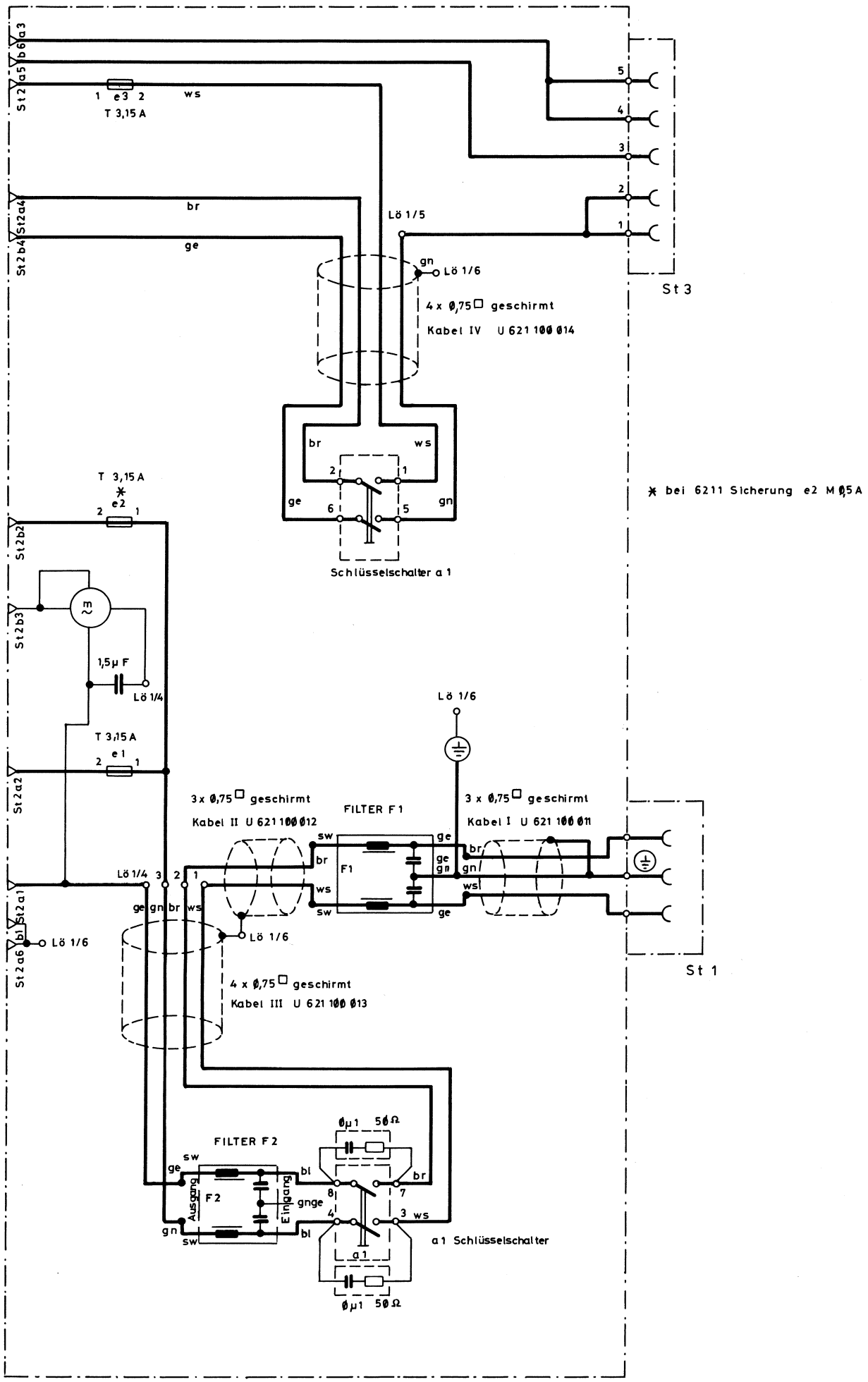
z. B. SN74121



MONOFLOP

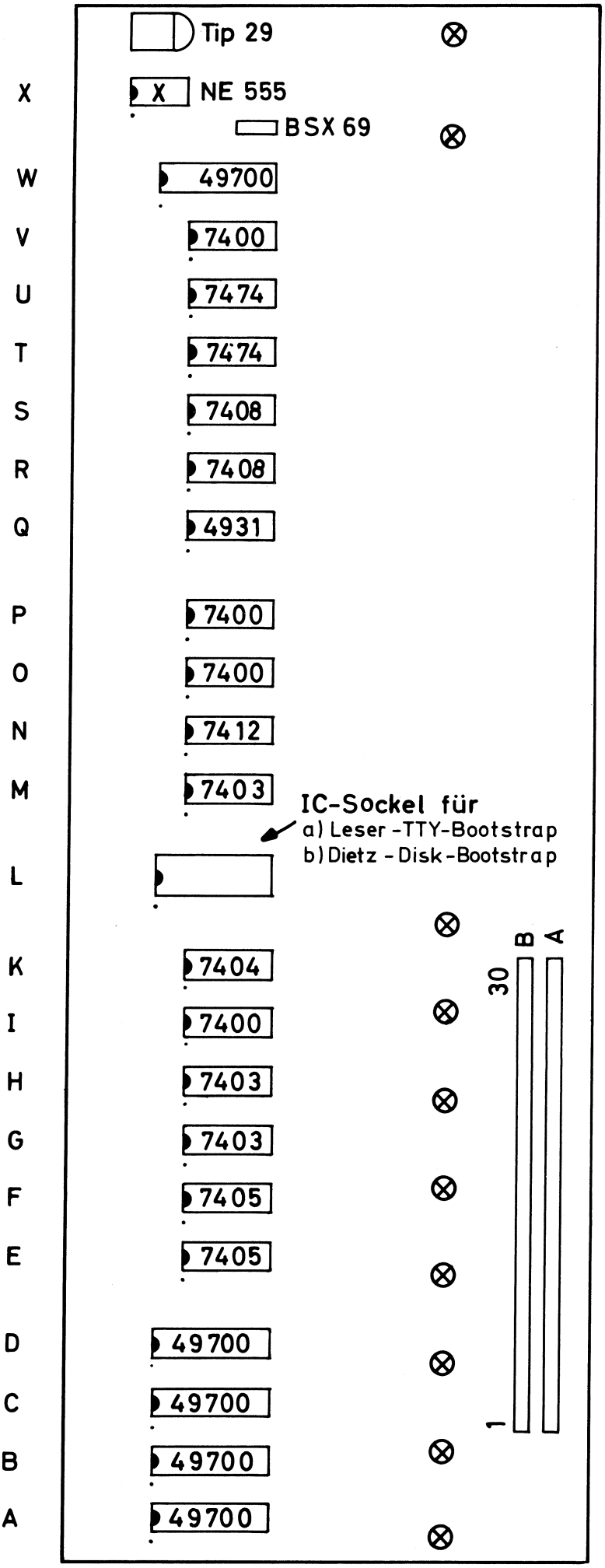


Rechnergehäuse Rückansicht	01.02.01



Rechnerverdrahtung SV 621

01.02.02


Tip 29
X
X NE 555
BSX 69
W
49700
V
7400
U
7474
T
7474
S
7408
R
7408
Q
4931
P
7400
O
7400
N
7412
M
7403
IC-Sockel für
a) Leser -TTY-Bootstrap
b) Dietz - Disk-Bootstrap
L
K
7404
I
7400
H
7403
G
7403
F
7405
E
7405
D
49700
C
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B
49700
A
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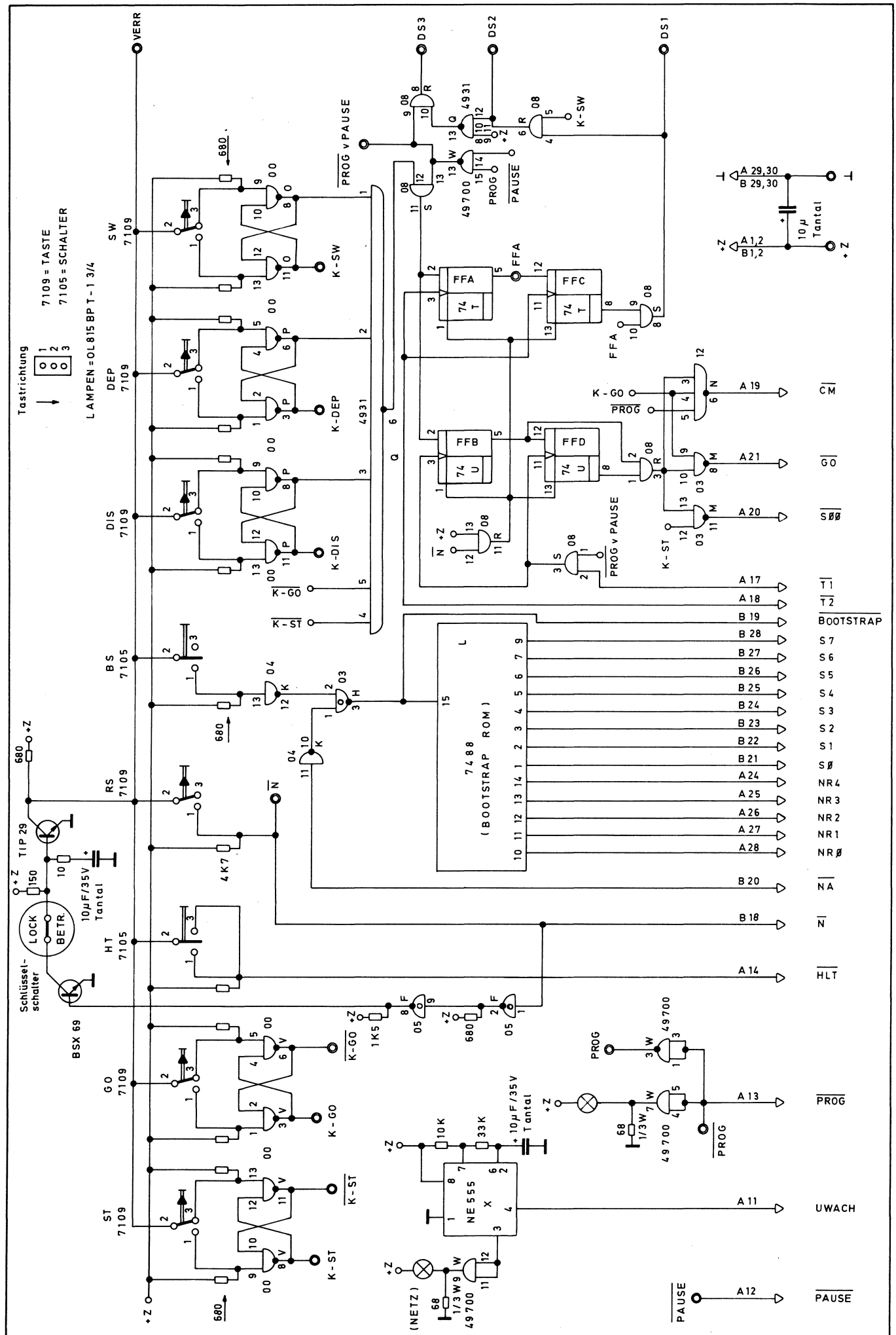
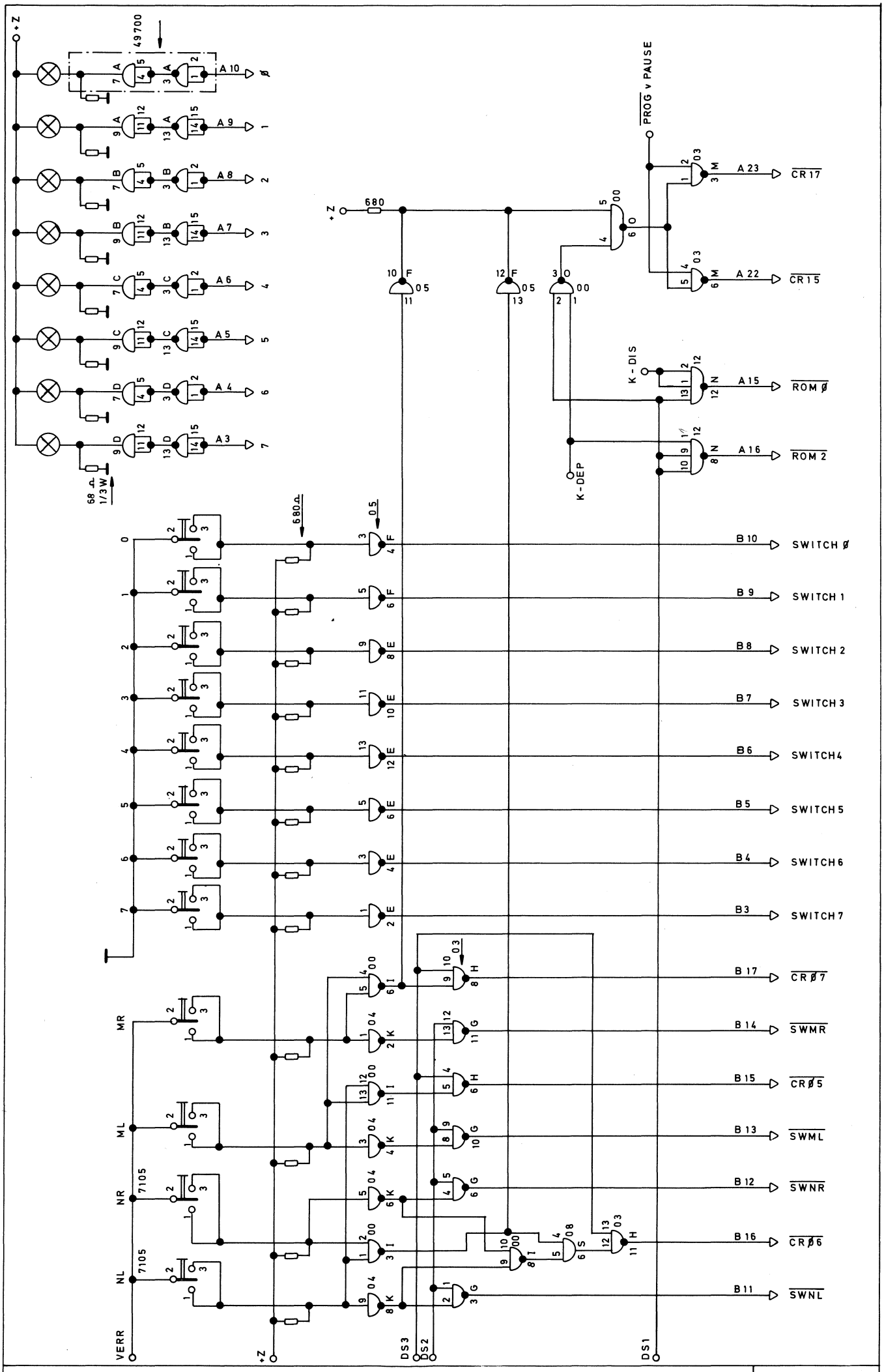
30
B
A
1



621 600 C Bedienungskonsole

01.03.02



621 600 C Bedienungskonsole 01.03.03

```
                BOOTSTRAP-PROGRAMM;
      4000                LDC ,   3,      6;        81 03 06
      4003                GS  ,   5;                23 05
      4005 A2  :          LDC ,@   ,'12   ;         80 12
      4007                STA ,@   ,'1001 ,   5;    EE 01 10 05
      400B                HLT ;                     02
      400C                LDA ,@   ,'1000 ,   5;    8E 00 10 05
      4010                BNEC,@   ,'FF   ,A1  ;    58 FF 05
      4013                BEC ,   3,      6,A2  ;   51 03 06 EF
      4017 A1  :          STX ,@   ,      ,   3;    E2 03
      4019                INZ ,   3,       ,A2  ;   4B 03 EA
      401C                LDC ,@   ,      0;        80 00
      401E                JPR ,    ,      7;        F4 07
```

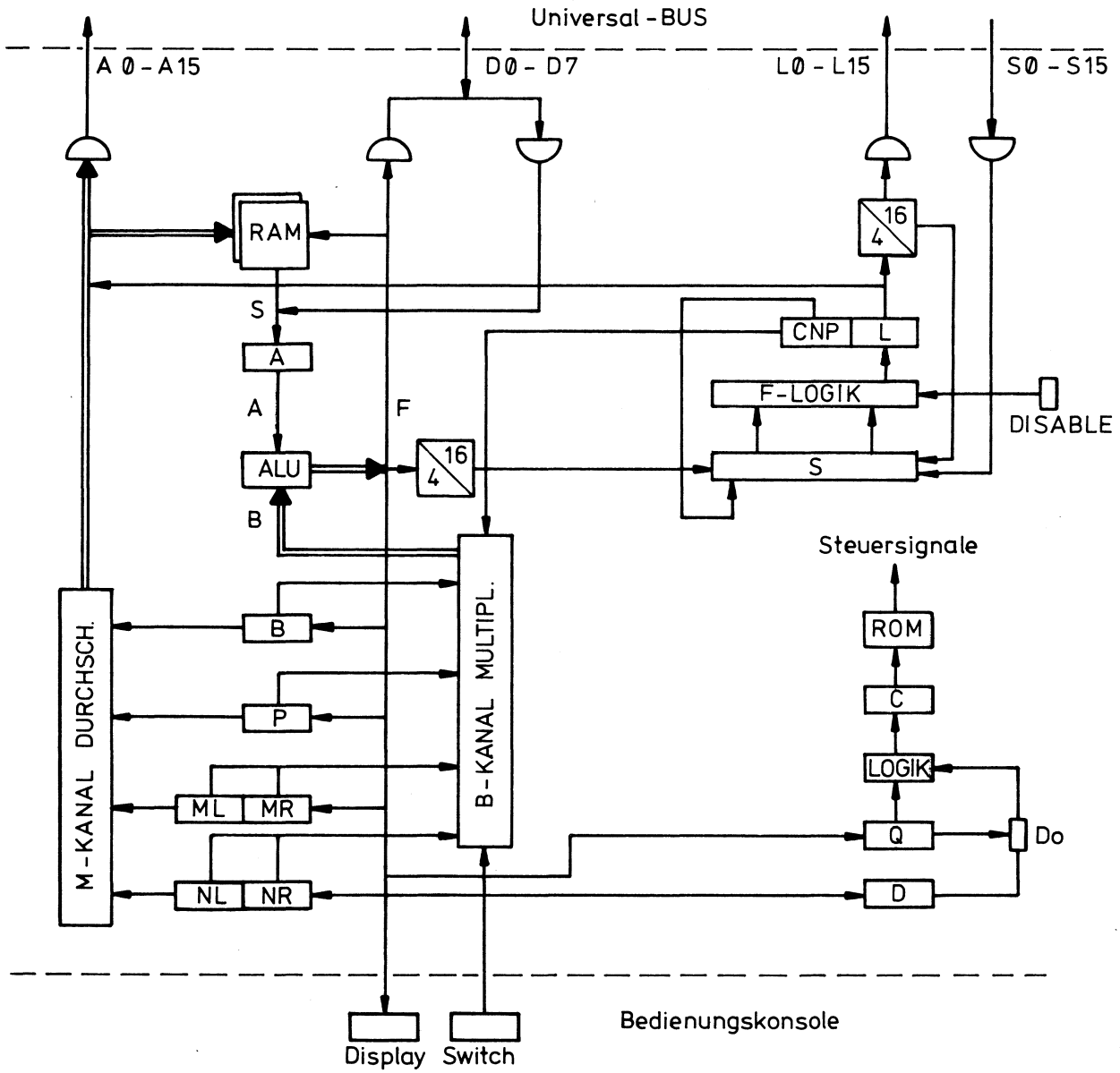
	ADRESSEINGÄNGE					DATEN - AUSGÄNGE							
Wort	NR4	NR3	NR2	NR1	NRØ	S7	S6	S5	S4	S3	S2	S1	SØ
1	L	L	L	L	L	H	L	L	L	L	L	L	H
2	L	L	L	L	H	L	L	L	L	L	L	H	H
3	L	L	L	H	L	L	L	L	L	L	H	H	L
4	L	L	L	H	H	L	L	H	L	L	L	H	H
5	L	L	H	L	L	L	L	L	L	L	H	L	H
6	L	L	H	L	H	H	L	L	L	L	L	L	L
7	L	L	H	H	L	L	L	L	H	L	L	H	L
8	L	L	H	H	H	H	H	H	L	H	H	H	L
9	L	H	L	L	L	L	L	L	L	L	L	L	H
1Ø	L	H	L	L	H	L	L	L	H	L	L	L	L
11	L	H	L	H	L	L	L	L	L	L	H	L	H
12	L	H	L	H	H	L	L	L	L	L	L	H	L
13	L	H	H	L	L	H	L	L	L	H	H	H	L
14	L	H	H	L	H	L	L	L	L	L	L	L	L
15	L	H	H	H	L	L	L	L	H	L	L	L	L
16	L	H	H	H	H	L	L	L	L	L	H	L	H
17	H	L	L	L	L	L	H	L	H	H	L	L	L
18	H	L	L	L	H	H	H	H	H	H	H	H	H
19	H	L	L	H	L	L	L	L	L	L	H	L	H
2Ø	H	L	L	H	H	L	H	L	H	L	L	L	H
21	H	L	H	L	L	L	L	L	L	L	L	H	H
22	H	L	H	L	H	L	L	L	L	L	H	H	L
23	H	L	H	H	L	H	H	H	L	H	H	H	H
24	H	L	H	H	H	H	H	H	L	L	L	H	L
25	H	H	L	L	L	L	L	L	L	L	L	H	H
26	H	H	L	L	H	L	H	L	L	H	L	H	H
27	H	H	L	H	L	L	L	L	L	L	L	H	H
28	H	H	L	H	H	H	H	H	L	H	L	H	L
29	H	H	H	L	L	H	L	L	L	L	L	L	L
3Ø	H	H	H	L	H	L	L	L	L	L	L	L	L
31	H	H	H	H	L	H	H	H	H	L	H	L	L
32	H	H	H	H	H	L	L	L	L	L	H	H	H

```
                BOOTSTRAP-PROGRAMM ;
      4000              LDC ,@    ,'0A    ;       80 0A
      4002              STA ,@    ,'1012  ;       EC 12 10
      4005 A2  :        LDA ,@    ,'1012  ;       8C 12 10
      4008              BZC ,@    ,     1,A2  ;   60 01 FB
      400B              LDC ,@    ,     0;        80 00
      400D              STA ,@    ,'1012  ;       EC 12 10
      4010              LDC ,     3,'1E   ;       81 03 1E
      4013 A1  :        LDA ,@    ,'1014  ;       8C 14 10
      4016              STX ,@    ,       ,'03 ;  E2 03
      4018              INEC,     3,'9E   ,A1  ;  5B 03 9E F8
      401C              JPR ,     ,'1E    ;       F4 1E
      401E              HLT ;                     02
```

ADRESSEINGÄNGE NR						DATENAUSGÄNGE							
WORT	NR4	NR3	NR2	NR1	NR0	S7	S6	S5	S4	S3	S2	S1	S0
1	L	L	L	L	L	H	L	L	L	L	L	L	L
2	L	L	L	L	H	L	L	L	L	H	L	H	L
3	L	L	L	H	L	H	H	H	L	H	H	L	L
4	L	L	L	H	H	L	L	L	H	L	L	H	L
5	L	L	H	L	L	L	L	L	H	L	L	L	L
6	L	L	H	L	H	H	L	L	L	H	H	L	L
7	L	L	H	H	L	L	L	L	H	L	L	H	L
8	L	L	H	H	H	L	L	L	H	L	L	L	L
9	L	H	L	L	L	L	H	H	L	L	L	L	L
10	L	H	L	L	H	L	L	L	L	L	L	L	H
11	L	H	L	H	L	H	H	H	H	H	L	H	H
12	L	H	L	H	H	H	L	L	L	L	L	L	L
13	L	H	H	L	L	L	L	L	L	L	L	L	L
14	L	H	H	L	H	H	H	H	L	H	H	L	L
15	L	H	H	H	L	L	L	L	H	L	L	H	L
16	L	H	H	H	H	L	L	L	H	L	L	L	L
17	H	L	L	L	L	H	L	L	L	L	L	L	H
18	H	L	L	L	H	L	L	L	L	L	L	H	H
19	H	L	L	H	L	L	L	L	H	H	H	H	L
20	H	L	L	H	H	H	L	L	L	H	H	L	L
21	H	L	H	L	L	L	L	L	H	L	H	L	L
22	H	L	H	L	H	L	L	L	H	L	L	L	L
23	H	L	H	H	L	H	H	H	L	L	L	H	L
24	H	L	H	H	H	L	L	L	L	L	L	H	H
25	H	H	L	L	L	L	H	L	H	H	L	H	H
26	H	H	L	L	H	L	L	L	L	L	L	H	H
27	H	H	L	H	L	H	L	L	H	H	H	H	L
28	H	H	L	H	H	H	H	H	H	H	L	L	L
29	H	H	H	L	L	H	H	H	H	L	H	L	L
30	H	H	H	L	H	L	L	L	H	H	H	H	L
31	H	H	H	H	L	L	L	L	L	L	L	H	L
32	H	H	H	H	H	L	H	L	H	L	L	H	H

A			B	
+Z		1	+Z	
+Z		2	+Z	
7		3	SWITCH7	
6		4	SWITCH6	
5		5	SWITCH5	
4		6	SWITCH4	
3		7	SWITCH3	
2		8	SWITCH2	
1		9	SWITCH1	
Ø		10	SWITCHØ	
UWACH		11	SWNL-	
PAUSE-		12	SWNR-	
PROG-		13	SWML-	
HLT-		14	SWMR-	
ROMØ-		15	CRØ5-	
ROM2-		16	CRØ6-	
T1-		17	CRØ7-	
T2-		18	NF-	
CM-		19	BOOTSTRAP-	
SØØ-		20	NA-	
GO-		21	SØ	
CR15-		22	S1	
CR17-		23	S2	
NR4		24	S3	
NR3		25	S4	
NR2		26	S5	
NR1		27	S6	
NRØ		28	S7	
ØV		29	ØV	
ØV		30	ØV	
A			B	

(N- ab 621 602 E)



Selektionen durch ROM-Steuersignale

M-Kanal		
-	-	M
-	Ø4	B
Ø3	-	N
Ø3	Ø4	P

B-Kanal			
-	-	-	SWITCH
-	-	Ø7	MR
-	Ø6	-	NR
-	Ø6	Ø7	P
Ø5	-	-	L
Ø5	-	Ø7	ML
Ø6	Ø6	-	NL
Ø5	Ø6	Ø7	B

ALU

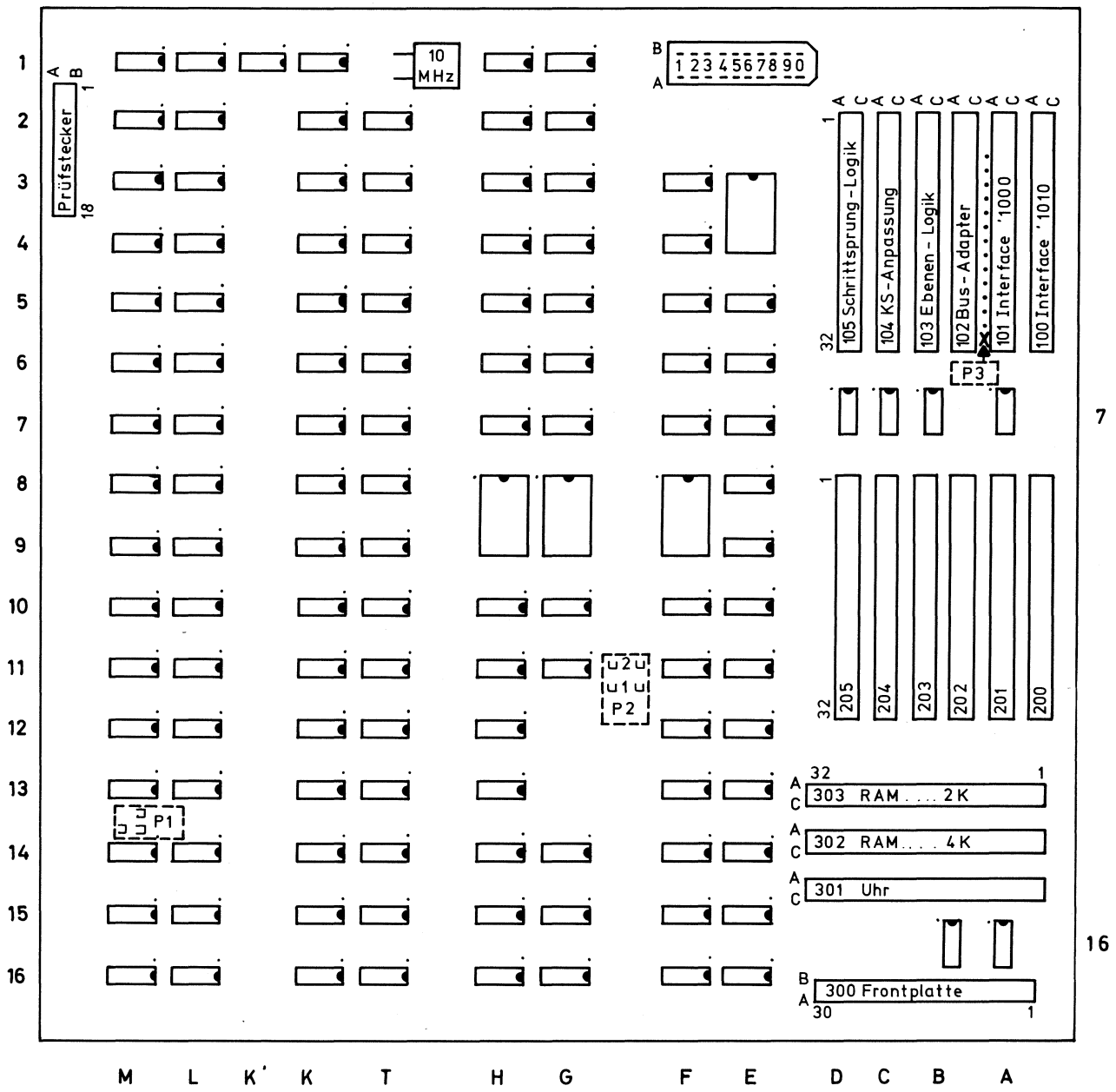
-	-	-	-	-	A
-	-	-	-	17	A ∨ B = F
-	-	15	-	-	A ∧ B = F
-	-	15	-	17	$\bar{}$ B = F
-	-	15	16	17	$\bar{A}$ ∨ B = F
-	14	-	-	17	$\overline{A \neq B}$ = F
-	14	-	16	17	$\overline{A \wedge B}$ = F
-	14	15	16	17	$\bar{A}$ = F
13	-	15	16	-	A + B = F
13	14	-	-	17	A + B = F (A-B-1=F)
13	14	15	16	17	A + CARRY = F

F-Kanal

-	-	-	25	LOAD-D
-	-	12	25	LOAD-MR
-	11	-	25	LOAD-NR
-	11	12	25	LOAD-P
10	-	-	25	LOAD-Q
10	-	12	25	LOAD-ML
10	11	-	25	LOAD-NL

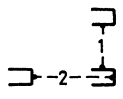
10	11	12	25	LOAD-B
X	X	X	-	<M-Kanal>

Blockschaltbild DIETZ 621 | 01.04.00

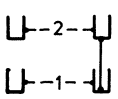


Programmfelder:

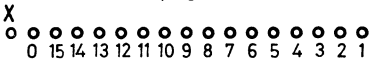
P1



P2



P 3



Brücke

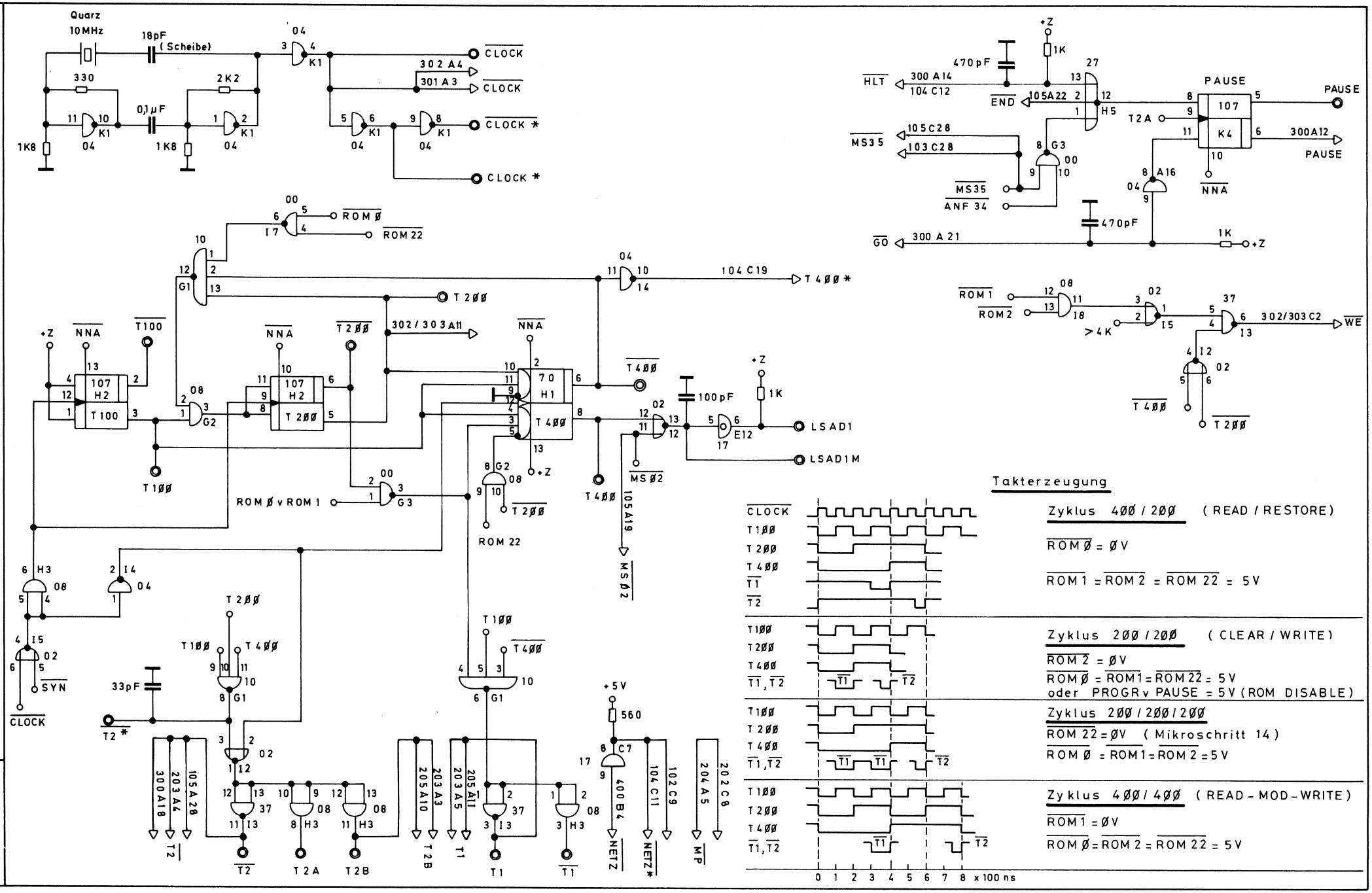
X - 0	Interrupt	von	Level	0
X - 1	"	"	"	1
X - 2	"	"	"	2

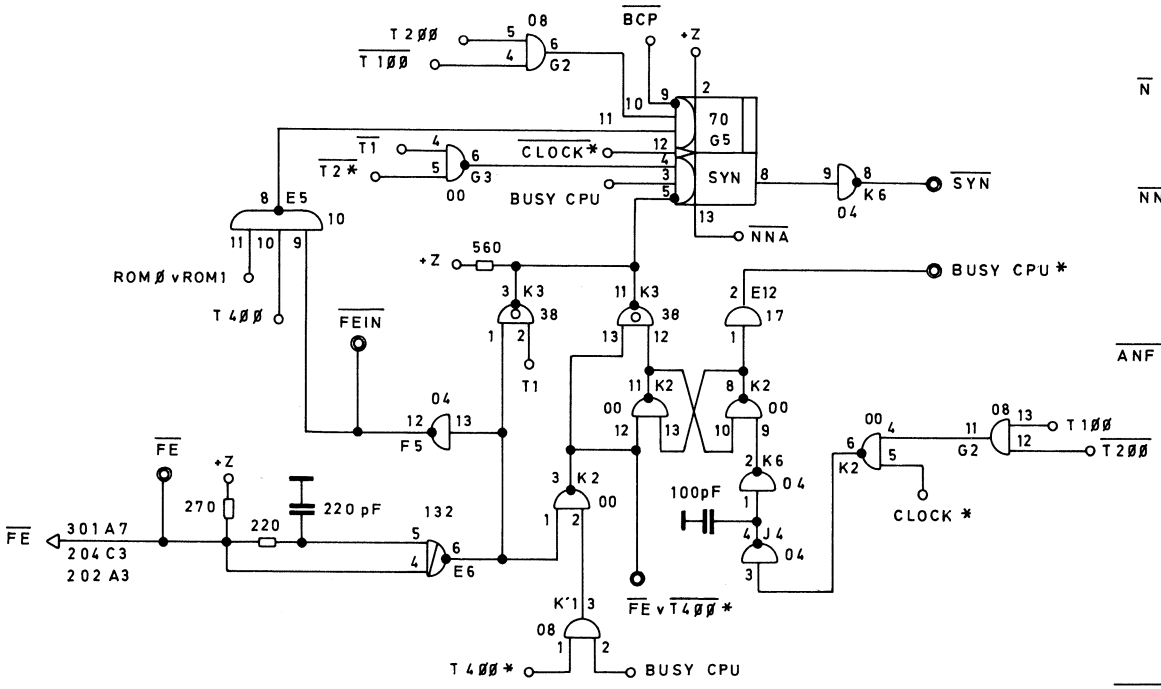
Brücke 1 : Urstart bei Adresse 4###

Brücke 2 : " " " 2###

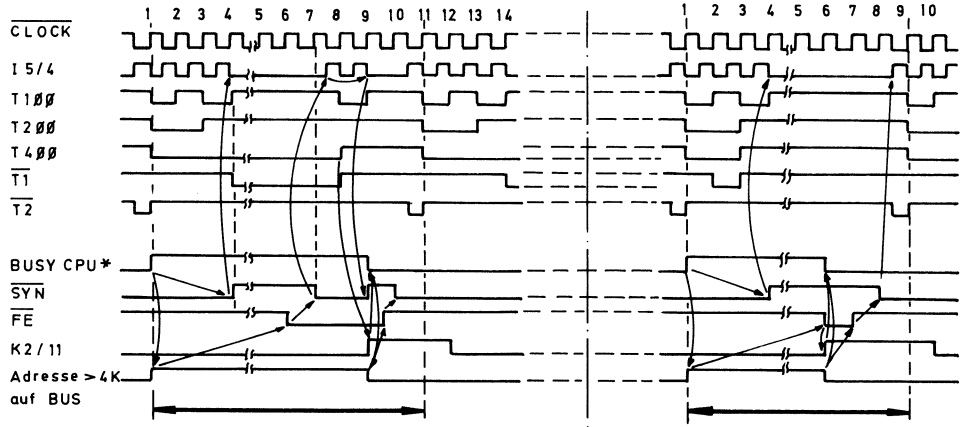
621602 K CPU Taktsteuerung

(1) 01.04.02



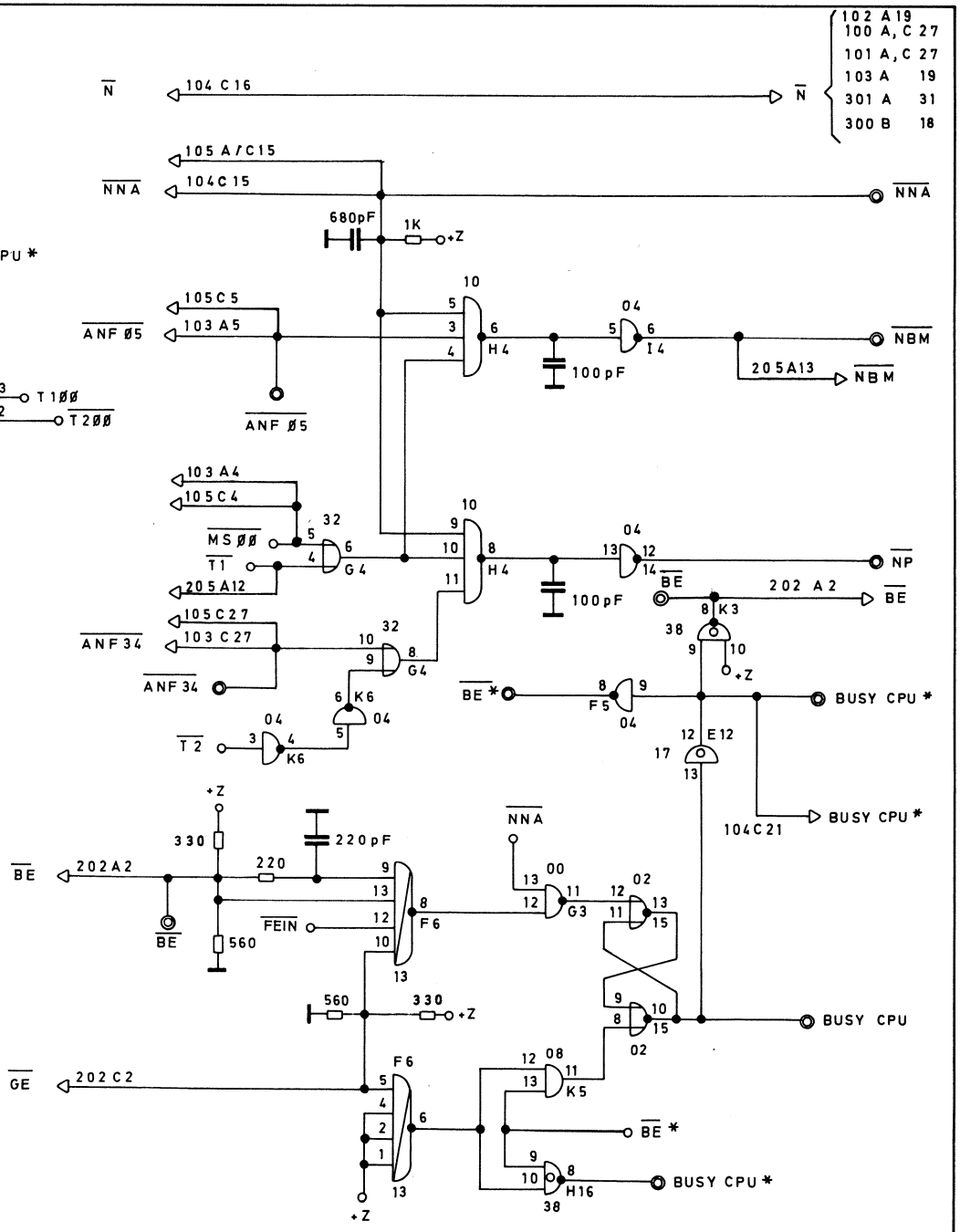


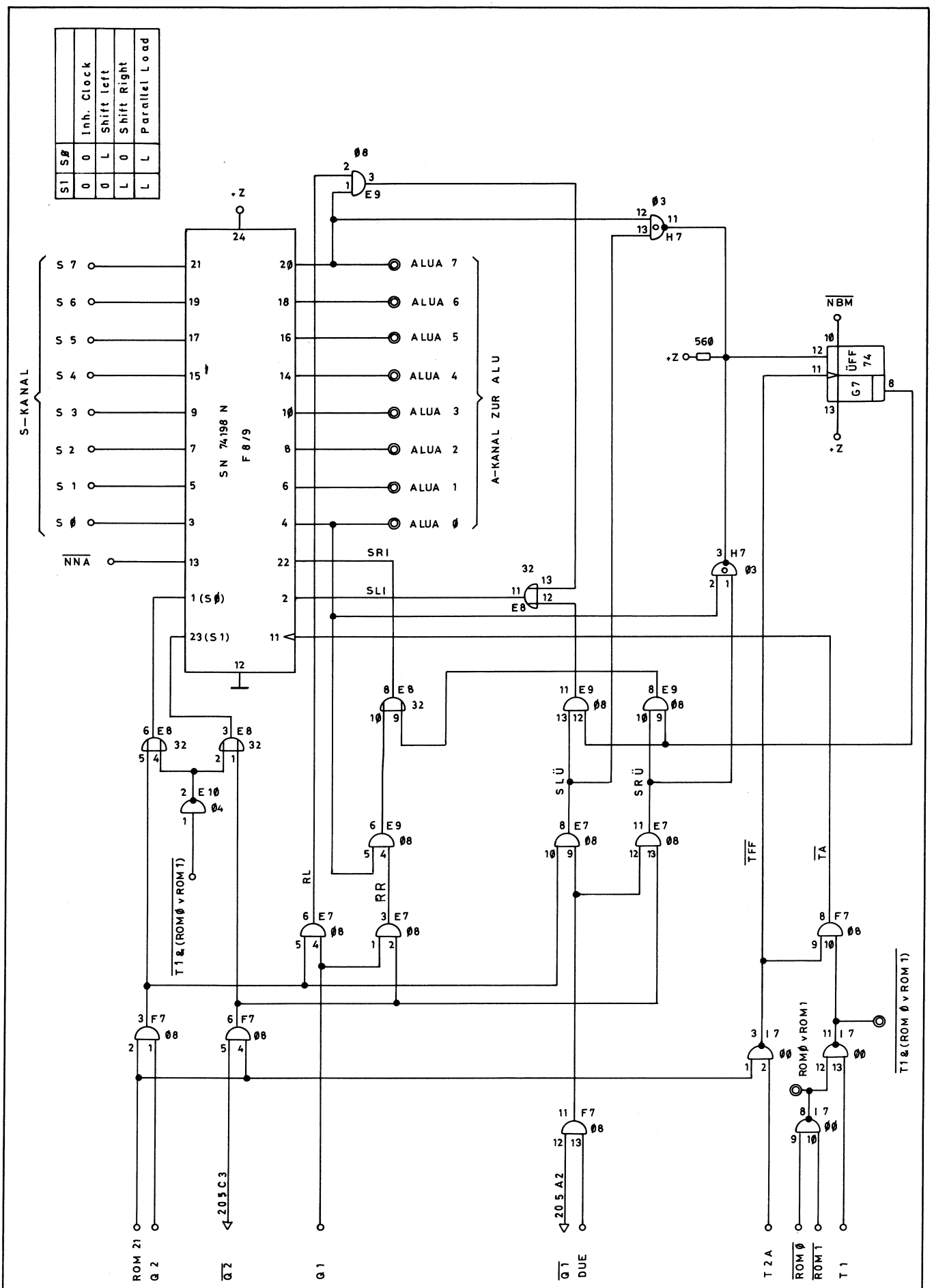
BUS-Synchronisation mit SYN-FF

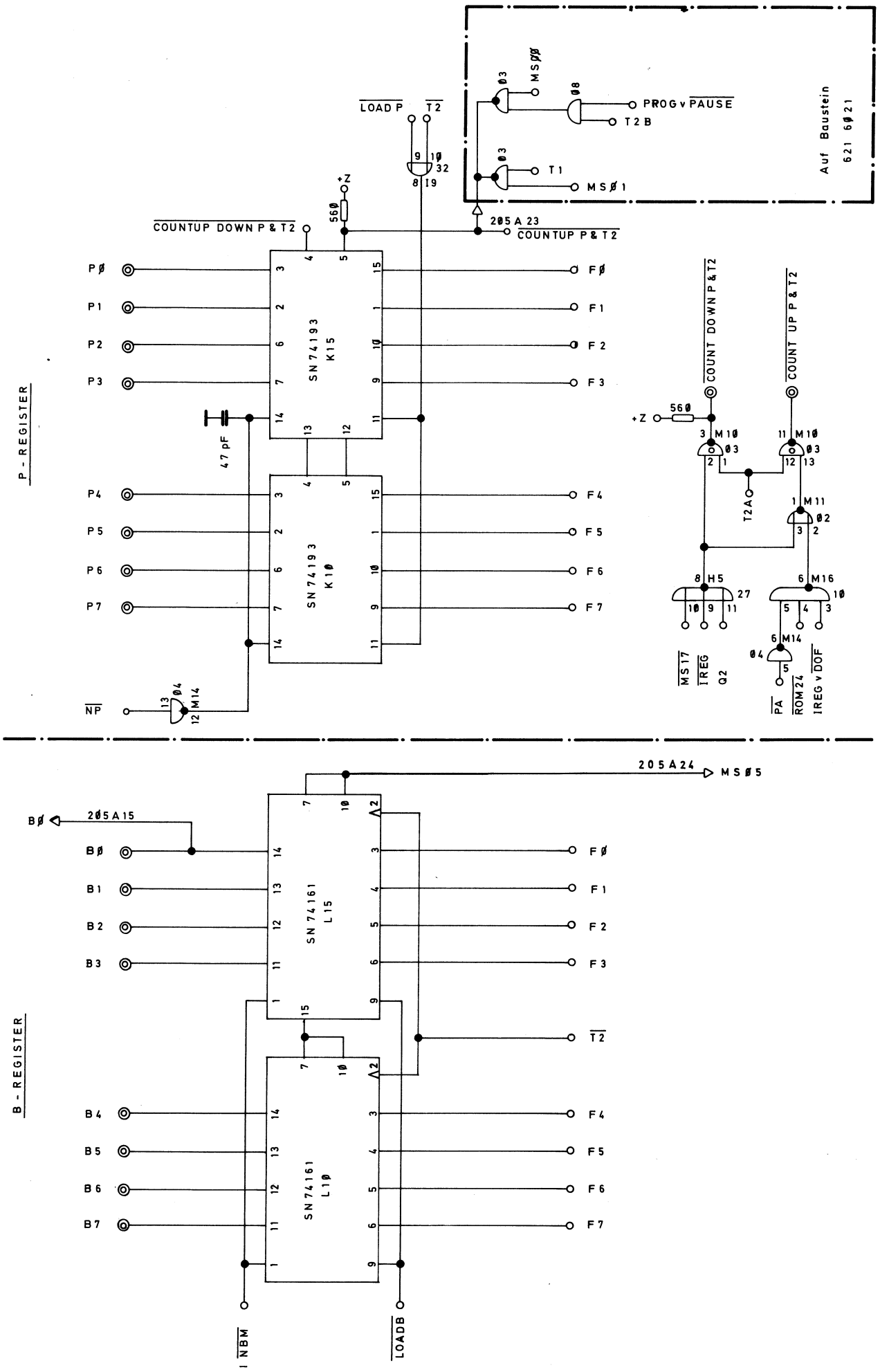


READ / RESTORE - ZYKLUS
mit Adresse
größer als 'ØFFF

CLEAR / WRITE - ZYKLUS
mit Adresse
größer als 'ØFFF

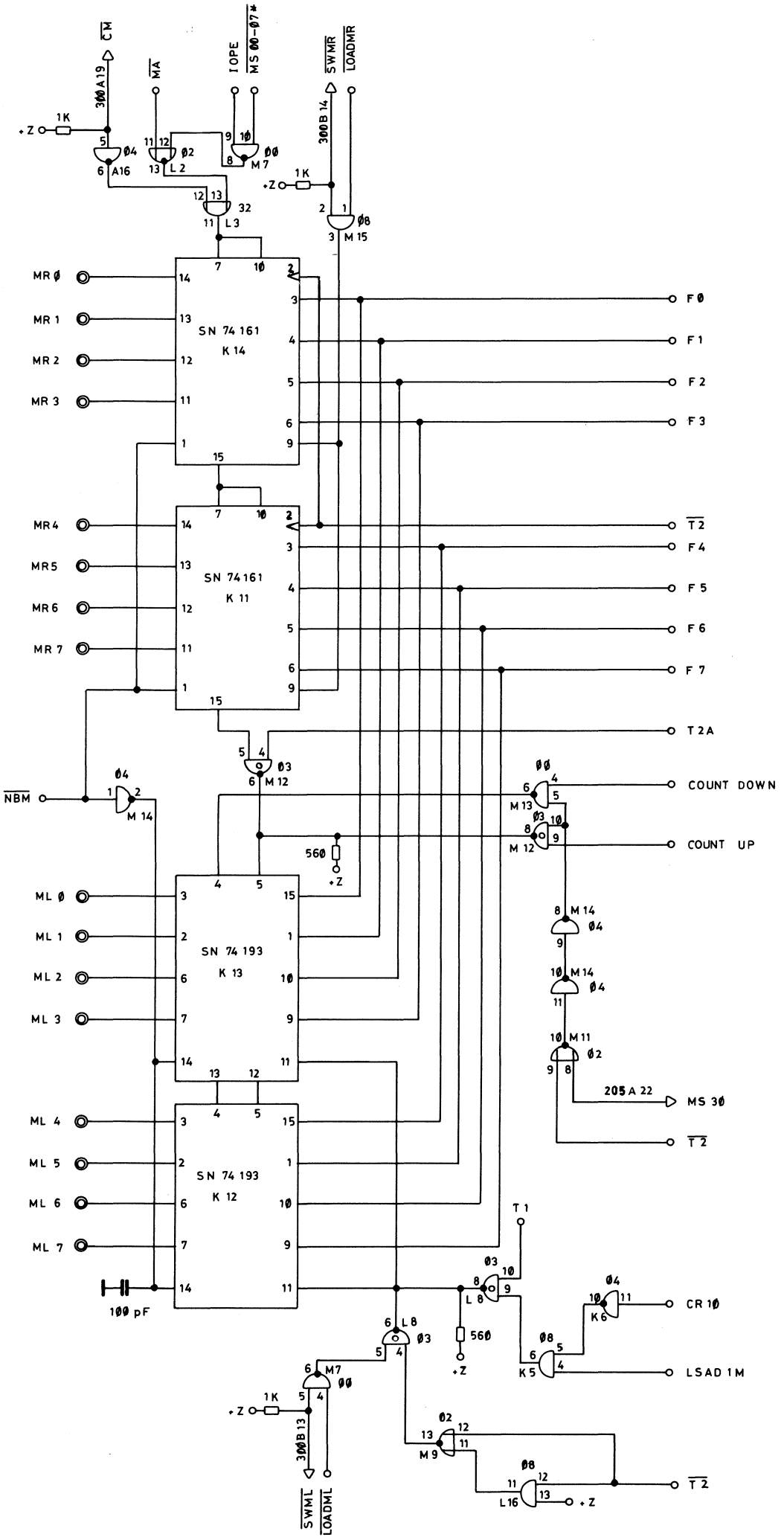



S1 S0 Inh. Clock
0 0 L
0 L Shift left
L 0 Shift Right
L L Parallel Load
S-KANAL
A-KANAL ZUR ALU
SN 74198 N
F 8/9
+Z
S 7
S 6
S 5
S 4
S 3
S 2
S 1
S Ø
NNA
SRI
SLI
ALUA 7
ALUA 6
ALUA 5
ALUA 4
ALUA 3
ALUA 2
ALUA 1
ALUA Ø
E9
H7
E8
E10
E7
F7
I 7
F8
ÜFF 74 G7
NBM
560
SLÜ
SRÜ
RL
RR
TFF
TA
T1 & (ROMØ v ROM 1)
ROMØ v ROM 1
205 C3
205 A2
ROM 21 Q 2
Q2
Q1
Q1 DUE
T2A
ROMØ
ROM 1
T1



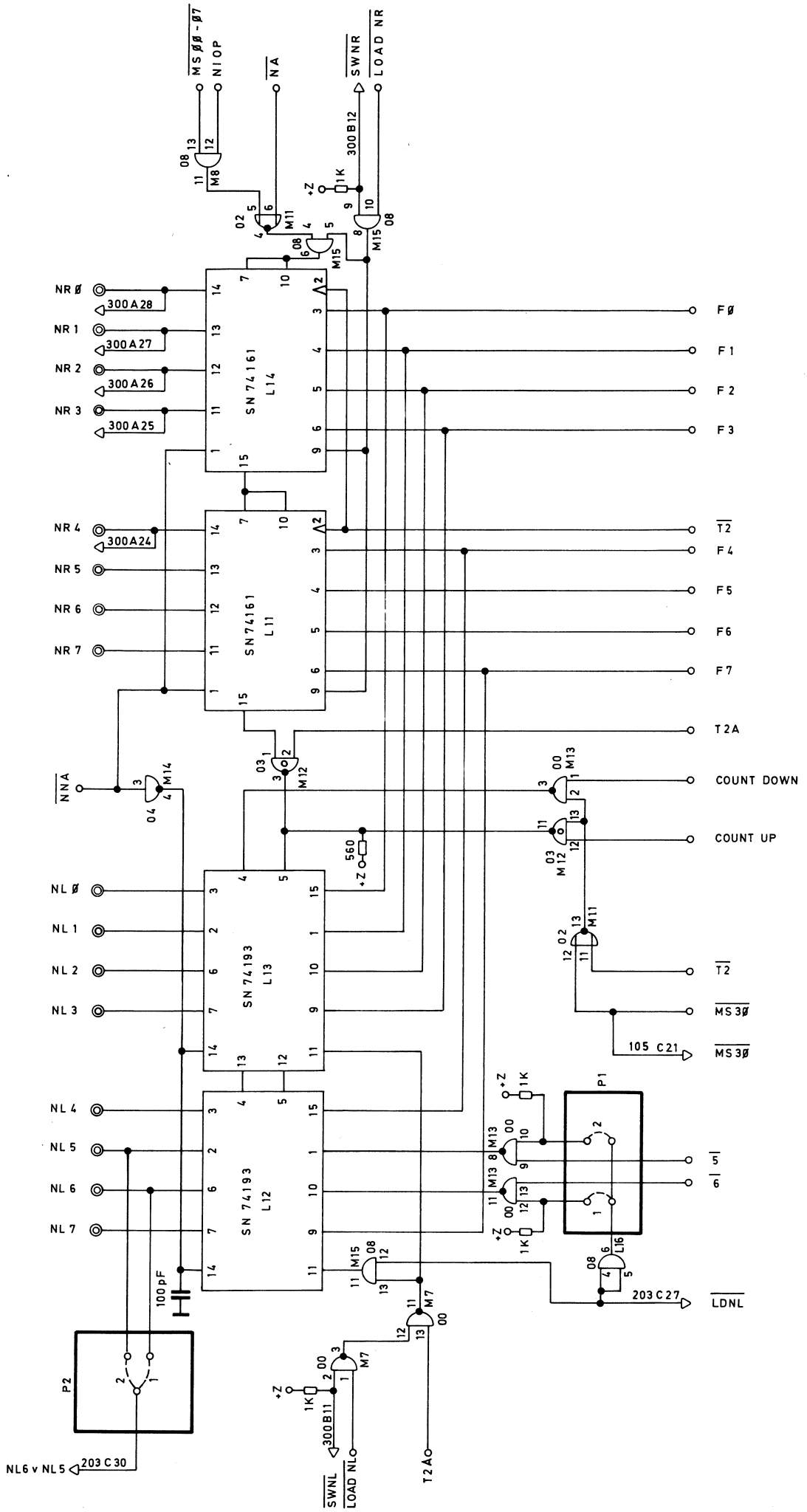
621 602 K CPU P & B Register

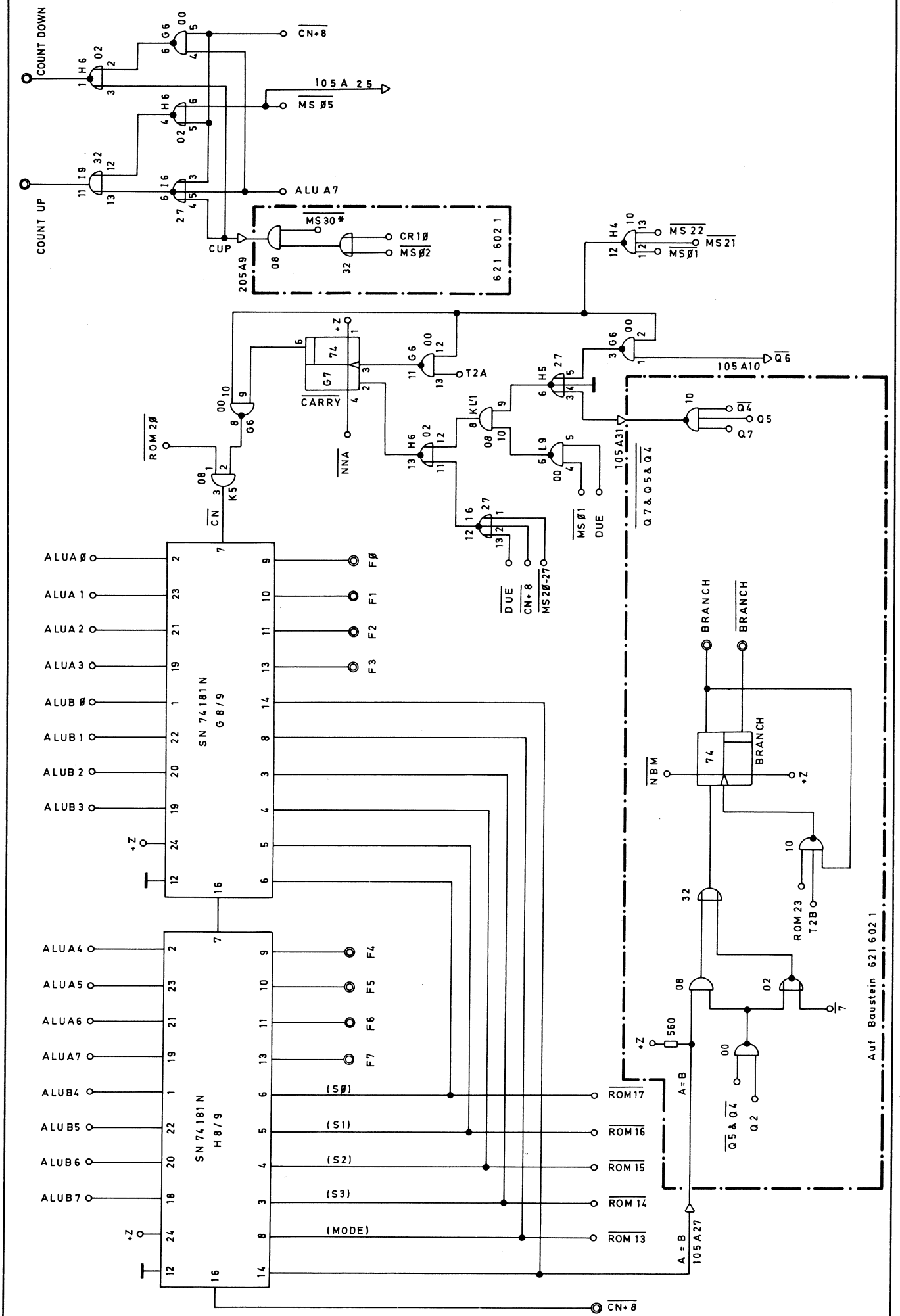
(3) 01.04.05



621 602 K CPU M-Register

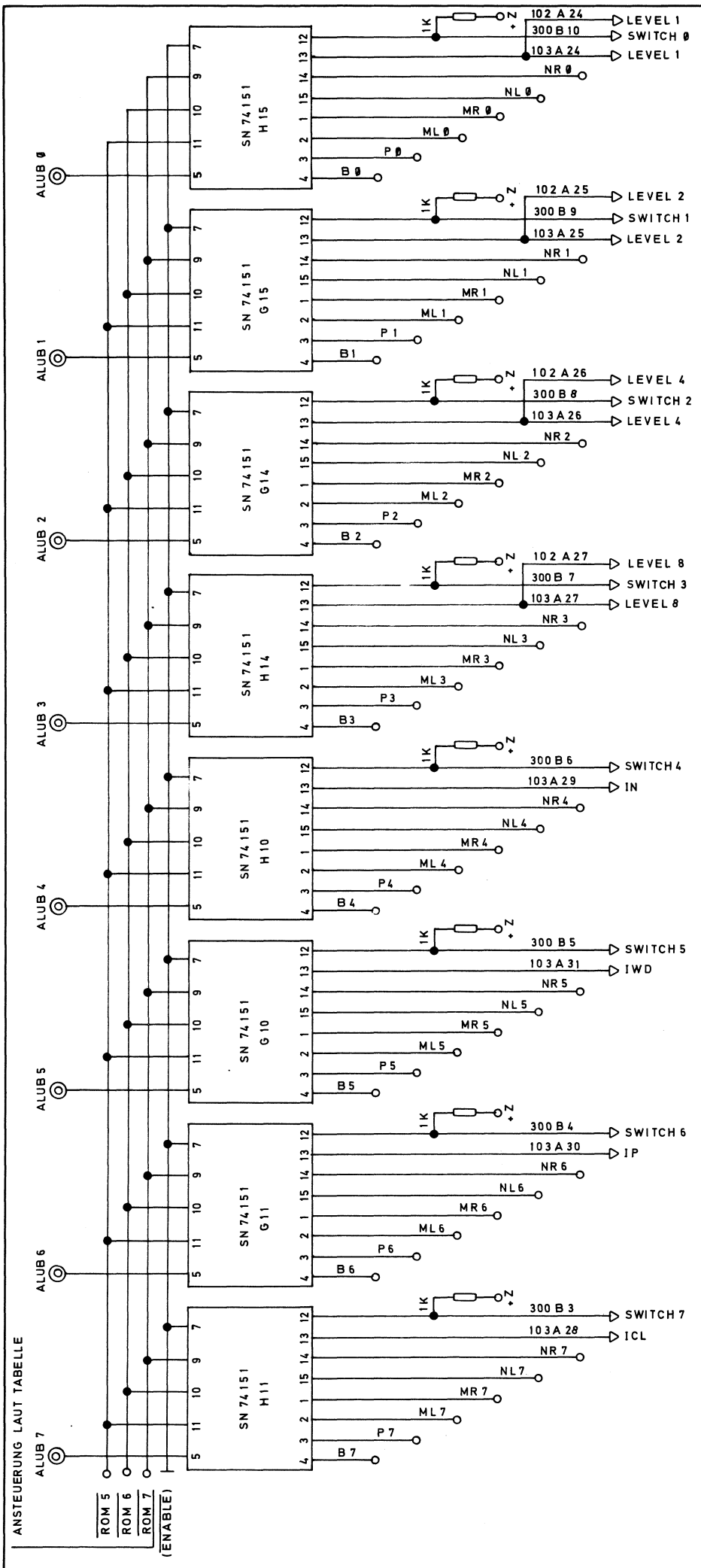
(4) 01.04.06


MSØØ-Ø7
NIOP
NA
SWNR
LOAD NR
300B12
M8
M11
M15
NR Ø
NR 1
NR 2
NR 3
NR 4
NR 5
NR 6
NR 7
300A28
300A27
300A26
300A25
300A24
SN74161
L14
L11
F Ø
F 1
F 2
F 3
F 4
F 5
F 6
F 7
T2
T2A
NNA
M14
M12
M13
COUNT DOWN
COUNT UP
560
NL Ø
NL 1
NL 2
NL 3
NL 4
NL 5
NL 6
NL 7
SN74193
L13
L12
MS3Ø
105 C21
P1
P2
100pF
L16
203 C27
LDNL
M7
300B11
SWNL
LOAD NL
T2A
NL6 v NL5
203 C30
Brücke 1: Urstart bei Adresse '4ØØØ
Brücke 2: Urstart bei Adresse '2ØØØ

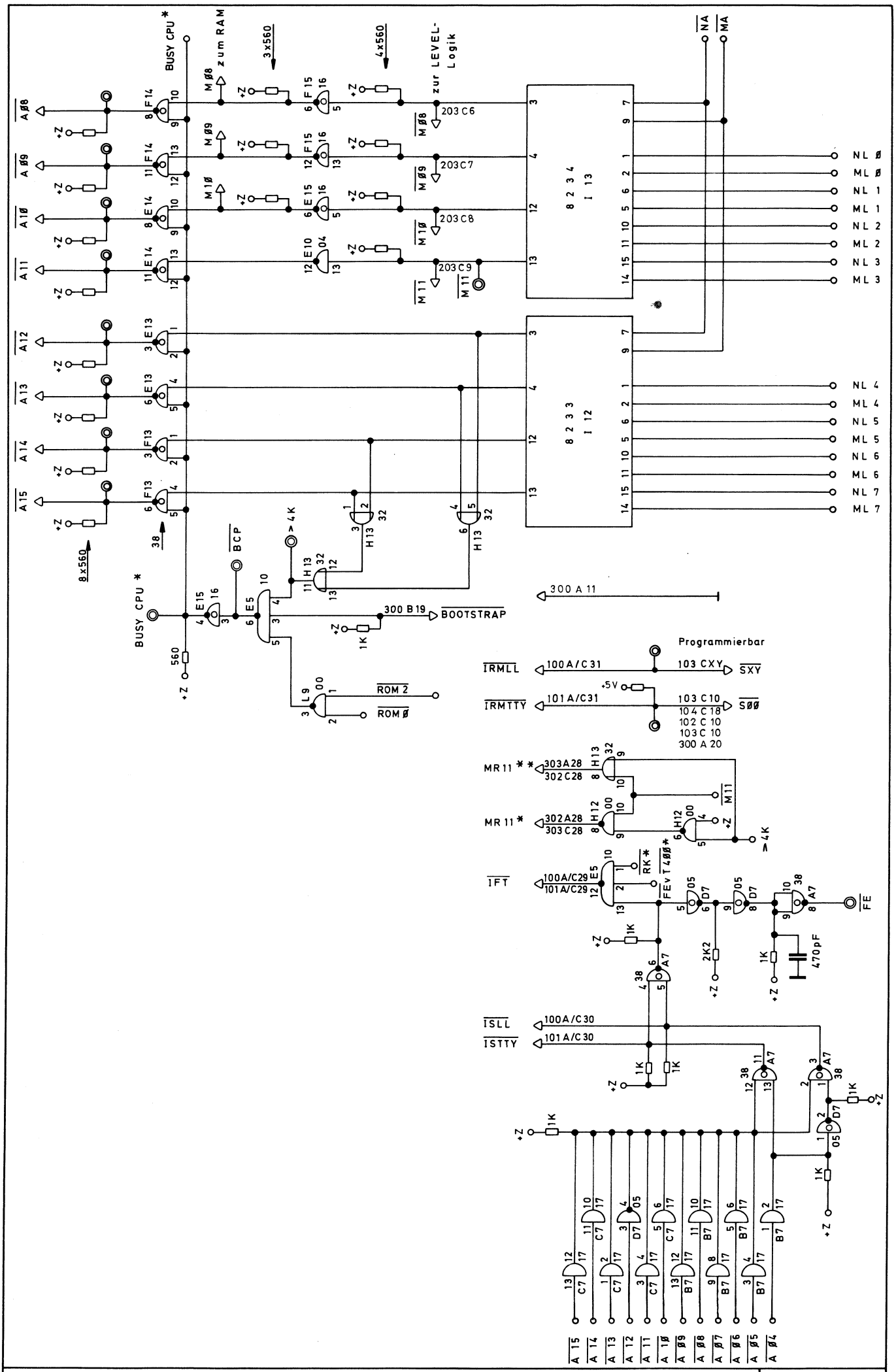


621 602 K CPU ALU

(6) | 01.04.08



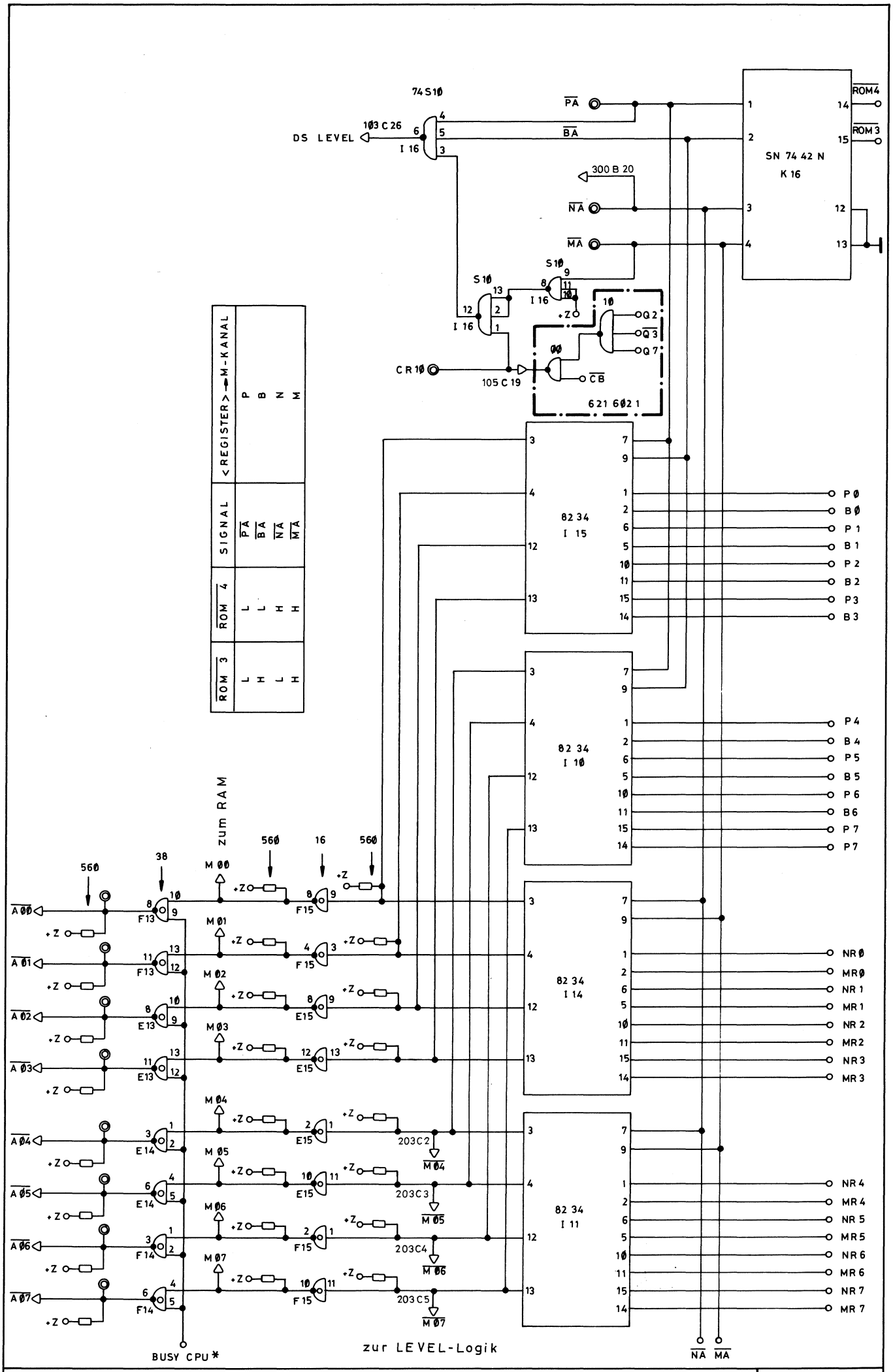
ROM 7	ROM 6	ROM 5	‹REGISTER› ⟶ ALU
L	L	L	B
L	L	H	P
L	H	L	ML
L	H	H	MR
H	L	L	NL
H	L	H	NR
H	H	L	LEVEL
H	H	H	SWITCH



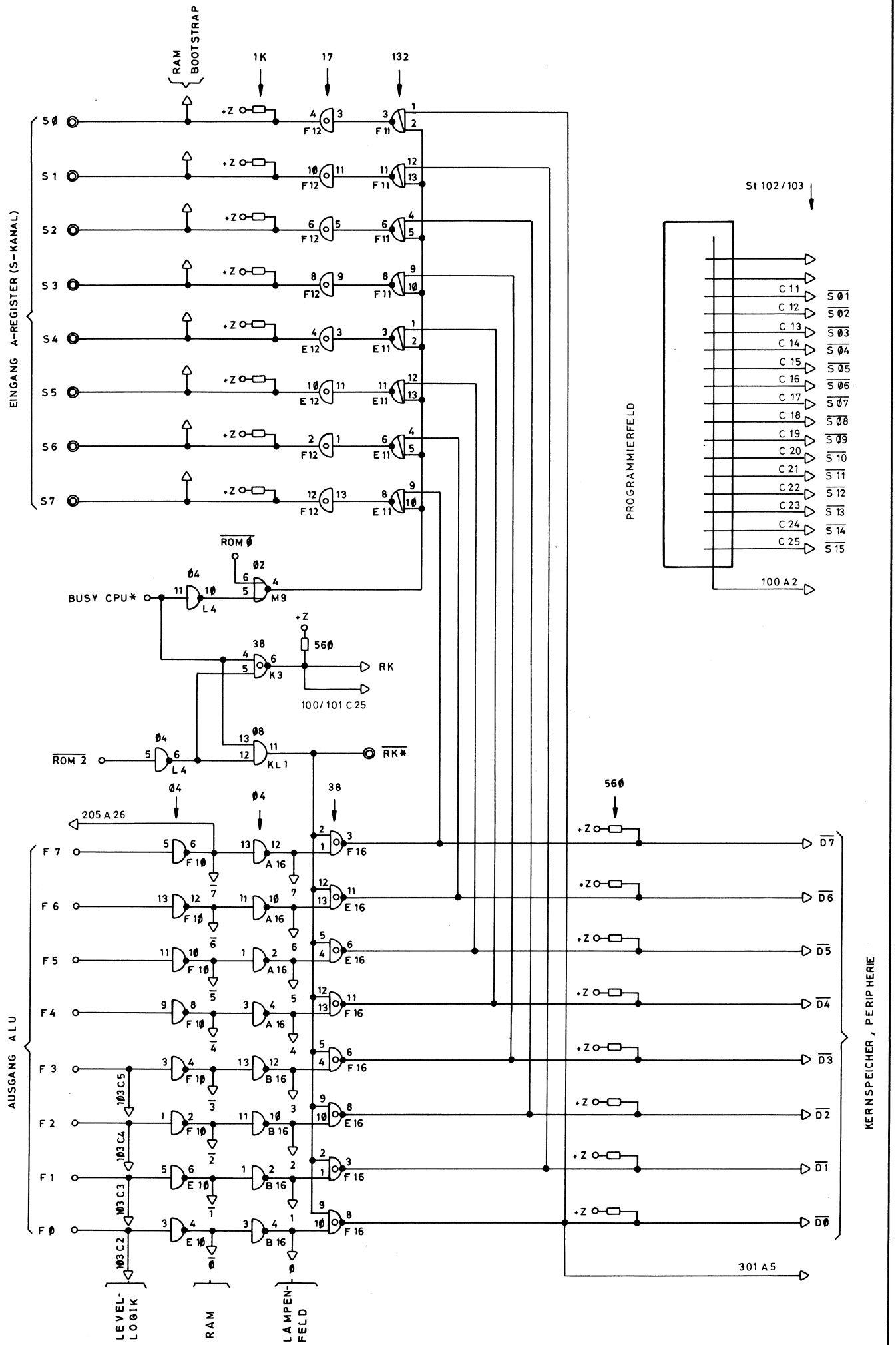
621 602 K CPU M-Kanal Durchschaltungen

(8)

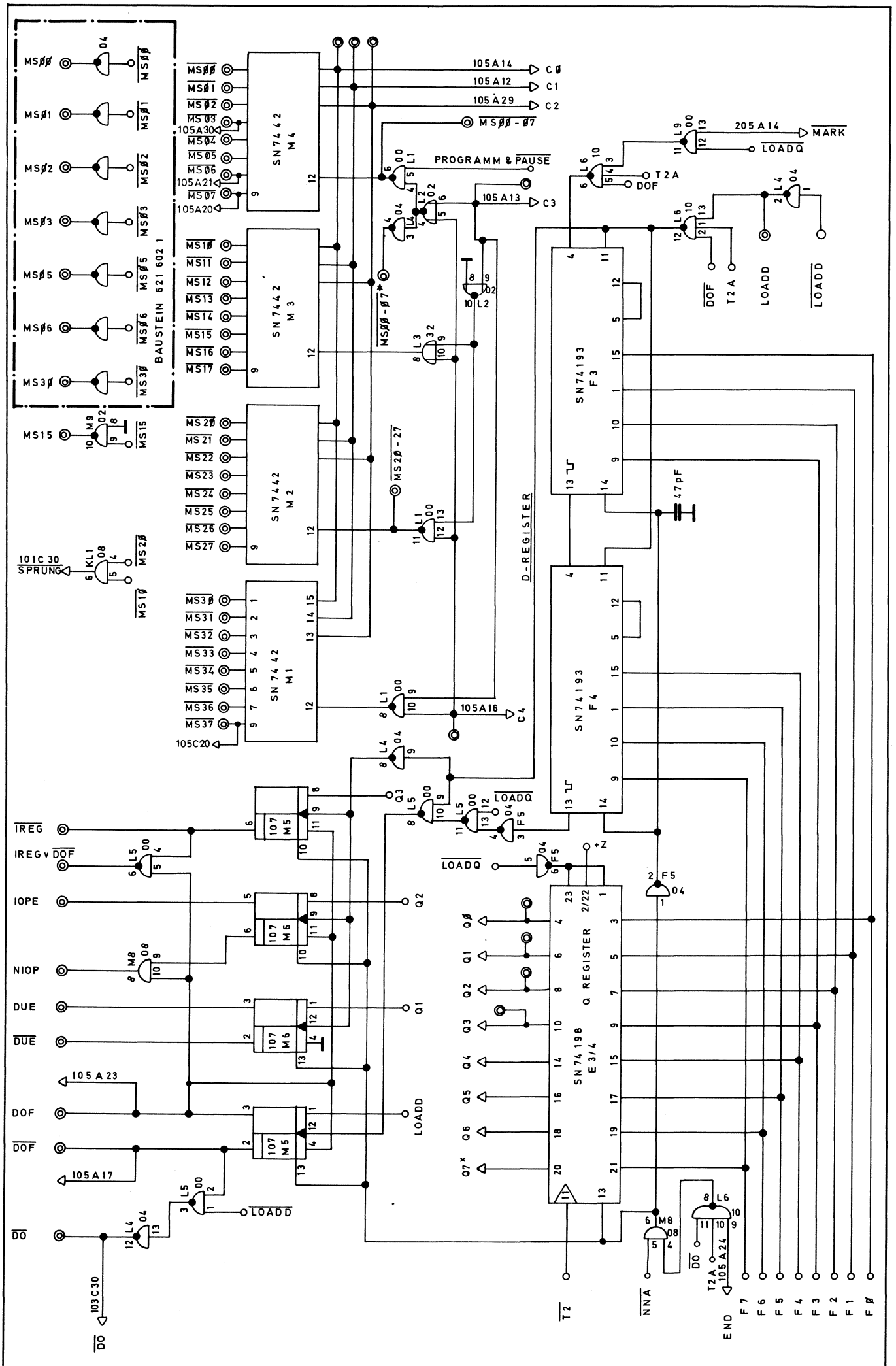
01.04.10



621 602 K CPU M-Kanal Durchschaltungen	(8)	01.04.11

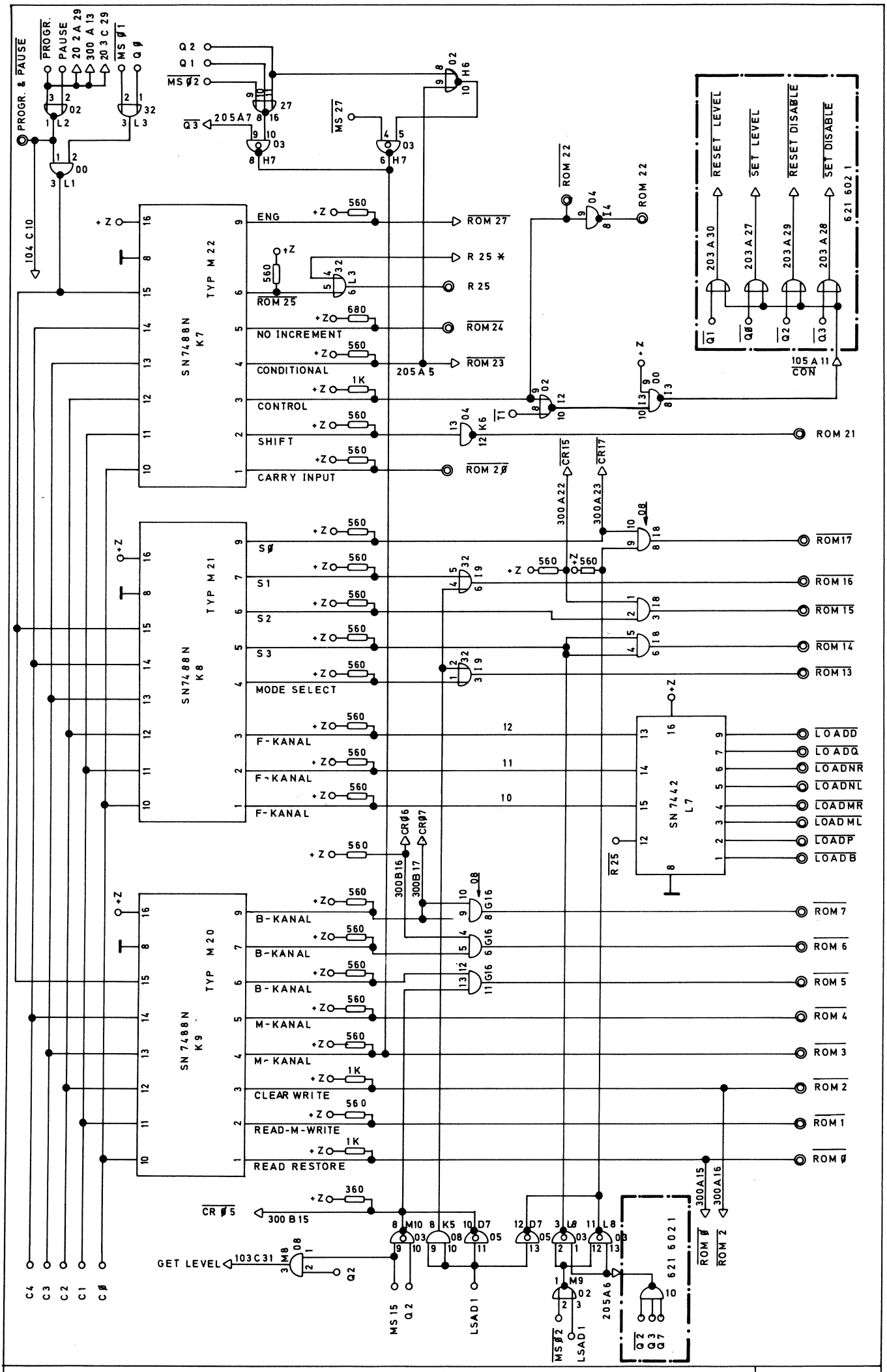


621 602 K CPU F-Kanal Durchschaltungen (9) 01.04.12



621 602 K CPU D & Q Register

(10) 01.04.13



621 602 K CPU ROM Steuersignale

(11) 01.04.14

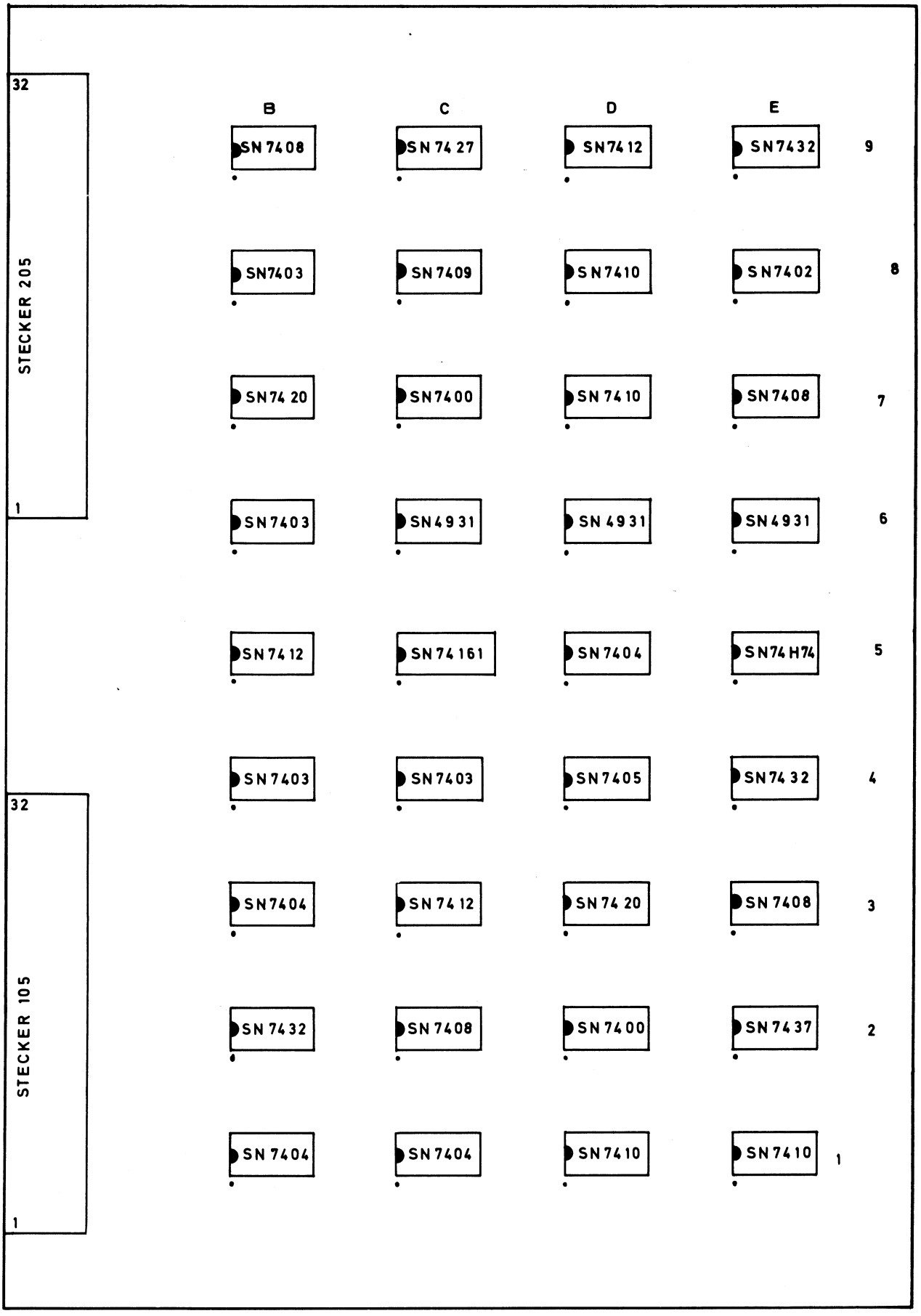
Codierung der ROMs

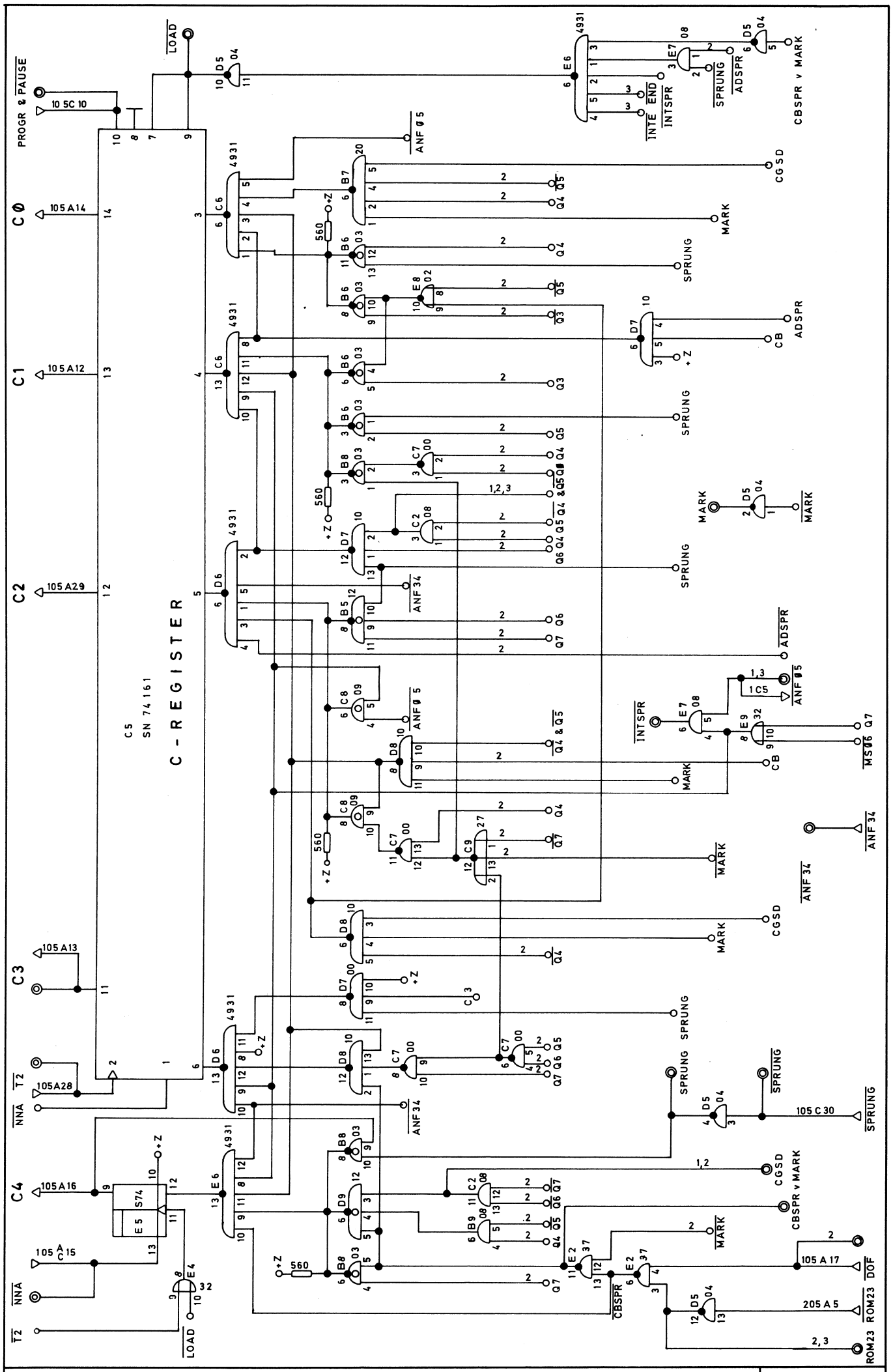
Oktale Adresse	M 20 (K9)									M 21 (K8)									M 22 (K7)								
	ROM	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17		20	21	22	23	24	25	26	27	
	Pin	1	2	3	4	5	6	7	9	1	2	3	4	5	6	7	9		1	2	3	4	5	6	7	9	
0		L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H		H	H	H	H	H	L	L	H	
1		L	H	H	L	H	H	H	H	H	L	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
2		L	H	H	L	H	H	L	H	H	H	L	L	H	L	L	H		H	H	H	H	H	L	L	H	
3		L	H	H	L	H	H	H	H	L	H	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
4		L	H	H	L	H	H	H	H	L	L	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
5		L	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H		H	H	H	H	H	L	L	H	
6		L	H	H	H	L	L	H	L	L	H	L	L	H	L	L	H		H	H	H	H	H	L	L	H	
7		H	L	H	L	L	H	H	H	H	H	H	L	L	L	L	L		L	H	H	H	L	H	L	H	
10		L	H	H	L	L	H	H	H	L	L	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
11		L	H	H	H	H	L	L	L	H	H	H	L	L	H	H	L		H	H	H	L	H	H	L	H	
12		L	H	H	H	H	L	L	L	H	H	H	H	L	H	L	L		H	H	H	L	H	H	L	H	
13		L	H	H	H	H	L	L	L	H	H	H	H	H	L	L	L		H	H	H	L	H	H	L	H	
14		H	H	H	H	H	H	L	L	H	H	H	H	H	L	H	L		H	H	L	H	H	H	L	L	
15		H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	L		H	H	H	H	H	H	L	L	
16		L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H		H	L	H	H	L	H	L	H	
17		H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H		H	H	H	H	H	H	L	L	
20		L	H	H	H	H	H	H	H	L	L	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
21		H	L	H	L	L	L	L	L	H	H	H	L	H	L	L	H		H	H	H	H	H	H	L	L	
22		H	L	H	L	L	L	L	L	H	H	H	L	L	H	H	L		H	H	H	H	H	H	L	L	
23		H	L	H	L	L	L	L	L	H	H	H	H	H	L	H	H		H	H	H	H	H	H	L	L	
24		H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L		H	H	H	H	H	H	L	L	
25		H	L	H	L	L	L	L	L	H	H	H	H	L	H	H	L		H	H	H	H	H	H	L	L	
26		H	H	L	L	L	L	L	L	H	H	H	H	H	L	H	L		H	H	H	H	H	H	L	L	
27		L	H	H	L	L	H	H	H	H	H	H	H	L	L	L	L		H	H	H	L	H	H	L	H	
30		L	H	H	L	H	H	L	H	H	L	H	L	H	L	L	H		H	H	H	H	H	L	L	L	
31		H	H	H	H	H	H	L	L	H	H	H	H	H	L	H	L		H	H	H	H	H	L	L	L	
32		L	H	H	L	L	H	H	H	L	L	L	H	H	H	H	H		H	H	H	H	H	L	L	H	
33		H	H	L	H	H	L	L	L	H	H	H	H	H	L	H	L		H	H	H	H	H	H	L	L	
34		H	H	L	L	L	H	L	H	H	H	H	H	H	L	H	L		H	H	H	H	H	H	L	H	
35		H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L		H	H	H	H	H	H	L	H	
36		H	H	H	H	H	H	H	L	H	L	H	H	H	L	H	L		H	H	H	H	L	L	L	H	
37		H	H	H	H	H	L	H	L	L	L	H	H	H	L	H	L		H	H	H	H	H	L	L	L	

H = ca. 5 V

L = ca. 0 V

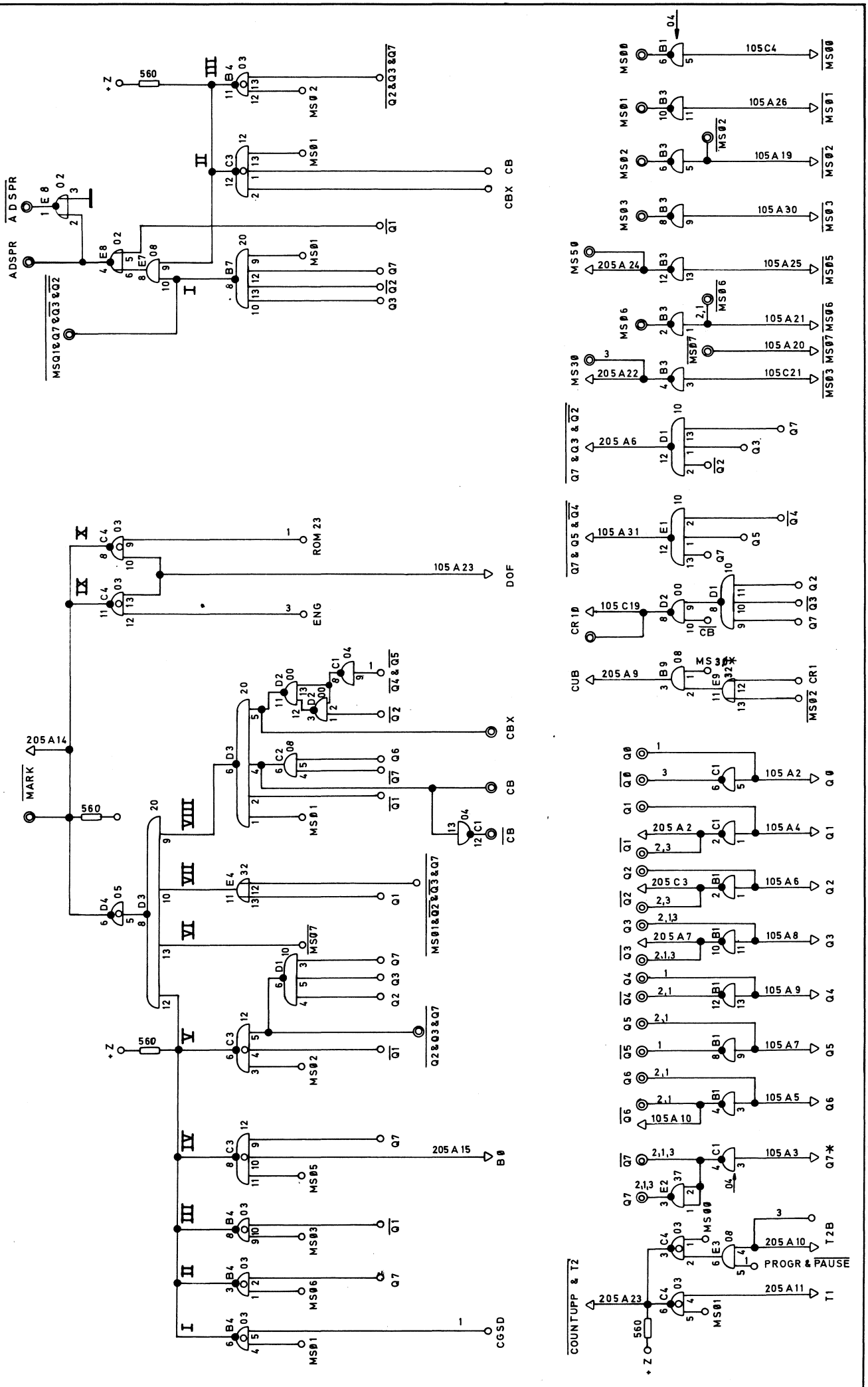
A			B	
ØV		1	MS35-	
T1-		2	MS36-	
MS34-		3	MS33-	
MS32-		4	MS31-	
MS3Ø-		5	MS37-	
MS2Ø-		6	MS21-	
MS26-		7	MS25-	
MS24-		8	MS23-	
MS22-		9	MS27-	
MS15-		10	MS16-	
MS14-		11	MS13-	
MS12-		12	MS11-	
MS1Ø-		13	MS17-	
T2-		14	MSØ1-	
MSØØ-		15	MSØ2-	
MSØ3-		16	MSØ4-	
MSØ5-		17	MSØ6-	
MSØ7-		18	+Z	


32
STECKER 205
1
B
C
D
E
SN7408
SN7427
SN7412
SN7432
9
SN7403
SN7409
SN7410
SN7402
8
SN7420
SN7400
SN7410
SN7408
7
SN7403
SN4931
SN4931
SN4931
6
SN7412
SN74161
SN7404
SN74H74
5
SN7403
SN7403
SN7405
SN7432
4
SN7404
SN7412
SN7420
SN7408
3
SN7432
SN7408
SN7400
SN7437
2
SN7404
SN7404
SN7410
SN7410
1
32
STECKER 105
1

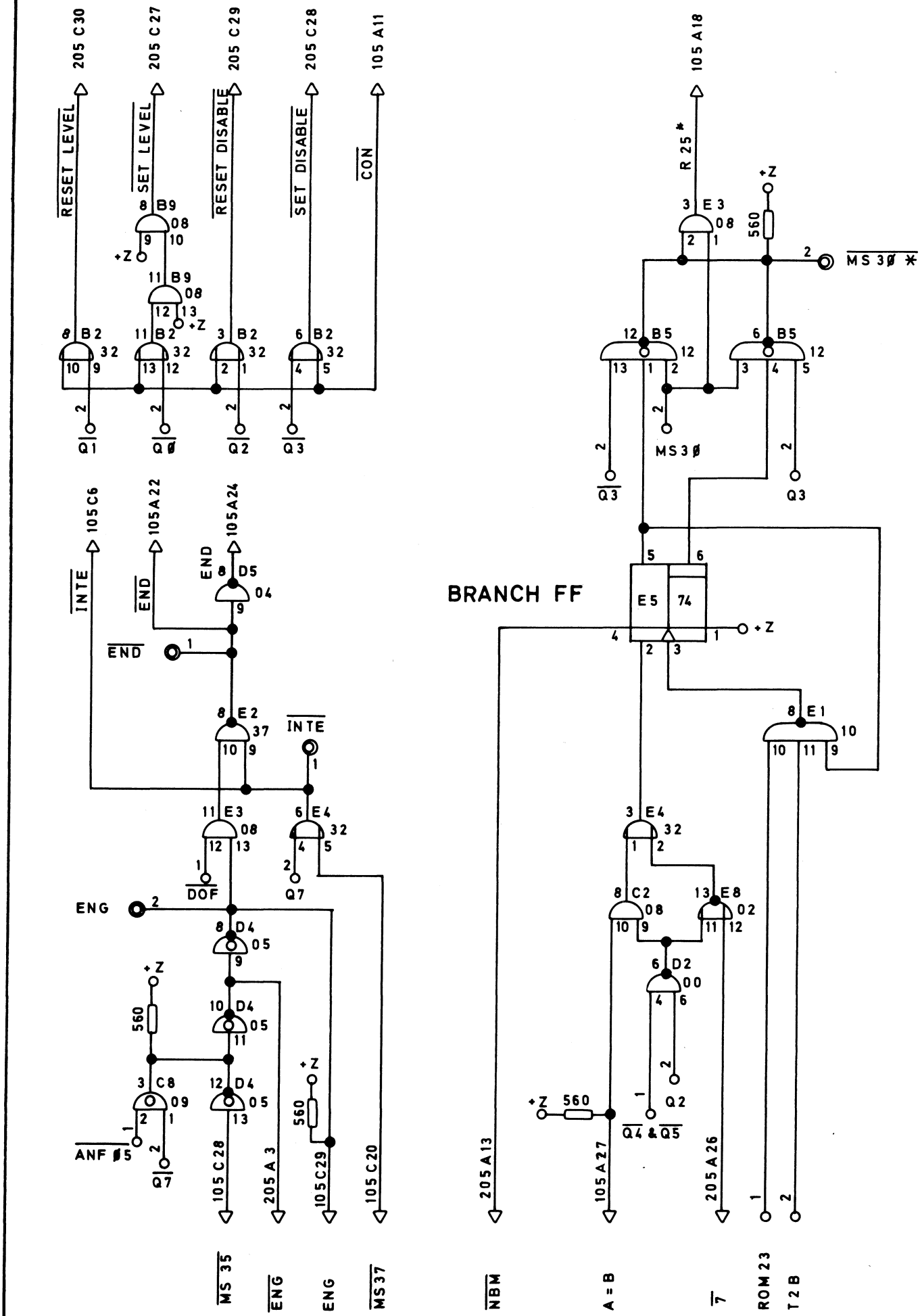


621 6021 B,C1 Schritt - Sprung - Logik

(1) | 01.05.02



621 6021 B,C1	Schritt-Sprung-Logik	(2)	01.05.03



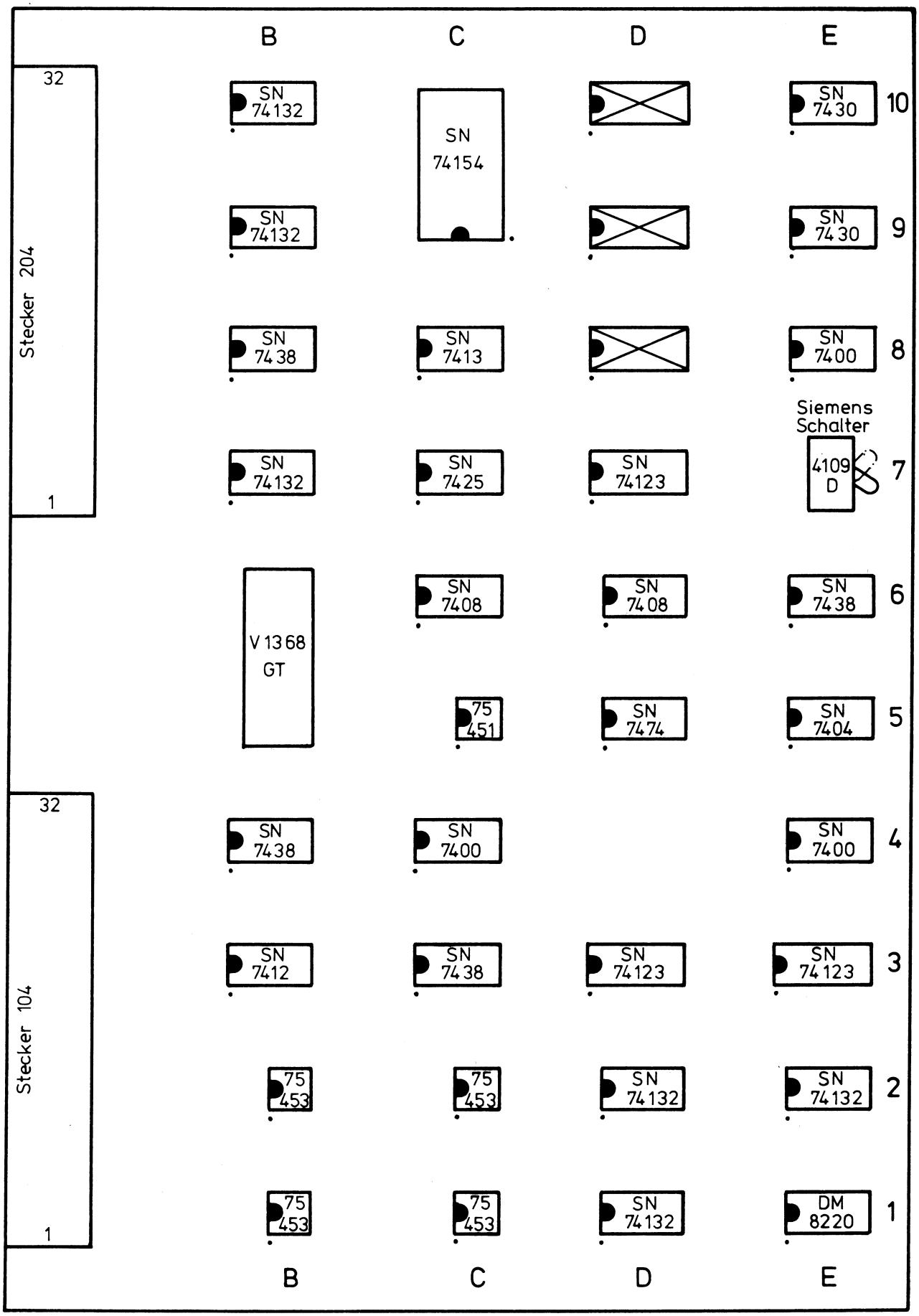
621 602 1 B,C1	Schritt-Sprung-Logik	(3)	01.05.04

105

LEITERSEITE 1 A		BAUELEMENTSEITE 1 C
+ Z	1	+ Z
Q Ø	2	
Q 7 *	3	
Q 1	4	$\overline{\text{MS ØØ}}$
Q 6	5	$\overline{\text{ANF Ø5}}$
Q 2	6	$\overline{\text{INTE}}$
Q 5	7	
Q 3	8	
Q 4	9	
$\overline{\text{Q 6}}$	10	PROG & $\overline{\text{PAUSE}}$
$\overline{\text{CON}}$	11	
C 1	12	
C 3	13	
C Ø	14	
$\overline{\text{NNA}}$	15	$\overline{\text{NNA}}$
C 4	16	
$\overline{\text{DOF}}$	17	
R 25 *	18	
$\overline{\text{MS Ø2}}$	19	CR 1Ø
$\overline{\text{MS Ø7}}$	20	$\overline{\text{MS 37}}$
$\overline{\text{MS Ø6}}$	21	$\overline{\text{MS 3Ø}}$
$\overline{\text{END}}$	22	
DOF	23	
END	24	
$\overline{\text{MS Ø5}}$	25	
$\overline{\text{MS Ø1}}$	26	
A = B	27	$\overline{\text{ANF 34}}$
$\overline{\text{T 2}}$	28	$\overline{\text{MS 35}}$
C 2	29	ENG
$\overline{\text{MS Ø3}}$	30	$\overline{\text{SPRUNG}}$
$\overline{\text{Q 7 & Q 5 & Q 4}}$	31	
⊥	32	⊥

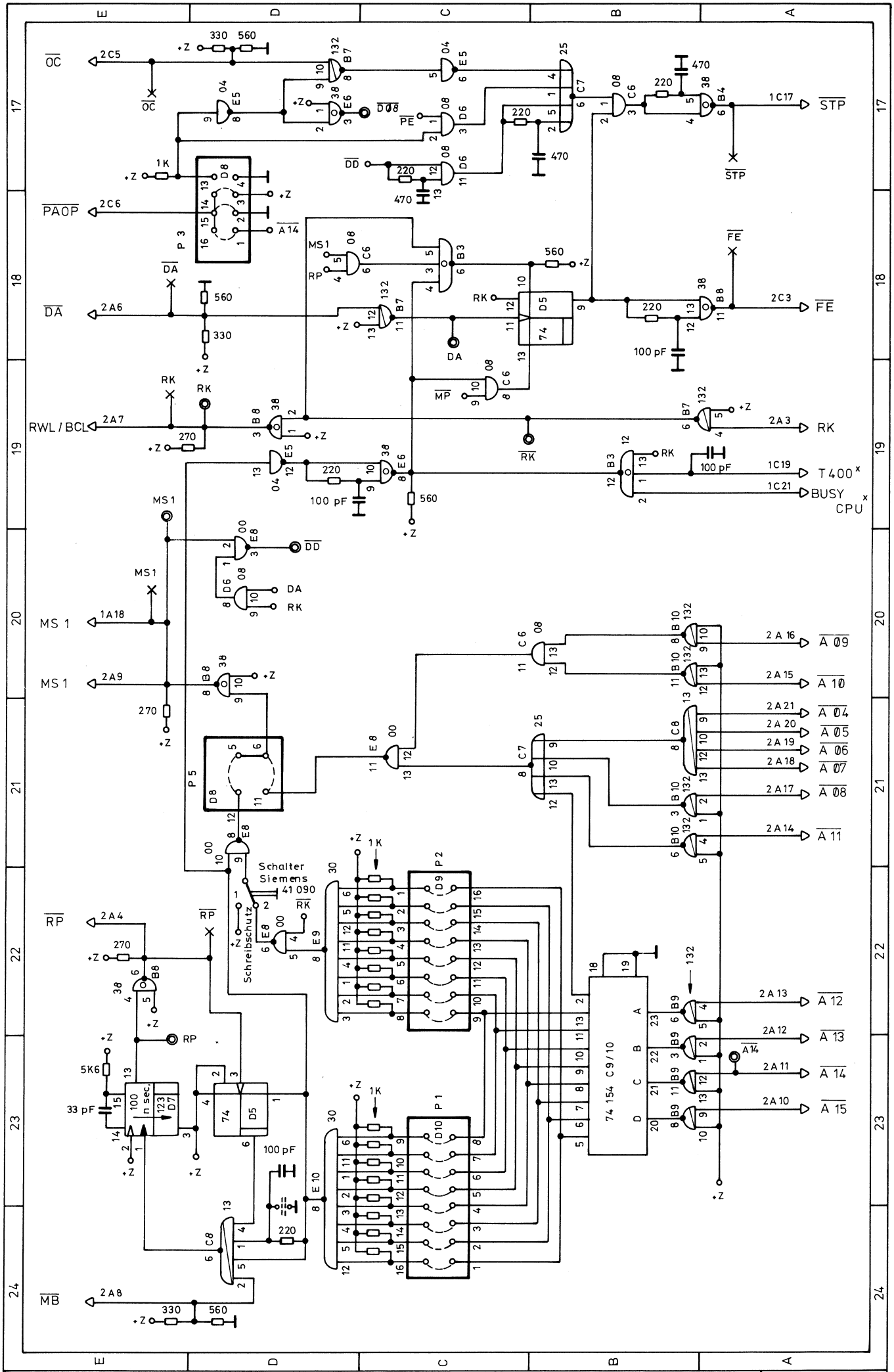
205

LEITERSEITE 2 A		BAUELEMENTSEITE 2 C
+ Z	1	+ Z
$\overline{\text{Q 1}}$	2	
$\overline{\text{ROM 27}}$	3	$\overline{\text{Q 2}}$
	4	
$\overline{\text{ROM 23}}$	5	
$\overline{\text{Q 7 & Q 3 & Q 2}}$	6	
$\overline{\text{Q 3}}$	7	
	8	
CUP	9	
T 2 B	10	
T 1	11	
$\overline{\text{T 1}}$	12	
$\overline{\text{NBM}}$	13	
$\overline{\text{MARK}}$	14	
B Ø	15	
	16	
	17	
	18	
	19	
	20	
	21	
MS 3Ø	22	
$\overline{\text{COUNTUPP & T 2}}$	23	
MS Ø5	24	
	25	
$\overline{7}$	26	
	27	SET LEVEL
	28	SET DISABLE
	29	RESET DISABLE
	30	RESET LEVEL
	31	
⊥	32	⊥



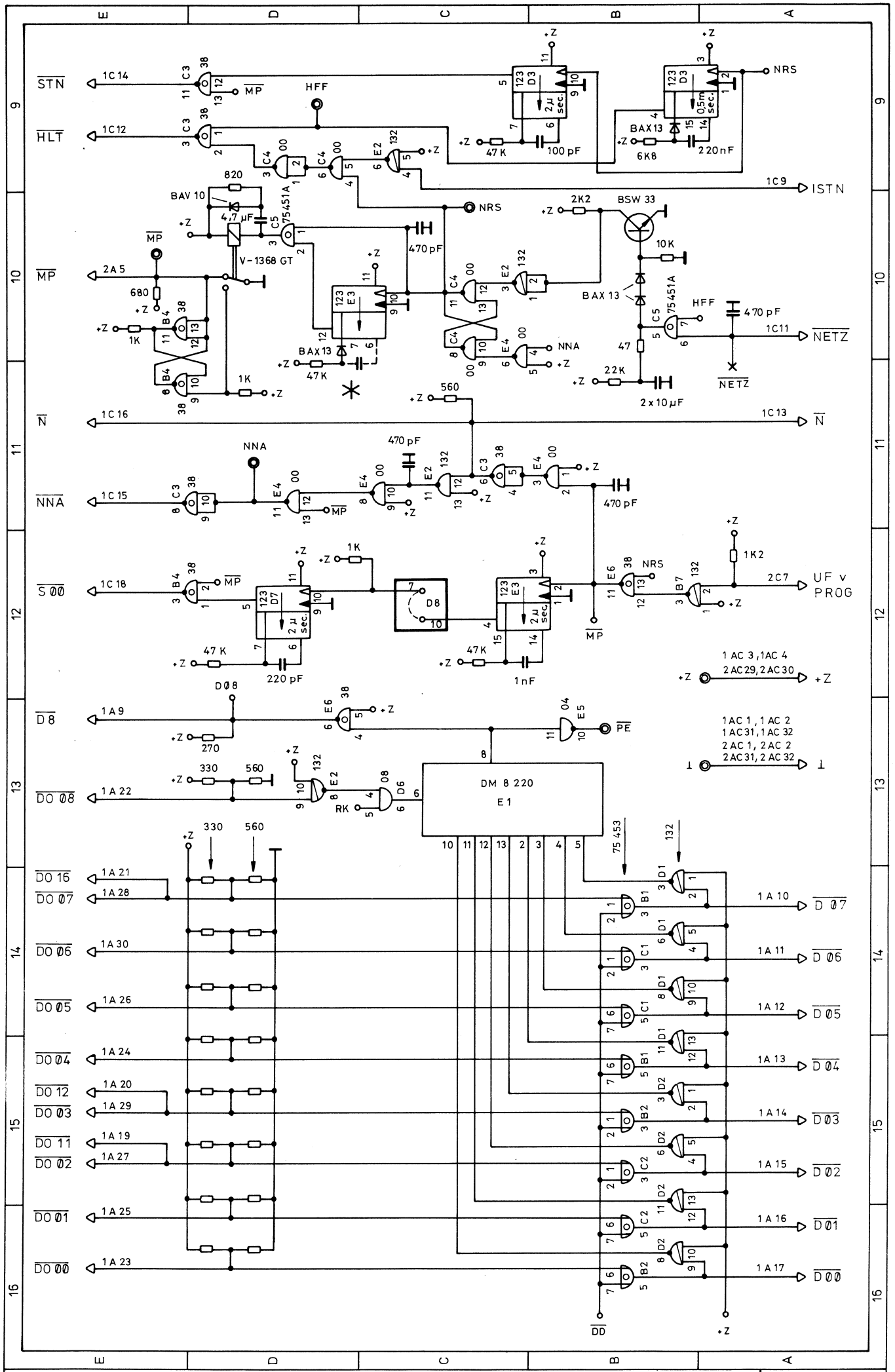
Lötsockel
DIL-Sockel
16pol-Burndy
Plattform 16pol
A 23-2049 LC

621 603 8 R, S1, S2	Kernspeicher Anpassungskarte	01.06.01



621 603 8 R,S1,S2 KERNSPEICHER-ANPASSUNGSK.

01.06.02



621 603 8 R,S1,S2 KERNSPEICHER-ANPASSUNGSK.

01.06.03

Programmierfelder:

P1 Adreßentschlüsselung

Kernspeicher	Brücken	Adreßbereiche
4K	1-16	'4ØØØ - '4FFF
8K	1-16,2-15	'4ØØØ - '5FFF
16K	1-16, 2-15, 3-14, 4-13	'4ØØØ - '7FFF
32K	1-16, 2-15, 3-14, 4-13 5-12, 6-11, 7-10, 8- 9	'4ØØØ - 'BFFF

P2 Sperrbereich

Jede Brücke schützt einen Bereich von 4K gegen Einschreiben

Adreßbereiche	Brücke	Adreßbereiche	Brücke
'4ØØØ - '4FFF	1-16	'8ØØØ - '8FFF	5-12
'5ØØØ - '5FFF	2-15	'9ØØØ - '9FFF	6-11
'6ØØØ - '6FFF	3-14	'AØØØ - 'AFFF	7-10
'7ØØØ - '7FFF	4-13	'BØØØ - 'BFFF	8- 9

P3 Parityerzeugung

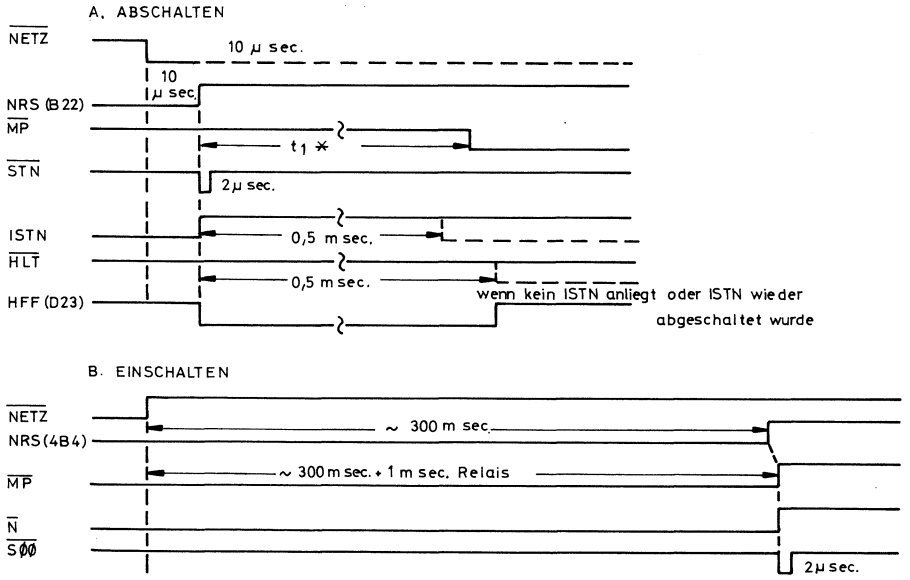
Kernspeicher	Brücken	Parityerzeugung
4,8,16K	2-15	auf KS-Anpassungskarte
4,8,16K	3-14, 4-13	im KS
32K	1-16	auf KS-Anpassungskarte

P4 Wiederstart: Brücke 7-10
kein Wiederstart: keine Brücke

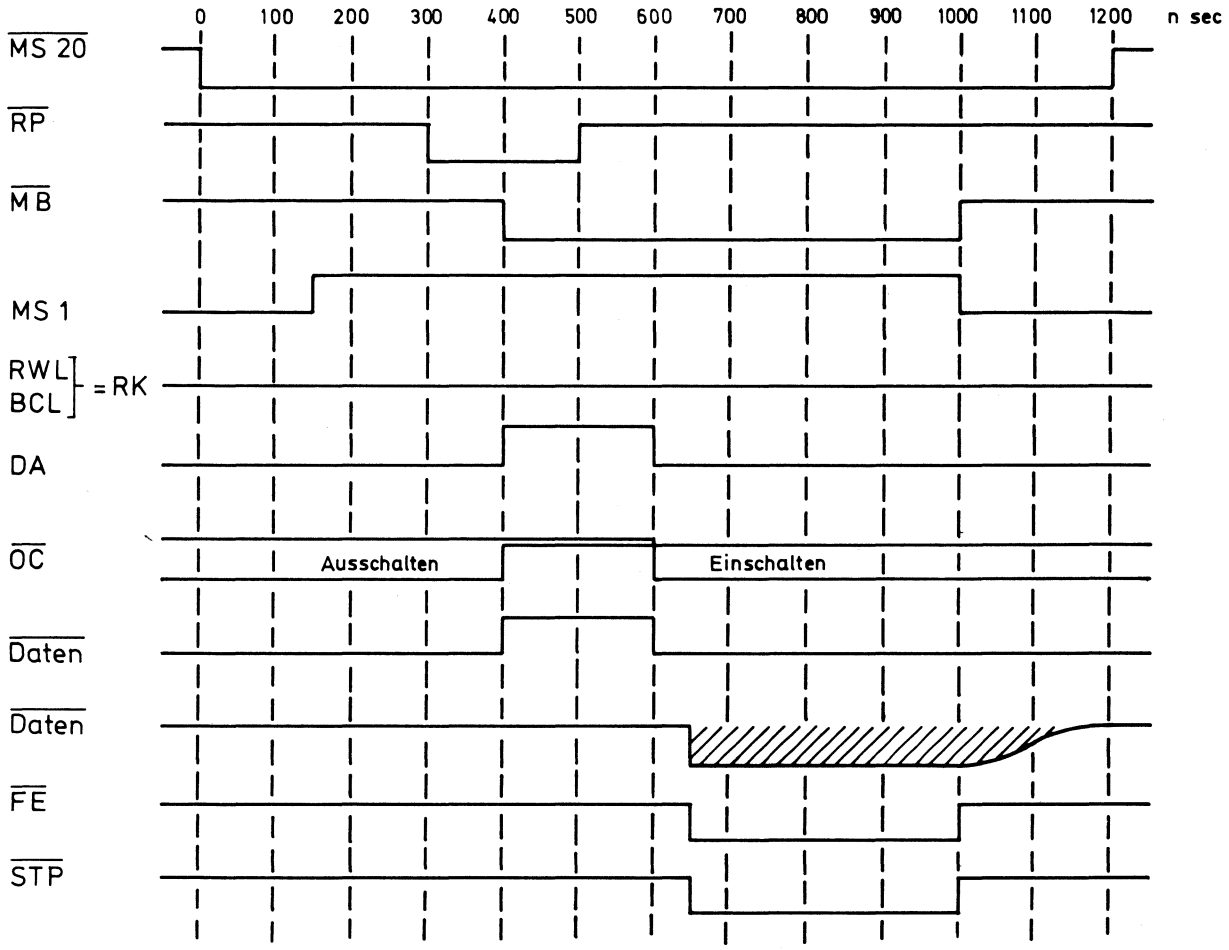
P5 Anwahl KS-Gleitkommarechenwerk
Anwahl KS : Brücke: 5-12
Anwahl GKR: Brücke: 6-11 (Adresse '16 ØX)

* C = Ø bei Stromversorgung 621 3 (t_1 = 1,4 ms)
C = 100 nF bei Stromversorgung 621 720 (t_1 = 3 msec)

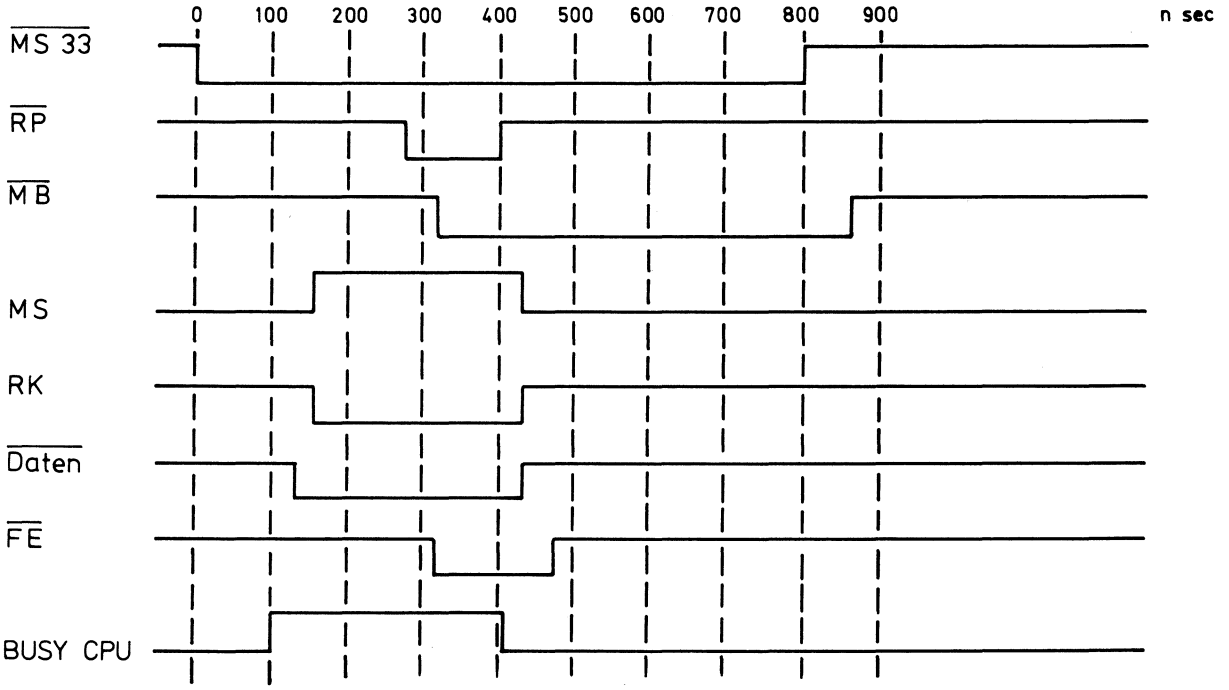
Impulsdiagramm Netzausfallschutz



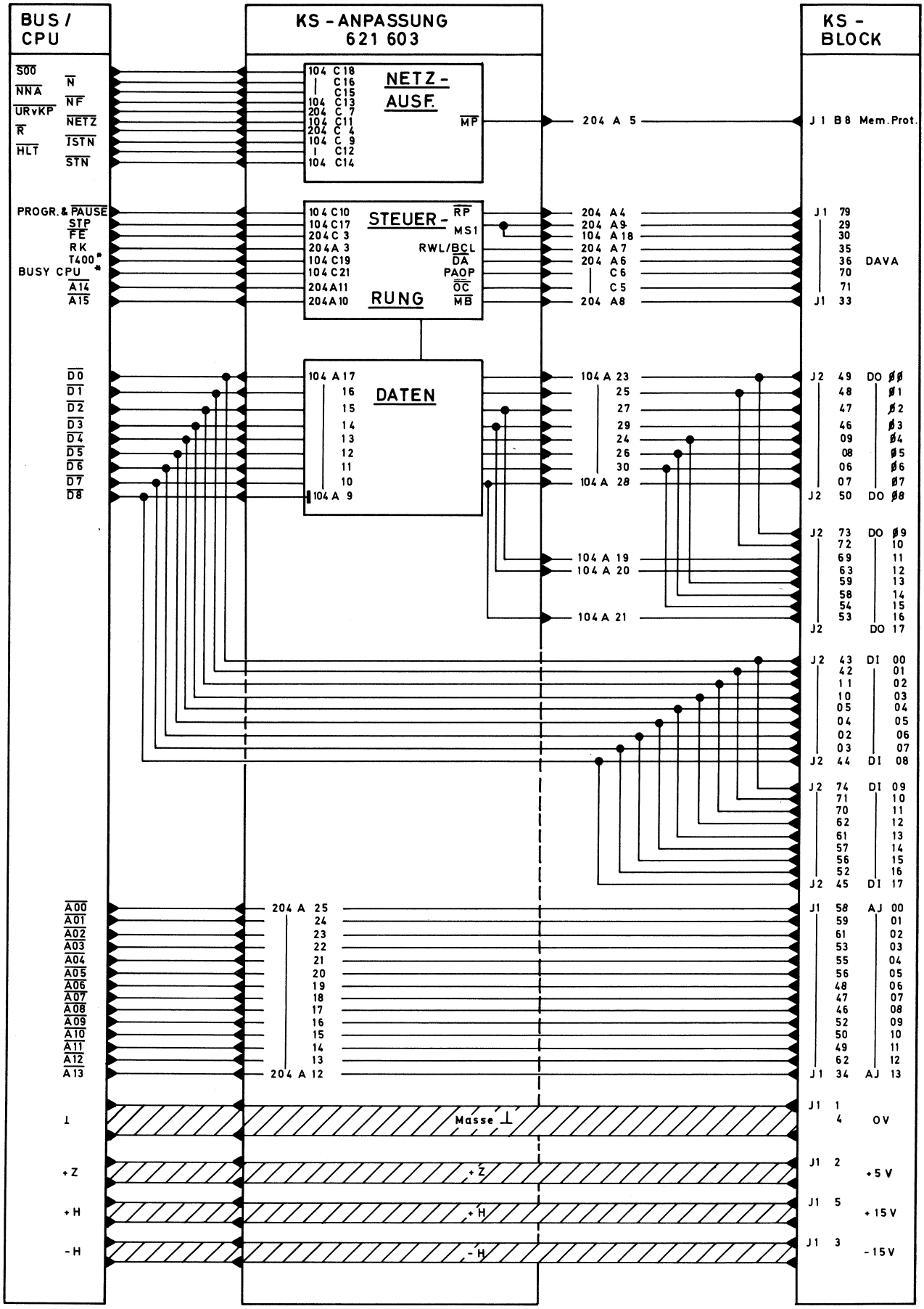
READ RESTORE ZYKLUS



CLEAR WRITE ZYKLUS



Ablaufdiagramm Kernspeicherzugriff	01.06.05


BUS / CPU
KS - ANPASSUNG 621 603
KS - BLOCK
NETZ - AUSF.
STEUER - RUNG
DATEN
Masse ⊥
Blockdiagramm Kernspeicheranschluß
01.06.06

104

Leiterseite 1A			Bauelementseite 1C	
ØV		1	ØV	
ØV		2	ØV	
+Z		3	+Z	
+Z		4	+Z	
ØV		5	ØV	
+H		6	+H	
-H		7	ST-H	
ST+Z		8	ST+H	
DØ8-		9	ISTN	
DØ7-		10	Progr.&Pause-	
DØ6-		11	Netz-	
DØ5-		12	HLT-	
DØ4-		13	NF-	
DØ3-		14	STN-	
DØ2-		15	NNA-	
DØ1-		16	N-	
DØØ-		17	STP-	
MS1(4k)		18	SØØ-	
DO11-		19	T4ØØ^{x}	
DO12-		20	Busy CPU*	
DO16-		21		
DOØ8-		22	ØV	
DOØØ-		23	ØV	
DOØ4-		24	ØV	
DOØ1-		25	ØV	
DOØ5-		26	ØV	
DOØ2-		27	ØV	
DOØ7-		28	ØV	
DOØ3-		29	ØV	
DOØ6-		30	ØV	
ØV		31	ØV	
ØV		32	ØV	

204

Leiterseite 2A			Bauelementseite 2C	
ØV		1	ØV	
ØV		2	ØV	
RK		3	FE-	
RP-		4	R-	
MP-		5	OC-	
DA-		6	PAOP-	
RWL/BCL		7	UF v PROG	
MB-		8		
MS1 (16k)		9	+T	
A15-		10	+T	
A14-		11	ØV	
A13-		12	ØV	
A12-		13	ØV	
A11-		14	ØV	
AlØ-		15	ØV	
AØ9-		16	ØV	
AØ8-		17	ØV	
AØ7-		18	ØV	
AØ6-		19	ØV	
AØ5-		20	ØV	
AØ4-		21	ØV	
AØ3-		22	ØV	
AØ2-		23	ØV	
AØ1-		24	ØV	
AØØ-		25	ØV	
-H		26	-H	
+H		27	+H	
ØV		28	ØV	
+Z		29	+Z	
+Z		30	+Z	
ØV		31	ØV	
ØV		32	ØV	

CPU St 1 Platz 104				Rangierleiterplatte				KS-Stecker 4k J2 621603500	
				a		b			
a		c		a		b			
⊥	1	⊥		⊥	1	⊥		1	⊥
⊥	2	⊥		DØØ6/15-	2	⊥		18	DØØ8 -
+Z	3	+Z		DØØ3 -	3	⊥		20	DØØ7 -
+Z	4	+Z		DØØ7 -	4	⊥		22	DØØ6 -
⊥	5	⊥		DØØ2 -	5	⊥		25	DØØ5 -
+H	6	+H		DØØ5/14-	6	⊥		27	DØØ4 -
-H	7	ST-H		DØØ1/1Ø-	7	⊥		29	DØØ3 -
ST+Z	8	ST+H		DØØ4/13-	8	⊥		32	DØØ2 -
D Ø8-	9	ISTN		DØØØ/Ø9-	9	⊥		34	DØØ1 -
D Ø7-	10	PP -		DØØ8/17-	10	⊥		36	DØØØ -
D Ø6-	11	Netz-		DØ16 -	11	BUSY CPU*	x	38	+Z
D Ø5-	12	HLT -		DØ12 -	12	MS2	x	39	+Z
D ØØ-	13	NF -		DØ11 -	13	T4ØØ x	x	40	⊥
D Ø3-	14	STN -		MS 1	14	SØØ -		41	⊥
D Ø2-	15	NNA -		DØØ/Ø9 -	15	STP -		43	MS 1
D Ø1-	16	N -		DØ1/1Ø -	16	N -		46	MS2
D ØØ-	17	STP -		DØ2/11--	17	NNA -		49	+Z
MS 1	18	SØØ -		DØ3/12 -	18	STN -		58	DØ8 -
DØ11-	19	T4ØØ x	x	DØ4/13 -	19	NF -		60	DØ7 -
DØ12-	20	MS2	x	DØ5/14 -	20	HLT -		62	DØ6 -
DØ16-	21	BUSY CPU*	x	DØ6/15 -	21	Netz -		65	DØ5 -
DØØ8-	22	⊥		DØ7/16 -	22	PP -		67	DØ4 -
DØØØ-	23	⊥		DØ8/17 -	23	ISTN		69	DØ3 -
DØØ4-	24	⊥		ST+Z	24	ST+H		72	DØ2 -
DØØ1-	25	⊥		-H	25	ST-H		74	DØ1 -
DØØ5-	26	⊥		+H	26	+H		76	DØØ -
DØØ2-	27	⊥		⊥	27	⊥		78	+Z
DØØ7-	28	⊥		+Z	28	+Z		79	+Z
DØØ3-	29	⊥		+Z	29	+Z		80	⊥
DØØ6-	30	⊥		⊥	30	⊥			
⊥	31	⊥							
⊥	32	⊥		x ab CPU 621 602 E					

4kJ2 ist ⊥ auf 3;6;9;13;15;17;19;21;23;26;28;30;33;35;37;
4k

Adapterkabel KS 4 K J2 | 01.06.08

CPU St 2 Platz 204			Rangierleiterplatte			KS-Stecker 4k J1 621603400	
a		c	a		b		
⊥	1	⊥	⊥	1	⊥	1	⊥
⊥	2	⊥	+Z	2	+Z	2	+Z
RK-	3	FE -	+Z	3	+Z	3	+Z
RP-	4	R- x	⊥	4	⊥	4	⊥
MP-	5	OC- x	+H	5	+H	6	AØ7-
DA-	6	PAOP- x	-H	6	-H	9	AØ5-
RWL/BCL	7	UFvPROG- x	AØØ-	7	⊥	13	AØ4-
MB-	8	+T x	AØ1-	8	⊥	16	AØ2-
MS1	9	+T x	AØ2-	9	⊥	19	AØØ-
A15-	10	frei x	AØ3-	10	⊥	22	A1Ø-
A14-	11	MS2- x	AØ4-	11	⊥	32	⊥
A13-	12	⊥	AØ5-	12	⊥	40	⊥
A12-	13	⊥	AØ6-	13	⊥	41	⊥
A11-	14	⊥	AØ7-	14	⊥	42	+Z
A10-	15	⊥	AØ8-	15	⊥	43	+Z
AØ9-	16	⊥	AØ9-	16	⊥	46	AØ6-
AØ8-	17	⊥	A1Ø-	17	⊥	49	AØ8-
AØ7-	18	⊥	A11-	18	⊥	53	AØ3-
AØ6-	19	⊥	A12-	19	⊥	56	AØ1-
AØ5-	20	⊥	A13-	20	⊥	59	A11-
AØ4-	21	⊥	A14-	21	MS2- x	62	AØ9-
AØ3-	22	⊥	A15-	22	frei x	64	+Z
AØ2-	23	⊥	MS 1	23	+T x	66	RP -
AØ1-	24	⊥	MB -	24	+T x	67	+Z -
AØØ-	25	⊥	RWL/BCL	25	frei x	69	RWL-
-H	26	-H	DA-	26	PAOP- x	70	MB -
+H	27	+H	MP-	27	OC- x	72	DA -
⊥	28	⊥	RP-	28	R- x	73	MP -
+Z	29	+Z	RK-	29	FE-	80	⊥
+Z	30	+Z	⊥	30	⊥	34	A12- } FWSp.
⊥	31	⊥				11	+T } FWSp.
⊥	32	⊥					

x ab CPU 621 602 E

4kJ1 ist ⊥ auf 7;10;14;17;20;23;25;28;30;31;33;44;47;50;54; 57;60;63;65;68;71;

Adapterkabel KS 4 K J 1 | 01.06.09

CPU St 1 Platz 104			Rangierleiterplatte			KS-Stecker 8k/16k/J2 U621605200		
a		c	a		b			
⊥	1	⊥	⊥	1	⊥	1 ⊥		
⊥	2	⊥	DØØ6/15-	2	⊥	2 DØ6-		
+Z	3	+Z	DØØ3 -	3	⊥	3 DØ7-		
+Z	4	+Z	DØØ7 -	4	⊥	4 DØ5-		
⊥	5	⊥	DØØ2 -	5	⊥	5 DØ4-		
+H	6	+H	DØØ5/14-	6	⊥	6 DØØ6-		
-H	7	ST-H	DØØ1/1Ø-	7	⊥	7 DØØ7-		
ST+Z	8	ST+H	DØØ4/13-	8	⊥	8 DØØ5-		
DØ8-	9	IST N	DØØØ/Ø9-	9	⊥	9 DØØ4-		
DØ7-	10	PP -	DØØ8/17-	10	⊥	10 DØ3		
DØ6-	11	Netz-	DØ16 -	11	BUSY CPU* x	11 DØ2-		
DØ5-	12	HLT -	DØ12 -	12	MS2 x	36 +H		
DØ4-	13	NF -	DØ11 -	13	T4ØØ	37 ⊥		
DØ3-	14	STN -	MS1	14	SØØ -	38 -H		
DØ2-	15	NNA -	DØØ/Ø9 -	15	STP -	39 +Z		
DØ1-	16	N -	DØ1/1Ø -	16	N -	40 ⊥		
DØØ-	17	STP -	DØ2/11 -	17	NNA -	41 ⊥		
MS1	18	SØØ -	DØ3/12 -	18	STN -	42 DØ1-		
DØ11-	19	T4ØØ x	DØ4/13 -	19	NF -	43 DØØ-		
DØ12-	20	MS2- x	DØ5/14 -	20	HLT -	44 DØ8-		
DØ16-	21	BUSY CPU* x	DØ6/15 -	21	Netz -	45 D17-		
DØ8-	22	⊥	DØ7/16 -	22	PP -	46 DØ3-		
DØØØ-	23	⊥	DØ8/17 -	23	ISTN	47 DØ2-		
DØØ4-	24	⊥	ST+Z	24	ST+H	48 DØ1-		
DØØ1-	25	⊥	-H	25	ST-H	49 DØØØ-		
DØØ5-	26	⊥	+H	26	+H	50 DØØ8-	69	D011-
DØØ2-	27	⊥	⊥	27	⊥	51 D017-	70	D11-
DØØ7-	28	⊥	+Z	28	+Z	52 D16-	71	D1Ø-
DØØ3-	29	⊥	+Z	29	+Z	53 DØ16-	72	DØ1Ø-
DØØ6-	30	⊥	⊥	30	⊥	54 DØ15-.	73	DØØ9-
⊥	31	⊥	x CPU 621 602 E			56 D15-	74	DØ9-
⊥	32	⊥				57 D14-	76	+H
						58 DØ14-	77	⊥
						59 DØ13-	78	-H
						61 D13-	79	+Z
						62 D12-	80	⊥
						63 DØ12-		

8k/16k/J2 ist ⊥ auf 35;37;55;60;64;
65;66;67;68;

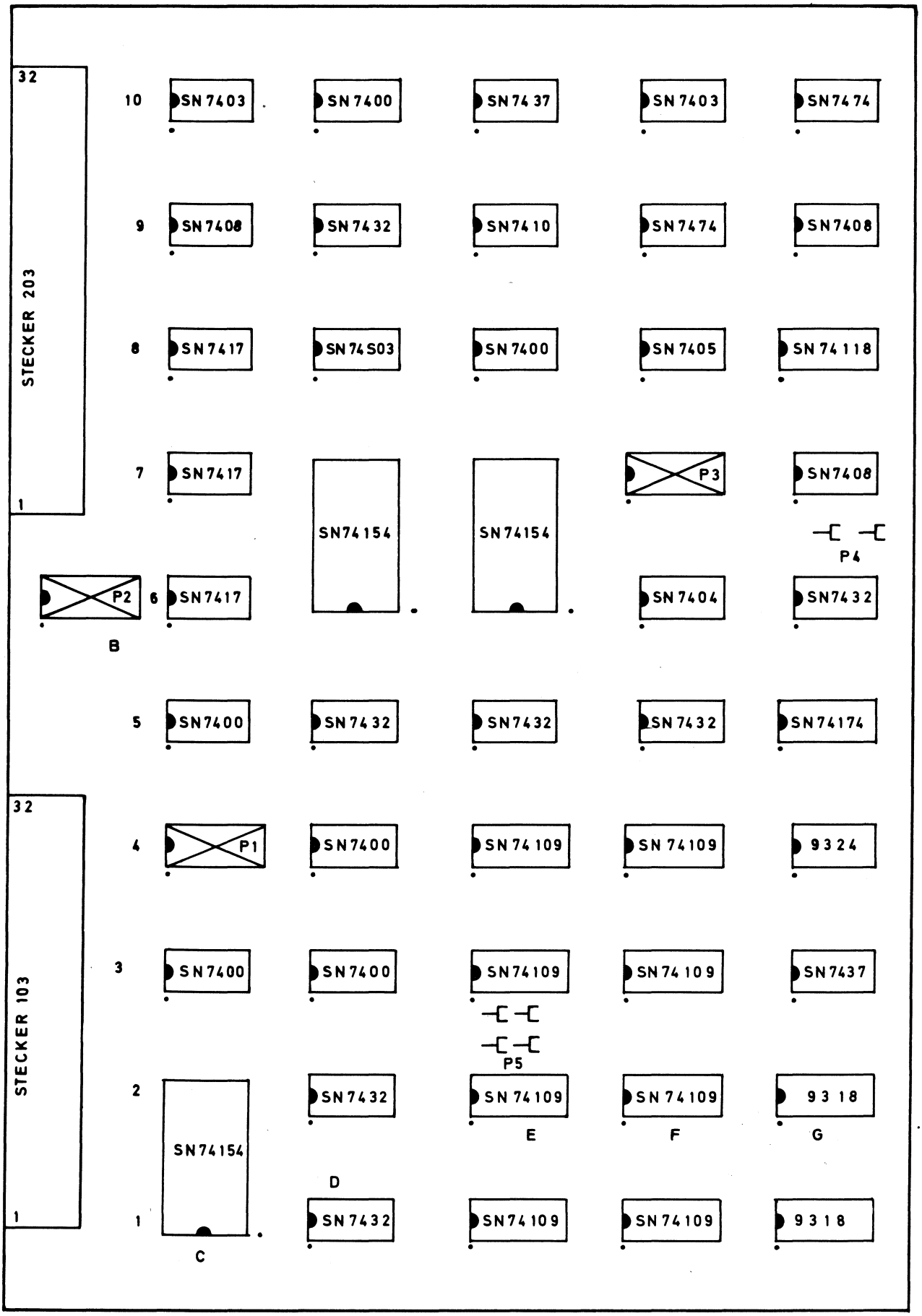
Adapterkabel KS 8 K / 16 K / J2	01.06.10

CPU St 2 Platz 204			Rangierleiterplatte			KS-Stecker 8k/16k/J1 U 621605100
a		c	a		b	
⊥	1	⊥	⊥	1	⊥	1 ⊥
⊥	2	⊥	+Z	2	+Z	2 +Z
RK-	3	FE-	+Z	3	+Z	3 -H
RP-	4	R- x	⊥	4	⊥	4 ⊥
MP-	5	OC- x	+H	5	+H	5 +H
DA-	6	PAOP- x	-H	6	-H	27 +Z
RWL/DCL	7	UF v PROG- x	AØØ-	7	⊥	28 +Z
MB-	8	+T x	AØ1-	8	⊥	29 +Z (MS2 KS2/SPE)
MS1	9	+T x	AØ2-	9	⊥	30 MS1 (+Z KS2/SPE)
A15-	10	frei x	AØ3-	10	⊥	31 BCL2 -
A14-	11	MS2 x	AØ4-	11	⊥	33 MB -
A13-	12	⊥	AØ5-	12	⊥	34 A13
A12-	13	⊥	AØ6-	13	⊥	35 BCL1 -
A11-	14	⊥	AØ7-	14	⊥	36 DA -
A10-	15	⊥	AØ8-	15	⊥	38 MP -
AØ9-	16	⊥	AØ9-	16	⊥	40 ⊥
AØ8-	17	⊥	A1Ø-	17	⊥	41 ⊥
AØ7-	18	⊥	A11-	18	⊥	42 +Z
AØ6-	19	⊥	A12-	19	⊥	43 -H
AØ5-	20	⊥	A13-	20	⊥	44 ⊥
AØ4-	21	⊥	A14-	21	MS2 x	45 +H
AØ3-	22	⊥	A15-	22	frei x	46 AØ8-
AØ2-	23	⊥	MS1	23	+T x	47 AØ7-
AØ1-	24	⊥	MB-	24	+T x	48 AØ6-
AØØ-	25	⊥	RWL/BCL-	25	UF v PROG*	49 A11-
-H	26	-H	DA-	26	PAOP- x	50 A1Ø-
+H	27	+H	MP-	27	OC- x	52 AØ9-
⊥	28	⊥	RP-	28	R- x	53 AØ3-
+Z	29	+Z	RK-	29	FE-	55 AØ4-
+Z	30	+Z	⊥	30	⊥	56 AØ5-
⊥	31	⊥				58 AØØ-
⊥	32	⊥	x ab CPU 621 602 E			59 AØ1-
						61 AØ2-
						62 A12-
						65 +Z
						79 RP-
						80 ⊥

73 MS2 für SPE
68/71 OC-
70 PAOP-
Parity intern

8k/16k/J1 ist ⊥ auf 51;54;57;60;66;
67; 37;
Beim KS2 in SPE wird MS2 Punkt 73 nach Punkt 29 verbunden.

Adapterkabel KS 8K/16K/J1	01.06.11



P1: Zuordnung CNP-Start

P2: Anzahl Byte/Level

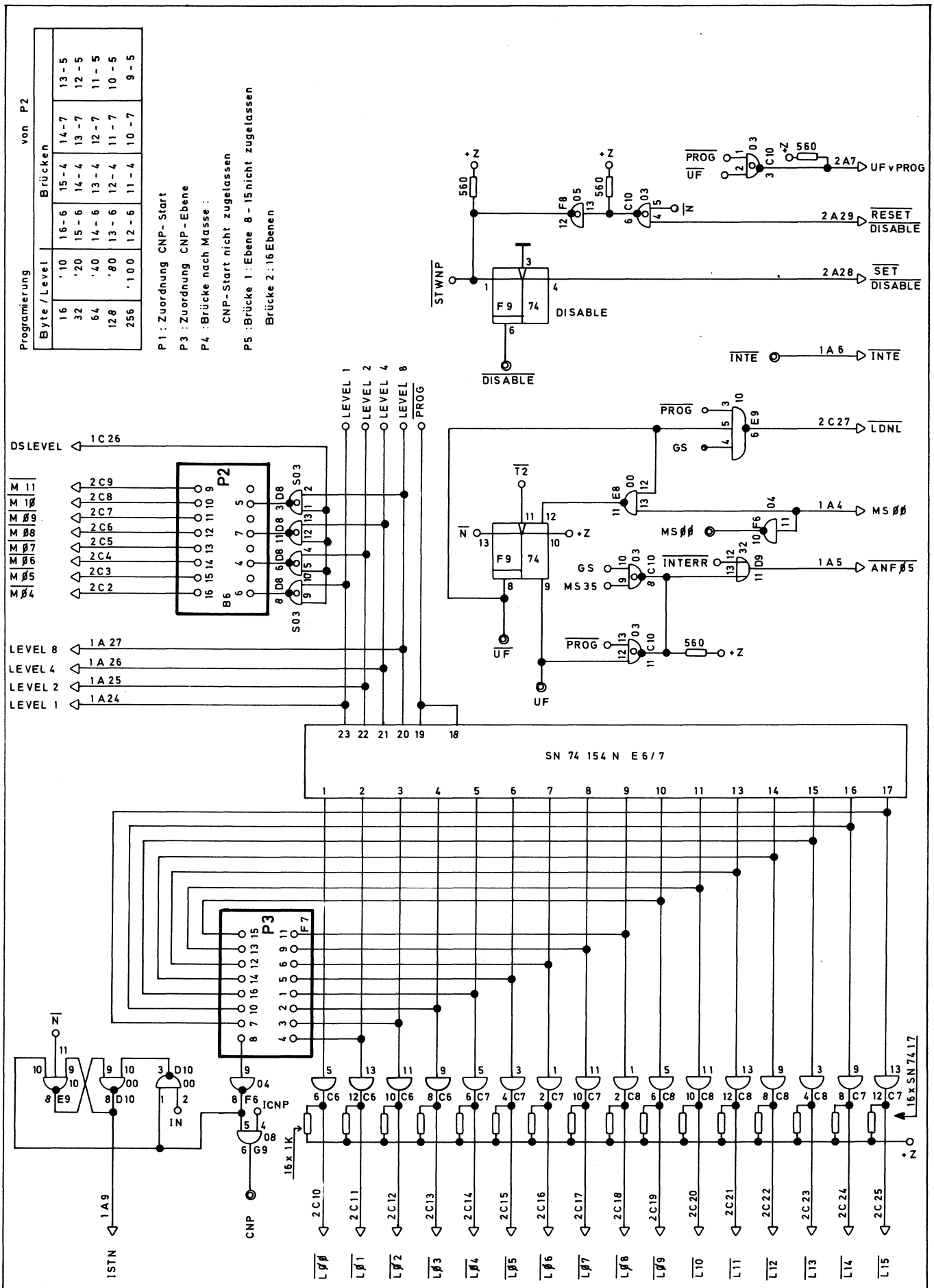
P3: Zuordnung CNP-Ebene

P4: Brücke: CNP-Start nicht zugelassen

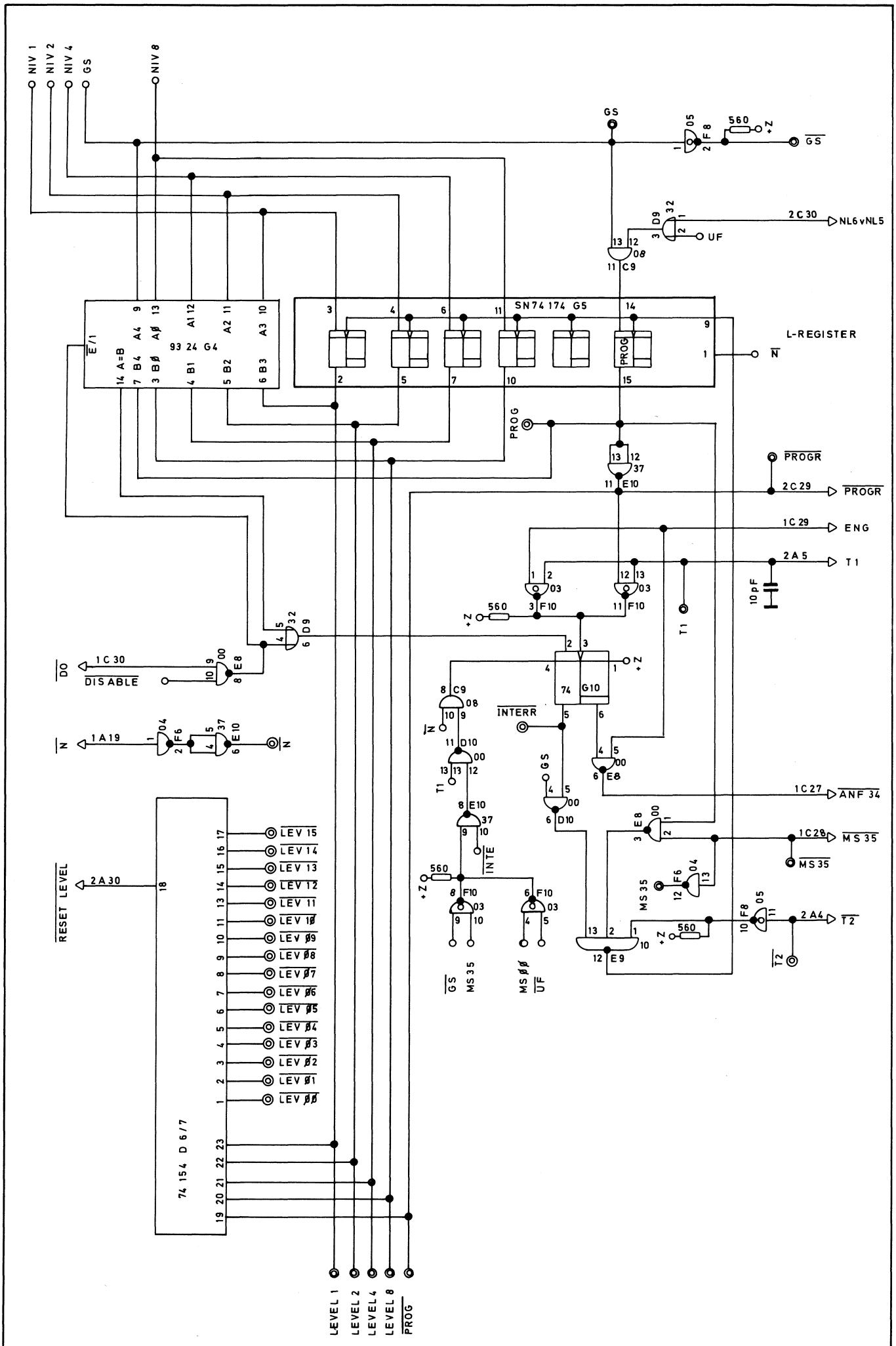
P5: -C-2-C 16 Ebenen

-C-1-C Ebene 8 - 15 nicht zugelassen

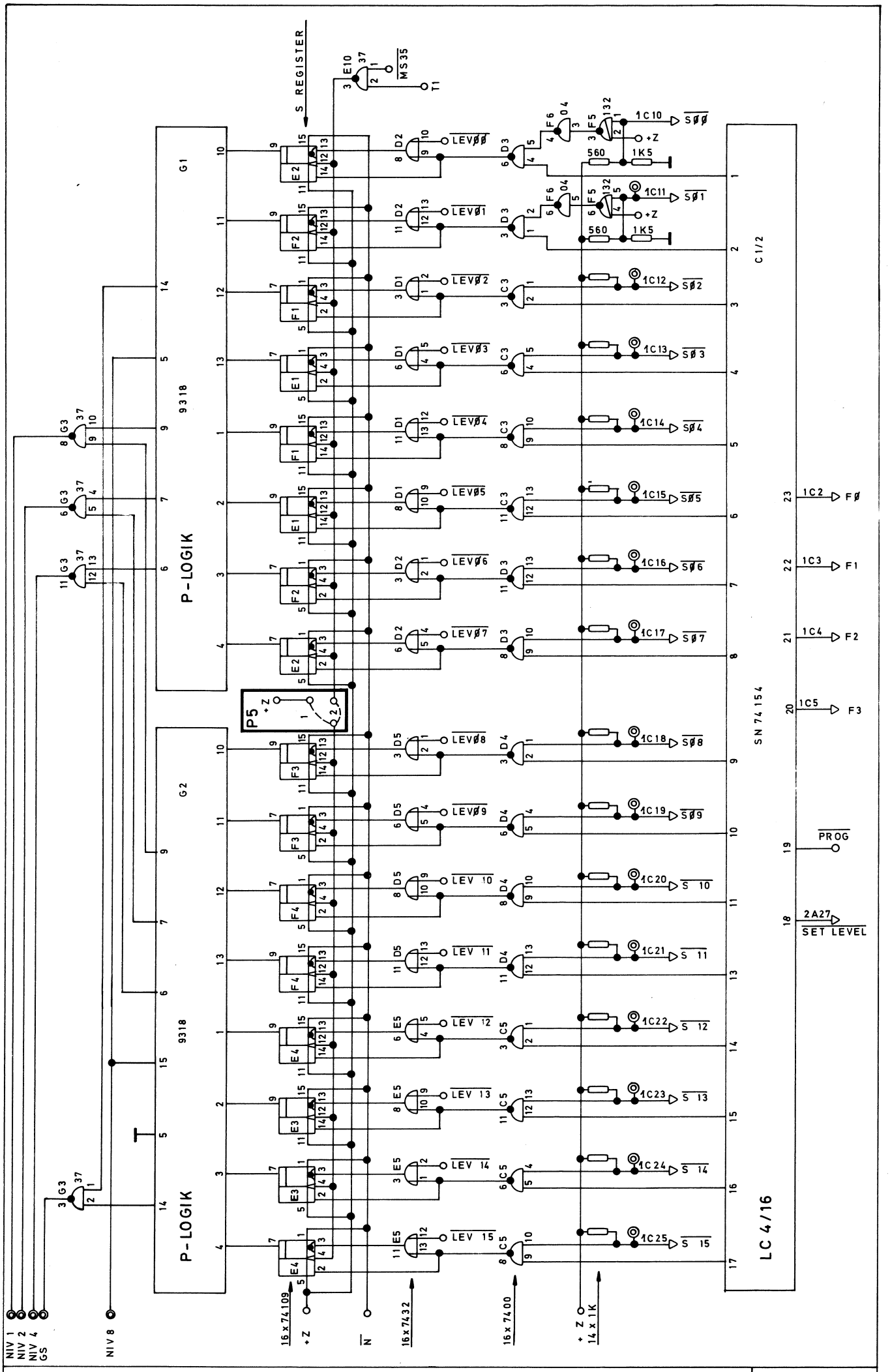
621 643 G,H1 Level Logik	01.07.01



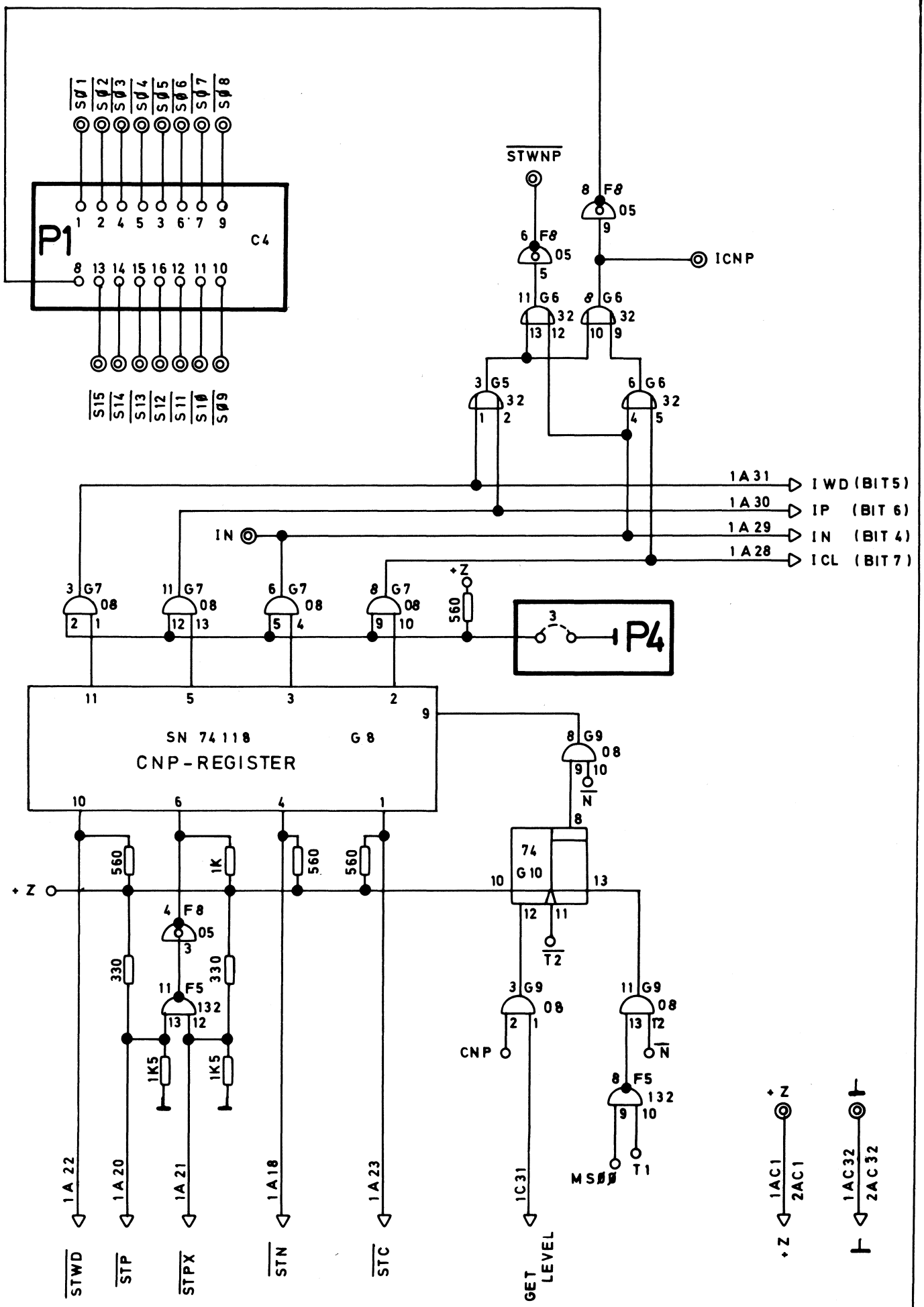
621 643 G,H1 Level - Logik 01.07.02



621 643 G,H1	Level-Logik	01.07.03



621 643 G,H1 Level-Logik 01.07.04



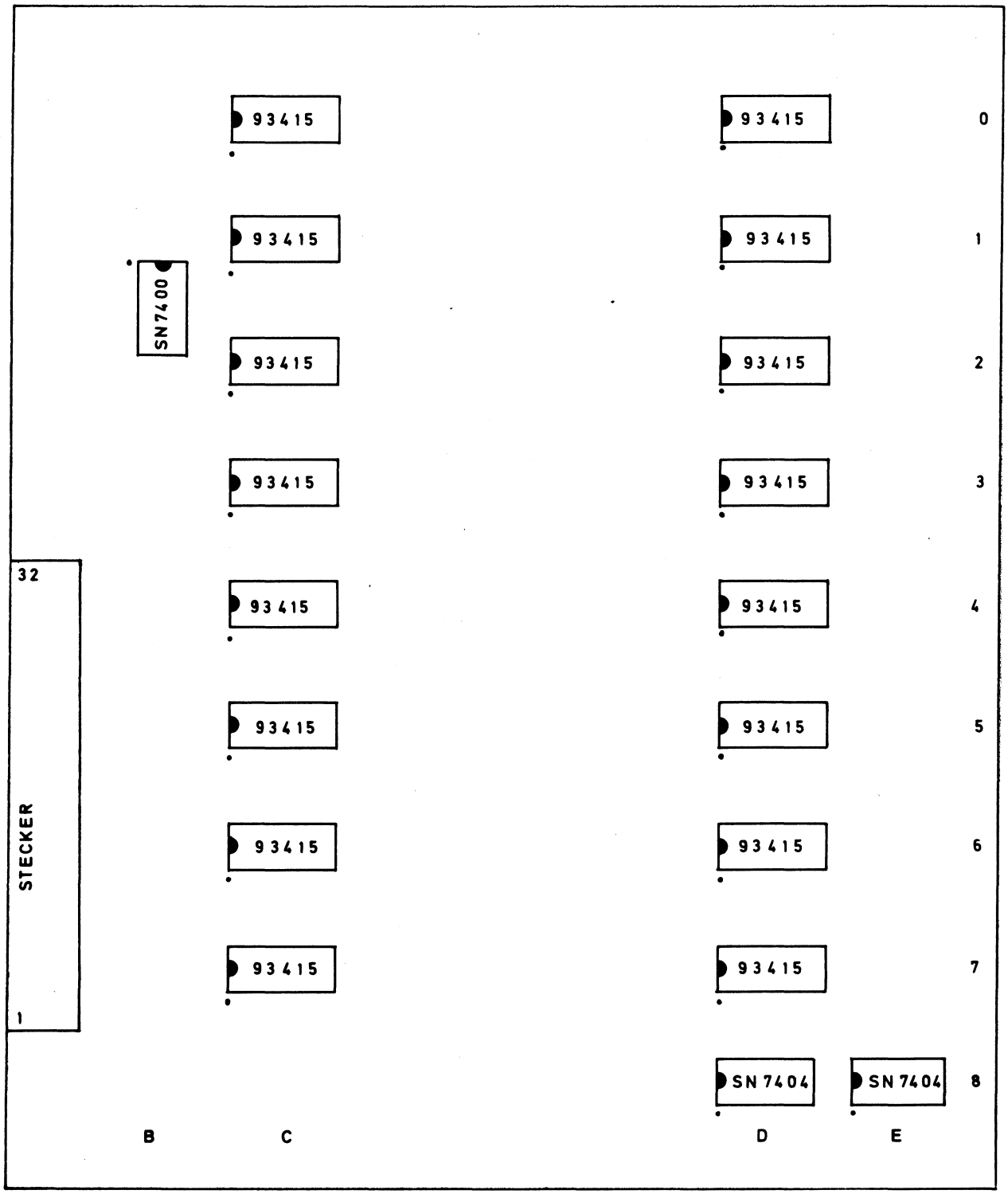
621 643 G,H1	Level-Logik	01.07.05

1A		1C
+Z	1	+Z
	2	FØ
	3	F1
MSØØ–	4	F2
ANPØ5–	5	F3
INTE –	6	
	7	
	8	
ISTN	9	
	10	SØØ –
	11	SØ1 –
	12	SØ2 –
	13	SØ3 –
	14	SØ4 –
	15	SØ5 –
	16	SØ6 –
	17	SØ7 –
STN–	18	SØ8 –
N	19	SØ9 –
STP–	20	S1Ø –
STPX–	21	S11 –
STWD–	22	S12 –
STC –	23	S13 –
LEVEL1	24	S14 –
LEVEL2	25	S15 –
LEVEL4	26	DSLEVEL
LEVEL8	27	ANF34 –
ICL	28	MS35 –
IN	29	ENG
IP	30	DO –
IWD	31	GETLEVEL
ØV	32	ØV

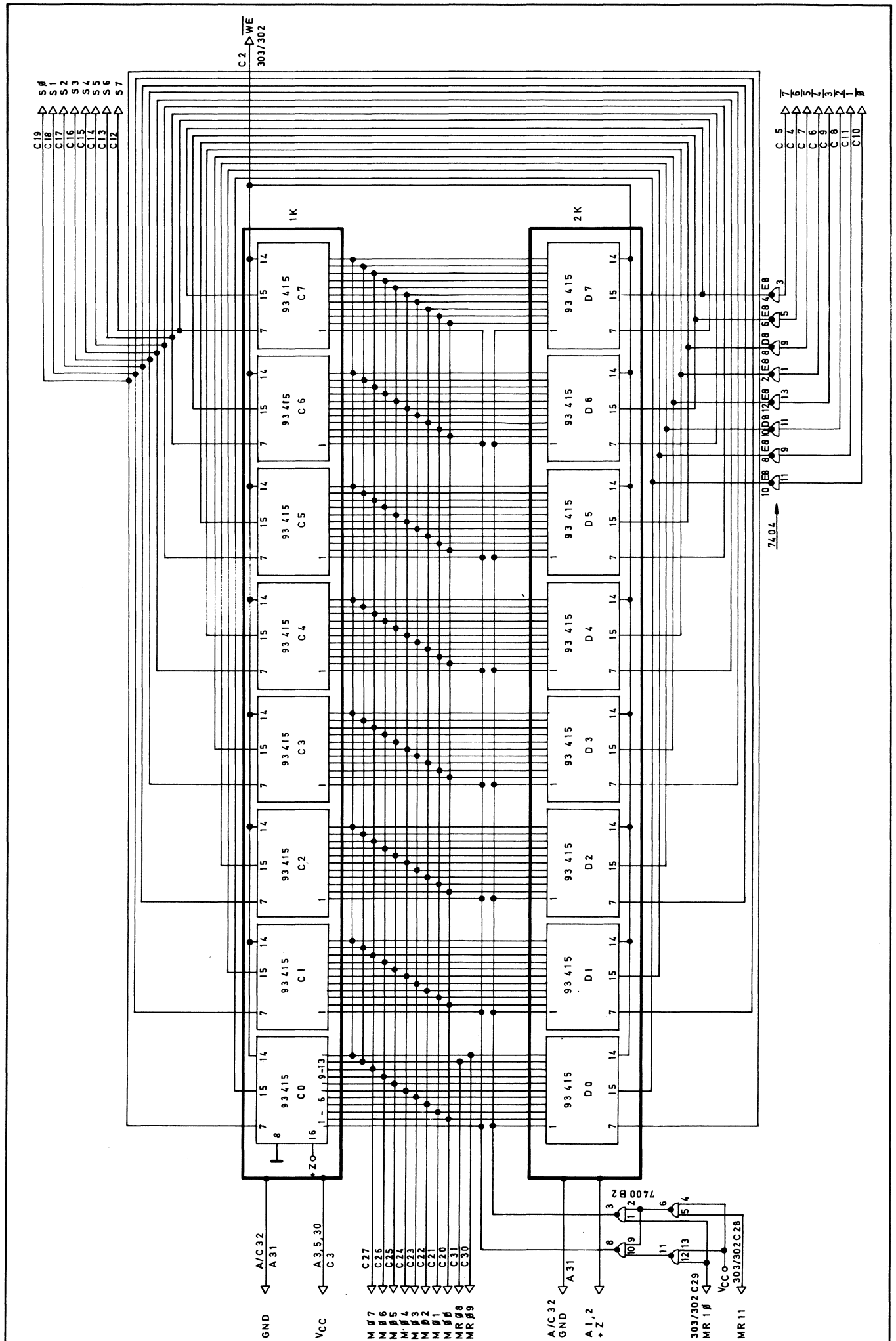
1Ø3

2A		2C
+Z	1	+Z
	2	MØ4 –
T2B	3	MØ5 –
T2–	4	MØ6 –
T1	5	MØ7 –
	6	MØ8 –
UF v PROG	7	MØ9 –
	8	M1Ø –
	9	M11 –
	10	LØØ –
	11	LØ1 –
	12	LØ2 –
	13	LØ3 –
	14	LØ4 –
	15	LØ5 –
	16	LØ6 –
	17	LØ7 –
	18	LØ8 –
	19	LØ9 –
	20	L1Ø –
	21	L11 –
	22	L12 –
	23	L13 –
	24	L14 –
	25	L15 –
	26	
SETLEVEL	27	LDNL-
SETDISABLE	28	
RESDISABLE	29	PROG-
RESETLEVEL	30	NL6
ØV	31	ØV
ØV	32	ØV

2Ø3

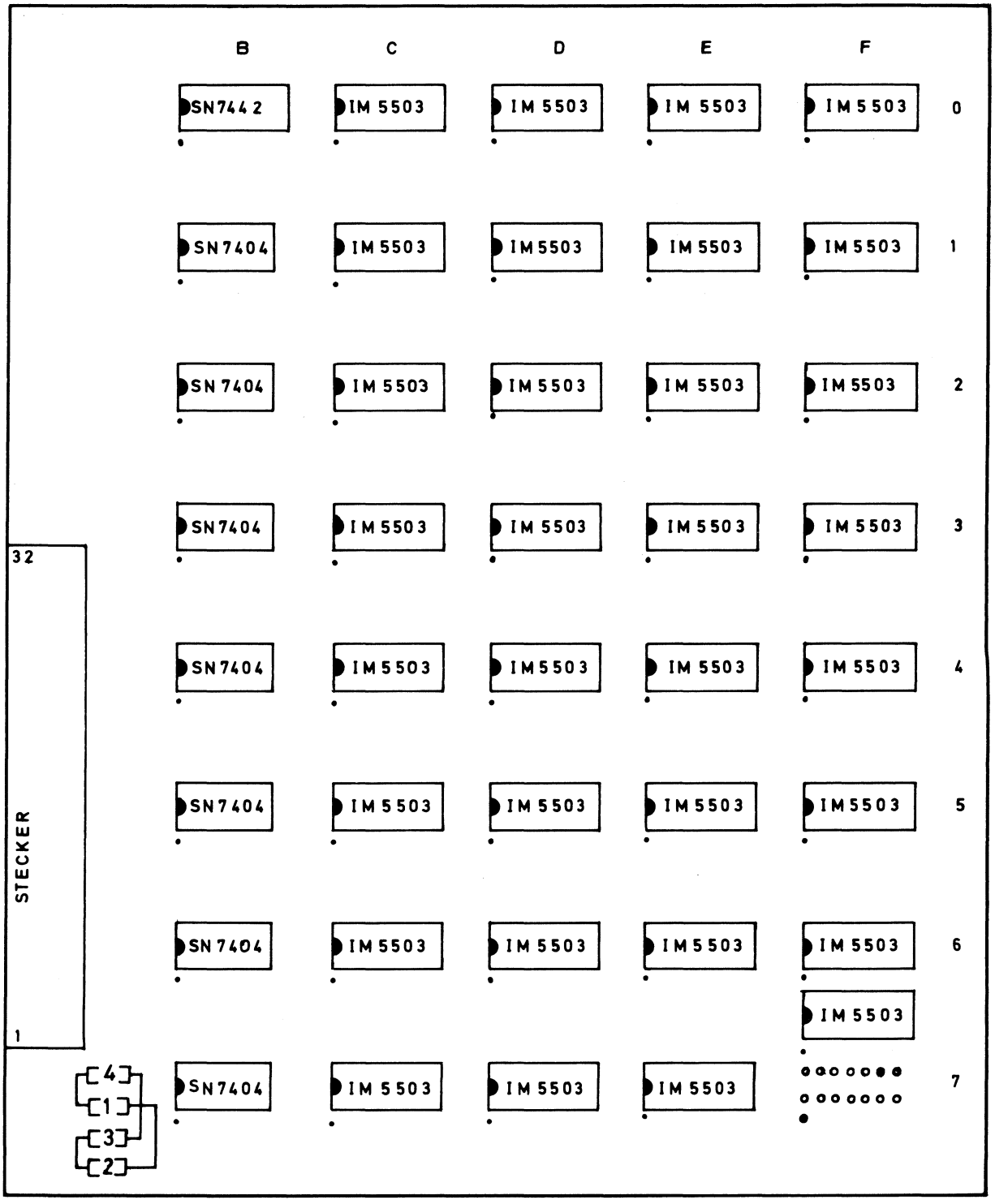


621 626 C	RAM-Baustein	01.08.01



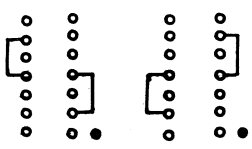
621 626 C RAM - Baustein 2 K

01.08.02



Adresse 000.....0FF [B4] } Spannungsversorgung
100.....1FF [B1] } von jeweils 1/2K über $+Z_B$

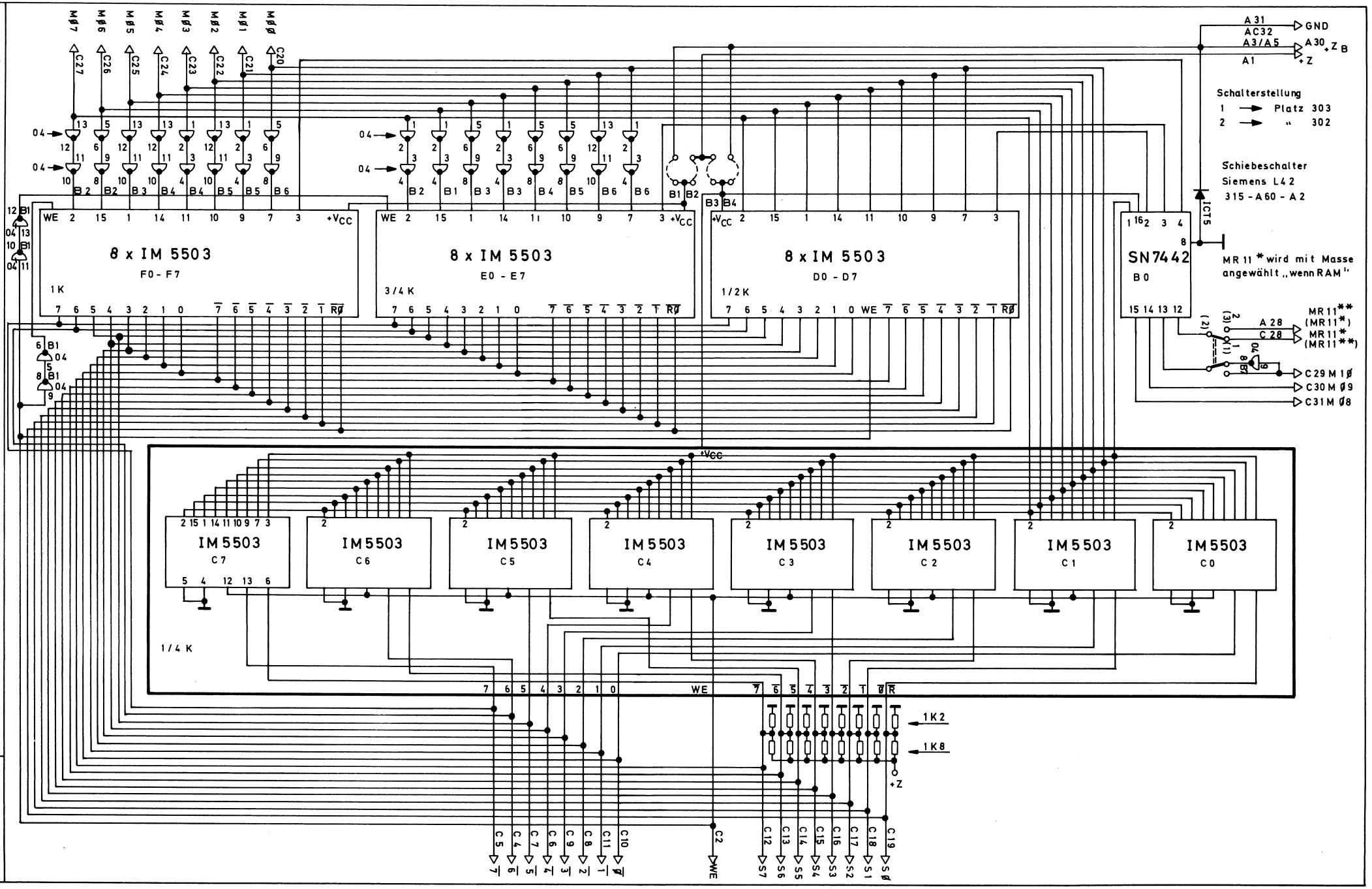
000.....0FF [B3] } Spannungsversorgung
100.....1FF [B2] } von jeweils 1/2K über $+Z$



Platz 303 Platz 302

621 639 D RAM Baustein 1K

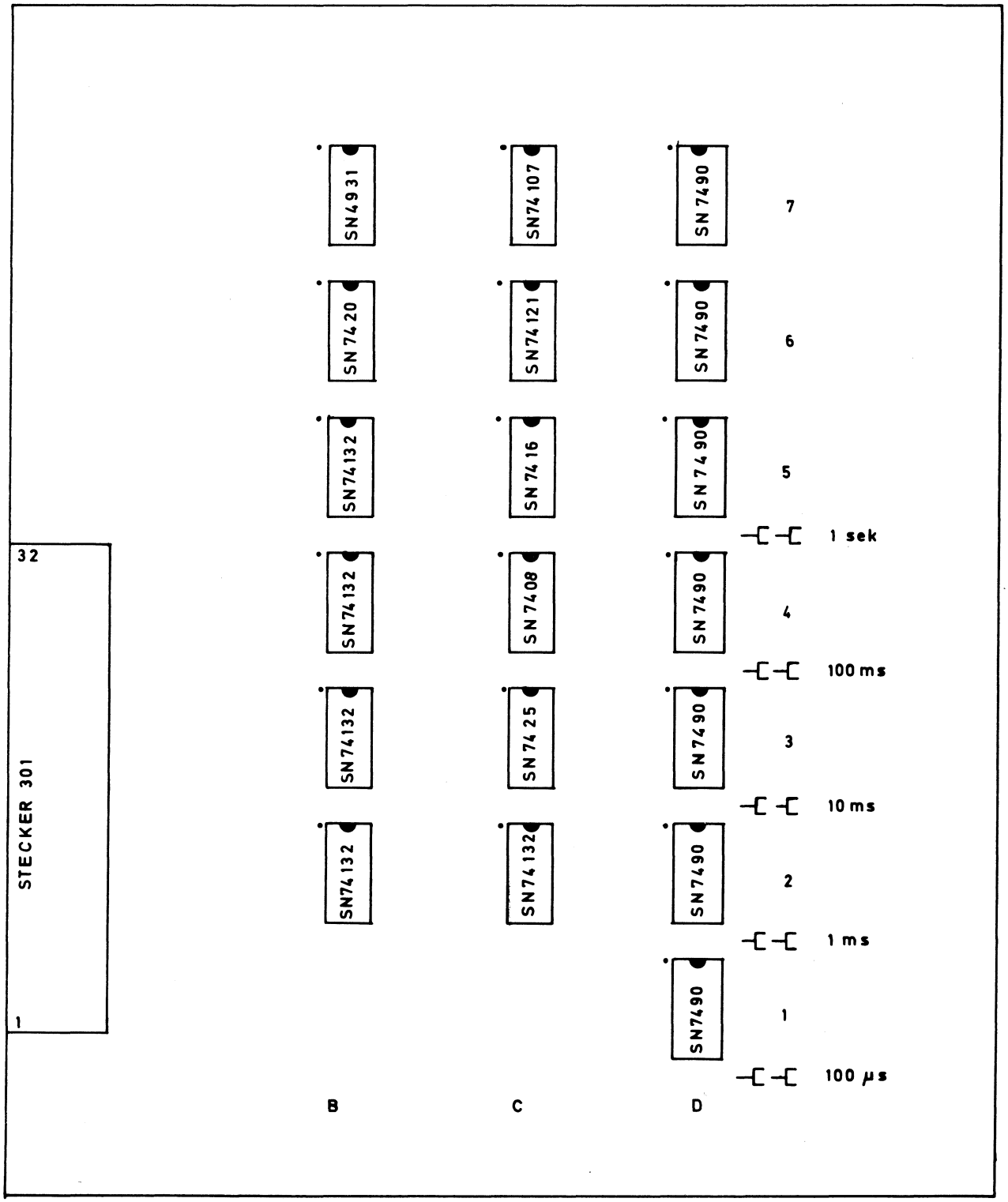
01.08.04

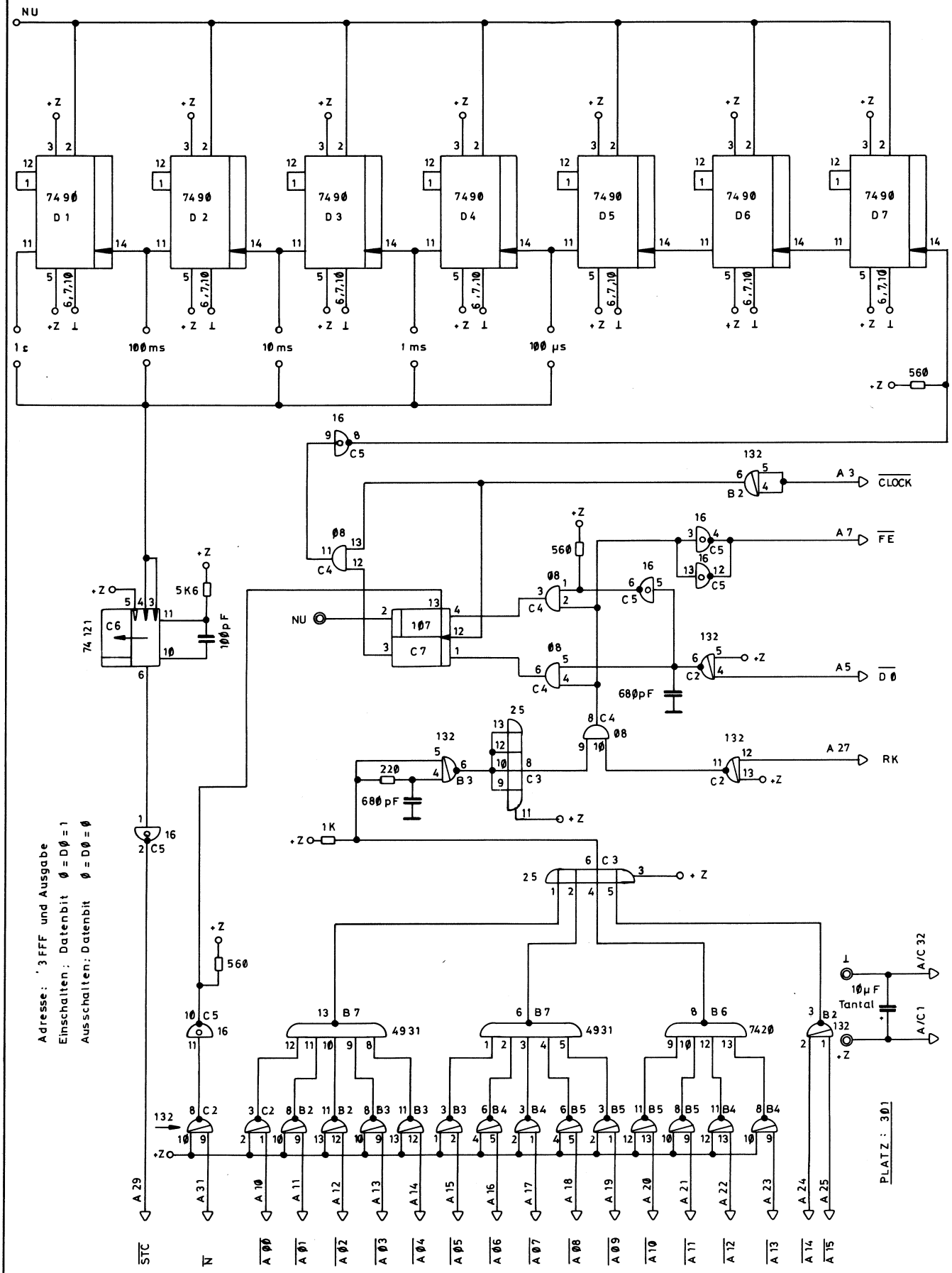


302 / 303

Leiterseite **Bauelentseite**

A		C
+Z	1	
+Z	2	WE-
+ZB	3	UWACH
CLOCK-	4	6-
+ZB	5	7-
	6	4-
+H	7	5-
	8	2-
-H	9	3-
	10	Ø-
$\overline{T2}$	11	1-
	12	S7
	13	S6
	14	S5
	15	S4
	16	S3
	17	S2
	18	S1
	19	SØ
	20	MØØ
	21	MØ1
	22	MØ2
	23	MØ3
	24	MØ4
	25	MØ5
	26	MØ6
	27	MØ7
MR11 **(*)	28	MR11 *(**)
	29	M1Ø
+ZB	30	MØ9
ØV	31	MØ8
ØV (St +ZB)	32	ØV


STECKER 301
32
1
SN4931
SN74107
SN7490
7
SN7420
SN74121
SN7490
6
SN74132
SN7416
SN7490
5
1 sek
SN74132
SN7408
SN7490
4
100 ms
SN74132
SN7425
SN7490
3
10 ms
SN74132
SN74132
SN7490
2
1 ms
SN7490
1
100 µs
B
C
D



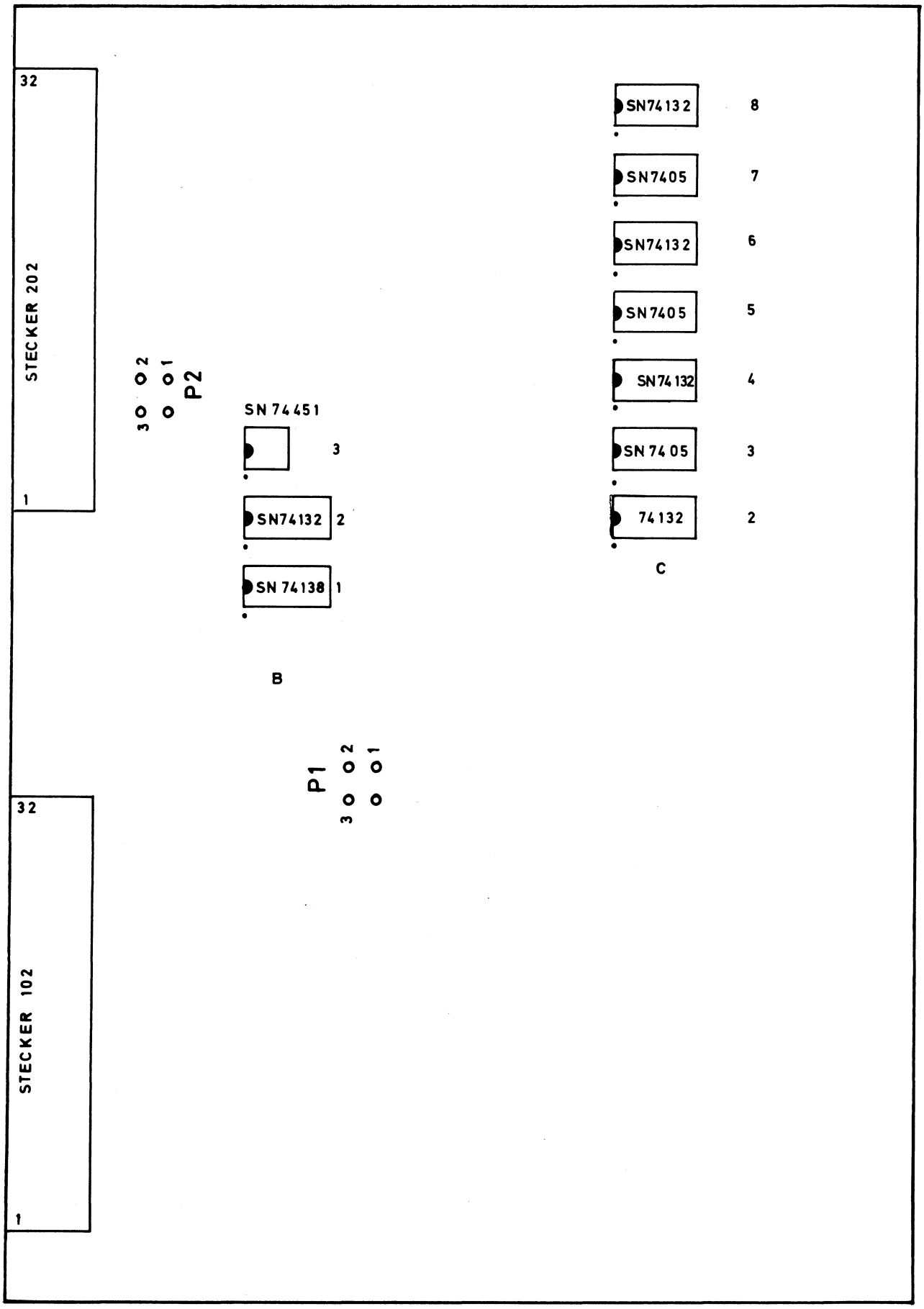
621610 D Rechner Uhr

01.09.02

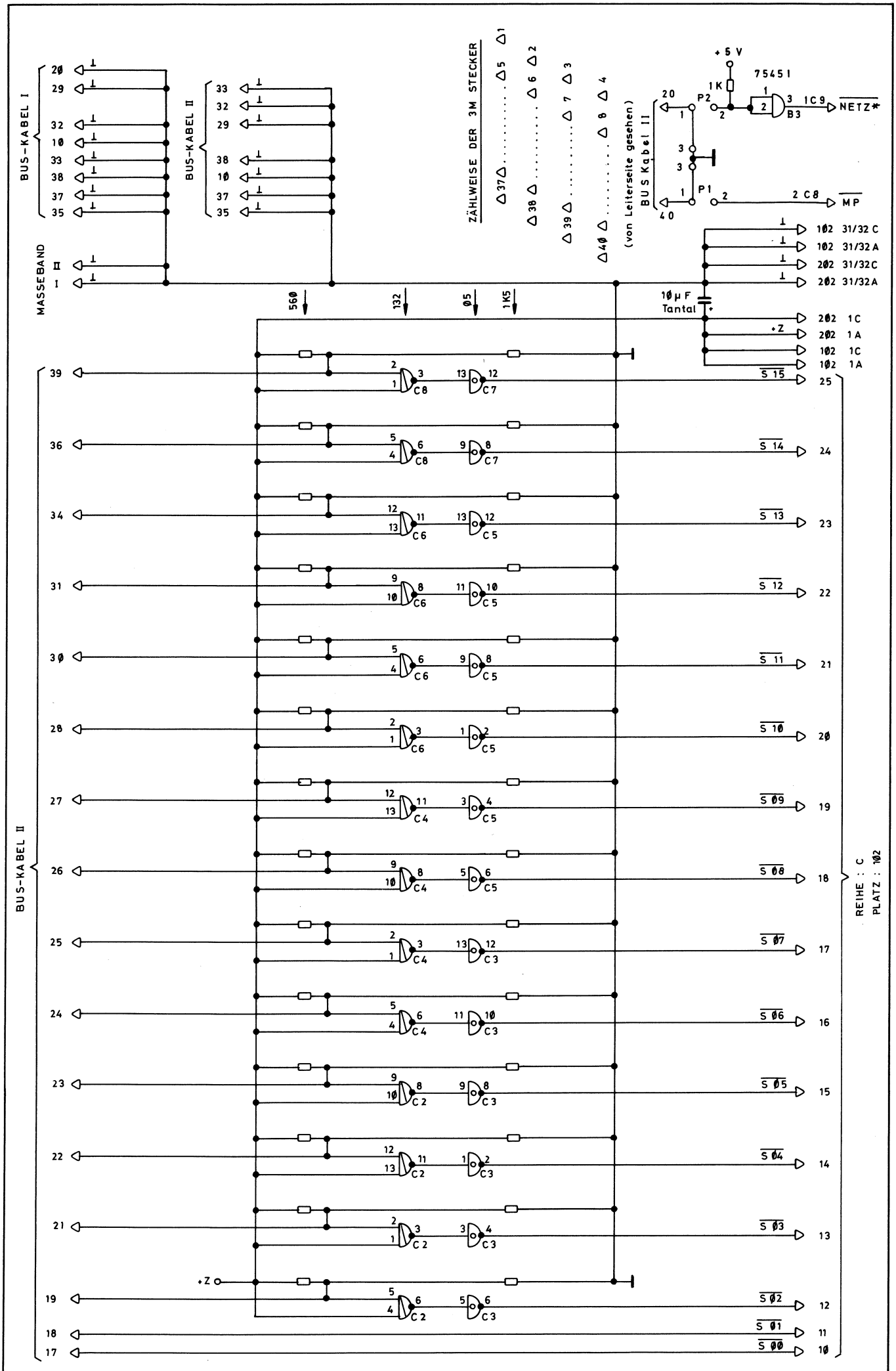
301

Leiterseite Bauelementseite

A			C	
+Z		1	+Z	
		2		
CLOCK-		3		
		4		
DØ-		5		
		6		
FE-		7		
		8		
		9		
AØØ-		10		
AØ1-		11		
AØ2-		12		
AØ3-		13		
AØ4-		14		
AØ5-		15		
AØ6-		16		
AØ7-		17		
AØ8-		18		
AØ9-		19		
A1Ø-		20		
A11-		21		
A12-		22		
A13-		23		
A14-		24		
A15-		25		
		26		
RK		27		
		28		
STC-		29		
		30		
N-		31		
ØV		32	ØV	

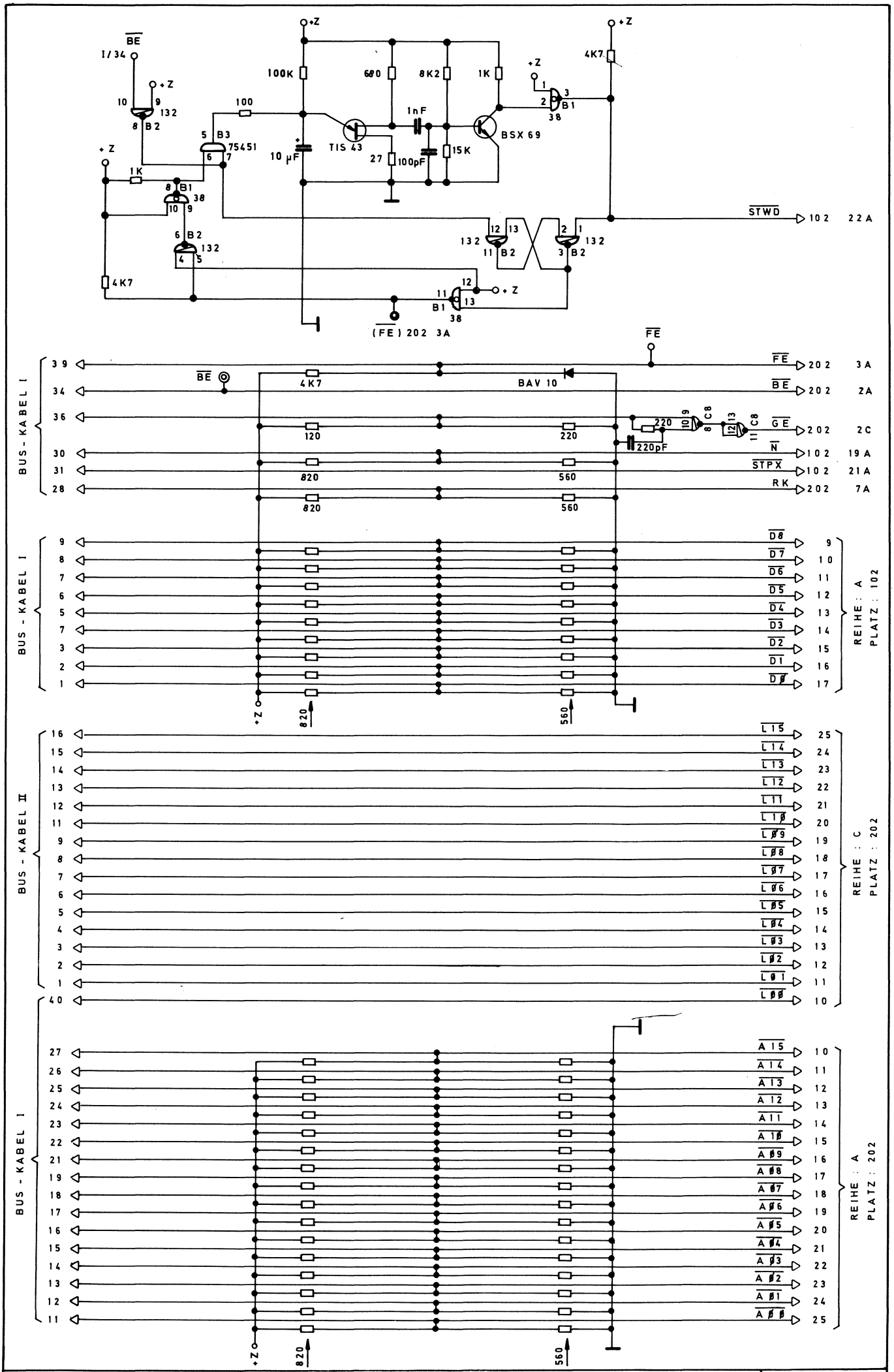


621 611 1 M	BUS-Anschlußkarte	01.10.01

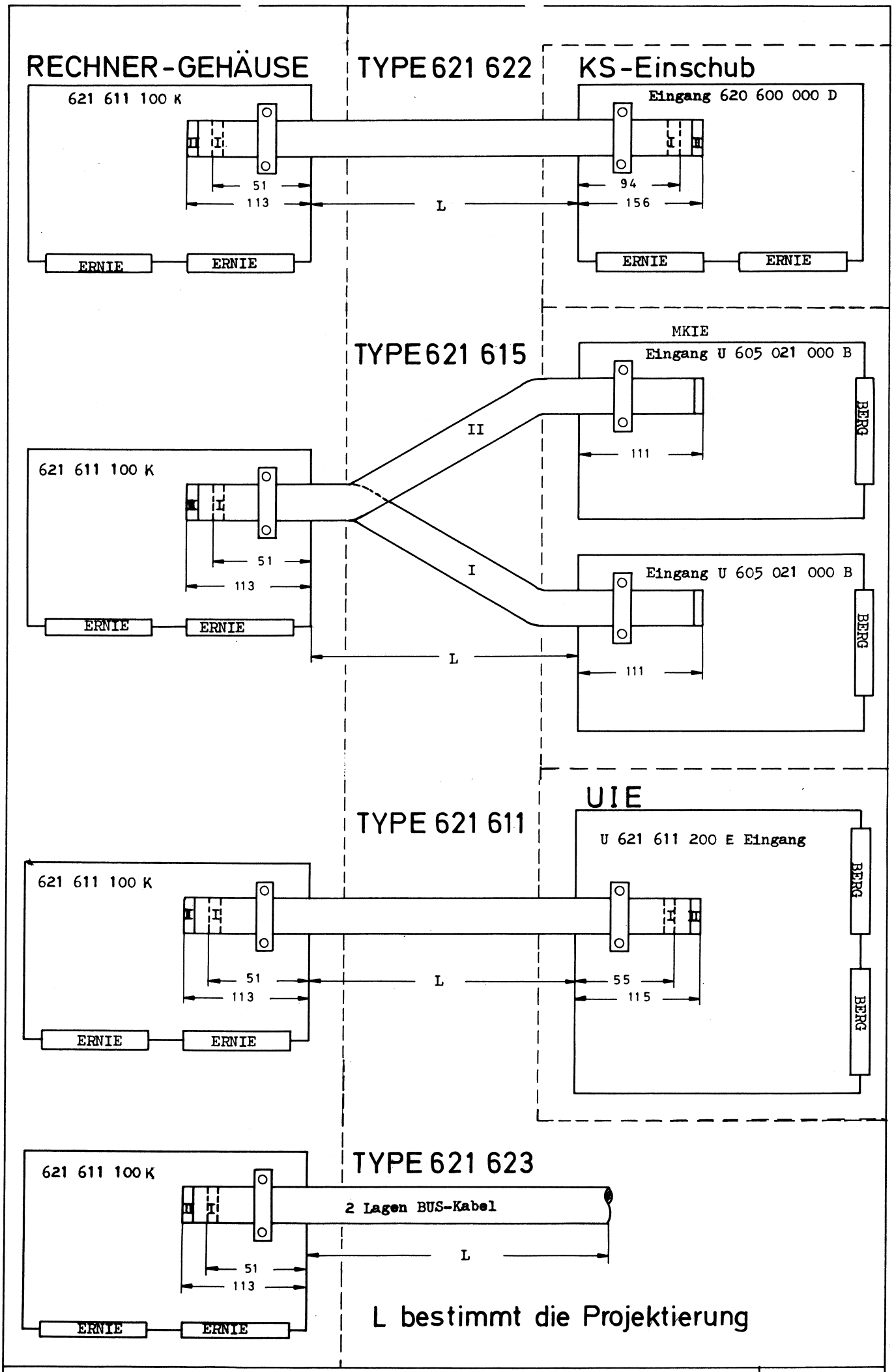


6216111M BUS-Anschlußkarte

01.10.02



621 6111 M	BUS-Anschlußkarte	01.10.03



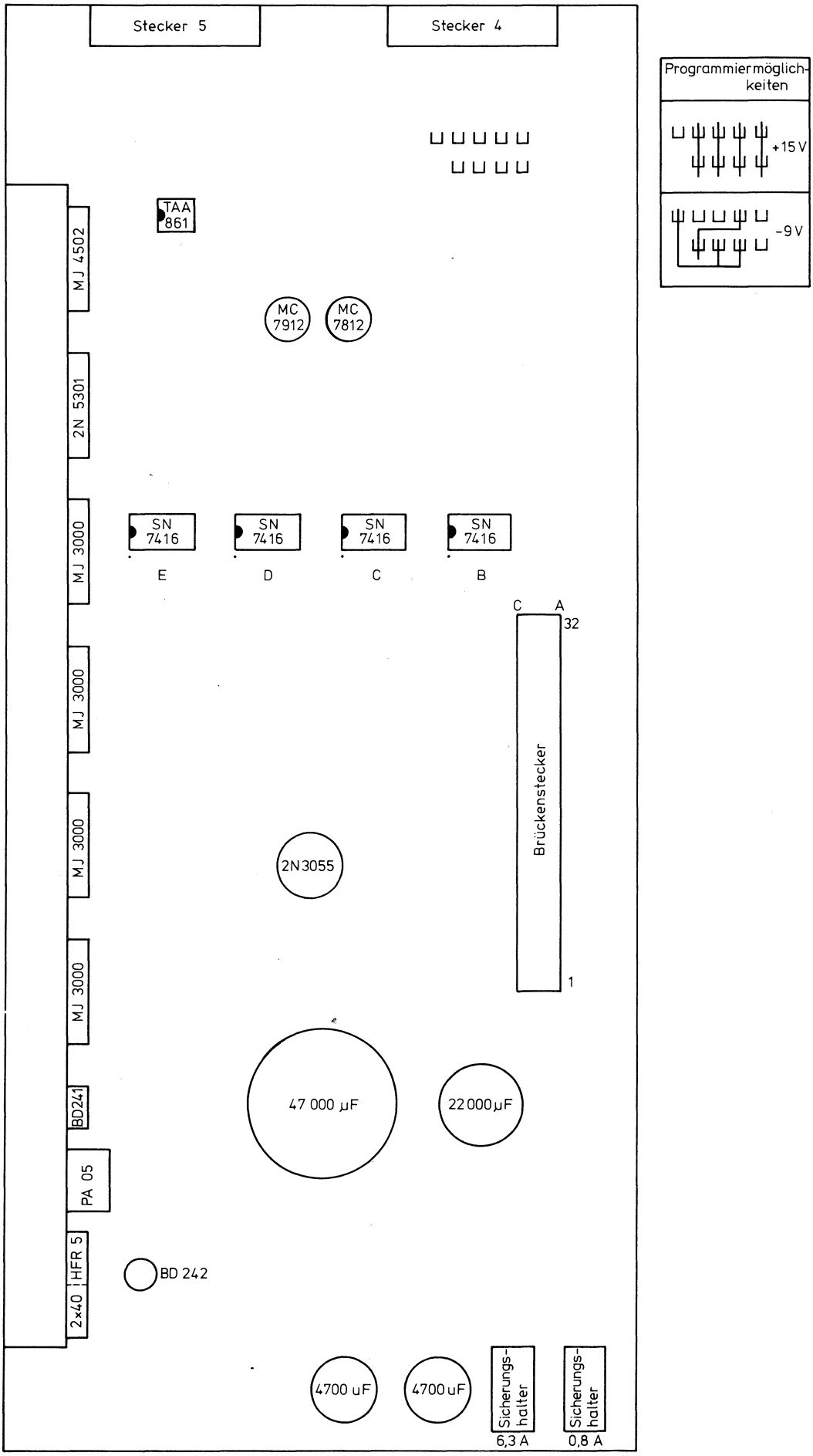
621611M Kombinationsmöglichkeit BUS-Anschlußkarte | 01.10.04

102

Leiterseite 1A			Bauelementseite 1C	
+Z		1	+Z	
		2		
		3		
		4		
		5		
		6		
		7		
		8		
D8-		9	NETZ *	
D7-		10	SØØ-	
D6-		11	SØ1-	
D5-		12	SØ2-	
D4-		13	SØ3-	
D3-		14	SØ4-	
D2-		15	SØ5-	
D1-		16	SØ6-	
DØ-		17	SØ7-	
		18	SØ8-	
N-		19	SØ9-	
		20	S1Ø-	
STPX-		21	S11-	
STWD-		22	S12-	
		23	S13-	
LEVEL 1		24	S14-	
LEVEL 2		25	S15-	
LEVEL 4		26		
LEVEL 8		27		
		28		
		29		
		30		
ØV		31	ØV	
ØV		32	ØV	

202

Leiterseite 2A			Bauelementseite 2C	
+Z		1	+Z	
BE-		2	GE-	
FE-		3		
		4		
		5		
		6		
RK		7		
		8	$\overline{MP}$	
		9		
A15-		10	LØØ-	
A14-		11	LØ1-	
A13-		12	LØ2-	
A12-		13	LØ3-	
A11-		14	LØ4-	
A1Ø-		15	LØ5-	
AØ9-		16	LØ6-	
AØ8-		17	LØ7-	
AØ7-		18	LØ8-	
AØ6-		19	LØ9-	
AØ5-		20	L1Ø-	
AØ4-		21	L11-	
AØ3-		22	L12-	
AØ2-		23	L13-	
AØ1-		24	L14-	
AØØ-		25	L15-	
		26		
		27		
		28		
PROGR-		29		
		30		
ØV		31	ØV	
ØV		32	ØV	



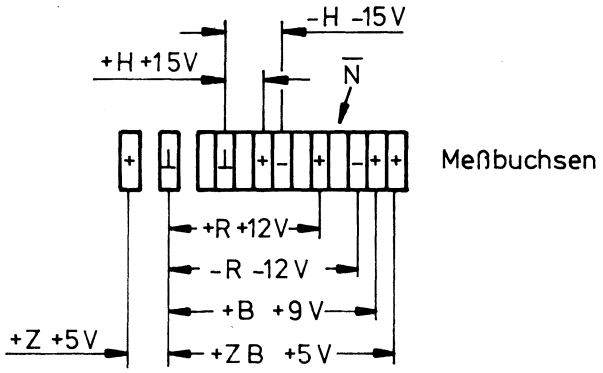
621 7 STROMVERSORGUNG

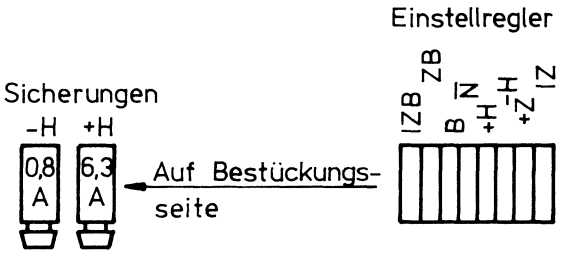
01. 11. 01

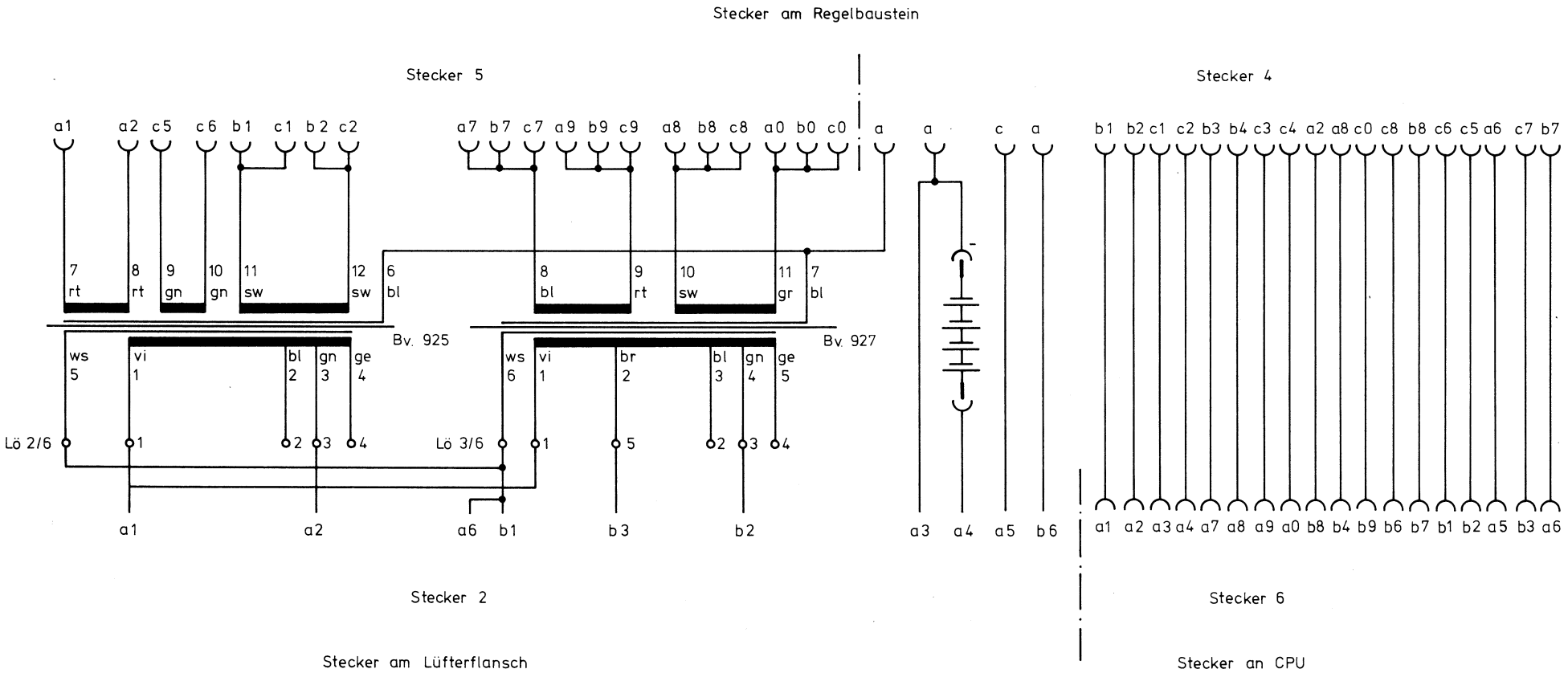
Bezeichng.	U / V	U gegen	I nenn / A	U Brumm / mV_{ss}	Ansprechschwelle Übersp. Schutz	Poti	Regel-verstärker f. Platz	Trafo	Bemerkung
+ Z	+500	⊥ Z	20	5	6,6 - 7,0	+Z	B	2	Strombegrenzung mit "IZ" Poti auf 21,5-22,5A einstellen
+ R	+12	⊥ Z	0,05	50	-	-		1	-
-R	-12	⊥ Z	0,05	50	-	-		1	-
+B	+9,∞	⊥ Z	2	50	-	B	E	2	-
$+Z_B$	+5	⊥ Z	6	5	6,8 - 7,2	ZB		2	Strombegrenzung m. "IZB" Poti auf 7,5-8A einst.
+H	+15,∞	⊥ H	5,5	20	17,2-18,0	+H	D	1	-
-H	-15,∞	⊥ H	0,75	20	17,2-18,0	-H	C	1	

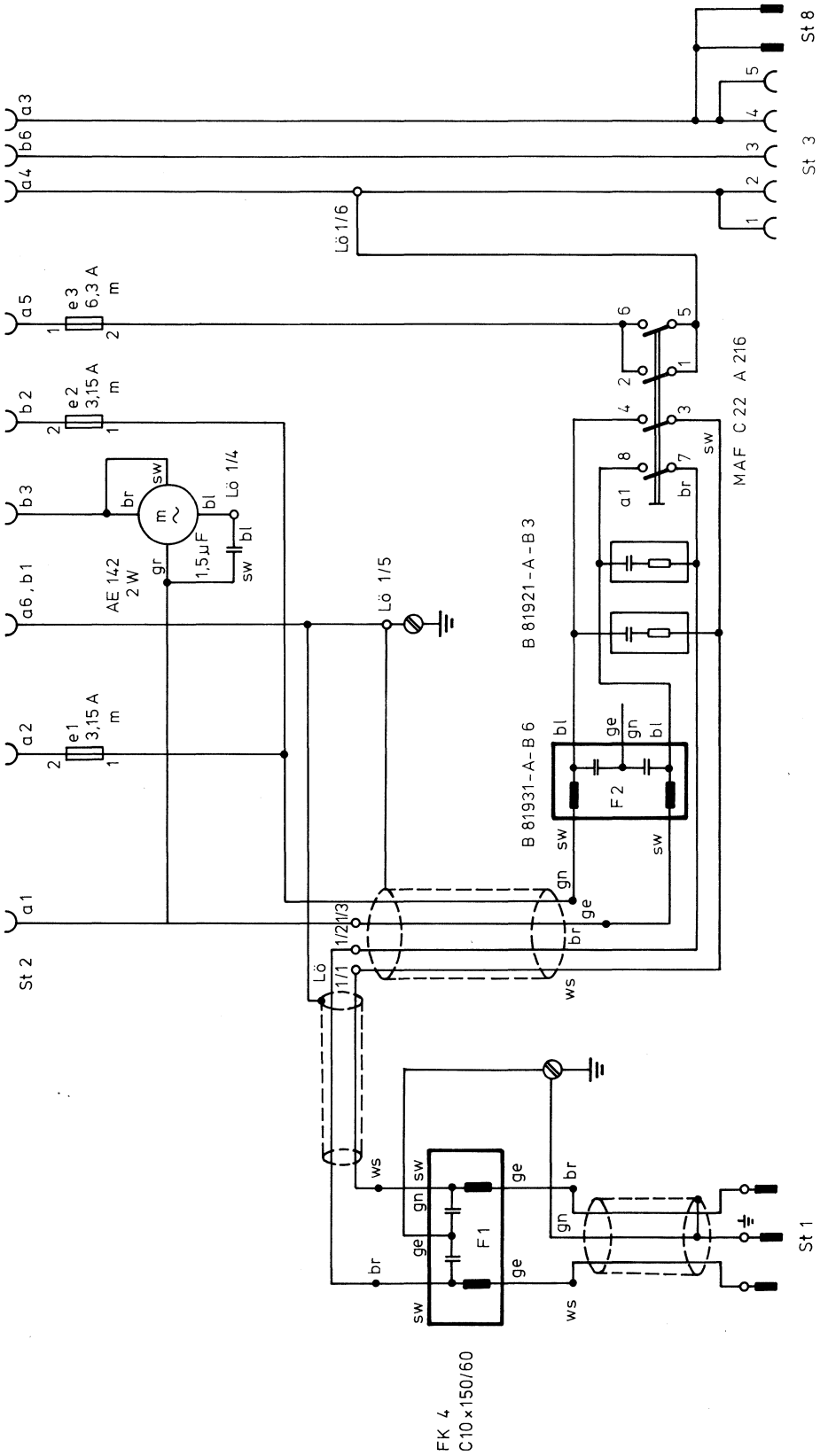
Mittels Poti "N" wird $\overline{NETZ}$ bei 198 V Netzspannung eingestellt

⊥ ⊓ Bei einer Netzspannung 198 V muß der Ausgang $\overline{NETZ}$ ⊥-Impulse anzeigen.



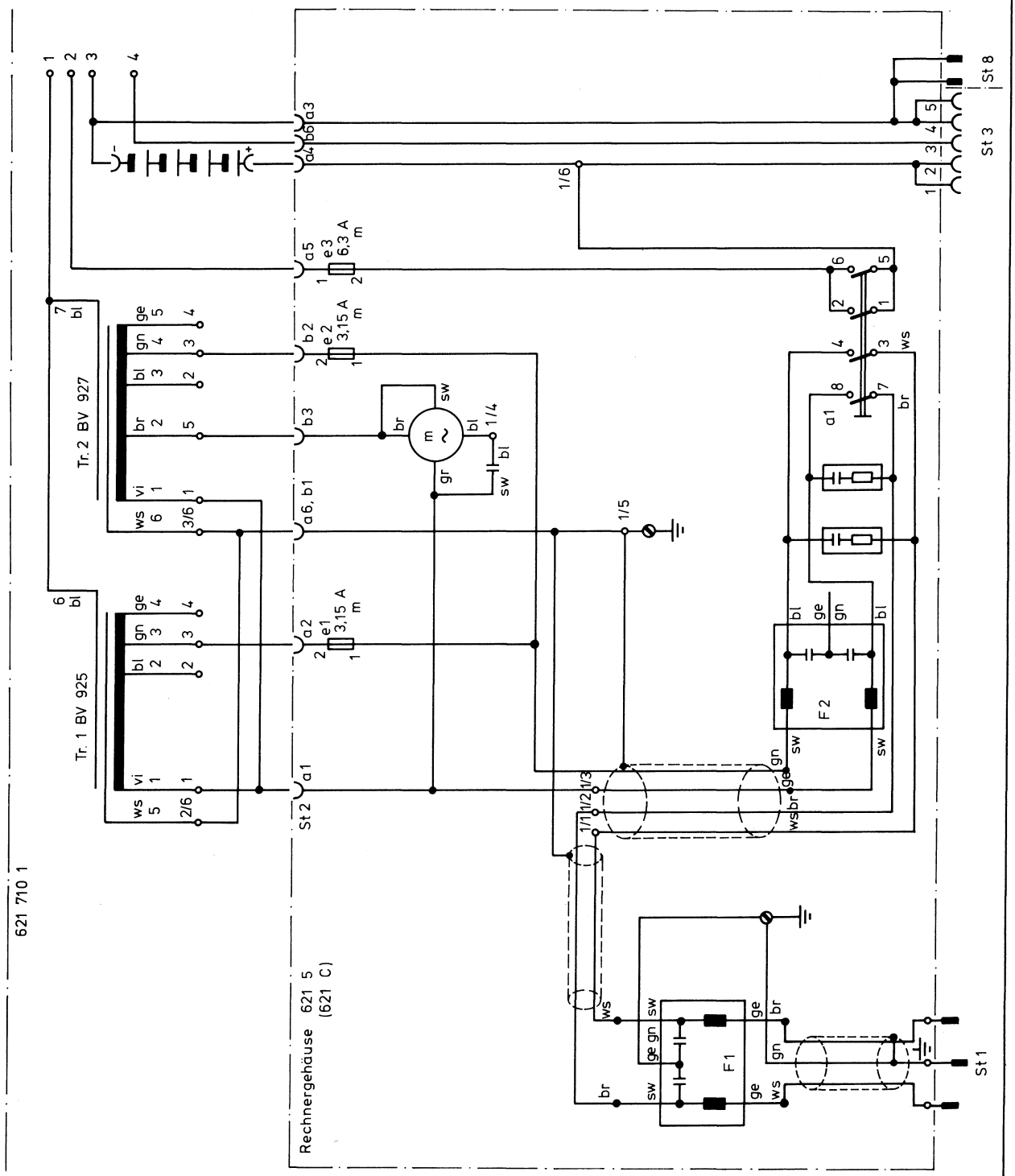


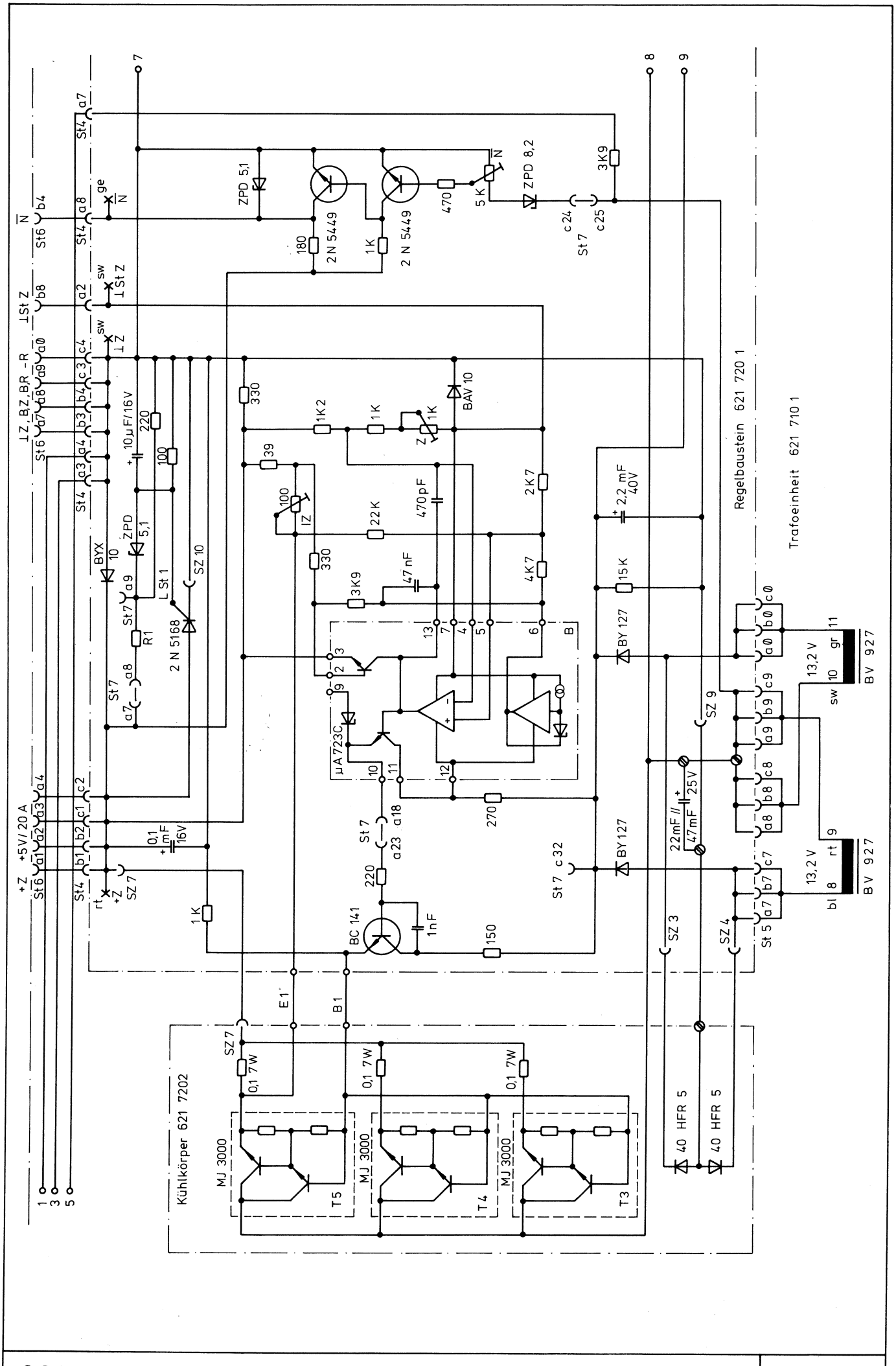

Stecker am Regelbaustein
Stecker 5
Stecker 4
a1 a2 c5 c6 b1 c1 b2 c2
a7 b7 c7 a9 b9 c9 a8 b8 c8 a0 b0 c0
a a c a
b1 b2 c1 c2 b3 b4 c3 c4 a2 a8 c0 c8 b8 c6 c5 a6 c7 b7
7 rt
8 rt
9 gn
10 gn
11 sw
12 sw
6 bl
8 bl
9 rt
10 sw
11 gr
7 bl
Bv. 925
Bv. 927
ws 5
vi 1
bl 2
gn 3
ge 4
ws 6
vi 1
br 2
bl 3
gn 4
ge 5
Lö 2/6
Lö 3/6
a1
a2
a6 b1
b3
b2
a3 a4 a5 b6
a1 a2 a3 a4 a7 a8 a9 a0 b8 b4 b9 b6 b7 b1 b2 a5 b3 a6
Stecker 2
Stecker 6
Stecker am Lüfterflansch
Stecker an CPU



621 5 RECHNERGEHÄUSE VERDRAHTUNG

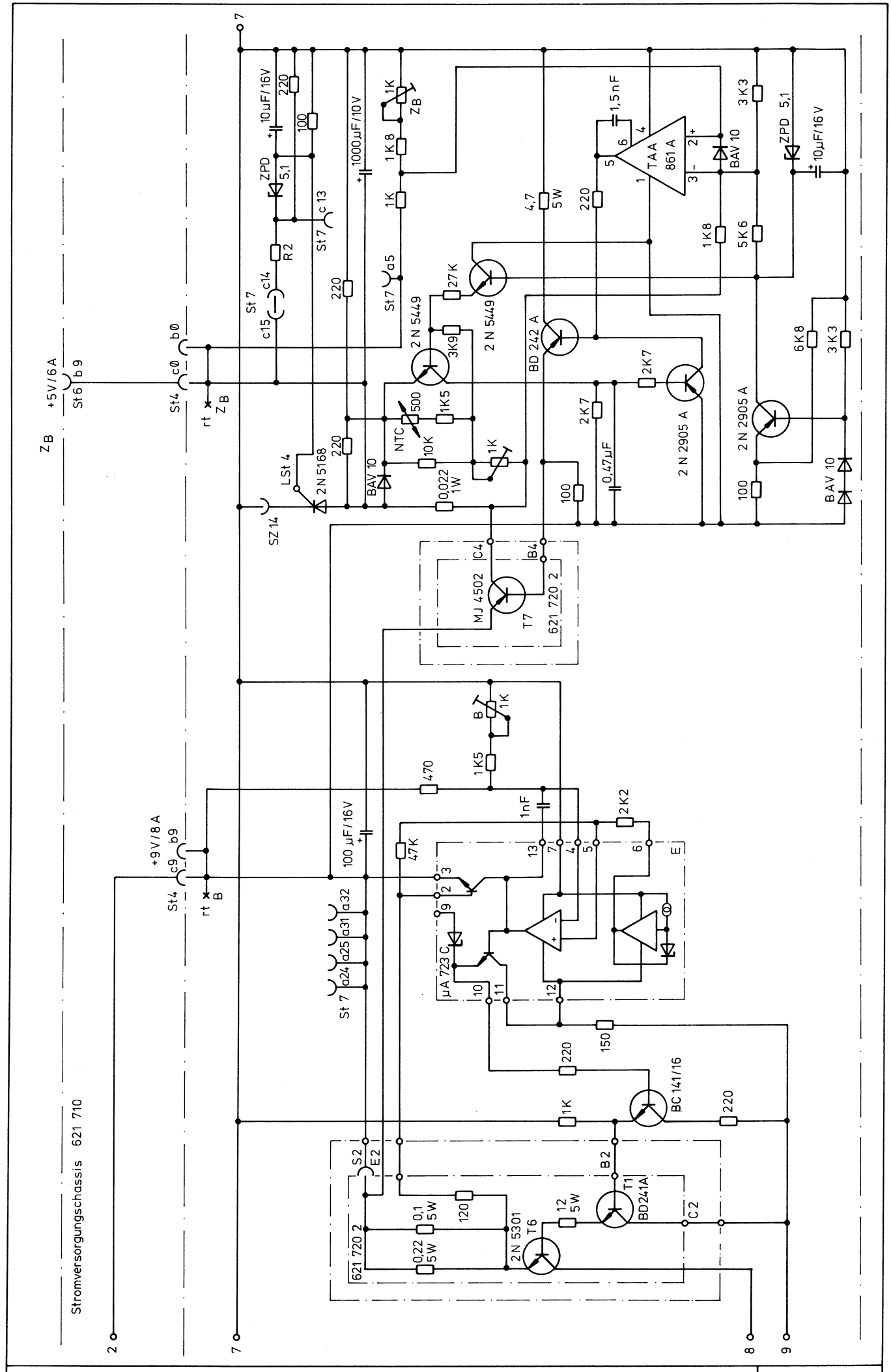
01.11.04


621 710 1
Rechnergehäuse 621 5
(621 C)
Tr. 2 BV 927
Tr. 1 BV 925
St 1
St 2
St 3
St 8
F1
F2
a1
a2
a3
a4
a5
a6, b1
b2
b3
e1 3,15 A m
e2 3,15 A m
e3 6,3 A m
1/1
1/2
1/3
1/4
1/5
1/6
2/6
3/6



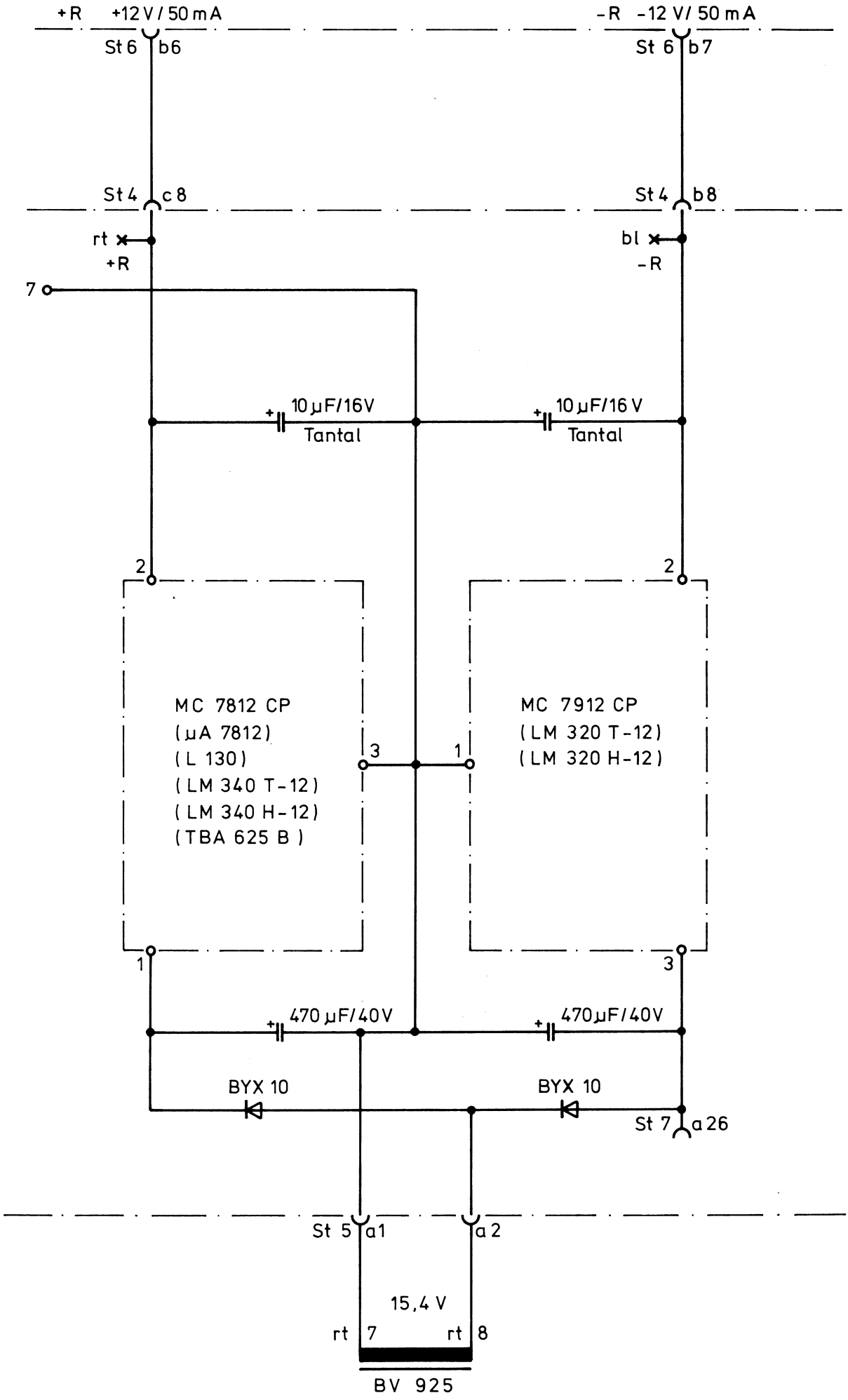
621 7 STROMVERSORGUNG

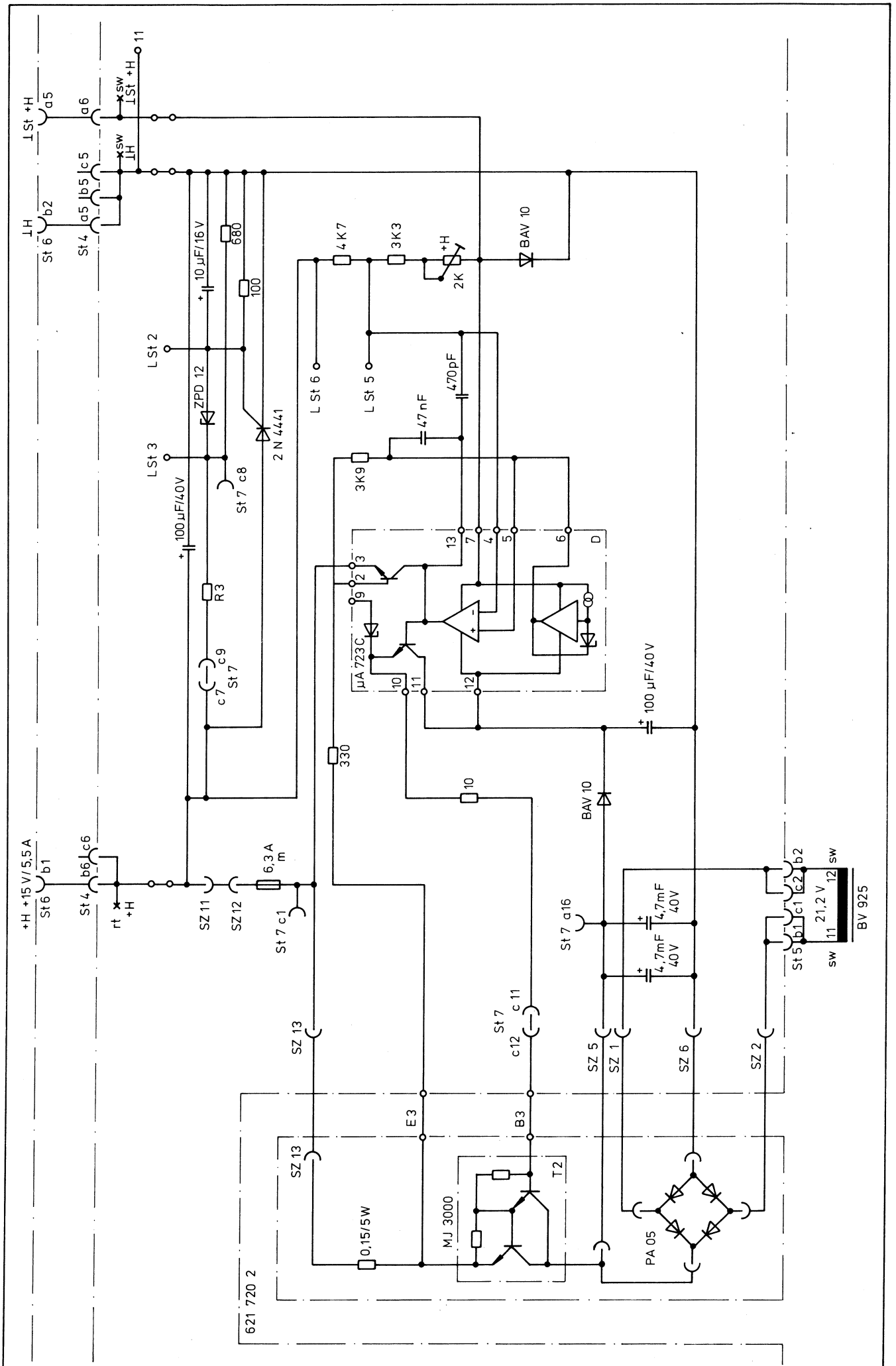
01. 11. 06



621 7 STROMVERSORGUNG

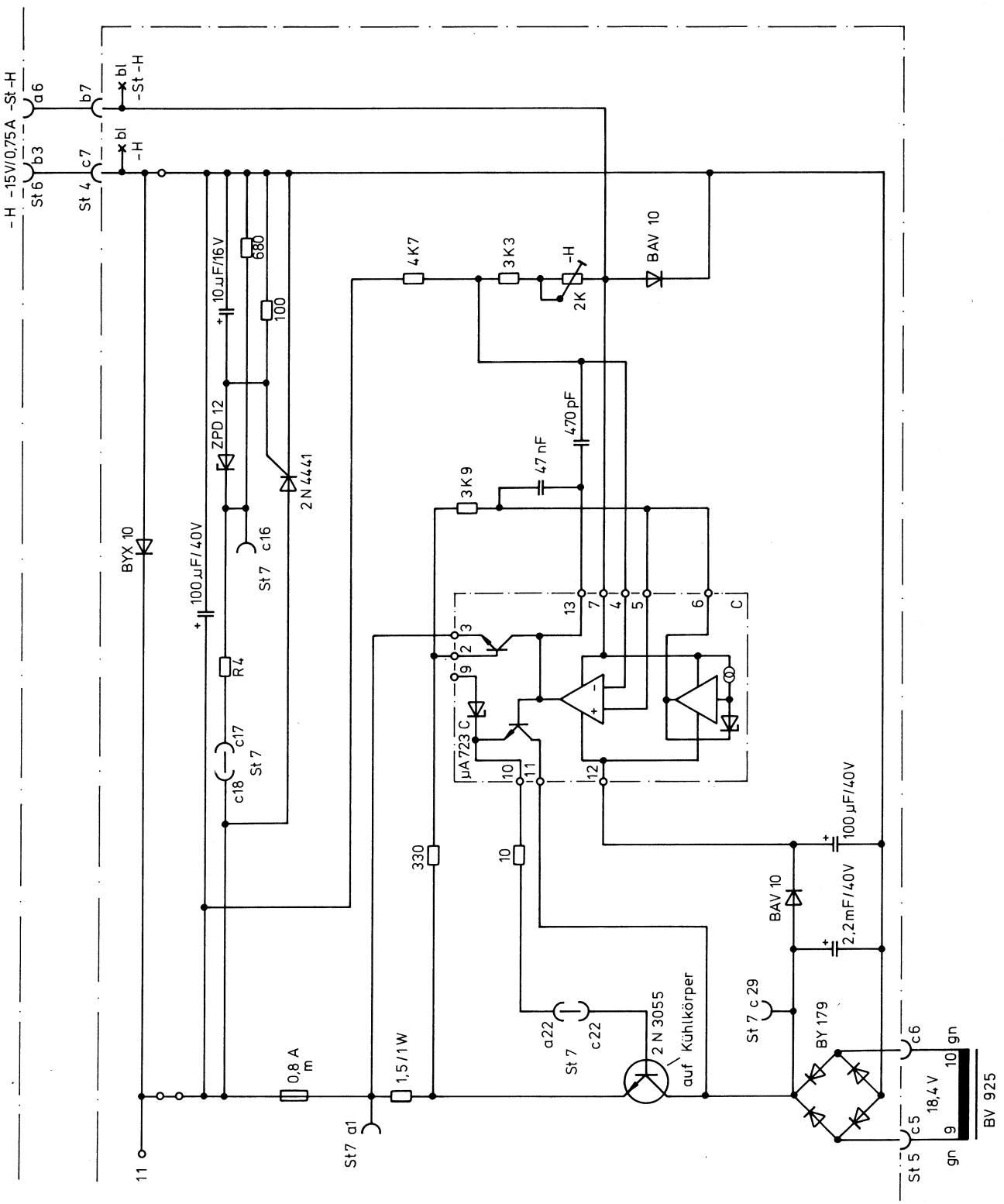
01. 11.07


+R +12 V / 50 mA
St 6 b6
-R -12 V / 50 mA
St 6 b7
St 4 c 8
St 4 b 8
rt
+R
bl
-R
7
10 µF/16V
Tantal
10 µF/16 V
Tantal
2
2
MC 7812 CP
(µA 7812)
(L 130)
(LM 340 T-12)
(LM 340 H-12)
(TBA 625 B)
3
1
MC 7912 CP
(LM 320 T-12)
(LM 320 H-12)
1
3
470 µF/40V
470µF/40V
BYX 10
BYX 10
St 7 a 26
St 5 a1
a 2
15,4 V
rt 7
rt 8
BV 925



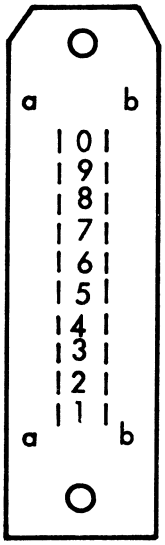
621 7 STROMVERSORGUNG

01. 11. 09



621 7 STROMVERSORGUNG 01. 11. 10

St.Nr.	Pol	Bezeichnung	Erklärung
	a0	⊥	
	a9	⊥	
	a8	⊥	
	a7	⊥	
	a6	ST -H	Steuer-Leitung
	a5	ST +H	Steuer-Leitung
	a4	+Z	
	a3	+Z	
	a2	+Z	
	a1	+Z	
	b0		
	b9	$+Z_B$	
	b8	ST +Z	Steuer-Leitung
	b7	-R	
	b6	+R	
	b5		
	b4	$\overline{\text{Netz}}$	
	b3	-H	
	b2	⊥ H	
	b1	+H	



20pol DIN-Stecker nach DIN 41622

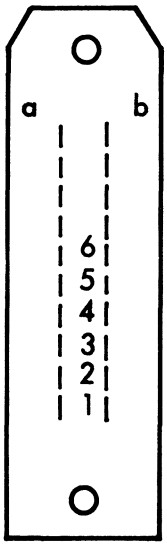
20 pol

O m. Riegelwanne
O m. Schirmwanne
O m. Griffschutz

am Stecker 302/303 mit ØV verbunden

am Stecker 104-204 mit ØV verbunden

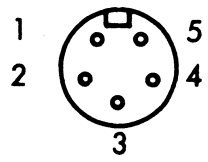
St.Nr.2



Pol	Bezeichnung	Erklärung
a6	⏚	
a5	+B	
a4	+Batterie	intern und extern
a3	⊥ Batterie	extern und Logikmasse
a2	220V-Trafo 1	
a1	CV-Trafo 1 u. 2	
b6	Aktivierung Batterie-Einschub	
b5		
b4		
b3	110V-Trafo 2	Ausg. f. Lüfter
b2	220V-Trafo 2	
b1	⏚	

12pol
⊗ m. Riegelwanne
O m. Schirmwanne
O m. Griffschutz

ST.3



Pol	Bezeichnung	Erklärung
1	+ Batterie	extern
2	+ Batterie	extern
3	Aktivierung Batterie-Einschub	
4	⊥ Batterie	extern
5	⊥ Batterie	extern

Flanschdose B
5-polig
Anschluß für Batterie-Einschub

St.8

Beide Flachsteckzungen an Logikmasse

Reihe: A

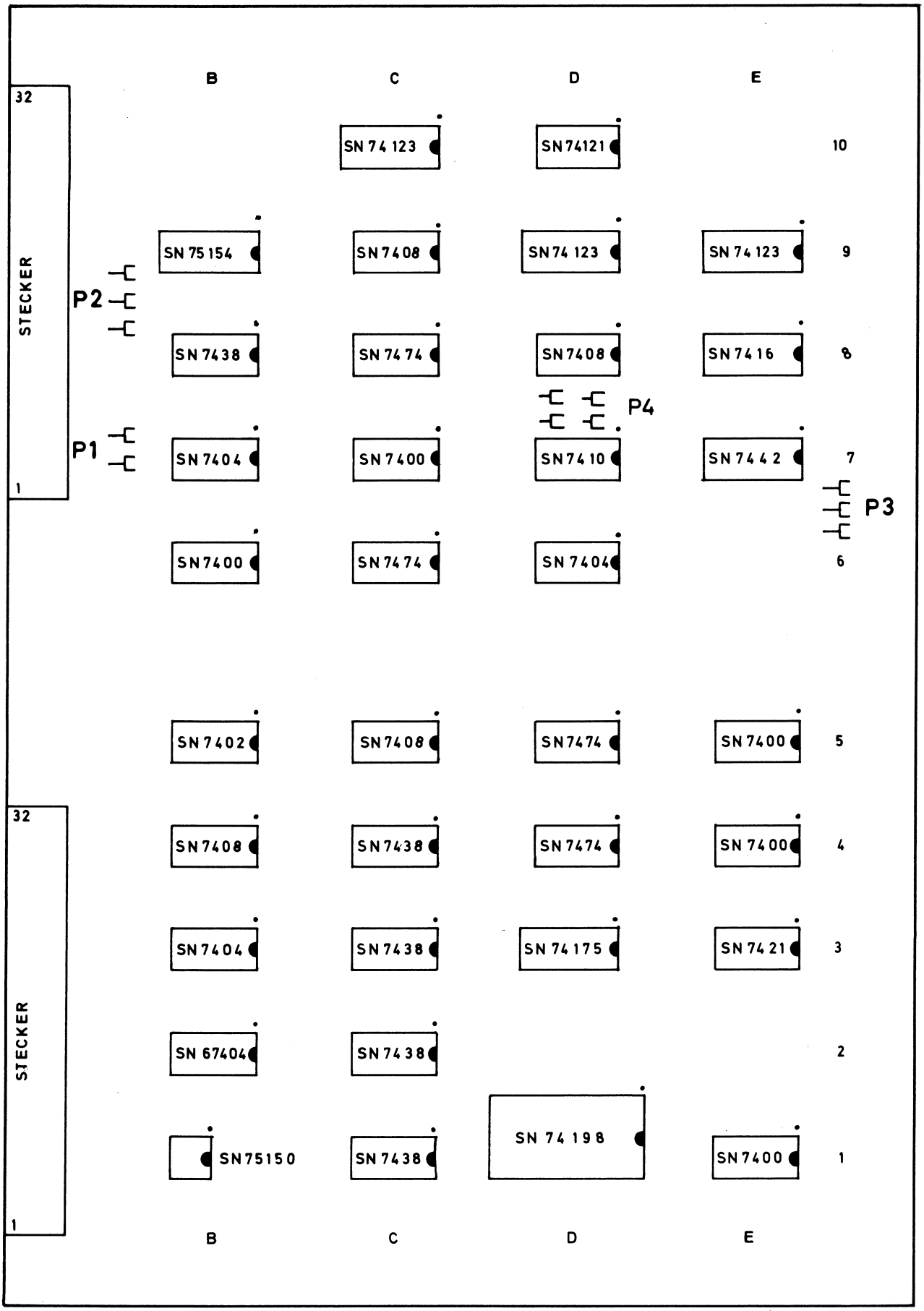
Pol	Bezeichnung	Erklärung
1	-H Masse	vor Sicherung
2		
3		
4		
5		Ausgang
6		
7	+Z	Ausgang
8	+Z Ü-Sch	
9	+Z Z-Diode	
10		
11		
12		
13		
14		
15		
16	+H U_{EL}	ungeregelt
17		
18	+Z PIN 10	Regler
19		
20		
21		
22	-H PIN 10	Regler
23	+Z Basis	BC 141/16
24	+B	
25	+B	
26	-R UEL	ungeregelt
27		
28		
29		
30		
31	+B	
32	+B	

Reihe: C

Pol	Bezeichnung	Erklärung
1	+H	vor Sicherung
2		
3		
4		
5		
6		
7	+H	Ausgang
8	+H Z-Diode	
9	+H Ü-Sch.	
10		
11	+H PIN 10	Regler
12	+H Basis	MS 3000
13	+Z_B Z-Diode	
14	+Z_B U-Sch	
15	+Z_B	Ausgang
16	-H Z-Diode	
17	-H U-Sch	
18	-H Masse	
19		
20		
21		
22	-H Basis	2 N 3055
23		
24	$\overline{N}$ Z-Diode	
25	$\overline{N}$ /+Z U_{EL} '	ungeregelt
26		
27		
28		
29	-H U_{EL}	ungeregelt
30		
31		
32	+Z Hilfs-U_{EL}	

	Pol	Bezeichnung	Erklärung			
St.5	a0	Z ~				
	b0	Z ~	parallel			
	c0	Z ~				
	a9	Z ~				
	b9	Z ~				
	c9	Z ~	+ Z ungeregelt			
	a8	Z ~				DIN-Stecker
	b8	Z ~				30pol
	c8	Z ~				
	a7	Z ~				
	b7	Z ~	parallel			
	c7	Z ~				
	a6					
	b6					
	c6	-H ~				
	a5					
	b5					
	c5	-H ~				
	a4					
	b4					
	c4					
	a3					
	b3					
	c3					
	a2	R ~				
	b2	+H ~	parallel			
	c2	+H ~				
	a1	R ~				
	b1	+H ~	parallel			
	c1	+H ~				

	Pol	Bezeichnung	Erklärung			
St.4	a0					
	b0	$+Z_B$				
	c0	$+Z_B$				
	a9					
	b9	+B				DIN-Stecker
	c9	+B				30 pol
	a8	$\overline{\text{Netz}}$				
	b8	-R				
	c8	+R				
	a7	Aktivierung Batterie-Einschub				
	b7	-ST -H	Steuer-Ltg.			
	c7	-H				
	a6	⊥ ST +H	Steuer-Ltg.			
	b6	+H				
	c6	+H				
	a5	⊥ H				
	b5	⊥ H				
	c5	⊥ H				
	a4	⊥ Z				
	b4	⊥ Z				
	c4	⊥ Z				
	a3	⊥ Z				
	b3	⊥ Z				
	c3	⊥ Z				
	a2	ST +Z	Steuer-Ltg.			
	b2	+Z				
	c2	+Z				
	a1					
	b1	+Z				
	c1	+Z				



P1 mit Brücke für Hazeltine

P2

Buffer Full für Logabox

Start

P3

Lo

Logabox

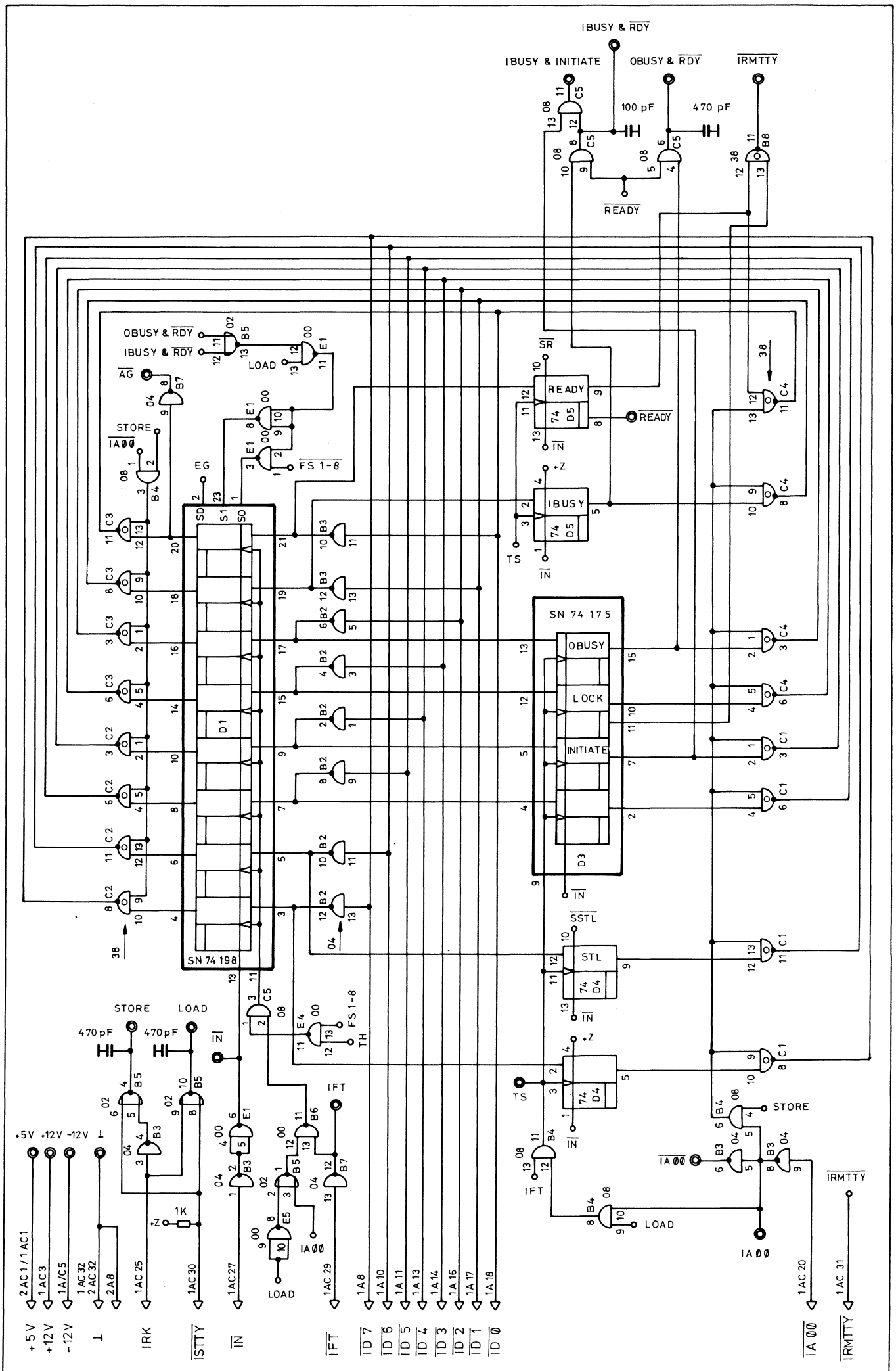
TTY
DIS
Teleprint

P4

1 Sperr - schritt

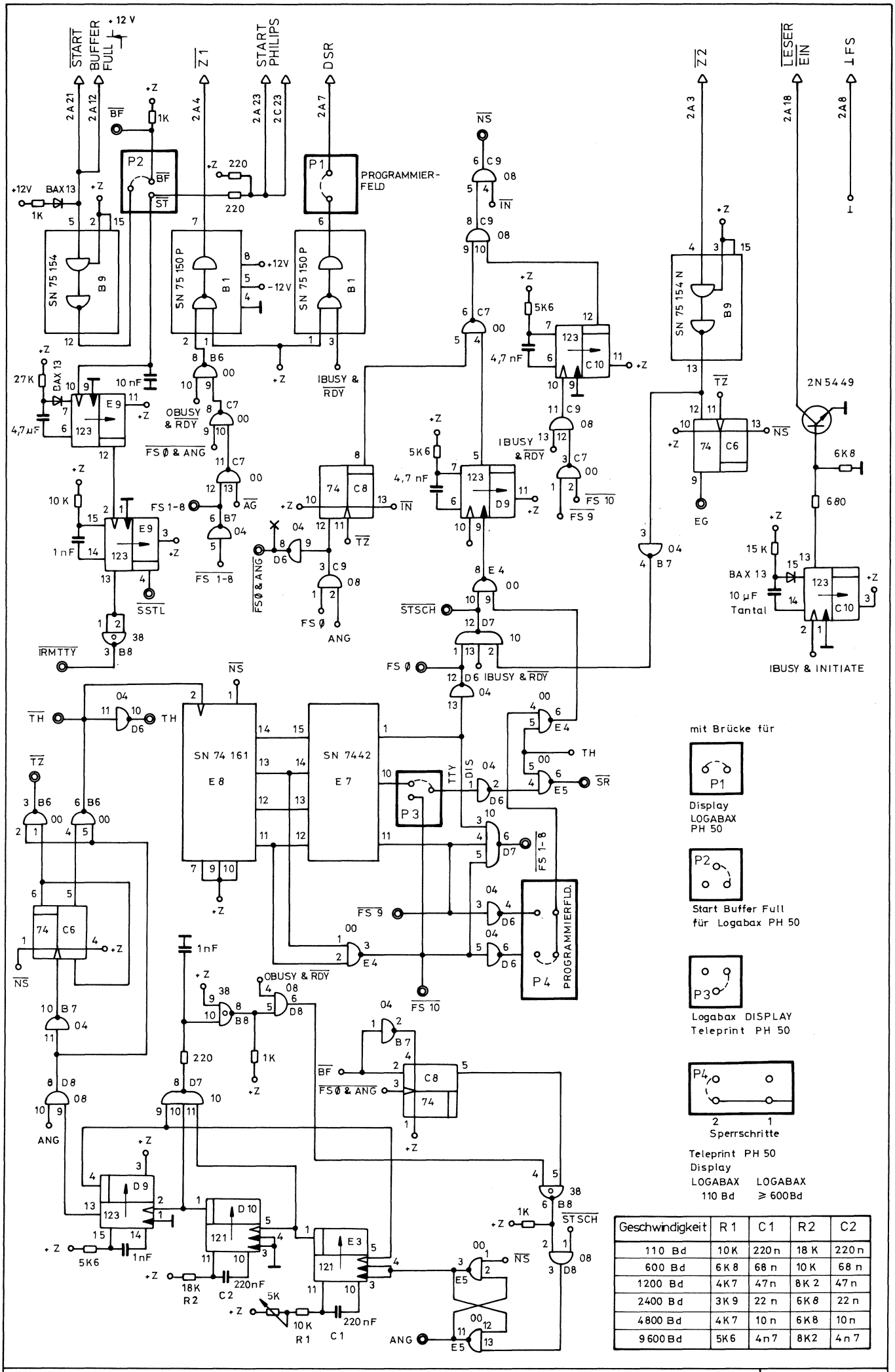
2 Sperrschritte

602 000 H	Interface Teletype / Display	01.12.01



602 000 H INTERFACE TELETYPE / DISPLAY

01.12.02



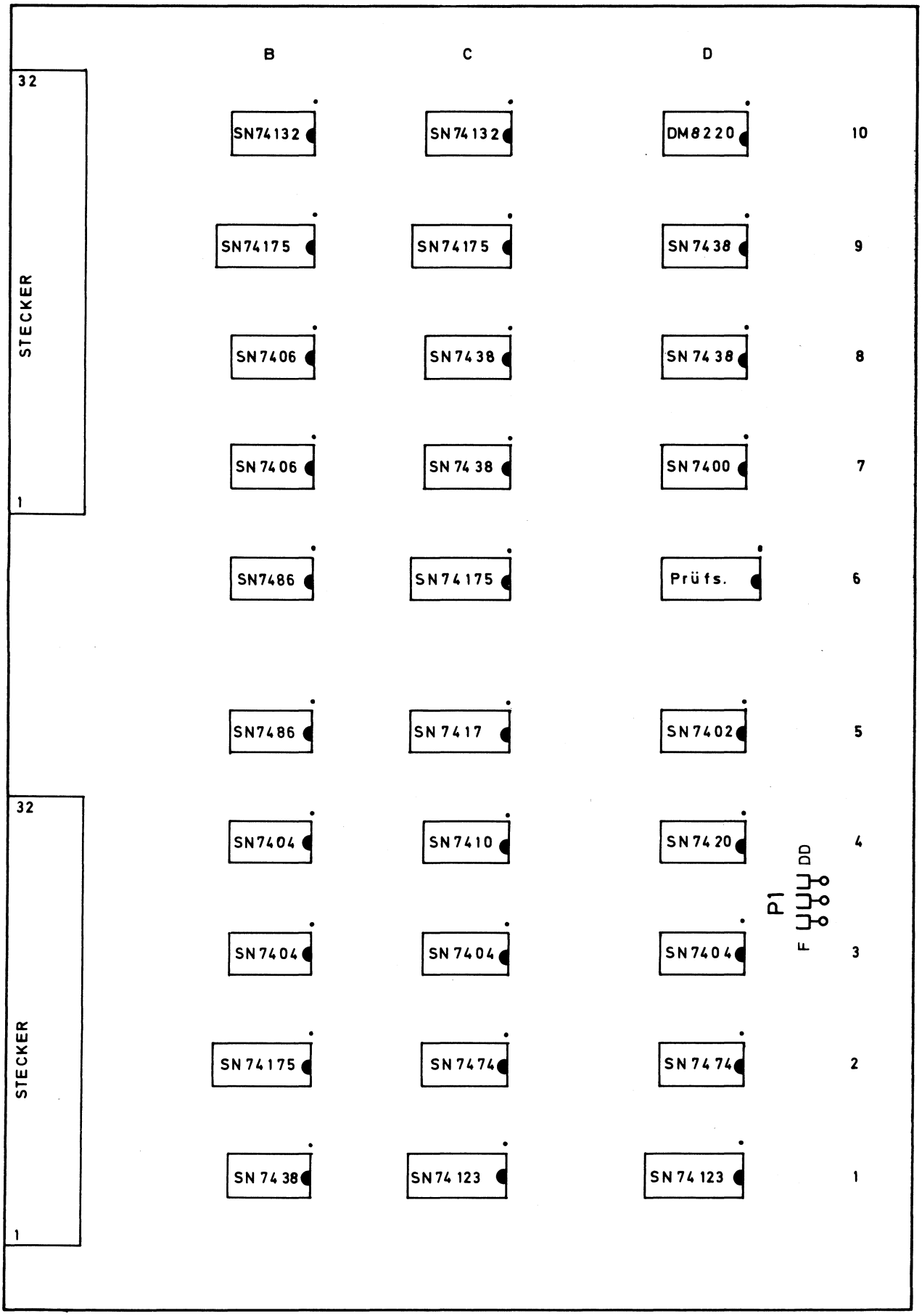
Geschwindigkeit	R 1	C1	R2	C2
110 Bd	10K	220n	18 K	220n
600 Bd	6K8	68 n	10 K	68 n
1200 Bd	4K7	47n	8K 2	47n
2400 Bd	3K 9	22 n	6K8	22n
4800 Bd	4K7	10 n	6K8	10n
9600 Bd	5K6	4n7	8K2	4n 7

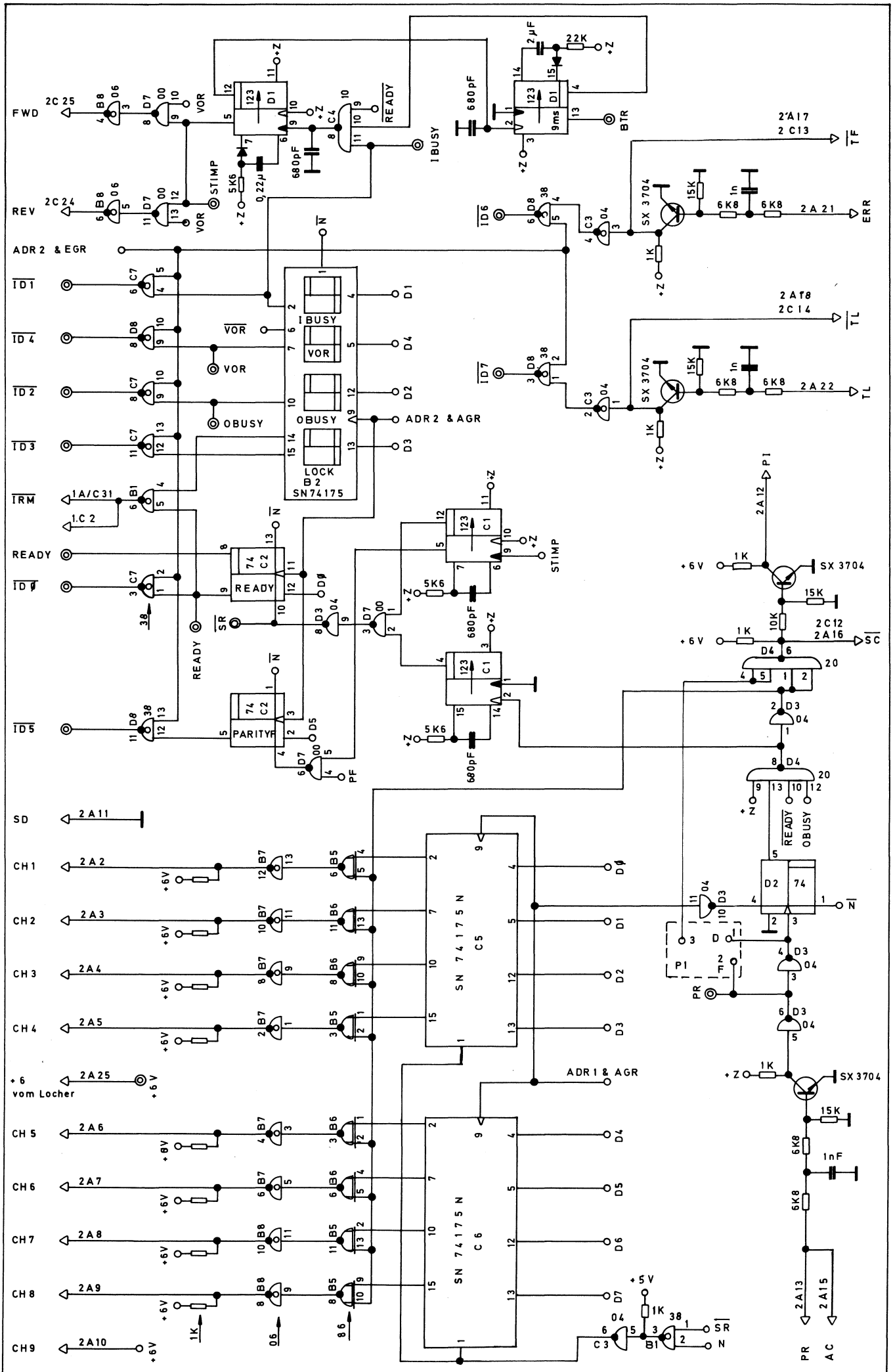
602 000 H INTERFACE TELETYPE / DISPLAY

01.12.03

Leiterseite 1A			Bauelementeseite 1C	
+Z		1	+Z	
		2		
+12V		3	+12 V	
		4		
-12 V		5	-12 V	
		6		
		7		
$\overline{ID7}$		8		
		9		
$\overline{ID6}$		10		
$\overline{ID5}$		11		
		12		
$\overline{ID4}$		13		
$\overline{ID3}$		14		
		15		
$\overline{ID2}$		16		
$\overline{ID1}$		17		
$\overline{ID\emptyset}$		18		
		19		
$\overline{IA\emptyset\emptyset}$		20	$\overline{IA\emptyset\emptyset}$	
		21		
		22		
		23		
		24		
IRK		25	IRK	
		26		
$\overline{IN}$		27	$\overline{IN}$	
		28		
$\overline{IFT}$		29	$\overline{IFT}$	
$\overline{ISTTY}$		30	$\overline{ISTTY}$	
$\overline{IRMTTY}$		31	$\overline{IRMTTY}$	
⊥		32	⊥	

Leiterseite 2A			Bauelementeseite 2C	
+Z		1	+Z	
		2		
$\overline{Z2}$		3		
$\overline{Z1}$		4		
		5		
		6		
DSR		7		
⊥		8		
		9		
		10		
		11		
Buffer Full		12		
		13		
		14		
		15		
		16		
		17		
$\overline{Leser\ Ein}$		18		
		19		
		20		
$\overline{Start}$		21		
		22		
		23		
		24		
		25		
		26		
		27		
		28		
		29		
		30		
		31		
⊥		32	⊥	

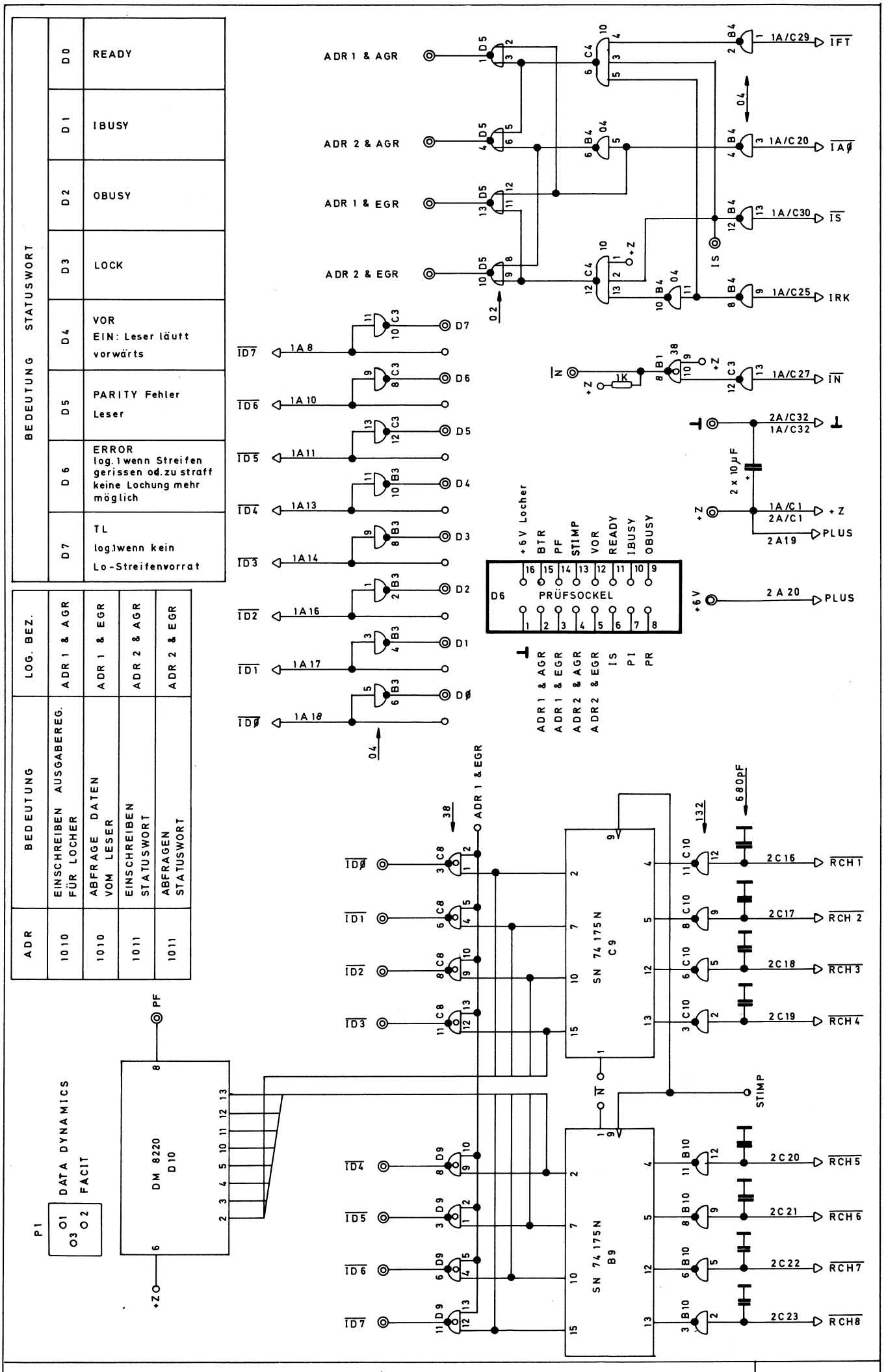

B
C
D
32
STECKER
1
SN74132
SN74132
DM8220
10
SN74175
SN74175
SN7438
9
SN7406
SN7438
SN7438
8
SN7406
SN7438
SN7400
7
SN7486
SN74175
Prüfs.
6
SN7486
SN7417
SN7402
5
32
SN7404
SN7410
SN7420
4
SN7404
SN7404
SN7404
3
STECKER
SN74175
SN7474
SN7474
2
1
SN7438
SN74123
SN74123
1
P1
DD



602 005 D,E2,E5 Interface Locher / Leser 01.13.02

BEDEUTUNG STATUSWORT		
D0	READY	
D1	IBUSY	
D2	OBUSY	
D3	LOCK	
D4	VOR EIN: Leser läuft vorwärts	
D5	PARITY Fehler Leser	
D6	ERROR log.1 wenn Streifen gerissen od. zu straff keine Lochung mehr möglich	
D7	TL log.1 wenn kein Lo-Streifenvorrat	

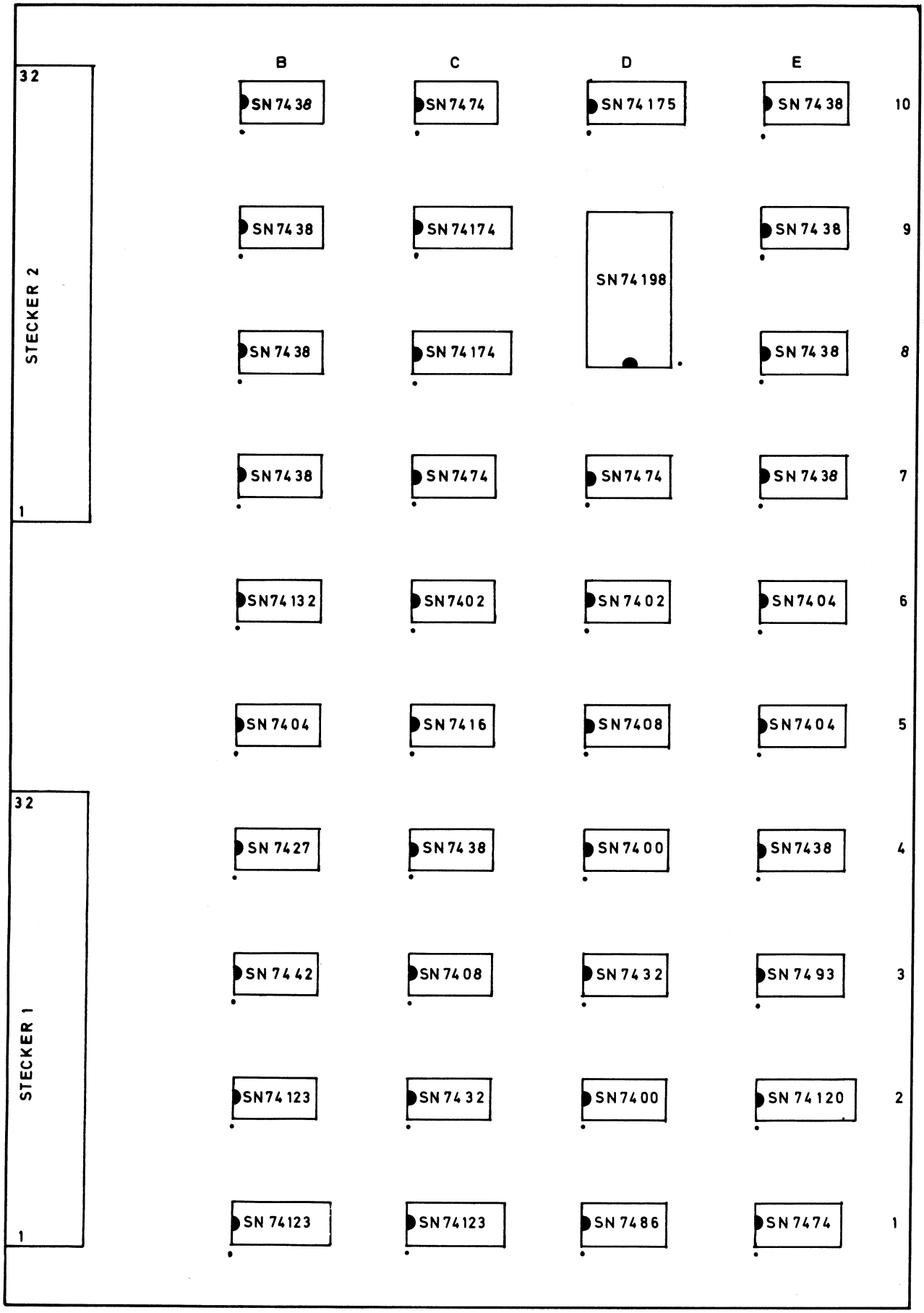
ADR	BEDEUTUNG	LOG. BEZ.
1010	EINSCHREIBEN AUSGABEREG. FÜR LOCHER	ADR 1 & AGR
1010	ABFRAGE DATEN VOM LESER	ADR 1 & EGR
1011	EINSCHREIBEN STATUSWORT	ADR 2 & AGR
1011	ABFRAGEN STATUSWORT	ADR 2 & EGR

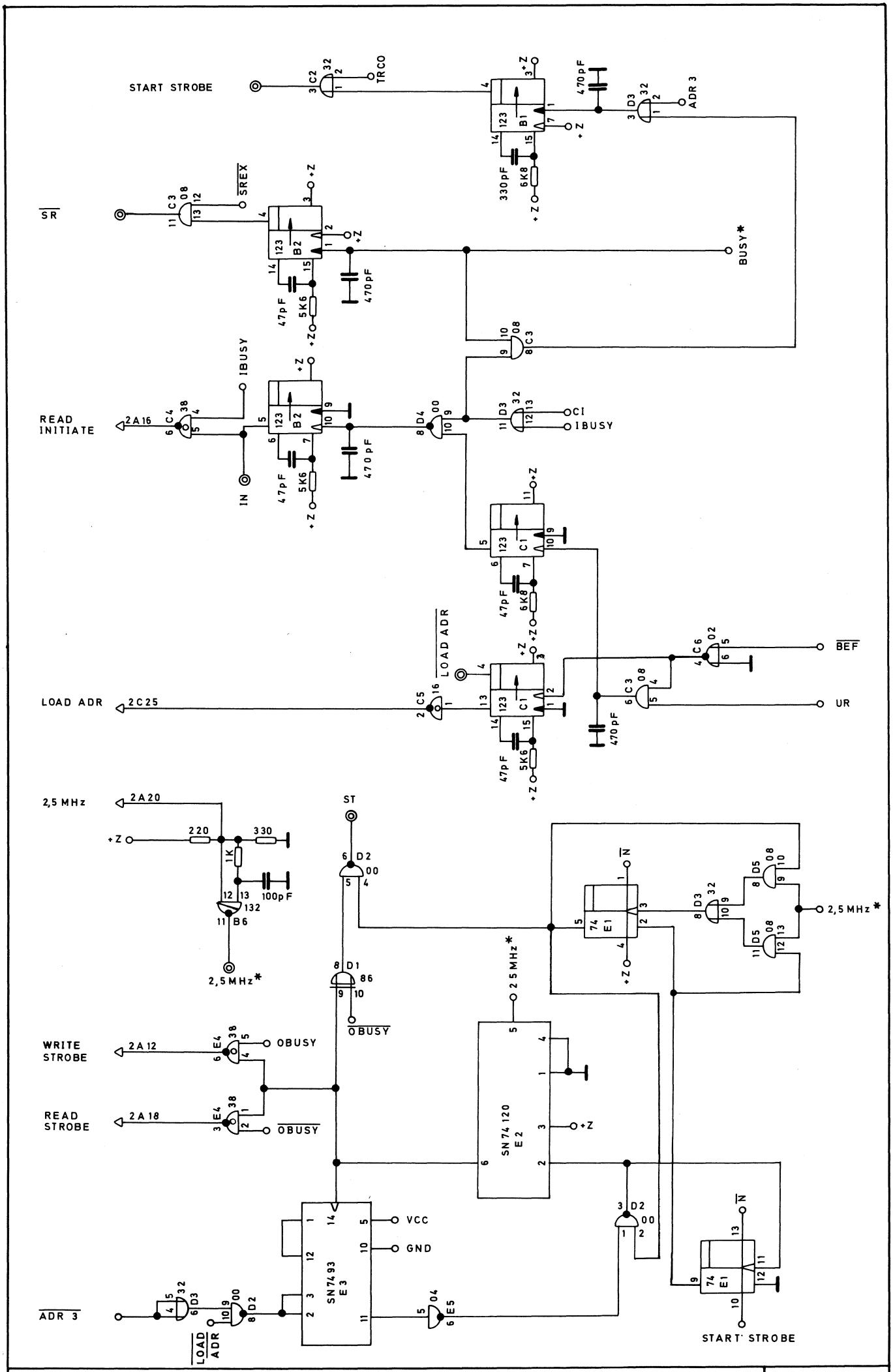


602 005 D E2 E5 Interface Locher / Leser 01.13.03

Leiterseite			Bauelementeseite	
1A			1C	
+Z		1	+Z	
		2	$\overline{IRM}$	
		3		
		4		
		5		
		6		
		7		
$\overline{ID7}$		8		
		9		
$\overline{ID6}$		10		
$\overline{ID5}$		11		
		12		
$\overline{ID4}$		13		
$\overline{ID3}$		14		
		15		
$\overline{ID2}$		16		
$\overline{ID1}$		17		
$\overline{ID\emptyset}$		18		
		19		
$\overline{IA\emptyset}$		20	$\overline{IA\emptyset}$	
		21		
		22		
		23		
		24		
IRK		25	IRK	
		26		
$\overline{IN}$		27	$\overline{IN}$	
		28		
$\overline{IFT}$		29	$\overline{IFT}$	
$\overline{IS}$		30	$\overline{IS}$	
$\overline{IRM}$		31	$\overline{IRM}$	
⊥		32	⊥	

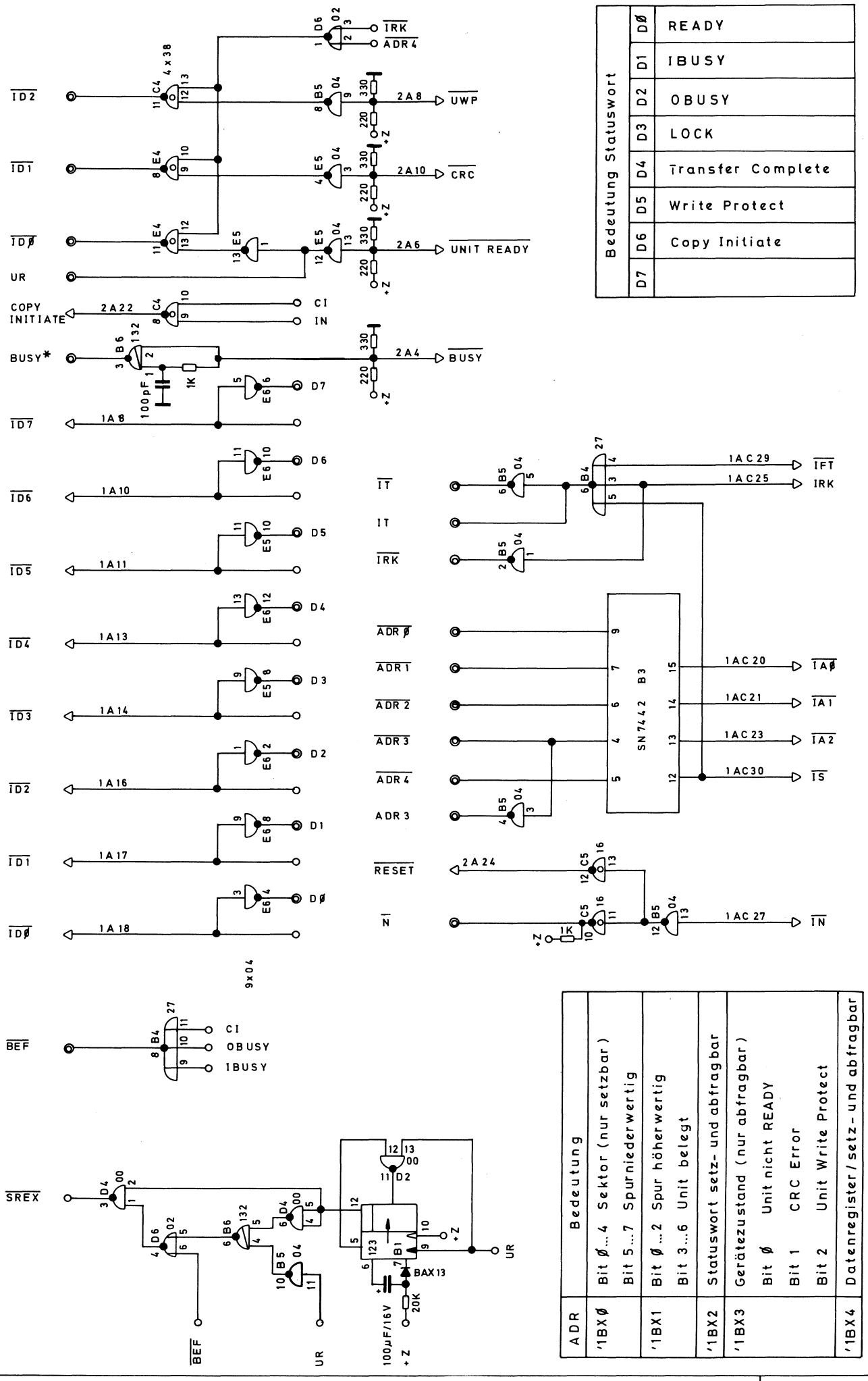
Leiterseite			Bauelementeseite	
2A			2C	
+Z		1	+Z	
CH1		2		
CH2		3		
CH3		4		
CH4		5		
CH5		6		
CH6		7		
CH7		8		
CH8		9		
CH9		10		
SD		11		
PI		12		
PR		13		
		14		
		15		
		16	$\overline{RCH1}$	
		17	$\overline{RCH2}$	
		18	$\overline{RCH3}$	
		19	$\overline{RCH4}$	
		20	$\overline{RCH5}$	
ERR		21	$\overline{RCH6}$	
TL		22	$\overline{RCH7}$	
		23	$\overline{RCH8}$	
		24	REV	
+6		25	FWD	
		26		
		27		
		28		
		29		
		30		
		31		
⊥		32	⊥	


B
C
D
E
32
STECKER 2
1
SN 74 38
SN 74 74
SN 74 175
SN 74 38
10
SN 74 38
SN 74174
SN 74198
SN 74 38
9
SN 74 38
SN 74 174
SN 74 38
8
SN 74 38
SN 7474
SN 7474
SN 74 38
7
SN 74 132
SN 7402
SN 7402
SN 7404
6
SN 7404
SN 7416
SN 7408
SN 7404
5
32
STECKER 1
1
SN 7427
SN 74 38
SN 7400
SN 7438
4
SN 74 42
SN 7408
SN 74 32
SN 74 93
3
SN 74 123
SN 74 32
SN 7400
SN 74 120
2
SN 74 123
SN 74123
SN 7486
SN 7474
1



602 018B,C1,C2,C3 Interface DIETZ-Disk

01.14.02

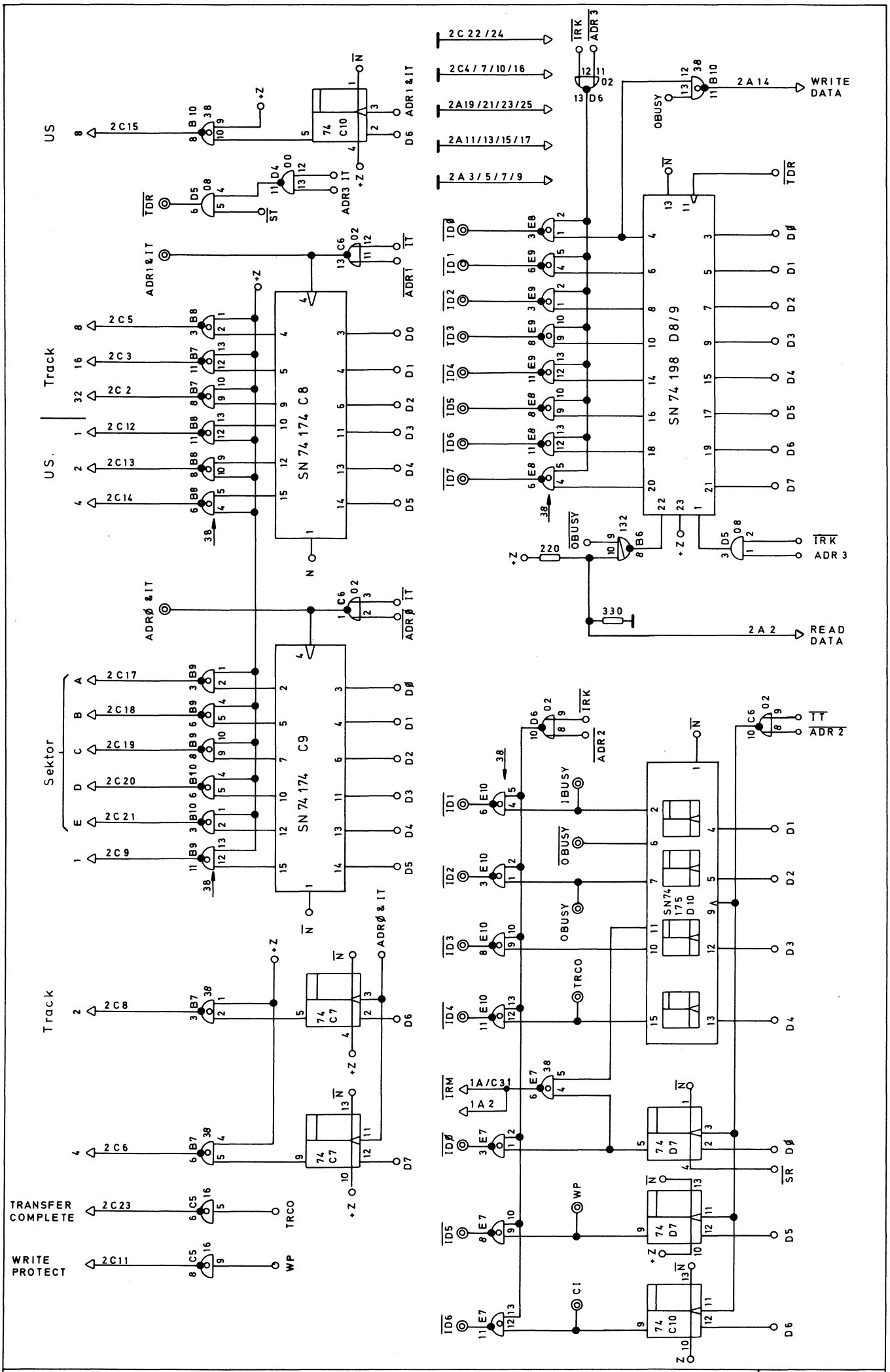


Bedeutung Statuswort		
	DØ	READY
	D1	IBUSY
	D2	OBUSY
	D3	LOCK
	D4	Transfer Complete
	D5	Write Protect
	D6	Copy Initiate
	D7	

ADR	Bedeutung
'1BXØ	Bit Ø...4 Sektor (nur setzbar) Bit 5...7 Spurniederwertig
'1BX1	Bit Ø...2 Spur höherwertig Bit 3...6 Unit belegt
'1BX2	Statuswort setz- und abfragbar
'1BX3	Gerätezustand (nur abfragbar) Bit Ø Unit nicht READY Bit 1 CRC Error Bit 2 Unit Write Protect
'1BX4	Datenregister/setz- und abfragbar

602 018B,C1,C2,C3 Interface DIETZ-Disk

01.14.03



602 018B C1 C2 C3 Interface DIETZ-Disk 01.14.04

Leiterseite			Bauelementeseite	
1A			1C	
+Z		1	+Z	
$\overline{IRM}$		2		
		3		
		4		
		5		
		6		
		7		
$\overline{ID7}$		8		
		9		
$\overline{ID6}$		10		
$\overline{ID5}$		11		
		12		
$\overline{ID4}$		13		
$\overline{ID3}$		14		
		15		
$\overline{ID2}$		16		
$\overline{ID1}$		17		
$\overline{ID\emptyset}$		18		
		19		
$\overline{IA\emptyset}$		20	$\overline{IA\emptyset}$	
$\overline{IA1}$		21	$\overline{IA1}$	
		22		
$\overline{IA2}$		23	$\overline{IA2}$	
		24		
IRK		25	IRK	
		26		
$\overline{IN}$		27	$\overline{IN}$	
		28		
$\overline{IFT}$		29	$\overline{IFT}$	
$\overline{IS}$		30	$\overline{IS}$	
$\overline{IRM}$		31	$\overline{IRM}$	
⊥		32	⊥	

Leiterseite			Bauelementeseite	
2A			2C	
+Z		1	+Z	
READ DATA		2	TRACK 32	
⊥		3	TRACK 16	
BUSY		4	⊥	
⊥		5	TRACK 8	
Unit Ready		6	TRACK 4	
⊥		7	⊥	
UWP		8	TRACK 2	
⊥		9	TRACK 1	
CRC		10	⊥	
⊥		11	WRITE PROTECT	
WRITE STROBE		12	US1	
⊥		13	US2	
WRITE DATA		14	US4	
⊥		15	US8	
Read Initiate		16	⊥	
⊥		17	Sektor A	
Read Strobe		18	Sektor B	
⊥		19	Sektor C	
2,5 MHz		20	Sektor D	
⊥		21	Sektor E	
Copy Initiate		22	⊥	
⊥		23	Transfer complete	
		24	⊥	
⊥		25	Load ADR	
		26		
		27		
		28		
		29		
		30		
		31		
⊥		32	⊥	

Potentialtabelle MINCAL 621

Die Potentialtabelle ist eine Auflistung aller JC-Plätze und der JC-Anschlüsse sowie aller Steckerpunkte auf der CPU, im folgenden Positionen genannt.

Zu jeder Position ist die Blatt-Nr. des Stromlaufplans aufgeführt.

Jede Position ist mit einem Namen versehen.
Nicht benannte Positionen sind frei bzw. sind mit der Betriebsspannung +Z oder Masse belegt.

Das Balkenkreuz vor einem Namen kennzeichnet Signalquellpunkte z.B. # ALUB

Ein Strich hinter dem Namen definiert das Signal im Betriebszustand mit Masse z.B. AØ4-

Signal mit einem Punkt und einer Nr. sind im Stromlaufplan nicht mit diesem Namen erwähnt, sind aber direkt oder indirekt mit der Erzeugung des bezeichneten Potentialnamens in Zusammenhang zu bringen z.B. M13.1

Die Potentialtabelle besteht aus zwei Teilen gleichen Inhalts.

Signal table of MINCAL 621

The table is a list of all the signal names and their associated IC and connector points in the CPU.

Sheets 02/03 list the signal names with the diagram numbers on which they are generated and a description of their function in the CPU.

Sheets 04-11 list the signal names in alphabetical order with all their respective connection points in the CPU.

Sheets 12 -20 list the IC and connector points in alphanumerical order with the respective signal name connected to the point.

The following is an explaination of the symbols and terminology used in this listing.

Every position has a signal name, and any free position is connected to +Z or 0 V.

The mark (#) before a signal name indicates this point is a sourse of the signal.

The dash (-) following a signal name indicates that the active level is 0 V, otherwise it is TTL high.

A signal name followed by a point and a number is not mentioned on the circuit diagram, but indicates a sourse (#) and any points to which it is connected.

eg.	F 15.Ø4	# M 13.1	(Sourse)
	L 03.08	M 13.1	goes to these points
	A 14.02	M 13.1	goes to these points

The circuit diagram numbers are listed in the table under "Schaltblatt" and can be found on the circuit diagram in the bottom right hand corner, indicated so - eg. Bl. No. 10.

Contents:

Signalname	Quell-punkt	Bedeutung	Description
+ Z		Spannungsversorgung + 5 V	+ Vcc
0 V		Masse	Logic ground
¹ - 7	9	F-Kanal-Anschluß zur Bedienungskonsole	F Channel 8 bit data display to the console
- 7	9	F-Kanal-Anschluß für RAM-Baustein	F Channel 8 bit data input to the RAM
>4k	8	Adresse ist größer 4k	Address > 4k
A ØØ - A 15	8	Adreßleitungen zum BUS	16 bit address BUS-Universal
A = B	6	Ergebnisausgang ALU	A = B Signal from the ALU
ALU A Ø - ALU A7	6	ALU-Anschluß A-Kanal	8 bit A Channel input to the ALU
ALU BØ - ALU B7	6	ALU-Anschluß B-Kanal	8 bit B Channel input to the ALU
ANF Ø5	Niv	Vorbereitungssignal MS Ø5	Force jump to MStep Ø5
ANF 34	Niv	Vorbereitungssignal MS 34	" " " " 34
B Ø - B 7	3	Datenausgang B-Register	8 bit B-Register output
BA	8	B-Register adreßgebend	B-Register on M Channel
BCP	8	Freigabe Adreßkanal zum BUS	Address BUS enabled
BE	1	Belegt-Signal für BUS	BUS in use control signal
Bootstrap	Bed	Bootstraptaste eingelegt	Hardware-Bootstrap selected on console
BusyCPU	1	Steuersignal für BUS-Belegung	Control signal, indicates BUS busy
Count down NP & T2	3	Zählimpuls für P-Register	Count P-Register down by 1
Count up P & T2	3	Zählimpuls für P-Register	Count P-Register up by 1
CR 5	Bed	ROM Ø5 erzeugt über Bedienungskonsole	Forces ROM Ø5 under console control
CR 6	Bed	ROM Ø6 erzeugt über Bedienungskonsole	" ROM Ø6 " " "
CR 7	Bed	ROM Ø7 " " "	" ROM Ø7 " " "
CR 10	Bed	ROM 10 " " Q-Register-Inhalt	" ROM 10 " Q-Register control
CR 15	Bed	ROM 15 " " Bedienungskonsole	" ROM 15 " console control
CR 17	Bed	ROM 17 " " "	" ROM 17 " " "
C Ø - C 4	Spl	Ausgang C-Register	5 bit "C"-Register output
ck	1	Taktsignal vom Oszillator 10 MHz	Computer clock 10 MHz
CM	Bed	Zählimpuls für M-Register	Count M-Register under console control
CN + 8	6	Übertragsausgang der ALU	Carry out from the ALU
CN	6	Übertragseingang der ALU	Carry in for the ALU
Count up	6	Steuersignal für Zähleingang NL und ML-Register	Count NL & ML up by 1
Count down	6	" " " " " "	Count NL & ML down by 1
D Ø - D 7	9	Daten-Ein/Ausgang für BUS	BI-Direction universal data BUS
DoF	10	Steuersignal für DO-Befehle	Control signal for DO-instruction
DS LEVEL	8	Durchschaltung der Level	Control signal connect L-Register on M Channel
DUE	10	Steuersignal für DO-Befehle mit Übertragsverarbtg.	Control signal for DO-instruction with LINK effective
END	Spl	Steuersignal für Befehlsende	Control signal for instruction end
F Ø - F 7	6	Datenausgänge der ALU	F Channel 8 bit output of the ALU
FE	BUS	Rückmeldesignal für BUS-Belegung (fertig)	BUS control signal indicating transfer completed
FEIN	1	Rückmeldesignal für BUS-Belegung intern	internal FE
GE	BUS	Aktives Element wünscht BUS zu belegen (gewünscht)	BUS signal to enable an active element to demand the BUS
GET LEVEL	11	Abfragesignal der Level-Information	Control signal for GL instruction
GO	Bed	Signal von der GO-Taste der Bed.-Konsole	Signal from the GO-switch on console
HLT	Bed	Signal von der HLT-Taste der Bed.-Konsole	Signal from the HALT-switch on console
ICL	Niv	Identifizierung Clock-Start	CNP real time clock interrupt
IFT	8	Einschreibtakt für Interface-Schaltungen	Interface clock
IN	7	Identifizierung Netzausfall-Start	CNP mains fail interrupt
'E	10	Steuersignal für DO-Befehl mit Inkrement Operant	Control signal for DO-instruction with M + 1
Ir	Niv	Identifizierung Parity-Start	CNP parity fail interrupt
IREG	10	Steuersignal für DO-Befehl mit Inkrement Register	Control signal for DO-instruction with REG + 1
IRMLL	8	Interface-Rückmeldung für Locher/Leser	Read/punch ready set program level
IRMTTY	8	Interface-Rückmeldung für Teletype	Teletype ready, set program level
ISLL	8	Interface-Selektion für Locher/Leser	Read/punch interface addressed
ISTTY	8	Interface-Selektion für Teletype	Teletype interface addressed
IWD	Niv	Identifizierung Watchdog-Start	CNP watchdog interrupt
LDNL	Niv	Lade N-Register linke Seite	Load NL
Level 1 - Level 8	Niv	Level-Information 1 - 8	4 bit BCD level information
LOAD Q	11	Ladepotential für Q-Register	Enable load Q-Register
LOAD B	11	" " B-Register	" " B- "
LOAD D	11	" " D-Register	" " D-"
LOAD ML	11	" " M-Register links	" " most significant 8 bits of M
LOAD MR	11	" " M-Register rechts	" " least " " " M
LOAD NL	11	" " N-Register links	" " most " " " N
LOAD NR	11	" " N-Register rechts	" " least " " " N
LOAD P	11	" " P-Register	" " P-Register
LSAD 1	1	Steuersignal für Übernahme N-Reg.links nach M-Reg. links	Control signal to load ML from NL
M ØØ - M 15	8	M-Kanal = Adreßkanal intern	M BUS 16 bit internal address BUS
MA	8	M-Register adreßgebend	M Register on M Channel
MARK	Spl	Steuersignal für MS-Zähler	Control signal for μ program jumps
Ø - ML 7	4	Inhalt M-Register links	Most significant 8 bits of M Register
MR Ø - MR 7	4	Inhalt M-Register rechts	Least " 8 bits of M "
MR 11*	8	Anwahlleitung für RAM-Baustein	Selects RAM card
MS ØØ - MS 37	10	Mikroschritt ØØ bis 37	Current μ program step
N	Bed	Nullstellung allgemein	Clear switch on console

Signalname	Quell-punkt	Bedeutung	Description
$\overline{NA}$	8	N-Register adreßgebend	N Register on M Channel
$\overline{NBM}$	1	Nullstellung B-Register, M-Register	Clear B & M Registers
[illegible]A	1	Nullstellung allgemein	Clear the control Registers, N, A, Q etc.
[illegible]	1	Nullstellung P-Register	Clear P Register
NL Ø - NL 7	5	Inhalt N-Register links	Most significant 8 bits of N Register
NR Ø - NR 7	5	Inhalt N-Register rechts	Least " 8 bits of N Register
P Ø - P 7	3	Inhalt P-Register	8 bit P Register output
PA	8	P-Register ist adreßgebend	P-Register on M Channel
PAUSE	1	Rechner in Pause-Stellung	Computer in pause mode
PROGR	Niv	Rechner ist im Programmlauf	Computer in program mode
Q Ø - Q 7	10	Inhalt Q-Register	Q-Register 8 bit output
R 25	11	Gesteuertes Signal ROM 25 für Branch-Befehle	Control signal ROM 25 for branch instructions
RK	9	Richtungskennzeichen für BUS-Steuerung	Signal indicating direction of data transfer
RL	2	Übertragssignal für A-Register (Shift links)	Shift left A-Register
RR	2	" " " (Shift rechts)	Shift right A-Register
ROM ØØ - ROM 27	11	CPU-Steuersignale aus dem ROM-Speicher	24 bit μ program word
S Ø - S 7	9	Dateneingang für das A-Register	8 bit data input to the A-Register
SLI	2	Übertragssignal für A-Register (intern 1 Byte)	Overflow signal for shift left
SLUE	2	" " " (Mehrbyte)	Shift left open control signal for multi byte
SWITCH Ø -SWITCH7	Bed	Dateneingang des Switch-Registers über Bed.Kons.	8 bit switch register on the console
SWML	Bed	Setzimpuls M-Register links	Console-enable display/load M-Reg. left
SWMR	Bed	" " rechts	" " " " right
SWNL	Bed	" N-Register links	" " " N-Reg. left
SWNR	Bed	" " rechts	" " " " right
SYN	1	Synchronsignal für BUS-Steuerung	Synchronization signal for BUS operations
[illegible]	1	Taktimpuls 1	Clock inputs fetch cycle
[illegible]00	1	Taktring Stellung 1	Clock position 1
T 2	1	Taktimpuls 2	Clock inputs execute cycle
T 200	1	Taktring Stellung 2	Clock position 2
T 400	1	" " 4	Clock position 4
$\overline{TA}$	2	Einschreibtakt für A-Register	CLK for "A"-Register
$\overline{SPRUNG}$	10	Steuersignal für MS-Zähler	Control signal for program jumps

Zeichenerklärung:

Bed	Quellpunkt	liegt	auf	der	Bedienungskonsole
BUS	"	"	"	"	BUS-Anschlußkarte
Niv	"	"	"	"	Level-Logik
SpL	"	"	"	"	Schritt-Sprung-Logik

Alle übrigen Quellpunkte liegen auf der CPU. Die Zahlen stehen in Klammern links vor der Seitennumerierung.

PLATZ	SCHALTBLATT	POTENTIAL
G05.02	01	+Z
G07.01	06	+Z
G07.13	02	+Z
E06.04	01	+Z
H01.13	01	+Z
H02.01	01	+Z
H02.04	01	+Z
H12.04	08	+Z
I16.10	08	+Z
I16.11	08	+Z
K03.10	01	+Z
K07.16	11	+Z
K08.16	11	+Z
K09.16	11	+Z
L07.16	11	+Z
L16.13	04	+Z
F16.10	09	0
B16.04	09	#0
300A10	09	0
E10.04	09	#0-
B16.03	09	0-
302C10	09	0-
F08.12	02	0V
G08.12	06	0V
G10.07	07	0V
G11.07	07	0V
G14.07	07	0V
G15.07	07	0V
H01.09	01	0V
H05.04	06	0V
H08.12	06	0V
H10.07	07	0V
H11.07	07	0V
H14.07	07	0V
H15.07	07	0V
K07.08	11	0V
K08.08	11	0V
K09.08	11	0V
K16.12	08	0V
K16.13	08	0V
L02.08	10	0V
L07.08	11	0V
M06.04	10	0V
M09.08	10	0V
B16.02	09	#1
300A09	09	1
E16.01	09	1
E10.06	09	#1-
B16.01	09	1-
302C11	09	1-
303C10	09	1-
E16.10	09	2
B16.10	09	#2
300A08	09	2
F10.02	09	#2-
B16.11	09	2-
302C08	09	2-
303C08	09	2-
303C11	09	2-
F16.04	09	3
B16.12	09	#3

PLATZ	SCHALTBLA	POTENTIAL
300A07	09	3
F10.04	09	#3-
B16.13	09	3-
302C09	09	3-
303C09	09	3-
F16.13	09	4
A16.04	09	#4
300A06	09	4
F10.08	09	#4-
A16.03	09	4-
302C06	09	4-
303C06	09	4-
A16.02	09	#5
300A05	09	5
E16.04	09	5
F10.10	09	#5-
A16.01	09	5-
M13.09	05	5-
302C07	09	5-
303C07	09	5-
A16.10	09	#6
E16.13	09	6
300A04	09	6
F10.12	09	#6-
A16.11	09	6-
M13.13	05	6-
302C04	09	6-
303C04	09	6-
F16.01	09	7
A16.12	09	#7
300A03	09	7
F10.06	09	#7-
A16.13	09	7-
302C05	09	7-
303C05	09	7-
E05.04	08	>4K
H12.05	08	>K
H13.09	08	>K
I05.02	01	>K
F13.08	08	#A00-
100A20	08	A00-
100C20	08	A00-
101A20	08	A00-
101C20	08	A00-
202A25	08	A00-
204A25	08	A00-
301A10	08	A00-
F13.11	08	#A01-
100A21	08	A01-
100C21	08	A01-
101A21	08	A01-
101C21	08	A01-
202A24	08	A01-
204A24	08	A01-
301A11	08	A01-
E13.08	08	#A02-
100A23	08	A02-
100C23	08	A02-
101A23	08	A02-
101C23	08	A02-
202A23	08	A02-

PLATZ	SCHALTBLATT	POTENTIAL
204A23	08	A02-
301A12	08	A02-
E13.11	08	#A03-
100A24	08	A03-
100C24	02	A03-
101A24	08	A03-
101C24	08	A03-
202A22	08	A03-
204A22	08	A03-
301A13	08	A03-
B07.01	08	A04-
E14.03	08	#A04-
202A21	08	A04-
204A21	08	A04-
301A14	08	A04-
B07.03	08	A05-
E14.06	08	#A05-
202A20	08	A05-
204A20	08	A05-
301A15	08	A05-
F14.03	08	#A06-
B07.05	08	A06-
202A19	08	A06-
204A19	08	A06-
301A16	08	A06-
F14.06	08	#A07-
B07.09	08	A07-
202A18	08	A07-
204A18	08	A07-
301A17	08	A07-
F14.08	08	#A08-
B07.11	08	A08-
202A17	08	A08-
204A17	08	A08-
301A18	08	A08-
F14.11	08	#A09-
B07.13	08	A09-
202A16	08	A09-
204A16	08	A09-
301A19	08	A09-
C07.05	08	A10-
202A15	08	A10-
204A15	08	A10-
301A20	08	A10-
E14.08	08	#A10-
E14.11	08	#A11-
C07.03	08	A11-
202A14	08	A11-
204A14	08	A11-
301A21	08	A11-
E13.03	08	#A12-
D07.03	08	A12-
202A13	08	A12-
204A13	08	A12-
301A22	08	A12-
E13.06	08	#A13-
C07.01	08	A13-
202A12	08	A13-
204A12	08	A13-
301A23	08	A13-
C07.11	08	A14-

PLATZ	SCHALTBLATT	POTENTIAL
202A11	08	A14-
F13.03	08	#A14-
204A11	08	A14-
301A24	08	A14-
C07.13	08	A15-
F13.06	08	#A15-
202A10	08	A15-
204A10	08	A15-
301A25	08	A15-
G08.14	06	A=B
H08.14	06	A=B
105A27	06	A=B
G08.16	06	ALU.1
H08.07	06	ALU.1
E08.06	02	#ALU.1
F08.01	02	ALU.1
H05.06	06	#ALU.10
KL0110	06	ALU.10
H05.03	06	ALU.11
105A31	06	ALU.11
G06.03	06	#ALU.12
H05.05	06	ALU.12
G06.08	06	#ALU.2
E08.03	02	#ALU.2
K05.02	06	ALU.2
F08.23	02	ALU.2
G06.02	06	ALU.3
G06.10	06	ALU.3
G06.12	06	ALU.3
H04.12	06	#ALU.3
E08.02	02	ALU.3
E08.04	02	ALU.3
E10.02	02	#ALU.3
G06.09	06	ALU.4
G07.06	06	#ALU.4
G07.02	06	ALU.5
H06.13	06	#ALU.5
G06.11	06	#ALU.6
G07.03	06	ALU.6
H06.11	06	ALU.7
I06.12	06	#ALU.7
H06.12	06	ALU.8
KL0108	06	#ALU.8
KL0109	06	ALU.9
L09.06	06	#ALU.9
G08.02	06	ALUA0
H07.02	02	ALUA0
E09.05	02	ALUA0
F08.04	02	#ALUA0
G08.23	06	ALUA1
F08.06	02	#ALUA1
G08.21	06	ALUA2
F08.08	02	#ALUA2
G08.19	06	ALUA3
F08.10	02	#ALUA3
G14.15	07	NL2
H08.02	06	ALUA4
F08.14	02	#ALUA4
H08.23	06	ALUA5
F08.16	02	#ALUA5
H08.21	06	ALUA6

PLATZ	SCHALTBLATT	POTENTIAL
F08.18	02	#ALUA6
H07.12	02	ALUA7
H08.19	06	ALUA7
E09.01	02	ALUA7
I06.05	06	ALUA7
F08.20	02	#ALUA7
G08.01	06	ALUB0
H15.05	07	#ALUB0
G08.22	06	ALUB1
G15.05	07	#ALUB1
G08.20	06	ALUB2
G14.05	07	#ALUB2
G08.18	06	ALUB3
H14.05	07	#ALUB3
H08.01	06	ALUB4
H10.05	07	#ALUB4
G10.05	07	#ALUB5
H08.22	06	ALUB5
G11.05	07	#ALUB6
H08.20	06	ALUB6
H08.18	06	ALUB7
H11.05	07	#ALUB7
H04.03	01	ANF05-
103A05	01	ANF05-
G04.10	01	ANF34-
G03.10	01	ANF34-
103C27	01	ANF34-
H15.04	07	B0
I15.02	08	B0
L15.14	03	#B0
205A15	03	B0
G15.04	07	B1
I15.05	08	B1
L15.13	03	#B1
G14.04	07	B2
I15.11	08	B2
L15.12	03	#B2
H14.04	07	B3
I15.14	08	B3
L15.11	03	#B3
H10.04	07	B4
I10.02	08	B4
L10.14	03	#B4
G10.04	07	B5
I10.05	08	B5
L10.13	03	#B5
G11.04	07	B6
I10.11	08	B6
L10.12	03	#B6
H11.04	07	B7
I10.14	08	B7
L10.11	03	#B7
I10.09	08	BA-
I15.09	08	BA-
I16.05	08	BA-
K16.02	08	#BA-
E15.03	08	BCP-
E05.06	08	#BCP-
G05.09	01	BCP-
L09.03	08	#BCP.1-
E05.05	08	BCP.1-

PLATZ	SCHALTBLATT	POTENTIAL
H13.03	08	#BCP.2-
H13.06	08	#BCP.3-
H16.09	01	BE*-
K05.13	01	BE*-
K03.08	01	#BE- 90 LET I=0
300B19	08	BOOTSTRAP-
L10.07	03	BREG.1
L10.10	03	BREG.1
L15.15	03	BREG.1
I05.10	01	#BUSYCPU
I05.11	01	BUSYCPU
E12.13	01	BUSYCPU
G05.03	01	BUSYCPU
F14.02	08	BUSYCPU*
E15.04	08	#BUSYCPU*
F14.12	08	BUSYCPU*
H16.08	01	#BUSYCPU*
K03.04	09	BUSYCPU*
K03.09	01	BUSYCPU*
E12.02	01	#BUSYCPU*
E12.12	01	#BUSYCPU*
E13.02	08	BUSYCPU*
E13.05	08	BUSYCPU*
F13.02	08	BUSYCPU*
E13.09	08	BUSYCPU*
E13.12	08	BUSYCPU*
E14.02	08	BUSYCPU*
E14.05	08	BUSYCPU*
KL0113	09	BUSYCPU*
L04.11	09	BUSYCPU*
E14.09	08	BUSYCPU*
F14.09	08	BUSYCPU*
F13.12	08	BUSYCPU*
F14.05	08	BUSYCPU*
F13.09	08	BUSYCPU*
F13.05	08	BUSYCPU*
E14.12	08	BUSYCPU*
F05.09	01	BUSYCPU*
K02.08	01	#BUSYCPU*.1
K02.13	01	BUSYCPU*.1
E12.01	01	BUSYCPU*.1
K02.06	01	#BUSYCPU*.2
K02.09	01	BUSYCPU*.2
K02.04	01	BUSYCPU*.3
G02.11	01	#BUSYCPU*.3
H16.10	01	BUSYCPU.1
K05.12	01	BUSYCPU.1
F06.06	01	#BUSYCPU.1
I05.08	01	BUSYCPU.2
K05.11	01	#BUSYCPU.2
F06.08	01	#BUSYCPU.3
G03.12	01	BUSYCPU.3
G03.11	01	#BUSYCPU.4
I05.12	01	BUSYCPU.4
I05.09	01	BUSYCPU.5
I05.13	01	#BUSYCPU.5
K07.10	11	C0

PLATZ	SCHALTBLATT	POTENTIAL
K15.04	03	COUNTDOWNP&T2-
M10.03	03	#COUNTDOWNP&T2-
H05.08	03	#COUNTDOWNP&T2.1-
M10.02	03	COUNTDOWNP&T2.1-
M11.03	03	COUNTDOWNP&T2.1-
I09.11	06	#COUNTUP
M12.09	04	COUNTUP
M12.12	05	COUNTUP
H06.04	06	COUNTUP.1
I09.12	06	COUNTUP.1
I06.06	06	#COUNTUP.2
I09.13	06	COUNTUP.2
K15.05	03	COUNTUPP&T2-
M10.11	03	#COUNTUPP&T2-
205A23	03	COUNTUPP&T2-
M14.06	03	#COUNTUPP&T2.1-
M16.05	03	COUNTUPP&T2.1-
M11.02	03	COUNTUPP&T2.2-
M16.06	03	#COUNTUPP&T2.2-
M10.13	03	COUNTUPP&T2.3-
M11.01	03	#COUNTUPP&T2.3-
G16.13	11	CR05-
D07.10	11	#CR05-
M10.08	11	#CR05-
300B15	11	CR05-
G16.05	11	CR06-
300B16	11	CR06-
K09.09	11	#CR07-
G16.09	11	CR07-
G16.10	11	CR07-
300B17	11	CR07-
I16.01	08	CR10
K05.05	04	CR10
105C19	08	CR10
I08.01	11	CR15-
300A22	11	CR15-
I08.10	11	CR17-
K08.09	11	#CR17-
300A23	11	CR17-
H06.03	06	CUP
I06.04	06	CUP
100A18	09	D0-
101A18	09	D0-
102A17	09	D0-
104A17	09	D0-
F11.01	09	D0-
F16.08	09	#D0-
100A17	09	D1-
101A17	09	D1-
102A16	09	D1-
104A16	09	D1-
F11.12	09	D1-
100A16	09	D2-
101A16	09	D2-
102A15	09	D2-
104A15	09	D2-
E16.08	09	#D2-
F11.04	09	D2-
F16.06	09	#D3-
F11.09	09	D3-
100A14	09	D3-

PLATZ	SCHALTBLATT	POTENTIAL
K08.10	11	C0
K09.10	11	C0
M01.15	10	C0
M02.15	10	C0
M03.15	10	C0
M04.15	10	C0
105A14	10	C0
K07.11	11	C1
K08.11	11	C1
K09.11	11	C1
M01.14	10	C1
M02.14	10	C1
M03.14	10	C1
M04.14	10	C1
105A12	10	C1
K07.12	11	C2
K08.12	11	C2
K09.12	11	C2
M01.13	10	C2
M02.13	10	C2
M03.13	10	C2
M04.13	10	C2
105A29	10	C2
K07.13	11	C3
K08.13	11	C3
K09.13	11	C3
L01.09	10	C3
L02.06	10	C3
L02.09	10	C3
105A13	10	C3
K07.14	11	C4
K08.14	11	C4
K09.14	11	C4
L01.10	10	C4
105A16	10	C4
K01.06	01	#CLOCK*
K01.09	01	CLOCK*
K02.05	01	CLOCK*
I03.09	11	CLOCK*-
K01.08	01	#CLOCK*-
G05.12	01	CLOCK*-
I05.06	01	CLOCK-
K01.04	01	#CLOCK-
K01.05	01	CLOCK-
301A03	01	CLOCK-
A16.05	04	CM-
300A19	04	CM-
H06.05	06	CN+8-
H08.16	06	#CN+8-
I06.02	06	CN+8-
I06.03	06	CN+8-
K05.03	06	CN-
G08.07	06	CN-
I03.08	11	#CON
105A11	11	CON
I02.10	11	#CON.1
I03.10	11	CON.1
H06.01	06	#COUNTDOWN
M13.01	05	COUNTDOWN
M13.04	04	COUNTDOWN
H06.02	06	COUNTDOWN.1

PLATZ	SCHALTBLATT	POTENTIAL
101A14	09	D3-
102A14	09	D3-
104A14	09	D3-
E11.01	09	D4-
100A13	09	D4-
101A13	09	D4-
102A13	09	D4-
104A13	09	D4-
F16.11	09	#D4-
E11.12	09	D5-
E16.06	09	#D5-
100A11	09	D5-
101A11	09	D5-
102A12	09	D5-
104A12	09	D5-
E16.11	09	#D6-
E11.04	09	D6-
100A10	09	D6-
101A10	09	D6-
102A11	09	D6-
104A11	09	D6-
F16.03	09	#D7-
E11.09	09	D7-
100A08	09	D7-
101A08	09	D7-
102A10	09	D7-
104A10	09	D7-
L04.12	10	#DO-
L06.11	10	DO-
103C30	10	DO-
L04.13	10	DO.1-
L05.03	10	#DO.1-
L05.05	10	DOF
L06.05	10	DOF
M05.03	10	#DOF
M05.04	10	DOF
M05.11	10	DOF
M06.11	10	DOF
M08.10	10	DOF
105A23	10	DOF
L05.02	10	DOF-
L06.02	10	DOF-
M05.02	10	#DOF-
105A17	10	DOF-
L05.08	10	#DOF.1
M05.12	10	DOF.1
L05.10	10	DOF.2
L05.11	10	#DOF.2
L05.13	10	DOF.3
F04.13	10	#DOF.4
L04.09	10	DREG.1
L05.09	10	DREG.1
L06.12	10	#DREG.1
F03.11	10	DREG.1
F04.11	10	DREG.1
F04.05	10	DREG.2
F04.12	10	DREG.2
L06.03	10	DREG.3
F03.04	10	DREG.4
L06.06	10	#DREG.4
F03.13	10	#DREG.5

PLATZ	SCHALTBLATT	POTENTIAL
F04.04	10	DREG.5
F03.05	10	DREG.6
F03.12	10	DREG.6
I16.06	08	#DSLEVEL
103C26	08	DSLEVEL
I16.02	08	DSLEVEL.1
I16.08	08	#DSLEVEL.1
I16.13	08	DSLEVEL.1
I16.03	08	DSLEVEL.2
I16.12	08	#DSLEVEL.2
L09.05	06	DUE
M06.03	10	#DUE
F07.13	02	DUE
I06.13	06	DUE-
M06.02	10	#DUE-
L04.08	10	#DUE.1
M05.09	10	DUE.1
M06.09	10	DUE.1
M06.12	10	DUE.1
L06.09	10	END
105A24	10	END
H05.02	01	END-
E10.03	09	F0
E03.03	10	F0
G08.09	06	#F0
K13.15	04	F0
K14.03	04	F0
K15.15	03	F0
L13.15	05	F0
L14.03	05	F0
L15.03	03	F0
103C02	09	F0
F03.15	10	F0
E10.05	09	F1
K13.01	04	F1
G08.10	06	#F1
K14.04	04	F1
K15.01	03	F1
F03.01	10	F1
L13.01	05	F1
L14.04	05	F1
L15.04	03	F1
103C03	09	F1
E03.05	10	F1
K13.10	04	F2
K14.05	04	F2
G08.11	06	#F2
K15.10	03	F2
F03.10	10	F2
L13.10	05	F2
L14.05	05	F2
L15.05	03	F2
103C04	09	F2
F10.01	09	F2
E03.07	10	F2
F10.03	09	F3
K13.09	04	F3
K14.06	04	F3
K15.09	03	F3
F03.09	10	F3
G08.13	06	#F3

PLATZ	SCHALTBLATT	POTENTIAL
L14.06	05	F3
L15.06	03	F3
103C05	09	F3
E03.09	10	F3
K10.15	03	F4
K11.03	04	F4
K12.15	04	F4
F04.15	10	F4
F10.09	09	F4
E03.15	10	F4
L10.03	03	F4
L11.03	05	F4
L12.15	05	F4
L13.09	05	F4
H08.09	06	#F4
F04.01	10	F5
K10.01	03	F5
K11.04	04	F5
K12.01	04	F5
E03.17	10	F5
L10.04	03	F5
L11.04	05	F5
H08.10	06	#F5
F10.11	09	F5
K10.10	03	F6
F10.13	09	F6
K11.05	04	F6
K12.10	04	F6
L10.05	03	F6
L11.05	05	F6
E03.19	10	F6
H08.11	06	#F6
F04.10	10	F6
H08.13	06	#F7
E03.21	10	F7
K10.09	03	F7
K11.06	04	F7
K12.09	04	F7
L10.06	03	F7
L11.06	05	F7
L12.09	05	F7
F10.05	09	F7
F04.09	10	F7
A07.08	08	#FE-
E06.05	01	FE-
202A03	01	FE-
204C03	01	FE-
301A07	01	FE-
K02.03	01	#FE-VT400*-
K02.12	01	FE-VT400*-
K03.13	01	FE-VT400*-
E05.02	08	FE-VT400*-
A07.10	08	FE.1-
A07.09	08	FE.1-
D07.08	08	#FE.1-
D07.09	08	FE.2-
D07.06	08	#FE.2-
D07.05	08	FE.3-
E05.13	08	FE.3-
A07.06	08	#FE.3-
E05.09	01	FEIN-

PLATZ	SCHALTBLATT	POTENTIAL
F06.13	01	FEIN-
F06.12	01	FEIN-
F05.12	01	#FEIN-
F06.05	01	GE-
202C02	01	GE-
F06.10	01	GE-
M08.03	11	#GETLEVEL
103C31	11	GETLEVEL
A16.09	01	GO-
300A21	01	GO-
H05.13	01	HLT-
104C12	01	HLT-
300A14	01	HLT-
H11.13	07	ICL
103A28	07	ICL
E05.12	08	#IFT-
100A29	08	IFT-
100C29	08	IFT-
101A29	08	IFT-
101C29	08	IFT-
H10.13	07	IN
103A29	07	IN
M06.05	10	#IOPE
M07.09	04	IOPE
G11.13	07	IP
103A30	07	IP
L05.04	10	IREG-
M05.06	10	#IREG-
H05.09	03	IREG-
L05.06	10	#IREG-VDOF
M16.03	03	IREGVDOF-
100A31	08	IRMLL-
100C31	08	IRMLL-
101A31	08	IRMTTY-
101C31	08	IRMTTY-
A07.05	08	ISLL-
A07.03	08	#ISLL-
100A30	08	ISLL-
100C30	08	ISLL-
C07.04	08	#ISLL.1-
B07.12	08	#ISLL.1-
A07.12	08	ISLL.1-
C07.06	08	#ISLL.1-
C07.10	08	#ISLL.1-
D07.04	08	#ISLL.1-
B07.10	08	#ISLL.1-
B07.06	08	#ISLL.1-
B07.08	08	#ISLL.1-
B07.04	08	#ISLL.1-
B07.02	08	#ISLL.1-
D07.01	08	ISLL.1-
C07.12	08	#ISLL.1-
C07.02	08	#ISLL.1-
D07.02	08	#ISLL.2-
A07.13	08	ISLL.2-
A07.02	08	ISLL.2-
A07.01	08	ISLL.3-
101A30	08	ISTTY-
101C30	08	ISTTY-
A07.11	08	#ISTTY-
A07.04	08	ISTTY-

PLATZ	IALTBLATT	POTENTIAL
103A31	07	IWD
G10.13	07	IWD
L07.07	11	#L0ADQ-
M15.12	05	LDNL-
203C27	05	LDNL-
M13.12	05	LDNL.1
M13.10	05	LDNL.2
H15.13	07	LEVEL1
103A24	07	LEVEL1
G15.13	07	LEVEL2
103A25	07	LEVEL2
G14.13	07	LEVEL4
103A26	07	LEVEL4
H14.13	07	LEVEL8
103A27	07	LEVEL8
K08.01	11	#LOAD.1
L07.15	11	LOAD.1
K08.02	11	#LOAD.2
L07.14	11	LOAD.2
K08.03	11	#LOAD.3
L07.13	11	LOAD.3
L07.01	11	#LOADB-
L10.09	03	LOADB-
L15.09	03	LOADB-
L04.02	10	#LOADD
L06.13	10	LOADD
M05.01	10	LOADD
L04.01	10	LOADD-
L05.01	10	LOADD-
L07.09	11	#LOADD-
L07.03	11	#LOADML-
M07.04	04	LOADML-
300B13	04	LOADML-
L07.04	11	#LOADMR-
M15.01	04	LOADMR-
L07.05	11	#LOADNL-
M07.01	05	LOADNL-
L07.06	11	#LOADNR-
M15.10	05	LOADNR-
L07.02	11	#LOADP-
I09.09	03	LOADP-
F05.05	10	LOADQ
L05.12	10	LOADQ-
E12.06	01	#LSAD1
K05.09	11	LSAD1
K05.10	11	LSAD1
M09.03	11	LSAD1
D07.13	11	LSAD1
D07.11	11	LSAD1
E12.05	01	LSAD1M
K05.04	04	LSAD1M
I02.13	01	#LSAD1M
F15.08	08	#M00
F13.10	08	M00
F15.09	08	M00-
302C20	08	M00-
303C20	08	M00-
I14.03	08	#M00.1
I15.03	08	#M00.1
F15.04	08	#M01
F13.13	08	M01

PLATZ	SCHAL	ATT	POTENTIAL
F15.03	08		M01-
302C21	08		M01-
303C21	08		M01-
I14.04	08		#M01.1
I15.04	08		#M01.1
E15.08	08		#M02
E13.10	08		M02
E15.09	08		M02-
302C22	08		M02-
303C22	08		M02-
I14.12	08		#M02.1
I15.12	08		#M02.1
E13.13	08		M03
E15.12	08		#M03
E15.13	08		M03-
302C23	08		M03-
303C23	08		M03-
I14.13	08		#M03.1
I15.13	08		#M03.1
E14.01	08		M04
E15.02	08		#M04
E15.01	08		M04
I11.03	08		#M04-
I10.03	08		#M04-
203C09	08		M04-
302C24	08		M04-
303C24	08		M04-
E15.10	08		#M05
E14.04	08		M05
E15.11	08		M05-
I11.04	08		#M05-
I10.04	08		#M05-
203C08	08		M05-
302C25	08		M05-
303C25	08		M05-
F15.02	08		#M06
F14.01	08		M06
F15.01	08		M06-
I11.12	08		#M06-
I10.12	08		#M06-
203C07	08		M06-
302C26	08		M06-
303C26	08		M06-
F15.10	08		#M07
F14.04	08		M07
I10.13	08		#M07-
F15.11	08		M07-
I11.13	08		#M07-
203C06	08		M07-
302C27	08		M07-
303C27	08		M07-
F15.06	08		#M08
F15.05	08		M08-
F14.10	08		M08-
203C05	08		M08-
I13.03	08		#M08-
302C31	08		M08-
F15.12	08		#M09
F14.13	08		M09
F15.13	08		M09-
I13.04	08		#M09-

PLATZ	SCHALTBLA	POTENTIAL
203C04	08	M09-
302C30	08	M09-
303C30	08	M09-
E14.10	08	M10
E15.06	08	#M10
E15.05	08	M10-
203C03	08	M10-
I13.12	08	#M10-
302C29	08	M10-
303C29	08	M10-
E10.12	08	#M11
E10.13	08	M11-
E14.13	08	M11-
H13.10	08	M11-
203C02	08	M11-
H12.10	08	M11-
I13.13	08	#M11-
E13.01	08	M12.1
I12.03	08	#M12.1
H13.05	08	M12.1
E13.04	08	M13.1
H13.04	08	M13.1
I12.04	08	#M13.1
F13.01	08	M14.1
H13.02	08	M14.1
I12.12	08	#M14.1
H13.01	08	M15.1
F13.04	08	M15.1
I12.13	08	#M15.1
I12.09	08	MA-
I16.09	08	MA-
K16.04	08	#MA-
L02.11	04	MA-
I11.09	08	MA-
I13.09	08	MA-
I14.09	08	MA-
205A14	10	MARK-
I13.02	08	ML0
K13.03	04	#ML0
H15.02	07	ML0
K13.02	04	#ML1
G15.02	07	ML1
I13.05	08	ML1
G14.02	07	ML2
K13.06	04	#ML2
I13.11	08	ML2
K13.07	04	#ML3
H14.02	07	ML3
I13.14	08	ML3
K12.03	04	#ML4
H10.02	07	ML4
I12.02	08	ML4
K12.02	04	#ML5
I12.05	08	ML5
G10.02	07	ML5
I12.11	08	ML6
G11.02	07	ML6
K12.06	04	#ML6
K12.07	04	#ML7
H11.02	07	ML7
I12.14	08	ML7

PLATZ	SCHALTBLATT	PO .TIAL
I14.02	08	MR0
H15.01	07	MR0
K14.14	04	#MR0
K14.13	04	#MR1
G15.01	07	MR1
I14.05	08	MR1
H12.08	08	#MR11*
303C28	08	MR11*
H13.08	08	#MR11**
302C28	08	MR11**
H12.06	08	#MR11*.1
H12.09	08	MR11*.1
G14.01	07	MR2
K14.12	04	#MR2
I14.11	08	MR2
I14.14	08	MR3
K14.11	04	#MR3
H14.01	07	MR3
K11.14	04	#MR4
H10.01	07	MR4
I11.02	08	MR4
K11.13	04	#MR5
I11.05	08	MR5
G10.01	07	MR5
G11.01	07	MR6
K11.12	04	#MR6
I11.11	08	MR6
K11.11	04	#MR7
H11.01	07	MR7
I11.14	08	MR7
K11.07	04	MREG.1
K11.10	04	MREG.1
K14.15	04	MREG.1
K13.05	04	MREG.10
M12.06	04	#MREG.10
M12.08	04	#MREG.10
K13.04	04	MREG.11
M13.06	04	#MREG.11
K11.15	04	MREG.12
M12.05	04	MREG.12
K12.04	04	MREG.13
K13.13	04	MREG.13
K12.05	04	MREG.14
K13.12	04	MREG.14
K12.11	04	MREG.15
K13.11	04	MREG.15
L08.06	04	#MREG.15
L08.08	04	#MREG.15
L08.05	04	MREG.16
M07.06	04	#MREG.16
L08.04	04	MREG.17
M09.13	04	#MREG.17
L16.11	04	#MREG.18
M09.11	04	MREG.18
K05.06	04	#MREG.19
L08.09	04	MREG.19
K14.07	04	MREG.2
K14.10	04	MREG.2
L03.11	04	#MREG.2
K12.14	04	MREG.21
K13.14	04	MREG.21

H06.02	06	COUNTDOWN.1
H06.03	06	CUP
H06.04	06	COUNTUP.1
H06.05	06	CN+8-
H06.06	06	MS05-
H06.08	11	Q2
H06.09	11	ROM23-
H06.10	11	#ROM3.2-
H06.11	06	ALU.7
H06.12	06	ALU.8
H06.13	06	#ALU.5
H07.01	02	SRUE
H07.02	02	ALUA0
H07.03	02	#UEFF.1
H07.04	11	MS27-
H07.05	11	ROM3.2-
H07.06	11	#ROM3-
H07.08	11	#ROM3-
H07.09	11	Q3
H07.10	11	ROM3.3-
H07.11	02	#UEFF.1
H07.12	02	ALUA7
H07.13	02	SLUE
H08.01	06	ALUB4
H08.02	06	ALUA4
H08.03	06	ROM14-
H08.04	06	ROM15-
H08.05	06	ROM16-
H08.06	06	ROM17-
H08.07	06	ALU.1
H08.08	06	ROM13-
H08.09	06	#F4
H08.10	06	#F5
H08.11	06	#F6
H08.12	06	0V
H08.13	06	#F7
H08.14	06	A=B
H08.16	06	#CN+8-
H08.18	06	ALUB7
H08.19	06	ALUA7
H08.20	06	ALUB6
H08.21	06	ALUA6
H08.22	06	ALUB5
H08.23	06	ALUA5
H10.01	07	MR4
H10.02	07	ML4
H10.03	07	P4
H10.04	07	B4
H10.05	07	#ALUB4
H10.07	07	0V
H10.09	07	ROM7-
H10.10	07	ROM6-
H10.11	07	ROM5-
H10.12	07	SWITCH4
H10.13	07	IN
H10.14	07	NR4
H10.15	07	NL4
H10.16		
H11.01	07	MR7
H11.02	07	ML7
H11.03	07	P7
H11.04	07	B7
H11.05	07	#ALUB7
H11.06		
H11.07	07	0V
H11.08		
H11.09	07	ROM7-
H11.10	07	ROM6-
H11.11	07	ROM5-
H11.12	07	SWITCH7
H11.13	07	ICL
H11.14	07	NR7
H11.15	07	NL7
H11.16		
H12.01		
H12.02		
H12.03		
H12.04	08	+Z
H12.05	08	>K
H12.06	08	#MR11*.1
H12.07		
H12.08	08	#MR11*
H12.09	08	MR11*.1
H12.10	08	M11-
H12.11		
H12.12		
H12.13		
H12.14		
H13.01	08	M15.1
H13.02	08	M14.1
H13.03	08	#BCP.2-
H13.04	08	M13.1
H13.05	08	M12.1
H13.06	08	#BCP.3-
H13.07		
H13.08	08	#MR11**
H13.09	08	>K
H13.10	08	M11-
H13.11		
H13.12		
H13.13		
H13.14		
H14.01	07	MR3
H14.02	07	ML3
H14.03	07	P3
H14.04	07	B3
H14.05	07	#ALUB3
H14.06		
H14.07	07	0V
H14.08		
H14.09	07	ROM7-
H14.10	07	ROM6-
H14.11	07	ROM5-
H14.12	07	SWITCH3
H14.13	07	LEVEL8
H14.14	07	NR3
H14.15	07	NL3
H14.16		
H15.01	07	MR0
H15.02	07	ML0
H15.03	07	P0
H15.04	07	B0
H15.05	07	#ALUB0
H15.06		
H15.07	07	0V
H15.08		
H15.09	07	ROM7-
H15.10	07	ROM6-
H15.11	07	ROM5-
H15.12	07	SWITCH0
H15.13	07	LEVEL1
H15.14	07	NR0
H15.15	07	NL0
H15.16		
H16.01		
H16.02		
H16.03		
H16.04		
H16.05		
H16.06		
H16.07		
H16.08	01	#BUSYCPU*
H16.09	01	BE*-
H16.10	01	BUSYCPU.1
H16.11		
H16.12		
H16.13		
H16.14		
I02.01	01	#T2.1
I02.02	01	T400.1
I02.03	01	T2*-
I02.04	01	#WE.1-
I02.05	01	T400-
I02.06	01	T200-
I02.07		
I02.08	11	T1-
I02.09	11	ROM22-
I02.10	11	#CON.1
I02.11	01	MS02-
I02.12	01	T400
I02.13	01	#LSAD1M
I02.14		
I03.01	01	T1.1
I03.02	01	T1.1
I03.03	01	#T1
I03.04	01	WE.1-
I03.05	01	WE.2-
I03.06	01	#WE-
I03.07		
I03.08	11	#CON
I03.09	11	CLOCK*-
I03.10	11	CON.1
I03.11	01	#T2-
I03.12	01	T2.1
I03.13	01	T2.1
I03.14		
I04.01	01	T100.2
I04.02	01	T400.1
I04.03		
I04.04		
I04.05	01	NBM.2-
I04.06	01	#NBM-
I04.07		
I04.08	11	ROM22-
I04.09	11	#ROM22
I04.10	01	#T400*
I04.11	01	T400-
I04.12	01	#NP-
I04.13	01	NP.4-
I04.14		
I05.01	01	#WE.2-
I05.02	01	>K
I05.03	01	WE.3-
I05.04	01	#T100.2
I05.05	01	SYN-
I05.06	01	CLOCK-
I05.07		
I05.08	01	BUSYCPU.2
I05.09	01	BUSYCPU.5
I05.10	01	#BUSYCPU
I05.11	01	BUSYCPU
I05.12	01	BUSYCPU.4
I05.13	01	#BUSYCPU.5
I05.14		
I06.01	06	MS20-27-
I06.02	06	CN+8-
I06.03	06	CN+8-
I06.04	06	CUP
I06.05	06	ALUA7
I06.06	06	#COUNTUP.2
I06.07		
I06.08	11	#ROM3.3-
I06.09	11	MS20-
I06.10	11	Q1
I06.11	11	Q2
I06.12	06	#ALU.7
I06.13	06	DUE-
I06.14		
I07.01	02	ROM21
I07.02	02	T2A
I07.03	02	#TFF-
I07.04	01	ROM22-
I07.05	01	ROM0-
I07.06	01	#T200.2
I07.07		
I07.08	02	#ROM0VROM1
I07.09	02	ROM0-
I07.10	02	ROM1-
I07.11	02	#T1&(ROM0VROM1)-
I07.12	02	ROM0VROM1
I07.13	02	T1
I07.14		
I08.01	11	CR15-
I08.02	11	ROM15.1-
I08.03	11	#ROM15-
I08.04	11	ROM14.1-
I08.05	11	ROM14.1-
I08.06	11	#ROM14-
I08.07		
I08.08	11	#ROM17-

I08.09	11	ROM17.1-
I08.10	11	CR17-
I08.11	01	#WE.3-
I08.12	01	ROM1-
I08.13	01	ROM2-
I08.14		
I09.01	11	ROM13.1-
I09.02	11	ROM13.2-
I09.03	11	#ROM13-
I09.04	11	ROM13.2-
I09.05	11	ROM16.1-
I09.06	11	#ROM16-
I09.07		
I09.08	03	#PREG.4
I09.09	03	LOADP-
I09.10	03	T2-
I09.11	06	#COUNTUP
I09.12	06	COUNTUP.1
I09.13	06	COUNTUP.2
I09.14		
I10.01	08	P4
I10.02	08	B4
I10.03	08	#M04-
I10.04	08	#M05-
I10.05	08	B5
I10.06	08	P5
I10.07	08	PA-
I10.08		
I10.09	08	BA-
I10.10	08	P6
I10.11	08	B6
I10.12	08	#M06-
I10.13	08	#M07-
I10.14	08	B7
I10.15	08	P7
I10.16		
I11.01	08	NR4
I11.02	08	MR4
I11.03	08	#M04-
I11.04	08	#M05-
I11.05	08	MR5
I11.06	08	NR5
I11.07	08	NA-
I11.08		
I11.09	08	MA-
I11.10	08	NR6
I11.11	08	MR6
I11.12	08	#M06-
I11.13	08	#M07-
I11.14	08	MR7
I11.15	08	NR7
I11.16		
I12.01	08	NL4
I12.02	08	ML4
I12.03	08	#M12.1
I12.04	08	#M13.1
I12.05	08	ML5
I12.06	08	NL5
I12.07	08	NA-
I12.08		

I12.09	08	MA-
I12.10	08	NL6
I12.11	08	ML6
I12.12	08	#M14.1
I12.13	08	#M15.1
I12.14	08	ML7
I12.15	08	NL7
I12.16		
I13.01	08	NL0
I13.02	08	ML0
I13.03	08	#M08-
I13.04	08	#M09-
I13.05	08	ML1
I13.06	08	NL1
I13.07	08	NA-
I13.08		
I13.09	08	MA-
I13.10	08	NL2
I13.11	08	ML2
I13.12	08	#M10-
I13.13	08	#M11-
I13.14	08	ML3
I13.15	08	NL3
I13.16		
I14.01	08	NR0
I14.02	08	MR0
I14.03	08	#M00.1
I14.04	08	#M01.1
I14.05	08	MR1
I14.06	08	NR1
I14.07	08	NA-
I14.08		
I14.09	08	MA-
I14.10	08	NR2
I14.11	08	MR2
I14.12	08	#M02.1
I14.13	08	#M03.1
I14.14	08	MR3
I14.15	08	NR3
I14.16		
I15.01	08	P0
I15.02	08	B0
I15.03	08	#M00.1
I15.04	08	#M01.1
I15.05	08	B1
I15.06	08	P1
I15.07	08	PA-
I15.08		
I15.09	08	BA-
I15.10	08	P2
I15.11	08	B2
I15.12	08	#M02.1
I15.13	08	#M03.1
I15.14	08	B3
I15.15	08	P3
I15.16		
I16.01	08	CR10
I16.02	08	DSLEVEL.1
I16.03	08	DSLEVEL.2
I16.04	08	PA-

I16.05	08	BA-
I16.06	08	#DSLEVEL
I16.07		
I16.08	08	#DSLEVEL.1
I16.09	08	MA-
I16.10	08	+Z
I16.11	08	+Z
I16.12	08	#DSLEVEL.2
I16.13	08	DSLEVEL.1
I16.14		
K01.01	01	#QUARZ.3
K01.02	01	#QUARZ.4
K01.03	01	QUARZ.4
K01.04	01	#CLOCK-
K01.05	01	CLOCK-
K01.06	01	#CLOCK*
K01.07		
K01.08	01	#CLOCK*-
K01.09	01	CLOCK*
K01.10	01	QUARZ.2
K01.11	01	QUARZ.1
K01.12		
K01.13		
K01.14		
K02.01	01	SYN.6
K02.02	01	T400*
K02.03	01	#FE-VT400*-
K02.04	01	BUSYCPU*.3
K02.05	01	CLOCK*
K02.06	01	#BUSYCPU*.2
K02.07		
K02.08	01	#BUSYCPU*.1
K02.09	01	BUSYCPU*.2
K02.10	01	SYN.7
K02.11	01	#SYN.7
K02.12	01	FE-VT400*-
K02.13	01	BUSYCPU*.1
K02.14		
K03.01	01	SYN.6
K03.02	01	T1
K03.03	01	#SYN.4
K03.04	09	BUSYCPU*
K03.05	09	RK.1
K03.06	09	#RK
K03.07		
K03.08	01	#BE-
K03.09	01	BUSYCPU*
K03.10	01	+Z
K03.11	01	#SYN.4
K03.12	01	SYN.7
K03.13	01	FE-VT400*-
K03.14		
K04.01		
K04.02		
K04.03		
K04.04		
K04.05	01	#PAUSE
K04.06	01	#PAUSE-
K04.07		
K04.08	01	PAUSE.2

K04.09	01	T2A
K04.10	01	NNA-
K04.11	01	PAUSE.3
K04.12		
K04.13		
K04.14		
K05.01	06	ROM20-
K05.02	06	ALU.2
K05.03	06	CN-
K05.04	04	LSAD1M
K05.05	04	CR10
K05.06	04	#MREG.19
K05.07		
K05.08	11	#ROM13.2-
K05.09	11	LSAD1
K05.10	11	LSAD1
K05.11	01	#BUSYCPU.2
K05.12	01	BUSYCPU.1
K05.13	01	BE*-
K06.01		
K06.02		
K06.03	01	T2-
K06.04	01	#NP.1-
K06.05	01	NP.1-
K06.06	01	#NP.2-
K06.07		
K06.08	01	#SYN-
K06.09	01	SYN.5
K06.10		
K06.11		
K06.12	11	#ROM21
K06.13	11	ROM21.1
K06.14		
K07.01	11	#ROM20-
K07.02	11	#ROM21.1
K07.03	11	#ROM22-
K07.04	11	#ROM23-
K07.05	11	#ROM24-
K07.06	11	#ROM25-
K07.07		
K07.08	11	0V
K07.09	11	#ROM27-
K07.10	11	C0
K07.11	11	C1
K07.12	11	C2
K07.13	11	C3
K07.14	11	C4
K07.15	11	ROMDISABLE
K07.16	11	+Z
K08.01	11	#LOAD.1
K08.02	11	#LOAD.2
K08.03	11	#LOAD.3
K08.04	11	#ROM13.1-
K08.05	11	#ROM14.1-
K08.06	11	#ROM15.1-
K08.07	11	#ROM16.1-
K08.08	11	0V
K08.09	11	#CR17-
K08.10	11	C0
K08.11	11	C1

K08.12	11	C2
K08.13	11	C3
K08.14	11	C4
K08.15	11	ROMDISABLE
K08.16	11	+Z
K09.01	11	#ROM0-
K09.02	11	#ROM1-
K09.03	11	#ROM2-
K09.04	11	#ROM3-
K09.05	11	#ROM4-
K09.06	11	#ROM5.1-
K09.07	11	#ROM6.1-
K09.08	11	0V
K09.09	11	#CR07-
K09.10	11	C0
K09.11	11	C1
K09.12	11	C2
K09.13	11	C3
K09.14	11	C4
K09.15	11	ROMDISABLE
K09.16	11	+Z
K10.01	03	F5
K10.02	03	#P5
K10.03	03	#P4
K10.04	03	PREG.1
K10.05	03	PREG.2
K10.06	03	#P6
K10.07	03	#P7
K10.08		
K10.09	03	F7
K10.10	03	F6
K10.11	03	PREG.4
K10.12		
K10.13		
K10.14	03	PREG.3
K10.15	03	F4
K10.16		
K11.01	04	NBM-
K11.02	04	T2-
K11.03	04	F4
K11.04	04	F5
K11.05	04	F6
K11.06	04	F7
K11.07	04	MREG.1
K11.08		
K11.09	04	MREG.6
K11.10	04	MREG.1
K11.11	04	#MR7
K11.12	04	#MR6
K11.13	04	#MR5
K11.14	04	#MR4
K11.15	04	MREG.12
K11.16		
K12.01	04	F5
K12.02	04	#ML5
K12.03	04	#ML4
K12.04	04	MREG.13
K12.05	04	MREG.14
K12.06	04	#ML6
K12.07	04	#ML7
K12.08		
K12.09	04	F7
K12.10	04	F6
K12.11	04	MREG.15
K12.12		
K12.13		
K12.14	04	MREG.21
K12.15	04	F4
K12.16		
K13.01	04	F1
K13.02	04	#ML1
K13.03	04	#ML0
K13.04	04	MREG.11
K13.05	04	MREG.10
K13.06	04	#ML2
K13.07	04	#ML3
K13.08		
K13.09	04	F3
K13.10	04	F2
K13.11	04	MREG.15
K13.12	04	MREG.14
K13.13	04	MREG.13
K13.14	04	MREG.21
K13.15	04	F0
K13.16		
K14.01	04	NBM-
K14.02	04	T2
K14.03	04	F0
K14.04	04	F1
K14.05	04	F2
K14.06	04	F3
K14.07	04	MREG.2
K14.08		
K14.09	04	MREG.6
K14.10	04	MREG.2
K14.11	04	#MR3
K14.12	04	#MR2
K14.13	04	#MR1
K14.14	04	#MR0
K14.15	04	MREG.1
K14.16		
K15.01	03	F1
K15.02	03	#P1
K15.03	03	#P0
K15.04	03	COUNTDOWNP&T2-
K15.05	03	COUNTUPP&T2-
K15.06	03	#P2
K15.07	03	#P3
K15.08		
K15.09	03	F3
K15.10	03	F2
K15.11	03	PREG.4
K15.12	03	PREG.2
K15.13	03	PREG.1
K15.14	03	PREG.3
K15.15	03	F0
K15.16		
K16.01	08	#PA-
K16.02	08	#BA-
K16.03	08	#NA-
K16.04	08	#MA-
K16.12	08	0V
K16.13	08	0V
K16.14	08	ROM4-
K16.15	08	ROM3-
KL0104	10	MS20-
KL0105	10	MS18-
KL0106	10	#SPRUNG-
KL0108	06	#ALU.8
KL0109	06	ALU.9
KL0110	06	ALU.10
KL0111	09	#RK*-
KL0112	09	RK.1
KL0113	09	BUSYCPU*
L01.01	11	PROGR&PAUSE-
L01.02	11	ROMDISABLE.1
L01.03	11	#ROMDISABLE
L01.04	10	MS.5-
L01.05	10	PROGR&PAUSE-
L01.06	10	#MS00-07-
L01.08	10	#MS.1-
L01.09	10	C3
L01.10	10	C4
L01.11	10	#MS20-27-
L01.12	10	MS.2-
L01.13	10	MS.3-
L02.01	11	#PROGR&PAUSE-
L02.02	11	PAUSE
L02.03	11	PROGR-
L02.04	10	#MS.5-
L02.05	10	MS.2-
L02.06	10	C3
L02.08	10	0V
L02.09	10	C3
L02.10	10	#MS.3-
L02.11	04	MA-
L02.12	04	MREG.5
L02.13	04	#MREG.4
L03.01	11	Q0
L03.02	11	MS01-
L03.03	11	#ROMDISABLE.1
L03.04	11	R25*
L03.05	11	ROM25-
L03.06	11	#R25
L03.08	10	#MS.4-
L03.09	10	MS.3-
L03.10	10	MS.2-
L03.11	04	#MREG.2
LO3.12	04	MREG.3
L03.13	04	MREG.4
L04.01	10	LOADD-
L04.02	10	#LOADD
L04.03	10	MS.5-
L04.04	10	#MS00-07*-
L04.05	09	ROM2-
L04.06	09	#RK.1
L04.08	10	#DUE.1
L04.09	10	DREG.1
L04.10	09	#SKAN.1
L04.11	09	BUSYCPU*
L04.12	10	#DO-
L04.13	10	DO.1-
L05.01	10	LOADD-
L05.02	10	DOF-
L05.03	10	#DO.1-
L05.04	10	IREG-
L05.05	10	DOF
L05.06	10	#IREG-VDOF
L05.08	10	#DOF.1
L05.09	10	DREG.1
L05.10	10	DOF.2
L05.11	10	#DOF.2
L05.12	10	LOADQ-
L05.13	10	DOF.3
L06.01	10	T2A
L06.02	10	DOF-
L06.03	10	DREG.3
L06.04	10	T2A
L06.05	10	DOF
L06.06	10	#DREG.4
L06.08	10	#QREG.3
L06.09	10	END
L06.10	10	T2A
L06.11	10	DO-
L06.12	10	#DREG.1
L06.13	10	LOADD
L07.01	11	#LOADB-
L07.02	11	#LOADP-
L07.03	11	#LOADML-
L07.04	11	#LOADMR-
L07.05	11	#LOADNL-
L07.06	11	#LOADNR-
L07.07	11	#L0ADQ-
L07.08	11	0V
L07.09	11	#LOADD-
L07.12	11	R25-
L07.13	11	LOAD.3
L07.14	11	LOAD.2
L07.15	11	LOAD.1
L07.16	11	+Z
L08.01	11	ROM17.3-
L08.02	11	ROM17.2-
L08.03	11	#ROM.1-
L08.04	04	MREG.17
L08.05	04	MREG.16
L08.06	04	#MREG.15
L08.08	04	#MREG.15
L08.09	04	MREG.19
L08.10	04	T1
L08.11	11	#ROM17.1-
L08.12	11	ROM17.2-
L08.13	11	ROM17.3-
L09.01	08	ROM2-
L09.02	08	ROM0-
L09.03	08	#BCP.1-
L09.04	06	MS01-
L09.05	06	DUE
L09.06	06	#ALU.9
L10.01	03	NBM-
L10.02	03	T2-

L10.03	03	F4
L10.04	03	F5
L10.05	03	F6
L10.06	03	F7
L10.07	03	BREG.1
L10.09	03	LOADB-
L10.10	03	BREG.1
L10.11	03	#B7
L10.12	03	#B6
L10.13	03	#B5
L10.14	03	#B4
L11.01	05	NNA-
L11.02	05	T2-
L11.03	05	F4
L11.04	05	F5
L11.05	05	F6
L11.06	05	F7
L11.07	05	NREG.14
L11.09	05	NREG.13
L11.10	05	NREG.14
L11.11	05	#NR7
L11.12	05	#NR6
L11.13	05	#NR5
L11.14	05	#NR4
L11.15	05	NREG.12
L12.01	05	NREG.5
L12.02	05	#NL5
L12.03	05	#NL4
L12.04	05	NREG.7
L12.05	05	NREG.6
L12.06	05	#NL6
L12.07	05	#NL7
L12.09	05	F7
L12.10	05	NREG.4
L12.11	05	NREG.2
L12.14	05	NREG.8
L12.15	05	F4
L13.01	05	F1
L13.02	05	#NL1
L13.03	05	#NL0
L13.04	05	NREG.11
L13.05	05	NREG.10
L13.06	05	#NL2
L13.07	05	#NL3
L13.09	05	F4
L13.10	05	F2
L13.11	05	NREG.3
L13.12	05	NREG.6
L13.13	05	NREG.7
L13.14	05	NREG.8
L13.15	05	F0
L14.01	05	NNA-
L14.02	05	T2-
L14.03	05	F0
L14.04	05	F1
L14.05	05	F2
L14.06	05	F3
L14.07	05	NREG.15
L14.09	05	NREG.13
L14.10	05	NREG.15
L14.11	05	#NR3
L14.12	05	#NR2
L14.13	05	#NR1
L14.14	05	#NR0
L14.15	05	NREG.14
L15.01	03	NBM-
L15.02	03	T2-
L15.03	03	F0
L15.04	03	F1
L15.05	03	F2
L15.06	03	F3
L15.07	03	MS05
L15.09	03	LOADB-
L15.10	03	MS05
L15.11	03	#B3
L15.12	03	#B2
L15.13	03	#B1
L15.14	03	#B0
L15.15	03	BREG.1
L16.11	04	#MREG.18
L16.12	04	T2-
L16.13	04	+Z
M01.01	10	#MS30-
M01.02	10	#MS31-
M01.03	10	#MS32-
M01.04	10	#MS33-
M01.05	10	#MS34-
M01.06	10	#MS35-
M01.07	10	#MS36-
M01.09	10	#MS37-
M01.12	10	MS.1-
M01.13	10	C2
M01.14	10	C1
M01.15	10	C0
M02.01	10	#MS20-
M02.02	10	#MS21-
M02.03	10	#MS22-
M02.04	10	#MS23-
M02.05	10	#MS24-
M02.06	10	#MS25-
M02.07	10	#MS26-
M02.09	10	#MS27-
M02.12	10	MS20-27-
M02.13	10	C2
M02.14	10	C1
M02.15	10	C0
M03.01	10	#MS10-
M03.02	10	#MS11-
M03.03	10	#MS12-
M03.04	10	#MS13-
M03.05	10	#MS14-
M03.06	10	#MS15-
M03.07	10	#MS16-
M03.09	10	#MS17-
M03.12	10	MS.4-
M03.13	10	C2
M03.14	10	C1
M03.15	10	C0
M04.01	10	#MS00-
M04.02	10	#MS01-
M04.03	10	#MS02-
M04.04	10	#MS03-
M04.05	10	#MS04-
M04.06	10	#MS05-
M04.07	10	#MS06-
M04.09	10	#MS07-
M04.12	10	MS00-07-
M04.13	10	C2
M04.14	10	C1
M04.15	10	C0
M05.01	10	LOADD
M05.02	10	#DOF-
M05.03	10	#DOF
M05.04	10	DOF
M05.06	10	#IREG-
M05.08	10	Q3
M05.09	10	DUE.1
M05.10	10	QREG.2
M05.11	10	DOF
M05.12	10	DOF.1
M05.13	10	QREG.2
M06.01	10	Q1
M06.02	10	#DUE-
M06.03	10	#DUE
M06.04	10	0V
M06.05	10	#IOPE
M06.06	10	#NIOP.1
M06.08	10	Q2
M06.09	10	DUE.1
M06.10	10	QREG.2
M06.11	10	DOF
M06.12	10	DUE.1
M06.13	10	QREG.2
M07.01	05	LOADNL-
M07.02	05	SWNL-
M07.03	05	#NREG.1
M07.04	04	LOADML-
M07.05	04	SWML-
M07.06	04	#MREG.16
M07.08	04	#MREG.5
M07.09	04	IOPE
M07.10	04	MS00-07*-
M07.11	05	#NREG.3
M07.12	05	NREG.1
M07.13	05	T2
M08.01	11	MS15
M08.02	11	Q2
M08.03	11	#GETLEVEL
M08.04	10	QREG.3
M08.05	10	NNA-
M08.06	10	#QREG.2
M08.08	10	#NIOP
M08.09	10	NIOP.1
M08.10	10	DOF
M08.11	05	#NREG.17
M08.12	05	NIOP
M08.13	05	MS00-07-
M09.01	11	#ROM17.2-
M09.02	11	MS02-
M09.03	11	LSAD1
M09.04	09	#SKAN.2
M09.05	09	SKAN.1
M09.06	09	ROM0-
M09.08	10	0V
M09.09	10	MS15-
M09.10	10	#MS15
M09.11	04	MREG.18
M09.12	04	T2-
M09.13	04	#MREG.17
M10.01	03	T2A
M10.02	03	COUNTDOWNP&T2.1-
M10.03	03	#COUNTDOWNP&T2-
M10.08	11	#CR05-
M10.09	11	MS15
M10.10	11	Q2
M10.11	03	#COUNTUPP&T2-
M10.12	03	T2A
M10.13	03	COUNTUPP&T2.3-
M11.01	03	#COUNTUPP&T2.3-
M11.02	03	COUNTUPP&T2.2-
M11.03	03	COUNTDOWNP&T2.1-
M11.04	05	#NREG.16
M11.05	05	NREG.17
M11.06	05	NA-
M11.08	04	MS30
M11.09	04	T2-
M11.10	04	#MREG.7
M11.11	05	T2-
M11.12	05	MS30-
M11.13	05	#NREG.9
M12.01	05	NREG.12
M12.02	05	T2A
M12.03	05	#NREG.10
M12.04	04	T2A
M12.05	04	MREG.12
M12.06	04	#MREG.10
M12.08	04	#MREG.10
M12.09	04	COUNTUP
M12.10	04	MREG.9
M12.11	05	#NREG.10
M12.12	05	COUNTUP
M12.13	05	NREG.9
M13.01	05	COUNTDOWN
M13.02	05	NREG.9
M13.03	05	#NREG.11
M13.04	04	COUNTDOWN
M13.05	04	MREG.9
M13.06	04	#MREG.11
M13.08	05	#NREG.5
M13.09	05	5-
M13.10	05	LDNL.2
M13.11	05	#NREG.4
M13.12	05	LDNL.1
M13.13	05	6-
M14.01	04	NBM-
M14.02	04	#MREG.21
M14.03	05	NNA-
M14.04	05	#NREG.8
M14.05	03	PA-
M14.06	03	#COUNTUPP&T2.1-

M14.12	03	#PREG.3
M14.13	03	NP-
M15.01	04	LOADMR-
M15.02	04	SWMR-
M15.03	04	#MREG.6
M15.04	05	NREG.16
M15.05	05	NREG.13
M15.06	05	#NREG.15
M15.08	05	#NREG.13
M15.09	05	SWNR-
M15.10	05	LOADNR-
M15.11	05	#NREG.2
M15.12	05	LDNL-
M15.13	05	NREG.3
M16.03	03	IREGVDOF-
M16.04	03	ROM24-
M16.05	03	COUNTUPP&T2.1-
M16.06	03	#COUNTUPP&T2.2-
100A08	09	D7-
100A10	09	D6-
100A11	09	D5-
100A13	09	D4-
100A14	09	D3-
100A16	09	D2-
100A17	09	D1-
100A18	09	D0-
100A20	08	A00-
100A21	08	A01-
100A23	08	A02-
100A24	08	A03-
100A25	09	RK
100A27	01	N-
100A29	08	IFT-
100A30	08	ISLL-
100A31	08	IRMLL-
100C10	08	SXY-
100C20	08	A00-
100C21	08	A01-
100C23	08	A02-
100C24	02	A03-
100C27	01	N-
100C29	08	IFT-
100C30	08	ISLL-
100C31	08	IRMLL-
101A08	09	D7-
101A10	09	D6-
101A11	09	D5-
101A13	09	D4-
101A14	09	D3-
101A16	09	D2-
101A17	09	D1-
101A18	09	D0-
101A20	08	A00-
101A21	08	A01-
101A23	08	A02-
101A24	08	A03-
101A25	09	RK
101A27	01	N-
101A29	08	IFT-
101A30	08	ISTTY-
101A31	08	IRMTTY-
101C20	08	A00-
101C21	08	A01-
101C23	08	A02-
101C24	08	A03-
101C27	01	N-
101C29	08	IFT-
101C30	08	ISTTY-
101C31	08	IRMTTY-
102A10	09	D7-
102A11	09	D6-
102A12	09	D5-
102A13	09	D4-
102A14	09	D3-
102A15	09	D2-
102A16	09	D1-
102A17	09	D0-
103A05	01	ANF05-
103A19	01	N-
103A24	07	LEVEL1
103A25	07	LEVEL2
103A26	07	LEVEL4
103A27	07	LEVEL8
103A28	07	ICL
103A29	07	IN
103A30	07	IP
103A31	07	IWD
103C02	09	F0
103C03	09	F1
103C04	09	F2
103C05	09	F3
103C10	08	S00-
103C26	08	DSLEVEL
103C27	01	ANF34-
103C30	10	DO-
103C31	11	GETLEVEL
104A10	09	D7-
104A11	09	D6-
104A12	09	D5-
104A13	09	D4-
104A14	09	D3-
104A15	09	D2-
104A16	09	D1-
104A17	09	D0-
104C10	11	PROGR&PAUSE-
104C12	01	HLT-
104C16	01	N-
104C19	01	T400*
105A10	06	Q6-
105A11	11	CON
105A12	10	C1
105A13	10	C3
105A14	10	C0
105A16	10	C4
105A17	10	DOF-
105A18	11	R25*
105A23	10	DOF
105A24	10	END
105A27	06	A=B
105A29	10	C2
105A31	06	ALU.11
105C19	08	CR10
105C21	05	MS30-
105C30	10	SPRUNG-
202A02	01	BE-
202A03	01	FE-
202A07	09	RK
202A10	08	A15-
202A11	08	A14-
202A12	08	A13-
202A13	08	A12-
202A14	08	A11-
202A15	08	A10-
202A16	08	A09-
202A17	08	A08-
202A18	08	A07-
202A19	08	A06-
202A20	08	A05-
202A21	08	A04-
202A22	08	A03-
202A23	08	A02-
202A24	08	A01-
202A25	08	A00-
202C02	01	GE-
203C02	08	M11-
203C03	08	M10-
203C04	08	M09-
203C05	08	M08-
203C06	08	M07-
203C07	08	M06-
203C08	08	M05-
203C09	08	M04-
203C27	05	LDNL-
203C30	05	NL6VNL5
204A03	09	RK
204A10	08	A15-
204A11	08	A14-
204A12	08	A13-
204A13	08	A12-
204A14	08	A11-
204A15	08	A10-
204A16	08	A09-
204A17	08	A08-
204A18	08	A07-
204A19	08	A06-
204A20	08	A05-
204A21	08	A04-
204A22	08	A03-
204A23	08	A02-
204A24	08	A01-
204A25	08	A00-
204C03	01	FE-
205A03	11	ROM27-
205A05	11	ROM23-
205A06	11	ROM17.3-
205A11	11	T1
205A14	10	MARK-
205A15	03	B0
205A22	04	MS30
205A23	03	COUNTUPP&T2-
205A24	03	MS05
300A03	09	7
300A04	09	6
300A05	09	5
300A06	09	4
300A07	09	3
300A08	09	2
300A09	09	1
300A10	09	0
300A12	01	PAUSE-
300A14	01	HLT-
300A15	11	ROM0-
300A16	11	ROM2-
300A19	04	CM-
300A21	01	GO-
300A22	11	CR15-
300A23	11	CR17-
300A25	05	NR3
300A26	05	NR2
300A27	05	NR1
300A28	05	NR0
300B03	07	SWITCH7
300B04	07	SWITCH6
300B05	07	SWITCH5
300B06	07	SWITCH4
300B07	07	SWITCH3
300B08	07	SWITCH2
300B09	07	SWITCH1
300B10	07	SWITCH0
300B11	05	SWNL-
300B13	04	LOADML-
300B14	04	SWMR-
300B15	11	CR05-
300B16	11	CR06-
300B17	11	CR07-
300B18	01	N-
300B19	08	BOOTSTRAP-
300B21	09	S0
300B22	09	S1
300B23	09	S2
300B24	09	S3
300B25	09	S4
300B26	09	S5
300B27	09	S6
300B28	09	S7
301A03	01	CLOCK-
301A07	01	FE-
301A10	08	A00-
301A11	08	A01-
301A12	08	A02-
301A13	08	A03-
301A14	08	A04-
301A15	08	A05-
301A16	08	A06-
301A17	08	A07-
301A18	08	A08-
301A19	08	A09-
301A20	08	A10-
301A21	08	A11-
301A22	08	A12-

```
301A23    08    A13-
301A24    08    A14-
301A25    08    A15-
301A27    09    RK
301A31    01    N-
302C02    01    WE-
302C04    09    6-
302C05    09    7-
302C06    09    4-
302C07    09    5-
302C08    09    2-
302C09    09    3-
302C10    09    0-
302C11    09    1-
302C12    09    S7
302C13    09    S6
302C14    09    S5
302C15    09    S4
302C16    09    S3
302C17    09    S2
302C18    09    S1
302C19    09    S0
302C20    08    M00-
302C21    08    M01-
302C22    08    M02-
302C23    08    M03-
302C24    08    M04-
302C25    08    M05-
302C26    08    M06-
302C27    08    M07-
302C28    08    MR11**
302C29    08    M10-
302C30    08    M09-
302C31    08    M08-
303C02    01    WE-
303C04    09    6-
303C05    09    7-
303C06    09    4-
303C07    09    5-
303C08    09    2-
303C09    09    3-
303C10    09    1-
303C11    09    2-
303C12    09    S7
303C13    09    S6
303C14    09    S5
303C15    09    S4
303C16    09    S3
303C17    09    S2
303C18    09    S1
303C19    09    S0
303C20    08    M00-
303C21    08    M01-
303C22    08    M02-
303C23    08    M03-
303C24    08    M04-
303C25    08    M05-
303C26    08    M06-
303C27    08    M07-
303C28    08    MR11*
303C29    08    M10-
303C30    08    M09-
303C31    08    M08-

ANZAHL DER ZEILEN= 1983

*READY
```

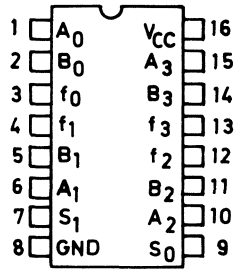
IC-Katalog

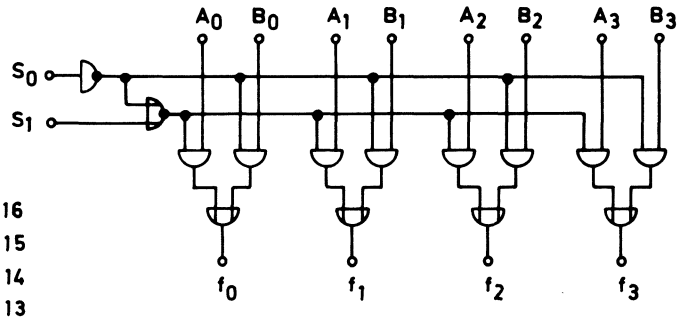
Folgende IC-Typen sind in diesem Katalog aufgeführt:

		Anzahl der Eingänge je Gatter	offener Kollektor
NE 555			
N 8233	4-Bit-Multiplexer		
N 8234	4-Bit-Multiplexer		
9318	8-bit-Prioritätsentkoder		
9324	5-bit-Vergleicher		
SN 4931	2 x NAND	5	
SN 49700	2 x NAND	2	
	2 x Leistungsgatter	2	
SN 7400	4 x NAND	2	
SN 7402	4 x NOR	2	
SN 7403	4 x NAND	2	x
SN 74S03	4 x NAND	2	x
SN 7404	6 x Inverter	1	
SN 7405	6 x Inverter	1	x
SN 7406	6 x Inverter	1	x
SN 7408	4 x AND	2	
SN 7409	4 x AND	2	x
SN 7410	3 x NAND	3	
SN 74510	3 x NAND	3	
SN 7412	3 x NAND	3	x
SN 7413	2 x Schmitt-Trigger		
SN 7416	6 x Inverter	1	x
SN 7417	6 x Treiberstufe	1	x
SN 7420	2 x NAND	4	
SN 7425	2 x NOR	4	
SN 7427	3 x NOR	3	
SN 7432	4 x OR	2	
SN 7437	4 x NAND	2	
SN 7438	4 x NAND	2	x

		Anzahl der Eingänge je Gatter	offerner Kollektor
SN 7442	BCD zu Dezimal-Decoder		
SN 7470	J-K-Flip-Flop		
SN 7474	2 x D-Flip-Flop		
SN 74H74	2 x D-Flip-Flop		
SN 7486	4 x Exklusiv OR	2	
SN 7488	256 Bit-ROM		
SN 7490	Dezimalzähler		
SN 74107	2 x J-K-MS-Flip-Flop		
SN 74109	2 x J-$\overline{K}$ -Flip-Flop		
SN 74118	6 x Flip-Flop ungetaktet gemeins. Reset		
SN 74119	6 x Flip-Flop ungetaktet indiv. Reset		
SN 74121	Monost. Multivibrator		
SN 74123	2 x Monost. Multivibrator		
SN 74132	4 x Schmitt-Trigger		
SN 74151	8 zu 1 Multiplexer		
SN 74154	1 zu 16 Demultiplexer		
SN 74161	asynchroner Zähler		
SN 74174	6 x Flip-Flop getaktet		
SN 74175	4 x Flip-Flop getaktet		
SN 74181	4 Bit-Recheneinheit		
SN 74193	Vor-Rück-Binär-Zähler synchron		
SN 74198	8 Bit Schieberegister rechts/links		
SN 74202	256 x 1 Bit-RAM		
SN 75150	Line receiver		
SN 75154	Line driver		
SN 75451	Leistungstreiber		

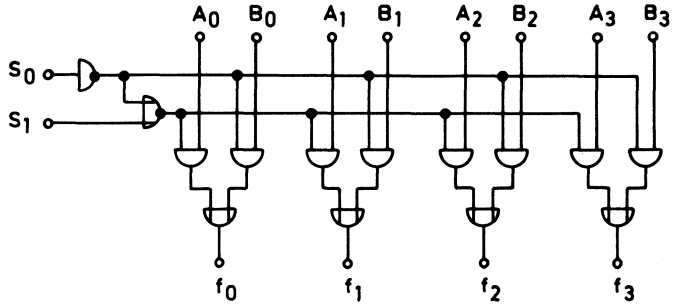
8233





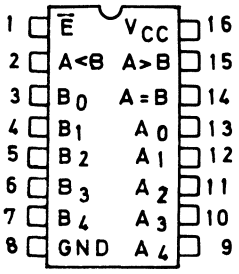
S_0	S_1	f_n
L	L	B
H	L	A
L	H	B
H	H	L

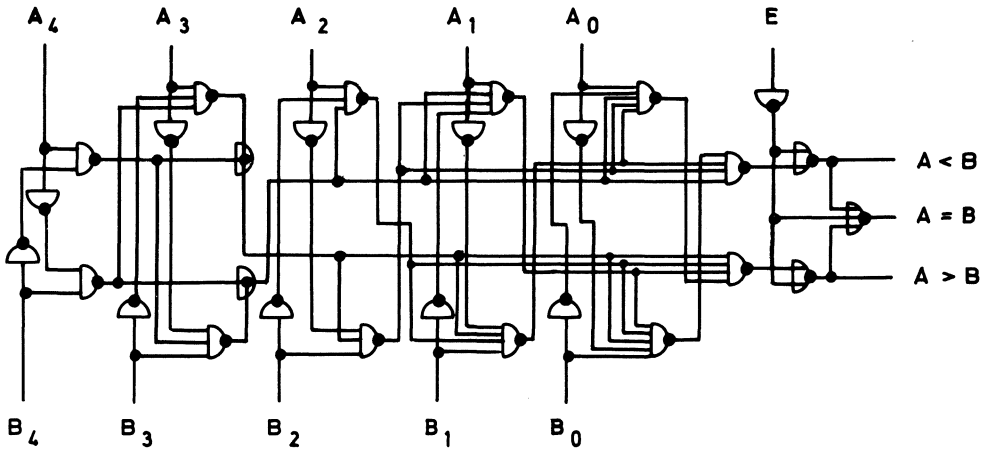
8234



S_0	S_1	f_n
L	L	$\overline{B}$
H	L	$\overline{A}$
L	H	$\overline{B}$
H	H	L

9324



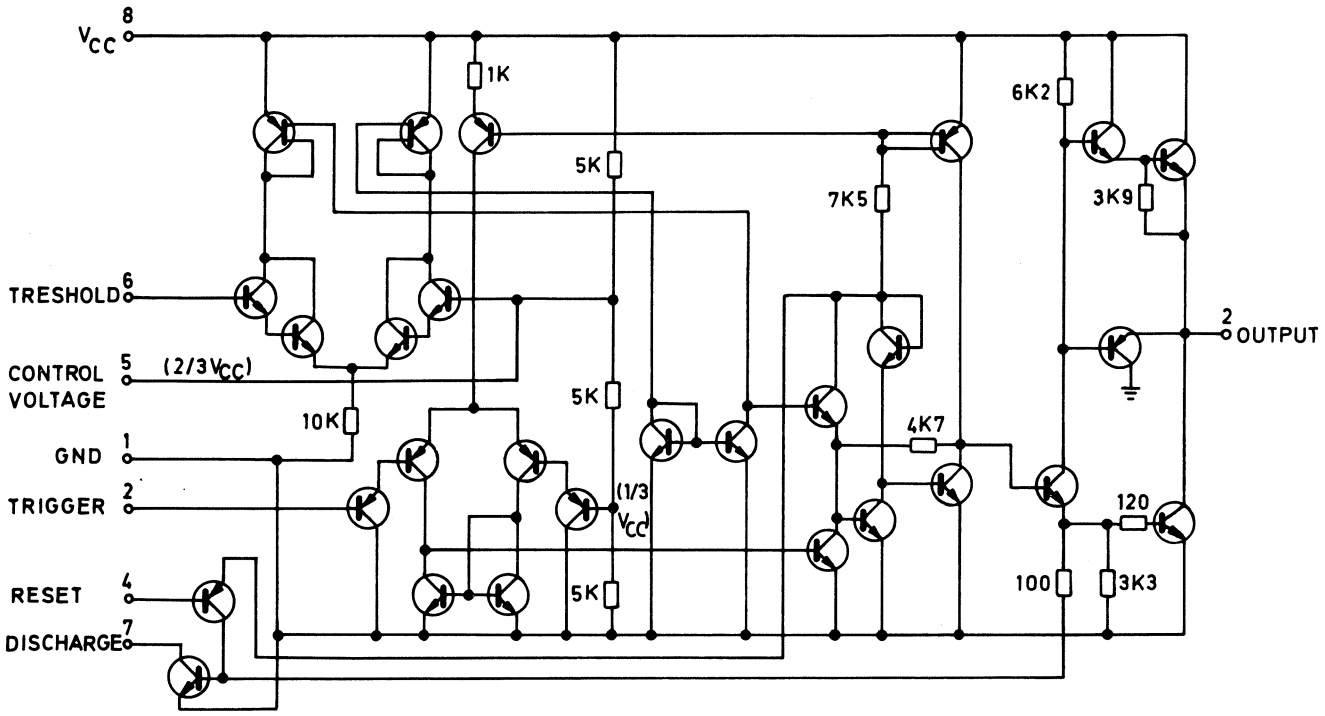


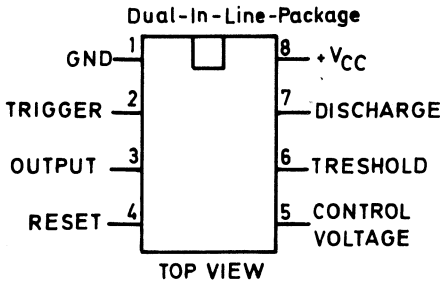
E	A	B	A < B	A > B	A = B
H	X	X	L	L	L
L	Word = A	Word = B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B >	Word A	H	L	L

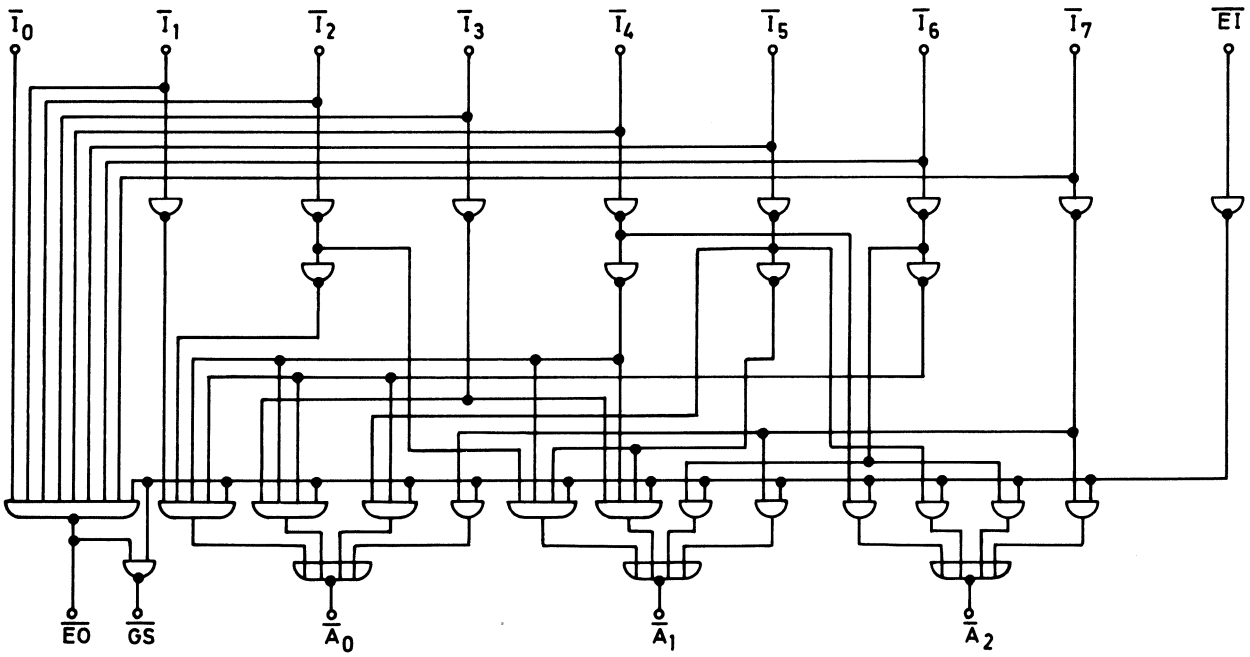
H = HIGH Voltage Level

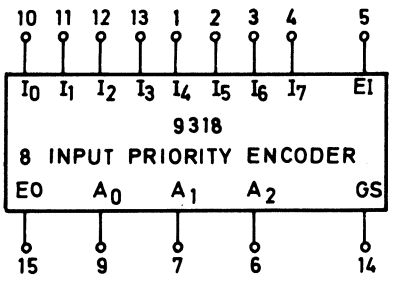
L = LOW Voltage Level

X = Either HIGH or LOW Voltage Level





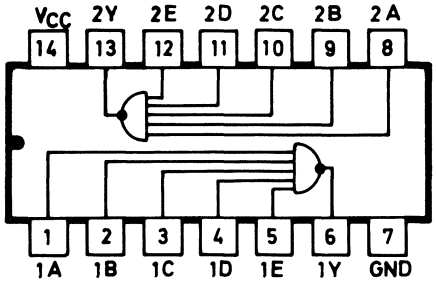




V_{CC} = PIN 16
GND = PIN 8

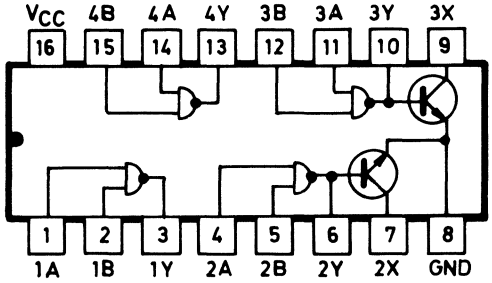
9318

SN 4931



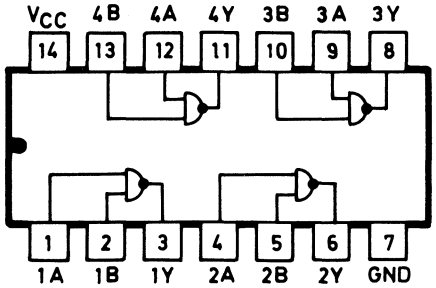
positive logic: $Y = \overline{ABCDE}$

SN 49700



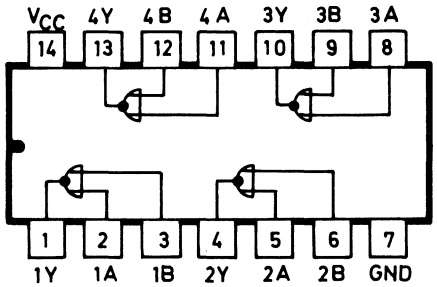
Anschlüsse 2Y und 3Y nicht für Logiksteuerung weiter verwenden

SN 7400



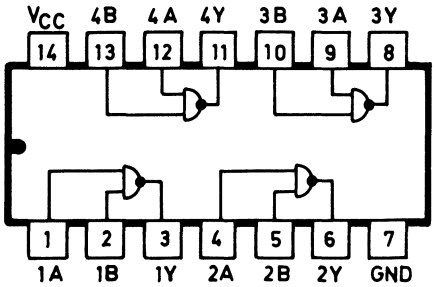
positive logic: $Y = \overline{AB}$

SN 7402



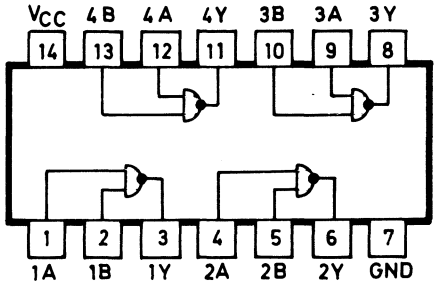
positive logic: $Y = \overline{A+B}$

SN 7403



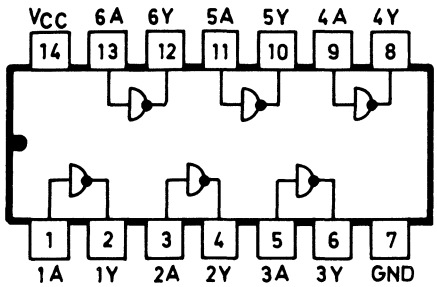
positive logic: $Y = \overline{AB}$

SN 74S03



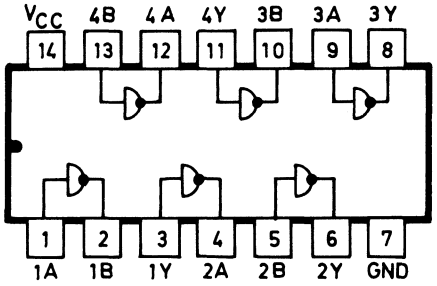
positive logic: $Y = \overline{AB}$

SN 7404



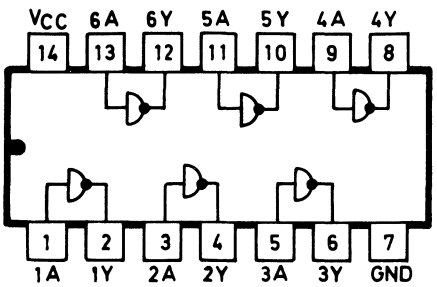
positive logic: $Y = \overline{A}$

SN 7405



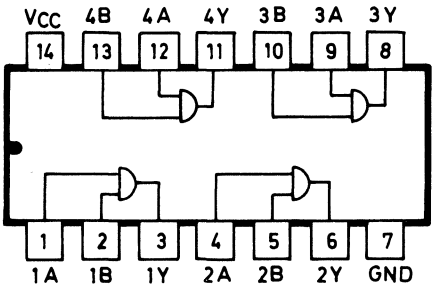
positive logic: $Y = \overline{A}$

SN 7406



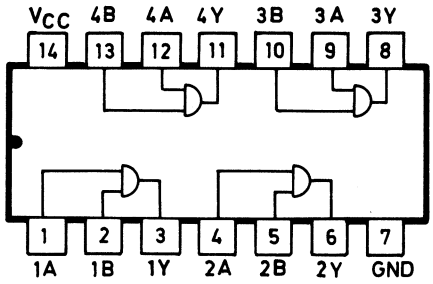
positive logic: $Y = \overline{A}$

SN 7408



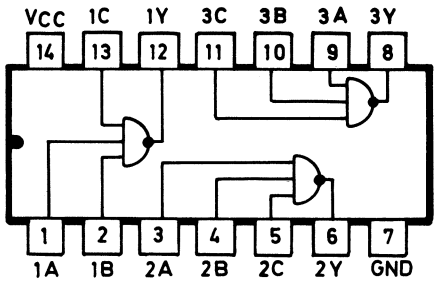
positive logic $Y = AB$

SN7409



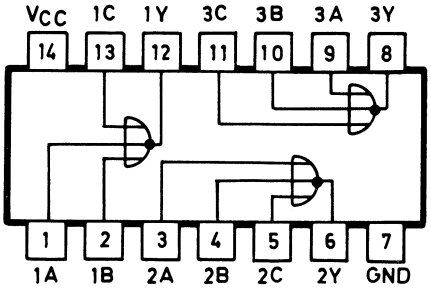
positive logic: $Y = AB$

SN7410

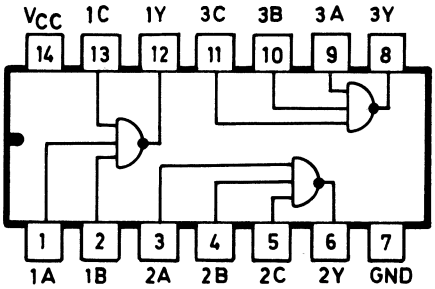


positive logic: $Y = \overline{ABC}$

SN74S10

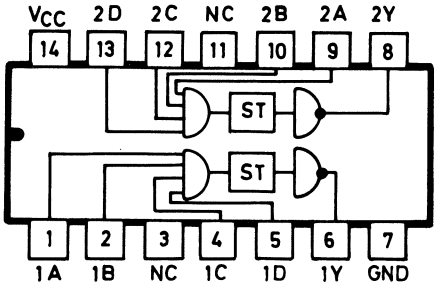


SN 7412



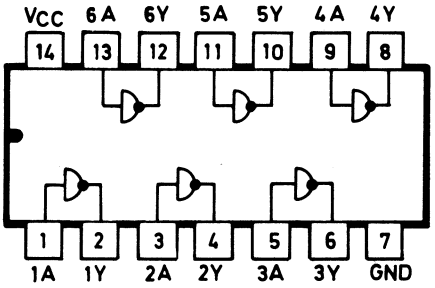
positive logic: $Y = \overline{ABC}$

SN7413



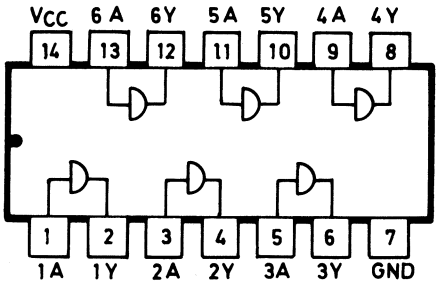
positive logic: $Y = \overline{ABCD}$

SN7416



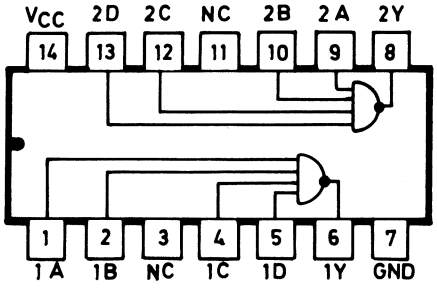
positive logic: $Y = \overline{A}$

SN7417



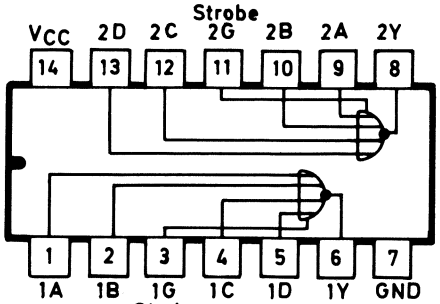
positive logic: $Y = A$

SN7420



positive logic: $Y = \overline{ABCD}$

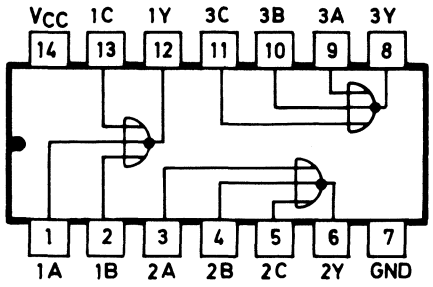
SN7425



positive logic: $Y = \overline{G(A+B+C+D)}$

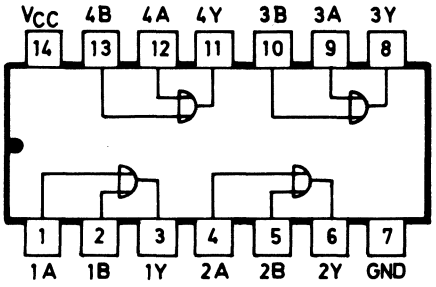
Inputs					Output
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

SN 7427



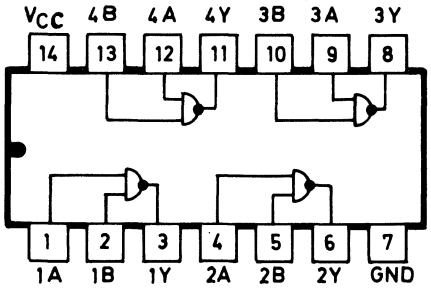
positive logic: $Y = \overline{A+B+C}$

SN 7432



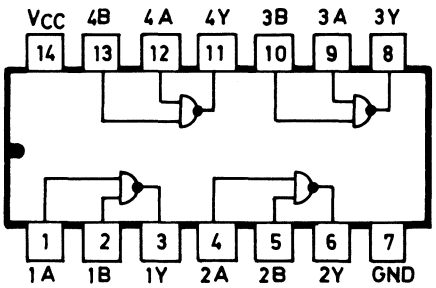
positive logic: $Y = A+B$

SN 7437



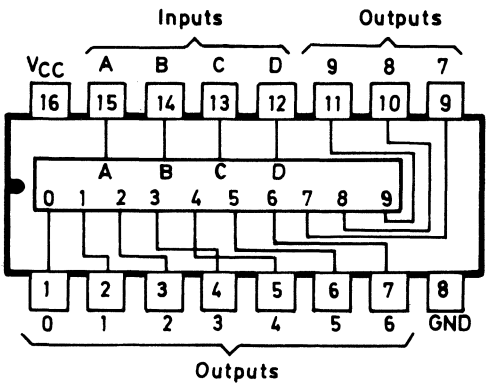
positive logic: $Y = \overline{AB}$

SN 7438



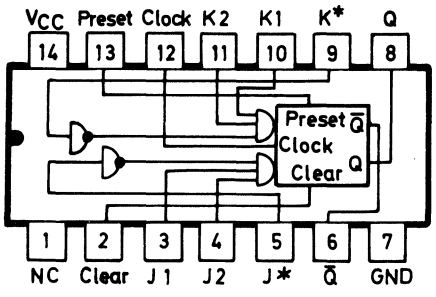
positive logic: $Y = \overline{AB}$

SN 7442



BCD Input				All Types decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

SN 7470

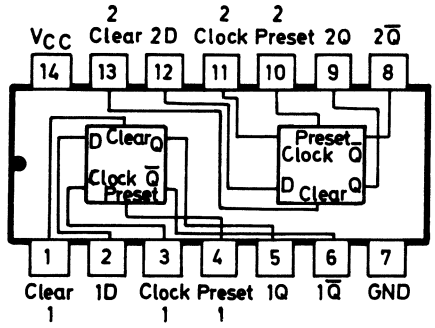


t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

Notes:

1. $J = J1 \cdot J2 \cdot \overline{J}^*$
2. $K = K1 \cdot K2 \cdot \overline{K}^*$
3. t_n = Bit time before clock pulse
4. $t_n + 1$ = Bit time after clock pulse
5. If inputs J^* oder K^* are not used they must be grounded

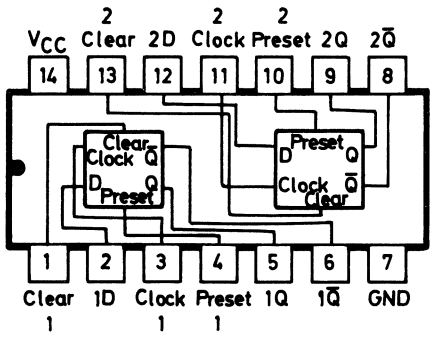
SN7474



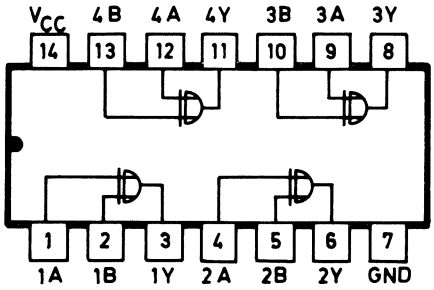
(Each Flip-Flop)

t_n	$t_n + 1$	
Input	Output	Output
D	Q	$\overline{Q}$
L	L	H
H	H	L

SN 74H74



SN 7486

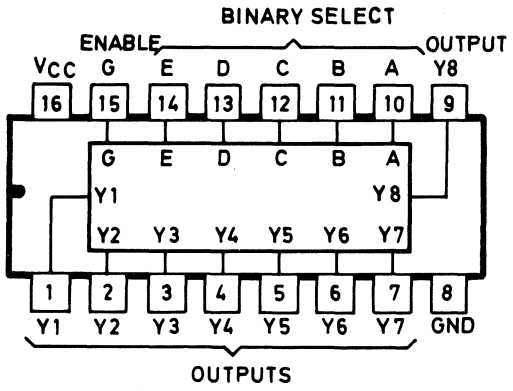


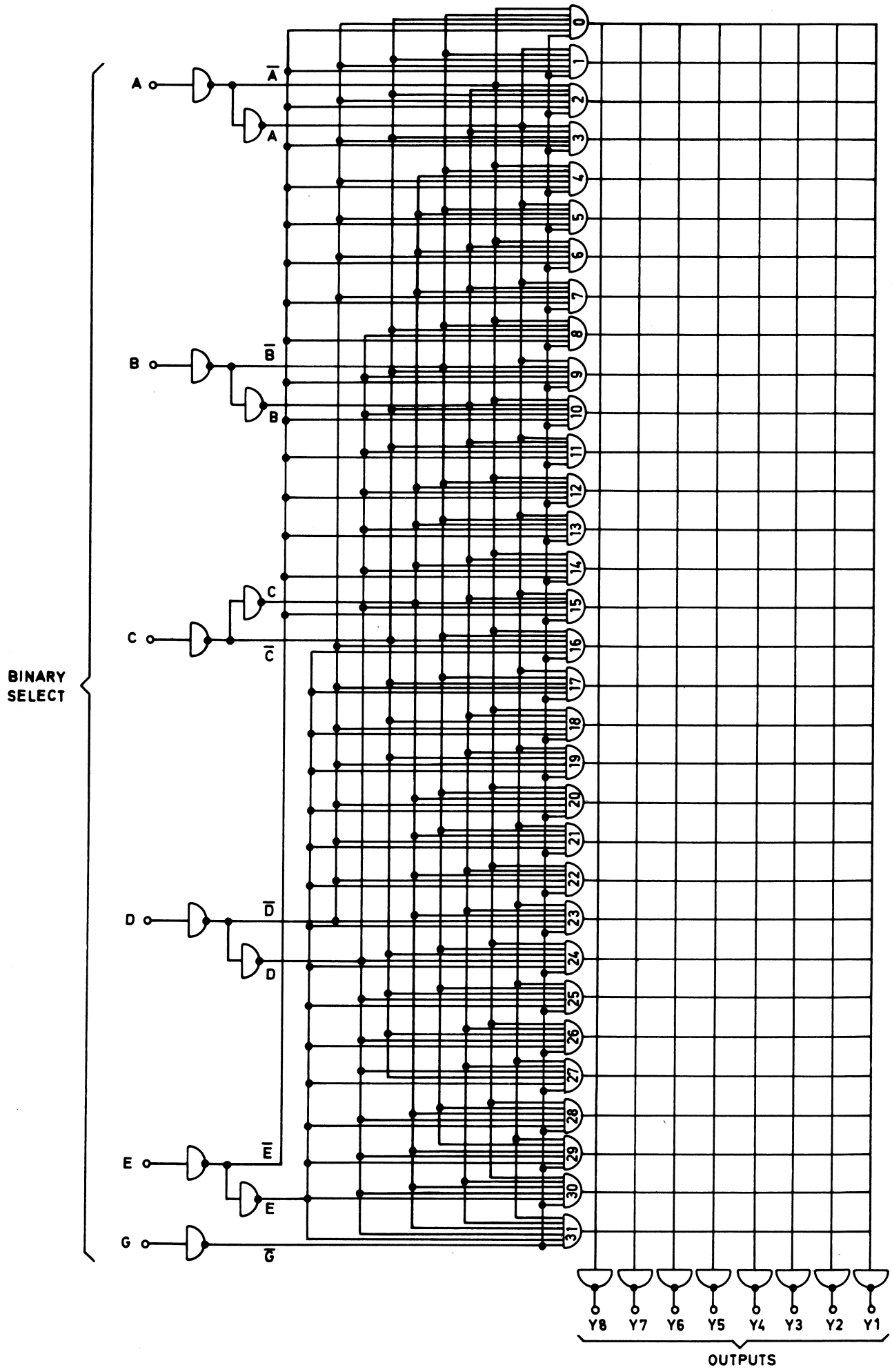
positive logic : $Y = A \bullet B$

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

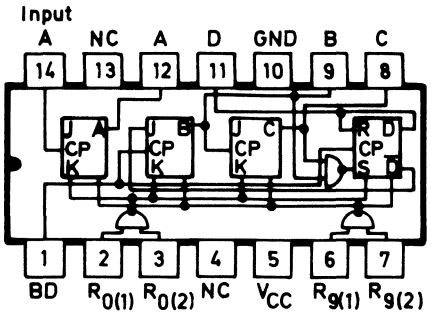
WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	L	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant




A
$\overline{A}$
A
B
$\overline{B}$
B
C
C
$\overline{C}$
D
$\overline{D}$
D
E
$\overline{E}$
E
G
$\overline{G}$
BINARY SELECT
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
OUTPUTS

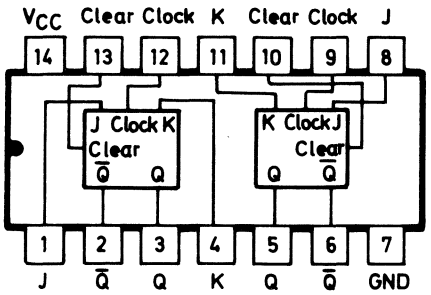
SN 7490



Reset / Count

Reset inputs				output			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

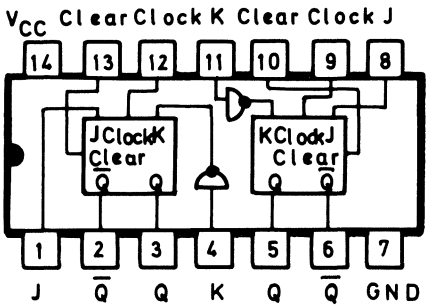
SN 74107



(Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

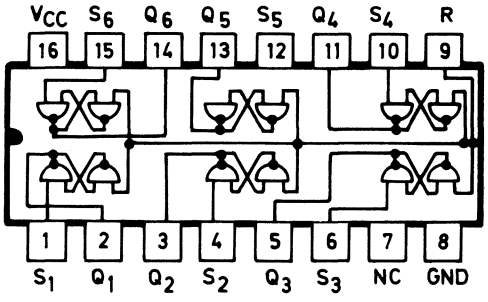
SN 74109



(Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
L	H	Q_n
L	L	L
H	H	H
H	L	$\overline{Q_n}$

SN 74118

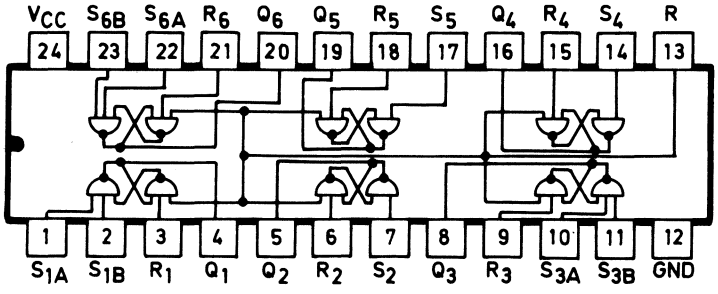


(each latch)

S	Reset	Q
L	X	H
H	L	L
H	H	Store

Notes:
1. X indicates input may be logical H or L
2. Reset is common to all latches

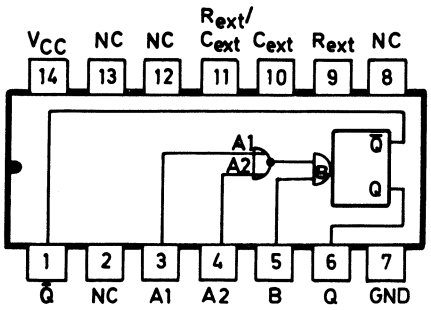
SN 74119



(each latch)

SA	SB	R	Reset	Q
L	X	X	X	H
X	L	X	X	H
H	H	L	X	L
H	H	X	L	L
H	H	H	H	Store

SN 74121

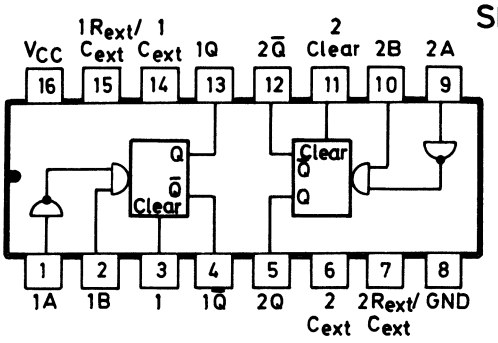


tn Input			tn+1 Input			
A1	A2	B	A1	A2	B	Output
H	H	L	H	H	H	Inhibit
L	X	H	L	X	L	Inhibit
X	L	H	H	L	L	Inhibit
L	X	L	L	X	H	One Shot
X	L	L	X	L	H	One Shot
H	H	H	X	L	H	One Shot
H	H	H	L	X	H	One Shot
X	L	L	X	H	L	Inhibit
L	X	L	H	X	L	Inhibit
X	L	H	H	H	H	Inhibit
L	X	H	H	H	H	Inhibit
H	H	L	X	L	L	Inhibit
H	H	L	L	X	L	Inhibit

$H = V_{in(1)} \geqslant 2V$

$L = V_{in(0)} \leqslant 0{,}8V$

SN 74123



Inputs		Outputs	
A	B	Q	Q̄
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

Notes:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level

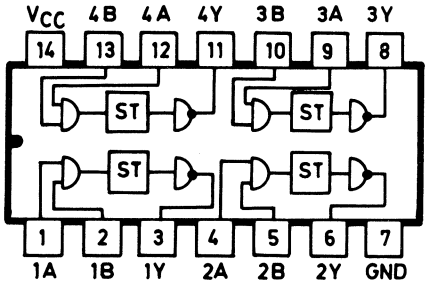
↓ = transition from high to low level

⎍ = one high level pulse

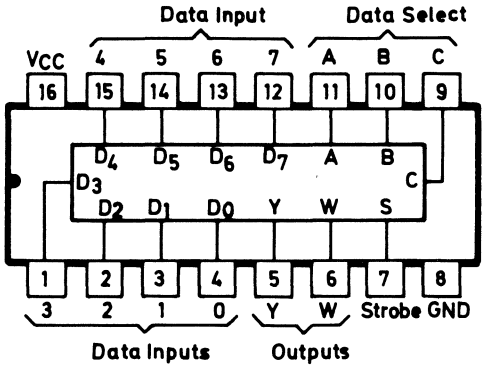
⎎ = one low level pulse

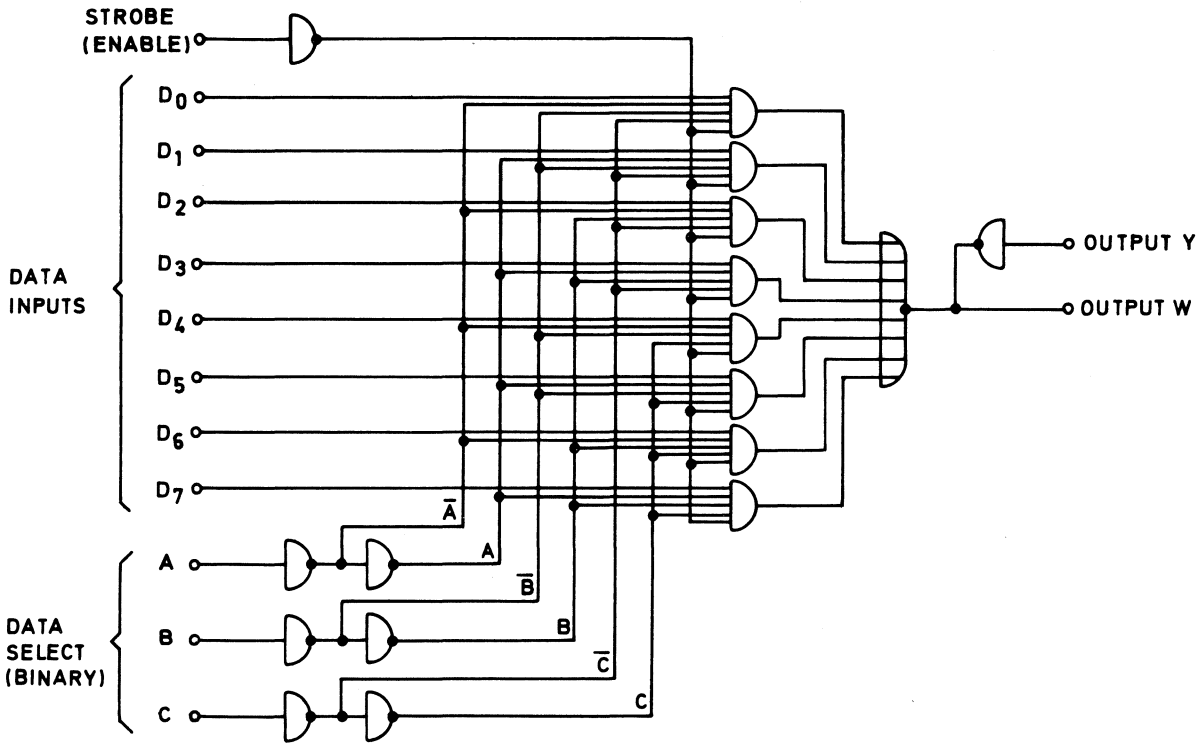
X = irrelevant (any input, including transition)

SN 74132



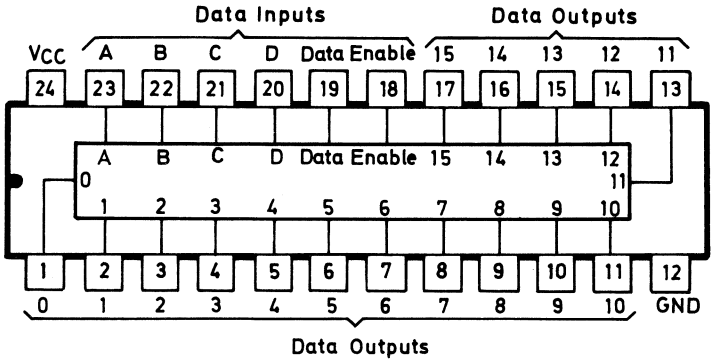
positive logic : $Y = \overline{AB}$

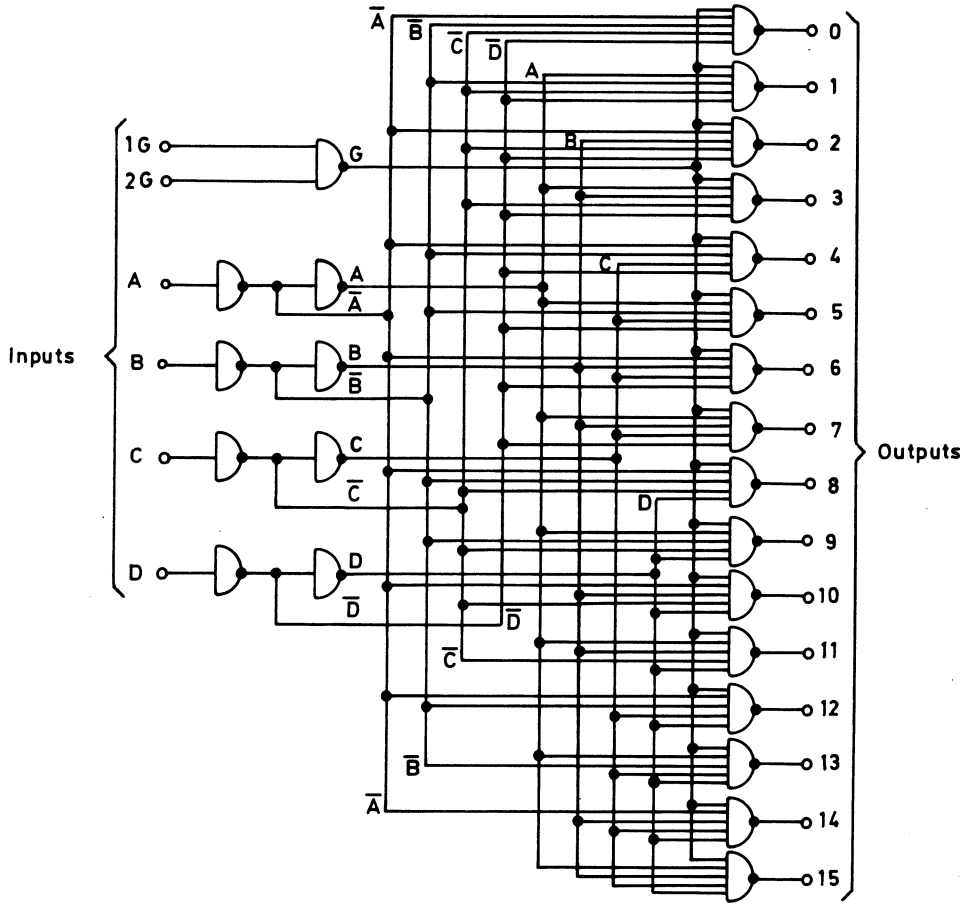


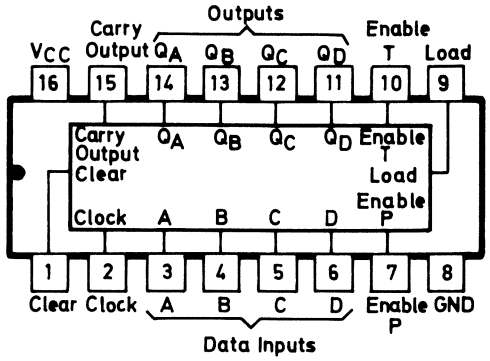


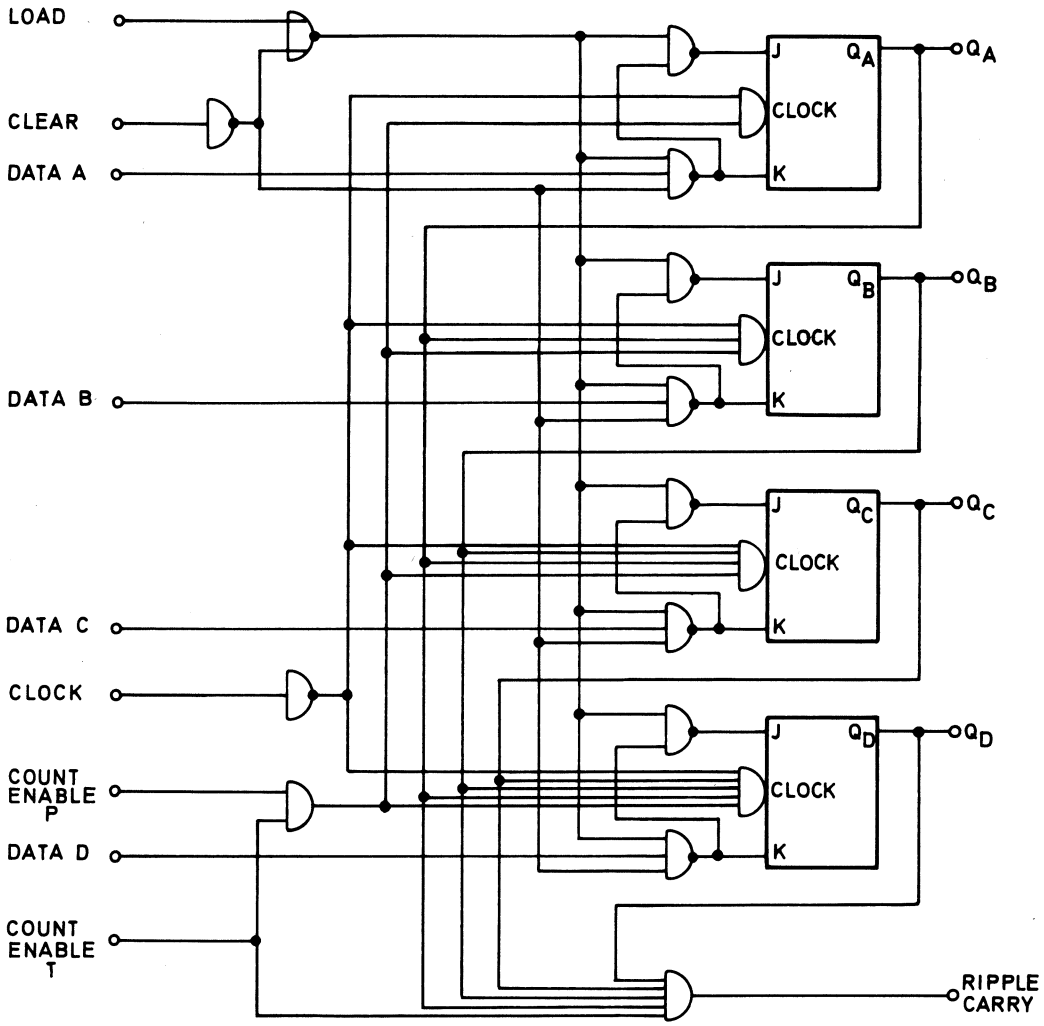
INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

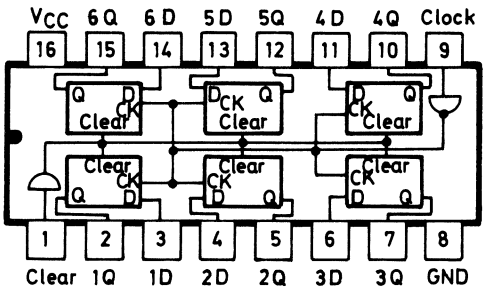
NOTES: 1. SN 54151 / SN 74151 only
2. When used to indicate an input, X= irrelevant


Data Inputs
Data Outputs
VCC
A B C D Data Enable
15 14 13 12 11
24 23 22 21 20 19 18 17 16 15 14 13
A B C D Data Enable 15 14 13 12
0 11
1 2 3 4 5 6 7 8 9 10
1 2 3 4 5 6 7 8 9 10 11 12
0 1 2 3 4 5 6 7 8 9 10 GND
Data Outputs


Inputs
1G
2G
G
A
B
C
D
Outputs
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15



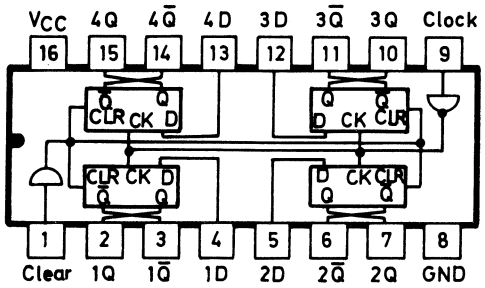




Input	Outputs
t_n	t_{n+1}
D	Q $\overline{Q}$
H	H L
L	L H

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse



Input	Outputs	
t_n	t_n+1	
D	Q	$\overline{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse

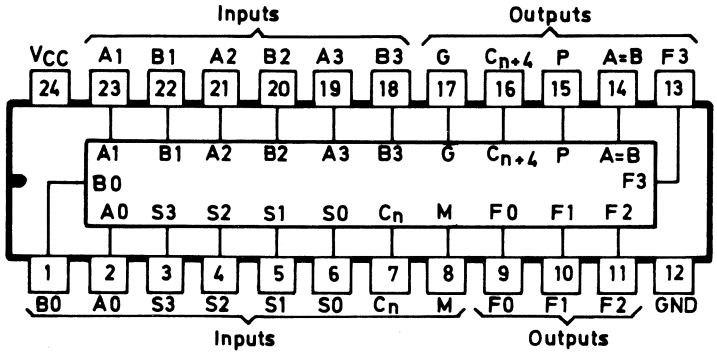
t_{n+1} = Bit time after clock pulse

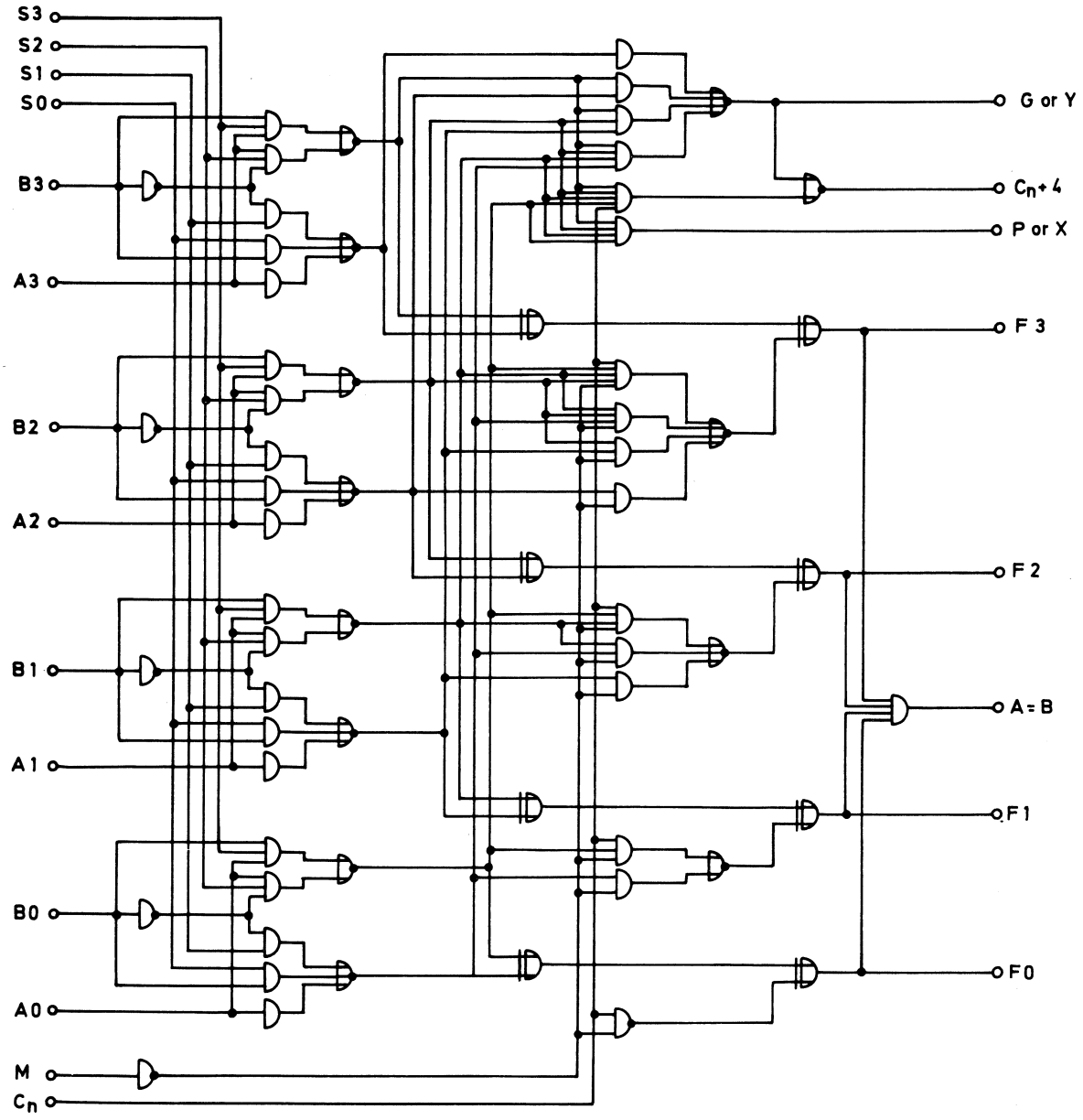
SN 74181

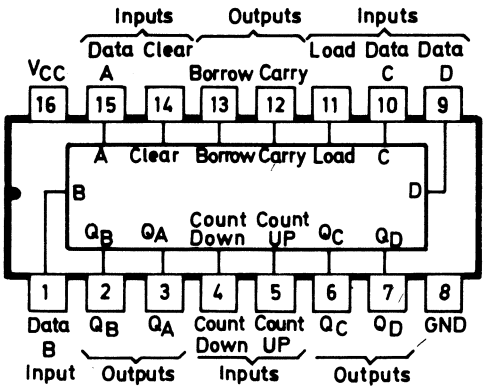
SELECTION S_3 S_2 S_1 S_0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: C_n = 0, $\overline{C_n}$ = 1 = H	C_n = 1, $\overline{C_n}$ = 0 = L
L L L L	F = A	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A+B	F = (A+B) PLUS 1
L L H L	F = $\overline{A}$B	F = A+$\overline{B}$	F = (A+$\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A+B) PLUS A$\overline{B}$	F = (A+B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A⊕B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$+B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A+B) PLUS AB	F = (A+$\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A+$\overline{B}$	F = (A+B) PLUS A	F = (A+B) PLUS A PLUS 1
H H H L	F = A+B	F = (A+$\overline{B}$) PLUS A	F = (A+$\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

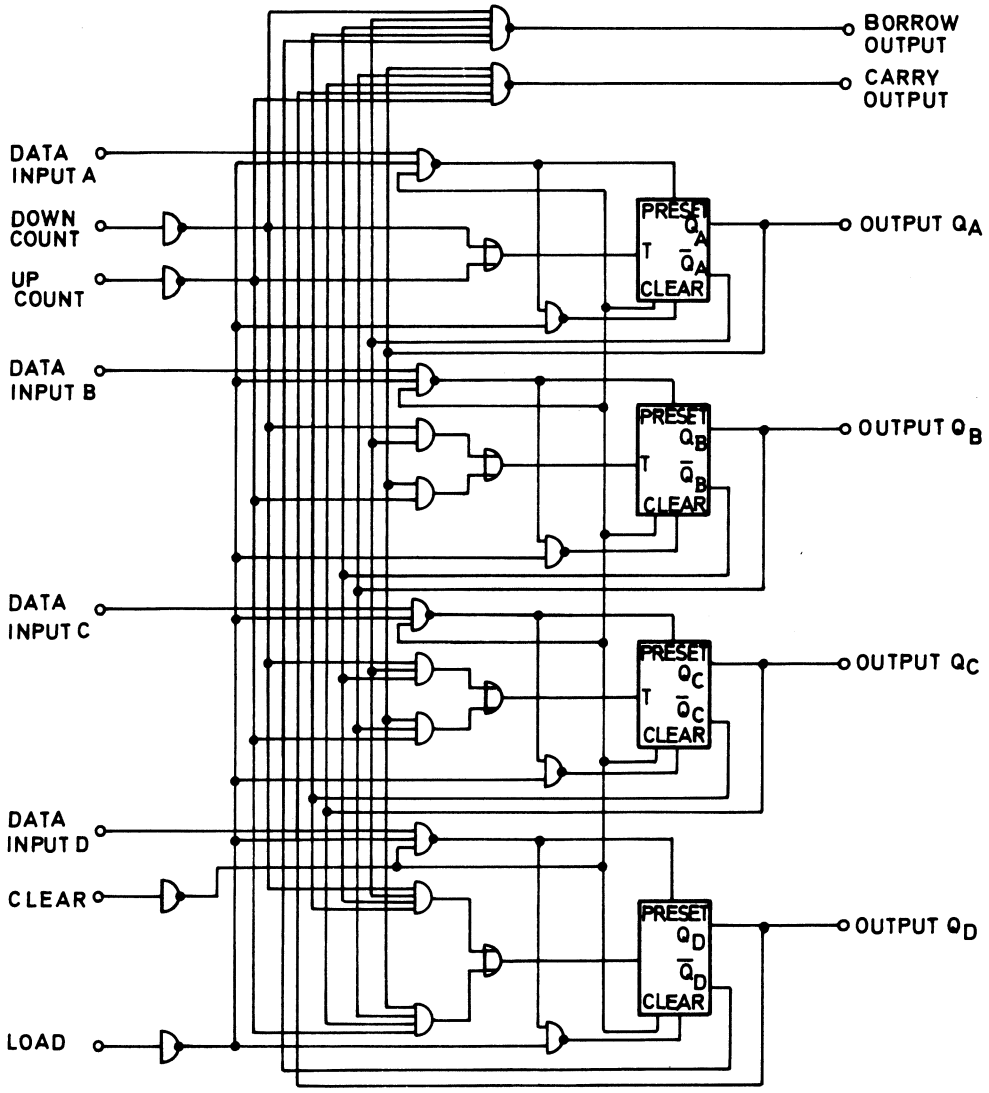
* Each bit is shiftet to the next more significant position.

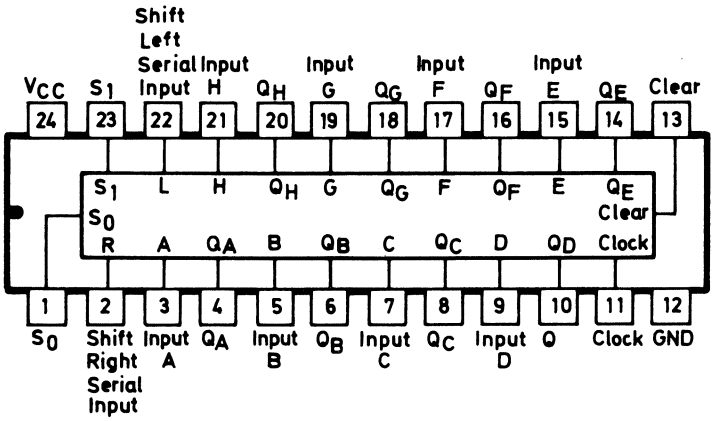
SELECTION S_3 S_2 S_1 S_0	ACTIVE-LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: C_n = 0, Cn = 0 = L	C_n = 1, Cn = 1 = H
L L L L	F = A	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$+B	F = A$\overline{B}$ MINUS 1	F = AB
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A+$\overline{B}$)	F = A PLUS (A+$\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A+$\overline{B}$)	F = AB PLUS (A+$\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A+$\overline{B}$	F = A+$\overline{B}$	F = (A+$\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A+B)	F = A PLUS (A+B) PLUS 1
H L L H	F = A⊕B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A+B)	F = A$\overline{B}$ PLUS (A+B) PLUS 1
H L H H	F = A+B	F = A+B	F = (A+B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1


Inputs
Outputs
VCC A1 B1 A2 B2 A3 B3 G Cn+4 P A=B F3
24 23 22 21 20 19 18 17 16 15 14 13
A1 B1 A2 B2 A3 B3 G Cn+4 P A=B
B0 F3
A0 S3 S2 S1 S0 Cn M F0 F1 F2
1 2 3 4 5 6 7 8 9 10 11 12
B0 A0 S3 S2 S1 S0 Cn M F0 F1 F2 GND
Inputs
Outputs

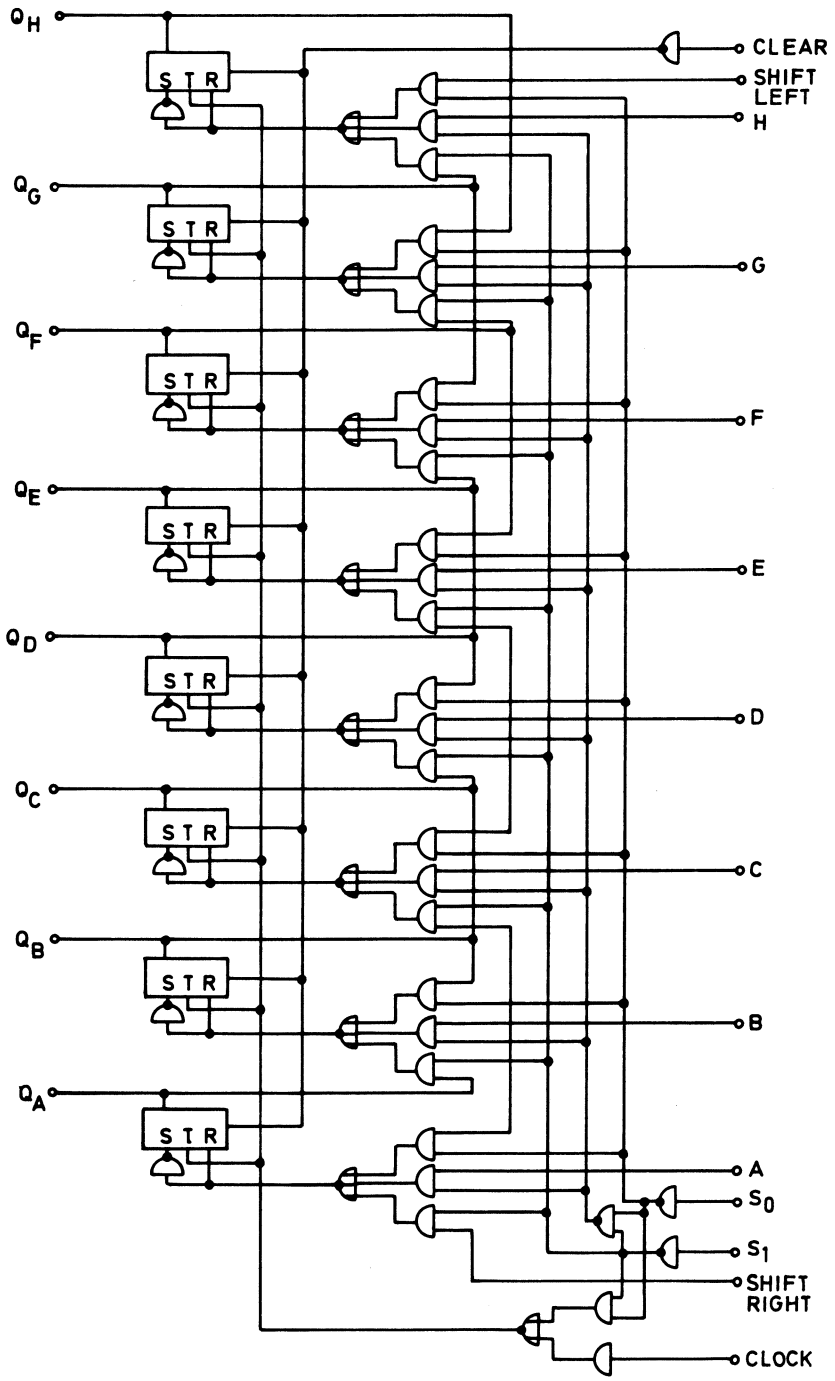

S3
S2
S1
S0
B3
A3
B2
A2
B1
A1
B0
A0
M
Cn
G or Y
Cn+4
P or X
F 3
F 2
A=B
F1
F0


Inputs
Outputs
Inputs
Data Clear
Load Data Data
VCC A Borrow Carry C D
16 15 14 13 12 11 10 9
A Clear Borrow Carry Load C
B D
QB QA Count Down Count UP QC QD
1 2 3 4 5 6 7 8
Data B Input
QB QA
Count Down Count UP
QC QD GND
Outputs
Inputs
Outputs

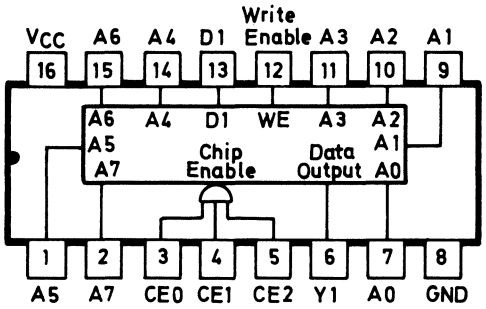

BORROW OUTPUT
CARRY OUTPUT
DATA INPUT A
DOWN COUNT
UP COUNT
DATA INPUT B
DATA INPUT C
DATA INPUT D
CLEAR
LOAD
PRESET
T
CLEAR
OUTPUT QA
OUTPUT QB
OUTPUT QC
OUTPUT QD



S_0	S_1	
H	H	parallel load
H	L	shift right
L	H	shift left
L	L	inhibit clock



SN 74 202



CE	WE	Operation	Output
L	L	Write	High Z
H	H	Read	D
H	L	Do nothing	High Z
H	H	Do nothing	High Z

Notation

A - Address

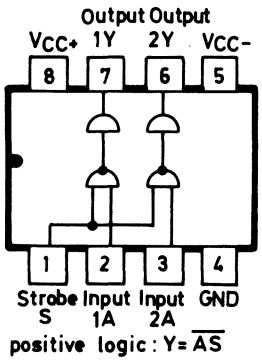
D - Data input

Y - Data output

CE - Chip enable

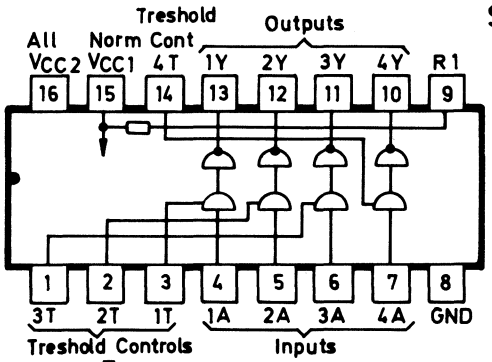
WE - Write enable

SN 75150



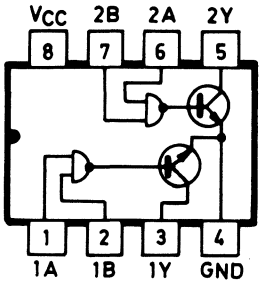
positive logic : $Y = \overline{AS}$

SN 75154



logic : $Y = \overline{A}$

SN 75 451



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