HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Address:

Abbreviation: Mode:

Address	Abbreviation	Name	Mode
80	MBRQ	MP/M Bus Request	W
81	DTRC	Data Transmit/Receive Control	RP
82	SYSCON STAT	System Control Status	RP
83	IM	Interrupt Mask	WP
84	DRP	Data Receive Port	RP
84	DTP	Data Transmit Port	WP
85	BSIV	Bank Select/$\overline{\text{INT}}$-Vector Port	R/W P
86	SYSCLR	SYSCON Port Clear	W
87	DRIVE SEL	Disk Drive Select	R/W P
88	FDC STATUS	Floppy Disk Controller Status	RP
88	FDC COMMAND	Floppy Disk Controller Command	WP
89	FDC TRACK	Floppy Disk Controller Track Reg.	R/W P
8A	FDC SECTOR	Floppy Disk Controller Sector Reg	R/W P
8B	FDC DATA	Floppy Disk Controller Data Reg.	R/W P
8C	PHP	Printer Handshake Port	R/WP
8D	PHPC	Printer Handshake Port Control Register	R/WP
8E	PDP	Printer Data Port	WP
8F	PDPC	Printer Data Port Control Reg.	R/WP
90	KEYBOARD	Keyboard Port	RW/P
91	SIASTAT	Serial Interface 1 Status	RW/P
92	SIAD	Serial Interface 1 Data	RW/P
93	SIBSTAT	Serial Interface 2 Status	RW/P
94	SIBD	Serial Interface 2 Data	RW/P
95	SIACON	Serial Interface 1 Control	WP
96	SIBCON	Serial Interface 2 Control	WP
97	SICC	Serial Interface Common Control	WP
98 to 9F	-	GPIB-Controller µPD 7210	-

W = Write / R = Read / P = Parallel / S = Serial

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

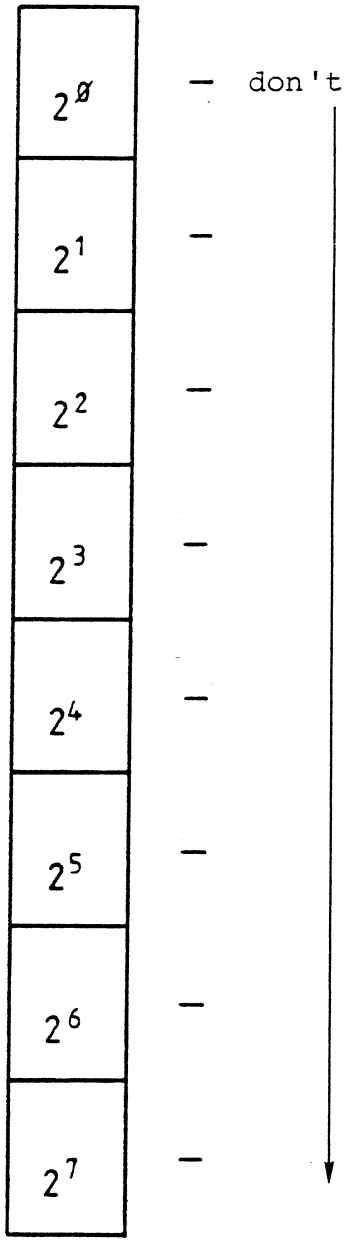
PRODUCT: ATLAS DATE:

Port Description

Port Name: MP/M Bus Request Address: 80

Abbreviation: MBRQ Mode: W

Data Bit | Detailed Description



Any write operation to this port establishes a MBRQ signal in the ATLAS system. This signal is automatically cleared by MP/M bus control.

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Data Transmit/Receive Control Address: 81

Abbreviation: DTRC Mode: RP

Data Bit		Detailed Description
2^0	→ LOR	LOR: This bit is "1" if data is valid in the MP/M's own DRP.
2^1	→ LIR	LIR: This bit is "1" if the MP/M's DTP is not completely filled. Writing a next byte is possible. If LIR = "0", DTP is completely full. No additional write is allowed.
2^2	→ OR*	OR: A "1" indicates that the DTP of a subsystem which is addressed with SLOT contains data.
2^3	→ IR*	IR: A "1" indicates that a write to the DRP of a subsystem - addressed with SLOT - is possible "0" shows that the addressed DRP contains no free space for new data.
2^4	— don't care	
2^5	— don't care	
2^6	— don't care	
2^7	— don't care	

*OR and IR are both invalid if the MP/M-Processor has no bus control.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

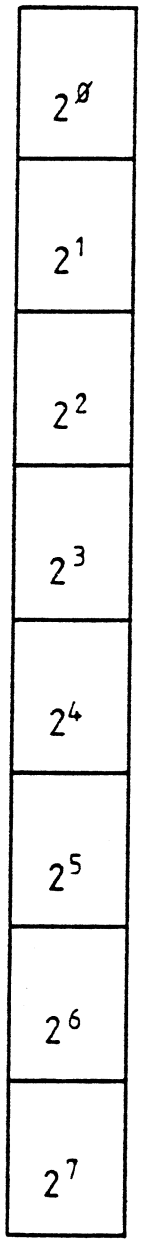
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: System Control Status Address: 82

Abbreviation: SYSCON STAT Mode: RP



Detailed Description

SYSCON 0 .. 3:

Four bits which contain the information about what subsystem bus has control

ØØØØ is MP/M - processor
1111 is LA - processor

$\overline{\text{ACTIVE}}$:

"0" indicates that a minimum of one plug-in is in an active mode. For example, a logic analyzer plug-in samples data. "1" indicates that all plug-ins are inactive.

$\overline{\text{SYSBRQ}}$:

One or more other subsystem(s) ask for bus control if this bit is read as "0". "1" = no pending bus request.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

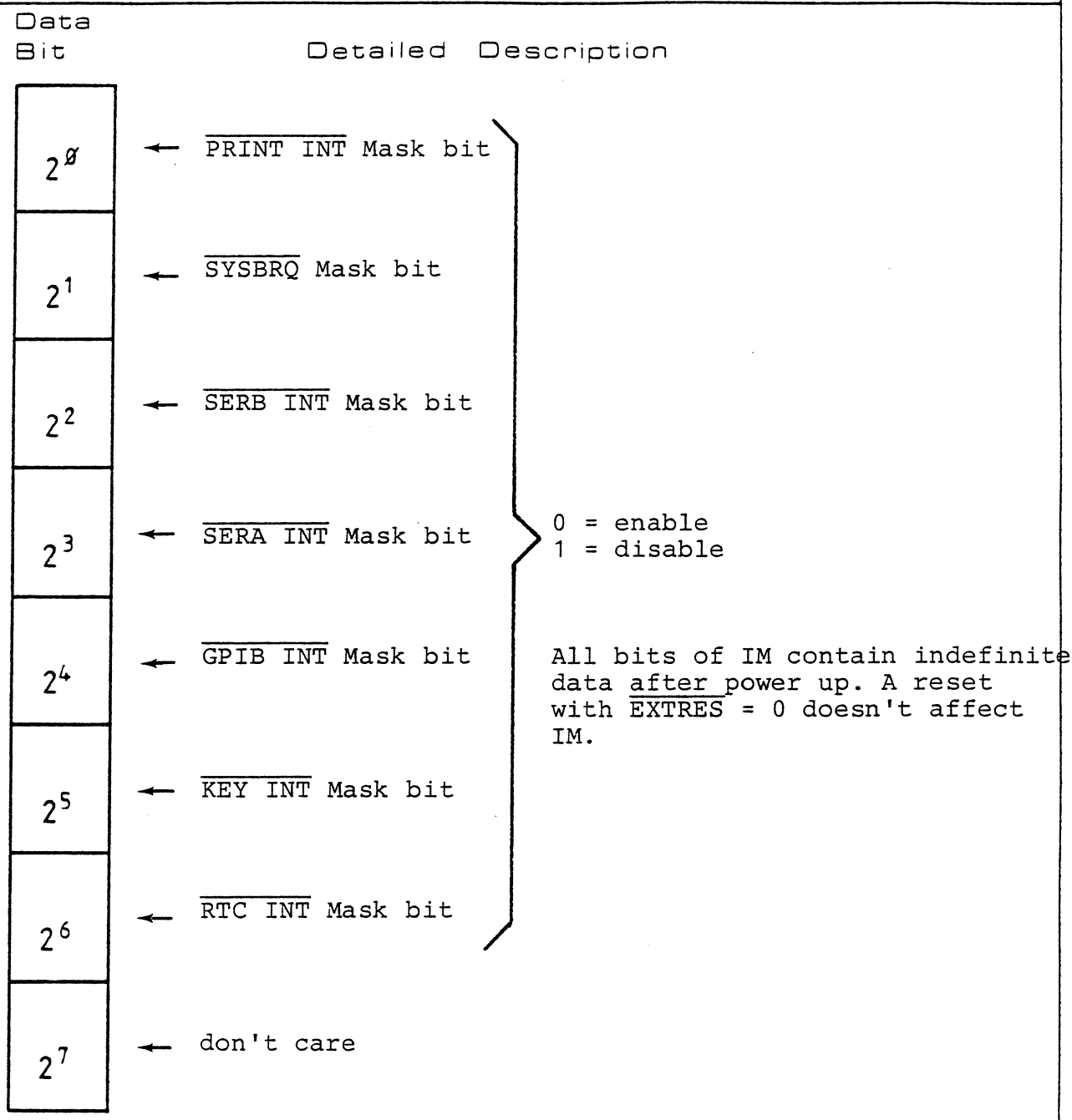
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Interrupt Mask Address: 83

Abbreviation: IM Mode: WP



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

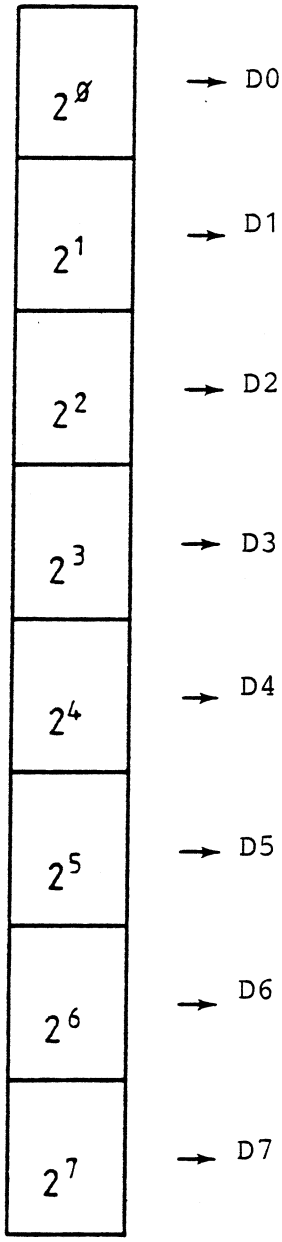
PRODUCT: ATLAS DATE:

Port Description

Port Name: Data Receive Port Address: 84

Abbreviation: DRP Mode: RP

Data Bit Detailed Description



→ D0

→ D1

→ D2

→ D3

→ D4

→ D5

→ D6

→ D7

DRP is a 16 byte deep FIFO which is used as an interface for receiving data if no bus control is available.

LOR (local output ready) control bit is available on DTCP.

DRP is cleared with reset!

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Data Transmit Port Address: 84

Abbreviation: DTP Mode: WP

Data Bit		Detailed Description
2^0	← D0	DTP is a 16 byte deep FIFO which is used to transmit data to other subsystems in the case of no bus control.
2^1	← D1	LIR (local input ready) control bit is available on DTCP.
2^2	← D2	DTP is cleared with reset.
2^3	← D3	
2^4	← D4	
2^5	← D5	
2^6	← D6	
2^7	← D7	

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

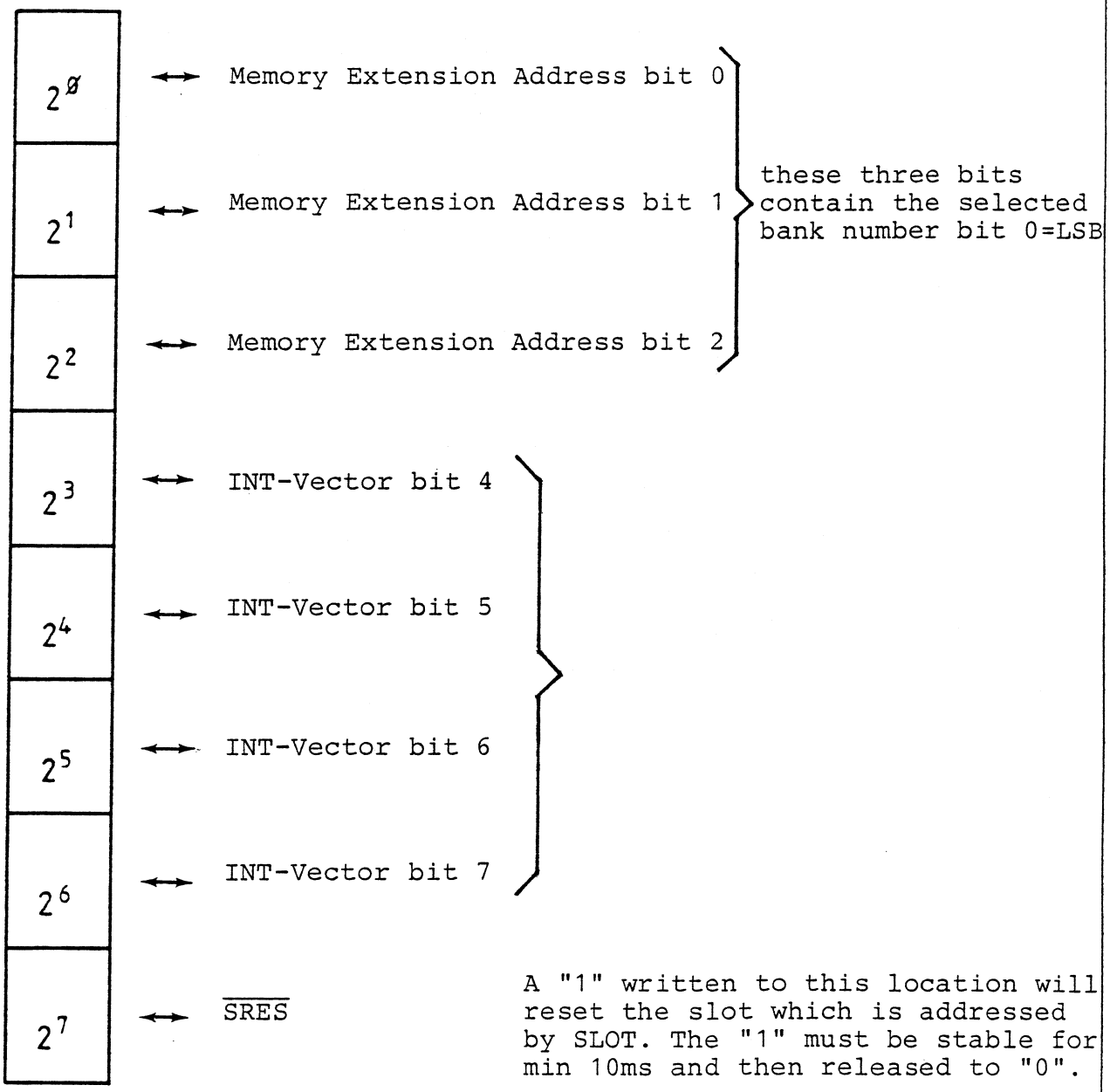
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Bank Select/$\overline{\text{INT}}$-Vector Port Address: 85

Abbreviation: BSIV Mode: R/W P



A "1" written to this location will reset the slot which is addressed by SLOT. The "1" must be stable for min 10ms and then released to "0".

BSIV is cleared by any reset. That enables memory bank 0 = boot PROM and forces the four interrupt vector bits to 0. SRES is not activated by a reset condition.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: SYSCON Port Clear Address: 86

Abbreviation: SYSCLR Mode: W

Data Bit		Detailed Description
2^0	—	don't care
2^1	—	
2^2	—	
2^3	—	
2^4	—	
2^5	—	
2^6	—	
2^7	—	

Any write operation to this port resets port SYSCON to zero and forces MP/M processor to bus control. SYSCLR is automatically inactive after the IO-write to port 86.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

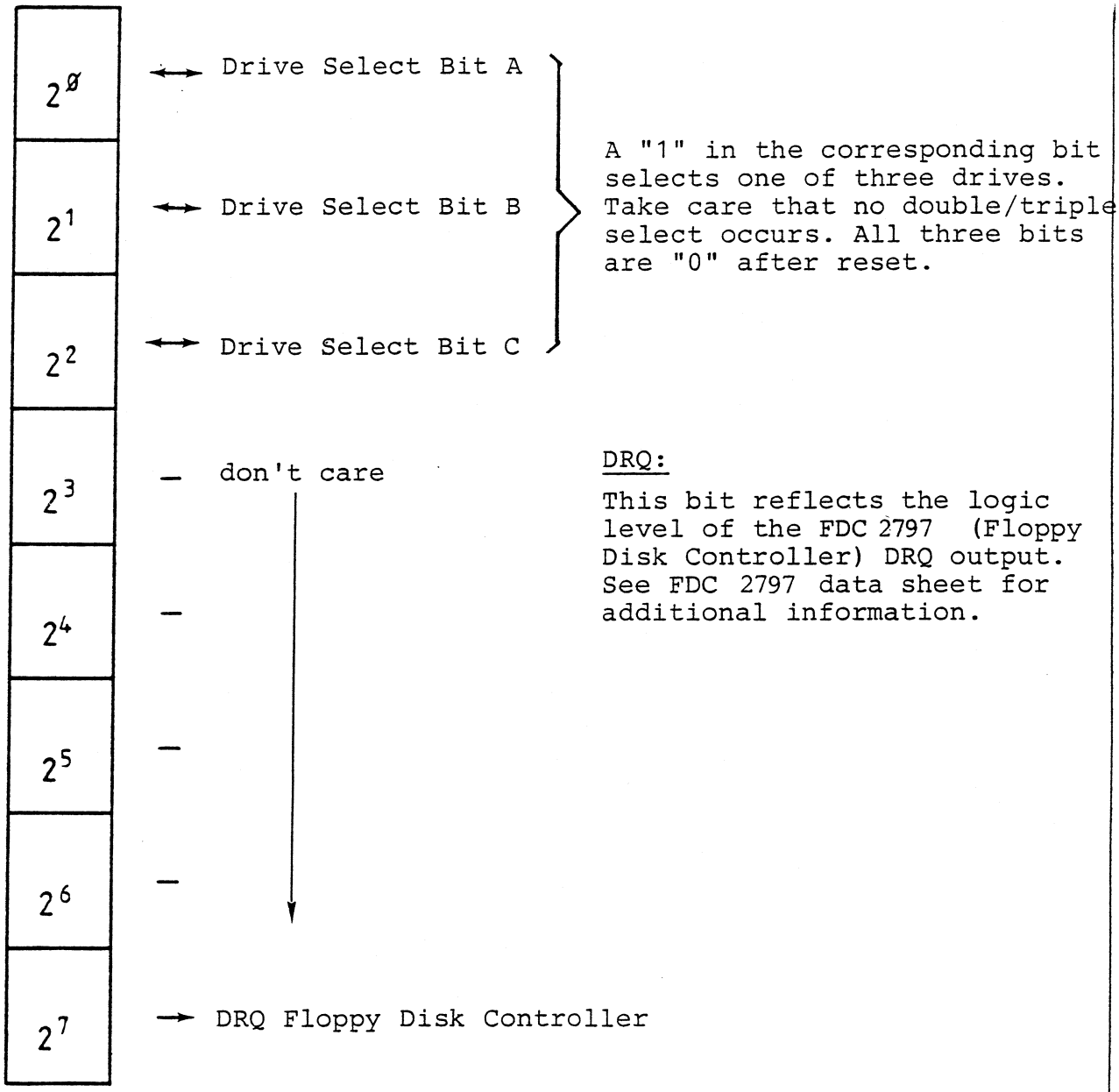
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Disk Drive Select Address: 87

Abbreviation: DRIVE SEL Mode: R/W P



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

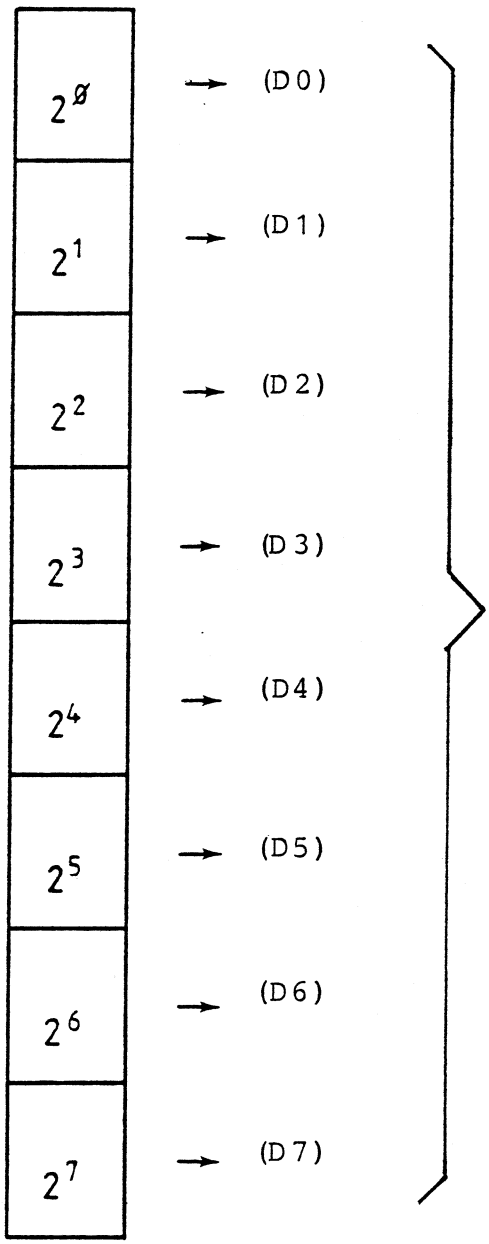
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Floppy Disk Controller Status Address: 88

Abbreviation: FDC STATUS Mode: RP



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

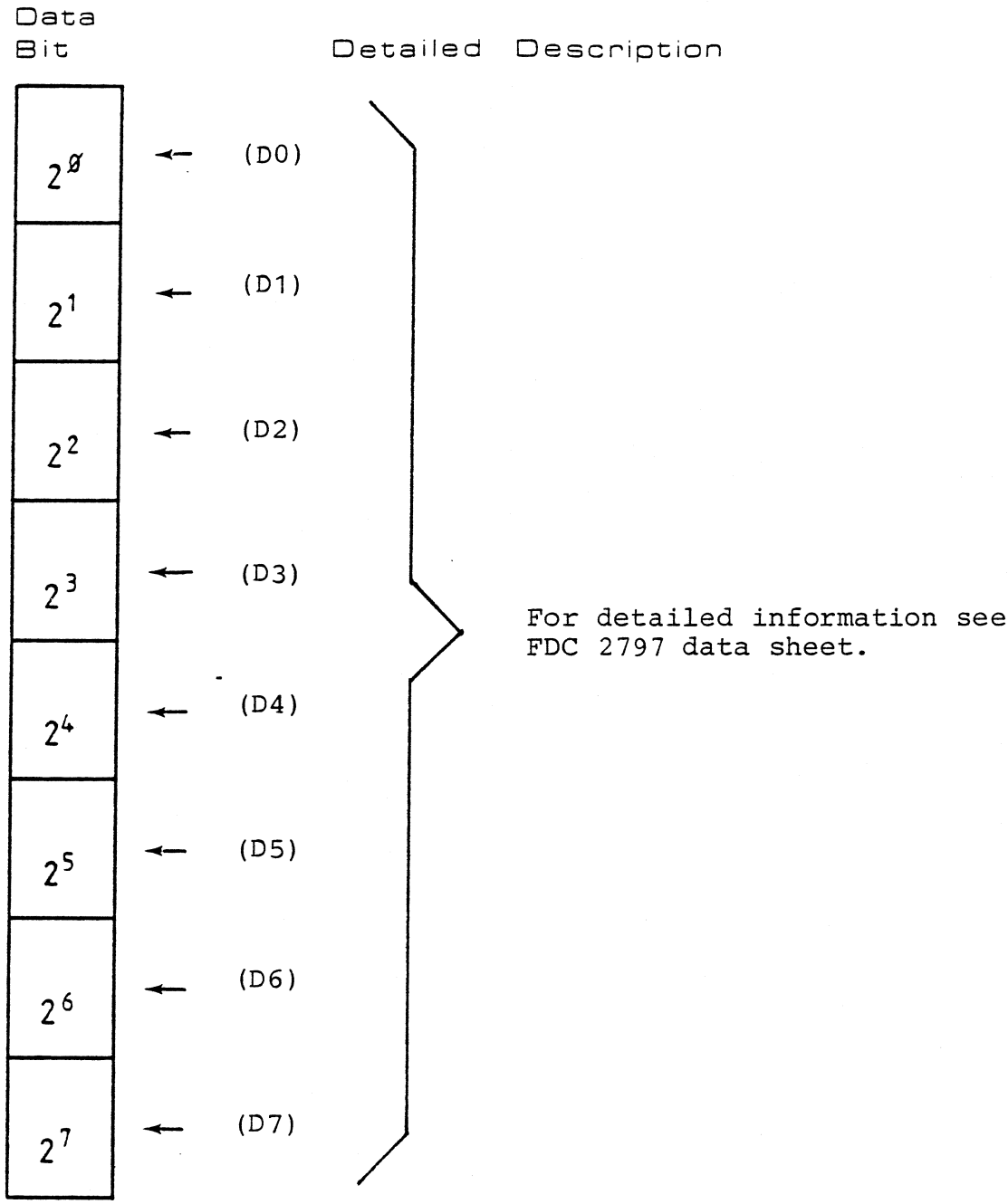
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Floppy Disk Controller Command Address: 88

Abbreviation: FDC COMMAND Mode: WP



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

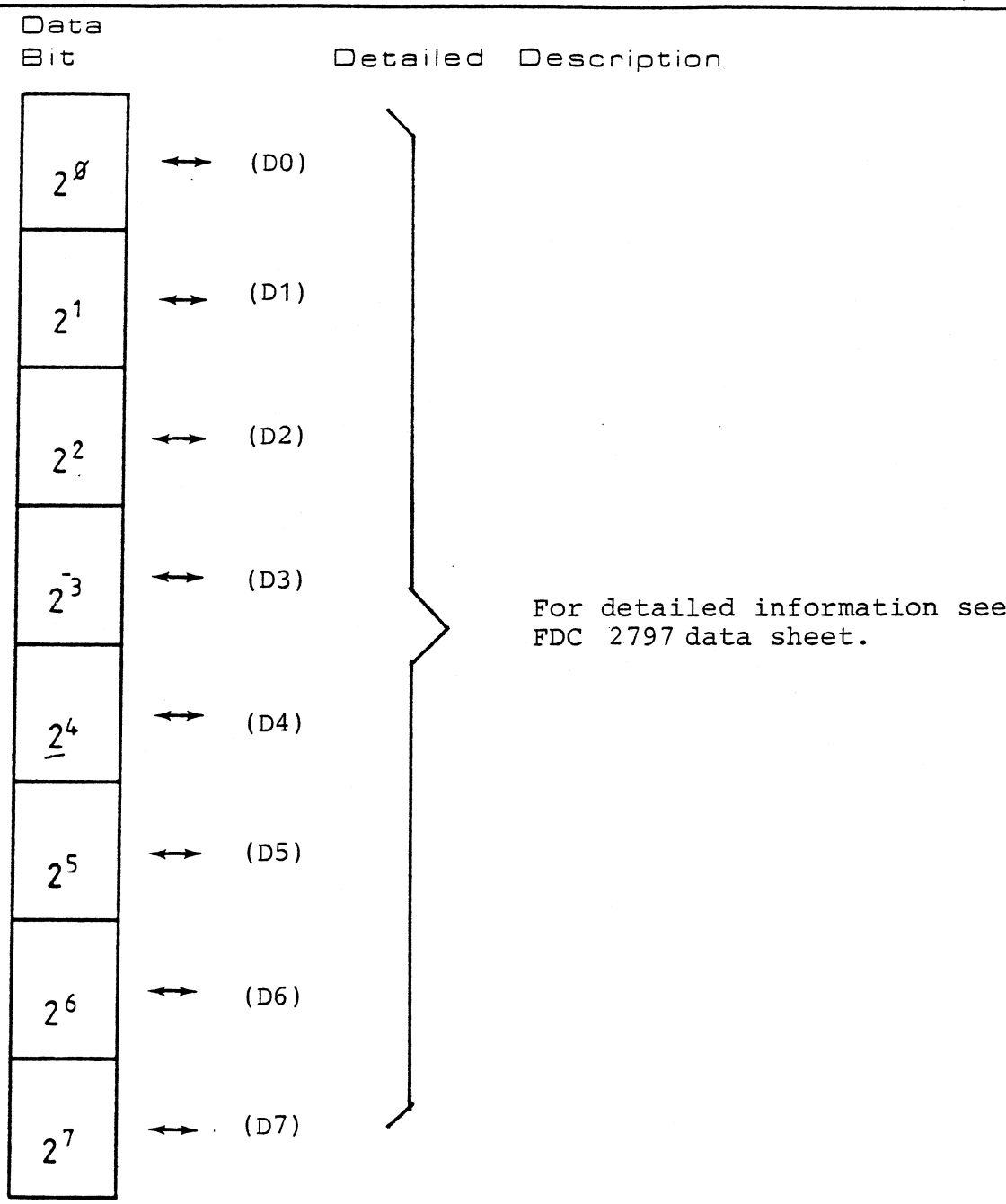
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Floppy Disk Controller Track Register Address: 89

Abbreviation FDC TRACK Mode: R/W P



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

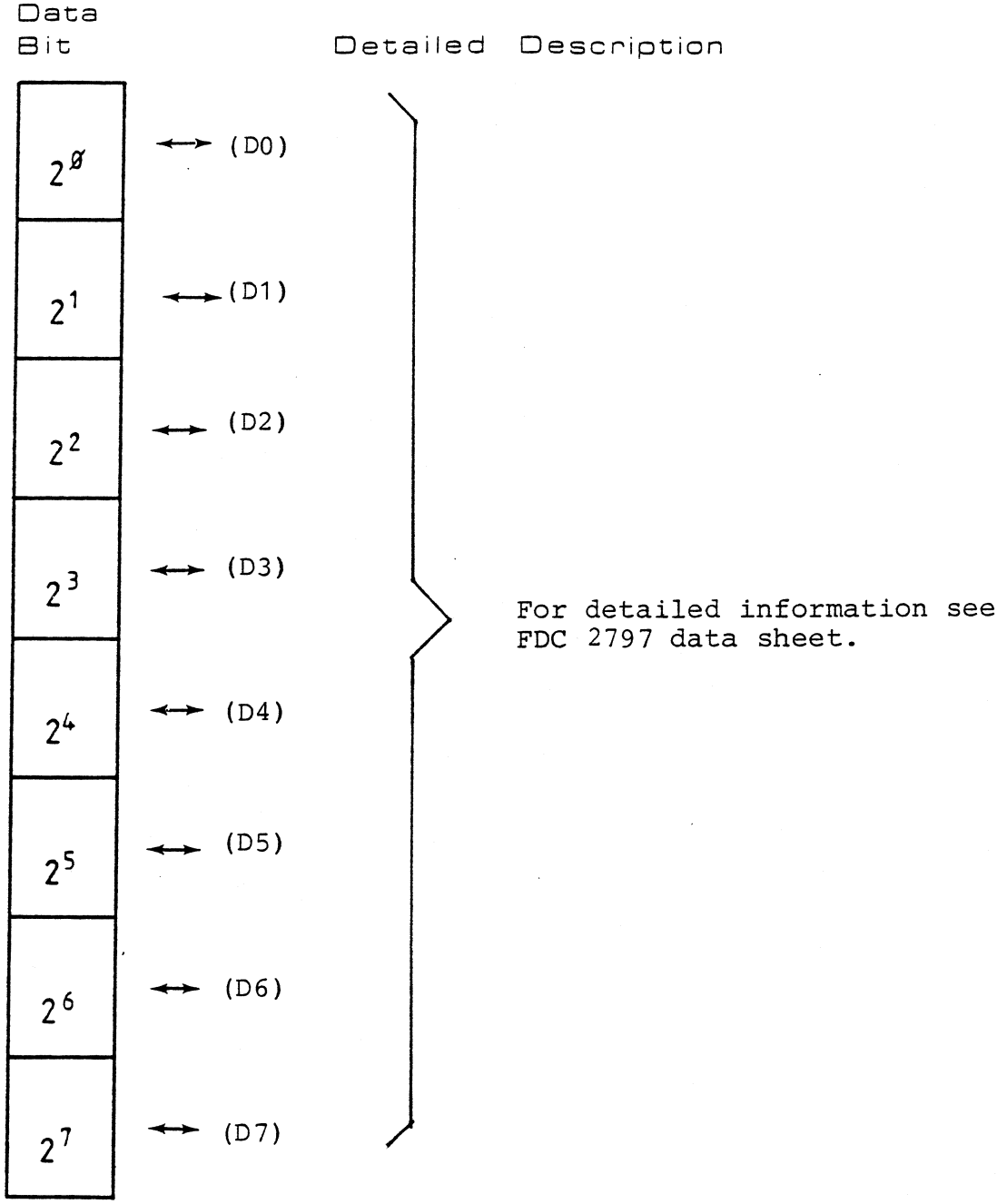
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Floppy Disk Controller Sector Register Address: 8A

Abbreviation: FDC SECTOR Mode: R/W P



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Floppy Disk Controller Data Reg. Address: 8B

Abbreviation: FDC DATA Mode: R/W P

Data Bit		Detailed Description
2^0	↔ (D0)	For detailed information see FDC 2797 data sheet.
2^1	↔ (D1)	
2^2	↔ (D2)	
2^3	↔ (D3)	
2^4	↔ (D4)	
2^5	↔ (D5)	
2^6	↔ (D6)	
2^7	↔ (D7)	

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

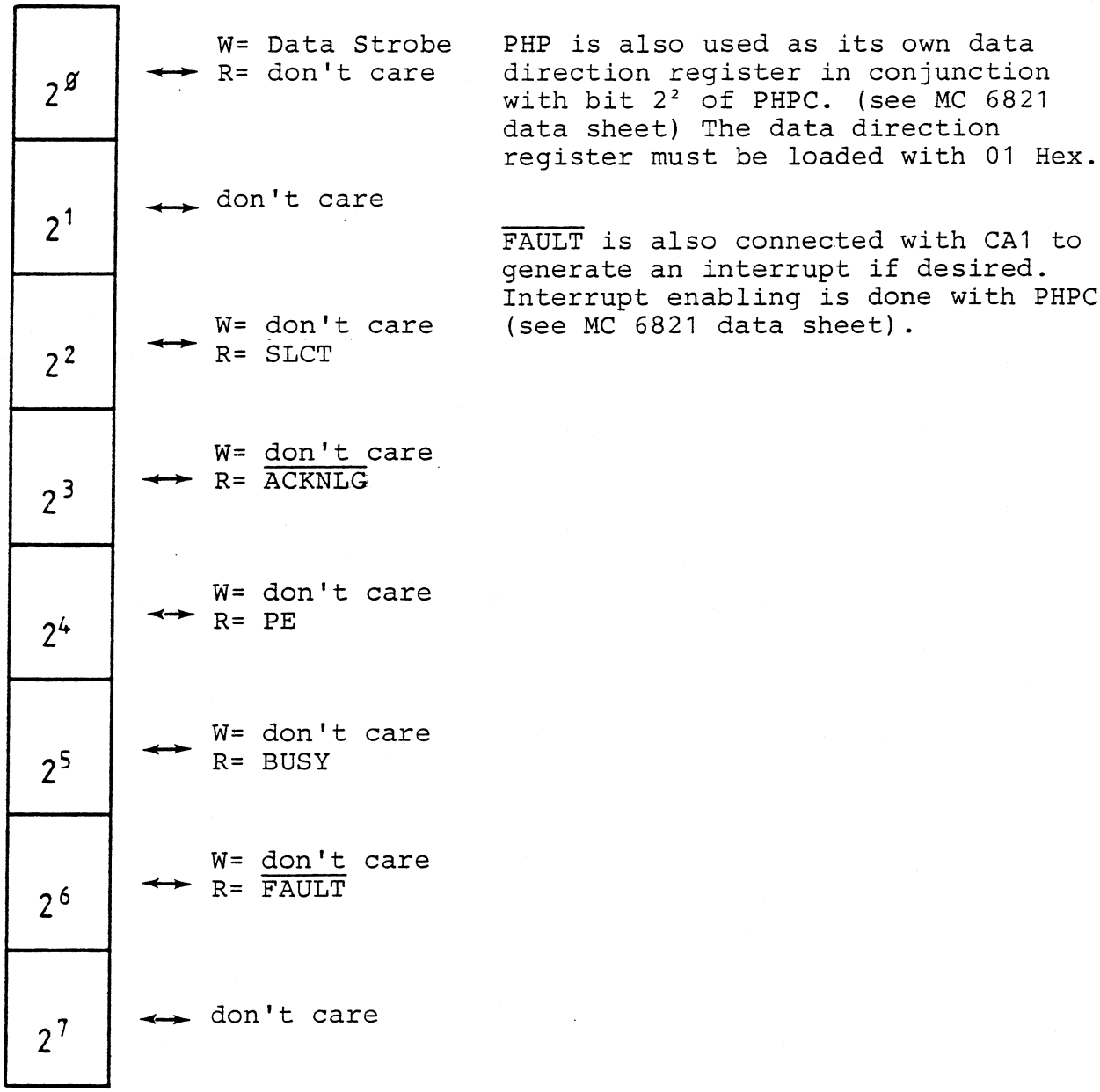
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Printer Handshake Port Address: 8C

Abbreviation: PHP Mode: R/W P



Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Printer Handshake Port Control Reg Address: 8D

Abbreviation: PHPC Mode: R/W P

Data Bit	Detailed Description
2^0 ↔	see MC 6821 data sheet - (control register) for additional information.
2^1 ↔	
2^2 ↔	
2^3 ↔	
2^4 ↔	
2^5 ↔	
2^6 ↔	
2^7 ↔	

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

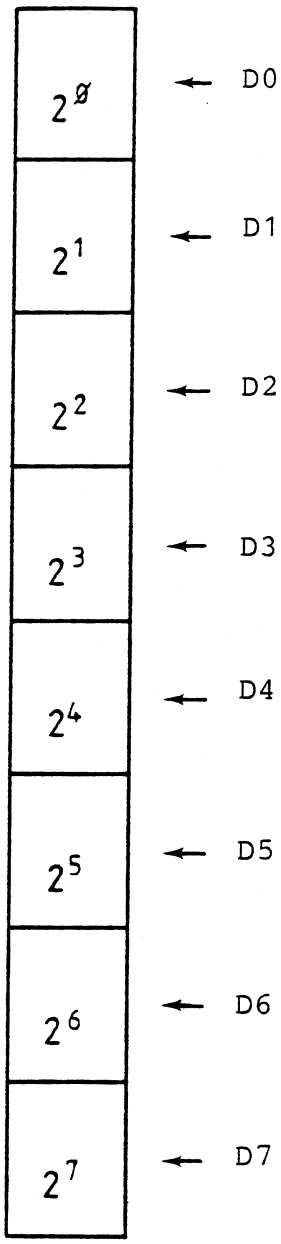
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Printer Data Port Address: 8E

Abbreviation: PDP Mode: WP



PDP is also used as its own data direction register in conjunction with bit 2^2 of PDPC (see MC 6821 data sheet). The data direction register must be loaded with FF Hex.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Printer Data Port Control Register Address: 8F

Abbreviation: PDPC Mode: R/W P

Data Bit		Detailed Description
$2^{\emptyset}$	↔	see MC 6821 data sheet - (control register) for additional information.
2^1	↔	
2^2	↔	
2^3	↔	
2^4	↔	
2^5	↔	
2^6	↔	
2^7	↔	

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

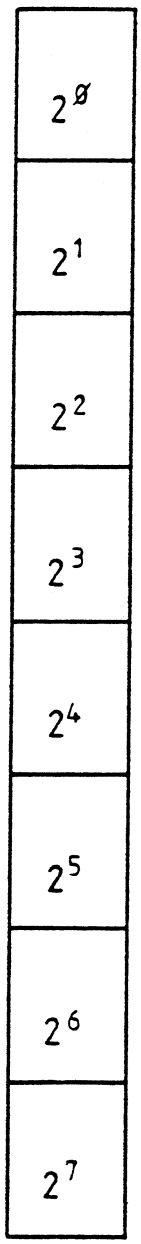
PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Keyboard Port Address: 90

Abbreviation: KEYBOARD Mode: RW/P



Reading from KEYBOARD delivers the pending Key-code. If no key is pressed data is FF.

Writing to the two lower data bits of KEYBOARD sets Keyprom page.

Keyprom page is set to 0 after reset or power up.

MSB	LSB	Page
0	0	0
0	1	1
1	0	2
1	1	3

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

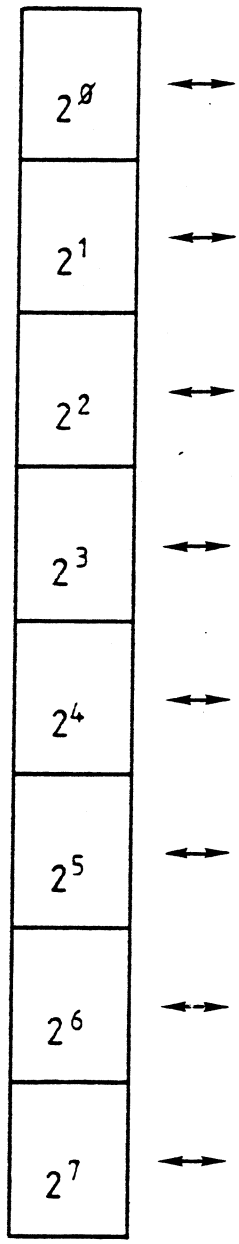
PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface 1 Status Address: 91

Abbreviation: SIASTAT Mode: RW/P

Data Bit



Detailed Description

For detailed information see 8251A data sheet.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

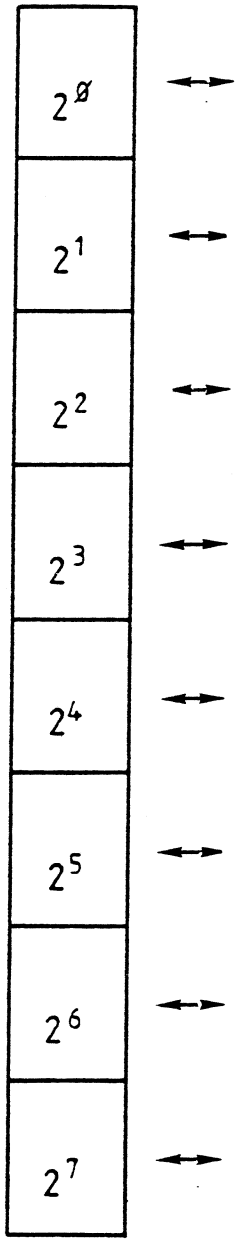
PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface 1 Data Address: 92

Abbreviation: SIAD Mode: RW/P

Data Bit



Detailed Description

For detailed information see 8251A data sheet.

Read = →

Write = ←

Signature:

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface 2 Status Address: 93

Abbreviation: SIBSTAT Mode: RW/P

Data Bit	Detailed Description
$2^{\emptyset}$ ↔	For detailed information see 8251A data sheet.
2^1 ↔	
2^2 ↔	
2^3 ↔	
2^4 ↔	
2^5 ↔	
2^6 ↔	
2^7 ↔	

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

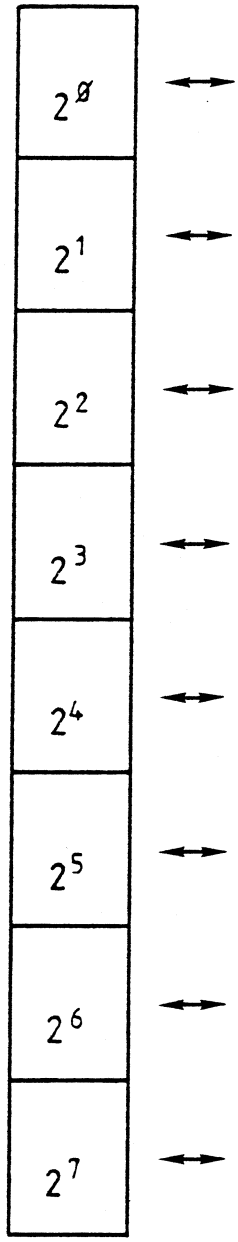
PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface 2 Data Address: 94

Abbreviation: SIBD Mode: RW/P

Data Bit



Detailed Description

For detailed information see 8251A data sheet.

Read = →

Write = ←

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

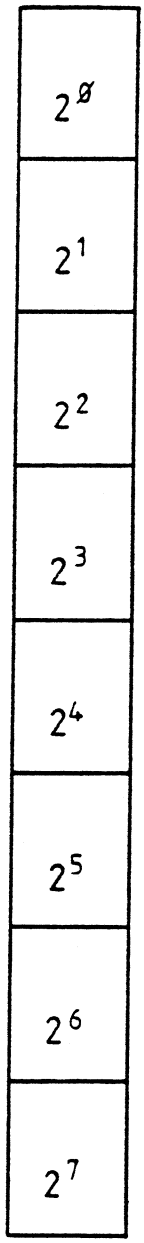
PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface 1 Control Address: 95

Abbreviation: SIACON Mode: WP

Data Bit | Detailed Description



← S0

← S1

← S2

← S3

← 1 = reset for 8251A (SIF 1) A

← 0 = T x D, R x D
1 = T x D, R x D

← D6

← D7

Clock options

D7	D6	Clock
0	0	R x C = T x C Baudrate Gen. A
0	1	R x C fr. RCK inp; TxC fr. Baudrate Gen.A
1	0	R x C = T x C from XCK input
1	1	R x C fr. RCK inp; TxC fr. Baudrate Gen.A

S3	S2	S1	S0	Baudrate
0	0	0	0	extern
0	0	0	1	extern
0	0	1	0	50
0	0	1	1	75
0	1	0	0	134,5
0	1	0	1	200
0	1	1	0	600
0	1	1	1	2400
1	0	0	0	9600
1	0	0	1	4800
1	0	1	0	1800
1	0	1	1	1200
1	1	0	0	2400
1	1	0	1	300
1	1	1	0	150
1	1	1	1	110

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

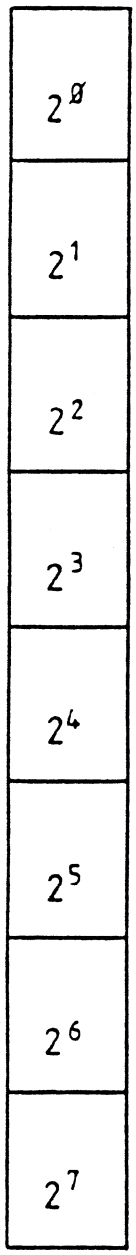
Port Description

Port Name: Serial Interface 2 Control Address: 96

Abbreviation: SIBCON Mode: WP

Data Bit

Detailed Description



← S0

← S1

← S2

← S3

← 1 = reset for 8251A (SIF 2) B

← 0 = $\overline{\text{T x D}}$, $\overline{\text{R x D}}$
1 = T x D, R x D

← D6

← D7

S3	S2	S1	S0	Baudrate
0	0	0	0	extern
0	0	0	1	extern
0	0	1	0	50
0	0	1	1	75
0	1	0	0	134,5
0	1	0	1	200
0	1	1	0	600
0	1	1	1	2400
1	0	0	0	9600
1	0	0	1	4800
1	0	1	0	1800
1	0	1	1	1200
1	1	0	0	2400
1	1	0	1	300
1	1	1	0	150
1	1	1	1	110

Clock options

D7	D6	Clock
0	0	R x C = T x C Baudrate Gen. B
0	1	R x C fr. RCK inp; TxC fr. Baudrate Gen.B
1	0	R x C = T x C from XCK input
1	1	R x C fr. RCK inp; TxC fr. Baudrate Gen.B

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: Serial Interface Common Control Address: 97

Abbreviation: SICC Mode: WP

Data Bit	Detailed Description
2^0	← 0 = $\overline{\text{T x D}}$, $\overline{\text{R x D}}$ 1 = T x D, R x D
2^1	← S2, S1 00 = R x C = T x C from Baudrate Gen. B 10 = R x C = T x C from XCKINP
2^2	←
2^3	← TCK (SIF 2, B) 0 = TCK; 1 = $\overline{\text{TCK}}$
2^4	← CTS (SIF 2, B) 0 = CTS; 1 = $\overline{\text{CTS}}$
2^5	— don't care
2^6	← CTS (SIF 1, A) 0 = CTS; 1 = $\overline{\text{CTS}}$
2^7	← TCK (SIF 1, A) 1 = $\overline{\text{TCK}}$; 0 = TCK

Read = →

Write = ←

Signature: Page 1 of 1

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HARDWARE - DOCUMENTATION

PART - NO: 5-2000-01 REV.:

PRODUCT: ATLAS DATE:

Port Description

Port Name: GPIB-Controller µPD 7210 Address: 98 to 9F

Abbreviation: Mode:

Data Bit	Detailed Description
$2^{\emptyset}$ –	For details see data sheet of the µPD 7210.
2^{1} –	
2^{2} –	
2^{3} –	
2^{4} –	
2^{5} –	
2^{6} –	
2^{7} –	

Read = →

Write = ←

Signature:

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