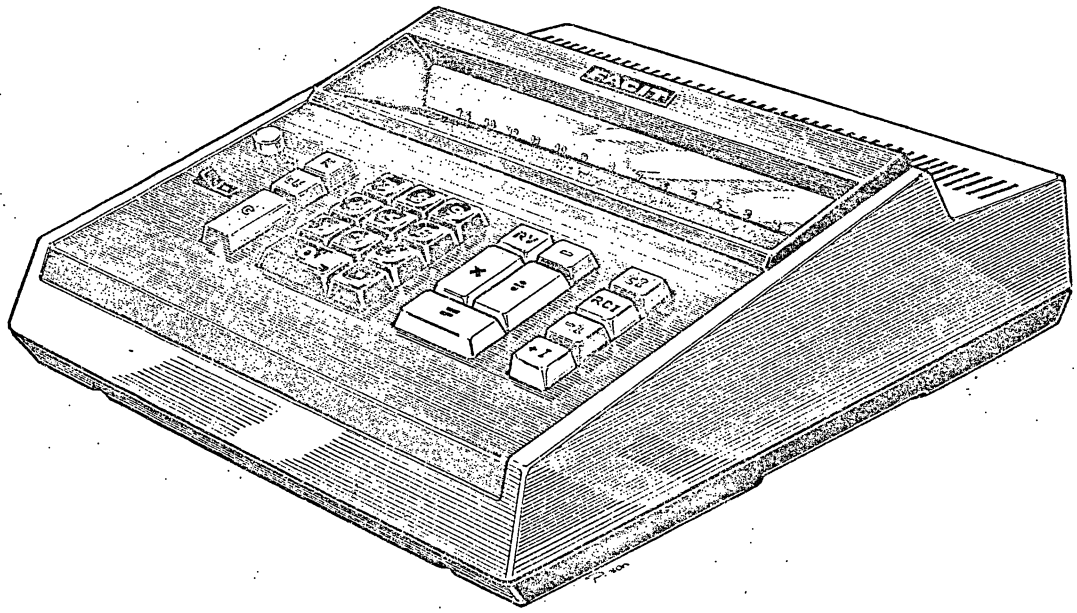
FACIT 1129

Electronic desk calculator

SERVICE MANUAL



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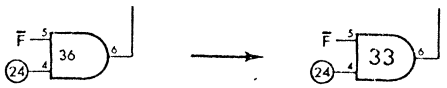
1129.03.01 Eng. 0.5 M 02.71

CORRECTIONS

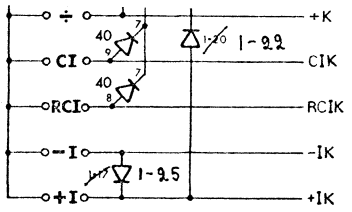
Appendix 4

1 Correction of gate numbering



2 Correct diode numbering 1-20 to 1-22

Correct diode numbering 1-17 to 1-25

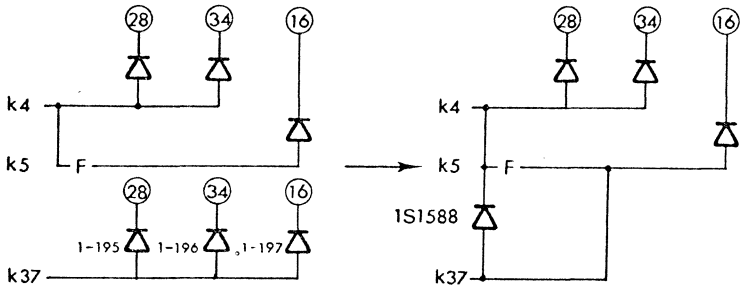


MODIFICATIONS

With the following notes we want to inform you about a few production modifications. These modifications do not influence the calculator operations.

Appendix 8

In some calculators diodes 1-195, 1-196 and 1-197 in address k37 can have been removed and replaced by a direct connection between addresses k37 and k5, and by a diode 1S1588 between addresses k37 and k4.



Appendix 9

The following components can be removed without effect on the function:

- Diode No. 1-1, 1-6, 1-7, 1-14, 1-15, 1-16, 1-17, 1-18, 1-19, 1-20.
- Diode No. 1-21, 1-154 can be replaced by a direct connection.
- Resistor No. 1-R47 can be replaced by a direct connection.

TABLE OF CONTENTS – SECTION I

1 GENERAL

This calculator performs the four fundamental arithmetic operations, with a setting/result capacity of 14 digits of which max. 6 (or 7) can be decimals.[x)] The calculator is provided with a 14 position accumulating register and a four bit register for the number of decimals and sign.

The calculator can also perform constant calculation operations, mixed multiplication, division and squaring operations.

All registers are automatically cleared when the mains supply is switched on. (ACL).

The calculator incorporate MOS-FET (Metal Oxide Semi-conductor, Field Effect Transistor) components. Because MOS-FET elements are very sensitive to static electricity, special precautions must be taken when servicing these types of calculators.

The manual is divided into two main sections:

I Detailed description of the calculator.

II Spare part catalogue.

[x)] Some calculators in the early production can display 7 decimals

2 SPECIFICATIONS

Setting capacity

Max. 14 digits including decimals - max. 6 decimals. Some calculators in the early production can display up to 7 decimals.

Calculating capacity

Addition	Max. 14 digits in result including integers and decimals. Number of decimals read in may exceed number preset using the decimal selector.
Subtraction	Same as addition.
Multiplication	Sum of digits in multiplier and multiplicand can total max. 14.
Division	Divisor or dividend can contain max. 13 digits.

The result of addition and subtraction will always contain the number of decimals preset. Products obtained by multiplication will contain as many decimals as there are in the multiplier and multiplicand together unless this total should exceed the number preset. In such case, the number of decimals in the product will be truncated to the number preset using the decimal selector. Quotients obtained by division will contain the number of decimals that were preset unless the integers plus decimals exceed the display register capacity. In such case, the integers will be displayed correctly along with as many decimals as there is room for.

Calculation speeds

Addition/subtraction	Max. 50 ms.
Multiplication	Max. 460 ms.
Division	Max. 530 ms.

Error, store and sign indication

Errors are indicated by displaying an E. In the event of an error, the [C] -key must be depressed before calculation can proceed. A minus sign is displayed to indicate negative results.

Store contents are indicated by an I symbol.

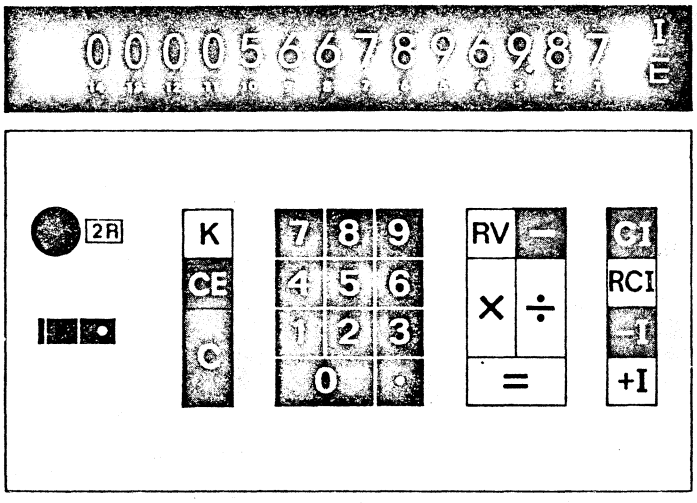


Fig. 2.1 Keyboard

Keyboard (Fig. 2.1)

Power ON/OFF switch (ACL signal clears all registers)

Decimal selector switch (provides TAB signal). Black selector numbers provide truncation without rounding off. Red selector numbers followed by letter R provide truncation and rounding off.

[K] For constant factor operations. Repeated addition and subtraction is possible. In multiplication the first factor is used as the constant. In division the second factor is used as the constant.

[C] Clears all registers (Except the store register).

[CE] Clear entry key for clearing the read-in (X) register. Does not affect sign circuits.

[0-9] Figure-setting keys.

[·] Decimal key.

[×] Sets up conditions for reading in the multiplicand (multiplier). (Provides $xX \rightarrow yY$ and $0 \rightarrow xX$.) A lamp in the key lights up when it is depressed.

[+] Sets up conditions for reading in divisor (dividend). (Provides $xX \rightarrow yY$ and $0 \rightarrow xX$.) A lamp in the key lights up when it is depressed.

[=] Carries out addition, multiplication or division.

[-] Carries out subtraction.

[RV] Carries out operation X, Xs, $x \leftrightarrow$ Y, Ys, y.

[+I] For adding displayed digits to the store register. When used in conjunction with multiplication or division, it performs the operation and adds the result to the store register.

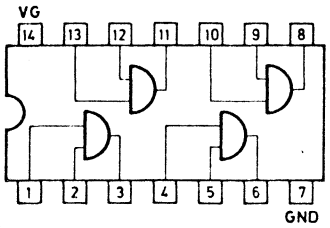
[-I] For subtracting displayed digits from the store register. When used in conjunction with multiplication or division, it performs the operation and subtracts the result from the store register.

[RCI] For calling the content of the store register into the X-register. The previous content of X-register is transferred to the Y-register. The previous content of the Y-register is destroyed.

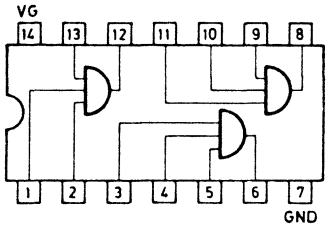
[CI] For clearing the store register (M).

Calculator operations	Result
Addition/subtraction	
A [=] B [=] C [=]	A + B + C
A [-] B [-] C [-]	-A - B - C
A [=] B [-] C [=]	A - B + C
Multiplication and division	
A [x] B [=]	AB
A [x] B [x] C	ABC
A [:] B [=]	A/B
A [x] B [:] C	AB/C
A [x] B [=] [=]	A + AB (premium calculations)
A [x] B [=] [-]	A - AB (discount calculation)
Addition/subtraction of constant	
[K] A [=] [=] B [-] [-] [-]	2A - 3B
Constant multiplicand	
[K] A [x] B [=] C [=] D [=]	AB AC AD
Constant divisor	
[K] A [:] B [=] C [=] D [=]	A/B C/B D/B
Raising to a power	
[K] A [x] [=] [=]	AAA (A^3)
Erroneous calculation	
0 [x] A [=]	0
A [x] 0 [=]	0
0 [:] A [=]	0
A [:] 0 [=]	ERROR INDICATION

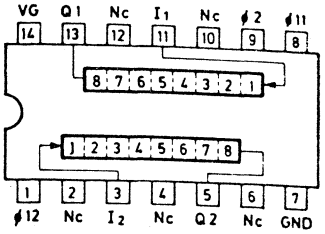
μPD 101 C 4 x 2 AND gate



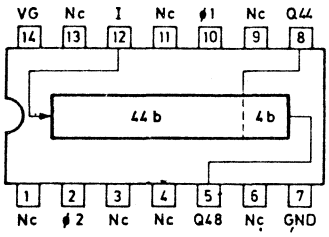
μPD 102 C 3 x 3 AND gate



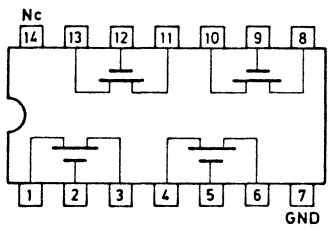
μPD 104 C Dual 8-bit shift register



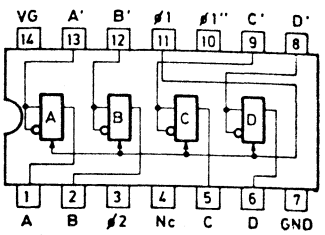
μPD 106 C 44 + 4-bit shift register



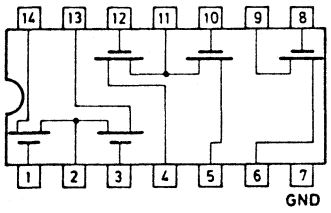
μPD 110 C 4 MOS transistors



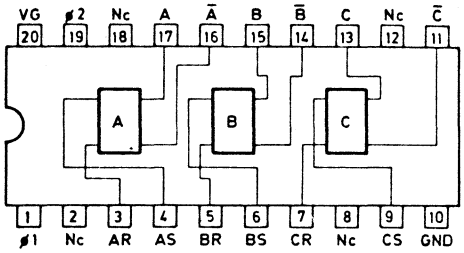
μPD 134 C Quadruple D-FF



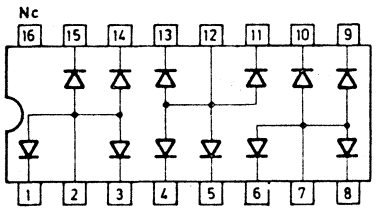
μPD 136 C 5 MOS transistors



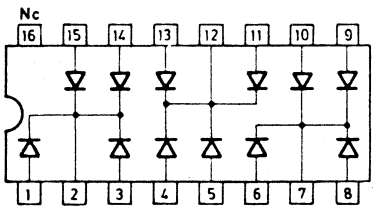
μPD 135 C Triple RSS FF



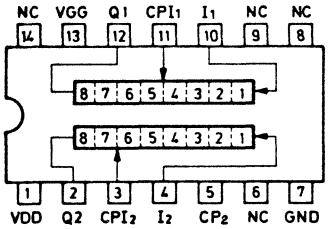
HD - 9004 (DP4)



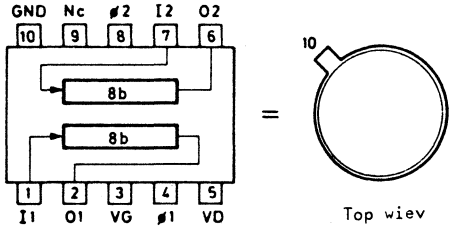
HD - 9003 (DN3)



HD - 3101 Dual 8-bit shift register



HD - 709 (μPD 141) Dual 8-bit shift register



HD - 3102 (M 58202) Delayed adder

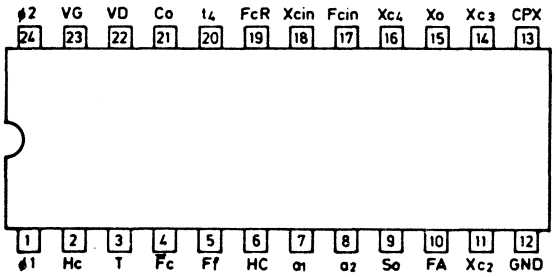


Fig. 2.2 Package pin numbering

Components

The calculator contains two printed circuit boards and a power supply that include:

56 IC packages (mostly MOS packages). See Fig. 2.2
58 transistors
340 diodes
1 zener diode
15 display tubes (14 for digits/decimal-points and 1 for the sign)

Operational data

Voltage	110/127/220 V. Separate transformer for each voltage.
Frequency	50 - 60 Hz.
Power consumption	Approx. 21 W.
Temperature	0° - 40°C.
Relative humidity	Max. 90 %.

Dimensions and weight

Height	120 mm.
Width	280 mm.
Depth	330 mm.
Weight	Approx. 5 kg.

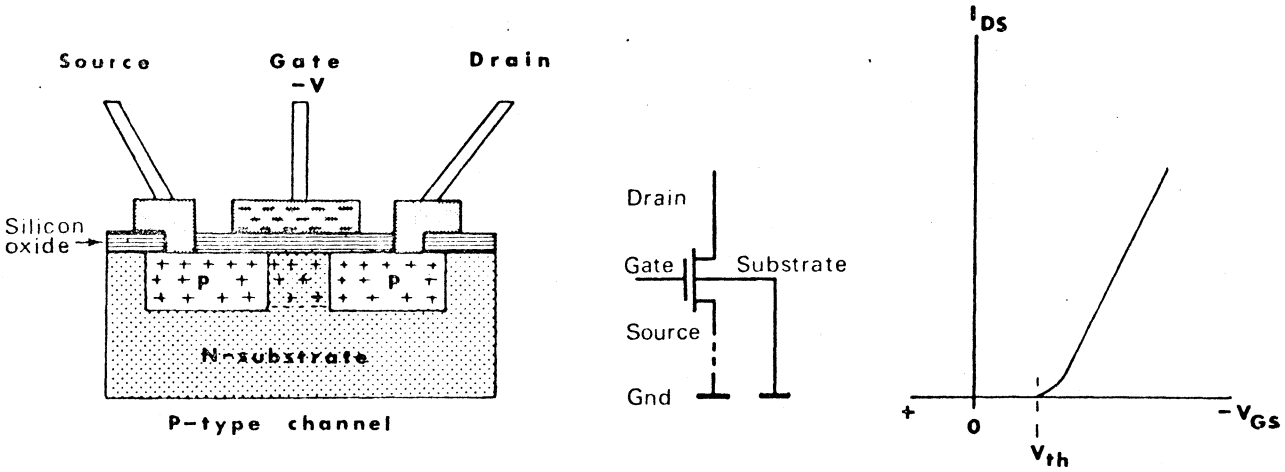


Fig. 3.1 Cross-section of a MOS transistor. The circuit-diagram symbol is shown at centre. V_{th} in the I_{DS} - V_{GS} diagram is the voltage at which current commences to flow at a given drain-source voltage

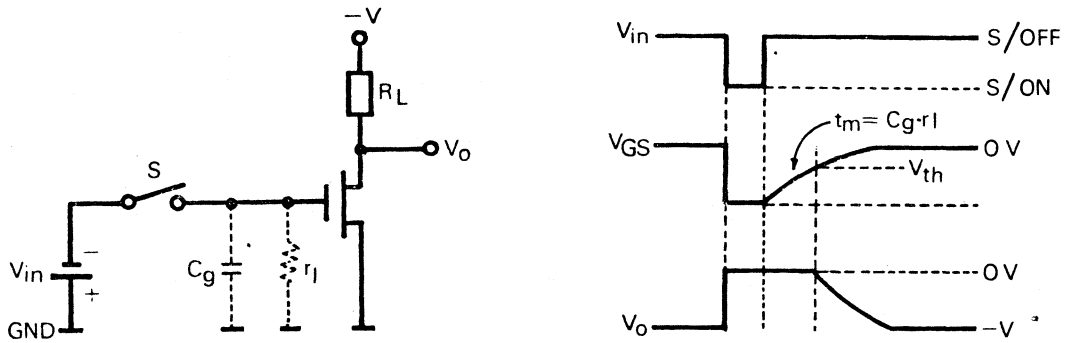


Fig. 3.2 Circuit equivalent to a MOS transistor. Substrate connections not shown

3 GENERAL ABOUT BASIC CALCULATOR CIRCUITS

The logic circuits in the calculator consist primarily of MOS (Metal Oxide Semiconductor) packages, but there are also a large number of discrete components such as transistors, diodes and resistors. The transistors are used mostly to drive the indicator tubes. Most of the diodes perform various gating functions. Note that the calculator is designed with positive true logic. This means that a logic 1 is represented by the high level (H = 0 V to approx. -5 V) and a logic 0 is represented by the low level (L = approx. -10 V to -24 V).

3.1 MOS CIRCUITS

Transistors in the integrated MOS circuits comprise two P-type regions that are diffused in an N-type crystal called the substrate. See Fig. 3.1. The P-type regions located adjacent to each other are called the SOURCE and the DRAIN. Between them on the substrate is a thin layer of silicon dioxide that provides the insulation between the substrate and a metal electrode called the GATE.

If sufficient negative voltage relative to the substrate is applied to the gate electrode, electrons (-) are repelled from the interface between the source and the drain and holes (+) are attracted to this interface. A conducting P-type channel is thus formed. If a suitable voltage is applied across the source and drain, current will flow between them. The strength of this current is controlled by the applied gate voltage.

A MOS transistor with a P-type channel has polarity corresponding to that of a PNP transistor. The drain electrode shall have a negative voltage relative to the source electrode. When a negative bias is applied to the gate electrode, the MOS transistor conducts, and when the bias is 0 V (V_{GS} = 0 V) it is cut off. V_{th} on the I_{DS} - V_{GS} characteristic is the voltage at which current commences to flow at a given drain-source voltage.

Since the gate electrode is insulated from the substrate by the silicon dioxide, the MOS transistor has very high input resistance.

At its input, the MOS transistor acts as a capacitor; it can thus be used as a memory element. Fig. 3.2 shows the principles of a temporary memory circuit comprising a MOS transistor. When S is turned on, Cg will be charged to Vin, whereupon the transistor becomes conducting. When S is turned off, the transistor will continue to conduct until Cg discharges to the threshold value V_{th}. The time interval elapsing from the turning on of S to the cutting off of the transistor is called the memory time. The memory time (tm) is approximately equal to Cg.rl.

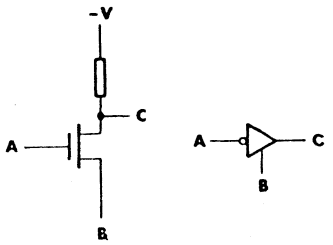


Fig. 3.3 MOS inverter.
Circuit-diagram symbol at right

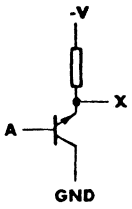


Fig. 3.4 Emitter followers comprise discrete transistors in this calculator

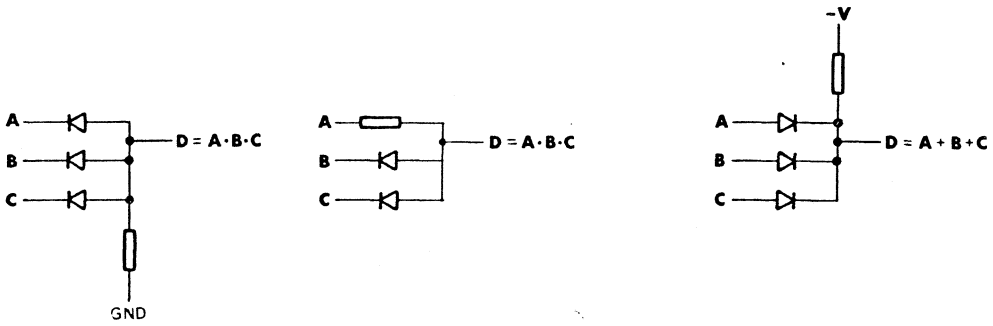


Fig. 3.5 Diode gates. AND gates at left; OR gate at right

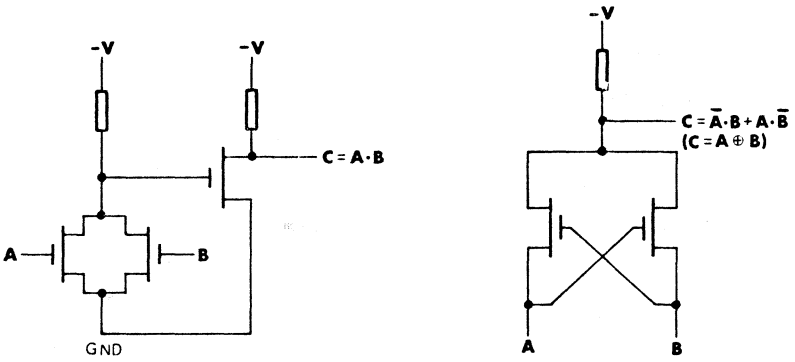


Fig. 3.6 MOS gates. AND gate at left; EXCLUSIVE OR gate at right

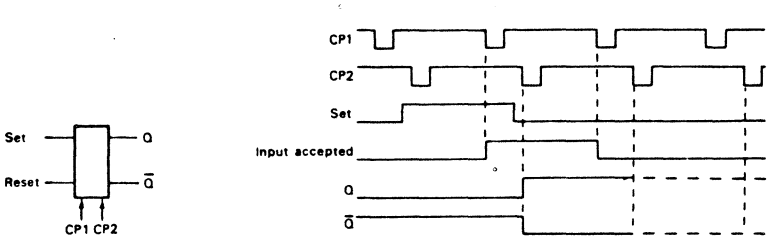


Fig. 3.7 RSS flip-flop

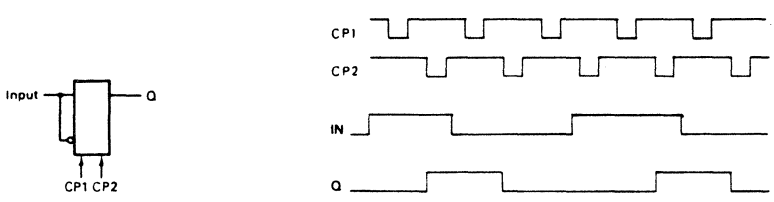


Fig. 3.8 D flip-flop

3.2 INVERTERS

The inverters are built up of discrete transistors or MOS transistors. Discrete inverters are represented by transistor symbols on the circuit diagrams. The MOS inverters are contained in type μPD136 and μPD110 packages. The appearance of the MOS inverters is shown in Fig. 3.3. The package pin numbering is shown in Fig. 2.2.

3.3 EMITTER FOLLOWERS

Certain signals such as the signals from the timing unit (Appendix 3) are used as gating conditions at several points in the calculator, and since they are therefore loaded more heavily than other signals, they are amplified in emitter followers. See Fig. 3.4. All emitter followers comprise discrete transistors, and are represented by transistor symbols on the circuit diagrams.

3.4 GATES

The gates are built up of MOS transistors μPD101, 102, 136 or diodes. Many of the diode gates are contained in integrated diode array packages of type HD 9003 (DN3), HD 9004 (DP4). Fig. 3.5 shows the diode gates used in the calculator, and Fig. 3.6 shows the MOS gates.

3.5 FLIP-FLOPS

Two types of flip-flops are used, namely the RSS flip-flop (μPD135C) and the D flip-flop (μPD134C). Both of these are of the master-slave type and are built up of MOS transistors.

The symbol used to represent the RSS flip-flop on the circuit diagrams appears on Fig. 3.7 which also shows the RSS flip-flop timing diagram. The flip-flop has two clock pulse inputs, CP1 and CP2. The output of the flip-flop follows the input at which the level is high (0 V). If both inputs are at the high level, the set input is dominant, i.e. the flip-flop is 1-set. The input signal is clocked into the master flip-flop by CP1. When CP2 arrives, the content of the master flip-flop is transferred to the slave flip-flop.

The D flip-flop shown in Fig. 3.8 has only one input and, as shown on the timing diagram, the output level follows the input level.

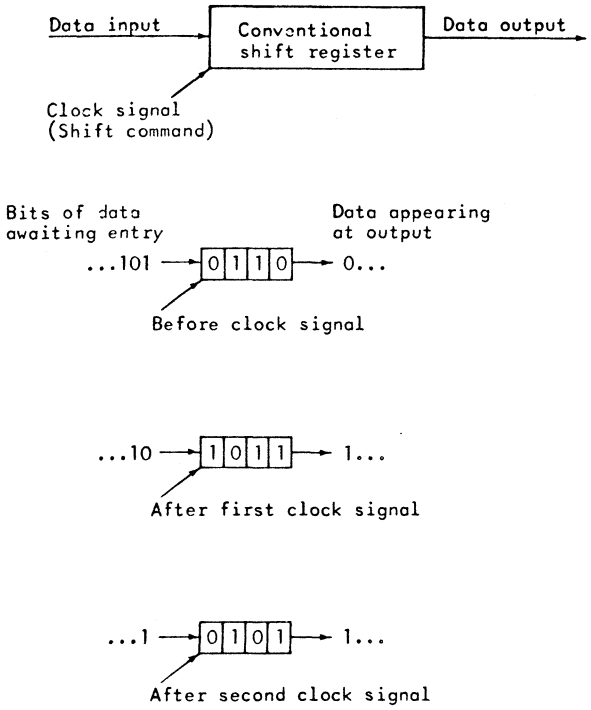


Fig. 3.9 Example of static shift register

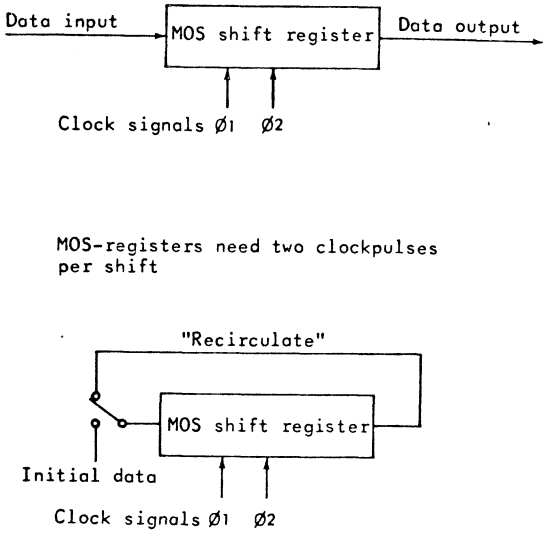


Fig. 3.10 MOS registers are dynamic. Their contents must be end-around shifted repeatedly to prevent destruction

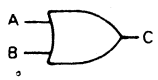
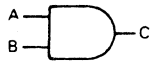
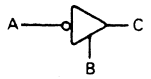
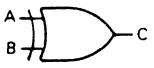
Logic symbol	Truth table A	B	C	Remarks
	L	L	L	OR gate
	H	L	H	A + B = C
	L	H	H	
	H	H	H	
	L	L	L	AND gate
	H	L	L	A·B = C
	L	H	L	
	H	H	H	
	L	L	L	INVERTER with two inputs
	H	L	L	$\bar{A}$·B = C
	L	H	H	
	H	H	L	
	L	L	L	EXCLUSIVE OR gate
	H	L	H	A ⊕ B = C
	L	H	H	
	H	H	L	

Fig. 3.11 Logic symbols with truth tables (complying with MIL standards)

3.6 SHIFT REGISTERS

The shift registers comprise only MOS packages. Four types of shift register packages are used in this calculator. Fig. 2.2 shows the package layout and pin numbering.

Fig. 3.9 shows the function of a conventional shift register with serial input/output. When the clock pulse arrives, the data being fed in is entered into the first position in the register, while the information previously stored at this position is transfered to the next position, etc. A MOS register functions in the same way, but two clock pulses are needed for each shift. The MOS shift registers can be designed in different ways:

1. As a pure dynamic register, which means that the content must constantly be shifted around, otherwise the content will be destroyed.

2. As a static register where clock pulses are applied only when a shift operation is to be carried out (both CP1 and CP2).

3. As a quasi-static register where CP2 is always applied and carries out an internal feedback within the register. CP1 is obtained when a shift is to be carried out.

The number of bits in a shift register may vary. Examples of MOS used in this calculator:

1. μPD 106C (44 + 4 bits)
   μPD 104C (2 x 8 bits)
   HD 709 (2 x 8 bits)

2. The RSS flip-flop, μPD 135C (x register and y register)
   D-type flip-flop, μPD 134C

3. HD 3101 (2 x 8 bits)

3.7 SPECIAL PACKAGES

One special package is used - namely the M 58202, delayed adder, which is described in section 4.4.4.

3.8 SYMBOLS USED IN DIAGRAMS

Truth tables for the logic symbols used on the circuit diagrams are shown in Fig. 3.11. These symbols comply with MIL standards.

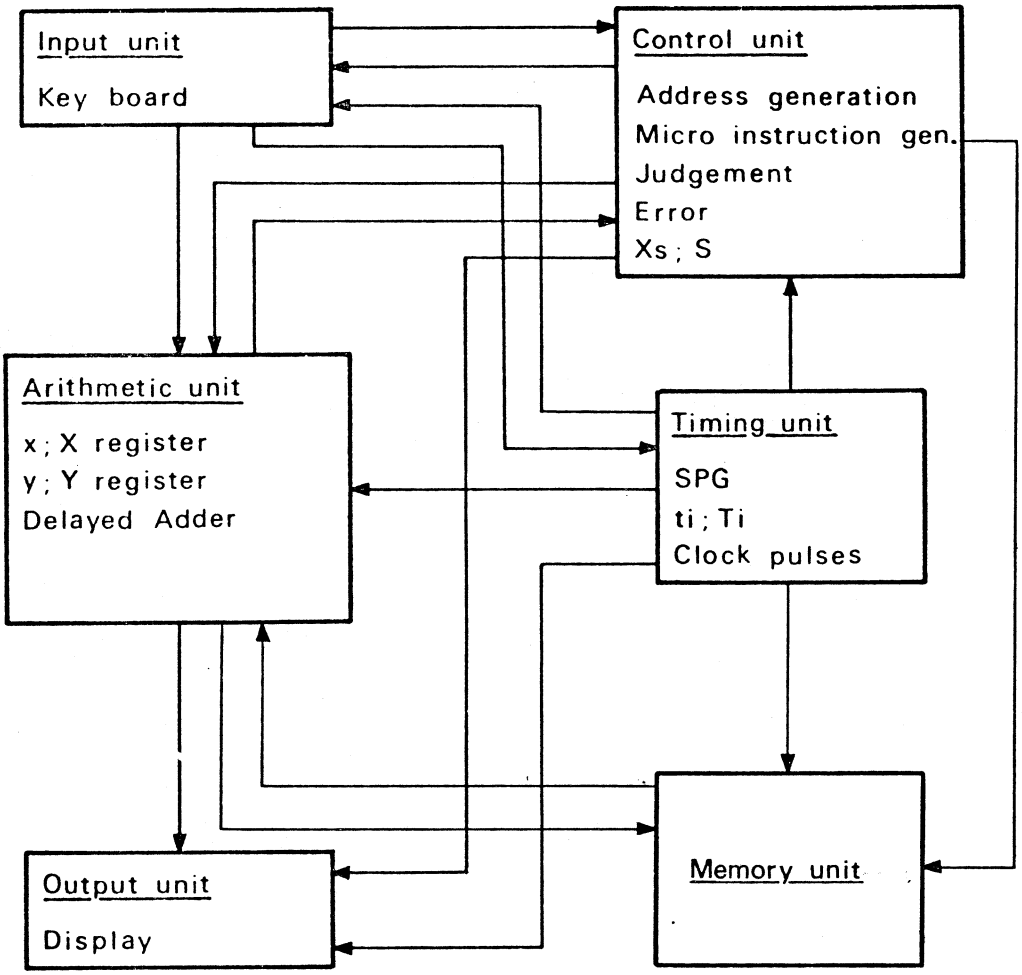


Fig. 4-1 Block diagram of the calculator

4 OPERATION

The calculator comprises six main units. See Fig. 4.1.

Timing unit	Provides the other units with necessary clock pulses.
Arithmetic unit	Carries out operations.
Memory unit	Operates as an accumulating register or store.
Input unit	Enables the operator to enter operands and start calculations.
Output unit	Displays results.
Control unit	Contains the program and control circuits needed to carry out the various calculation operations.

The calculator uses POSITIVE TRUE LOGIC. A logical 1 is represented by a high (H) level (0V to -5V). A logical 0 is represented by a low (L) level (-10V to -24V).

All arithmetic operations in the calculator are carried out as series of sub-operations. These sub-operations are controlled by the address condition(s) existing at a given time. The address conditions generate a number of microinstructions which, via gating systems, connect the circuits that are needed to carry out a given sub-operation. The microinstructions also gate out the required number of shift pulses to the registers. Moreover, they set up the conditions for address changes.

Read-in

Read-in is accomplished by decoding signals from the figure-setting keys and loading the data thus acquired into the X-register. An address set up by this read-in operation generates the microinstructions needed to shift the existing digits in the X-register one position to the left each time that a new digit is read in to the least significant position.

The decimal point key signal causes the x-register to be incremented by one for every digit that is read in after the decimal point key has been depressed. If more than seven decimals are read in, an error indication is obtained (E in the rightmost display tube). This also occurs if more than 14 digits are read in.

Calculation

When a number has been read in, one of the operational keys must be depressed. This sets up certain address conditions that may be used for a later read-in (mult, div) or for starting a calculation or other event.

Depending upon which operational key was depressed, the program will run through particular addresses and the previously read in numbers will be processed at these addresses. Processing involves decimal adjustment, calculation, error checks and the like.

4.1 DESIGNATIONS

a1, a2	- input signals to the full adder (FA)
BC	- boundary code (1111)
CPA,CPC,CPD,CPX,CPY, CPy, CP1,CP2	- clock pulses
CL	- clear signal
CE	- clear entry signal
Co	- correction instruction, $\pm$6 correction
Er	- error indication flip-flop
FA	- full adder (also output for non corrected (binary) addition)
Fc,Hc	- digit and bit carry flip-flops within the full adder
FcR	- signal which inhibits transfer of digit carry between two T-times
Ff	- $\pm$6 correction flip-flop within the full adder
G,F,J,SM	- conditional flip-flops
Key out,10key,11key	- start signals from the keyboard
N1-N3	- address flip-flops
n_0	- initial address
n_1-n_7	- read-in and calculation addresses
P,Q1,Q2	- synchronization flip-flops within the start pulse generator
Rin	- read-in signal (binary coded decimal)
S	- subtraction instruction flip-flop
So	- subtraction instruction to the full adder
Ti(T1-T15),ti(t1-t4)	- digit and bit times
VG	- minus potential (-24 V)
VD	- minus potential (-14 V)
xX,yY	- registers
Xs	- sign flip-flop
Xc	- buffer register within the full adder (4 bits)
Xo	- output for decimal addition (after $\pm$6 correction)

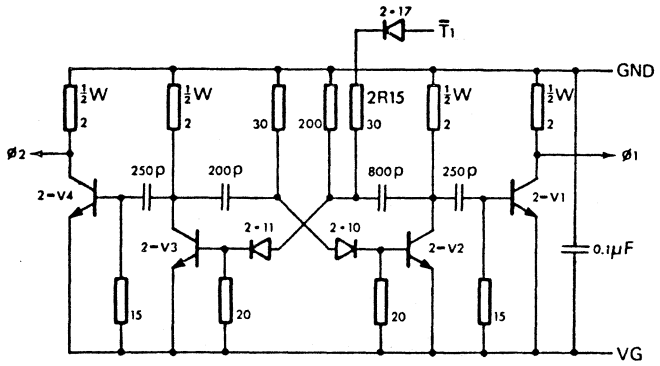


Fig. 4.2 Pulse generator circuit diagram

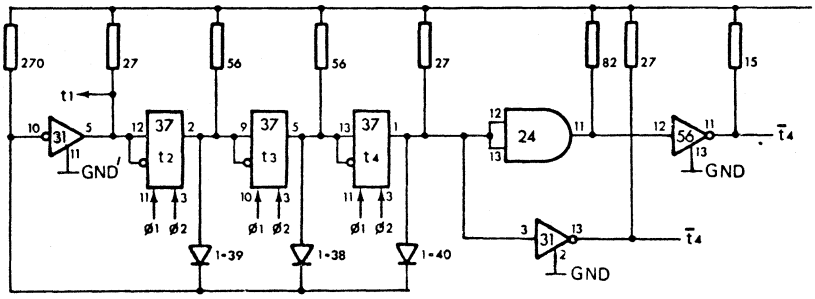


Fig. 4.3 Bit time counter circuit diagram

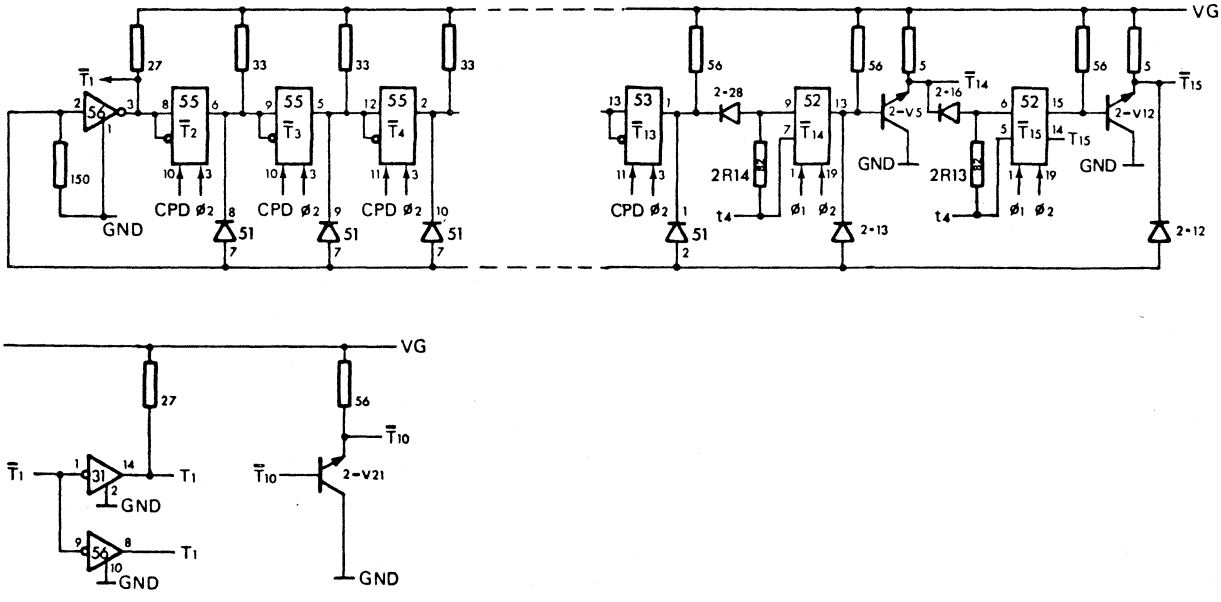


Fig. 4.4 Digit time counter circuit diagram

xd	- signal which indicates that the content of x = 0000
XI_{1-4}	- display register
xD	- decimal point display flip-flop
I_1, I_2, I_3	- address flip-flops used during multiplication/ division
K	- signal which indicates constant operation

4.2 TIMING UNIT

4.2.1 Clock pulse generator

Fig. 4.2 shows the circuit diagram for the clock pulse generator which comprises an approx. 50 kHz multivibrator. The output signals from this multivibrator are differentiated and amplified. From the pulses thus obtained, called Ø1 and Ø2, are derived a number of other timing conditions - particularly bit time pulses. During T1 the frequency is reduced so that T1 becomes longer than the other time intervals. T1 is prolonged so that there will be sufficient time for the address flip-flops that are triggered at the end of the previous timing cycle to be changed and provide the next address before the ensuing timing cycle commence.

4.2.2 Bit time generator

The bit time generator comprises a ring counter built up of three D flip-flops. The counter is clocked by Ø1 and is used to generate bit times (ti ≈ 20 µs). Signal t1 is obtained when all three flip-flops are 0-set.

4.2.3 Digit time generator

The digit times are also generated by a ring counter (see Fig. 4.4). The ring counter comprises 12 D-type FF:s, 2 RSS FF:s, one decoder and one inverter. The decoder ascertains when all flip-flops are 1-set. This is done because the counter generates digit time signals having negative representation (designated $\overline{T1}$ - $\overline{T15}$). Negative representation is used since these signals are intended primarily for the display holding off all except one of the display tubes. The D-type flip-flops are shifted by CPD=t4.Ø1. The RSS flip-flops are triggered by Ø1 but the reset input is taken to t4, thus giving the same effect as triggering by CPD.

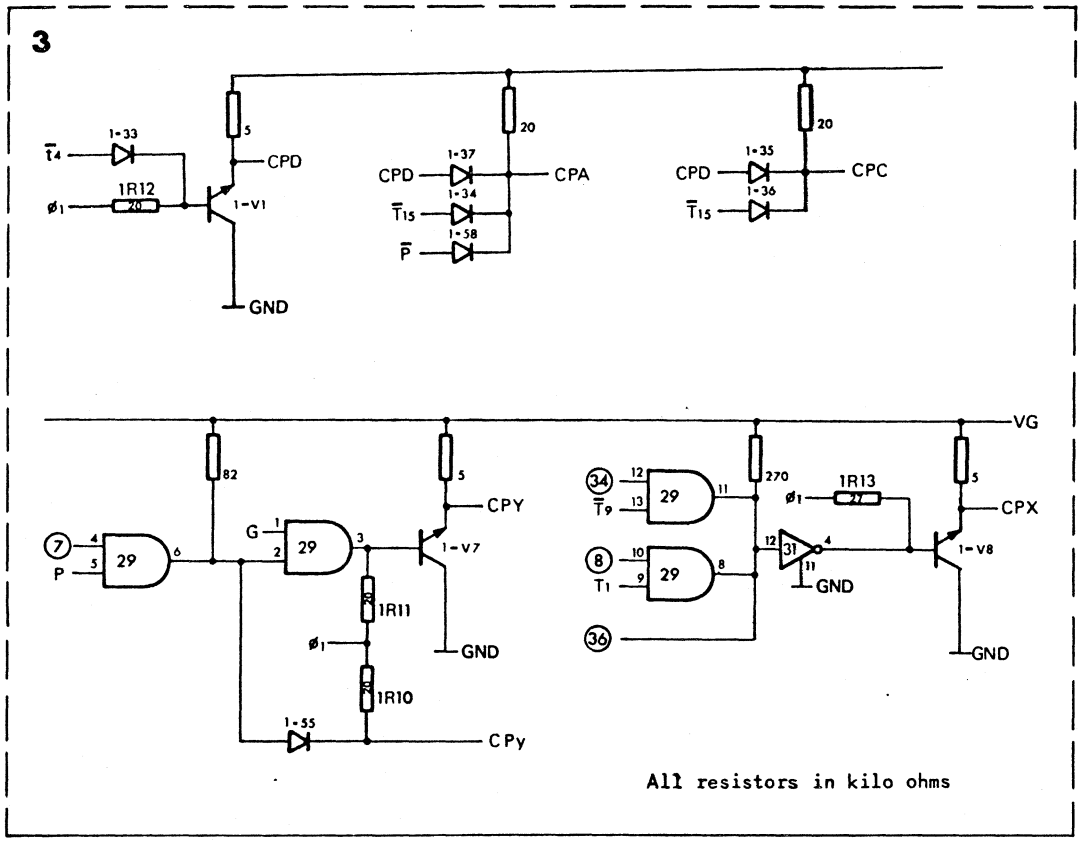


Fig. 4.5 Clock pulse generation

4.2.4 Combined clock pulses

Note that all clock pulses are low-level pulses because of the characteristics of the MOS circuitry. However, they are nonetheless designated $\emptyset 1$, CPD etc. without any inversion bar.

In the calculator a two phase clock system is used where CP2 always is represented by $\emptyset 2$ and where CP1 can be represented by different signals but always in combination with $\emptyset 1$.

The following combined clock pulses are generated. See Fig. 4.5.

CPD = t4.$\emptyset 1$; CPC = T15.CPD and CPA = P.T15.CPD

Clock pulses CPX, CPY and CPy are generated for the registers. These clock pulses are generally gated out by microinstructions. See Fig. 4.5.

CPX = $\emptyset 1.(36 + 34.\overline{T9} + 8.T1)$, used for the x, X and Xc registers.

36 causes clock pulse CPX to be generated during all T times. That state is used for end around shift.

34 provides clock pulses during all T times except T9 and is used for left shift operations.

8 provides clock pulses during T1 only and is used for right shift operations.

CPY = $\emptyset 1.(\overline{7} + \overline{P} + \overline{G})$, used for the Y register
CPy = $\emptyset 1.(\overline{7} + \overline{P})$, used for the y register

$\overline{P}$ provides clock pulses during all T times except P time.

$\overline{7}$ provides clock pulses during all T times.

$.7.P.\overline{G}$ provides clock pulses until the G flip-flop is 1-set after which the generation of clock pulses ceases. This operation is called CPY stop.

The clockpulse for the M-register is CPM = $\emptyset 1$

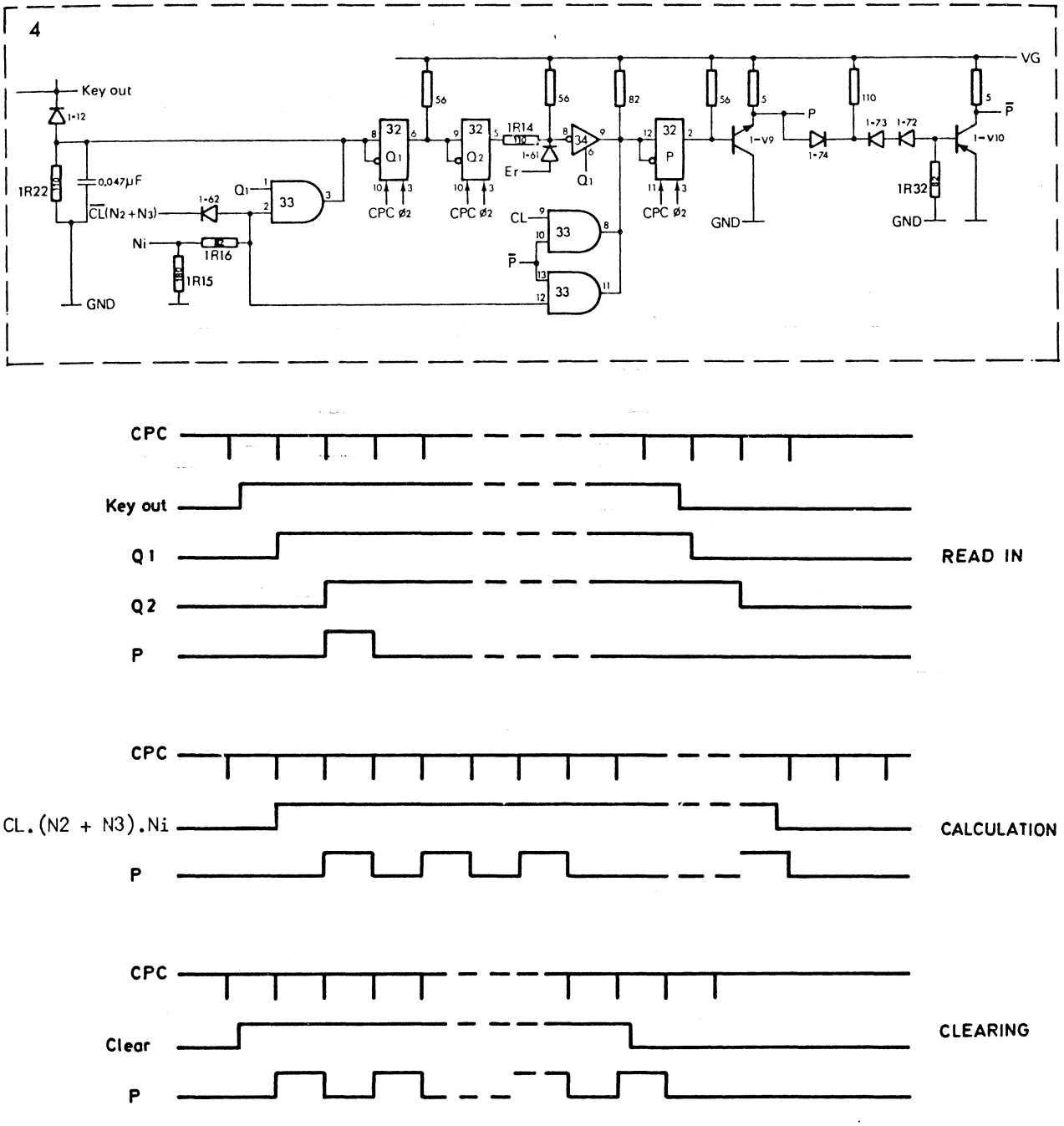


Fig. 4.6 Start pulse generator

4.2.5 Start pulse generator

The start pulse generator circuits are built up of MOS and discrete components. See Fig. 4.6.

It generates P and $\overline{P}$ signals to control the various events within the calculator. During P time digits are read in from the keyboard and program operations are carried out. During $\overline{P}$ time certain tests are carried out and addresses are changed accordingly to alter the subsequent program.

Input conditions for the generator are:

Key out	- signal obtained from all keys except K and C.
Er	- signal from the error flip-flop.
$\overline{CL}.(N2 + N3)$	- address condition that exists only during calculation.
CL	- generated when the clear key is depressed or by ACL signal.
Ni	- input connected to -VG if a Manual-step key is connected.

The start pulse generator comprises three flip-flops, Q1, Q2 and P. Flip-flops Q1 and Q2 synchronise the 1-setting of P to CPC = T15.t4.Ø1.

The condition for Q1 is CPC.(Key out + Q1.Ni.(N2 + N3).$\overline{CL}$). Input Ni is used for manual-step key operation and is then connected to -VG when the key is depressed.

The condition for Q2 is CPC.Q1.

The condition for P is CPC.[Q1.$\overline{Q2}$.$\overline{Er}$ + CL . $\overline{P}$ + Ni(N_2 + N_3) $\overline{CL}$.$\overline{P}$]

Q1.$\overline{Q2}$.$\overline{Er}$	is obtained in read-in addresses and manual-step key operation and initiates one P time for every Key out signal.
Ni(N_2 + N_3)$\overline{CL}$.$\overline{P}$	is obtained to control the generation of P cycles during calculation, ($\overline{P}$,P,$\overline{P}$,P,$\overline{P}$,P,$\overline{P}$). Note that Ni means that no external connection exists. When manual-step key is used the Ni input is connected to -VG via the key and results in the logic expression $\overline{Ni}$ when the key is depressed.
CL.$\overline{P}$	is obtained when the C-key is depressed and generates a $\overline{P}$ P $\overline{P}$ P pulse train as long as the key is depressed. The CL signal is also generated by the signal ACL.

An error, obtained, in normal operation has no influence on the calculation program. However the signal Er inhibits the generation of P-signals at the end of the operation. A new number can not be read in until the [C] -key has been depressed.

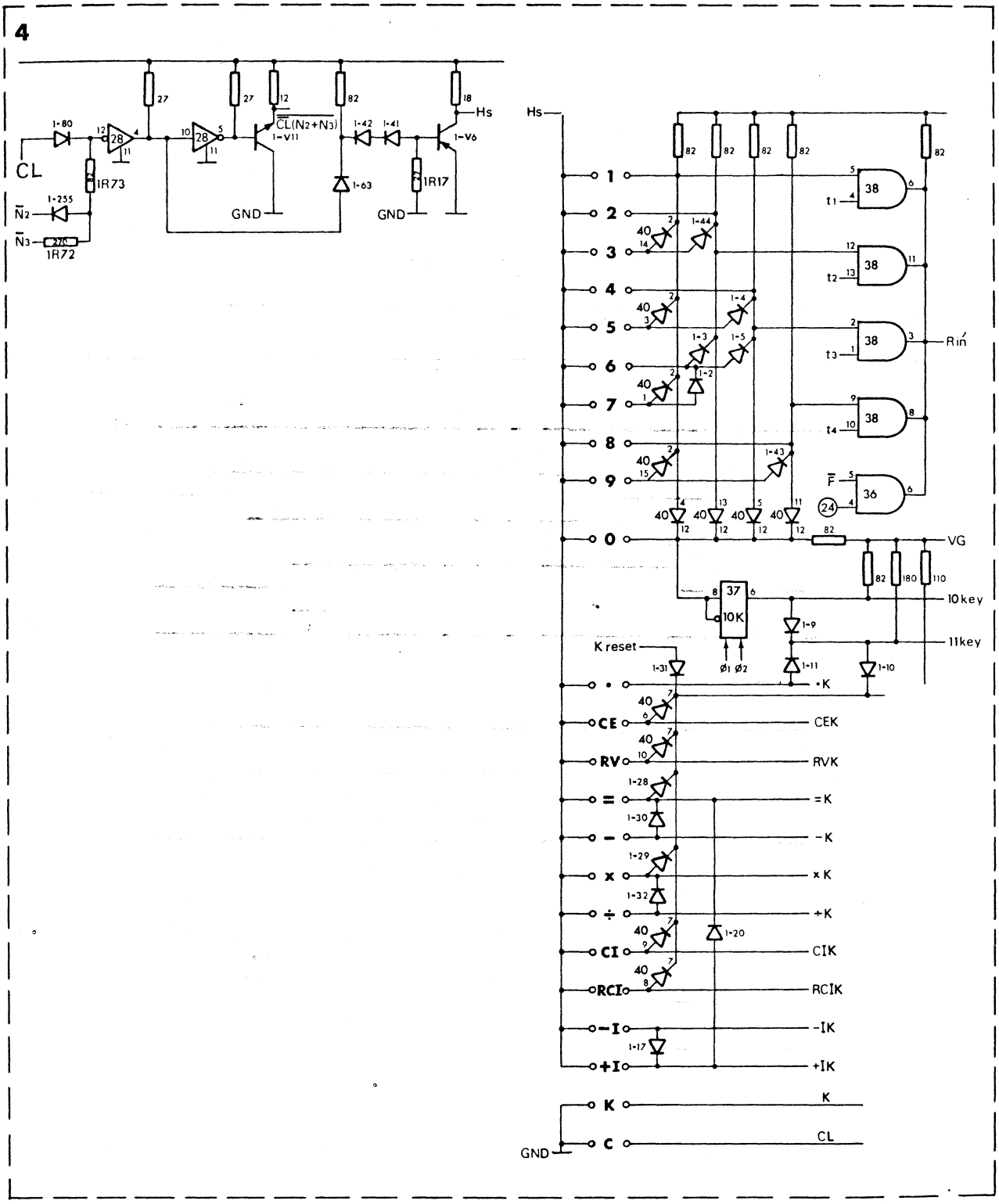


Fig. 4.7 Generation of Hs signal

If an error is obtained during manual-step key operation, no further step operations are possible.

In either case the clear key must be depressed before any new operations can be started.

4.3 INPUT UNIT

The input unit enables the calculator operator to insert operands and initiate calculations. The unit comprises figure setting keys, operational keys and a decimal selector.

4.3.1 Figure setting keys

The figure setting keys are only operative when Hs = 1 (see Fig. 4.7). $Hs = \overline{\overline{CL}.(N_2 + N_3)} = CL + \overline{N2}.\overline{N3}$ and will thus be high at addresses n0 + n1 only.[x] The key signal for each digit is converted to BCD code and gated with bit time signals to give a serial Rin.

Key	Rin'			
	t4	t3	t2	t1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Rin' inserts the digit into the X-register as described later. Each digit key also gives 10key → 11key → Key out. Key out initiates a P signal during which the digit is read in. The ⊡ -key provides 11key → Key out. Key out initiates a P signal, during which flip-flop F is 1-set, causing subsequent digits to be considered as decimals.

[x] Note that the depressing of the C -key also provides Hs = 1. It is thus possible to read in a digit to position X1, but when the digit key is released the X-register is immediately cleared again.

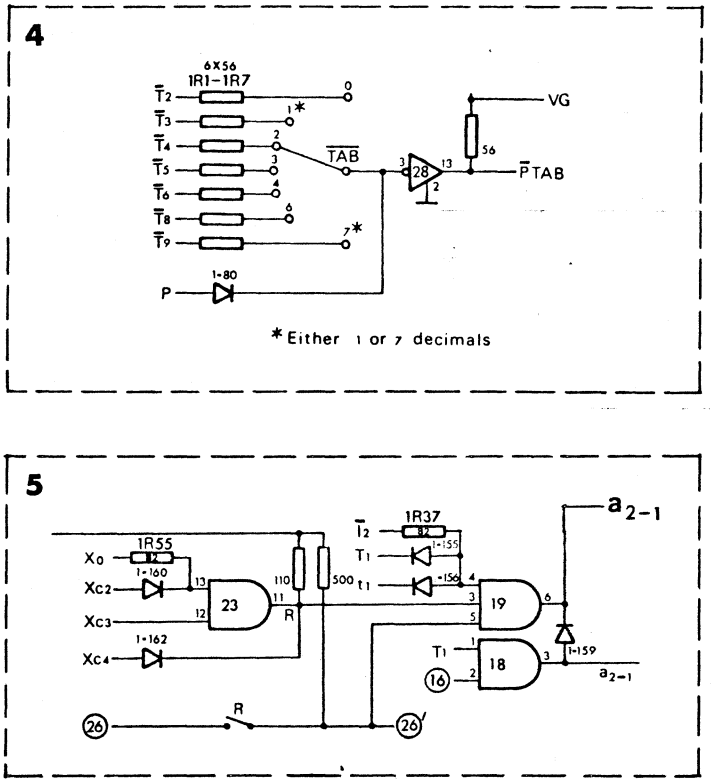


Fig. 4.8 Decimal selector circuit diagram and Rounding circuits

4.3.2 Operational keys

The operational keys, with the exception of [C] and [K] are only operative when (n0 + n1) → Hs. Each key, with the same exceptions, gives Key out to initiate a P signal. Each key controls one or more addresses which become operative during P. The addresses, in turn, generate the micro instructions and address changes needed to start calculation at the appropriate addresses.

The effect of each operational key is:

[CE] 0 → xX and Xs

[RV] xX ⟷ yY, Xs ⟷ Ys

[x] generates the conditions for multiplication

[:] generates the conditions for division

[CI] 0 → mM and Ms

[RCI] mM → xX, xX → yY and Ms → Xs → Ys

[K] ensures that the constant operand is perserved

[C] 0 → xX and Xs, 0 → yY and Ys

[+I] initiates the last read in operand or the result of an mult/div to be added to the store content

[-I] initiates the last read in operand or the result of an mult/div to be subtracted from the store content

[=] [-] initiate the different calculations. Depressing [=] provides the last operand read in to be added to the earlier result. Depressing [-] provides the last operand read in to be subtracted from the earlier result. The operation initiated by depressing [=] or [-] will be performed as addition or subtraction, depending upon the sign of the previous result. [=] and [-] also initiate a mult/div operation if [x] or [:] was previously depressed. The sign of the answer will be positive or negative depending upon the signs of the two operands.

4.3.3 Decimal and Rounding selector

This selector switch is used to determine the number of decimals of operands (Fig. 4.8). A T pulse is selected which, gated with P, gives signal $\overline{P}$.TAB. Thus if, for example, 4 is selected $\overline{P}$.TAB = 1 at T6. At position R this switch can be used for rounding operations, R.Xc ⩾ 5.$\overline{I2}$.T1.t1 provides +1 to X. Note that R provides 26.

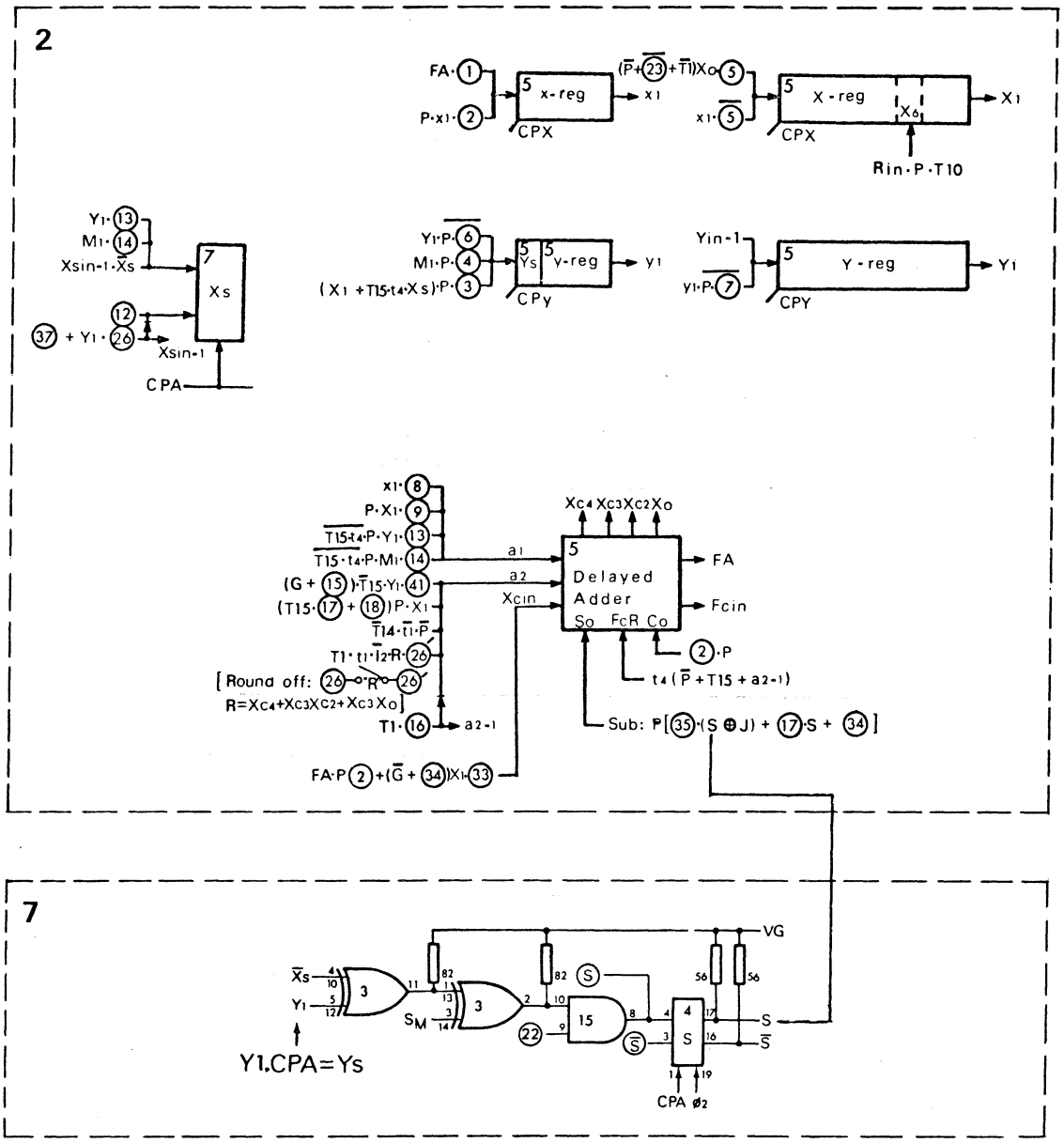


Fig. 4.9 Arithmetic unit sub-units

4.4 ARITHMETIC UNIT

The arithmetic unit includes two 56-bit registers designated X-register and Y-register. One 4-bit register designated x-register, one 1+3 bit-register designated y-register (Ys and y1 through y3) and one flip-flop designated Xs. Moreover it contains a Delayed Adder with addition circuits, into which are incorporated correction circuits and a 4-bit register designated Xc. See Fig. 4.9.

4.4.1 Registers

The X- and Y-registers are built up by either HD 709 or μpD 141C MOS IC. Each contains two 8-bit quasi-static shift registers. They are used for administration of the numbers being processed and for calculation. The x-register keeps track of the number of decimals in the X-register content. The y-register keeps track of the number of decimals in the Y-register content. Note that the sign flip-flop Ys is part of the y-register.

Both x-register and y-register consist of four D-type flip-flops. The X-register has two inputs, located at bit 4 of position 14 and bit 4 of position 6. The latter input is used for reading in numbers from the keyboard and for applying the boundary code (BC) used in multiplication and division. The input to the Y-register is at bit 4 of position 14. The inputs to the x-register and the y-register are both at bit 4.

4.4.2 Xs flip-flop

This flip-flop indicates the sign of the number in the X-register and determines the sign condition on the display. The signal Xs is used in connection with signals Ys and SM to determine whether the S flip-flop should be 1-set or not. The state of the S flip-flop is used to determine whether addition or subtraction shall be performed in the adder circuits. Note that S is not the abbreviation for Subtraction.

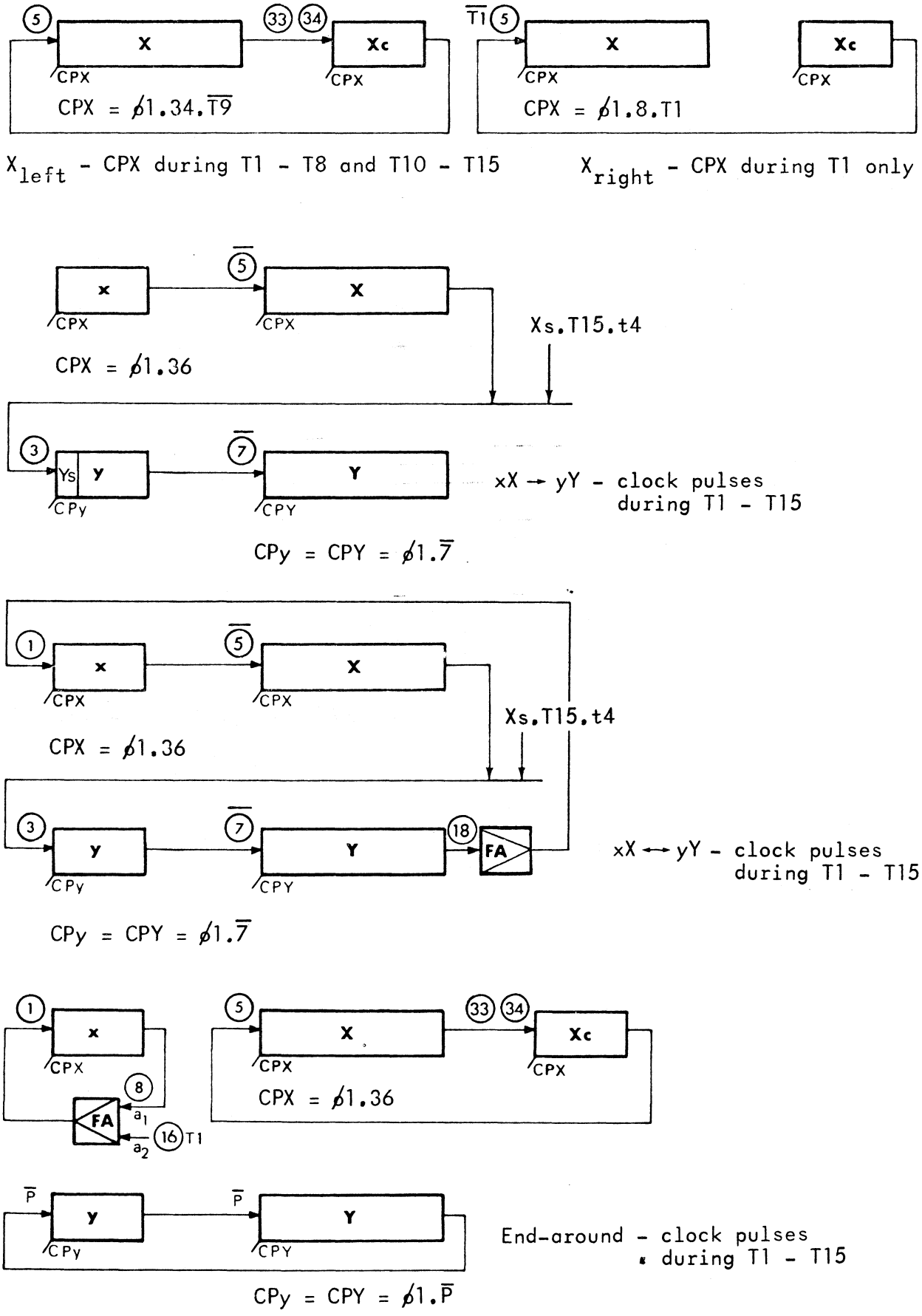


Fig. 4.10 Register connections and timing for shift operations

4.4.3 Register shifts

The calculator carries out the following shifts: left shift, right shift, X → Y shift, X ←→ Y shift and end-around shifts. See Fig. 4.10.

- A left shift can only be carried out in the X-register. To carry out this shift, the X-register and Xc-register are coupled together (comprising 15 positions) and shift pulses are sent to the registers during all T-times except T9. The result is a 14-position end around shift to the right which is equivalent to a left shift.

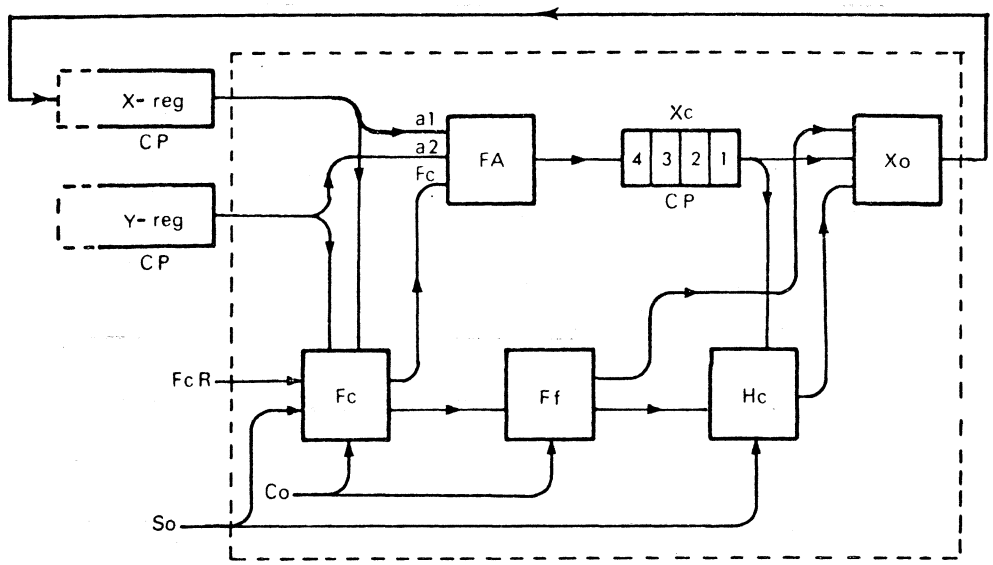
- A right shift can be carried out in both X-register and Y-register. The X-register is shifted to the right by receiving shift pulses only during time T1. Note that X1 is not connected to the Xc-register.x) The Y-register is right shifted by incoming shift pulses until its content reaches the rightmost position, after which the shift pulses stop. This operation is called CPY stop and occure only in multiplication and division operations. CPY = $\emptyset 1.\bar{G}$, which means that CPY is inhibited when G is 1set.

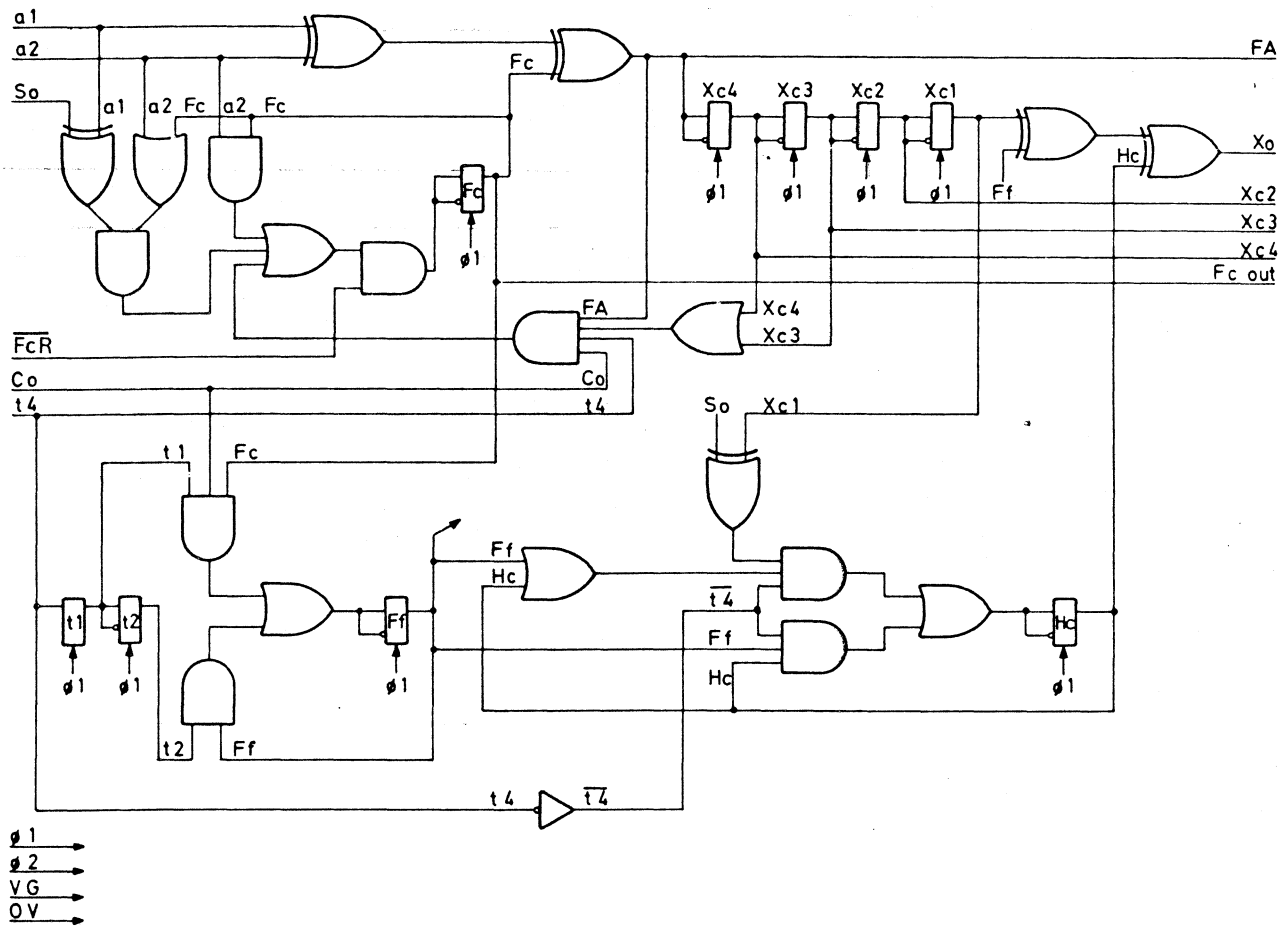
- For an X → Y shift, the content of the X-register is transferred to the Y-register. The contents of the x-register and sign flip-flop Xs are also transferred to the y-register.

- For an X ←→ Y shift, the content of the X-register is transferred to the Y-register and vice versa via the delayed adder (FA). This also includes x ←→ y and Xs ←→ Ys.

- All registers are repeatedly end-around shifted unless otherwise instructed. This takes place during $\overline{P}$ time. End-around shift of the xX-register is necessary for display purposes.

x) In Round off operations (k31), X1 and Xc are connected.





$$Fc = \overline{FcR}.\left[\overline{So}.a1.(a2 + Fc) + So.\overline{a1}.(a2 + Fc) + a2.Fc + t4.FA.Co.(Xc4 + Xc3)\right]$$

$$FA = \overline{a1}.\overline{a2}.Fc + a1.\overline{a2}.\overline{Fc} + \overline{a1}.a2.\overline{Fc} + a1.a2.Fc$$

$$Ff = t1.Fc.Co + t2.Ff$$

$$Hc = \overline{t4}.\left[\overline{So}.Xc1.(Ff + Hc) + So.\overline{Xc1}.(Ff + Hc) + Ff.Hc\right]$$

$$Xo = \overline{Xc1}.\overline{Ff}.Hc + Xc1.\overline{Ff}.\overline{Hc} + \overline{Xc1}.Ff.\overline{Hc} + Xc1.Ff.Hc$$

Fig. 4.11 Block diagram and logic diagram for the full adder

4.4.4 Full adder

All arithmetic operations can be broken down into additions, shifts and complement-forming operations. It is assumed that the reader is familiar with this aspect of design. Basic theory is beyond the scope of this manual.

All arithmetic operations carried out in this calculator make use of an MSI package of type M58202. This package contains the circuits needed for addition and subtraction of two binary numbers. Fig. 4.11 presents a block diagram and logic diagram for the full adder. The logic expressions that describe the functioning of the full adder also appear in Fig. 4.11. These expressions are referred to in connection with the examples of addition and subtraction.

Signals

a1, a2 — are inputs for the serial BCD numbers from the outputs of invidual registers. See block diagram in Fig. 4.11.

FA — is the binary result of the operation (a1 + a2) or (a1 - a2).

Fc — is obtained in connection with the generation of carry digit (bit carry or digit carry).

So — determines whether subtraction (So = high level) or addition ($\overline{So}$ = low level) shall be carried out within the full adder. The signal So can be expressed as $So = P.\left[34 + 17.S + 35.(S \oplus J)\right]$ where the level of the signal S depends on the sign of the numbers being processed and the key depressed on the keyboard. See Fig. 4.12.

Xc — is a 4-bit buffer register used for temporary storage of results obtained from FA (note that Xc effects a delay of one digit time, by which time the correction is available).

Xo — is the result (in serial BCD form) of the operation a1 + a2 or a1 - a2 after correction. This signal output is connected directly to the X-register where the calculated result is stored.

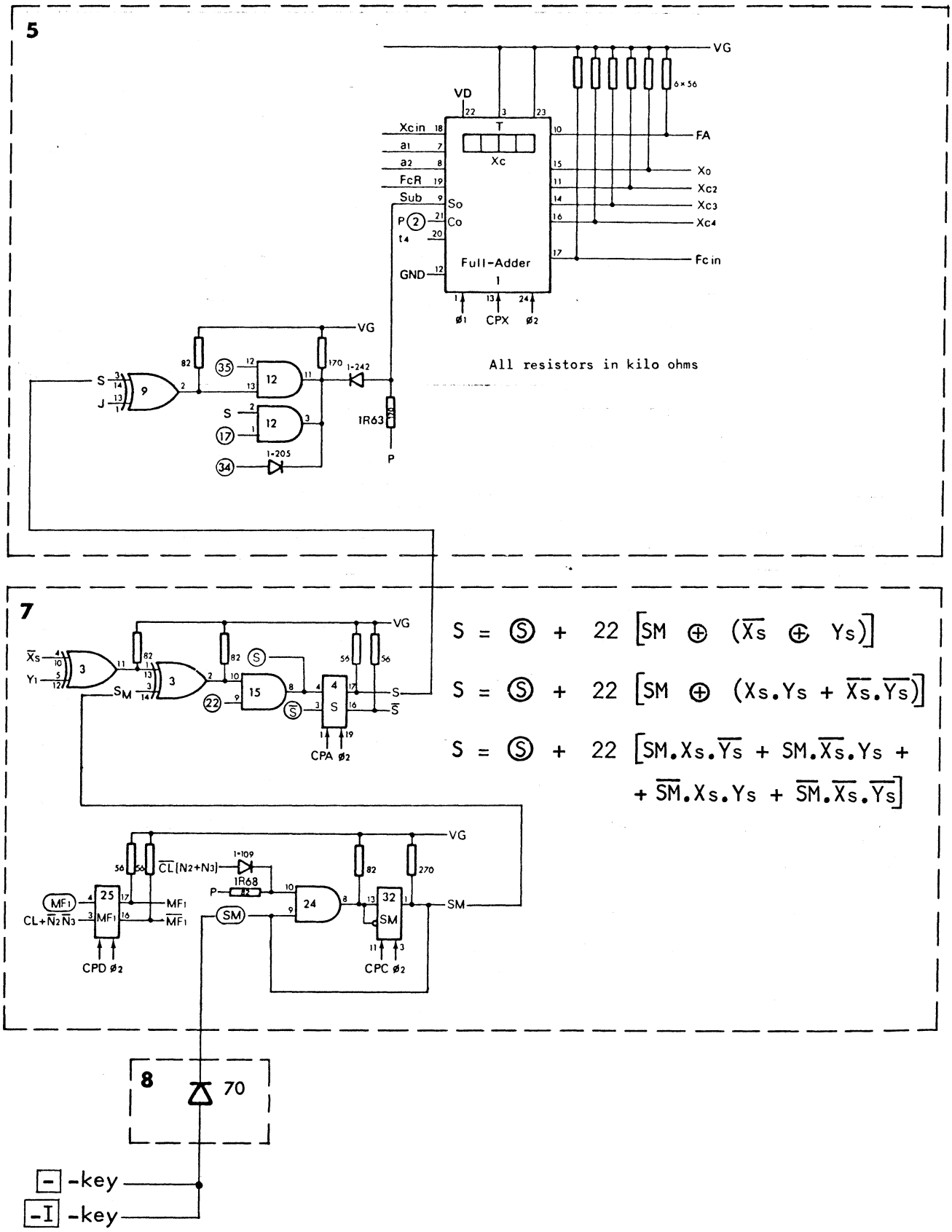
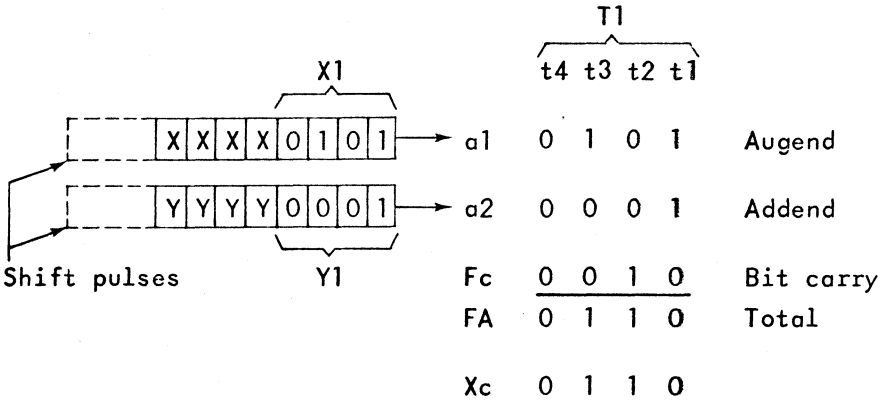


Fig. 4.12 Circuits for generation of add/sub instructions for the full adder

Co	indicates whether the binary result FA shall be corrected or not. The signal Co depends on microinstruction 2 (Fig. 4.12). Signal Co exists as a high-level signal at all addresses containing microinstruction 2. Correction is initiated by the generation of digit carry, i.e. when the content of Xc >9 (>1001). This correction is delayed one T time (one digit position) and the package is thus called the "Delayed full adder".
Ff	is the correction flip-flop.
Hc	is the carry flip-flop used in connection with correction.
$\overline{t4}$	inhibits transfer of correction carry to the next digit position.
$\overline{FcR}$	inhibits the transfer of digit carry to the next T cycle.
Ø1, Ø2	are clock pulses for the register and flip-flops in the full adder package.

Simple addition example

The following example shows how the operation 5 + 1 = 6, i.e. 0101 + 0001 = = 0110 is carried out. The digit 5 can thus be considered the least significant digit in a number stored in the X-register while the digit 1 is the least significant digit in a number stored in the Y-register.



The decimal number is represented in NBCD (Natural Binary Coded Decimal) code, sometimes referred to as 8,4,2,1 code. In this code, the binary equivalent of every digit takes up four bit positions (5 becomes 0101 for example). The contents of the two registers are sent bit by bit, to the full adder - inputs a1 and a2. After four bit times (T1.t1 through T1.t4) the contents of positions X1 and Y1 (least significant positions) in the two register have been added one bit at a time in the full adder and stored in buffer register Xc. The above example shows the situation that prevails after time T1.

Description:

T1.t1 — During T1.t1, the condition for bit carry (Fc) is generated since Fc = $(\overline{FcR}.\overline{So})$.a1.a2. This bit carry will exist during T1.t2 since flip-flop Fc is 1-set at T1.t2.Ø2. The binary result obtained from FA will thus be FA = = 1 + 1 + 0 = 0 which is stored in Xc4 during T1.t2.

T1.t2 — During T1.t2 no condition for bit carry is generated. The binary result obtained from FA will then be FA = 0 + 0 + + 1 = 1. This result is stored in Xc4 at the same time that the previously stored 0 is shifted to positon Xc3.

T1.t3 — Since no condition for bit carry was generated during T1.t2, Fc is 0-set at T1.t3.Ø2 and the result obtained from FA will be FA = 1 + 0 + 0 = 1.

T1.t4 — During T1.t4, FA will provide 0 + 0 + 0 = 0.

Addition example that results in digit carry

In the example 5 + 7 = 12, illustrated below, binary coded digits are added using ordinary binary addition. The total (>9) calculated during T1 results in a digit carry **1** to the next digit position, whereupon the code for six (0110) will be added to the content of Xc during T2, thus providing the correct total for the units digit **2.**

T1

	t4			t1	
a1	0	1	0	1	
a2	0	1	1	1	
Fc	1	1	1	0	
FA	1	1	0	0	>9

T2

	t4			t1					
a1	0	0	0	0	Xc1	1	1	0	0
a2	0	0	0	0	Ff	0	1	1	0
Fc	0	0	0	**1**	Hc	1	0	0	0
FA	0	0	0	1	Xo	0	0	1	0 = **2**

T3

	t4			t1					
a1	0	0	0	0	Xc1	0	0	0	1
a2	0	0	0	0	Ff	0	0	0	0
Fc	0	0	0	0	Hc	0	0	0	0
FA	0	0	0	0	Xo	0	0	0	1 = 1

Xc1	0	0	0	0
Ff	0	0	0	0
Hc	0	0	0	0
Xo	0	0	0	0

T1.t1 — $(\overline{FcR}.\overline{So}).a1.a2$ provides bit carry, FA = 1 + 1 + 0 = 0.

T1.t2 — $(\overline{FcR}.\overline{So}).a2.Fc$ provides bit carry, FA = 0 + 1 + 1 = 0.

T1.t3 — $(\overline{FcR}.\overline{So}).a1.(a2 + Fc)$ provides bit carry, Fa = 1 + 1 + + 1 = 1.

T1.t4 — $\overline{FcR}$.t4.FA.Co.(Xc4 + Xc3) provides digit carry **1** to the next digit position, FA = 0 + 0 + 1 = 1. Digit carry initiates a six-correction operation, i.e. addition of 0110 to the content of Xc. This correction will be carried out during T2. See timing diagram in Fig. 4.13.

T2.t1 — t1.Fc.Co provides the 1-setting condition for flip-flop Ff which will be 1-set by T2.t2.Ø2, Xo = 0 + 0 + 0 = 0 and (FA = 0 + 0 + **1** = 1).

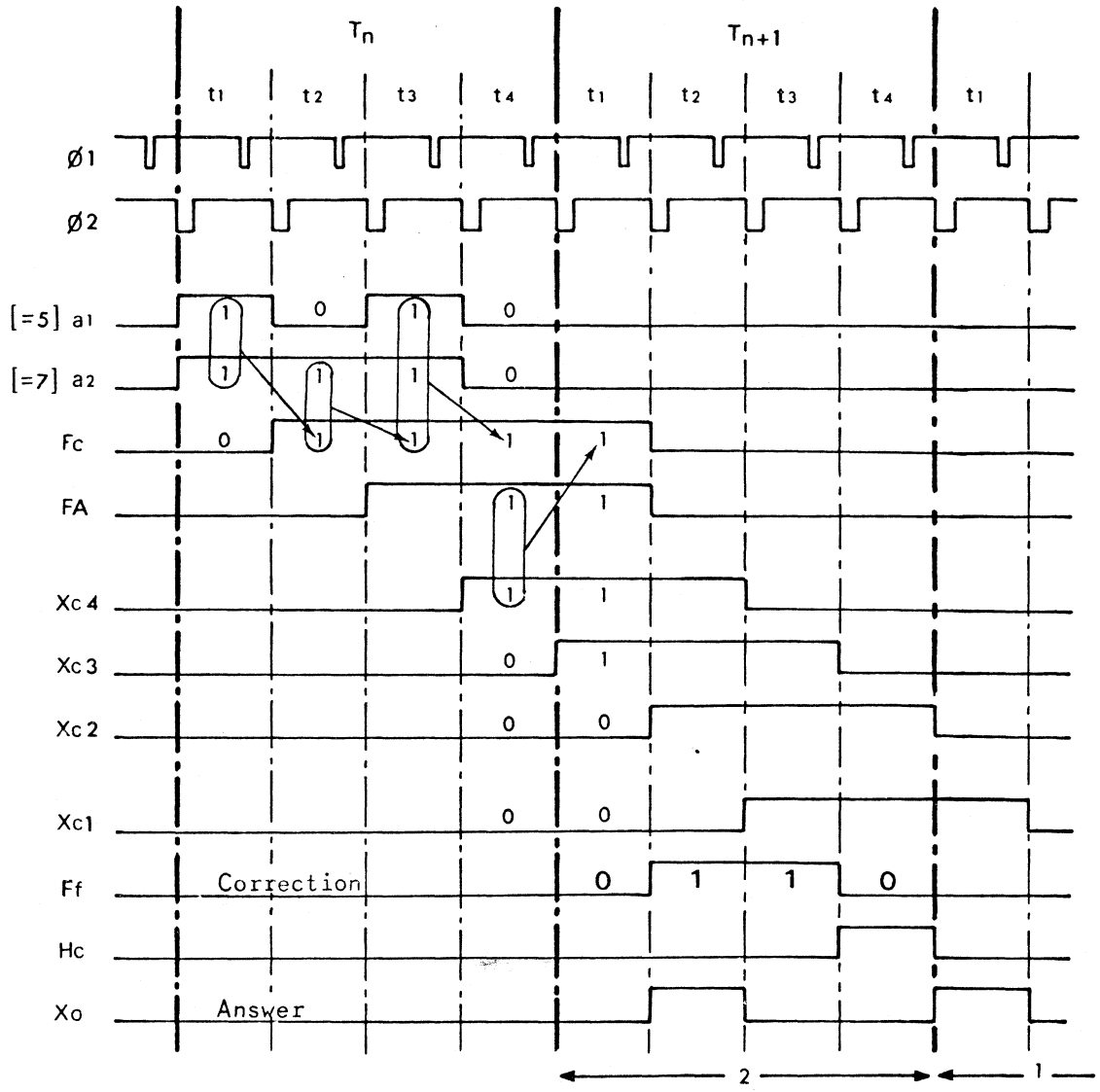


Fig. 4.13 Timing diagram for the addition 5 + 7 = 12 with subsequent correction. Note that this diagram is drawn as displayed on an oscilloscope screen

T2.t2 — t2.Ff provides the 1-setting condition to flip-flop Ff which will thus remain 1-set during T2.t3, Xo = 0 + 1 + + 0 = 1.

T2.t3 — During t3, Ff does not retain its 1-setting condition, and is thus 0-set at T2.t4.Ø2, Xo = 1 + 1 + 0 = 0, but $(\overline{t4}.\overline{So})$.Xc1.Ff provides bit carry (Hc).

T2.t4 — The condition $\overline{t4}$ in the expression for Hc inhibits carry to the next digit position, Xo = 1 + 0 + 1 = 0.

Summary:

Binary addition is thus carried out during T1 and corrected during T2. The units digit thus obtained (in this case 0010 = **2**) is sent to the X-register. During T2, the binary result obtained from FA = 0001 = 1 is stored in the buffer register Xc. During T3 no correction is made, and as a result the content of Xc is sent uncorrected to the X-register.

The full adder also functions as described above for multi-digit numbers.

Subtraction with positive difference

Subtraction can be carried out as addition of the minuend to the tens complement of the subtrahend. The logic design needed to carry out this procedure is quite simple, but requires a relatively large number of circuit functions. However, whether the operation is A + B + Fc or A - B + Fc (borrow), the generation of FA is the same, only conditions for carry or borrow changes. In subtraction the correct borrow will be obtained by replacing a1, in the Fcin expression, by $\overline{a1}$. In this calculator therefore during addition Fcin = $\overline{FcR}.\overline{So}.a1.(a2 + Fc)$ and during subtraction Fcin = $\overline{FcR}.So.\overline{a1}.(a2 + Fc)$.

Another matter that should be explained before proceeding further is that the logical relationship between the signs of the numbers and the operational key that was depressed determines whether subtraction (or addition of two negative numbers) shall be carried out in the full adder. See logical derivation of the subtraction signal S in Fig. 4.12. The signal S is included as one condition for Sub signal P. 35(S ⊕ J) + 17.S + 34.

The following example illustrates the operation 8 - 3 = 5.

T1

	t4	t1
a1	1	0 0 0
a2	0	0 1 1
Fc	1	1 1 0
FA	0	1 0 1

T2

	t4	t1		
a1	0	0 0 0	Xc1	0 1 0 1
a2	0	0 0 0	Ff	0 0 0 0
Fc	0	0 0 0	Hc	0 0 0 0
FA	0	0 0 0	Xo	0 1 0 1

T1.t1 ($\overline{FcR}.So).\overline{a1}.a2$ provides bit carry, FA = 0 + 1 + 0 = 1.

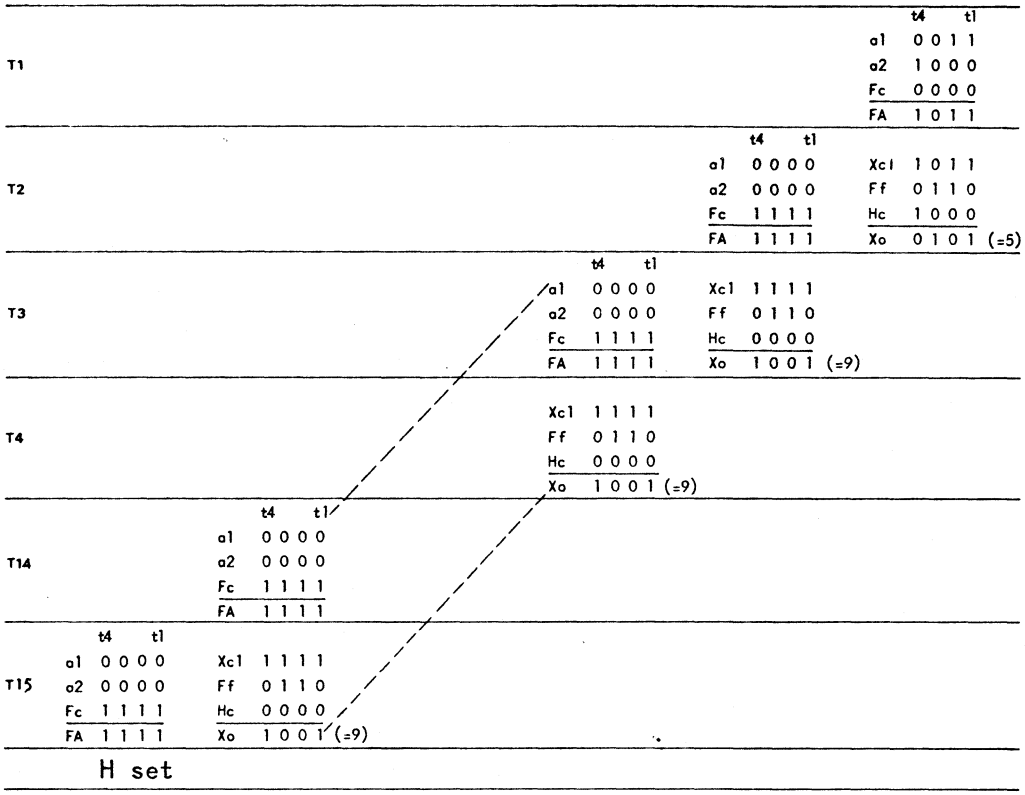
T1.t2 ($\overline{FcR}.So).\overline{a1}.(a2 + Fc)$ provides bit carry, FA = 0 + 1 + + 1 = 0.

T1.t3 ($\overline{FcR}.So).\overline{a1}.Fc$ provides bit carry, FA = 0 + 0 + 1 = 1.

T1.t4 During t4 the condition for generation of bit carry is not fulfilled, FA = 1 + 0 + 0 = 0.

The calculated result 0101 (5) is stored in Xc and transferred to the X-register during T2.

Step I



Step II

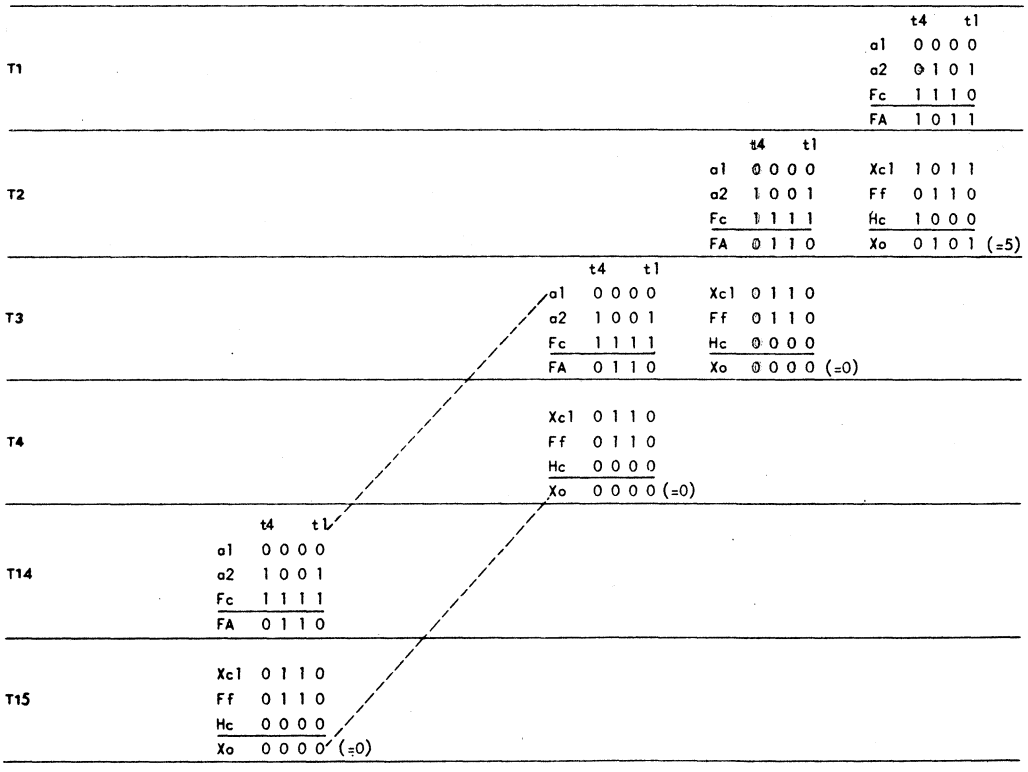


Fig. 4.14 Subtraction example: 3 - 8 = -5

Subtraction with negative difference

The operation 3 - 8 = -5 can be used as an example of subtraction with negative difference. This is carried out in two steps in the calculator. The first step provides the answer 99999999999995. This is the complement of the final answer. Complement formation provides a BC in Xc. When this is sensed, the program is modified so that the operations 0 - 99999999999995 and Xs invert will be carried out. The answer will then be presented correctly and the sign circuits will keep track of the sign. See example in Fig. 4.14.

Step 1:

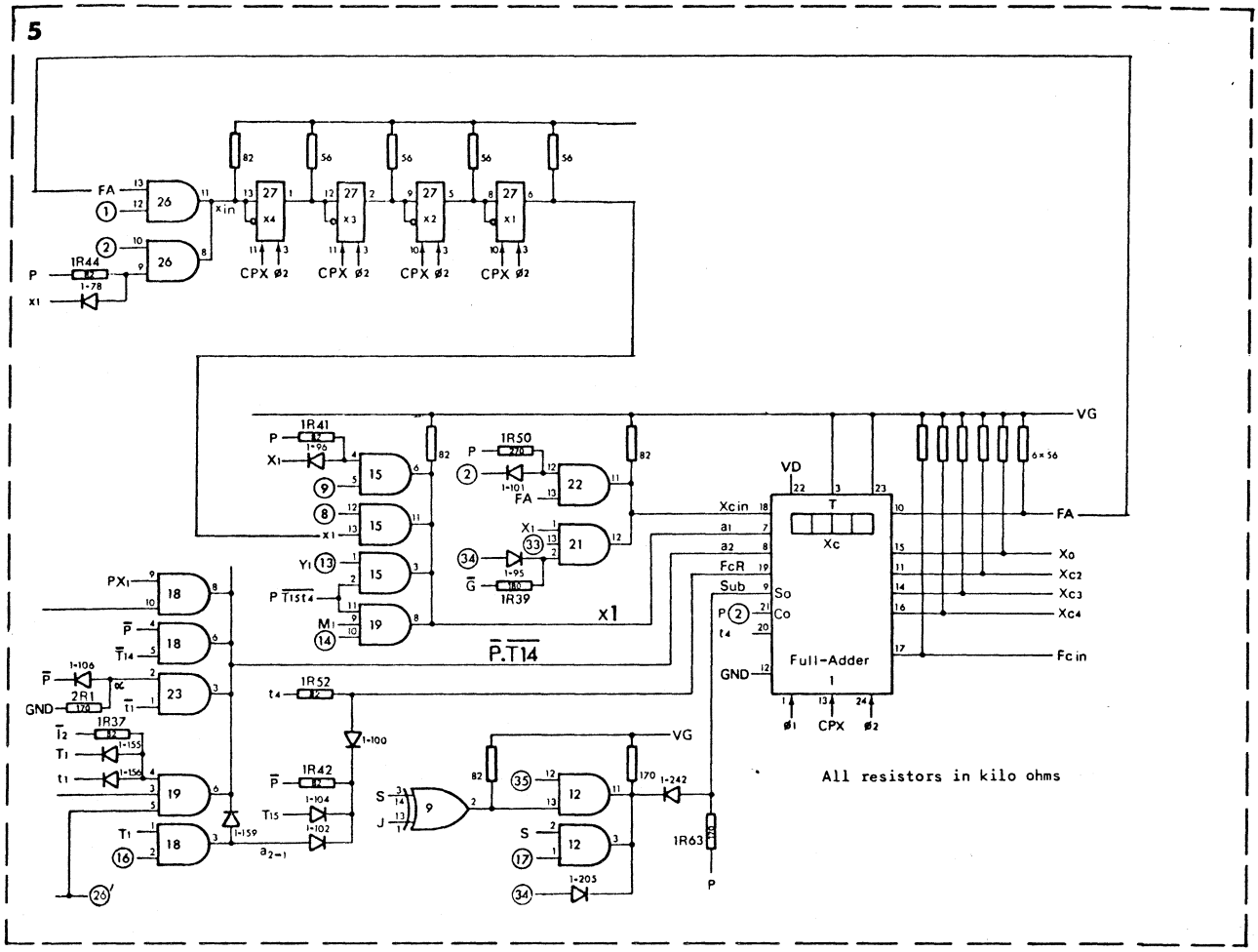
T1.t1 through T1.t4 — Bit carry is generated according to the expression Fc = $= \overline{FcR}.So.\overline{a1}.(a2 + Fc)$. During t4 the condition for digit carry is generated, and as a result a six-correction will be carried out during T2.

T2 through T14 — Condition $\overline{FcR}.So.\overline{a1}.Fc$ will provide carry during all bit times, and consequently the complement of the result will be formed.

T15 — Xc was initially 0000. 1111 will be added, giving a BC. During the subsequent $\overline{P}$ time J will be 1-set by BC, causing step 2.

Step 2:

At the new address, the operation 0 minus the complement will be carried out. As a result, the answer will be presented correctly (with minus sign).




```
T1:      a1 1000
         a2 1111
         Fc 0000
T2: a1= FA 0111 = 7
         a2 1111
         Fc 1110
    a1= FA 0110 = 6

T3:              = 5
T4:              = 4
 .                .
 .                .
 .                .
T8:              = 0
T9:      a1 0000
         a2 1111
         Fc 0000  → Fcin.
T10:a1= FA 1111 = 15
         a2 1111
         Fc 1110
    a1= FA 1110 = 14

T11:             = 13
T12:             = 12
T13:             = 11
T14:     a1 1011
(P.T14.t1) a2 1110
         Fc 1100
T15:a1= FA 1001 = 9
         a2 1111
         Fc 1110
         FA 1000 = 8
```

Fig. 4.15 Example of decrementing the x-register during $\overline{P}$-time

End-around shifting of x during $\overline{P}$ time

During $\overline{P}$ time (k0) the content of x is circulated through FA, 14 times while X circulates through Xc once. Each time, x is decremented, to maintain a record of the decimal point position in X.

The content of x is passed by microinstruction 8 to adder input a1 (see Fig. 4.15). Input a2 = 1111 at all times except T14. Thus, at T1 through T13 and T15, x + 1111 → x is carried out but the 1-setting of Fo is inhibited (by FcR = $\overline{P}$.t4) which provides x - 1 → x.

Since the capacity of x is 16 but there are only 15 T times, at T14, the operation x + **1110** → x is carried out, which is equivalent to x - 2 → x, the extra increment correcting the position count.

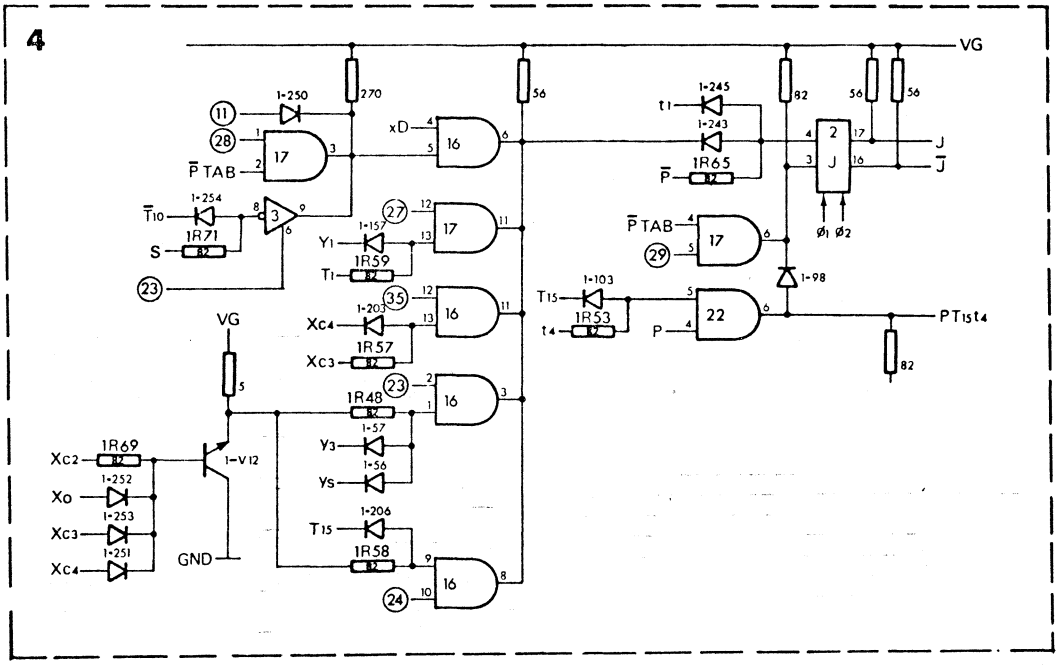
When x = 0, and the operation 0000 + 1111 is performed, no bit carry will be generated at t4 and thus, there will be no Fcin at t4. This is used to determine the decimal point display position (see Section 4.6.3).

4.5 CONTROL UNIT

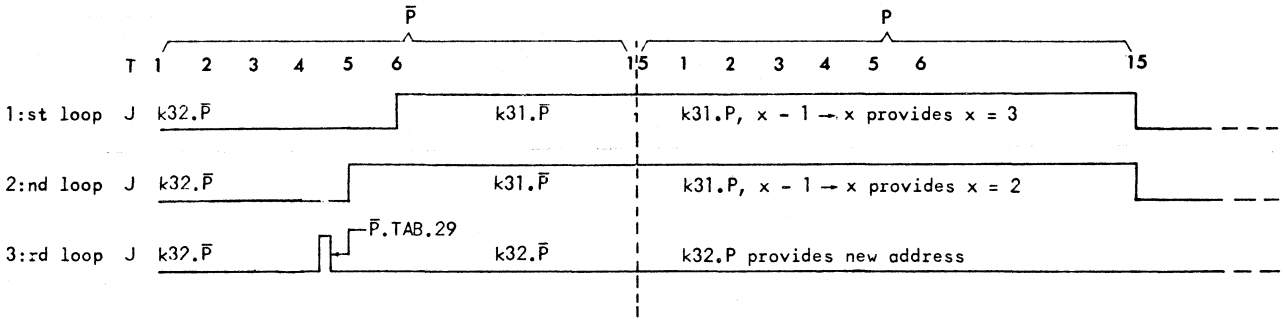
This unit contains the circuits that generate and modify the calculator programs. During each program a number of addresses are generated to control the connection of the various elements to be used. This is accomplished using micro instructions. The micro instructions also determine the times during which shift pulses are generated. For the most part, address selection is controlled from the input unit but the control unit also contains circuits that can modify the program within certain limits while processing proceeds. The circuits that determine addition/subtraction and the sign of the result are also located in the control unit.

4.5.1 Address flip-flops

The addresses consist primarily of combinations of signals from flip-flops N1, N2 and N3. Modifications within the program (address jumps) are controlled by signals from flip-flops J, F and S. Combinations of N1, N2 and N3 (address groups) are designated n_i. Combinations of n_i and J, F and S are designated k_i. See Appendix 1. The clock pulse for N1, N2, N3, F and S is CPA, which is equal to P.T15.t4.ϕ1. This means that address changes can only take place at the end of a P cycle. During the following $\overline{P}$ time a test may be carried out, leaving J 1-set or 0-set accordingly. The J flip-flop is clocked by ϕ1 and can be 1-set during $\overline{P}$.t1 only. Flip-flop J, with F and S, determines which address is to be used during P. The P time is the active time during which a demanded operation is executed.



TAB = 2 (same as $\bar{T}4$), x = 4 (xD during T6)



Test	Address	J-expression
x > TAB	k32 = n4.$\bar{J}$	11.xD.$\bar{P}$.t1 → J → k31
	k31 = n4.J	29.TAB.$\bar{P}$ → $\bar{J}$ → k32
DIV.STOP		
(Yi = BC).(Xc≠0)	k52	(23.y3.Ys).(Xc4 + Xc3 + Xc2 + Xo).$\bar{P}$.t1
+ x = 8	k52	23.T10.xD.$\bar{P}$.t1
MULT.($\bar{S}$)	k52	23.$\bar{S}$.xD.$\bar{P}$.t1
X14 ≠ 0	k45	24.(Xc4 + Xc3 + Xc2 + Xo).T15.$\bar{P}$.t1
Y1 ≠ 0	k48	27.Y1.T1.$\bar{P}$.t1
x = TAB	k37	28.TAB.xD.$\bar{P}$.t1
Xi = BC	k41,47	35.Xc4.Xc3.$\bar{P}$.t1

Fig. 4.16 J-flip-flop circuit diagram and test expressions

4.5.2 Generation of instructions

Micro instructions are generated by a diode matrix. See Appendix 8. The inputs to the diode matrix comprise read-in addresses (initiated from the keyboard) and calculation addresses. The microinstructions exist as long as the controlling addresses exist. Some instructions are called macro instructions because they, in turn, generate one or more micro instructions.

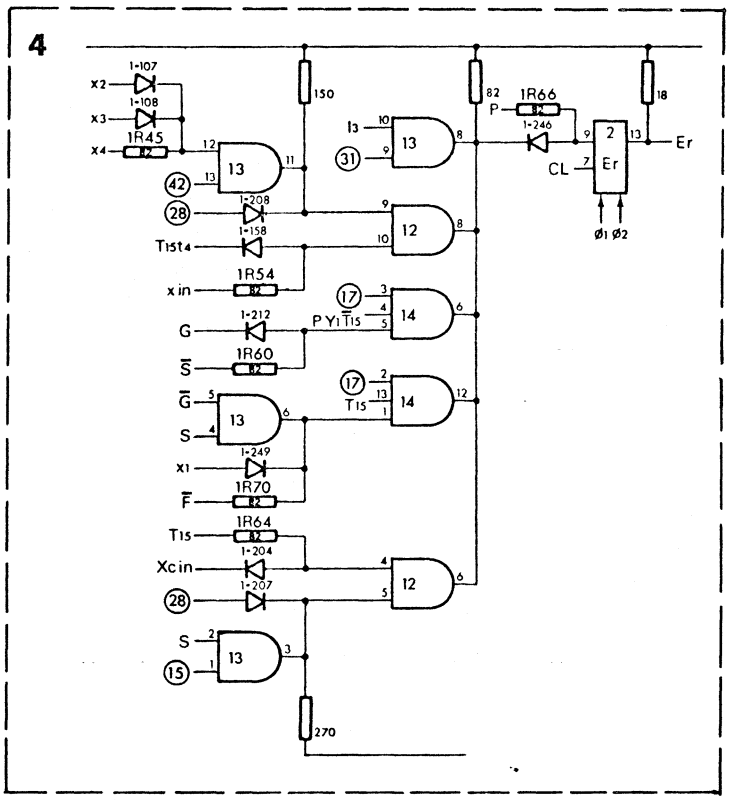
2, 3, 8, 12, 13, 34, 41, $\overline{N1}$ and Ar are macro instructions.

4.5.3 Program-controlling address flip-flops

J flip-flop

This flip-flop is used to store the result of a number of tests, all of which take place at times t1 during $\overline{P}$. (See Fig. 4.16 and Appendix 1.)

x > Tab (xD → J) (TAB → $\overline{J}$)	This test is used during n4.$\overline{P}$ to control the truncation of decimals. Signal xD = 1 when x = 0, this occuring at a T time depending on the content of x at the start of $\overline{P}$.Signal $\overline{P}$.TAB = 1 when the T time is reached which corresponds to the preset TAB value. See example in Fig. 4.16. The test and shift are repeated until $\overline{P}$.TAB.29 provides $\overline{J}$.
Div.stop: (Y_1 = BC). .(Xc ≠ 0) + x = 8	The test at address k52 ensures that division stops if certain conditions arise. If Yi = BC and Xc ≠ 0 at the same time, the divisor and partial quotient will overlap if division continues and division is therefore stopped. x = 0 provides xD. If xD = 1 during T10, the initially content of x = 8. Enough decimals have been calculated and division stops. In each case the program proceeds at k53, k54.
Mult.stop: ($\overline{S}$)	This test is used during multiplication but always results in J (because S is 0-set during multiplication and 23.$\overline{S}$.xD.T10.t1.$\overline{P}$ → J) causing the program to proceed to k53.
x14 ≠ 0	During k45($\overline{P}$), end-around shift is performed with the X-register. At T15, Xc contains the original content of X14. Thus if Xc ≠ 0 at T15, X14 ≠ 0 and no left-shift with the X-register is allowed during P-time in address k45. Xc ≠ 0 → J and the program proceeds to k46.



Test	Address		Er-expression
Add. overflow	k39		15.S.Xcin.P.T15
Mult/div. error	k46	I	17.P.$\overline{T15}$.G.$\overline{S}$.Y1
		II	17.P.T15.$\overline{F}$
		III	17.P.T15.x1
		IV	17.P.T15.$\overline{G}$.S
Xleft overflow	k37		28.P.T15.Xcin
			28.P.T15.t4.Xcin
I3	k15		31.P.I3
$x \geqslant 9$	k54		42.P.T15.t4.Xcin.(x2 + x3 + x4)

Fig. 4.17 Er-flip-flop circuit diagram and test expressions

Y1 ≠ 0 — This test controls the number of digits multiplied or divided. Each time that a digit is multiplied or divided another 0001 code is placed in Y (k48), to the right of the previous one. When all digits have been calculated Y1 = 0001 at T1 and the program procedes to k50, 51.

TAB = x — Address n6 is used to adjust the number of decimals when x < TAB. Repeated left shifts (and x + 1 → x) take place at k37 until TAB.xD = 1, i.e. x = TAB. The program then proceeds to k38 or k39.

Xi = BC — This test is used during subtraction (n2) to detect if the operation resulted in a complemented answer, or in multiplication/division if the various sub-operations resulted in complemented form. This occurs in sub. and div. at T15 and in mult. at T1. If J is set at n2 it initiates 0 - X → X. In n7 it initiates a change of add. to sub. or vice versa, thus anulling the last in sub-operation (add./sub.) in mult./div.

Error flip-flop

The error flip-flop will be 1-set (during P time only) if an overflow or other error occurs (see Fig. 4.17). The particular error test is selected by microinstructions. Once 1-set the flip-flop can only be reset by signal CL, this being obtained when C-key is pressed.

Addition Overflow — During addition at k39, S = 1. If the result of the addition gives more than 14 digits Xcin will not be 0000 during T15 and S.Xcin.T15 → Er.

Mult/div error — This test takes place early in the multiplication/division program. The contents of X and Y are exchanged and the error test made. The expression for the test has been broken down for ease of description.

I. — Multiplication → $17.\bar{S}.\overline{T14}.t4.yin \rightarrow G$. If Y1 ≠ 0 and G = 1, the two operands overlap and would give a result > 14 digits and $17.P.\overline{T15}.G.\bar{S}.Y1 \rightarrow Er$.

II. — If X14 was initially ≠ 0 the X-register content is too big and $17.P.T15.\bar{F}$ provides Er.

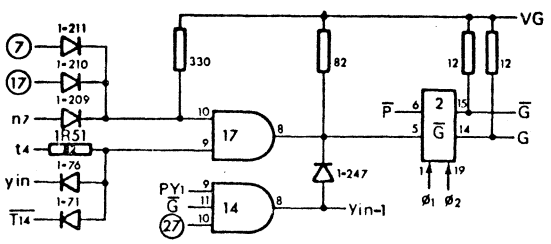
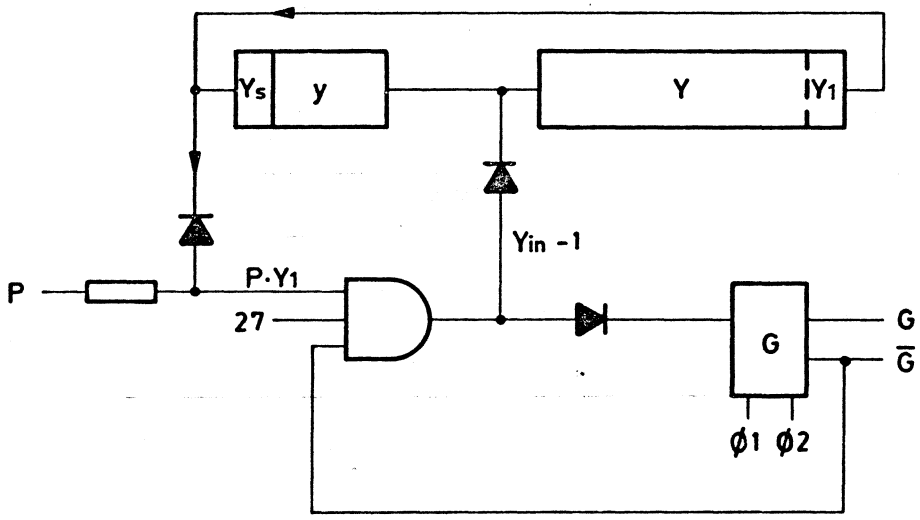


Fig. 4.18 G flip-flop



$P \cdot Y_1 \cdot 27 \cdot \overline{G} \rightarrow Y_{in}\,-1 \rightarrow G \rightarrow \overline{Y_{in}\,-1}$

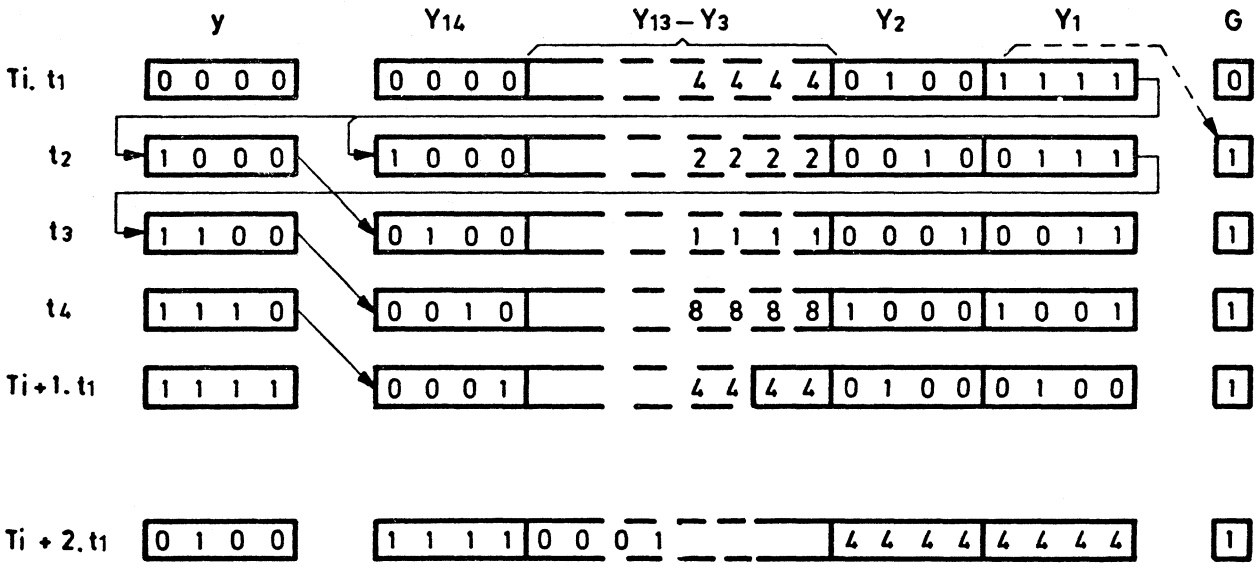


Fig. 4.19 Use of G flip-flop to give Y_{BC} right

III. The initial Y14 will be in x at T14. If Y14 $\neq$ 0 (Y content too big) 17.P.T15.x1 provides Er.

IV Division → S, and 17.T14.t4.J in → G. Thus, G will be 1-set before T14.t4 unless X was initially zero. If X was zero 17.P.T15.G.S → Er.

X left overflow This test is used during X left. If Xcin is $\neq$ 0 during T15, the content in position X14 sas $\neq$ 0 before the shift and has now been lost, thus Xcin.T15 → Er. If xin = 1 at T15.t4, x $\geqslant$ 8 thus giving Er.

I3 This error test prevents the "raising to a power" program being used to find roots.

x $\geqslant$ 9 If division has stopped and x $\geqslant$ 9 this indicates that the integers of the quotient are more than 14 and 42.P.T15.t4.(x > 8) → Er.

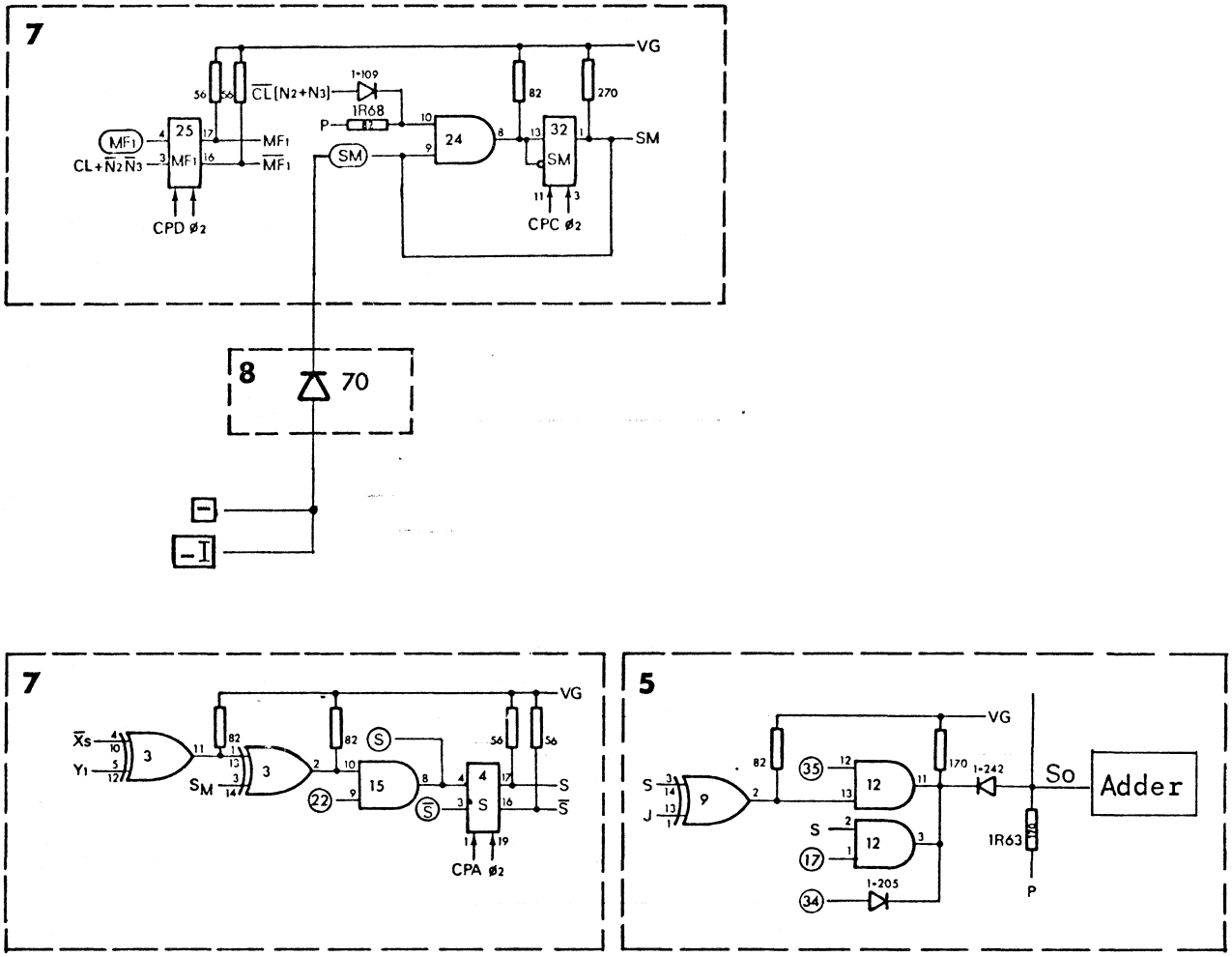
G flip-flop

The G flip-flop controls the adder input, (a2) during multiplication and division, ensuring that BC and 0001 codes are not used as part of the operands. It also controls the operations Y_{BC} right and CPY stop. See Fig. 4.18.

k47 As yY circulates during the repeated addition at k47, the first digit position where Yi.t4 = 1 will be BC. This 1-sets G enabling the remaining digits of Y to be added/subtracted into X. G inhibits Y1 → FA while 0001 and BC are at Y1 (see address k47 bottom diagram).

k46 G i 1-set as described above and is used to detect an error indication (see Er flip-flop).

k53 This operation is called CPY stop (see address k53 diagram). Register Y is right shifted during k53 until G is 1-set as described above. G then inhibits further Y clock pulses (CPY) and hence stops the shift with the least signficant digit in Y1.



$$CPA.\ \left[(\overline{Xs} \oplus Y1 \oplus XM).22 + \overline{S}\right] \rightarrow S$$

$$CPA\ .\ \overline{S} \rightarrow \overline{S}$$

$$P.\ \left[(S \oplus J).35 + S.17 + 34)\right] \rightarrow So$$

Fig. 4.20 SM and S flip-flops circuit diagram

k48 This operation i called $Y_{BCright}$ (see address k48 diagram and Fig. 4.19).

As Y is circulated during P, the first time that Y1 = 1 will be the 1 of the last-entered 0001 code. Then 27.P.Y1.$\bar{G}$ → Yin - 1. At the next T time G is 1-set by Yin - 1, this inhibiting Yin - 1, which was high for one bit time. A 0001 code is thus entered into Y one digit position to the right of the last-entered 0001 code (still in y).

SM and S flip-flops

The SM flip-flop is 1-set by the [-] -or [-I] - key to remember that a subtraction has been demanded. SM holds on until n0 + n1, i.e. until the demanded program is completed.

The state of the S flip-flop is determined by the demanded operation (SM) and the signs of the operands (Xs and Ys) as follows (Fig. 4.20):

SM	Xs	Ys	S	
0	0	0	1	addition demand, like signs give S = 1
0	0	1	0	unlike signs give S = 0
0	1	0	0	
0	1	1	1	
1	0	0	0	subtraction demand, like signs give S = 0
1	0	1	1	unlike signs give S = 1.
1	1	0	1	
1	1	1	0	

The states of S and J determine whether the adder carries out X - Y or X + Y. It is necessary to include J because during multiplication/division "add" must be changed to "subtract" and vice versa according to the result of a J test.

S may also be 1-set or 0-set by micro instructions, according to the add/subtract requirement during operations other than multiply/divide.

MLD and MF1 flip-flops

These flip-flops are associated with the memory register control. See Fig. 4.21.

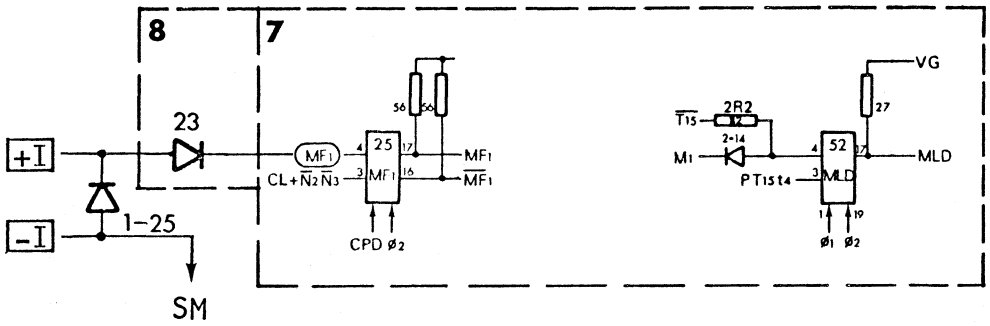


Fig. 4.21 MF1 and MLD flip-flops circuit diagram

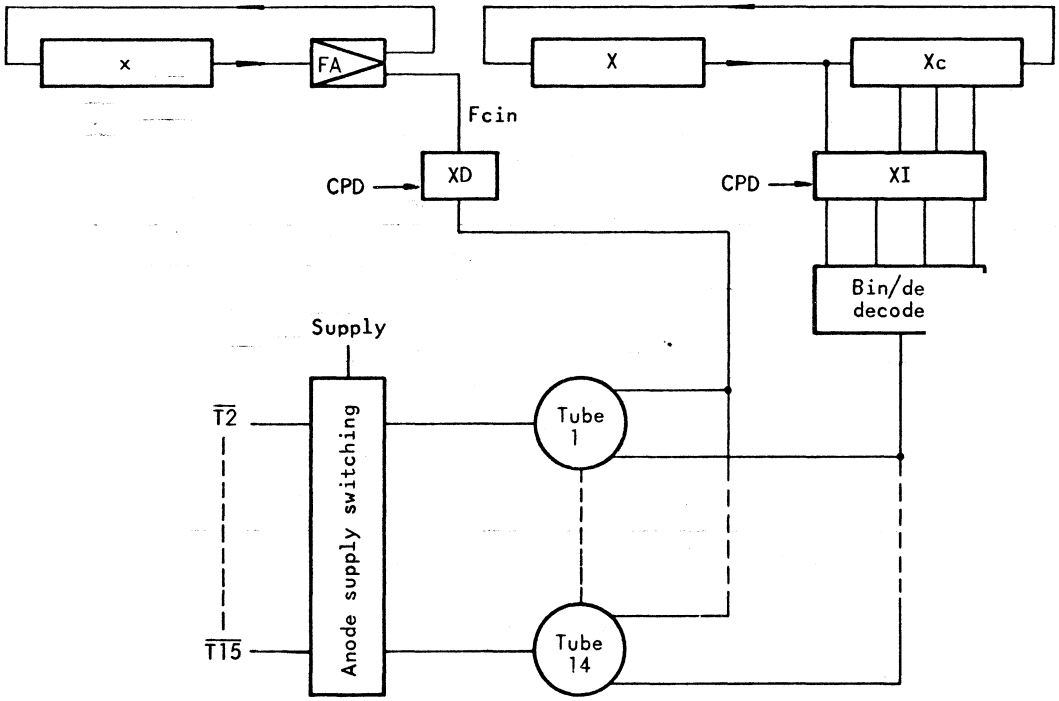


Fig. 4.22 Display circuit block diagram

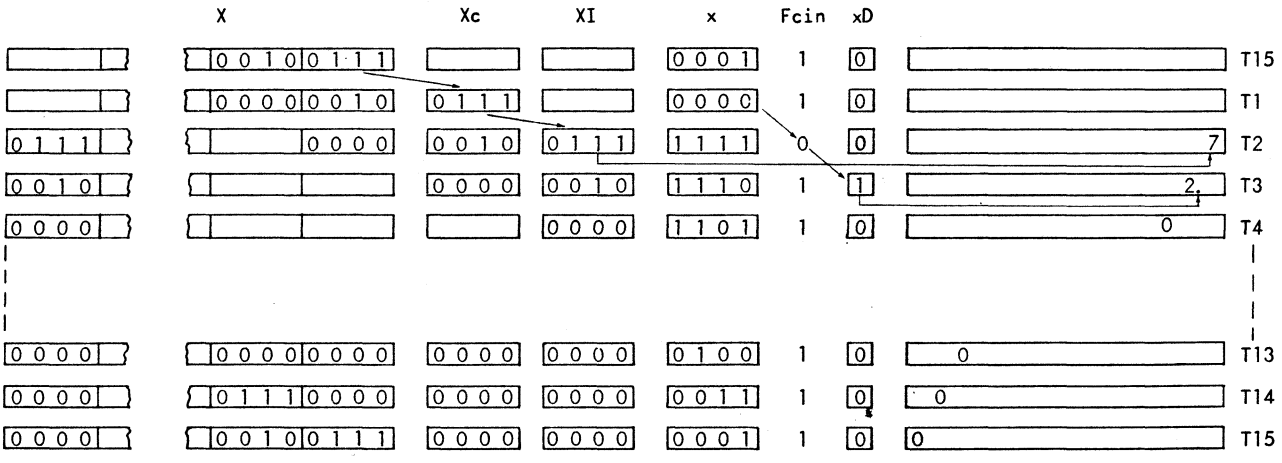


Fig. 4.23 Display example (2.7)

MF1 is 1-set by the [+I] -or [-I] -keys, and confirm that a memory operation has been demanded. MLD is 1-set if the memory register M1 $\neq$ 0, causing the I indicator lamp to light.

4.6 OUTPUT UNIT

The output unit comprises 15 display tubes, 14 for digits/decimal points and one for sign, error and memory indication. See Fig. 4.22.

Numerals

As the registers are recirculated during $\overline{P}$ the operand in X passes through Xc. CPD causes Xc → XI and XI remains until the next CPD. The four-bit BCD output of XI is decoded and the 10 outputs control the display tubes.

4.6.1 Display tubes

Each numeral display tube has a single anode and ten cathodes shaped like numerals. The sign display tube is similar in principle but has cathodes shaped to indicate, E or ¯. To display the E-sign, both E and ¯ must be selected.

4.6.2 Timing

Only one display tube is on at any time. The 10 outputs of the decoder controls the 10 cathodes of all tubes but the anode supply is switched by Ti. Each tube thus light for one T time, displaying the content of XI during that T time.

4.6.3 Decimal Point display

As X recirculates x is being decremented to maintain relative position control of the decimal point. Register x will be at 0 two T times before the decimal point needs display. When x = 0, the next decrementing action (in the full adder) gives Fcin = 0 this 1-setting xD at the following T-time. xD = 1 for one T time and causes the decimal point to light in whichever display tube is selected during that T time. For the example in Fig. 4.23 this occurs at time T3.

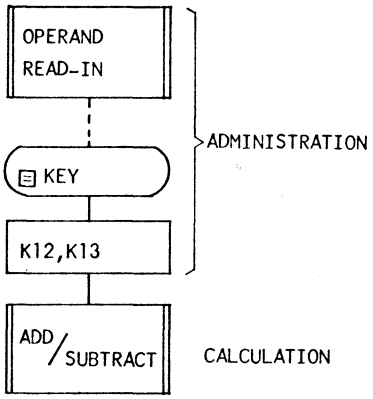
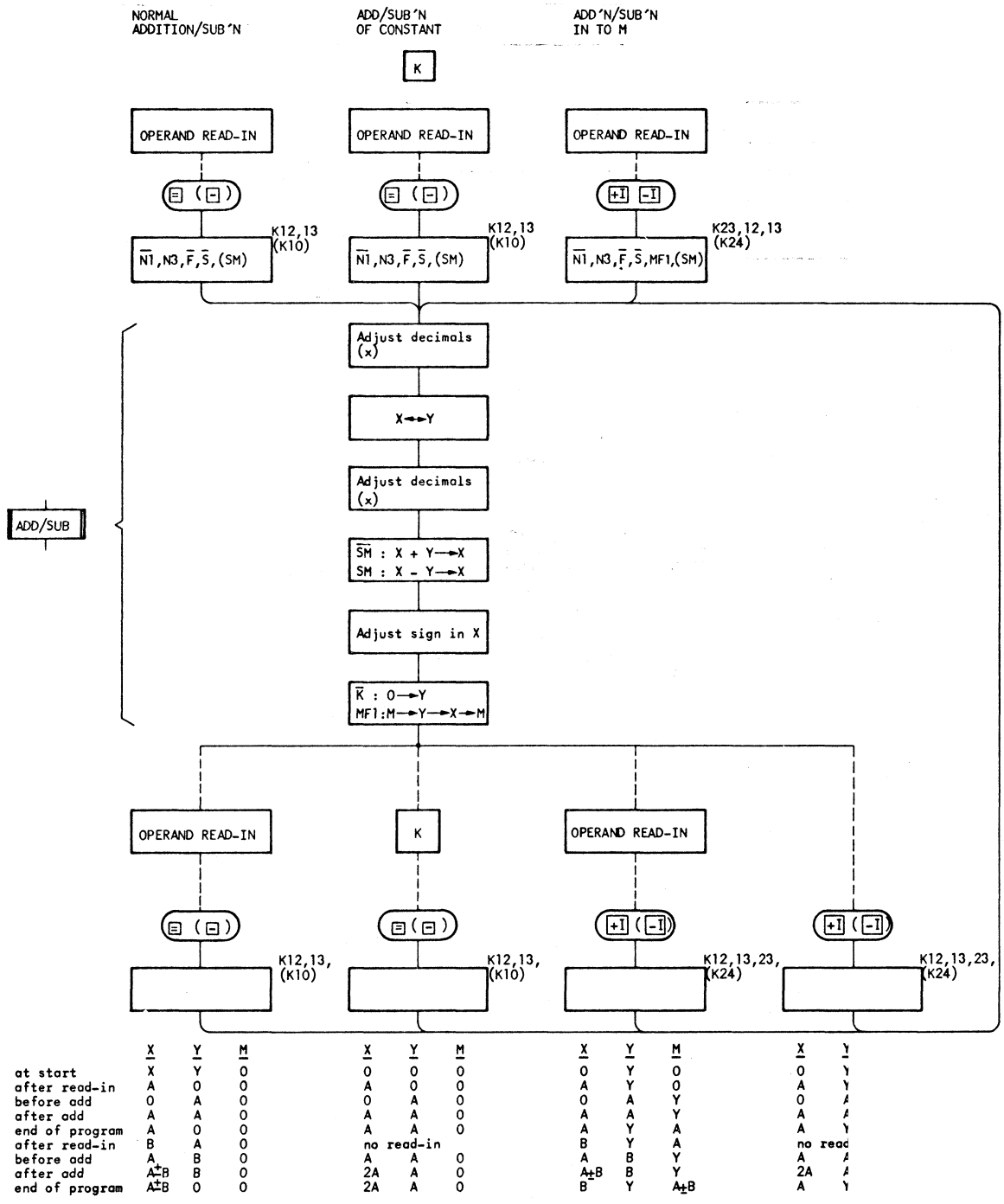


Fig. 4.24 Organisation of calculator operations



	X	Y	M	X	Y	M	X	Y	M	X	Y
at start	X	Y	0	0	0	0	0	Y	0	0	Y
after read-in	A	0	0	A	0	0	A	Y	0	A	Y
before add	0	A	0	0	A	0	0	A	Y	0	A
after add	A	A	0	A	A	0	A	A	Y	A	A
end of program	A	0	0	A	A	0	A	Y	A	A	Y
after read-in	B	A	0	no read-in			B	Y	A	no read	
before add	A	B	0	A	A	0	A	B	Y	A	A
after add	A±B	B	0	2A	A	0	A±B	B	Y	2A	A
end of program	A±B	0	0	2A	A	0	B	Y	A±B	A	Y

Fig. 4.25 Use of addition/subtraction flowchart

5 CALCULATION EXAMPLES

Any calculation may be considered as two sub-operations: administration and calculation (Fig. 4.24).

Administration - here operands are read in and calculation initiated.
Calculation - here the required calculation is carried out.

In order to minimise the calculator components one calculation sub-operation may be used with different read-in operations; similar the read-in for several calculations will use the same sub-operation. In the following text, where a complex operation is described, read-in will be shown as in Fig. 4.24, but a full description will be found else where; similarly the description of multiplication/division administration shows the calculation as in Fig. 4.24 but a full description is also given.

Operations are carried out as a sequence of sub-operations in accordance with certain programs. The programs are controlled by a number of address conditions (addresses). The addresses are numbered from k0 - k54, and they are tabulated in Appendix 1 which shows, among other things, the operations that are to be carried out at the various addresses and the microinstructions that are generated to make logic circuit connections.

5.1 USE OF ADDITION/SUBTRACTION FLOWCHART

Fig. 4.25 shows how the basic addition/subtraction program is used for a variety of operations. Normal addition comprises a read-in of an operand, followed by [=] . This initiates the addition program:

1. adjust decimals in X
2. interchange X with Y and compare signs
3. adjust decimals of X (formerly Y)
4. add Y to X
5. complement X if necessary
6. clear Y.

This operation may be repeated as often as required by entering a new operand and then depressing [=], each operand being added to the previous total. If CL has been pressed the "previous total" = 0 and the next operand, although actually added to 0, appears to have been only read in. If [-] replaces [=] at any time a flip-flop SM is 1-set, causing a subsequent subtraction to replace addition (refer to detailed description of addition program).

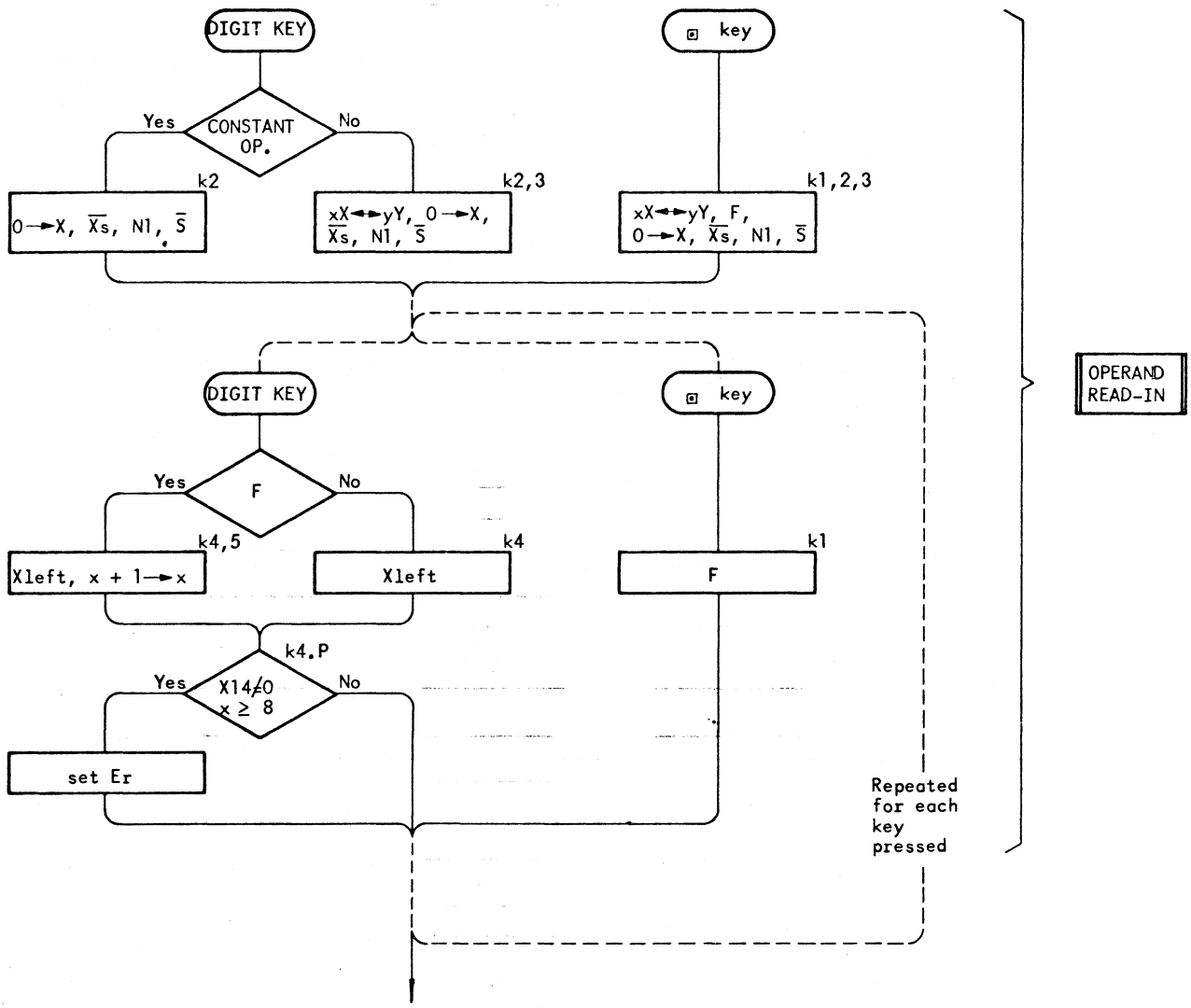


Fig. 4.26 Operand read-in flowchart

If K is depressed (and locked) the first operand read in, located in Y at the end of addition/subtraction, will not be cleared. Each time that [=] or [-] is depressed this first operand will be added/subtracted to the previous total in X.

If [+I] or [-I] is depressed after read in, the operand is added to the previous total in the memory.

The tables below Fig. 4.25 show the way in which operands are transferred from register to register during addition/ subtraction.

Operand read-in

Read-in is a part of each arithmetic operation. Five addresses can exist in connection with read-in, k1 through k5. A distinction is made between reading in the first digit and reading in subsequent digits. If a normal (not constant) operation is being carried out, the content of the X-register is transferred to the Y-register when the first digit is read in. The first digit is read in at addresses k2 and k3. If a constant operation is being carried out, read-in occurs only at address k2. See Fig. See Fig. 4.26.

Addresses k2 and k3 are also obtained when a read-in operation is started by depressing the decimal key ([·] → 11key → k2, k3). However, this operation differs from digit read-in operations in that nothing is read into X from the keyboard.

As a result of the first read-in operation, the N1 flip-flop is 1-set at the end of the P cycle, thus causing subsequent read-in operations to take place at address k4. Read-in continues at address k4 as long as the decimal key has not been depressed. If the decimal key is depressed F is 1-set and read-in operations continue at addresses k4 and k5.

At address k4 the X-register is end-around shifted via Xc, but only during 14 T times. During T9, no CPX pulses are gated to the X-register. This means that the content of the register is left shifted. Each digit is read into position X during T10, and during T10 through T15 the digit in X6 is shifted into position X1. During T15, a test is made to ascertain whether Xc $\neq$ 0. If Xc $\neq$ 0 during T15 it means that the most significant digit in the number read in has been shifted out (overflow) and an error indication is obtained.

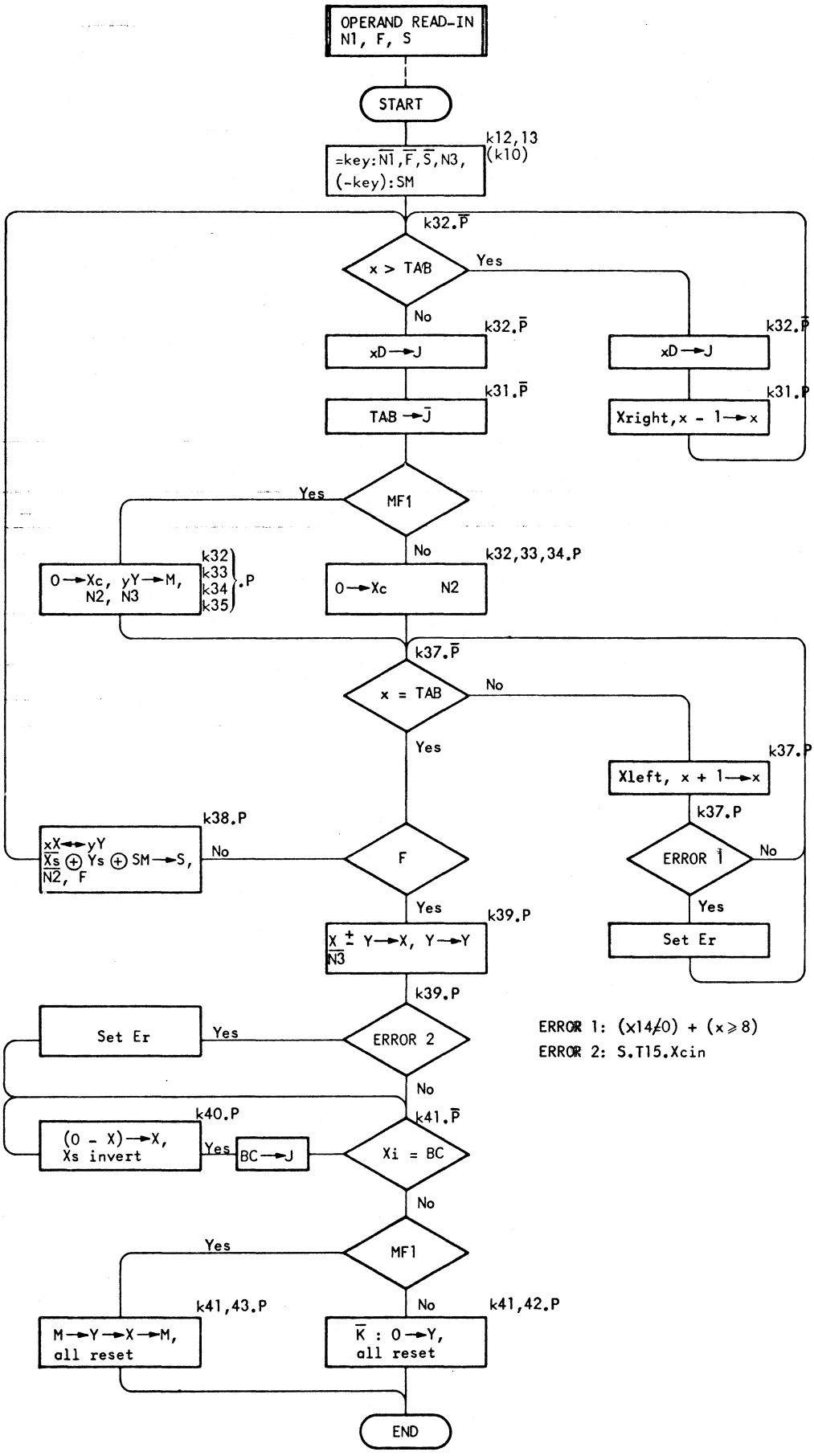


Fig. 4.27 Addition/subtraction and memory operation flowchart

At address k5 the content of the x-register is end-around shifted via FA, and during T1, a "1"is added to the x-register. This is carried out as x - 1111 → x with the resulting digit carry suppressed. The register is also tested to ascertain whether an error has occured. If xin is present during T15.t4, it means that the x-register contains at least 8 (1000), which comprises an error (x > 8). The Y-register and y-register are end-around shifted during read-in at k4 or k4,5.

5.1.1 Addition/subtraction example

The example given in Appendix 12 shows how three addition/subtraction operations are carried out. The example should be used with the detailed flowchart of Fig. 4.27.

The first operand read in shows how the first, subsequent and fractional digits are read in at different addresses.

The second operand (3.45) read in has the correct number of decimals (Tab = 2) and no adjustment is necessary.

The third operand has too many decimals and the example shows how this is truncated at n4. It is also seen that ⊟ sets SM which causes a subtraction to take place.

The last operation gives a result in complement form and it can be seen that (0 - X) → X gives the normal form, with Xs inverted to indicate a negative result.

Add./sub. flowchart

The flowchart or Fig. 4.27 shows in detail the various addresses used during addition and how flip-flops J and F influence the program.

After read in ⊟ → k12,13 → n4.

During n4.$\bar{P}$ the J flip-flop will be 1-set if x > Tab or 0-set if x ⩽ Tab. If x > Tab, the program proceeds to address k31 where X is shifted right and x decremented.

The test and shift operations are repeated until x = Tab, then Xc is cleared. (This operation - trunction - is described in detail later.)

During n6.$\overline{P}$ flip-flop J will be 1-set if Tab = x or 0-set if Tab < x (after n4 Tab cannot be greater than x). If Tab < x, X is shifted left and x incremented. The test and shift are repeated until x = Tab, whereupon xX and yY are interchanged and F is 1-set. During the interchange a sign comparison is made. This is described later, but causes the Full Adder to give the correct result from operands of varying signs. After the operands are interchanged decimal adjustment takes place on the second operand, now in X. Thereafter the actual addition/subtraction follows.

The addition/subtraction result may be in complemented form but by subtracting from 0 (0 - X → X) the normal form is obtained and Xs must be inverted. When the result is in normal form, Y is cleared and the operation is complete.

n4-truncation/decimal adjustment

If the number of decimal digits read in is greater than that set on the decimal selector, the operand is truncated and the decimal register adjusted accordingly.

During the first part of P time the n4 address is set up and as J = 0 the address is k32. Flip-flop J is controlled during the remainding P as follows:

(a) J is set by xD.11.$\overline{P}$.t1 causing a change to k31
(b) J may be reset by TAB.29.$\overline{P}$ causing a change back to k32

Thus if xD precedes TAB, which will happen if x ⩽ TAB, J = 0 at the end of $\overline{P}$ and the subsequent P time is k32. If TAB precedes xD, which will happen if x > TAB, J = 1 at the end of $\overline{P}$ and the subsequent P time is k31.

During k31 X is shifted right, by one digit position, and x is decremented (by the addition of 1111). The previously described test is then repeated during $\overline{P}$ and the shift repeated during P until x = TAB.

Modifications to basic program

The states of other flip-flops or keys may influence the program:

If K is depressed Y is not cleared at the last step; the operand being retained for further use.

If [+I] or [-I] initiates addition/subtraction MF1 flip-flop will be 1-set causing the contents of yY and mM to be interchanged so that the former content of M becomes the first operand. Then, after addition, the operation M → Y → X → M places the result in M and leaves X and Y as they were initially.

Flip-flop S is set (during k38) according to the operand signs and demanded operation, to determine the subsequent full adder action.

If a subtraction is demanded by [-] or [-I] a flip-flop SM is set. This, together with the operand signs, controls the setting of S, which, in turn, determines whether the operands are actually added or subtracted.

If an addition is demanded SM = 0 and if the operand signs are the same ($Xs.Ys + \overline{Xs}.\overline{Ys} \rightarrow S$) an addition is carried out but if the operand signs are different ($\overline{Xs}.Ys + Xs.\overline{Ys} \rightarrow \overline{S}$) a subtraction is carried out. Similary if a subtraction is demanded SM = 1 and if the operand signs are the same a subtraction is carried out but if the signs are different an addition is carried out.

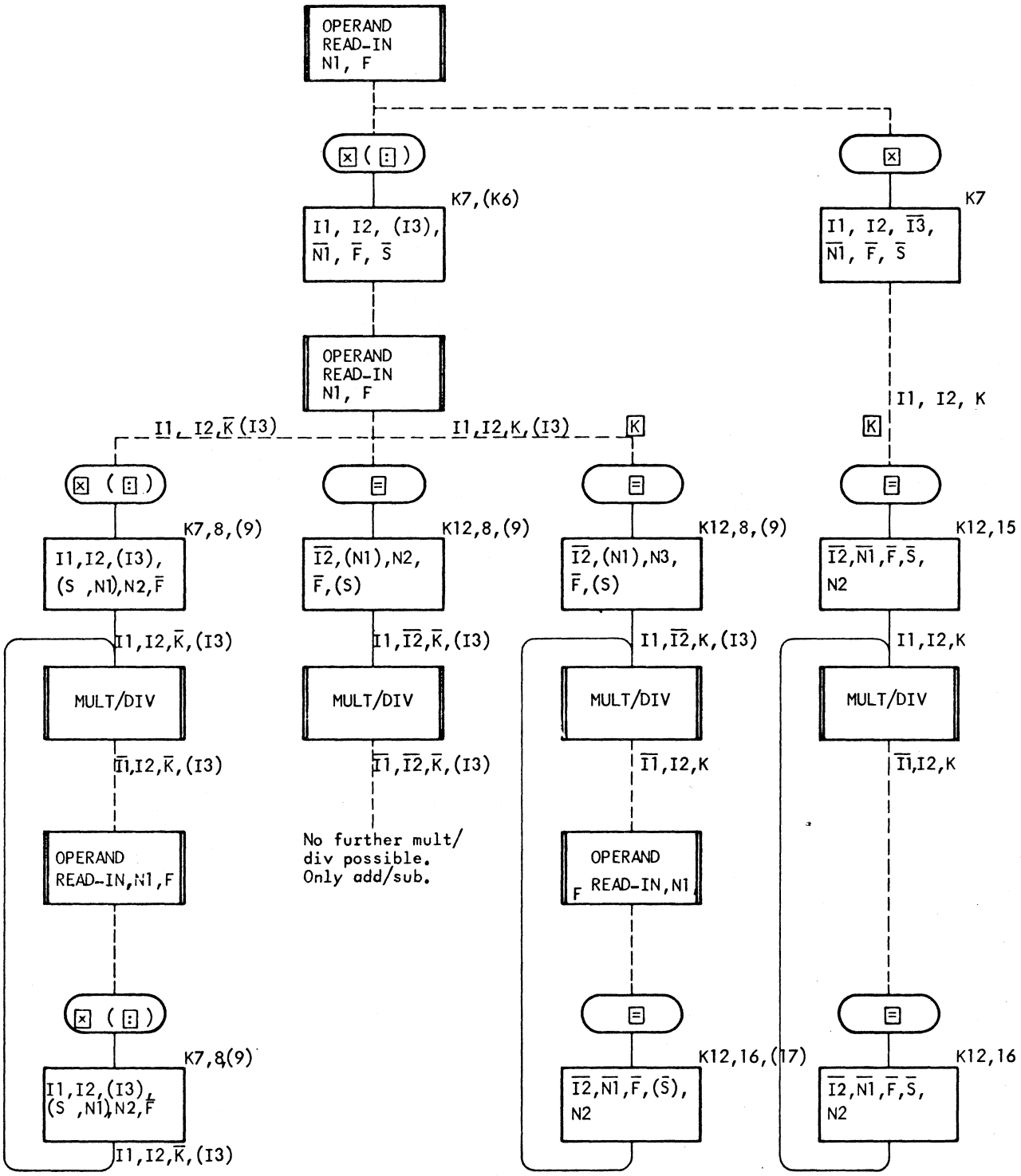


Fig. 4.28 Use of multiplication/division flowchart

5.2 USE OF MULT/DIV FLOWCHARTS

There are several ways in which the calculator operator may use the mult/div program.

Normal operation A [X] B [=]

Repeated operation A [X] B [X] C [X] D [=]

Constant operation A [X] B [=] provides A.B
C [=] provides A.C
D [=] provides A.D

Raising to a power (mult. only) A [X] [=] [=] [=]

Each of these ways uses the same basic program. This means that the administration before, and after, the basic program must be altered according to the required calculation method. This alteration is effected by flip-flops I1, I2 and I3. Flip-flop I3 is used to determine whether multiplication or division is carried out. Fig. 4.28 shows the way in which flip-flops I1, I2 and I3 influence the mult/div program.

Note: [-] may be used in place of [=] . This causes a flip-flop SM to be set and inverts Xs, the operation then being (-X) multiplied/divided by Y.

5.2.1 Multiplication/division examples

The examples given shows how the numbers are multiplied and divided together.

Multiplication program flowchart

The contents of xX and yY are interchanged. See Fig. 4.29 and Appendix 13.

k45 A test is made to see if X14 = 0. If X14 = 0, J remains 0-set and during n3(P) the content of X is shifted left. The test and shift are repeated until X14 $\neq$ 0, whereupon the program proceeds at k46.

The X content is shifted left by one digit position. Initially F is 0-set. During k45 a 1111 code (boundary code) is introduced into X1 and F is 1-set. This results in subsequent k45 shifts not having a BC inserted.

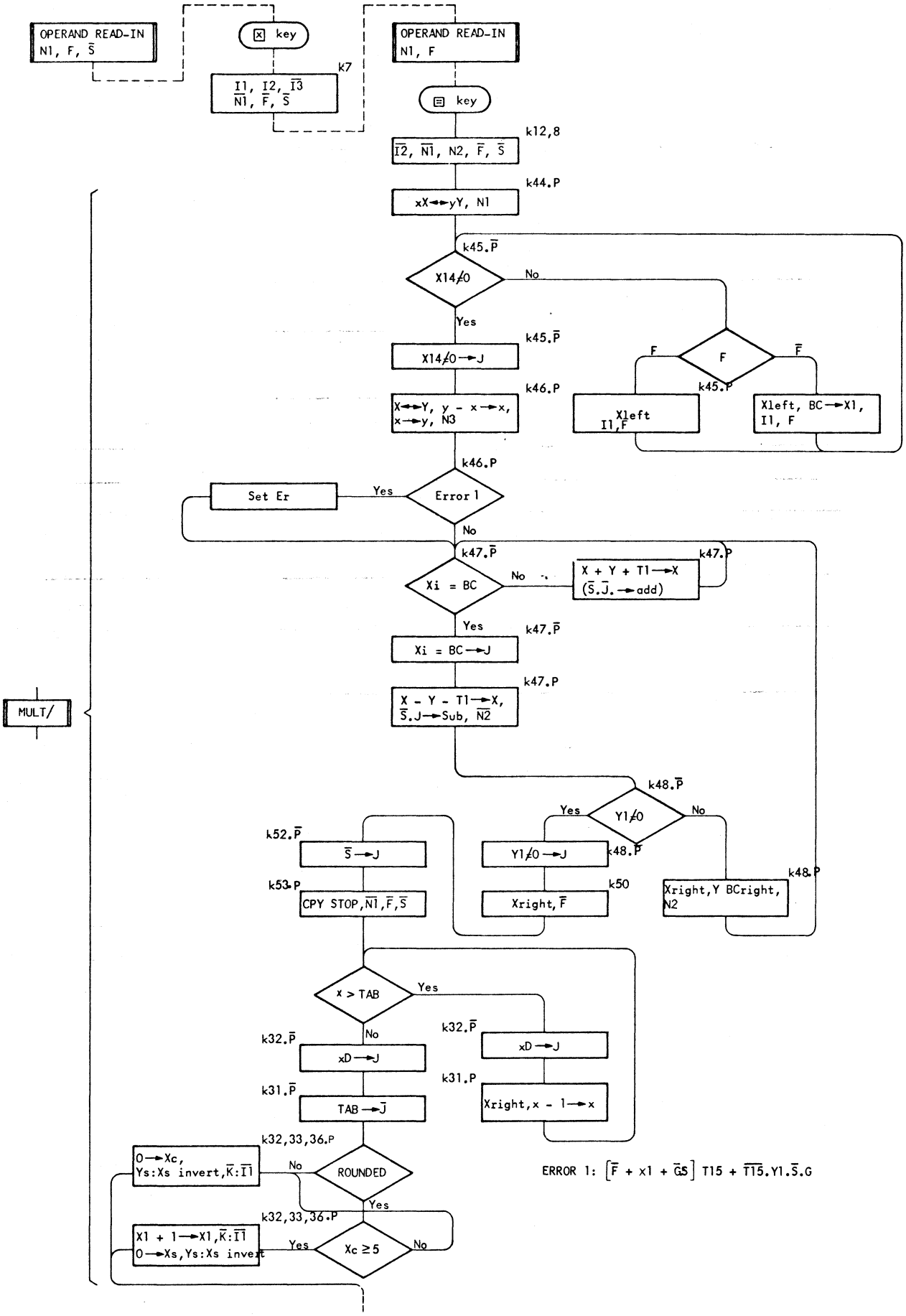


Fig. 4.29 Multiplication flowchart

k46 — $xX \leftrightarrow yY$, $x \rightarrow y$, $x + y \rightarrow x$. This restores the operands to their original registers and x contains the number of decimals to be in the calculated result.

k47(P) — A test is made to see if any X position = 1111. Initially this will not be so and k47 is carried out.

k47($\overline{J}$) — $\overline{S}.\overline{J} \rightarrow$ add. This results in Y being added in to X and X1 being decreased by 1 (X1 + 1111 = X1 - 1). The BC in Y does not appear in X (see flip-flop G, page I.4:20).

The above test and add operations are repeated until X1 is reduced to 0000, then 1111 (BC), causing J to be 1-set during the next $\overline{P}$. At the following P the last addition is anulled, by carrying out X - Y - T1 → X ($\overline{SJ} \rightarrow$ Sub). This restores X to its state before the last addition, with X1 = 0 (1111 - 1111 = 0000).

k48(P) — The test Y1 ≠ 0 determines whether all digits have been multiplied. Initially Y1 = 0 → $\overline{J}$ → k48(P).

k48 — X is shifted one digit position right and the operation $Y_{BCright}$ inserts 0001 in the next zero position of Y (see explanation of G flip-flop).

The k47, k48 loop described above is repeated for each multiplicand digit, with an additional 0001 being inserted into Y each time. Then, during k48($\overline{P}$), Y1 ≠ 0 → J which, in turn, provides k50.

k50 — X is shifted one digit position right, this putting the content of X into the correct significance. F is 0-set.

k52 — $23.\overline{S} \rightarrow J$. The other tests of this address are ineffective during multiplication and J always becomes 1-set. (S = 1 only during division).

k53 — Y is now shifted right, one digit position each T time until all 0001 codes and the BC have been lost and the least significant digit of the multiplier is in Y1 (CPY stop - see explanation of the G flip-flop).

n4 — Truncation takes place as described on page I.4:27. Additionally if Ys = 1, Xs is inverted (positive multiplier with negative multiplicand gives negative product). If the decimal selector switch is in one of the "R" positions and Xc 5, the operation X1 + 1 → X1 takes place. Thus, if the last digit shifted out of X was ≥5, X is rounded up.

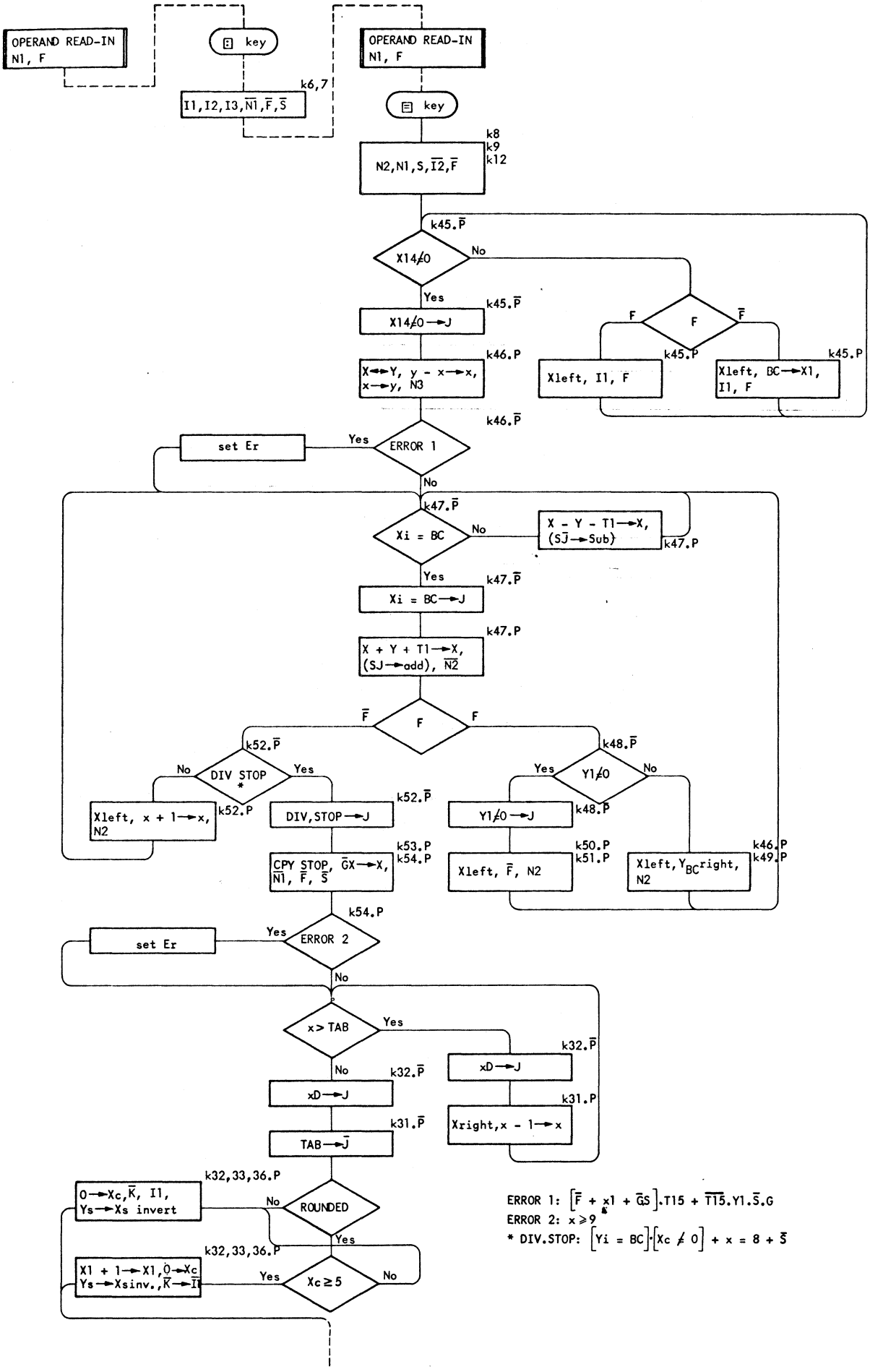


Fig. 4.30 Division flowchart

Division program flowchart (Fig. 4.30 and App. 14)

k45 — A test is made to see if X14 $\neq$ 0. If X14 = 0, J is 0-set and during P time X is shifted left. The test and shift are repeated until X14 $\neq$ 0, whereupon the program proceeds to k46.

X is shifted left by one digit position. Initially, F is 0-set. During k45 a 1111 (boundary code) is introduced into X1 and F is 1-set. This results in subsequent k45 shifts not having a BC inserted.

k46 — xX$\longleftrightarrow$yY, Y $\rightarrow$ X, y - x $\rightarrow$ x. This exchanges the operands and contains the number of decimals to be in the calculated result.

k47($\overline{P}$) — A test is made to see if any X position = 1111. Initially this will not be so and k47 is carried out.

k47($\overline{J}$) — S.$\overline{J}$. $\rightarrow$ Sub. This results in Y being subtracted in to X and X1 being increased by 1 (X1 - 1111 = X1 + 1). The BC in Y does not appear in X (see explanation of flip-flop G, page I.4:20).

The above test and subtract operations are repeated until the X-content goes negative (BC in Xc), then 1111 (BC) causes J to be 1-set during the remaining $\overline{P}$ time. At the following P time the last subtraction is annulled, by carrying out X + Y + T1 $\rightarrow$ X.

This restores X to its state before the last subtraction.

k48($\overline{P}$) — The Y1 $\neq$ 0 test determines whether all digits have been multiplied. Initially Y1 = 0 $\rightarrow$ $\overline{J}$ $\rightarrow$ k48, 49.

k48 — The X content is shifted one digit position left, and the operation BC Y_{BC}right inserts 0001 in the next zero position of Y. (See explanation of G flip-flop.)

The k47, k48 loop described above is repeated for each divisor digit, with an additional 0001 being inserted into Y each time. Then, during k48($\overline{P}$), Y $\neq$ 0 $\rightarrow$ J, whereupon the program proceeds to k50.

k50 — The X content is shifted one digit position left, and F is 0-set.

k52($\overline{P}$) — The test for division stop is now carried out. (See explanation of J flip-flop.) If no stop condition exists $\overline{J}$ $\rightarrow$ k52(P), otherwise J $\rightarrow$ k53,54.

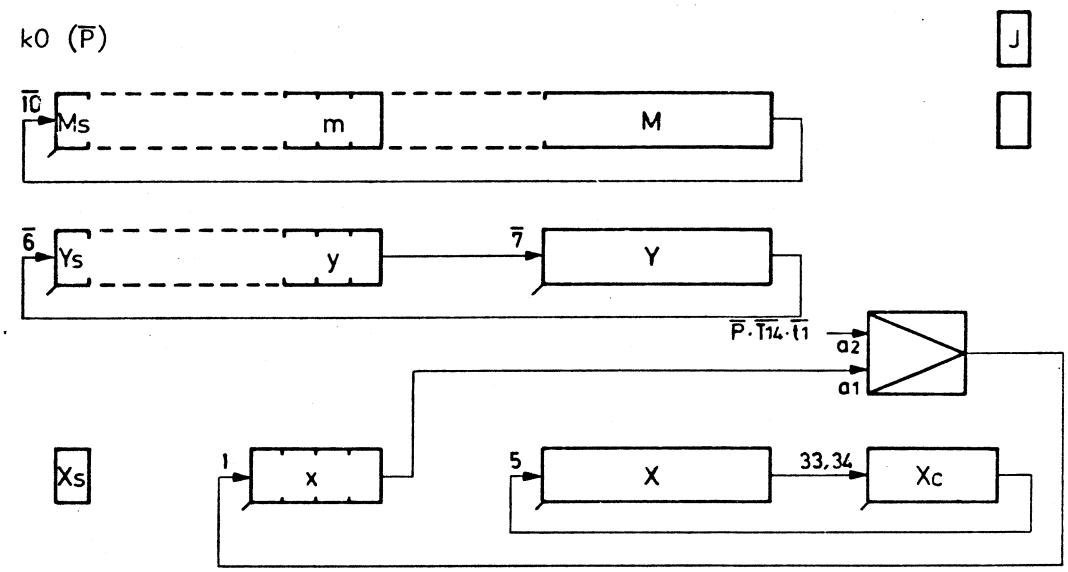
The k52, 47 loop is repeated until a stop condition arises. This calculates the quotient to max. number of decimals and hence it is necessary to carry out the operation x + 1 → x each time the X-content is shifted.

k53,54 Y is now shifted right, one digit position each T time until all 0001 codes and the BC have been lost and the least significant digit of the dividend is in position Y1 (for the CPY stop operation, see explanation of G flip-flop).

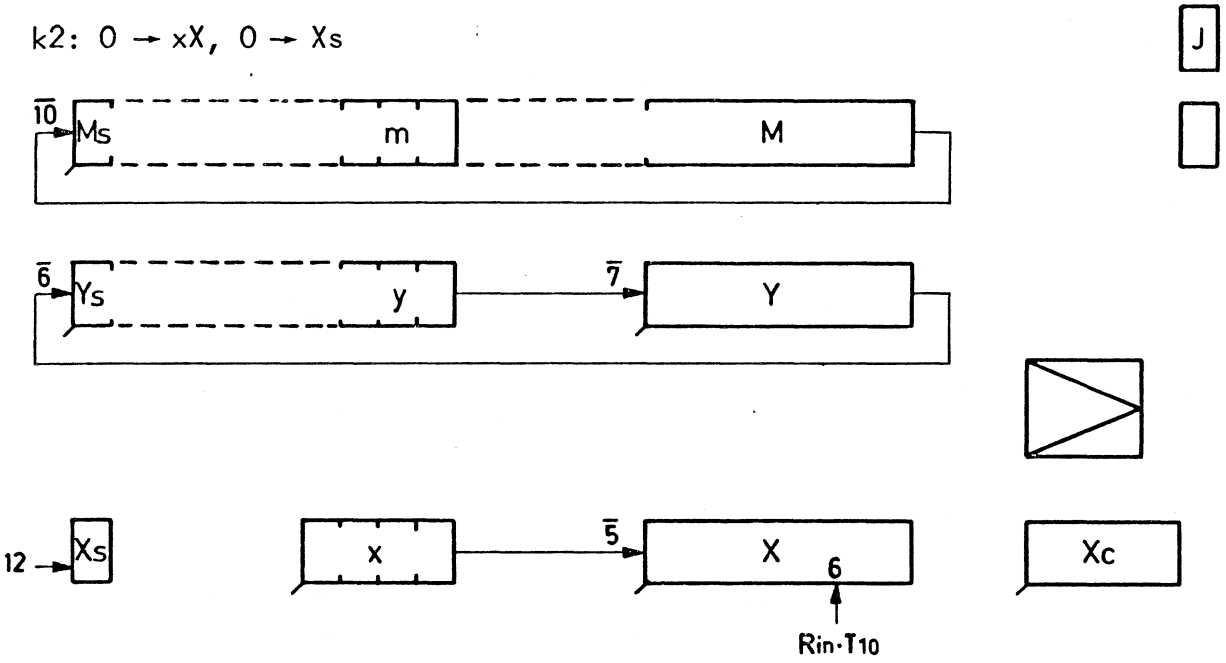
The X-content is recirculated until G is 1-set. This causes the unwanted remainder to be lost (if any).

n4 Truncation takes place as described on page I.4:27. Additionally if Ys = 1, Xs is inverted. If the decimal selector switch is in one of the "R" positions and Xc ⩾ 5, the operation X1 + 1 → X1 takes place. Thus, if the last digit shifted out of X was ⩾ 5, X is rounded up.

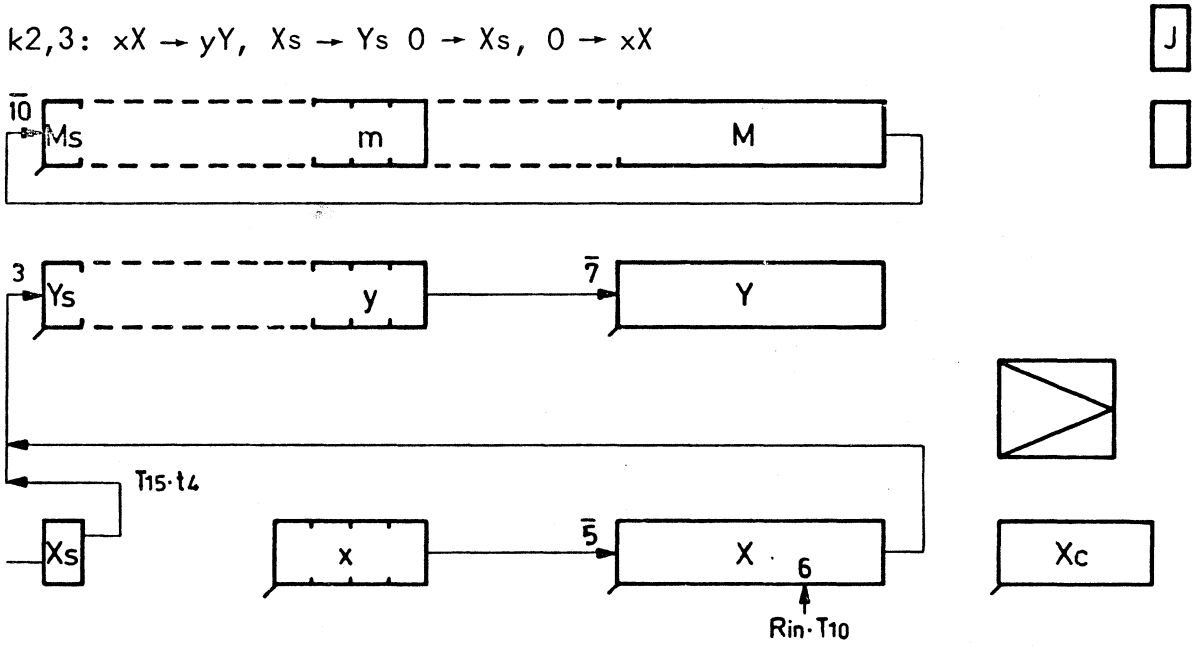
5.3 BLOCK ADDRESSES



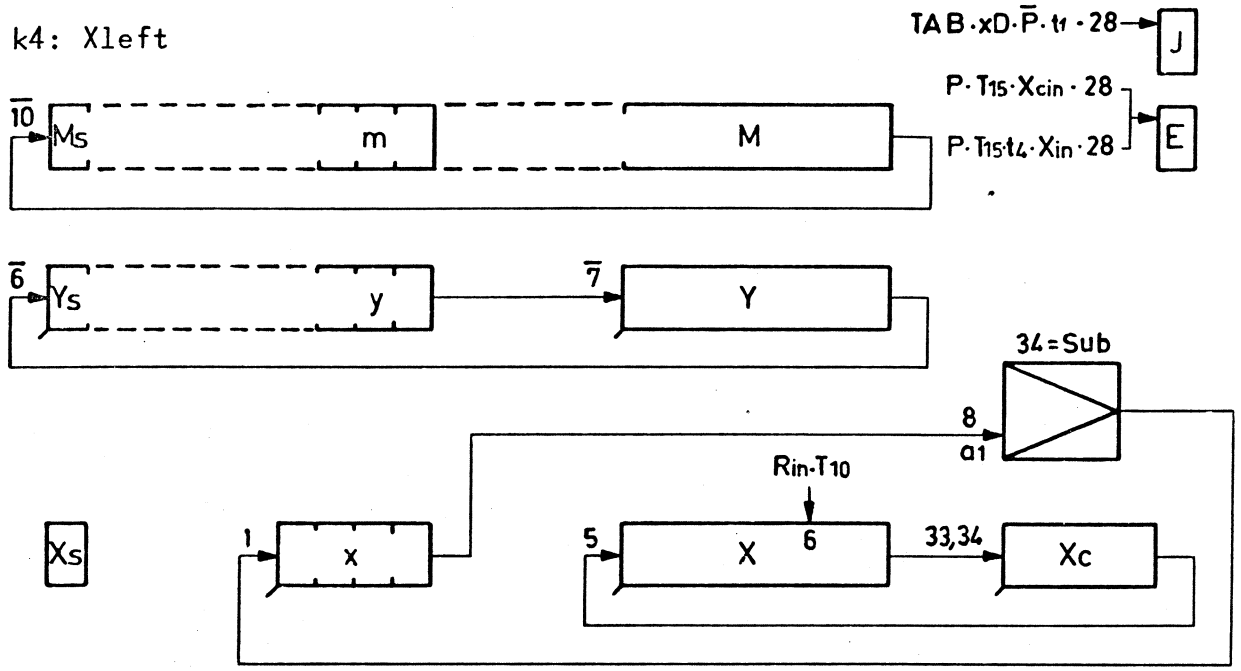
k2: 0 → xX, 0 → Xs



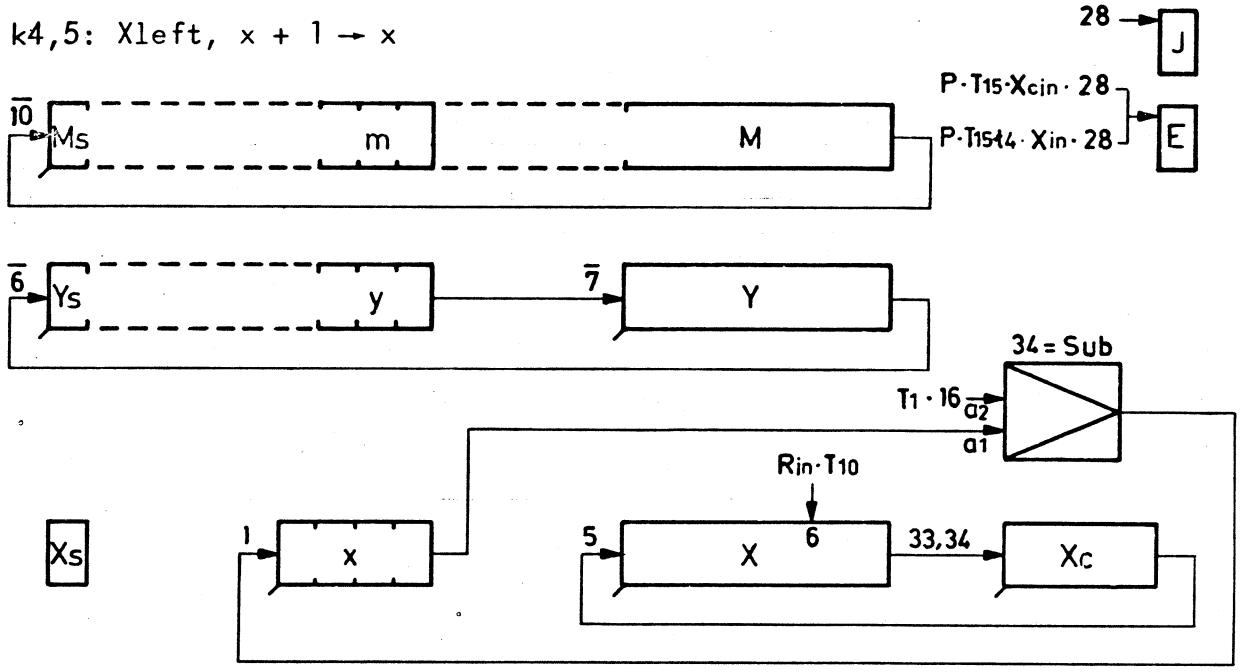
k2,3: xX → yY, Xs → Ys 0 → Xs, 0 → xX



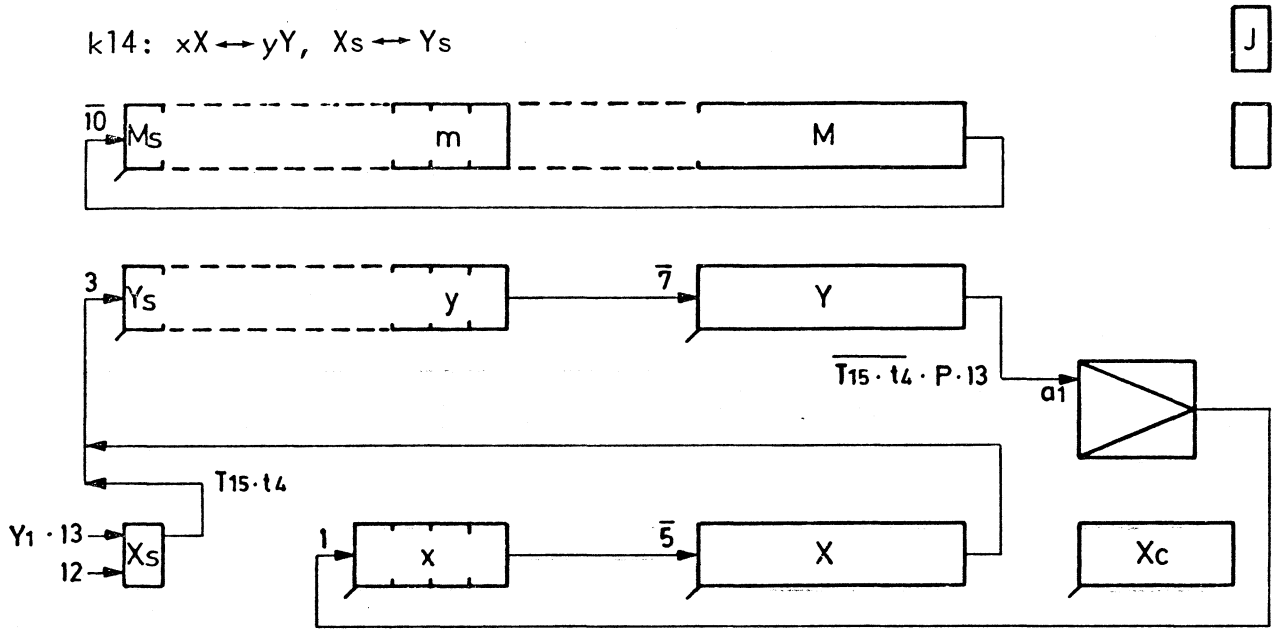
k4: Xleft



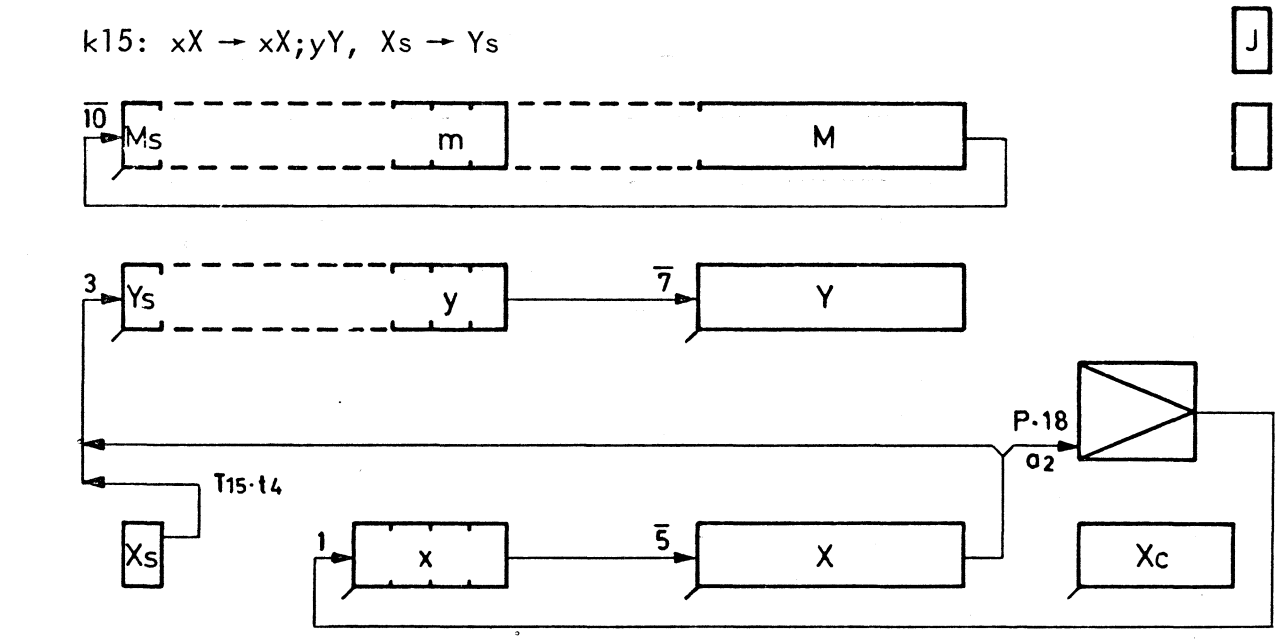
k4,5: Xleft, x + 1 → x



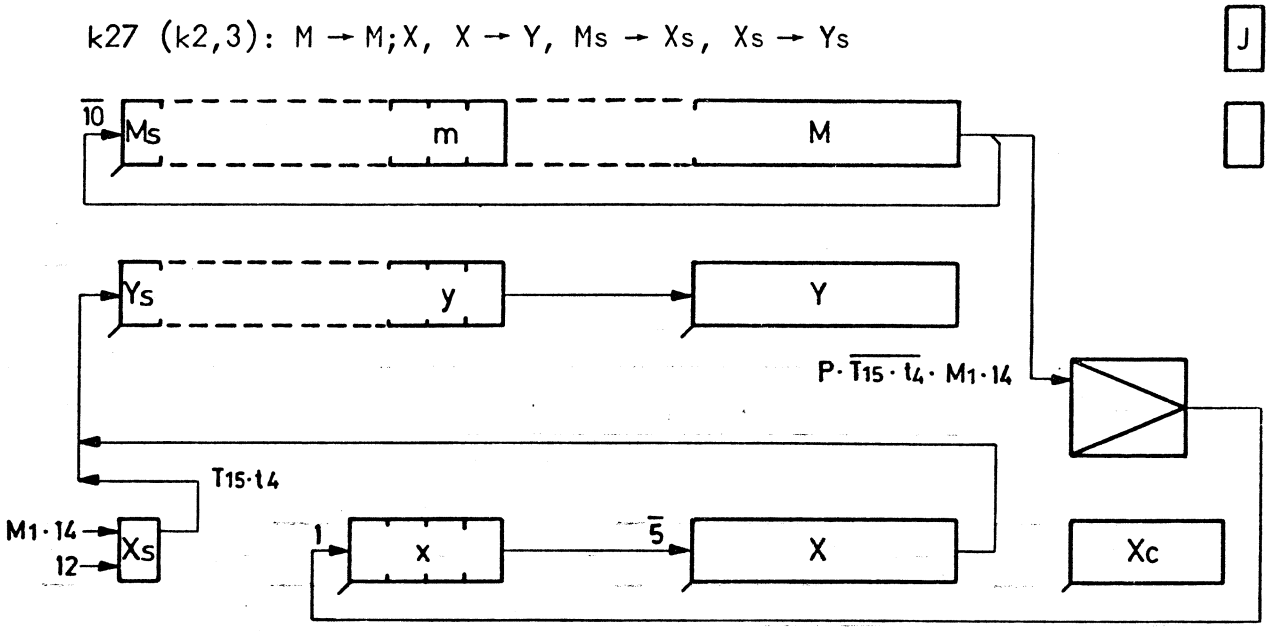
k14: $xX \leftrightarrow yY$, $Xs \leftrightarrow Ys$



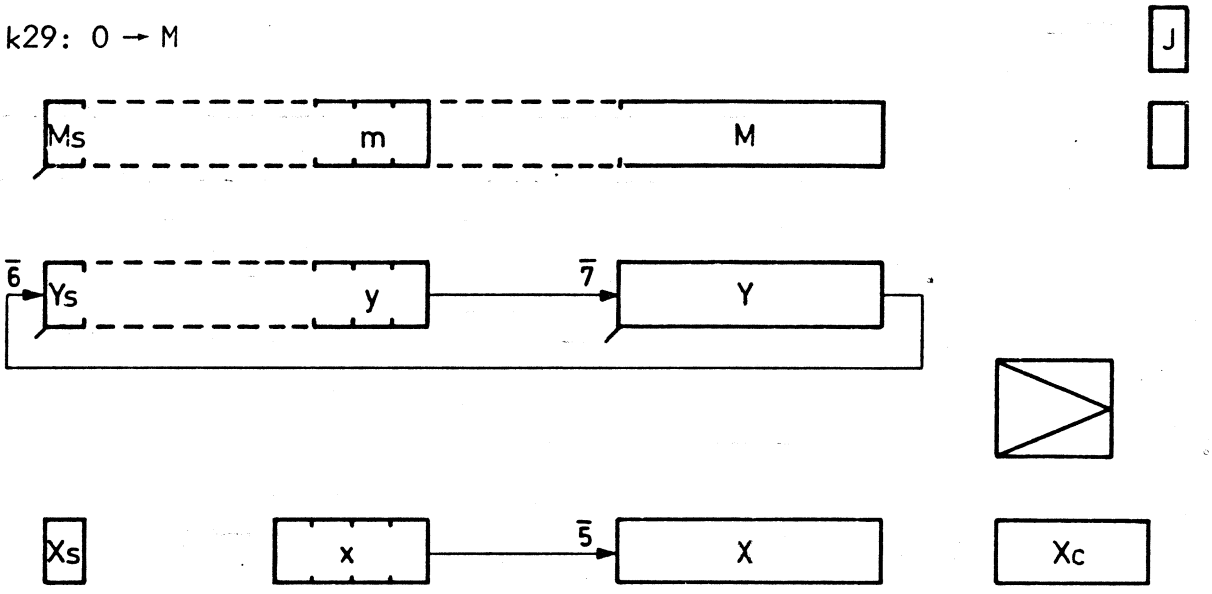
k15: $xX \rightarrow xX;yY$, $Xs \rightarrow Ys$



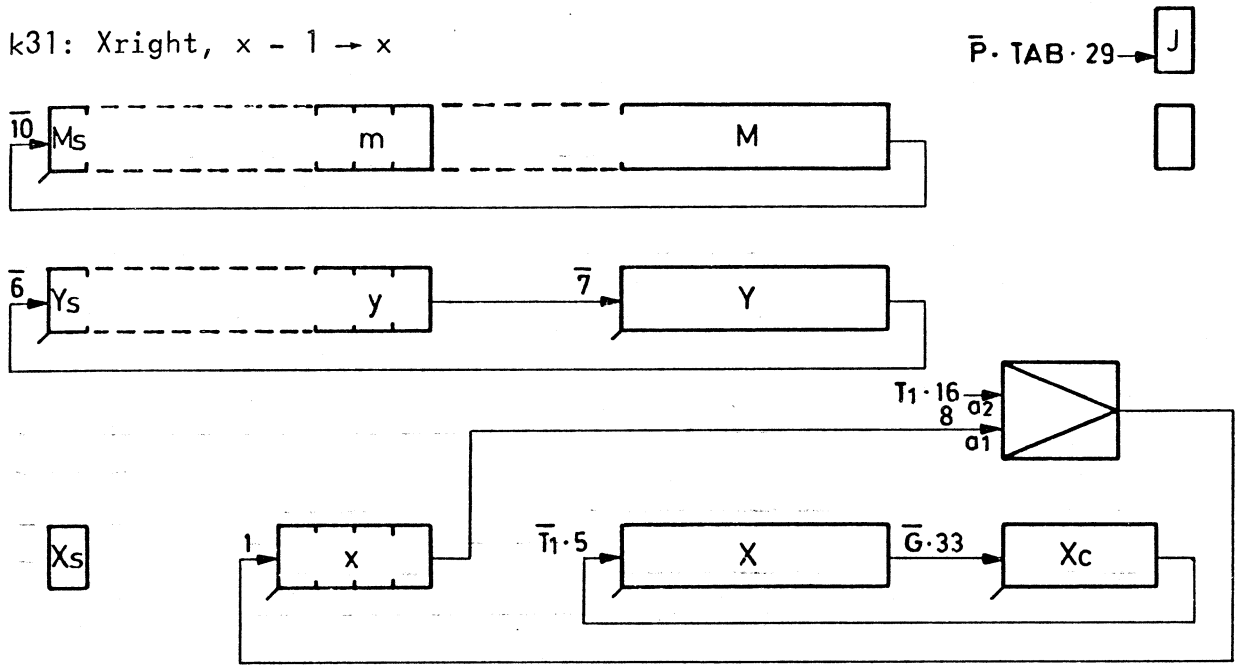
k27 (k2,3): M → M;X, X → Y, Ms → Xs, Xs → Ys



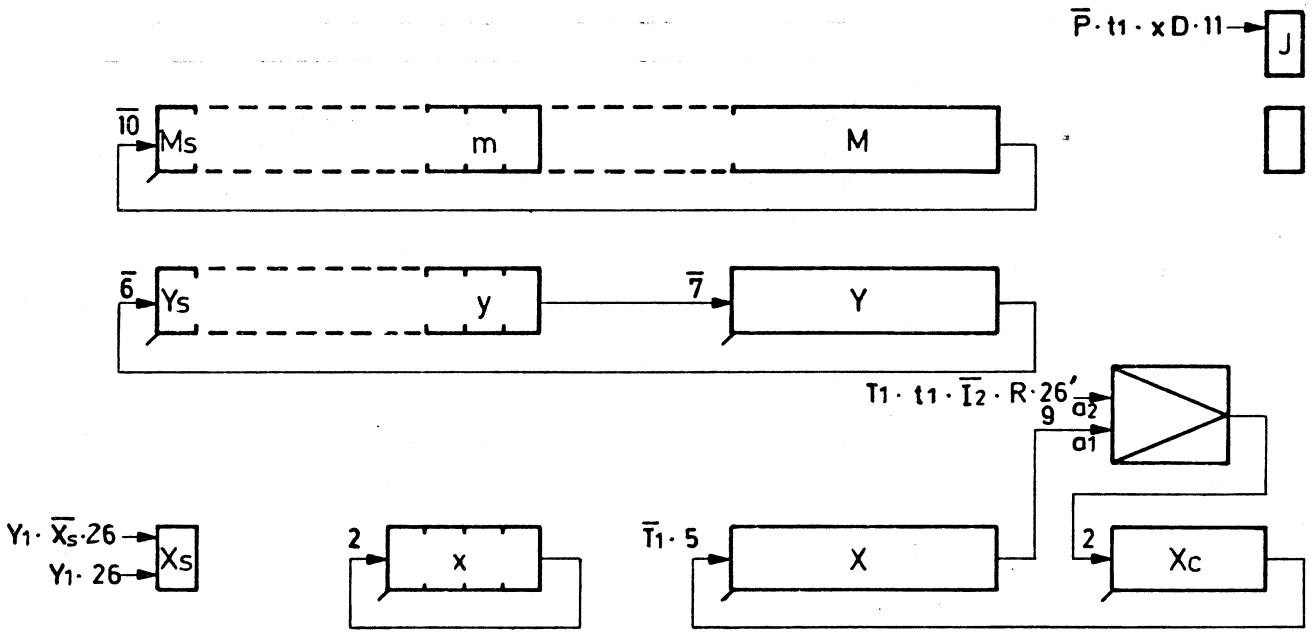
k29: 0 → M



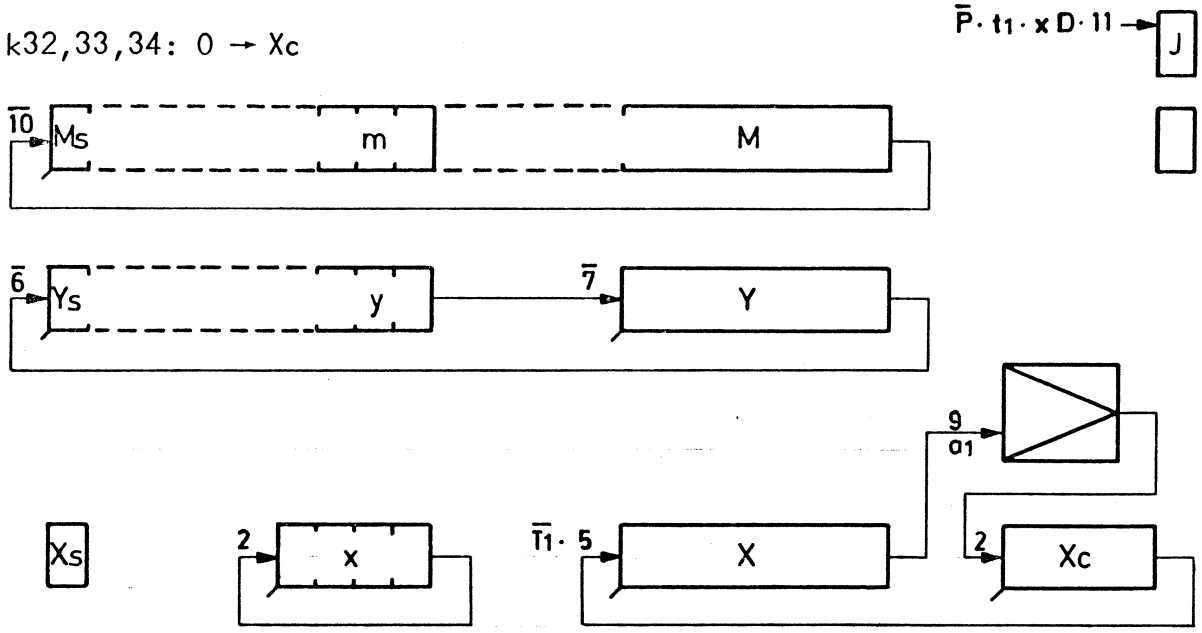
k31: Xright, x - 1 → x



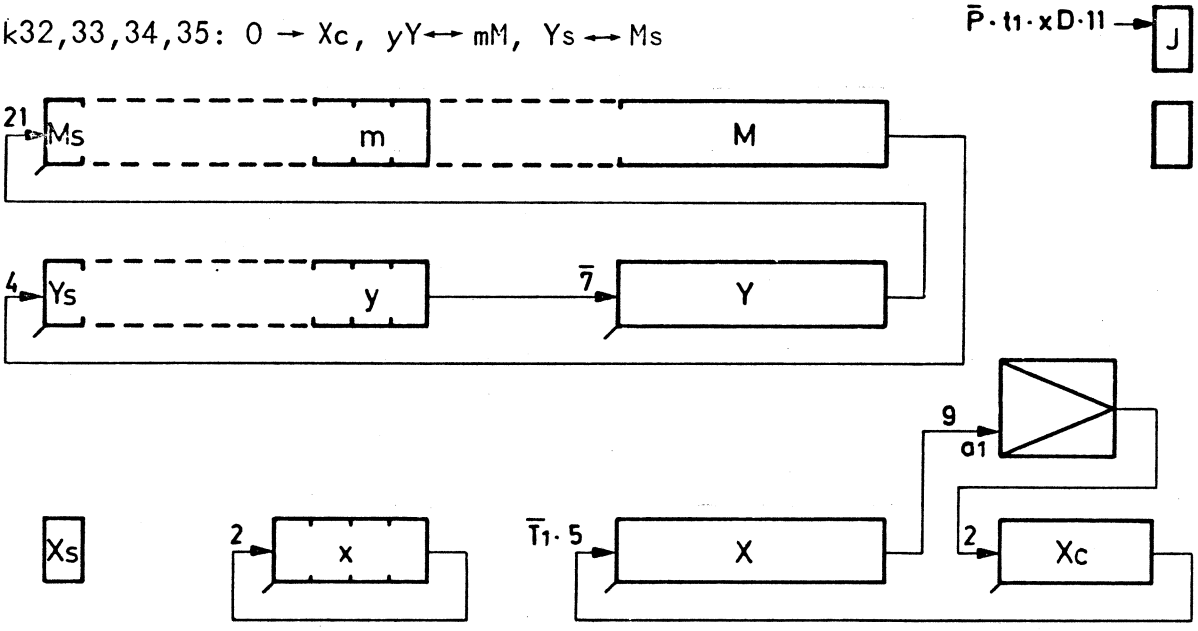
k32,33,36: 0 → Xc, Ys → Xs invert, R provides X1 + 1 → X1



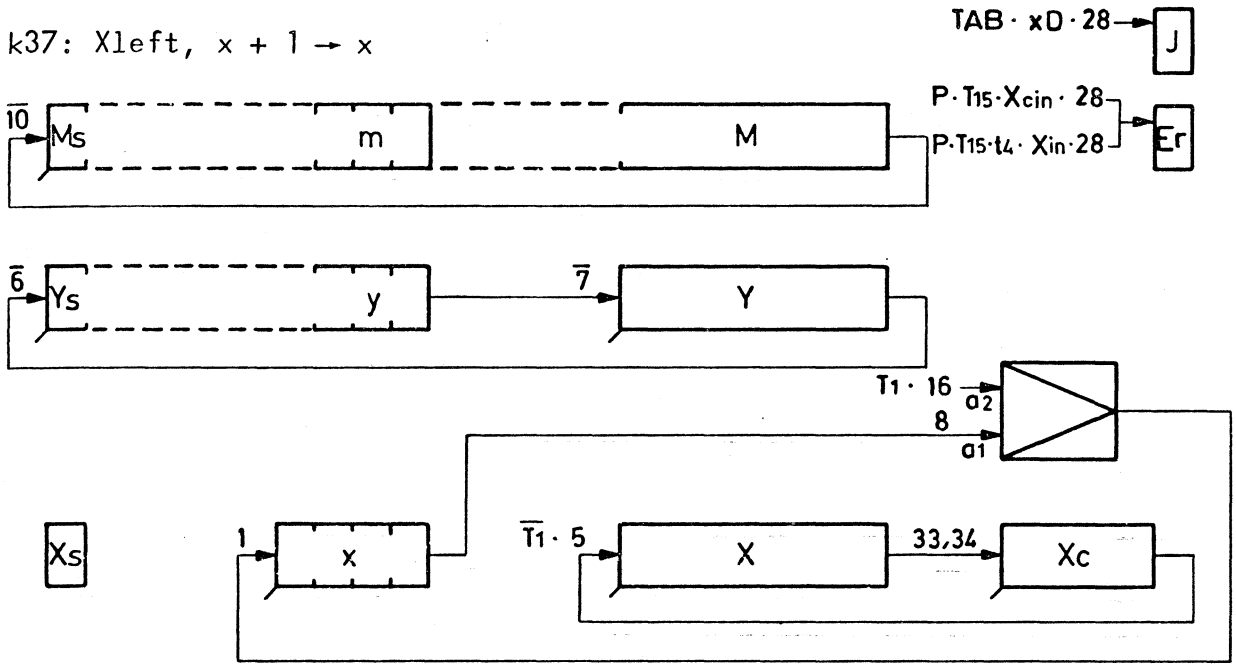
k32,33,34: 0 → Xc



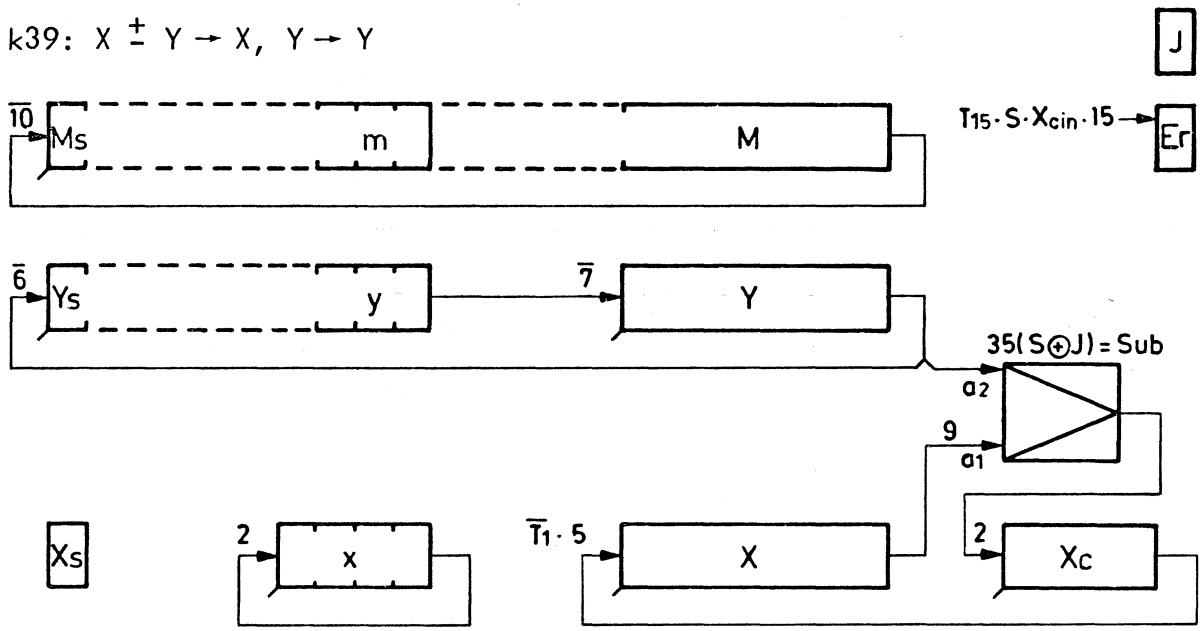
k32,33,34,35: 0 → Xc, yY ↔ mM, Ys ↔ Ms



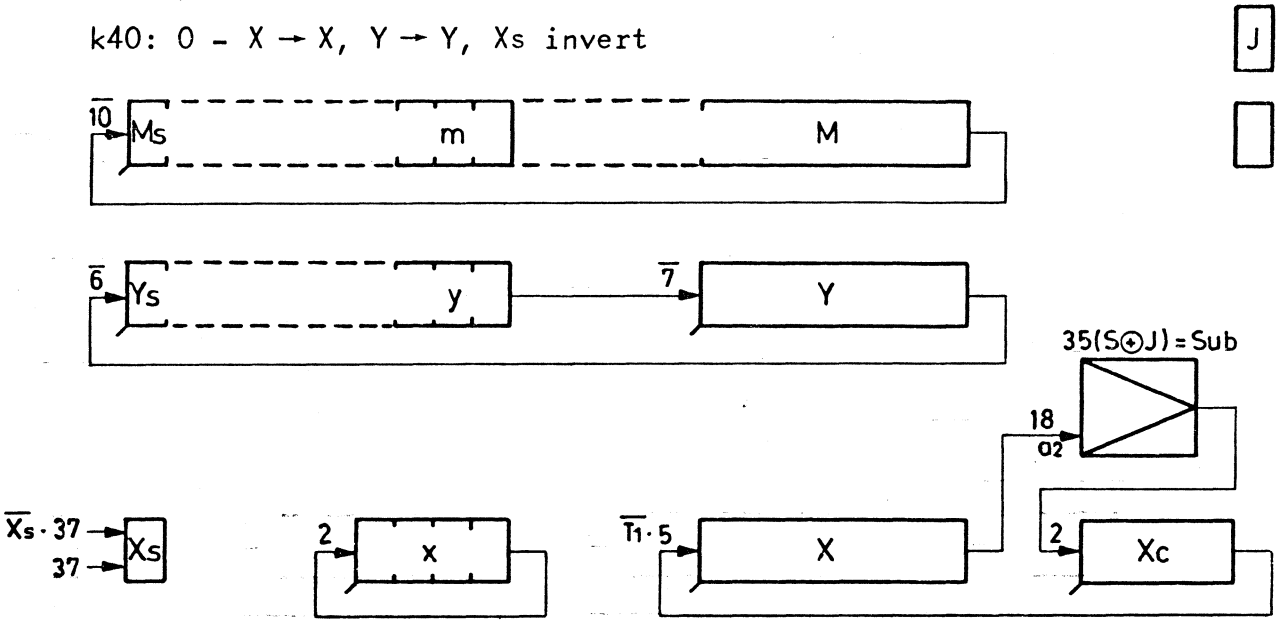
k37: Xleft, x + 1 → x



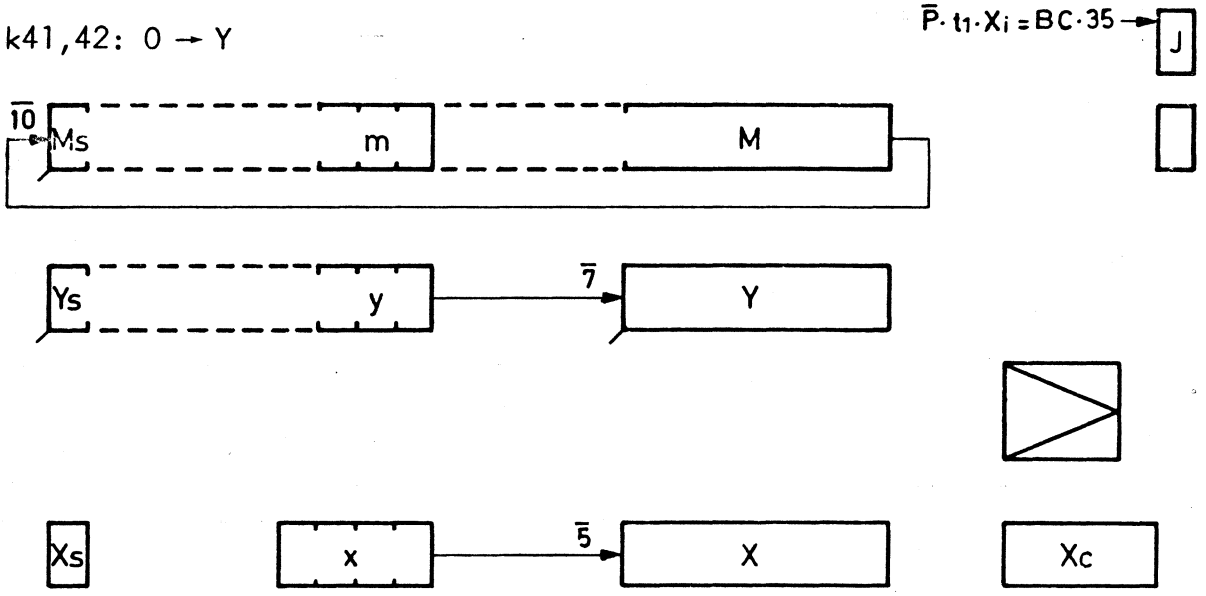
k39: X ± Y → X, Y → Y



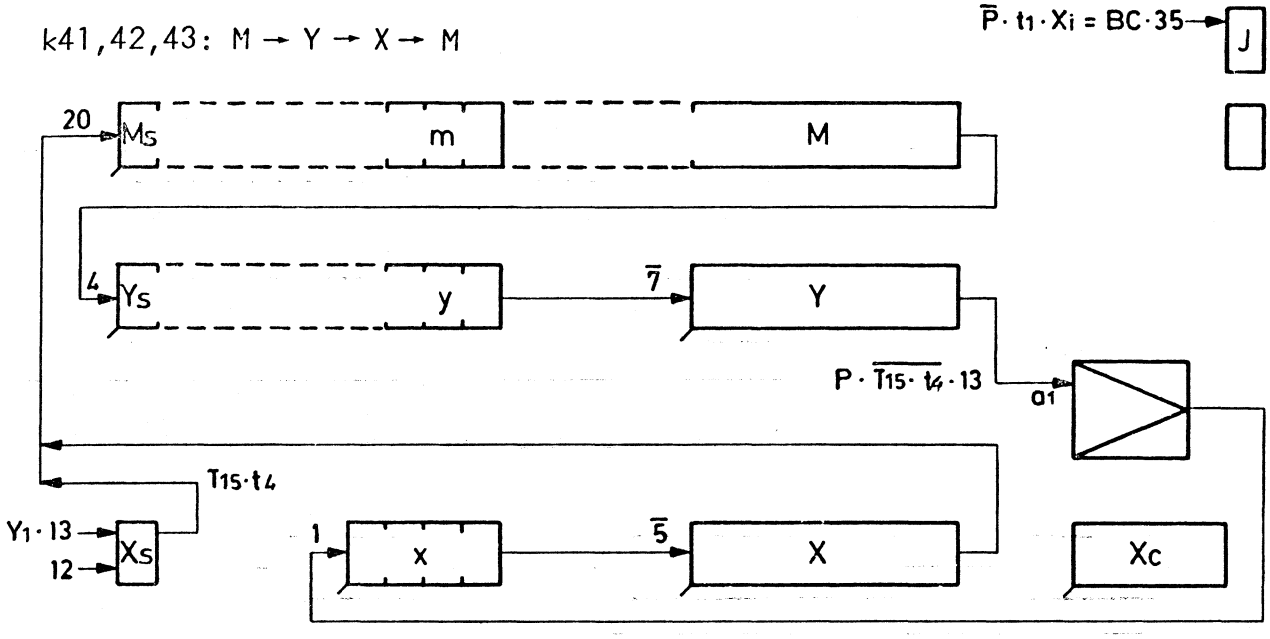
k40: 0 - X → X, Y → Y, Xs invert



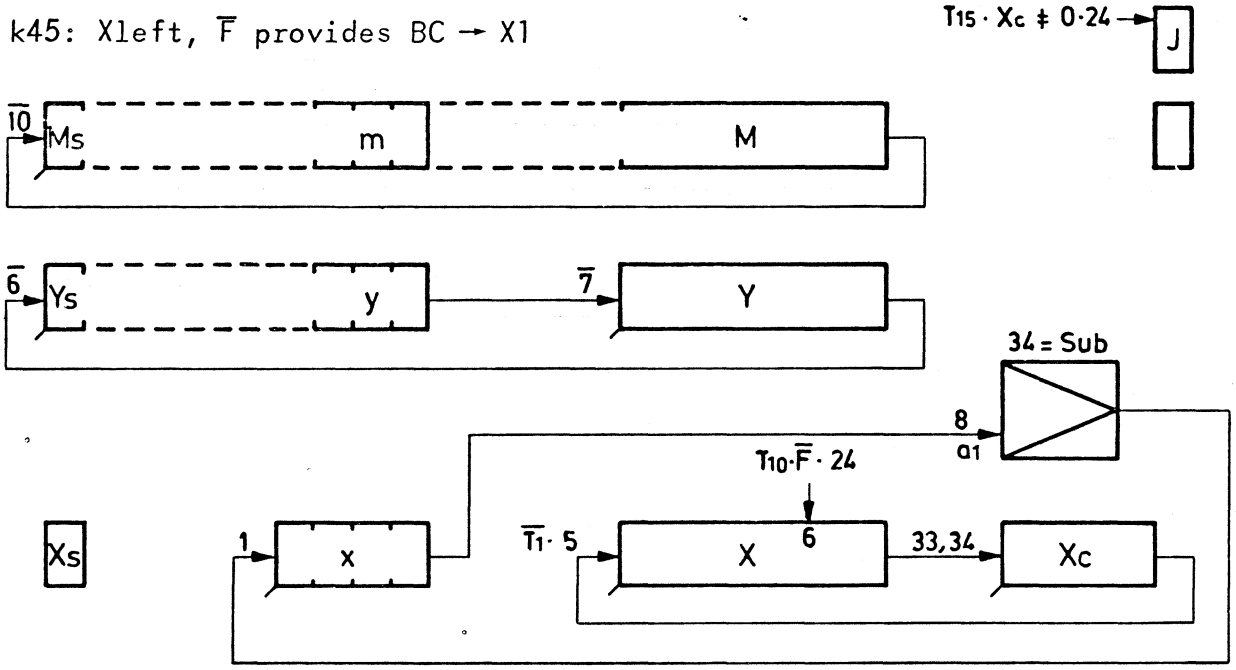
k41,42: 0 → Y



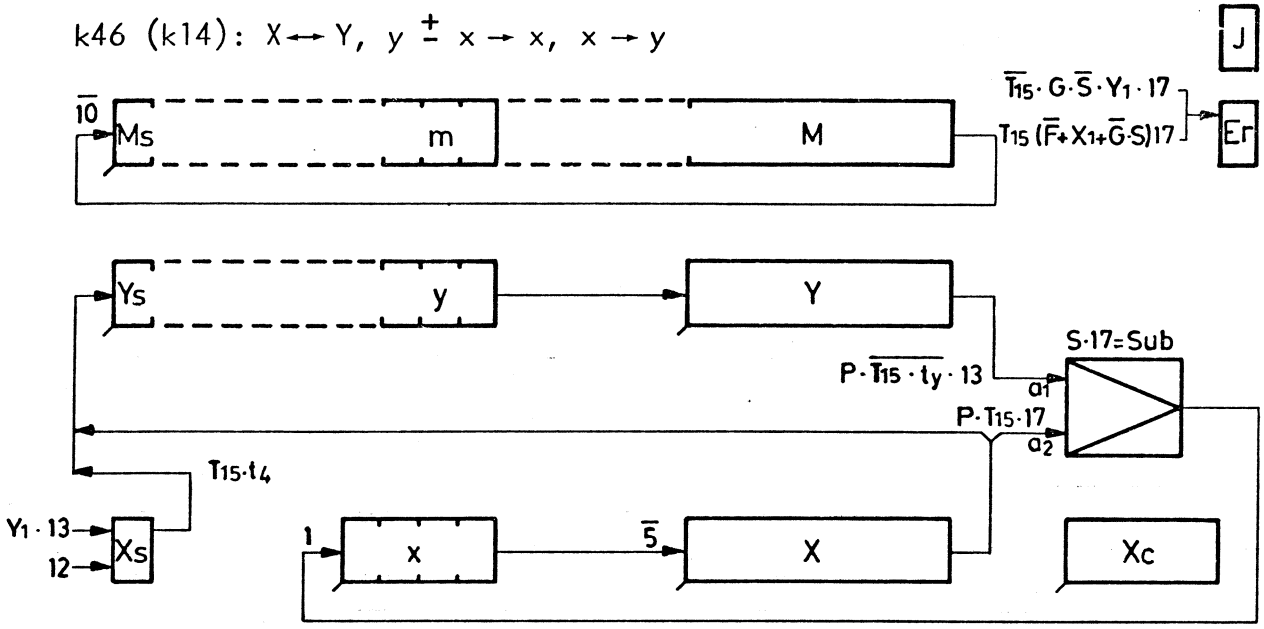
k41,42,43: M → Y → X → M



k45: Xleft, $\overline{F}$ provides BC → X1

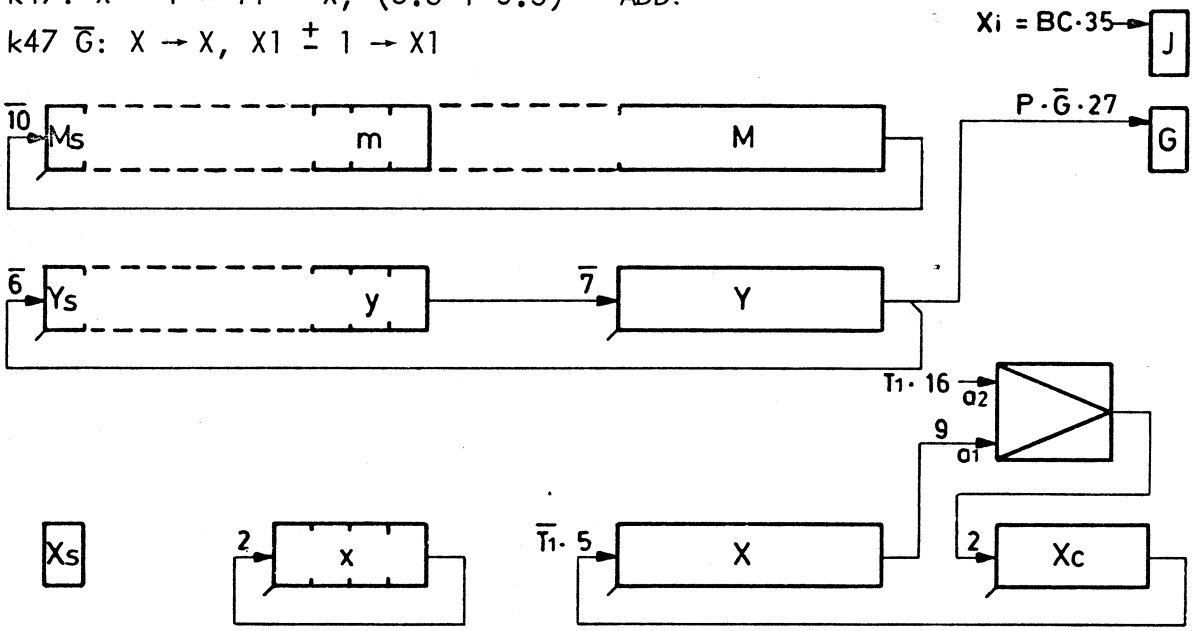


k46 (k14): X ↔ Y, y ± x → x, x → y



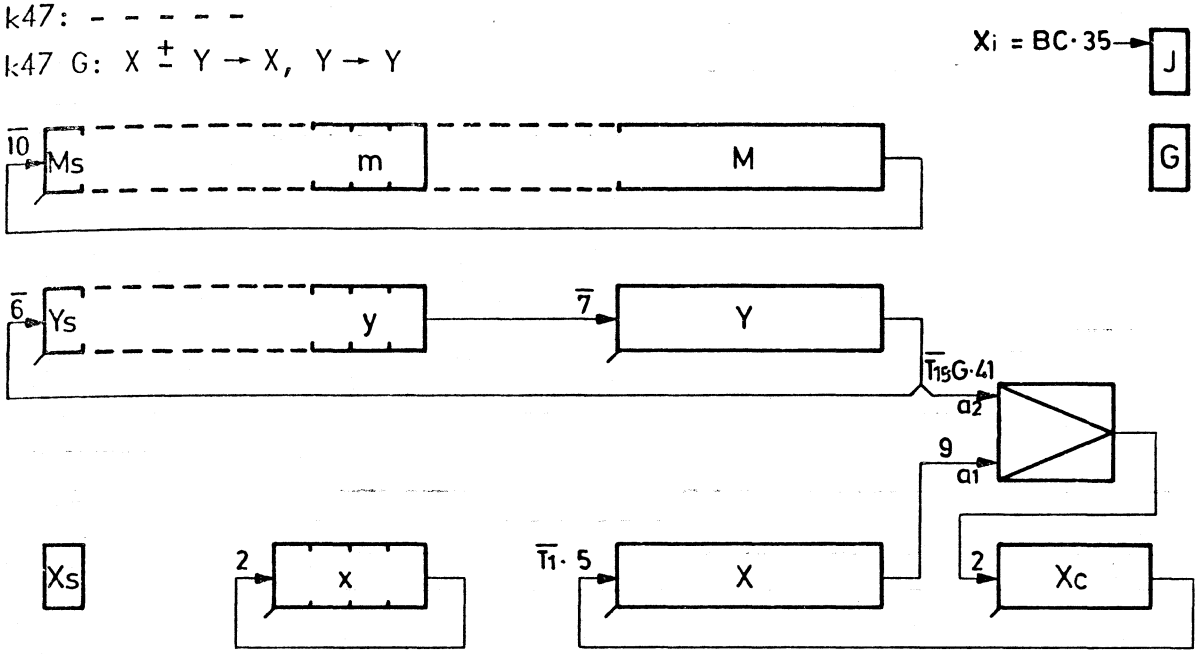
k47: X ± Y ± T1 → X, (S.J + $\overline{S}$.$\overline{J}$) → ADD.

k47 $\overline{G}$: X → X, X1 ± 1 → X1

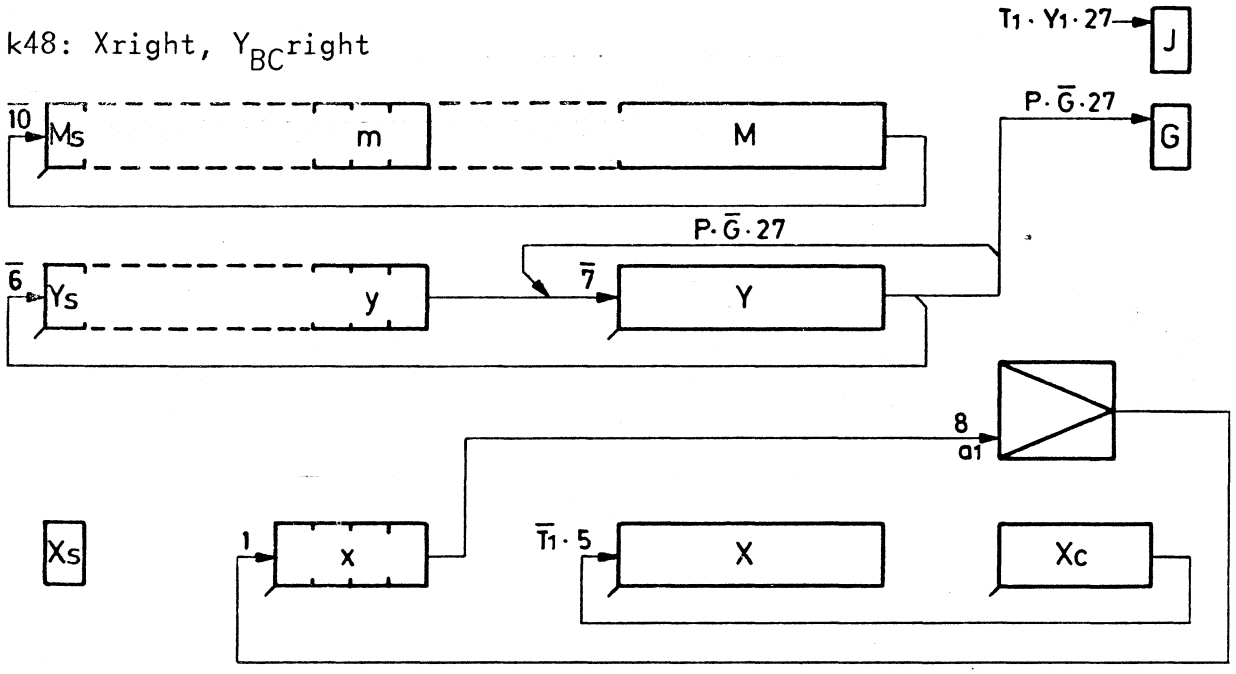


k47: - - - - - -

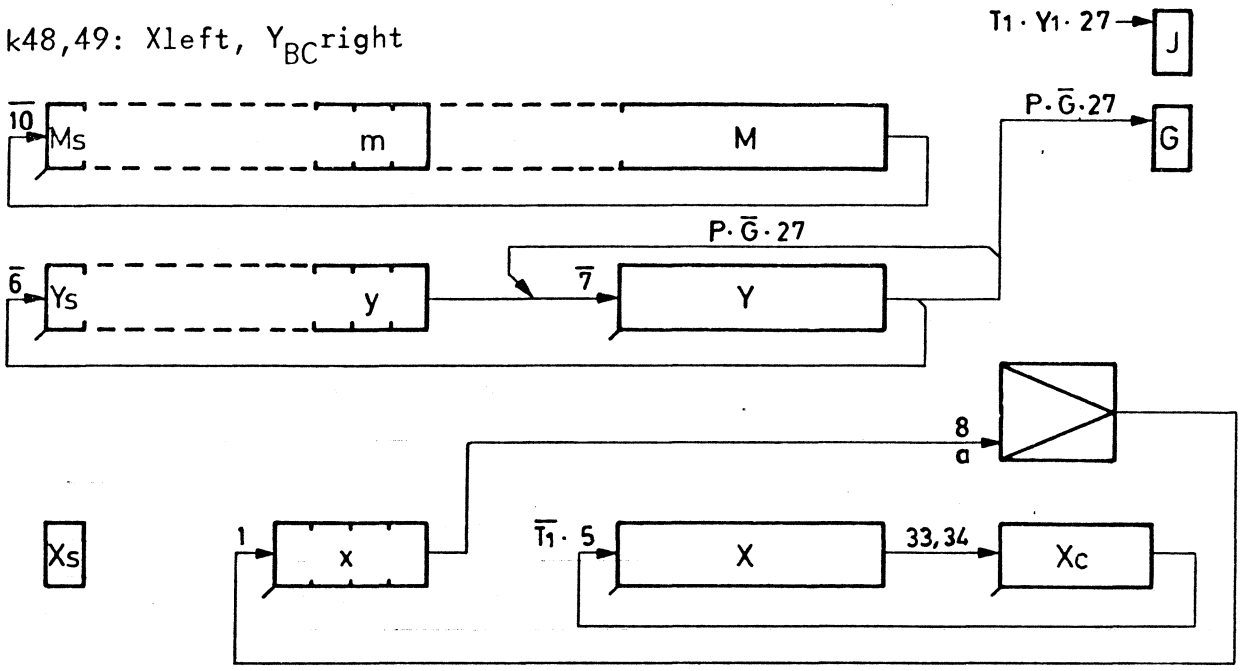
k47 G: $X \pm Y \rightarrow X,\ Y \rightarrow Y$



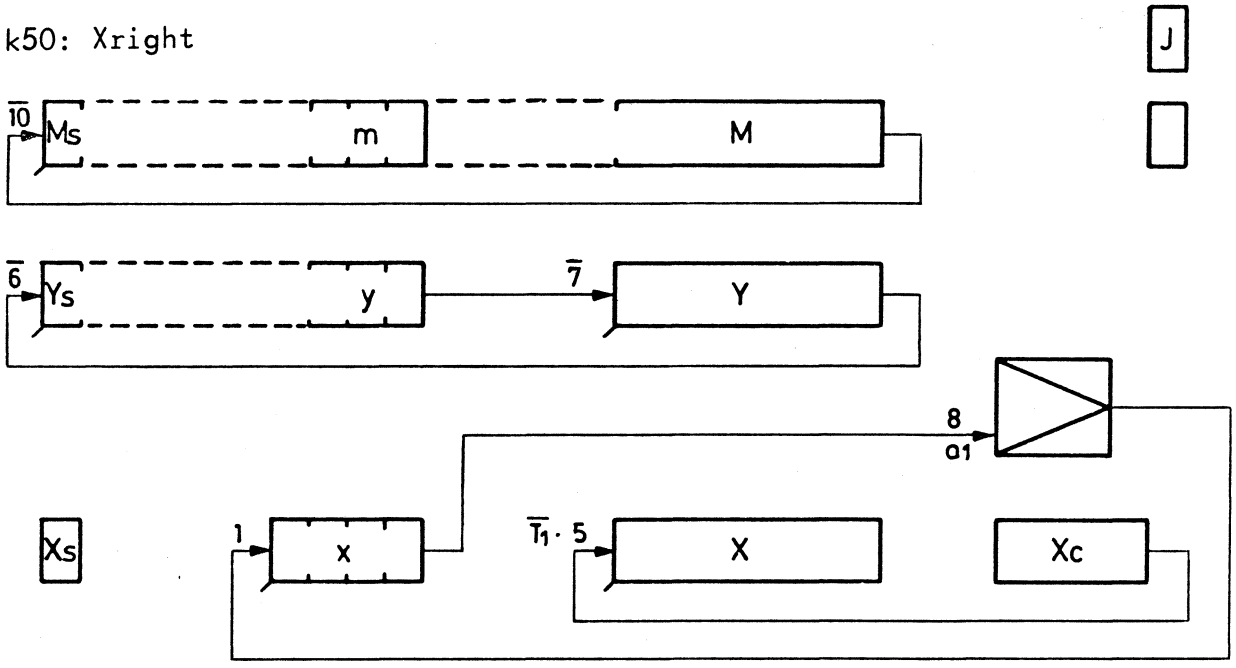
k48: Xright, Y_{BC}right



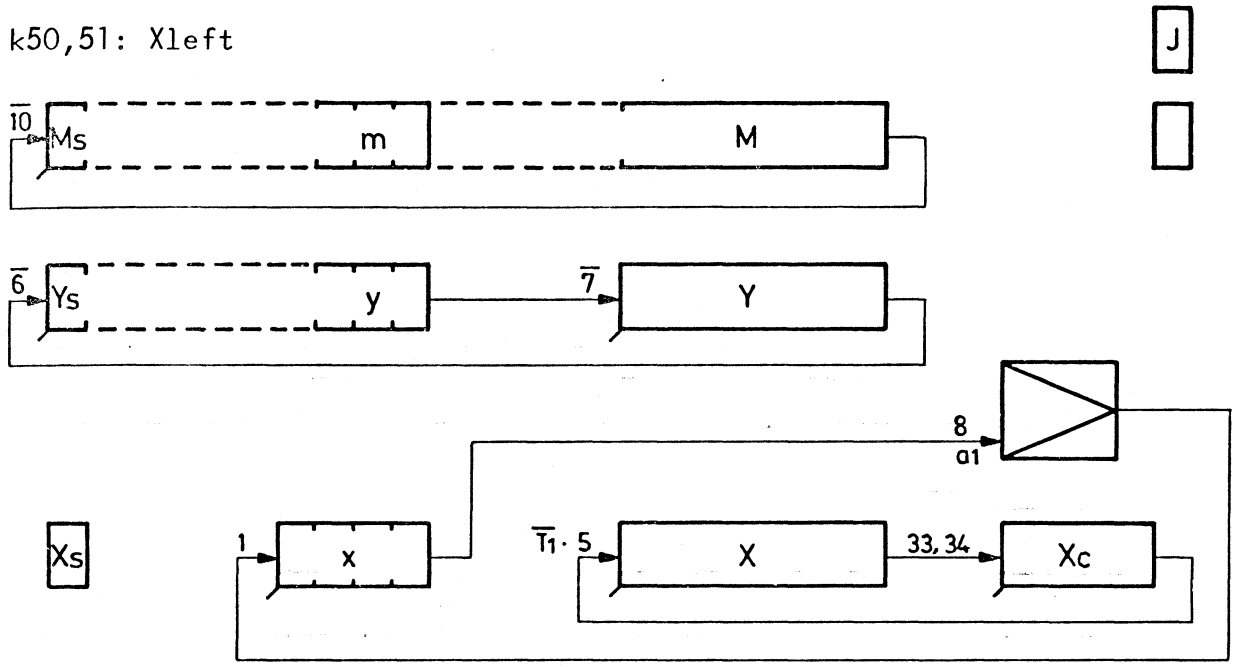
k48,49: Xleft, Y_{BC}right



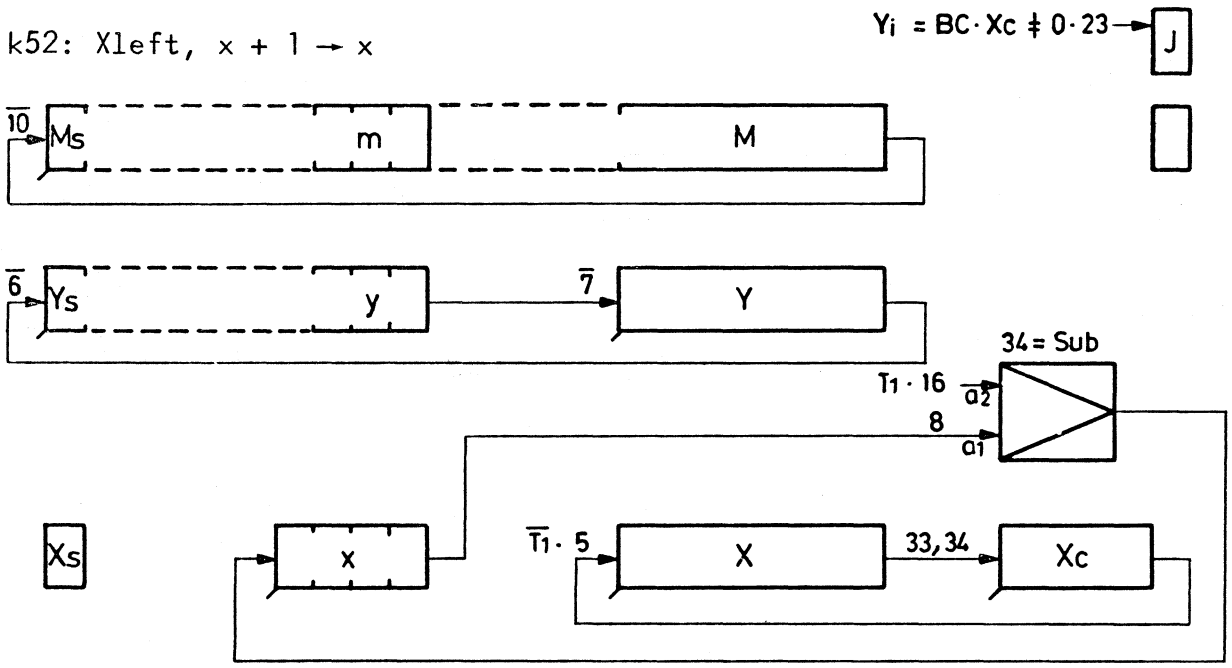
k50: Xright



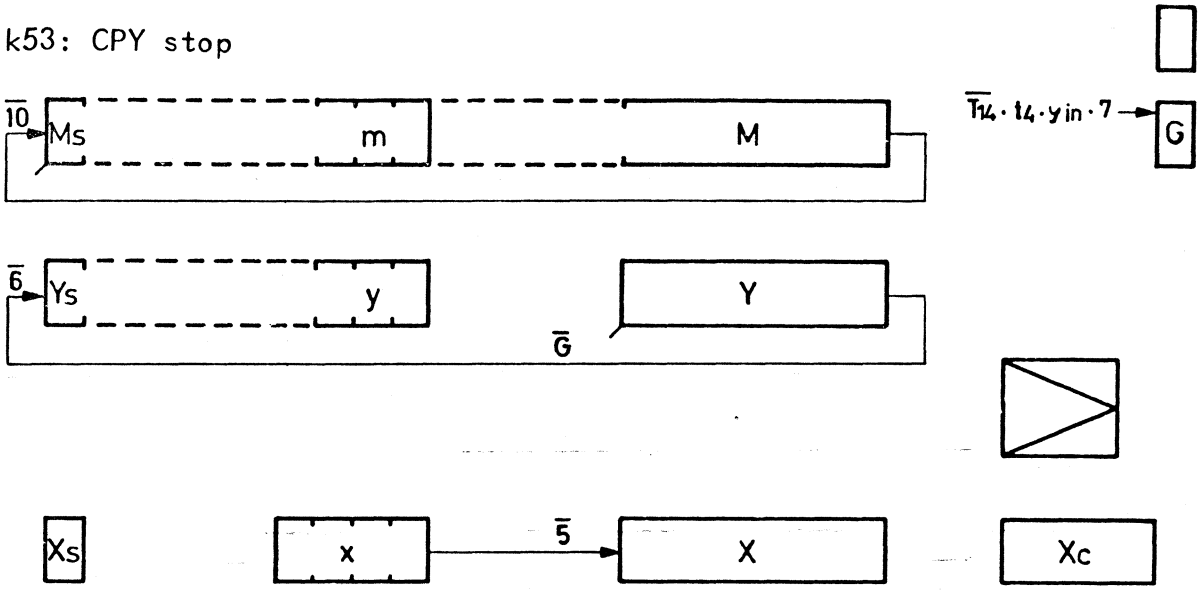
k50,51: Xleft



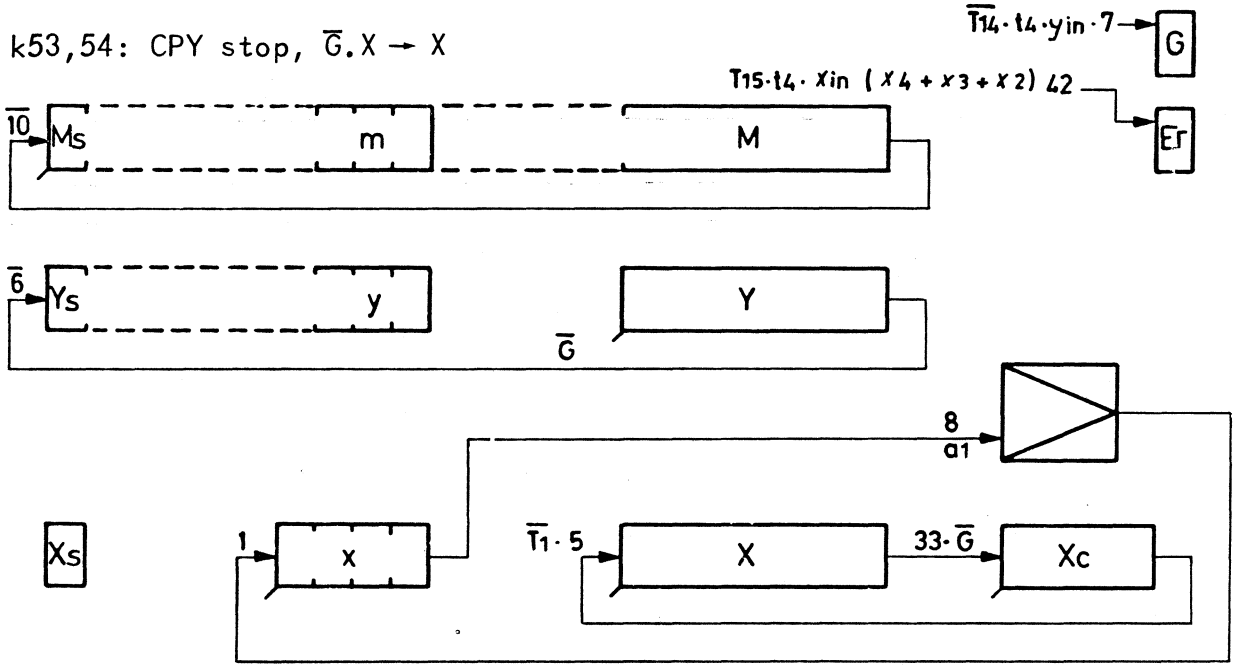
k52: Xleft, x + 1 → x

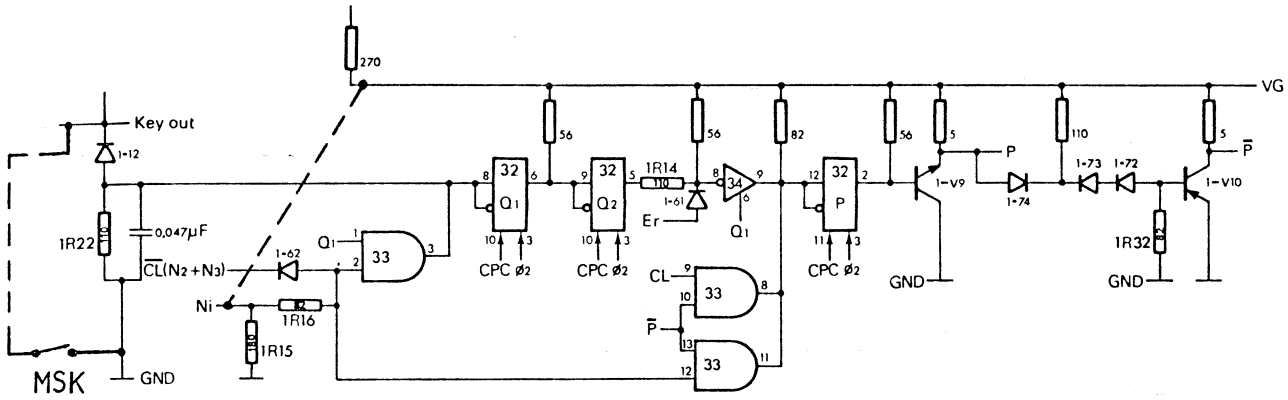


k53: CPY stop

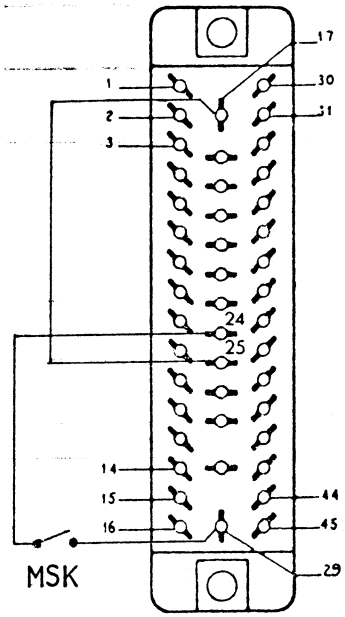


k53,54: CPY stop, G.X → X



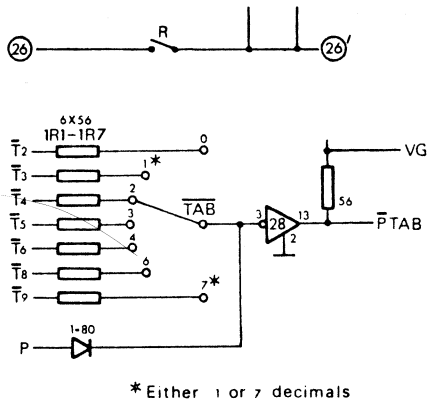


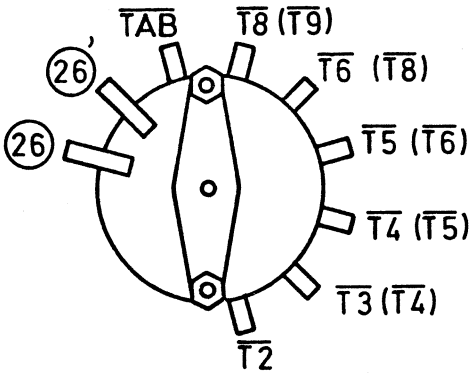
Check connector



Pin No	Signal	Pin No	Signal	
1	K1	24	Key out	←
2	K2	25	VG	←
3	K3	26	K	
4	K4	27	P	
5	K5	28	xD	
6	K6	29	GND	←
7	K7 8	30	.K	
8	K8	31	xK	
9	K9	32	+K	
10	K0	33	=K	
11		34	-K	
12		35	RV	
13		36	CL	
14	26'	37	CE	
15	26	38	+I	
16	$\overline{T5}$	39	-I	
17	Ni	40	RCI	→
18	Hs	41	CI	
19	X1	42	Xs	
20	Er	43	xL	
21		44	Ø1	
22	$\overline{T8}$	45	+L	
23	Ø2			

Fig. 6.1 Connection of the manual-step key





Rear view

Fig. 6.2 Decimal selector with corresponding wiring diagram. The signals within parentheses apply to calculators with a display capacity of 7 decimals

6 SERVICE

For this calculator the same instructions are applicable that have been given in the service manuals for other calculators containing MOS-packages.

However, the manual-step key connection differs from model to model. Fig. 6.1 shows the procedure for FACIT 1129.

Fig. 6.2 shows wiring differences between decimal selectors for 6 and 7 decimals.

TEST PROGRAM

	Decimal setting	Figure setting				Operational key K		Display				Lamps/sign x	+	-	E	I
	4	11	1111	1111	1111	K̄	RV	000	0000	0000	000.					
							RV	111	1111	1111	111.					
		222	2222	2222	22.2		RV	000	0000	0000	000.					
							RV	222	2222	2222	22.2					
		333	3333	3333	3.33		RV	000	0000	0000	000.					
							RV	333	3333	3333	3.33					
		444	4444	4444	.444		RV	000	0000	0000	000.					
							RV	444	4444	4444	.444					
		555	5555	555.	5555		RV	000	0000	0000	000.					
							RV	555	5555	555.	5555					
		666	6666	66.6	6666		RV	000	0000	0000	000.					
							RV	666	6666	66.6	6666					
		777	7777	7.77	7777		RV	000	0000	0000	000.					
							RV	777	7777	7.77	7777					
		888	8888	.888	8888		RV	000	0000	0000	000.					
							RV	888	8888	.888	8888					
		999	9999	9999	999.		RV	000	0000	0000	000.					
							RV	999	9999	9999	999.					
							C	000	0000	0000	000.					
	0				5		=	000	0000	0000	005.					
1)	1						=	000	0000	0000	05.0					
	2						=	000	0000	0000	5.00					
	3						=	000	0000	0005	.000					
	4						=	000	0000	005.	0000					
	6						=	000	0000	5.00	0000					
2)	7						=	000	0005	.000	0000					
2)	6						=	000	0000	5.00	0000					
	4						=	000	0000	005.	0000					
	3						=	000	0000	0005	.000					
	2						=	000	0000	0000	5.00					
1)	1						=	000	0000	0000	05.0					
	0						=	000	0000	0000	005.					
					3		+I	000	0000	0000	003.					x
							C	000	0000	0000	000.					x
1)	6						+I	000	0000	0.00	0000					x
1)							RCI	000	0000	3.00	0000					x
2)	7						+I	000	0000	.000	0000					x
							RCI	000	0003	.000	0000					x
	0						+I	000	0000	0000	003.					x
							RCI	000	0000	0000	006.					x
		11	1111	1111	1111		+I	111	1111	1111	111.					x
							C	000	0000	0000	000.					x
	2						+I	000	0000	0000	0.00				x	x
							C	000	0000	0000	000.					x
							CI	000	0000	0000	000.					
					5		:	000	0000	0000	005.		x			
							x	000	0000	0000	005.	x				
							-	000	0000	0000	025.			x		

1) Only calculators with a setting capacity of 6 decimals.

2) Only calculators with a setting capacity of 7 decimals.

K̄ means released constant key (K-key).

Decimal setting	Figure setting	Operational key		Display				Lamps/sign				
		K						x	+	-	E	I
	Power switch OFF ON 2 sec.	$\overline{K}$		000	0000	0000	000.					
	3 times		=	000	0000	0000	0.00					
			RCI	000	0000	0000	000.					
4	123 4567 .890		RV	000	0000	0000	000.					
			=	000	1234	567.	8900					
	123 4567 .890		RV	000	1234	567.	8900					
	987 6543 .210 0000		RV	000	0123	4567	.890					
			=	001	1111	111.	1000					
	888 8888 8.89 9999		=	009	9999	999.	9999					
			C	000	0000	0000	000.					
	345 678. 9876 5432			345	678.	9876	5432				x	
	1289			345	678.	9876	5432				x	
			RV	345	678.	9876	5432				x	
			=	345	678.	9876	5432				x	
			C	000	0000	0000	000.					
	12 3456 7891 2345			123	4567	8912	345.					
	67			234	5678	9123	456.				x	
			C	000	0000	0000	000.					
	11 1111 111. 1111		=	011	1111	111.	1111					
	55 5555 555. 5555		=	066	6666	666.	6666					
	9 9999 9999		=	166	6666	665.	6666					
	.33 3444		=	166	6666	666.	0000					
	.33 3444		-	166	6666	665.	6666					
	88 8888 888. 8888		-	077	7777	776.	7778					
	7 7777 7777		-	000	0000	000.	2222			x		
	.333 3333		-	000	0000	000.	5555			x		
	.222 2222		=	000	0000	000.	3333			x		
	.333 3333		=	000	0000	000.	0000			x		
	111 1111 111. 1111		=	111	1111	111.	1111					
	444 4444 444. 4444		-	333	3333	333.	3333			x		
			RV	000	0000	0000	000.					
	333 3333 333. 3333		CE	000	0000	0000	000.					
	777 7777 777. 7777		=	444	4444	444.	4444					
	999 9999 999. 5556		=	444	4444	444.	0000				x	
			C	000	0000	0000	000.					
	111 1111 1111		=	111	1111	111.	0000				x	
			C	000	0000	0000	000.					
	111 1111 1111		RV	000	0000	0000	000.					
			-	111	1111	111.	0000				x	
			C	000	0000	0000	000.					
	753 .357		x	000	0000	0753	.357	x				
	951 .159		=	000	0716	562.	2907					
			x	000	0716	562.	2907	x				
	.789		=	000	0565	367.	6473					
			RV	000	0716	562.	2907					
			x	000	0716	562.	2907	x				

Decimal setting	Figure setting	Operational key K		Display	Lamps/sign ×	+	-	E	I
	.456	K̄	-	000 0326 752. 4045			×		
	10 0000 0000 0000		×	100 0000 0000 000.	×				
	1		=	000 0000 0000 000.				×	
			C	000 0000 0000 000.					
	1		×	000 0000 0000 0C1.	×				
	10 0000 0000 0000		=	000 0000 0000 001.				×	
			C	000 0000 0000 000.					
	1 2345 6789		×	000 0012 3456 789.	×				
	45 6789		=	070 1098 7590 525.				×	
			C	000 0000 0000 000.					
	2 .222		×	000 0000 0002 .222	×				
			-	000 0000 004. 9372			×		
			RV	000 0000 0002 .222					
	12 3.45		×	000 0000 0012 3.45	×				
	123. 4567		-	000 0015 240. 7296			×		
			RV	000 0000 0012 3.45					
	123 4567		×	000 0000 1234 567.	×				
	.12		-	000 0001 4814 8.04			×		
			=	000 1086 418. 9600					
	999 9999 99.9		:	000 0999 9999 99.9		×			
	8 .100		-	000 0123 4567 90.1			×		
			RV	000 0000 0008 .100			×		
	5		:	000 0000 0000 005.		×			
	9		=	000 0000 000. 5555					
			=	000 0000 009. 5555					
	2		:	000 0000 0000 002.		×			
			-	000 0000 0000 004.				×	
			C	000 0000 0000 000.					
	5		:	000 0000 0000 005.		×			
	0		=	147 4444 4444 461.				×	
			C	000 0000 0000 000.					
	1 0000 0000 0000		:	010 0000 0000 000.		×			
	.01		-	000 0000 000. 0100				×	
			C	000 0000 0000 000.					
	1 2345 6789 .000		:	001 2345 6789 .000		×			
	10 0000 0000 0000		=	000 0456 788. 9944				×	
			C	000 0000 0000 000.					
	°5		:	000 0000 0000 005.		×			
	9		=	000 0000 000. 5555					
	4		:	000 0000 0000 004.		×			
	9		=	000 0000 000. 4444					
	5		:	000 0000 0000 005.		×			
	9		×	000 0000 000. 5555	×				
			C	000 0000 0000 000.					
	5		-I	000 0000 005. 0000					×
			C	000 0000 0000 000.					×
	3		-	000 0000 003. 0000			×		×
			×	000 0000 003. 0000	×		×		×

Decimal setting	Figure setting				Operational key		Display				Lamps/sign				
					K						×	+	-	E	I
					$\bar{K}$	RCI	000	0000	005.	0000	×		×		×
						-	000	0000	015.	0000			×		×
						RV	000	0000	003.	0000			×		×
						×	000	0000	003.	0000	×		×		×
						RCI	000	0000	005.	0000	×		×		×
						=	000	0000	015.	0000					×
						RV	000	0000	003.	0000			×		×
						RV	000	0000	015.	0000					×
4 R				11		+I	000	0000	011.	0000					×
						RV	000	0000	003.	0000			×		×
						×	000	0000	003.	0000	×		×		×
						RCI	000	0000	006.	0000	×				×
						-	000	0000	018.	0000					×
						RV	000	0000	003.	0000			×		×
						×	000	0000	003.	0000	×		×		×
						RCI	000	0000	006.	0000	×				×
						RV	000	0000	003.	0000	×		×		×
						=	000	0000	018.	0000			×		×
						RV	000	0000	006.	0000					×
						CI	000	0000	006.	0000					
			753	.357		×	000	0000	0753	.357	×				
			456	.789		=	000	0344	125.	1907					
						:	000	0344	125.	1907		×			
						RV	000	0000	0753	.357		×			
						=	000	0000	456.	7890					
						×	000	0000	456.	7890	×				
						RV	000	0000	0753	.357	×				
						=	000	0344	125.	1907					
			111	.111		×	000	0000	0111	.111	×				
						-	000	0012	345.	6543			×		
						RV	000	0000	0111	.111					
						×	000	0000	0111	.111	×				
						=	000	0012	345.	6543					
						C	000	0000	0000	000.					
			123	.456		×	000	0000	0123	.456	×				
			456	.789		×	000	0056	393.	3427	×				
			789	.12		:	004	4501	114.	5914		×			
			1	23.4		:	000	0360	624.	9156		×			
			456	.789		:	000	0000	789.	4781		×			
			789	.557		=	000	0000	000.	9999					
						C	000	0000	0000	000.					
4				123	K	×	000	0000	0000	123.	×				
						=	000	0000	0015	129.	×				
				456		=	000	0000	0056	088.	×				
						RV	000	0000	0000	123.	×				
						RV	000	0000	0056	088.	×				
				789		×	000	0000	0000	789.	×				

Decimal setting	Figure setting				Operational key		Display				Lamps/sign				
					K						×	÷	-	E	I
					K	RV	000	0000	0000	123.	×				
						=	000	0000	0097	047.	×				
				123		=	000	0000	0097	.047	×				
						=	000	0007	6570	.083	×				
			3.	0000		-	000	0002	367.	0000	×		×		
					$\bar{K}$		000	0002	367.	0000			×		
		8888	.999	9999		=	000	0006	521.	9999					
		8478	.000	1000		=	000	0015	000.	0000					
				5		:	000	0000	0000	005.		×			
				9	K	=	000	0000	000.	5555		×			
				.4		=	000	0000	000.	0444		×			
				.03		=	000	0000	000.	0033		×			
				.002		-	000	0000	000.	0002		×		×	
						RV	000	0000	0000	009.		×			
						C	000	0000	0000	000.					
				2		:	000	0000	0000	002.		×			
						×	000	0000	0000	002.	×				
						=	000	0000	0000	004.	×				
						=	000	0000	0000	008.	×				
						=	000	0000	0000	016.	×				
						=	000	0000	0000	032.	×				
						=	000	0000	0000	064.	×				
						=	000	0000	0000	128.	×				
						=	000	0000	0000	256.	×				
						=	000	0000	0000	512.	×				
						=	000	0000	0001	024.	×				
						=	000	0000	0002	048.	×				
						×	000	0000	0002	048.	×				
						:	000	0000	0002	048.		×			
						RV	000	0000	0000	002.		×			
4						=	000	0001	024.	0000		×			
						=	000	0000	512.	0000		×			
						=	000	0000	256.	0000		×			
						=	000	0000	128.	0000		×			
						=	000	0000	064.	0000		×			
						=	000	0000	032.	0000		×			
						=	000	0000	016.	0000		×			
						=	000	0000	008.	0000		×			
						=	000	0000	004.	0000		×			
						=	000	0000	002.	0000		×			
						RV	000	0000	0000	002.		×			
						RV	000	0000	002.	0000		×			
						C	000	0000	0000	000.					
				123		×	000	0000	0000	123.	×				
					$\bar{K}$	=	000	0000	0015	129.					
					K	:	000	0000	0015	129.		×			
				123	$\bar{K}$		000	0000	0000	123.		×			
						=	000	0000	123.	0000					

Decimal setting	Figure setting				Operational key		Display				Lamps/sign				
					K						x	+	-	E	I
					K̄	C	000	0000	0000	000.					
			123	.456	K	=	000	0000	123.	4560					
						=	000	0000	246.	9120					
						=	000	0000	370.	3680					
						=	000	0000	493.	8240					
						=	000	0000	617.	2800					
						=	000	0000	740.	7360					
						=	000	0000	864.	1920					
						=	000	0000	987.	6480					
						=	000	0001	111.	1040					
						=	000	0001	234.	5600					
						-	000	0001	111.	1040					
						-	000	0000	987.	6480					
						-	000	0000	864.	1920					
						-	000	0000	740.	7360					
						-	000	0000	617.	2800					
						-	000	0000	493.	8240					
						-	000	0000	370.	3680					
4						-	000	0000	246.	9120					
						-	000	0000	123.	4360					
						-	000	0000	000.	0000					
						-	000	0000	123.	4560			x		
						-	000	0000	246.	9120			x		
						C	000	0000	0000	000.					
			456	.789		-	000	0000	456.	7890			x		
						-	000	0000	913.	5780			x		
						=	000	0000	456.	7890			x		
						RV	000	0000	456.	7890					
					K̄	=	000	0000	000.	0000			x		
						=	000	0000	000.	0000					
				123		=	000	0000	123.	0000					
		789	.000	0000	K	=	000	0000	912.	0000					
						RV	000	0000	789.	0000					
						-	000	0000	123.	0000					
				123		=	000	0000	246.	0000					
				456		=	000	0000	702.	0000					
				789		-	000	0000	087.	0000			x		
						C	000	0000	0000	000.					
			258	.852	K̄	x	000	0000	0258	.852	x				
						+I	000	0067	004.	3579					x
			852	.258		x	000	0000	0852	.258	x				x
						+I	000	0726	343,	6985					x
						RCI	000	0793	348.	0564					x
			852	.258		x	000	0000	0852	.258	x				x
						-I	000	0726	343.	6985					x
			258	.852		x	000	0000	0258	.852	x				x
						-I	000	0067	004.	3579					

Decimal setting	Figure setting				Operational key		Display				Lamps/sign				
					K						×	÷	-	E	I
					K̄	C	000	0000	0000	000.					
	999	9999	.999	9999		+I	000	9999	999.	9999					×
			8765	4321		×	000	0008	7654	321.	×				×
						+I	573	5406	2971	128.				×	×
						C	000	0000	0000	000.					×
						RCI	000	9999	999.	9999					×
4	11	1111	1111	1111		+I	111	1111	111.	0111				×	×
						C	000	0000	0000	000.					×
						CI	000	0000	0000	000.					
	999	9999	999.	9999		+I	999	9999	999.	9999					×
			.	0001		+I	000	0000	000.	0001				×	
						C	000	0000	0000	000.					
						CI	000	0000	0000	000.					
				5	K	×	000	0000	0000	005.	×				
				9		+I	000	0000	045.	0000	×				×
				6		+I	000	0000	030.	0000	×				×
						RV	000	0000	0000	005.	×				×
						RCI	000	0000	075.	0000	×				×
						C	000	0000	0000	000.					×
						CI	000	0000	0000	000.					
4 R				5		:	000	0000	0000	005.		×			
				9		+I	000	0000	000.	5556		×			×
				4		+I	000	0000	000.	4444		×			×
						RCI	000	0000	001.	0000		×			×
						C	000	0000	0000	000.					×
						CI	000	0000	0000	000.					
6 R			.555	5556		×	000	0000	.555	5556	×				
						=	000	0000	0,30	8642	×				
	1	0000	0000	0000		:	010	0000	0000	000.		×			
				.1		=	010	0000	0000	000.		×		×	
						C	000	0000	0000	000.					
				1	K̄	:	000	0000	0000	001.		×			
				6		=	000	0000	0,16	6667					
						C	000	0000	0000	000.					

	N3	N2	N1
n0	0	0	0
n1	0	0	1
n2	0	1	0
n3	0	1	1
n4	1	0	0
n5	1	0	1
n6	1	1	0
n7	1	1	1

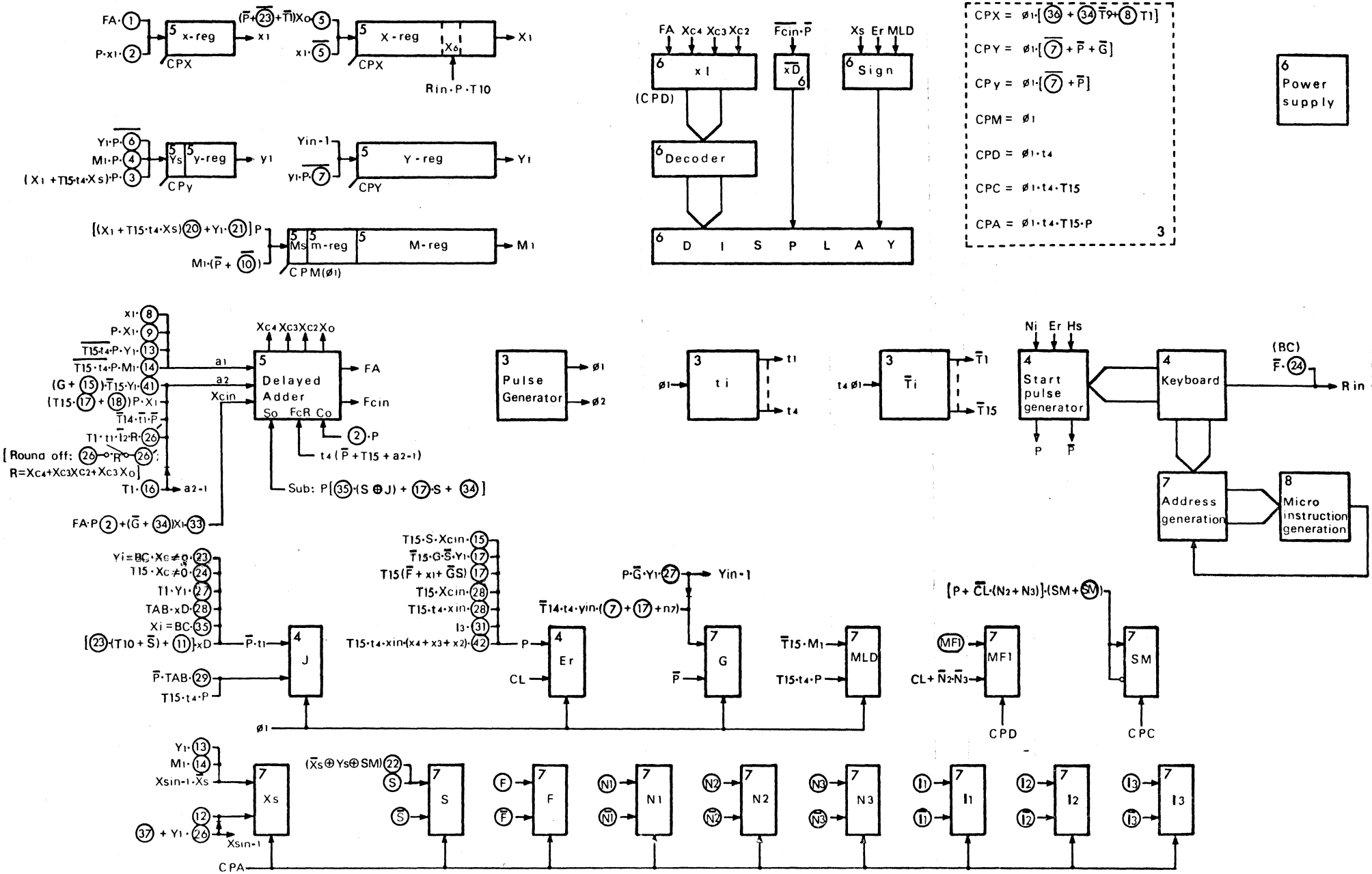
k38

$\bar{X}s \oplus Ys \oplus SM \rightarrow S$

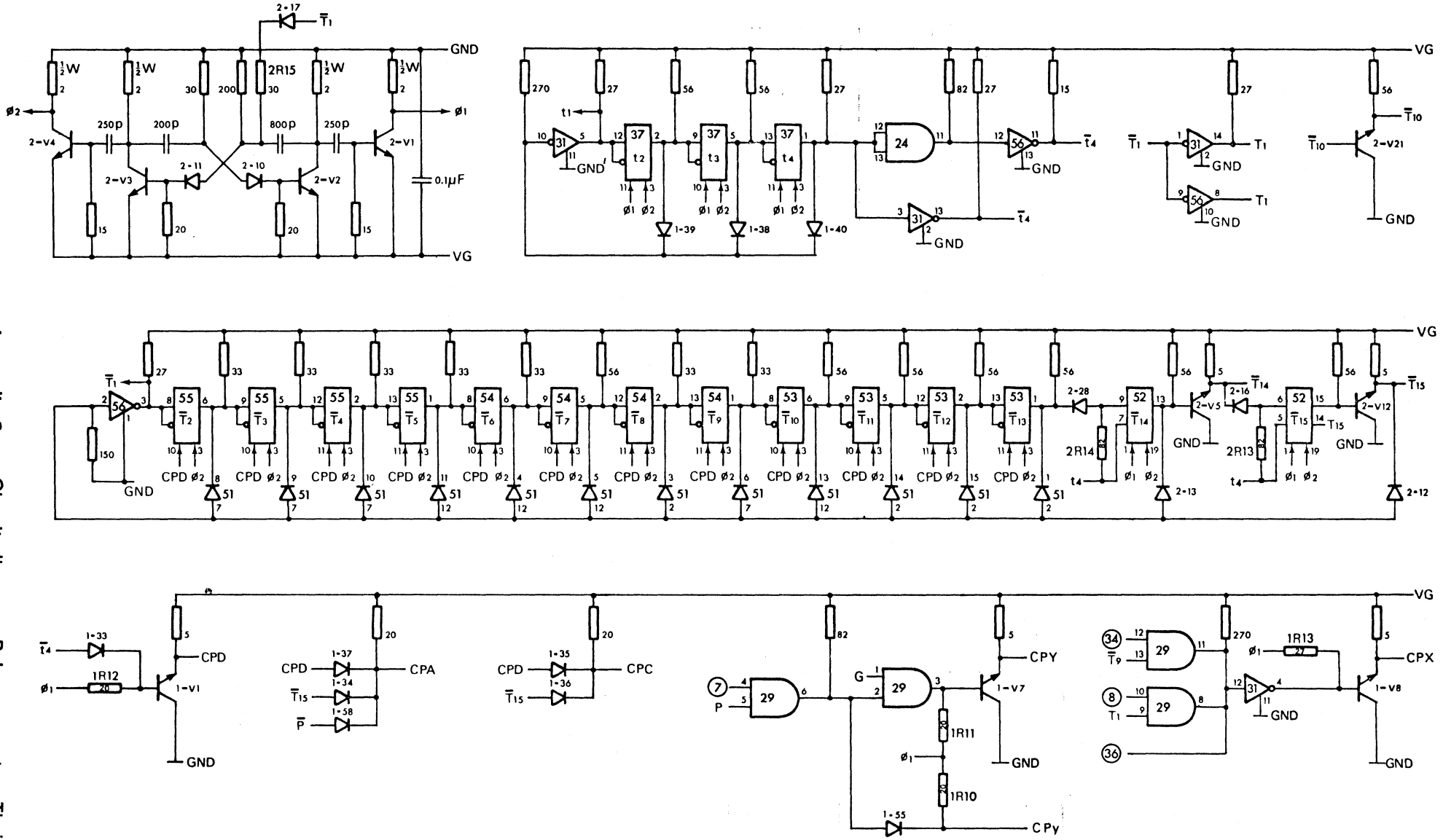
Xs	Ys	SM	S
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Address		ki	Operation	Judgement $\bar{P}t_1$	Error	Set up for next address	next addr.	Instructions J	Er	macro	micro	ki
	$\bar{P}$	0	X→X							8 34	1 5 33 36	0
CL+$\bar{N}_2\bar{N}_3$ = Hs	•key	1				F						1
	11key($\bar{N}_1$+S)	2	0→X $\bar{X}s$			$N_1\bar{S}$				12	36	2
	11key $\bar{N}_1(\bar{I}_1+I_2)$	3	xX→yY							3	6 36	3
	10key $N_1\bar{S}$	4	Xleft	[TAB=x]	X14≠0 x≥8			28	28	8 34	1 5 33	4
	F	5	x+1→x								16	5
	+key	6				I_3						6
	×key	7				$I_1I_2\bar{I}_3N_1\bar{F}\bar{S}$						7
	N_1I_2	8	[mult]			N_2	n2					8
	I_3	9	[div]			N_1S	n3					9
	−key	10	SM								SM	10
	I_1+I_2	11	Xs invert								37	11
	=key	12				$\bar{N}_1\bar{I}_2\bar{F}\bar{S}$						12
	$\bar{I}_1\bar{I}_2$	13				N_3	n4					13
	$\bar{N}_1\bar{M}F_1K$	14	xX↔yY [rep. add or sub]							3 12 13	1 6 36	14
	$I_2\bar{N}_1$	15	xX→xX;yY [square]		I_3	N_2	n2		31	3	1 6 18 36	15
	$I_1\bar{I}_2$	16	[constant mult]			N_2	n2					16
	I_3	17	[constant div]			S						17
	K-reset	18				$\bar{I}_1$						18
	RV	19	xX↔yY			$N_1S\bar{F}$						19
	CE	20	0→xX $\bar{X}s$			$\bar{F}$ G				12	36	20
	C	21	0→xX; 0→yY $\bar{X}s$			(Ar) $\bar{E}r$ $\bar{I}_1$				12	6 36	21
	ACL	22	0→M								10 39	22
	+I	23				MF_1						23
	−I	24	SM			SM					SM	24
		25										25
		26										26
	RCI	27	M→M;X X→Y			S $\bar{F}$					1 14	27
		28										28
	CI	29	0→M								10	29
	All reset (Ar.)	30				$\bar{N}_1\bar{N}_2\bar{N}_3\bar{I}_2\bar{F}\bar{S}$						30
$\bar{CL}$ (N_2+N_3=$\bar{H}s$	n4 J	31	Xright x−1→x	TAB→$\bar{J}$				23 29		8	1 5 16 33	31
	n4 $\bar{J}$	32	0→Xc	xD→J				11 23		2	5 9 36	32
	$\bar{K}$	33				$\bar{I}_1$						33
	$\bar{I}_1\bar{I}_2$+F	34				N_2	n6					34
	$\bar{F}\cdot MF_1\cdot\bar{E}r$	35	YY→M			N_2N_3	n6				4 6 10 21	35
	$(I_1+I_2)\cdot\bar{F}$	36	Ys→Xs invert [R:X1+1→X1]			$\bar{N}_3$	n0				26	36
	n6 $\bar{J}$	37	Xleft x+1→x	TAB=x	X14≠0 x≥8			28	28	8 34	1 5 16 33	37
	n6 $\bar{F}$J	38	xX↔yY $\bar{X}s\oplus Ys\oplus SM\rightarrow S$			$\bar{N}_2F$	n4				22	38
	n6 FJ	39	X±Y→X Y→Y		S·T15·Xcin	$\bar{N}_3$	n2	35	15	2 41	5 9 36	39
	n2 FJ	40	0−X→X Y→Y Xs invert					35		2	5 18 36 37	40
	n2 F$\bar{J}$	41		Xi=BC		(Ar)	n0	35				41
	$\bar{K}$	42	0→Y								6	42
	MF_1	43	M→Y→X→M							12 13	1 4 6 10 20 36	43
	n2 $\bar{F}$	44	xX↔yY			N_1	n3					44
	n3 $\bar{J}$	45	Xleft $\bar{F}$: BC→X1	X14≠0		F I_1		24		8 34	1 5 33	45
	n3 J	46	X→Y y±x→x x→y		$[\bar{F}+x_1+\bar{G}S]T15+\bar{T}15\cdot Y_1\cdot\bar{S}\cdot G$	N_3	n7		17			46
	n7	47	X±Y±T1→X [SJ+$\bar{S}\bar{J}$→Add]	Xi=BC		J→$\bar{N}_2$	J→n5	35		2 41	5 9 16 36	47
	n5 F$\bar{J}$	48	Xright Y_{BC}right	Y1≠0		N_2	n7	27		8	1 5	48
	S	49	Xleft							8 34	1 5 33	49
	n5 FJ	50	Xright			$\bar{F}$				8	1 5	50
	S	51	Xleft			N_2	n7			8 34	1 5 33	51
	n5 F$\bar{J}$	52	X left x+1→x	[Yi=BC][Xc≠0]+x=8+$\bar{S}$		N_2	n7	23		8 34	1 5 33 16	52
	n5 F$\bar{J}$	53	CPY stop			$\bar{N}_1\bar{F}\bar{S}$	n4				7	53
	S	54	$\bar{G}$X→x		x≥9				42	8	1 5 33 36	54

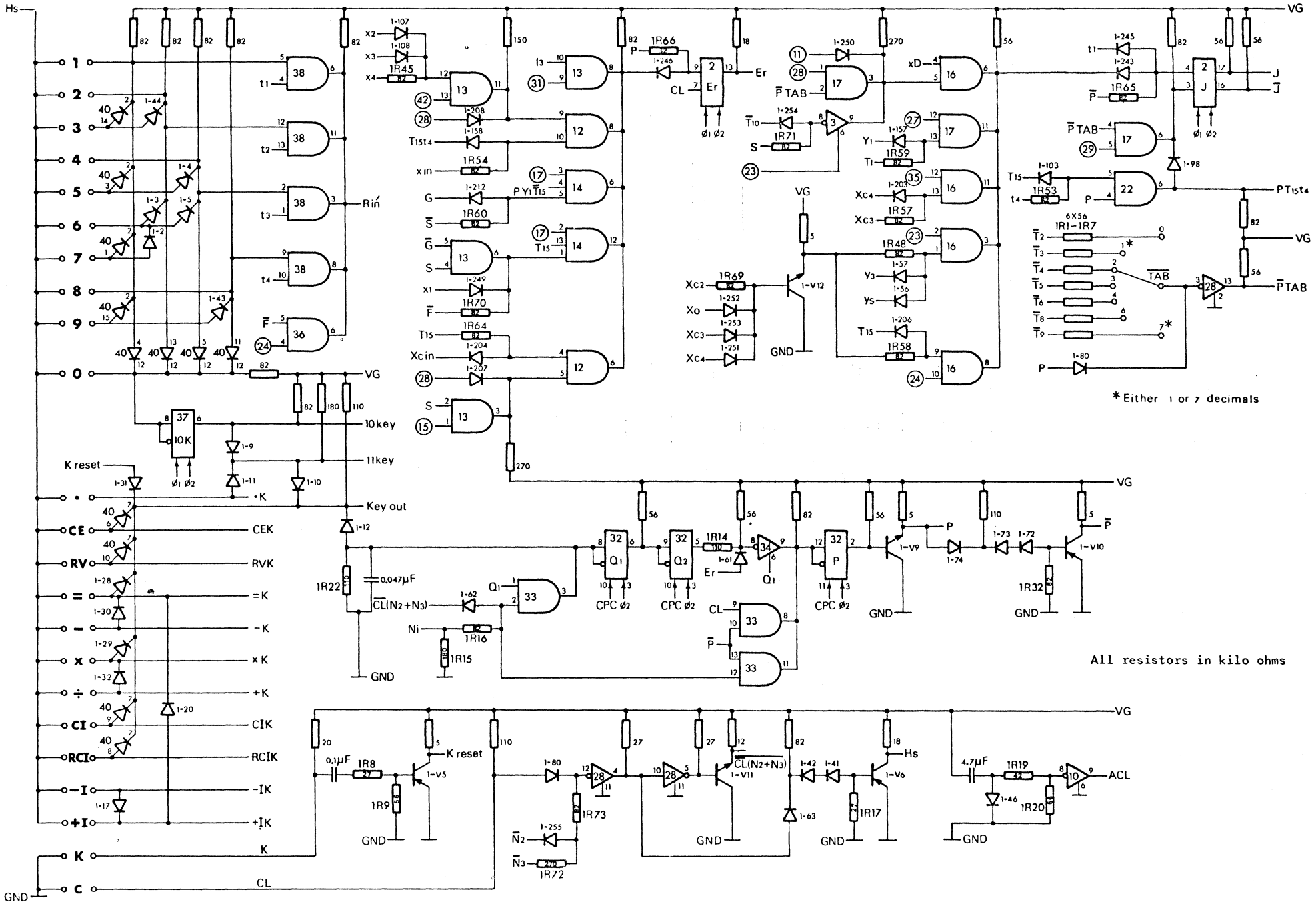
Appendix 1 Operational program chart



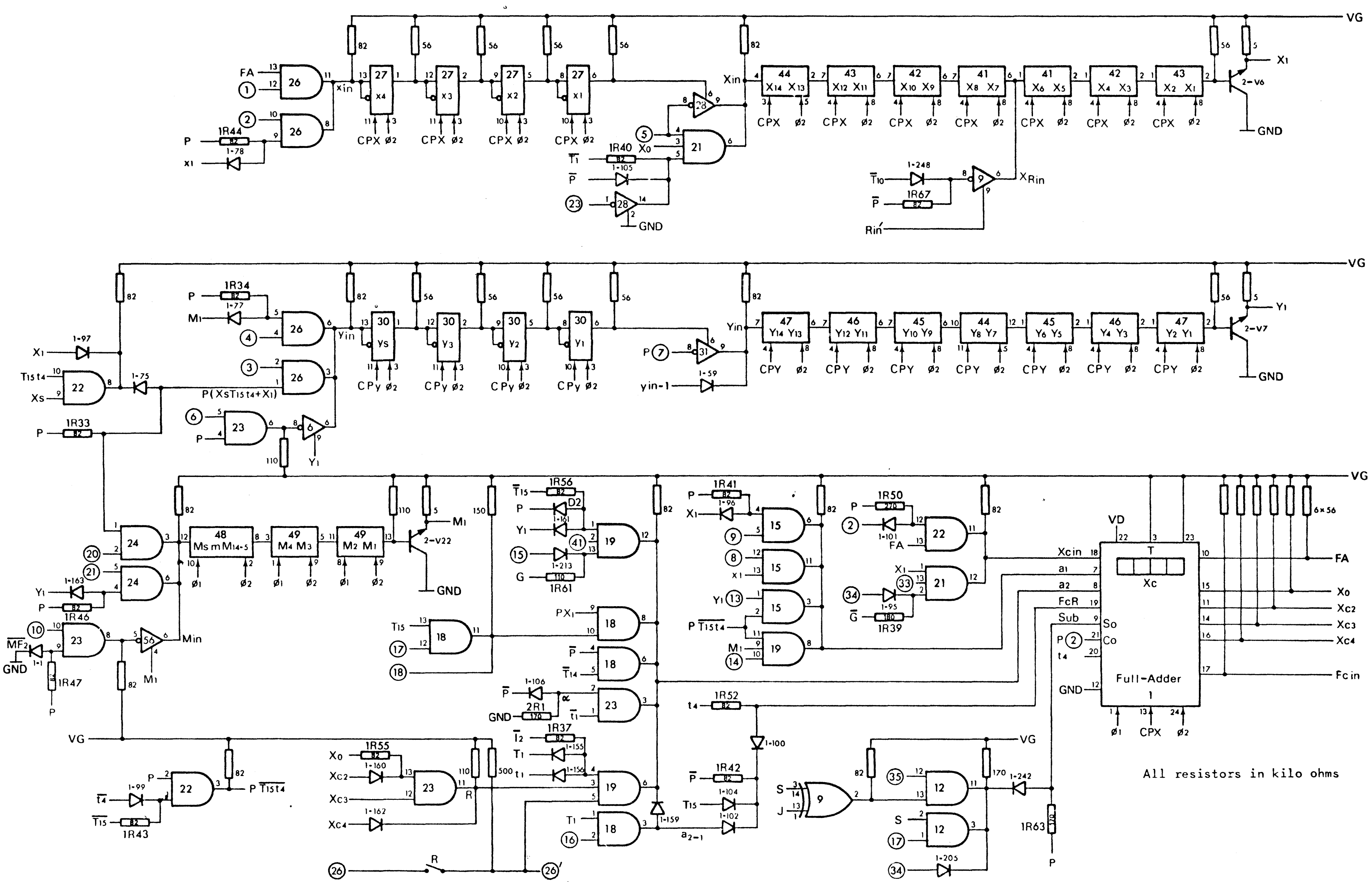
Appendix 2 Block diagram



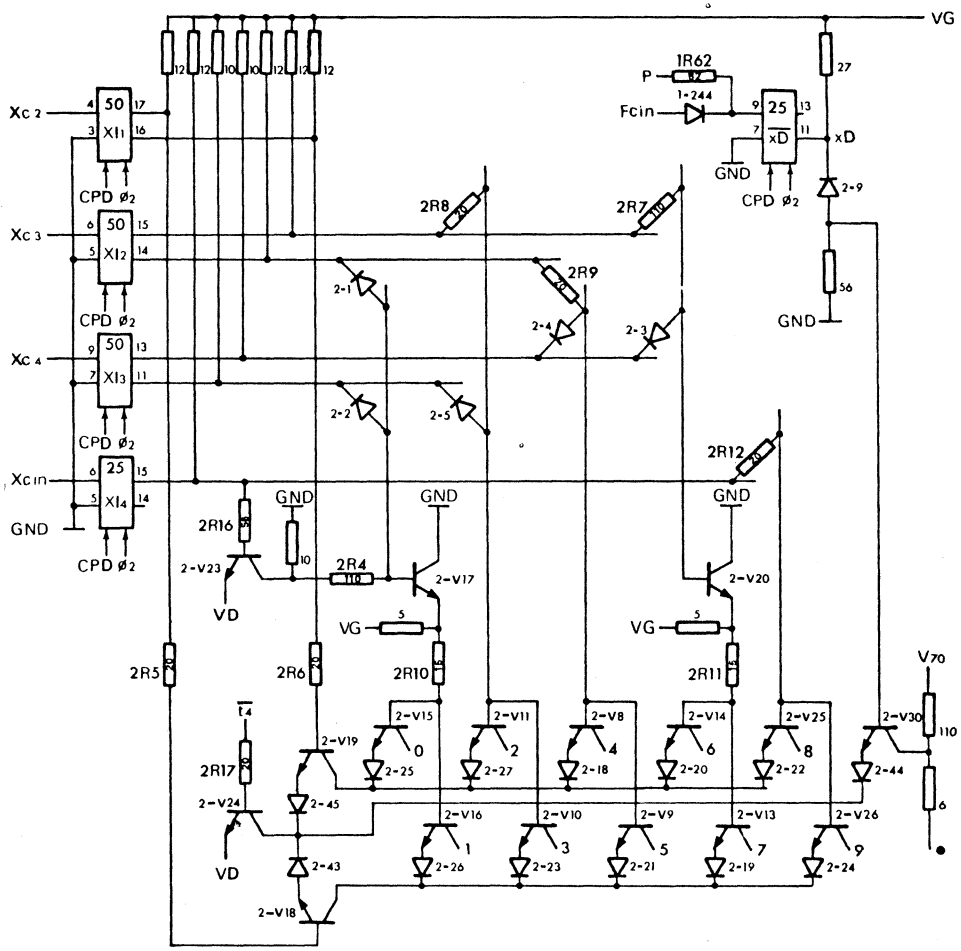
Appendix 3 Circuit diagram: Pulse generator, Timing circuits and Clock pulses

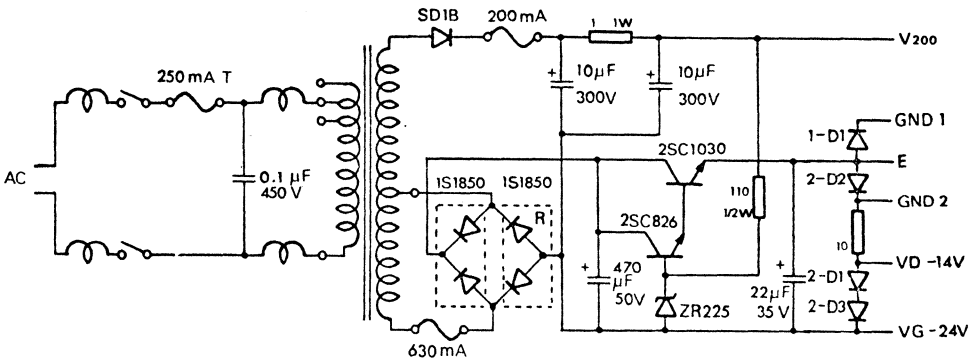


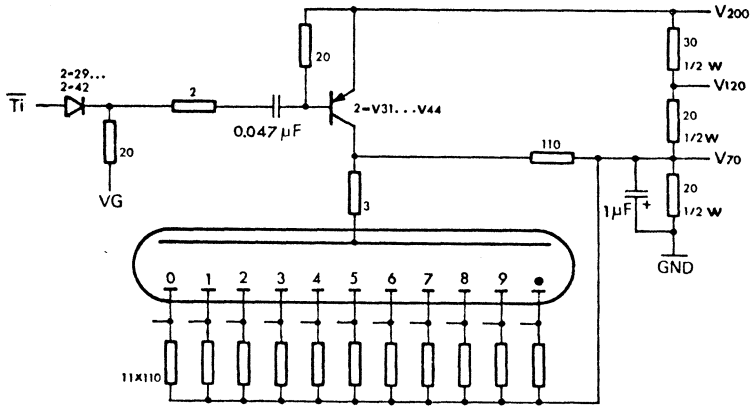
Appendix 4 Circuit diagram: Read-in, P-signal generation
J- and Error flip-flops

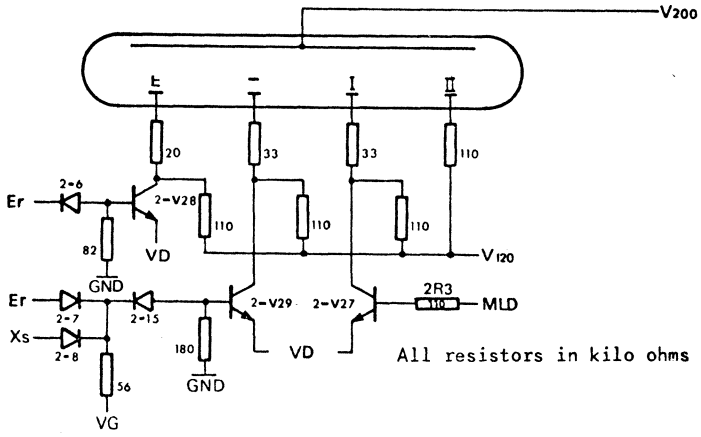


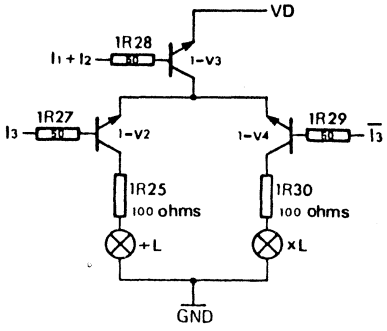
Appendix 5 Circuit diagram: Registers and Full adder



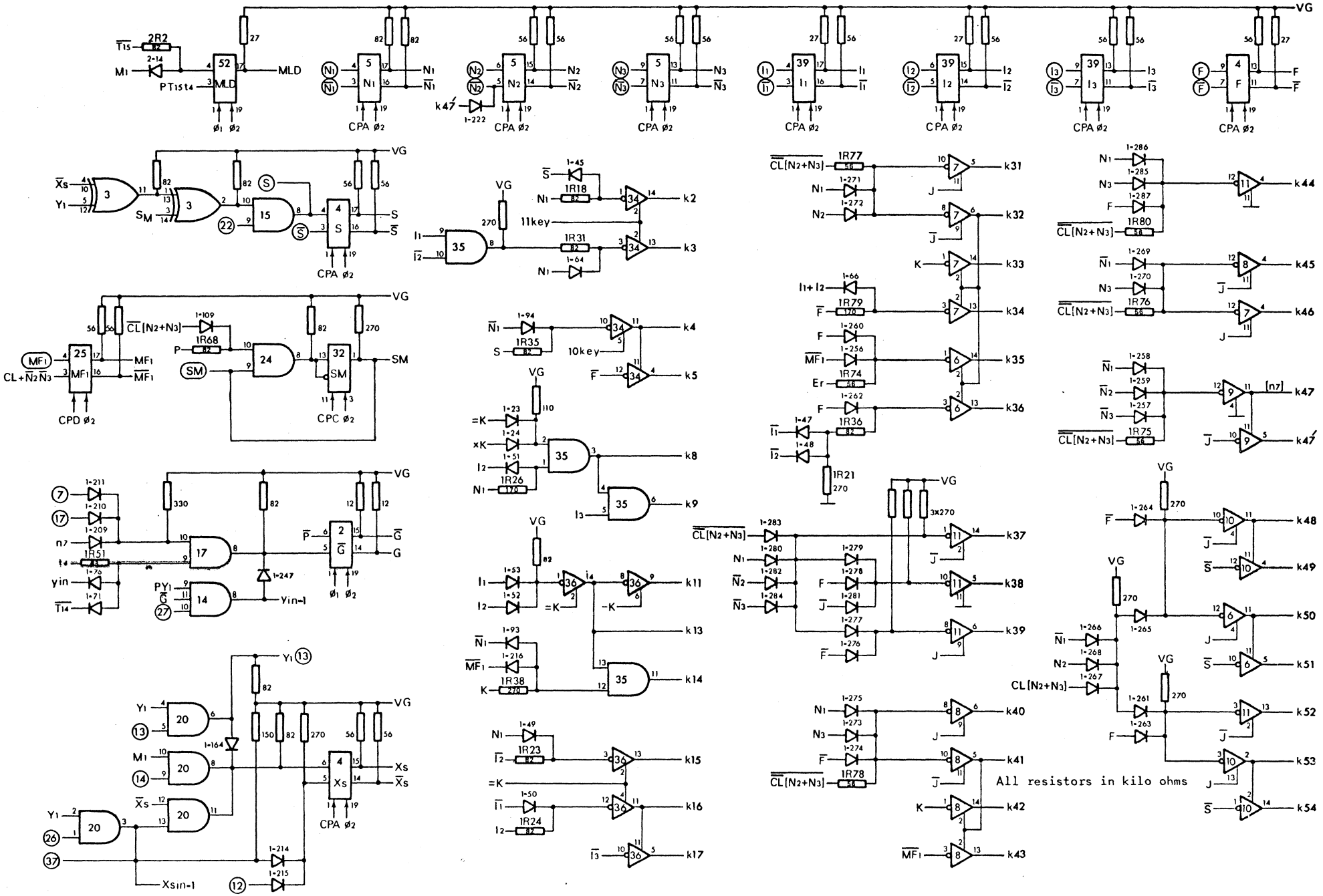




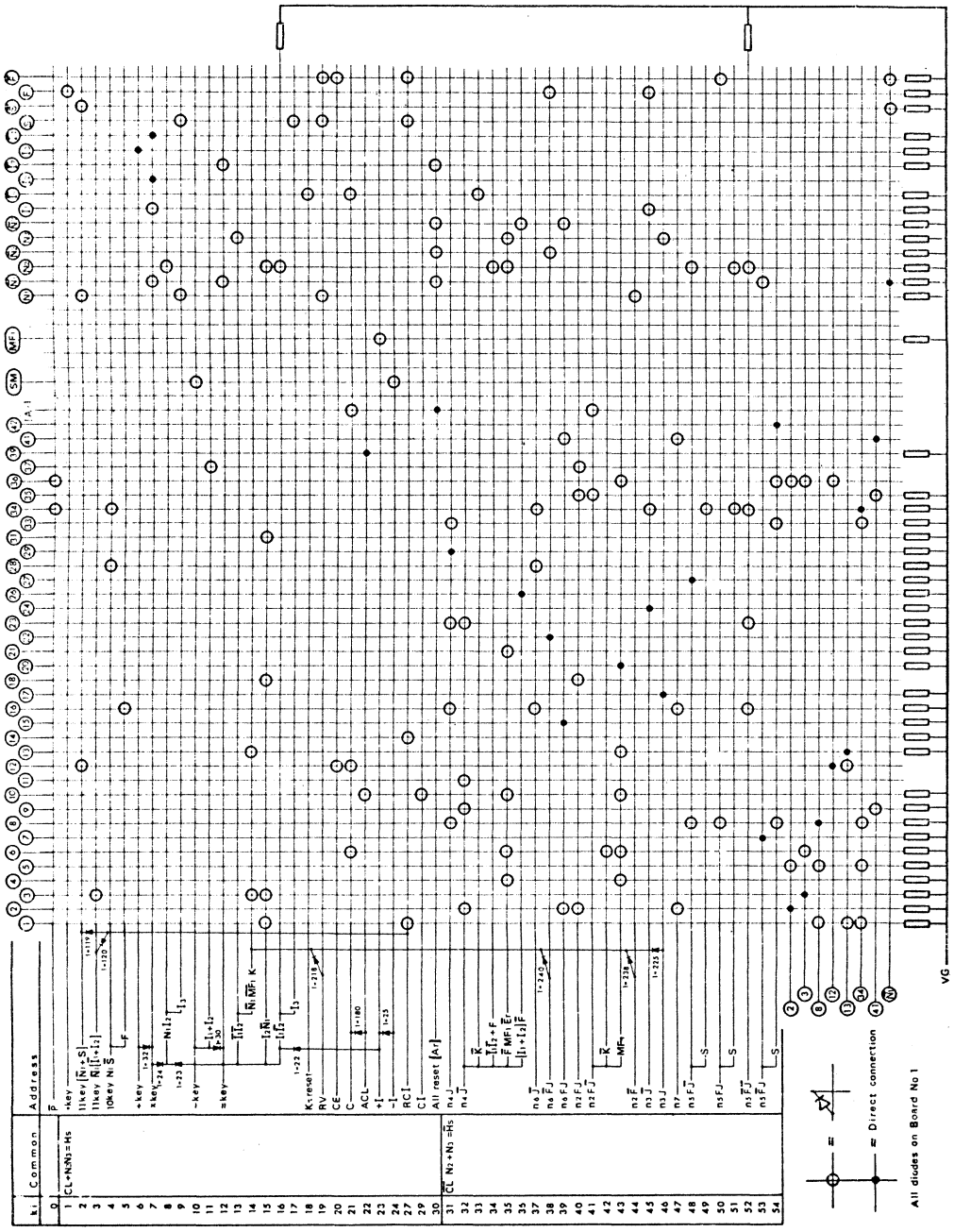




Appendix 6 Circuit diagram: Display circuits and Power supply



Appendix 7 Circuit diagram: Address generation, Address, Sign and S-flip-flops



Microinstructions												Micro/macro instructions		
ki	Diode	Instr	ki	Diode	Instr	ki	Diode	Instr	ki	Diode	Instr	Macro	Diode	Micro
k0	110	34	k19	83	N1	k36	•	26	k47	168	2			
	81	36		82	S		169	$\overline{N3}$		166	16	2	115	5
k1	13	F		217	$\overline{F}$	k37	197	16		165	41		79	36
k2	219	12	k20	229	12		195	28				3	139	6
	84	N1		228	$\overline{F}$		196	34	k48	132	8		135	36
	220	$\overline{S}$	k21	138	6	k38	•	22		•	27			
k3	114	3		231	12		239	$\overline{N2}$		133	N2	8	111	1
k4	171	28		89	$\overline{I1}$		241	F					112	5
	129	34		141	(Ar)	k39	186	2	k49	131	34			
k5	172	16	k22	178	10		•	15	k50	113	8	12	140	36
				•	39		183	41						
k6	•	I3	k23	23	MF1		202	$\overline{N3}$		221	$\overline{F}$	13	122	1
k7	152	$\overline{N1}$	k24	27	SM	k40	189	2	k51	117	34		226	12
	54	I1	k27	137	1		190	18		123	N2	34	125	1
	•	I2		•	14		184	35					130	5
	•	$\overline{I3}$		136	S		192	37	k52	201	16		126	8
k8	65	N2		227	$\overline{F}$	k41	182	35		237	23		167	33
k9	91	N1	k29	8	10		187	(Ar)		200	34			
	92	S	k31	134	8	k42	194	6		153	N2	41	174	9
k10	70	SM		175	16	k43	142	4	k53	•	7		173	35
k11	198	37		176	23		143	6		88	$\overline{N1}$	N1	223	$\overline{S}$
k12	67	$\overline{N1}$		•	29		188	10	k54	128	8		224	$\overline{F}$
	68	$\overline{I2}$		177	33		193	13		170	33	(Ar)	233	$\overline{N1}$
k13	147	N3	k32	181	2		•	20		87	36		234	$\overline{N2}$
k14	151	3		179	9		145	36		•	42		191	$\overline{N3}$
	236	13		250	11								144	$\overline{I2}$
k15	146	1		230	23	k44	199	N1						
	148	3	k33	86	$\overline{I1}$	k45	•	24						
	235	18	k34	288	N2		185	34						
	•	31	k35	121	4		90	I1						
	150	N2		116	6		232	F						
k16	94	N2		118	10	k46	•	17						
k17	69	S		•	21		127	N3						
k18	26	$\overline{I1}$		124	N2									
				85	N3									

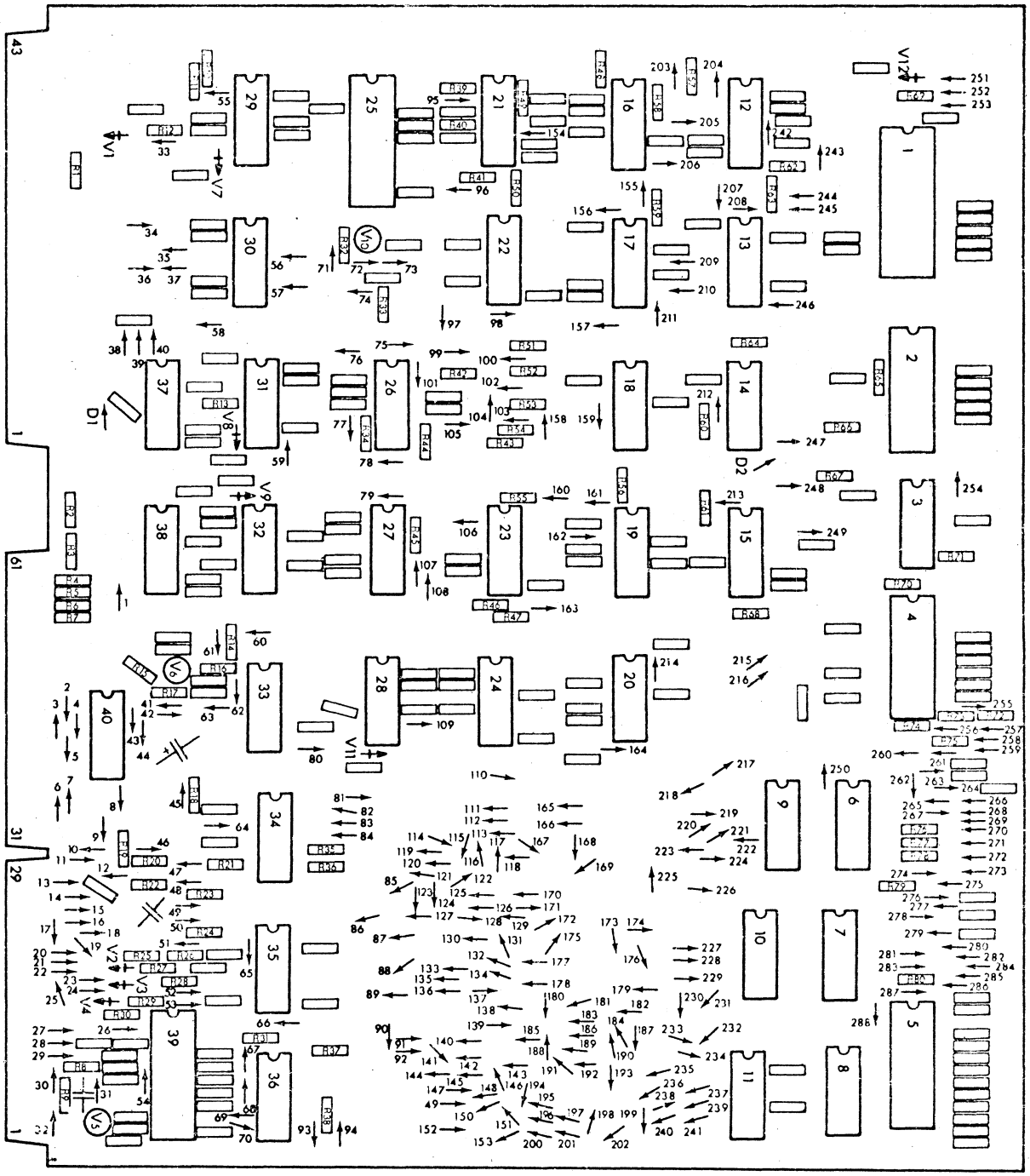
• Indicates direct connection

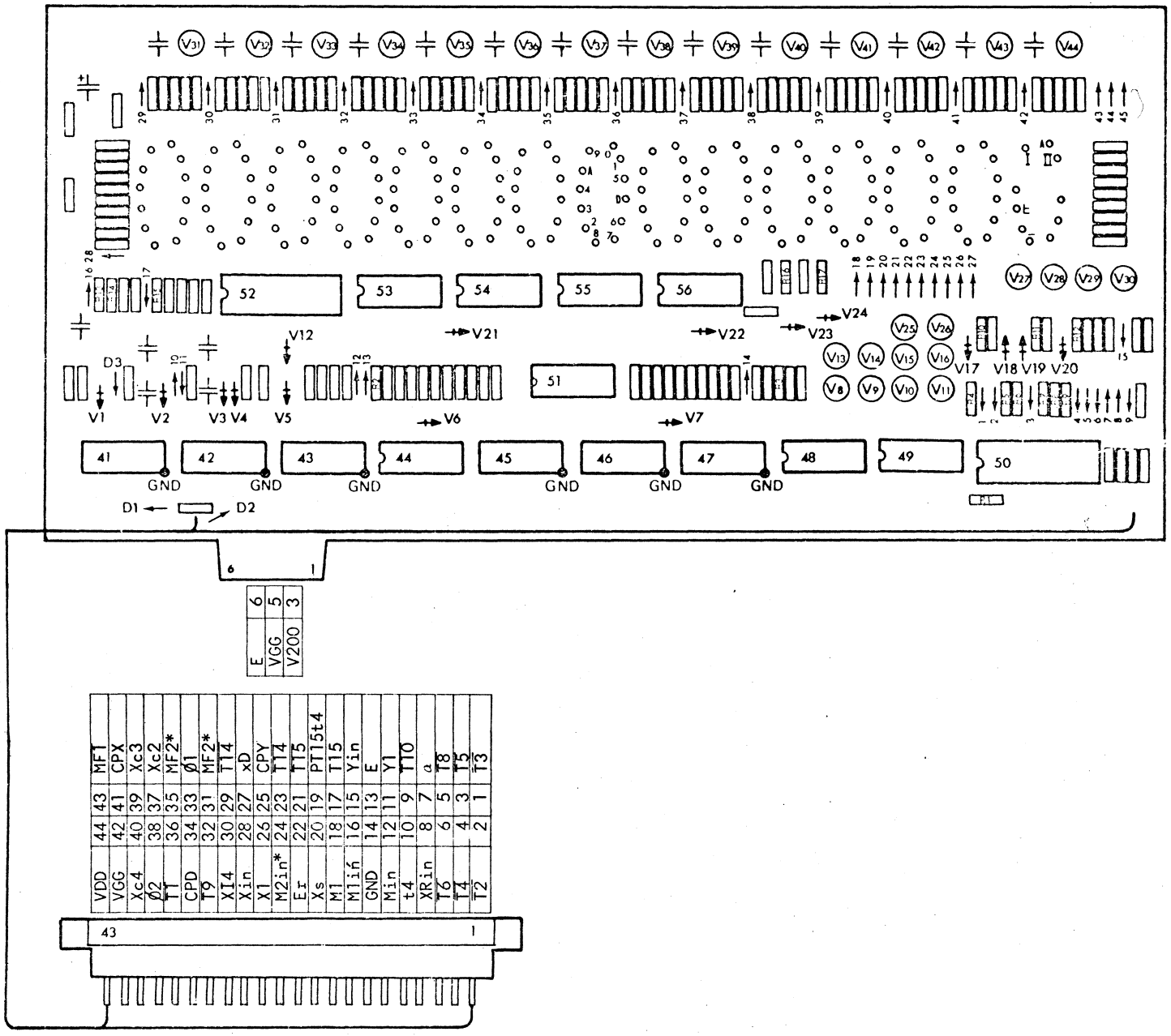
*Signal not used in this calculator

VDD	44	43	MFT
VGG	42	41	CPX
Xc4	40	39	Xc3
Ø2	38	37	Xc2
T1	36	35	MF2*
CPD	34	33	Ø1
T9	32	31	MF2*
XI4	30	29	T14
Xin	28	27	xD
X1	26	25	CPY
M2in*	24	23	T14
Er	22	21	T15
Xs	20	19	PT15t4
M1	18	17	T15
M1in	16	15	Yin
GND	14	13	E
Min	12	11	Y1
t4	10	9	T10
XRin	8	7	a
T6	6	5	T8
T4	4	3	T5
T2	2	1	T3

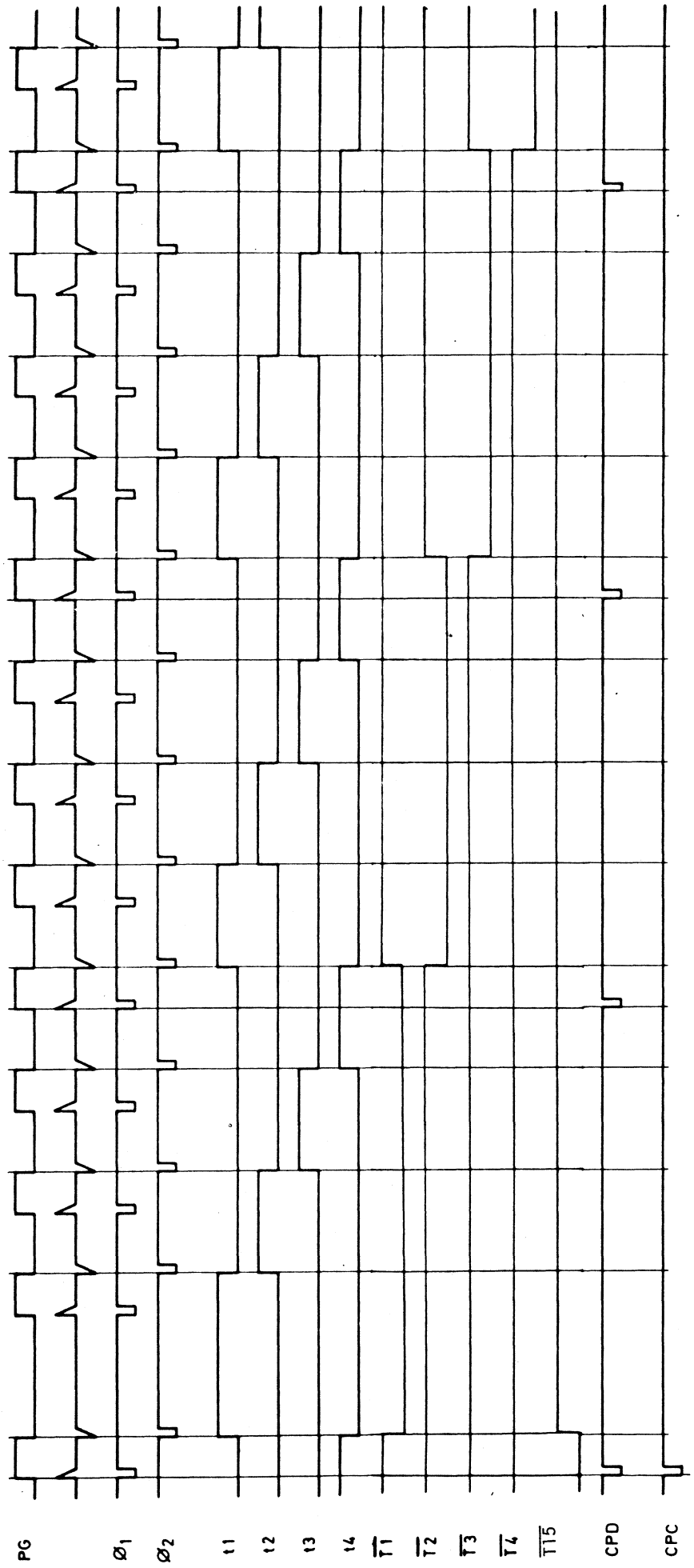
T2	62	61	T3
T4	60	59	T5
T6	58	57	T8
Xs	56	55	P
Er	54	53	Tab
X1	52	51	Ni
T9	50	49	Hs
Ø1	48	47	xD
K7	46	45	K9
K1	44	43	K3
K5	42	41	K2
K6	40	39	K0
K4	38	37	K8
CE	36	35	RVK
RCIK	34	33	CIK
26'	32	31	26

	30	29	
·K	28	27	CL
	26	25	Key out
	24	23	
	22	21	
+IK	20	19	
	18	17	+L
-IK	16	15	xL
VGG	14	13	VGG
	12	11	Ø2
-K	10	9	=K
	8	7	
xK	6	5	
+K	4	3	K
GND	2	1	GND





*Signal not used in this calculator



Appendix 11 Timing chart

Operation	Address	REGISTERS X-reg Xs	x	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Xc	REGISTERS Y-reg Ys	y	14	13	12	11	10	9	8	7	6	5	4	3	2	1	M-reg Ms	m	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Conditions for next address	Next address
ACL	k22,21,30	0	0														0		0	0														0	0																0		
1	k2,3																1		0	0														0																		N1	
·	k1																1																																			N1,F	
2	k4,5		1													1	2																																				
=	k12,13		1													1	2																																			N3	n4
n4,J̄	k32,33,34		1													1	2	0																																	N2,N3	n6
n6.J̄	k37		2												1	2																																			n6.J
n6.F̄.J	k38		0														0			2													1	2																	N3,F,S	n4
n4.J̄.S	k32,33,34		0														0	0		2													1	2																	N2,N3,F,S	n6
n6.J̄,S	k37		1													0				2													1	2																		
n6.J̄.S	k37		2												0					2													1	2																		n6.J
n6.F.J.S ADD	k39		2												1	2				2													1	2																	N2,F,S	n2
n2.F.J̄.S	k41,42		2												1	2				0															0																	n0
3	k2,3		0														3			2													1	2																	N1	
·	k1		0														3			2													1	2																	N1,F	
4	k4,5		1													3	4			2													1	2																		
5	k4,5		2												3	4	5			2													1	2																		
=	k12,13		2												3	4	5			2													1	2																	N3	n4
n4.J̄	k32,33,34		2												3	4	5	0		2													1	2																	N2,N3	n6.J
n6.F̄.J	k38		2												1	2				2													3	4	5																N3,F,S	n4
n4.J̄.S	k32,33,34		2												1	2		0		2													3	4	5																N2,N3,F,S	n6
n6.F.J.S ADD	k39		2												4	6	5			2													3	4	5																N2,F,S	n2
n2.F.J̄.S	k41,42		2												4	6	5			0															0																	n0
6	k2,3																6			2													4	6	5																N1	
·	k1																6			2													4	6	5																N1,F	
7	k4,5		1													6	7			2													4	6	5																	
8	k4,5		2												6	7	8			2													4	6	5																	
9	k4,5		3											6	7	8	9			2													4	6	5																	
-	k10,12,13		3											6	7	8	9			2													4	6	5																N3,SM	n4
n4.J	k31		2												6	7	8	9		2													4	6	5																	
n4.J̄	k32,33,34		2												6	7	8	0		2													4	6	5																N2,N3,SM	n6.J
n6.F̄.J	k38		2												4	6	5			2													6	7	8																N3,F,SM	n4
n4.J̄	k32,33,34		2												4	6	5	0		2													6	7	8																N2,N3,F,SM	n6
n6.F.J SUB	k39		2	9	9	9	9	9	9	9	9	9	9	7	8	7	*		2													6	7	8																N2,F,SM	n2.J
n2.F.J	k40	1	2											2	1	3	0		2													6	7	8																	
n2.F.J̄	k41,42	1	2											2	1	3			0															0																	n0

Appendix 12 Calculation example: Addition and subtraction

1.2 = 3.45 = 6.789 -

TAB=2

Appendix 13 Calculation example: Multiplication 1.2 [×] 3.45 [=]

TAB=2

Operation	Address	Xs	x	X-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Xc	Ys	y	Y-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ms	m	M-reg 14–1	Conditions for next address	Next address
[1]	k2,3																1																					N1	
[·]	k1																1																					N1,F	
[2]	k4,5		1													1	2																						
[×]	k7		1													1	2																					I1,I2	
[3]	k2,3																3			1													1	2				N1,I1,I2	
[·]	k1																3			1													1	2				N1,I1,I2,F	
[4]	k4,5		1													3	4			1													1	2					
[5]	k4,5		2												3	4	5			1													1	2					
[=]	k12,8		2												3	4	5			1													1	2				N2,I1	n2
n2.F̄	k44,14		1													1	2			2												3	4	5				N1,N2,I1	n3
n3.J̄	k45		1												1	2	*			2												3	4	5				N1,N2,F,I1.	
			1											1	2	*				2												3	4	5					
			1										1	2	*					2												3	4	5					
			1									1	2	*						2												3	4	5					
			1								1	2	*							2												3	4	5					
			1							1	2	*								2												3	4	5					
			1						1	2	*									2												3	4	5					
			1					1	2	*										2												3	4	5					
			1				1	2	*											2												3	4	5					
			1			1	2	*												2												3	4	5					
			1		1	2	*													2												3	4	5					
			1	1	2	*														2												3	4	5					n3.J
n3.J	k46,14		3												3	4	5			1	1	2	*															N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2										3	4	4			1	1	2	*																
			3	2	4										3	4	3			1	1	2	*																
n7	k47		3	3	6										3	4	2			1	1	2	*																
			3	4	8										3	4	1																						
			3	6	0										3	4	0																						
			3	7	2										3	4	*																					N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3	6	0										3	4	0																					N1,N3,F,I1	n5
n5.F.J̄	k48		3		6	0										3	4	0		1	1	2	*	1														N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	8	0										3	3																						
			3	3	0	0										3	2																						
			3	4	2	0										3	1																						
			3	5	4	0										3	0																						
			3	6	6	0										3	*																					N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3	5	4	0										3	0																					N1,N3,F,I1	n5
n5.F.J̄	k48		3		5	4	0										3	0		1	1	2	*	:	1													N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	7	4	0										2																						
			3	2	9	4	0										1																						

Operation	Address	REGISTERS: Xs	x	X-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Xc	Ys	y	Y-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ms	m	M-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Conditions for next address	Next address
			3	4	1	4	0										0																																		
			3	5	3	4	0										*																																		N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3	4	1	4	0										0																																		N1,N3,F,I	n5
n5.F.J̄	k48		3		4	1	4	0										0		1	1	2	*	1	1	1																								N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	6	1	4	0									*																																		N1,N2,N3,F,I1,	n7.J
n7 SUB	k47		3		4	1	4	0									0																																		N1,N3,F,I1	n5
n5.F.J̄	k48		3			4	1	4	0									0		1	1	2	*	1	1	1	1																								N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2	4	1	4	0								*																																		N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3			4	1	4	0								0																																		N1,N3,F,I1	n5
n5.F.J̄			3				4	1	4	0								0		1	1	2	*	1	1	1	1	1																							N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2		4	1	4	0							*																																		N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3				4	1	4	0							0																																		N1,N3,F,I1	n5
n5.F.J̄	k48		3					4	1	4	0							0		1	1	2	*	1	1	1	1	1	1																						N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2			4	1	4	0						*																																		N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3					4	1	4	0						0																																		N1,N3,F,I1	n5
n5.F.J̄	k48		3						4	1	4	0						0		1	1	2	*	1	1	1	1	1	1	1																				N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2				4	1	4	0					*																																		N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3						4	1	4	0					0																																		N1,N3,F,I1	n5
n5.F.J̄	k48		3							4	1	4	0					0		1	1	2	*	1	1	1	1	1	1	1	1																		N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2					4	1	4	0				*																																	N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3							4	1	4	0				0																																	N1,N3,F,I1	n5
n5.F.J̄	k48		3								4	1	4	0				0		1	1	2	*	1	1	1	1	1	1	1	1	1																N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2						4	1	4	0			*																																N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3								4	1	4	0			0																																N1,N3,F,I1	n5
n5.F.J̄	k48		3									4	1	4	0			0		1	1	2	*	1	1	1	1	1	1	1	1	1	1														N1,N2,N3,F,I1	n7
n7 ADD	k47		3	1	2							4	1	4	0	*																															N1,N2,N3,F,I1	n7.J
n7 SUB	k47		3									4	1	4	0	0																															N1,N3,F,I1	n5
n5.F.J	k50		3										4	1	4	0		0		1	1	2	*	1	1	1	1	1	1	1	1	1	1														N1,N3,I1	
n5.F̄.J CPY STOP	k53		3										4	1	4	0				1														1	2														N3,I1	n4
n4.J	k31		2											4	1	4		0		1														1	2														N3,I1	
n4.J̄	k32,33,36		2											4	1	4		0		1														1	2															n0

Operation	Address	REGISTERS Xs	x	X-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Xc	Ys	y	Y-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ms	m	M-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Conditions for next address	Next address
1	k2,3	0															1		0	0													0	0	0													0	N1	
·	k1																1																																		N1,F	
2	k4,5		1													1	2																																			
:	k6,7		1													1	2																																		I1,I2,I3	
3	k2,3																3			1													1	2																		N1,I1,I2,I3	
·	k1																3			1													1	2																		N1,F,I1,I2,I3	
4	k4,5		1													3	4			1													1	2																			
5	k4,5		2												3	4	5			1													1	2																			
=	k12,8,9		2												3	4	5			1													1	2																		N1,N2,S,I1,I3	n3
n3.J	k45		2											3	4	5	*			1													1	2																		N1,N2,F,S,I1,I3	n3
			2										3	4	5	*				1													1	2																			
			2									3	4	5	*					1													1	2																			
			2								3	4	5	*						1													1	2																			
			2							3	4	5	*							1													1	2																			
			2						3	4	5	*								1													1	2																			
			2					3	4	5	*									1													1	2																			
			2				3	4	5	*										1													1	2																			
			2			3	4	5	*											1													1	2																			
			2		3	4	5	*												1													1	2																			
n3.J	k45		2	3	4	5	*													1													1	2																		N1,N2,F,S,I1,I3	n3.J
n3.J	k46,14		5													1	2			2	3	4	5	*																										N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5										1	3		*	2	3	4	5	*																										N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5													1	2			2	3	4	5	*																										N1,N3,F,S,I1,I3	n5
n5.J.F	k48,49		5												1	2				2	3	4	5	*	1																										N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5									1	2	1		*	2	3	4	5	*																										N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5												1	2				2	3	4	5	*	1																										N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5											1	2					2	3	4	5	*	1	1																										N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5								1	2		1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5											1	2																																				N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5										1	2						2	3	4	5	*	1	1	1																										N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5							1	2			1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5										1	2																																				N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5									1	2							2	3	4	5	*	1	1	1	1																								N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5						1	2				1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5									1	2																																				N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5								1	2								2	3	4	5	*	1	1	1	1	1																						N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5					1	2					1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5								1	2																																						N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5							1	2									2	3	4	5	*	1	1	1	1	1	1																					N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5					1	2					1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5								1	2																																						N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5						1	2										2	3	4	5	*	1	1	1	1	1	1																				N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5					1	2					1		*																																N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		5								1	2																																						N1,N3,F,S,I1,I3	n5
n5.F.J	k48,49		5							1	2									2	3	4	5	*	1	1	1	1	1	1																				N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		5	6	5	5					1	2					1		*																																N1,N2,N3,F,S,I1,I3	n7.J

Appendix 14 Calculation example: Division 1.2 + 3,45 =
TAB=2R

Operation	Address	REGISTERS: Xs	x	X-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Xc	Ys	y	Y-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ms	m	M-reg 14	13	12	11	10	9	8	7	6	5	4	3	2	1	Conditions for next address	Next address
n7 ADD	k47		15													1	2																																	N1,N3,F,S,I1,I3	n5
n5.F.$\bar{J}$	k48,49		15												1	2				2	3	4	5	*	1	1	1	1	1	1	1																					N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		15	6	5	5									1	2		*																																	N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		15													1	2																																	N1,N3,F,S,I1,I3	n5
n5.F.$\bar{J}$	k48,49													1	2					2	3	4	5	*	1	1	1	1	1	1	1																					N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		15	6	5	5									1	2		*																																	N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		15													1	2																																	N1,N3,F,S,I1,I3	n5
n5.F.$\bar{J}$	k48,49		15											1	2					2	3	4	5	*	1	1	1	1	1	1	1	1																			N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		15	6	5	5	1	2							1	2		*																																	N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		15				1	2																																										N1,N3,F,S,I1,I3	n5
n5.F.$\bar{J}$	k48,49		15				1	2												2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,F,S,I1,I3	n7
n7 SUB	k47		15	6	5	6	2								1			*																																	N1,N2,N3,F,S,I1,I3	n7.J
n7 ADD	k47		15				1	2																																										N1,N3,F,S,I1,I3	n5
n5.F.J	k50,51		15			1	2													2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		15	6	6	7									1			*																																	N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		15			1	2																																										N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		0	1	2															2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		0	7	7	5									1			*																																	N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		0	1	2																																												N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		1	2														1		2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		1	8	5	5									1																																					
			1	5	1	0									2																																					
			1	1	6	5									3																																					
			1	6	2	0									4			*																																	N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		1	1	6	5									3																																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		2	6	5									3				1		2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		2	3	0	5								3	1			1																																		
			2	9	6	0								3	2			0																																	
			2	6	1	5								3	3			0																																	
			2	2	7	0								3	4			0																																	
			2	9	2	5								3	5			*																																	N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		2	2	7	0								3	4			0																																	N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		3	7									3	4	0			2		2	3	4	5	*	1	1	1	1	1	1	1	1	1																	N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		3	3	5	5								3	4	1		2																																	
			3		1	0								3	4	2		2																																	
			3	6	6	5								3	4	3		1																																	
			3	3	2	0								3	4	4		1																																	
			3	9	7	5								3	4	5		0																																	
			3	6	3	0								3	4	6		0																																	
			3	2	8	5								3	4	7		0																																	

Appendix 14 continued (1)

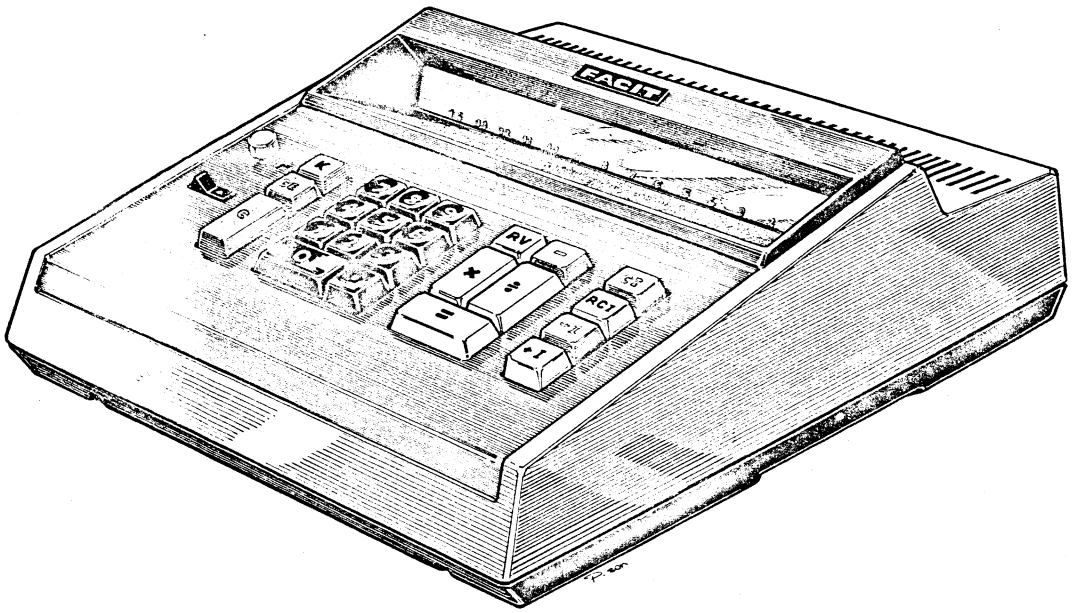
Operation	Address	Xs	x	X-reg 14													1	Xc	Ys	y	Y-reg 14													1	Ms	m	M-reg 14 … 1	Conditions for next address	Next address
			3	9	4	0									3	4	8	*																				N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		3	2	8	5									3	4	7	0																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		4	8	5									3	4	7	0	2		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		4	5	0	5								3	4	7	1	2																					
			4	1	6	0								3	4	7	2	2																					
			4	8	1	5								3	4	7	3	1																					
			4	4	7	0								3	4	7	4	1																					
			4	1	2	5								3	4	7	5	1																					
			4	7	8	0								3	4	7	6	0																					
			4	4	3	5								3	4	7	7	0																					
			4		9	0								3	4	7	8	0																					
			4	7	4	5								3	4	7	9	*																				N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		4		9	0								3	4	7	8	0																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		5	9									3	4	7	8	0	0		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		5	5	5	5							3	4	7	8	1	0																					
			5	2	1	0							3	4	7	8	2	0																					
			5	8	6	5							3	4	7	8	3	*																				N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		5	2	1	0							3	4	7	8	2	0																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		6	1	0							3	4	7	8	2		2		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		6	7	5	5						3	4	7	8	2	1	1																					
			6	4	1							3	4	7	8	2	2	1		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
			6		6	5						3	4	7	8	2	3	1																					
			6	7	2	0						3	4	7	8	2	4	0																					
			6	3	7	5						3	4	7	8	2	5	0																					
			6		3	0						3	4	7	8	2	6	0																					
			6	6	8	5						3	4	7	8	2	7	*																				N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		6		3	0						3	4	7	8	2	6	0																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		7	3							3	4	7	8	2	6	0	0		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		7	9	5	5					3	4	7	8	2	6	1	*																				N1,N2,N3,S,I1,I3	n7.J
n7 ADD	k47		7	3							3	4	7	8	2	6	0	0																				N1,N3,S,I1,I3	n5
n5.$\bar{F}$.$\bar{J}$	k52		8							3	4	7	8	2	6	0	0	3		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1				N1,N2,N3,S,I1,I3	n7
n7 SUB	k47		8	6	5	5				3	4	7	8	2	6	0	1	2																					
			8	3	1	0				3	4	7	8	2	6	0	2	2																					
			8	9	6	5				3	4	7	8	2	6	0	3	1																					
			8	6	2	0				3	4	7	8	2	6	0	4	1																					
			8	2	7	5				3	4	7	8	2	6	0	5	1																					
			8	9	3					3	4	7	8	2	6	0	6	0																					
			8	5	8	5				3	4	7	8	2	6	0	7	0																					
			8	2	4					3	4	7	8	2	6	0	8	0																					
			8	8	9	5				3	4	7	8	2	6	0	9	*																				N1,N2,N3,S,I1,I3	n7.J

Operation	Address	Xs	x	X-reg 14													X-reg 1	Xc	Ys	y	Y-reg 14													Y-reg 1	Ms	m	M-reg 14													M-reg 1	Conditions for next address	Next address
n7 ADD	k47		8	2	4					3	4	7	8	2	6	0	8	0		2	3	4	5	*	1	1	1	1	1	1	1	1	1	1																	N1,N3,S,I1,I3	n5
n5.$\bar{F}$.J CPY STOP	k53,54		8							3	4	7	8	2	6	0	8			2												3	4	5																	N3,I1,I3	n4
n4.J	k31		7								3	4	7	8	2	6	0	8		2												3	4	5																		
n4.J	k31		6									3	4	7	8	2	6	0		2												3	4	5																		
n4.J	k31		5										3	4	7	8	2	6		2												3	4	5																		
n4.J	k31		4											3	4	7	8	2		2												3	4	5																		
n4.J	k31		3												3	4	7	8		2												3	4	5																		
n4.J	k31		2													3	4	7		2												3	4	5																	N3,I1,I3	n4.J
n4.$\bar{J}$	k32,33,36		2													3	5	0		2												3	4	5																	I3	n0

FACIT 1129

Electronic desk calculator

SPARE PARTS LIST



FACIT AB · SWEDEN

1129.05.01 Eng. 0.5 M 02.71

GENERAL

This parts list contains components and sub-units for the Facit 1129 desk calculator. Sub-units and associated parts are grouped together in the parts list. However, every spare part must be specified separately.

Numbers of complete sub-units are shown in boxes 55.33160.55.0

The column headed "Old No." in the price list contains the part designations used in the spare part lists for previous electronic desk calculators.

These designations should be used only for cross-referencing with the new ten-digit part numbers; they are not to be used when ordering spare parts.

When ordering transistors specify the colour code along with the spare part number.

It is important to state model type designation on every spare part order. In order to facilitate and expedite the handling of spare part orders, they shall be issued in duplicate and preferably on special forms. These forms can be obtained free of charge from us on request.

Guarantee Replacement

In conjunction with orders for spare parts covered by guarantee the defective parts shall be returned to Facit-Sweden with the following information:

The service report "Fas 3" must be sent for every defective part. Note that the data of delivery from Japan of the respective calculator must always be stated. It can be taken from the dispatch documents. The defective parts should be attached to the corresponding report or clearly marked to enable the identification.

Guarantee claims for LSI components must be accompanied not only by the service report "Fas 3" (1 copy) but also by the form "QC3" (3 copies) for every defective LSI.

AQL Replacement

Claims for parts, which have been replaced at your arrival inspection by AQL, should be made on the forms "Fas 1" and "Fas 2" in accordance with the rules issued by us.

The above mentioned forms can be obtained from Facit AB, Marketing Management, Technical Service.

Kindly address your orders for spare parts to:

FACIT AB
Marketing Management
Administrative Department
Fack

S-103 80 STOCKHOLM 7
Sweden

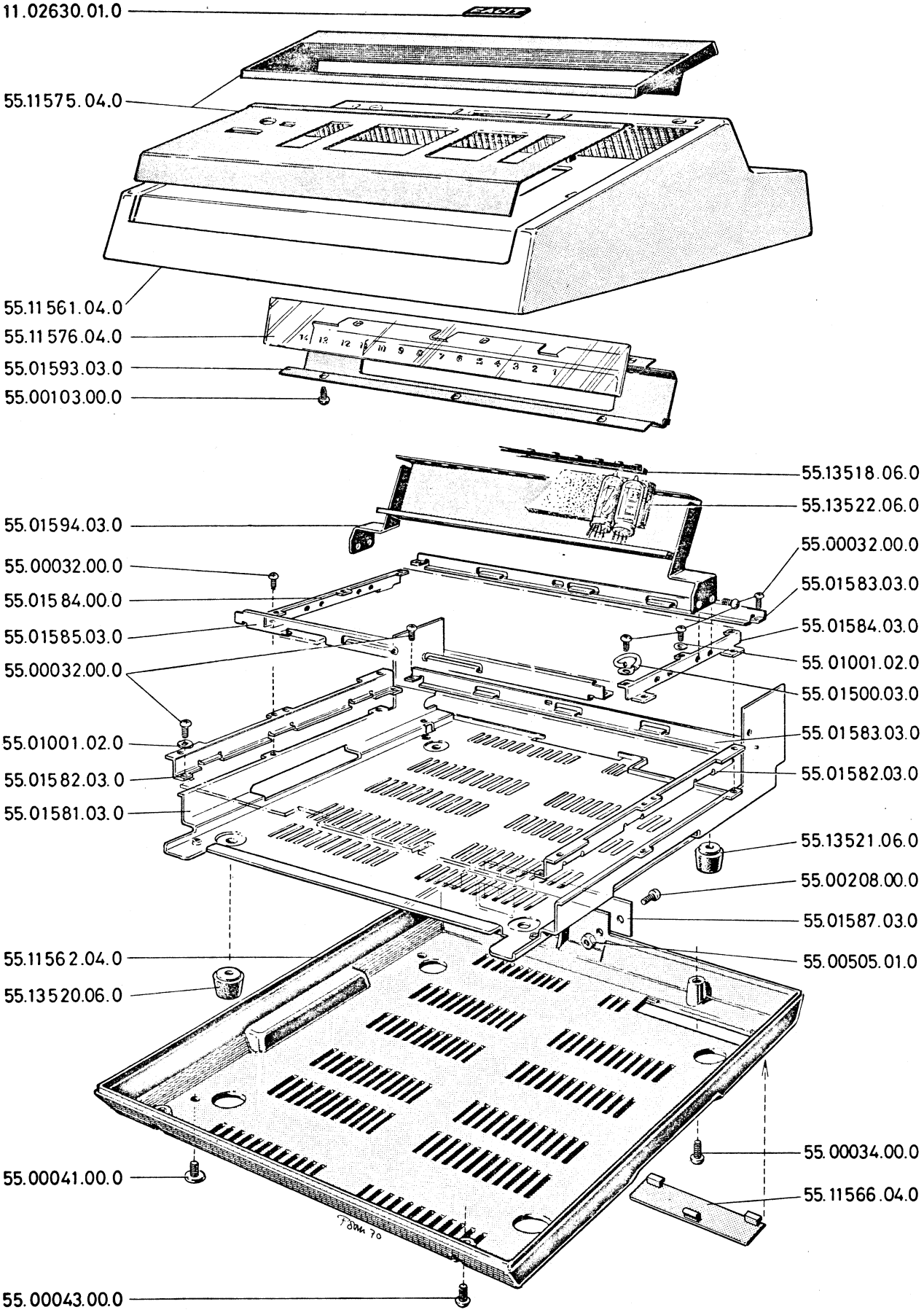
From July 1, 1971, our address is:

FACIT AB
Marketing Management
Administrative Department
Fack

S-597 00 ÅTVIDABERG
Sweden

SECTION II

TABLE OF CONTENTS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55.13522.06.0
55.01594.03.0
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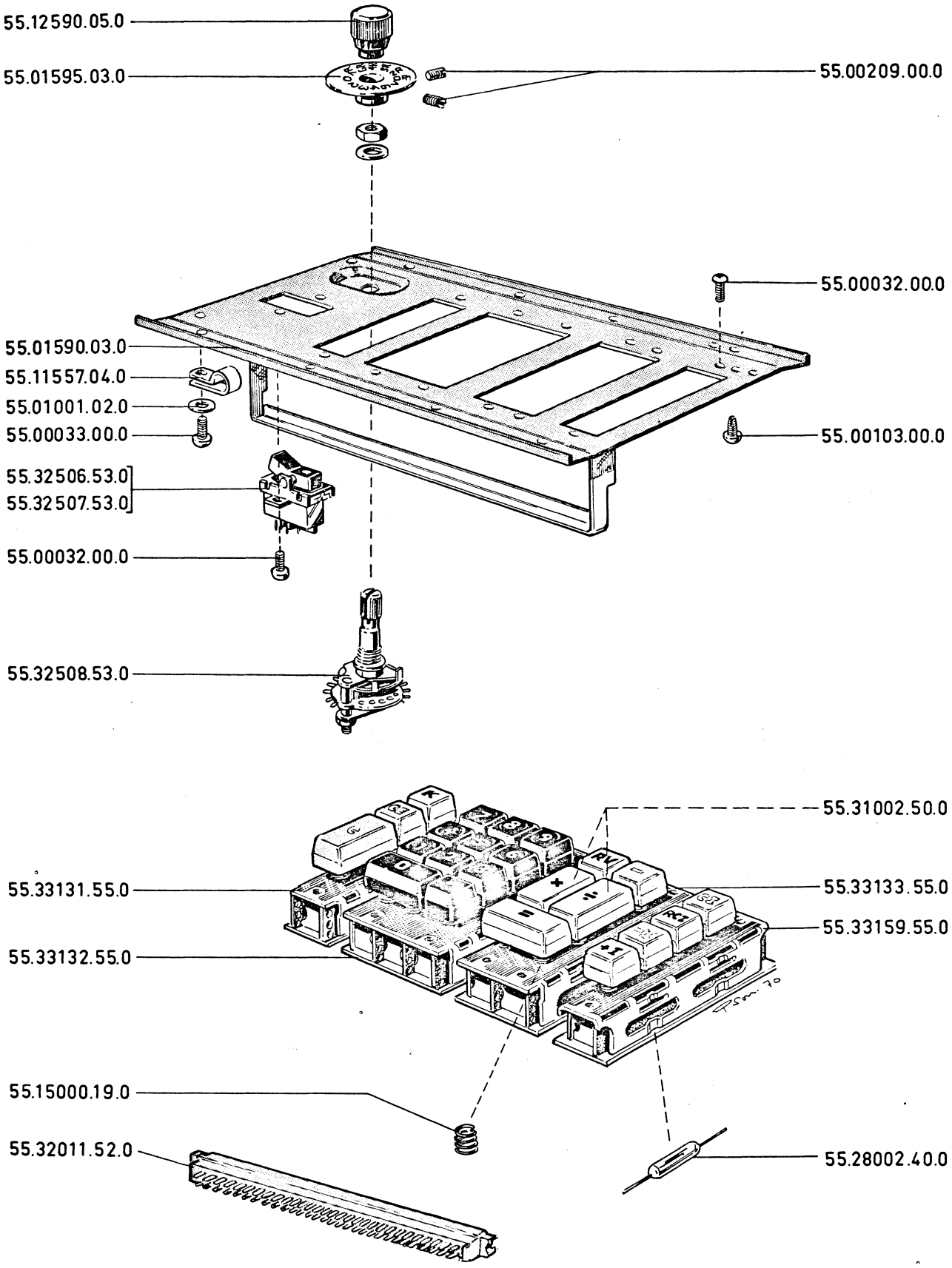
55.01001.02.0
55.01582.03.0
55.01581.03.0
55.11562.04.0
55.13520.06.0
55.00041.00.0
55.00043.00.0
55.00032.00.0
55.01583.03.0
55.01584.03.0
55.01001.02.0
55.01500.03.0
55.01583.03.0
55.01582.03.0
55.13521.06.0
55.00208.00.0
55.01587.03.0
55.00505.01.0
55.00034.00.0
55.11566.04.0

1 CASING AND CHASSIS

Part No.	Description	Qty
55.11561.04.0	Casing top	1
55.00043.00.0	Screw RX 4x8	2
55.00034.00.0	Screw RX 3x10	2
55.11575.04.0	Keyboard panel	1
11.02630.01.0	Facit plate	2
55.11576.04.0	Window	1
55.01593.03.0	Window holder	1
55.00102.00.0	Screw RX 3x1.1x6	6
55.01581.03.0	Chassis	1
55.00041.00.0	Screw RX 4x6	4
55.01582.03.0	Board No. 1 side bracket (left, right)	2
55.01583.03.0	Rear bracket	1
55.00032.00.0	Screw RX 3x6	4
55.01001.02.0	Washer 0.5x3.1x8	2
55.01584.03.0	Board No.2 side bracket (left,right)	2
55.01585.03.0	Board No.2 front bracket	1
55.01583.03.0	Rear bracket	1
55.00032.00.0	Screw RX 3x6	6
55.01001.02.0	Washer 0.5x3.1x8	2
55.01500.03.0	Wire holder	1
55.01594.03.0	Nixie tube holder	1
55.00032.00.0	Screw RX 3x6	4
55.13518.06.0	Rubber protector for indicator tubes	1
55.13522.06.0	Foamed plastic protector for tubes	1
55.11562.04.0	Casing bottom	1
55.13520.06.0	Rubber foot (front)	2
55.13521.06.0	Rubber foot (rear)	2
55.11566.04.0	Cover plate for test connector	1
55.01587.03.0	Rear panel	1
55.00208.00.0	Screw RX 2.5x8	2
55.00505.01.0	Nut	2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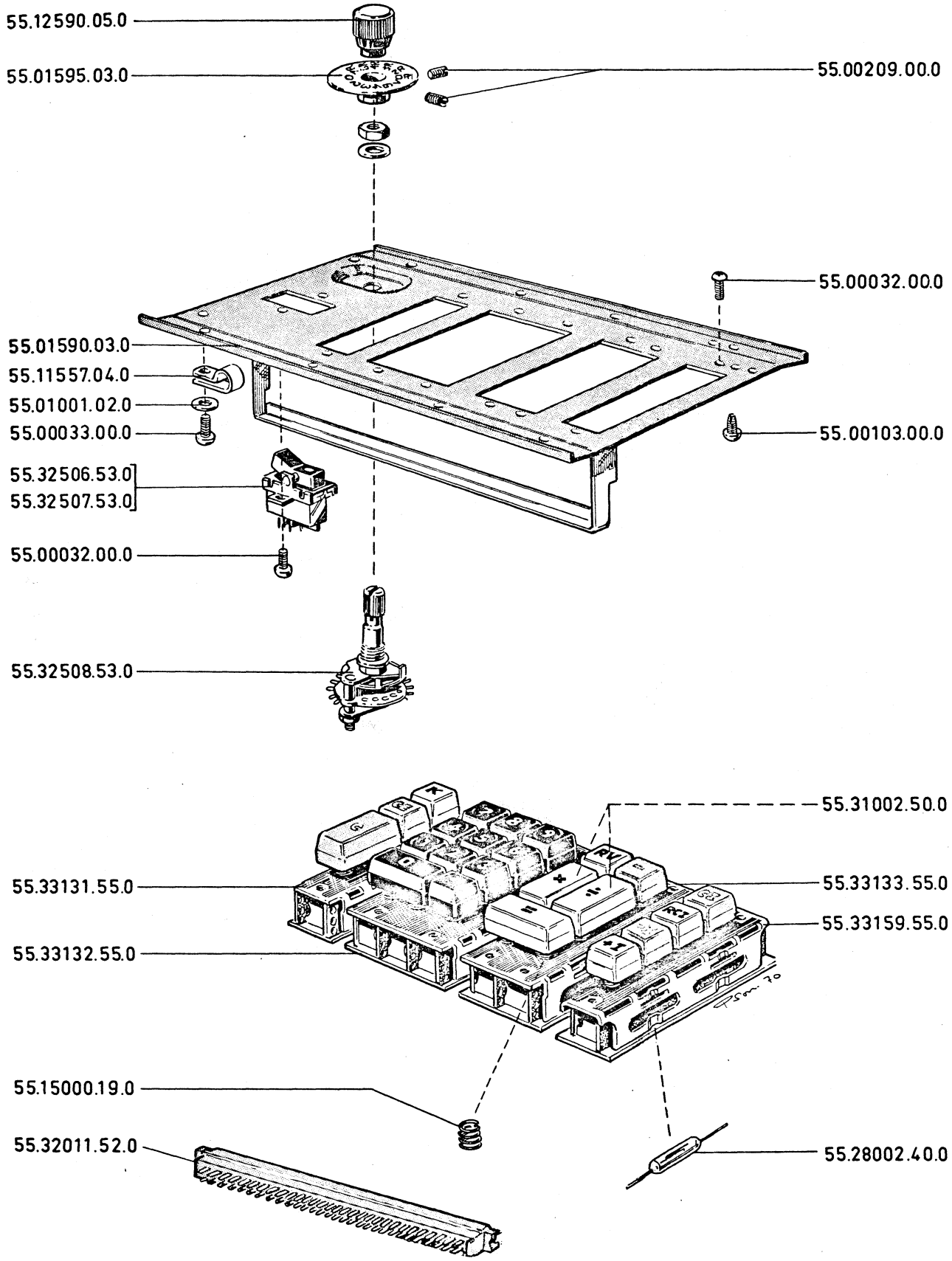
55.32507.53.0
55.00032.00.0
55.32508.53.0
55.31002.50.0
55.33131.55.0
55.33133.55.0
55.33159.55.0
55.33132.55.0
55.15000.19.0
55.32011.52.0
55.28002.40.0

2 KEYBOARD

Part No.	Description	Qty
55.33160.55.0	Keyboard complete	1
55.00103.00.0	Screw RX 3x1.1x8	8
55.32506.53.0	Power switch (SEMKO)	1
55.32507.53.0	Power switch (U.L.,CSA,Japan)	1
55.00032.00.0	Screw RX 3x6	2
55.11557.04.0	Cable clip (plastic)	1
55.00033.00.0	Screw RX 3x8	1
55.01001.02.0	Washer 0.5x3.1x8	1
55.32508.53.0	Rotary switch	1
55.12590.05.0	Rotary switch knob	1
55.01595.03.0	Dial plate	1
55.00209.00.0	Stop screw 3x5	2
55.33131.55.0	Clear and constant key set	1
55.33132.55.0	Figure key set	1
55.33133.55.0	Operation key set	1
55.33159.55.0	Store operation key set	1
55.00032.00.0	Screw RX 3x6	12
55.01590.03.0	Key set holder	1
55.12580.05.0	[K] key top	1
55.12518.05.0	[CE] key top	1
55.12581.05.0	[C] key top	1
55.12520.05.0	[0] key top	1
55.12521.05.0	[1] key top	1
55.12522.05.0	[2] key top	1
55.12523.05.0	[3] key top	1
55.12524.05.0	[4] key top	1
55.12525.05.0	[5] key top	1
55.12526.05.0	[6] key top	1
55.12527.05.0	[7] key top	1
55.12528.05.0	[8] key top	1
55.12529.05.0	[9] key top	1
55.12530.05.0	[·] key top	1
55.12517.05.0	[RV] key top	1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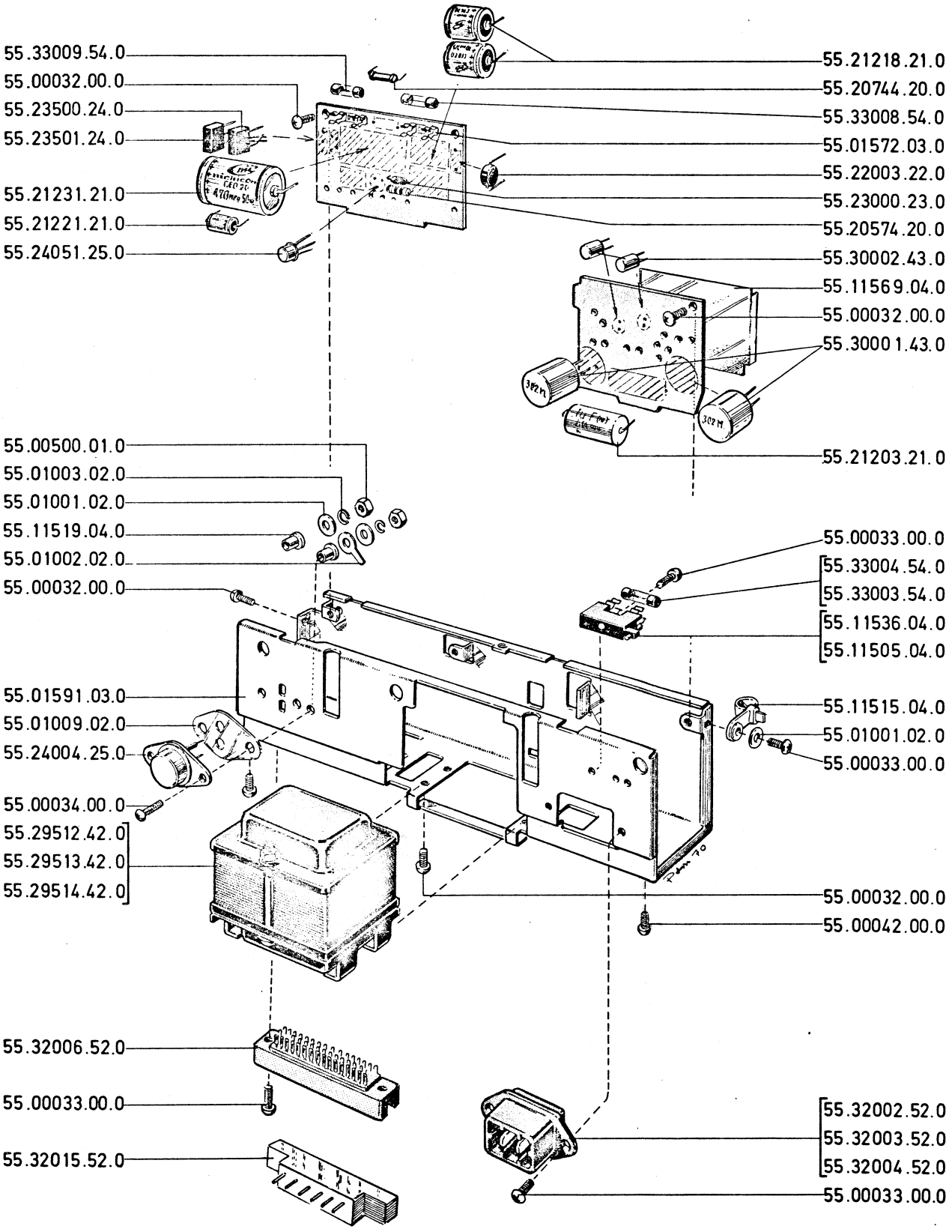
55.33133.55.0
55.33159.55.0
55.33132.55.0
55.15000.19.0
55.32011.52.0
55.28002.40.0

Part No.	Description	Qty
55.12532.05.0	[-] key top	1
55.12533.05.0	[x] key top	1
55.12534.05.0	[+] key top	1
55.12535.05.0	[=] key top	1
55.12582.05.0	[CI] key top	1
55.12584.05.0	[RCI] key top	1
55.12538.05.0	[-I] key top	1
55.12539.05.0	[+I] key top	1
55.15000.19.0	Key spring	28
55.28002.40.0	Reed relay	23
55.31002.50.0	Lamp for [x] and [+] keys	2
55.32011.52.0	Connector, 62-pin	1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55.21218.21.0
55.20744.20.0
55.33008.54.0
55.01572.03.0
55.22003.22.0
55.23000.23.0
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55.30002.43.0
55.11569.04.0
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55.11519.04.0
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55.33004.54.0
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55.24004.25.0
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55.29512.42.0
55.29513.42.0
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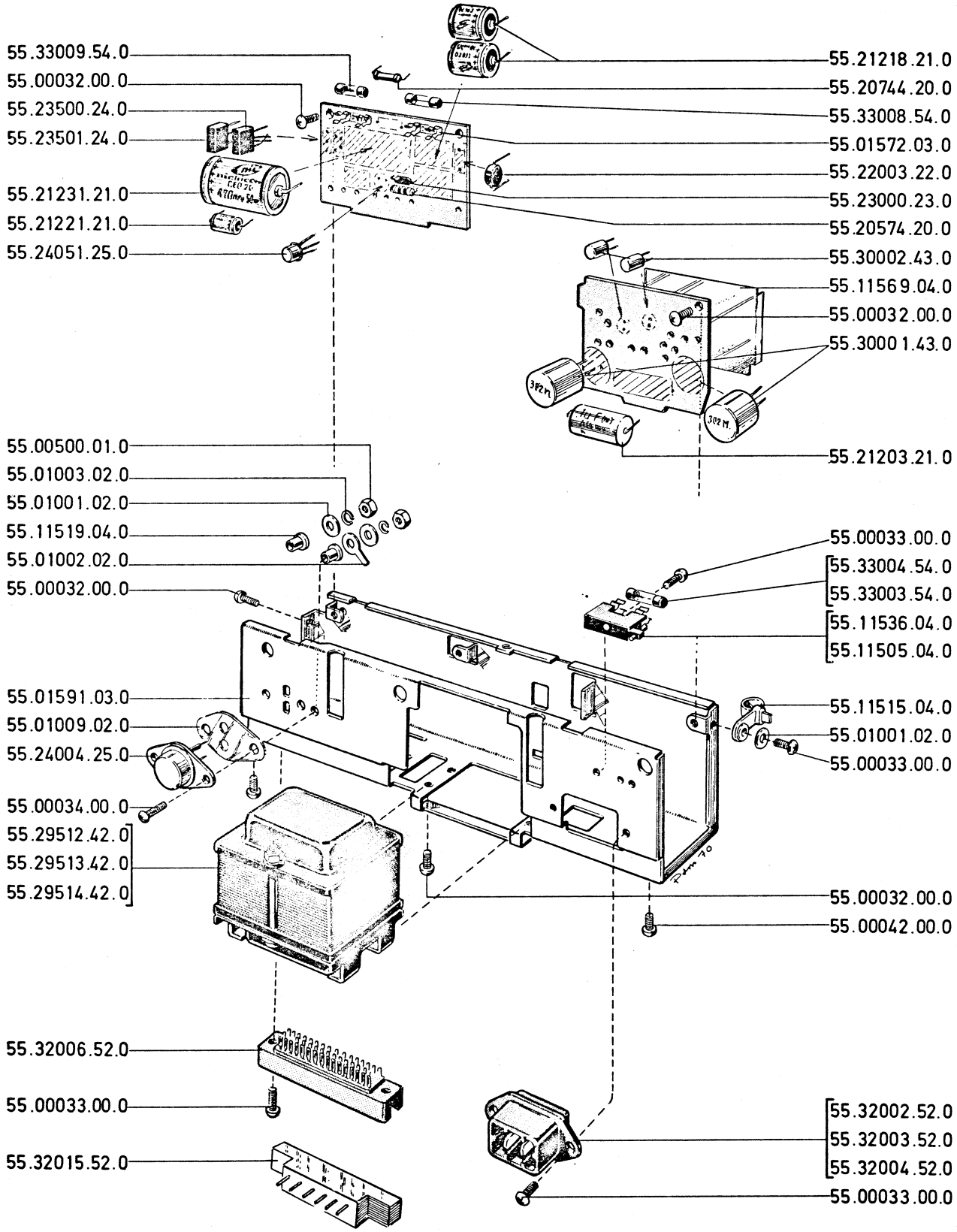
55.01001.02.0
55.00033.00.0
55.00032.00.0
55.00042.00.0
55.32006.52.0
55.00033.00.0
55.32015.52.0
55.32002.52.0
55.32003.52.0
55.32004.52.0
55.00033.00.0

3 POWER SUPPLY

Part No.	Description	Qty
55.33161.55.0	Power supply, complete	1
55.00042.00.0	Screw RX 4x6	2
55.00032.00.0	Screw RX 3x6	1
55.00033.00.0	Screw RX 3x8	1
55.01001.02.0	Washer 0.5x3.1x8	1
55.11515.04.0	Plastic harness holder	1
55.01591.03.0	Chassis for power supply	1
55.33162.55.0	Rectifier circuit board with components	1
55.00032.00.0	Screw RX 3x6	2
55.33146.55.0	Interference circuit board with components	1
55.00032.00.0	Screw RX 3x6	2
55.11569.04.0	Insulator sheet	1
55.24051.25.0	Transistor 2SC-826	1
55.24004.25.0	Transistor 2SC-1030	1
55.01009.02.0	Insulating washer	1
55.11519.04.0	Insulating bushing	2
55.01002.02.0	Lug	1
55.01001.02.0	Washer	2
55.01003.02.0	Washer FBB 3.1	2
55.00034.00.0	Screw RX 3x10	2
55.00500.01.0	Nut	2
55.22003.22.0	Diode SD-1B	1
55.23000.23.0	Zener diode ZR-225	1
55.23500.24.0	Diode array 1S-1850	1
55.23501.24.0	Diode array 1S-1850R	1
55.20574.20.0	Resistor 110k 1/2 W 10%	1
55.20744.20.0	Resistor 1k 1 W 10%	1
55.21203.21.0	Capacitor 0.1 µF 450 V	1
55.21218.21.0	Capacitor 10 µF 315 V	2
55.21221.21.0	Capacitor 22 µF 35 V	1
55.21231.21.0	Capacitor 470 µF 50 V	1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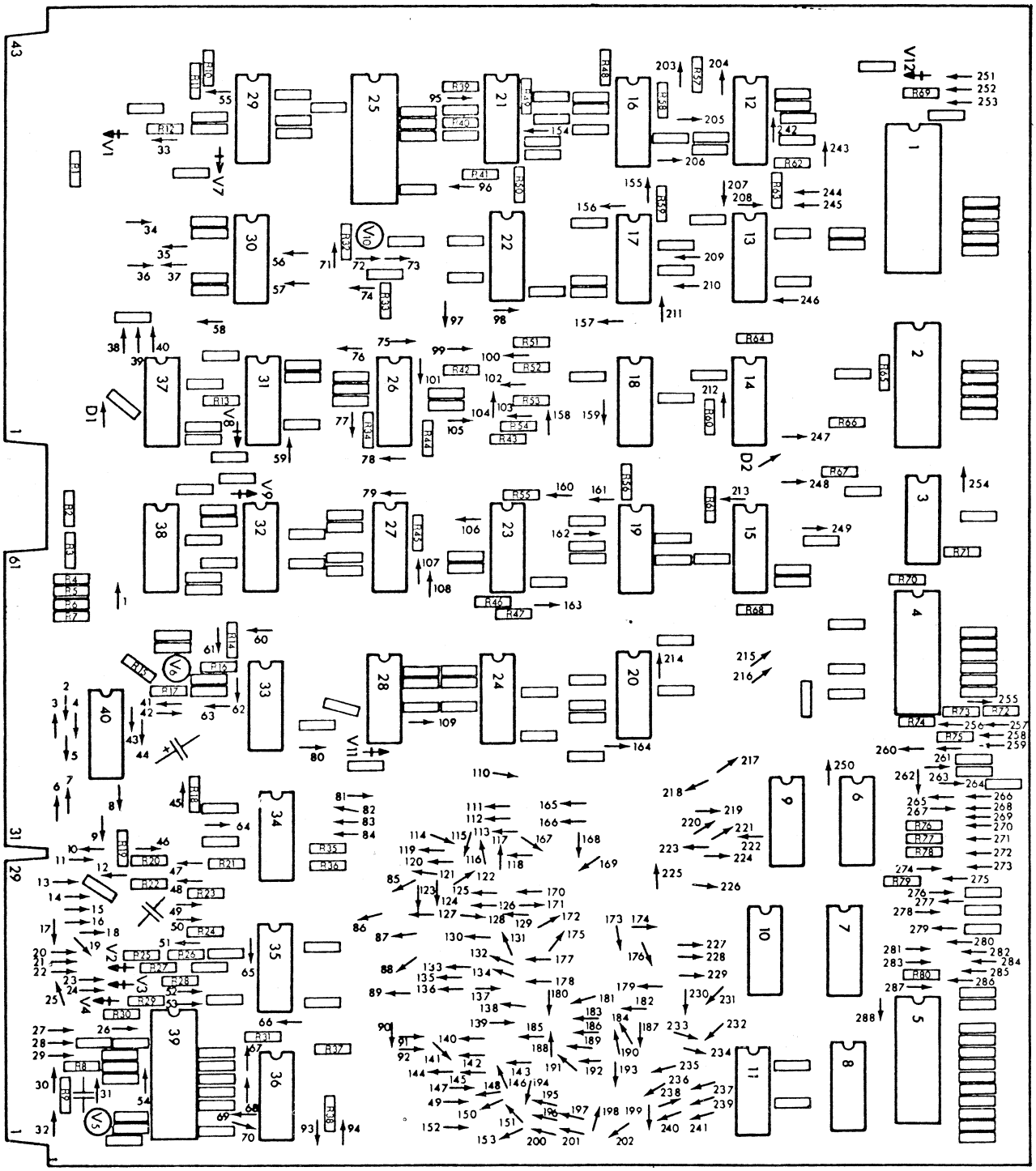
55.32015.52.0
55.32002.52.0
55.32003.52.0
55.32004.52.0
55.00033.00.0

Part No.	Description	Qty
55.30001.43.0	Coil	2
55.30002.43.0	Coil	2
55.29512.42.0	Transformer 100/110/120 V (408-PT)	1
55.29513.42.0	Transformer 115/120/127 V (409-PT)	1
55.29514.42.0	Transformer 200/220/240 V (410-PT)	1
55.00032.00.0	Screw RX 3x6	4
55.32002.52.0	Power inlet,American standard, 3-pin	1
55.32003.52.0	Power inlet, European standard, 3-pin	1
55.32004.52.0	Power inlet, European standard, 2-pin	1
55.00033.00.0	Screw RX 3x8	2
55.33004.54.0	Fuse 0.25 AT (SEMKO)	1
55.33008.54.0	Fuse 0.2 A (SEMKO)	1
55.33009.54.0	Fuse 0.63 A (SEMKO)	1
55.01572.03.0	Fuse holder clamp	4
55.11536.04.0	Fuse holder (SEMKO)	1
55.00033.00.0	Screw RX 3x8	1
55.33003.54.0	Fuse 0.5 AT (U.L., CSA, Japan)	1
55.11505.04.0	Fuse holder (U.L., CSA, Japan)	1
55.32015.52.0	Connector, 6-pin	1
55.32006.52.0	Connector, 45-pin	1
55.00033.00.0	Screw RX 3x8	2

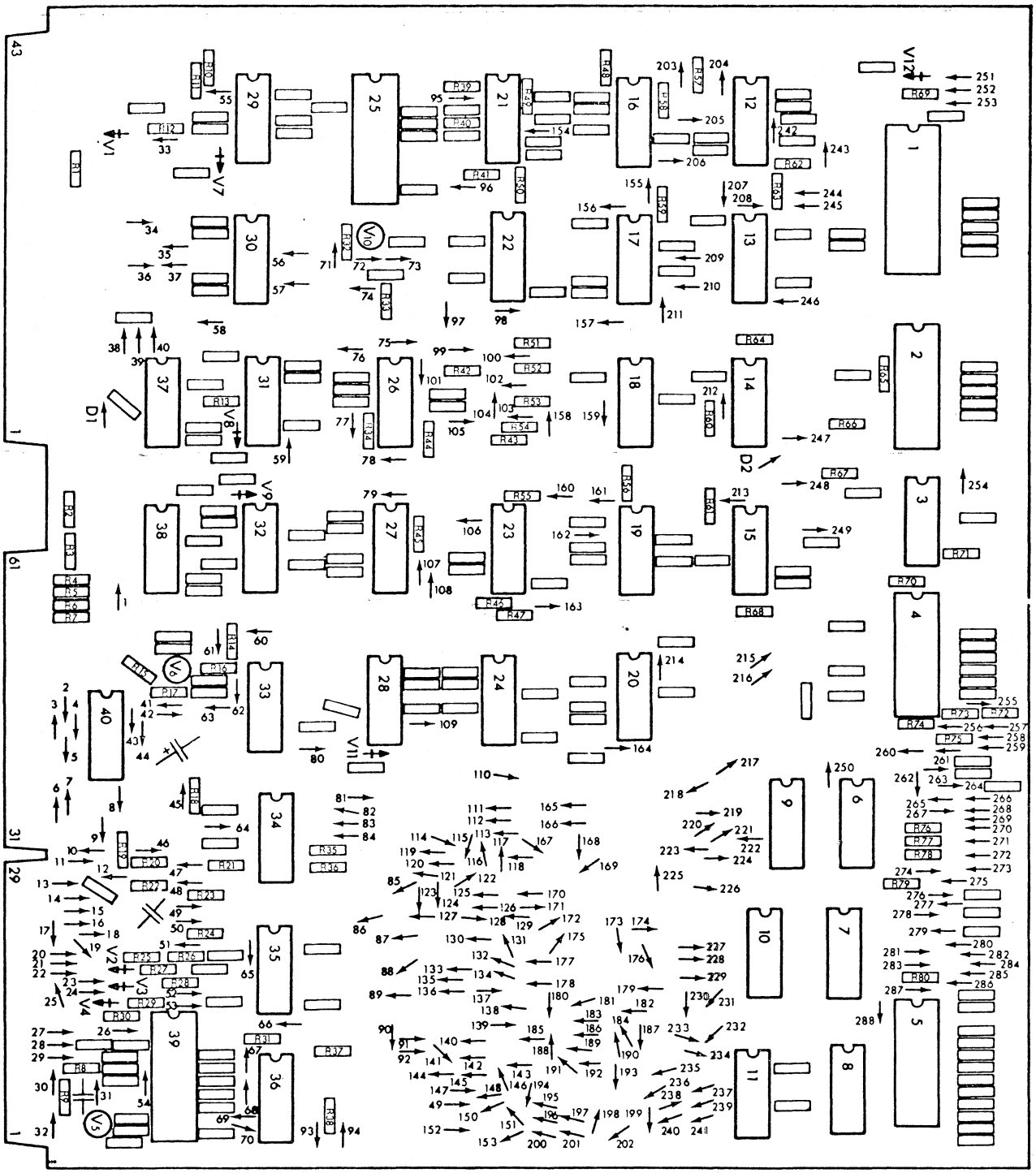


Board No. 1

4 CIRCUIT BOARDS

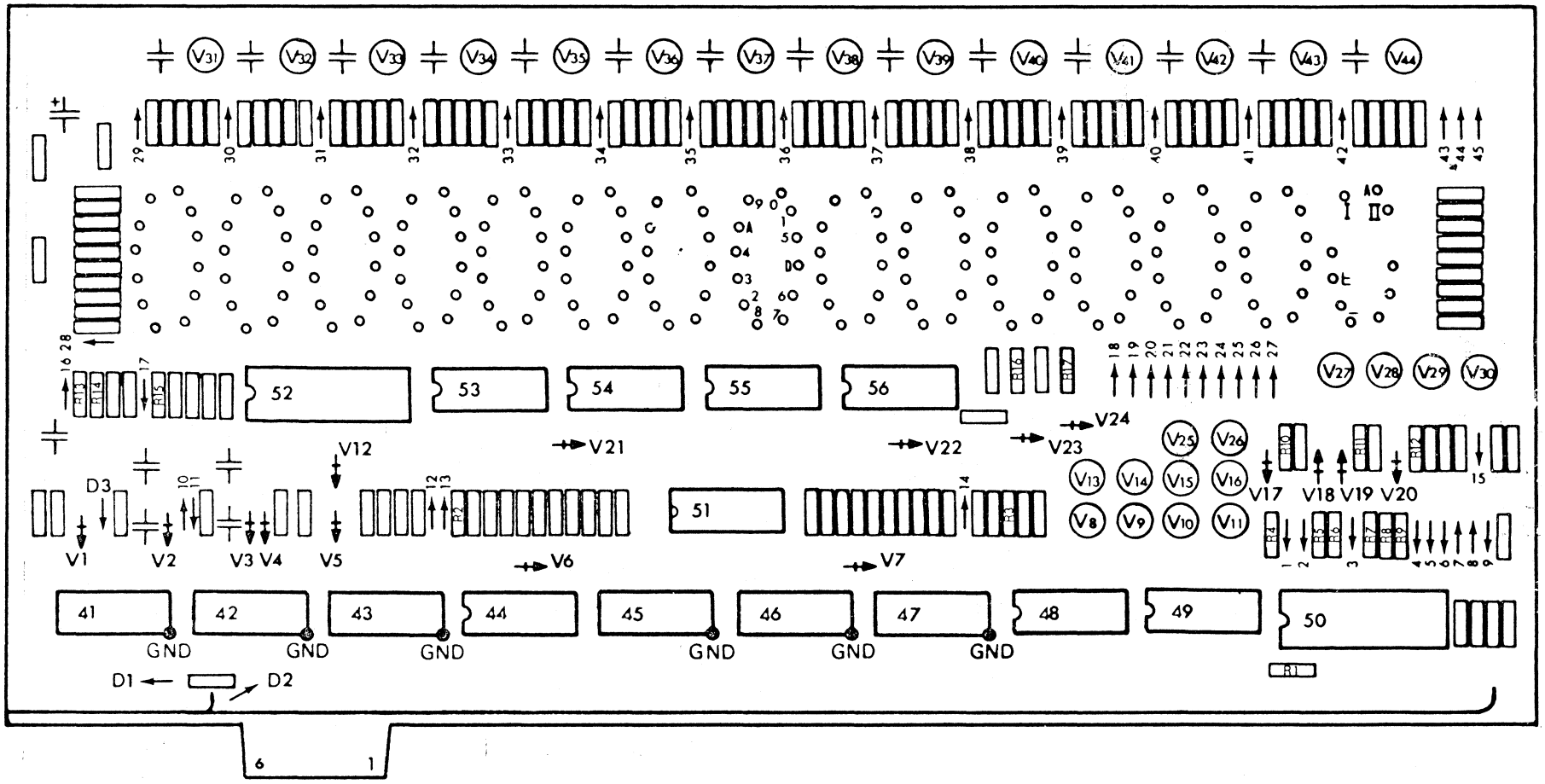
4.1 BOARD NO. 1

Part No.	Description	Qty
55.33163.55.0	Board No.1 complete	1
55.01582.03.0	Board No.1 side bracket (left,right)	2
55.01583.03.0	Rear bracket	1
55.00032.00.0	Screw RX 3x6	4
55.01001.02.0	Washer 0.5x3.1x8	2
55.24000.25.0	Transistor 2SA-549 K	2
55.24001.25.0	Transistor 2SC-458 KB	9
55.24050.25.0	Transistor 2SA-565 K	1
55.22000.22.0	Diode 1N-34 A	161
55.22015.22.0	Diode 1S-1588 L_1	74
55.22019.22.0	Diode 10D-1	1
55.22010.22.0	Diode array DN-3	1
55.25021.30.0	IC μPD 101C	15
55.25022.30.0	IC μPD 102C	3
55.25034.30.0	IC μPD 134C	4
55.25035.30.0	IC μPD 135C	5
55.25036.30.0	IC μPD 136C	11
55.25052.30.0	IC M-58202P	1
55.20230.20.0	Resistor 100 ohms 1/4 W 10%	1
55.20254.20.0	Resistor 5k 1/4 W 10%	5
55.20259.20.0	Resistor 12k 1/4 W 10%	4
55.20261.20.0	Resistor 18k 1/4 W 10%	2
55.20262.20.0	Resistor 20k 1/4 W 10%	7
55.20263.20.0	Resistor 27k 1/4 W 10%	11
55.20270.20.0	Resistor 39k 1/4 W 10%	5
55.20253.20.0	Resistor 42k 1/4 W 10%	1
55.20267.20.0	Resistor 50k 1/4 W 10%	2
55.20276.20.0	Resistor 56k 1/4 W 10%	48
55.20271.20.0	Resistor 82k 1/4 W 10%	71
55.20273.20.0	Resistor 100k 1/4 W 10%	2
55.20274.20.0	Resistor 110k 1/4 W 10%	16
55.20279.20.0	Resistor 150k 1/4 W 10%	7
55.20281.20.0	Resistor 180k 1/4 W 10%	9



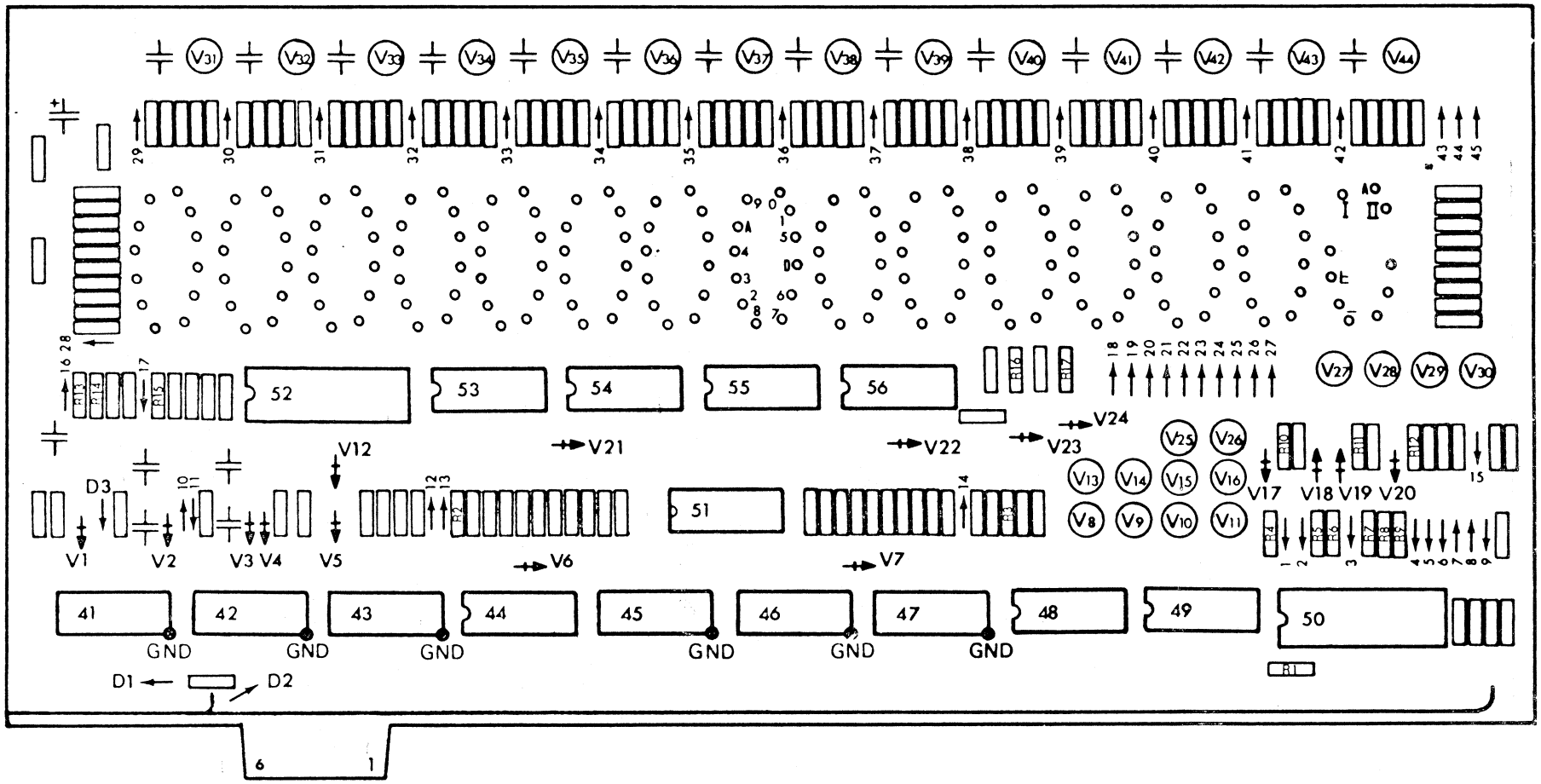
Board No. 1

Part No.	Description	Qty
55.20283.20.0	Resistor 270k 1/4 W 10%	18
55.20285.20.0	Resistor 330k 1/4 W 10%	39
55.20289.20.0	Resistor 500k 1/4 W 10%	1
55.21202.21.0	Capacitor 0.047 µF 50 V	1
55.21204.21.0	Capacitor 0.1 µF 50 V	1
55.21212.21.0	Capacitor 4.7 µF 50 V	1


Board No. 2
V31
V32
V33
V34
V35
V36
V37
V38
V39
V40
V41
V42
V43
V44
52
53
54
55
56
V12
V21
V22
V23
V24
V27
V28
V29
V30
V13
V14
V15
V16
V25
V26
V17
V18
V19
V20
D3
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
51
41
42
43
44
45
46
47
48
49
50
GND
D1
D2
6
1

4.2 BOARD NO. 2

Part No.	Description	Qty
55.33164.55.0	Board No.2 complete	1
55.01584.03.0	Board No.2 side bracket (left,right)	2
55.01585.03.0	Board No.2 front bracket	1
55.01583.03.0	Board No.2 rear bracket	1
55.00032.00.0	Screw RX 3x6	6
55.01001.02.0	Washer 0.5x3.1x8	2
55.01500.03.0	Wire holder	1
55.31505.51.0	Nixie tube H-1501 (sign)	1
55.31506.51.0	Nixie tube CD-81 (digit)	14
55.13518.06.0	Rubber protector for indicator tubes	1
55.13522.06.0	Foamed plastic protector for indicator tubes	1
55.01594.03.0	Nixie tube holder	1
55.00032.00.0	Screw RX 3x6	4
55.24041.25.0	Transistor 2SA-429	14
55.24001.25.0	Transistor 2SC-458 KB	16
55.24010.25.0	Transistor 2SC-857 K	14
55.22000.22.0	Diode 1N-34 A	36
55.22015.22.0	Diode 1S-1588 L_1	4
55.22006.22.0	Diode SV-08	2
55.22008.22.0	Diode array DP-4	1
55.25001.30.0	IC HD 3101	1
55.25089.30.0	IC HD 709M	6
55.25024.30.0	IC μPD 104C	1
55.25026.30.0	IC μPD 106C	1
55.25030.30.0	IC μPD 110C	1
55.25034.30.0	IC μPD 134C	3
55.25035.30.0	IC μPD 135C	2
55.20247.20.0	Resistor 2k 1/4 W 10%	14
55.20250.20.0	Resistor 3k 1/4 W 10%	14
55.20254.20.0	Resistor 5k 1/4 W 10%	7
55.20256.20.0	Resistor 6k 1/4 W 10%	1
55.20258.20.0	Resistor 10k 1/4 W 10%	3
55.20259.20.0	Resistor 12k 1/4 W 10%	4
55.20260.20.0	Resistor 15k 1/4 W 10%	5


Board No. 2
V31
V32
V33
V34
V35
V36
V37
V38
V39
V40
V41
V42
V43
V44
29
30
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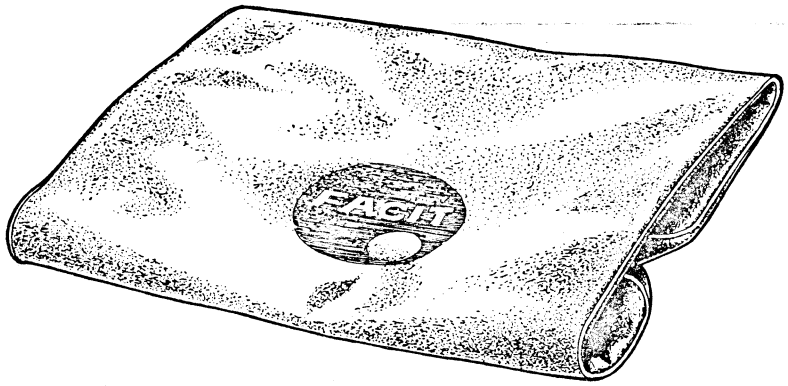
53
54
55
56
V12
V21
V22
V23
V24
V1
V2
V3
V4
V5
V6
V7
D3
51
V13
V14
V15
V16
V17
V18
V19
V20
V25
V26
V8
V9
V10
V11
41
42
43
44
45
46
47
48
49
50
GND
GND
GND
GND
GND
GND
D1
D2
B1
6
1

Part No.	Description	Qty
55.20262.20.0	Resistor 20k 1/4 W 10%	31
55.20263.20.0	Resistor 27k 1/4 W 10%	3
55.20265.20.0	Resistor 30k 1/4 W 10%	2
55.20278.20.0	Resistor 33k 1/4 W 10%	9
55.20276.20.0	Resistor 56k 1/4 W 10%	14
55.20271.20.0	Resistor 82k 1/4 W 10%	6
55.20274.20.0	Resistor 110k 1/4 W 10%	34
55.20279.20.0	Resistor 150k 1/4 W 10%	1
55.20281.20.0	Resistor 180k 1/4 W 10%	2
55.20280.20.0	Resistor 200k 1/4 W 10%	1
55.20549.20.0	Resistor 2k 1/2 W 10%	4
55.20562.20.0	Resistor 20k 1/2 W 10%	6
55.20565.20.0	Resistor 30k 1/2 W 10%	1
55.21003.21.0	Capacitor 250 pF 50 V	2
55.21006.21.0	Capacitor 400 pF 50 V	1
55.21009.21.0	Capacitor 800 pF 50 V	1
55.21018.21.0	Capacitor 0.047 µF 250 V	14
55.21204.21.0	Capacitor 0.1 µF 50 V	1
55.21206.21.0	Capacitor 1.0 µF 160 V	1
55.32010.52.0	Connector, 44-pin	1



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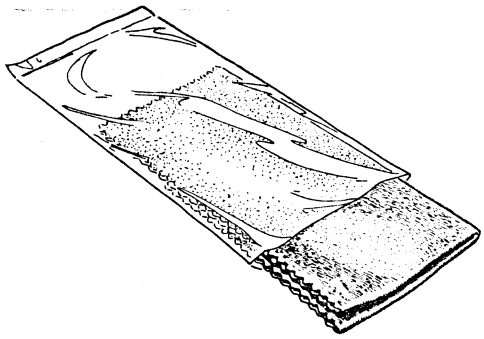

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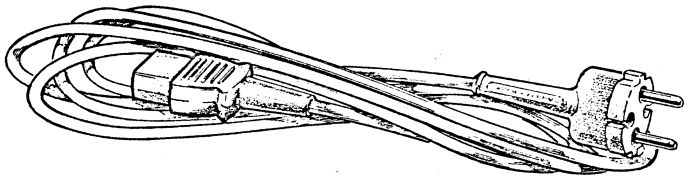

10.982.101.00
10.983.101.00
10.984.101.00
10.985.101.00
10.993.101.00
10.999.101.00

5 ACCESSORIES

Part No.	Description	Qty
55.40020.99.0	Protective cover	
55.40001.99.0	Cleaning cloth	
10.982.101.00	Mains cable,European standard,3-conductor	
10.983.101.00	Mains cable,European standard,2-conductor plug with 5 mm diameter	
10.984.101.00	Mains cable,American standard,2-conductor	
10.985.101.00	Mains cable,European standard,2-conductor plug with 4 mm diameter	
10.993.101.00	Mains cable,British standard,3-conductor without plug	
10.999.101.00	Mains cable,American/Canadian standard 3-conductor	

Facit 1129 cross-reference list Edition 1 1971

Part No.	Description	Section II Page No.	Remark	Old No.
10.982.101.00	Mains cable Eur. 3-conductor	5-1		
10.983.101.00	Mains cable Eur. 2-conductor, plug 5 mm	5-1		
10.984.101.00	Mains cable Amer.2-conductor	5-1		
10.985.101.00	Mains cable Eur. 2-conductor, plug 4 mm	5-1		
10.993.101.00	Mains cable Brit.3-conductor, without plug	5-1		
10.999.101.00	Mains cable Amer.3-conductor	5-1		
11.02630.01.0	Facit plate	1-1		
55.00032.00.0	Screw RX 3x6	1-1,2-1,3-1, -2,4-1,-3		
55.00033.00.0	Screw RX 3x8	2-1,3-1,-2		
55.00034.00.0	Screw RX 3x10	1-1,3-1		
55.00041.00.0	Screw RX 4x6	1-1		
55.00042.00.0	Screw RX 4x6	3-1		
55.00043.00.0	Screw RX 4x8	1-1		
55.00102.00.0	Screw RX 3x1.1x6	1-1		
55.00103.00.0	Screw RX 3x1.1x8	2-1		
55.00208.00.0	Screw RX 2.5x8	1-1		
55.00209.00.0	Stop screw 3x5	2-1		
55.00500.01.0	Nut	3-1		
55.00505.01.0	Nut	1-1		
55.01001.02.0	Washer 0.5x3.1x8	1-1,2-1,3-1, 4-1,-3		380 002 11
55.01002.02.0	Lug	3-1		
55.01003.02.0	Washer FBB 3.1	3-1		380 002 13
55.01009.02.0	Insulating washer	3-1		
55.01500.03.0	Wire holder	1-1,4-3		380 000 64
55.01572.03.0	Fuse holder clamp	3-2		
55.01581.03.0	Chassis	1-1		
55.01582.03.0	Board No. 1 side bracket	1-1,4-1,-2		

Part No.	Description	Section II Page No.	Remark	Old No.
55.01583.03.0	Rear bracket	1-1,4-1,-3		
55.01584.03.0	Board No. 2 side bracket (left, right)	1-1,4-3		
55.01585.03.0	Board No. 2 front bracket	1-1,4-3		
55.01587.03.0	Rear panel	1-1		
55.01590.03.0	Key set holder	2-1		
55.01591.03.0	Chassis for power supply	3-1		
55.01593.03.0	Window holder	1-1		
55.01594.03.0	Nixie tube holder	1-1,4-3		
55.01595.03.0	Dial plate	2-1		
55.11505.04.0	Fuse holder (U.L.,CSA,Japan)	3-2		
55.11515.04.0	Plastic harness holder	3-1		
55.11519.04.0	Insulating bushing	3-1		
55.11536.04.0	Fuse holder (SEMKO)	3-2		
55.11557.04.0	Cable clip (plastic)	2-1		
55.11561.04.0	Casing top	1-1		
55.11562.04.0	Casing bottom	1-1		
55.11566.04.0	Cover plate for test connector	1-1		
55.11569.04.0	Insulator sheet	3-1		
55.11575.04.0	Keyboard panel	1-1		
55.11576.04.0	Window	1-1		
55.12517.05.0	[RV] key top	2-2		
55.12518.05.0	[CE] key top	2-2		
55.12520.05.0	[0] key top	2-1		380 000 38
55.12521.05.0	[1] key top	2-1		380 000 39
55.12522.05.0	[2] key top	2-1		380 000 40
55.12523.05.0	[3] key top	2-1		380 000 41
55.12524.05.0	[4] key top	2-1		380 000 42
55.12525.05.0	[5] key top	2-1		380 000 43
55.12526.05.0	[6] key top	2-1		380 000 44
55.12527.05.0	[7] key top	2-1		380 000 45

Facit 1129 cross-reference list Edition 1 1971

Part No.	Description	Section II Page No.	Remark	Old No.
55.12528.05.0	[8] key top	2-1		380 000 46
55.12529.05.0	[9] key top	2-1		380 000 47
55.12530.05.0	[.] key top	2-1		380 000 48
55.12532.05.0	[-] key top	2-2		380 000 53
55.12533.05.0	[x] key top	2-2		380 000 54
55.12534.05.0	[+] key top	2-2		
55.12535.05.0	[=] key top	2-2		380 000 56
55.12538.05.0	[-I] key top	2-2		
55.12539.05.0	[+I] key top	2-2		
55.12580.05.0	[K] key top	2-1		
55.12581.05.0	[C] key top	2-1		
55.12582.05.0	[CI] key top	2-2		
55.12584.05.0	[RCI] key top	2-2		
55.12590.05.0	Rotary switch knob	2-1		380 000 31
55.13518.06.0	Rubber protector for indicator tubes	1-1,4-3		
55.13520.06.0	Rubber foot (front)	1-1		
55.13521.06.0	Rubber foot (rear)	1-1		
55.13522.06.0	Foamed plastic protector for indicator tubes	1-1,4-3		
55.15000.19.0	Key spring	2-2		380 000 36
55.20230.20.0	Resistor 100 ohms 1/4 W 10%	4-1		380 003 07
55.20247.20.0	Resistor 2 k 1/4 W 10%	4-3		380 003 10
55.20250.20.0	Resistor 3 k 1/4 W 10%	4-3		380 003 11
55.20253.20.0	Resistor 42 k 1/4 W 10%	4-1		380 003 29
55.20254.20.0	Resistor 5 k 1/4 W 10%	4-3		360 331 18
55.20256.20.0	Resistor 6 k 1/4 W 10%	4-3		
55.20258.20.0	Resistor 10 k 1/4 W 10%	4-3		360 331 20
55.20259.20.0	Resistor 12 k 1/4 W 10%	3-1,4-1,-3		360 331 21
55.20260.20.0	Resistor 15 k 1/4 W 10%	4-4		360 331 22
55.20261.20.0	Resistor 18 k 1/4 W 10%	4-1		

Part No.	Description	Section II Page No.	Remark	Old No.
55.20262.20.0	Resistor 20 k 1/4 W 10%	4-1,-4		360 331 24
55.20263.20.0	Resistor 27 k 1/4 W 10%	4-4		
55.20265.20.0	Resistor 30 k 1/4 W 10%	4-4		360 331 26
55.20267.20.0	Resistor 50 k 1/4 W 10%	4-1 ~ 3		360 331 27
55.20270.20.0	Resistor 39 k 1/4 W 10%	4-1 ~ 3		
55.20271.20.0	Resistor 82 k 1/4 W 10%	4-1,-3		360 331 49
55.20273.20.0	Resistor 100 k 1/4 W 10%	4-1 ~ 3		360 331 29
55.20274.20.0	Resistor 110 k 1/4 W 10%	4-2,-4		380 003 30
55.20276.20.0	Resistor 56 k 1/4 W 10%	4-1,-3		
55.20278.20.0	Resistor 33 k 1/4 W 10%	4-4		
55.20279.20.0	Resistor 150 k 1/4 W 10%	4-1,-4		360 331 30
55.20280.20.0	Resistor 200 k 1/4 W 10%	4-4		360 331 31
55.20281.20.0	Resistor 180 k 1/4 W 10%	4-1,-4		
55.20283.20.0	Resistor 270 k 1/4 W 10%	4-1 ~ 3		
55.20285.20.0	Resistor 330 k 1/4 W 10%	4-2		
55.20289.20.0	Resistor 500 k 1/4 W 10%	4-2		380 003 35
55.20549.20.0	Resistor 2 k 1/2 W 10%	4-4		360 331 12
55.20562.20.0	Resistor 20 k 1/2 W 10%	4-4		
55.20565.20.0	Resistor 30 k 1/2 W 10%	4-4		
55.20574.20.0	Resistor 110 k 1/2 W 10%	3-1		
55.20744.20.0	Resistor 1 k 1 W 10%	3-1		380 003 21
55.21003.21.0	Capacitor 250 pF 50V	4-4		
55.21006.21.0	Capacitor 400 pF 50V	4-4		380 004 14
55.21009.21.0	Capacitor 800 pF 50V	4-4		
55.21018.21.0	Capacitor 0.047 µF 250V	4-4		
55.21202.21.0	Capacitor 0.047 µF 50V	4-2,-4		
55.21203.21.0	Capacitor 0.1 µF 450V	3-1		380 004 17
55.21204.21.0	Capacitor 0.1 µF 50V	4-2,-4		
55.21206.21.0	Capacitor 1.0 µF 160V	4-4		380 004 30
55.21212.21.0	Capacitor 4.7 µF 50V	4-2		
55.21218.21.0	Capacitor 10 µF 315V	3-1		

Facit 1129 cross-reference list Edition 1 1971

Part No.	Description	Section II Page No.	Remark	Old No.
55.21221.21.0	Capacitor 22 µF 35V	3-1		
55.21231.21.0	Capacitor 470 µF 50V	3-2		
55.22000.22.0	Diode 1N-34A	4-1,-3		360 331 09
55.22003.22.0	Diode SD-1B	3-1		380 005 59
55.22006.22.0	Diode SV-08	4-3		
55.22008.22.0	Diode array DP-4	4-3		
55.2201C.22.0	Diode array DN-3	4-1		
55.22015.22.0	Diode 1S-1588L1	4-1,-3		
55.22019.22.0	Diode 10D-1	4-1		
55.23000.23.0	Zener diode ZR-225	3-1		
55.23500.24.0	Diode 1S-1850	3-1		
55.23501.24.0	Diode 1S-1850R	3-1		
55.24000.25.0	Transistor 2SA-549K	4-1,-3		380 005 09
55.24001.25.0	Transistor 2SC-458KB	4-1,-3		
55.24004.25.0	Transistor 2SC-1030	3-1		
55.24010.25.0	Transistor 2SC-857K	4-3		380 005 02
55.24041.25.0	Transistor 2SA-429	4-3		380 005 10
55.24050.25.0	Transistor 2SA-565K	4-1		
55.24051.25.0	Transistor 2SC-826	3-1		380 005 06
55.25001.30.0	IC HD 3101	4-3		
55.25021.30.0	IC µPD 101 C	4-1		
55.25022.30.0	IC µPD 102 C	4-1		
55.25024.30.0	IC µPD 104 C	4-3		
55.25026.30.0	IC µPD 106 C	4-3		
55.25030.30.0	IC µPD 110 C	4-3		
55.25034.30.0	IC µPD 134 C	4-1,-3		
55.25035.30.0	IC µPD 135 C	4-1,-3		
55.25036.30.0	IC µPD 136 C	4-1		
55.25052.30.0	IC M-58202P	4-1,-2		
55.25089.30.0	IC HD 709 M	4-3		

Part No.	Description	Section II Page No.	Remark	Old No.
55.28002.40.0	Reed relay	2-2		
55.29512.42.0	Transformer 100/110/120V	3-2		
55.29513.42.0	Transformer 115/120/127V	3-2		
55.29514.42.0	Transformer 200/220/240V	3-2		
55.30001.43.0	Coil	3-2		380 002 50
55.30002.43.0	Coil	3-2		
55.31002.50.0	Lamp for [×] and [+] keys	2-2		
55.31505.51.0	Nixie tube H-1501 (sign)	4-3		
55.31506.51.0	Nixie tube CD-81 (digit)	4-3		
55.32002.52.0	Power inlet Amer.std.,3-pin	3-2		
55.32003.52.0	Power inlet Eur.std., 3-pin	3-2		
55.32004.52.0	Power inlet,Eur.std., 2-pin	3-2		
55.32006.52.0	Connector, 45-pin	3-2		
55.32010.52.0	Connector, 44-pin	4-4		
55.32011.52.0	Connector, 62-pin	2-2		
55.32015.52.0	Connector, 6-pin	3-2		
55.32506.53.0	Power switch (SEMKO)	2-1		
55.32507.53.0	Power switch (U.L.,CSA,Japan)	2-1		
55.32508.53.0	Rotary switch	2-1		
55.33003.54.0	Fuse 0.5AT (U.L.,CSA,Japan)	3-2		
55.33004.54.0	Fuse 0.25AT (SEMKO)	3-2		
55.33008.54.0	Fuse 0.2A (SEMKO)	3-2		
55.33009.54.0	Fuse 0.63A (SEMKO)	3-2		
55.33131.55.0	Clear and constant key set	2-1		
55.33132.55.0	Figure key set	2-1		
55.33133.55.0	Operation key set	2-1		
55.33146.55.0	Interference circuit board with components	3-1		
55.33159.55.0	Store operation key set	2-1		
55.33160.55.0	Keyboard complete	2-1		