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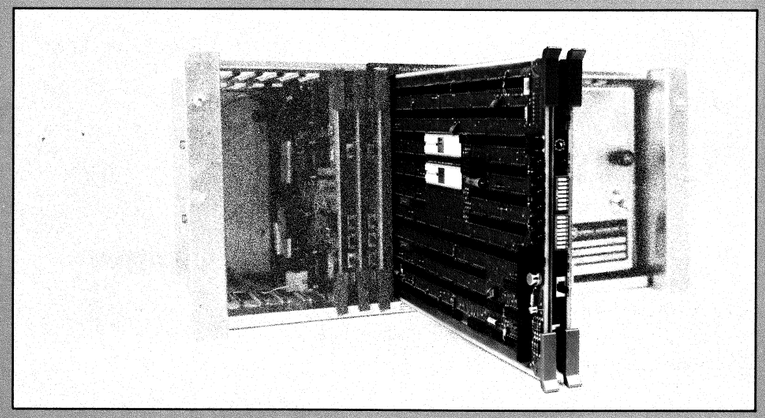


GA-16/110 AND GA-16/220 MICROCOMPUTERS

PRODUCT DESCRIPTION

General Automation's new GA-16/110 and GA-16/220 offer a new standard of performance in LSI microcomputers. Full-fledged 16-bit computers in all respects, they outperform every other microcomputer on the market.

Their speed is significantly faster, their instruction repertoire is superior and their system features are more complete. They are totally compatible with the full array of General Automation software and I/O products. Still, they are directly competitive in the microcomputer price range.

The GA-16/110 is a complete computer with CPU, memory and I/O on a single board. The GA-16/220 adds a second CPU board to provide additional system features.

The GA-16/110 and GA-16/220 are ideal for all microcomputer applications requiring not only low price but also a wide margin of performance and support above typical chip sets and other microcomputers.

FEATURES

Total compatibility – software and I/O compatible with GA-16/440, GA-16/330 and SPC-16.

Off-the-shelf software – 7 field-proven operating systems, 5 sub-systems, 5 languages, plus extensive utilities and programming aids.

Off-the-shelf controllers – more than 100 field-proven I/O controllers for peripherals, process I/O and communications.

Memory parity and write protect – for operating integrity.

High performance –
- 16 general purpose registers
- Fast real-time context switching
- 3 I/O Ports
- Interleaved DMA
- Hardware Multiply/Divide
- Vectored priority interrupts

OEM configuration versatility – A wide choice of hardware and software options to configure individual OEM systems.

Low price – minicomputer performance and support at microcomputer prices.

GENERAL AUTOMATION

COMPATIBILITY

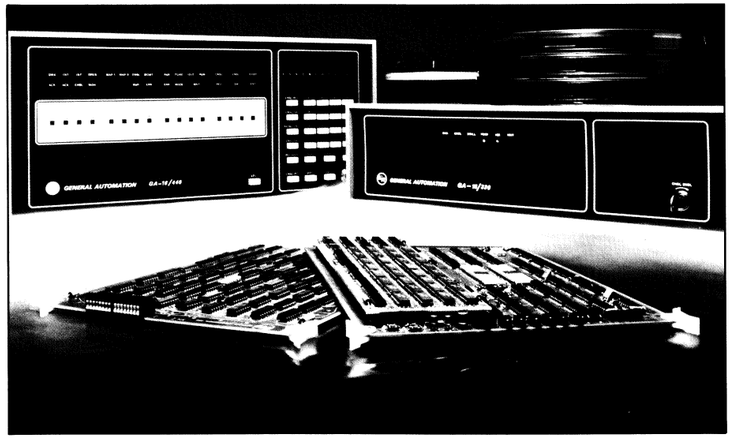
The family compatibility of the Solution Series is complete – and it is real. It gives the OEM designer immediate access to more software and more I/O controllers than are available with any other microcomputer.

The GA-16/110 and GA-16/220 are compatible in software and I/O not only with the new Solution Series Computers but also with the SPC-16. They run existing SPC-16 programs as well as programs assembled on the GA-16/330 and GA-16/440 with GA's machine level software, high level languages and operating systems.

Application programs for the GA-16/110 are generated on any of GA's larger machines. The GA-16/110 is especially designed as a low cost, high performance "load-and-go" worker computer for dedicated applications – not as a software development system or to run under sophisticated disk-based operating systems.

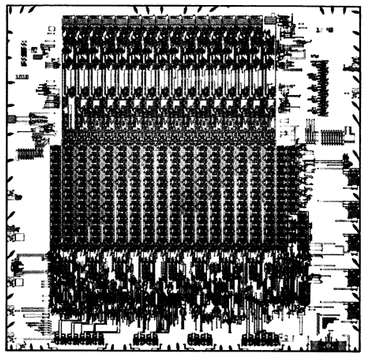
The GA-16/220, on the other hand, offers the full complement of hardware features for program generation and to run with all GA operating systems and software (except CONTROL IV, the sophisticated Memory Management Operating System for large GA-16/440 Supermini's).

The I/O bus on the GA-16/110 and GA-16/220 is totally compatible with the SPC-16 and all Solution Series computers. Both the GA-16/110 and GA-16/220 operate with all GA Programmed I/O controllers. In addition, the GA-16/220 operates with all GA DMA controllers. GA currently offers more than 100 field-proven I/O controllers and related software which run on the Solution Series Microcomputers.

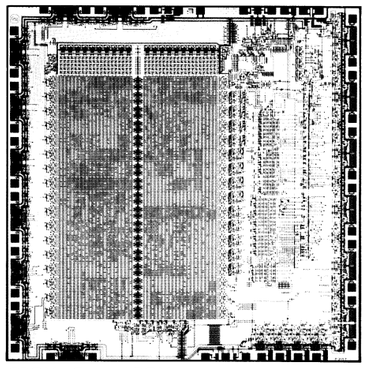


PERFORMANCE AND TECHNOLOGY

The heart of the GA-16/110 and GA-16/220 is a 16-bit microprogrammed LSI CPU consisting of two proprietary n-channel silicon gate MOS chips – the Register, Arithmetic and Logic Unit (RALU) which essentially duplicates the CPU organization of GA's SPC-16 and GA-16/440 minicomputers – and the Control Read-Only Memory (CROM) which contains the microcode and logic emulating an expanded SPC-16 instruction set. Microinstructions are 34-bits in length, giving an especially versatile branching capability, a key factor in achieving 16-bit performance substantially superior to other microcomputers.



RALU – Register, Arithmetic and Logic Unit



CROM – Control ROM

The LSI n-channel silicon gate MOS CPU is equivalent to more than 20,000 components

Microcycle time is 500 nanoseconds. Representative instruction execution times are:

LDR	Load any register	2.70 µsec
ADDC	Add registers and compare	2.10 µsec
JSR	Jump to subroutine	2.10 µsec
SBIT	Set bit	4.10 µsec
STBY	Store Byte	3.60 µsec
DTOM	Transfer word directly to I/O from memory	3.20 µsec

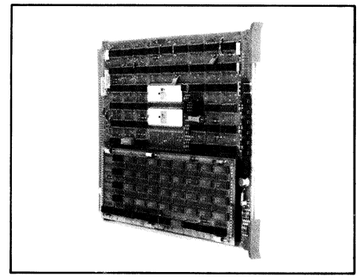
FEATURES

The GA-16/110 and GA-16/220 provide more system features than any other microcomputers.

Standard

- ☐ nMOS technology
- ☐ 500 nsec microcycle
- ☐ Integral Microconsole
- ☐ Asynchronous memory bus
- ☐ Semiconductor RAM/PROM/ROM
- ☐ 64K direct addressability
- ☐ GA-16/SPC-16 compatibility modes
- ☐ Memory expansion to 128K bytes
- ☐ Eleven addressing modes
- ☐ 16 General-purpose registers (6 index, 2 base relative, 2 subroutine link)
- ☐ Dual 8-register banks for fast context switching
- ☐ Hardware multiply/divide
- ☐ Vectored priority interrupts
- ☐ Critical interrupts are non-inhibitable
- ☐ Power Fail/Auto Restart
- ☐ Real Time Clock input and interrupt
- ☐ *Fully implemented 1 msec RTC
- ☐ Operations Monitor Alarm
- ☐ System Fail Restart
- ☐ Programmed I/O
- ☐ *Fully implemented SPC-16 DMA
- ☐ *Serial I/O controller
- ☐ Remote control lines
- ☐ Bit, byte, word instructions

*220 Only



GA-16/110 with 2K words of RAM – a complete, high performance microcomputer on a single board, optimized for OEM designers to bury in their products.

Optional

- ☐ *System Console Interface
- ☐ *Interrupt program time out
- ☐ *Memory byte parity
- ☐ *Memory write protect
- ☐ Memory error correction
- ☐ High-speed signed multiply/divide
- ☐ Autoload PROM's
- ☐ Backup battery power supply

MULTI-REGISTERS

Like GA's large 16-bit minicomputers, the GA-16/110 and GA-16/220 microcomputers are organized around 16 general purpose 16-bit registers, arranged in two groups of eight for fast context switching. All registers can be used as accumulators and the content of any register can be executed as an instruction register. In addition to their general purpose functions, three registers in each group are used as index registers, one for base relative addressing and one for subroutine linking. No other microcomputer provides this degree of versatility and processing power.

VERSATILE ADDRESSING POWER

The GA-16/110 and GA-16/220 provide unmatched memory addressing power, with 11 address modes which access all words, bytes and individual bits in a full range of 64K words of memory.

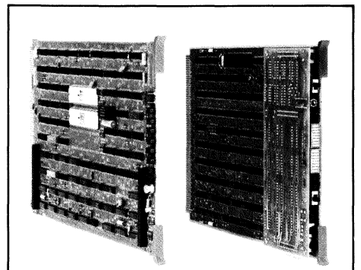
- ☐ Direct
- ☐ Direct, indexed
- ☐ Indirect
- ☐ Indirect, indexed
- ☐ Program relative
- ☐ Program relative, indirect
- ☐ Base relative
- ☐ Base relative, indexed
- ☐ Base relative, indirect
- ☐ Base relative, indirect/indexed
- ☐ Literal

This high degree of addressing versatility is not available in any other microcomputer.

FAST CONTEXT SWITCHING

Context switching between the foreground and background registers provides a powerful means to enhance system throughput. It takes only a few microseconds to shift from one program to another simply by switching from one 8-register bank to the other without disturbing either set of registers. This is particularly important in real time environments with repetitive interrupts from sources such as high speed A-D converter, real-time clock or serial communication lines.

For example, a GA-16/220 handling several channels of heavy traffic in a message store-and-forward system services high frequency interrupts on an SDLC channel, interspersed with many random interrupts from asynchronous data channels. In receiving, storing and transmitting data, a prime requirement is that the CPU get in and out of interrupt routines quickly.



The GA-16/220 adds DMA, Serial I/O, 1msec RTC, system console interface and IPL PROM.

In GA microcomputers, with fast context switching, subroutine entry and exit is typically 5 times faster than microcomputers limited to one set of registers. Furthermore, in an application having one very high speed interrupt, it can be serviced with even greater efficiency by dedicating the background registers to handling that interrupt alone. Interrupt routine parameters, such as indirect and indexing memory references values, conversion constants or format constants, can reside permanently in the background registers, ready for use when context is switched. Not only are entry and exit accelerated, but the interrupt routine itself is shorter and its execution is faster.

REAL-TIME CLOCK

The GA-16/110 provides two RTC input pins, one for RTC enable and one for an external frequency which triggers the RTC interrupt. The input signal may be from AC line frequency, a precision counter, the OEM system clock, or other source.

In the GA-16/220, a 1 msec signal is derived from a 20 mega Hz crystal to provide a fully-implemented 1 msec real-time clock, with selective masking by software.

In OEM systems, the RTC routine is written by the OEM programmer for the particular requirements of his system. GA's generalized software operating systems use the 1 msec RTC interrupt for time-of-day, elapsed time and a variety of task scheduling operations.

The RTC interrupt is disabled when the interrupt system is inhibited, thus its priority is lower than the non-inhibitable class of interrupts. It has highest priority among all other interrupts.

OPERATIONS MONITOR ALARM (OMA) AND SYSTEM SAFE LINE

OMA surveys overall system operation by requiring execution of a Pulse Monitor Alarm (PMA) instruction periodically during the running of a program. The 220 msec OMA counter is initially enabled by the PMA instruction and is reset by each subsequent PMA in the program.

If reset occurs within 220 msec, the program is considered to be running normally. If not, the system is considered to be malfunctioning, causing OMA to switch the microcomputer to an IDLE condition and set the System Safe Line false. It also flags the unsafe condition on the Microconsole by turning the RUN light off and the PMA light on. The system can be restarted manually. However, in most applications external system logic uses the System Safe Signal to trigger recovery procedures which may transfer operation to a back-up computer; notify a host computer which would attempt to download program or diagnostics; or direct the Microcomputer to PROM for program reload or diagnostic procedures.

POWER FAIL/AUTO RESTART

Compact and Jumbo power supplies monitor AC primary voltage and signal the CPU when voltage drops below a pre-set level. This initiates a non-inhibitable interrupt through the power fail vector, to execute the user's power-down routine. It also starts a timer which allows 250 μsec for an orderly shutdown; then the CPU automatically goes into a WAIT condition.

(When the microcomputers are powered by a user's system power supply, the OEM designer must provide the Power Fail Detect signal to the CPU's).

On power-up the system is reset (i.e. reset I/O, disable interrupts, set CPU in foreground and 32K modes) and a non-hibitable interrupt causes one of **several** power-up options to occur:

1. If the Cold Start Line is not grounded the GA-16/110 and GA-16/220 execute the user's power-up routine, via the restart vector in RAM. This requires preservation of semi conductor memory when AC is down, thus is valid only in systems having a back-up battery power supply. Otherwise, PROM or manual restart procedures apply.
2. If Cold Start is grounded:
   a) Small, dedicated GA-16/110/220's (with piggyback memory and without System Console Interface) automatically reload via the IPL PROM on the memory board.
   b) The GA-16/220, **with** the System Console Interface option, goes to the console PROM for interactive manual restart or, if the console is disabled by the Microconsole switch, the CPU goes to the IPL PROM on the System Console Interface Module and automatically reloads the program.

User's special routines can be placed in these PROM locations.

HARDWARE MULTIPLY & DIVIDE

Multiplication and division of 15-bit fixed point, positive numbers is performed directly in hardware and microcode, rather than through the shift/add/subtract software subroutines required in most microcomputers. Hardware multiply and divide run approximately nine times faster than their equivalent software subroutines. Negative numbers are handled by performing positive operations and labeling the sign by means of short subroutines in the FORTRAN library.

The programmer can set the number of bits to be processed. For example, with a 4-bit multiplier, execution time is 11.5 μsec, with a 15-bit multiplier it is 33.5 μsec. Most microcomputers require several hundred μsec for comparable functions.

For applications requiring even higher speed **signed** multiply/divide a standard two-board option plugs into regular I/O slots. The complete multiplication cycle for two signed numbers is 15.3 μsec, producing a 30-bit signed product. A 30-bit dividend is divided by a 15-bit divisor in 19.4 μsec. Quotient and remainder are both 15-bit + sign. This high speed multiply/divide processor runs in parallel with the CPU, and DMA .

GA-16, SPC-16 COMPATIBILITY MODES

The Solution Series microcomputers are primarily designed to address 64K 16-bit words of memory and to take advantage of new instructions and new features in the Solution Series. Operation in this condition is called the 64K Mode. Programs written on GA-16/440's or GA-16/330's as well as CONTROL I, II, and III operating systems run in this mode.

All Solution Series computers can be put into a 32K Mode (by switch on the GA-16/220, or by jumper on the GA-16/110) which converts them to function as a standard SPC-16 with 32K word address range. Existing SPC-16 programs, written according to GA software conventions, run without alteration. DBOS, RTX and RTOS run in this mode.

The GA-16/110, when set to 32K or 64K mode, is locked in that condition. The GA-16/220, when switched to 32K Mode is locked in that mode; when switched to the programmed mode the GA-16/220 is under software control and can be dynamically switched between 64K and 32K modes.

INTERRUPTS

The GA-16/110 and GA-16/220 have three types of interrupts:

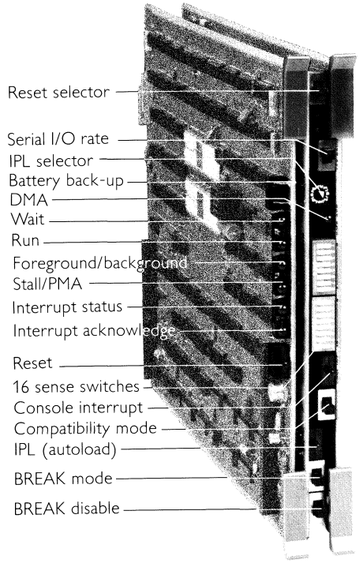
Non-inhibitable (NI) interrupts Related to conditions which are critical to proper system operation, these are always serviced immediately upon completion of the current instruction, even though the interrupt system may be inhibited.

- ☐ Power Fail Detect
- ☐ Auto Restart
- ☐ TTY Break
- ☐ Memory Parity Error
- ☐ Write Protect Violation
- ☐ Interrupt Program Time-out
- ☐ Non-implemented Op Code

I/O Interrupts Their order of priority is real time clock, TTY ready, operator's microconsole interrupt plus an unlimited number of individually vectored I/O interrupts. Each can be selectively masked and the entire interrupt system is dynamically enabled by software. GA's standard software supports 64 I/O interrupts with priority of peripheral controllers determined by their physical location on the I/O bus.

MICROCONSOLE

A unique feature of the GA-16/110 and GA-16/220 is the Microconsole. This is a group of indicators and controls on the front edge of the boards, providing displays and controls for operation in a dedicated application. With the Microconsole, the OEM designer and the end user have positive, inexpensive manual control of the operating environment. A separate computer console is not needed. LED's show the running status of the machine; active controls permit autoload, reset and console interrupt functions while other switches set-up system configuration parameters such as serial I/O rate and compatibility mode.



The unique Microconsole provides firm system control to the operator.

SYSTEM CONSOLE

The GA-16/220 features an optional System Console Interface Module providing complete programmer's console capability via TTY or CRT. Mounted piggyback on the GA-16/220 board, this module contains GA's Basic Utility Software (BUS) package in PROM, which permits interactive communications through the GA-16/220's built-in serial I/O controller. Console functions include:

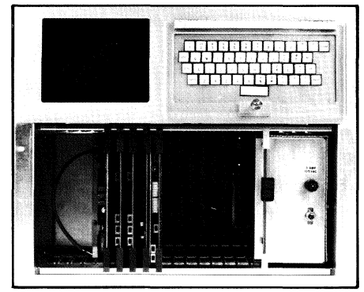
- ☐ Display and change all registers
- ☐ Display and change all memory locations
- ☐ Display a block of data from memory
- ☐ Store a pattern in a block of memory
- ☐ Load and punch binary tapes
- ☐ Set 4 traps
- ☐ Single step
- ☐ Reset I/O
- ☐ Go (begin execution at selected address)

Also in the Console PROM are callable subroutines frequently used in software development, program execution and equipment trouble-shooting – such as, input/output single hex or ASCII character, hex/ASCII conversion, output 4 hex digits and check for required address or value specification.

The System Console Interface Module provides additional controls for setting TTY BREAK condition and reset mode selection as well as two additional areas of memory:

- ☐ 256 words of RAM for the PGS Loader during IPL and for storing registers and flags, during console operations. This avoids the need to reserve main memory for these purposes. Console operations use up to 56 words of RAM; the balance is available to the user's program for special functions.
- ☐ Positions for GA's optional 256-word IPL PROM, or a user's special PROM for autoload, restart, downloading, diagnostics.

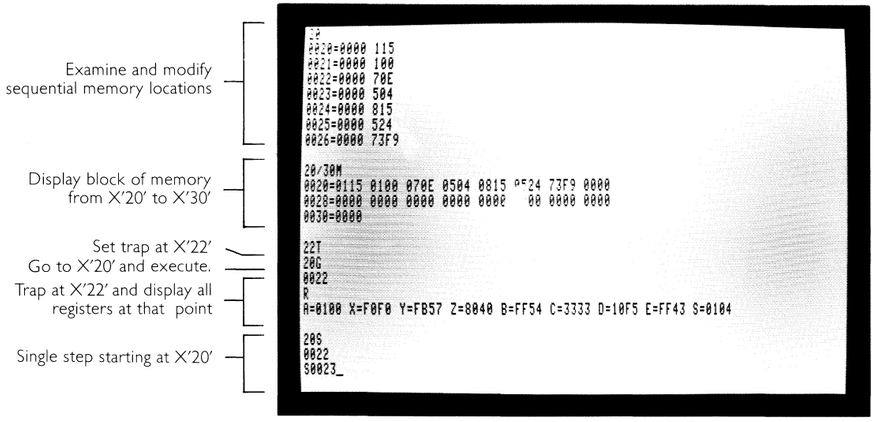
The 1K of memory represented by the System Console Interface Module resides in the top 1K of address range



GA Model 3381 5" rack mounted CRT used as system console for GA-16/220 pictured with 16K X 18-bit RAM

– (at 31K in the 32K mode and at 63K in the 64K mode). While that area is unavailable for applications programs, (except for the RAM space mentioned above) all routines in the module are accessible to the user's program.

TYPICAL SYSTEM CONSOLE FUNCTIONS



REMOTE MONITOR AND CONTROL

In many applications, the OEM designer needs to incorporate certain microcomputer display and control functions into his product console. To facilitate this, many CPU signals are available at the edge connector on the microcomputer board; for example:

RUN*	Run
SFEC*	System Safe
CLDS*	Cold Start
RSET*	System Reset
PRRT	Processor Reset
IPLSW	Autoload
SYNC	Synch pulse for external device (such as a scope) triggered by SYNC instruction – also 50 nsec, 10 μsec and 1 mse pulse trains for system synch.

In addition to using these unique lines, the OEM's console can be placed on the I/O bus as a peripheral, providing full access to the registers and memory of the microcomputer.

In the GA-16/220, the System Console Interface Module and the serial I/O port provide additional flexibility for remotely monitoring and controlling the microcomputer from an OEM product console, or from a host computer.

*In GA's microcomputer chassis, these signals are carried through to convenient paddle-board connectors on the rear of the Master Interconnect Board.

INITIAL PROGRAM LOAD (IPL)

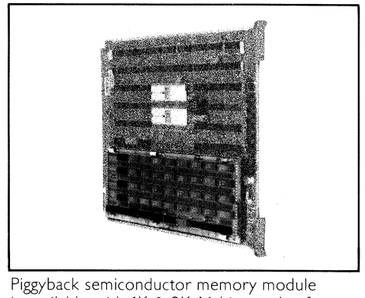
Several optional autoload PROM's are offered:

1. For the GA-16/220 – a combined 256-word PROM for TTY/PTR/CR/Floppy disk/Moving head disk/Head-per-track disk. This IPL PROM mounts on the System Console Interface Module which contains a small switch to select the desired autoload routine. Autoload is initiated remotely by an IPL signal, also by Reset or Power-up signals with the Cold Start Line grounded. Locally, IPL is initiated via the Microconsole IPL pushbutton or the Reset pushbutton with Cold Start grounded. The IPL PROM routines are bootstrap loaders, so the first block of data which the user puts on his autoload media is the standard GA PGS Loader, which the IPL PROM loads into RAM. The PGS Loader then proceeds to load the full program.
   PGS format is the normal object output of GA's CAP-16 Macro-assembler, FSOS, DBOS, RTOS, and Control I and Control III Operating Systems. It provides several features not found in other microcomputer software; for example, it is relocatable with selectable start address; it performs checksumming to insure correct loading; and it loads-and-goes or loads-and-stops.
2. For the GA-16/110 and GA-16/220 – single-device IPL PROM's for either TTY or PTR. These mount on the 1K and 2K piggyback RAM boards and, therefore, are most suitable for small dedicated systems. (They may not be used in GA-16/220's with the multi-device IPL PROM described above). They contain a 64-word modified PGS loader which loads absolute format with checksumming, selectable start address, and load-and-go. The PROM contains the complete loader so that no memory is consumed by the IPL routine itself.
   In both the GA-16/110 and GA-16/220, these IPL's are initiated remotely by a Reset signal or locally by the Reset pushbutton, in both cases with the Cold Start Line grounded. These PROM's reside at the 2K or 10K locations depending on whether the piggyback RAM is jumpered to start at zero or 8K.

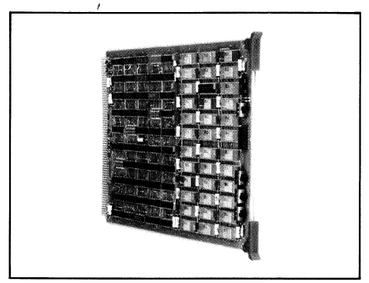
MEMORY

The asynchronous memory bus is organized for fast program execution and simple memory expansion. For more reliable data transfer it uses tristate drivers to isolate the bus from inactive memory modules. Bi-directional data transfers are 16 bits parallel. Sixteen parallel address lines are also provided for the full range of 64K words of direct addressability.

Small GA-16/110 and GA-16/220 systems are configured with piggyback memory modules which plug onto the GA-16/110 processor board. There are two types of piggyback memory. One is static RAM with 1K or 2K words plus positions for 64 words of IPL PROM. This is for simple applications with small programs which cannot be committed to PROM. The second configuration is 3K words of EPROM, plus 1K words of RAM working storage. This fits the requirements of many small dedicated systems where the application program can be fixed in EPROM and only a small RAM area is required for variable data. (Parity is not available on piggyback memories).



Piggyback semiconductor memory module is available with 1K & 2K 16-bit words of RAM – or 2K PROM combined with 0.5K words of RAM.



Large systems are configured with plug-in memories as this 8K X 18-bit module with byte parity.

For larger systems, memory is expanded with plug-in modules (7¾" X 11") containing 4K or 8K words of dynamic semiconductor RAM. These are available in a 16-bit version and an 18-bit version with byte parity. Refresh of dynamic RAM is performed automatically by the memory system, requiring no attention from the user's program or the CPU. Refresh imposes essentially no delay on program execution. A 22-bit 8K memory module will be available for later delivery. It automatically corrects all single-bit memory errors and detects all dual-bit errors.

An optional plug-in battery power supply is available to sustain semiconductor memory when AC power is off.

For customers who require other mixes of RAM, ROM, PROM, the piggyback and plug-in memories can be configured to suit their particular systems.

Refer to the Memory Data Sheet for more details.

PUSH-POP STACKS

Push-pop stacks operate with exceptional efficiency using special stack instructions, SARS and LARS. These eliminate the necessity of storing registers individually to save machine context when branching to subroutines and servicing interrupts.

One instruction does it all. SARS, for example, is a multi-function instruction which stores – or pushes – all registers and status onto the stack in a single, fast, microcoded sequence. Auto-increment functions are integrated into the SARS microcode, simplifying programming and accelerating stack operations. LARS is a similar instruction which automatically loads – or pops – all registers and status, restoring machine context in a short sequence of microcycles.

As a result, the microcomputers enter and exit from subroutines and interrupt routines with greater efficiency than microcomputers which push and pop registers individually.

As an option the CONTROL operating system implements the GA-16/440 dual protected stack system. This is a very powerful feature, unique among microcomputers. It is described under "Extended Instructions" on page 18.

INPUT/OUTPUT

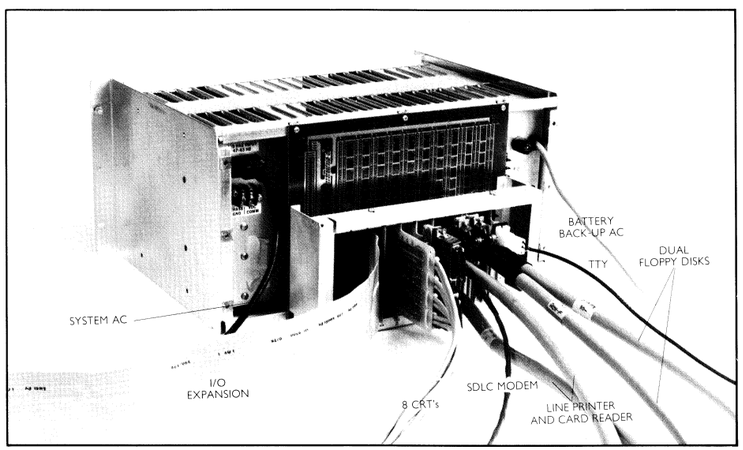
One of the principal benefits of the GA-16/110 and GA-16/220 is their I/O compatibility with GA's other 16-bit computers – SPC-16, GA-16/440, and GA-16/330.

For example, more than 100 standard I/O controllers for GA's larger minicomputers also run on the GA-16/110/220. With off-the-shelf delivery, they are supported not only by machine level drivers but also by GA's standard high level I/O System software package (IOS). IOS provides device-independent I/O and a degree of I/O flexibility unique among microcomputers.

The GA-16/110 and GA-16/220 provide four distinct types of I/O: Programmed I/O, Direct Memory Access, Direct Memory Transfer and Serial I/O. One of the principal differences between the GA-16/110 and GA-16/220 is the fact that the GA-16/110 provides two of these I/O paths while the GA-16/220 provides all four.

Programmed I/O (GA-16/110 and GA-16/220)

This is a parallel asynchronous bus. Under CPU control, 16-bit parallel transfers take place at rates up to 120K words per second. "Register" I/O instructions transfer between peripheral devices and any of the eight working registers while "memory" I/O instructions operate directly between I/O devices and any memory location. Bus length may be up to 50 feet. All device controllers on the bus may participate in the priority chain, those closest to the CPU having highest priority. Devices interrupt at random for service, or the program may test devices periodically to determine if they are ready for service. The programmed I/O bus is generally regarded as the "workhorse" bus of the micro-computers and, because of its simplicity, most interfaces designed by users are placed on this bus.



Rear view of compact GA-16/220 showing positive retention feature for I/O cables.

Interleaved DMA (GA-16/220 only)

The second CPU board interfaces the I/O bus to the memory bus. By implementing additional I/O and memory control signals it expands the I/O bus to operate directly with memory. This duplicates GA-16/440 and SPC-16 DMA so that all DMA controllers for GA's largest mini-computers run on the GA-16/220. Nominal DMA transfer rate is 900K words per second. Maximum DMA bus length is 25 feet.

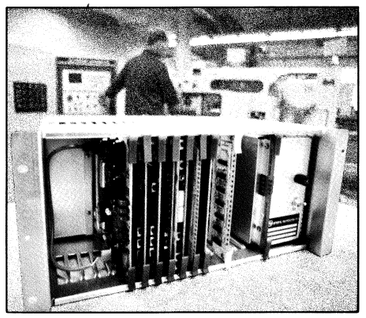
Many of GA's DMA controllers operate through an 8-Channel DMA multiplexer which performs inde-pendent DMA housekeeping functions for 8 different devices. Other device controllers have self-contained DMA logic and operate directly on the I/O bus. DMA con-trollers participate in the standard I/O priority interrupt chain, generally having highest priority.

The GA-16/220 DMA is an inter-leaved process, with CPU operations and DMA transfers running simul-taneously. The CPU and DMA devices contend for the Memory Bus in a similar manner, with the CPU having a lower priority (which is optimum for its memory access requirements). DMA devices can gain command of the memory bus virtually any time the CPU is not on the bus fetching instructions or transferring data. The CROM and RALU are not involved in memory bus management; therefore, when they complete a fetch, the memory bus can be allocated immediately to a DMA device without stopping execution within the LSI CPU chips.

DMA transfers and instruction execution proceed in parallel. Instructions which execute in registers (arithmetic, logical, shift, control) will always run to completion. Instructions which require subsequent memory access by the CPU may, or may not, be extended in order to complete the DMA transfer.

Overall interleaved performance is a function of factors such as instruction mix in a program and when, during each microcycle, DMA devices might request the memory bus and complete their DMA transfers. In some instances, as when a DMA device acquires the memory bus late in a microcycle, the CPU may be delayed one or more microcycles for completion of the DMA operation. However, in most instances, interleaved DMA and instruction execution will proceed simultaneously, totally transparent to the CPU, with no microcycles stolen from the CPU.

The net result is increased system performance with more efficient use of memory and I/O, higher DMA throughput and optimized program execution by the CPU.



16K compact GA-16/220 with dual axis servo controller, 16-bit digital inputs and outputs and control system console interface.

Serial I/O (GA-16/220 only)

The GA-16/220 board provides a 3-wire serial I/O controller for standard ASCII code with one start bit, two stop bits and no parity. Two data rates may be selected: 110 baud for TTY or 9600 baud for CRT. The serial I/O port is the interactive communication link between the System Console Interface Module and a TTY or CRT for full pro-grammer's console capabilities. The user's program also has full accesses to this serial controller for normal program I/O with TTY or CRT.

In addition, the serial I/O port may be used for 3-wire communications with a host computer for remote monitoring and control or remote program loading. Connection is via direct wire, dedicated modems or acoustic couplers since dial-up and answer-back provisions are not built into the GA-16/220's serial I/O controller.

Small adapter cards, which plug into the rear of the Compact or Jumbo Chassis, are available to connect to RS232 and current loop peripherals.

Special I/O Controllers

In addition to the wide selection of standard I/O controllers, GA has produced dozens of special I/O controllers for customer's particular needs – for example, a communica-tions line switch, video tape recorder, time code generator, flatbed plotter, graphic digitizer, IBM digital I/O Mux, and many more. These are available for use with the GA-16/110 and GA-16/220.

Ask your GA Salesman about your special requirements.

MEMORY PARITY AND PROTECT OPTION (220 only)

Parity With 18-bit memories the memory system generates and checks byte parity. The MPP option provides a means of dealing with parity errors by "capturing" the following information and generating a non-inhibitable interrupt for corrective action by the user's program.

☐ CPU or DMA generated parity error

☐ Address and content of memory location causing parity error

☐ Upper or lower byte caused parity error

Intentional parity errors can be produced by a special instruction for maintenance purposes.

Write Protect MPP provides a simple means to protect 1K segments of memory against overwriting by CPU or DMA store instructions. CPU and DMA protect maps are created by setting bits in two 64-bit registers on the MPP board. Write protect violations generate non-inhibitable interrupts and "capture" the following data in MPP status registers for corrective action.

☐ Violation caused by CPU or DMA

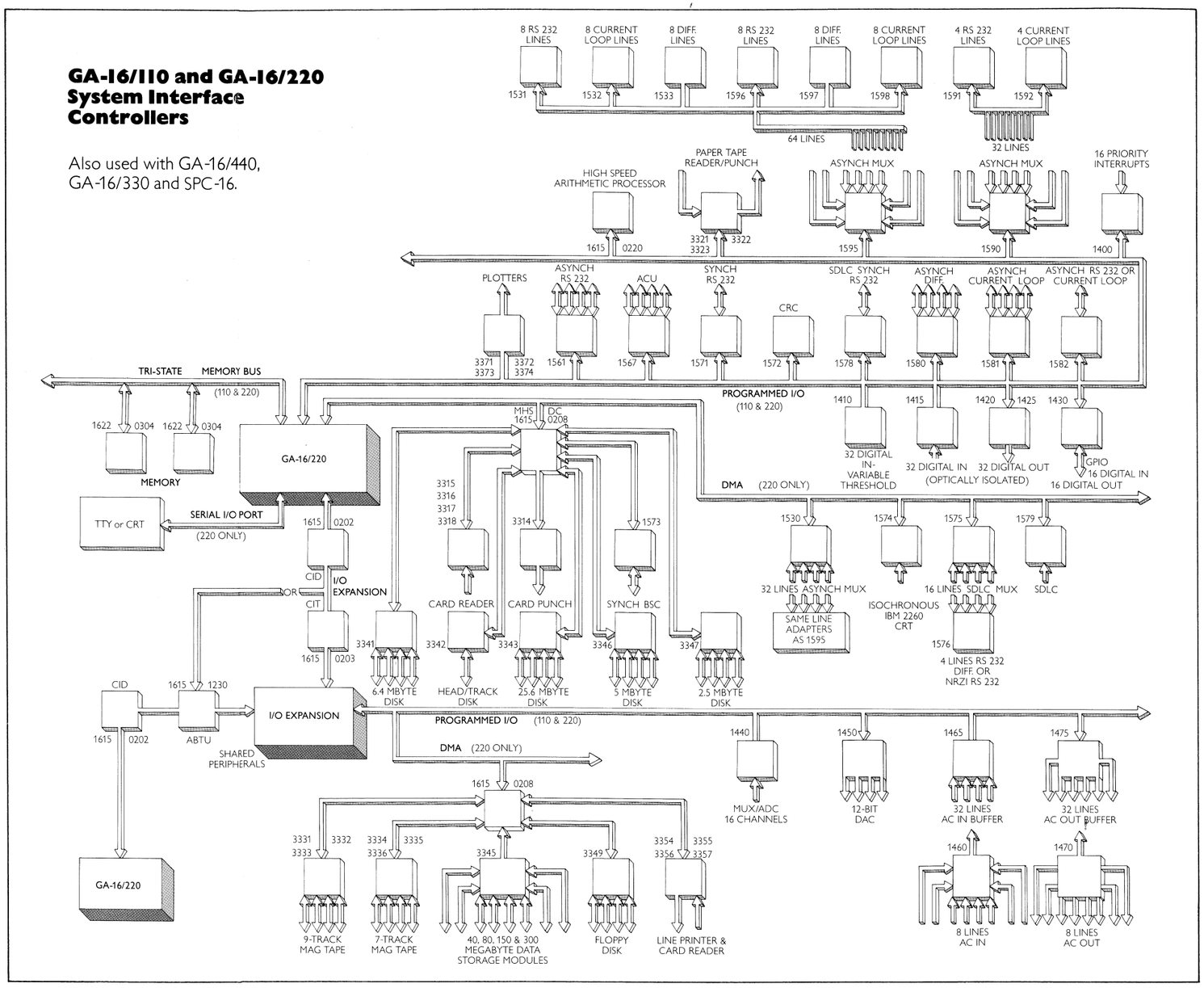
☐ Addresses of instruction and memory word causing violation.

Interrupt Program Time-out PTO permits the user to set a limit on the length of time the interrupt system may be inhibited (selectable by jumpers from 20 to 640 μsec). If a program or a system fault inhibits interrupts beyond the limit, a non-inhibitable interrupt is generated for corrective procedures.

All features on the MPP option can be independently enabled.

GA-16/110 and GA-16/220 System Interface Controllers

Also used with GA-16/440, GA-16/330 and SPC-16.



PACKAGING

To simplify OEM system packaging GA offers several chassis and power options. The Compact system offers the advantage of a completely self-contained package. The Jumbo system offers expanded memory and I/O capacity. Both chassis feature easy front access as well as positive-retention rear connectors for I/O cables and TTY/CRT adapter. In addition, for large systems with a great deal of I/O, both the compact and jumbo chassis have provisions for plugging in the standard 18-slot I/O expansion chassis.

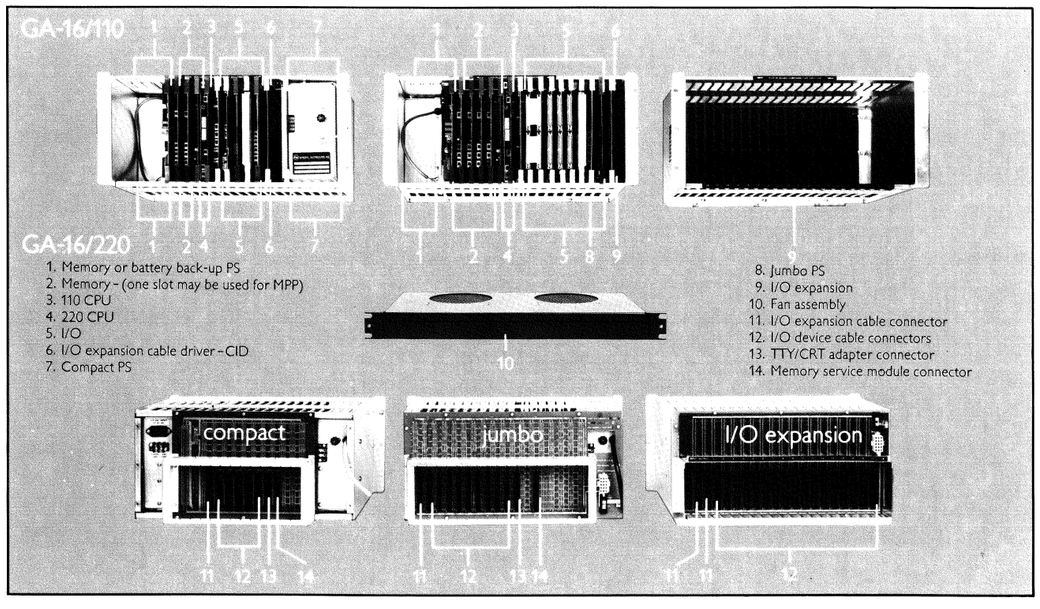
CHASSIS CAPACITY

	COMPACT		JUMBO	
1. Memory (16 bit words)	110	220	110	220
a. Maximum	32K	24K	56K	48K
b. With BUPS OR MPP	24K	16K	48K	40K
c. With BUPS AND MPP	16K	8K	40K	32K
2. I/O Slots	5	5	8	8
3. I/O Expansion Slot	1	1	1	1

The plug-in compact power supply, a switching regulator type, provides up to 18 amps of +5V; the jumbo supply provides up to 30 amps. Both supplies provide power-fail and power-up signals to the CPU. The compact supply operates on 100-120VAC. A stepdown transformer is used for 220-240VAC. The jumbo supply has standard transformer taps for nominal voltages of 100, 110, 200 and 240VAC.

The back-up power supply performs the dual functions of providing +12VDC and −5VDC to the dynamic semiconductor RAM and providing standby power to RAM when AC is off. Since it plugs into AC it sustains memory indefinitely when main system power is turned off, and its 1.5 amp hour battery sustains 8K RAM for 1 hour (16K, ½ hour) when AC is lost.

The memory service module is an alternate, low-cost means of supplying +12VDC and −5VDC to dynamic semiconductor RAM in systems which do not require standby battery back-up. It is a small printed circuit card which plugs into a connector on the back of the compact and jumbo chassis.



SOFTWARE

The GA-16/110 and GA-16/220 are supported by the same software which supports GA's larger mini-computers, the GA-16/440, GA-16/330 and SPC-16. Thus, General Automation's micro-computer software embodies these big-computer concepts:

Programs are re-entrant and recursive. These techniques operate with exceptional efficiency, using dynamic storage allocation and base relative addressing.

Programs are I/O device independent. Programs written in any of GA's programming languages may make requests to I/O devices and files through a set of modular calling sequences which are device independent.

Programs are relocatable. Object programs, translated and linked, may be loaded and executed anywhere in memory.

Programming languages and software are compatible. FORTRAN, Commercial FORTRAN and COBOL modules may be linked with assembly language subroutines to form a single program.

When used according to GA's standard programming rules, all of the software discussed below is source compatible. Different versions exist for the new GA-16 computers and the SPC-16 in order to produce appropriate executable code for the particular computer to be used.

PROGRAM GENERATION TOOLS

CAP-16 Macro Assembler A symbolic assembler with macro capability for programming with machine-level mnemonics and user-defined labels

FORTRAN IV ANSI Standard X3.9-1968 with extensions for in-line assembly language, bit and byte arrays, logical expressions, rational expressions, labeled and unlabeled COMMON, encode/decode statements, free format I/O and subscripts of any legal integer expression

Commercial FORTRAN Combines FORTRAN IV with elements of BASIC and COBOL for business and computational applications

COBOL ANSI Standard X3.23-1974 Level One, with numerous extensions from Level Two, for business data processing

BASIC Single-user operations with Assembly Language or FORTRAN subroutines callable from BASIC

Core Load Overlay Builder Links main programs and subroutines for loading and execution by operating systems with sophisticated disk overlay capabilities. Produces either relocatable or absolute object programs with check summing which can be loaded at designated addresses

Dynamic Debug For interactive debugging of user-written programs

Text Editor For flexible entry, modification and output of source text

Concordance Provides symbol cross reference tables for program documentation and debugging

Utilities Interactive routines to load and punch, display and alter memory and registers, trap, step, search memory for value, fill memory with value, hex add and subtract, relocate programs, display block of memory

Hardware Diagnostics Routines to determine if hardware elements are functioning correctly

OPERATING SYSTEMS

Two series of operating systems run on the GA-16/220: CONTROL I, II, III designed for the GA-16 Series and FSOS, DBOS, RTX, RTOS designed for the SPC-16.

FSOS-16/440, FSOS-16 Program generation and execution on minimal hardware configuration – principally for TTY-based systems without high-speed bulk storage

CONTROL I, DBOS-16 Disk-based batch processing for program generation and data processing

CONTROL II, RTX-16 Memory-resident, real-time operations with priority scheduling of up to 255 separate programs

CONTROL III, RTOS-16 Disk-based, real-time, multi-programmed operations in the foreground with batch processing in background. Automatic overlay and roll-out of programs to disk, with dynamic memory allocation. CONTROL I and II are modular subsets of CONTROL III.

CONTROL operating systems utilize the full GA-16/440 instruction set, including new stack and argument transfer instructions. The standard GA-16/220 runs under CONTROL with these nonimplemented instructions simulated by the operating systems.

SPC-16 operating systems run without simulation on the GA-16/220 in the 32K mode with the standard microcomputer instruction set.

SUBSYSTEMS

I/O System Provides device-independent I/O by linking programs to actual I/O devices and files via logical I/O units

FMS A modular file management system for creating and manipulating data bases. It includes the powerful ISAM extension with multiple keys for fast data access. It supports the broad range of disks up to 300 megabyte drives.

Overlay Manager For run-time management of disk overlays, automatically loading program sections from disk as needed

Output Spooler For automatic disk buffering of low speed peripherals to achieve higher system throughput

SORT Used with COBOL to create sorted records in ascending or descending order on the basis of multi-level key fields

SOFTWARE APPLICABILITY

Since the GA-16/110 is a low-cost, high performance worker computer for dedicated applications, its design is optimized for "load-and-go" execution of user's programs. Application programs for the GA-16/110 are developed on any GA-16/440/330/220 or SPC-16, using all of the software tools described above. Application programs are placed in EPROM or are autoloaded into RAM for execution by the GA-16/110.

The GA-16/220 directly runs the complete array of GA Software. Thus, it functions not only as an economical, high-performance micro-computer in small OEM systems but it also operates as a powerful, high-level programming tool and performs large-computer tasks under sophisticated operating systems – but still at microcomputer prices.

GA's microcomputers are supported by the most complete software in the industry.

SPECIAL INSTRUCTIONS

The standard instruction set in the GA-16/110 and GA-16/220 includes a number of unique instructions which save time in program development, conserve memory and accelerate program execution. For example,

☐ Bit instructions which test, set or reset any bit in memory – valuable for setting flags and for monitoring and controlling "on-off" functions such as switches, relays, valves, and indicators

☐ Byte instructions which load or store any byte in memory or swap bytes in a register – valuable in data communications and EDP

☐ Register-to-register and memory-to-register instructions for fast arithmetic and logic operations

☐ Compare instruction for efficient memory search – valuable in table look-up

☐ Execute instruction which causes any register to execute as the instruction register

☐ Jump-to-subroutine instruction and return via the address stored in the E register. This method of return via a hardware register decreases subroutine and interrupt overhead. Using a register also permits subroutines to be executed in ROM.

☐ Load/save-all-registers and status – single instructions which speed execution and greatly simplify coding of re-entrant interrupt routines and subroutines

☐ I/O instructions which move programmed I/O data directly to and from memory

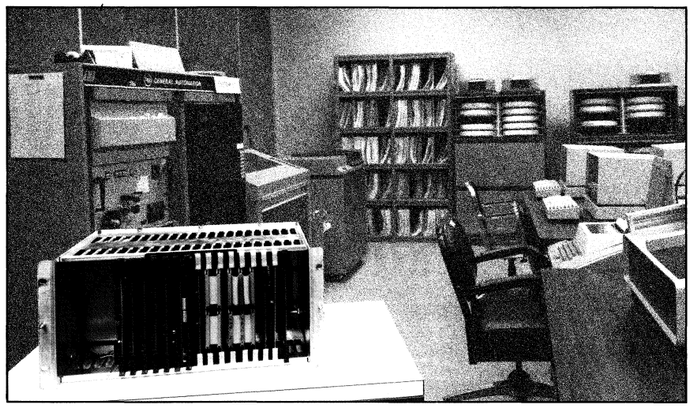
☐ Multiply/divide instructions which perform these functions 5 times faster than software routines

EXTENDED INSTRUCTIONS

The CONTROL operating system extends the microcomputer instruction set to the full GA-16/440 repertoire. This adds 3 argument transfer instructions and 22 stack instructions.

Argument transfer instructions facilitate the movement of arguments (or parameters) from a program to a subroutine. The full addressing power of the GA-16 architecture is applied to these functions; base relative, indexed, and indirect argument addresses are passed to subroutines and resolved by these instructions to 16-bit absolute addresses for fast argument accessing. A single instruction resolves any number of argument addresses, storing the results in the stack for use by the subroutine as needed. This is especially significant in programs with frequent parameter transfers (such as FORTRAN or data collection with scaling and conversion).

Dual stacks are implemented by the extended instructions with overflow and underflow protection on all stack operations, regardless of stack placement in memory. The stack instructions provide complete subroutine and interrupt routine entry and exit sequences, fully supported by CONTROL operating systems and all languages. Typical functions include saving and restoring of CPU context, management of working storage areas in the stack, base register loading, interrupt system control, argument transfer instruction interface, and return to calling or interrupted programs. In addition, other instructions allow programs to allocate/deallocate stack areas and to push/pop individual registers and register pairs. These capabilities let a program dynamically assign temporary storage as needed, eliminating the need to dedicate large areas of memory for stack operations.



A powerful data processing computer. Jumbo GA-16/220 with byte parity and memory write protect – plus controllers for quad 25-megabyte disks, magtape, 1000 cpm card reader, 600 lpm printer, dual CRT's and ASR 35.

An unlimited number of stacks can reside in main memory with two of them operational at any moment. Typically, one stack is used by the operating system and the other by the application program.

The operating system has access to all stacks simply by placing new stack addresses in the current stack pointers. Each operational stack has its own stack pointer, its individual upper and lower limit detectors, as well as its stack fault vector which points to the user's diagnostic and recovery program.

With this arrangement of dual protected stacks, the GA-16/220 provides a more advanced push/pop stack system than any other microcomputer.

SPECIFICATIONS

Architecture

Microprogrammed, 16-bit general purpose microcomputers

All registers and buses 16-bit parallel

Parallel binary two's complement arithmetic

64K direct addressability

Single and double word addressing

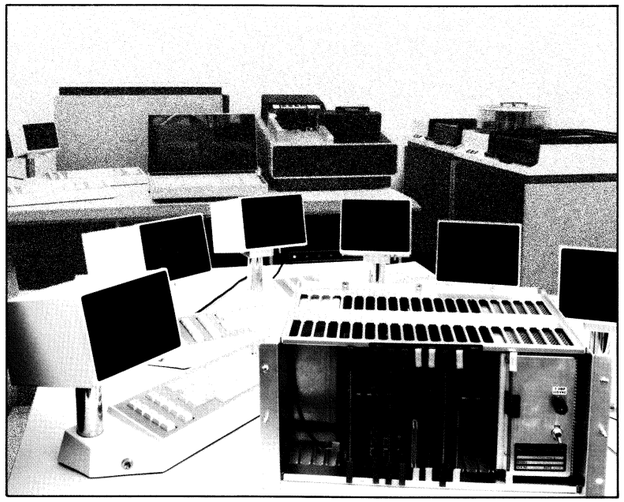
Software and I/O compatible with GA-16 Series and SPC-16

Technology

Processor – LSI n-Channel MOS

Memory RAM – n MOS
PROM – bipolar

Four-layer PC boards



A high-capacity cluster controller. Compact GA-16/110 with 16K RAM and down-loading PROM, battery back-up and multiplexed asynchronous controllers for 16 serial devices such as CRT's, printers and magnetic card readers – also SDLC link to large host computer.

Semiconductor Memory

Expandable to 64K 16-bit words

Plug-in dynamic RAM
4K and 8K X 16-bit/18-bit/22-bit
Byte parity and error correction
Transparent on-board refresh

Piggyback PROM
2K PROM + 512 RAM

Piggyback RAM
1K and 2K X 16-bit static RAM + 64 word autoload PROM

NI interrupts

Powerfail

Auto Restart

TTY Break

Memory Parity and Protect (Option)

Interrupt Program Time Out (Option)

Non-implemented Op code

I/O interrupts

Real Time Clock

TTY ready

Operator interrupt

External I/O (Unlimited number)

Input/Output

Programmed I/O bus (GA-16/110 and GA-16/220)

Parallel lines for address, data in, data out and control

50′ maximum length

Priority chain

GA software supports 64 devices

120K word/sec transfer rate

Transfers – To/from memory
– To/from any of 16 registers

Compatible with all SPC-16 programmed I/O controllers

DMA Channel (GA-16/220 only)

Parallel lines for address, data in, data out and control

25′ maximum length

Priority chain for multidevices

Interleaved with CPU

900K words/sec transfer rate

Compatible with all SPC-16 DMA controllers

Serial I/O Port (GA-16/220 only)

3 wire, ASCII, 1 start, 2 stop, no parity bits

UART interface at 110 baud for TTY and 9600 baud for CRT

Adapters for 60V, 20 ma current loop and RS232

Dimensions

All plug-in boards
19.7cm X 28.0cm
7¾″ X 11″ – 140 pin connector

Compact, jumbo and I/O expansion chassis
22.2cm X 48.3cm X 38.9cm
8.75″ X 19″ X 15.3″

Jumbo system power supply
27.8cm X 25.4cm X 14.6cm
10.57″ X 10″ X 5.75″

DC Power

Compact PS	18A at + 5V
PS 115VAC,	3.0A at +15V
47-63Hz,	2.0A at −15V

Requires transformer for other primary voltages

Jumbo PS	30A at + 5V
115 or 220VAC,	5A at +15V
47-63Hz	5A at −15V

Battery backup PS – 1.5 amp hour battery, plugs into 115VAC or 220VAC, 47-63Hz

Provides ±5VDC and +12VDC to memory.
Connector for large external battery
Memory Retention:
Normal shutdown – Indefinite
Loss of AC – Approximately one hour with 8K, ½ hour with 16K

Environmental

Temperature	0°C-50°C
Humidity	90% non-condensing

INSTRUCTION SET

The GA-16/110 and GA-16/220 have an enhanced SPC-16 instruction set - 91 **basic** instructions (with approximately 2100 variants) specifically designed for data acquisition, communications, processing and control. Their standard instruction set listed below is a subset of the GA-16/440.

OP Code	Description	Instruction Execution (µs)
MEMORY REFERENCE*		
LDA	Load Register A	2.70
STA	Store Register A	3.00
JMP	Jump Unconditionally	1.60
JSR	Jump to Subroutine	2.10
MEMORY REFERENCE WITH INDEXING*		
LDR	Load Register	2.70
STR	Store Register	3.00
CMR	Compare Memory w/Register	3.70
LDBY	Load Byte	3.70
STBY	Store Byte	3.60
LARS	Load All Registers & Status	12.00
SARS	Store All Registers & Status	15.10
INCM	Increment Memory	4.10
DECM	Decrement Memory	4.10
SBIT	Set Bit n	4.10
RBIT	Reset Bit n	4.10
TBIT	Test Bit n	4.10
SKIP		
SKZ	Skip if Zero	2.10
SKN	Skip if Non Zero	2.10
SKP	Skip if Plus	2.10
SKM	Skip if Minus	2.10
SKOT	Skip on Overflow True	2.60
SKOF	Skip on Overflow False	2.60
SKS	Skip on Link Set	2.10
SKR	Skip on Link Reset	2.10

OP Code	Description	Instruction Execution (µs)
REGISTER CHANGE		
ZERO	Zero Register	2.60
XEC	Execute Register Contents	2.10
TRS	Transfer Register to Status	2.60
TSR	Transfer Status to Register	2.60
ZLBY	Zero Left Byte	2.60
ZRBY	Zero Right Byte	2.60
EXBY	Exchange Bytes	2.60
RTRN	Subroutine Return	2.60
RISE	Restore Interrupt System Enable	2.60
EXIT	Subroutine Return	2.60
RLK	Add Link to Register	3.10
INCR	Increment Register	2.60
DECR	Decrement Register	2.60
CMPL	Complement Register	3.10
ADDS	Add Shift Counter to Register	3.60
RCSM**	Read Console Switches to Memory	4.50
RCSR**	Read Console Switches to Register	3.10
SHIFTS		
SRA	Shift Right Arithmetic	3.10 +1.0 N
SRC	Shift Right Circular	3.10 +1.0 N
SRLC	Shift Right Logical & Count	3.10 +1.0 N
SRCL	Shift Right Circular Thru Link	3.10 +1.0 N
SLC	Shift Left Circular	2.60
SLCL	Shift Left Circular Thru Link	3.10
SLZ	Shift Left Logical Insert Zeros	2.60
SLO	Shift Left Logical Insert Ones	2.60

OP Code	Description	Instruction Execution (µs)
INPUT/OUTPUT		
DTOR	Data Out From Register	2.60
DTIR	Data In To Register	3.10
DTOM	Data Out From Memory	3.20
DTIM	Data In To Memory	4.50
CTRL	Output Control Pulse	2.10
TEST	Test Device	2.60 (False) 3.10 (True)
MULTIPLY/DIVIDE		
MPY	Multiply	3.60 + 1.5 N + .5 N per "1" bit
DIV	Divide	3.60 + 2.0 N
REGISTER OPERATE		
RTR	Transfer Register	2.10
ADD	Add Registers	2.10
SUB	Sub Registers	2.10
AND	And Registers	2.10
XOR	Exclusive or Registers	2.10
REGISTER OPERATE COMPARE		
OR	Or Registers	2.10
ADDC	Add Registers & Compare	2.10
SUBC	Subtract Registers & Compare	2.10
ANDC	And Registers & Compare	2.10
XORC	Exclusive or Registers & Compare	2.10
ORC	Or Registers & Compare	2.10

see Programmer's Reference Manual for data regarding added times for various memory addressing modes.

**220 only

OP Code	Description	Instruction Execution (µs)
REGISTER OPERATE LITERAL		
LDV	Load Value Into Register	3.20
ADDV	Add Value to Register	3.20
SUBV	Subtract Value From Register	3.20
ANDV	AND Value w/Register	3.20
XORV	Exclusive OR Value w/Register	3.20
ORV	OR Value w/Register	3.20
RTNIV	Return From NI Interrupt	4.90
REGISTER OPERATE COMPARE LITERAL		
ADDVC	Add Value to Register & Compare	3.20
SUBVC	Subtract Value From Register & Compare	3.20
ADNVC	AND Value w/Register & Compare	3.20
XORVC	Exclusive OR w/Register & Compare	3.20
ORVC	OR Value w/Register & Compare	3.20
CONTROL		
INE	Interrupt Enable	2.60
INH	Interrupt Inhibit	2.60
FMS	Foreground Mode Set	2.60
BMS	Background Mode Set	2.60
PMA	Pulse Monitor Alarm	2.60
LKS	Set Link	2.60
LKR	Reset Link	2.60
SYNC	General Sync Pulse	2.60
WAIT	Stop Instruction Execution	2.60
TRAP	Program Sequence Interrupt (Includes NI interrupt overhead)	8.95