ABSOLUTE BINARY PROGRAM NO. 24318-16001
DATE CODE 1431

I/O INSTRUCTIONS AND INTERRUPT DIAGNOSTIC

reference manual

For HP 2100 Series Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *HP 2000 Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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Introduction

The I/O Instructions and Interrupt Diagnostic tests the interrupt priority structure and the interrupt capability of any of the I/O select code slots. The secondary objective is to check the Central Interrupt Register (CIR), if present.

This diagnostic operates in any 2100 series computer with a minimum of 4K of memory. It is one of the HP 2000 computer system diagnostics executed in conjunction with the HP 2000 Computer Systems Diagnostic Configurator. Communication to the operator is provided through the teleprinter, if available, through the computer Memory Data Register (T-register), and the A- and B-registers. Operator input is made via the switch register and teleprinter, if available.

This diagnostic assumes that the following 2100 series diagnostics have been successfully executed:

Alter-skip Instruction Diagnostic

Memory Reference Instruction Diagnostic

Shift-rotate Instructions Diagnostic

Memory Diagnostic

GENERAL ENVIRONMENT

Hardware Requirements

1. The diagnostic can be run on any 2100 series computer with a minimum of 4K of memory.

2. A paper tape reader is required to load the program; the teleprinter paper tape reader can be used.

3. Standard flag and interrupt logic I/O interface cards are required for each I/O slot to be tested. Empty I/O slots between the highest and lowest priority interruptable interface cards must be filled with priority jumper cards.

The following is optional hardware:

4. System console teleprinter.

5. Either a Duplex Register card (8 bit, HP 12597 or 16 bit, HP 12554) or a Microcircuit card (HP 12566) are required for the optional I/O bus test. A special 24-pin test connector is also required (HP 1251-0332). If the Microcircuit card is used, pins 22 and 23 must be connected together on the 24-pin test connector. See Appendix A for full explanation of card jumper positions.

Software Requirements

The required software consists of the following binary object tapes:

1. HP 2000 Computer Systems Diagnostic Configurator (HP 24296)

2. I/O Instructions and Interrupt Diagnostic, part no. 24318-16001.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader* (HP 5951-1376).

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic Messages and Halts.

PREPARATION FOR DIAGNOSTIC RUN

Before the tests can be initiated, the user performs the following actions:

- Load the Diagnostic Configurator
- Configure to available system hardware
- Dump the configuration for later use (optional)
- Load the diagnostic
- Make the I/O and interrupt test hardware ready

Loading

Using the Binary Loader, load the Diagnostic Configurator. Perform the configuration procedure (see "Configuring" below) before loading the diagnostic. Then, load the I/O Instructions and Interrupt Diagnostic using the Configurator. The user may insure that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number = 101003_8.

Configuring

Procedures for inputting the system hardware configuration parameters are found in the *HP 2000 Computer Systems Diagnostic Configurator* manual under "CONFIGURING."

The configuration procedure accepts six groups of parameters. This diagnostic requires only four groups to be defined. They are:

- Computer type and options
- Teleprinter as system input device
- Teleprinter as system output device
- Memory size and type

The other parameters may be left undefined (zero).

Computer Type and *Options* and *Memory Size* and *Type* vary from one 2100 Series installation to the other. The user must determine the parameters of his installation and configure accordingly.

A teleprinter may be configured optionally as the *Slow System Input* and *Output* device to serve as operator/diagnostic communicator. If no teleprinter is available, configuration input is zero. The user must then rely on Halt codes and the switch register to monitor and control test sequence and determine degree of test success.

Dumping

Using procedures described in the Diagnostic Configurator manual, the user may dump memory onto paper tape so that the above configuration procedures need not be repeated. The dumped paper tape can thereafter be loaded via the Binary Loader.

Making Test Hardware Ready

- Install I/O Interface cards in the I/O slots to be tested. Insure that I/O slots that are not to be tested between the highest and lowest priority interruptable interface cards are filled with Priority Jumper cards.
- If the optional I/O Bus test is to be run, install either the proper eight or sixteen bit Duplex Register card or a microcircuit card, after verifying card jumpers are installed according to one of the settings shown in Appendix A.
- Install the appropriate Special Test Connector.

RUNNING THE DIAGNOSTIC

Starting Up

a. *Initiate Execution*

ACTION	EXPLANATORY INFORMATION
Set switch register for tests and options desired. Set P-register to 100_8. Press PRESET (EXTERNAL & INTERNAL, if applicable) Press RUN.	Table 1 holds summary of switch register options. Bits 0 through 5 (I/O slot select code) may be left clear until later.

Result: Halt with MDR = 107000_8 indicates that no teleprinter was configured. Use procedure b. below for I/O slot select code entry via switch register.

The message

2100 SERIES INTERRUPT TEST
ENTER SELECT CODES-

is printed with teleprinter-configured test. Follow procedure c. below for I/O slot select code (SC) entry via the teleprinter.

Table 1. Switch Register Options

Bit	Function If Set
0-5	Hold select code of I/O slots to be tested (Used only when TTY not available.)
6	Select Switch Register Test
7	Select I/O Bus Test
8	Reserved
9	Enter new select code(s) to be tested
10	Suppress End of Pass Message
11	Suppress Error Messages
12	Loop on diagnostic. Clear to HALT 102077_8 at end of pass. A-register = pass count
13	Reserved
14	Suppress Error HALT's
15	Indicates 8-bit Duplex card for I/O Bus test.

b. *Switch Register Select Code Entry*

ACTION	EXPLANATORY INFORMATION
Set switch register bits 0 through 5 to the first I/O slot select code of the list to be tested. Press RUN.	These select codes (SC) may be entered in any order. They must have octal values $10 \leqslant SC \leqslant 77$. An SC=0 signals end of test select code entry. Note that switch options already set in bits six through fifteen should not be disturbed.

Result: Halt with MDR = 107001_8 indicates valid SC entry. Halt with MDR = 107000_8 indicates invalid or duplicated SC. SC entry procedure must be repeated from entry of first SC.

ACTION	EXPLANATORY INFORMATION
Repeat SC entry for each one required, pressing RUN after each. Enter SC=0_8 to signal completion of SC entry.	

Result: Halt with MDR = 102074_8 indicates successful SC entry sequence.

Press RUN.	This initiates execution of diagnostic tests. See Diagnostic Execution, below.

c. *Teleprinter Select Code Entry*

ACTION	EXPLANATORY INFORMATION
Type in SC's of all I/O slots to be tested.	Each SC is specified by a pair of octal digits in the range $10_8 \leqslant SC \leqslant 77_8$. Up to 72 characters can appear in an input line. Each line must be terminated by a CARRIAGE RETURN & LINE FEED. Spaces and commas may be inserted freely (they are ignored). SC's do not have to be in any order. SC=0 followed by CARRIAGE RETURN & LINE FEED signals end of input.

Result: Successful entry of SC's initiates execution of diagnostic tests. See Diagnostic Execution, below.

Error on SC input (i.e., SC's out of range, illegal characters, or duplicate SC's) causes the message

? TRY AGAIN-

to be printed. The SC input sequence must be repeated from the beginning.

Diagnostic Execution

Upon completion of Starting Up Procedures, the actual tests are initiated. Basic Interrupt and Interrupt Priority tests execute automatically and the length of time required is 2 to 5 seconds.

If the I/O Bus Test is selected, the special procedure a. is followed to define the interface select code the first time this test is executed. Thereafter, the test will execute with the specified SC unless change is specified via switch register bit 7.

a. *I/O Bus Test Procedure*

ACTION	EXPLANATORY INFORMATION
Select I/O Bus Test via program option switch 7 during test start up.	

Result: Halt with MDR = 102041_8.

ACTION	EXPLANATORY INFORMATION
Enter test card select code into switch register bits 0 through 5.	
Set bit 15 of switch register, if an eight bit Duplex Register Card is used.	Leave switch 15 clear if 16 bit interface used.

ACTION	EXPLANATORY INFORMATION
Press RUN.	

Result: I/O Bus test executes and then diagnostic proceeds to next selected test.

The Overflow Test executes automatically, if selected. The Switch Register test requires the following special procedure, if selected.

b. *Switch Register Test Procedure*

ACTION	EXPLANATORY INFORMATION
Select Switch Register Test via program option switch 7 during test start up (see Table 1).	

Result: HALT with MDR = 102051_8. Overflow lamp should be on; if not, it is in error.

ACTION	EXPLANATORY INFORMATION
Set 052525_8 into switch register. Press PRESET (INTERNAL PRESET, if applicable). Press RUN.	This is a test code of alternating 1's and 0's.

Result: Halt with MDR = 102057_8. Overflow lamp should *not* be on; if it is, it is in error.

ACTION	EXPLANATORY INFORMATION
Set 125252_8 into switch register. Press PRESET (INTERNAL PRESET, if applicable). Press RUN.	This test code is complement of first test code.

Result: Diagnostic execution proceeds with next selected test.

DIAGNOSTIC MESSAGES AND HALTS

The diagnostic communicates to the operator by teleprinter, HALTS, or both, based on configuration and switch register settings. Thus, messages consist of both HALT codes (MDR, A- and B-register values) and teleprinter text. Table 2 lists the Halt codes, text and meanings of diagnostic messages.

Table 2. Program Halts and Messages

Octal HALT Codes	Message	Meaning
—	2100 SERIES INTERRUPT TEST	Introductory Message.
107000	—	Begin entry of I/O slot SC's via switch register (this HALT occurs if an error was made in SC entry; signals restart of SC entry); press RUN.
107001	—	Enter next SC by switch register; press RUN.
102074	—	I/O slot SC entry completed; press RUN to continue.
1030*xx*	—	Unexpected interrupt occurred for SC=*xx*, when interrupt system was off. Unrecoverable: do not continue test.
1060*xx*	—	Unexpected interrupt occurred for SC=*xx*; interrupt system on/off state not determined. Unrecoverable: do not continue test.
102000	E-0 CLF SC-SFC SC	SFC did not skip after flag cleared by CLF; Interrupt System Off (ISO).
102001	E-1 CLF SC-SFS SC	SFS skipped after flag cleared by CLF; (ISO).
102002	E-2 STF SC-SFC SC	SFC skipped after flag set by STF; (ISO).
102003	E-3 STF SC-SFS SC	SFS did not skip after flag set by STF; (ISO).
102004	E-4 CLC SC-SFC SC	SFC skipped even though flag should still be set; CLC may have cleared flag.
102005 (A=*xx*)	E-5 NI SC-*xx*	No interrupt on SC=*xx*.
102006 (A=*xxxxxx* B=*yyyyyy*)	E-6 CIR=*xxxxxx* SB=*yyyyyy*	Central Interrupt Register (CIR) = *xxxxxx*; should be *yyyyyy*.
102007 (A=*xx*)	E-7 DI SC=*xx*	Double interrupt occurred for SC=*xx*.
102010 (A=*xx*)	E-10 NI SC=*xx*	No interrupt for SC=*xx*.

Table 2. Program Halts and Messages (Continued)

Octal HALT Codes	Message	Meaning
102011 (A=*xx* B=*yy*)	E-11 UI SC=*xx* SB*yy*	Unexpected interrupt for SC=*xx;* interrupt should be for SB=*yy*; Unrecoverable: do not continue test.
102012	E-12 INTERRUPT EXECUTION ERROR	Last instruction before interrupt did not execute properly.
102013	E-13 INTERRUPT RETURN ADDRESS ERROR	Interrupt occurred at wrong address in program.
102020	E-20 OVERFLOW ERROR; SEE MOD	Overflow not cleared by CLO, or SOS caused skip with overflow clear.
102021	E-21 OVERFLOW ERROR; SEE MOD	SOS did not skip with overflow clear.
102022	E-22 OVERFLOW ERROR; SEE MOD	STO did not set overflow, or SOC caused skip with overflow set.
102023	E-23 OVERFLOW ERROR; SEE MOD	SOS didn't skip with overflow set.
102024	E-24 OVERFLOW ERROR; SEE MOD	SOS C didn't skip because overflow cleared first.
102025	E-25 OVERFLOW ERROR; SEE MOD	SOS C didn't clear overflow.
102026	E-26 OVERFLOW ERROR; SEE MOD	SOC C skipped because overflow cleared first.
102027	E-27 OVERFLOW ERROR; SEE MOD	SOC C didn't clear overflow.
102030	E-30 OVERFLOW ERROR; SEE MOD	When A-077777, no overflow on ADA+1.
102031	E-31 OVERFLOW ERROR; SEE MOD	When B=000001, no overflow on ADB+ 077777.
102032	E-32 OVERFLOW ERROR; SEE MOD	When A=177777, no overflow on ADA- 100000.
102033	E-33 OVERFLOW ERROR; SEE MOD	When B=100000, no overflow on ADB- 177777.
102034	E-34 OVERFLOW ERROR; SEE MOD	When A=077777 no overflow on INA.
102035	E-35 OVERFLOW ERROR; SEE MOD	When B=077777, no overflow on INB.

Table 2. Program Halts and Messages (Continued)

Octal HALT Codes	Message	Meaning
102040 (A=*xxxxxx* B=*yyyyyy*)	E-40 I/O BUS DATA OUT=*xxxxxx* IN=*yyyyyy*	Data input not the same as output.
102041	–	Enter select code of test card into Switch register bits 0-5. (Set bit 15 if using an 8-bit Duplex Register.)
102050	–	LIA 0 failed.
102051 (OVERFLOW LAMP Should be On)	–	Set 052525_8 into switch register; Press PRESET (INTERNAL, if applicable), then RUN.
102052	–	SOS or PRESET (INTERNAL) failed (2100A or later CPU)
102053	–	LIA failed; unrecoverable failure, abort test.
102054 (A=*xxxxxx*)	–	MIA failed; A-reg. should be all ones, but is equal to *xxxxxx*.
102055	–	LIB failed.
102056 (B=*yyyyyy*)	–	MIB failed; B-reg. should be all ones, but is equal to *yyyyyy*.
102057 (OVERFLOW LAMP Should Be Off)	–	Set 125252_8 into switch register, Press RUN.
102060	–	SOC or CLO failed.
102061	–	LIA failed; unrecoverable failure, abort test.
102062 (A=*xxxxxx*)	–	MIA failed; A-reg. should be all ones, but is equal to *xxxxxx*.
102063	–	LIB failed.
102064 (B=*yyyyyy*)	–	MIB failed; B-reg. should be all ones, but is equal to *yyyyyy*.
102065	–	OTA failed or I/O Bus lines are incorrect.
102066	–	OTB failed or I/O Bus lines are incorrect.
102077 (A = *x*)	EOP *x*	End of pass through diagnostic; *x* holds pass count.

Test Sections

The Basic Tests, Interrupt Priority Test and Overflow Test are always executed. The I/O Bus Test and Switch Register Test are optionally selected via the switch register.

Following the last selected test, an end of pass message is printed (unless switch 10 is set) and an end of pass halt occurs (unless switch12 is set). A pass is 1 diagnostic cycle since the last input of slot parameters.

BASIC TESTS

Initially 5 tests are run to check the ability to clear, set, and test the interrupt system. These tests are repeated for all select codes entered to the I/O buffer.

INTERRUPT PRIORITY TEST

A check is made to insure that no interrupt occurs if the flags and control flip-flops of each given select code are set and the interrupt system is off. An unexpected interrupt here results in a halt with 1030*xx* (*xx* is the select code of the bad slot). The user should not continue if this happens. Each select code in the slot buffer is then checked individually.

The following checks are made:

1. that each slot interrupts
2. the contents of the Central Interrupt Register (if present) following the interrupt are correct
3. that a 2nd interrupt doesn't occur
4. that no unexpected interrupts occur
5. that the last instruction before the interrupt is executed
6. that the address at which interrupt occurs is correct

The failure of a slot to interrupt results in error E-5. Incorrect contents in the Central Interrupt Register results in error E-6. A double interrupt results in error E-7 and an irrecoverable halt. An unexpected interrupt results in a halt with 1060*xx* in the MDR; the user should not continue if this happens.

All select codes in the slot buffer are tested as a group. All given flag and control flip-flops are set and the interrupt system is turned on. The interrupts should occur in the order expected: lowest select code first, next lowest second, etc. Error E-10 results if an expected interrupt doesn't occur. An unexpected interrupt results in error E-11 and an irrecoverable halt.

OVERFLOW TEST

This test checks the ability to clear, set, and test the overflow bit. Also tested is the ability to cause an overflow from arithmetic instruction execution. Errors are reported by halts.

I/O BUS TEST

This program tests the sixteen data lines, and the control lines associated with an I/O location. The test requires that a duplex register card or microcircuit card with a 24-pin jumper connector attached be inserted in the I/O slot to be tested. (See Hardware Requirements section for full specification.)

The I/O data check first places self-addressed halts in each I/O location (000002_8 through 000077_8). The routine configures the I/O instructions required to drive the general purpose duplex register card or microcircuit interface card.

The program then outputs a set of data patterns to the slot under test. As each pattern is output, it is read back in and tested for correctness. Any errors encountered are reported by a message or by a halt with A,B containing expected and actual data.

SWITCH REGISTER TEST

This test will check the ability to execute the I/O instruction associated with the switch register of the computer type being tested. It assumes that the LIA 1 instruction works since the program would not execute correctly at all if it did not work. The execution of this test requires operator intervention and therefore may be run when operations dealing with the switch register are in doubt. Errors are reported by halts.

APPENDIX A
Jumper Installations For I/O Bus Test

The cards which may be used in the I/O Bus Test must have, during a run of the program, an allowed combination of circuit jumper positions installed. The combinations allowed are listed below, according to the type of interface board to be used.

HP 12554 16-Bit Duplex Register (Positive Logic)

Use Test Connector A which connects all output pins to adjacent input pins (Table 3). Any one of six different combinations is allowed:

Positions under Combination Number

Jumper Number	1	2	3	4	5	6
W4	B	B	A/B	A	A	A/B
W5	B	A	A/B	A	B	A/B
W6	A/B	A	C	A/B	A	C
W7	A	A	A	B	B	B

Note: Jumpers not listed may be installed in any position described in the Operating and Service Manual for this board.

HP 12554-01 16-Bit Duplex Register (Negative Logic)

Use Test Connector A (Table 3). Any one of six different combinations is allowed:

Positions under Combination Number

Jumper Number	1	2	3	4	5	6
W4	A/B	A	A/B	A/B	B	A/B
W5	A	A	A/B	B	A	A/B
W6	B	A	C	B	A	C
W7	B	B	B	A	A	A

Note: Jumpers not listed may be installed in any position described in the Operating and Service Manual for this board.

HP 12566 *Microcircuit Interface (Ground-true output)*

HP 12566-M1 *Microcircuit Interface (Ground-true output, party-line)*

HP 12566-M2 *Microcircuit Interface (Positive-true)*

Use test connector B (Table 4).

Any one of six different combinations is allowed:

Positions under Combination Number

Jumper Number	1	2	3	4	5	6
W1	B	A	A	A	B	B
W2	A	B	C	C	C	C
W3	A	B	B	B	A	A
W4	B	B	A	B	A	B

Note: Jumpers not listed may be installed in any position described in the Operating and Service Manual for these boards.

***HP** 12597 8-Bit Duplex Register (Positive Logic)*

Use test connector A (Table 3).

Only one combination is allowed:

W1	A	W7	connected
W2	A	W8	not connected
W3	connected	W9	not connected
W4	connected	W10	not connected
W5	connected	W11	not connected
W6	connected	W12	not connected

HP 12597-01 8-Bit Duplex Register (Negative Logic)

Use test connector A (Table 3). Only one combination is allowed:

W1	A	W7	not connected
W2	A	W8	not connected
W3	connected	W9	not connected
W4	connected	W10	connected
W5	not connected	W11	connected
W6	not connected	W12	connected

Table 3. Test Connector A Connections (HP 1251-0332)

From		To	
Pin No.	Signal	Pin No.	Signal
A	Output Bit 0	1	Input Bit 0
B	1	2	1
C	2	3	2
D	3	4	3
E	4	5	4
F	5	6	5
H	6	7	6
J	7	8	7
K	8	9	8
L	9	10	9
M	10	11	10
N	11	12	11
P	12	13	12
R	13	14	13
S	14	15	14
T	Output Bit 15	16	Input Bit 15
Z	Device Command	22	Device Command
AA	Device Flag	23	Device Flag
BB	Return Signal	24	Return Signal

Table 4. Test Connector B Connections (HP 1251-0332 with pin 22, 23 tied together)

From		To	
Pin No.	Signal	Pin No.	Signal
A	Output Bit 0	1	Input Bit 0
B	1	2	1
C	2	3	2
D	3	4	3
E	4	5	4
F	5	6	5
H	6	7	6
J	7	8	7
K	8	9	8
L	9	10	9
M	10	11	10
N	11	12	11
P	12	13	12
R	13	14	13
S	14	15	14
T	Output Bit 15	16	Input Bit 15
Z,22	Device Command	23,AA	Device Flag
BB,24	N/C (GROUND)		