

PAPER TAPE NO. 24319-16001

EXTENDED ARITHMETIC
INSTRUCTIONS DIAGNOSTIC

for

hp-2100 SERIES COMPUTERS

reference manual

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *HP 2000 Diagnostic Configurator Manual*, part no. 02100-90157, dated August 1976 or later.



HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

This document contains proprietary information which is protected by copyright. All rights are reserved. No part of this document may be photocopied, reproduced or translated to another program language without the prior written consent of Hewlett-Packard Company.

Contents

Section	Page
INTRODUCTION	
General Environment	1
Hardware Requirements	1
Software Requirements	2
OPERATING PROCEDURES	
Preparation for Diagnostic Run	3
Loading	3
Configuring	3
Dumping	4
Running the Diagnostic	4
Switch Register Settings	4
Diagnostic Execution	5
Diagnostic Messages and Halts	6
Error HALT Codes	6
Messages	7
Information Messages	7
Error Messages	8
TEST SECTIONS	
Test Sections	11
Number Generation	12
Indirect Addressing	12
E- and Overflow-Register Checking	12

Tables

Table	Title	Page
1	Switch Register Options	5
2	Memory Contents for Error Tests	6
3	Program HALTs	7
4	Information Messages	7
5	Error Messages	9

Extended Arithmetic Instructions Diagnostic

Introduction

The Extended Arithmetic Instructions Diagnostic performs a “Go/no-go” test of the instructions executed by the Extended Arithmetic Unit (EAU). This diagnostic operates in any 2100 series computer with a minimum of 4K of memory. It is one of the HP 2000 computer system diagnostics executed in conjunction with the HP 2000 Computer Systems Diagnostic Configurator. Communication to the operator is provided through the teleprinter (if available), through the computer Memory Data Register (T-register), and the A- and B-registers. The only operator input required is via the switch register.

The test method consists of executing instructions involving the EAU and then comparing the results to results obtained by non-EAU instruction simulation routines. This involves the use of many other CPU instructions and thus requires that they be fully tested first. Hence, this diagnostic should be run only after the following other CPU diagnostics have been successfully completed.

- Memory Reference Instruction Diagnostic
- Alter-skip Instruction Diagnostic
- Shift-rotate Instructions Diagnostic
- Teletype Diagnostic (optional)

GENERAL ENVIRONMENT

Hardware Requirements

1. The diagnostic can be run on any 2100 series computer with a minimum of 4k of memory.
2. A paper tape reader is required to load the program; a teleprinter paper tape reader can be used, if available.
3. A system console teleprinter is optional.
4. The Extended Arithmetic Unit (EAU) must be installed on the CPU.

Software Requirements

The required software consists of the following binary object tapes:

1. HP 2100 Series Diagnostic Configurator (HP 24296)
2. Extended Arithmetic Instructions, part no. 24319-16001.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader* (HP 5951-1376).

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic Messages and Halts.

PREPARATION FOR DIAGNOSTIC RUN

Before the tests can be initiated, the user performs the following actions:

- Load the Diagnostic Configurator
- Configure to available system hardware
- Load the diagnostic
- Dump the configuration for later use (optional)

Loading

Using the Binary Loader, load the Diagnostic Configurator. Perform the configuration procedure (see “Configuring” below), before loading the diagnostic. Then load the Extended Arithmetic Instructions Diagnostic using the Configurator. The user may ensure that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number 101004_8 .

Configuring

Procedures for inputting the system hardware configuration parameters are found in the *HP 2000 Computer Systems Diagnostic Configurator* manual (02100-90157) under “CONFIGURING.”

The configuration procedure accepts six groups of parameters. This diagnostic requires only four groups to be defined. They are:

- Computer type and options
- Teleprinter as system slow input device (optional)
- Teleprinter as system slow output device (optional)
- Memory size and type

The other parameters may be left undefined (zero).

Computer Type and Options and *Memory Size and Type* vary from one 2100 series installation to the other. The user must determine the parameters of his installation and configure accordingly.

A teleprinter may be configured optionally as the *Slow System Input Device* and *Output Device* to serve as operator/diagnostic communicator. If no teleprinter is available, configuration input is zero. The user must then rely on Halt codes and the switch register to monitor and control test sequence and determine the degree of test success.

Dumping

Using procedures described in the Diagnostic Configurator manual, the user may dump memory onto paper tape so that the above configuration procedures need not be repeated. The dumped paper tape holding the configured diagnostic can thereafter be loaded via the Binary Loader.

RUNNING THE DIAGNOSTIC

Switch Register Settings

Table 1 lists a summary of switch registers options.

Normally a random number generator produces new test arguments for each instruction test. *Switch 6* is used to suppress the random number generator allowing test to proceed with existing arguments.

Some instruction tests involve indirect addressing. *Switch 7* is used to suppress indirect addressing in these tests.

Table 1. Switch Register Options

Bits	Function
0-5	Reserved
6	Set ON to suppress the number generator at the beginning of each instruction test. Set OFF to generate new arguments for each execution of an instruction test.
7	Set ON to suppress the indirect addressing portions of the instruction tests.
8	Reserved.
9	Set ON to break out of any test which finds an error.
10	Set ON to suppress non-error messages.
11	Set ON to suppress error messages.
12	Clear to halt the program at the end of a pass. ($MDR = 102077_8$) Set ON to loop on diagnostic.
13	Set ON to repeat current test (with new arguments if bit 6 is OFF).
14	Set ON to suppress error HALTS.
15	Set ON to halt the program at the end of a test. (102076_8 and A- and B-registers contain the octal test number.)

To access a specific test (see Test Sections), set *switch register bit 15*. The program halts at the end of each test. The octal test number is in both the A- and B-registers. Press RUN to continue to the next test. If necessary, set *switch register bits 11 and 14* to suppress halts and messages to reach the desired test. When the test is reached, clear switch register bit 15 and set bit 13. The test will then loop with new arguments each time it is executed.

Diagnostic Execution

1. Set P-register to 100_8 .
2. Make switch register settings required.
3. Press PRESET (INTERNAL and EXTERNAL, if applicable).
4. Press RUN.

If no error is detected, the program makes a complete cycle approximately once in 40 to 50 seconds.

DIAGNOSTIC MESSAGES AND HALTS

The diagnostic communicates to the operator by teleprinter, HALTs, or both, based on configuration and switch register settings. Thus, messages consist of both HALT codes (MDR, A- and B-register values) and, if teleprinter present, teleprinter text.

Error HALT Codes

Error HALTs occur when an EAU instruction fails a test (unless switch register bit 14 is set). On an error HALT, the actual register results are in the A-, B-, E-, and Overflow (OV) registers. (For a DST instruction, A- and B-registers contain the results actually doubly stored.)

When running without a teleprinter or with messages suppressed, the arguments and expected results can be found in the fixed memory locations listed in Table 2.

Table 2. Memory Contents for Error Tests

Octal Memory Locating	Contents
132	A-register test value before test instruction executed
133	B-register test value before test instruction executed
134	E-register test value (bit 0) before test instruction executed
135	Memory test value before test instruction executed
136	OV register test value (bit 0) before test instruction executed
137	Shift count test value before shift/rotate instruction executed
140	Number of indirect addressing levels (0 is direct) test value
141	Expected A-register result
142	Actual A-register result
143	Expected B-register result
144	Actual B-register result
145	Expected E-register (bit 0) result
146	Actual E-register (bit 0) result
147	Expected OV register (bit 0) result
150	Actual OV register (bit 0) result
151 } 152 }	Actual double store result

Table 3 holds a summary of diagnostic program HALTs.

Table 3. Program HALTs

Octal MDR (T-register) Value	Meaning
1020xx	Instruction test failure (xx = test number)
102076	End of test section; A- and B-registers contain test number
102077	End of pass through all tests
1060xx	Unexpected trap cell interrupt (xx = select code)

Messages

There are two types of messages: information and error messages. All message data is octal except for the decimal end of pass count.

INFORMATION MESSAGES. The three information messages are shown in Table 4. They are printed, if switch 10 is clear.

Table 4. Information Messages

Text	Meaning
2100 SERIES EAU DIAGNOSTIC	Introductory header to the diagnostic
EOT <i>n</i>	End of test message where <i>n</i> is the octal test number
END OF PASS <i>n</i>	End of pass message printed at the end of each diagnostic cycle, where <i>n</i> is the decimal count of passes.

ERROR MESSAGES. A distinct error message format exists for each EAU instruction tested. In general each error message has the format

E-n mmm register and memory results

where *n* is the octal test number, *mmm* is the EAU instruction mnemonic, and *register and memory results* are a variable combination of data describing initial test conditions and expected and actual results of instruction test. Table 5 describes the error message format for each test.

The text is coded with the following mnemonics:

A means A-register
B means B-register
E means E-register except for first character of text
OV means Overflow register
M means Memory contents
SB means "Should Be"
IL = *n* means *n* indirect addressing levels used

For example,

E-3 MPY IL = 0 A,M was 000001 000003
B,A = 000000 000001 SB 000000 000003

This message indicates the following

- a. Error message from test 3 where the EAU instruction "MPY" is tested
- b. Indirect addressing was not used
- c. A-reg. = 000001 was initial test condition
Memory = 000003 was initial test condition
- d. B-reg. = 000000 was result
A-reg. = 000001 was result
- e. Result in B-reg. should have been = 000000
Result in A-reg. should have been = 000003

Table 5. Error Messages

Test Data	Text (x's are variable octal data)
E-1 DLD	IL = x B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx E = x SB x OV = x SB x
E-2 DST	IL = x STORED was xxxxxx xxxxxx SB xxxxxx xxxxxx
E-3 MPY	IL = x A,M was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-4 DIV	IL = x B,A,M was xxxxxx xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-5 ASR xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-6 ASL xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-7 LSR xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-10 LSL xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-11 RRR xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx
E-12 RRL xx	B,A was xxxxxx xxxxxx B,A = xxxxxx xxxxxx SB xxxxxx xxxxxx

Test Sections

The diagnostic consists of 10 tests, one for each EAU instruction.

TEST SECTIONS

Octal Test Number	EAU Instruction Tested
1	DLD (Double Load)
2	DST (Double Store)
3	MPY (Multiply)
4	DIV (Divide)
5	ASR (Arithmetic Long Shift Right)
6	ASL (Arithmetic Long Shift Left)
7	LSR (Logical Long Shift Right)
10	LSL (Logical Long Shift Left)
11	RRR (Rotate A- and B-registers Right)
12	RRL (Rotate A- and B-registers Left)

Each test is exercised in sequence using arguments from a number generator to get the actual results, unless switch register option 6 is used to suppress the generation of new arguments.

The execution of all 10 tests with switch 6 clear is a loop. A pass is 1500 decimal loops. One pass takes approximately one minute to run, if all switches are clear and no errors are encountered.

NUMBER GENERATION

At the start of each test new arguments are generated unless switch register bit 6 is set. Then arguments are stored in five fixed memory locations:

Octal Location	Purpose
132	A-register argument
133	B-register argument
134	E-register argument (bit 0)
135	Memory contents argument
136	Overflow register argument (bit 0)
137	Shift argument for shift/rotate instructions

Before each EAU instruction is tested, the E-register is set with bit 0 of location 134₈ and the Overflow register is set with bit 0 of location 136₈. Before testing all EAU instructions except "DLD," the A- and B-registers are loaded with the contents of 132₈ and 133₈ respectively. In DLD instructions the A- and B-registers are double loaded from locations 132₈ and 133₈. Location 135₈ holds the multiplier for the MPY instruction test and the division for the DIV instruction test.

It is possible to check an instruction using specific data by setting the above locations with the operator's test data and running the diagnostic with switch register bit 6 set.

INDIRECT ADDRESSING

The DLD, DST, MPY, and DIV instruction tests normally loop five times. The first time through, the addressing is direct. Thereafter, one level of indirect addressing is added for each additional loop. Switch register bit 7 set suppresses indirect addressing.

E- AND OVERFLOW-REGISTER CHECKING

Before each EAU instruction is executed, the E-register and Overflow registers are loaded with bit 0 of locations 134₈ and 136₈, respectively. After each EAU instruction is tested, these two registers are checked.

The E-register should never change. The Overflow register should show the following results:

Instruction	Result
DST	Should never change
DLD	
RRR	
RRL	
LSR	
LSL	
ASR	Should remain zero
MPY	Should remain zero
DIV	Should be zero unless a divide error occurred; in that case it should be 1.
ASL	Should be zero unless a significant bit was shifted out; in that case it should be 1.

