PAPER TAPE NO. 24324-16001

MEMORY PROTECT DIAGNOSTIC

for

hp-2100 SERIES COMPUTERS

reference manual

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *HP 2000 Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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Introduction

The Memory Protect Diagnostic confirms proper operation of the memory protect feature of 2100 series computers.

The diagnostic is one of the HP 2000 computer system diagnostics executed in conjunction with the HP 2000 Computer Systems Diagnostic Configurator.

Test sequence and test failure is communicated to the operator through a teleprinter, and through the computer Memory Data Register (also referred to as the MDR or T-register). Operator input is required via switch register, PRESET, and RUN/HALT switches at the computer front panel.

GENERAL ENVIRONMENT

The general hardware and software environments and system configuration procedures are described in *HP 2000 Computer Systems Diagnostic Configurator (02100-90157).*

Hardware Requirement

1. The diagnostic is run on 2100 series computers with the Memory Protect feature installed and a minimum of 4K of memory.

2. A paper tape reader is required to load the program only; the teleprinter paper tape reader may be used.

3. A console teleprinter is optional.

Software Requirement

The required software consists of the following binary object tapes:

1. HP 2000 Computer Systems Diagnostic Configurator (24296)

2. Memory Protect Diagnostic, part no. 24324-16001.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the HP 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader — Basic Moving Head Disc Loader (5951-1376).*

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic Messages and HALT Codes.

PREPARATION FOR DIAGNOSTIC RUN

Before tests can be initiated, the user performs the following actions:

1. Load the Diagnostic Configurator
2. Configure to available system hardware
3. Load the diagnostic
4. Dump the configuration for later use (optional)

Loading

Using the Binary Loader, load the Diagnostic Configurator. Perform the configuration procedure (see "Configuring" below) before loading the diagnostic. Then load the Memory Protect Diagnostic using the Binary Loader. The user may ensure that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number = 102001_8.

Configuring

Procedures for inputting the system hardware configuration parameters are found in the *HP 2000 Computer Systems Diagnostic Configurator* manual under "CONFIGURING."

The configuration procedure accepts six groups of parameters. This diagnostic requires only three groups to be defined. They are

- Computer type and options
- Teleprinter as system output device
- Memory size and type

Enter zero for all other parameters.

Computer Type and Options and *Memory Size and Type* must be carefully determined. They hold significant parameters for the execution of this diagnostic. In particular, the diagnostic will not execute, if the Memory Protect feature is not installed and configured. The EAU feature should be configured, if present.

Dumping

Using procedures described in the *HP 2000 Computer Systems Diagnostic Configurator* manual, the user may dump the configured diagnostic from memory onto paper tape so that the above configuration need not be repeated. The dumped paper tape holding the configured diagnostic can thereafter be loaded via the Binary Loader.

RUNNING THE DIAGNOSTIC

Switch Register Settings

Table 1 gives a summary of switch register options.

Table 1. Switch Register Settings

Bit	Meaning If Set
0 to 7	Reserved
8	Suppress operator intervention
9	Reserved
10	Suppress operator messages
11	Suppress error messages
12	Loop on diagnostic
13	Loop on test
14	Suppress error halts
15	Halt on test

Diagnostic Execution

1. Set P-register to 100_8.

2. Enter program options into switch register (according to Table 1).

3. Press RESET (EXTERNAL and INTERNAL, if applicable).

4. Press RUN.

   Result: the messages

   H15 HP 2100 SERIES MEMORY PROTECT DIAGNOSTIC
   H07 PRESS PRESET (EXT/INT), RUN

   are printed followed by a HALT with MDR = 102007_8.

5. Press PRESET (EXTERNAL and INTERNAL, if applicable).

6. Press RUN.

   Result: the message

   H13 PRESS HALT, PRESET (INT), RUN
   IN LESS THAN 15 SECS.

   is printed.

7. In less than 15 seconds from the completion of the message, press HALT.

8. Press PRESET (or PRESET INTERNAL, if applicable).

9. Press RUN.

   Result: The rest of the diagnostic completes automatically, if no test failure is encountered.

10. The operator can restart the diagnostic automatically (eliminating the two PRESET switch entries), by having switch register bit 8 set, when the diagnostic completes. Diagnostic completion is signalled by the message

    PASS *xxxxxx*
    (*xxxxxx* = pass count in octal and A-register = pass count)

    followed by a HALT with MDR = 102077_8.

11. If errors occur in test 4, let the teleprinter print a large number of errors (allowing the fence register to increment) before terminating the printout using switch register bit 11. This will assist in diagnosing the error, especially if the error is located in the address.

DIAGNOSTIC MESSAGES AND HALT CODES

The diagnostic communicates to the operator by teleprinter, HALTS, or both, based on switch register settings. Thus messages consist of both teleprinter text and HALT Codes (MDR). Message text and HALT codes are summarized in Table 2.

Message Text

Text formats consist of a letter, an octal message number, and message text. If the letter is an "H", the message is information only. If the letter is an "E", the message indicates an error detected in a memory protect test. Error messages are only printed if switch register bit 11 is clear.

HALTS

Whenever an error or information HALT occurs, press RUN to continue test. Error HALTS will only occur if switch register bit 14 is clear.

Table 2. Diagnostic Messages

Text	Octal MDR HALT Code	Meaning
E01. CLF CH-SFS CH ERROR	102001	Failed the combination of instructions CLF/SFS operating on the teleprinter channel.
E02. CLF CH-SFC CH ERROR	102002	Failed the combination of instructions CLF/SFC operating on the teleprinter channel.
E03. STF CH-SFC CH ERROR	102003	Failed the combination of instructions STF/SFC operating on the teleprinter channel.
E04. STF CH-SFS CH ERROR	102004	Failed the combination of instructions STF/SFS operating on the teleprinter channel.
E05. DID NOT INTERRUPT	102005	Teleprinter channel failed to interrupt.
E06. RETURN ADDRESS INCORRECT	102006	Return address from interrupt was incorrect.
H07. PRESS PRESET (EXT/INT), RUN	102007	Message requesting operator to perform actions.

Table 2. Diagnostic Messages (Continued)

Text	Octal MDR HALT Code	Meaning
E10. PRESET (EXT) DID NOT SET FLAG	102010	PRESET failed to set the teleprinter flag.
H11. END BI/O	102011	Test 1, BI/O, completed.
E12. A/B REG. TEST FAILED, INSTR *xxxxxx* WAS EXEC. AT LOC *yyyyyy*, FENCE REG. AT *zzzzzz*	102012	Failure of test which checks if memory protect will allow use of A- and B-registers (STA B or STB A); instruction was *xxxxxx;* address of instruction was *yyyyyy;* fence register was set at *zzzzzz.*
H13. PRESS HALT, PRESET (INT), RUN IN LESS THAN 15 SEC.	(None)	Message requesting operator to perform actions; HALT must be pressed in less than 15 seconds from completion of message.
E14. PRESET (INT) DID NOT TURN OFF M.P.	102014	PRESET did not turn memory protect off or HALT pressed in more than 15 seconds after message H13.
H15. HP 2100 SERIES MEMORY PROTECT DIAGNOSTIC	—	Heading message.
E16. ERROR, PHASE 1 OF INSTR FOLLOWING JSB,I M.P. VIOLATION WAS EXECUTED	102016	JSB,I should not have held off memory protect interrupt, but did hold it off until phase 1 of the following instruction.
E17. NO M.P. INTERRUPT DURING JMP,I	102017	No memory protect interrupt occurred during an indirect jump or an I/O instruction (CLF 0).
E20. INDIRECT ADDRESSING THRU M.P. AREA FAILED	102020	Memory protect interrupt occurred while executing a legal indirect addressing instruction through a protected area.
E21. I/O TRAP CELL INSTR ERROR	102021	I/O instruction (CLF CH) in an I/O trap cell turned off memory protect or I/O device failed to interrupt.
E22. NON I/O TRAP CELL INSTRUCTION ERROR	102022	A non-I/O instruction in a trap cell did not turn off memory protect.
E23. INDIRECT ADDRESSING THRU M.P. AREA FAILED (NO INTPT)	102023	Memory protect interrupt failed to occur after executing a legal indirect addressing instruction through a protected area followed by an I/O instruction (CLF 0).
H24. END MPIO	102024	Test 2, MPI/O, completed.
E25. NO INTERRUPT ON SECOND LEVEL OF JMP,I CHAIN	102025	CPU failed to produce a memory protect violation interrupt on the execution of the second level of an indirect jump.

Table 2. Diagnostic Messages (Continued)

Text	Octal MDR HALT Code	Meaning
E26. RETURN ADDRESS INCORRECT FOR CHAINED JMP,I INTERRUPTS	102026	Memory protect interrupts, during chained indirect jump instructions, caused bad return address entry.
E27. NO INTERRUPT ON THIRD LEVEL OF JSB,I CHAIN	102027	No memory protect interrupt occurred on the third level of an indirect subroutine-jump chain.
E30. RETURN ADDRESS INCORRECT FOR CHAINED JSB,I INTERRUPTS	102030	Memory protect interrupt execution caused a bad return address entry for interrupt during JSB indirect chain.
H31. END CIJI	102031	Test 3, CIJI, completed.
H32. ILLEGAL INTERRUPT FENCE REG. *xxxxxx* VIOLATION REG. *yyyyyy* INSTR IS *zzzzzz*	102032	An illegal memory protect interrupt occurred; fence register = *xxxxxx;* violation register = *yyyyyy;* instruction executing was *zzzzzz;* allow many printouts of this error in case the trouble is in the adder.
E33. NO INTPT. FENCE REG IS *xxxxxx*	102033	No memory protect interrupt occurred; fence register = *xxxxxx.*
E34. VIOLATION REG. *xxxxxx,* SHOULD BE *yyyyyy*	102034	Violation register holds wrong value *xxxxxx;* should be *yyyyyy.*
H37. END FR	102037	Test 4, FR, completed.
E40. INTERRUPT OCCURRED WHILE EXECUTING LEGAL INSTR *xxxxxx* FENCE REG. *yyyyyy,* VIOL. REG *zzzzzz*	102040	An interrupt occurred while executing the instruction *xxxxxx;* fence register = *yyyyyy;* violation register = *zzzzzz.*
H47. END NVI	102047	Test 5, NVI, completed.
E50. NO M.P. INTERRUPT AFTER EXECUTING INSTR *xxxxxx* AT LOC. *yyyyyy,* FENCE AT *zzzzzz*	102050	No memory protect interrupt occurred after executing the instruction *xxxxxx* at address *yyyyyy;* fence register is set to *zzzzzz.*
E51. NO M.P. INTERRUPT AFTER EXECUTING EAU INSTR *xxxxxx* AT LOC. *yyyyyy,* FENCE AT *zzzzzz*	102051	No memory protect interrupt occurred after executing the EAU instruction *xxxxxx* at address *yyyyyy;* fence register is set to *zzzzzz.*
H53. END VI	102053	Test 6, VI, completed.
E60. NO INTERRUPT WHEN M.P. VIOLATED	102060	Memory protect violation was created, but no interrupt occurred.

Table 2. Diagnostic Messages (Continued)

Text	Octal MDR HALT Code	Meaning
E61. M.P. AREA VIOLATED AND M.P. INTERRUPT OCCURRED AT SAME TIME	102061	Memory protect interrupt occurred but failed to protect memory.
E62. NO M.P. INTERRUPT, STC OR OTA INSTR MAY HAVE FAILED OR M.P. NOT INSTALLED	102062	Memory protect interrupt did not occur; an STC or OTA instruction may have failed to cause a memory protect interrupt; this error may also occur if memory protect feature is not installed.
E63. M.P. INTERRUPT LOC NOT EQUAL TO VIOLATION REG. LIA MAY HAVE FAILED	102063	Violation register is not equal to the location of memory protect violation; LIA instruction may have failed.
E64. M.P. INTERRUPT LOC NOT EQUAL TO VIOLATION REG. LIB MAY HAVE FAILED	102064	Violation register is not equal to location where memory protect violation was created; LIB instruction may have failed.
E65. NO M.P. INTERRUPT, STC OR OTB INSTR MAY HAVE FAILED	102065	Memory protect interrupt did not occur; STC or OTB instruction may have failed.
E66. MEMORY PARITY ERROR, VIOLATION REGISTER = *xxxxxx*	102066	Interrupt to location 5 did set bit 15 of violation register. *xxxxxx* = violation register.
E71. RESET DOUBLE STORE FAILED	102071	Double store into protected memory did not elicit an interrupt or its execution was not inhibited.
H77. PASS *xxxxxx*	102077	Diagnostic completed. *xxxxxx* = pass count and A-register = *xxxxxx*.
(None)	1060*xx*	Trap cell HALT; *xx* = select code of device; this HALT may necessitate reloading diagnostic.
(None)	107000	This code (107000) did not create a memory protect violation interrupt, as it was supposed to, but executed the HALT.

Test Sections

The Memory Protect diagnostic is divided into six test sections.

TESTS

Test 1 — BI/O

This section tests the ability to set and clear teleprinter I/O flags and control bits and tests the interrupt operation of the teleprinter. A PRESET test for the teleprinter I/O channel is also performed. This section is skipped if there is no teleprinter.

Test 2 — MPIO

Memory protect I/O instructions are tested. Use of the A- and B-registers under memory protect is tested. Verifies that memory protect provides wrap-around protection, the proper interrupt in conjunction with proper values in the fence register, violation register, and return address. Verifies that memory protect executes properly for indirect jumps and indirect addressing through protected areas of memory.

Test 3 — CIJI

This section tests the ability to suppress interrupts for two levels of chained indirect jump (JMP) and subroutine jump (JSB) instructions allowing the sequence to be interrupted during the third level.

Test 4 — FR

This section tests the ability to turn on memory protect and to jump indirectly from below the fence to one instruction above the fence for all memory above address 400_8. Test is made for legal and illegal interrupts when executing violation and non-violation instructions on both sides of the fence for all memory above address 400_8. The violation register is tested for all memory above 400_8.

Test 5 — NVI

This section tests all non-violation instructions including the EAU instructions, if EAU is installed.

Test 6 — VI

All violation instructions are tested, including the EAU instructions, if EAU is installed. A specially coded memory protect violation HALT instruction, 107000_8, is executed to verify that the memory protect interrupt occurs instead of the execution of the HALT.

LIMITATION OF THIS DIAGNOSTIC

This diagnostic does not test the PRL operation of the memory protect feature.