PAPER TAPE NO. 24325-16001

MEMORY PARITY DIAGNOSTIC

for

hp-2100 SERIES COMPUTERS

reference manual

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Contents

Section	Page
INTRODUCTION	
General Environment	1
Hardware Requirements	2
Software Requirements	2
OPERATING PROCEDURES	
Preparation for Diagnostic Run	3
Loading	3
Configuring	3
Dumping	4
Making Test Hardware Ready	4
Running the Diagnostic	4
Switch Register Settings	4
Diagnostic Execution	5
Diagnostic Halt Codes	7
TEST SECTIONS	
Initialization	9
Test	9
Termination	10

Tables

Table	Title	Page
1	Switch Register Program Options	5
2	HALT Codes	7

Memory Parity Diagnostic

Introduction

The Memory Parity Diagnostic confirms proper operation of the memory parity check circuitry.

The diagnostic operates on 2100 series computers and is one of the HP 2000 computer system diagnostics executed in conjunction with the HP 2000 Computer Systems Diagnostic Configurator.

Communication to the operator is made via these CPU front panel indicators: the PARITY ERROR light, the Memory Data Register (MDR or T-register), and the A- and B-registers.

Switch and jumper connection actions must be performed to initiate and conduct the test. See "Diagnostic Execution" section.

To assure validity, run this diagnostic only after the following other CPU diagnostics have been successfully completed in the order shown.

- Memory Reference Instruction Diagnostic
- Alter-skip Instruction Diagnostic
- Shift-rotate Instructions Diagnostic
- Memory Diagnostic
- Memory Protect Diagnostic

GENERAL ENVIRONMENT

The general hardware and software environments and system configuration procedures are described in *HP 2000 Computer Systems Diagnostic Configuration (02100-90157)* manual.

Hardware Requirements

1. The diagnostic is run on 2100 series computers with 4K of memory.

2. A paper tape reader is required to load the program only.

3. At least one standard Interface PCA with interrupt capability must be installed in an I/O slot.

Software Requirements

The required software consists of the following binary object tapes:

HP 2000 Computer Systems Diagnostic Configurator (HP 24296).

2. Memory Parity Diagnostic, part no. 24325-16001.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader — Basic Moving Head Disc Loader (5951-1376).*

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic HALT Codes.

PREPARATION FOR DIAGNOSTIC RUN

Before the tests can be initiated, the user performs the following actions:

1. Load the Diagnostic Configurator
2. Configure to available system hardware
3. Load this diagnostic
4. Dump the configuration for later use (optional)
5. Make test hardware ready

Loading

Using the Binary Loader, load the Diagnostic Configurator. Perform the configuration procedure (see "Configuring" below) before loading the diagnostic. Then load the Memory Parity Diagnostic using the Binary Loader. The user may ensure that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number = 102002_8.

Configuring

Procedures for inputting the system hardware configuration parameters are found in the *HP 2000 Computer Systems Diagnostic Configurator* manual under "CONFIGURING."

The configuration procedure accepts six groups of parameters. This diagnostic requires only two groups be defined. They are:

- Computer type and options
- Memory size and type

Enter zero for all other parameters.

Computer Type and Options and *Memory Size and Type* must be carefully determined. These hold significant parameters for the execution of this diagnostic and vary from one 2100 series installation to the other.

Dumping

Using procedures described in the *HP Computer Systems Diagnostic Configurator*, the user may dump the configured diagnostic from memory onto paper tape so that the above configuration procedures need not be repeated. The dumped paper tape holding the configured diagnostic can thereafter be loaded via the Binary Loader.

Making Test Hardware Ready

1. Insure that at least one standard I/O board is installed in an I/O slot.
2. Insure that the ARS/$\overline{\text{ARS}}$ switch is in the $\overline{\text{ARS}}$ position.
3. Insure that the INTERRUPT/HALT switch is in the INTERRUPT position.
4. Clear memory location 5_8.

RUNNING THE DIAGNOSTIC

Switch Register Settings

Table 1 gives a summary of switch register options.

Table 1. Switch Register Program Options

Bit	Function If Set
0 to 7	Reserved.
8	Suppress operator intervention.
9-11	Reserved.
12	Loop on diagnostic. Clear to HALT at end of pass.
13 to 15	Reserved.

Diagnostic Execution

1. Set P-register to 100_8.

2. Enter the select code of the standard I/O device installed into the switch register.

3. Press PRESET (EXTERNAL and INTERNAL, if applicable).

4. Press RUN.

   Result: A HALT occurs with MDR = 102074_8.

5. Press RUN.

   Result: A HALT occurs with MDR = 102002_8. The Memory Data Control Parity Bit light should be OFF (2100 only). If it is ON, a circuit error exists and must be fixed before restarting the diagnostic. If light is OFF, continue with step 6.

6. Turn CPU power OFF.

7. If the CPU is a 2116, 2115, or 2114, remove the Parity Check board to create bad parity.

8. If the CPU is a 2100, create bad parity by making the following jumper connections via terminal posts on the Memory Data Control board:

   E1 to E2
   E3 to E4

9. If the CPU is a 21MX, create bad parity by making the jumper connection via terminal posts on the Memory Controller board from PAR to ground.

10. Turn CPU power ON.

11. Set P-register to 130_8.

12. Clear switch register.

13. Press PRESET (EXTERNAL and INTERNAL, if applicable).

14. Press RUN.

    Result: A HALT occurs with MDR = 102003_8.

15. Turn CPU power OFF.

16. If the CPU is a 2116, 2115, or 2114, replace the Parity Check board to restore good parity.

17. If the CPU is a 2100 or 21MX, restore good parity by removing clip leads installed.

18. Place the INTERRUPT/HALT switch in the HALT position.

19. Turn CPU power ON.

20. Set P-register to 131_8.

21. Clear switch register.

22. Press PRESET (INTERNAL PRESET, if applicable).

23. Press RUN.

    Result: A HALT occurs (MDR is clear) with a 1_8 in the B-register, if the parity circuits are working correctly. The front panel PARITY light should be ON and the Memory Data Control Parity light should be ON (2100 only).

24. Place the INTERRUPT/HALT switch in the INTERRUPT position.

25. Select program options in switch register. Press PRESET (EXTERNAL and INTERNAL, if applicable).

    Result: PARITY lights should go OFF. If not, parity error detected circuitry must be corrected before restarting diagnostic.

26. Press RUN.

Result: If an error is not detected, the rest of the diagnostic completes. If switch register bit 12 is clear, a HALT occurs with MDR = 102077_8.

27. To restart diagnostic, return to step 5 of this procedure. If switch register bit 8 was selected in step 24, return to step 26.

DIAGNOSTIC HALT CODES

The diagnostic communicates to the operator by coded HALTs. The Memory Data Register (MDR or T-register), A-register, and B-register hold information which indicates test procedure and test failure. HALTs fall into two types: information and error HALTs. Table 2 lists the HALT codes and meanings. The second column of the table, headed by *E/I*, indicates whether the HALT is an error HALT, *E*, or an information HALT, *I*.

Table 2. HALT Codes

Octal MDR (A- & B-reg.) HALT Codes	E/I	Test	Meaning
102000 (A = *xxxxxx*, B = *yyyyyy*)	*E*	PEB05 PEH05	Last instruction before interrupt failed to execute properly; *xxxxxx* is actual A-register result; *yyyyyy* is the expected A-register result.
102001 (A = *xxxxxx*, B = *yyyyyy*)	*E*	PEB05 PEH05	Interrupt occurred at wrong address *xxxxxx;* should be *yyyyyy.*
102002	*I*	ODPTN	Perform step 6 of the Diagnostic Execution procedure.
102003	*I*	ODPTN	Perform step 15 of the Diagnostic Execution procedure.
102004	*E*	PEA05	Parity error interrupt indicator (bit 15) was not reset by CPU power turn-on.
102005	*E*	PEA05	CPU failed to HALT on parity error.
102006 (A = *xxxxxx*)	*E*	PEB05	Parity error did not cause interrupt at address *xxxxxx;* interrupt function is not working or parity tree is faulty.
102007 (A = *xxxxxx*, B = *yyyyyy*)	*E*	PEB05	Parity error memory address is incorrect; *xxxxxx* is expected address, *yyyyyy* is actual address. Perform Memory Protect diagnostic to determine if source of error is Memory Protect or Parity Error circuitry.
102010	*E*	PEC05	CLF 5 did not inhibit parity error interrupt.

Table 2. HALT Codes (Continued)

Octal MDR (A- & B-Reg.) HALT Codes	E/I	Test	Meaning
102011	*E*	PED05	A parity error interrupt was caused by accessing protected memory.
102020	*E*	PEE05	A parity error interrupt was caused during memory write time.
102027	*E*	PED05	A parity error interrupt was caused by accessing non-existent memory.
102040	*E*	PEH05	Parity error failed to take priority over I/O interrupt.
102041	*E*	PEH05	Neither parity error nor I/O interrupt was received in priority test.
102042	*E*	PEH05	No I/O interrupt received in priority test.
102043	*E*	PEI05	Parity error interrupt indicator (bit 15) was not set in parity error.
102044 (A = *xxxxxx*)	*E*	PEI05	Parity error did not cause interrupt at address *xxxxxx;* the interrupt function is not working or the parity tree is faulty.
102045 (A = *xxxxxx*, B = *yyyyyy*)	*E*	PEI05	Parity error memory address is incorrect; should have been *xxxxxx*, but actually is *yyyyyy;* perform Memory Protect diagnostic to determine if source of error is Memory Protect or Parity Error circuitry.
102046 (A = *xxxxxx*)	*E*	PEI05	Parity error at address *xxxxxx* was restored to good parity by an LDB instruction.
102047 (A = *xxxxxx*)	*E*	PEI05	Parity error at address *xxxxxx* was not restored to good parity by an STB instruction.
102050, 102051, 102052, 102053, 102054	*E*	PEI05	Since the Memory Protect feature is not installed on the computer (this HALT should not occur on 2116, 2115, 2114, or 2100 computers), an interrupt should not occur, but did occur.
102073	*E*	START	Select code in switch register is less than 10_8.
102074	*I*	START	Configuration completed.
102077	*I*	END	Diagnostic pass has completed.
1060*xx*	*E*	Any	Trap cell interrupt; *xx* = select code; Memory Address Register holds execution address, when interrupted.

Test Sections

The Memory Parity Diagnostic consists of ten routines: two initialization routines, seven test routines, and the termination routine.

INITIALIZATION

START. Trap cell halts are set up in memory locations 2_8 to 77_8. I/O instructions are configured. A program HALT is executed to allow the user to make switches and jumper connections to force bad parity.

ODPTN. Even parity data is loaded into special locations used during test, since the memory parity circuitry uses odd parity as valid. This "bad" parity data is used by test routines to check the memory parity circuitry.

TEST

PEA05. Confirmation is made that bit 15 of the A-register is not set when the violation register is loaded following power-on at the end of START routine. The ability to detect a parity error is verified. A number of operator actions are required to test parity error detection and indicator functions.

PEB05. The ability to interrupt on parity error detection is tested. This test must be passed before continuing with subsequent tests.

PEC05. The ability of a "CLF 5" instruction to inhibit parity error interrupts is tested. A CLF 5 instruction is executed to turn off the interrupt circuitry; then an even parity word (bad parity), generated by ODPTN, is accessed. An interrupt should *not* occur.

PED05. It is verified that parity error interrupts are inhibited when non-existent or protected memory is accessed. An attempt is made to read the contents of the highest location in memory, when the loader-protect switch "PROTECT" (2100 and earlier computers only) is set, without detecting a parity error interrupt. Then an attempt is made to read from non-existent memory. A parity error interrupt should not occur in either case.

PEE05. It is verified that parity error interrupts are inhibited during memory write time. A "JSB" instruction is used to write an even parity value from the program counter (P-register) into memory. An interrupt should not occur.

PEH05. Priority control is tested by generating an I/O interrupt on the I/O channel selected during program configuration of the diagnostic. That interrupt is immediately followed by a parity error interrupt, which should inhibit the I/O interrupt.

PEI05. For each of the locations set to even parity by ODPTN, this routine tests the parity tree by performing the following tests:

a. Is parity error detected?

b. Does an interrupt occur?

c. Is the location address strobed into the Memory Protect violation register?

It is then verified that a read/write instruction (LDB) does not restore good parity to a location containing bad parity. Finally, it is verified that a clear/write type instruction (STB) does restore good parity to a location containing bad parity.

TERMINATION

END. A HALT is performed with 102077_8 in the MDR.