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ABSOLUTE BINARY PROGRAM NO. 12892-16001
DATE CODE 1705

MEMORY PROTECT-PARITY ERROR DIAGNOSTIC

reference manual

For HP 2100A/S and 21MX Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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SECTION I
INTRODUCTION

1-1. GENERAL

This diagnostic program verifies the proper operation of the memory protect and parity error circuits in an HP 2100A/S Computer and the HP 12892A/B Memory Protect and parity error option for the HP 21MX Computer Series. The serial number of this diagnostic is 102305 (octal) and is located in memory address 126 (octal).

1-2. REQUIRED HARDWARE

The following hardware is required:

a. This diagnostic may be executed in any of the following computers with at least 4K of memory:

   (1) 2100A/S where memory protect is standard.

   (2) 21MX M-Series:* 2108 or 2112 computer with 12892A/B Memory Protect option installed; 2105 computer cannot accommodate the 12892A/B Memory Protect option.

   (3) 21MX E-Series:* 2109 or 2113 computer with 12892B Memory Protect option installed.

b. A console device is optional for error and message reporting.

c. A diagnostic input device as specified in the *Diagnostic Configurator Reference Manual* is to be used to load the Configurator and the diagnostic program.

d. Any standard I/O** interface with flag, control, and interrupt circuitry (including the console device interface) must be used to test I/O related functions of memory protect.

e. A 12976A/13305A Dynamic Mapping System (DMS) on a 21MX computer is optional.

f. DMA (DCPC) for Test 11 only.

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*21MX M-Series and 21MX E-Series will be referred to as 21MX throughout this reference manual.

**Standard I/O implies that the interface will respond to the assigned meaning of the I/O instructions and will also interrupt when the Control and Flag are set and the interrupt system is enabled.

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator used for equipment configuration and as a console driver:

Absolute Binary Program, part no. 24296-60001
Reference Manual, part no. 02100-90157

b. Memory Protect-Parity Error Diagnostic:

Absolute Binary Program, part no. 12892-16001
Reference Manual, part no. 12892-90005

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic consists of an Initialization section, a Control section and 14 tests. The Initialization section prepares the diagnostic with the test select code (used to test interruptible functions) and options specified by the operator.

2-2. TEST CONTROL AND EXECUTION

The Control section is responsible for printing an introductory header message on the console (if available) and then executing tests according to the options selected in the Switch Register. These options are fully defined in the following sections. (Refer to table 3-2.) The Control section also keeps count of the number of completed diagnostic passes and, if Switch Register bit 10 is clear, will output the pass count to the console device.

2-3. MESSAGE REPORTING

If a console device is used, two types of messages are reported: error and information.

Error messages are used to inform the operator if the memory protect-parity error circuits have failed to properly execute a function.

Information messages are used to instruct the operator to perform an operation related to the diagnostic's function or to inform him of the progress of the diagnostic. An Information halt will occur to allow the operator an opportunity to perform a function. A printed message will be preceded by an E (error) or H (information) and an octal number which relates to a halt code (last two octal digits only). An example of an error message follows:

Error Halt

Message: E052 NO MEM VIOLATION
Halt Code: 102052 (octal)

Error messages can be suppressed by setting Switch Register bit 11. Error halts can be suppressed by setting Switch Register bit 14. Information messages may be suppressed by setting Switch Register bit 10.

2-4. DIAGNOSTIC LIMITATIONS

Several tests require that an I/O interface with standard flag, control, and interrupt circuitry be installed in order to properly test the memory protect-parity error functions involving the I/O structure.

Several tests require that the Memory Expansion Module (MEM) be installed and operational in order to execute all test functions of the diagnostic. The operator must inform the diagnostic via S-register bit 14 if DMS (MEM) is installed.

3-1. CONFIGURATION

If testing a 21MX computer, turn the power off and remove the 12892A/B Memory Protect PCA; ensure that the PCA jumpers are set as specified in table 3-1. Ensure that the HLT/INT-IGNORE switch A1S1 is set to INT-IGNORE and turn the power on. If testing a 2100A/S computer, ensure that switch S1 on Data Control Card A107 is set to PROTECT and that switch S2 on I/O Buffer Card A8 is set to P.E. INT during the entire diagnostic execution. A flow chart of the diagnostic operating procedure is provided in figure 3-1.

Operator error or abnormal aborting of the diagnostic may cause various memory locations to be written with even parity. For 2100A/S or 21MX M-Series computers, reload the Configurator and run the Pretest (P=2) as explained in the Configurator Manual to write proper parity into memory. Then reload the diagnostic.

For 21MX E-Series computers, press IBL which will write correct parity when performing the microcoded diagnostic and then set the P-register to 100 (octal) for rerun of the diagnostic.

Table 3-1. Memory Protect Jumper Configurations

PCA TYPE	JUMPER SETTING	COMMENTS
12892A	W1 = A	Setting used throughout entire diagnostic.
12892B	RME = OUT SEL1 = OUT INT = IN JSB = IN HLTPE = OUT MX = OUT = 21MX E-Series = IN = 21MX M-Series	Setting used for Test 00 thru 10 only.

3-2. EXECUTION

After configuring the diagnostic, it will execute the memory protect portion of the diagnostic (Test 00 through 09) and then halt with 106000 (octal) in Test 10. The operator is then instructed to:

a. Depending on computer type, generate even parity for parity error portion of the diagnostic as follows:

For 21MX computers — On front center of 2102A/B Memory Controller which is behind the computer's front panel, connect jumper wire between PAR (parity) and ⏚ (ground) terminal posts.

For 2100A/S computers — On top center of Data Control Card A107, connect a jumper wire between ODD terminal post E1 and GND terminal post E2 and connect another jumper wire between EVEN terminal post E3 and +5V terminal post E4.

b. Depending on computer type, set parity error and power fail/auto restart switches as follows:

For 2100A/S computers — On top of I/O Buffer Card A8, set HALT/P.E. INT switch S2 to HALT (halt on parity error position). On top of I/O Control Card A7, set ARS/$\overline{\text{ARS}}$ switch S1 to ARS (auto restart position).

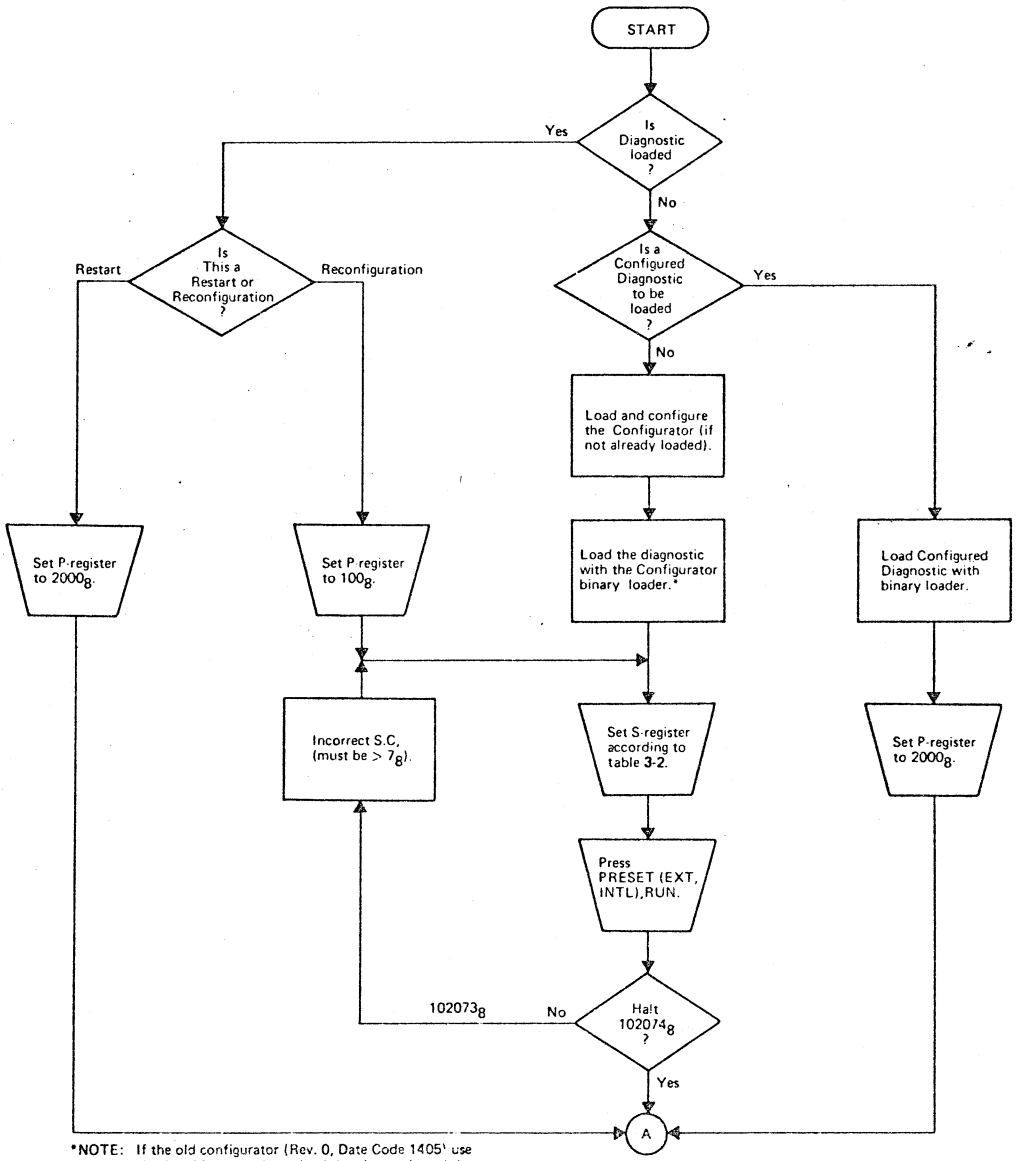
For 21MX computers — At rear of CPU PCA A1, set HLT/INT-IGNORE switch A1S1 (left-hand switch when viewed from rear of PCA) to HLT (right-hand position). This will create a halt on parity error. At rear of CPU PCA A1, set ARS/$\overline{\text{ARS}}$ switch A1S2 (right-hand switch when viewed from rear of PCA) to ARS (right-hand position). This is the auto restart position.

c. If testing with a 12892B Memory Protect PCA, change jumper configurations for Test 11 in accordance with table 3-5.

It should be noted that jumpers need only to be changed for the execution of Test 11. Test 11 is not part of the standard test run and must be selected by the operator. Refer to paragraph 3-4. Once the jumpers have been changed and Test 11 has been completed, the jumpers must be changed back to the initial settings listed in table 3-1 before continuing with another pass of the diagnostic.

When Test 11 is entered and Test 10 has not been executed, a message H061 will be printed followed by a halt 102061. This halt allows the operator to change the jumpers. However, if Test 10 has been executed, the jumpers have already been changed during halt 106001. (Refer to table 4-2, halt 106001.) When Test 10 has been executed, the message H061 and halt 102061 will not occur in Test 11. After Test 11 has been completed and before reaching the end of the diagnostic, a message H062 and halt 102062 occurs. This allows the operator to restore the jumpers to the settings listed in table 3-1 before another pass of the diagnostic is initiated.

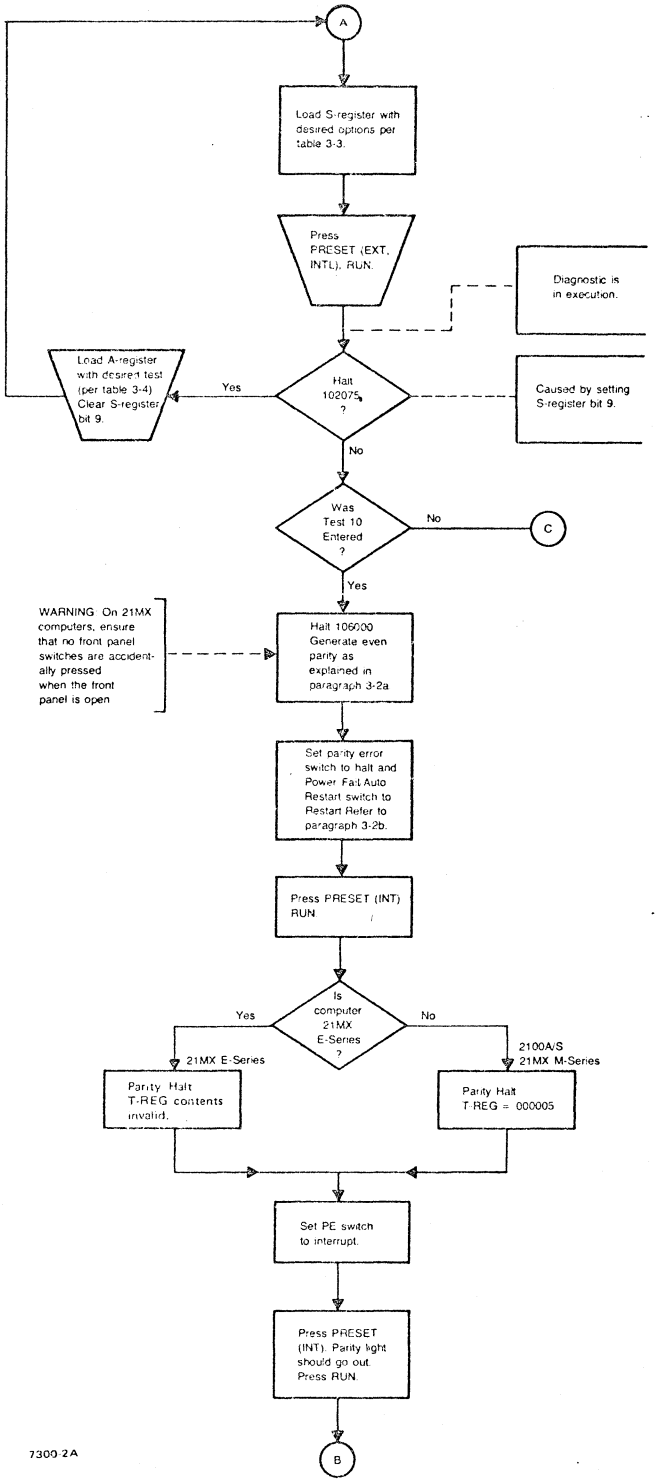
The operator powers down the computer (STANDBY for 21MX computers), changes the jumper configurations, and then powers up the computer (OPERATE for 21MX computers). The computer will immediately reach a halt 102077, indicating the end of the diagnostic. The operator then needs only to press RUN to initiate another pass of the diagnostic.



*NOTE: If the old configurator (Rev. 0, Date Code 1405) use absolute binary loader to load the diagnostic and then set P-register to 100_8.

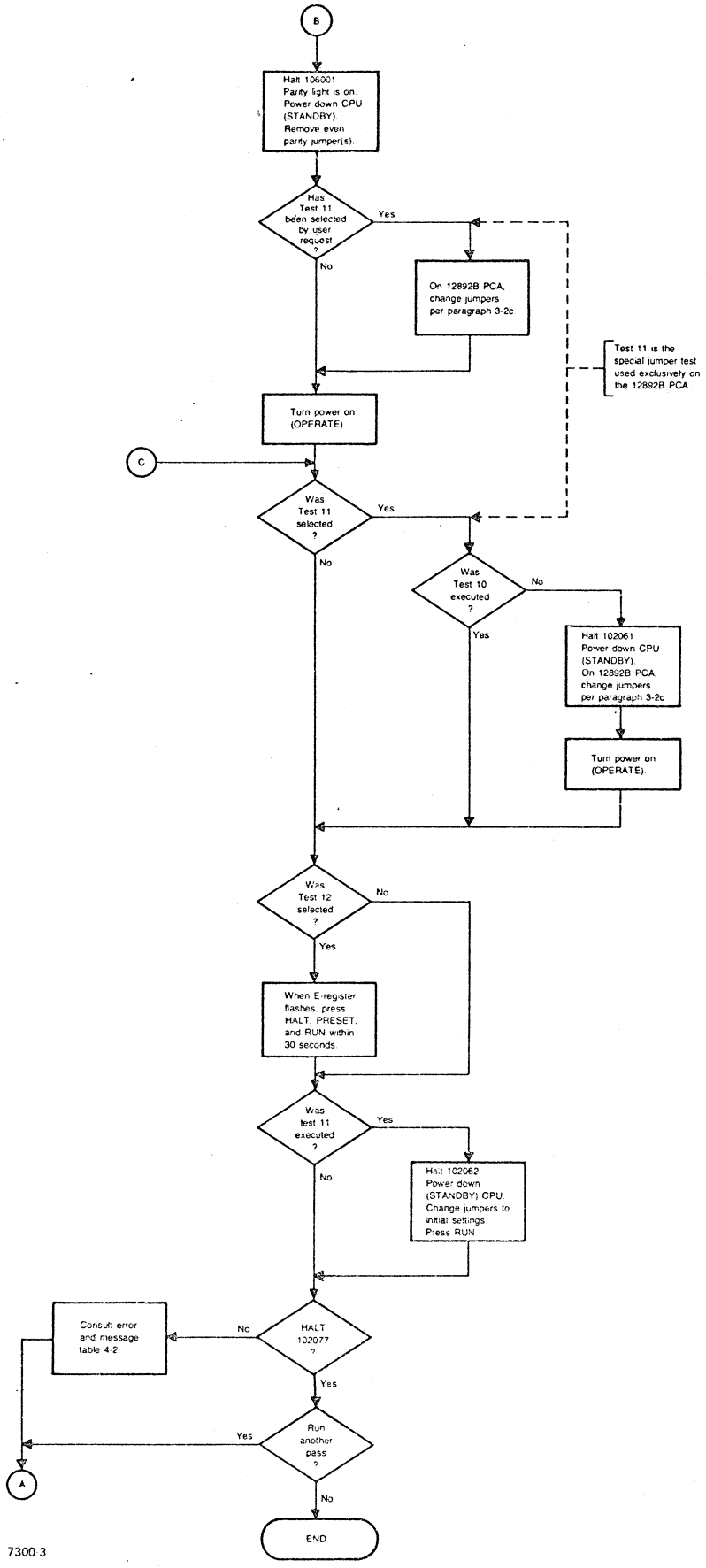
7300-1

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 3)



7300-2

Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 3)



7300-3

Figure 3-1. Operating Procedure Flowchart (Sheet 3 of 3)

3-3. ILLEGAL TRAP CELL HALTS

If an illegal trap cell halt (106077) occurs during the diagnostic execution, the operator must determine the source of the failure by inspecting the P-Register and M-Register. (The operator may be able to recover by restarting the program as described in figure 3-1 or the program may have to be reloaded.

3-4. TEST SELECTION BY OPERATOR

The Control section allows the operator the option of selecting a test or sequence of tests to be executed. The operator sets Switch Register bit 9 to indicate that he wants to make a selection and then presses RUN. The computer will come to a halt 102075 (octal) to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. Now the operator loads the A-Register with the test(s) desired. A-Register bit 0 represents test 00, bit 1 represents test 01, and so on up to bit 13 which represents test 13. The operator must now clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run.

Table 3-2. Entry of I/O Interface via S-Register

S-REG BIT	FUNCTION
15	If set, 12892B under test; if clear 12892A or 2100A/S computer under test.
14	If set, DMS present (DMS related test will be exercised); if clear, no DMS (MEM) present).
13-6	Reserved.
5-0	Select code of I/O interface to verify I/O related Memory Protect functions.

Table 3-3. Desired Test Options via S-Register

S-REG BIT	MEANING IF SET
15	Halt 102076 (octal) at the end of each test. The A-Register contains the test number in octal.
14	Suppress error halts.
13	Loop on last test section being executed.
12	Loop on diagnostic.
11	Suppress error messages.
10	Suppress information messages.
9	Abort diagnostic execution after the current test section and halt (102075). Operator can specify a new group of test(s) in the A-Register. Then clear Switch Register bit 9 and press RUN.
8	Suppress operator intervention tests.
7-0	Reserved.

Table 3-4. Test Selection Summary via A-Register

A-REG BIT	IF SET WILL EXECUTE*	TEST
0	Halt Test (MPT)	00
1	Basic Fence Test	01
2	I/O Violation Test	02
3	MPT Control Test	03
4	MPT Trap Cell Logic Test	04
5	MPT Indirect Logic Test	05
6	Memory Expansion-MPT Test	06
7	Fence and Violation Register Test	07
8	Non-Violation Instruction Test	08
9	Violation Instruction Test	09
10	Parity Error Halt and Interrupt Logic Test	10
11*	12892B Special Jumper Test	11
12	DMA Test	12
13	Preset Test (to clear MPT)	13

If all A-register bits are cleared, all possible tests will be executed (excluding Test 11), considering the 12892A or 12892B Memory Protect, and the availability of DMS (MEM).

*Test 11 is not part of the standard test run. If the operator desires to run Test 11, he must select Test 11. Refer to paragraph 3-4.

Table 3-5. 12892B Jumper Settings for Test 11

RME	= OUT	
SEL1	= IN	
INT	= OUT	
JSB	= OUT	
HLTPE	= OUT	
MX	= OUT	= 21MX E-Series
	= IN	= 21MX M-Series

4-1. TEST DESCRIPTION

4-2. TEST 00

Tests the ability of memory protect (when enabled) to disallow a halt instruction to be executed. If a halt is allowed (illegally), the computer will halt 102026 (octal) with no error message reported.

4-3. TEST 01

SUBTEST 1. Basically tests the ability to set the fence register to the value 4. Proper setting of the fence is verified by attempting to store (legally) at address 4 and then storing (illegally) at address 3.

SUBTEST 2. Verifies that address 3 was not altered by the illegal store attempt in Subtest 1.

4-4. TEST 02

SUBTEST 1. Tests the ability of memory protect to generate an interrupt on an illegal I/O instruction (LIB 0).

SUBTEST 2. Verifies that the B-register was not altered to zero by the illegal I/O instruction in Subtest 1.

4-5. TEST 03

SUBTEST 1. Tests that no memory protect interrupt occurs with memory protect control off.

SUBTEST 2. Verifies that memory protect is not enabled by any STC instruction except STC 5.

4-6. TEST 04

Tests the ability of memory protect to allow the execution of an I/O instruction in a trap cell and to ensure that this trap cell I/O instruction does not turn off memory protect control.

4-7. TEST 05

Verifies that interrupts are enabled after the third level of a multilevel indirect jump instruction.

4-8. TEST 06

This test is performed only on a 21MX computer when the related DMS tests were selected during configuration. A memory expansion violation is created and the MEXFL skip flag logic is tested with the MEXFL Flip-Flop set. A second test will be performed to ensure the MEXFL skip flag logic is good with the MEXFL Flip-Flop clear.

4-9. TEST 07

Tests the ability of the fence and violation registers to be set to all values from the end of the test control program to the beginning of the Configurator. The ability of the memory protect violation detection circuitry is also tested at each fence register setting.

4-10. TEST 08

Verifies that all non-violating instructions can be executed without a memory protect interrupt. The following instruction groups are always tested:

a. Memory Reference
b. Shift-Rotate
c. Alter-Skip
d. Input/Output
e. Extended Arithmetic
f. Floating Point (if installed in the 2100A/S)

If the test computer is not a 2100A/S, the Extended Instruction group is also tested.

4-11. TEST 09

Verifies that all violating instructions will generate a memory protect interrupt. These instructions include:

a. Memory Reference (STA/B, JMP, JSB, ISZ)
b. EAU (DST)
c. Input/Output (non-select code 01)

If the test computer is not a 2100A/S, the following Extended Instruction group instructions are tested:

SAX,SBX,SAY,SBY,STX,STY,JPY,JLY,CBS,SBS,MVW,MBT,SBT

4-12. TEST 10

Test 10, Subtests 1 through 7 will verify proper parity error halt and interrupt logic.

SUBTEST 1.

a. The computer will halt with a 106000 which instructs the operator to set the parity halt/interrupt mode switch to parity-halt, set the power fail/auto restart switches to auto

restart, force even parity on the Memory Controller PCA (Data Control PCA if 2100A/S), and press PRESET and RUN.

In a 2100A/S or 21MX M-Series, the computer should halt with 5 (octal) displayed in the T-register and the front panel PARITY lamp on. In the 2100A/S, the parity bit lamp located on the Data Control PCA should also be on.

In a 21MX E-Series, the value in the T-register depends on the memory option and whether or not MEM is installed. Therefore, the only visual indication that the parity-error-halt test has been executed will be that the PARITY lamp will be on and the CPU halted.

The operator must now set the parity halt interrupt switch to interrupt, and press PRESET and RUN. The computer should halt 106001. This halt instructs the operator to power down the computer, remove the even parity jumper previously installed, install jumpers in accordance with table 3-1 if testing a 12892B and Test 11 is to be executed, and power up the computer. Testing will now resume automatically.

b. The diagnostic ensures that a parity error will not interrupt with the Power Fail Control Flip-Flop clear.

c. Verifies that parity error can generate an interrupt and strobe the violation register properly.

d. Ensures that a parity error interrupt turns off the parity error logic.

e. Verifies that an STF 5 turns on the parity error logic and that parity is not restored after a load type instruction.

f. Verifies that a CLF 5 disables parity error.

SUBTEST 2.

a. Ensures that a parity error does not occur on a store type instruction.

b. Verifies that good parity is restored after a store type instruction.

SUBTEST 3. Tests the ability of the parity error logic to override memory protect when both occur together.

SUBTEST 4. Ensures that a parity error will hold off an I/O interrupt.

SUBTEST 5. Tests that no parity errors are detected when accessing non-existent memory (is tested only with memory sizes $\leq$ 28K).

SUBTEST 6. Tests the ability of the parity error violation register to latch the proper address of an indirect address parity error.

SUBTEST 7. Verifies proper operation of the separate parity error violation register (if 12892B).

4-13. TEST 11

Test 11 is a special hardware test only for 12892B. Operator must select this test. Refer to paragraph 3-4.

SUBTEST 1. Ensures that memory protect will not allow a JSB 0 or JSB 1 to be executed when the JSB Jumper is removed.

SUBTEST 2. Verifies that all I/O instructions (except halt) are allowed by memory protect if the INT Jumper is removed.

SUBTEST 3. Verifies that when the INT jumper is removed from the 12892B board, an I/O interrupt will occur immediately after a STC 5 instruction.

4-14. TEST 12

If DCPC is installed, this test ensures that no memory protect interrupt occurs during a DCPC transfer into protected memory.

4-15. TEST 13

Tests the ability of preset to reset the Memory Protect Control Flip-Flop. If a console is present, a message will be reported instructing the operator to press HALT, PRESET, and RUN within 30 seconds. The EXTEND lamp will flash approximately every one-half second until 30 seconds have elapsed. (This is the only indication if no console is available.) If preset fails to clear memory protect control, the Display Register will alternately flash all ones and all zeros indefinitely to indicate this error.

4-16. HALT CODE SUMMARY

The diagnostic communicates to the operator through the console, via a CPU halt, or both, based on configuration and Switch Register settings. Thus, messages consist of halt codes (T-register and A-register values) and/or output to the console. Table 4-1 lists octal halt codes and their meanings.

4-17. MESSAGE SUMMARY

Table 4-2 lists diagnostic messages in diagnostic message order number. The test that outputs each message is also indicated in the same table. "TC" refers to the Test Control program; otherwise, the numbers refer to the test number.

Table 4-1. Halt Code Summary

HALT	MEANING
102026-102062	Error (E) and information (H) messages 26-62 (octal) described in table 4-2.
106000-106013	Error (E) and information (H) messages 100-113 (octal).
107001-107014	Error (E) and information (H) messages 301-314 (octal).
CONTROL	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test. (A = test number.)
102077	End of diagnostic run.
106077	Trap cell halts in location 2-77 (octal).
106070-106076	Configurator halts. Refer to Diagnostic Configurator Manual.
Note: Refer to table 4-2 for complete explanation of individual halts.	

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102073	Initialization	None	I/O select code entered during configuration is invalid. Must be greater than 7 (octal). Reenter a valid select code and press RUN.
102074	Initialization	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	TC	None	Test selection resulting from Switch Register bit 9 being set. Enter in A-register desired group of tests to be executed and press RUN. (Refer to table 3-3.)
102076	TC	None	End-of-test halt resulting from Switch Register bit 15 being set. (A-register contains test number.) To continue, press RUN.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102077	TC	PASS xxxxxx	Diagnostic run complete. Register options can be changed. (A-Register has the pass count.) Set all jumpers and switches to their original positions. To continue, press RUN.
106077	TC	None	Halts stored in location 2-77 (octal) to trap interrupts which can occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded. The problem should be corrected before proceeding.
None	TC	MEMORY PROTECT-PARITY ERROR DIAGNOSTIC	Header message. Output at initial start of diagnostic.
None	TC	TEST xx	Information message before error messages (xx = test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102026	00	None	MPT allowed halt to execute.
102027	06	None	MEM has been specified during configuration but hardware is not installed or is faulty.
102030	01-03,09	E030 INVALID VIOLATION REGISTER EXPECTED=xxxxxx ACTUAL=xxxxxx FENCE=xxxxxx	Violation Register not as expected. A-register = expected VR. B-register = actual VR. Press RUN. When no console is used and halt E030 occurs, the A-register contains the expected VR and the T-register contains the actual VR. The operator then presses RUN and halt 102060 occurs. The A-register contains the Fence Register. Press RUN to continue.
102031	01,02, 07-09	None	This halt is used to trap when intended violation did not occur.
102032	TESTS 1-3, 9	E032 NO MEMORY PROTECT INTERRUPT ON VIOLATING INSTRUCTION AT ADDRESS xxxxxx	The instruction found at ADDR xxxxxx did not cause an MPT violation. (This halt is also reached if incorrect jumper setting on 12892B.)

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102033	01	E033 MEMORY ALTERED BY ILLEGAL STB INSTRUCTION	A store instruction below the fence caused an MPT interrupt, but was allowed to execute.
102034	02	E034 B-REG NOT ALTERED BY ILLEGAL LIB	An LIB instruction caused an MPT interrupt, but was not allowed to execute.
102035	03	E035 INTERRUPT ON LIA 0 WITH MPT OFF	An MPT violation occurred with memory protect control (MPC) off.
102036	03	E036 LIA NOT ALLOWED WITH MPT OFF	No MPT interrupt occurred, but an LIA instruction was not allowed with MPC off.
102037	03	E037 ILLEGAL DECODE OF OF SELECT CODE FIVE	A-register contains the instruction that turned on MPC (simulated STC 5).
102042	05	E042 I/O INTERRUPT AFTER SECOND LEVEL INDIRECT	Interrupts were enabled after the second level indirect of a multi-level indirect jump instruction.
102043	05	E043 I/O INTERRUPT AFTER FIRST LEVEL INDIRECT	Interrupts were enabled after the first level indirect jump instruction.
102044	05	E044 NO I/O INTERRUPT ON MULTI-LEVEL INDIRECT	No interrupts were allowed after three levels of indirect.
102046	06	E046 NO SKF ON SFS 5 AFTER MEM VIOLATION	With MEXFL Flip-Flop set, an SFS 5 did not skip.
102047	06	E047 ILLEGAL SKF ON SFC 5 AFTER MEM VIOLATION	With MEXFL Flip-Flop set, an SFC 5 caused an legal skip.
102050	06	E050 ILLEGAL SKF ON SFS 5 WITH NO MEM VIOLATION	With MEXFL Flip-Flop clear, an SFS 5 caused an illegal skip.
102051	06	E051 NO SKF ON SFC 5 WITH NO MEM VIOLATION	With MEXFL Flip-Flop clear, an SFC 5 did not skip.
102052	06	E052 NO MEM VIOLATION	An XMA instruction with memory protect on did not cause a MEM violation.
102053	08	E053 LEGAL INSTRUCTION AT ADDRESS xxxxxx CAUSED AN MPT VIOLATION	A-register = violating instruction. B-register = address of violating instruction.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102054	04	E054 I/O TRAP CELL INST ERR	I/O instruction (CLF CH) in an I/O trap cell turned off memory protect or I/O device failed to interrupt.
102060	00-03,09	None	Secondary halt A = Fence Register. This halt only occurs if no console is used. After HLT E030, RUN is pressed and halt 102060 occurs. Refer to halt 102030.
102061	11	H061 POWER DOWN COMPUTER INSTALL JUMPERS PER TABLE 3-5 IN MOD POWER UP COMPUTER	12892B only. Test 11 is not a standard test. When selected and Test 10 is not executed, the message/halt occurs. The operator powers down the CPU, changes the jumpers per paragraph 3-2c, and then powers up the CPU. Testing will resume automatically.
102062	11	H062 POWER DOWN COMPUTER SET JUMPERS TO INITIAL SETTINGS PER TABLE 3-1 IN MOD POWER UP COMPUTER	After Test 11 has completed and before the diagnostic has come to halt 102077, this message indicates to the operator to set back the jumpers to the initial settings. The operator powers down the CPU, reinstalls the jumpers, and powers up the CPU. The CPU will then halt with 102077 indicating end of diagnostic pass. Press RUN for another diagnostic pass.
106000	10	H100 FORCE EVEN PARITY ON THE MEMORY CONTROLLER. SET PE SWITCH TO HALT MODE. PFAR SWITCH TO AUTO-RESTART. PRESS PRESET RUN.CPU HALTS WITH 5 OR 106000 IN T-REG. PARITY LAMP ON. SET PARITY HALT SWITCH TO INTP. PRESS PRESET, RUN – HALT 106001 SHOULD OCCUR. FOLLOW INSTRUCTION IN MOD FOR HALT 106001	Informs operator to ready the computer for a parity error test section. Refer to paragraph 4-12. When the parity halt occurs in a 21MX-E Series with Hi Speed Memory, the value (5 or 106000) in the T-Register will be invalid. The only indication that the test has been executed is the PARITY lamp will be on and the CPU halted.
106001	10	None	Informs operator to remove the even parity jumper and to power down the computer. If 12892B and Test 11 has been selected, change the jumpers as specified in paragraph 3-2c. Power up the computer. Testing will continue automatically.
106002	10	E102 PE INT WITH CNTL 4 CLEAR	With power fail disabled, an illegal PE interrupt occurred.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
106003	10	E103 NO PE INTP WHEN ACCESSING ADDRESS XXXXXX	A-register = address which contains undetected bad parity.
106004	10	E104 PE NOT TURNED OFF BY PE INTP	A previous PE did not disable the PE logic.
106005	10	E105 STF 5 DOES NOT ENABLE PE OR LOAD INSTRUCTION RESTORED GOOD PARITY.	A previous LDA/B instruction illegally restored good parity or an STF 5 did not enable PE.
106006	10	E106 CLF 5 FAILED	CLF 5 did not disable PE.
106007	10	E107 PE ON STORE INSTRUCTION	Parity errors should not occur on store memory operations.
106010	10	E110 PARITY NOT RESTORED BY STORE INSTRUCTION	A store memory operation should restore good parity.
106011	10	E111 PE DID NOT OVERRIDE MPT	When an address generates a parity error and MPT violation, PE should override the Violation Register. In addition to a problem on the 12892 PCA, error can be caused by a faulty memory controller PCA.
106012	10	E112 PE DID NOT BREAK PRIORITY CHAIN	A parity error should break the priority chain.
106013	10	E113 PE FROM NON-EXISTENT MEMORY	A read from non-existent memory generated a PE (A-register = address causing PE).

Note: Test 11 is executed only if the test has been explicitely selected and the PCA board is a 12892B. (Refer to Table 3-2 and 3-3.)

106070-106076 Configurator Halts. See Diagnostic Configurator Manual.

107001	10	E301 NO PE INT ON INDIRECT	An indirect address contained bad parity, but did not generate a PE.
107002	10	E302 MPT INDIRECT LOGIC HELD OFF I/O INTP	INT jumper (out) should allow immediate interrupts.
107005	11	E305 JSB 0 ALLOWED	JSB jumper (out) should not allow a JSB 0 to execute.
107006	11	E306 JSB 1 ALLOWED	JSB jumper (out) should not allow a JSB 1 to execute.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
107007	11	E307 LEGAL INSTRUCTION AT ADDRESS XXXXXX CAUSED AN MPT VIOLATION	A legal I/O instruction has caused an MPT violation.
107013	11	E313 MPT VIOLATION DURING DCPC TRANSFER	DCPC (DMA) transfers into protected memory should not cause an MPT violation.
None	12	H314 PRESS HALT, PRESET AND RUN WITHIN 30 SECONDS	Follow message instructions. If no console is used, these instructions must be executed when the Extend Register flashes approximately every 1/2 second.
None	13	None	If PRESET failed to clear MPC, the Switch Register will flash alternately all ones and all zeros indefinitely.

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