ABSOLUTE BINARY PROGRAM 13197-16002
DATE CODE 1640

HP 13197A WRITABLE CONTROL STORE DIAGNOSTIC

reference manual

For 21MX Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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SECTION I
INTRODUCTION

1-1. GENERAL

The HP 13197A Writable Control Store (WCS) Diagnostic verifies proper operation of the HP 13197A Writable Control Store Kit used with HP 21MX M-Series and E-Series Computers. The program also indirectly checks the computer Control Memory priority chain.

1-2. REQUIRED HARDWARE

The required hardware consists of the following:

a. An HP 21MX M-Series or E-Series Computer with a minimum 4K of memory.

b. A loading device for the diagnostic.

c. An HP 13197A Writable Control Store Kit.[1]

d. A Dual-Channel Port Controller is optional.

e. A system console device is optional but recommended for report and error message output.

1-3. SOFTWARE REQUIREMENTS

The following software is required:

a. The Diagnostic Configurator (part numbers listed below) is used for equipment configuration and as a console device driver.

   Absolute binary program, part no. 24296-60001
   Reference Manual, part no. 02100-90157

b. 13197A WCS Diagnostic

   Absolute binary program, part no. 13197-16002
   Reference Manual, part no. 13197-90002

The diagnostic serial number (DSN) for this diagnostic is 103023 and is contained in memory location 126 (octal).

[1]Jumper W1 must be installed for 21MX E-Series; jumper W1 must be removed for 21MX M-Series. (See *13197A Writable Control Store Kit Reference Manual*, part no. 13197-90005.)

1-4. TEXT CONVENTIONS

All halt codes, select codes, and addresses used in this manual are octal unless specifically shown otherwise. All references to control memory are to be taken as synonymous with control store. The abbreviations used are listed below:

CMAR — Control Memory Address Register (same as ROM Address Register — RAR)
DCPC — Dual-Channel Port Controller
EIG — Extended Instruction Group
I/O — Input/Output
LHJ — Left-Hand Justified
LI* — An LIA or LIB instruction
LSB — Least Significant Bits
MIR — Microinstruction Register (same as ROM Instruction Register — RIR)
MOD — Control Memory Module (256_{10} microinstructions in length)
MSB — Most Significant Bits
OT* — An OTA or OTB instruction
RAM — Random Access Memory
RHJ — Right-Hand Justified
WCS — Writable Control Store

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic program contains a Control section, and Initialization section, 21 (decimal) standard tests (TST00-TST24), and one optional test (TST25).

2-2. TEST CONTROL AND EXECUTION

The program executes the tests according to the options selected in the S-register by the operator. The control section mainly supervises S-register bits 15, 13, and 12. The program also keeps count of the number of passes that have been completed and loads the A-register with the pass count at the completion of each pass. The count is cleared whenever the program is restarted. Tests are executed one after another in each diagnostic pass.

2-3. SELECTION OF TESTS BY OPERATOR

User selection or default will determine which tests will be executed. The operator may select his own test or tests to be executed via S-register bit 9. Paragraph 3-4 outlines the procedures and default tests.

2-4. MESSAGE REPORTING

There are two types of messages: error and information. Error messages are used to inform the operator of a failure within the hardware. Information messages are used to inform the operator of the progress of the diagnostic and for information about the diagnostic.

When a console device is used, the printed message will be preceded by an E (error) or H (information) letter prefix and a three-digit octal number. The two least-significant digits of this number are the same as the last two octal digits of an associated halt code.

Example — Error with halt

Message: E001 BAD COMMAND STATE
Halt Code: 102001 (T-register)

Example — Information with halt

Message: H033 PRESS PRESET,RUN
Halt Code: 102033 (T-register)

Example — Information without halt

Message: H054 NO MEMORY PROTECT
Halt Code: None

Error messages can be suppressed by setting S-register bit 11 and error halts can be suppressed by setting S-register bit 14. Information messages are suppressed by setting S-register bit 10.

2-5. PROGRAM LIMITATIONS

The microprograms to be executed from WCS will have recovery capability in the event of power fail, parity error, bad WCS hardware, etc. However, the microprograms cannot guarantee recovery back to program control in all cases. If the diagnostic is trapped in the microcode, the user has no alternative but to power off and determine the source of the malfunction.

All possible CMAR lines are not addressed when executed in a 21MX M-Series Computer (2105/2108/2112). The base set in MOD's 0 and 1 is not overlayed.

If DCPC is not present, the direct memory loading feature of WCS will not be checked.

The optional User Looping Test (TST25) will accept up to 32 (decimal) microinstructions. The user is responsible for correct selection of RAM addresses, MOD numbers, or micro-jump placement.

OPERATING PROCEDURE

SECTION III

3-1. OPERATING PROCEDURE

Before running the diagnostic, turn the computer power off and check that WCS board jumper W1 is configured for the proper computer. (Refer to paragraph 1-2c.) Check also that the flat ribbon cable assembly, part no. 5060-8393, is installed and attached firmly to the WCS board and the CPU. A flowchart of the operating procedure is provided in figure 3-1.

3-2. RUNNING THE DIAGNOSTIC

The program configuration S-register setting is listed in table 3-1. The program options are listed in table 3-2.

At the completion of each pass of the diagnostic, the pass count is output to the A-register for operator information. If S-register bit 12 was clear, the computer will halt with 102077 in the T-register. To run another pass, press RUN.

If the optional User Looping Test (TST25) is selected, the program will remain in TST25 until S-register bit 7 is set. The operating procedure for TST25 is provided in figure 3-2. Note that microcode loaded and executed from TST25 is not checked for content or correctness and is used exactly as entered. The test allows the user to loop on RAM data via either I/O instructions or execution of microcode.

If a trap cell halt occurs (T-register = 106077), the user must determine the cause of the interrupt or transfer of control to the location in the M-register. The program may need to be reloaded to continue.

Refer to table 4-1 for halts and messages and to table 4-2 for test execution times.

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000, selecting the desired program options per table 3-2 in the S-register and pressing PRESET, RUN. The program may be reconfigured and restarted by setting the P-register to 100, selecting the program configuration per table 3-1 in the S-register and pressing PRESET, RUN. Refer to figure 3-1.

3-4. TEST SELECTION BY OPERATOR

The control portion of the program allows the operator the option to select a test or sequence of tests to be run. The operator sets S-register bit 9 and presses RUN. If the computer is running already, the test in progress will be completed and then the program will halt 102075. The operator loads the A- and B-registers with the tests desired per table 3-3. The operator then must clear S-register bit 9 and press RUN. The operator selected test(s) will then be executed. If the operator clears all the bits in the A- and B-registers, the default set of tests (TST00-TST24) will be run.

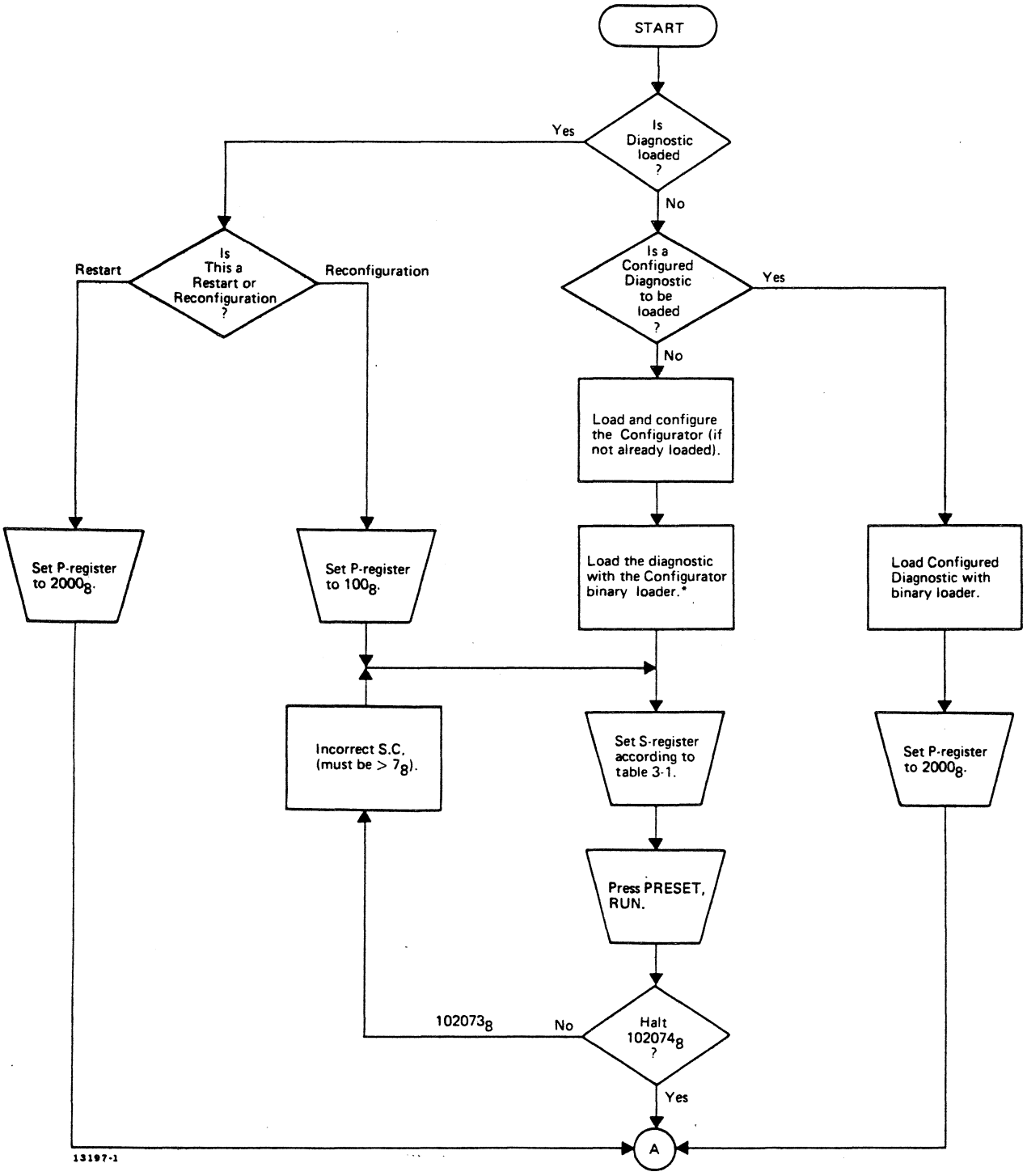

Figure 3-1. TST00-TST24 Operating Procedure Flowchart (Sheet 1 of 2)

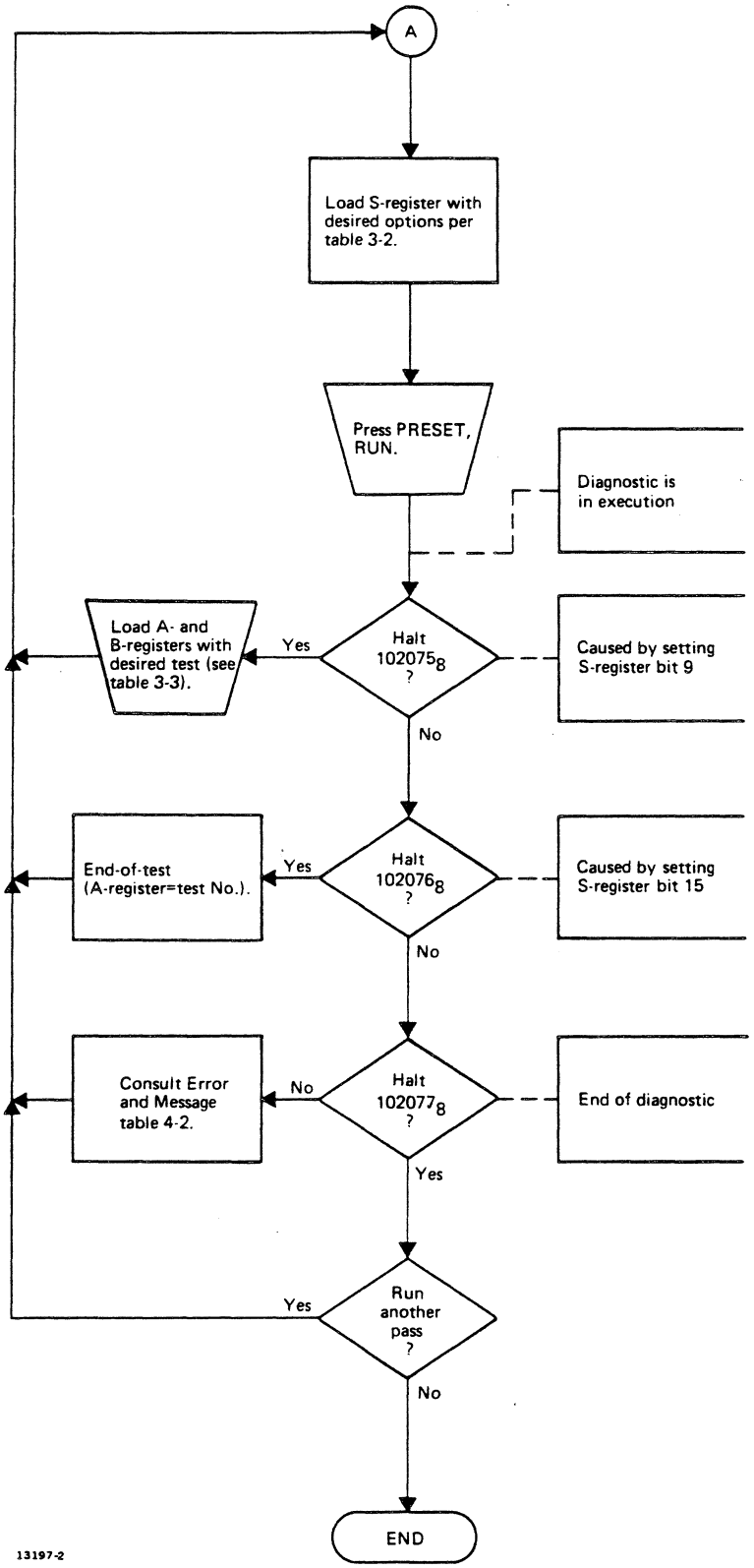

Figure 3-1. TST00-TST24 Operating Procedure Flowchart (Sheet 2 of 2)

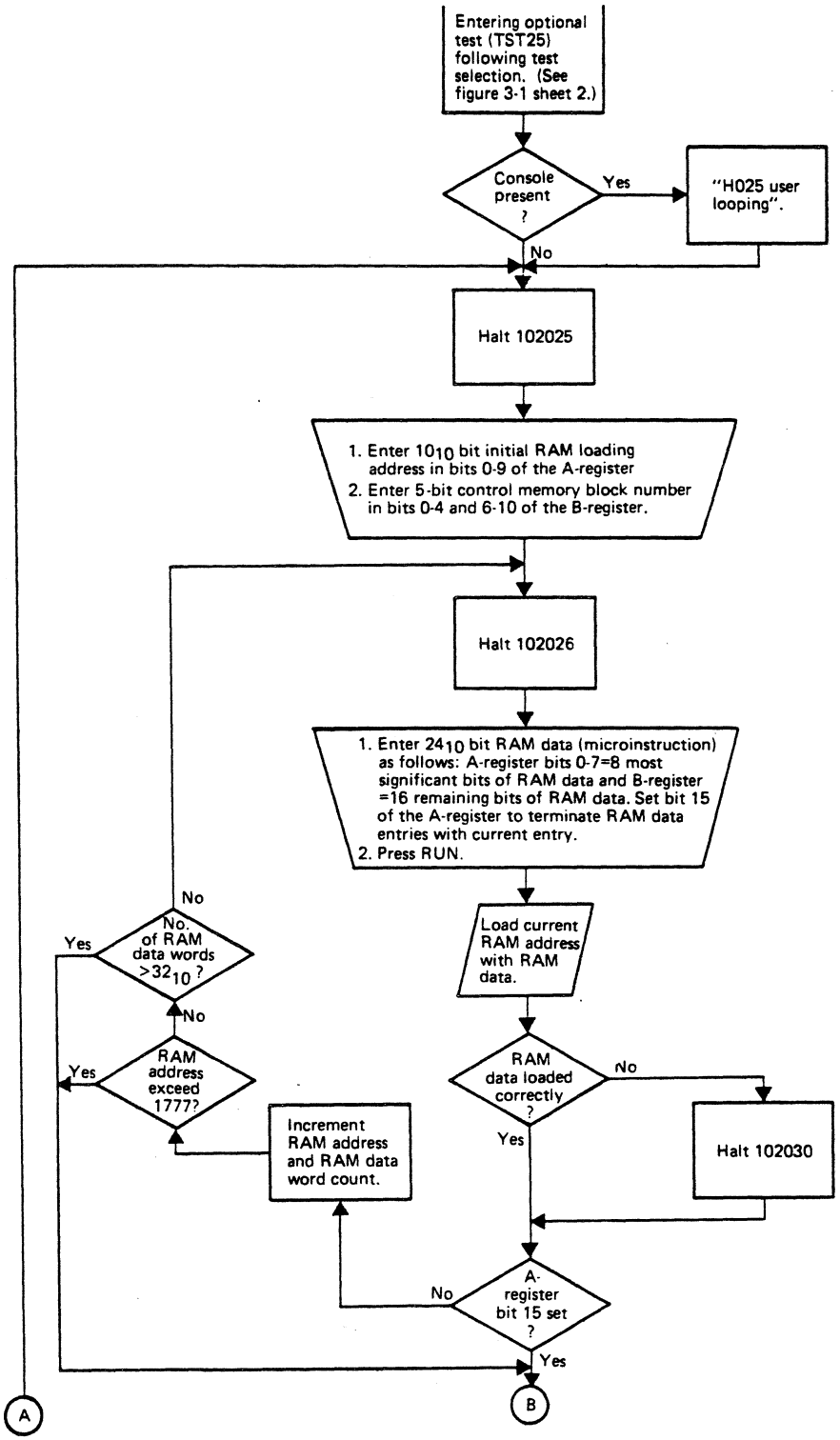

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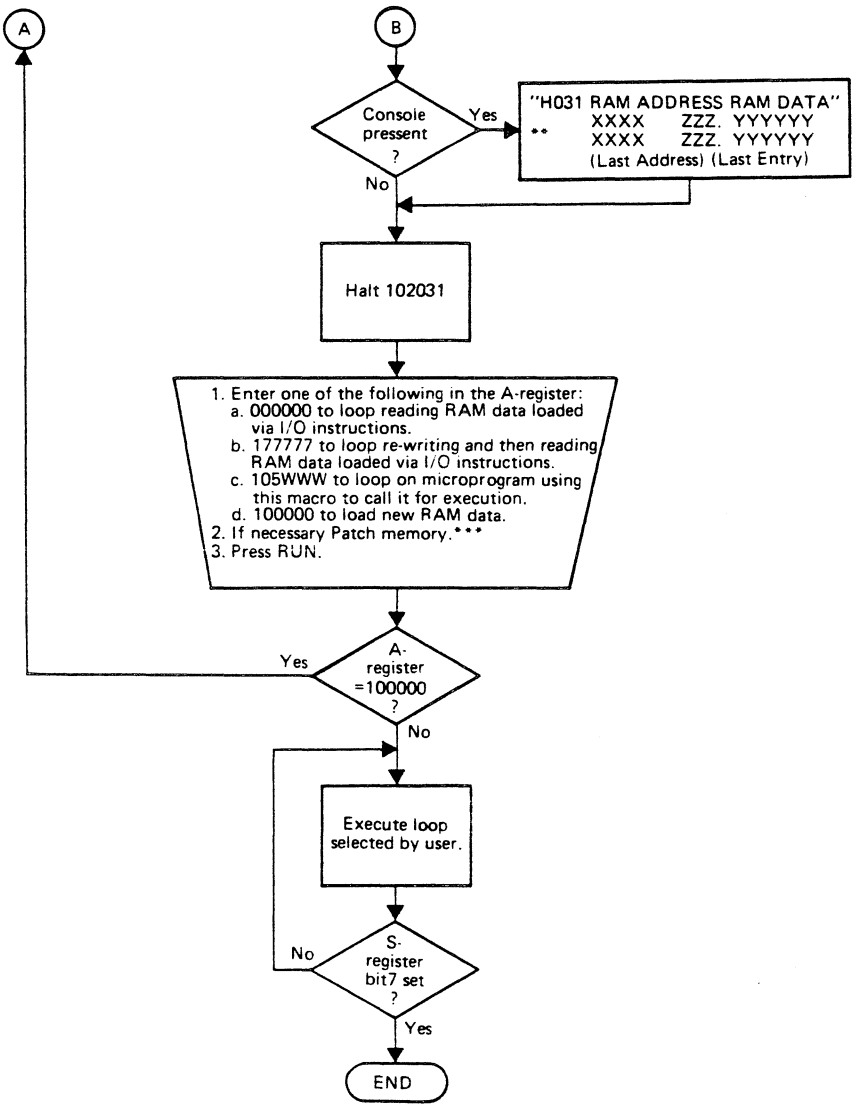
Figure 3-2. TST25 Operating Procedure Flowchart (Sheet 1 of 2)



** XXXX = 4-digit (octal) RAM address (0-1777)
ZZZ = 8 most significant bits of RAM data word (in octal)
YYYYYY = 16 least signifcant bits of RAM data word (in octal)
ZZZ. YYYYYY = RAM data word (i.e.,24_{10} bit microinstruction)

*** If the microprogram is to use any special memory locations, registers or return other than P+1, then the user must patch memory with his own instructions as required. The execution of the macro-call is located as follows:

MEMORY ADDRESS	CONTENTS	COMMENTS
6000	NOP	May be used to load any registers with desired values.
6001	NOP	
6002	NOP	
6003	NOP	
6004	105WWW	Macro-call supplied at halt 102031.
6005	NOP	
6006	NOP	May be used for halts or required parameters.
6007	NOP	
6010	NOP	

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Figure 3-2. TST25 Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Initial S-Register Settings

BITS	FUNCTIONS
5-0	Enter select code of WCS board. Select code must be 10, 11, or 12 (octal) depending on where WCS board is physically installed.
15-6	Reserved

Table 3-2. S-Register Options

BITS	MEANING IF SET
6-0	Reserved
7	Abort TST25 and end current pass of diagnostic.*
8	Suppress tests requiring operator intervention.
9	Abort diagnostic execution at end of current test section and halt 102075. User may specify a new group of tests in the A-register. (See table 3-3.) Clear S-register bit 9 and press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Loop on diagnostic. Message "H077 PASS xxxxx" is printed if a console is present. (Eliminates automatically all tests that require operator intervention.)
13	Repeat last test section.
14	Suppress error halts.
15	Halt 102076 at the end of each test. The A-register contains the test number in octal.

*Setting of bit 7 applies only when executing TST25.

Table 3-3. Test Selection Via A- and B-Registers

A-REG BIT	IF SET WILL EXECUTE
0	TST00 — Basic Load Test
1	TST01 — Command State Test
2	TST02 — Data Mode Screen Test
3	TST03 — Command State Screen Test
4	TST04 — I/O Screen Test
5	TST05 — RAM Address Rollover Test
6	TST06 — Preset Test
7	TST07 — Zeros Data Test
8	TST10 — Ones Data Test
9	TST11 — Lonely Bit Data Test
10	TST12 — RAM Address Parity Test
11	TST13 — RAM Checkerboard Test
12	TST14 — Alternate Word Data Test
13	TST15 — DCPC Test
14	TST16 — Control Memory Priority Test
15	TST17 — WCS Enable/Disable Test
B-REG BIT	**IF SET WILL EXECUTE**
0	TST20 — WCS Enable/Disable Screen Test
1	TST21 — Command State Alteration Test
2	TST22 — Block Priority Test
3	TST23 — RAM Data Test
4	TST24 — RAM MOD Decoder Test
5	TST25 — User Looping Test
6-15	Reserved

Note: If the A- and B-registers are clear, the default set of tests (TST00 through TST24) are run. TST25 is an optional test.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

The tests in this diagnostic are described in the following paragraphs. Table 4-1 contains a list of the halts and messages. Table 4-2 contains the various test execution times. The microinstructions used in the following tests will depend on whether the computer is a 21MX M-Series or 21MX E-Series.

4-2. BASIC LOAD TEST — TST00

The entire RAM storage (RAM addresses 0-1777) is loaded and verified via I/O instructions using a return microinstruction for RAM data.

4-3. COMMAND STATE TEST — TST01

The entire RAM storage is loaded and verified via I/O instructions to a data pattern equal to a return microinstruction. WCS is then placed in the command state and subjected to a series of OT* instructions and then checked to verify that the RAM address is the one loaded by the last OT*.

4-4. DATA MODE SCREEN TEST — TST02

The entire RAM storage is loaded and verified via I/O instructions to a data pattern equal to a return microinstruction. WCS is then placed in the command state and subjected to a series of OT* instructions. The RAM's are then verified again to ensure no RAM data has been altered.

4-5. COMMAND STATE SCREEN TEST — TST03

WCS is placed in the command state and subjected to a series of LI* instructions and then checked to verify that the RAM address is not incremented.

4-6. I/O SCREEN TEST — TST04

WCS is placed in the command state and all other select codes are issued a STC. WCS is then checked to verify that STC did not erroneously place WCS in the data mode.

4-7. RAM ADDRESS ROLLOVER TEST — TST05

RAM storage is loaded using more than 1024 (decimal) OT* instructions in the data mode. The RAM data is then examined for proper RAM address rollover.

4-8. PRESET TEST — TST06

WCS is placed in the data mode, the computer is halted, and the operator presses PRESET, RUN. WCS is then checked to verify that it is in the command state.

4-9. ZEROS DATA TEST — TST07

All the RAM locations are loaded and verified via I/O instructions to a data pattern of all zeros, and a one is rippled through a field of 23 (decimal) zeros.

4-10. ONES DATA TEST — TST10

All the RAM locations are loaded and verified via I/O instructions to a data pattern of all ones and a zero is rippled through a field of 23 (decimal) ones.

4-11. LONELY BIT DATA TEST — TST11

All RAM locations are loaded and verified via I/O instructions using a data pattern of all ones or all zeros to create a pattern of 1023 (decimal) ones and 1 zero on the RAM chips. The same pattern is repeated 1024 (decimal) times, rotating the zero position each time. The entire process is then repeated using 1023 (decimal) zeros and 1 one on the RAM chips.

4-12. RAM ADDRESS PARITY TEST — TST12

All RAM addresses are loaded and verified via I/O instructions using the parity of the RAM address for data. Using odd parity as an example, each RAM location would contain all zeros for an odd number of bits in the RAM address or all ones for an even number of bits in the RAM address. This test is run using even and odd parity.

4-13. RAM CHECKERBOARD DATA TEST — TST13

All the RAM locations are loaded and verified via I/O instructions using a data pattern of all ones or all zeros to create a checkboard pattern on the 32 × 32 (decimal) array of the RAM chips.

4-14. ALTERNATE WORD DATA TEST — TST14

All RAM locations are loaded and verified via I/O instructions in an alternating OT*, LI*, OT*, LI*, etc. sequence using data patterns of alternating ones, zeros, ones, zeros, etc.

4-15. DCPC TEST — TST15

If DCPC is present, a check of the DCPC flag circuitry is made and then a number of DCPC transfers to all RAM locations are performed. Data transferred to WCS via DCPC is verified via I/O instructions.

4-16. CONTROL MEMORY PRIORITY TEST — TST16

WCS is loaded with microprograms to give unique responses to specific maps in microcode. WCS is then turned on to overlay the module that contains the Floating Point Instruction Group. (This is the first time in the execution of the diagnostic that the WCS board is turned on by a STF WCSSC.) Macroinstructions which map to that module are then executed to verify WCS priority over firmware.

4-17. WCS ENABLE/DISABLE TEST — TST17

WCS is loaded with microprograms to give unique responses to macroinstructions which map to a unique address in WCS control memory. The enable/disable WCS controls are then verified by attempting various macroinstructions with WCS enabled or disabled.

4-18. WCS ENABLE/DISABLE SCREEN TEST — TST20

WCS is enabled/disabled and subjected to a series of I/O instructions to verify that the enable/disable circuitry is not affected and that an I/O instruction to WCS will execute the microinstruction to which the counter is pointing.

4-19. COMMAND STATE ALTERATION TEST — TST21

WCS is put in the command state and subjected to a series of OT*'s. A macroinstruction is then executed to verify that the command state is set to the MOD dictated by the last OT*.

4-20. BLOCK PRIORITY TEST — TST22

Both 512 (decimal) WCS RAM data blocks are set to the same MOD's in control memory. A macroinstruction to the MOD's is then executed to verify that the high block (RAM addresses 1000-1777) has priority.

4-21. RAM ADDRESS DECODER AND DATA TEST — TST23

WCS is loaded with microprograms which are lengthy and exercise all MIR lines. A macroinstruction then calls these programs.

4-22. RAM MODULE DECODER TEST — TST24

WCS is loaded with microprograms which perform a series of micro JSB's to all modules. This checks that all modules can be accessed and the module decoders work correctly. The only modules not tested are modules 0 and 1 in the 21MX M-Series (2105/2108/2112) and modules 0 through 3 in the 21MX E-Series (2109/2113).

4-23. USER LOOPING TEST — TST25

Allows the user to loop on any RAM address with any RAM data. Also provides capability to write and call microprograms loaded using a utility WCS driver and microcode object code.

4-24. HALTS AND MESSAGES

Table 4-1 lists diagnostic halts and messages in test order number. The test that outputs each message is also indicated in the same table. "TC" refers to the Test Control program; otherwise, the numbers refer to the test number. Table 4-2 lists the maximum execution time required to run each test in a 21MX M-Series Computer. Table 4-3 tabulates the RAM data error microcode.

Table 4-1. Halts and Messages

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102000	00	E000 BAD LOAD RAM ADDRESS=xxxx DATA LOADED=zzz.yyyyyy DATA READ=vvv.wwwwww	WCS loaded incorrectly. At RAM address xxxx the data loaded was zzz.yyyyyy and the data read is vvv.wwwwww. (Note 1)
102001	01	E001 BAD COMMAND STATE	The RAM address counter was not set up correctly by an OT* in the command state.
102002	02	E002 BAD LOAD RAM ADDRESS=xxxx DATA LOADED=zzz.yyyyyy DATA READ=vvv.wwwwww	An OTA to WCS in the command state altered data in the RAM's. At RAM address xxxx the data loaded was zzz.yyyyyy and the data read is vvv.wwwwww. (Note 1)
102003	03	E003 BAD COMMAND STATE	With WCS in the command state a series of LI* instructions altered the RAM address counter.
102004	04	E004 SELECT CODE FAILURE	WCS responded to a STC issued to another select code. A-register = other select code.
102005	05	E005 BAD LOAD RAM ADDRESS=xxxx DATA LOADED=zzz.yyyyyy DATA READ=vvv.wwwwww	WCS RAM address counter did not rollover correctly. At RAM address xxxx the data loaded was zzz.yyyyyy and the data read is vvv.wwwwww. (Note 1)
102006	06	E006 BAD COMMAND STATE	PRESET or CLC 0 did not put WCS into the command state.
102007 102010 102011 102012 102013 102014	07 10 11 12 13 14	E0uu BAD LOAD RAM ADDRESS=xxxx DATA LOADED=zzz.yyyyyy DATA READ=vvv.wwwwww	In TSTuu (07-14), WCS was loaded incorrectly. At RAM address xxxx the data loaded was zzz.yyyyyy and the data read was vvv.wwwwww. (Note 1)
102015	15	E015 BAD LOAD RAM ADDRESS=xxxx DATA LOADED=zzz.yyyyyy DATA READ=vvv.wwwwww	WCS was loaded incorrectly via a DCPC transfer. At RAM address xxxx the data which should have been loaded was zzz.yyyyyy and the data read was vvv.wwwwww. (Note 1)
102016	16	E016 NO PRIORITY	WCS set to overlay Floating Point module and did not hold off execution of a floating point instruction. WCS may not have been enabled. Check flat cable assembly.
102017	17	E017 WCS NOT ENABLED (DISABLED)	WCS enable/disable circuitry failed.
102020	20	E020 WCS NOT ENABLED (DISABLED)	An I/O instruction (not STF or CLF) altered the state of the WCS enabled/disabled circuitry.
102021	21	E021 BAD COMMAND STATE	With WCS in the command state, a series of OT* instructions modified the MOD for which WCS was set. A-register = MOD number for which WCS should be set.
102022	22	E022 BAD WCS PRIORITY	Both 512 (decimal) word blocks on WCS were set to the same MOD and the high block failed to have priority over the low block.

Table 4-1. Halts and Messages (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102023	23	E023 BAD MOD MOD NUMBER uu RAM ADDR MICRO-OBJECT CODE xxxx zzz.yyyyyy xxxx zzz.yyyyyy	An error occurred in microcode execution with WCS set up for MOD number uu. The microcode attempted is located in locations xxxx and is zzz.yyyyyy. (Note 2)
102024	24	E024 BAD MOD DECODER	An attempt to execute in a specific MOD has failed. A-register contains the last output to the MOD decoders.
102025 (Note 3)	25	H025 USER LOOPING	TST25 has been entered. Enter 10-bit starting RAM address in bits 0-9 of A-register; enter 5-bit number of first block in bits 0-4 of B-register; enter 5-bit number of second block in bits 6-10 of B-register. Press RUN.
102026 (Note 3)	25	None	RAM address for loading is set. Enter 24-bit RAM data word as follows: A-register bits 0-7 = 8 MSB of RAM data word and B-register = 16 LSB of RAM data word. Set A-register bit 15 to terminate RAM data entries and press RUN.
102027	Reserved		
102030 (Note 3)	25	None	WCS RAM data error. Refer to table 4-3 for error registers information. Press RUN.
102031 (Note 3)	25	H031 RAM ADDR RAM DATA xxxx zzz.yyyyyy xxxx zzz.yyyyyy • • • (last) (last)	RAM data entries complete. Starting at RAM address xxxx, the RAM data loaded is zzz.yyyyyy. See figure 3-2 for A-register setting and how to set up loop desired. When loop is set up, press RUN.
102032	Any	E032 BAD RAM OUTPUT	First read of RAM data word picked up a bit(s) in bits 8-15. A-register contains the bit(s) picked up and the B-register contains the RAM address.
102033	06	H033 PRESS PRESET, RUN	Press PRESET, RUN.
102034	15	E034 NO DCPC FLAG	DCPC transfer to WCS did not return a flag at the end of the transfer or no transfer took place. Press RUN to continue and skip TST15.
102035	16 17 20 21 22 23 24	E035 BAD LOAD	WCS RAM data error. Accompanied by message H100 if a console is present. See table 4-3 for error registers information.
102036	16 17 20	E036 BAD MACRO	The FLT (105120) or WCS microcode did not execute correctly. WCS microcode was RTN INC A A. A- and B-registers contain values after macro execution and X- and Y-registers contain contents of A- and B-registers prior to macro execution.
102037	11	E037 BAD ADDRESS RAM ADDRESS xxxx ALTERED ADDRESS yyyy	Address lines on WCS board are shorted or open. A-register = altered address. B-register = address accessed when error occurred.

Table 4-1. Halts and Messages (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102071	Initial-ization	None	An invalid computer type has been selected. Computer must be a 21MX M-Series or 21MX E-Series. The Diagnostic Configurator must be reloaded and configured.
102072	Reserved		
102073	Initial-ization	None	I/O select code entered at configuration was invalid. Must be 10, 11, or 12 (octal). See table 3-1. Reenter valid select code and press RUN.
102074	Initial-ization	None	Select code entered during configuration valid. Enter program options in S-register and press PRESET, RUN.
102075	TC	None	Test selection request resulting from S-register bit 9 being set. Enter into A- and B-registers the desired test(s) to be run (see table 3-3). Clear S-register bit 9 and press RUN.
102076	TC	None	End of test halt resulting from S-register bit 15 being set. The A-register contains the test number of the test just executed.
102077	TC	H077 PASS xxxxxx	Pass number xxxxxx of the diagnostic is complete. A-register contains the pass count equal to xxxxxx. Press RUN to execute another pass.
None	Initial-ization	TSTnn	Information message indicates the test number where the error message nn occurred.

NOTES:

1. A-REG = RAM address
   B-REG (0-7) = 8 MSB of RAM data read
   B-REG (8-15) = 8 MSB of RAM data loaded
   X-REG = 16 LSB of RAM data loaded
   Y-REG = 16 LSB of RAM data read

2. A-REG (10-15) = Module number where error occurred

   A-REG (0-9) = Lower RAM address of microprogram attempted
   B-REG (0-9) = Upper RAM address of microprogram attempted
   } The microprogram is therefore stored between the specified two RAM addresses in the module specified in A-register bits 10-15.

   B-REG (10-15) = Number corresponding to the microcode attempted. See table 4-3.

3. See figure 3-2.

Table 4-2. Test Execution Times*

TEST SECTION	EXECUTION TIME (SECONDS)
TST00 — Basic Load Test	1
TST01 — Command State Test	2
TST02 — Data Mode Screen Test	1
TST03 — Command State Screen Test	1
TST04 — I/O Screen Test	1
TST05 — RAM Address Rollover Test	1
TST06 — Preset Test	Note 1
TST07 — Zeros Data Test	2
TST10 — Ones Data Test	2
TST11 — Lonely Bit Data Test	220
TST12 — RAM Address Parity Test	2
TST13 — RAM Checkerboard Test	2
TST14 — Alternate Word Data Test	1
TST15 — DCPC Test	1
TST16 — Control Memory Priority Test	1
TST17 — WCS Enable/Disable Screen Test	1
TST20 — WCS Enable/Disable Screen Test	1
TST21 — Command State Alteration Test	1
TST22 — Block Priority Test	1
TST23 — RAM Data Test	3
TST24 — RAM Module Decoder Test	1
TST25 — User Looping Test	Note 2

NOTES:

1. Depends on operator response.
2. Depends on loop used and operator response.

*Maximum time required in a 21MX M-Series Computer.

Table 4-3. RAM Data Error Microcode

B-REG BITS 0-5	MICRO-OBJECT CODE ATTEMPTED	MICROCODE ATTEMPTED
	21MX M-SERIES	
00	000.026576	RTN INC A A
01	017.136757	PASS
	260.071617	ENVE INC X X
	007.126576	RTN DEC A A
02	017.136757	PASS
	017.172504	R1 PASS B Y
	007.126576	RTN DEC A A
03	017.136757	PASS
	354.001643	IMM L4 CMLO Y 0
	007.126576	RTN DEC A A
04	017.136757	PASS
	017.124557	PASS A B
	007.126576	RTN DEC A A
	21MX E-SERIES	
00	227.106140	READ RTN INC A A
01	010.036747	PASS
	267.171607	ENVE INC X X
	220.006140	READ RTN DEC A A
02	010.036747	PASS
	010.072224	R1 PASS B Y
	220.006140	READ RTN DEC A A
03	010.036747	PASS
	350.001663	IMM L4 CMLO Y 0
	220.006140	READ RTN DEC A A
04	010.036747	PASS
	010.010147	PASS A B
	220.006140	READ RTN DEC A A