HP Vectra Technical Reference Manual Volume 1: Hardware

Hewlett-Packard

Notice

The information contained in this document is subject to change without notice.

Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

Personal Office Computer Division
974 East Arques Avenue
P.O. Box 486
Sunnyvale, CA 94086, U.S.A.

First Edition - August 1985
Printed in U.S.A.

FCC Statement

Federal Communications Commission Radio Frequency Interference Statement

Warning: This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

More About Radio and Television Interference

Because the HP Vectra PC generates and uses radio frequency energy, it may cause interference with radio and television reception in a residential installation.

Hewlett-Packard's system certification tests were conducted with HP-supported peripheral devices and HP shielded cables, such as those you receive with you system. The HP Vectra PC meets the requirements for a Class B computing device in accordance with the specifications of Part 15, Subpart J, of protection against interference with radio and television reception in a residential installation.

Hewlett-Packard provides instructions for using this computer in manuals covering setup, connection of peripheral devices, operation, service, and technical reference.

Installing and using the computer in strict accordance with Hewlett-Packard's instructions will minimize the chances that the HP Vectra PC will cause radio or television interference. However, Hewlett-Packard does not guarantee that the computer will not interfere with radio and television reception. If you think your computer is causing interference, turn it off to see if the radio or television reception improves. If the reception:

- Does not improve, you computer is not causing the problem.
- Does improve, you computer is causing the problem.

To correct interference, take one or more of the following steps:

- Relocate the radio or television antenna.
- Move the computer away from the radio or television.
- Plug the computer into a different electrical outlet, so that the computer and the radio or television are on separate electrical circuits.
- Make sure that all of your peripheral devices are certified Class B by the FCC.
- Make sure you use only shielded cables to connect peripheral devices to you computer.
- Consult your computer dealer, Hewlett-Packard, or an experienced radio/television technician for other suggestions.
- Order the FCC booklet called How to Identify and Resolve Radio-TV Interference Problems for the U.S. Government Printing Office, Washington, D.C. 20402.

Table of Contents

SECTION 7. MULTI MODE VIDEO ADAPTER CARD

SECTION 8. NUMERIC COPROCESSOR

SECTION 9. DISC DRIVE OVERVIEW

SECTION 10. MEMORY EXPANSION CARDS

SECTION 11. SERIAL/PARALLEL CARD

SECTION 12. SCHEMATICS

Illustrations

List of Tables

PREFACE

The *HP Vectra Technical Reference Manual* is divided into two volumes. Volume 1 is focused on the hardware. It is intended for use by design engineers, system programmers, or any other person who wishes to know the HP Vectra PC at a very detailed technical level.

This volume consists of a hardware description of the processor board and the components of the board. A basic capability description and a system interface description is given. Included in the description of the processor board are: memory and I/O address maps, backplane I/O pin assignments and signal descriptions, connectors, and subsystem-to-system register definitions.

Also included is a description of the accessory cards that append to the system through the backplane I/O channels. The emphasis of the accessory card description will be the interfaces the cards have with the system. The information is limited to the port addresses, pin assignments and signal definitions, register definitions, and jumpers.

This manual also includes: a glossary, a bibliography, and an index. A glossary is given for HP-specific term clarification. The bibliography should be used to aid the engineer or the programmer in search of detailed data on a specific chip or circuit. Hewlett-Packard defines some specifications for the IC's, therefore, some parameters may vary. The index is an alphabetical listing of important subjects. It is used to refer the reader to the appropriate page(s) for a listed subject.

SECTION 1. HP VECTRA PC OVERVIEW

System Design Overview

The Hewlett-Packard Vectra PC is designed to provide a wide range of system solutions for the computing needs of today. The system architecture supports a wide range of expansion capabilities, and it is compatible with a broad line of industry standard software and hardware.

The heart of the HP Vectra PC system is the Intel 80286 microprocessor. The 80286 is one of the most powerful microprocessors available today, yet it maintains a high degree of compatibility with 8086/8088 microprocessor used in many industry standard personal computers. The HP Vectra PC owes much of its power and flexibility to the inherent capabilities of the 80286.

The basic HP Vectra PC systems contain either 256 Kbytes or 640 Kbytes of internal RAM. The 256 Kbyte memory may be expanded up to 640 Kbytes without using internal expansion cards. All HP Vectra PC systems come with 64 Kbytes of system firmware. An additional 192 Kbytes of firmware may be added in modules, bringing the total to 256 Kbytes of ROM.

The HP Vectra PC has mounting space and power connections for three internal disc drives. Three different disc drive units are available: a 360 KB Internal Flexible Disc Drive, a 1.2 MB Internal Flexible Disc Drive, and a 20 Mbyte hard disc drive. The hard disc drive may be installed along with two flexible discs. The flexible drives may be of the same type, or a 360 KB and a high-capacity (1.2 MB) drive may be installed together. Another option could be, two hard disc drives installed with one flexible disc drive.

Expandibility is the focus of the HP Vectra PC system. The system is equipped with seven backplane expansion slots. Through the use of internal expansion cards, the HP Vectra PC can support many types of peripheral products. In addition, the HP Vectra PC includes the HP Human Interface Link (HP-HIL) which provides a flexible interface with a wide range of input devices.

System Components

Typical HP Vectra PC systems have certain basic components, regardless of the configuration. Figure 1 shows the basic components contained in any HP Vectra PC system. The components marked with an asterisk have certain options, but are nontheless required.

Basic Components of the HP Vectra PC System

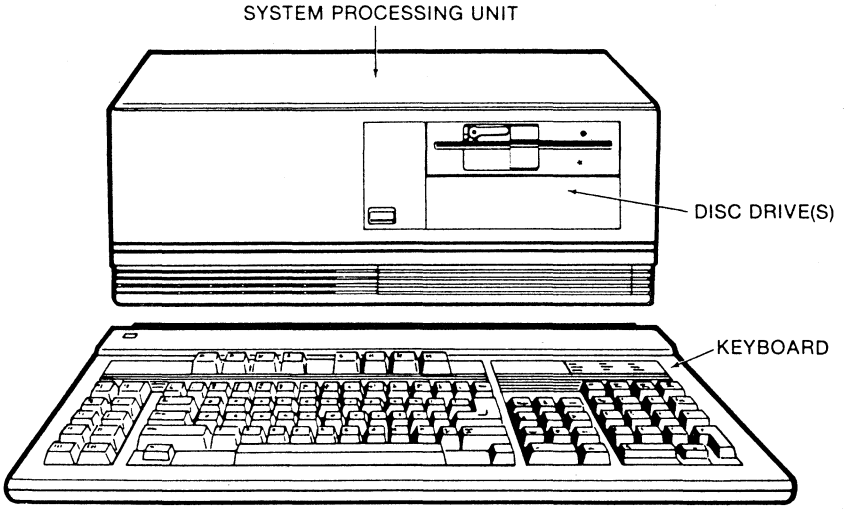


Figure 1

The computer contains the processor board and the processor extension card, the power supply, and up to three internal disc drives. Figure 2 shows these components.

Internal Components of the HP Vectra

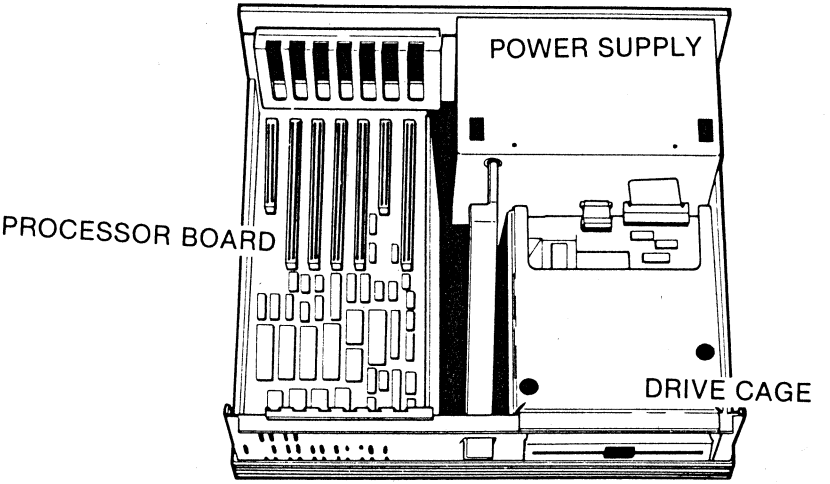


Figure 2

Specifications and Environment

The following table defines the HP Vectra PC system specifications and operating environment.

Table 1.1

Specifications and Environment

Mainframe Dimensions	
Length	42.5cm (16.7 in.)
Height	16.0cm (6.3 in.)
Width	39.0cm (15.4 in.)
Keyboard Dimensions	
Length	52.5cm (20.6 in.)
Height	3.5cm (1.3 in.)
Width	22 cm (8.8 in.)
Weight 11.8kg (26 lbs.) (includes one flexible disc drive)	
Temperature Limits	
Operating	5 C to 40 C (41 F to 104 F)
Storage	– 55 C to 75 C (– 67 F to 158 F)
Humidity	
Operating	5-80% RH
Storage	90% for 24 hours
Power	
BTU output	710 BTU/hour maximum
AC input	115V at 50/60 Hz (+ / – 5%)
	230V at 50/60 Hz (+ / – 5%)
Power Consumption 360W (450W) maximum with 110V (220V) supply, convenience outlet unused. 510W (600W) maximum with 110V (220V) supply, convenience outlet used.	
FCC compliance Class B	
Maximum Operating Altitude at 40 degrees C: 2286m (7500 ft.)	
Cable length	
Video Cable	1m and 3m (3.28 ft. and 9.84 ft.)
HP-HIL Cable	2.5m (8.2 ft.)

The following are drawings of backplane I/O expansion cards. The maximum dimensions of these cards are given in the figure.

I/O Card Dimensions

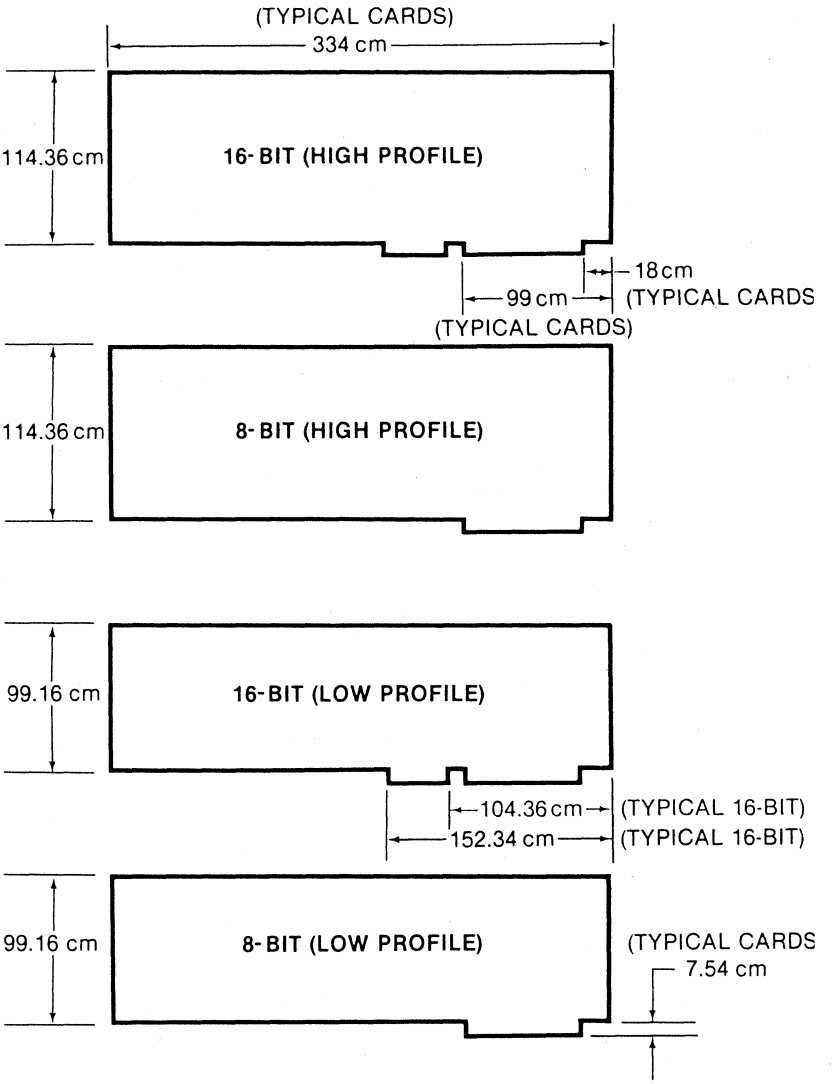


Figure 3

SECTION 2. PROCESSOR BOARD

The cpu of the processor board is the Intel 80286 microprocessor. Other components of this board are:

- ★ 16MHz system clock
- ★ three programmable timers
- ★ seven backplane I/O slots
- ★ 19-level interrupt controller
- ★ 7-channel DMA
- ★ CMOS real-time clock plus RAM chip that operates with battery back-up when the system is off or during a power failure
- ★ keyboard and input device controller
- ★ speaker attachment
- ★ flexible disc controller subsystem

A processor extension card for memory is attached to the processor board of the HP Vectra PC through connector P5.

The following illustration is a layout of the processor board (HP assembly number 45935-60001). Included in the illustration are the components and the connectors.

Layout of the Processor Board

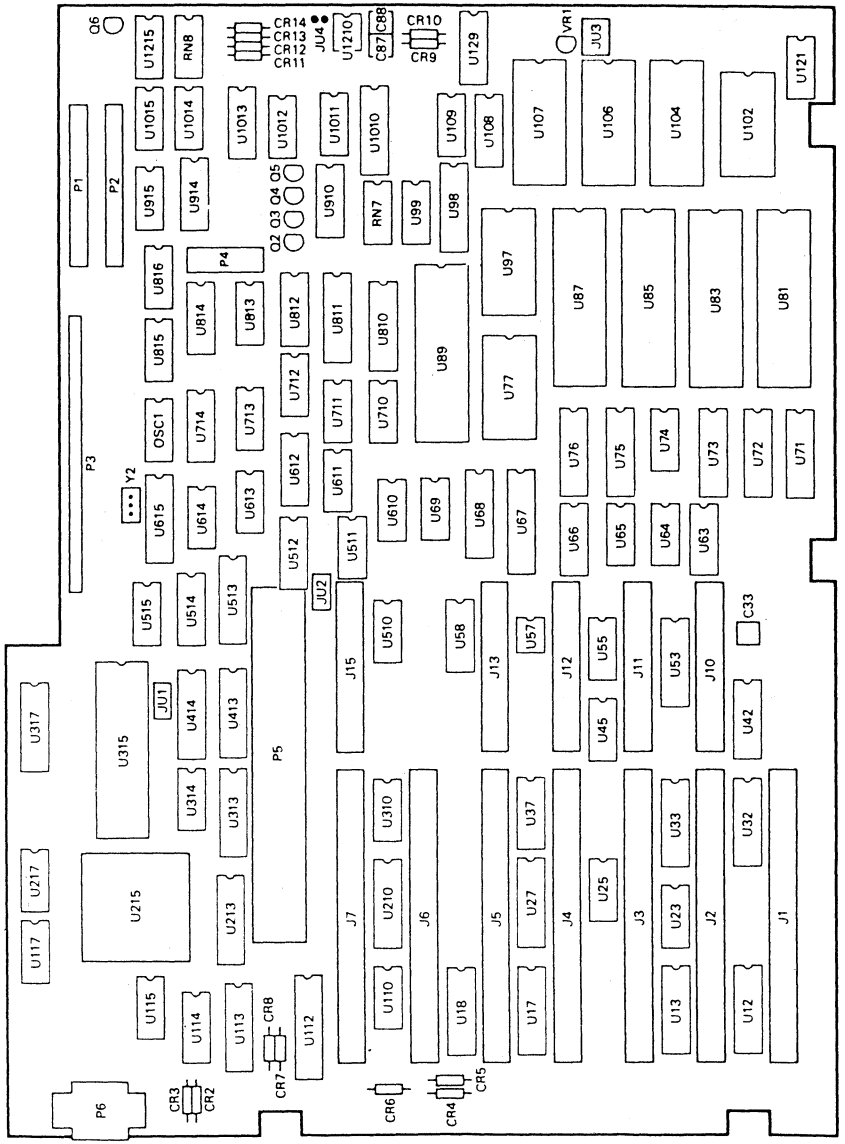


Figure 4

The following illustration is a block diagram of the processor board.

Processor Board Block Diagram

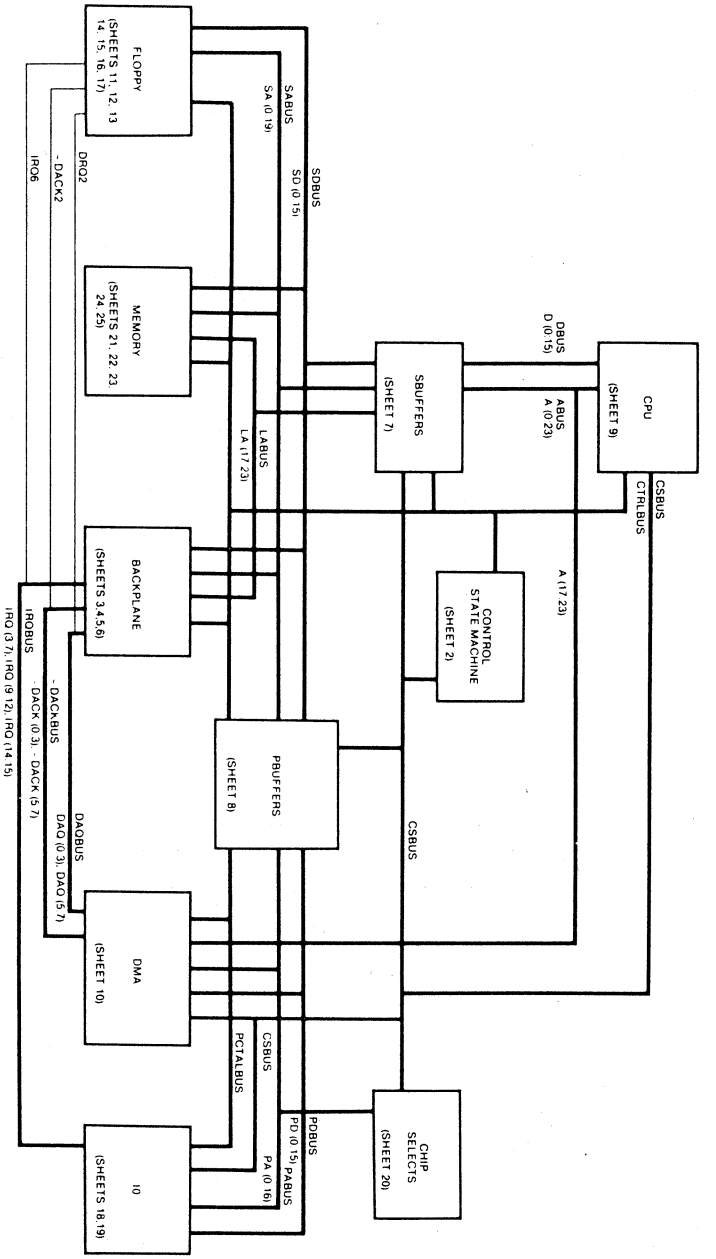


Figure 5

The block diagram illustrates the flow of operation.

Memory

The processor extension card on the processor board contains the system RAM with parity, and the 64 Kbytes of system ROM. The 256 Kbytes RAM processor extension card (HP assembly number 45935-60002) can be expanded to a maximum of 640 Kbytes RAM by 128 Kbytes increments without additional I/O cards. The 640 Kbyte processor extension card (HP assembly number 45945-60002) is considered fully loaded.

ROM

The processor extension card has four ROM sockets; two at hex address F0000 (even and odd), and two at hex address E0000. The following chart shows where the ROM sockets are addressed. These sockets can accept either 16 Kbyte (16K x 8) or 32 Kbyte (32K x 8) parts. The 16 Kbyte parts start at hex address E8000; the 32 Kbyte parts start at hex address E0000. The HP Vectra PC is equipped with two 32 Kbyte parts. Their access time is 170ns.

		Even	Odd
System	F0000	U183	U191
Open	E0000	U152	U192

RAM

The RAM chips used in the HP Vectra PC have an access time of 150ns and a cycle time of 275ns. The parts used for the system RAM are 256 Kbit parts (64K x 4). The parts used for parity are 64 Kbit parts (64K x 1). The following figure illustrates the RAM organization.

RAM Organization

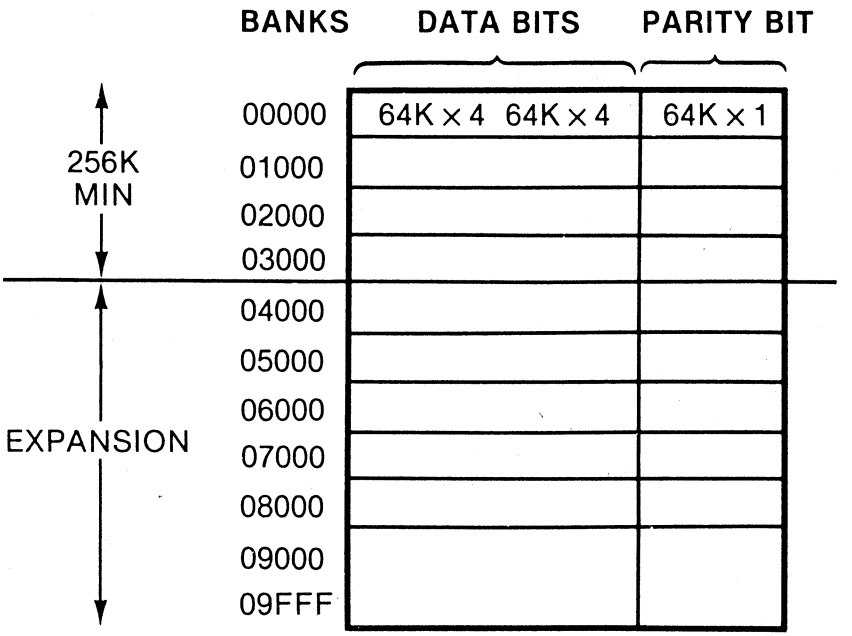


Figure 6

Refresh Cycles

The refresh controller operates from the 8 MHz system clock. A RAM refresh occurs approximately once every 16us. Each refresh cycle requires five system clock cycles.

Parity

Parity is generated for each byte of RAM during write operations, and checked during read operations. If a parity error occurs, the

parity check (PCK) signal is generated. If PCK is enabled, a non-maskable interrupt (NMI) occurs.

Memory Map

The 80286 can address 1 Mbyte of system memory in the real-address mode, and 16 Mbytes in the protected mode. Certain areas in memory have been specified or mapped for various system functions. These areas are defined in table 2.1.

Table 2.1

System Memory Map

Address	Description	Function
000000-09FFFF	Processor ext. card memory	Real-address mode system RAM
0A0000-0BFFFF	Video RAM	Reserved for video display card.
0C0000-0DFFFF	I/O Expansion ROM	Reserved for ROM modules on I/O cards.
0E0000-0EFFFF	Processor ext. card	Reserved for ROM on processor extension card
0F0000-0FFFFF	Processor ext. card ROM	Used for system firmware on processor extension card.
----------End of Real-Address Mode Memory Boundary----------		
100000-FDFFFF	I/O channel memory	Expansion memory
FE0000-FEFFFF	Processor ext. card ROM	Duplicate mapping of ROM on processor extension card.
FF0000-	Processor ext. card ROM	Duplicate mapping of firmware on processor extension card.

80286 Processor

HP Vectra PC utilizes the Intel 80286 microprocessor. The 80286 has a 24-bit address bus (a 16 Mbyte physical address range), a 16-bit data bus, and a comprehensive instruction set. The 80286 supports two addressing modes: the real-address mode and the protected mode. These modes of operation are detailed in the following sections.

Real-Address Mode

In real-address mode the 80286 operates as a high performance 8086. It supports 1 Mbyte of contiguous system memory using 20 address bits (A0-A19). With a few differences (which are described in the *HP Vectra Technical Reference Manual Volume 2: System BIOS* the 80286 is object code compatible with the 8088 and 8086 microprocessors. In addition, the 80286 supports several new instructions in the real-address mode not found in the 8088 or 8086. All system software (i.e., ROM BIOS, MS-DOS Version 3.1, etc.) currently operates only in the real-address mode.

Protected Operating Mode

The protected mode allows the use of the extended features of the 80286. These include 1 Gigabyte of virtual address space, 16 Mbytes of physical address space, on-board memory management, and four-level memory protection. The protected mode is designed to support multitasking/multiuser operating systems and highly advanced languages. When the 80286 is operating in the protected mode, it is not object code compatible with the 8088 and 8086 software. Several new instructions are provided in the protected mode to control these advanced features. These instructions are not compatible with the 8088, 8086, or the 80286 operating in the real-address mode.

80286 Clock

The 80286 processor clock is generated by the 82284 clock chip. A 16 MHz crystal serves as the input to the 82284 oscillator. The 82284 outputs a 16 MHz signal which serves as the input clock for the 80286. (This signal is called PROCCLK in the schematics.) This signal is divided by two to get the 8 MHz SYSCLK signal which is present on the I/O channel. In addition, the 82284 provides power-on reset and wait-state synchronization.

System Performance

The HP Vectra PC employs a 16 MHz clock to drive the 80286 at 8 MHz. There is a 14.318 MHz clock used to provide a timing clock for the I/O bus and the system timer/counter. The 14.318 MHz clock has a variable capacitor for fine tuning.

The 80286 requires two clock cycles (SYSCLK) to complete a bus cycle. With an 8 MHz clock, this translates into a 250ns bus cycle time. This bus cycle time is too fast for many memory and I/O devices, therefore, wait-states are inserted. The processor board is configured to insert one wait-state in every bus cycle. This extends the bus cycle time to 375ns, allowing standard memory devices sufficient time. This is the bus cycle time for all 16-bit transfers, either I/O or memory.

Any transfer to an 8-bit device requires additional wait-states. The number of extra wait-states depends on the setting of jumper JU2 on the processor board. It has two positions and may be set for four or five wait-states (including the one normally inserted) for each 8-bit transfer. Figure 7 shows the configuration settings for JU2.

JU2 Configurations

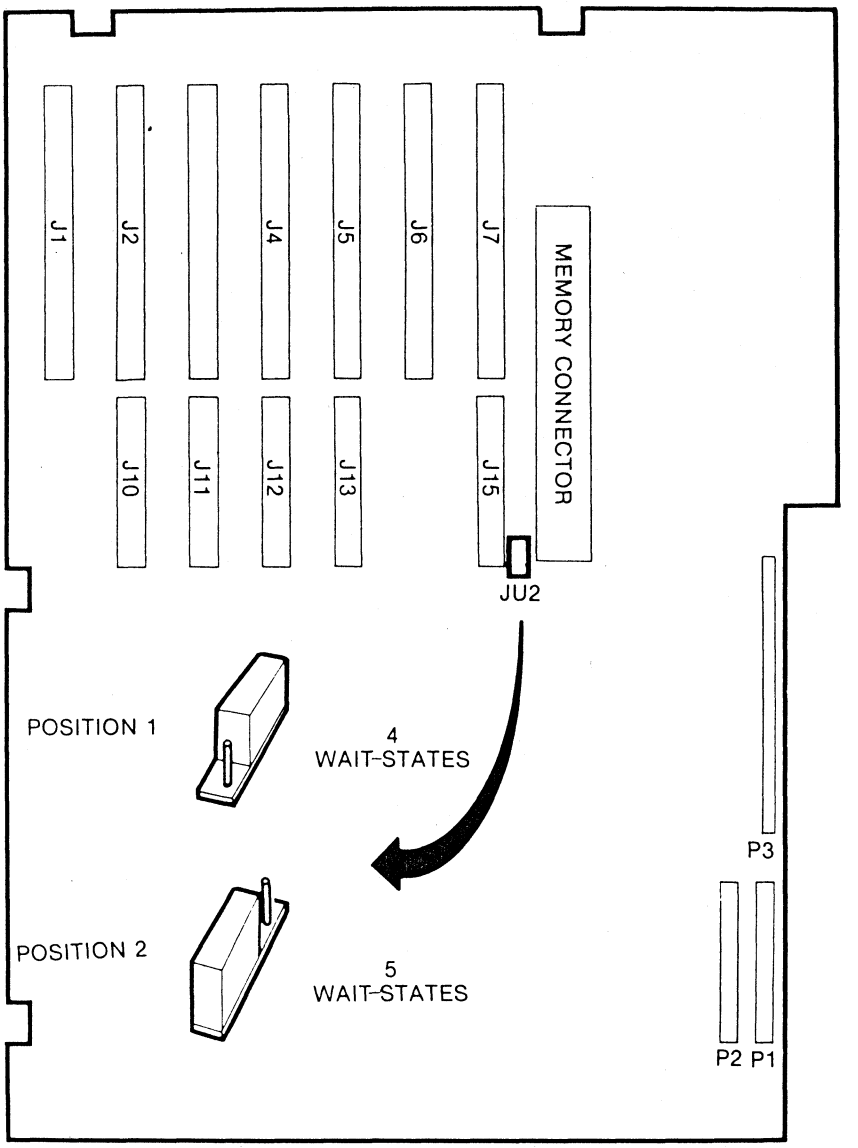


Figure 7

The following table summarizes the number of wait-states inserted for different types of data transfer.

Table 2.2

Wait-State Generation

TRANSFER TYPES	POSITION 1 WAIT-STATES	POSITION 2 WAIT-STATES	NORMAL CYCLES	TOTAL
16 to 16	1	1	2	3
8 to 8	4	5	2	6 or 7*
16 to 8	8	10	4	12 or 14*
8 to 16	8	10	4	12 or 14*

The HP Vectra PC has provisions to maximize system performance when fast memory and I/O devices are installed in the I/O channel connectors. The ~0WS signal may be asserted by a peripheral to signal the processor board to insert fewer wait-states. If this signal is asserted during a transfer to a 16-bit device, no wait-states will be inserted. If it is asserted during a transfer to an 8-bit device, either two or three wait-states will be inserted, depending on the timing of the assertion.

*Depends on setting of JU2.

System Timers/Counters

The HP Vectra PC contains the Intel 8254 timer/counter device which provides three independent 16-bit counters. The input frequency of 1.19MHz is derived from the 14.318 MHz system timing clock. The minimum time resolvable is approximately 838 nanoseconds (1 input clock cycle), and the maximum is 55 milliseconds (65,536 clock cycles).

All three timers have dedicated system uses. Timer 0 is used to generate the real-time clock interrupt. Counter 1 is dedicated to RAM refresh. No attempt should be made to reprogram this channel. Counter 2 is used to drive the speaker.

Counter 2 has a Gate input which is under program control. This Gate input is Bit 0 of "Port B" (61H). Setting this bit to 0 inhibits counting action, effectively turning the speaker off. In addition, bit 1 is "AND"ed with the timer output; writing a 0 also disables the speaker. The following is a block diagram of the timer.

Timer Block Diagram

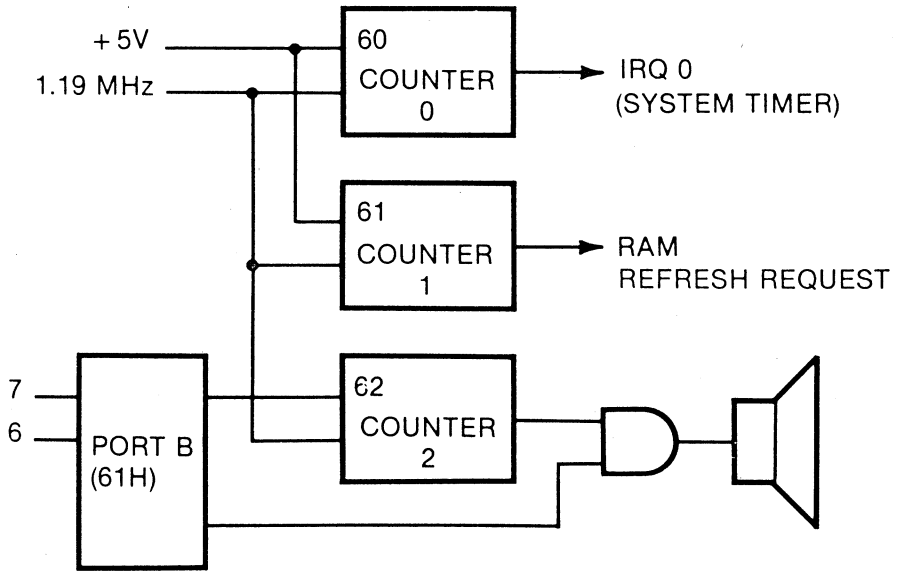


Figure 8

The 8254 occupies four port addresses; three are used to load count values into each of the timer channels, the fourth is used as a command and status port. The port addresses are listed in the following chart.

ADDRESS	PORT
040H	Channel 0 counter
041H	Channel 1 counter
042H	Channel 2 counter
043H	Command register

System Interrupts

The 80286 microprocessor provides a non-maskable interrupt (NMI) bit that can be set and reset with system programs. An interrupt controller provides another 19-levels of system interrupt.

The Intel 8259A interrupt controller chip U107 is the master chip. Cascaded to the master chip are two other 8259A chips. Each chip has an 8-bit interrupt request function. The primary function of the third controller chip is keyboard and input device interface. The following chart gives the port addresses of the interrupt controllers.

020H	Master 8259A Port 0
021H	Master 8259A Port 1
0A0H	Slave 8259A (#2) Port 0
0A1H	Slave 8259A (#2) Port 1
07CH	Slave 8259A (#3) Port 0
07DH	Slave 8259A (#3) Port 1

Interrupt Controller

The following figure indicates the possible interrupt vector offset mappings. The current address in hex is given in the parentheses. In the far right hand column is the function of the interrupt vector employed by HP Vectra.

Interrupt Controller Structure

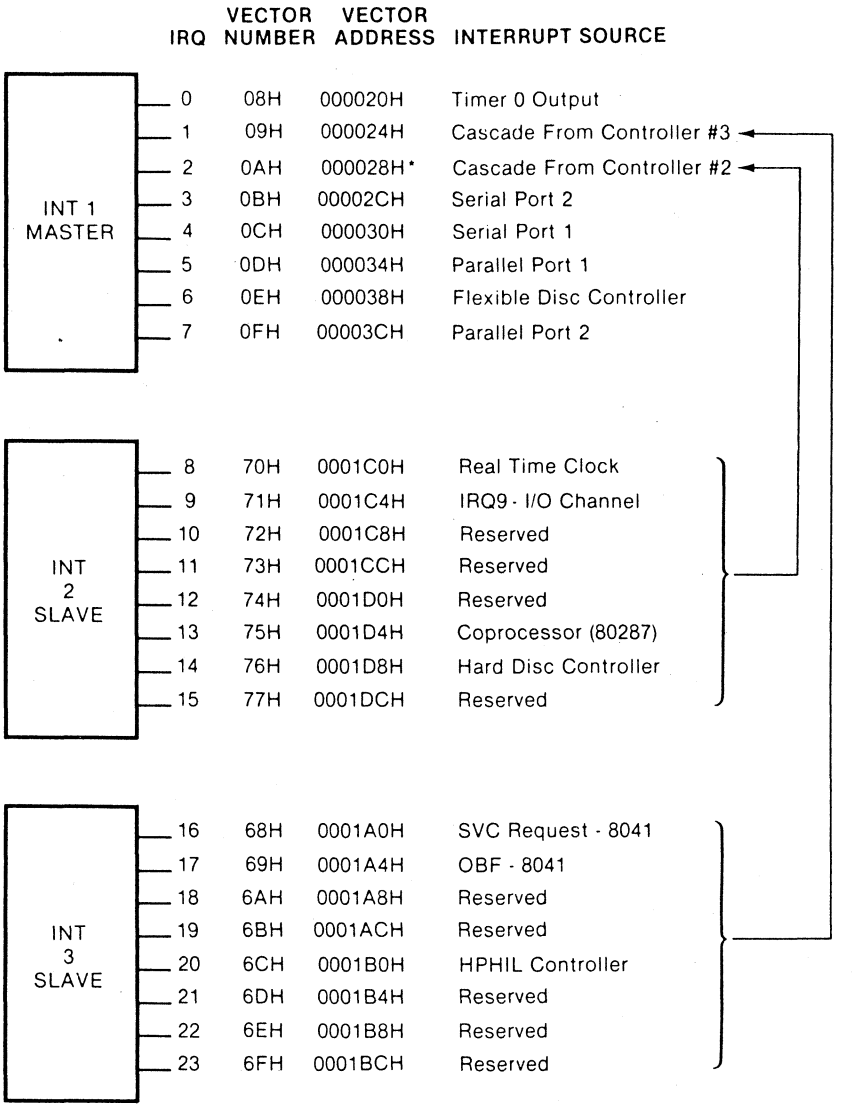


Figure 9

*Vector from IRQ9 should be repeated here for industry standard compatibility.

Only one interrupt level may be active for each signal. The duplicates must be masked off using the 8259A interrupt mask register.

Non-maskable Interrupts

The non-maskable interrupt is used to process the system response to a memory parity error, an error signaled by an expansion card through the I/O CHCK signal, or a hard reset from the keyboard. The signal is masked from the 80286 at system reset, and must be enabled by the system software. The NMI signal is enabled by setting bit 7 of port 70H to 0, or it can be masked by setting the same bit 7 to 1.

The NMI generates a type 2 interrupt. The vector to the service routine should be placed at 0000:0008H. Refer to the *HP Vectra Technical Reference Manual Volume 2: System BIOS* for additional information regarding programming considerations.

Direct Memory Access (DMA) Controller

DMA control is provided by two Intel 8237A chips that provide timing, control functions, and most of the address generation, and a 74LS612 page register IC that generates the most significant memory address bits. Each 8237A chip supports four channels, with DMA controller 2 cascaded to DMA controller 1 for seven DMA channels. The DMA controller regulates transfers from I/O to memory or from memory to I/O. Buffering the system address bus and the system backplane bus signals with three-state gates permits DMA operations to take over the bus.

DMA Controller Clock Cycle

The DMA controller operates at 4MHz, which results in a clock cycle time of 250ns. The DMA clock is derived by dividing the backplane clock by two. All DMA data transfers use five DMA clock cycles with a sum of 1.25us. Not included in this time are the cycles spent in transfer of bus control to the DMA controller.

Controller Channels

DMA allows an I/O device to gain direct access to the system bus via the backplane channel connectors. The DMA controller allows prioritized bus access for individual devices.

DMA controller 1 contains channels 0 through 3. It supports 8-bit data transfers between 8-bit I/O devices and 8-bit or 16-bit memory. During 8-bit to 16-bit transfers the backplane state machine provides the required multiplexing. Each channel can transfer data throughout the 16 Mbyte system address space in 64 Kbyte blocks.

DMA controller 2 contains channels 4 through 7. Channel 4 is used to cascade controller 1 to the 80286 microprocessor, and is unavailable. Channels 5, 6, and 7 support 16-bit data transfers between 16-bit I/O adapters, and 16-bit memory.

These 16-bit DMA channels can transfer data throughout the 16 Mbyte system address space in 128 Kbyte blocks (64 Kbyte words). Each 128 Kbyte block is a page of memory. All DMA memory transfers through channels 5-7 must occur on even-byte boundaries.

Address Generation

Addresses for DMA channels are not incremented or decremented through page boundaries. The following figure shows the 24-bit system address is generated by the DMA controller and the DMA page register together.

DMA Address Generation

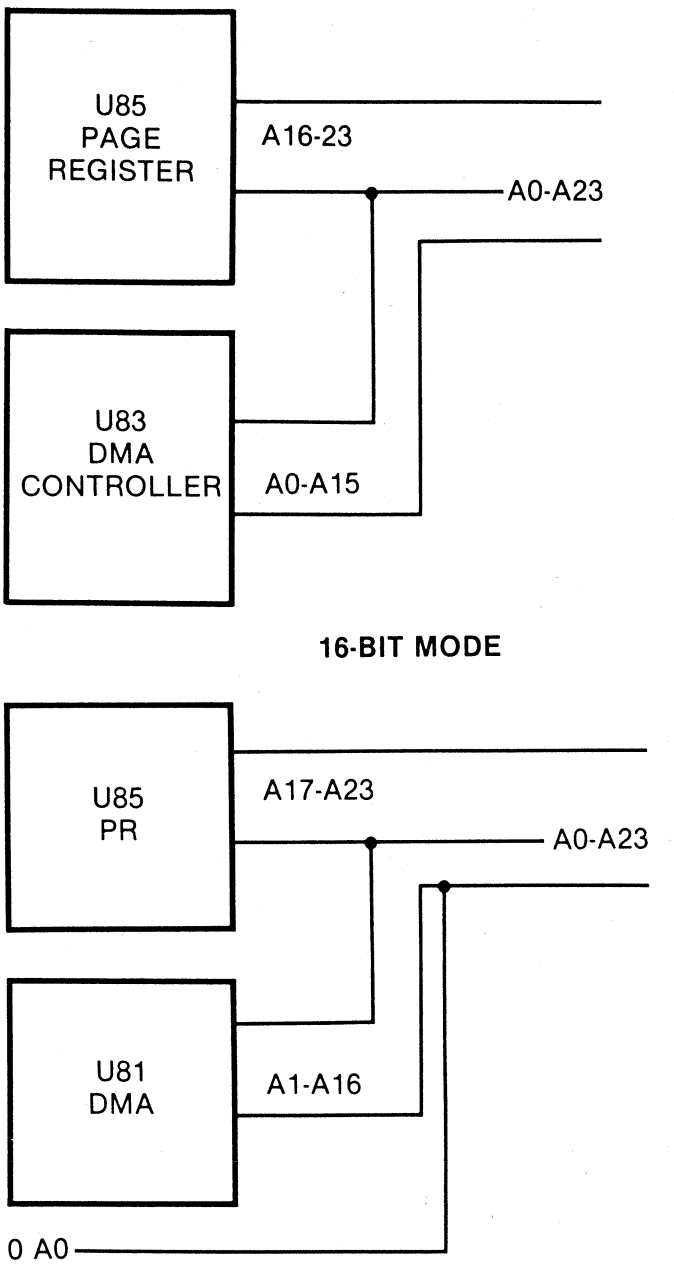


Figure 10

The following table defines the port addresses for the DMA controller.

Table 2.3

DMA Port Assignments

PORT ADDRESS	IC	REGISTER
0000H	DMA # 1	Ch 0 Address
0001H		Ch 0 Count
0002H		Ch 1 Address
0003H		Ch 1 Count
0004H		Ch 2 Address
0005H		Ch 2 Count
0006H		Ch 3 Address
0007H		Ch 3 Count
0008H		Read Status/Write Command
0009H		Write Request
000AH		Write Single Mask Register Bit
000BH		Write Mode Register
000CH		Clear Byte Pointer Flip-flop
000DH		Read Temporary Reg/Write Master Clear
000EH		Clear Mask Register
000FH		Write All Mask Register Bits
0081H	Page Reg	Channel 2 A16 - A23
0082H		Channel 3 A16 - A230083H
0083H		Channel 1 A16 - A23
0087H		Channel 0 A16 - A23
0089H		Channel 6 A17 - A23
008AH		Channel 7 A17 - A23
008BH		Channel 5 A17 - A23
008FH		Refresh

PORT ADDRESS	IC	REGISTER
00C0H	DMA # 2	Ch 4 Address
00C2H		Ch 4 Count
00C4H		Ch 5 Address
00C6H		Ch 5 Count
00C8H		Ch 6 Address
00CAH		Ch 6 Count
00CCH		Ch 7 Address
00CEH		Ch 7 Count
00D0H		Read Status / Write command
00D2H		Write Request
00D4H		Write Single Mask Register Bit
00D6H		Write Mode Register
00D8H		Clear Byte Pointer Flip-flop
00DAH		Read Temporary Reg/Write Master Clear
00DCH		Clear Mask Register
00DEH		Write All Mask Register Bits

Note, the I/O ports for DMA controller 1 (for 8-bit transfers) are located on consecutive addresses, while the ports for controller 2 are on even-byte addresses. All registers should be loaded with valid parameters after power-up or reset. This should be done even if some channels are unused.

Backplane I/O

The backplane I/O channel supports accessory cards. Included in the I/O channel support are 11-levels of interrupt and 7 DMA channels. The I/O channel allows either 8-bit or 16-bit data bus access, 24-bit memory address, control lines for memory and I/O, refresh of dynamic memory, and wait-state generation.

I/O devices are addressed using I/O address space hex 100 to hex 3FF. The channel is designed so that 512 I/O device addresses are available to the I/O channel accessory cards.

Connectors

The I/O channel connectors are located at the upper left of the processor board. J1 and J6 only support 8-bit I/O devices. These slots use 62-pin connectors. Slots J2, J3, J4, J5, and J7 each consist of a 62-pin connector and a 36-pin connector. The corresponding 36-pin connectors are J10, J11, J12, J13, and J15, respectively. These five slots can be used for either 8-bit or 16-bit I/O devices. Figure 11 shows the I/O channel connectors location.

I/O Channel Connectors

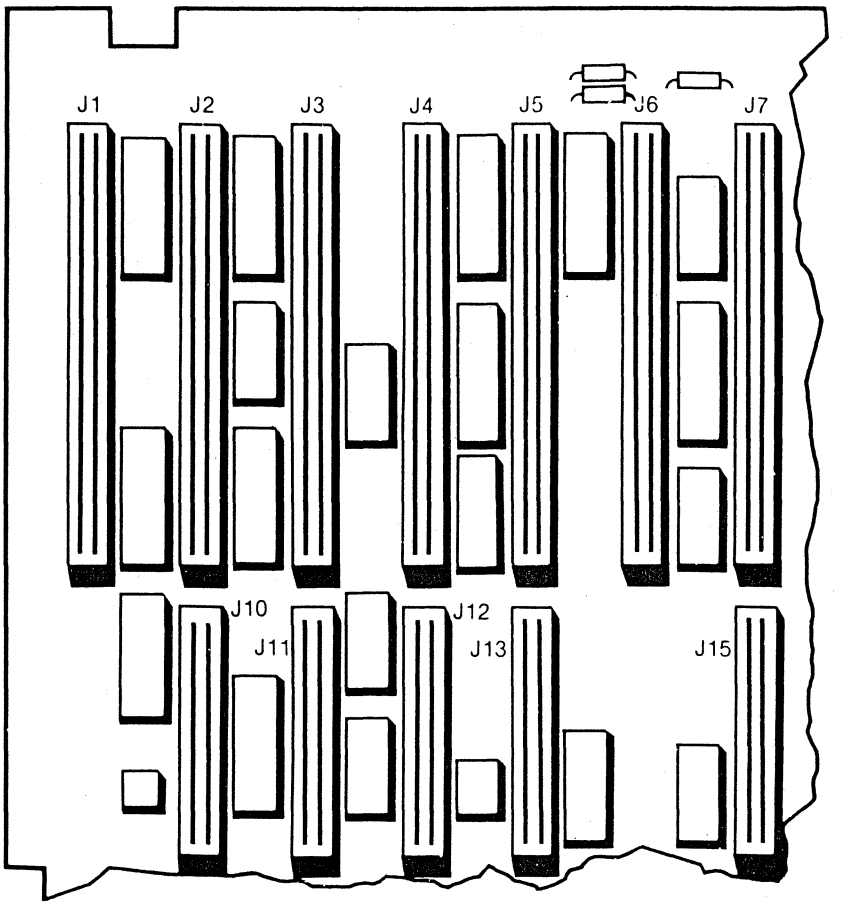


Figure 11

Power Availability

The backplane I/O channel is sufficiently powered to drive seven system expansion slots. For a complete channel power budget refer to the Section 6.

Table 2.4 gives the 62 pin assignments for the backplane I/O connectors. Table 2.5 gives the 36 pin assignments for the

backplane I/O connectors. The signals are alphabetically described in the section following the tables. The "~" (tilde) symbol is used before the signals that are defined as active low.

Table 2.4

62-Pin Connector Assignments

Circuit Side			Component Side		
Pin	**I/O**	**Signal Name**	**Pin**	**I/O**	**Signal Name**
B1		GND	A1	I	~I/O CH CK
B2	O	RESET DRV	A2	I/O	SD7
B3		+5Vdc	A3	I/O	SD6
B4	I	IRQ9	A4	I/O	SD5
B5		−5Vdc	A5	I/O	SD4
B6	I	DRQ2	A6	I/O	SD3
B7		−12Vdc	A7	I/O	SD2
B8	I	0WS	A8	I/O	SD1
B9		+12Vdc	A9	I/O	SD0
B10		GND	A10	I	~I/O CH RDY
B11	O	~SMEMW	A11	O	AEN
B12	O	~SMEMR	A12	I/O	SA19
B13	I/O	~IOW	A13	I/O	SA18
B14	I/O	~IOR	A14	I/O	SA17
B15	O	~DACK3	A15	I/O	SA16
B16	I	DRQ3	A16	I/O	SA15
B17	O	~DACK1	A17	I/O	SA14
B18	I	DRQ1	A18	I/O	SA13
B19	I/O	~REFRESH	A19	I/O	SA12
B20	O	SYSCLK	A20	I/O	SA11
B21	I	IRQ7	A21	I/O	SA10
B22	I	IRQ6	A22	I/O	SA9
B23	I	IRQ5	A23	I/O	SA8
B24	I	IRQ4	A24	I/O	SA7
B25	I	IRQ3	A25	I/O	SA6
B26	O	~DACK2	A26	I/O	SA5
B27	O	T/C	A27	I/O	SA4
B28	O	BALE	A28	I/O	SA3
B29		+5Vdc	A29	I/O	SA2
B30	O	OSC	A30	I/O	SA1
B31		GND	A31	I/O	SA0

Table 2.5

36-Pin Connector Assignments

Circuit Side			Component Side		
Pin	I/O	Signal Name	Pin	I/O	Signal Name
D1	I	~MEM CS16	C1	I/O	~SBHE
D2	I	~I/O CS16	C2	I/O	LA23
D3	I	IRQ10	C3	I/O	LA22
D4	I	IRQ11	C4	I/O	LA21
D5	I	IRQ12	C5	I/O	LA20
D6	I	IRQ15	C6	I/O	LA19
D7	I	IRQ14	C7	I/O	LA18
D8	O	~DACK0	C8	I/O	LA17
D9	I	DRQ0	C9	I/O	~MEMR
D10	O	~DACK5	C10	I/O	~MEMW
D11	I	DRQ5	C11	I/O	SD8
D12	O	~DACK6	C12	I/O	SD9
D13	I	DRQ6	C13	I/O	SD10
D14	O	~DACK7	C14	I/O	SD11
D15	I	DRQ7	C15	I/O	SD12
D16		+5Vdc	C16	I/O	SD13
D17	I	~MASTER	C17	I/O	SD14
D18		GND	C18	I/O	SD15

I/O Signal Descriptions

Signal	I/O	Description
AEN	O	This signal is used to inform the system that the DMA controller has control of the address and control buses. This signal is active during DMA transfers.
BALE	O	This is the buffered ALE signal from the 82288 bus controller. Its falling edge indicates valid address and control signals. BALE is forced high during DMA cycles.

Signal	I/O	Description
~DACK0-3 ~DACK5-7	O	These signals are used by the processor board to acknowledge DMA requests. They are active low.
DRQ0-DRQ3 DRQ5-DRQ7	I	These lines are used by adapter cards to request DMA service or to gain control of the system. The DMA channels are prioritized with Channel 0 having the highest priority and channel 7 having the lowest. The signal must be held high until its corresponding acknowledge signal is asserted.
~I/O CHCK	I	This signal is used by an adapter card to indicate to the system that an error has been detected on the card. This signal is active low.
~I/O CH RDY	I	This signal is used to synchronize slow memory or I/O devices during read and write operations. If an adapter card wishes to extend a read or write operation, it should pull this line low as soon as a valid address and a read or write command is detected. A read or write operation should not be extended to more than 15 SYSCLK cycles. Clock cycles added via this signal are in addition to any added by the system.
~I/O CS16	I	This signal is used to indicate to the system that the adapter board can perform 16-bit I/O operations. The driver should be an open collector or a tri-state device capable of sinking 20ma.
~IOR	I/O	This signal indicates an I/O read cycle is in progress. IOR may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted). This signal is active low.

Signal	I/O	Description
~IOW	I/O	This signal indicates an I/O write cycle is in progress. IOW may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted). This signal is active low.
IRQ3-IRQ7 IRQ9-IRQ12 IRQ14, IRQ15	I	These signals are used by adapter cards to signal request for interrupt service. The signal are edge sensitive, and are asserted by a low to high transition. The signal must be held high until the interrupt is acknowleged. The signals are prioritized; the following list gives their relative priorities starting with the highest. IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7
LA17-LA23	I/O	These are the upper system address lines. When combined with SA0-SA19 they produce 16 Mbytes of memory address space. These signals are not latched on the processor board; they should be latched by the adapter card on the trailing edge of BALE. LA17-LA23 may be driven by a DMA controller or processor on the I/O channel.
~MASTER	I	This signal is used by an adapter card to disable the 80286 and gain control of the system buses. In order to gain control, one of the DMA channels must be placed in the cascade mode, and the adapter card must issue a DRQ request and receive a DACK acknowledge. The adapter card may then assert MASTER and gain control of the system. It must wait one clock cycle before attempting to drive the address or data lines, and two clock cycles before issuing a read or write command. Holding this signal low for 15 us or more may cause a loss of memory due to the absence of refresh.

Signal	I/O	Description
~MEM CS16	I	This signal is used to indicate to the system that the adapter board can perform 16-bit memory operations. The driver should be an open collector or a tri-state device capable of sinking 20ma. This signal should be derived from LA17 - LA23.
OSC	O	This is a 14.318 MHz timing reference signal. It has a 50% duty cycle and a period of approximately 70 ns. This signal is asynchronous with the SYSCLK.
~REFRESH	I/O	This signal indicates a memory refresh operation is in progress. This signal may be driven by a processor on the I/O channel. This signal is active low.
RESET DRV	O	This signal is used to reset all system devices during power-on resets and indicate low line-voltage conditions. The signal is active high.
SA0-SA19	I/O	These are the system address lines. When combined with LA17-LA23 they produce 16 Mbytes of memory address space. SA0-SA19 begin to change on the rising edge of BALE, and are latched for the duration of the cycle by the falling edge of BALE. SA0-SA19 may be driven by a DMA controller or processor on the I/O channel. The system refresh controller places the refresh address on SA0-SA7 during refresh cycles.
~SBHE	I/O	This signal indicates that data is to be transfered on SD8-SD15. SBHE indicates a 16-bit transfer or an 8-bit transfer to an odd address (A0 = 1) is progress.

Signal	I/O	Description
SD0-SD15	I/O	This is the system data bus. Data is transferred to and from the system on these lines. Sixteen-bit transfers occur on SD0-SD15. Eight-bit transfers occur on SD0-SD7, unless SBHE is asserted. In which case, data is transferred on SD8-SD15. Sixteen-bit to 8-bit transfers are multiplexed by the backplane state machine into two 8-bit transfers on SD0-SD7.
~SMEMR ~MEMR	O I/O	These signals indicate a memory read cycle is progress. MEMR may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted). ~SMEMR is active if ~MEMR is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space. Both of these signals are active low.
~SMEMW ~MEMW	O I/O	These signals indicate a memory write cycle is in progress. ~MEMW may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted). ~SMEMW is active if ~MEMW is active and the address decode circuit indiactes a valid address in the bottom 1 Mbyte of memory space. Both of these signals are active low.
SYSCLK	O	This is the 8 MHz processor system clock. It has a 50% duty cycle and a period of approximately 125 ns. This signal can be used to synchronize activities to the 80286.
T/C	O	This signal informs the system that the terminal count for one of the DMA channels has been reached. The signal is active high.

Signal	I/O	Description
~ 0WS	I	This signal indicates to the system that a read or write operation can take place without additional system generated wait-states. To perform a 16-bit memory cycle with zero wait-states, this signal should be asserted as soon as a valid address decode and a read or write command is detected. To shorten cycles for 8-bit devices, ~ 0WS should be asserted on the falling edge of SYSCLK after detecting a valid address and a read or write command for two wait-states. If asserted on the second falling edge of SYSCLK after detecting a valid address and a read or write command, three wait-states will be generated for 8-bit devices. The driver should be an open collector or a tri-state device capable of sinking 20ma.

I/O Map

The HP Vectra uses the first 1024 I/O port addresses, 000H through 3FFFH. Note that ports 000H through 0FFH are reserved for I/O on the processor board and ports 100H through 3FFH are available to adapters connected to the seven I/O channel connectors. The one exception to this is the flexible disc controller subsystem. which uses either I/O ports 3F0H through 3F7H (when configured for its primary address) or I/O ports 370H through 377H (when configured for its secondary address), even though it resides on the processor card.

Table 2.6

I/O Address Map

IO Address Range	Device
000-01FH	DMA Controller, 8237
020-03FH	Master Interrupt Controller, 8259
040-05FH	Timer, 8254
060H	Keyboard Data Buffer, 8041
061H	Port B R/W
062H	Unused
063H	Unused
064H	Keyboard Command Buffer. 8041
065H-067H	Unused
068H	HP 8041 Control Buffer-Write Only
069H	HP 8041 SVC-Read Only
06AH	HP 8041 Clear Processing Done-Write
06BH	Unused
06CH-06FH	HP-HIL
070H	NMI/RTC Address Buffer, MC146818
071H	CMOS/RTC Data buffer, MC146818
072-077H	Unused
078H	Hard Reset:NMI enable/disable
079-07BH	Unused
07CH-07DH	Interrupt Controller 3, 8259
080-09FH	DMA Page Register, 74LS612
0A0-0BFH	Interrupt Controller 2,8259
0C0-0DFH	DMA Controller 2. 8237
0F0H	Clear Numeric Coprocessor "BUSY", 80287
0F1H	Reset Numeric Coprocessor, 80287
0F8-0FFH	Numeric Coprocessor, 80287

I/O Channel	
1F0H-1F8H	Hard Disc Subsystem
200H-207H	Reserved for Game I/O
278H-27FH	Parallel Printer Port 2
2F8H-2FFH	Serial Port 2
300H-31FH	Reserved for Prototype Card
360H-36FH	Reserved
378H-37FH	Parallel Printer Port 1
380H-38FH	Reserved
3A0H-3AFH	Reserved
3B0H-3BFH	Multi-Mode Video Adapter Card, HP45981A
3C0H-3CFH	Reserved
3D0H-3DFH	Reserved
3F0H-3F7H	Flexible Disc Controller Susbystem
3F8H-3FFH	Serial Port 1

Speaker

The tones for the HP Vectra PC are produced in a 2 1/4 inch permanent-magnetic speaker. The speaker can be driven by the I/O port output bit and/or the 8254A timer/counter's clock out.

Table 2.7

P4 Speaker/Keylock Connector

Pin	Assignment
1	Speaker Data
2	+ 5 Vdc
3-4	Key
5	Keyboard inhibit
6	Key
7	Ground

Attachment Connectors

The following tables define the pin assignments for the Power/ Battery connector P3. Refer to figure 4 for the locations of these connectors.

Table 2.8

P3 Power/Battery Connector Pin Assignments

Pin	Assignment
1	Return for + 12M
2	+ 12M
3-7	+ 5 Vdc
8	Key
9-13	Ground
14	+ 12 Vdc
15	− 12 Vdc
16	− 5 Vdc
17	PFAIL
18	Battery Ground
19	Battery +

Real Time Clock plus CMOS RAM

The HP Vectra PC maintains an accurate real-time clock with the MC146818 RT/CMOS plus RAM chip without processor interaction. This chip is designed to perform RAM, time, and calendar functions. The CMOS RAM, timebase, and oscillator maintain their functions during a power failure by using battery backup. The backup power is a lithium battery pack, which has an average life of 2.3 years. The battery pack is located in a bracket on the power supply.

Real-Time Clock

The real-time clock (RTC) uses a 32.768kHz crystal as its timebase. It counts seconds, minutes, hours, days, and years. In addition, it keeps track of the day of the week and provides automatic leap year compensation.

The RTC can provide an interrupt request (IRQ8) at either a fixed interval (i.e., every second), or when a certain time has arrived (in the alarm clock mode). The RTC keeps track of the time and day when the system power is off. During power-on reset, the system software reads the current time and date from the RTC and converts it into the appropriate number of system clock "ticks". From this point on, system time is kept via system clock ticks which are generated by Counter/Timer 0.

The RTC is accessed via two ports in the system I/O map: the Address Port (70H), and the Data Port (71H). The RTC contains 64 bytes of memory. The first 14 of these bytes are the Real-Time Clock registers, the remaining 50 bytes are CMOS RAM for storing system parameters.

In order to access the RTC, the address of the byte of RAM (or clock register) to be accessed is output to port 70H. The address (in the range of 0 - 3FH) is placed on bits 0 - 5. (Bit 6 is unused and bit 7 is the NMI mask.) After the desired register or RAM byte has been selected, data may be either read or written to the Data Port, 71H.

CMOS RAM Memory

The 50 bytes of CMOS RAM are used to store system parameters when power is removed from the system. These bytes are all currently used or reserved; there are no user-definable bytes. Applications may read these bytes to determine system configuration, or write to them provided the byte definitions are adheared to. The function of each byte is listed in the following table. Byte definitions are contained in the *HP Vectra Technical Reference Manual Volume 2: System BIOS.*

Table 2.9

CMOS RAM Memory Map

Address	Type	Notes	Application
00H	RTC Reg	*	Seconds
01H	RTC Reg	*	Seconds alarm
02H	RTC Reg	*	Minutes
03H	RTC Reg	*	Minutes alarm
04H	RTC Reg	*	Hours
05H	RTC Reg	*	Hours alarm
06H	RTC Reg	*	Day of Week
07H	RTC Reg	*	Date of Month
08H	RTC Reg	*	Month
09H	RTC Reg	*	Year
0AH	RTC Reg	*	Status Register A
0BH	RTC Reg	*	Status Register B
0CH	RTC Reg	*	Status Register C
0DH	RTC Reg	*	Status Register D
0EH	RAM Byte	*	Diagnostic status byte
0FH	RAM Byte	*	Shutdown status byte
10H	RAM BYTE		Flexible disc drive type (A and B)
11H	RAM BYTE		Reserved
12H	RAM BYTE		Hard disc drive type (C and D)
13H	RAM BYTE		Reserved
14H	RAM BYTE		Equipment byte
15H	RAM BYTE		Low base memory byte
16H	RAM BYTE		High base memory byte
17H	RAM BYTE		Low expansion memory byte
18H	RAM BYTE		High expansion memory byte
19H-20H	RAM BYTE		Reserved
21H-27H	RAM BYTE	*	Reserved
28H	RAM BYTE		HP Checksum
29H	RAM BYTE	* %	Reserved
2AH-2BH	RAM BYTE	* %	Reserved
2CH-2DH	RAM BYTE	* %	Reserved
2EH-2FH	RAM BYTE	*	2 byte CMOS checksum
30H	RAM BYTE	*	Low expansion memory byte
31H	RAM BYTE	*	High expansion memory byte
32H	RAM BYTE	*	Date century byte
33H	RAM BYTE	*	Information flags
34H-3FH	RAM BYTE		Reserved

* Indicate bytes which are not included in the CMOS checksum calculation.

% These bytes will be included in the HP checksum calculation.

Flexible Disc Controller Subsystem

The flexible disc controller subsystem is responsible for converting high level software commands into the control and data signals used by a flexible disc drive. The flexible disc controller subsystem can support up to two flexible disc drives. The flexible drives supported are the HP45812A 1.2 MB Internal Flexible Disc Drive and the HP45811A 360 KB Internal Flexible Disc Drive. The subsystem controller is located on the processor board. It interfaces to the various drive configurations via a 34-pin connector.

Jumpers

There are three jumpers on the processor board used to configure the flexible disc controller subsystem. The jumpers are: EE, EC, ED; E3, E2, E1; and E7, E8. The following figure shows the configurations for these jumpers.

FDC Jumper Configurations

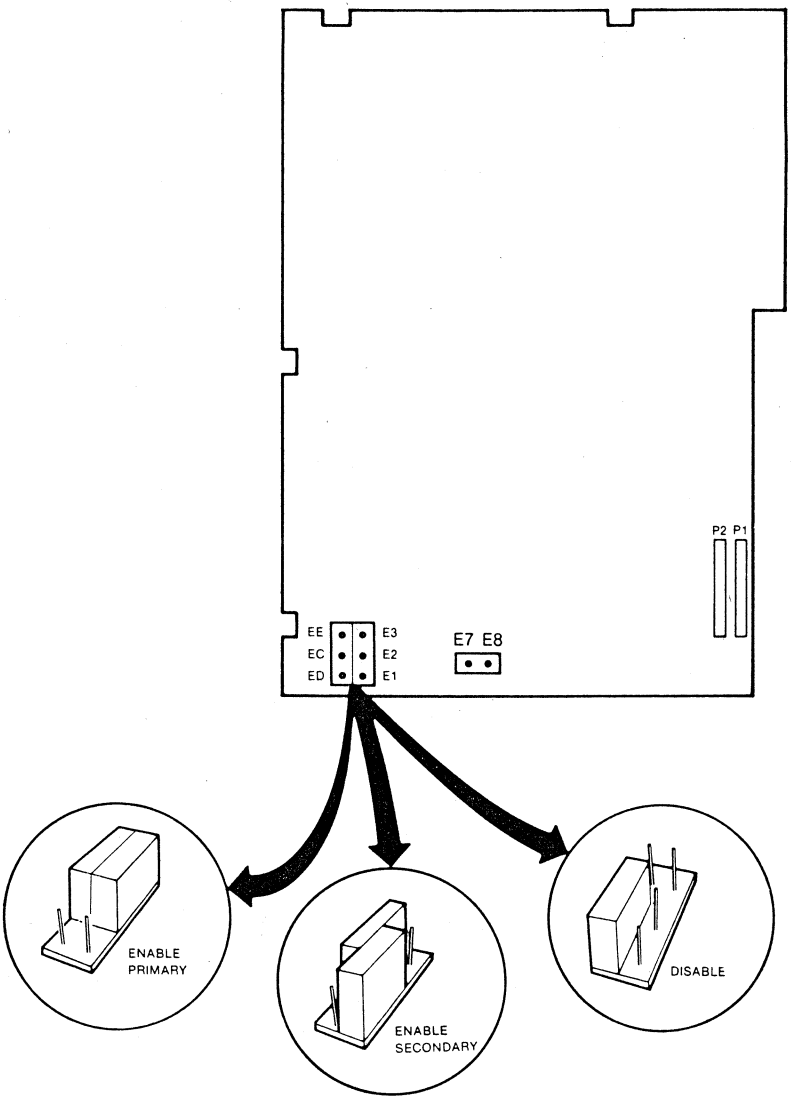


Figure 12

The jumper EE, EC, ED is used to select or deselect the flexible disc controller subsystem on the processor board. Placing a shunt between EE and EC enables the flexible disc subsystem (operation state-default). Placing a shunt between EC and ED disables the flexible disc subsystem.

The jumper E3, E2, E1 selects the location of the interface registers in the system I/O map. Placing a shunt between E3 and E2 selects the primary addressing, 3F0H through 3F7H (operational state-default). Placing a shunt between E1 and E2 selects the secondary addressing, 370H through 377H.

The jumper E7, E8 closes the phase lock loop (PLL) feedback path. The operational state is with a shunt between E7 and E8, which closes the feedback path. The removal of this shunt allows adjustments to the PLL and is not the operational state.

FDC Function

The flexible disc controller subsystem is responsible for: generating various signals needed to control the electromechanical parts of the drive, interpreting the status signals received from the drive, and converting between parallel and serial data formats. It is centered around the NEC 765A flexible disc controller (FDC) chip.

The FDC chip converts parallel data from the 80286 to serial data for the write path, and inversely, converts serial data from the read path to parallel data for the 80286. The FDC chip transfers parallel data to and from the system memory space via DMA (Channel 2). Commands to the FDC chip and status information from it are transferred via programmed I/O. Command termination and error conditions are signaled through interrupts (IRQ6). The subsystem employs an analog phase locked loop (PLL) to generate a clock synchronous to the disc data. This clock is used by the FDC chip during disc read transfers. The PLL can operate at 250kHz, 300kHz, or 500kHz data rates. The data rates are selected via the digital control port.

System-to-Subsystem Interface

The flexible disc controller subsystem interfaces with the microprocessor through six registers. There are three write registers and three read registers. The following table lists the registers and their primary and secondary I/O addresses.

Table 2.10

Accessible Registers

Register	R/W	I/O Address Primary	Secondary
Digital Output Register	W	3F2	372
Digital Control Register	W	3F7	377
FDC Data Register	R/W	3F5	375
FDC Status Register	R	3F4	374
Digital Input Register	R	3F7	377

Digital Output Register

Bit	Data	Definition
7		Reserved
6		Reserved
5		Drive B motor enable, active high turns on motor 5 1/4" drive
4		Drive A motor enable, active high turns on motor 5 1/4" drive
3		Interrupt and DMA enable, activ high
2		FDC reset, active low will reset
1		Reserved
0	0	Drive select, Drive A
	1	Drive B

Digital Control Register

Bit	Data	Definition
7		3 1/2" motor control, active high turn on motor
1		Most significant bit in rate select code of PLL
0		Least significant bit in rate select code of PLL

Bit		Data
1	0	kHz
0	0	500
0	1	300
1	0	250

FDC Status Register

Bit	Data	Definition
7		Request for master(RQM) indicates data register is ready to send or receive data to or from the 80286.
6	1	Data Input/Output (DIO). Data transfer from the data register of the FDC to the 80286.
	0	Data transfer from the 80286 to the data register of the FDC.
5		Disc controller is in non-DMA mode (NDM).
4		Disc controller is busy (CB) read/write being executed.
3-2		Reserved
1		Disc drive B busy (DBB) in seek mode.
0		Disc drive A Busy (DBA) in seek mode.

FDC Data Register

This is a bidirectional register. Write Function: 8-bit data is written to FDC chip as commands via programmed I/O and write data during disc transfers via DMA.

Read Function: 8-bit data is read from FDC chip as result of commands via programmed I/O and read data during disc transfers via DMA.

Digital Input Register

Bit	Data	Definiton
7		State of the disc change line. Becomes active when the drive door is opened and at power-on. It will remain active until reset when a step pulse is issued. It is active high.

FDC-to-Disc Drive Interface

The 5 1/4 inch disc drive interface with the controller is through control signals, status signals and data signals. The 5 1/4 inch drives are daisy-chained on one connector and cable. The following table shows the pin assignments for the 34-pin connector. The input or output of the signals are referenced to the processor board.

In the HP Vectra system the HP45812A 1.2 MB Internal Flexible Disc Drive provides a ~DISC CHG signal on the drive interface pin 34. This signal indicates the detection of the drive door being opened. The HP45811A 360 KB Internal Flexible Disc Drive does not provide a ~DISC CHG signal on pin 34. Thus, this signal will always be inactive and the system cannot detect a possible media

change via hardware. (Refer to *HP Vectra Technical Reference Manual Volume 2: System BIOS* for the appropriate techniques to accomplished this detection.)

Table 2.11

Control Interface Pin Assignments

Pin	I/O	Signal Name
2	O	~REDWRCUR
4		Not used
6		Not used
8	I	~INDEX
10	O	~MOTEN 1
12	O	~DS2
14	O	~DS1
16	O	~MOTEN2
18	O	~DIRECTION
20	O	~STEP
22	O	~WRITE DATA
24	O	~WRITE ENABLE
26	I	~TRACK 00
28	I	~WRITE PROTECT
30	I	~READ DATA
32	O	~HEAD SELECT
34	I	~DISC CHG
1-33		Odd pins are ground

The following signal descriptions are for the interface between the controller and the 5 1/4 inch drives. All output signals are driven with the 7438. All inputs are 74LS14 wth 2.2K pull-ups.

Control Signals

Signal	I/O	Description
~DIRECTION	O	Active level indicates the read/write head to move toward the spindle. Inactive level instructs the heads to move away from the spindle.
~DS1 or ~DS2	O	Drive select lines 1 or 2 are used by drives 1 and 2 to degate all adapter and receiver drivers from the attachment, except ~MOTEN, when the line associated with a drive is inactive.
~HEAD SELECT	O	Head 1 will be selected when this line is active. An inactive level will select the head on side 0.
~MOTEN1 or ~MOTEN2	O	~MOTEN controls the spindle motor of the drive (1 or 2) associated with each line. The line controls the spindle motor such that it starts when the line becomes active and stops when the line becomes inactive.
~REDWRCUR	O	Selects read channel filters and write current on the 1.2 MB drive. It is active only when the PLL is in 300kHz mode and inactive for the 500kHz and 250kHz modes.
~STEP	O	The selected drive moves the read/write head one cylinder in or out per the direction line for each pulse present on this line. Motion is started each time the signal changes from an active to inactive level.
~WRITE ENABLE	O	Disables write current in the drive head unless this line is active.

Data Signals

Signal	I/O	Description
~READ DATA	I	The selected drive supplies a pulse on the line for each flux change encountered on the disc.
~WRITE DATA	O	For each inactive to active transition of this line while write enable is active, the selected drive causes a flux change to be stored on the disc.

Status Signals

Signal	I/O	Description
~DISC CHG	I	Indicates that the drive door has been opened.
~INDEX	I	The selected drive supplies one pulse per disc revolution on this line.
~TRACK 00	I	The selected drive makes this line active if the read/write head is over track 0.
~WRITE PROTECT	I	The selected drive makes this line active if a write-protected disc is mounted in the drive.

SECTION 3. BASIC INPUT/ OUTPUT SYSTEM

The Basic Input/Output System (BIOS) is a set of programs that is stored in the ROM on the processor extension card in the F0000 segment. For a more complete description of the BIOS refer to *HP Vectra Technical Reference Manual Volume 2: System BIOS.*

Table 3.1

BIOS Interrupt Summary

Address Range	INT	BIOS Entry	Summary
8-B	2	NMI	Parity error is detected.
14-17	5	PRINT SCREEN	Default routine that prints the video screen characters.
20-23	8	TIMER INT	Called each clock tick (18.2 sec.).
24-27	9	KEYBOARD INT	Handles keyboard activity and controller.
40-43	10	VIDEO IO	Handles all video reads and writes, palettes, lightpens, and scrolling.
44-47	11	EQUIPMENT DETERMINATION	Reports attached devices, i.e., printers, RS-232 ports,video, disc drives, 80287.

Address Range	INT	BIOS Entry	Summary
48-4B	12	DETERMINE MEMORY SIZE	Reports the number of contiguous 1Kb blocks of memory.
4C-4F	13	DISKETTE INT	Reset, status, read, write, verify, format, read DASD, read change line, and set DASD.
50-53	14	RS232 IO	Initialize port, read character, write character read status.
54-57	15	CASSETTE IO & 80286 FUNCTIONS	Device open, device close, program termination, event wait, joystick support, system request key, wait, move block, determines extended memory size, processor to virtual mode, device busy loop, and interrupt complete flag set.
58-5B	16	KEYBOARD IO	Read character, read buffer status, read shift status.
5C-5F	17	PRINTER IO	Initialize port, print character, read status.
64-67	19	BOOTSTRAP	Power up code.
68-6B	1A	TIME OF DAY	Read and write clock, time, date, set and reset alarm.

SECTION 4. KEYBOARD INTERFACE

The HP Vectra interface to its keyboard is through an HP-Human Interface Link (HP-HIL). HP-HIL is the Hewlett-Packard proprietary standard for interfacing one or more input devices to the system. HP-HIL provides an asynchronous serial communication protocol that enables the user to select a set of input devices (up to seven), and connect them to the HP Vectra without purchasing additional I/O cards or using additional I/O slots. Cable management is simplified because the various input devices are "daisy-chained" from the HP Vectra. The term daisy-chained refers to process of plugging the first input device into the HP Vectra, plugging the second input device into the first, and so on.

The keyboard interface consists of two blocks: the keyboard controller, and the HP-HIL interface. This section will describe these two blocks. Also included, is a cursory description of the data flow necessary to receive a keycode from the keyboard and to send a command to the keyboard. For a detailed description of the keyboard interface refer to the *HP Vectra Technical Reference Manual Volume 2: System BIOS*.

Keyboard Controller

The keyboard controller is an 8041 microcomputer (U87) which has been programmed to provide a communication path between the BIOS and/or application programs and the HP-HIL subsystem. It also provides three output lines and one input line for various hardware system purposes. The 8041 provides two logical paths for communicating with the 80286: the application path and the keyboard path.

Application Path

The application path consists of two read/write registers and an interrupt line. The register at port 60H is used for keyboard commands and data, and controller data. The register at port 64H is used to write commands to the controller and to read the 8041 status. The interrupt line (OBFINT) is set to interrupt when the 8041 places data in the read register at port 60H.

Keyboard Path

The keyboard path provides a way for the 80286 to receive commands to be sent to the HP-HIL keyboard, and to return data from the HP-HIL keyboard, through the keyboard controller. The keyboard path consists of a read register at port 69H, a write register at port 68H, and an interrupt line.

The read register is a buffered version of the 8041 Port 1 (P10-P17). The 8041 places data on its port, then signals the 80286 that new information is available by pulsing ~INTHP (P23) low. This causes HPINT to go active, generating an interrupt. When the 80286 has completed processing the interrupt, it clears HPINT by doing a write to port 6AH. This write informs the 8041 (through its T1 input) that the 80286 has completed processing the data.

Output Lines

The keyboard controller also provides three output lines for uses in other parts of the system. These output lines are: the AP line, the RC line, and the A20__GATE.

The output line AP provides a 60 Hz signal to the HP-HIL controller for use in polling the HP-HIL.

The second line, RC, resets the 80286 when pulsed low. It is used to return the processor to the real-address mode from protected mode or to reset the system in response to a Control-Alt-Del.

The A20__GATE either enables the 80286 address line A20 (when high) or forces it to a logical 0 (when low). It is used to cause 80286 addresses above 1 Megabyte to wrap when operating in the real-address mode. Also, the 8041 writes to port 69H.

Input Line

The keyboard controller has an input line (KBINH) which is used by the optional keylock keyboard inhibit switch. This front-panel switch allows keyboard operation to be inhibited by turning the key to the lock position. When locked, the keyboard responses will still be returned, but scan codes from the keyboard will not be returned by the 8041.

HP-HIL Interface

The keyboard (and other input devices) are connected to the HP Vectra via a 4-pin HP-HIL interface connector. See table 4.1 for the pin assignments. The Serial In and Serial Out signals are connected to the HP-HIL controller (U777), which is an integrated circuit developed by Hewlett-Packard to control the HP-HIL. The HP-HIL controller converts parallel data from the 80286 into serial data on the HP-HIL, and conversely, converts serial data from the input devices into parallel data to be read by the 80286. Approximately 60 times per second, the HP-HIL controller polls the input devices to read any input they may ready, and to send commands and data to the devices. After receiving data from one or more input devices, the HP-HIL controller interrupts the 80286 by asserting "CERBINT", and then the 80286 reads the data from the HP-HIL controller.

Table 4.1

Keyboard Connector Pin Assignments

Pin	Assignment
1	+ 12 Vdc
2	Serial In
3	Serial Out
4	Ground

Keyboard Interface

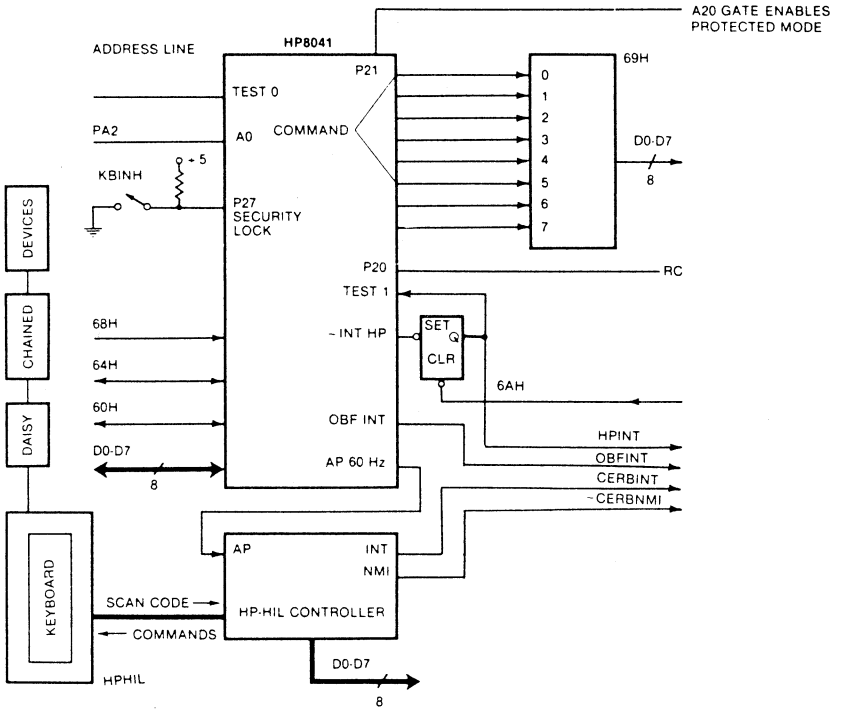


Figure 13

Keyboard-to-System Interface

When a key is pressed or released on the keyboard, the corresponding scan code for that key motion is reported over the HP-HIL to the HP-HIL controller. The HP-HIL controller interrupts the 80286, which executes the HP-HIL driver to read the scan codes(s). Inputs from the keyboard are passed to the logical keyboard driver, where they may be translated, then sent to the 8041 through port 68H. The 8041 then reports the scan code by placing it in its output buffer, causing an output buffer interrupt (OBFINT). Then, the scan code may be read by either the BIOS or directly by an application.

System-to-Keyboard Interface

When the BIOS requires commands to be sent to the keyboard (i.e., to program the LED's), it sends the byte(s) to port 60H of the 8041. The 8041 acknowledges each byte by returning OFAH to Port 60H. It then places the command in output Port 69H and causes an interrupt (HPINT) by pulsing ~INTHP (P23) low. In response to this interupt the 80286 executes the logical keyboard driver, which the reads the command from Port 69H and passes it on to the HP-HIL driver. The HP-HIL driver translates the command and sends it to the HP-HIL controller to be sent to the keyboard. When the command processing is completed, the logical keyboard driver clears HPINT by writing to Port 6AH, freeing Port 69H.

The following is a figure that shows the HP Vectra keyboard with the keys numbered and the American legend. Refer to Appendix B for the international keyboards and the keyboard scan codes.

HP Vectra Keyboard (American)

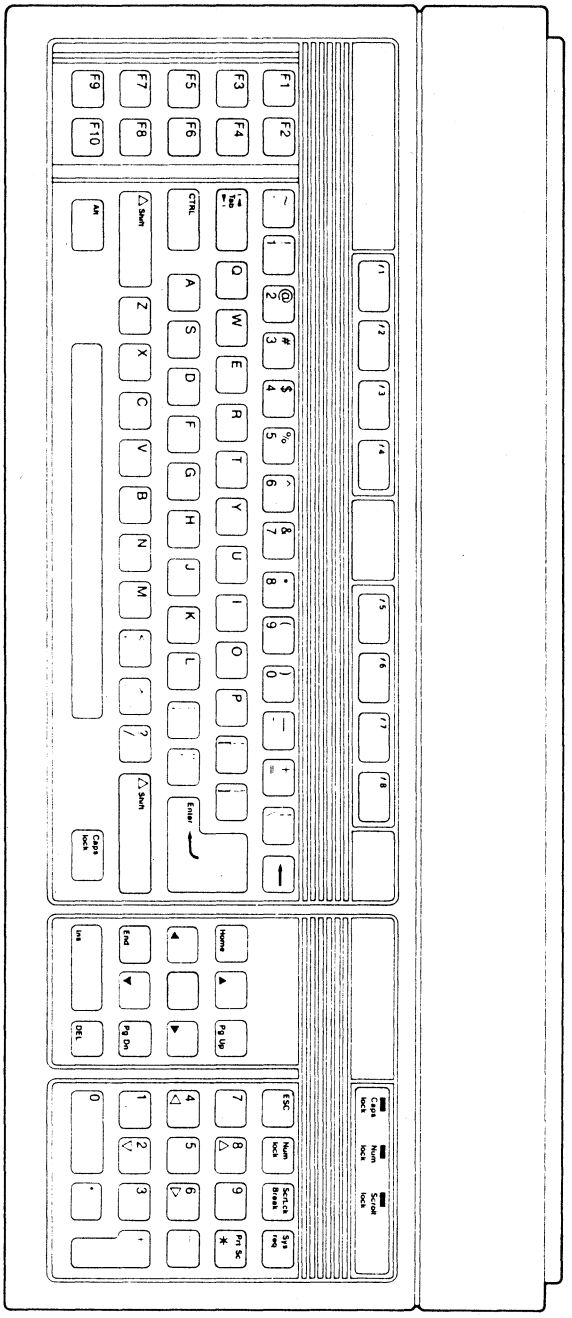


Figure 14

SECTION 5. KEYSTROKES AND CHARACTERS

Keystroke	Note	ASCII Value Hex	Dec	Character Set STD	HP	Color Background	Foreground
Ctrl 2		00	0	Blank (Null)	N U	Black	Black
Ctrl A		01	1	☺	S T	Black	Blue
Ctrl B		02	2	☻	S H	Black	Green
Ctrl C		03	3	♥	E H	Black	Cyan
Ctrl D		04	4	♦	E T	Black	Red
Ctrl E		05	5	♣	E Q	Black	Magenta
Ctrl F		06	6	♠	A K	Black	Brown
Ctrl G		07	7	•		Black	Lt. Gray
Ctrl H Backspace, Shift Backspace		08	8	◘	B S	Black	Dk. Gray
Ctrl I		09	9	○	H T	Black	Lt. Blue
Ctrl J Ctrl		0A	10	◙	L F	Black	Lt. Green
Ctrl K		0B	11	♂	V T	Black	Lt. Green
Ctrl L		0C	12	♀	F F	Black	Lt. Red
Ctrl M Shift		0D	13	♪	C R	Black	Lt. Magenta

Keystroke	Note	ASCII Value Hex	Dec	Character Set STD	HP	Color Background	Foreground
Ctrl N		0E	14	♫	S O	Black	Yellow
Ctrl O		0F	15	☼	S I	Black	White
Ctrl P		10	16	►	D L	Blue	Black
Ctrl Q		11	17	◄	D 1	Blue	Blue
Ctrl R		12	18	↕	D 2	Blue	Green
Ctrl S		13	19	!!	D 3	Blue	Cyan
Ctrl T		14	20	¶	D 4	Blue	Red
Ctrl U		15	21	§	N K	Blue	Magenta
Ctrl V		16	22	■	S Y	Blue	Brown
Ctrl W		17	23	↨	E B	Blue	Lt. Gray
Ctrl X		18	24	↑	C N	Blue	Dk. Gray
Ctrl Y		19	25	↓	E M	Blue	Lt. Blue
Ctrl Z		1A	26	→	S B	Blue	Lt. Green
Ctrl [, Esc, Shift Esc, Ctrl Esc		1B	27	←	E C	Blue	Lt. Cyan
Ctrl \		1C	28	∟	F S	Blue	Lt. Red
Ctrl]		1D	29	↔	G S	Blue	Lt. Magenta
Ctrl 6		1E	30	▲	R S	Blue	Yellow
Ctrl -		1F	31	▼	V S	Blue	White

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Space Bar, Shift, Space, Ctrl Space, or Alt Space		20	32	Blank Space		Green	Black
!	*	21	33	!	!	Green	Blue
"	*	22	34	"	"	Green	Green
#	*	23	35	#	#	Green	Cyan
$	*	24	36	$	$	Green	Red
%	*	25	37	%	%	Green	Magenta
&	*	26	38	&	&	Green	Brown
'		27	39	'	'	Green	Lt. Gray
(	*	28	40	(	(	Green	Dk. Gray
)	*	29	41	)	)	Green	Lt. Blue
*	&,*	2A	42	*	*	Green	Lt. Green
+	*	2B	43	+	+	Green	Lt. Cyan
,		2C	44	,	,	Green	Lt. Red
		2D	45	-	-	Green	Lt. Magenta
.	$	2E	46	.	.	Green	Yellow
/		2F	47	/	/	Green	White
0	+	30	48	0	0	Cyan	Black
1	+	31	49	1	1	Cyan	Blue
2	+	32	50	2	2	Cyan	Green
3	+	33	51	3	3	Cyan	Cyan
4	+	34	52	4	4	Cyan	Red
5	+	35	53	5	5	Cyan	Magenta
6	+	36	54	6	6	Cyan	Brown
7	+	37	55	7	7	Cyan	Lt. Gray
8	+	38	56	8	8	Cyan	Dk. Gray
9	+	39	57	9	9	Cyan	Lt. Blue

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
:	*	3A	58	:	:	Cyan	Lt. Green
;		3B	59	;	;	Cyan	Lt. Cyan
<	*	3C	60	<	<	Cyan	Lt. Red
=		3D	61	=	=	Cyan	Lt. Magenta
>	*	3E	62	>	>	Cyan	Yellow
?	*	3F	63	?	?	Cyan	White
@	*	40	64	@	@	Red	Black
A	#	41	65	A	A	Red	Blue
B	#	42	66	B	B	Red	Green
C	#	43	67	C	C	Red	Cyan
D	#	44	68	D	D	Red	Red
E	#	45	69	E	E	Red	Magenta
F	#	46	70	F	F	Red	Brown
G	#	47	71	G	G	Red	Lt. Gray
H	#	48	72	H	H	Red	Dk. Gray
I	#	49	73	I	I	Red	Lt. Blue
J	#	4A	74	J	J	Red	Lt. Green
K	#	4B	75	K	K	Red	Lt. Cyan
L	#	4C	76	L	L	Red	Lt. Red
M	#	4D	77	M	M	Red	Lt. Magenta
N	#	4E	78	N	N	Red	Yellow
O	#	4F	79	O	O	Red	White
P	#	50	80	P	P	Magenta	Black
Q	#	51	81	Q	Q	Magenta	Blue
R	#	52	82	R	R	Magenta	Green
S	#	53	83	S	S	Magenta	Cyan
T	#	54	84	T	T	Magenta	Red
U	#	55	85	U	U	Magenta	Magenta
V	#	56	86	V	V	Magenta	Brown
W	#	57	87	W	W	Magenta	Lt. Gray

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
X	#	58	88	X	X	Magenta	Dk. Gray
Y	#	59	89	Y	Y	Magenta	Lt. Blue
Z	#	5A	90	Z	Z	Magenta	Lt. Green
[		5B	91	[	[	Magenta	Lt. Cyan
\		5C	92	\	\	Magenta	Lt. Red
]		5D	93	]	]	Magenta	Lt. Magenta
^	*	5E	94	^	^	Magenta	Yellow
_	*	5F	95	_	_	Magenta	White
'		60	96	'	'	Yellow	Black
a	-	61	97	a	a	Yellow	Blue
b	-	62	98	b	b	Yellow	Green
c	-	63	99	c	c	Yellow	Cyan
d	-	64	100	d	d	Yellow	Red
e	-	65	101	e	e	Yellow	Magenta
f	-	66	102	f	f	Yellow	Brown
g	-	67	103	g	g	Yellow	Lt. Gray
h	-	68	104	h	h	Yellow	Dk. Gray
i	-	69	105	i	i	Yellow	Lt. Blue
j	-	6A	106	j	j	Yellow	Lt. Green
k	-	6B	107	k	k	Yellow	Lt. Cyan
l	-	6C	108	l	l	Yellow	Lt. Red
m	-	6D	109	m	m	Yellow	Lt. Magenta
n	-	6E	110	n	n	Yellow	Yellow
o	-	6F	111	o	o	Yellow	White
p	-	70	112	p	p	White	Black
q	-	71	113	q	q	White	Blue
r	-	72	114	r	r	White	Green
s	-	73	115	s	s	White	Cyan
t	-	74	116	t	t	White	Red
u	-	75	117	u	u	White	Magenta

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
v	-	76	118	v	v	White	Brown
w	-	77	119	w	w	White	Lt. Gray
x	-	78	120	x	x	White	Dk. Gray
y	-	79	121	y	y	White	Lt. Blue
z	-	7A	122	z	z	White	Lt. Green
{	*	7B	123	{	{	White	Lt. Cyan
	*	7C	124	|	|	White	Lt. Red
}	*	7D	125	}	}	White	Lt. Magenta
~	*	7E	126	~	~	White	Yellow
Ctrl ←		7F	127	△	■	White	White
Alt 128	%"	80	128	Ç	HP Reserved	Black	Black
Atl 129	%"	81	129	ü	HP Reserved	Black	Blue
Alt 130	%"	82	130	é	HP Reserved	Black	Green
Alt 131	%"	83	131	â	HP Reserved	Black	Cyan
Alt 132	%"	84	132	ä	HP Reserved	Black	Red
Alt 133	%"	85	133	à	HP Reserved	Black	Magenta
Alt 134	%"	86	134	å	HP Reserved	Black	Brown
Alt 135	%"	87	135	ç	HP Reserved	Black	Lt. Gray
Alt 136	%"	88	136	ê	HP Reserved	Black	Dk. Gray
Alt 137	%"	89	137	ë	HP Reserved	Black	Lt. Blue
Alt 138	%"	8A	138	è	HP Reserved	Black	Lt. Green
Alt 139	%"	8B	139	ï	HP Reserved	Black	Lt. Green
Alt 140	%"	8C	140	î	HP Reserved	Black	Lt. Red

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Alt 141	%"	8D	141	ì	HP Reserved	Black	Lt. Magenta
Alt 142	%"	8E	142	Ä	HP Reserved	Black	Yellow
Alt 143	%"	8F	143	Å	HP Reserved	Black	White
Alt 144	%"	90	144	É	HP Reserved	Blue	Black
Alt 145	%"	91	145	æ	HP Reserved	Blue	Blue
Alt 146	%"	92	146	Æ	HP Reserved	Blue	Green
Alt 147	%"	93	147	ô	HP Reserved	Blue	Cyan
Alt 148	%"	94	148	ö	HP Reserved	Blue	Red
Alt 149	%"	95	149	ò	HP Reserved	Blue	Magenta
Alt 150	%"	96	150	û	HP Reserved	Blue	Brown
Alt 151	%"	97	151	ù	HP Reserved	Blue	Lt. Gray
Alt 152	%"	98	152	ÿ	HP Reserved	Blue	Dk. Gray
Alt 153	%"	99	153	ö	HP Reserved	Blue	Lt. Blue
Alt 154	%"	9A	154	ü	HP Reserved	Blue	Lt. Green
Alt 155	%"	9B	155	¢	HP Reserved	Blue	Lt. Cyan
Alt 156	%"	9C	156	£	HP Reserved	Blue	Lt. Red
Alt 157	%"	9D	157	¥	HP Reserved	Blue	Lt. Magenta
Alt 158	%"	9E	158	Pt	HP Reserved	Blue	Yellow
Alt 159	%"	9F	159	ƒ	HP Reserved	Blue	White
Alt 160	%	A0	160	á		Green	Black

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Alt 161	%	A1	161	í	À	Green	Blue
Alt 162	%	A2	162	ó	Â	Green	Green
Alt 163	%	A3	163	ú	È	Green	Cyan
Alt 164	%	A4	164	ñ	Ê	Green	Red
Alt 165	%	A5	165	Ñ	Ë	Green	Magenta
Alt 166	%	A6	166	ª	Î	Green	Brown
Alt 167	%	A7	167	º	Ï	Green	Lt. Gray
Alt 168	%	A8	168	¿	´	Green	Dk. Gray
Alt 169	%	A9	169		`	Green	Lt. Blue
Alt 170	%	AA	170	⌐	ˆ	Green	Lt. Green
Alt 171	%	AB	171	½	¨	Green	Lt. Cyan
Alt 172	%	AC	172	¼	˜	Green	Lt. Red
Alt 173	%	AD	173	¡	Ù	Green	Lt. Magenta
Alt 174	%	AE	174	<<	Û	Green	Yellow
Alt 175	%	AF	175	>>	£	Green	White
Alt 176	%	B0	176	⣿	—	Cyan	Black
Alt 177	%	B1	177	▒	Ý	Cyan	Blue
Alt 178	%	B2	178	▓	ý	Cyan	Green
Alt 179	%	B3	179	│	°	Cyan	Cyan
Alt 180	%	B4	180	┤	Ç	Cyan	Red
Alt 181	%	B5	181	╡	ç	Cyan	Magenta
Alt 182	%	B6	182	╢	Ñ	Cyan	Brown
Alt 183	%	B7	183	╖	ñ	Cyan	Lt. Gray
Alt 184	%	B8	184	╕	¡	Cyan	Dk. Gray
Alt 185	%	B9	185	╣	¿	Cyan	Lt. Blue
Alt 186	%	BA	186	║	★	Cyan	Lt. Green
Alt 187	%	BB	187	╗	£	Cyan	Lt. Cyan
Alt 188	%	BC	188	╝	¥	Cyan	Lt. Red
Alt 189	%	BD	189	╜	§	Cyan	Lt. Magenta
Alt 190	%	BE	190	╛	ƒ	Cyan	Yellow

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Alt 191	%	BF	191		¢	Cyan	White
Alt 192	%	C0	192		à	Red	Black
Alt 193	%	C1	193		è	Red	Blue
Alt 194	%	C2	194		ò	Red	Green
Alt 195	%	C3	195		ù	Red	Cyan
Alt 196	%	C4	196		á	Red	Red
Alt 197	%	C5	197		é	Red	Magenta
Alt 198	%	C6	198		ó	Red	Brown
Alt 199	%	C7	199		ú	Red	Lt. Gray
Alt 200	%	C8	200		â	Red	Dk. Gray
Alt 201	%	C9	201		ê	Red	Lt. Blue
Alt 202	%	CA	202		ô	Red	Lt. Green
Alt 203	%	CB	203		û	Red	Lt. Cyan
Alt 204	%	CC	204		ä	Red	Lt. Red
Alt 205	%	CD	205		ë	Red	Lt. Magenta
Alt 206	%	CE	206		ö	Red	Yellow
Alt 207	%	CF	207		ü	Red	White
Alt 208	%	D0	208		Â	Magenta	Black
Alt 209	%	D1	209		Ê	Magenta	Blue
Alt 210	%	D2	210		Ô	Magenta	Green
Alt 211	%	D3	211		Æ	Magenta	Cyan
Alt 212	%	D4	212		Â	Magenta	Red
Alt 213	%	D5	213		Í	Magenta	Magenta
Alt 214	%	D6	214		Ô	Magenta	Brown
Alt 215	%	D7	215		æ	Magenta	Lt. Gray
Alt 216	%	D8	216		Ä	Magenta	Dk. Gray
Alt 217	%	D9	217		Ì	Magenta	Lt. Blue
Alt 218	%	DA	218		Ö	Magenta	Lt. Green
Alt 219	%	DB	219		Ü	Magenta	Lt. Cyan
Alt 220	%	DC	220		É	Magenta	Lt. Red

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Alt 221	%	DD	221	▌	ï	Magenta	Lt. Magenta
Alt 222	%	DE	222	▐	β	Magenta	Yellow
Alt 223	%	DF	223	▀	ð	Magenta	White
Alt 224	%	E0	224	α	Á	Yellow	Black
Alt 225	%	E1	225	β	Ã	Yellow	Blue
Alt 226	%	E2	226	Γ	ã	Yellow	Green
Alt 227	%	E3	227	π	Đ	Yellow	Cyan
Alt 228	%	E4	228	Σ	đ	Yellow	Red
Alt 229	%	E5	229	δ	Í	Yellow	Magenta
Alt 230	%	E6	230	μ	Ì	Yellow	Brown
Alt 231	%	E7	231	τ	Ó	Yellow	Lt. Gray
Alt 232	%	E8	232	Φ	Ò	Yellow	Dk. Gray
Alt 233	%	E9	233	θ	Õ	Yellow	Lt. Blue
Alt 234	%	EA	234	Ω	õ	Yellow	Lt. Green
Alt 235	%	EB	235	δ	˘	Yellow	Lt. Cyan
Alt 236	%	EC	236	∞	ˉ	Yellow	Lt. Red
Alt 237	%	ED	237	φ	Ú	Yellow	Lt. Magenta
Alt 238	%	EE	238	ϵ	Ÿ	Yellow	Yellow
Alt 239	%	EF	239	∩	ÿ	Yellow	White
Alt 240	%	F0	240	≡	Þ	White	Black
Alt 241	%	F1	241	±	þ	White	Blue
Alt 242	%	F2	242	≥	˙	White	Green
Alt 243	%	F3	243	≤	μ	White	Cyan
Alt 244	%	F4	244	⌠	¶	White	Red
Alt 245	%	F5	245	⌡	¾	White	Magenta
Alt 246	%	F6	246	÷	‾	White	Brown
Alt 247	%	F7	247	≈	¼	White	Lt. Gray
Alt 248	%	F8	248	○	½	White	Dk. Gray
Alt 249	%	F9	249	●	ª	White	Lt. Blue

Keystroke		ASCII Value		Character Set		Color	
	Note	Hex	Dec	STD	HP	Background	Foreground
Alt 250	%	FA	250	•	₉	White	Lt. Green
Alt 251	%	FB	251	√	<<	White	Lt. Cyan
Alt 252	%	FC	252	₇	■	White	Lt. Red
Alt 253	%	FD	253	²	>>	White	Lt. Magenta
Alt 254	%	FE	254	■	±	White	Yellow
Alt 255	%	FF	255	**BLANK**		White	White

---

* Press and hold the shift key, while pressing the appropriate key.

To type uppercase letters: press and hold the shift key while pressing a letter key, or press Caps Lock key then press the appropriate key.

+ Numbers may be typed by pressing the numeric keys on the top row of the keyboard, or in Num Lock mode press the numeric keypad keys.

% After pressing the Alt key, the three digits must be pressed on the numeric keypad.

- To type lowercase letters: press the appropriate key, or press Caps Lock then hold the shift key and press the appropriate key.

& To type an asterisk (*): press and hold the shift key, then press the 8 key; or press the Prt key.

$ To type a period (.): press the . key, or press shift then the Del key, or press Num Lock then the Del key.

'' HP may change these characters without notice.

The foreign character sets are given in Appendix A.

SECTION 6. POWER SUPPLY

The HP Vectra power supply provides the power for:

- the processor board
- the backplane I/O slots
- the flexible disc drives
- the hard disc drives
- the keyboard or other input devices
- the primary power to the monitor

The power supply, and its components (the fan, AC receptacle, AC outlet, fuseholder, line select switch, and on/off switch) are located inside the main unit of the HP Vectra PC. The power supply and its components are installed in a steel and zinc plated enclosure. The following illustrations show the backview of the power supply components and the top view of the cables.

Power Supply Components

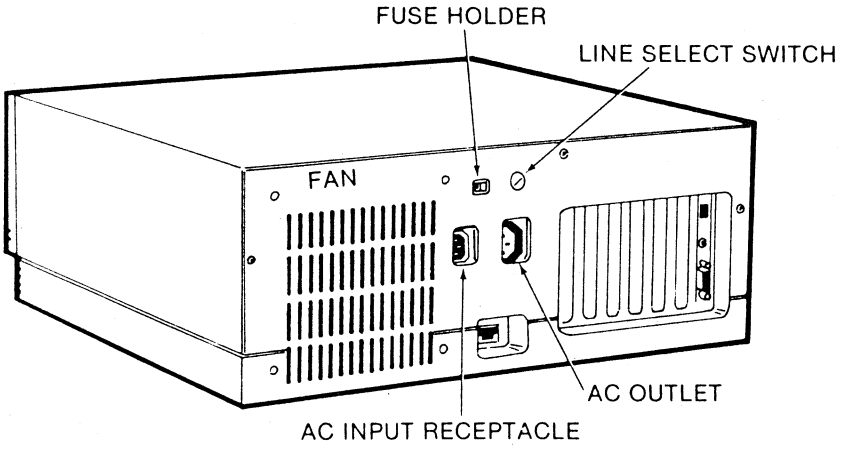


Figure 15

Power Supply Cabling

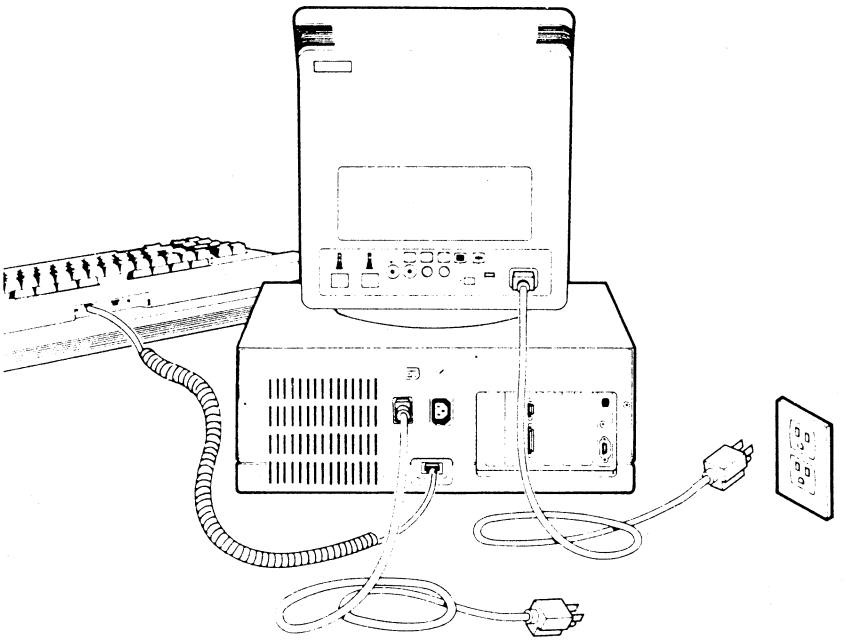


Figure 16

Input

The two line voltage levels are user-selectable by a switch and protected by an accessible five amp fuse. This fuse is shown in figure 16 and is easily accessible from the back panel of the unit. Should the fuse need to be replaced, use a fuse of the same type and rating, HP product number 2110-0729. The following chart defines the voltage input range.

Input Voltage
110V (+ 10% – 25%) @ 50/60 Hz (+/– 5%)
230V (+ 10% – 25%) @ 50/60 Hz (+/– 5%)

AC Inrush Current

AC inrush current is limited to 40 amps under any condition. Inrush current shall not open the line fuse under any condition.

Line Dropout

The power supply will continue regulated operation when a 20ms dropout occurs at the input under any condition, including low line at rated load.

Output

The HP Vectra PC establishes a five output power supply as defined in the following table.

Table 6.1

System Totals Output Voltages and Current

Startup (10 second) Output	Voltage Range	Minimum	Maximum	Ripple (p-p)
+5	+4.85 to +5.25V	5.0A	18.3A	50mv
+12	+11.4 to +12.6V	0.0A	1.0A	120mv
+12M	+11.4 to 13.2V	1.1A	5.5A	100mv
−5	−5.25 to −4.75	0.0A	0.25A	50mv
−12	−12.6 to −11.4	0.0A	0.25A	120mv
Total power: 176 watts maximum				

After Startup				
+5	+4.85 to +5.25V	5.0A	17.5A	50mv
+12	+11.4 to +12.6V	0.0A	1.0A	120mv
+12M	+11.4 to +12.6V	1.1A	2.4A	100mv
−5	−5.25 to −4.75	0.0A	0.25A	50mv
−12	−12.6 to −11.4	0.0A	0.25A	120mv
Total power: 135 watts				

Overvoltage Protection

Overvoltage protection takes place within 500us. Afterwards, the reset procedure to take is: unplug the system, wait for five minutes, plug in the system, then restart the system.

Overcurrent Protection

All outputs are protected (to ground or to other outputs) against short circuit. No damage shall result, however, the system will require the reset procedure as given in the preceding paragraph.

AC Outlet

Power supply has a switched AC outlet. This outlet is capable of supplying power to a load of 150 watts and an inrush current not exceeding 30 amps.

Undercurrent Protection

It is possible for any or all outputs to open without damage to the power supply. All outputs do not exceed overvoltage specifications given in the following chart.

Overvoltage Protection

Output	
+ 5V	7
+ 12M	16.8
+ 12	3 terminal regulators, inherent overvoltage protection.
− 5	
− 12	

Fan

The fan is a component of the power supply and provides 20CFM and cools the components of the system.

I/O Channel Budget

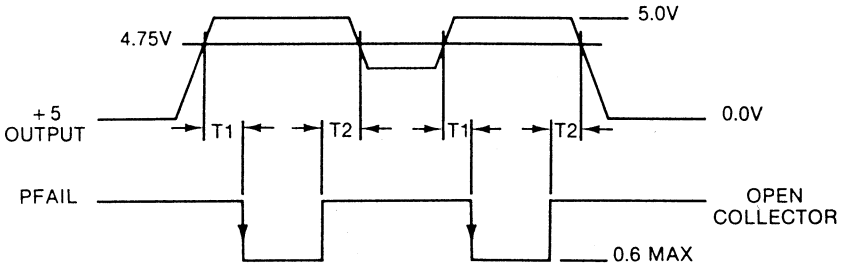
Each of the I/O channels can support an average of seven watts per channel. The following charts the power totals not to be exceeded for the I/O backplane slots.

+5V	7200ma
+12V	390ma
−5V	250ma
−12	250ma

PFAIL

The PFAIL signal indicates all power supply is valid within 100 msec after supplies are valid. The falling edge of PFAIL indicates to the CMOS clock to go into power-down mode and operate from the battery pack. PFAIL generates a reset to the system via an interrupt control. The following figure is a timing diagram of the PFAIL signal.

PFAIL Timing Diagram



T1: 100 msec MIN/300 msec MAX
T2: 100 usec MIN
RISE & FALL TIMES (10%-90%) 1 usec TYP

Figure 17

SECTION 7. MULTI-MODE VIDEO ADAPTER CARD

The HP45981A Multi-Mode Video Adapter Card has available memory to support eight pages of alpha and fast memory with full access interleaving. There is no need to wait for retrace to access memory for a clean display. An 8 x 16 dot alpha character cell is supported for improved alpha.

Other features include:

- ★ underline enhancement support
- ★ hardware that will support gray-scale for monochrome monitors
- ★ selectable HP or industry standard character sets
- ★ support for both 15kHz (200 line) and 25kHz (400 line) monitors, but not simultaneously

The following, figure 18, is a block diagram of the multi-mode video adapter card.

Multi-Mode Video Adapter Card Block Diagram

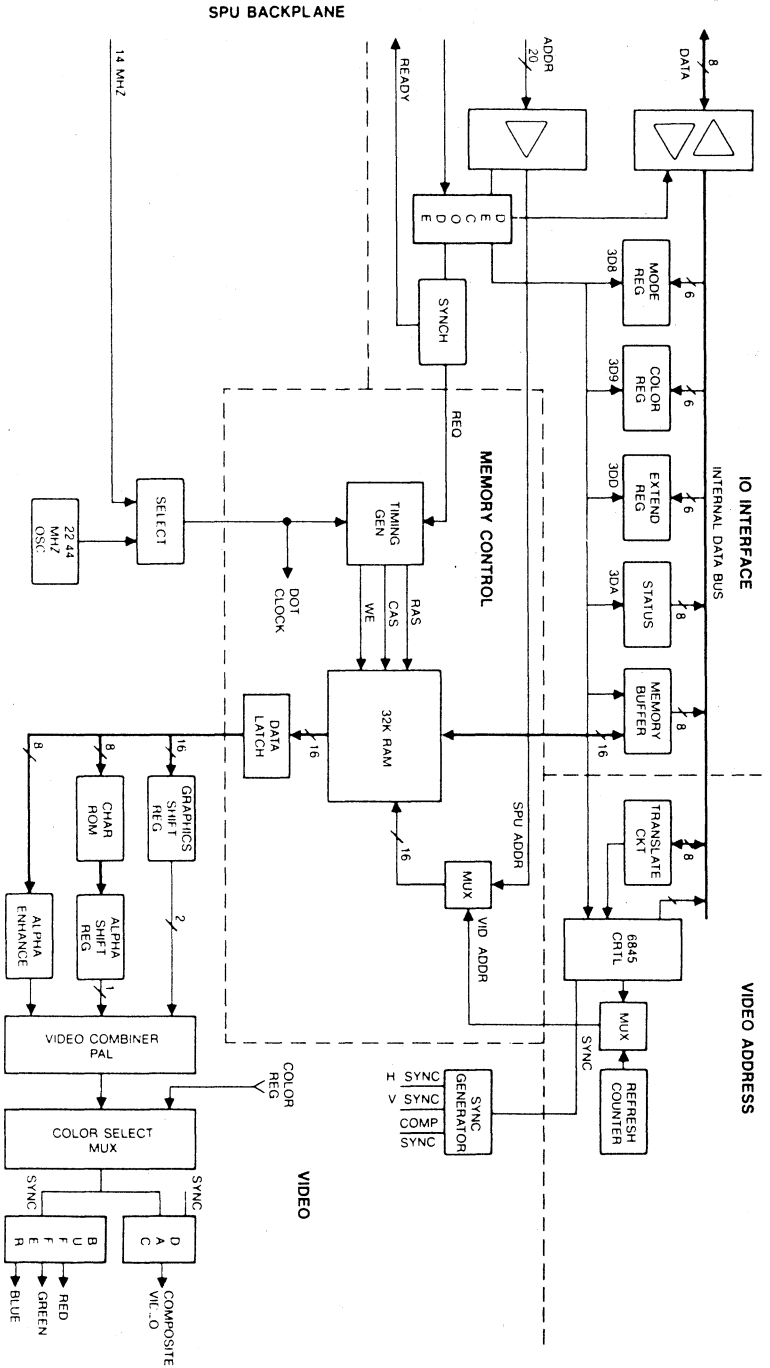


Figure 18

Clock Cycle

The HP45981A operates from the master oscillator at 22.440MHz and the backplane clock at 14.3818MHz.

Adapter-to-System Hardware Interface

The HP45981A is interfaced to the 80286 microprocessor as an 8-bit memory device and and 8-bit I/O device. All signal lines are buffered onto the card and load to the system bus. Wait-states are provided for memory accesses to synchronize the 80286. The RAM on the card is on four 16 Kbyte x 4 RAM chips.

Jumpers and Connectors

The following card layout shows the connectors and jumpers on the HP45981A.

Multi-Mode Video Adapter Card Layout

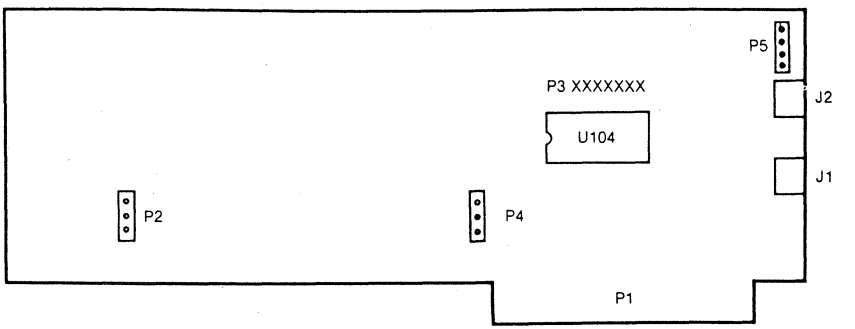


Figure 19

Jumper W2 must be installed on pins 1 and 2 of P4 for operation with a 15 kHz monitor. Jumper W2 must be installed on pins 2 and 3 of P4 for operation with a 25 kHz monitor. The following figure shows the configurations for this jumper.

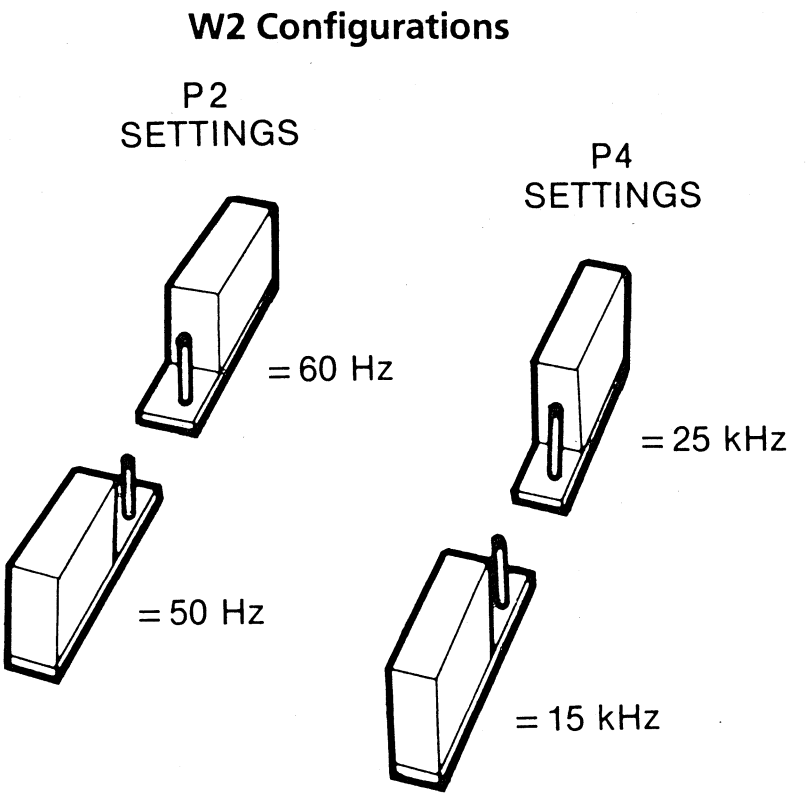


Figure 20

Table 7.1 defines the pin assignments for the hardware interface. The signal definitions for these pins are defined in Section 2. Tables 7.2 through 7.4 defines the pin assignments and signal definitions for peripheral devices.

Table 7.1

HP45981A-to-System Pin Assignments

P1 Component Side			P1 CKT Side		
Pin	I/O	Signal Name	Pin	I/O	Signal Name
1		n.c.	1	I	GND
2	I/O	SD7	2	I	RESET DRV
3	I/O	SD6	3	I	+ 5Vdc
4	I/O	SD5	4		n.c.
5	I/O	SD4	5		n.c.
6	I/O	SD3	6		n.c.
7	I/O	SD2	7		n.c.
8	I/O	SD1	8		n.c.
9	I/O	SD0	9	I	+ 12Vdc
10	O	~IO CH RDY	10	I	GND
11	I	AEN	11	I	~SMEMW
12	I	SA19	12	I	~SMEMR
13	I	SA18	13	I	~IOW
14	I	SA17	14	I	~IOR
15	I	SA16	15		n.c.
16	I	SA15	16		n.c.
17	I	SA14	17		n.c.
18	I	SA13	18		n.c.
19	I	SA12	19		n.c.
20	I	SA11	20	I	SYSCLK
21	I	SA10	21		n.c.
22	I	SA9	22		n.c.
23	I	SA8	23		n.c.
24	I	SA7	24		n.c.
25	I	SA6	25		n.c.
26	I	SA5	26		n.c.
27	I	SA4	27		n.c.
28	I	SA3	28		n.c.
29	I	SA2	29	I	+ 5Vdc
30	I	SA1	30	I	OSC
31	I	SA0	31	I	GND

Table 7.2

Light Pen Connector (P5) Pin Assignments

Pin	Signal	I/O	Signal Description
P2-1	~LPHIT	I	Light Pen Hit (TTL level)
P2-2	n.c.		Missing pin (key)
P2-3	~LPSWITCH	I	Light Pen Switch (TTL level)
P2-4	GND		Ground
P2-5	+5 Vdc	O	+5 Volts DC power
P2-6	+12Vdc	O	+12 Volts DC power

Table 7.3

Direct Connect (RGB) Monitor Connector (J1) Pin Assignments

Pin	Signal	I/O	Signal Description
J1-1	GND		Ground
J1-2	GND		Ground
J1-3	RED	O	Red Drive (TTL level)
J1-4	GREEN	O	Green Drive (TTL level)
J1-5	BLUE	O	Blue Drive (TTL level)
J1-6	INTENSIFY	O	Intensify (TTL level)
J1-7	n.c.		
J1-8	HSYNC	O	Horizontal Synchronization (TTL level)
J1-9	VSYNC	O	Vertical Synchronization (TTL level)

Table 7.4

Composite Video Connector (J2) Pin Assignments

Pin	Signal	I/O	Signal Description
J2-1	GND		Ground
J2-2	VIDEO	O	Composite Video

Table 7.5

Color Adapter Connector (P3) Pin Assignments

Pin	Signal	I/O	Signal Description
1	GND		Ground
2	INTENSITY	O	Intensity dot stream
3	RED	O	Red dot stream
4	GND		Ground
5	GREEN	O	Green dot stream
6	BLUE	O	Blue dot stream
7	GND		Ground
8	COMPSYNC	O	Composite sync
9	HSYNC	O	Horizontal sync
10	GND		Ground
11	VSYNC	O	Vertical sync
12	MCLK	O	Dot rate clock
13	GND		Ground
14	-PRESENT	I	Board present

Character Generator ROM

The character generator ROM for the HP45981A is an 128 Kbyte bit ROM (16 Kbyte x 8) containing four character sets. Each set consists of 256 patterns. Depending on the monitor in use either an 8 or 16 high cell is selected. The font bit (bit 2) of the extension control register and the monitor determines the character set that is selected. A 15kHz monitor selects the eight row version, while a 25kHz monitor selects the 16 row version.

Each character set is stored in contiguous 4 Kbytes in the ROM defined by the following chart. (The character sets are given in Section 5.)

Set	Font	Size	Location
0	STD	8x8	0000-0FFF
1	STD	16x8	1000-1FFF
2	HP	8x8	2000-2FFF
3	HP	14x8	3000-3FFF

Within each set the top row of each character is the first 256 bytes, the second row in the next 256, etc. Within each byte the high order bit 7 is displayed on the left side of the character. A 1 is stored for a lit dot, a 0 for an unlit dot.

The complete address definiton of the ROM is:

A13	A12	A11,10,9,8	A7,6,5,4,3,2,1,0
Font 0 = STD 1 = HP	Height 0 = 8x8 1 = 14x8	Row # Row 0 is the top of the cell.	Character Code

RAM Access

The HP45981A contains 32K of RAM based in a contiguous segment B8000-BFFFF. The memory on the video card is run asynchronously to the 80286. Therefore, any access to the video memory will include at least four wait-states, and as many as six wait-states to complete an instruction. Refresh is generated internally. Data is taken from memory depending on the mode of operation. The two modes of operation are: alpha mode and graphics mode.

Memory address wrapping and page selection is controlled by four bits in the extension control register. The 16/32K select (bit 4) and the page select (bit 5) determine the way the SPU has access to memory. The vertical resolution (bit 0) and the font select (bit 2) determine the way the display accesses the memory. The access to memory differs in the alpha and graphics modes. The various access methods are summarized in the following table:

Table 7.6

SPU Access and Display Access

SPU Access		Data	Description
Alpha	16/32K Select	0	First 16K of memory available. Wraps into the entire 32K address space.
	Page Select		Not used.
	16/32K Select	1	One 16K page of memory available.Wraps into entire 32K address space.
	Page Select		Not used.
Graphics	16/32K Select	0	First 16K of memory available. Wraps into the entire 32K address space.
	Page Select	0/1	Selects which page is active.
	16/32K Select	1	Entire 32K of memory available.
	Page Select		Not used.
Display Access			
Alpha	Vertical Resolution	0	Display first 16K of memory.Wraps into the entire 32K address space.
	Font Select	0/1	Selects character set displayed.
	Vertical Resolution	1	Display from entire 32K of memory. 400 line display.
	Font Select		Not used.
Graphics	Vertical Resolution	0	Display from one 16K page of memory. Wraps into enire 32K address space.
	Font	0/1	Selects which page is displayed.
	Vertical Resolution	1	Display from entire 32K of memory. 400 line display.
	Font Select		Not used.

Modes of Operation

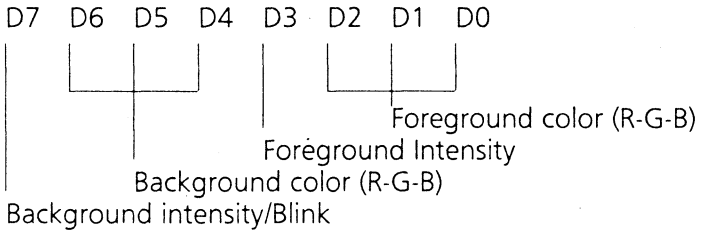
The mode control register determines the mode of operation. The following is a list of availabe RAM access modes.

* Alphanumeric Mode
  80 x 25
  40 x 25
* Graphics Mode
  640 x 1
  320 x 2

Alphanumeric Mode

When the HP45981A is set in the alphanumeric mode, words (attribute byte + character byte) are fetched from the memory starting at the offset programmed into the 6845 CRT controller. This address is a word pointer and will always be used to fetch from even byte boundaries. Words are fetched contiguously from memory. For an 80 x 25 display, 2000 words (8 pages) are fetched. For a 40 x 25 display, 1000 words (16 pages) are fetched.

The character code is a byte with the ASCII code for the character. The attribute byte is defined as:



If underline enable is set, an underline will be generated for any character with a foreground color of 001, and the color of the character will be forced to 111. If underline enable is not set the character will be displayed as blue or a gray level.

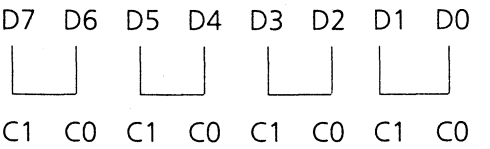
Graphics Mode

In the 200 line graphic modes the memory is mapped with even and odd lines of data in separate banks. Even lines start at offset 0000H and odd lines at offset 2000H. Sufficient memory exists for two pages of graphics to be stored. The second page stores the even lines at offset 4000H and the odd lines at offset 6000H. In this mode 25kHz monitors are supported by displaying each of the 200 lines twice.

In the 400 line graphics mode the memory is mapped into four banks. Lines 0,4,8, . . . are in the first bank at offset 0000H. Lines 1,5.9, . . . are in the second bank at offset 2000H. The third bank at offset 4000H contains lines 2,6,10, . . . while the fourth bank at offset 6000H contain lines 3,7,11,etc..

Data Format for Graphic Mode

In the data format mode the 320 x 2 mode maps two bits to each pixel. Each byte is displayed with the most significant bits to the left. As shown in the following chart:



C1 and C0 select the color as defined by the color register.

640 x 1

The data for the 640 x 1 mode is mapped one bit per pixel with the most significant bit displayed to the left.

6845 CRT Controller

The 6845 CRT controller (CRTC) contains 19 internal registers. One of these is the index register. It is accessed at any even I/O address in the range 3D0-3D6. This write-only register functions as a pointer to the other 18 registers in the chip. Reading it will return an undefined value. The 18 internal data registers are accessible at any odd I/O address in the range 3D1-3D7, after first setting the index to point to it. Table 6.7 defines the initial values that should be sent to the CRTC chip.

Table 7.7

Initial Chip Values

Mode			6845 Data register													
25kHZ	**Hz**	**Note**	**R0**	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**	**R9**	**R10**	**R11**	**3D8**	**3DD**
80x25 A	60	**	6D	50	57	0A	19	09	19	19	00	0F	0E	0F	0D	00
40x25 A	60	**	36	28	2C	0A	19	09	19	19	00	0F	0E	0F	0C	00
80x27 A	60		6D	50	57	0A	1D	05	1B	1C	00	0D	0D	0E	0D	00
40x27 A	60		36	28	2C	0A	1D	05	1B	1C	00	0D	0D	0E	0C	00
320x2x200	60	**	36	28	2B	0A	69	01	64	66	00	03	0E	0F	0E	00
640x1x200	60	**	36	28	2B	0A	69	01	64	66	00	03	0E	0F	1E	00
320x2x400	60		36	28	2B	0A	69	01	64	66	00	03	0E	0F	0E	11
640x1x400	60		36	28	2B	0A	69	01	64	66	00	03	0E	0F	1E	11
80x25 A	50	**	6D	50	57	0A	1E	0E	19	1C	00	0F	0E	0F	0D	00
40x25 A	50	**	36	28	2C	0A	1E	0E	19	1C	00	0F	0E	0F	0C	00
80x27 A	50	+ +	6D	50	57	0A	23	06	1B	1F	00	0D	0C	0D	0D	00
40x27 A	50	+ +	36	28	2C	0A	23	06	1B	1F	00	0D	0C	0D	0C	00
320x2x200	50	**	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	0E	00
640x1x200	50	**	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	1E	00
320x2x400	50	+ +	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	0E	11
640x1x400	50	+ +	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	1E	11
15kHZ																
80x25 A	60		71	50	5A	0A	1F	06	19	1C	02	07	06	07	0D	00
40x25 A	60		38	28	2D	0A	1F	06	19	1C	02	07	06	07	0C	00
320x2x200	60		38	28	2D	0A	7F	06	64	70	02	01	06	07	0E	00
640x1x200	60		38	28	2D	0A	7F	06	64	70	02	01	06	07	1E	00
80x25 A	50		71	50	5A	0A	26	02	19	1F	02	07	06	07	0D	00
40x25 A	50		38	28	2D	0A	26	02	19	1F	02	07	06	07	0C	00
320x2x200	55	*	38	28	2D	0A	7F	1F	64	75	02	01	06	07	0E	00
640x1x200	55	*	38	28	2D	0A	7F	1F	64	75	02	01	06	07	1E	00

*Due to limitations of the 6845 registers, 50Hz graphics is not possible.

**These modes should be programmed with 15KHz 60Hz values. They will be translated according to the W1/W2 jumper settings on the board.

+ +These modes shoud be programmed with 25KHz 60Hz values. They will be translated according to the W1 jumper setting on the board.

Translation

Data written to the CRTC passes through a translation circuit to allow applications written for a 15kHz monitor to operate without modification when a 25kHz monitor is connected. In this way the actual monitor connected is transparent to the program. The low four bits of any data written to the address index register is also latched external to the CRTC in a phase alternation line (PAL). When a subsequent write is performed to the data register of the CRTC, the latched data and the actual data written are combined and used as an address into the translation ROM. It is the data contained in the ROM that is written into the CRTC.

The translation will occur for any register needing it if the data written to the register is in the range 00H to 7FH. If an application needs to set a register to a specific value without translation, bit 7 must be set to 1. Data in the range 80 to FF will then be written to the chip as 00H to 7FH. The translation occurs only on the data written to the CRTC and only when a 25kHz monitor is connected. Data is read back directly from the chip. Translation will also occur for any monitor if the 50Hz jumper is installed. Again, values greater than 80H will be passed with bit 7 set to 0.

Programming Accessible Registers

The application must read the status register bit 4 to determine which monitor is connected. No harm will be done setting the 400 line mode bit with a 200 line monitor connected, but the display will not be as expected.

At power-on or reset all bits are cleared in I/O registers except the light pen latch. The following table lists the I/O registers.

Table 7.8

I/O Registers

Register I/O Address	Read	Write
3D0	CRTC undefined	CRTC Register Index
3D1	CRTC Data Register	CRTC Data Register
3D2	CRTC undefined	Duplicate CRTC Register Index
3D3	CRTC Data Register	Duplicate CRTC Data Register
3D4	CRTC undefined	Duplicate CRTC Register Index
3D5	CRTC Data Register	Duplicate CRTC Data Register
3D6	CRTC undefined	Duplicate CRTC Register Index
3D7	CRTC Data Register	Duplicate CRTC Data Register
3D8	Undefined*	Mode Control Register
3D9	Undefined*	Color Select Register
3DA	Status Register	Not allowed***
3DB	Clear LP Flag**	Clear LP Flag**
3DC	Set LP Flag**	Set LP Flag**
3DD	Undefined*	Extended Control Register
3DE	Undefined*	Unused
3DF	Board ID*	Unused

*Reading an undefined register will cause its contents to become undefined.

**Reading or writing will cause function. No data is written and value returned via read is meaningless.

***Do not write to this register.

Mode Control Register

The mode control register is a 6-bit write-only register.

Bit	Data	Definition
0	0	40 character alpha, 320x2 graphics, 640x1 graphics
	1	80 character alpha, 640x2 graphics
1	0	Alpha mode
	1	Graphics mode
2*	0	Color mode
	1	Black and white mode
3	0	Disable video
	1	Enable video
4	0	Select 320 pixel graphics
	1	Select 640 pixel graphics
5	0	Attribute bit 7 is background intensity
	1	Attribute bit 7 is blink

*Bit 2 provides a secondary function tying the blue and green guns together changing the displayed colors.

Color Register

The color register is a 6-bit write only register, that applies to the alphanumeric mode.

Bit	Data	Definition
0	0	Off, blue
	1	On, blue
1	0	Off, green
	1	On, green
2	0	Off, red
	1	On, red
3	0	Off, intensify
	1	On, intensify
4		Alternate set select
5		Pallet select

The use of bits 0, 1, 2, and 3 depends on the mode of operation selected. Defined as follows:

Alphanumeric: selects the screen border color.*
320x2 graphics: selects the screen background color.
640x1 graphics: selects the foreground color, background black.

Bit 4 when set to 1 intensifies the 320 x 2 colors to their alternates.

*Not implemented for 25kHz monitor.

Bit 5 determines the pallet of colors used in the 320 x 2 mode, as defined as:

Pixel		Bit 5 = 0		Bit 5 = 1	
C1	C0	Normal	Alternate	Normal	Alternate
0	0	Background determined by bits 0-3.			
0	1	Green	Lt. Green	Cyan	Lt. Cyan
1	0	Red	Lt. Red	Magenta	Lt. Magenta
1	1	Brown	Yellow	White	Bright White

Status Register

The status register is an 8-bit read-only register.

Bit	Data	Definition
0	0	Display Enable, Active Area
	1	Retrace
1	0	Light pen hit, register reset
	1	Register set
2	0	Light Pen Switch, open
	1	Closed
3	0	Vertical Sync,
	1	within vertical sync time
4	0	Monitor type, 25kHz
	1	Monitor type, 15kHz
5	0	Color adapter connected
	1	Color adapter not connected
6		Diagnostic purposes
7		Diagnostic purposes

Light Pen

Any access to I/O address 3DB, read or write, will clear the light pen latch. No data is transferred, if a read is performed the data returned is meaningless.

Any access to I/O address 3DC, read or write, will set the light pen latch. No data is transferred, if a read is performed, the data returned is meaningless.

Extension Control Register

The extension control register is a 6-bit write-only register.

The programmer has control over the font style, but not the height. The type of monitor determines the cell size of the alphanumeric character font.

Bit	Data	Definition
0	0	Vertical Resolution, emulate 200 line display
	1	Enable 400 line display
1	0	Underline Enable, normal
	1	Enable underline if bits 2-0 are 001.
2	0	Font Select, STD on Display Graphics page 1
	1	HP, Roman 8 font on Display Graphics page 2
3	0	Memory Disable, normal
	1	Disable memory from responding to R/W access.
4	0	16/32K select, wrap first 16K into 32K
	1	Use all 32K
5	0	Page, use first 16K
	1	Use second 16K (graphics)

The underline enable bit must be set for underlines to be displayed. If it is not set an underlined character will be displayed as blue or a shade of gray.

Board ID Register

The board ID register is a read-only register. It will return the value 41H when read.

SECTION 8. NUMERIC COPROCESSOR

HP45977A is the Intel 80287 numeric coprocessor chip that enables HP Vectra PC to perform high-speed mathematical functions with seven numeric data types. This section will provide an overview to the 80287. For detailed information on this chip refer to the bibliography for source material.

The coprocessor works in parallel with the 80286 microprocessor. The parallel operation increases execution speed by allowing the coprocessor to do mathematical calculations while the microprocessor continues to do other routines. Similar to the 80286, the 80287 has two operating modes.

Real-Address Operating Mode

The system is in real-address mode at power-up. An I/O write to port 0F1H with D7 through D0 equal to 0 will reset the 80287, and also place it in real-address mode. Real-address mode of the 80287 is compatible with the 8087 numeric coprocessor used in many industry standard personal computers.

Protected Mode

Setting the 80286 microprocessor into protected mode does not automaticaly set the coprocessor into protected mode. The coprocessor can be placed in the protected mode by executing the appropriate software instruction. Refer to *HP Vectra Technical Reference Manual Volume 2: System BIOS* for 80287 programming information. Placing the 80287 into protected mode provides memory management, protection mechanisms, and associated instructions. Protected mode allows HP Vectra PC to use other operating systems and to use multi-user applications.

Hardware Interface

The 80287 operates on the same 16MHz clock as the 80286. It internally divides this clock by three.

The 80286 sends OP codes and operands to the 80287 through the bidirectional I/O port addresses 0F8H, 0FAH, 0FCH. It also receives results through these same ports.

The coprocessor asserts the BUSY signal when processing an arithmetic, logarithmic, or trigonometric calculation. The WAIT instruction forces the 80286 to wait until the coprocessor is finished executing the calculation before it can retrieve the data. (Many numeric instructions have an implicit WAIT.)

There are six different error conditions that the 80287 can detect. If the corrsponding exception mask is not set, the 80287 will set its ERROR signal. In turn, this will generate a hardware interrupt (INT 13), and will latch the BUSY signal. The offending calculation remains in the 80287, so the 80286 can read the status and handle the error. The latched BUSY can be cleared by an I/O write to port 0F0H with D0 through D7 equal to 0. The 80287 can also be set to handle errors internally (using predefined results).

At power-up the BIOS detects the 80287 and enables hardware interrupt 13. The interrupt handler clears the latched BUSY signal, and transfers control to the NMI handler. The NMI handler should read the status of the coprocessor to determine if the NMI was caused by the 80287. If it was not, control should be passed to the original NMI interrupt handler.

Capability Extensions

By programming with the instruction set of the 80287 coprocessor the data types, registers, and instructions to the microprocessor are extended. The data types are expanded because the 80287 deals with these directly rather than employing a program sub-routine. The register space of the coprocessor is equivalent to the register space of the microprocessor, but it is organized as eight 80-bit registers. This register space allows constants and temporary results to be held in registers during calculations, thus reducing memory accesses and improving speed as well as system bus availability. The register space can be used as a stack or as a fixed register set. When used as a stack, operations are only on the top two stack elements.

SECTION 9. DISC DRIVES

The HP Vectra has two different internal hard disc drives as accessories: the HP45817A 40MB 5 1/4 inch disc drive and the HP45816A 20MB disc drive.

The HP Vectra PC is equipped with one internal flexible disc drive and has the capabilities to support another flexible disc drive. The flexible disc drives that are accessories to the HP Vectra PC are: the HP45811A 360KB Internal Flexible Disc Drive and the HP45812A 1.2MB Internal Flexible Disc Drive. The flexible disc controller subsystem is a component of the processor board.

The following illustration shows the drive installation possibilities for the HP Vectra PC drive cage.

HP Vectra Drive Cage

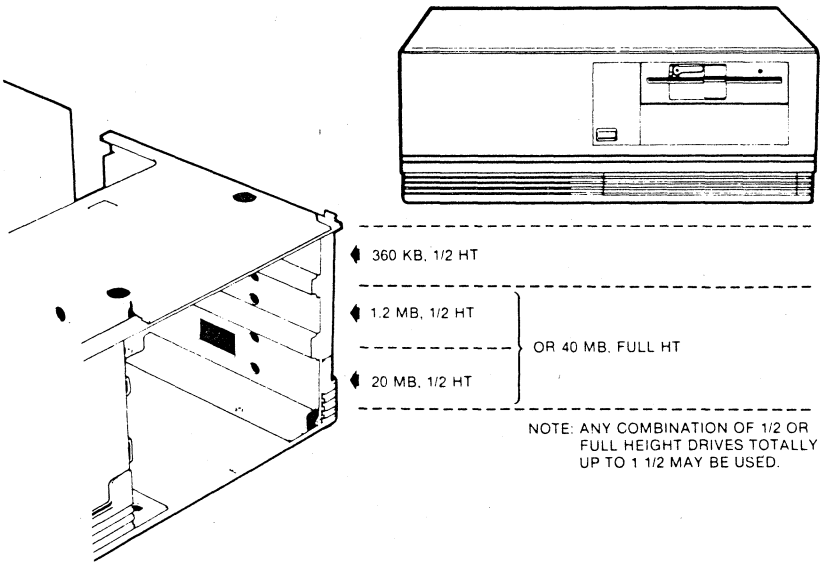


Figure 21

HP45811A 360KB Internal Flexible Disc Drive

The 360KB Internal Flexible Disc Drive can be purchased as an accessory to the HP Vectra (product number HP45811A). It is used to store formatted data on double-sided 5/14 inch flexible discs. It is easily identified by the asterisk molded into the faceplate just below the activity light. The flexible disc controller subsystem can support up to two flexible disc drives, either or both may be the 360KB internal flexible disc drive.

The drive can read and write on Double-Sided Mini-Discs (HP92190A or equivalent). Also, it can read and write to single-sided discs, however, excessive head wear results when single-sided discs are used. It is recommended that data from single-sided discs be copied to double-sided discs, then only the double-sided discs be used with the 360KB Internal Flexible Disc Drive.

The 360KB Internal Flexible Disc Drive chassis is 171mm wide x 41mm high x 207mm deep. It weighs 1.6kg and fits in either of the half-height disc drive cages. It draws a maximum of 19.8 watts from the power supply. Table 9.1 describes the performance of the 360KB Internal Flexible Disc Drive when properly installed in the HP Vectra PC.

Table 9.1

360KB Internal Flexible Disc Drive Drive Performance

Formatted Capacity(MFM)	360Kb
Media type	HP92190A or equivalent
Track density	48 tpi
Tracks/surface	40
Sectors/track	8 and 9 valid
Bytes/sector	512
Track-to-track seek time	6 msec
Average access time	93 msec
Motor start time	500 msec
Rotation speed	300 rpm
Data transfer rate	250kHz

Hardware Interface

The 360KB Internal Flexible Disc Drive interfaces with the flexible disc controller (FDC) in two areas: the control interface and the DC power interface. The signals for operating the disc drive are generated through the flexible disc controller (FDC) section on the processor board. The 34-pin connector pin assignments and signal descriptions are given in Section 2. The following table defines the pins used in the DC power interface.

Table 9.2

DC Power Interface Pin Assignments

Pin	Signal Name
1	+ 12 Vdc
2	+ 12 Vdc return
3	+ 5 Vdc return
4	+ 5 Vdc

HP45812A 1.2Mb Internal Flexible Disc Drive

The 1.2MB Internal Flexible Disc Drive can be purchased as an accessory (HP product number 45812A). The flexible disc controller subsystem can support up to two of these dual-mode internal flexible disc drives.

The 1.2MB drive differs from the 360KB disc drive in three major ways: 1) the media on the 1.2MB drive rotates at 360 rpm, 2) the read/write gap is half the width of the 360KB disc drive, 3) it has two distinct read/write channels.

One of the read/write channels is optimized to transfer data to and from the media at 500kHz, the other channel is optimized to transfer data to and from the media at 300kHz. The 500kHz channel is designed to be used with HP92190X High-Capacity 96 tpi Discs. HP92190X is a high coercivity (approximately 650 Oersteds) media. When this drive is used with HP92190X media, 1.2MB of formatted data can be stored and read.

The 300kHz channel is designed to be used with HP92190A Double-Sided Double-Density Discs. Because the bit storage density of the HP92190A disc is not as high as HP92190X discs, when this media is used in the 1.2MB drive, the flexible disc controller enables the 300kHz channel and issues double STEP pulses to the drive. (Refer to Section 2 for detailed information on the flexible disc controller subsystem.) As a result, the 1.2MB Internal Flexible Disc Drive can format and write a Double-Sided Double-Density Disc in a similar way as the 360KB Internal Flexible Disc Drive. However, since the read/write gap is half as wide as the gap in the 360KB Internal Flexible Disc Drive head, the 360KB Internal Flexible Disc Drive and other similar drives cannot read the signal on these smaller tracks.

Media

Note the following when using the 1.2MB Internal Flexible Disc Drive:

- Use of HP92190X High-Capacity Discs will result in maximum storage capacity.
- HP92190X High-Capacity Discs are designed to be used only with the 1.2MB Internal Flexible Disc Drive. They will not work in the 360KB Internal Flexible Disc Drive.*
- The 1.2MB Internal Flexible Disc Drive can read and write data with HP92190A Double-Sided Discs. After being used in the 1.2 drive, the discs will not be able to be read or written on the 360KB Internal Flexible Disc Drive because of the narrower track.**

*Caution

The HP92190X High-Capacity Disc are designed to be used with the 1.2MB Internal Flexible Disc Drive. They will not operate in the 360KB Internal Flexible Disc Drive. Always format or write high-capacity disc with the 1.2MB Internal Flexible Disc Drive.

**Caution

A HP92190A Double-Sided Disc that has been formatted and written on by a 360KB Internal Flexible Disc Drive and then updated with the 1.2MB Internal Flexible Disc Drive will only be able to be read and witten on by a 1.2MB Internal Flexible Disc Drive after the update. Label the discs that have been updated by the 1.2 drive, so that they will only be used in the 1.2MB Internal Flexible Disc Drive.

Drive Performance

During a read command, the disc drive mode is automatically selected by the flexible disc controller after a formatted disc is inserted.

The chassis of the 1.2MB Internal Flexible Disc Drive is 171mm wide x 41mm high x 207mm deep. It fits into either of the two half-height disc drive cages. It draws a maximum of 19.8 watts from the power supply. Table 9.3 describes the performance of the 1.2MB Internal Flexible Disc Drive when it is properly installed in the HP Vectra.

Table 9.3

1.2MB Internal Flexible Disc Drive

Drive Performance

	360KB Mode	1.2MB Mode
Formatted Capacity	360KB	1.2MB
Recommended Media	HP 92190A	HP 92190X
Track density	48 tpi	96 tpi
Tracks/surface	40	80
Sectors/track	8 or 9	15
Bytes/sector	512	512
Track-to-track seek time	6 msec	3 msec
Average access time	93 msec	93 msec
Data transfer rate	300kHz	500kHz
Motor Start time	500 ms	500 ms
Rotation speed	360 rpm	360 rpm

Hardware Interface

The 1.2MB Internal Flexible Disc Drive interfaces with the system in two areas; the control interface and the DC power interface. The signals for operating the disc drive are generated through the FDC section of the processor board. The 34-pin connector pin assignments and signal descriptions for the control interface is given in Section 2. The following table defines the pin assignments for the DC power interface.

Table 9.4

DC Power Interface Pin Assignments

Pin	Signal Name	Current Requirements
1	+ 12 Vdc	1.2 A (maximum)
2	+ 12 Vdc return	
3	+ 5 Vdc return	
4	+ 5 Vdc	0.9 A (maximum)

Hard Disc Subsystem

The HP45816A and HP45817A hard disc subsystem cards insert into slot seven of the backplane I/O slots. The disc controller is an intelligent subsystem using the 6809 processor to offload disc operations from the system processor. Its implementation uses the backplane I/O signals defined in Section 2 of this manual.

Hardware Interface

Interface to the system is through two registers: the control/status register, and the data register. Each port is connected to the 8-bit interface data bus. Each port is selected by a decoded address defined by the system.

The hard disc subsystem card occupies two address locations in the system I/O memory space. The selected lines for these registers are generated by the system address and IOR or IOW lines. One location addresses the write-only control register and the read-only status register, and the other location addresses the bidirectional FIFO data register.

The controller-to-system hardware interface is performed by programmable I/O. It interfaces with the system at software interrupt 13 BIOS level. Refer to the *HP Vectra Technical Reference Manual Volume 2: System BIOS* for detailed BIOS listings. The interface does not bottleneck the data transfer rate. The rate is determined by the speed of the system and the data rate of the disc drive.

Registers

The status register is accessed by system reads. It provides information to the system about the status of the hard disc controller card. Two of the bits indicate the protocol phase of the controller. The other bits of this register flag various conditions such as: the status of the last command, when a block of data is ready to be transferred, and when a command has been completed. This status register can be polled for programmed I/O applications.

The control register is a latch to which the system writes to inform the controller when to enter different phases of operation.

The data port is bidirectional and passes not only data, but command and status information also. To the system this data port appears to be a FIFO. The FIFO arrangement allows the system to read or write the data without handshaking each byte. The data register should be read or written to only during the appropriate command phases.

Memory

HP Vectra PC requires a system ROM and RAM on the hard disc subsystem card for the disc BIOS. These reside in 8 Kbytes of system memory space. The ROM occupies the first 6 Kbytes and the RAM the last 2 Kbytes.

The address of this 8 Kbytes block can be selected by the four switches on the subsystem card in the C0000 to DF000 hex range. The following figure shows the location of the switches on both the hard disc subsystem cards.

The jumpers are configured for the 20 Mbyte hard disc subsystem.

SW1, SW2, SW3, and SW4 Switch Locations

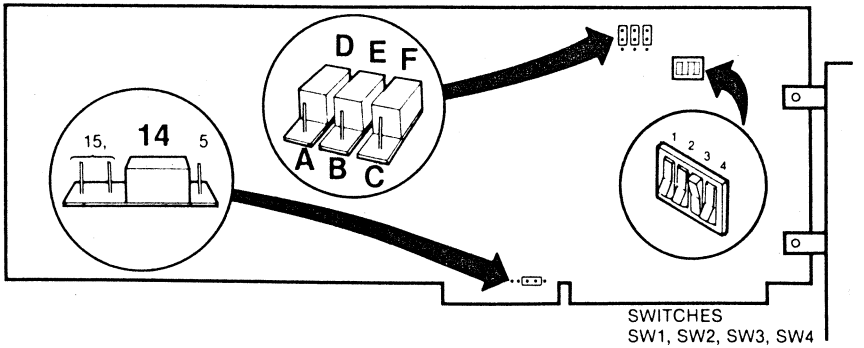


Figure 22

Switch settings for SW1, SW2, SW3, and SW4 which set the addresses are given in the following table.

Table 9.5

BIOS and I/O Address Switch Settings

Switch SW1	SW2	SW3	SW4	BIOS Address	I/O Address
0	0	0	0	C0000-C1FFF*	1F0
1	0	0	0	C2000-C3FFF*	320
0	1	0	0	C4000-C5FFF*	1F0
1	1	0	0	C6000-C7FFF*	320
0	0	1	0	C8000-C9FFF +	1F0
1	0	1	0	CA000-CBFFF	320
0	1	1	0	CC000-CDFFF	1F0
1	1	1	0	CE000-CFFFF	320
0	0	0	1	D0000-D1FFF	1F0
1	0	0	1	D2000-D3FFF	320
0	1	0	1	D4000-D5FFF	1F0
1	1	0	1	D6000-D7FFF	320
0	0	1	1	D8000-D9FFF	1F0
1	0	1	1	DA000-DBFFF	320
0	1	1	1	DC000-DDFFF	1F0
1	1	1	1	DE000-DFFFF	320

* These are illegal address settings.

\+ Factory default setting.

HP45816A 20MB Hard Disc Subsystem

The HP45816A 20MB hard disc drive chassis is 41.1mm high, 146.05mm wide, and 202.2mm deep. It fits in either of the half-height drive slots, however, the cabling is best managed when the hard disc drive is installed in the lower slot. The following table describes the performance of the HP45816A when installed in the HP Vectra PC.

Table 9.6

HP45816A Drive Performance

Formatted Capacity/Drive	21.09 Mbyte
Formatted Capacity/Surface	5 Mbyte
Formatted Capacity/Track	8,704 bytes
Formatted Capacity/Sector	512 bytes
Sector/Track	17
Data Transfer Rate	5.0 Mbit/sec
Track-to-Track Seek Time	20 msec
Average Access Time	85 msec
Maximum Seek	205 msec
Latency	8.33 msec
Rotational Speed	3,600 RPM +/– 1%
Recording Density	9,784 BPI
Flux Density	9,784 FCI
Track Density	588 tpi
Cylinders	606
Read/Write Heads	4
Discs	2
Recording scheme	MFM
Dissipation	15 watts typical

Drive-to-Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector is J3 and it is a 4-pin AMP "Mate-n-Lock" connector.

HP45817A 40MB Hard Disc Subsystem

The HP45817A 40MB hard disc subsystem is availible for fast access and high-capacity. The drive automatically retracts the read and write heads to a parking zone when powered off. This protects the disc against damage during handling or moving.

The chassis of the HP45817A is 82.55mm high, 146.05mm wide, and 203.2mm deep. It requires both of the lower half height drive slots. The following table defines the performance of the HP45817A when installed in the HP Vectra PC.

Table 9.7

HP45817A Drive Performance

Formatted capacity/drive	42.25 Mbyte (accessed as 2 20 Mbyte units)
Formatted capacity/sector	512 bytes
Sector/Track	17
Data Transfer Rate	5.0 Mbit/sec
Track-to-Track Seek Time	10msec
Average Access Time	40msec
Maximum Seek	80msec
Latency	8.33msec
Rotational Speed	3,600 RPM +/− 1%
Recording Density	9,848 BPI
Flux Density	9,848 FCI
Track Density	960 tpi
Cylinders	971
Read/Write Heads	5
Servo Heads	1
Discs	3
Recording Scheme	MFM
Heat Dissipation	24 watts typical

Drive-to-Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector is J3 and is a 4-pin AMP "Mate-n-Lock" connector.

SECTION 10. MEMORY EXPANSION CARDS

For memory capabilities beyond 640 Kbyte, HP provides two memory expansion cards: the HP45973A 1/2 MB Memory Expansion Card which contains 512 Kbytes of RAM, and the HP45974A 1 MB Memory Expansion Card which supports 1024 Kbytes of RAM.

The memory expansion cards use 256K x 1 dynamic memory chips. The HP45973A 1/2 MB Memory Expansion Card contains 18 of these RAM chips (including parity). The HP45974A 1 MB Memory Expansion Card contains 36 of these chips.

The memory expansion cards, must be inserted into two connector 16-bit I/O slots. Table 2.4 and table 2.5 give the pin assignments for these connectors, and signal descriptions can be found in Section 2.

Parity and Refresh

Memory data is parity-checked when accessed. If a parity error occurs, then a non-maskable interrupt (NMI) will be generated. The NMI can be cleared by writing to the memory expansion card where the parity error occurred.

Refresh of dynamic memory is controlled on the main system card. All memories using the ~REFRESH line are refreshed at the same time.

Clock Cycles

The memory expansion card operates from the 80286 microprocessor clock at a frequency of 8MHz. It takes three clock cyles (one wait-state) for memory access.

Switches

The address selection switches can be set so the memory expansion card can cover the entire 16 megabytes of system memory space in 512 Kbyte or 1024 Kbyte blocks. However, the processor board RAM is hardwired to the first megabyte of memory space. Therefore, address selection switches, SW1 and SW2, must be set to cover different blocks of the remaining 15 Mbyte memory address space. No two cards should be set to respond to the same address space.

The memory expansion cards must be configured to reside in sequential memory address within the system address space 100000 to FDFFFF hex. The first expansion memory address starts at 100000 hex. Configuration is done by setting the switches, SW1 and SW2. If more than one card is used, no gaps between memory are allowed. Switch settings for the HP45974A 1 MB Memory Expansion Card are given in figure 24, and switch settings for the HP45973A 1/2 MB Memory Expansion Card are given in figure 25.

This drawing shows the location of the switches on the memory expansion cards, HP45973A or HP45974A.

SW1 and SW2 Switch Locations

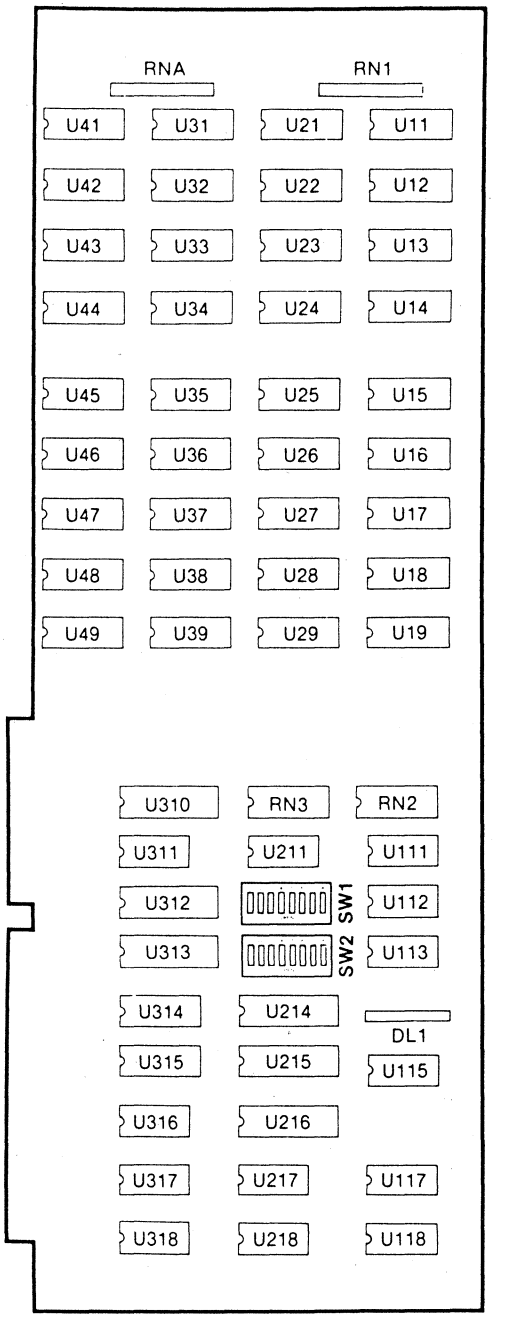


Figure 23

1 MB Memory Expansion Card

Address Switch Settings

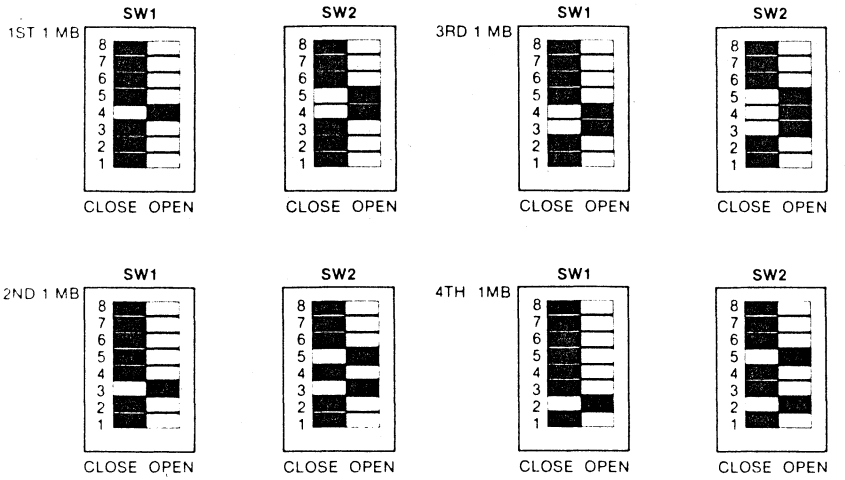


Figure 24

1/2 MB Memory Expansion Card

Address Switch Settings

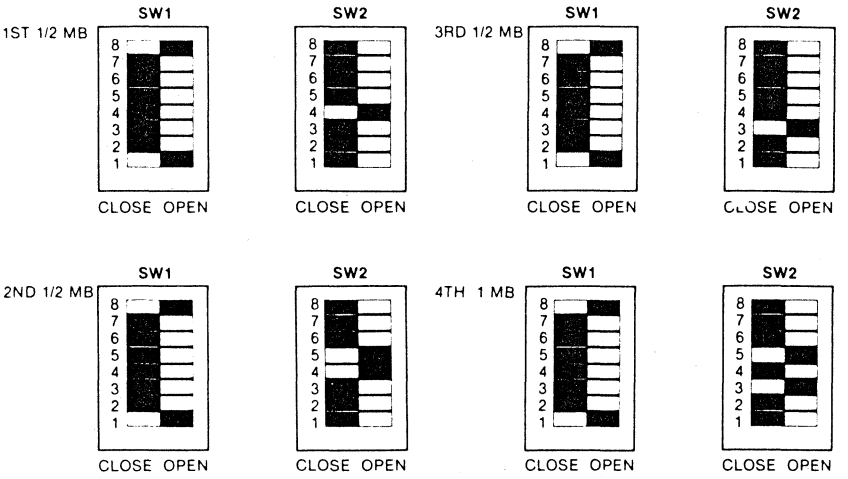


Figure 25

SECTION 11. SERIAL/ PARALLEL CARD

The HP Vectra supports an HP24540A Serial/Parallel Card. The HP24540A provides a serial port and a parallel port for external devices. The HP24540A card is inserted into one of the available I/O backplane slots. In this section the card will be described in two parts: the first part is the serial portion of the card, the second part is the parallel portion of the card.

The following diagram is a layout of the HP24540A. The positions of the jumpers and connectors are shown.

J1 and J2 Location

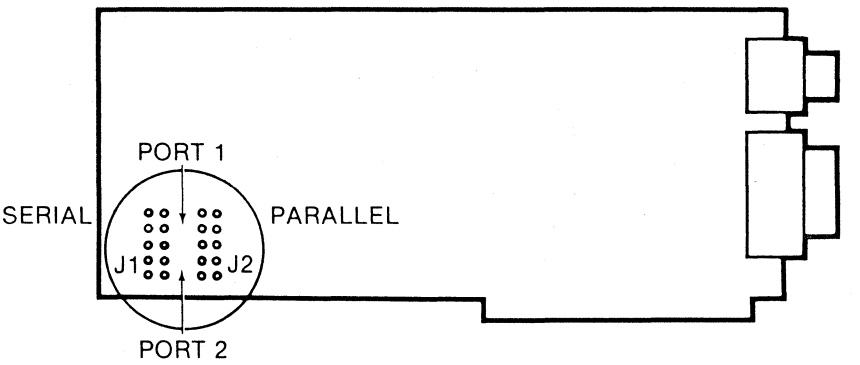


Figure 26

J1 is the address selective serial port, and J2 is the address selective parallel port.

Serial Portion of the Card

The serial portion of the HP24540A provides asynchronous communications at RS-232C levels. Other features include: a programmable baud rate of 75 to 19200 bps, character length of 5, 6, 7, or 8 bits, a stop bit of 1, 1 1/2, or 2, a parity bit, modem control signals, full double buffering, and automatic adding or deletion of start, stop, and parity bits.

Serial Jumpers

There is one serial jumper block on the HP24540A card. The physical jumper block represents two jumpers. The address select depends on the jumper configuration. This jumper can also be configured to inhibit the serial port. The following diagram shows the port selection by placing a jumper cap over the appropriate pins.

J1 Configurations

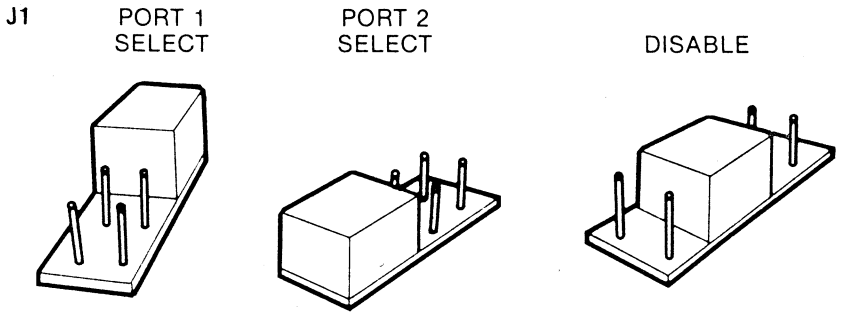


Figure 27

The address and interrupt of the serial port is defined in the following chart.

	Primary	Secondary
Address	3F8H	2F8H
Interrupt	4	3

Serial Port Interface to the System

The serial port uses an RS-232C connector type D9-pin male. The following table defines the pin assignments and signal descriptions for this connector.

Table 11.1

Serial Port Pin Assignments

Pin	I/O	Signal	Description
1	I	CF	When low, it indicates the device has detected the data carrier.
2	I	BB	Rx data
3	O	BA	Tx data
4	O	CD	When active, it informs the device that the card is available to communicate.
5		AB	GND, ground
6	I	CC	When low, it indicates the device is ready to establish the communications link in order to transfer data.
7	O	CA	When active, it informs the device that the card is ready to transmit data.
8	I	CB	When low, it indicates the device is available to receive data.
9	I	CE	When low, it indicates the device has a telephone ringing signal.

Registers

The card has 11 programmable registers that control the operation of the serial portion of the card. The system programmer may gain access or control any of the registers in the serial adapter through the 80286. The registers must be addressed before a read or write operation can take place. The following table defines the registers and their addresses.

Table 11.2

Accessible Registers

Address* Hex	Register
XF8	Transmit Buffer
XF8	Receive Buffer
XF8	Divisor Latch LSB
XF9	Divisor Latch MSB
XF9	Interrupt Enable Register
XFA	Interrupt Identification Register
XFB	Line Control Register
XFC	Modem Control Register
XFD	Line Status Register
XFE	Modem Status Register
XFF	Reserved

*The X is substituted with the port selection number, a 3 for port 1, a 2 for port 2.

Transmit Buffer Register (XF8H)

This register contains the characters to be transmitted via the serial connector. Data bit 0, the least significant bit (LSB), is transmitted first and data bit 7, the most significant bit (MSB), is the last bit transmitted.

Receive Buffer Register (XF8H)

This register contains the characters received via the serial connector. Data bit 0, the least significant bit (LSB), is received first and data bit 7, the most significant bit (MSB), is the last bit received.

Bit 7 of the Line Control Register (XFBH) determines whether the Transmit Buffer Register or the Divisor Latch Register LSB is accessed, and whether the Interrupt Enable Register or the Divisor Latch Register (MSB) is accessed.

Divisor Latch Registers LSB and MSB (XF8H and XF9H)

The divisor latch LSB (XF8H) and the divisor latch MSB (XF9H) registers are used to control the baud-rate of the transmitted and received data.

The HP24540A has a clock of 1.8432MHz. This frequency can be divided by any divisor from 1 to 65,525 as set on the two divisor latches. The output (baud out) frequency is 16 times the baud-rate.

The two divisor latches must be loaded to define the baud-rate before attempting to transmit or receive data. When either of the latches is loaded, a 16-bit baud-rate counter is immediately loaded to prevent long counts on the first load.

The following chart gives examples of loading the divisor latch registers to determine the baud-rate.

Baud Rate	Divisor	MSB (XF9H) Bits 7	6	5	4	3	2	1	0	(XF8H) Bits 7	6	5	4	3	2	1	LSB 0
75	1536	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
110	1047	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1
300	384	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
600	192	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
1200	96	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
2400	48	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
4800	24	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
9600	12	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
19200	6	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Interrupt Enable Register (XF9H)

This register enables and disables the four interrupt signals of the HP24540A.

Bit	Data	Interrupt
0	1	Enable the received data available interrupt.
	0	Disable interrupt.
1	1	Enable transmitter holding register empty interrupt.
	0	Disable interrupt.
2	1	Enable the receiver line status interrupt
	0	Disable interrupt.
3	1	Enable the modem status interrupt.
	0	Disable interrupt.
4-7	0	Always.

When the enabled interrupt signal is received it activates the chip interrupt (INTRPT) output signal which is sent to the system. When all interrupts are disabled, the Interrupt Enable Register and the INTRPT output signal are disabled. The other registers are not affected.

Bit 7 of the Line Control Register (XFB) determines whether the divisor latch MSB or the Interrupt Enable Register is accessed.

Interrupt Identification Register (XFAH)

This register identifies the highest priority pending interrupt signal. When this register is addressed it inhibits the highest priority interrupt. No other interrupts are acknowledged until this inhibited interrupt is cleared.

Bit	Data	Definition
0	0	Interrupt pending.
1-2		Identifies the pending interrupt with the highest priority as in the following:

Bit 1	Bit 2	Interrupt
1	1	Receiver line status
1	0	Received data available
0	1	Transmitter buffer empty
0	0	Modem status

3-7	0	Always.

The following table defines the interrupt priorities.

Table 11.3

Interrupt Priority

Interrupt	Priority	Interrupt Source	Clear Interrupt
Receiver line status	1	Overrun error or parity error or framing error or break (200mS space on receive data line).	Reading the line status register.
Received data available	2	Data available in receive buffer.	Reading the receive buffer register.
Transmitter buffer register empty	3	Data transmitted from transmit buffer.	Reading the interrupt identification register (if source), or writing to the transmit buffer register.
Modem status	4	CB, CC, CE or CF signal received.	Reading the modem status register.

Line Control Register (XFBH)

This register controls the format of the data communications.

Bit	Data	Definition
0-1		Specifies the number of bits in each transmitted or received character as in the following: Bit 0 1 / Character Length in bits 1 1 — 8 1 0 — 7 0 1 — 6 0 0 — 5
2	0	One stop bit is generated or deleted in the data sent or received.
	1	1 1/2 stop bit is generated or deleted for 5-bit words. For a 6, 7, or 8-bit word, 2 stop bits are generated or deleted.
3	0	Disable parity bit.
	1	A parity bit is generated (transmit data) or deleted (receive data).
4	0	When bit 3 is 1, parity bits sent or checked odd.
	1	When bit 3 is 1, parity bits sent or checked even.
5	1	When bit 3 is 1, the parity bit is set 0 for even parity and 1 for odd parity.
	0	Stuck parity disabled.
6	1	Break bit. The transmit data line is set to the space state (0) and remains at that state regardless of the state of the output buffer register.
	0	Set-breaking is disabled.
7	1	Address selection bit. Set to gain access of the divisor latches of the baud-rate generator during a read/write operation.
	0	Reset to gain access of the receiver buffer register, the transmit buffer register, or the interrupt enable register.

Modem Control Register (XFCH)

This register controls the modem signals. It also allows the HP24540A to be set into diagnostic mode. In the diagnostic mode, transmitted data is received immediately. The receiver and transmitter interrupts and the modem control interrupts are fully operational, allowing the interrupts to be tested.

Bit	Data	Definition
0	1	Data terminal ready (CD) signal active.
	0	CD signal inactive.
1	1	Request to sent (CA) signal active.
	0	CA signal inactive.
2		Controls the ~OUT1 signal from the controller chip. Can be 0 or 1.
3	1	Controls ~OUT2 signal from the controller chip. Enables INTRPT generated by the interrupt enable register.
	0	The ~OUT2 output is forced inactive.
4	1	Enables the modem loopback feature (diagnostic test) as follows: • Receiver serial input is disabled. • Transmitter serial output is set to the active state. • The output from the transmitter shift register is looped back to the receiver shift register. • The four modem control inputs to the modem status register are disabled. • The four modem control outputs from the modem control register are internally connnected to the four modem control inputs.
5-7	0	Always.

Line Status Register (XFDH)

This register provides information on the data transfer. Bits 1 through 4 are error conditions that generate a receiver line status interrupt. This register is not to be written to.

Bit	Data	Definition
0	1	Set when a complete incoming character has been received and transferred into the receiver buffer register.
	0	Reset by reading the data in the receiver buffer register or writing 0 in it.
1	1	Indicates that data in the receive buffer register was not read by the processor before the next character was transferred into the register, thereby erasing the previous character.
	0	Reset when the 80286 reads the Line Status Register.
2	1	Detection of a parity error.
	0	Reset when the 80286 reads the Line Status Register.
3	1	Framing error has occured, character does not have a valid stop bit.
	0	Reset when the 80286 reads the Line Status Register.
4	1	The received data line was at a space state (0) for longer than a transmission time of a complete data character. (Including start, data, parity, and stop bits.)
	0	Reset when the 80286 reads the Line Status Register.
5	1	Set when a character is transferred from the transmit buffer register to the transmit shift register indicating the card is available to transmit another character.
	0	Reset when the next character is written into the transmit buffer register.
6	1	Transmit buffer register and transmit shift register are empty.
	0	Reset when either register contains a character.
7	0	Always.

Modem Status Register (XFEH)

This register provides information on the current state of the control lines from the modem or device.

Bit	Data	Definition
0	1	Set if clear to send signal (CB) input changes state.
	0	Reset when the Modem Status Register is read.
1	1	Set if data set ready (CC) input changes state.
	0	Reset when the Modem Status Register is read.
2	1	Set when the ring indicator (CE) input changes from low to a high state.
	0	Reset when the modem stauts register is read.
3	1	Set if the received line signal detector (CF) input changes state.
	0	Reset when the Modem Status Register is read.
4	1	Set when the CB input is active. However, if the modem loopback is enabled, this bit is equivalent to CA of XFCH (bit 1).
	0	Reset when the CB input is inactive.
5	1	Set when the CC input is active. However, if the modem loopback is enabled, this bit is equivalent to CD of XFCH (bit 0).
	0	Reset when the CC input is inactive.
6	1	Set when the CE input is active. However, if the modem loopback is enabled, this bit is equivalent to ~OUT1 of XFCH (bit 2).
	0	Reset when the CE input is inactive.
7	1	Set when the CF input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT2 of XFCH (bit 3).
	0	Reset when the CF input is inactive.

Serial Port Cables

There are three cables available for connecting the serial port to a device. These cables are:

- The HP24542M serial US/European modem cable
- The HP24542G serial printer cable. (male/male)
- The HP24542H serial printer cable. (male/female)

The HP24542M serial (RS-232C) US/European modem cable, female 9-pin to male 25-pin, has the following pin assignments. Signal descriptions are defined in table 11.1 in this section.

Table 11.4

HP2452M Serial US/European Modem Cable Pin Assignments

Card Side Pin	Signal	Device Side Pin
1	CF	8
2	BB	3
3	BA	2
4	CD	20
5	AB	7
6	CC	6
7	CA	4
8	CB	5
9	CE	22
	AA (cable shield)	1

The HP24542M serial (RS-232C) printer cable, female 9-pin to male 25-pin) has the following pin assignments.

Table 11.5

HP24542G and HP24542H Serial Printer Cables

Pin Assignments

Card Side Pin	Signal	Device Side Pin
1	CF	4
2	BB	2
3	BA	3
4	CD	5-6
5	AB	7
6 }	CC	20
7 }	CA	8
8 }	CB	
	AA (cable shield)	1

Parallel Portion of the Card

The parallel portion of the card provides a parallel port to attach devices that accept eight bits of parallel data at standard TTL levels. It includes programmable printer control such as: automatic initialization, printer select, auto linefeed, and data strobe.

Parallel Jumpers

There is one parallel jumper block on the HP24540A card. The physical jumper block represents two jumpers. The address select depends on the jumper configuration. One jumper selects the address and the other jumper selects the interrupt being used. The following diagram shows the port selection by placing a jumper cap over the appropriate pins.

J2 Configurations

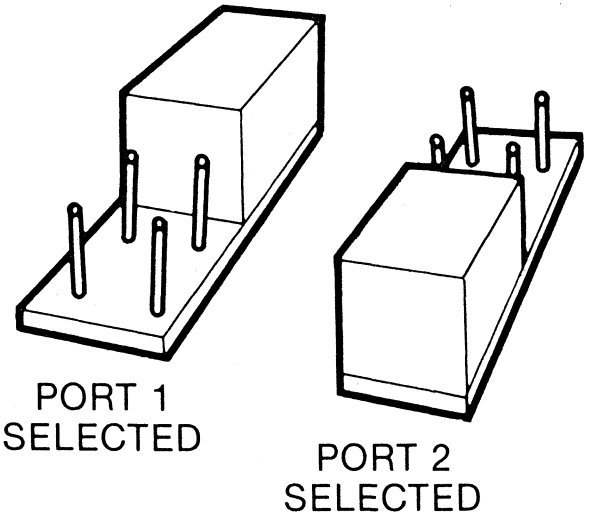


Figure 28

The following chart defines the addresses and interrupts for the parallel port.

	Primary	Secondary
Address	378H	278H
Interrupt	7	5

Parallel Port Interface to the System

The parallel port uses an RS-232C connector type D25-pin female. The following table defines the pin assignments and signal descriptions for this connector.

Table 11.6

Parallel Port Pin Assignments

Pin	I/O	Signal	Definition
1	O	~STROBE	Data strobe
2	O	D0	Data bit 0
3	O	D1	Data bit 1
4	O	D2	Data bit 2
5	O	D3	Data bit 3
6	O	D4	Data bit 4
7	O	D5	Data bit 5
8	O	D6	Data bit 6
9	O	D7	Data bit 7
10	I	~ACK	Printer has processed the received character.
11	I	BUSY	Printer is busy and will not accept more data.
12	I	PE	Printer detects end of paper.
13	I	~SLCT IN	Printer select.
14	O	~AUTO FD	Printer to perform a linefeed after a line is printed.
15	I	~ERROR	Printer has encountered an error.
16	O	~INIT	Initialize printer.
17	O	~SLCT IN	Set low to enable the printer to accept data.
18		GND	Ground
19		GND	Ground
20		GND	Ground
21		GND	Ground
22		GND	Ground
23		GND	Ground
24		GND	Ground
25		GND	Ground

Registers

The card has three programmable registers that control the operation of the parallel portion of the card. The system programmer may gain access or control any of the registers in the parallel adapter through the 80286. The registers must be addressed before a read or write operation can take place. The following table defines the registers and their addresses.

Table 11.7

Accessible Registers

Address* Hex	Register
X78 or X7C	Data Buffer Register
X7A or X7E	Printer Control Register
X79 or X7D	Printer Status Register

Data Buffer Register (X78H or X7CH)

This register contains the data character. Reading from this address causes the character to be read by the card. Writing to this address causes the character to be transmitted via the parallel connector.

*The X is substituted with the appropriate port selection number, a 3 for port 1, a 2 for port 2.

Printer Control Register (X7A to X7E)

This register controls the printer signals.

Bit	Data	Definition
0	1	Generates an active high STROBE signal for a minimum of 500nS. The STROBE signal clocks the data from the parallel port into the printer. The valid data must be present a minimum of 0.5uS before and after the STROBE signal.
	0	STROBE inactive.
1	1	Generates the AUTO FD signal.
	0	AUTO FD inactive.
2	0	Generates the ~INIT signal for a minimum of 50uS.
	1	~INIT inactive.
3	1	Generates the ~SLCT IN signal.
	0	SLCT IN inactive.
4	1	Enables the IRQ when the ~ACK input signal changes from true to false.
	0	Disable IRQ.
5-7	0	Always.

Printer Status Register (X79H or X7D)

This register provides information on the control lines from the printer.

Bit	Data	Definition
0-2	0	Always.
3	0	The ~ERROR input is active.
4	1	The SLCT input is active.
5	1	The PE input is active.
6	0	The ~ACK input is active.
7	0	The BUSY input is active.

Parallel Port Cable

Cable HP24542D is available to connect the parallel port to a printer.

The HP24542D parallel cable (male 25-pin to Amphenol 36-pin) has the following pin assignments. Signal descriptions are defined in table 11.6 in this section.

Table 11.8

HP24542D Parallel Cable Pin Assignments

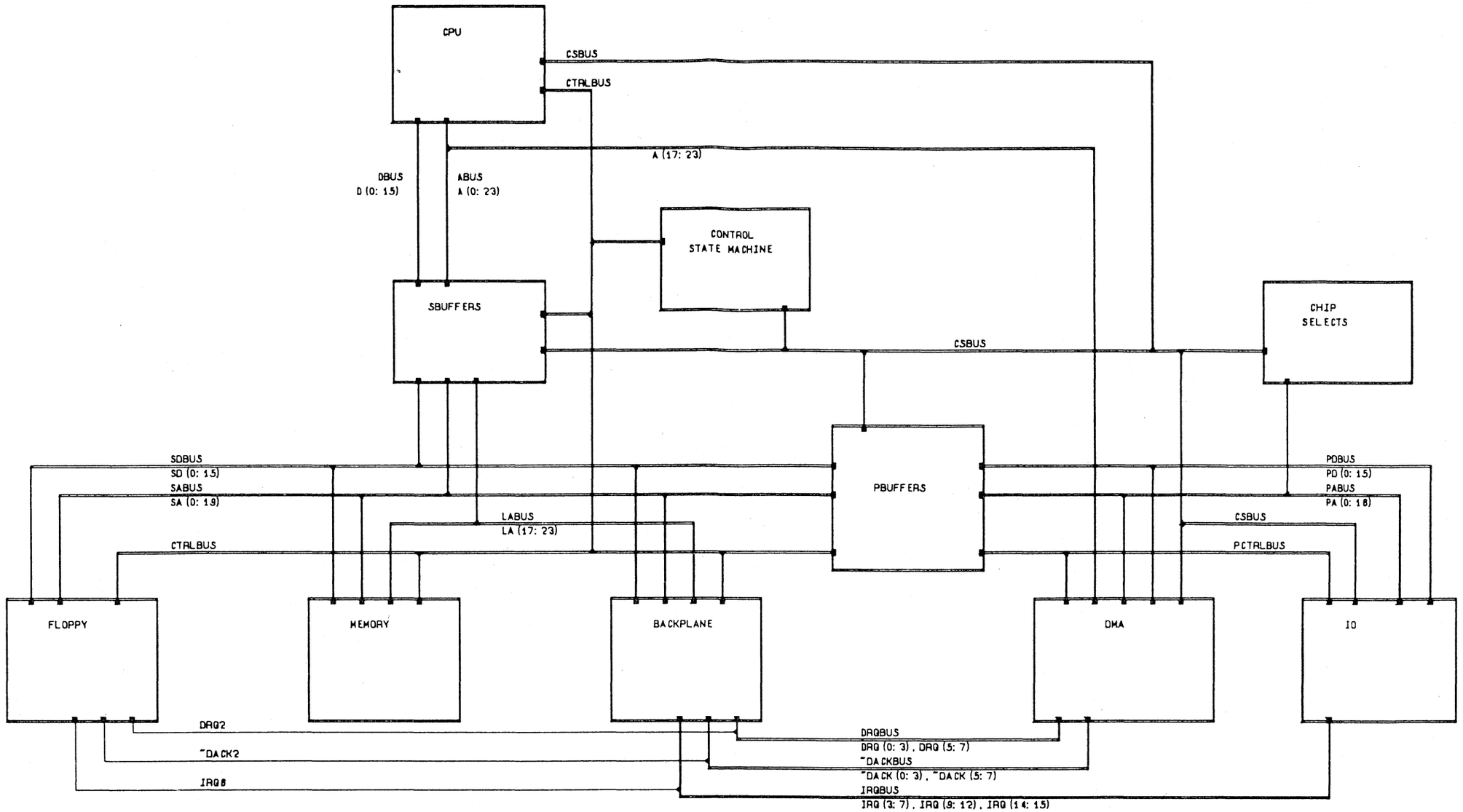
Card Side Pin	Signal	Device Side Pin
1	STROBE	1
2	D0	2
3	D1	3
4	D2	4
5	D3	5
6	D4	6
7	D5	7
8	D6	8
9	D7	9
10	~ACK	10
11	BUSY	11
12	PE	12
13	SLCT	13
14	~AUTO FD	14
15	~ERROR	32
16	~INIT	31
17	~SLCT (output)	36
18-25	GND	19-30

SECTION 12. SCHEMATICS

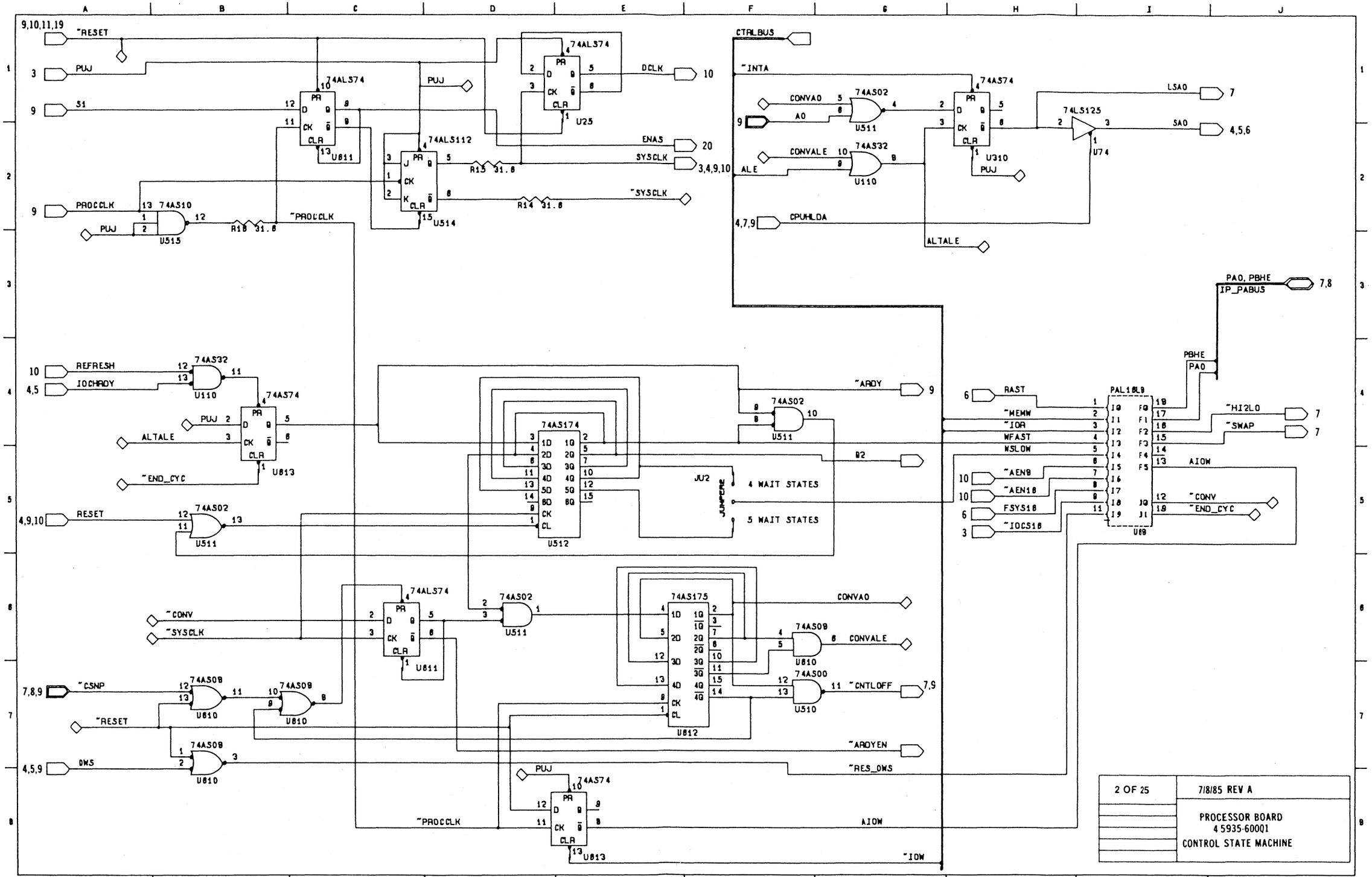
The following are schematic drawings of:

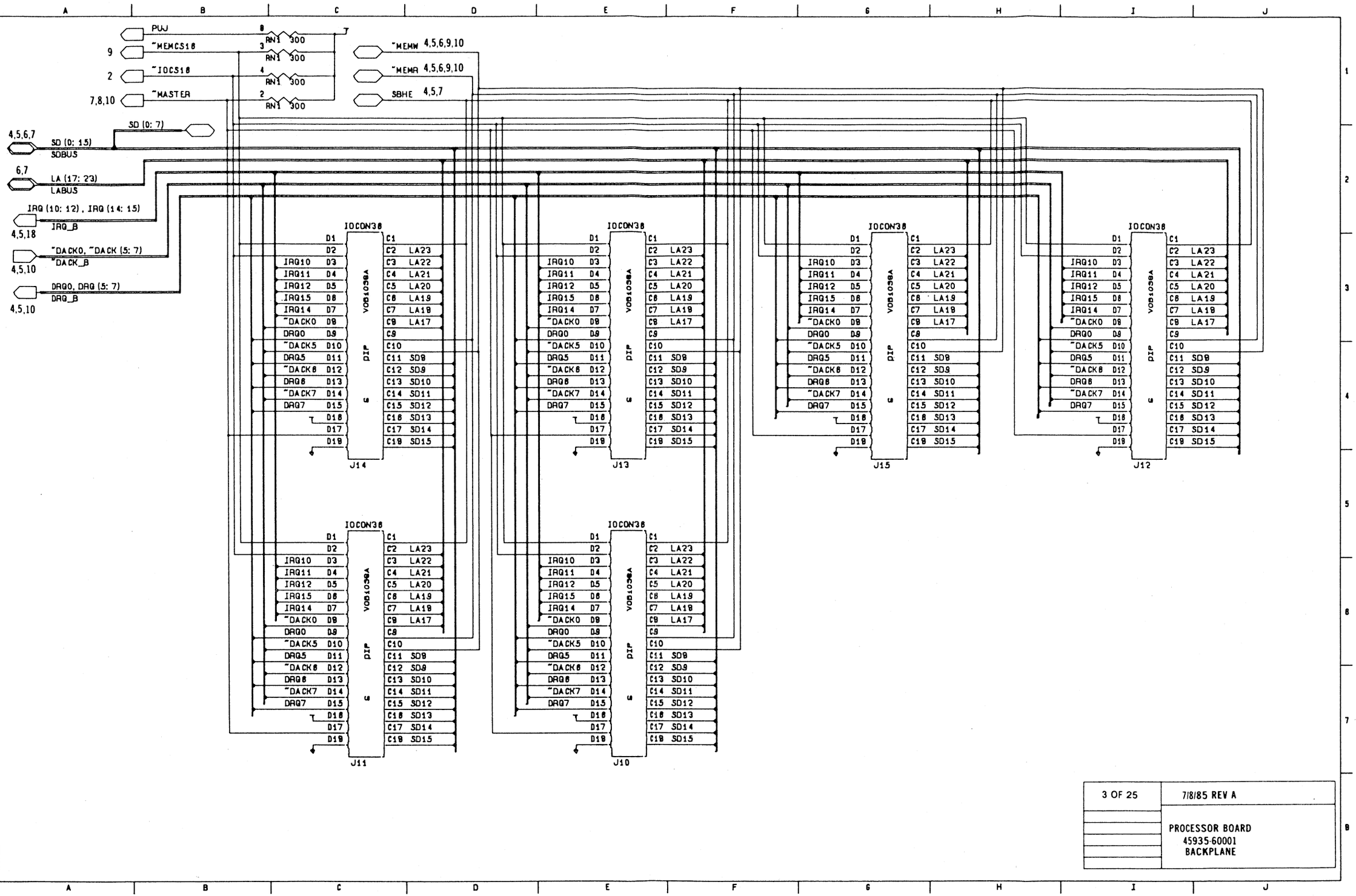
- Processor Board (45935-60001)
- Processor Extension Card (45935-60002)
- Multi-Mode Video Adapter Card (45981-60001)
- Memory Expansion Card (45974-60001)
- Serial/Parallel Adapter Card (24540-60001)

The drawings for the I/O cards are independently numbered. Lines that continue to or from other pages have the preceding or following page number referenced on that line.

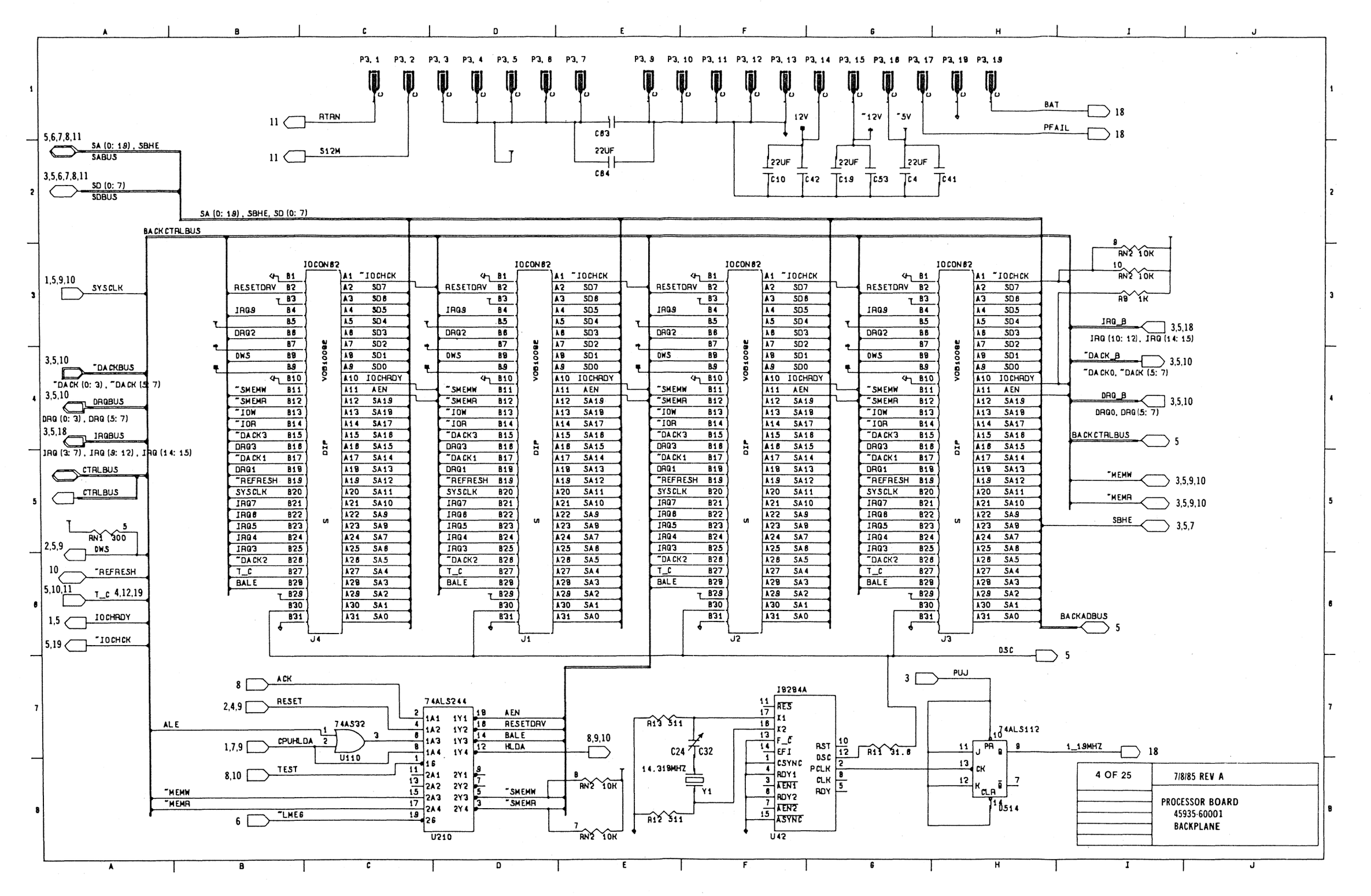


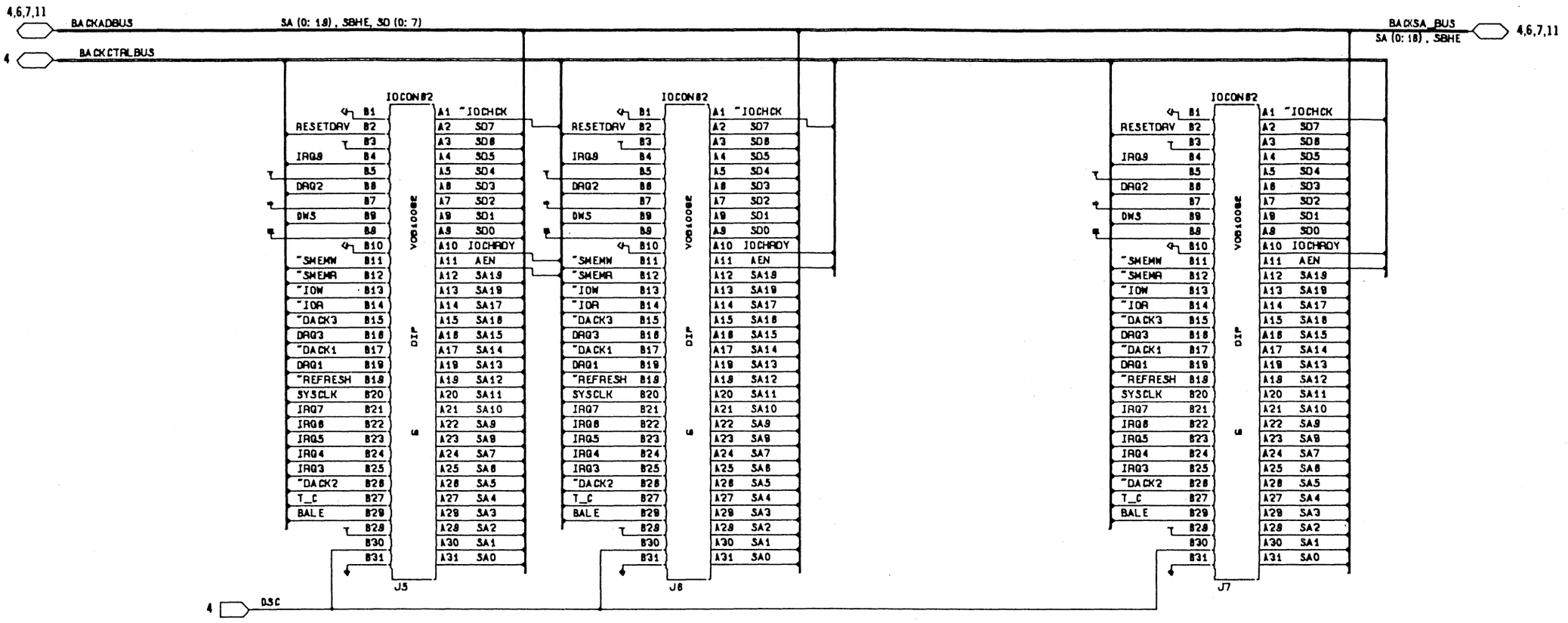
1 OF 25	7/8/85 REV A
PROCESSOR BOARD 45935-60001 **BLOCK DIAGRAM**	


9,10,11,19
~RESET
3
PUJ
9
S1
74ALS74
U611
74ALS112
U514
74ALS74
U25
DCLK
10
ENAS
20
SYSCLK
3,4,9,10
R15 31.6
~SYSCLK
R14 31.6
9
PROCCLK
74AS10
U515
R16 31.6
~PROCCLK
CTRLBUS
~INTA
74AS74
U310
CONVA0
A0
74AS02
U511
CONVALE
ALE
74AS32
U110
74LS125
U74
LSA0
7
SA0
4,5,6
4,7,9
CPUHLDA
ALTALE
PA0, PBHE
IP_PABUS
7,8
PBHE
PA0
10
REFRESH
4,5
IOCHRDY
74AS32
U110
74AS74
U613
ALTALE
~END_CYC
~ARDY
9
74AS02
U511
74AS174
U512
Q2
JU2
JUMPERE
4 WAIT STATES
5 WAIT STATES
6
RAST
~MEMW
~IOR
WFAST
WSLOW
~AEN8
~AEN16
F.SYS16
~IOCS16
PAL16L8
U69
~HI2LO
7
~SWAP
7
AIOW
~CONV
~END_CYC
4,9,10
RESET
74AS02
U511
~CONV
~SYSCLK
74ALS74
U611
74AS02
U511
74AS175
U812
CONVA0
CONVALE
74AS08
U810
~CNTLOFF
7,9
74AS00
U510
7,8,9
~CSNP
74AS08
U810
~RESET
~ARDYEN
4,5,9
0WS
~RES_0WS
PUJ
74AS74
U813
~PROCCLK
AIOW
~IOW
2 OF 25
7/8/85 REV A
PROCESSOR BOARD
4 5935-60001
CONTROL STATE MACHINE

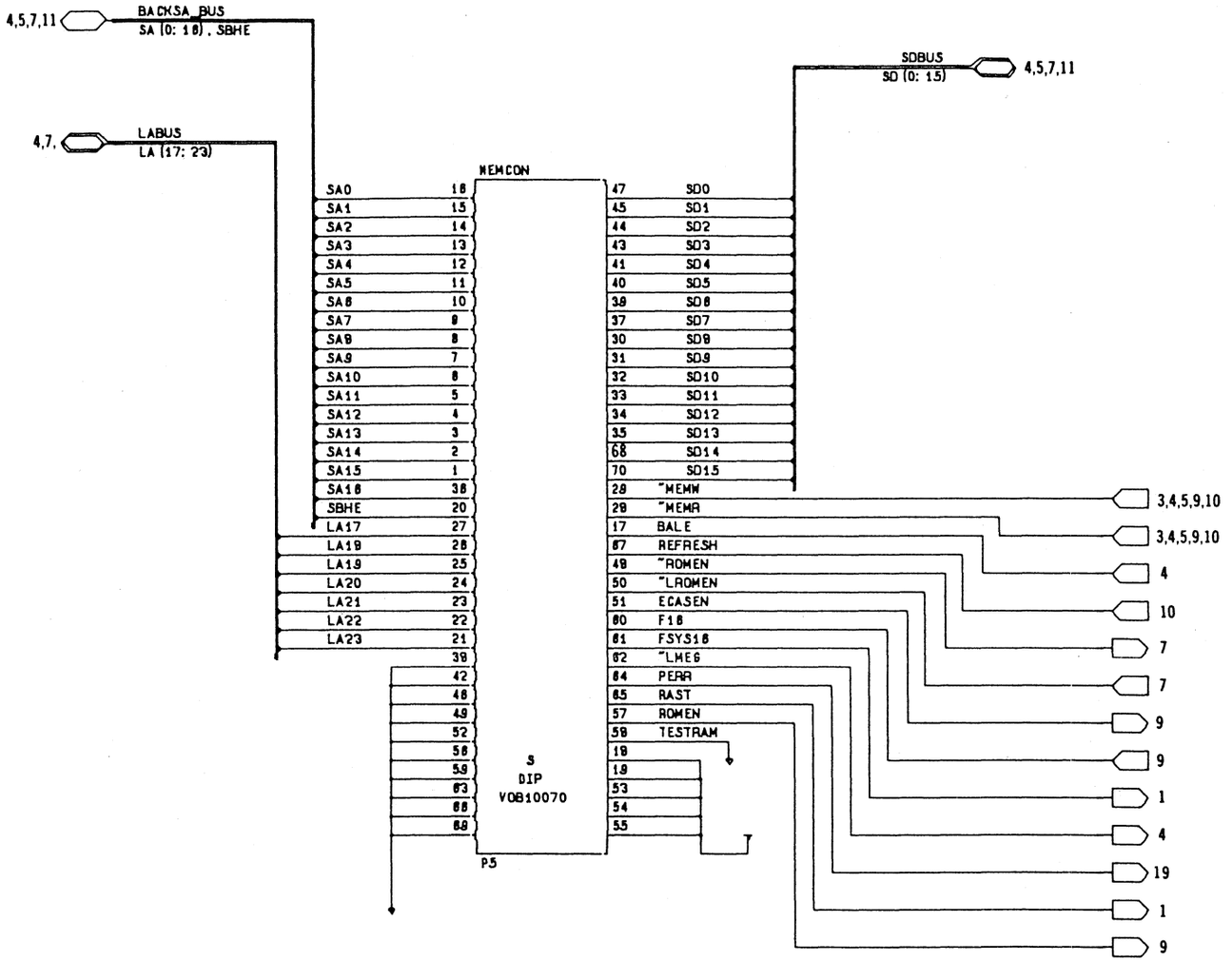


3 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 BACKPLANE


P3, 1 P3, 2 P3, 3 P3, 4 P3, 5 P3, 6 P3, 7 P3, 9 P3, 10 P3, 11 P3, 12 P3, 13 P3, 14 P3, 15 P3, 16 P3, 17 P3, 18 P3, 19
11 RTAN
11 S12M
C83 22UF C84
12V -12V -5V
22UF C10 C42 C19 C53 C4 C41
BAT 18
PFAIL 18
5,6,7,8,11 SA (0: 19), SBHE SABUS
3,5,6,7,8,11 SD (0: 7) SDBUS
SA (0: 19), SBHE, SD (0: 7)
BACKCTRLBUS
IOCON82
VOB1008E
DIP
J4 J1 J2 J3
1,5,9,10 SYSCLK
3,5,10 ~DACKBUS
~DACK (0: 3), ~DACK (5: 7)
3,5,10 DRQBUS
DRQ (0: 3), DRQ (5: 7)
3,5,18 IRQBUS
IRQ (3: 7), IRQ (9: 12), IRQ (14: 15)
CTRLBUS
RN1 300
2,5,9 DWS
10 ~REFRESH
5,10,11 T_C 4,12,19
1,5 IOCHRDY
5,19 ~IOCHCK
8 RN2 10K
10 RN2 10K
RB 1K
IRQ_B 3,5,18
IRQ (10: 12), IRQ (14: 15)
~DACK_B 3,5,10
~DACK0, ~DACK (5: 7)
DRQ_B 3,5,10
DRQ0, DRQ (5: 7)
BACKCTRLBUS 5
~MEMW 3,5,9,10
~MEMR 3,5,9,10
SBHE 3,5,7
BACKADBUS 5
DSC 5
8 ACK
2,4,9 RESET
ALE
74AS32 U110
1,7,9 CPUHLDA
8,10 TEST
~MEMW
~MEMR
6 ~LME6
74ALS244 U210
AEN RESETDRV BALE HLDA ~SMEMW ~SMEMR
8,9,10
8 RN2 10K
7 RN2 10K
R13 511
C24 C32
14.318MHZ Y1
R12 511
8284A U42
RES X1 X2 F_C EFI CSYNC RDY1 AEN1 RDY2 AEN2 ASYNC
RST DSC PCLK CLK RDY
R11 31.6
3 PUJ
74ALS112 U514
1_19MHZ 18
4 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
BACKPLANE

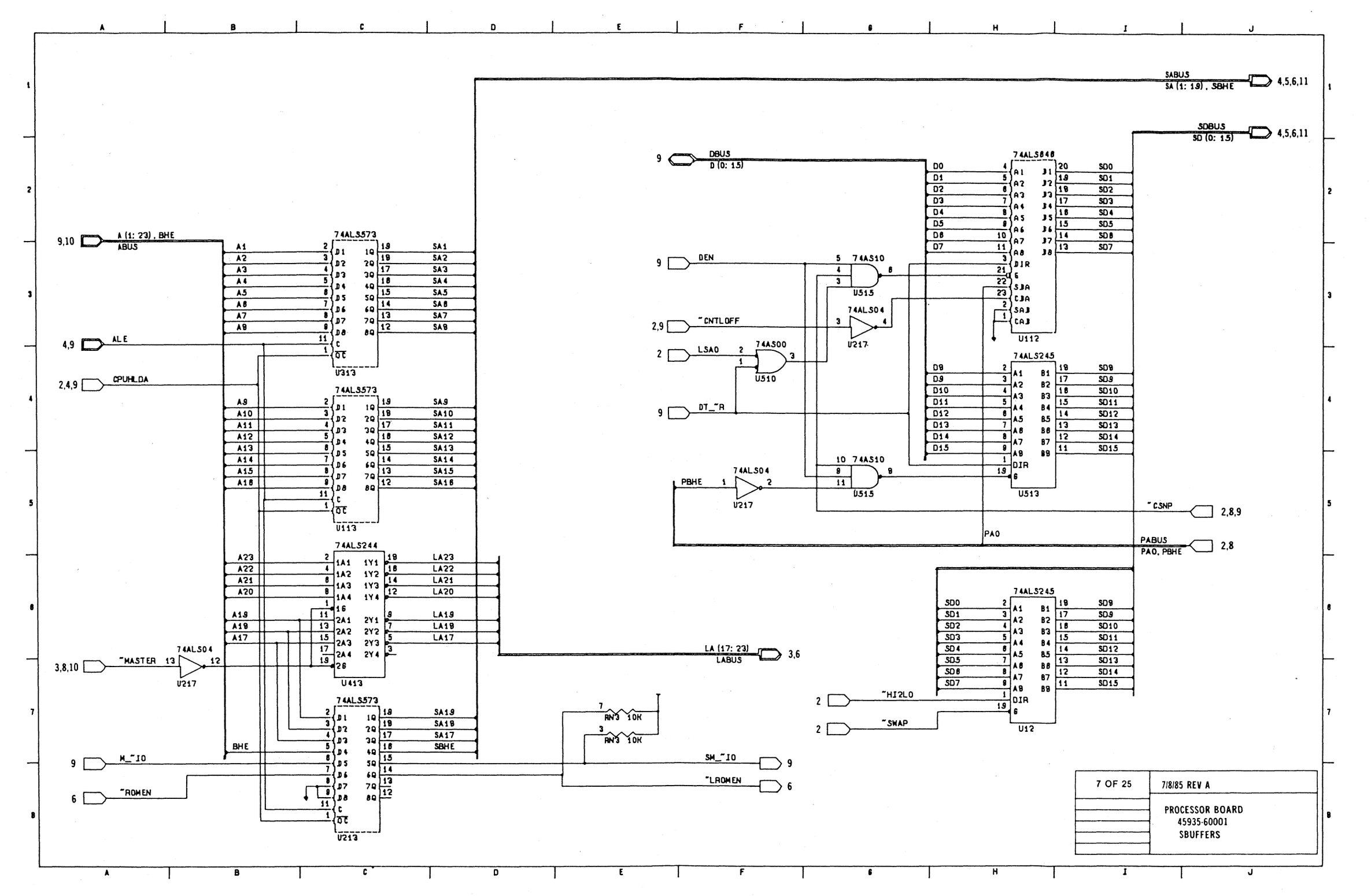


5 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 BACKPLANE

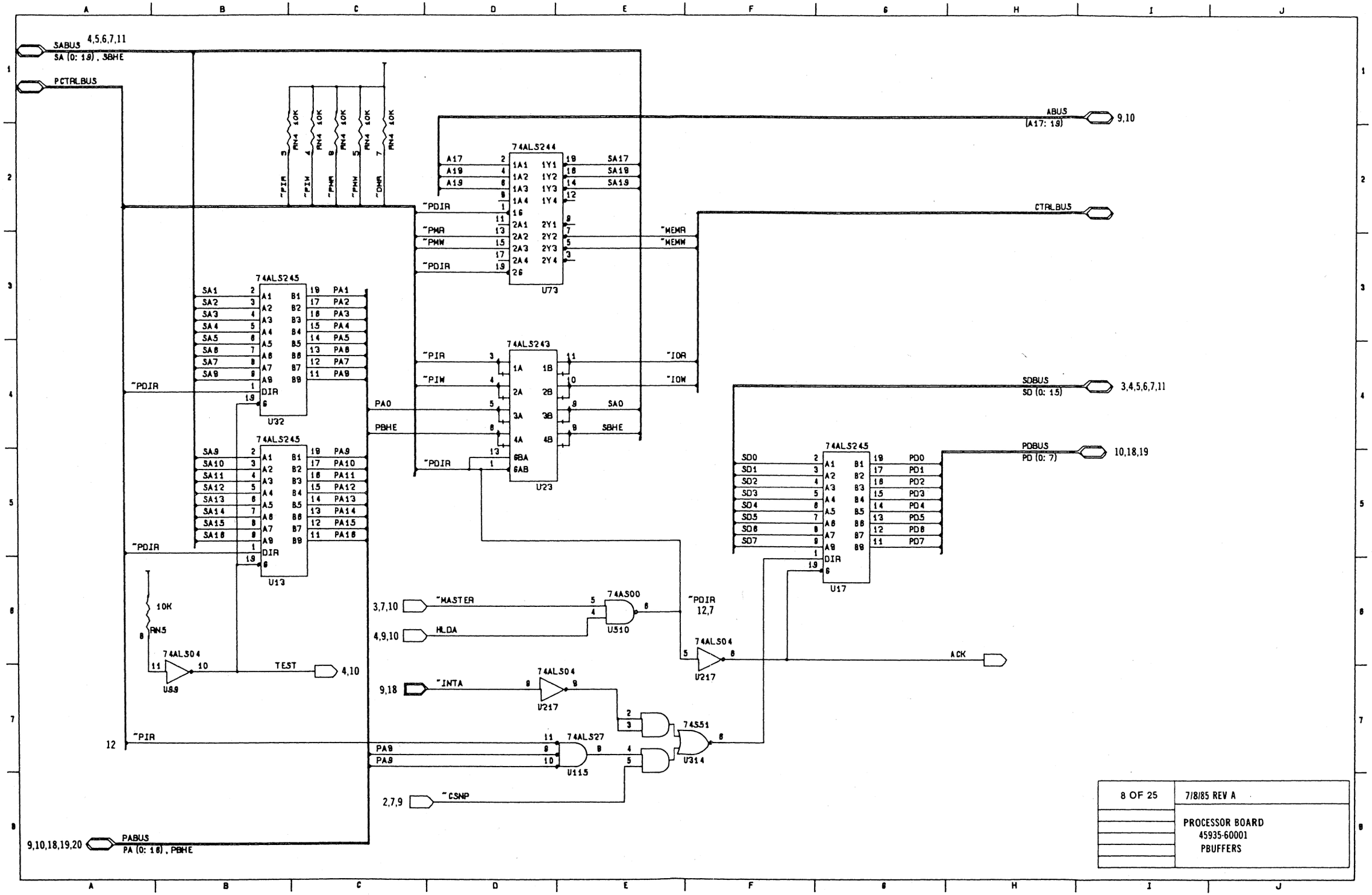


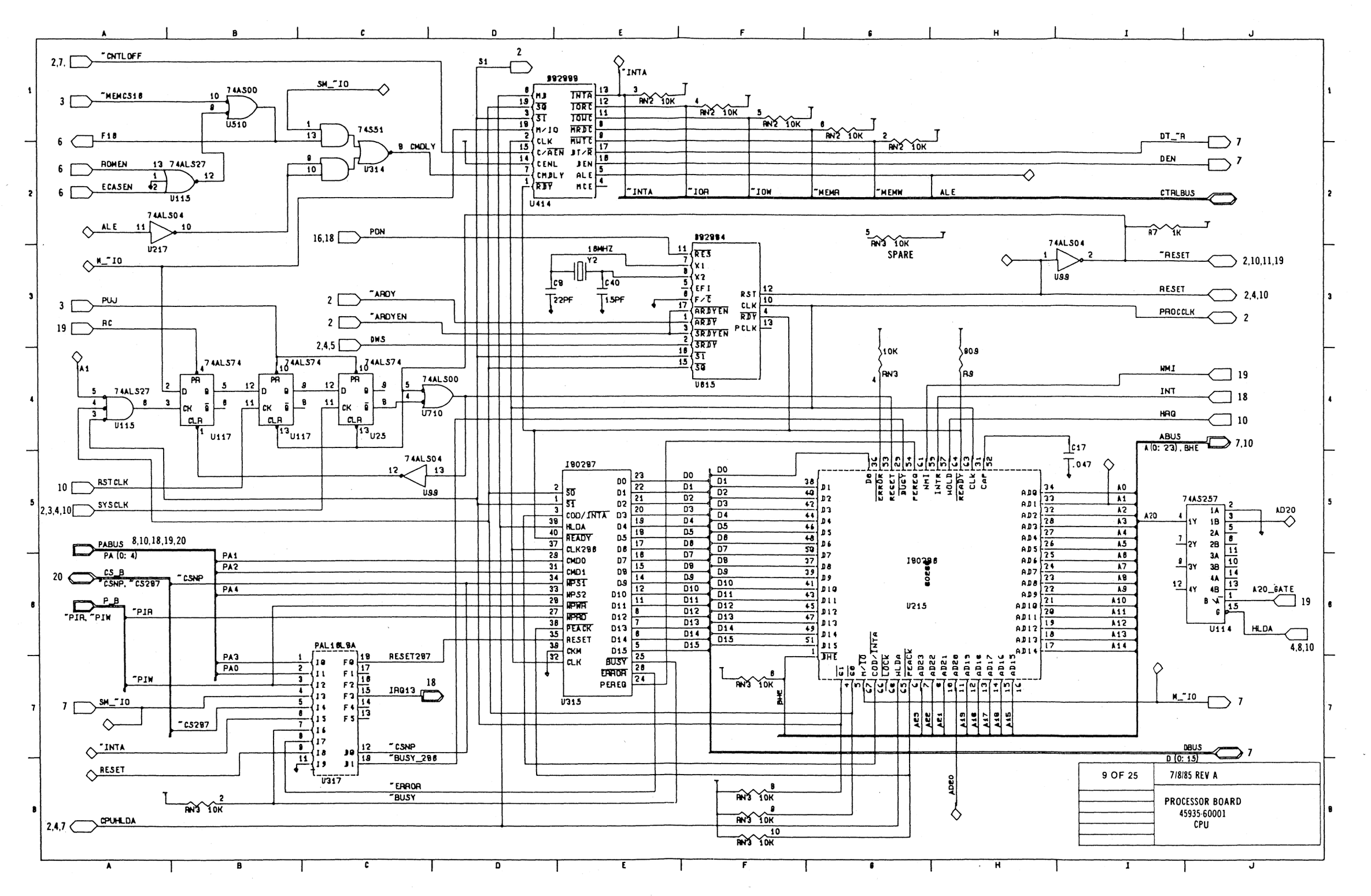
6 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 EXTENSION CONNECTOR

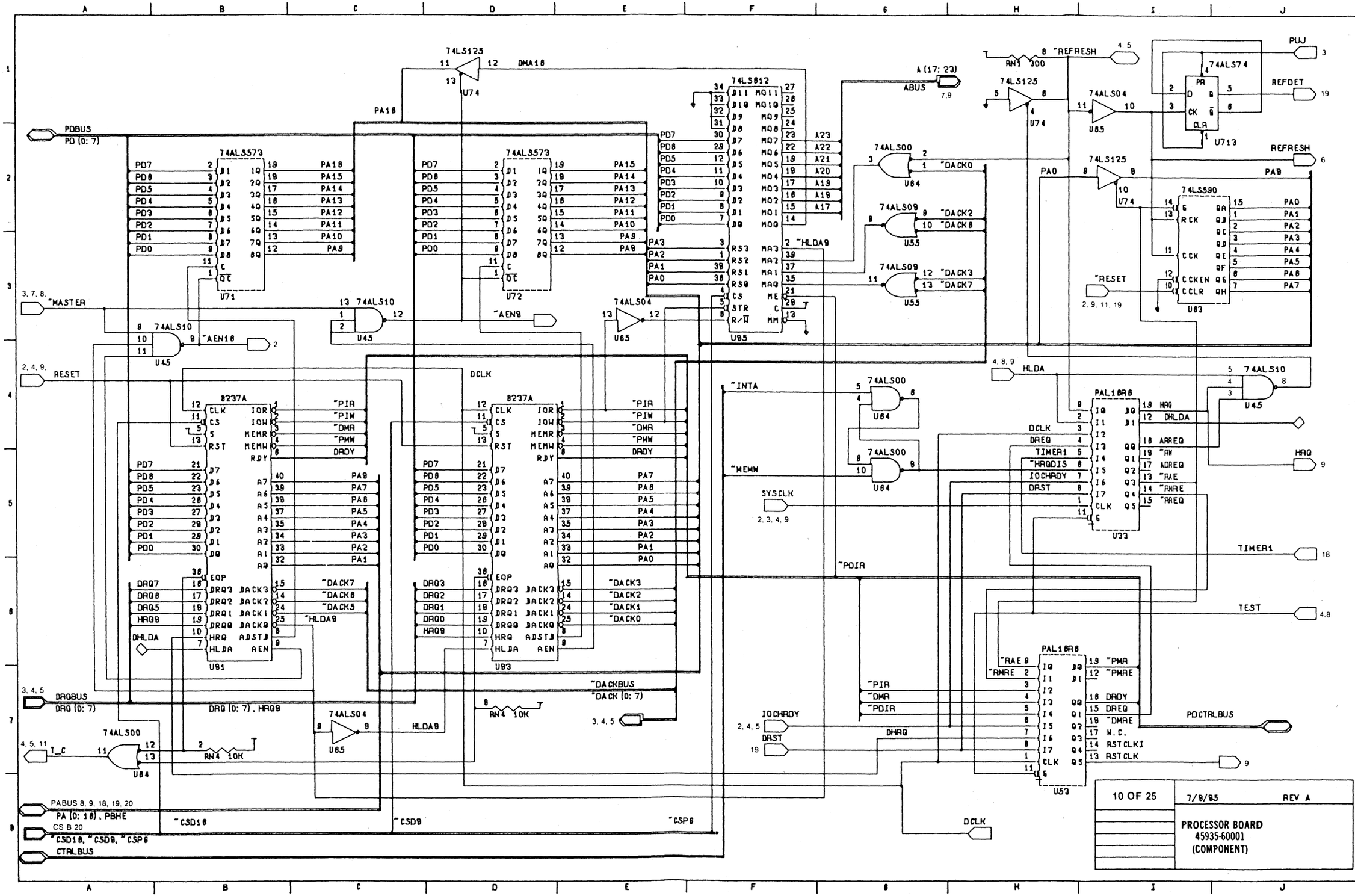
BORDER

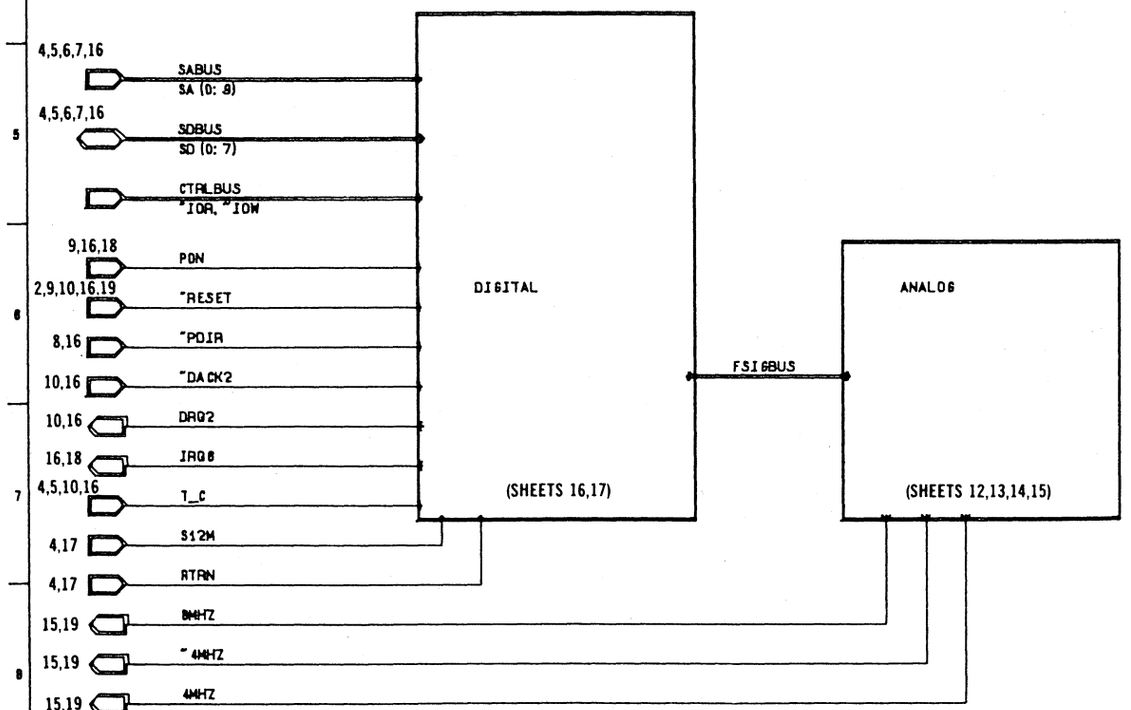


7 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 SBUFFERS

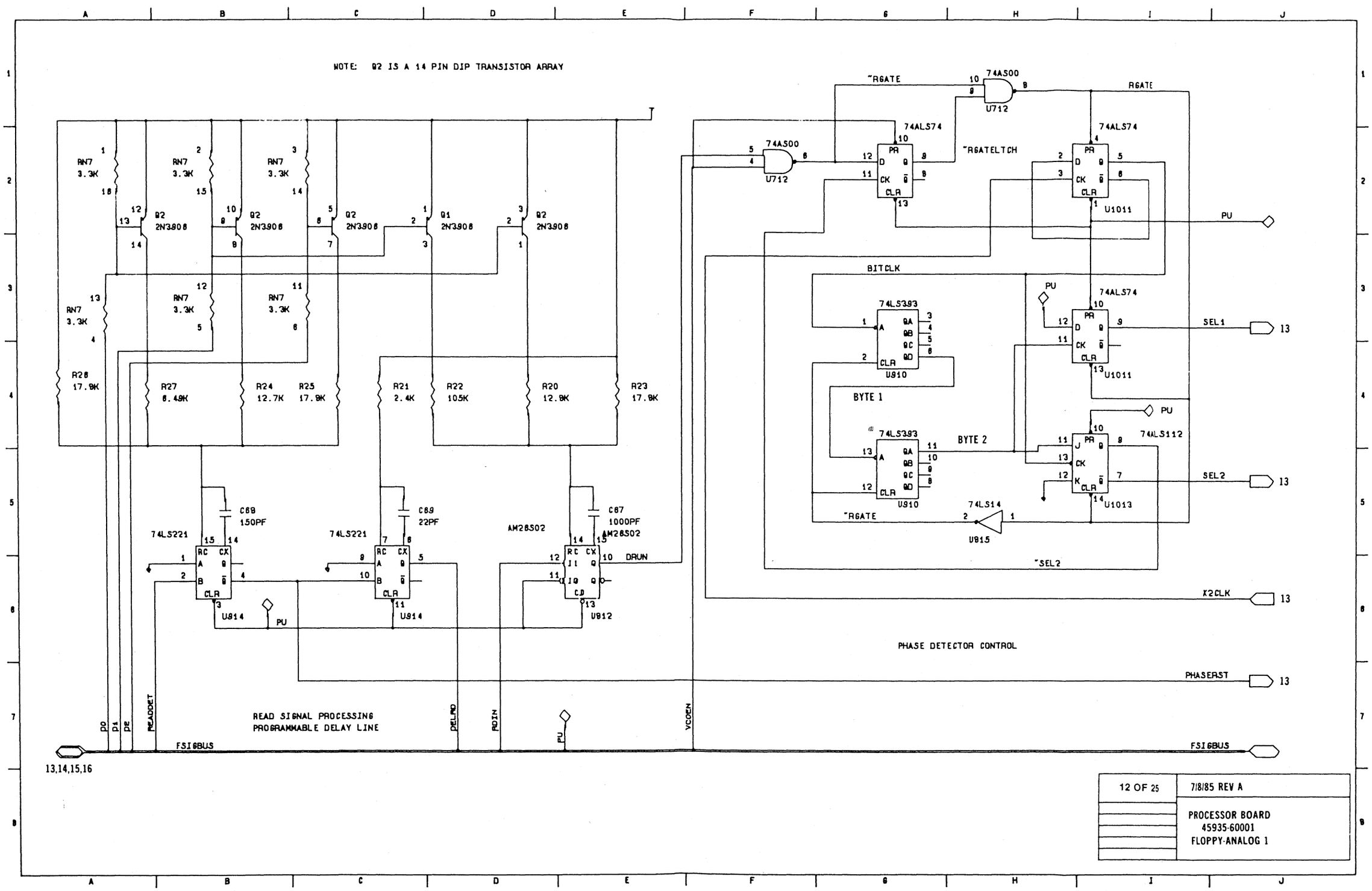

SABUS
SA (0: 19), SBHE
4,5,6,7,11
PCTRLBUS
RN4 10K
~PIR
~PIW
~PMR
~PMW
~DMR
74ALS244
U73
A17
A19
A19
SA17
SA19
SA19
~PDIR
~PMR
~PMW
~PDIR
~MEMR
~MEMW
ABUS
(A17: 19)
9,10
CTRLBUS
74ALS245
U32
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
~PDIR
74ALS243
U23
~PIR
~PIW
PA0
PBHE
~PDIR
SA0
SBHE
~IOR
~IOW
SDBUS
SD (0: 15)
3,4,5,6,7,11
74ALS245
U13
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PA16
~PDIR
74ALS245
U17
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PDBUS
PD (0: 7)
10,18,19
10K
RN5
74ALS04
U89
TEST
4,10
3,7,10
~MASTER
74AS00
U510
4,9,10
HLDA
~PDIR
12,7
74ALS04
U217
ACK
9,18
~INTA
74ALS04
U217
74S51
U314
12
~PIR
74ALS27
U115
PA9
PA9
2,7,9
~CSNP
9,10,18,19,20
PABUS
PA (0: 16), PBHE
8 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
PBUFFERS


2,7, ~CNTLOFF
3 ~MEMCS16
6 F18
6 ROMEN
6 ECASEN
74ALS00 U510
74ALS27 U115
SM_~IO
74S51 U314
B CMDLY
74ALS04 U217
ALE
M_~IO
16,18 PON
PUJ
19 RC
A1
74ALS27 U115
74ALS74 U117
74ALS74 U117
74ALS74 U25
74ALS00 U710
74ALS04 U99
10 RSTCLK
2,3,4,10 SYSCLK
2 ~ARDY
2 ~ARDYEN
2,4,5 DWS
S1
2
892999 U414
~INTA
RN2 10K
DT_~R
DEN
CTRLBUS
~INTA ~IOR ~IOW ~MEMR ~MEMW ALE
18MHZ Y2
C8 22PF
C40 15PF
892984 U815
RES X1 X2 EFI F/~C ARDYEN ARDY SRDYEN SRDY SO S1
RST CLK RDY PCLK
RN3 10K SPARE
74ALS04 U99
R7 1K
~RESET 2,10,11,19
RESET 2,4,10
PROCCLK 2
10K RN3
80.9 R9
WMI 19
INT 18
HRQ 10
ABUS A(0:23), BHE 7,10
C17 .047
I80297 U315
SO S1 COD/~INTA HLDA READY CLK288 CMD0 CMD1 ~MPS1 MPS2 ~MPWR ~MPRD PEACK RESET CKM CLK
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
BUSY ERROR PEREQ
I80286 U215
D0 ERROR RESET BUSY PEREQ NMI INTR HOLD READY CLK CAP
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
M/~IO COD/~INTA LOCK HLDA PEACK AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15
74AS257 U114
A20 AD20 A20_GATE 19 HLDA 4,8,10
PABUS 8,10,18,19,20
PA (0:4) PA1 PA2 PA4 PA3 PA0
20 CS_B ~CSNP, ~CS287 ~CSNP
P_B ~PIR, ~PIW ~PIR ~PIW
PAL16L8A U317
RESET287 IRQ13 18 ~CSNP ~BUSY_286
7 SM_~IO
~CS287
~INTA
RESET
~ERROR
~BUSY
RN3 10K
2,4,7 CPUHLDA
DBUS D(0:15) 7
M_~IO 7
9 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
CPU

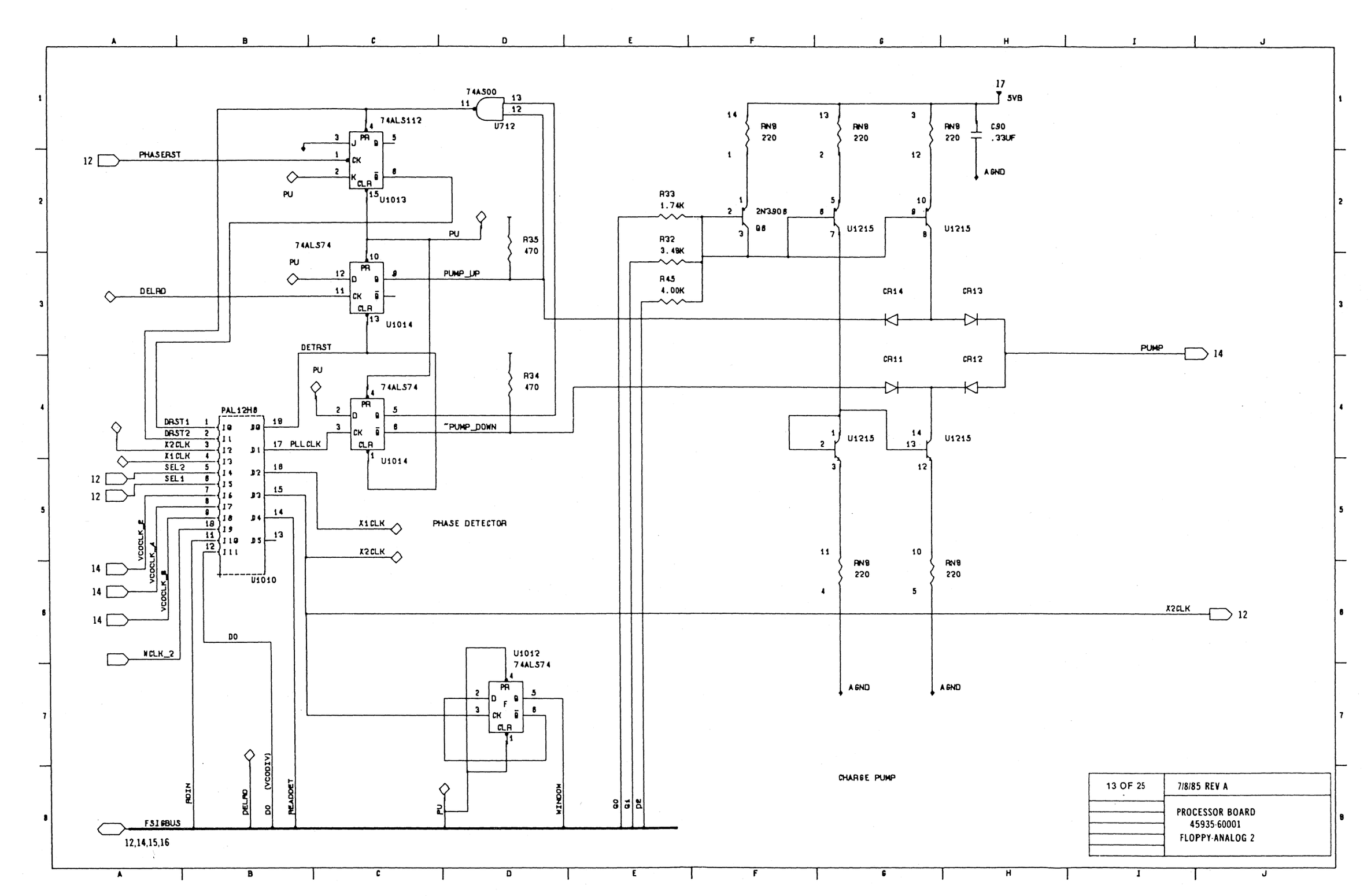

74LS125
DMA18
U74
PA18
PDBUS
PD (0: 7)
74ALS573
U71
U72
74LS812
U85
A (17: 23)
ABUS
7.9
RN1 300
"REFRESH
4, 5
74ALS74
U713
PUJ
REFDET
74ALS04
U85
74ALS00
U64
74ALS08
U55
REFRESH
PA0
PA9
74LS590
U83
"RESET
2, 9, 11, 19
3, 7, 8,
"MASTER
74ALS10
U45
"AEN16
"AEN8
RESET
8237A
U81
U83
DCLK
"INTA
"MEMW
SYSCLK
2, 3, 4, 9
4, 8, 9
HLDA
PAL16R8
U33
HRQ
TIMER1
TEST
"PDIR
DRQBUS
DRQ (0: 7)
DRQ (0: 7) , HRQ8
"DACKBUS
"DACK (0: 7)
RN4 10K
IOCHRDY
DRST
DHRQ
"PIR
"DMA
"PDIR
"RAE
"AMRE
"PMR
"PMRE
DRDY
"DMRE
PDCTRLBUS
RSTCLKI
RSTCLK
PABUS 8, 9, 18, 19, 20
PA (0: 18) , PBHE
CS B 20
"CSD16, "CSD8, "CSP6
CTRLBUS
"CSD16
"CSD8
"CSP6
10 OF 25
7/8/85
REV A
PROCESSOR BOARD
45935-60001
(COMPONENT)



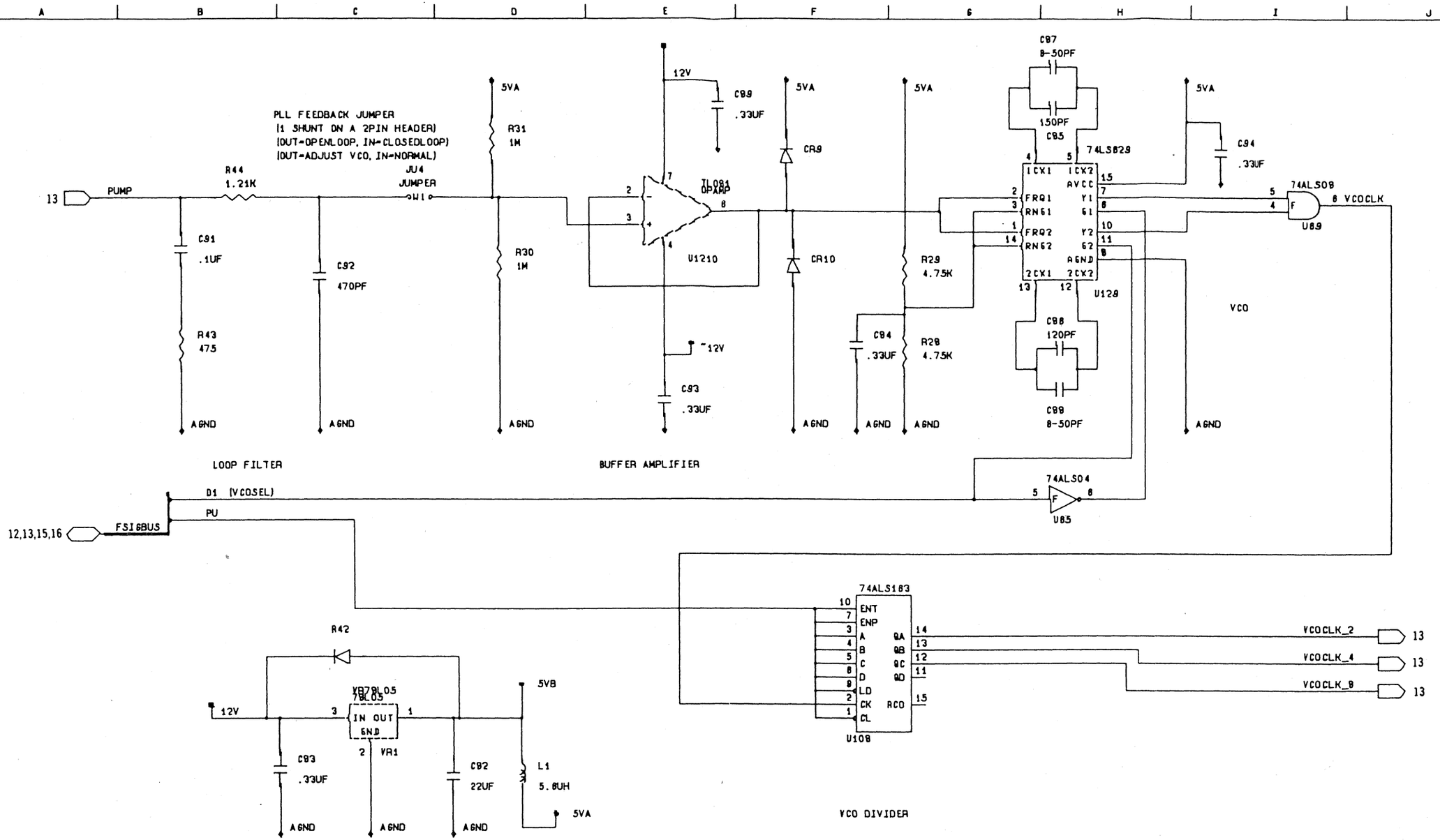
11 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 FLOPPY BLOCK DIGRAM



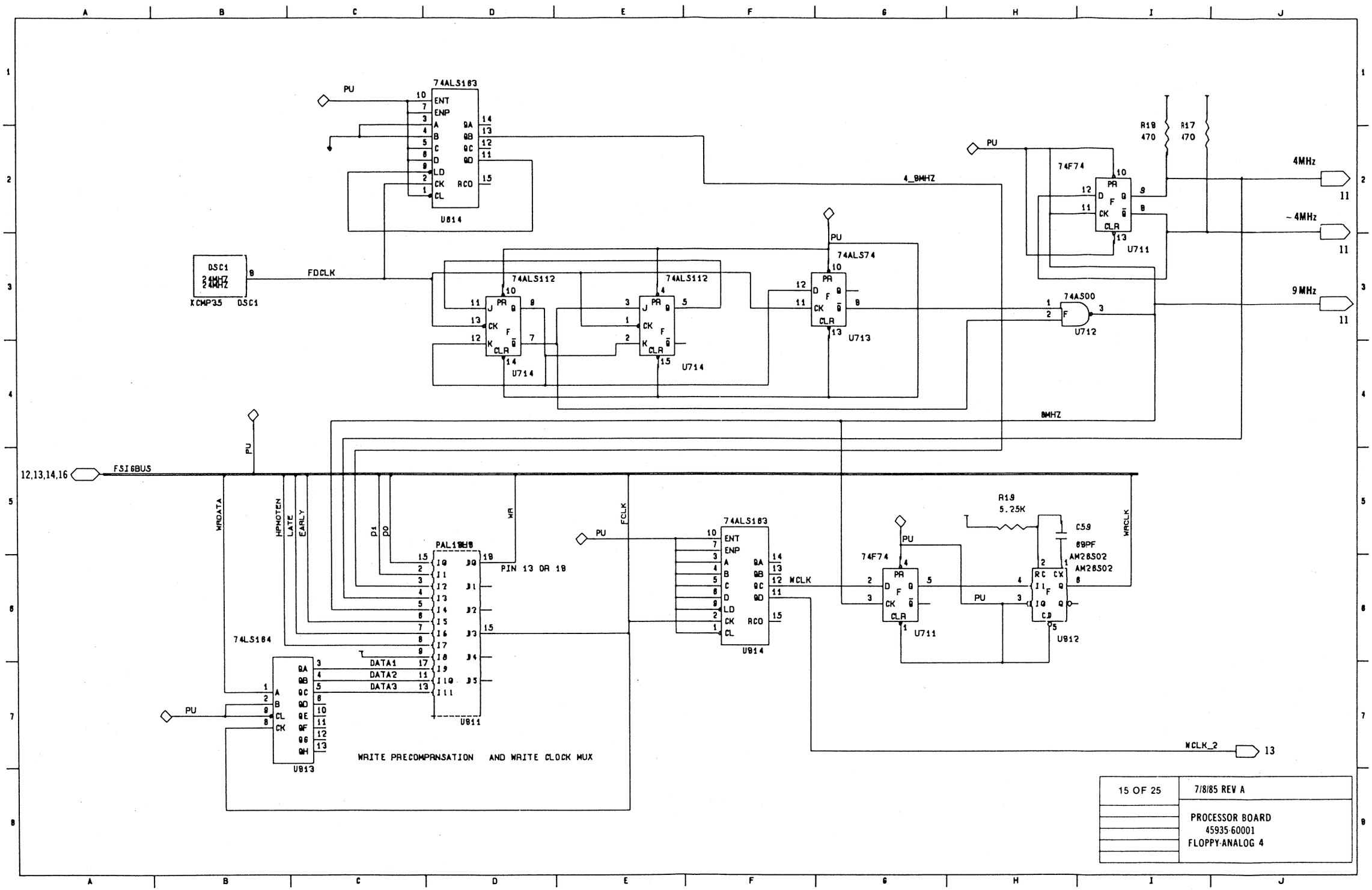
12 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 FLOPPY-ANALOG 1

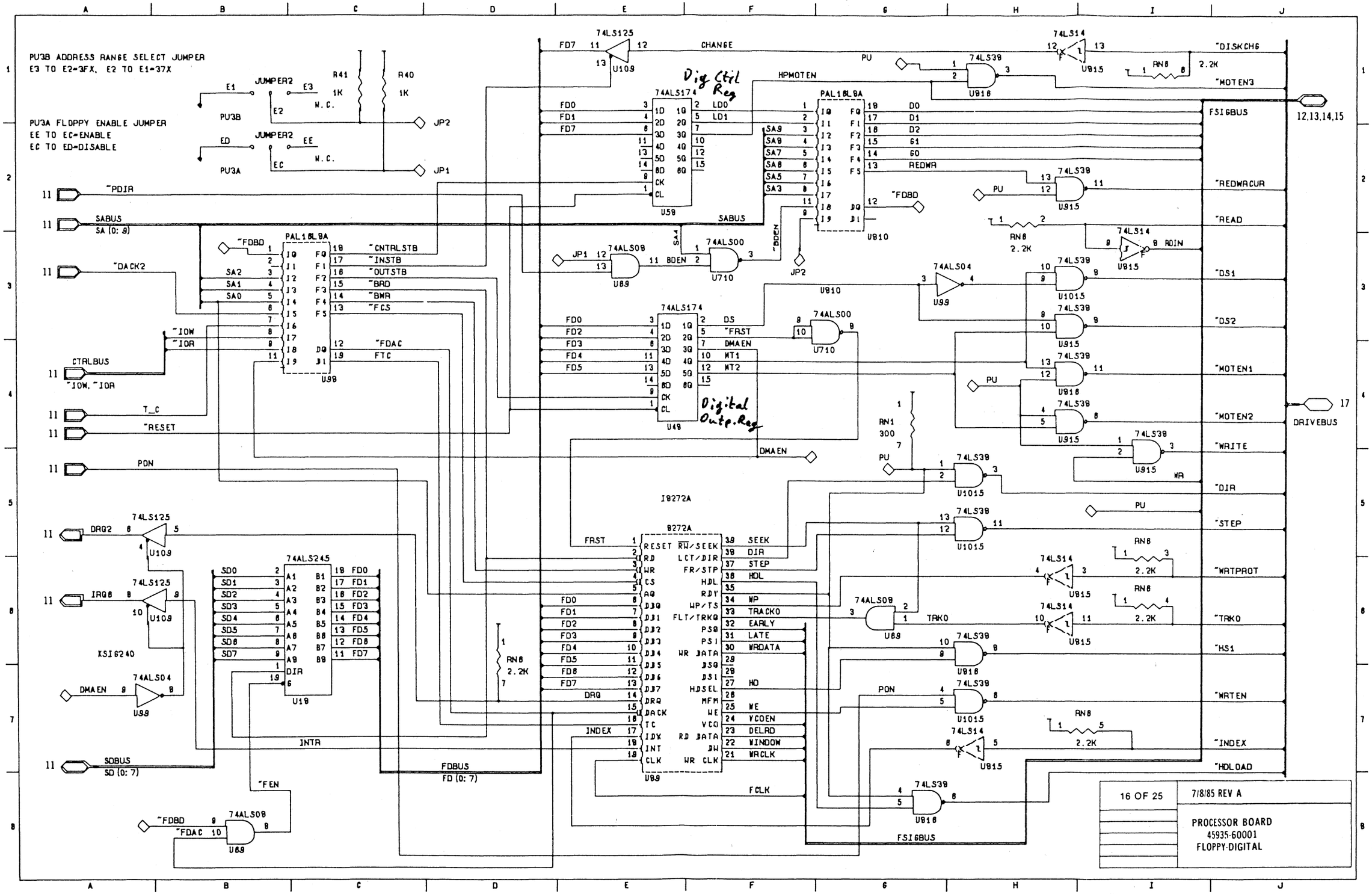


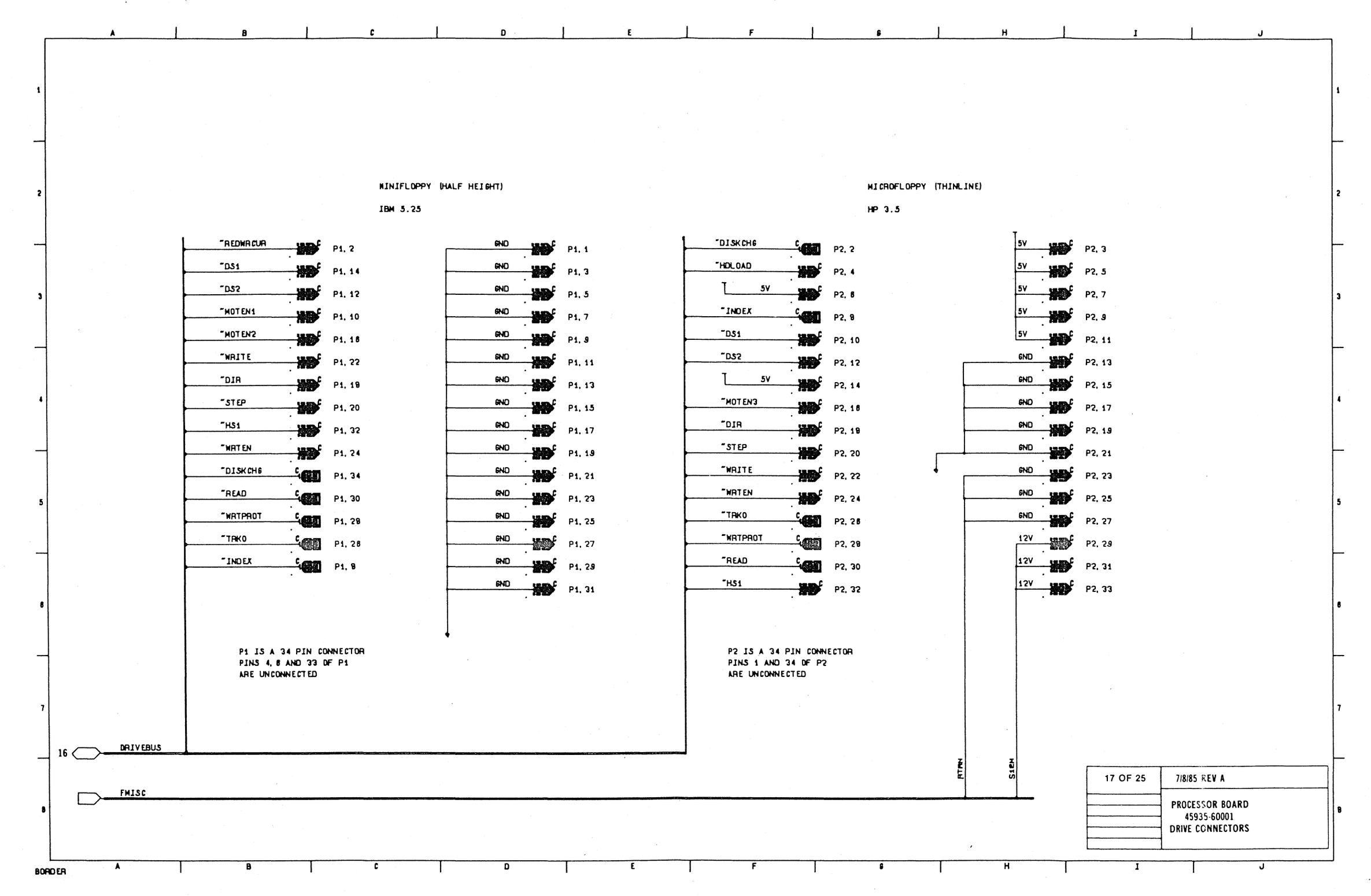
13 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 FLOPPY-ANALOG 2

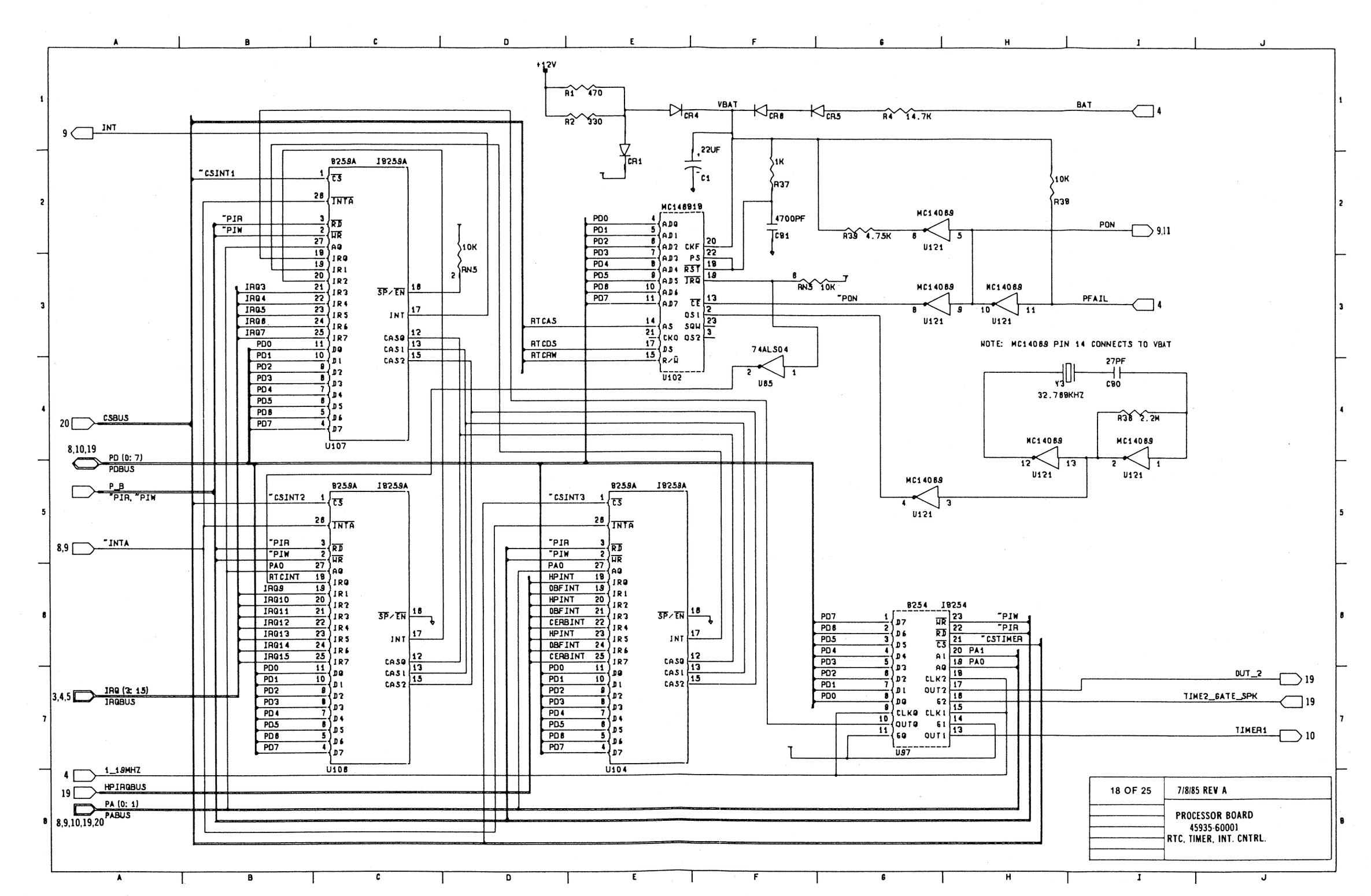


14 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 FLOPPY-ANALOG 3

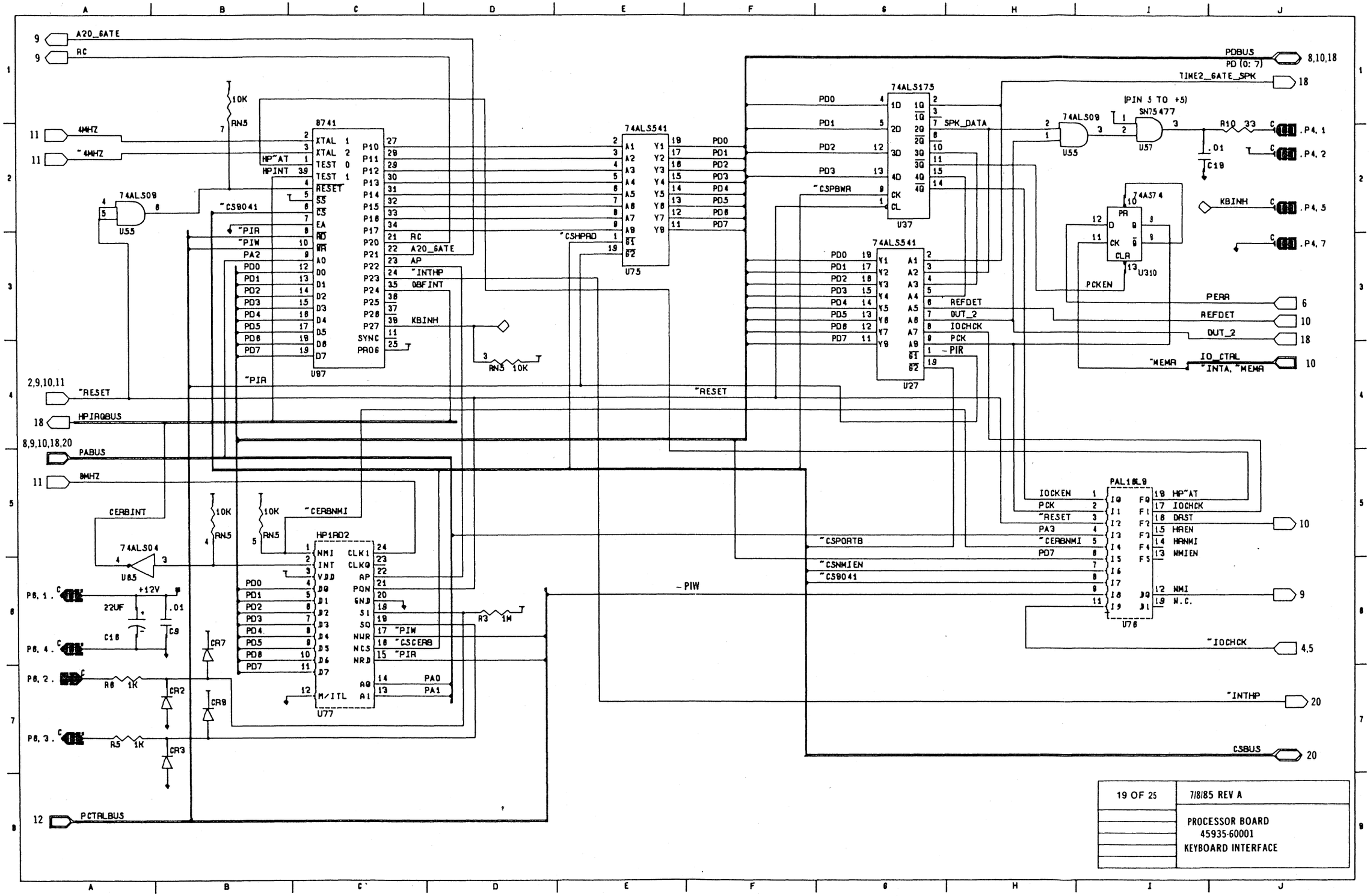

74ALS163
U814
PU
FDCLK
OSC1
24MHZ
XCMP35
74ALS112
U714
74ALS74
U713
74F74
U711
74AS00
U712
R18
470
R17
470
4_8MHZ
8MHZ
4MHz
~4MHz
9MHz
11
12,13,14,16
FSI6BUS
WRDATA
HPMOTEN
LATE
EARLY
WR
FCLK
WCLK
PAL16R8
PIN 13 OR 18
74LS164
DATA1
DATA2
DATA3
U811
U813
R19
5.25K
C59
68PF
AM26S02
U812
WCLK_2
13
WRITE PRECOMPRNSATION AND WRITE CLOCK MUX
15 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
FLOPPY-ANALOG 4

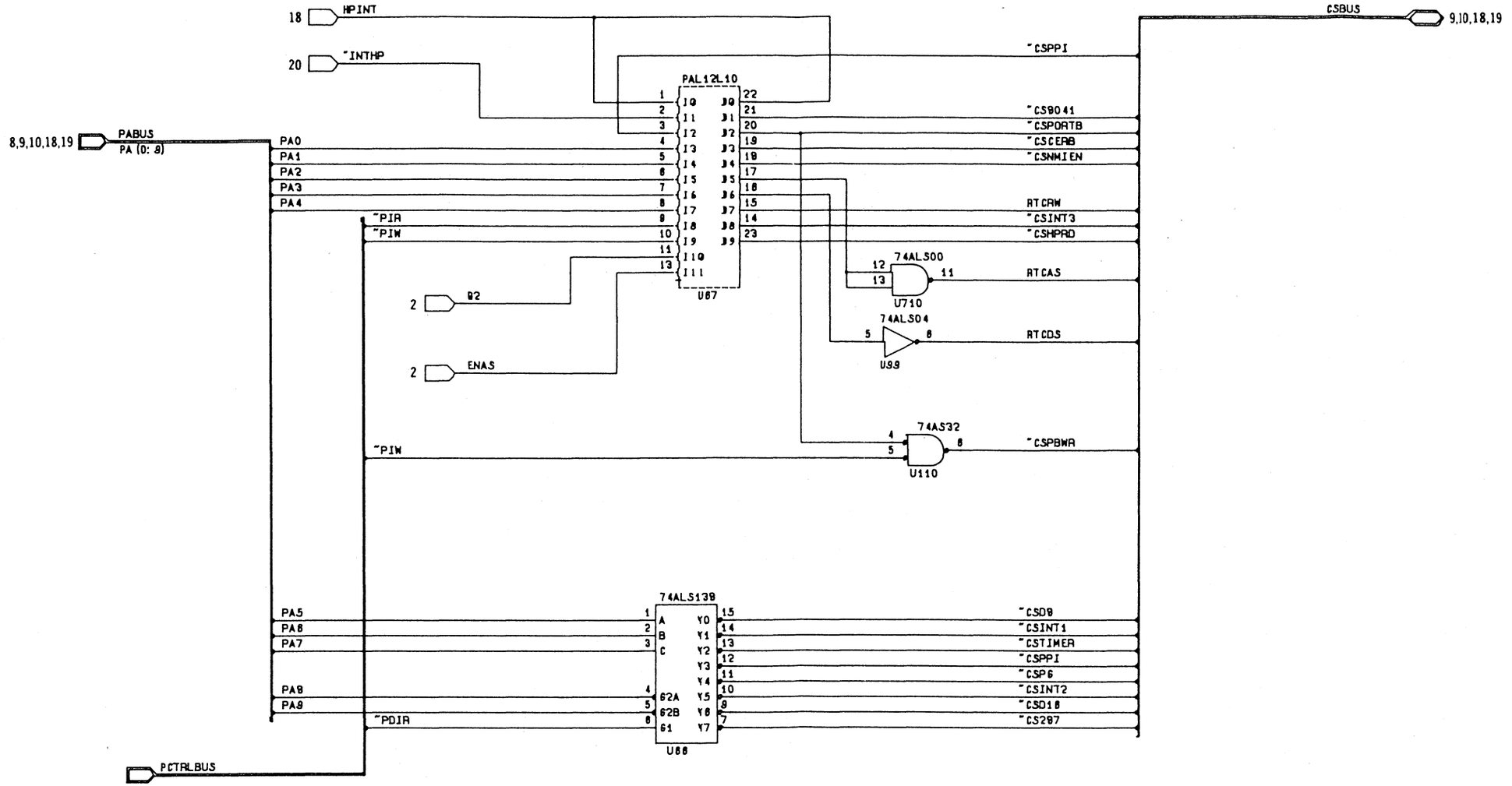

PU3B ADDRESS RANGE SELECT JUMPER
E3 TO E2=3FX, E2 TO E1=37X
PU3A FLOPPY ENABLE JUMPER
EE TO EC=ENABLE
EC TO ED=DISABLE
JUMPER2
R41 1K
R40 1K
N.C.
JP2
JP1
Dig Ctrl Reg
Digital Outp.Reg
74LS125
74LS174
PAL16L8A
74LS38
74LS14
74LS08
74LS00
74LS04
74LS245
8272A
I8272A
RN8 2.2K
RN1 300
SABUS
SA (0: 9)
SDBUS
SD (0: 7)
FDBUS
FD (0: 7)
FSI6BUS
DRIVEBUS
CTRLBUS
"IOW, "IOR
"DISKCH6
"MOTEN3
"REDWACUR
"READ
"DS1
"DS2
"MOTEN1
"MOTEN2
"WRITE
"DIR
"STEP
"WRTPROT
"TRK0
"HS1
"WRTEN
"INDEX
"HDLOAD
12,13,14,15
17
16 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
FLOPPY-DIGITAL


MINIFLOPPY (HALF HEIGHT)
IBM 5.25
~REDWRCUR P1, 2
~DS1 P1, 14
~DS2 P1, 12
~MOTEN1 P1, 10
~MOTEN2 P1, 16
~WRITE P1, 22
~DIR P1, 18
~STEP P1, 20
~HS1 P1, 32
~WRTEN P1, 24
~DISKCH6 P1, 34
~READ P1, 30
~WRTPROT P1, 28
~TRK0 P1, 26
~INDEX P1, 8
GND P1, 1
GND P1, 3
GND P1, 5
GND P1, 7
GND P1, 9
GND P1, 11
GND P1, 13
GND P1, 15
GND P1, 17
GND P1, 19
GND P1, 21
GND P1, 23
GND P1, 25
GND P1, 27
GND P1, 29
GND P1, 31
P1 IS A 34 PIN CONNECTOR
PINS 4, 6 AND 33 OF P1
ARE UNCONNECTED
MICROFLOPPY (THINLINE)
HP 3.5
~DISKCH6 P2, 2
~HDLOAD P2, 4
5V P2, 6
~INDEX P2, 8
~DS1 P2, 10
~DS2 P2, 12
5V P2, 14
~MOTEN3 P2, 16
~DIR P2, 18
~STEP P2, 20
~WRITE P2, 22
~WRTEN P2, 24
~TRK0 P2, 26
~WRTPROT P2, 28
~READ P2, 30
~HS1 P2, 32
5V P2, 3
5V P2, 5
5V P2, 7
5V P2, 9
5V P2, 11
GND P2, 13
GND P2, 15
GND P2, 17
GND P2, 19
GND P2, 21
GND P2, 23
GND P2, 25
GND P2, 27
12V P2, 29
12V P2, 31
12V P2, 33
P2 IS A 34 PIN CONNECTOR
PINS 1 AND 34 OF P2
ARE UNCONNECTED
16
DRIVEBUS
FMISC
RTRN
S12V
17 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
DRIVE CONNECTORS
BORDER

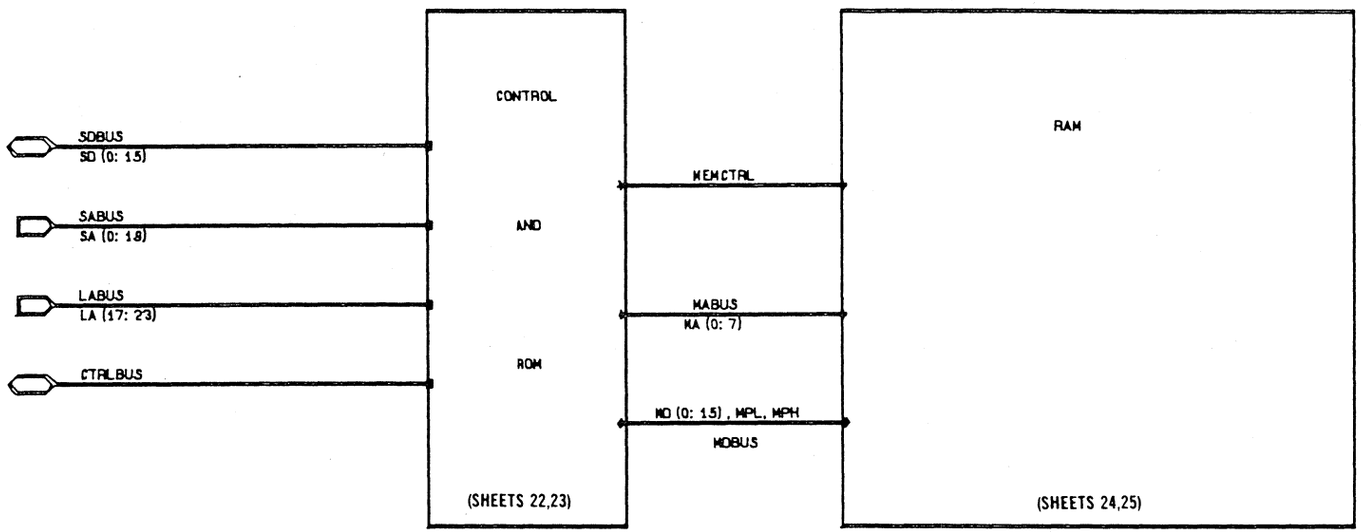


18 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 RTC, TIMER, INT. CNTRL.

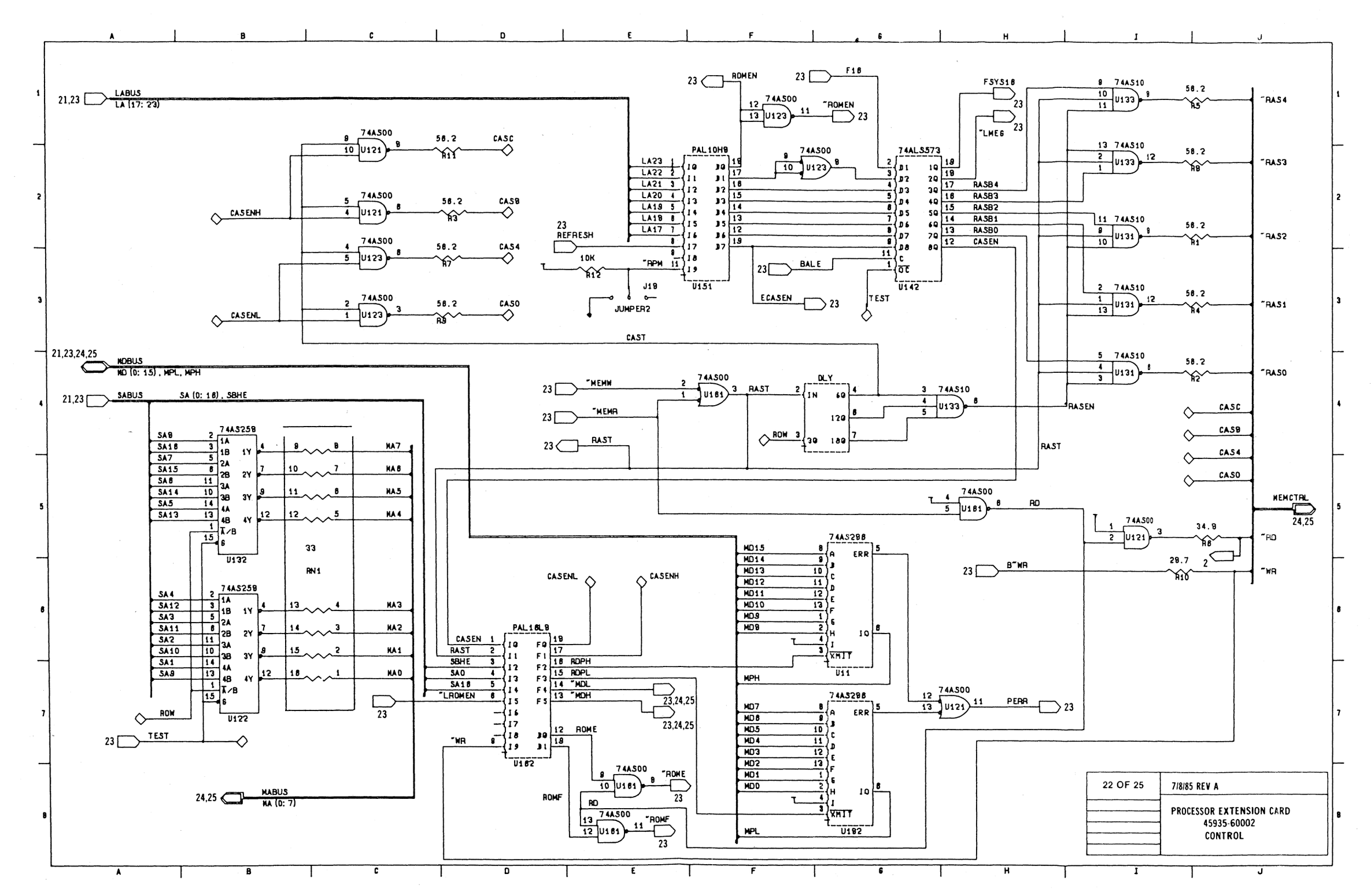

A20_GATE
RC
4MHZ
~4MHZ
8741
74ALS509
U55
~CS8041
~PIR
~PIW
PA2
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
~RESET
HPIRQBUS
PABUS
8MHZ
CERBINT
74ALS04
U85
HP1RD2
U77
~CERBNMI
~INTHP
OBFINT
KBINH
74ALS541
U75
~CSHPRD
74ALS175
U37
~CSPBWR
SPK_DATA
74ALS541
U27
REFDET
OUT_2
IOCHCK
PCK
PDBUS
PD(0:7)
TIME2_GATE_SPK
(PIN 5 TO +5)
74ALS08
U55
SN75477
U57
R10 33
.01
C19
.P4, 1
.P4, 2
74A374
U310
KBINH
.P4, 5
.P4, 7
PCKEN
PERR
REFDET
OUT_2
~MEMR
IO_CTRL
~INTA, ~MEMR
PAL16L8
U76
IOCKEN
PCK
~RESET
PA3
~CERBNMI
PD7
~CSPORTB
~CSNMIEN
~CS8041
~PIW
~IOCHCK
~INTHP
CSBUS
HP~AT
IOCHCK
DRST
HREN
HRNMI
NMIEN
NMI
N.C.
22UF
C18
C9
+12V
CR7
CR2
CR8
CR3
R8 1K
R5 1K
R3 1M
PB.1
PB.4
PB.2
PB.3
PCTRLBUS
19 OF 25
7/8/85 REV A
PROCESSOR BOARD
45935-60001
KEYBOARD INTERFACE

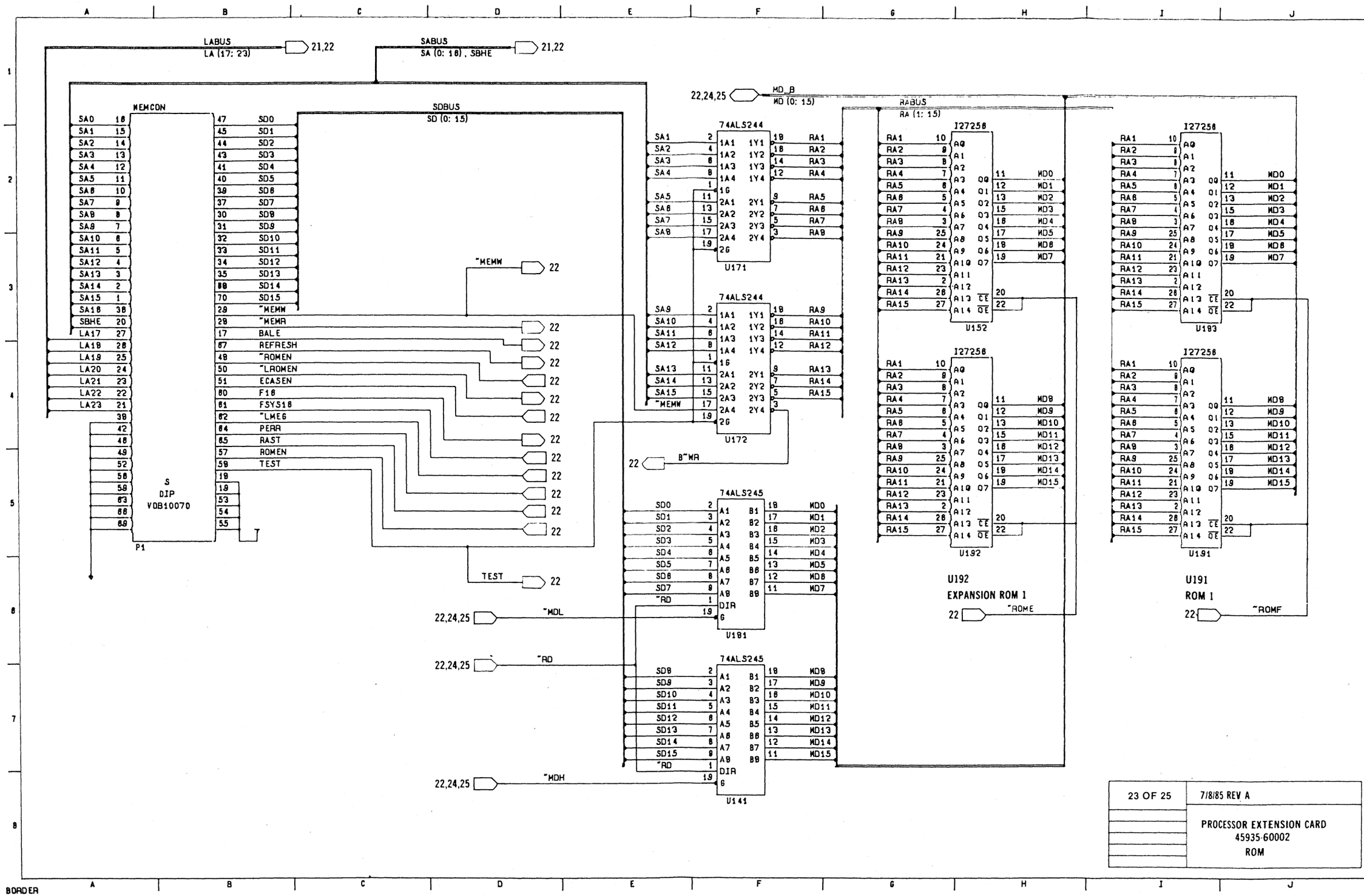


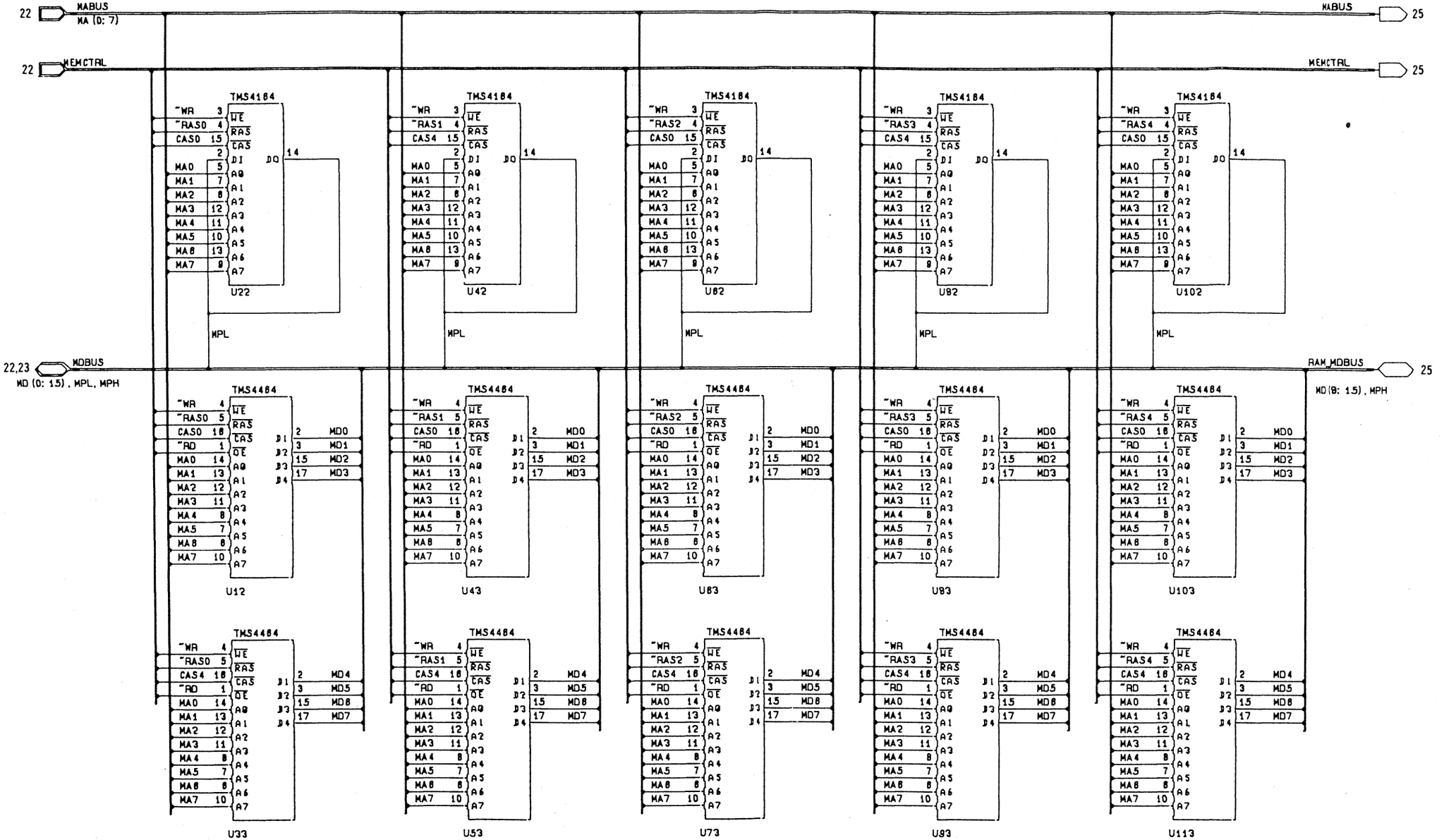
20 OF 25	7/8/85 REV A
	PROCESSOR BOARD 45935-60001 CHIP SELECTS

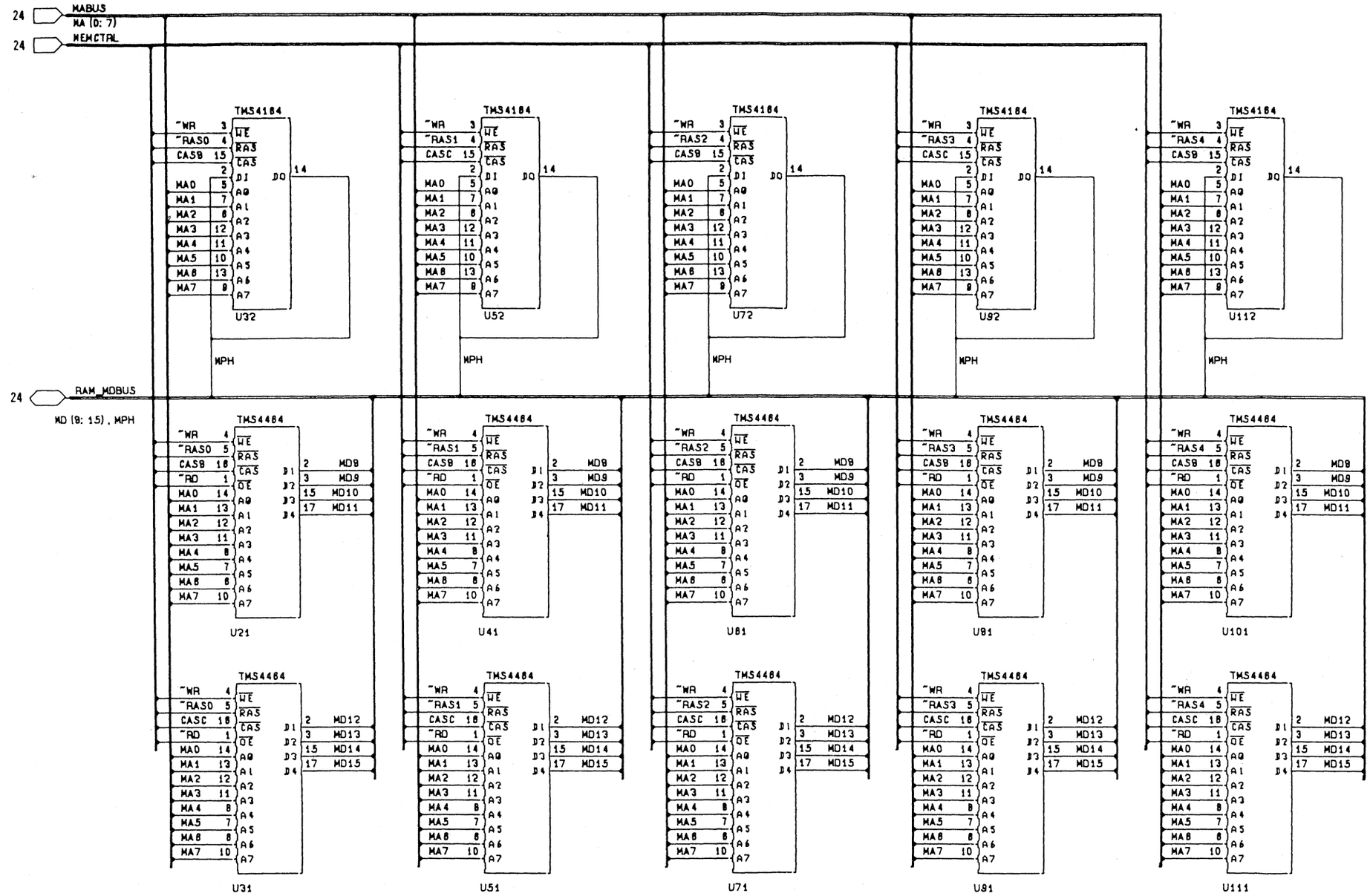


21 OF 25	7/8/85 REV A
	PROCESSOR EXTENSION CARD 45935-60002 BLOCK DIAGRAM

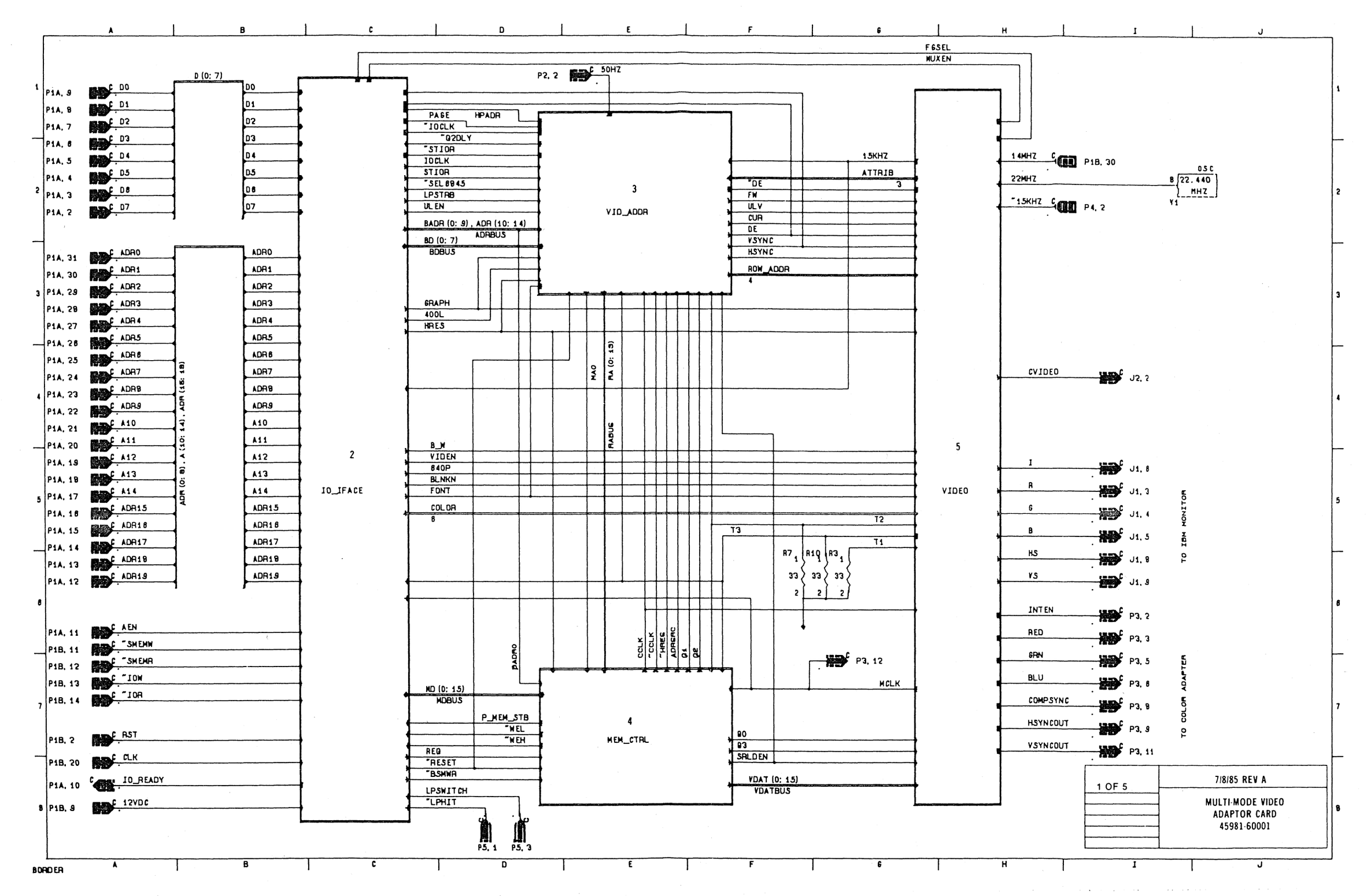

21,23 LABUS LA (17: 23)
21,23,24,25 MDBUS MD (0: 15), MPL, MPH
21,23 SABUS SA (0: 18), SBHE
24,25 MABUS MA (0: 7)
74AS00 U121 R11 CASC
74AS00 U121 R3 CASB
74AS00 U123 R7 CAS4
74AS00 U123 R9 CAS0
CASENH
CASENL
23 REFRESH
10K R12
J19 JUMPER2
PAL10H8 U151
LA23 LA22 LA21 LA20 LA19 LA18 LA17
23 RDMEN
74AS00 U123 "ROMEN 23
74AS00 U123
23 F16
74ALS573 U142
23 BALE
ECASEN 23
TEST
FSYS16 23
"LME6 23
RASB4 RASB3 RASB2 RASB1 RASB0 CASEN
74AS10 U133 58.2 R5 "RAS4
74AS10 U133 58.2 R8 "RAS3
74AS10 U131 58.2 R1 "RAS2
74AS10 U131 58.2 R4 "RAS1
74AS10 U131 58.2 R2 "RAS0
RASEN
RAST
CAST
CASC CASB CAS4 CAS0
MEMCTRL 24,25
23 "MEMW
23 "MEMR
23 RAST
74AS00 U181 RAST
DLY ROW
74AS10 U133
74AS00 U181 RD
74AS00 U121 34.8 R6 "RD
28.7 R10 "WR
23 B"WR
74AS258 U132
74AS258 U122
SA9 SA16 SA7 SA15 SA8 SA14 SA5 SA13
SA4 SA12 SA3 SA11 SA2 SA10 SA1 SA9
33 RN1
MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0
ROW
23 TEST
PAL16L8 U162
CASEN RAST SBHE SA0 SA18 "LROMEN "WR
RDPH RDPL "MDL "MDH ROME
23,24,25
74AS00 U161 "ROME 23
ROMF
74AS00 U161 "ROMF 23
74AS298 U11
74AS298 U182
MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0
ERR XMIT IO
MPH MPL
74AS00 U121 PERR 23
22 OF 25
7/8/85 REV A
PROCESSOR EXTENSION CARD
45935-60002
CONTROL

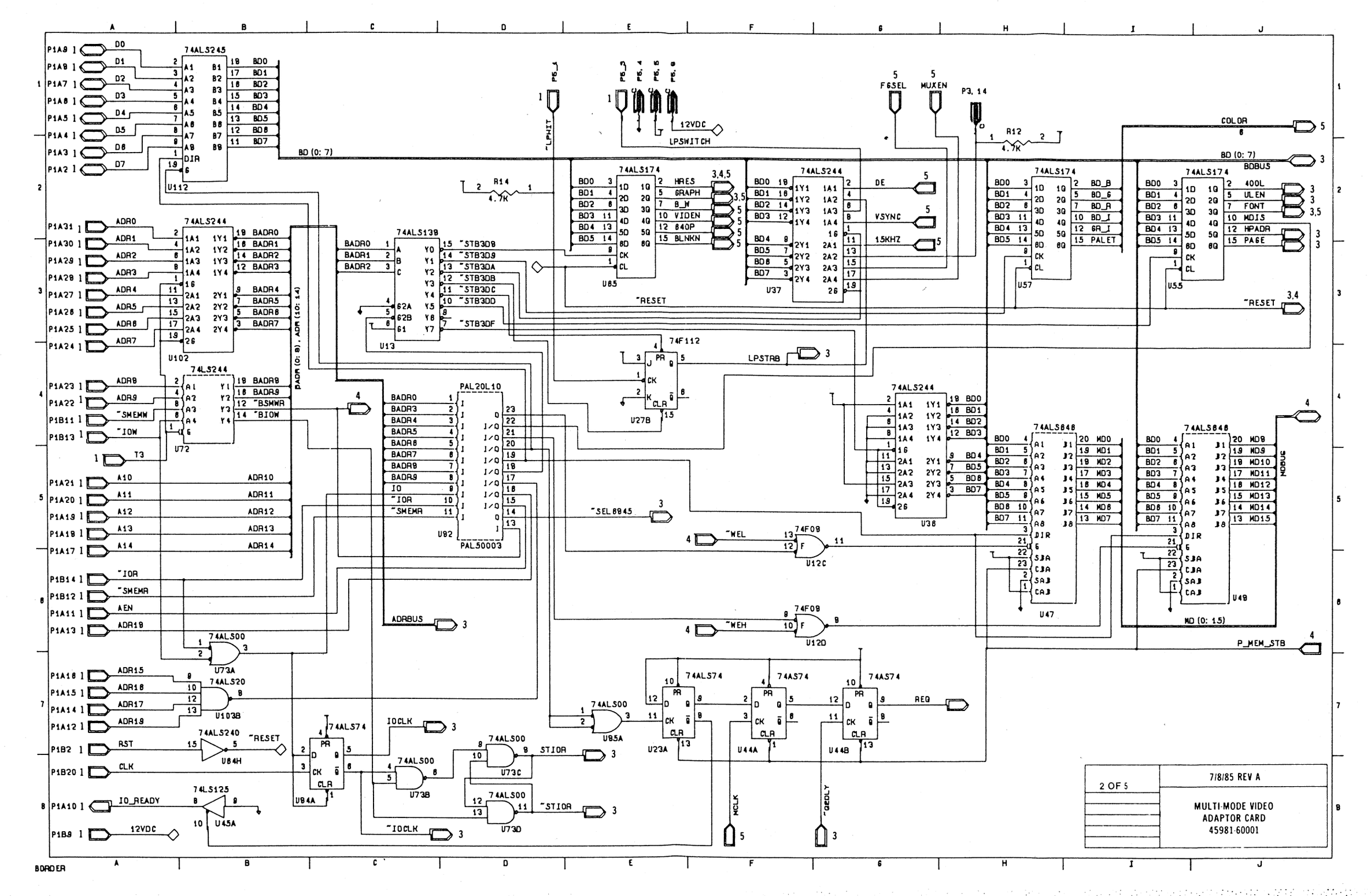

LABUS
LA (17: 23)
21,22
SABUS
SA (0: 18), SBHE
21,22
MEMCON
SDBUS
SD (0: 15)
22,24,25
MD_B
MD (0: 15)
RABUS
RA (1: 15)
S
DIP
VDB10070
P1
74ALS244
U171
U172
74ALS245
U181
U141
I27256
U152
U192
U193
U191
U192
EXPANSION ROM 1
U191
ROM 1
~MEMW
~MEMR
BALE
REFRESH
~ROMEN
~LROMEN
ECASEN
F16
FSYS16
~LMEG
PERR
RAST
ROMEN
TEST
B~WR
~MDL
~RD
~MDH
~ROME
~ROMF
23 OF 25
7/8/85 REV A
PROCESSOR EXTENSION CARD
45935-60002
ROM
BORDER

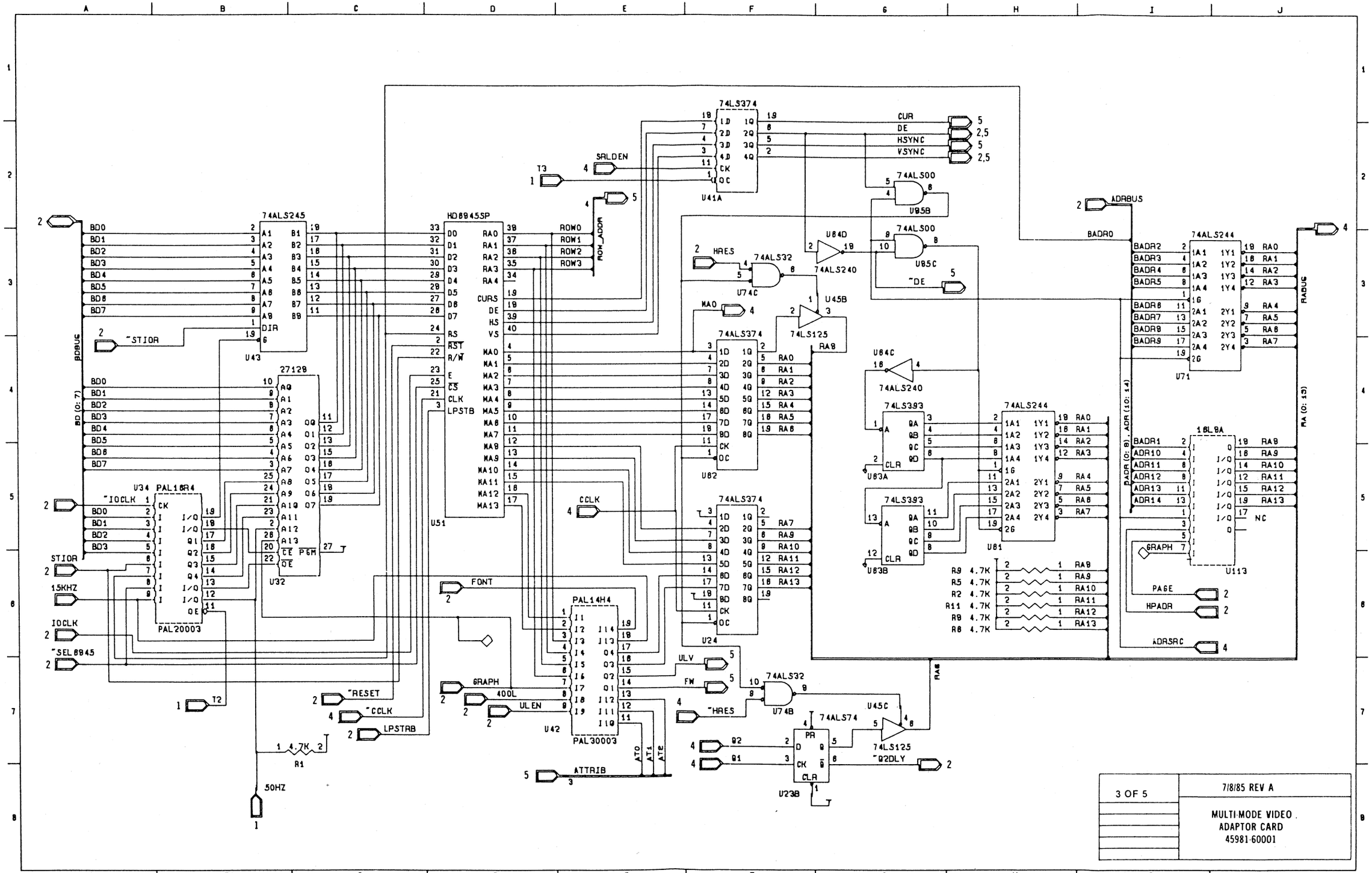

22 MABUS MA (0: 7)
MABUS 25
22 MEMCTRL
MEMCTRL 25
TMS4164
~WR 3
~RAS0 4
CAS0 15
MA0 5
MA1 7
MA2 8
MA3 12
MA4 11
MA5 10
MA6 13
MA7 9
WE
RAS
CAS
DI
DO
14
A0
A1
A2
A3
A4
A5
A6
A7
U22
~RAS1 4
CAS4 15
U42
~RAS2 4
CAS0 15
U82
~RAS3 4
CAS4 15
U92
~RAS4 4
CAS0 15
U102
MPL
22,23 MDBUS
MD (0: 15), MPL, MPH
RAM_MDBUS 25
MD (0: 15), MPH
TMS4464
~WR 4
~RAS0 5
CAS0 16
~RD 1
MA0 14
MA1 13
MA2 12
MA3 11
MA4 8
MA5 7
MA6 6
MA7 10
OE
D1
D2
D3
D4
2 MD0
3 MD1
15 MD2
17 MD3
U12
~RAS1 5
CAS4 16
U43
~RAS2 5
CAS4 16
U83
~RAS3 5
CAS4 16
U93
~RAS4 5
CAS4 16
U103
2 MD4
3 MD5
15 MD6
17 MD7
U33
U53
U73
U93
U113
SOCKETS ON 45935-60002
24 OF 25
7/8/85 REV A
PROCESSOR EXTENSION CARD
45935-60002
RAM (LO BYTE)



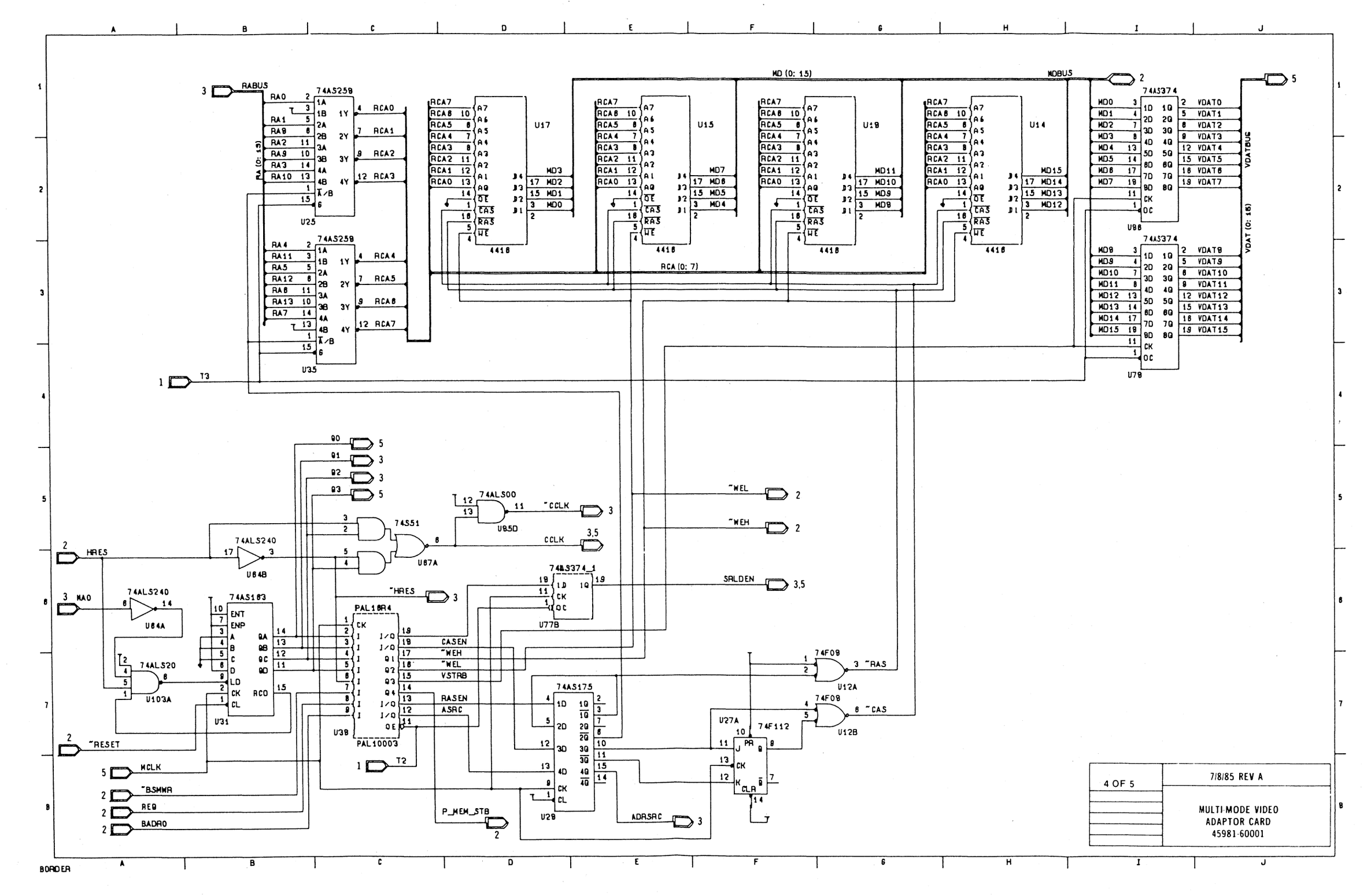
25 OF 25	7/8/85 REV A
	PROCESSOR EXTENSION CARD 45935-60002 RAM (HIGH BYTE)


FGSEL
MUXEN
P2, 2
50HZ
D (0: 7)
P1A, 9 D0
P1A, 8 D1
P1A, 7 D2
P1A, 6 D3
P1A, 5 D4
P1A, 4 D5
P1A, 3 D6
P1A, 2 D7
P1A, 31 ADR0
P1A, 30 ADR1
P1A, 29 ADR2
P1A, 28 ADR3
P1A, 27 ADR4
P1A, 26 ADR5
P1A, 25 ADR6
P1A, 24 ADR7
P1A, 23 ADR8
P1A, 22 ADR9
P1A, 21 A10
P1A, 20 A11
P1A, 19 A12
P1A, 18 A13
P1A, 17 A14
P1A, 16 ADR15
P1A, 15 ADR16
P1A, 14 ADR17
P1A, 13 ADR18
P1A, 12 ADR19
ADR (0: 8) , A (10: 14) , ADR (15: 19)
P1A, 11 AEN
P1B, 11 ~SMEMW
P1B, 12 ~SMEMR
P1B, 13 ~IOW
P1B, 14 ~IOR
P1B, 2 RST
P1B, 20 CLK
P1A, 10 IO_READY
P1B, 9 12VDC
2
IO_IFACE
PAGE HPADR
~IOCLK
~Q2DLY
~STIOR
IOCLK
STIOR
~SEL8845
LPSTRB
ULEN
BADR (0: 9) , ADR (10: 14)
ADRBUS
BD (0: 7)
BDBUS
GRAPH
400L
HRES
B_W
VIDEN
640P
BLNKN
FONT
COLOR
6
3
VID_ADDR
~DE
FW
ULV
CUR
DE
VSYNC
HSYNC
ROW_ADDR
4
15KHZ
ATTRIB
3
MA0
RA (0: 13)
RABUS
T2
T3
T1
R7 1 33 2
R10 1 33 2
R3 1 33 2
CCLK
~CCLK
~THREG
ADRSEL
Q1
Q2
P3, 12
MCLK
PADRO
MD (0: 15)
MDBUS
P_MEM_STB
~WEL
~WEH
REQ
~RESET
~BSMWR
LPSWITCH
~LPHIT
P5, 1
P5, 3
4
MEM_CTRL
Q0
Q3
SRLDEN
VDAT (0: 15)
VDATBUS
5
VIDEO
14MHZ
P1B, 30
22MHZ
OSC
22.440 MHZ
Y1
~15KHZ
P4, 2
CVIDEO
J2, 2
I J1, 6
R J1, 3
G J1, 4
B J1, 5
HS J1, 8
VS J1, 9
TO IBM MONITOR
INTEN P3, 2
RED P3, 3
GRN P3, 5
BLU P3, 6
COMPSYNC P3, 8
HSYNCOUT P3, 9
VSYNCOUT P3, 11
TO COLOR ADAPTER
1 OF 5
7/8/85 REV A
MULTI-MODE VIDEO
ADAPTOR CARD
45981-60001
BORDER


74ALS245
U112
74ALS244
U102
74ALS244
U72
74ALS139
U13
74ALS174
U85
74ALS244
U37
74F112
U27B
PAL20L10
PAL50003
U82
74ALS174
U57
74ALS174
U55
74ALS244
U38
74ALS648
U47
74ALS648
U48
74ALS00
U73A
74ALS20
U103B
74ALS240
U84H
74ALS74
U84A
74ALS125
U45A
74ALS00
U73B
74ALS00
U73C
74ALS00
U73D
74ALS00
U85A
74ALS74
U23A
74AS74
U44A
74AS74
U44B
74F08
U12C
74F08
U12D
R14
4.7K
R12
4.7K
BD (0: 7)
BDBUS
MDBUS
MD (0: 15)
ADRBUS
BADR (0: 8), ADR (10: 14)
12VDC
LPSWITCH
~LPHIT
F6SEL
MUXEN
P3, 14
COLOR
~RESET
LPSTRB
~SEL8845
~WEL
~WEH
P_MEM_STB
REQ
MCLK
~QEDLY
~STIOR
~IOCLK
IOCLK
STIOR
HRES
GRAPH
B_W
VIDEN
640P
BLNKN
DE
VSYNC
15KHZ
400L
ULEN
FONT
MDIS
HPADR
PAGE
BD_B
BD_G
BD_R
BD_I
GR_I
PALET
~STB3D8
~STB3D9
~STB3DA
~STB3DB
~STB3DC
~STB3DD
~STB3DF
~IOR
~SMEMR
~SMEMW
~IOW
AEN
RST
CLK
IO_READY
T3
2 OF 5
7/8/85 REV A
MULTI-MODE VIDEO
ADAPTOR CARD
45981-60001
BORDER

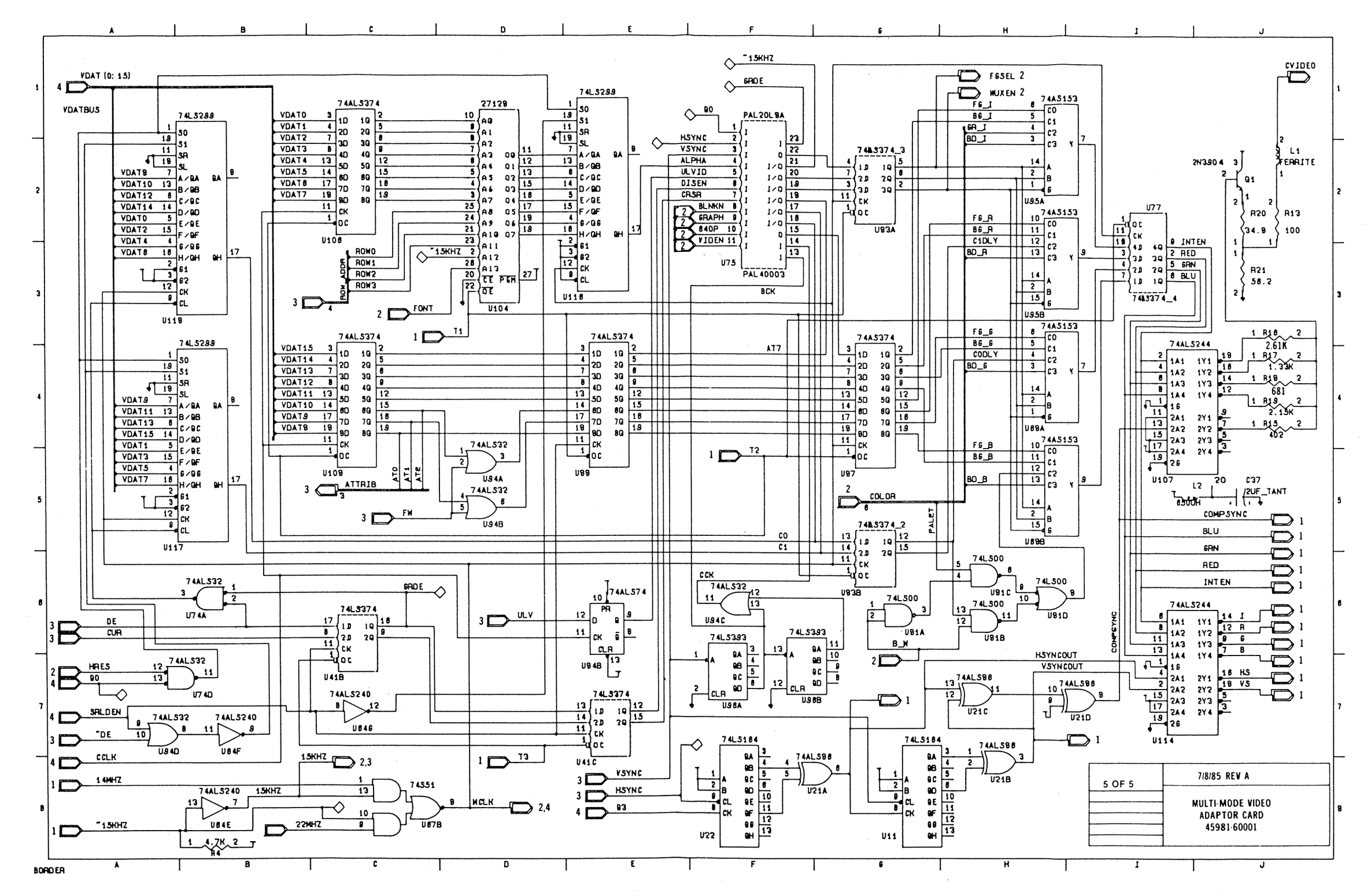


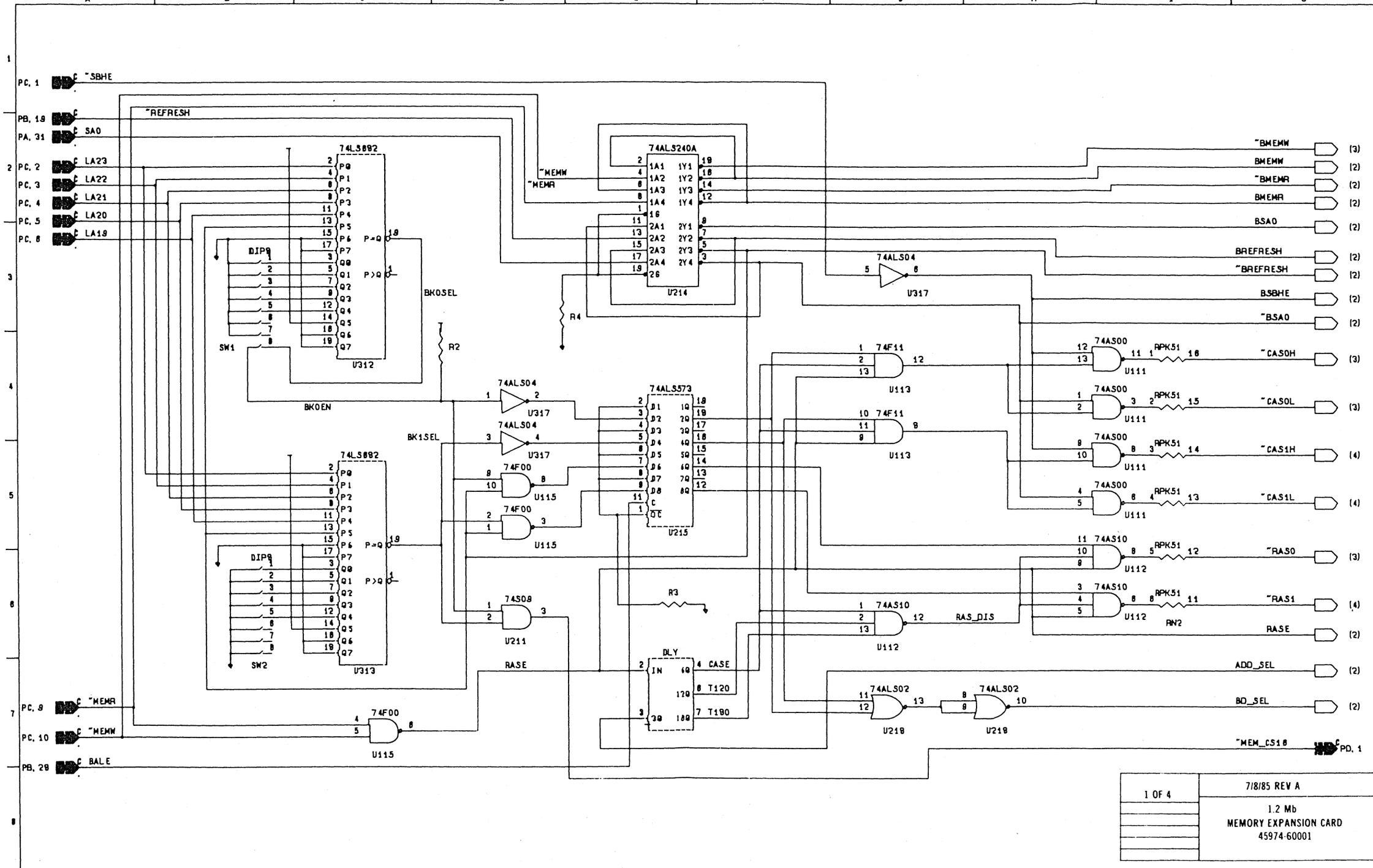
3 OF 5	7/8/85 REV A
	MULTI-MODE VIDEO ADAPTOR CARD 45981-60001



4 OF 5	7/8/85 REV A
	MULTI-MODE VIDEO ADAPTOR CARD 45981-60001

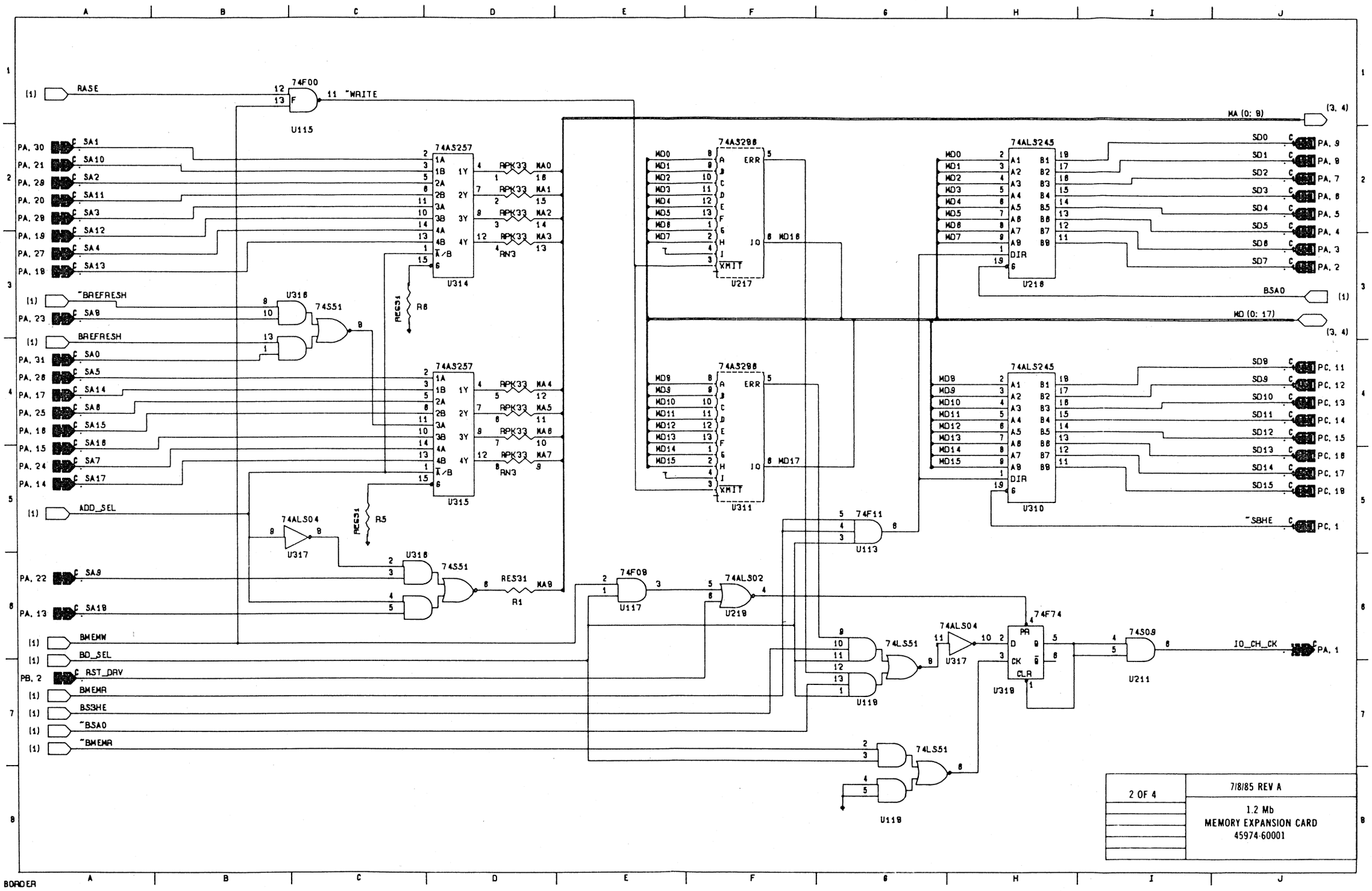
BORDER

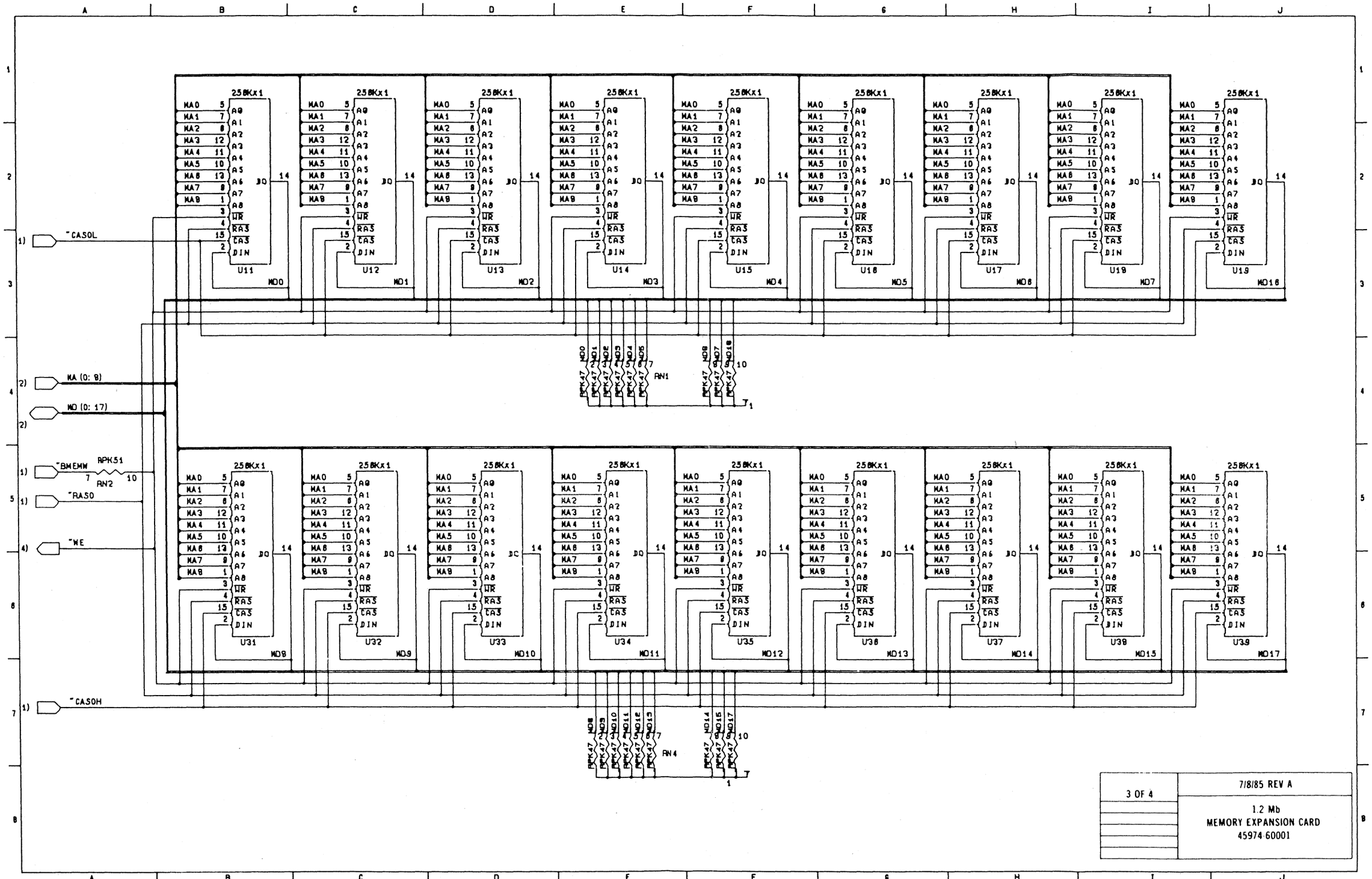

VDAT (0: 15)
VDATBUS
74LS299
74ALS374
27128
PAL20L8A
PAL40003
74AS153
74ALS244
74ALS32
74ALS240
74ALS74
74ALS393
74ALS00
74ALS86
74ALS164
74S51
~15KHZ
GRDE
HSYNC
VSYNC
ALPHA
ULVID
DISEN
CRSR
BLNKN
GRAPH
640P
VIDEN
FONT
ATTRIB
FW
COLOR
CCK
DE
CUR
HRES
SRLDEN
CCLK
14MHZ
22MHZ
MCLK
ULV
F6SEL 2
MUXEN 2
CVIDEO
L1
FERRITE
2N3904
Q1
R20
34.8
R13
100
R21
58.2
INTEN
RED
GRN
BLU
COMPSYNC
HSYNCOUT
VSYNCOUT
HS
VS
2.61K
1.33K
681
2.15K
402
6300H
/2UF_TANT
5 OF 5
7/8/85 REV A
MULTI-MODE VIDEO
ADAPTOR CARD
45981-60001
BORDER



1 OF 4	7/8/85 REV A
	1.2 Mb MEMORY EXPANSION CARD 45974-60001

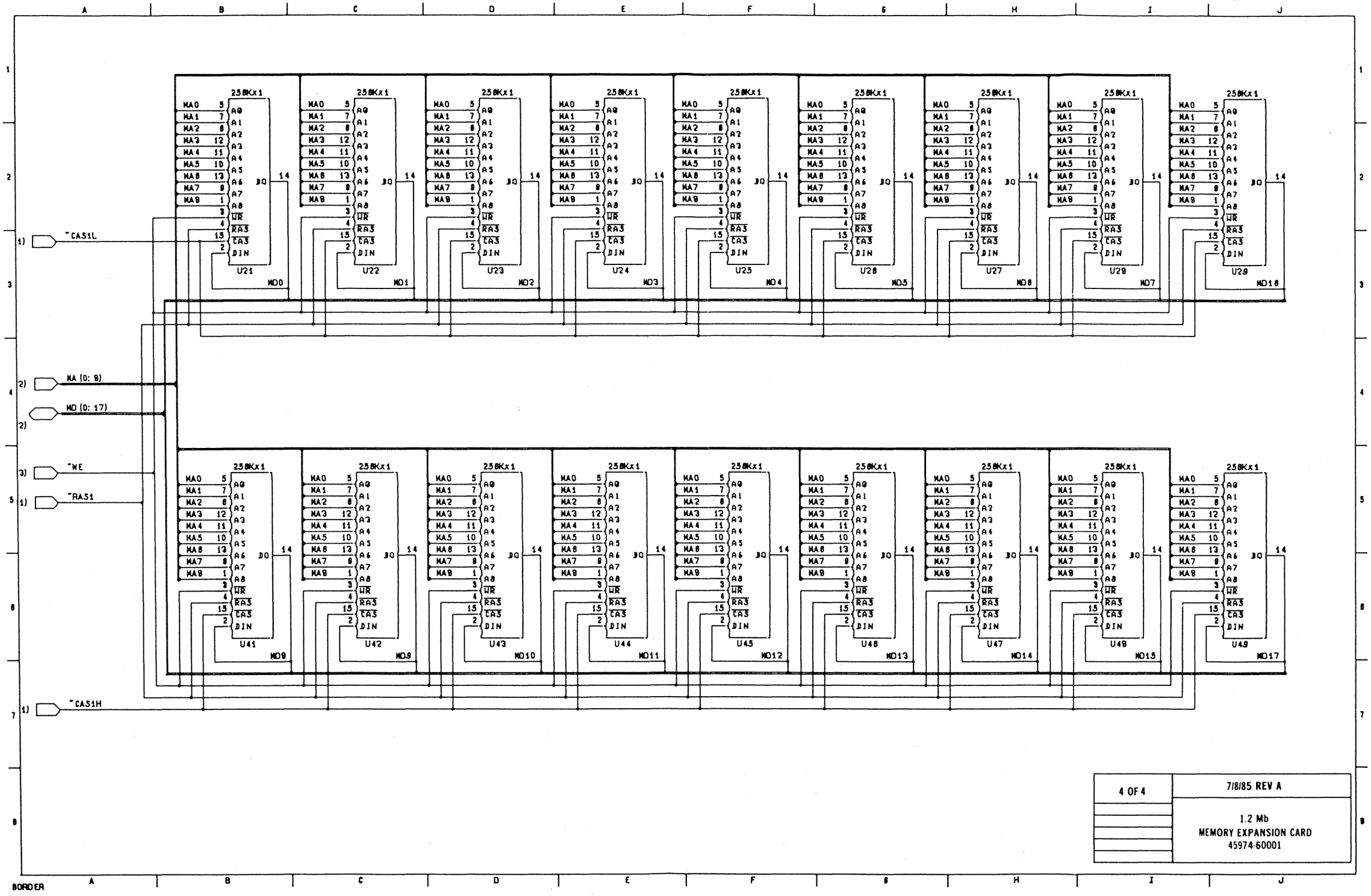
BORDER

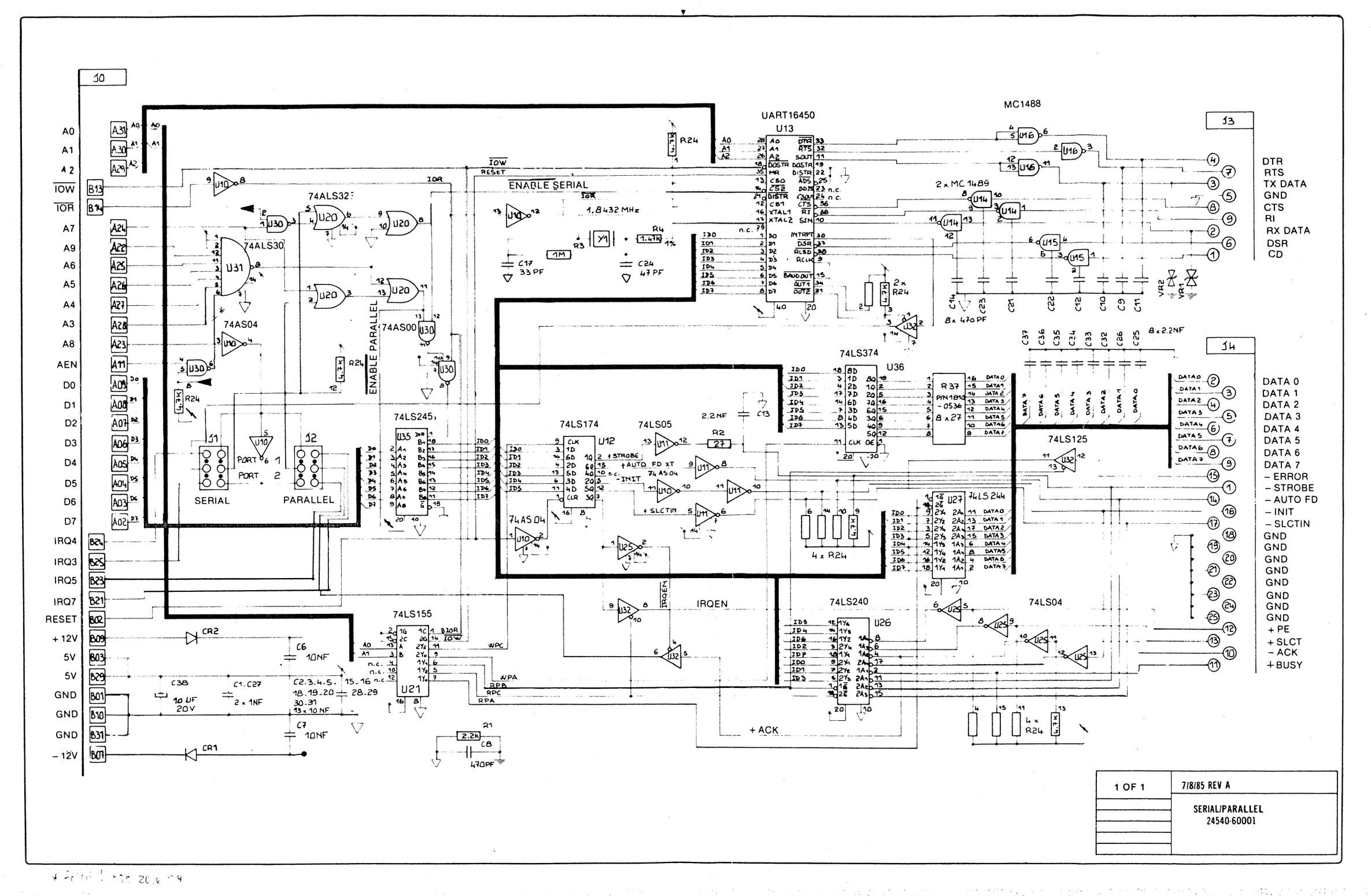

RASE
74F00
U115
~WRITE
MA (0: 8)
(3, 4)
74AS257
U314
U315
RPK33
RN3
RES31
R6
R5
R1
~BREFRESH
BREFRESH
U316
74S51
U317
74ALS04
U318
ADD_SEL
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
74AS288
U217
U311
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
ERR
XMIT
74ALS245
U218
U310
DIR
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
PA. 9
PA. 8
PA. 7
PA. 6
PA. 5
PA. 4
PA. 3
PA. 2
PC. 11
PC. 12
PC. 13
PC. 14
PC. 15
PC. 16
PC. 17
PC. 18
BSA0
(1)
WD (0: 17)
~SBHE
PC. 1
74F11
U113
74F09
U117
74ALS02
U218
74LS51
U118
74F74
74S09
U211
IO_CH_CK
PA. 1
BMEMW
BD_SEL
RST_DRV
PB. 2
BMEMR
BSSHE
~BSAO
~BMEMR
PA. 22
PA. 13
PA. 30
PA. 21
PA. 29
PA. 20
PA. 28
PA. 19
PA. 27
PA. 18
PA. 31
PA. 26
PA. 17
PA. 25
PA. 16
PA. 15
PA. 24
PA. 14
2 OF 4
7/8/85 REV A
1.2 Mb
MEMORY EXPANSION CARD
45974-60001
BORDER



3 OF 4	7/8/85 REV A
	1.2 Mb MEMORY EXPANSION CARD 45974-60001

BORDER


256Kx1
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
A0
A1
A2
A3
A4
A5
A6
A7
A8
WR
RAS
CAS
DIN
DQ
U21
U22
U23
U24
U25
U26
U27
U28
U29
U41
U42
U43
U44
U45
U46
U47
U48
U49
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD16
MD9
MD10
MD11
MD12
MD13
MD14
MD15
MD17
~CAS1L
MA (0: 8)
MD (0: 17)
~WE
~RAS1
~CAS1H
4 OF 4
7/8/85 REV A
1.2 Mb
MEMORY EXPANSION CARD
45974-60001
BORDER



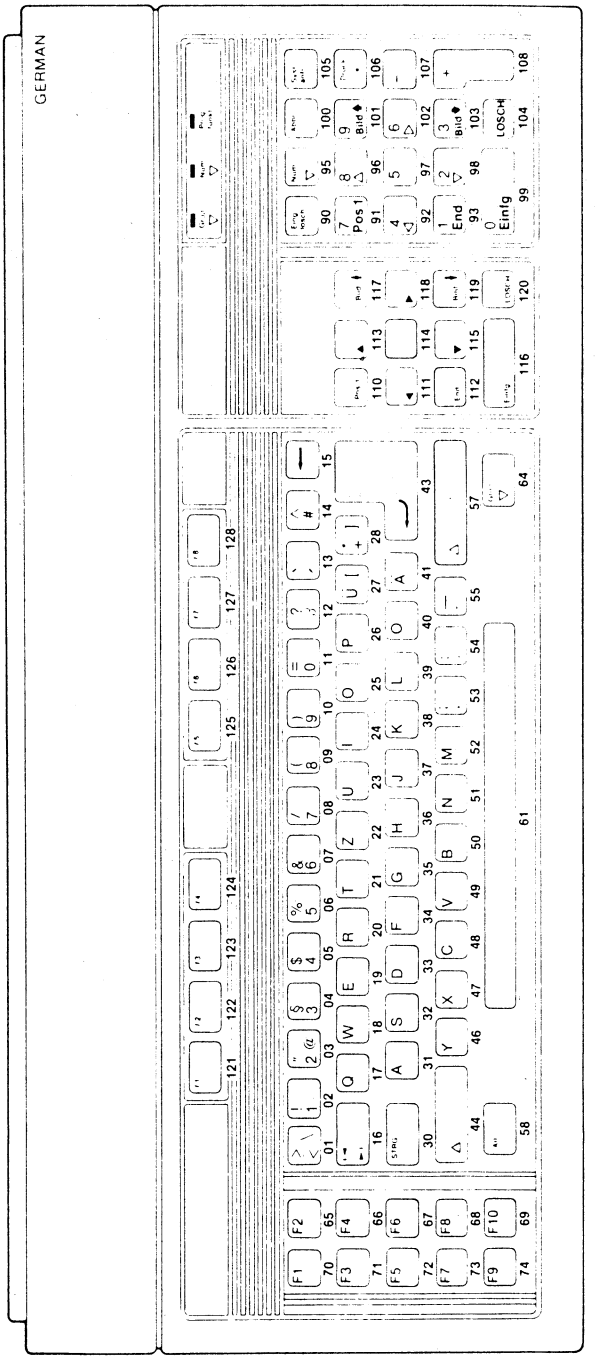
1 OF 1	7/8/85 REV A
	SERIAL/PARALLEL 24540-60001

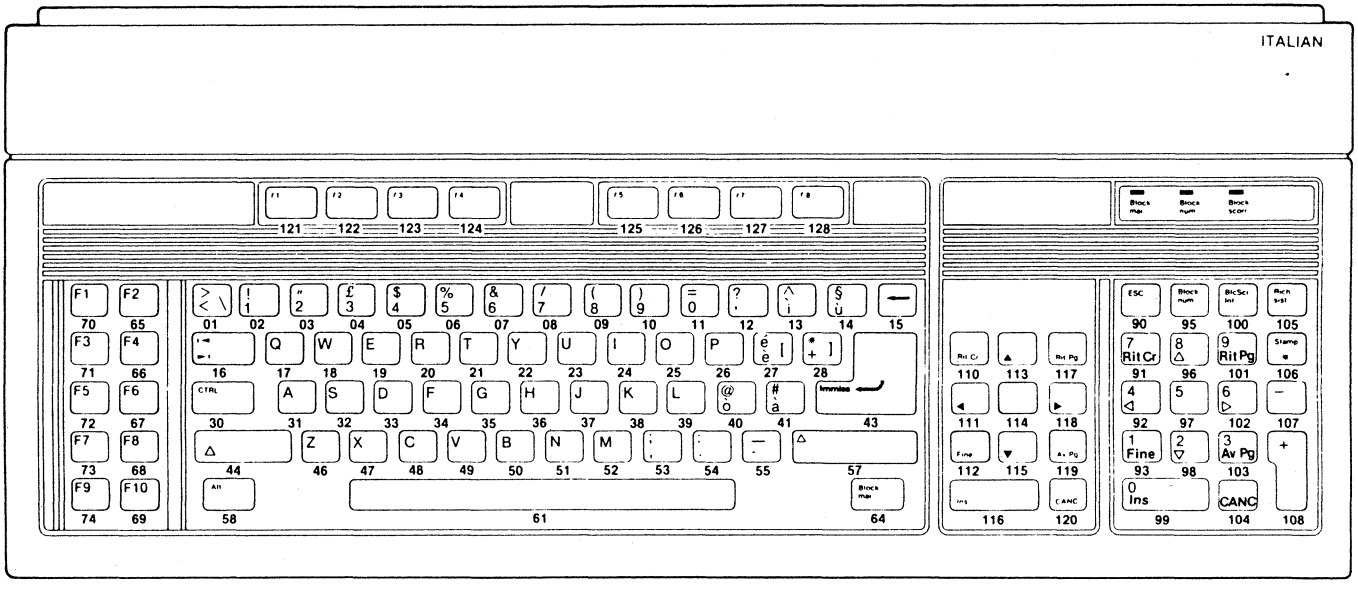
Appendix A

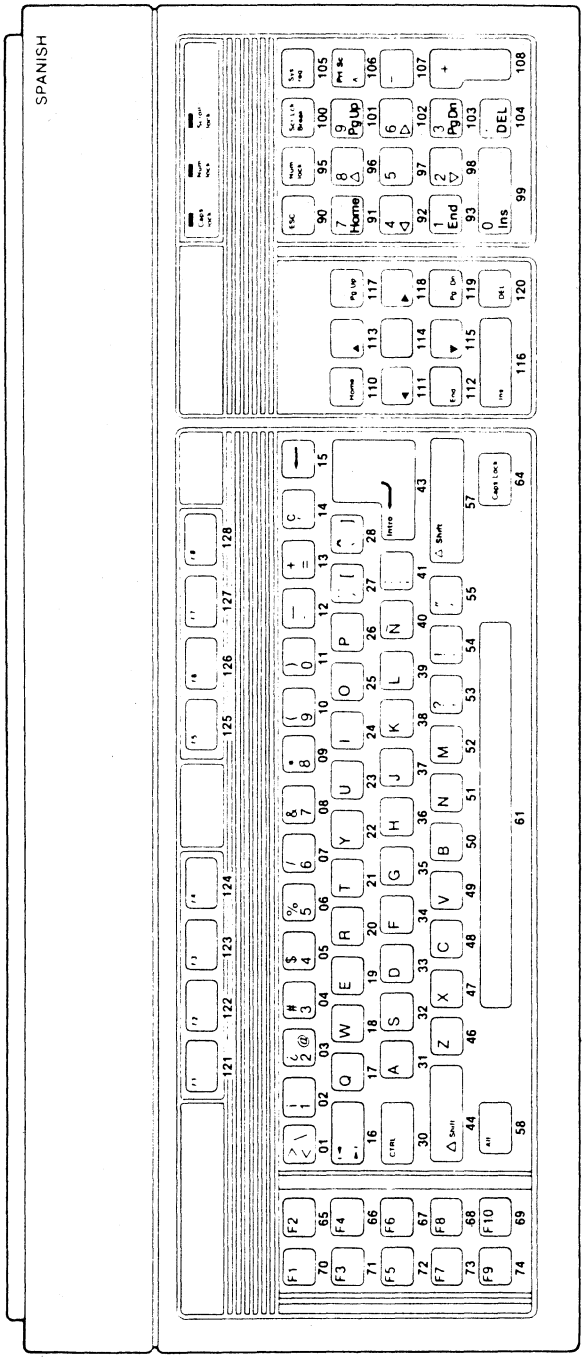
Norwegian/Danish Character Set

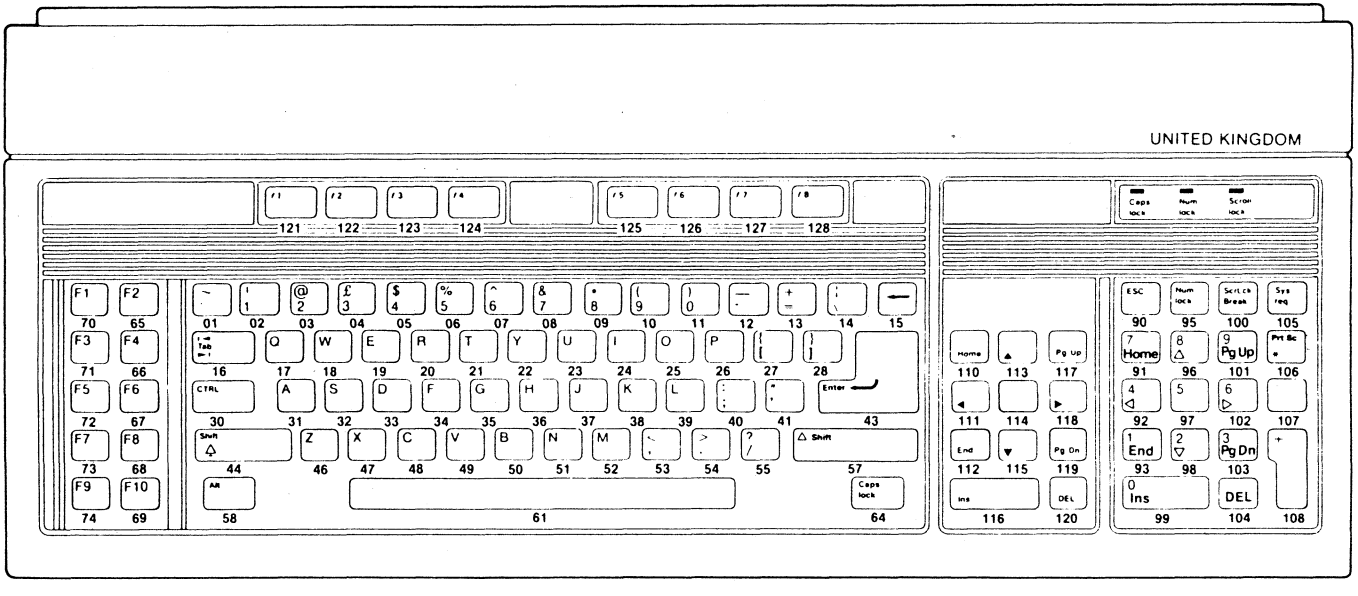
Hex Value	Character	Hex Value	Character	Hex Value	Character	Hex Value	Character	Hex Value	Character	Hex Value	Character	Hex Value	Character
00		20		40	@	60	`	80	ç	A0	á	E0	∞
01	☺	21	!	41	A	61	a	81	ü	A1	í	E1	β
02	☻	22	"	42	B	62	b	82	é	A2	ó	E2	Γ
03	♥	23	#	43	C	63	c	83	â	A3	ú	E3	π
04	♦	24	$	44	D	64	d	84	ä	A4	ñ	E4	Σ
05	♣	25	%	45	E	65	e	85	à	A5	Ñ	E5	o
06	♠	26	&	46	F	66	f	86	å	A6	ð	E6	μ
07	•	27	'	47	G	67	g	87	Ç	A7	Õ	E7	τ
08	◘	28	(	48	H	68	h	88	ê	A8	¿	E8	φ
09	○	29	)	49	I	69	i	89	ë	A9	ã	E9	θ
0A	◙	2A	*	4A	J	6A	j	8A	è	AA	Ã	EA	Ω
0B	♂	2B	+	4B	K	6B	k	8B	ï	AB	ℓ	EB	δ
0C	♀	2C	,	4C	L	6C	l	8C	î	AC	'n	EC	∞
0D	♪	2D	–	4D	M	6D	m	8D	ì	AD	¡	ED	Φ
0E	♫	2E	·	4E	N	6E	n	8E	Ä	AE	õ	EE	ϵ
0F	☼	2F	/	4F	O	6F	o	8F	Å	AF	ç	EF	∩
10	►	30	0	50	P	70	p	90	É	B0		F0	≡
11	◄	31	1	51	Q	71	q	91	æ	B1		F1	±
12	↕	32	2	52	R	72	r	92	Æ	B2		F2	≥
13	!!	33	3	53	S	73	s	93	ô	B3-DF		F3	≤
14	¶	34	4	54	T	74	t	94	ö	HP		F4	⌠
15	§	35	5	55	U	75	u	95	ò	Reserved		F5	⌡
16	▬	36	6	56	V	76	v	96	û			F6	÷
17	↨	37	7	57	W	77	w	97	ù			F7	≈
18	↑	38	8	58	X	78	x	98	ÿ			F8	°
19	↓	39	9	59	Y	79	y	99	Ö			F9	●
1A	→	3A	:	5A	Z	7A	z	9A	Ü			FA	·
1B	←	3B	;	5B	[	7B	{	9B	ø			FB	√
1C	∟	3C	<	5C	\	7C	¦	9C	£			FC	η
1D	↔	3D	=	5D	]	7D	}	9D	Ø			FD	2
1E	▲	3E	>	5E	^	7E	~	9E	L·			FE	■
1F	▼	3F	?	5F	_	7F	△	9F	l·			FF	

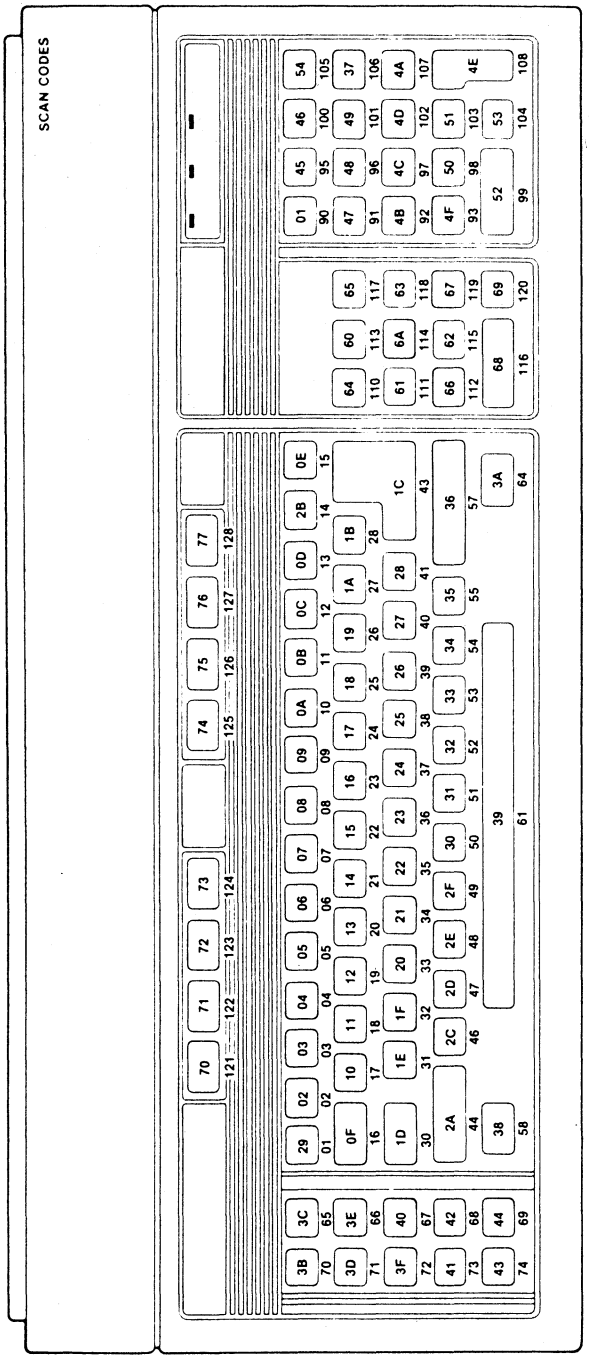
Keyboards

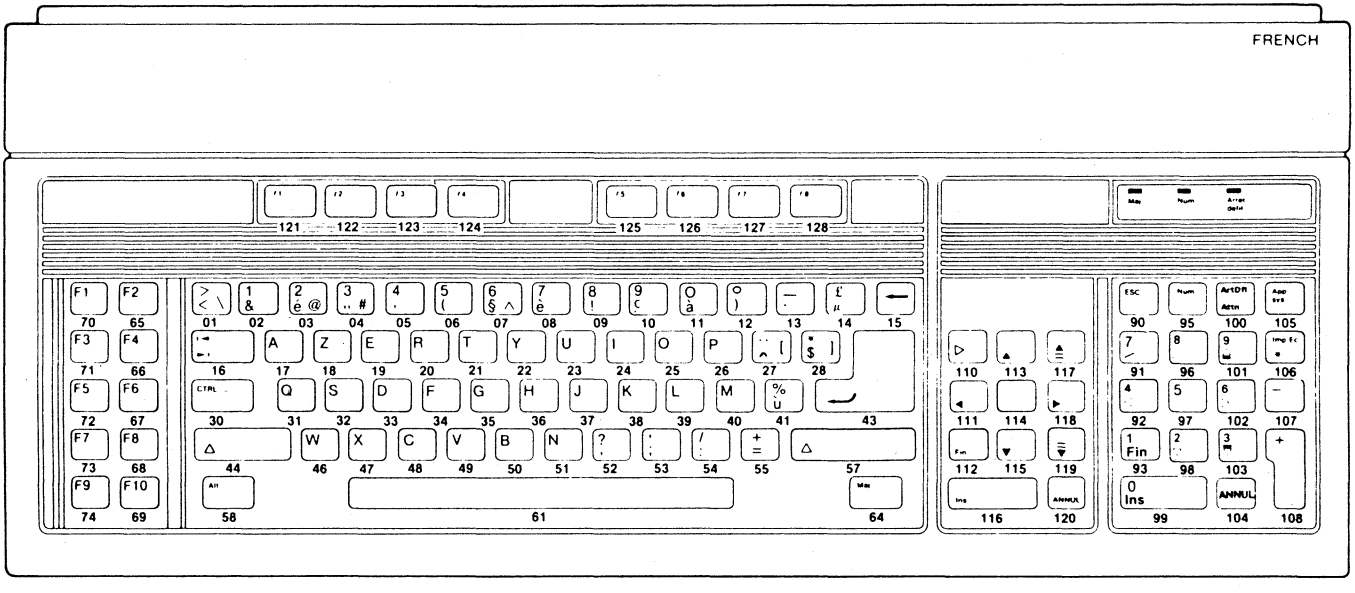



ITALIAN


SPANISH


UNITED KINGDOM


SCAN CODES


FRENCH

Glossary

Architecture: The design order of the system.

Break: The scan code the keyboard sends when a key that has been pressed is released.

Checksum: A sum of numbers used to detect equipment malfunctions in data-transfer operations.

Flexible disc: Thin flexible platter that is coated with a magnetic material used a a storage medium. Also know as floppy disk.

HP-HIL: The Hewlett-Packard Human Interface Link, a standard for interfacing a personal computer, terminal, or workstation to its input devices, providing a standard interface across the Hewlett-Packard computer product line.

HP-HIL Controller: Developed by Hewlett-Packard to interface the system to the HP-HIL input devices. It can accept commands from the system microprocessor and transmit and receive information via HP-HIL. It can also poll the input devices, collect data entered by the user, and relay it to the system.

Make: The scan code the keyboard sends for a key when it is pressed.

Processor Extension Card: On the HP Vectra, the system memory is contained on the processor extension card. This card is directly connected to the processor card via VLSI.

Schematic: A diagram with detailed information relating to circuitry, layout, terminal identification, showing gates, and showing circuits, etc.

Tilde: Symbolized by ~. Used to indicate signals that are active low.

Bibliography

Intel

iAPX 286/10 Hardware Reference Manual

iAPX 286/10 Programming Reference Manual including the 286 Numeric Supplement

iAPX 287 Support Library Reference Manual

Microcontroller Handbook

Microsystem Components Handbook, Volume II

Memory Components Handbook

Motorola

Single Chip Microcomputer Data, Series C

Texas Instruments

MOS Memory Data Book

INDEX

A

B

C

D

E

F

G

H

I

J

K

L

M

N

O

P

R

S

T

U

V

W

Printed U.S.A.
inventory number 45961-90001