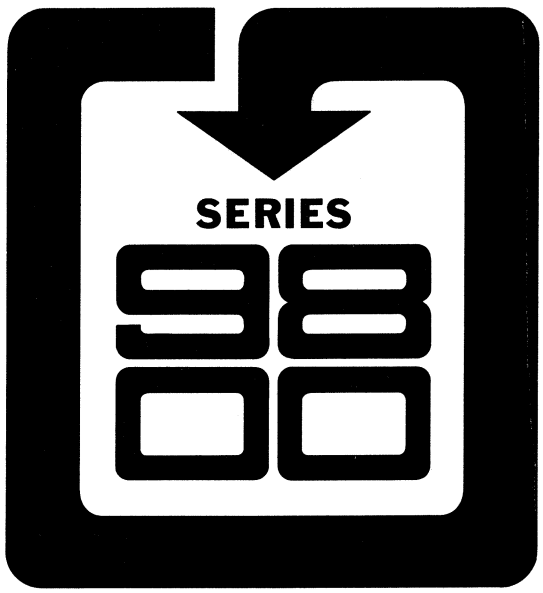

HEWLETT-PACKARD CALCULATOR

HEWLETT-PACKARD COMPANY

11202A I/O TTL INTERFACE

PRELIMINARY USER'S MANUAL

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GENERAL INFORMATION

The -hp- 11202A I/O TTL Interface is a general-purpose interface kit which provides the necessary storage, buffering, and conditioning of electrical signals which pass between a peripheral device and a 9800 Series Calculator. This interface is intended to be used with an appropriate Peripheral Control Block (ROM Block) to enable the calculator to control and to send or receive data from a 'non-standard' calculator peripheral device.

Refer to the Peripheral Control Block Operating Manual for a description of the calculator/peripheral operations which are available when using the peripheral block and this interface. That manual also describes the data formats which are available for I/O operation.

PHYSICAL DESCRIPTION

The interface kit consists of a circuit card, an I/O pac, and a 6' shielded cable. The I/O pac, which houses the circuit card, can be plugged into any one of the I/O slots at the back of the calculator. One end of the cable connects to the circuit card. The other end of the cable has been left open; this permits the interface to be easily connected to any peripheral device.

SETTING THE SELECT CODE

The select code (or address) of the peripheral device, which is interfaced to the calculator through the interface kit,can be selected on the interface card. Refer to the Peripheral Control Block Operating Manual for a further description of the select code.

The procedure given below should be used when setting the select code.

1. Switch the calculator and the peripheral device OFF.

2. Disconnect the interface from the calculator. Remove the four screws located on the top of the card assembly; then, turn the card over and lift off the bottom cover.

3. Locate the Select Code Switch (see Figure 1). Raise the hinged cover on the switch. Using a small, flat-blade screwdriver, carefully rotate the selector-tab until it is positioned at the desired select code number (numbers are printed on the side and on the top cover of the switch). Before closing the cover, be sure the slot in the selector-tab is positioned at a right angle with respect to the length of the switch.

4. Close the switch cover and replace the interface card bottom cover. Secure the cover with the four screws which were removed in step 2.

5. Place a Select Code Label on the peripheral

device to indicate the new select code. A package of labels is supplied with the interface kit.

6. Reconnect the interface to the calculator, and turn the calculator and the peripheral device ON. Verify that the desired select code is set by performing some peripheral control operations (or running a program) which specify the new code.

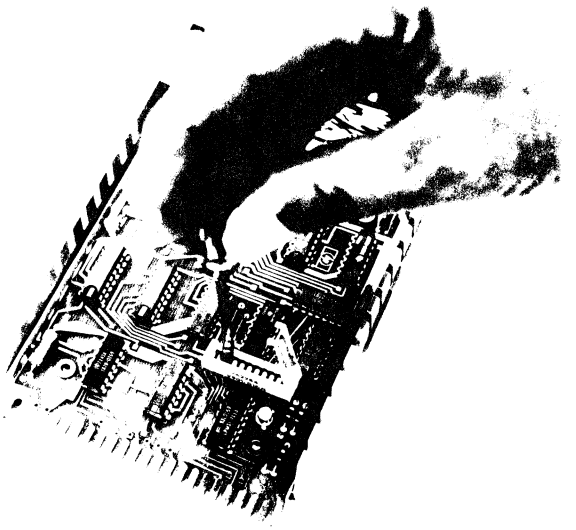


FIGURE 1. SETTING THE SELECT CODE

INTERFACING TO -hp- COMPUTER PERIPHERALS

The -hp- 2895A Tape Punch or the -hp- 2748A Tape Reader may be easily interfaced to a 9800 Series Calculator, when using the interface kit. Refer to the appropriate Peripheral Control Block Operating Manual for instructions on how to control these peripherals.

Use the table below when connecting the 11202A I/O Interface to either the Model 2895A Tape Punch or the Model 2748A Tape Reader.

11202A INTERFACE CARD			TAPE PUNCH INPUT **		TAPE READER OUTPUT	
SIGNAL	J_1 PIN NO.	CABLE * WIRE COLOR	SIGNAL	CONNECTOR PIN NO.	SIGNAL	CONNECTOR J_2 PIN NO.
IØ	16	Ø			Bit 1	B
I1	15	1			Bit 2	F
I2	14	2			Bit 3	L
I3	13	3			Bit 4	R
I4	12	4			Bit 5	V
I5	11	5			Bit 6	Z
I6	10	6			Bit 7	d
I7	9	7			Bit 8	j
OØ	T	9,Ø	Ch.1	1		
O1	S	9,1	Ch.2	2		
O2	R	9,2	Ch.3	3		
O3	P	9,3	Ch.4	4		
O4	N	9,4	Ch.5	5		
O5	M	9,5	Ch.6	6		
O6	L	9,6	Ch.7	7		
O7	K	9,7	Ch.8	8		
CTL	H	9,8	PI	11	Read	AA
STP	J	9,Ø,2				
I/O	F	9,Ø,1				
FLG	C	8	PR	12	Feed Hole	FF
ECH	B	9				
GND	17,18	9,Ø,3	ØV.	25	GND	HH
		9,Ø,4	(GND)			

* 9,2,4 Denotes Wire Color: color code same as resistor color code. First number identifies base color, second number identifies wider strip, third number identifies narrower strip. (e.g., 9,2,4 = White, Red, Yellow.)

** Connect a jumper from pin 9 to pin 24.

INTERFACE OPERATION

This section contains an abbreviated list of interface operational characteristics and a discussion of input and output operations.

> NOTE
> The 11202A Interface uses negative-true logic (i.e.,Øv.='low'="1"=true; +5v.='high'="Ø"=false).

OPERATIONAL CHARACTERISTICS

Data Input: (from peripheral device)

Eight input lines with low power (type 74L04) TTL loads, which have resistive dividers consisting of 1.8K to +5V, and 2.7K to ground.

Data Output: (to peripheral device)

Eight output lines with open collector, TTL - Hex Inverters (type 7406).

Control Lines:

Five control and mode lines are available.

Control ($\overline{CTL}$) - 'High' to 'low' transition signifies card ready for Input or Output. open collector TTL.

FLG (FLG) - Returned 'low' from device when data accepted (output) or data ready (input). TTL Schmitt Trigger.

Input/Output (I/O) - Signifies mode of operation (Input-'High' or Output-'Low'). TTL open collector.

Stop ($\overline{STP}$) - 'Low' level signifies stop key on calculator pressed. $\overline{STP}$ stays 'low' for the duration of time that the STOP key is pressed. $\overline{STP}$ also forces $\overline{CTL}$ 'High' when the calculator terminates an operation. TTL open collector.

Enable Handshake (ECH) - When connected to ground, requires peripheral device to have flag 'high' to indicate device ready. Normally (when not connected to ground), peripheral device cannot indicate when it is ready. STD.TTL input with 10K pull-up resistor to +5Volts

OUTPUT OPERATION

All output signals are negative true (i.e., ØV=true=low). Referring to Figures 2 and 5, the output data is transmitted from U1Ø and U12. The output lines are designated 0Ø-07. Output data is latched and sent at least 5µs before control ($\overline{CTL}$) is passed.

The I/O signal is high during an input operation. The signal is latched 'low' on the first output pass, (5µs before $\overline{CTL}$ is passed) and will continue to remain 'low' until an input operation is about to take place. Then it will be

latched 'high' 5µs before the first $\overline{CTL}$ is passed for input. It will then remain 'high' until an output is about to take place.

The control signal ($\overline{CTL}$) goes 'low' when data is being output, or when an input is being requested. The $\overline{CTL}$ signal will stay 'low' until the peripheral returns a flag; then the $\overline{CTL}$ will go 'high'. (If the STOP key is pressed, $\overline{CTL}$ will be driven 'high' immediately.)

The $\overline{STP}$ signal is 'low' when the STOP key is pressed.

The following is a typical output sequence.

Upon command from the calculator the interface is interrogated as to its 'ready-busy' status. When found ready, data and the output signal (SO3) are passed and latched; 5µs later, $\overline{CTL}$ is driven 'low'. The card is now in the busy state. When the peripheral has received the data and is done, or ready for more, it must return a flag to so indicate. The flag causes information on the input data lines to be loaded and stored. Then, the control flip-flop is clocked clear and $\overline{CTL}$ goes 'high'. The interface is now in the 'ready' state.

NOTE

Since the output buffers reflect the states of the storage elements when the flag is returned, the output will go to the same states as the input.

INPUT OPERATION

Input data signals are negative true. The receiving devices are U13 and U11. The lines are designated IØ-I7. Referring to Figures 3 and 5, data may be input only after the I/O signal is 'high' and $\overline{CTL}$ is driven 'low'. The input data must be present and settled at least 150ns before the flag is given.

The flag line is designated $\overline{FLG}$ and is negative true. The FLG receiver is a TTL Schmitt Trigger.

FALLING EDGE (ECH open)

Upon receipt of a falling edge (+3 volts to 0 volts), the Control flip-flop is cleared ($\overline{CTL}$ goes 'high') and the signals on the input data lines are loaded into the storage units. The Interface then goes to the not 'ready' state, indicating that the next operation can take place.

The following is a typical output sequence.

Upon command from the calculator, the input signal (SO3) and all data bits (which are 'low') are passed and latched; 5µs later, $\overline{CTL}$ is driven 'low'. The interface is now in the busy state and the peripheral should be ready to input. When input data is ready, the flag is transmitted. The data is latched 300 ns later. Then the control flip-flop is clocked clear and $\overline{CTL}$ goes 'high'. The interface is in the ready state when the input data is stored. The calculator interrogates the interface, and upon finding it ready, inputs the stored data.

CORPORATE HANDSHAKE (ECH GROUNDED)

The 'handshake control' requires that the peripheral must return the $\overline{FLG}$ signal 'high' to indicate the not busy state.

Output Sequence Example:

The calculator must check to see if the interface is ready. The control flip-flop must be in the ready state and the FLG signal must be 'high' before the interface will indicate ready. The eight-bit data word and the I/O bit (SO3) are sent from the calculator and are latched on the interface; 5µs later, $\overline{CTL}$ is driven 'low'. When $\overline{FLG}$ is returned 'low', $\overline{CTL}$ goes 'high' and the input signals are loaded into the interface storage units. The interface remains in the

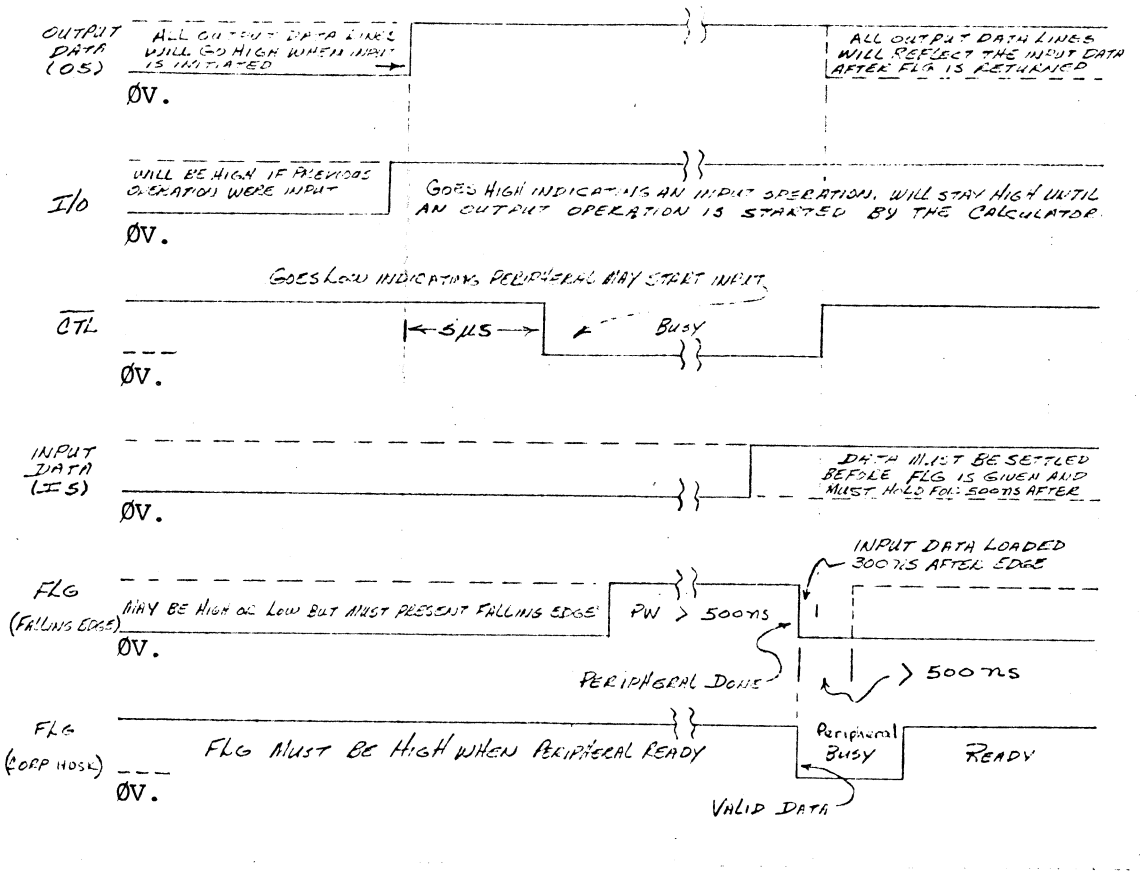


FIGURE 3. INPUT TIMING SEQUENCE

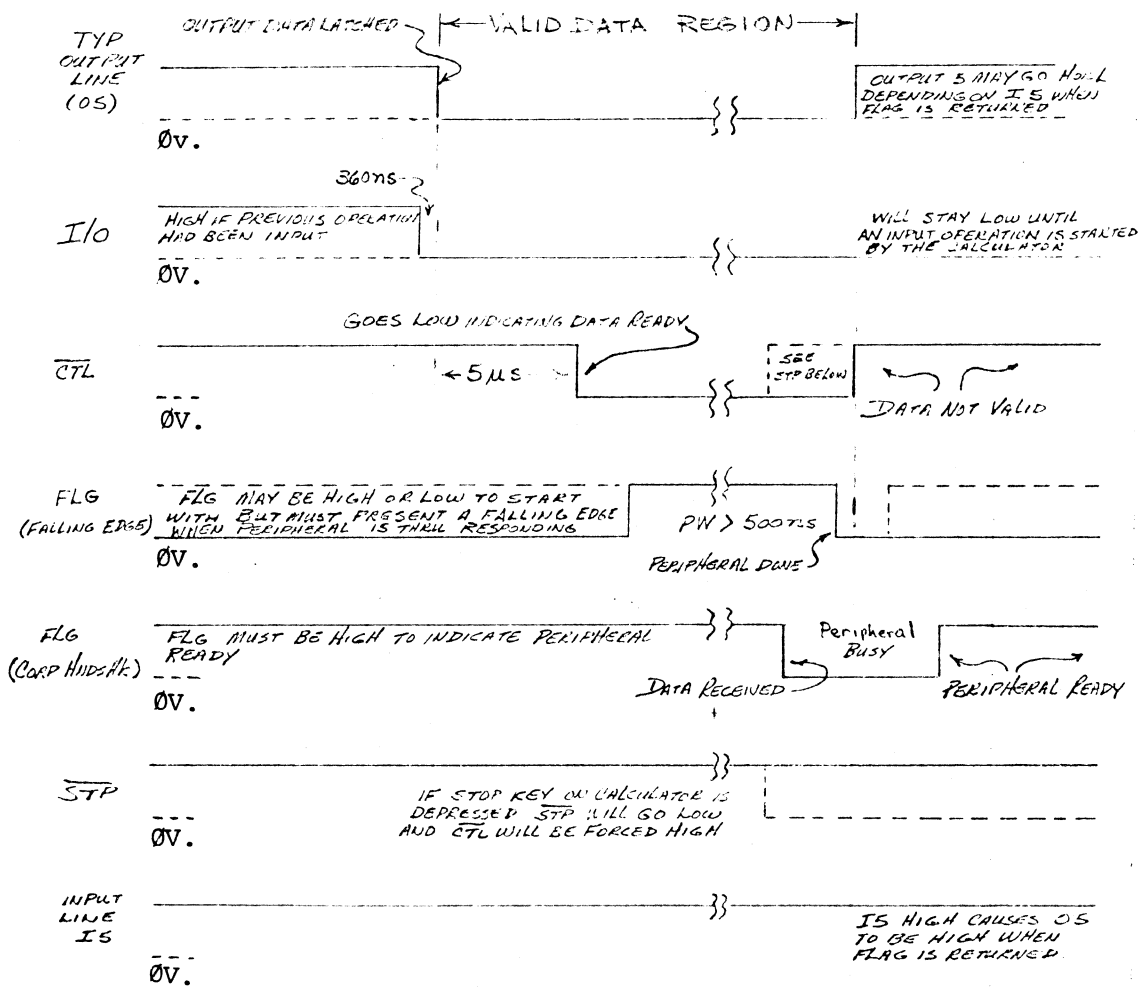
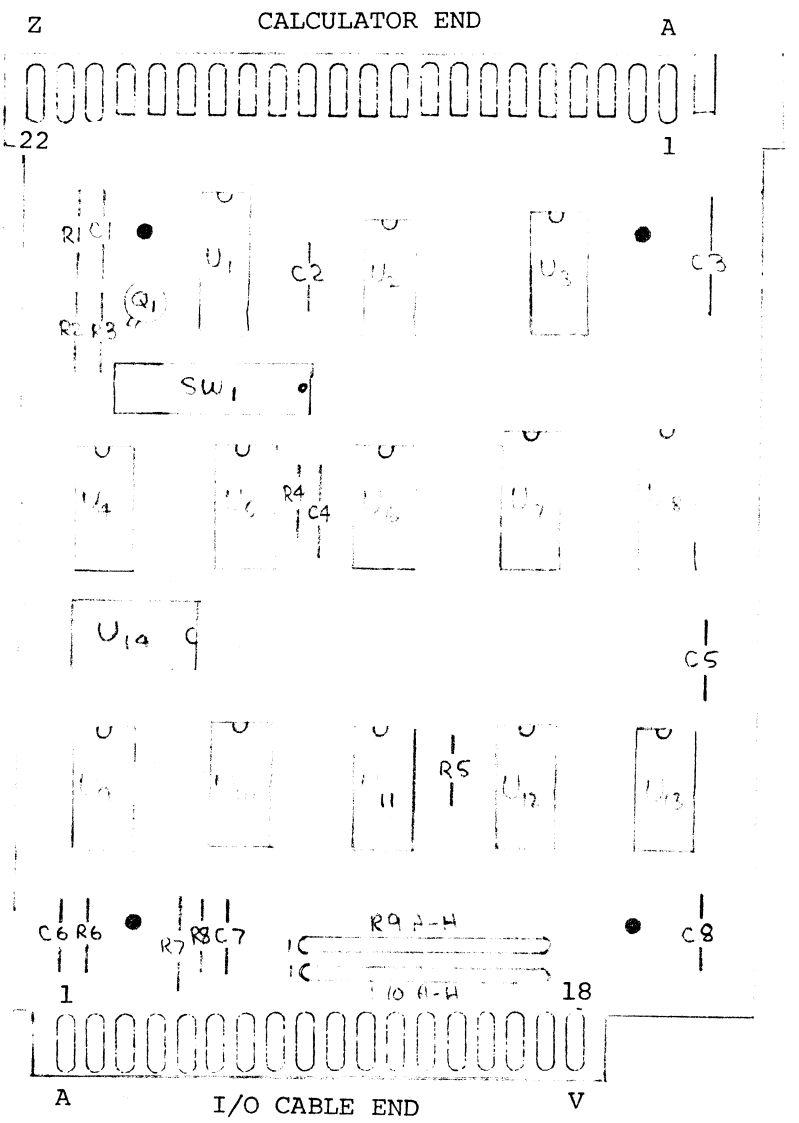


FIGURE 2. OUTPUT TIMING SEQUENCE



-hp- P/N 11202-66591 REV A

FIGURE 4. 11202A INTERFACE CIRCUIT CARD

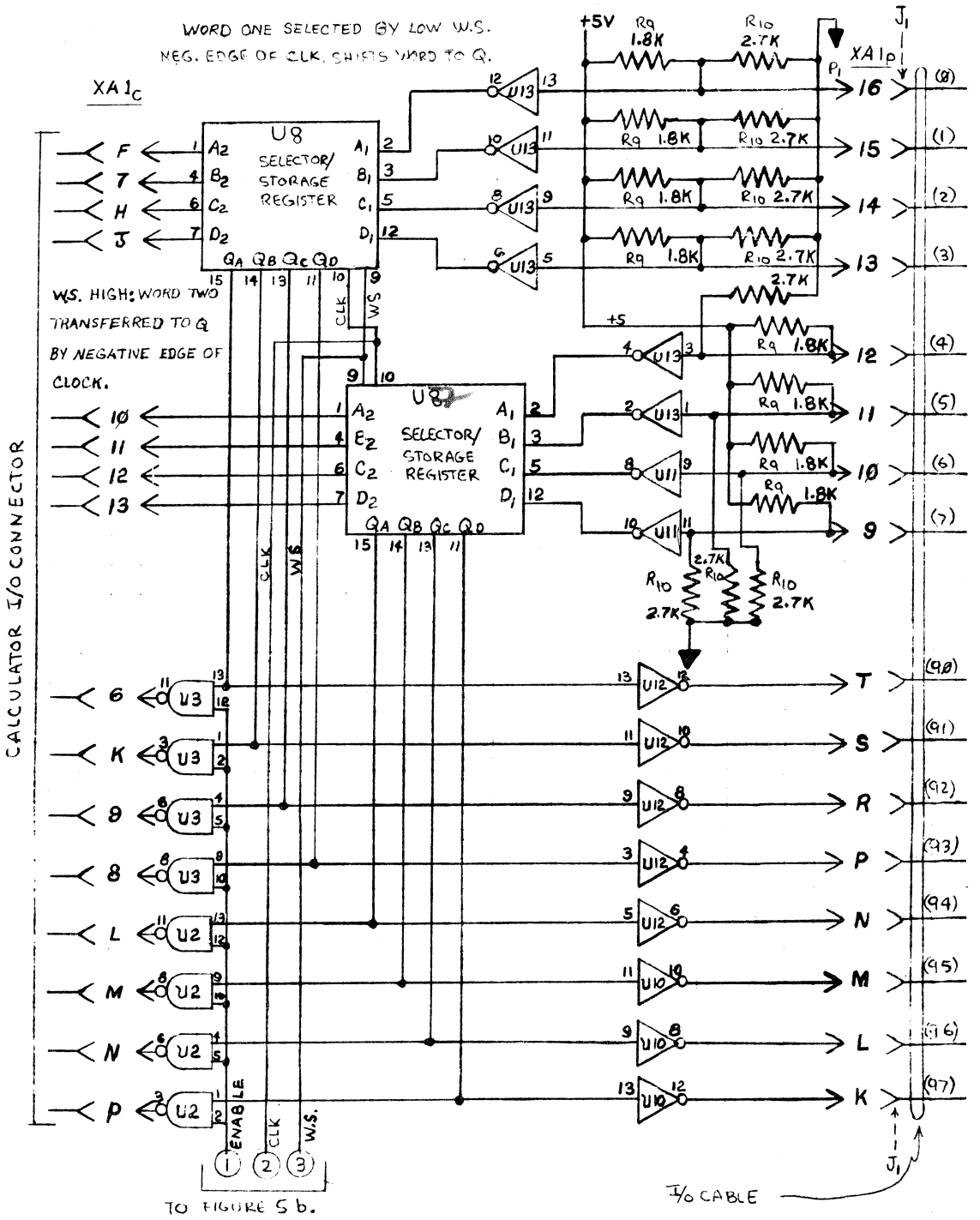
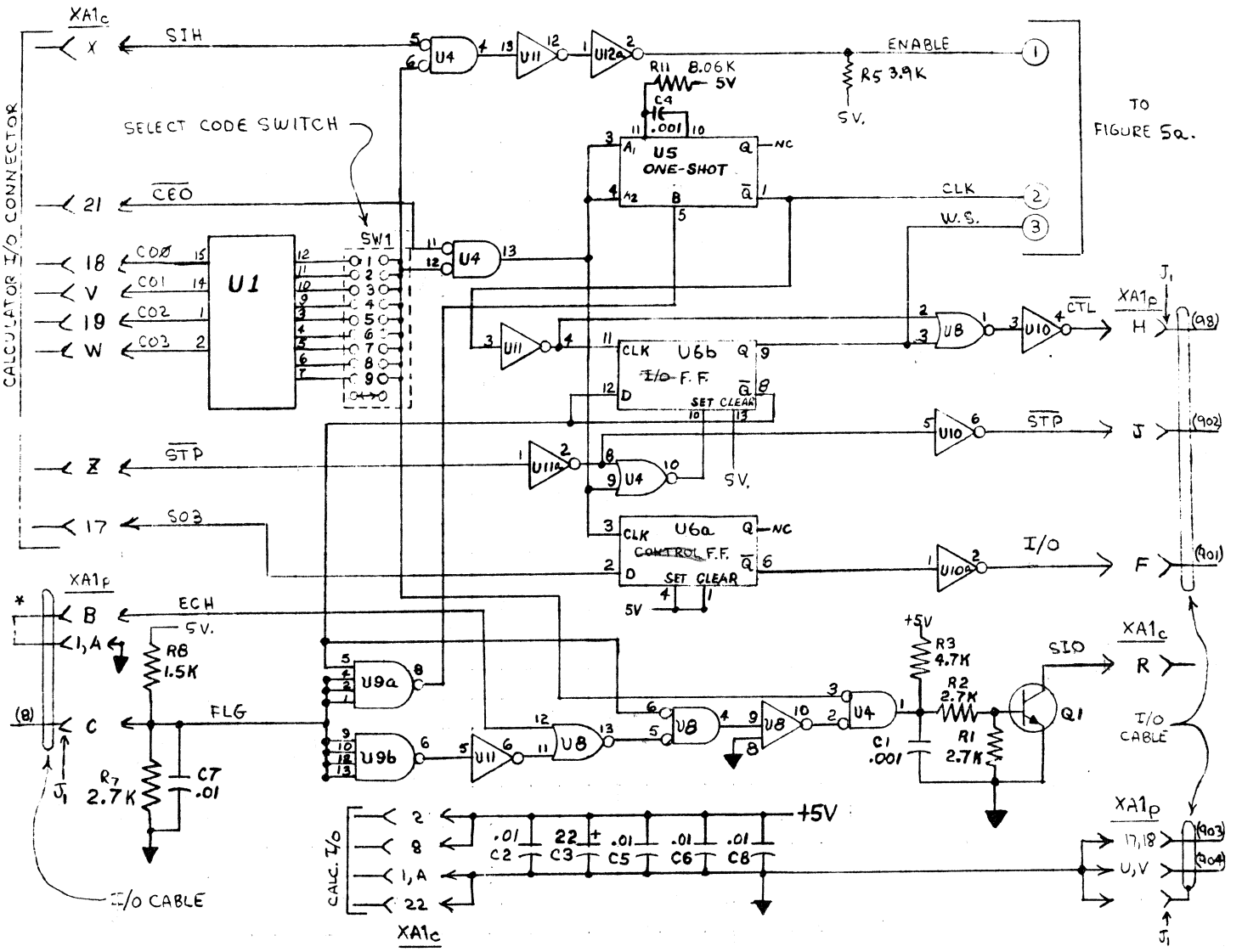


FIGURE 5a. I/O LOGIC DIAGRAM



*Connect A and B together for 'corporate handshake'.

(924) Denotes Wire Color: color code same as resistor color code. First number identifies base color, second number identifies wider strip, third number identifies narrower strip. (e.g. (924) = White, Red, Yellow.)

FIGURE 5b. CONTROL LOGIC DIAGRAM

RECOMMENDED CIRCUITS

OUTPUT CIRCUITS (TRANSMITTERS)

Each output signal from the interface is transmitted from an SN7406 TTL hex inverter buffer/driver with open collector high-voltage (+3ØV) outputs. The current sink capability of each buffer is 40ma and the breakdown voltage is +3Ø volts.

V_{OL} @ (I_{OL} = 16ma) = +Ø.4 volts maximum

@ (I_{OL} = 40ma) = +Ø.7 volts maximum

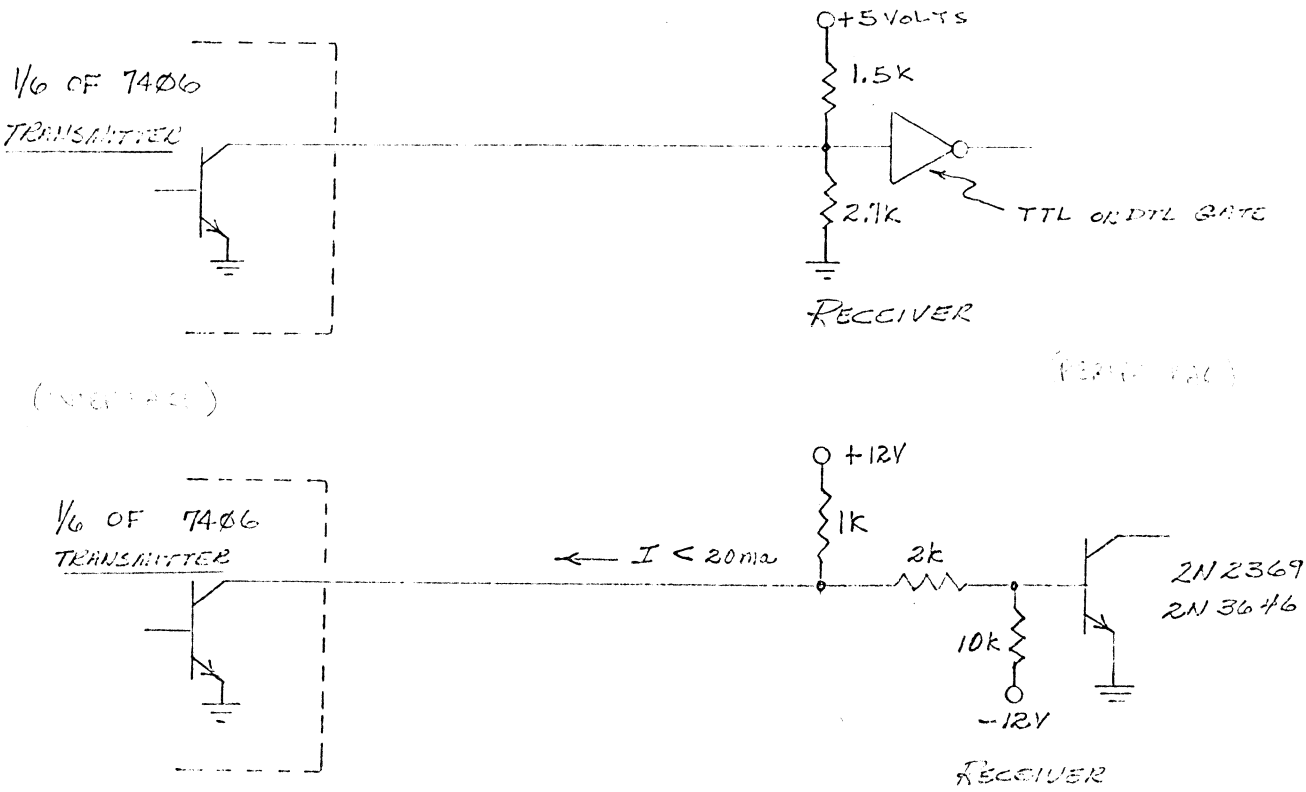
V_{OH} (Open Collector) = 3Ø volts maximum

I_{OL} = 4Ø ma maximum

I_{OH} @ (V_{OH} max.) =25Ø µA

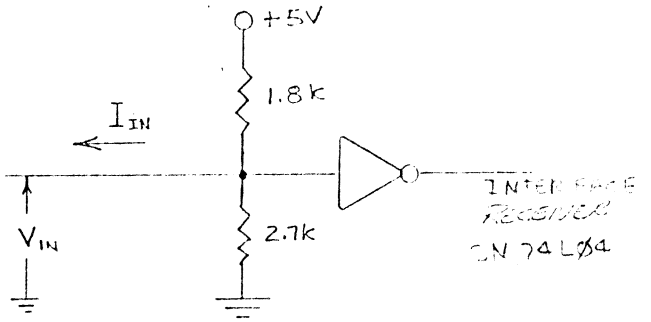
RECOMMENDED RECEIVING CIRCUITS

Output signals are described in the preceding text. Since each transmitter is an open collector, the receiving circuits (on the peripheral end of the cable) must have a positive pull-up voltage (not to exceed 3Ø volts), and they must be restricted to sourcing back to the transmitter less than 4Øma. Recommended receiving circuits are shown on the following page



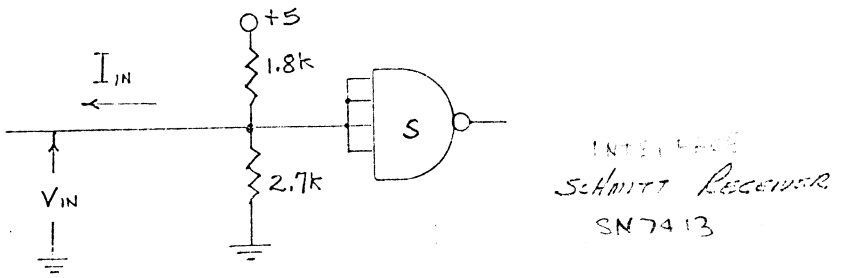
INPUT CIRCUITS (RECEIVERS)

Input signals, as described in the preceding text, are negative true (i.e., ØV=true=low). Each input data signal (IØ - I7) is received by an SN74L04 low power, hex-inverter. A resistive divider connected to each input line sets the voltage to about +3 volts when the cable is disconnected. The input voltage must not exceed +5.5 volts.



I_{IN}	"1"	= 3.5 ma
V_{IN}	max.	=+5.5 volts
V_{IN}	"Ø"	> +2 volts
V_{IN}	"1"	< +.7 volts

The input signal ($\overline{FLG}$) is received by an SN7413 Schmitt Trigger circuit. This circuit allows slowly rising or falling signals to be received, and provides better noise margins.



I_{IN} (high) = 5.Ø ma		V_{IN} (low)	+2.Ø volts
V_{IN} max. = +5.5 volts		V_{IN} (high)	+Ø.6 volts

Voltage on the input flag line must not exceed +5.5 volts.

There is no restriction on the input rise and fall time.

RECOMMENDED TRANSMITTING CIRCUITS

Transmitting circuits (on the peripheral end of the cable) may be various types; recommended transmitting circuits are shown below.

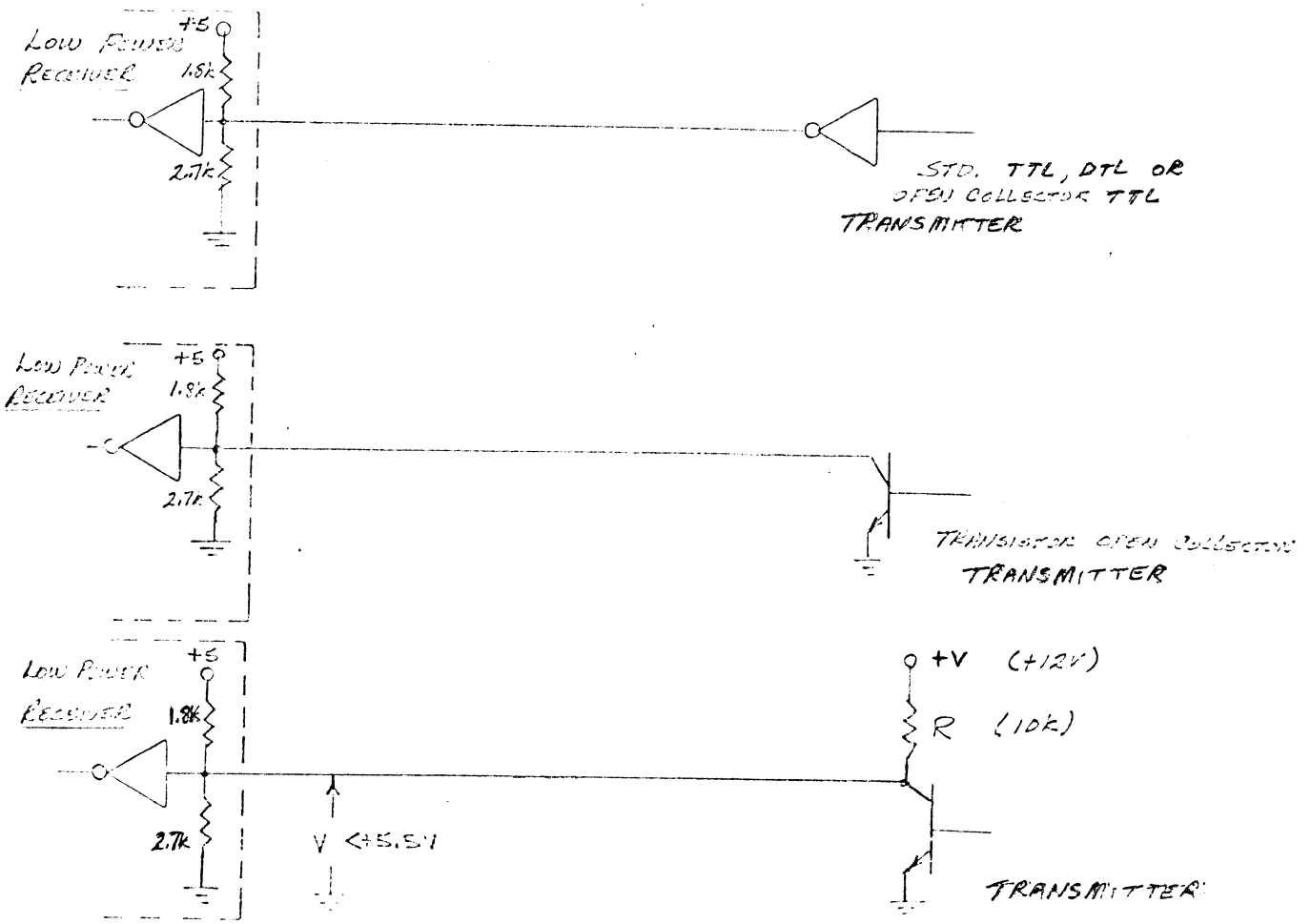


TABLE 2 REPLACEABLE PARTS LISTS

†	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	A1	11202-66591		1	P.C. Assembly - Interface	-hp-	
				2			
	C1, C4	0160-0153		2	C: fxd mylar .001uf +/- 10% 200wvdc	56289	292P10292-PTS
	C2, C5-C8	0160-3847		5	C: fxd ceramic dielectric .01uf -0 +100% 25wvdc	24546	CK12BX CMV
	C3	0180-0228		1	C: fxd solid tant 22uf +/-10% 15wvdc	90201	TAS226K015PIC
	R1, R2	0684-2721		2	R: fxd comp 2700ohms +/-10% ¼W	01121	CB2721
	R3	0684-4721		2	R: fxd comp 4700ohms +/-10% ¼W	01121	CB4721
	R5	0684-3921		1	R: fxd comp 3900ohms +/-10% ¼W	01121	CB3921
	R7	0687-2721		1	R: fxd comp 2.7K +/-10% ½W	01121	EB2721
	R8	0684-1521		1	R: fxd comp 1500ohms +/-10% ¼W	01121	CB1521
	R9	1810-0076		1	R: network, encap cermet, 8 resistors, all 1.8K +/-5%	56289	Type 200C
	R10	1810-0041		1	R: network, encap, 8 resistors, all 2.7K +/-5%	56289	200C 1641
	R11	0698-4473		1	R: fxd film 8.06K +/-1% 1/8W	24546	C4 T-O
	Q1	1854-0019		1	XSTR: Si NPN, Similar to 2N2369	04713	SS2188
	S1	3101-1677		1	Switch-programming, 10 position, gold plated contacts, straight pin terminals, P.C. mounting, Carry - 1.0A, 60Vac/dc, Switching 0.5A 60Vac/dc	00LOH	C42315-A61-A1
	U1	1820-0627		1	IC: Digital, One-of-ten Decoder TTL +Logic VS=5V +/-5%, 16 pin DIP ceramic	07263	SL16900
	U2, U3	1820-0269		2	IC: Digital, Quad 2-Input Nandgate with open collectors TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	01295	SN12785
	U4, U14	1820-0584		2	IC: Digital, Quad 2-Input Norgate TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	12040	DM74LO2N
	U5	1820-0261		1	IC: Digital, Monostable Multivibrator TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	01295	SN13617
	U6	1820-0596		1	IC: Digital, Dual D Flip-Flop TTL +Logic VS = 5V +/-5%, 14 pin DIP plastic	12040	DM74174N
	U7, U8	1820-0656		2	IC: Digital, Low Power 4-bit Data Selector/ Storage Register TTL +Logic VS=5V +/-5% 16 pin DIP plastic	01295	2N14266
	U9	1820-0537		1	IC: Digital, Dual 4-Input Nandgate Schmitt Trigger TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	01295	SN21158
	U10, U12	1820-0471		2	IC: Digital, Hex Invertor/Driver TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	01295	SN19235
	U11, U13	1820-0586		2	IC: Digital Hex Invertor TTL +Logic VS=5V +/-5%, 14 pin DIP plastic	12040	DM74LO4N
		11200-04101		1	Cover - I/O	-hp-	
		0590-0993		4	Standoff - Press		
		7204-0018		.190	Sht Al .080 thk		
		11202-26591		1	P.C. Board (unloaded) - TTL Interface	-hp-	
		4174-0093		.167	Sht - Plastic .059 thk		
		8500-0108		4.733	Gold - Soft		

Table 2. REPLACEABLE PARTS LISTS

†	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
		11202-61601		1	Cable Assembly		
		0362-0249		1	Terminal - Sleeve		
		0362-0309		1	Sleeve - Cable Terminal		
	J1	1251-2188		1	Connector: P.C. contacts, 36(2 x 18) ribbon type, 156 spacing	05574	000221-0172
		5040-7008		.5	Cable - molded		
		5040-5911		1	Boot - Bottom		
		4093-0336		.160	Molding Comp.		
		7120-2922		1	Plate - I.D.		
		7120-2940		2	Label - Select Code ,Pkg.		