11305A MASS MEMORY CONTROLLER

THEORY OF OPERATION

MASS MEMORY SYSTEM

Besides the disc drive, the mass memory system includes the elements shown in Fig. 1. A plug-in read-only memory (ROM) block is installed in one of the 9830's eight ROM slots to expand the calculator's instruction repertoire. An interface cable assembly containing interface circuitry and a small cache memory connects the calculator to the disc drive controller. Another cable assembly connects the controller and the disc drive.

The complete system is designated Model 9880 Mass Memory System. Model 9880A includes the 9867A Mass Memory (disc drive) and Model 9880B includes the 9867B.

Fig. 2 shows the information-transfer paths in the system. All data transfers between the calculator and the mass memory go through the cache memory. All addresses, commands, and status information are processed through the 9830 input/output structure. The basic difference is that cache memory transfers go directly to the calculator read/write memory and are much faster than transfers through the calculator I/O structure.

The cache memory is a 256-word (512-byte) MOS read/write memory. It allows data transfer from the calculator at one rate and to the mass memory at a different rate. This avoids any synchronization or timing problems between the two components. The full 256-word contents of the cache memory are transferred during any read/write operation with the mass memory. The cache memory appears to the calculator as an extension of its own memory, but it is not accessible by the user.

MULTIPLE CALCULATORS AND PLATTERS

The mass memory has an extremely large storage capacity. Each disc, or platter, as it is frequently called, can store 2.4 million bytes. Therefore, one mass memory is usually enough for an individual user.

For applications that require still more storage, the 11305A controller can handle up to four platters in the same system, giving a total storage capacity of 9.6 million bytes. This offers some important advantages to the user. For example, he can access separate data bases stored on different cartridges and process the data on another platter. It also makes duplication of important data bases very simple.

To match this storage and accessing capacity, the controller can also handle up to four 9830A Calculators in the same system (see Fig. 3). Any of the four calculators can access any of the four platters connected to the system. Each platter contains the full system software and is not dependent on any of the others for its operation.

It should be emphasized that this system is not a time-shared system. Only one calculator can access a platter at any given time. The remaining calculators in the system can access their respective cache memories during this time. The cache memory remains dedicated to the calculator, not to the controller.

It is true, however, that two or more users can be working on different applications and sharing one or more mass memories, and in most such situations, neither user would notice that someone else was using the system. An order processing system, for example, might have someone entering new orders, another preparing shipping papers and updating inventory records, and still another preparing order acknowledgements and billing customers. The new order entries could be transferred from a holding file to the main data base at the beginning of each day.

PLATTER ORGANIZATION

Each platter, removeable or fixed, represents a separate mass memory system. As such, each platter is independent and must have its own directory area, bootstraps, and so on. The platter organization is shown in Fig. 4.

The platter is a 14-inch diameter aluminum disc that has a ferromagnetic oxide coating on both sides. Two read/write heads, one for each surface, move back and forth over the surface, separated from it by a thin layer of air. The platter rotates at 2400 rpm.

Any location on the platter is defined by three variables: head, cylinder, and sector. CYLINDER defines the radial position. There are 203 cylinders, 0 thru 202, numbered from the outside of the platter towards the center. SECTOR defines the angular position around the platter. There are 24 sectors, numbered 0 thru 23. A thin metal skirt on the hub of the platter has 24 slots cut into it to define precisely the start of each sector. An index slot provides a reference for sector 0. HEAD 0 and HEAD 1 specify the upper and lower platter surfaces, respectively.

Each platter is divided into two areas, the system area and the user area. The system area is used by the mass memory system and is occupied by the following items.

Item	Location
Directory	Head 0, Cylinders 0 & 1
Availability Table and Defective	
Track Table	Head 0, Cylinder 2, [illegible]
Bootstraps	Head 0, Cylinders 3 to 7

The directory serves as the file index of the mass memory system. All file names, along with other pertinent information such as relative location and size, are

entered in the directory. The availability table contains a list of all vacant mass memory segments that are available for user files. The directory and the availability table are automatically updated by the system every time a file is created or deleted. The defective track table contains a list of the defective tracks present on the platter. A maximum of six defective tracks are allowed in the user area.

The remaining platter area is available for user data, program files, and key files. This area, the total area minus the system area, has a capacity of 4752 512-byte records.

MULTIPLE PLATTERS

When there are two or more platters in a system the UNIT numbers shown in Fig. 3 provide platter identification for the system software. The 9867A single-platter drive has a switch on the front panel that can be set to four positions, 0 thru 3. The 9867B two-platter drive has an internal setting corresponding to UNITS 0 and 1 or UNITS 2 and 3. In the 9867B, UNITS 0 and 2 correspond to the removeable cartridge and UNITS 1 and 3 to the fixed platter of the mass memory.

A UNIT n command from the calculator determines which platter in the system is to be accessed. Obviously, no two platters in the system can be assigned the same UNIT number. The UNIT number is part of the address that is sent to the mass memory. Only the drive with the selected UNIT number will respond to the controller commands.

SERVICE ALLOCATION FOR MULTIPLE CALCULATORS

When there are two or more calculators in a system the controller sequentially scans each of the service request lines from the calculators. As soon as a service request is detected, the controller halts the scanning process and enables the address and status lines from that calculator (see Fig. 2). These lines are common to all calculators connected to the system, so only one calculator can use them at any given time. The data lines (4 lines) between the cache memory and the controller are also common, so the controller must enable these lines to the cache memory corresponding to the calculator requesting service.

The controller remains dedicated to this calculator until it has released its service request for about 750 milliseconds. Then the controller resumes scanning the service request lines. The scan rate is about 150 kHz. The scanning circuits are designed so there is a dead zone between the time that each service request line is checked. This guarantees that there will be no transients that could cause access to be granted to the wrong calculator.

HANDSHAKE OPERATION

The calculator and the controller operate asynchronously. To guarantee that they do not get out of step and misinterpret data, all address and command signals from the calculator are flagged and receipt acknowledged by the controller (see Fig 7). Each time the controller acknowledges receipt of an address byte, the calculator checks the status lines to determine whether an error occurred. The controller does not always immediately acknowledge receipt; tests may be made on the information or some other operation performed first, but all transmissions are eventually acknowledged.

If an address error is detected during the transmission or reading of addresses, three attempts are made before the operation is terminated by the calculator. If a checkword error is detected in trying to read the data, ten attempts are made before the calculator gives up and displays an error message to the user. This technique makes momentary errors recoverable so the system is not affected by them.

RECORD FORMAT

A record is defined as the amount of information that is transferred to and from the mass memory in any given read or write operation. A record contains 256 words or 512 bytes of useable data. It also contains a preamble of 192 zero bits (See Fig. 5), a sync word, which is a 1 bit followed by 15 zeros, and an address word, which contains the binary equivalent of the three location variables (head, sector, and cylinder), followed by the data field of 256 words, the 16 bit checkword, and a postamble of 32 zero bits.

Each record occupies two sectors and begins only on the even numbered sectors. No address word exists for any odd numbered sector because this location is overwritten by the data field.

When information is written on the platter, a crystal controlled circuit provides a clock rate of 2.5 MHz. The data is mixed with this clock such that a 1 bit causes a transition to occur between clock pulses (See Fig. 5), while a zero bit does not cause a transition between clock pulses. When the information is read from the platter, the presence of a transition between clock pulses indicates a 1 bit; otherwise it is a zero bit.

Small variations in the speed of the platter cause the data transfer rate to fluctuate. Pulse crowding in the magnetic medium causes further perturbations in the transfer rate. When reading, therefore, it is necessary to synchronize with the data rate rather than any absolute reference. This synchronization is started at the beginning of each record. The 192 zero bits of the preamble allow a phase locked loop to synchronize to the 2.5 MHz data rate from the platter. Once it is locked, the loop becomes locked only to the clock rate.

There is uncertainty about exactly where in the preamble the phase locked loop becomes synchronized with the clock rate. The 1 bit of the sync word establishes a reference point so the remainder of the record can be correctly interpreted.

The checkword is a 16-bit word that is uniquely determined by the address word and the data field. It enables certain errors to be detected when the record is read from the platter. The postamble provides clock pulses at the end of the record to allow the read circuitry to complete the read operation.

The entire record must be written each time any portion of the data field is to be changed. However, the address word will always be the same because it corresponds to the physical location on the platter.

THE 11305A CONTROLLER

The 11305A controller can be functionally divided into several sections. These sections generally correspond to the different printed circuit boards of the controller. The calculator I/O board (11273-66591) provides communication between the calculator and cache memory and the calculator and disc controller. This board plugs into the back of the 9830A calculator. At the other end of the cable is the cache memory board (11273-66509). The cache memory is the receptacle for data transferred to and from the disc. Its operation is described in detail, along with the I/O card, elsewhere. Many of the calculator I/O system lines, particularly address lines, are passed through the cache memory card to the disc controller. The cache memory card plugs into the 11305A controller box.

In the controller itself are six PC boards, each having a more or less well defined function. The power supply board (11305-66502) has an obvious function, supplying +5VDC, +19VDC, and -19VDC to the system. One less obvious function is the supplying of +5VDC to each of up to four calculator I/O cards. The voltage is remotely sensed at each of the I/O cards. This was needed since the calculator I/O specifications do not allow enough current to be drawn from its +5V supply to operate these boards.

The memory control board (11305-66501) provides signals and control lines to the cache memory. Again, its functions are described in detail elsewhere.

The ROM board (11305-66503) contains the crystal clock circuits (5Mhz), system clock generation circuits, the qualifier selection and enabling circuits, ROM address circuitry, and the Read Only Memory itself. The ROM is a 256 state, 20 outputs per state, function generator. It is the heart of the system and its outputs control all of the functions of the controller.

Eight of its outputs are the next address. Six outputs provide three interdependent sets of instruction outputs, four bits each. Six more outputs select which of six decoders are to operate on the instruction outputs. The most significant present address bit is used to enable the address qualifier circuits. The address qualifiers are of two types. One inhibits any address change until the qualifier is met, and the second determines which of two next addresses is to be selected.

The instruction board (11305-66504) contains six decoder circuits for the six-bit ROM instruction outputs. Up to six different instructions may be given from each state of the ROM. These outputs are synchronously clocked into latches to maintain the proper system timing requirements and to avoid transient problems with switching states. The instruction outputs from the latches are also of two types: controlled and single state instructions. The controlled outputs are switched on and off and the single state outputs exist for only one state time, or 200 nanoseconds.

The data transfer board (11305-66505) contains the disc address multiplexing circuits, the cache memory data transfer multiplexing circuits, the address error comparators, the disc address latch circuits, the data transfer shift registers, and the disc operation control circuits.

The address control card (11305-66506) contains the user service director and disc availability selection circuits, the data encoding circuits, the phase locked loop and data decoding circuits, line drivers and receivers, the checkword computation and error detection circuits, and switching circuits for routing data to and from the disc and data transfer board.

Finally, the disc I/O card (11302-66510) provides the multiplexing for address and operation signals to the disc drive I/O lines, enable transfer of disc status signals to the controller, and decodes the address signals from calcualtor and controller to select the proper disc drive. The disc I/O card can be used with either a 9867A or 9867B disc drive by the proper positioning of four jumper wires. This card connects the disc drive to the controller and plugs into the controller.

The disc drive itself provides a head positioning servo system, address latch circuits, angular position detection circuits (sector information) disc status and disc selection decoding circuits, and read/write driver circuits for transfer of a data signal to and from the disc. A buffer card at the rear of the disc provides proper termination of the signal lines from the controller.

DISC OPERATIONAL SEQUENCE

Any operation involving the disc has several phases. These phases are the determination of the file address from a "directory" on the disc, the accessing of that file, and the updating of the directory as may be needed.

The disc directory contains the file names and addresses An availability table contains the addressess of unused records which may be selected for new files. A given file write operation could require as many as 10 or 20 read or write operations on the disc. While the average access time for the disc drive itself is about 50 milliseconds, it is apparent that no average file read or write time can readily be specified. A 1000 or 2000 word transfer could very easily require two or three seconds due to the large amount of bookkeeping needed by the program handling routines of the disc driver.

DETAILED WRITE OPERATION

In order to write a record onto the disc, the calculator must first place the data to be transferred in the cache memory. Then the calculator sends a service request (SRQ) to the controller via the calculator I/O system. The controller is continually sampling the service request lines as long as a disc operation is not in progress. A disc available signal (DAV) is sent to the calculator I/O card. The calculator then places the sector address, the disc select code, a read/write control bit, the head selection bit, and a sector address indentification bit on the I/O lines. A LOD pulse is sent to the controller which will latch the information and test the sector address for validity. The disc I/O board then enables the address information to appear on the disc address lines and it is latched into the disc with a SET HEAD pulse. The controller sends a data acknowledge signal (DAK) to the calculator I/O and waits for the next LOD pulse to signal that the cylinder address is present on the address lines. (This transfer of signals back and forth between the calculator I/O and controller is known as the "handshake" mode of operation. It is necessary when critical timing relationships must be met in asynchronous systems.) The disc select bits, must remain the same as for the sector address transfer. The disc I/O board places the cylinder address on the disc I/O lines and it is latched into the disc drive with a SET CYLINDER signal. An OUTPUT OPERATION signal is then sent to the disc I/O card. This switches the multiplex circuits to enable the disc status to be returned to the controller. When the SET CYLINDER signal is given to the disc drive, it begins a SEEK operation to find the appropriate cylinder. If the cylinder address was invalid (>203), the disc drive signals an illegal address and will not initiate the SEEK operation. The controller will, in that case, output SET HEAD and SET CYLINDER simultaneously, causing the head positioning servos to return to a reference position called HOME.

If all goes well, however, and the system has not been attacked by Murphy's Law, the controller will wait until the disc drive has found the correct location. This condition is indicated by the disc drive presenting three signals coincidently. They are ACCESS READY, SECTOR PULSE, and SECTOR COMPARE. The controller will then output a FORCE READ signal to the data transfer board. This in turn causes the read/write bit of the sector address to become a 1. This then transfers the correct bit pattern for a read operation to the disc I/O lines. The CONTROL signal is set low as soon as the end of the sector pulse is detected. This then switched into the clock generator circuits and the crystal clock switched off. The controller then waits until the SYNC 1 BIT is detected after the preamble zero bits. At this point the counter clocks are enabled and count the 16 bits of the synchronization word. At the end of 16 bits, the data from the disc is enabled and switched into the #1 shift register. The shift register clock has been previously enabled and begins to clock 8 bits of the address word into the shift register. As soon as the 8 bits are counted, the data and clock are switched to the #2 shift register and it is loaded with the second 8 bits of the address word. When this register is full, the data and clocks are switched off and the crystal clock is switched on. After a short delay to avoid switching transients, the CONTROL signal is set high, ending the disc operation. The controller then compares the address in the shift registers with the address sent by the calculator I/O. If they are exactly the same, a data acknowledge (DAK) is sent to the calculator I/O. The controller then waits for the calculator to send a LOD pulse to indicate that the sector address of the next record is on the calculator I/O lines. When this is received it is latched into the controller and placed on the disc I/O lines by an OUTPUT SECTOR pulse. A SET HEAD pulse is sent to the disc drive so that it can test for the proper sector location. The original read/write bit (assumed to be a 0, or write operation) is placed on the disc I/O lines. The controller again waits for the coincidence of the three signals from the disc drive. When this happens the multiplexed clock and data is switched to the disc and the CONTROL signal set low to begin the write operation. The counters are enabled to count 192 zero bits for the preamble.

While this is happening, the #1 shift register is filled with ones. After 192 zeroes have been recorded, a single 1 bit is gated from the #1 shift register to the multiplexer. This is the SYNC 1 BIT. After the 1 bit is gated in, 15 zeroes are switched to the multiplexer. After the first 8 bits of the sync word are recorded, the cylinder address data is gated into the #1 shift register. The data from the #2 shift register (which has been previously cleared) is gated into the multiplexer to fill out the last 8 zeroes of the sync word. As soon as the sync word is completed the data in the #1 shift register is gated into the multiplexer at the same time the checkword circuitry is enabled to begin the checkword computation for the record. While the contents of the #1 shift register are being written onto the disc, the sector address is being loaded into the #2 shift register. As soon as the cylinder address has been written, the #2 shift register is switched to the multiplexer and it is written on the disc. Corresponding switching is done to gate the data being written from the two shift registers to the checkword circuitry.

Here at last is the part everyone has been waiting for: Here comes THE DATA!! While the sector address is being written from the #2 shift register, data from the cache memory is gated into #1 shift register. A memory increment pulse ($\overline{\text{MIP}}$) is sent to the cache memory control card so that it can prepare the next 8-bit byte. When the last bit of the sector address has been written, the contents of the #1 shift register are gated into the multiplexer and the second byte of the data word is loaded into the #2 shift register. The controller then checks the cache memory to determine if it has emptied all 256 words. If not, a MIP is given and the cycle is repeated until the cache memory is completed (CMC). When the contents of the cache memory have been written on the disc, the checkword clock is shut off and the contents of the checkword register are gated into the multiplexer.

After all 16 bits have been written on the disc, 32 zero bits are written on the disc as a postamble. When the last word of the record has been written, the controller resets all of the pertinent signals and sends

a data acknowledge (DAK) to the calculator I/O which has been waiting since it last sent the incremented sector address to the disc. Finally, a disc operation complete (DOC) is sent to the memory control card and the calculator I/O card. The controller then again waits for a service request to begin another operation.

The read sequence is identical to the write operation except that the address word of the record is sent to the checkword circuits as it is read from the disc and data is transferred to the cache memory instead of being brought from it. After the read operation is completed, the controller tests the checkword register for all zeroes. If the contents are not all zeroes, an error message is set (CHECKWORD ERROR) before the data acknowledge pulse is sent to the calculator I/O. The disc driver software checks for any error message each time a DAK pulse is received from the controller.

CACHE MEMORY

The cache memory acts as temporary storage for data being transferred between the calculator memory and the platter. The memory portion of the system consists of four 1024 X 1, static, n-channel read/write memory devices. By accessing these four chips, four times, a 16 bit word can be written or read. Hence the system with a total capacity of 4096 bits, behaves like a 256 X 16 bit memory system.

The concept of using four bits parallel evolved from two considerations. First, the amount of time required to access the cache memory chips dictated that at least four or more bits should be accessed simultaneously (1.6µs for four bits transferring to and from the disc). Second, the number of chips required to give a 4096 bit memory capacity required by accessing two sectors of disc data. Eight chips would have halved the cache memory access time but would have wasted 50% of the memory.

Since the memory inside the 9830 operate from 8 Mhz clock signals and the disc and interface box should be capable of operating remote from the calculator, all signals from the calculator memory to the cache memory should be processed close to the internal calculator memory. Thus the calculator I/O card contains an address (M') register, data (T') register and control circuitry for the registers and cache memory instruction generation. There are two remaining cards in the cache memory system. One contains the memory chips, data register and address latches. The other acts as a control system and communication link between the cache memory and the disc controller.

OPERATION

The M' register, located on the calculator I/O card, is loaded simultaneously with data received by the internal address register. This is accomplished by bringing the most significant address bit from the internal address register (M15) and the two instructions which tell the address register to transfer data (MTS and TTM) to the I/O card. The OR of MTS and TTM gated with shift clock (SCK) allow data presented on the M15 line to be shifted into M' register. Hence the M' register always contains the current address shifted one bit to the left.

The addresses selected as cache memory addresses are octal 077000 to 077377 (Bit 15 used only for indirect addressing). Three open collector AND gates in IC 16 are wired ORed to decode address bits 9 thru 14 as all ones to indicate that the cache memory is being addressed Consequently the cache memory ignores bit 8 of the address.

Nothing is done with the ANDs output until either a read or write instruction is received from the calculator processor. The presence of either read (RDM) or write (WTM) and cache memory enable (output of the ANDs) allows the I/O card to take control. The first instruction given is EMB (extended memory busy) which must be received by the calculator memory control card immediately following RDM or WTM. This instruction causes the memory control card to hold the calculator processor in whichever state it is in until EMB is released. In this particular case, the calculator will continue to cycle through the read or write operation until the I/O releases EMB. Memory refresh of the 9830A will interrupt the read or write cycle.

WRITE OPERATION

After a valid cache memory address is in the M' register WTM causes an output line (RWC, read/write control) to go low which signals the cache memory card that a write operation is to be initiated. MBL (Memory Enable) going low triggers a 60 nanosecond monostable. The trailing edge of the monostable latches the lower 8 bits of the address from the M' register into two 4 bit latches (IC 18 and IC 19) located on the cache memory card. The J-input on flip-flop 01 of the I/O card then goes high which causes the Q output to go high on the next shift clock pulse. The $\overline{Q}$ output ($\overline{EDT}$ external data transfer) causes the internal T-register to shift data out on line TØØ into a four bit register (T'-register, IC 19). After the counter has been incremented from 0 to 3, thus allowing four clock pulses to pass, ff01 is reset. At this time the four least significant bits of data are in the T'-register.

The signal that reset ff01 is also the J-input of ff02. With the T'-register loaded with 4 bits of data, ff02 generates a signal DTB (data transfer begin). The four T' outputs are gated onto DBØ, DB1, DB2 and DB3. On the cache memory card, DTB triggers a 1µs monostable (IC 26). DTB and the output of this monostable are gated to the read/write control of the memory chips, thus acting as a write pulse. The write pulse allows the data to flow directly into the individual memory cells addressed by the address latches.

The trailing edge of the 1µs monostable fires a 250 ns monostable DTC (data transfer complete), which in turn goes back to the calculator I/O card setting an RS latch (IC 18). The output of this latch clears ff02 and causes the J-input of ff01 to go high. The RS latch holds the J-input of ff01 high until the next shift clock comes. This is necessary in case a refresh cycle interrupts the operation. DTC also clocks the flip-flops (IC 2) on the cache memory card. These two flip-flops act as the two most significant address bits to the memory chip. As they increment, a new cell/chip is addressed for each four bit byte.

This completes one portion of the write cycle. When ff01 is set by the next shift clock, $\overline{EDT}$ goes low and fetches four more bits from the T register. The cycle thus repeats four times until all 16 bits have been written into the cache memory. At this point the counter is in state 15 which acts as a J-input to ff00. SCK then causes $\overline{Q}$ output of ff00 to go low which in turn causes $\overline{EMB}$ to go high. This indicates that one word has been recorded in cache memory and the calculator goes on to its next step.

READ CYCLE

The addressing and memory enable portions of a memory cycle are identical for both read and write. During a read cycle RWC is high. The combination of RWC being high and MBL going low fires the 1µs monostable on the cache memory card. This time the lack of the write signal opens the memory chip outputs and data flows from the chips thru gates to the calculator I/O card.

The trailing edge of the 1µs one-shot fires the $\overline{\text{DTC}}$ one-shot which in turn acts as a parallel input strobe to the T' register. Therefore, the first four bits have been strobed into the T' register and now must be clocked into the internal T register. $\overline{\text{DTC}}$ increments the two address flip-flops so that the address is proper for the next 4 bit read. It also sets the RS latch on the calculator I/O card which in turn J's flip-flop 01. The next SCK sets ff01 causing $\overline{\text{EDT}}$ to go low. $\overline{\text{EDT}}$ is gated to the internal T register so that the calculator will accept serial-incoming data. SCK clocks both the counter and the T register causing T' data to be shifted out on the D-bus.

The counter at state 3 causes $\overline{\text{EDT}}$ to reset and $\overline{\text{DTB}}$ to be generated thus telling the cache memory to give the next four bits to the T' register. Again this cycle repeats four times until a full 16 bit word has been transferred from cache memory into the calculator.

This completes the data transfer between the calculator and cache memory.

MEMORY CYCLES TO AND FROM THE DISC

A third card in the cache memory system, the memory control card (11305-66501), acts as a data interface and instruction generator when there is communication between the disc and cache memory. The data interface allows bi-directional data flow from cache memory to memory control and disc controller to memory control. Cache memory addresses are kept track of by an 8 bit counter (IC 17 and IC 18). The read/write control for cache memory is also generated on the control card under disc direction. The disc read or write sequence is initiated from the calculator and is explained elsewhere in the write-up.

WRITE DATA ON DISC

When the calculator initiates a disc write, it generates a LOD (load pulse) on the cache memory card. The load pulse clears ff03 on the cache memory card which in turn enables the addresses to cache memory from the address counters located on the control card. When the controller is ready for data transfer from cache memory to the disc, a 1µs one-shot (IC 5 on memory control) holds the address at 000 octal until data can flow from cache memory to data latches (IC 6 and IC 10) on the control card. At the end of the 1µs one-shot, IAD (increment address), is fired which increments the two most significant bit address flip-flops on the cache memory card.

As the second one shot resets, it causes the 1st one-shot to again fire causing four more bits to flow and be latched into a second data latch on the control card. There are now 8 bits of data in the data registers. Nothing more happens until the disc controller has written this data on the disc.

The disc, upon completion of writing 8 bits, will issue a MIP (memory increment pulse) which will fire the 1µs one-shot and increment the address flip-flops. Again the two four-bit bytes are brought into the data latch. As the two most significant address bits are reset to zero, they cause a negative going transition on a signal called increment counter (ICT) which causes the address counter to increment by one. As the disc consumes each 8 bit byte, the MIP pulse is generated until the address counter has reached the 256th word.

The carry outputs of the counter clock a flip-flop which generates cache memory complete (CMC). This tells the controller that all 256 words (16 bit words) have been released from cache memory.

READ FROM THE DISC

A read instruction from the disc controller opens the gates to allow data flow from the controller to the cache memory control. When MIP is received, it causes the 1μs one-shot to fire and lets the four least significant bits to flow to memory. The 1μs one-shot is gated to the memory and acts as the write pulse to load the data into memory. As in the write cycle, when the one-shot resets, a second one-shot is fired to increment the address flip-flops. As the second one-shot resets, it refires the first and allows the second 4 bits to be written into memory.

After the 2nd four bits have been written the system waits for the next MIP. The process is repeated until the cache memory complete signal is fed back to the controller.

HEWLETT-PACKARD CO.

THEORY OF OPERATION

11305-66503

This assembly is the heart of the whole controller. It contains the system clocks, the address register, the address qualifier circuits, and the stored instruction set for controller operation - the ROM.

The ROM contains all of the information needed to generate the next state-of-machine address, issue a set of coded instructions and decoder selection, and determines which qualifiers are to be tested and when they are checked.

The ROM is made of five chips which are each organized in a 256 X 4 bit format. This gives a total output of 256 states of 20 output bits each. The outputs are all open collector. All five chips have common address lines. The first two chips, IC 12 and 14, provide the next address to be accessed. These lines are returned to the D inputs of the address register and the next clock pulse will latch in these levels. They then become the address inputs for the ROM.

The next six outputs, IC 16 and 18, pins 9 and 10, provide the selection bits which determine which of the six decoders on the 11305-66504 assembly are enabled. The last six bits, IC 18 pins 11 and 12 and IC 20, provide the coded instruction information which is sent to the 11305-66504 assembly. All of the ROM outputs are available on top edge connectors for monitoring with a test fixture or for use with a single step tester. The present address is also available. A means is also provided for setting the present address to any desired state with the single step tester (ET 7426).

The basic system clock is a 5 MHz crystal. This is gated through IC 32 pin 12 and all other clocks are derived from it. IC 32 also allows the system clock to be halted through the INHIBIT CLOCK signal..

MODEL 11305A	STK NO
THEORY OF OPERATION FOR 11305-66503	
BY R. Kochis & H. Bradl	DATE

When this signal is low, the controller may be operated by an EXTERNAL CLOCK. A third signal SELECT DISC CLOCK disconnects the crystal clock and allows the system to be run from the DISC CLOCK signal. This is the 5MHz clock which is derived from the information recorded on a platter. It is used only during read operations. The remaining circuitry associated with this section guarantees that, when switching from crystal clock to disc clock and back, that the proper phase of the clock is maintained and that no short spikes are encountered when switching the two asynchronous clocks.

IC 27 divides the 5MHz by 2 and provides the second input for the 2 to 4 decoder, IC 10. The inverter on IC 27 pin 1 and the two inverters in series on IC 10 pin 13 provide critical time delay equalizing and phase adjustment so that the outputs of IC 10 pins 4, 5, and 6 bear the proper phase relationship to the 5 MHz and 2.5 MHz system clocks. These relationships are defined in the system timing diagrams.

The qualifier circuits are designed to affect addresses in two ways. The most often used is the type that prevents the address register from clocking in the next address. The second type modifies the address to something different from what the ROM output might be.

Whenever the most significant ROM address bit (IC 6, pin 9) is a 1, all qualifiers are enabled. The least 4 significant bits of the address determine which of the qualifiers is selected. A total of 16 qualifiers are used.

When an address inhibit qualifier is selected, IC 29, pin 9 goes low. The 4 least significant address bits that appear on IC 29 pins 11, 13, 14. and 15 enable one of the 16 input lines. As long as the input line is high, the output at pin 10 remains low. This holds IC 8 pin 5 low and keeps the system clock from latching in the new address. When the qualifier input line goes low, IC 29 pin 10 then goes high. The next positive clock edge then releases the two clock gates of IC 7 and the next address is latched in.

If one of the address modifier qualifiers is selected, IC 29 pin 9 still goes low and one of its inputs is selected. However, this input is tied low so that the clock is not held up. In this case the output of one of IC 13,15,17,19,21,22, or 23 (whichever one was selected) will be either high or low, depending on the level of the qualifier input. The ROM output for the next address bit corresponding to the address bit which the qualifier modifies must always beaa 1. The qualifier bit and the ROM address bit are inputs to the AND gate which drives the D input of the address latch. There fore the qualifier has control over whether that next address bit is a 1 or Ø. Whenever a qualifier gate is not selected, its output is high and allows the ROM bit to determine the next address. There is no delay in the next address when this type of qualifier is used.

Whenever the controller detects an address error before a read or write operation, it sends a signal to the Mass Memory to seek home. This resets the head positioning service to a reference position. The address is then reissued.. If the address is sent to the Mass Memory before the same position is found, another address error is created. Therefore ACCESS READY is sent to IC 31 pin 5 as an enabling input for the LOD pulse sent by the calculator. The LOD pulse tells the controller that the address is ready to be sent to the Mass Memory. IF ACCESS READY did not hold off the next address, three address errors would be immediately generated and the calculator would halt with an ERROR 90. By holding off the LOD pulse, three attempts can be made to reread the address before ERROR 90 occurs.

Before a Mass Memory will output a valid ACCESS READY, the unit selectlines on the 11302-66510 assembly must have the proper code which corresponds to that Mass Memory. The LOD pulse which comes from the calculator is used to do this directly so that ACCESS READY in turn will allow the controller to receive the LOD pulse.. When the controller accepts the address, the LATCH PULSE clocks in the address on the 11305-66505 assembly and resets the LOD latch, IC 8. This guarantees that a new LOD pulse must be received before

the next address byte can be processed.

After the Mass Memory head has reached to proper location the SECTOR COMPARE signal indicates the proper record has been found. IC 30, pin 13 detects the leading edge of this signal. It must be gated with ACCESS READY to be sure the proper track is reached. IC 30 pin 13 provides a short delay before triggering IC 30 pin 9. When IC 30 pin 5, ACCESS READY and SECTOR COMPARE are all true, then the qualifier input on IC 29 pin 22 is valid. The delay at IC 30 pin 13 is needed because the SECTOR COMPARE will signal and will sometimes have noise on its trailing edge. This could be detected as a false leading edge and begin a read or write operation in the middle of a record and either give errors or destroy that track on the plotter.

HEWLETT-PACKARD CO.

THEORY OF OPERATION

11305-66504

This assembly converts ROM outputs from the 11305-66503 assembly into signals which control the entire system. It generates two kinds of signals-- those which are switched on and off, and those which last only for the duration of one clock period of 200 nano seconds.

All of these instructions (44) are generated by 12 signal lines coming from the 11305-66503 ROM. Six of these lines contain the coded instructions and six lines select which decoders are enabled to operate on the instructions.

Each decoder may be selected independently of the others; each is selected by one of the signals $\overline{50}$ - $\overline{55}$. Each decoder has four instruction signals; the decoders selected by $\overline{50}$ and $\overline{51}$ use 10, 11, 12, and 13. The encoders selected by $\overline{52}$ and $\overline{53}$ use instructions 11, 12, 13, and 14. The encoders selected by $\overline{54}$ and $\overline{55}$ use instructions 12, 13, 14, and 15. Because the instruction groups overlap, they are not independent of each other and certain instructions exclude others. This has been taken into consideration in designing the ROM on the 11305-66503 assembly.

The Instruction inputs are positive true logic, the selection lines are negative true. Each of sixteen possible outputs is also negative true.

To avoid any transient spikes in the system instructions, all of the decoder outputs are synchronously clocked into latches and flip flaps. The ROM outputs are generated on a negative clock edge and they are clocked into the output latches on the next negative clock edge. There is sufficient time for all of the signals to be decoded and appear at the latches before the next negative clock edge (200 nano seconds later). Those which must be turned on and off are inverted to positive true logic and then sent to J-K inputs of flip flops. In some cases further decoding is needed after the signals are latched.

When power is first turned on, the $\overline{POP}$, (see 11305-66501

				MODEL 11305A	STK NO
				THEORY OF OPERATION FOR THE 11305-66504	
				BY R Kochis & H Bradley	DATE
				APPD	SHEET NO 1 OF 2

THEORY OF OPERATION) pulse generates a $\overline{\text{RST}}$ which enables the crystal clock circuitry output. This is necessary to be sure system clocks are generated on turn on. If the disc clock were by chance inabled there would be no disc clock present and the system would be permanently locked up. The DRIVE UNSAFE signal will automatically set the DRIVE UNSAFE flip flop and then output a $\overline{\text{DAK}}$ (DATA ACKNOWLEDGE) pulse to the calculator. It will then reset the controller to its turn on state ($\overline{\text{RST}}$) and recycle the entire system. This guarantees that all parts of the system are properly initialized for further operations. The $\overline{\text{TMT}}$ pulse (from the 11305-66506 assembly) provides the same function in the event that signal communication is lost between the calculator and controller or the Mass Memory and controller. If communication is lost for approximately three seconds, $\overline{\text{TMT}}$ (Too Much Time) is generated and resets the system.

HEWLETT-PACKARD CO.

THEORY OF OPERATION

11305-66505

This assembly can best be described by the functional sequence of operations in a normal read/write operation. The sector address is first presented on DO Ø - DO 7 by the calculator. For this byte of data, 502 is a 1. This enables the clock pulse input of the 8 bit latch, IC 6. The LATCH PULSE then clocks in the five bit sector address (DOØ - D04), the head bit (D05), the read/write bit (D06; Ø + write, 1 + read), and the initialize bit, D07. If the LSB of the sector address (DO Ø) is a 1, this is an illegal odd sector address and it generates an ILLEGAL ADDRESS.

The next address byte is the eight bit cylinder address (DOØ - D07) and is gated into latch 2 by the LATCH PULSE because the 502 bit is now Ø. The SET HEAD pulse which latches the head and sector information into the Mass Memory (see 11302-66510 Theory of Operation) also enables the SEEK CHECK line (see 11302-66510). If the cylinderr address is illegal or unaccepted, this signal will also generate an ILLEGAL ADDRESS. Also, if the initialized bit (D07) and the setting of the CONTROLLER MODE switch on the front panel do not match, an ILLEGAL ADDRESS is generated and sent to the 11305-66503 assembly.

Whenever a read/write operation (NOT initialized) is being done, the address must first be read from the plotter and compared with the address latched into IC6 and IC 7. Therefore, regardless of whether the read/write bit is 1 or Ø, the FORCE READ pulse overrides whatever D06 may have been and generates a READ command. This is clocked into IC3 by the 5 MHZ system clock. This also prevents any cache memory operation from starting (by setting EMO high) when CONTROL goes low to start reading the address.

As soon as the start of the address is detected, the DISC DATA is gated into shift register 2, IC 16. This shifts in the sector and head address. The DISC DATA is then shifted to SR1 and shifts in the cylinder address as it is read. CONTROL then goes high and terminates the READ operation. The address (Sector,

LTR	P.C. NO	APPROVED	DATE	MODEL 11305A	STK NO
				THEORY OF OPERATION (11305-66505)	
				BY R. Kochis & H. Bradley	DATE
				APPD	SHEET NO 1 OF 3

head, and cylinder) contained in the shift registers is then compared bit for bit with the address in the latches. If any bit differs, POSITION CORRECT is low and is detected on the 11305-66503 assembly.

After the address is verified, the RELEASE R/W pulse allows the read/write bit to appear on the READ and READ lines. A new sector address byte that has been incremented by two is latched into IC 6. Assume that the operation is a write; D06 = Ø. When the proper position is found, CONTROL goes low. This sets EMO low and allows information to transfer from cache memory.

IC16, the #2 shift register has been cleared. Its output (zero) is gated to the encoder circuitry on the 11305-66506 assembly. This is recording the preamble of 192 zero bits. The shift register clock is enabled for a portion of the preamble and is gated to shift register 1, IC17. This fills SR1 with ones because its input at pin 2 remains high. The shift register clock is then shut off.

After 192 zero bits (12 words) have been counted, the output of SR1 is gated to the encoder for a single 1 bit. This is the sync. one bit. The output of SR2 is again gated to the encoder to complete the sync 1 word with zeros.

While this word is being recorded, the shift register mode control is set parallel (high on IC16 and 17, pin 23). The tri-state gates (IC 10 and 11) are enabled to pass data from latch 1, IC7 to SR1. The shift register clock is turned on and parallel loads the cylinder address into SR1 when the clock is gated into SR1. The clock is then removed from SR1 and the tri state gates disabled. (SR1 and SR2 have certain restrictions on the clock when changing modes of operation. Refer to the T.I. data sheet on 74198 specifications.) a MIP pulse is sent to the Memory Control (11305-66501 assembly) to bring the first eight bits of data to the inputs of tri-state gates which drive the inputs of SR1 and SR2. This is done so that the data will be present when it is needed. The mode control of SR1 is then set to shift.

When the end of the sync 1 word is reached, the output of SR1 is gated to the encoder and the SR clock is

gated to SR1. This begins recording of the address. While this being done, the tri-state gates are enabled which transfers the sector and head address to SR2 and the SR clock is also gated to SR2 which parallel loads the register. The SR clock is then removed from SR2 and the tri-state gates disabled. SR2 is then set to shift mode.

When the cylinder address from SR1 is recorded, the output of SR2 is gated to the encoder and the output of SR1 switched out. The mode control of SR1 is set to parallel load and CACHE MEMORY DATA TO SR1 enabled. After one SR clock pulse to load this data byte into SR1, the SR clock is disabled from SR1. SR1 is then set to shift mode. Another MIP pulse is sent to the Memory Control assembly to prepare the next data byte.

When the sector and head address are finished being recorded from SR2, the output of SR1 is switched to the encoder and the SR2 output switched out. SR2 is set to parallel load and the CACHE MEMORY DATA to SR2, the clock is disabled to SR1 and SR2 is set to shift mode.

This switching back and forth between SR1 and SR2 continues until all of the CACHE MEMORY DATA is recorded.

A READ operation uses exactly the same sequences except that there is no need to record the preamble and address. Therefore the shift registers are not enabled until the data field is reached. Then SR1 is set to shift mode, the SR clock switched to SR1, and DISC DATA gated into SR1. When the first eight bits have been shifted into SR1, the SR clock and DISC DATA are gated to SR2. The SR1 DATA TO CACHE MEMORY gates are enabled and a MIP sent to the Memory Control to process the data byte. When the second byte is shifted into SR2, the data is gated into SR1 and the SR2 contents gated to CACHE MEMORY. This continues until the CACHE MEMORY is filled.

HEWLETT-PACKARD CO.

THEORY OF OPERATION

11305-66506

This assembly has six relatively independent functions. These are: 1) service request control, 2) word and byte counters, 3) checkword computation, 4) line drivers and receivers, 5) data switching and encoding, and 6) data and clock recovery.

The counters have outputs for counting 8, 12, or 16 clock pulses. When both counters are driven in parallel, they function as counters for 8 and 16 bits. When they are switched to the serial mode, the #1 counter, IC 18, counts 16 bits. Its output is then fed into the #2 counter, IC1, as a clock input. Then the #2 counter functions as a word counter with outputs for eight and 12 words. This mode is used when recording the preamble to each record on the plotter.

The service request circuits must check each calculator position to determine if a Mass Memory operation is requested. When a service request (SRQX) is detected that calculator will retain control of the system for as long as its request line is low. It also has about 300 milliseconds to release control and then come back and still be in control of the system. If it requests service but does not release control at all within three seconds, the system resets and outputs an error condition. This prevents a faulty circuit from locking out all calculators.

When no service request is present, all outputs of IC21 are high. IC 26 remains cleared and thus the output of IC11 pun 11 is high. This maintains a high input at IC9, pin 1 and IC 22 pins 14 and 15. The 625KHZ clock output of IC 23 pin 12 then provides clock inputs for IC 25 pin 1, IC 22, pin 1, and IC2 pin 1. IC2 is constantly retriggered and will not output an error condition unless the clock input is gone for about three seconds. It then would set DUS low and trigger the TMT signal to the 11305-66504 assembly to reset the system.

With IC 22 pins 14 and 15 high and a clock present on pin 1, pin 3 has a 156.25 KHZ square wave signal on it.

				MODEL 11305A	STK NO
				THEORY OF OPERATION (11305-66506)	
				BY R.Kochis & H.Bradley	DATE

This causes the outputs at pins 4, 5, 6, and 7 of IC 22 to sequentially go low from their normal high state. There is a period of time between each output going low where all of the outputs are high. This is necessary to allow for timing delays in transferring signals back to the calculators. The outputs on pins 9, 10, 11, and 12 remain high as long as a high input on pins 14 and 15 keep them disabled.

When a calculator requests service, one of the $\overline{\text{SRQX}}$ lines goes low. As soon as one of the enabling inputs to the same gate on IC 21 goes low, the system will lock up and enable one of the outputs from IC 22, pins 9, 10, 11, or 12 ($\overline{\text{DAVX}}$) to allow that calculator to begin to transfer information.

The service request can go away for about 250 milliseconds without losing the service request lockup. IC 26, pin 4 will hold the lockup condition for this long. As soon as lockup is released, the service request circuitry again continues to look at each calculator service request line sequentially.

The data selection and encoding circuits switch the data to be recorded from shift register 1 or 2 (from the 11305-66505 assembly) as needed by the system timing requirements. The data then takes two paths for a write operation. IC 12, pin 13 allows the data to be sent to the checkword circuitry while the data is being recorded. IC 12, pin 9 allows the data to be sent to the checkword circuitry while it is being read from the plotter.

IC 12, pin 2 allows the data to be encoded with the clock pulses at IC 27, pins 1, 13, and 9. The encoded data is then converted into 60 nanosecond pulses at IC 26, pin 9. After all of the data is encoded, IC 12, pin 5 allows the checkword to be encoded and recorded on the plotter.

The line drivers accepts the 60 nanosecond pulses from IC 26, pin 5 and converts them to a differential signal of about 600 millivolts. This signal is transmitted on a twisted pair which is terminated at both ends by a line driver and receiver. This pair of wires is the bi-directional data bus. Because it is a differential

pair, it has excellent crosstalk and noise immunity. Care must be taken not to reverse the connections of the twisted pair as this will result in an inverted signal and improper operation of the phase locked loop.

The checkword circuitry performs a computation on the address and data field as it is recorded. At the end of the recording of data, the contents of the checkword register are sent through IC 12, pin 5 to be encoded and recorded on the plotter. When the information is read back, the address and data are sent through IC 9, 12 pin 12 to the checkword circuits. At the end of the data field, the previously recorded checkword is also sent to the checkword circuits. After this is completed, the checkword register should contain all zeros. If any bit is a one, the CHECKWORD ERROR signal is low, indicating that data has been misread. (Refer to appendix A for a detailed explanation of the theory of checkword computation and implementation.)

The phase locked loop circuitry is used to separate the clock and data in the signal read back from the plotter. Its function depends on the fact that all clock pulses are present in the signal read back. These pulses have a frequency of 2.5 MHZ, The only data pulses included are those for one bit. These pulses are inserted between the clock pulses. The phase locked loop responds to the average frequency of the clock pulses and can track a change in frequency that happens over 5 to 10 clock pulses. The first 192 bits of the preamble of any record all are zeros; these consist only of clock pulses and allow the phase locked loop time to become synchronized with the received clock pulses. This takes about 4 or 5 microseconds. The DISC DATA flip flop, IC 13, is held in a cleared state while this synchronization takes place. Therefore, the first 1 bit that is detected is the sync 1 bit and provides the controller with a reference point for its position in the recorded data field.

The controller circuitry uses a 5 MHZ basic clock rate. The voltage controlled oscillator of the phase locked loop is designed to operate a 10 MHZ rate.

There is inherently a large amount of variation in the symmetry of the 10 MHZ signal. Therefore, it is divided by 2 to reduce these variations in the 5 MHZ clock that is provided to the system on the 11305-66503 assembly by an edge triggered flip flop. It is critical that this flip flop maintain the proper phase relationship to the 5 MHZ signal. This timing is provided by the detection of the sync 1 bit. When this bit is detected the 2.5 MHZ flip flop is released and begins to toggle in the proper phase relationship with the 5 MHZ clock frequency.

Power supplies are needed for the +6V, -5V, and -12V used by the line drivers and receivers and the phase locked loop.

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THEORY OF OPERATION

11302-66510

This assembly has four primary functions. These are: 1) Mass Memory Unit selection, 2) address multiplex and transfer, 3) operation commands and initiation, and 4) Mass Memory status return.

Before any operation can take place, the Mass Memory unit must be selected. Both address bytes sent out by the 9830 contain the unit select bits. These appear on the SØ and SO 1 lines. SO Ø is sent out as the least significant bit. If the four jumper wires are in the A position (resulting in a 11302-66510 assembly for a 9867A) then these two signals appear on the D inputs (pins 2 and 12) of IC2 and 5. When the $\overline{\text{LOD}}$ pulse is received from the calculator, these signals are clocked into the D latches on the positive edge of $\overline{\text{LOD}}$ as it goes away. $\overline{\text{LOD}}$ is about 300 nanoseconds long.

SO Ø and SO 1 are positive true signals. Because all signals sent to the Mass Memory are negative true, the $\overline{Q}$ outputs of the D latches are used. These two si signals now appear at $\overline{\text{SELECT 1}}$ and $\overline{\text{SELECT Ø}}$.

Since up to four 9867A Mass Memory units can be used, both bits of data are used. Because the 11305A controller does not accept the first address byte until a Mass Memory indicates it is on line (see 11305-66503 theory of operation), it is necessary to use the $\overline{\text{LOD}}$ pulse to gate the unit select information to the Mass Memory. When the proper unit select is received by the Mass Memory, it then will return an $\overline{\text{ACCESS READY}}$ signal to the 11305A. The remaining address information will then be processed.

When the jumpers are in the B position (corresponding to a 9867B), the select bits are handled somewhat differently. The 9867B has two plotters in each Mass Memory. Since the system can handle four plotters, only two 9867B Mass Memory units can be used. Therefore, only one bit of the $\overline{\text{SELECT}}$ lines is used to select one of these two units. This is why $\overline{\text{SELECT 1}}$ is connected to +5 volts for a 11302-66511 (9867B) assembly.

LTR	P C NO	APPROVED	DATE	MODEL 11305A	STK NO
				THEORY OF OPERATION (11302-66510)	
				BY R Kockis & H Bradley	DATE
				APPD	SHEET NO 1 OF 4

The Mass Memory ROM treats each platter as a separate storage media. It cannot distinguish between four 9867As or two 9867Bs. This means that the unit select bits on SØ and S01 will be the same for both systems. Therefore only S01 is used to select one of two 9867B units. SØ is then routed to OUTBUSØ to select either the removeable cartridge (SØ=Ø) or the fixed platter (SØ=1).

The 9867B must be set internally to respond to unit Ø or unit 2. This is done by placing the jumper pins on assembly 07900-60058 (A7) to position AC for unit 2.

After the unit select has been acknowledged by ACCESS READY going low, the 11305 will give an OUTPUT SECTOR signal. This causes IC 3 pin 9 to go high and enable the sector address and head bit information on OTØ-OT7 to transfer to OUTBUS 7 - OUTBUS Ø, OT7 is always a Ø during the OUTPUT SECTOR operation (See 11305-66505 Theory of Operation), The OUTPUT OPERATION signal from IC 5 pin 5 is also low during this phase of address transfer. It is reset on turn on and at the end of each read or write operation. The OUTPUT ADDRESS line from IC 11 pin 8 will be high for both sector and cylinder address transfers. Note that if the jumpers are in position B, the platter select bit from SØ is sent through IC 7, 11, 6, and 10 to OUTBUS Ø for selecting either the removeable cartridge or the fixed platter. OT7 must be a Ø to avoid interfering with the signal. The OUTPUT SECTOR signal also performs the function of resetting the sector over run counter, IC 9 and 12. RELEASE OPERATION is also used for this function.

After the sector and head information is present on the OUTBUS 7 - OUTBUS Ø lines, the controller will output a SET HEAD pulse of 200 nanoseconds. This latches the sector and head information into the Mass Memory. The head bit appears on OT6. The next address information that appears is the cylinder address. This data appears on OTØ -OT7. The unit select bits remain the same as for the sector byte. The controller then gives an OUTPUT CYLINDER signal which resets the OUTPUT SECTOR signal and removes the platter select

bit from IC 7 pin 11. This lets the cylinder data on IC 11 pin 4 transfer through to OUTBUS Ø. The controller will then output a SET CYLINDER pulse to latch the cylinder address into the Mass Memory.

The controller will next give an OUTPUT OPERATION signal. This will reset both OUTPUT SECTOR and OUTPUT CYLINDER. This also allows the read/write bit on the READ line to be encoded on OUTBUS Ø-OUTBUS 2. In addition OUTBUS 3 - OUTBUS 6 are set high to prevent them from causing any interaction during the operation. OUTBUS 7 is set low to enable the Mass Memory to transfer its status signals back to the 11305.

The Read line determines which type of operation is to be performed. OUTBUS Ø - OUTBUS 2 signals are used by the Mass Memory to control which type of operation it does. These signals must remain constant during the operation.

When the proper platter location has been found (ACCESS READY and SECTOR COMPARE and SECTOR PULSE) the controller will begin the operation by setting CONTROL low. If it is a write operation, data will be sent to the Mass Memory on R/W DATA 1 and R/W DATA 2. For a read operation, the Mass Memory sends data to the controller on these two lines. They comprise a bi-directional differential pair data bus.

For a detailed explanation of the status lines and Mass Memory I/O lines, refer to 7900A or 7901A operating and service manuals and inferface guides.

A safety circuit is incorporated into IC 9 and 12 using SECTOR PULSE and CONTROL. All read/write operations must be terminated within two sectors - - one record. When CONTROL is low. Sector pulses begin incrementing a counter. If three sector pulses are detected before an operation is completed, CONTROL is forced high and a DRIVE UNSAFE error is generated.

Write protection is accomplished by setting a switch on the Mass Memory. This causes SURFACE PROTECT to

be low whenever status from the Mass Memory is enabled. This is then gated with READ and CONTROL so that if a write operation is attempted, a DRIVE UNSAFE is given at the completion of the operation. Nothing was actually written and this signal indicated that the operation was not performed successfully.

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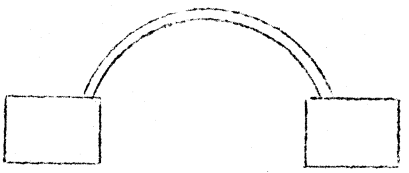
9860A/B MASS MEMORY SYSTEM

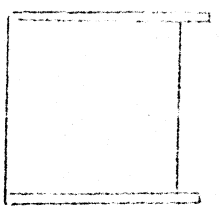
11273B PLUG IN ROM BLOCK

1K ROM CLIP IN BLOCK CONTAINS SOFTWARE TO ALLOW THE 9830 TO READ AND WRITE ON THE MASS MEMORY

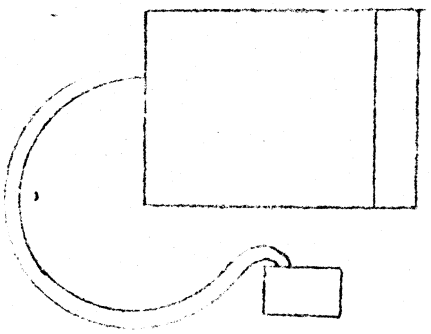


11272B INTERFACE CABLE ASSEMBLY

11273 INTERFACE CABLE ASSEMBLY CONTAINS 9830'S INTERFACE CABLE AND 256 WORD CACHE MEMORY



THE 11305 CONTROLLER CONTAINS THE ELECTRONICS TO TRANSFER DATA TO AND FROM THE 9867 MASS MEMORY



9867A/B MASS MEMORY (DISC DRIVE)

THE 9867A OR 9867B MASS MEMORY PROVIDES THE POSITIONING CIRCUITRY AND READ/WRITE ELECTRONICS FOR READING AND WRITING ON THE DISC PLATTER

FIG 1

MODEL		STK NO	
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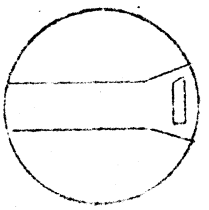


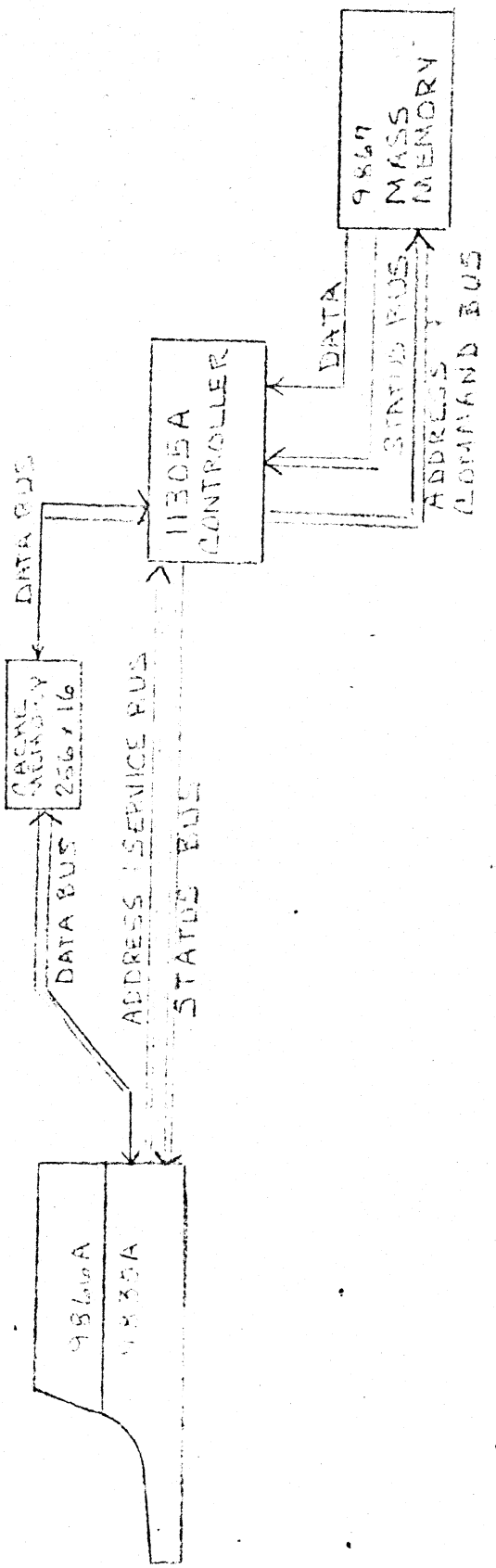
12869A CARTRIDGE

EACH 12869A CARTRIDGE PROVIDES 2.4M BYTES OF STORAGE. IN ADDITION, 7K OF SYSTEM SOFTWARE RESIDES ON EACH PLATTER AFTER IT IS FORMATTED FOR SYSTEM USE.

FIG 1 (CONT)

				MODEL	STK NO
				BY	DATE
LTR	P.C. NO	APPROVED	DATE	APPD	SHEET NO OF

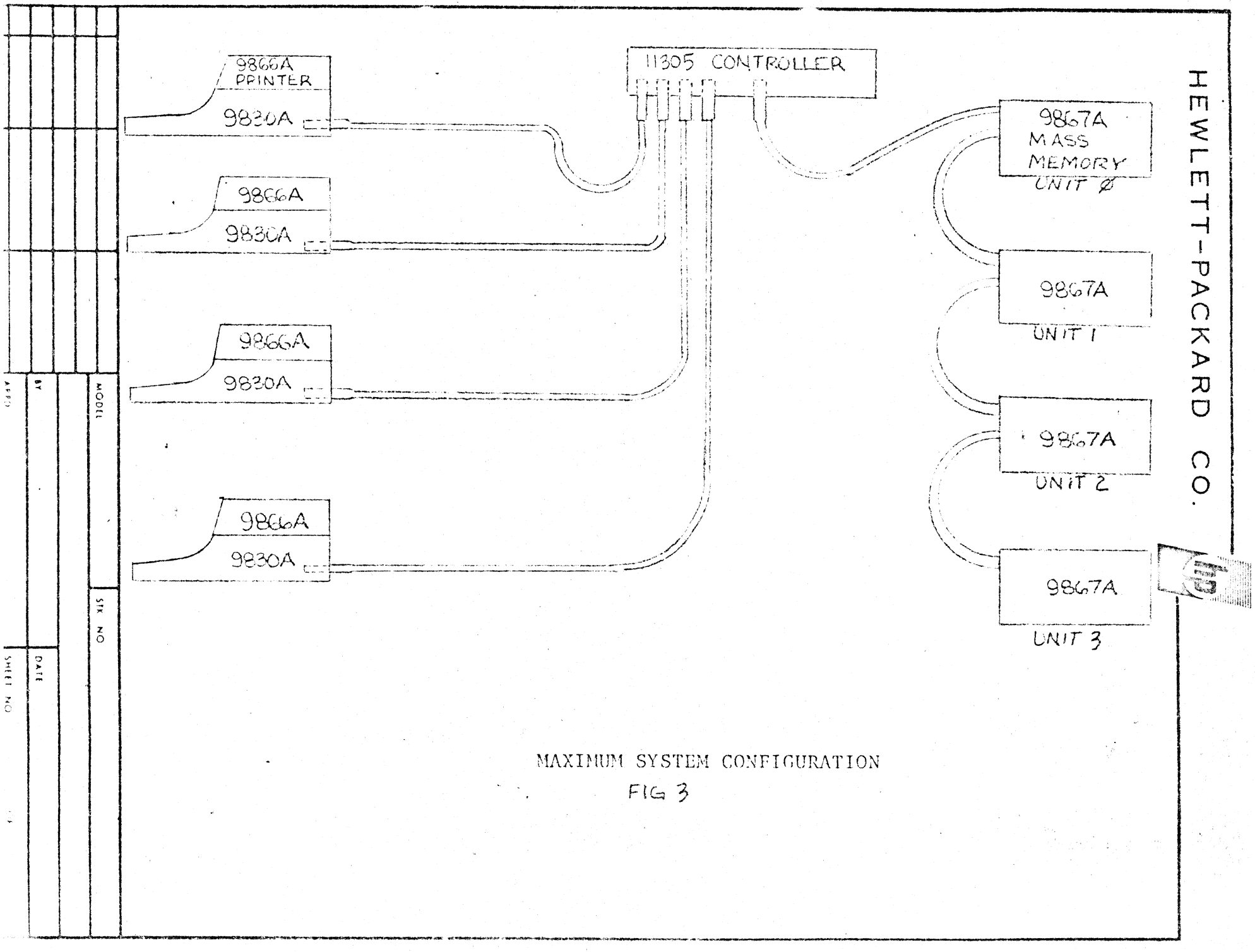
HEWLETT-PACKARD CO.



ADDRESS, DATA AND STATUS TRANSFER

FIG 2

				MODEL	STK NO
				BY	DATE
				APPD	SHEET NO OF



MAXIMUM SYSTEM CONFIGURATION

FIG 3

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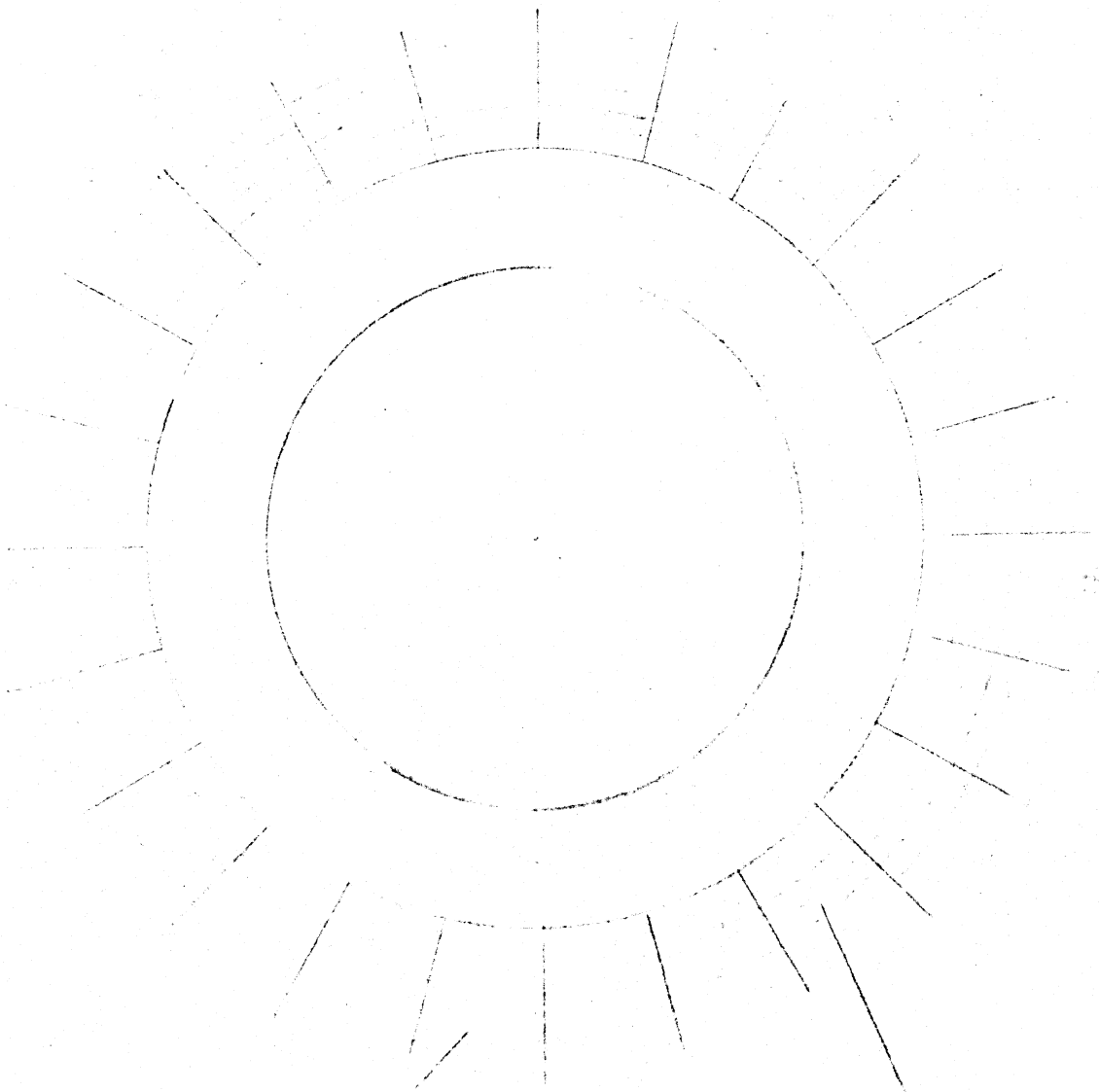
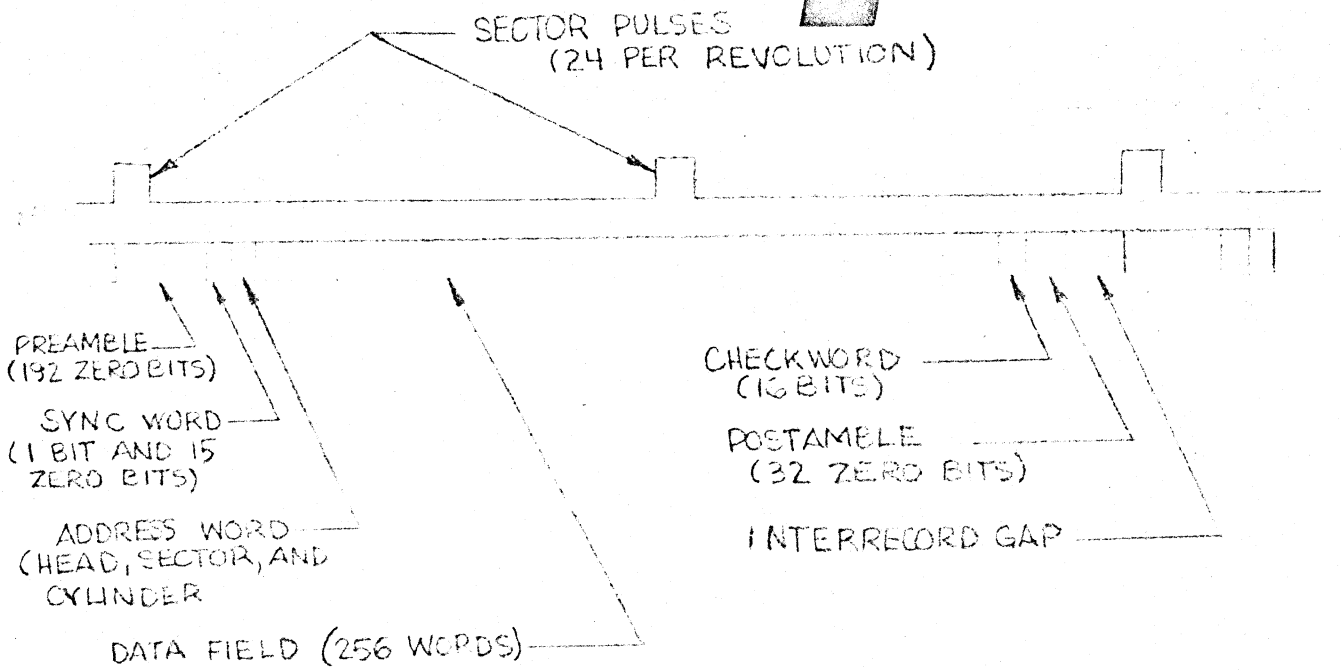
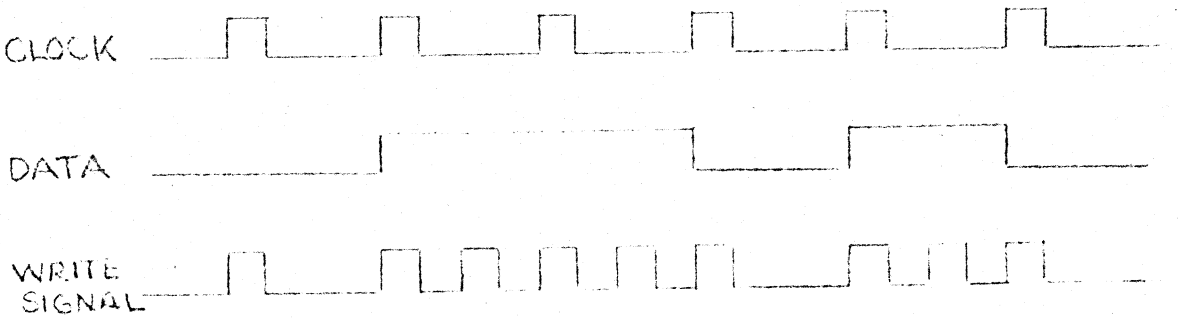


PLATTER ORGANIZATION FIG 4

				MODEL	STK NO
				BY	DATE

HEWLETT-PACKARD CO.



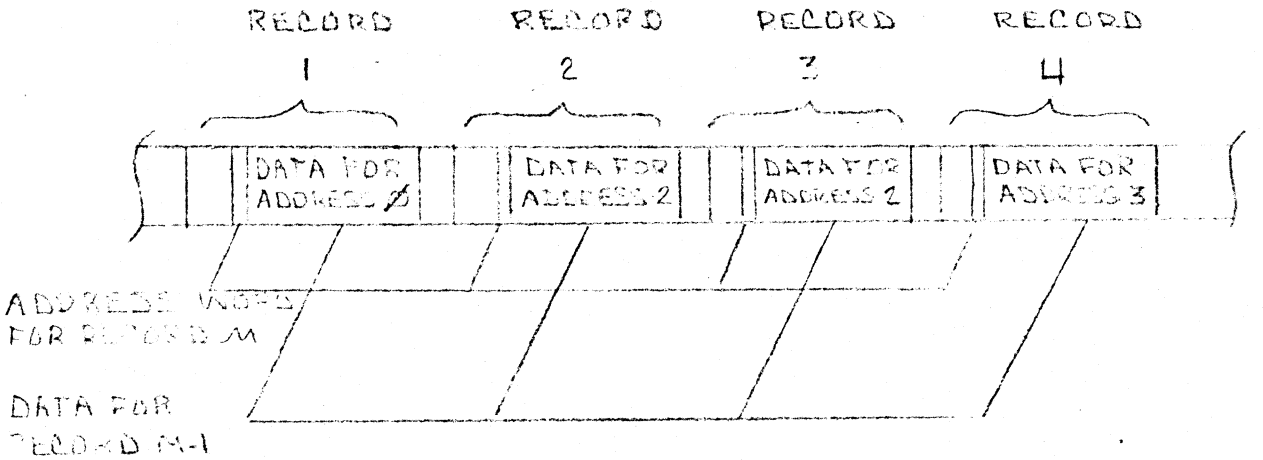


READ FORMAT AND
WRITE SIGNAL GENERATION

FIG 5

				MODEL	STK NO
				BY	DATE

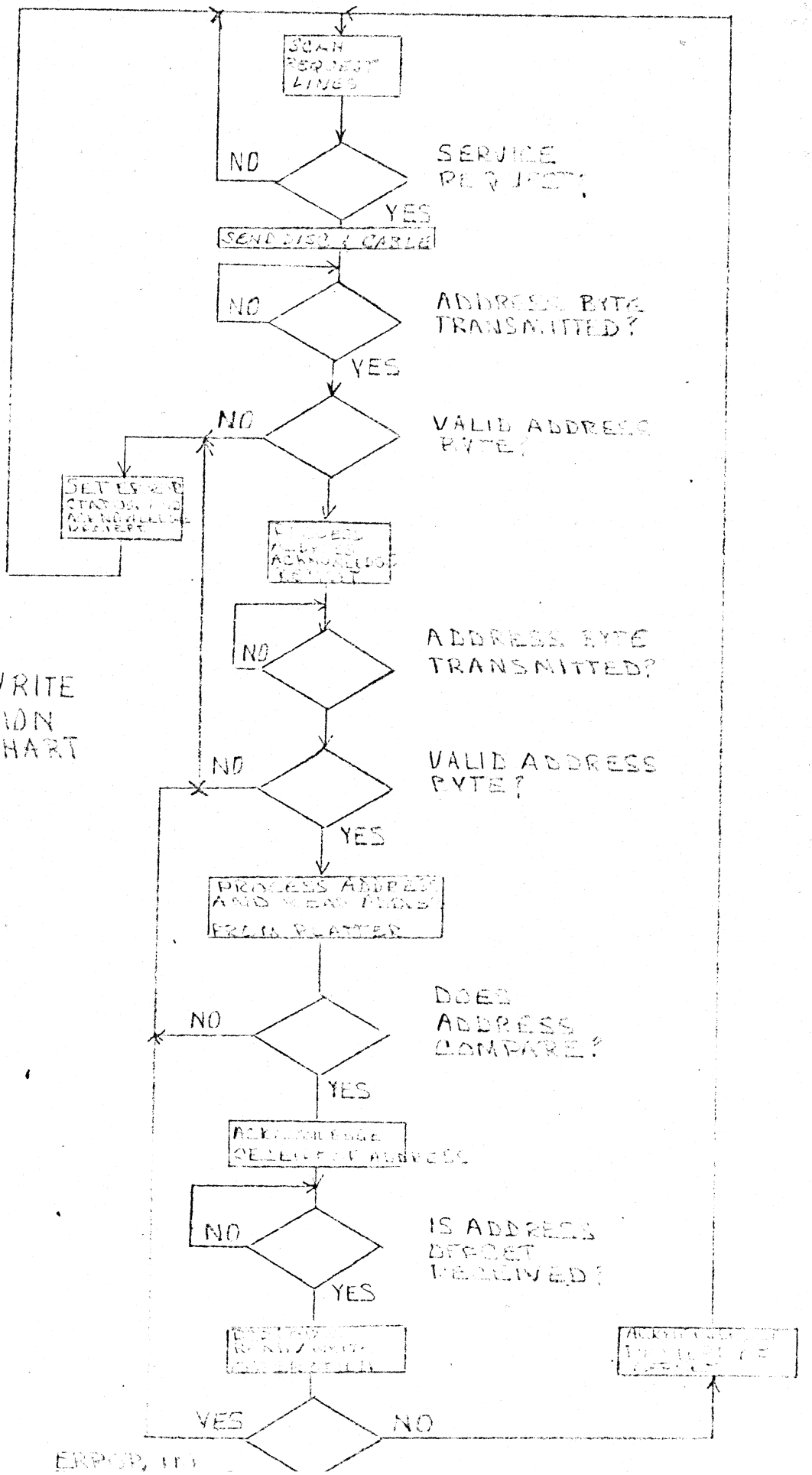
HEWLETT-PACKARD CO.



DATA OFFSET FOR ADDRESS M

FIG 6

				MODEL	STK NO
				BY	DATE
				APPD	SHEET NO OF



READ/WRITE OPERATION FLOW CHART

FIG 7