HEWLETT-PACKARD CO.
ELECTRONIC TEST INSTRUMENTS

# SPECIFICATION

## 9-1000

## 4096 BIT MOS N-CHANNEL ROM

## 9810 and 9820 CALCULATOR SPECIFICATIONS

GENERAL DESCRIPTION:

The 9-1000 is a 4096 bit static ROM that is organized as 512x 8 with fully decoded inputs. The inputs require external pullup resistors for use with open collector devices.

This specification applys only to the 9810 and 9820 Calculator usage of the 9-1000 ROM.

Part numbers are identified by testor tapes as described on page 8 and are derivable from the bit pattern number on the testor tape.

The part number is always of the form 1818-2xxx, where xxx is the three digit bit pattern number appearing on the testor tape. All parts will be imprinted on the kovar lid (page 7 ) with the appropriate part number.

All parameters and limits described in Electrical Characteristics, page 2, p. 3, p. 4, are design parameters and must be met, but need not be tested 100%.

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TITLE: 9-1000 ROM 9810, 9820 CALCULATOR SPECIFICATIONS

APPD.

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SUPERSEDES REV.

DWG. NO. A-1818-9001-1

## ELECTRICAL CHARACTERISTICS

Standard Operating Conditions:*

(Each of the Electrical Characteristics is met for the worst case in the following Standard Operating Conditions.)

$V_{DD}$ = +5 volts ± 5%

$V_{GG}$ = +12 volts +0% -10%

$V_{BG}$ = -2.0 volts ±5%

$V_{OR}$ = +12 volts ±5%

Output Loads: See Figure 2

$T_A$ = 0°C to 55°C

Programmed as 512 x 8

$V_{GG}$ and $V_{OR}$ are pulsed supplies

| CHARACTERISTIC | SYMBOL | MIN. | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Inputs $I_{0-8}$: | | | | | |
| Logical "0" | $V_{in}$"0" | | .8 | V | |
| Logical "1" | $V_{in}$"1" | 4 | 6 | V | With $I_{in} \leq$ lua |
| Capacitance to ground: | | | | | |
| $I_{0-7}$ | $C_{in}$ | | 13 | PF | at Ov, f= 1 MHz |
| $I_8, \overline{I_8}$ | $C_{in}$ | | 18 | PF | at Ov, f= 1 MHz |
| $V_{OR}$ | $CV_{OR}$ | | 13 | PF | at Ov, f = 1 MHz |
| $V_{gg}$ | $CV_{GG}$ | | 100 | PF | at Ov, f = 1 MHz |

* Referenced to common (pin 15)

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## ELECTRICAL CHARACTERISTICS (Continued)

| CHARACTERISTIC | SYMBOL | MIN. | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **Outputs: $0_0$-$0_7$** | | | | | |
| Logical "0" (D.C.) | $V_{out}$"0" | | .4 | V | $I_{sink}$ = 1.6 MA* |
| Logical "1" | $I_{leak}$ | | 1 | µA | At $V_{out}$ = 5 v |
| Capacitance to ground | $C_{out}$ | | 12 | PF | $V_{out}$ = OvDC f = 1 $MH_z$ |
| Output Pullups to $V_{DD}$ (enabled by $V_{OR}$) | $R_{out}$ | 1.4 (typ)* | | KΩ | At $V_{out}$ = 0.4 v |
| | $R_{out}$ | 1.5 (typ)* | | KΩ | At $V_{out}$ = 2.4 v |
| **Access Time** | $t_A$ | | 1160 | ns | See Figure 1 |
| **Supply Currents:** | | | | | |
| $V_{DD}$ Supply | $I_{DD}$ | | 80 | MA | |
| $V_{gg}$ Supply | $I_{gg}$ | | 1 | µA | |
| $V_{BG}$ | $I_{BG}$ | | 5 | µA | |
| $V_{OR}$ | $I_{OR}$ | | 1 | µA | |
| Power Dissipation | $P_d$ | 250 (typ) | | MW | |

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* For 9-1000 A artwork only, $I_{sink}$ = 1.4 ma
$R_{out}$ = .61 KΩ and .67 KΩ at $V_{out}$ = .4 and 2.4 respectively

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TITLE: ELECTRICAL CHARACTERISTICS

APPD.

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DWG. NO. A-1818-9001-1

## MAXIMUM RATINGS

25°C unless otherwise indicated.

| CHARACTERISTIC | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Voltage on all pins** | | 0 | 20 | V |
| Power Dissipation | $P_d$ | | 500 | mw. |
| Ambient Operating Temperature | $T_A$ | 0 | 55 | °C |
| Storage Temperature | $T_s$ | -25 | 100 | °C |

** Referenced to substrate. ($V_{BG}$)

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TITLE: MAXIMUM RATINGS

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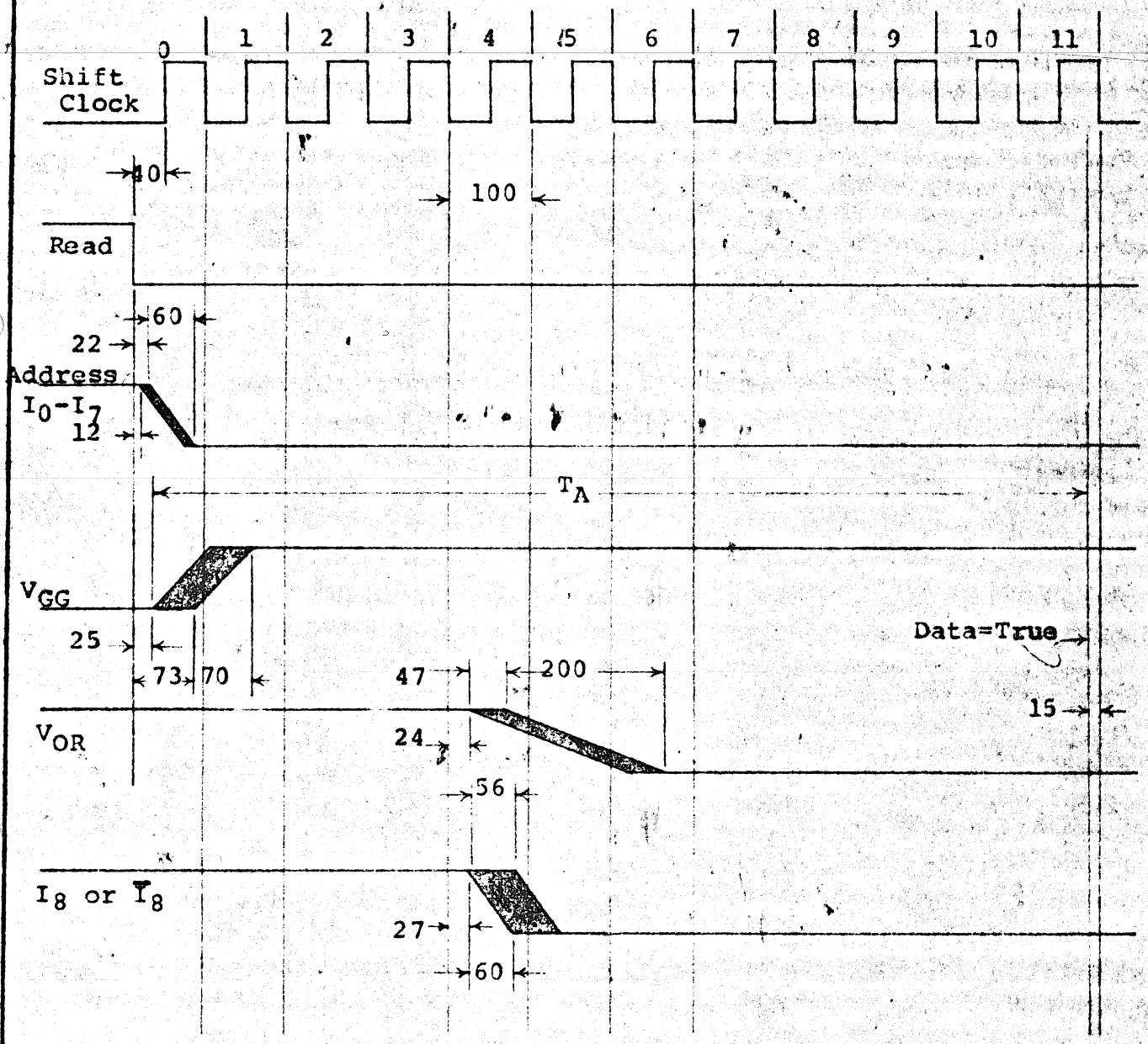


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NOTES: Minimum and maximum delays are shown.
Only maximum rise and fall times are given.
All times are in nanoseconds.
Shaded areas represent uncertainty.

Figure 1

| LTR. | REVISIONS | APPD. | DATE |
|---|---|---|---|
| B | | | |
| A | Issued Dave Maitland Orig. | DLT | 7-19-71 |

TITLE: 9810 and 9820 ROM TIMING DIAGRAM

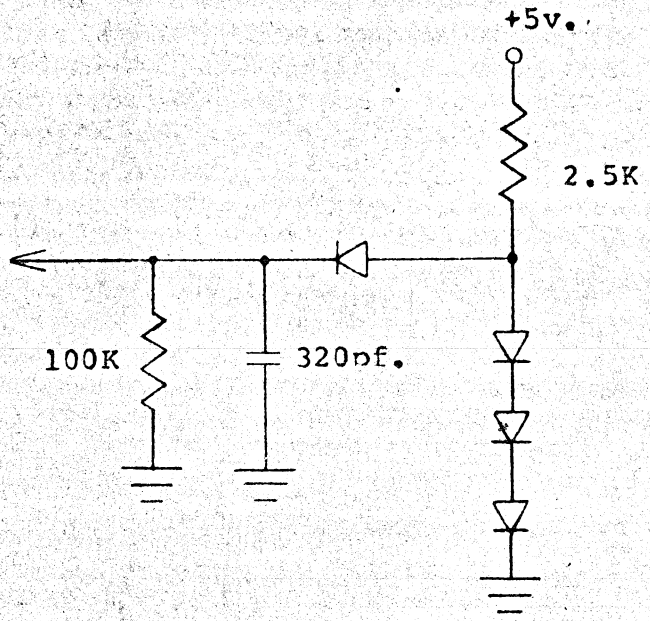
APPD.

SUPERSEDES REV.

SHEET 5 OF 10

DWG. NO. A-1818-9001-1

FORM NO. 0700006




All diodes IN 4363 or equivalent

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Figure 2

| LTR | REVISIONS | APPD. | DATE |
|---|---|---|---|
| B | [illegible] | | 5/18/71 |
| A | Issued Dave Maitland Orig.DCT | | 5/4/71 |

TITLE: OUTPUT LOADS

APPD.

SUPERSEDES REV.

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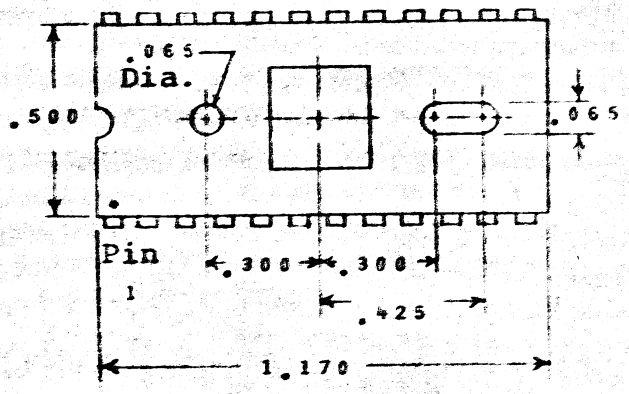
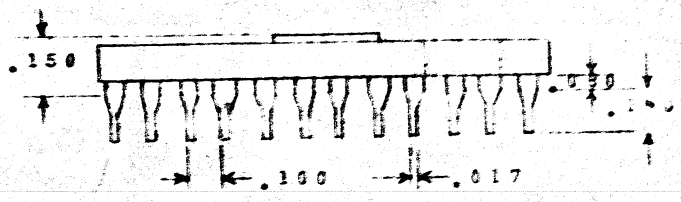
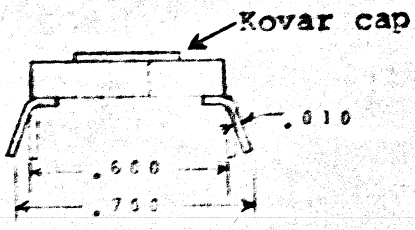
FORM NO. 0700006

## MECHANICAL DATA




* PACKAGE:**
24 lead, ceramic
dual-in-line

## PIN CONFIGUPATION*

TOP VIEW

| | | | |
|---|---|---|---|
| $V_{BG}$ (Sub.) | 1 | 24 | $V_{BG}$ (Sub.) |
| $V_{DD}$ | 2 | 23 | $V_{GG}$ |
| Input $I_4$ | 3 | 22 | Input $I_5$ |
| Input $I_2$ | 4 | 21 | Input $I_3$ |
| Input $I_0$ | 5 | 20 | Input $I_1$ |
| Output $O_1$ | 6 | 19 | Output $O_3$ |
| Output $O_3$ | 7 | 18 | Output $O_2$ |
| Output $O_5$ | 8 | 17 | Output $O_4$ |
| Output $O_7$ | 9 | 16 | Output $O_6$ |
| $V_{OR}$ | 10 | 15 | Common |
| Input $I_7$ | 11 | 14 | Input $I_6$ |
| Input $\overline{I}_8$ | 12 | 13 | Input $I_8$ |

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** For ROM programmed as a 512 x 8.

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TITLE: MECHANICAL DATA AND PIN CONFIGURATION

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DWG NO. A-1818-9001-1

## PART NUMBER IDENTIFICATION AND PROGRAMMING

Part numbers are identified and documented by means of testor tapes. The testor tapes are 8 level paper tapes coded in ASC II with a line format and an ASC II Carriage Return and Line Feed at the end of each line. All lines begin in column 1. The tape is comprised of three sections: Leader, Bit Pattern and Trailer.

### Leader Data - 3 lines

The first three lines on the testor tape contain header information formatted as shown in the following example (all lines start in column 1 with space indicated by ␣ ):

Line 1 `1B3B4B(000B)5B6B␣␣9810␣"␣comments␣25 char.`

- `1B3B4B(000B)5B6B`: Mask set to be used with this part number. Contact mask programming indicated as shown by (000B)
- `9810`: Instrument Number

Line 2 `010A␣␣03/17/71␣␣512 x 08␣␣Omit on 1`

- `010A`: Bit Pattern # & rev. letter
- `03/17/71`: Date
- `512 x 08`: Organization: # of words x # of Bits in word
- `Omit on 1`: Defines sense of testor tape

Line 3 `Line 2␣␣line 1` — Combined lines, truncate beyond 72 characters

All fields are to be the number of characters shown; leave blanks where necessary to fill the field.



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## Bit Pattern Data - 512 lines

For 4096 bit ROM organized as 8 bits per output word, there will be octal 777 lines (decimal 512 lines) following the three header lines. These lines define the logical states of the ROM and are formatted as follows (spaces are indicated by ␣ ):

XXX ␣ YYYYYYYY

- XXX: Octal chip Address, ($I_8 \rightarrow I_0$, right justified, LSB is $I_0$)
- YYYYYYYY: Binary output word ($O_7 \rightarrow O_0$)
- Output $O_0$ (either 0 or 1)

A logical "1" on a output corresponds to no gate cut in the bit array; a logical "0" on a output corresponds to the presence of a gate cut. Don't care states are encoded as logical "1".

## Trailer Data - 17 to 18 lines

The next three to four lines define miscellaneous programming and have the form:

For 9-1000A ←
```
00000000000000000000000000000000
1111111111111111
11111111111
1111100111101011111
```

For 9-1000C ←
```
00000000000000000
11111111111100
1111
```

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TITLE: PART NUMBER IDENTIFICATION AND PROGRAMMING

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FORM NO. 0700008

The next four lines contain the part number (bit pattern) and revision letter encoding in a binary format. The part number and revision letter are identical to the bit pattern number and revision letter on line 2 of leader. The first through the third lines represent digits one through three of the part number; the fourth line encodes the revision letter. The part number and revision letter are encoded by placing a "0" at the appropriate place in the lines; for example, the bit pattern number 018 (revision A) is encoded as follows:

```
0111111111
1011111111
1111111101
01111111111111111111111
```

The next four lines contain an exact copy of the bit pattern number and revision letter encoding described on the preceeding page. The next six lines contain a date coded which is formatted identically to the part number code. For example 3/15/71 is encoded as:

```
0111111111
1110111111
1011111111
1111101111
1111111011
1011111111
```

The date coded here is the same as the date appearing on line 2 of the leader.



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