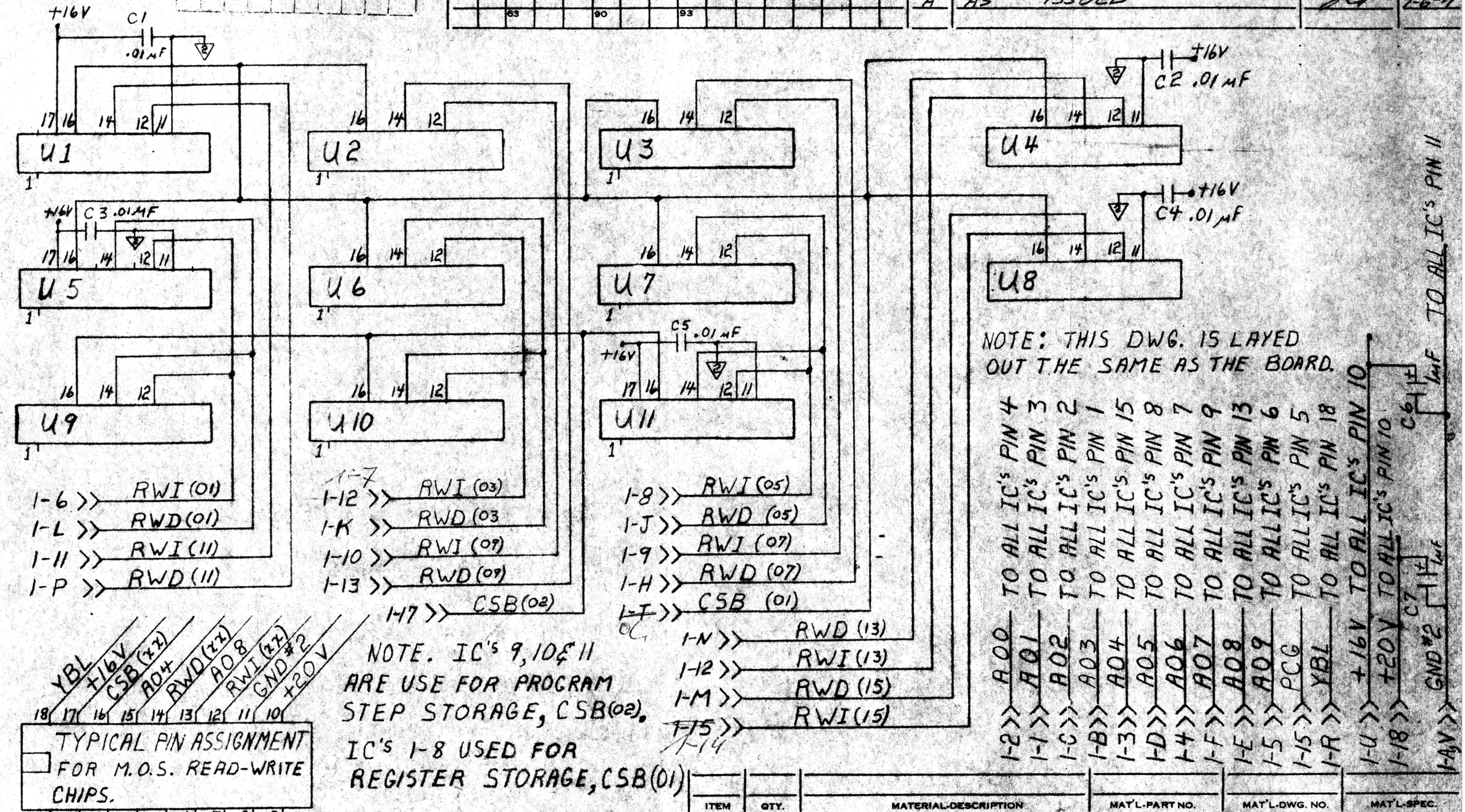
ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4	5	6	7	8	9◪	10	11	12◪	14	15
16	17	18	19	20	21	22			33	34	38		42	43
		63			90			93						

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	JC	7-6-71

B-09810 -66525 -2



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY B THAYER 2-25-71 DATE
ENGINEER FINN
RELEASE TO PROD. 7-6-71
SUPERSEDES DWG.

9810 BASIC MEMORY READ/WRITE
TITLE

NEXT ASSEMBLY 09810-66525
FINISH ok 6-16-71 SCALE

HEWLETT PACKARD

PART NUMBER B-09810-66525-2

STOCK NO. 9280-0002 PAPER K&E 10 9545

SHEET OF

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17	18	19	20	21	22			33	34	38		42	43	
		63			90			93							

B-11217-66526-2

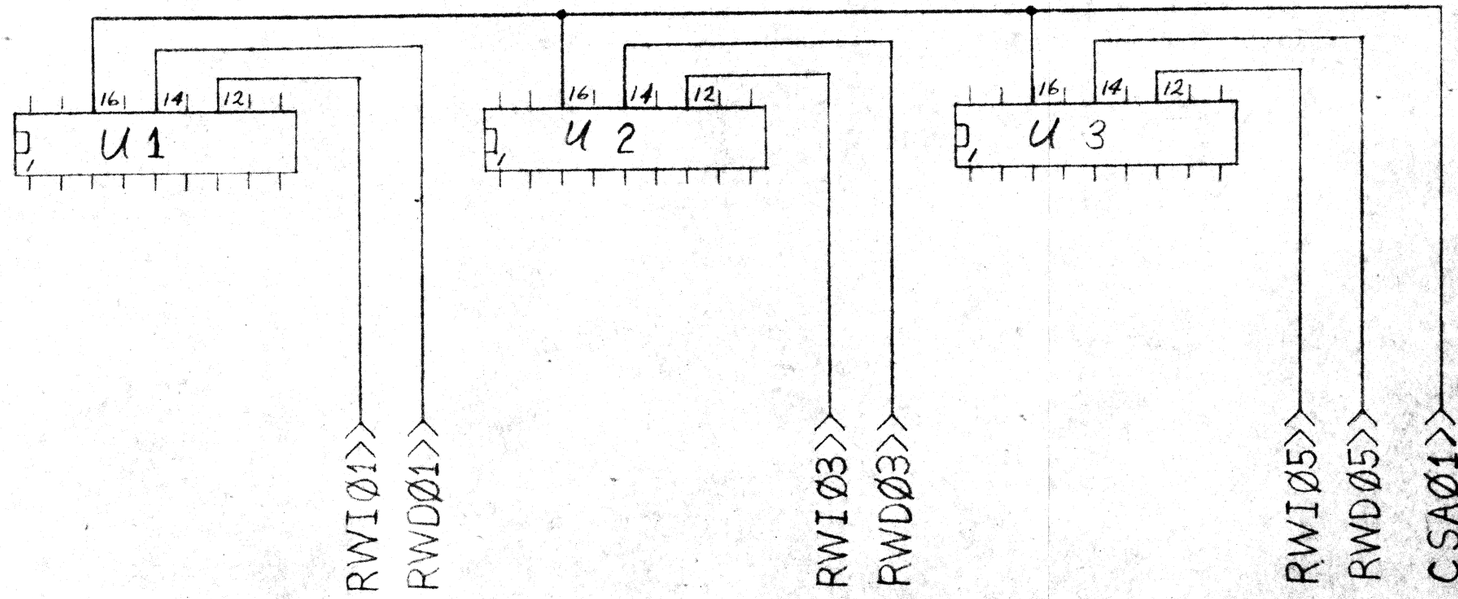
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	JCS	26-71

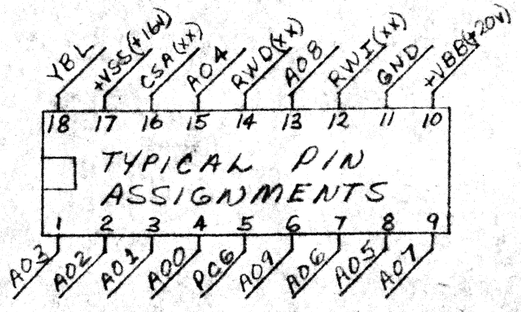
12

CONNECTOR PIN ASSIGNMENTS (P1)

A	GND	1	A01
B	A03	2	A00
C	A02	3	A04
D	A05	4	A06
E	A08	5	A09
F	A07	6	RWI Ø1
H	RWD Ø7	7	RWI Ø3
J	RWD Ø5	8	RWI Ø5
K	RWD Ø3	9	RWI Ø7
L	RWD Ø1	10	RWI Ø9
M	RWD 15	11	RWI 11
N	RWD 13	12	RWI 13
P	RWD 11	13	RWD Ø9
R	YBL	14	RWI 15
S	CSA Ø1	15	PCG
T	CSA Ø3	16	CSA Ø2
U	+VSS(+16V)	17	CSA 04
V	GND	18	+VCC(+20V)

512 PROGRAM STEPS.





NOTE: PIN ASSIGNMENTS ARE COMMON TO ALL IC'S, UNLESS OTHERWISE SHOWN.

NOTE: THIS DRAWING IS LAYED OUT THE SAME AS THE BOARD

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY Wayne Harlan	DATE 4-13-71	9810- OPT 002 READ/WRITE MEMORY (TITLE)	HEWLETT PACKARD
ENGINEER FINN			
RELEASE TO PROD. J.C. Smith	7-6-71	NEXT ASSEMBLY 11217-66526	PART NUMBER B-11217-66526-2
SUPERSEDES DWG.		FINISH OK 6-16-71 SCALE	SHEET OF

Opt. 002

12

CONNECTOR PIN ASSIGNMENTS (P1)

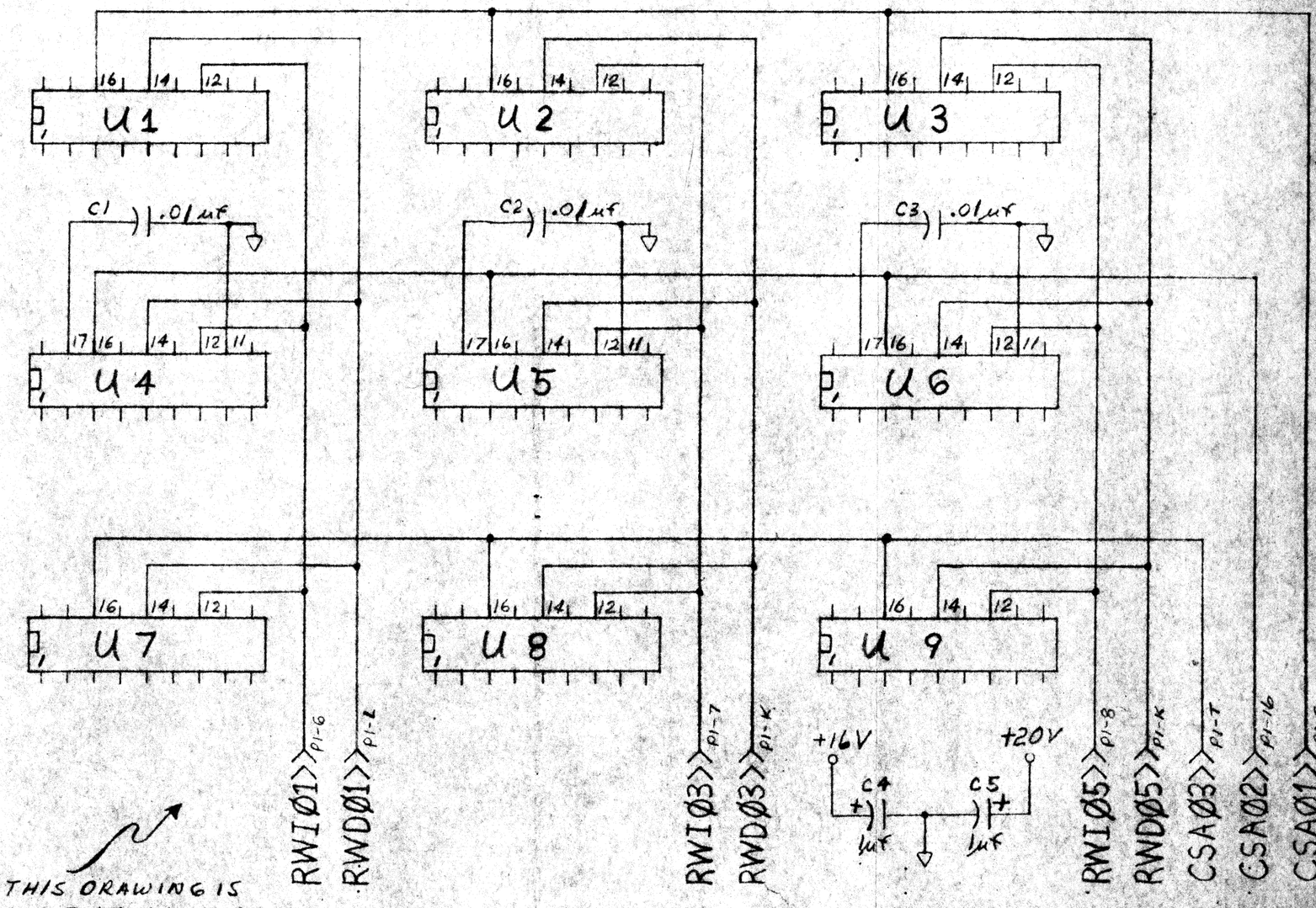
A	GND	1	A01
B	A03	2	A00
C	A02	3	A04
D	A05	4	A06
E	A08	5	A09
F	A07	6	RWI Ø1
H	RWDØ7	7	RWI Ø3
J	RWDØ5	8	RWI Ø5
K	RWDØ3	9	RWI Ø7
L	RWDØ1	10	RWI Ø9
M	RWD 15	11	RWI 11
N	RWD 13	12	RWI 13
P	RWD 11	13	RWD Ø9
R	YBL	14	RWI 15
S	CSA Ø1	15	PCG
T	CSA Ø3	16	CSA Ø2
U	+VSS(+16v)	17	CSA Ø4
V	GND	18	VCC (+20v)

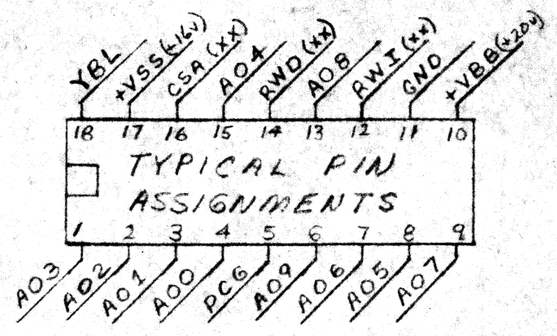
ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17	18	19	20	21	22			33	34	38		42	43	
		63			90			93							

B-11218-66526-2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		7-6-71





NOTE: PIN ASSIGNMENTS ARE COMMON TO ALL IC'S, UNLESS OTHERWISE SHOWN.

NOTE: THIS DRAWING IS LAYED OUT THE SAME AS THE BOARD

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED. DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY Wayne Harlan	DATE 7-12-71	9810 OPT 003 READ/WRITE MEMORY	HEWLETT PACKARD
ENGINEER FINN		TITLE	
RELEASE TO PROD.	7-6-71	NEXT ASSEMBLY 11218-66526	PART NUMBER B-11218-66526-2
SUPERSEDES DWG.		FINISH OK 6-16-71 SCALE	