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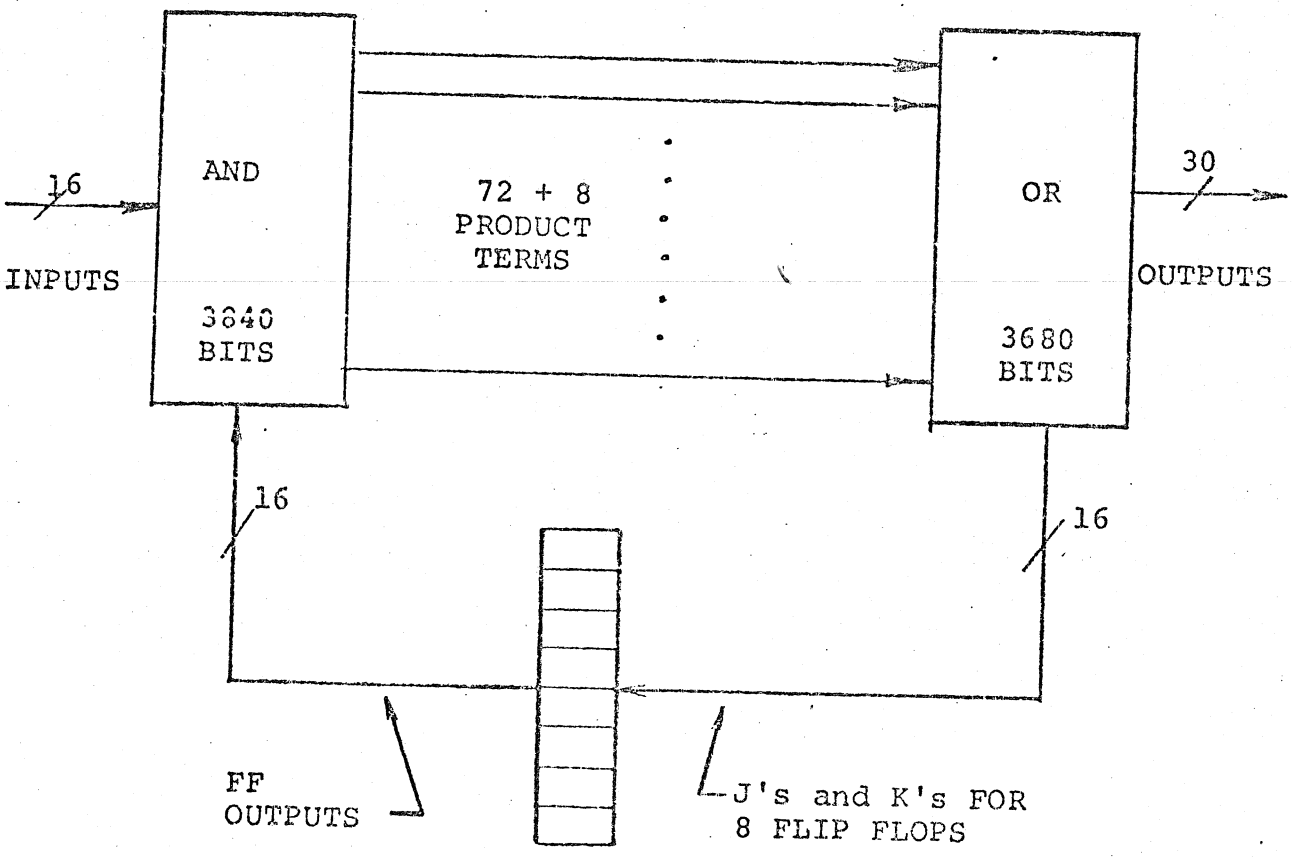
MOS

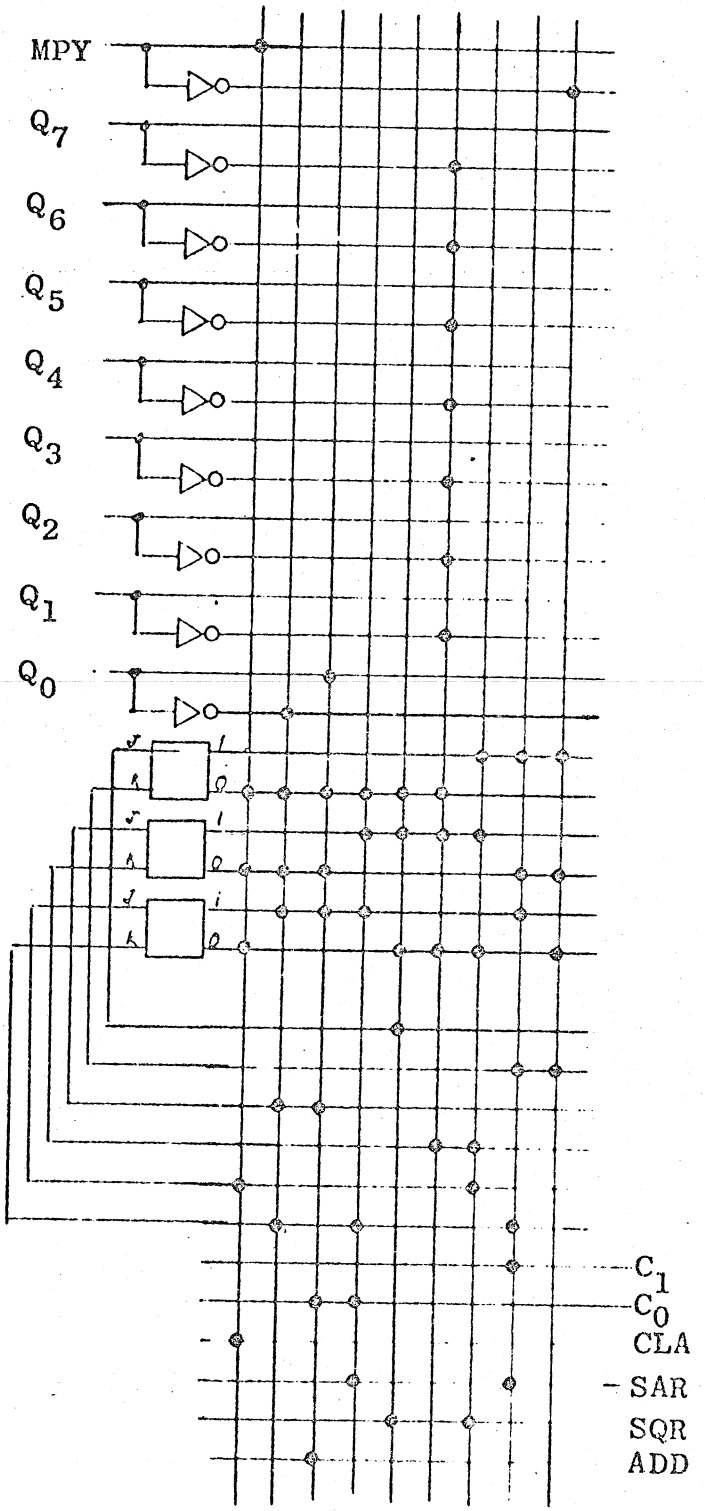
PROGRAM CONTROL ARRAY

BLOCK DIAGRAM



8 FLIP FLOPS

PCA PROGRAMMING



Abbreviated Array Map of 8-bit Multiply

PCA SPECIFICATIONS

INPUTS: 16

OUTPUTS: 30

FLIP FLOPS: 8

NO. OF "P" TERMS: 72 + 8

POWER: 500-600 mW

SPEED: 600 TO 1000 nS ACESS TIME, < 2 μS CYCLE TIME

TECHNOLOGY: P-CHANNEL

POWER SUPPLIES: GND, ±10

CLOCKS: 2 PHASE

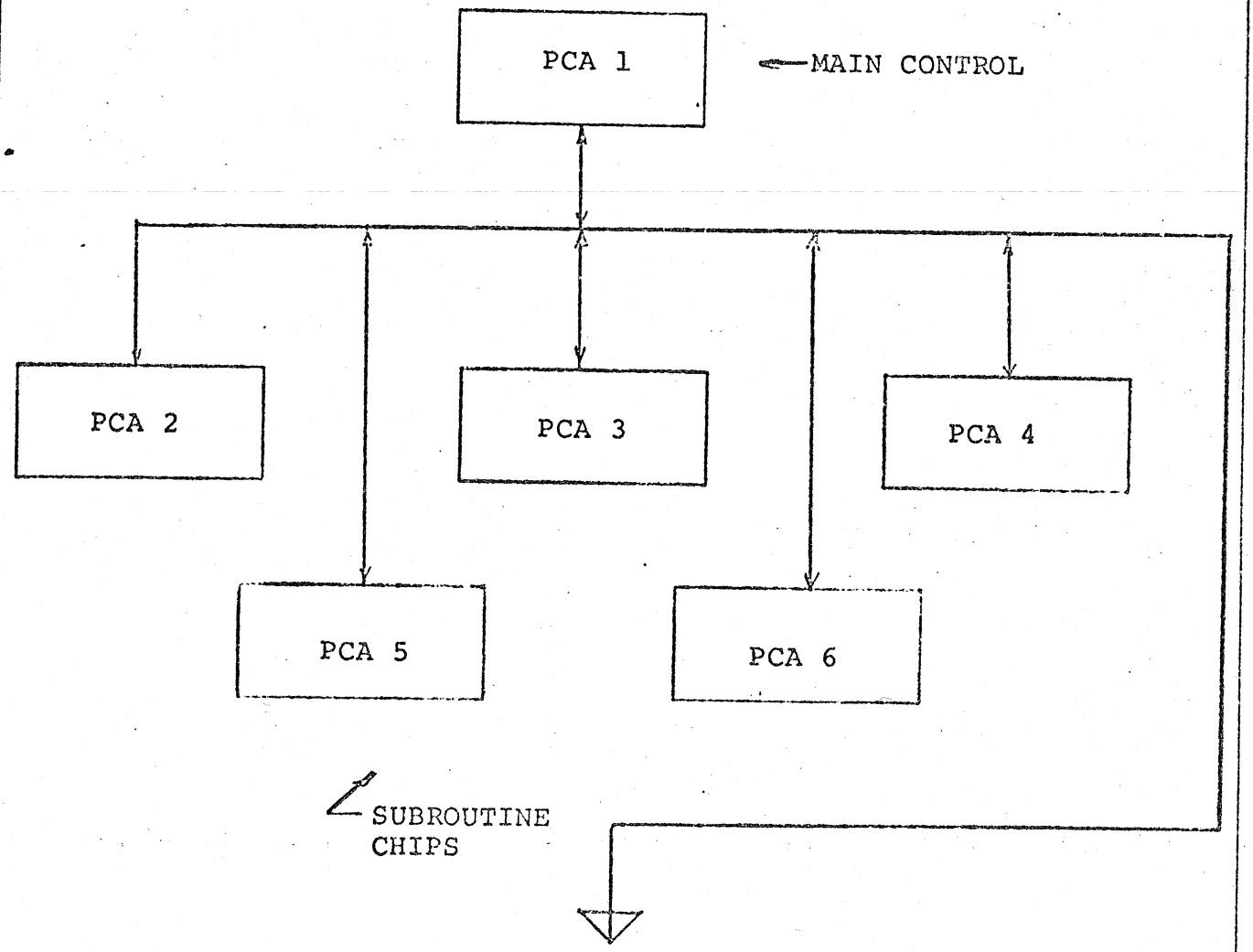
CHIP AREA: 133 * 120 $MILS^2$

ARRAY SIZE: 80 * 94 = 7520 BITS

PACKAGE: 51 LEADS; OTHERS AVAILABLE

PCA APPLICATIONS

LOVELAND NETWORK SYNTHESIZER



INSTRUCTIONS.
QUALIFIERS TO/FROM:
- 16 X 16 MEMORY
- M REGISTER
- P REGISTER
- EXTEND F-F
- A REGISTER
- ALU S.C. ROM
- INPUT-OUTPUT

SUBROUTINES:

- 8 DIGIT ADD-SUBTRACT
- MULTIPLY: X2, X10
- DIVIDE: ÷ 2, ÷ 10
- NUMERIC ENTRY
- SWEEP CONTROL
- PARAMETER MOD.
- AMPLITUDE CONTROL, ETC.

OTHER INFORMATION

.PLANS TO DIGITIZE IN THE SPRING

.DESIGNER WILL MAKE TAPE FOR DESIRED PROGRAMMED BITS

.TEST PROGRAM WILL BE MADE FROM THIS TAPE

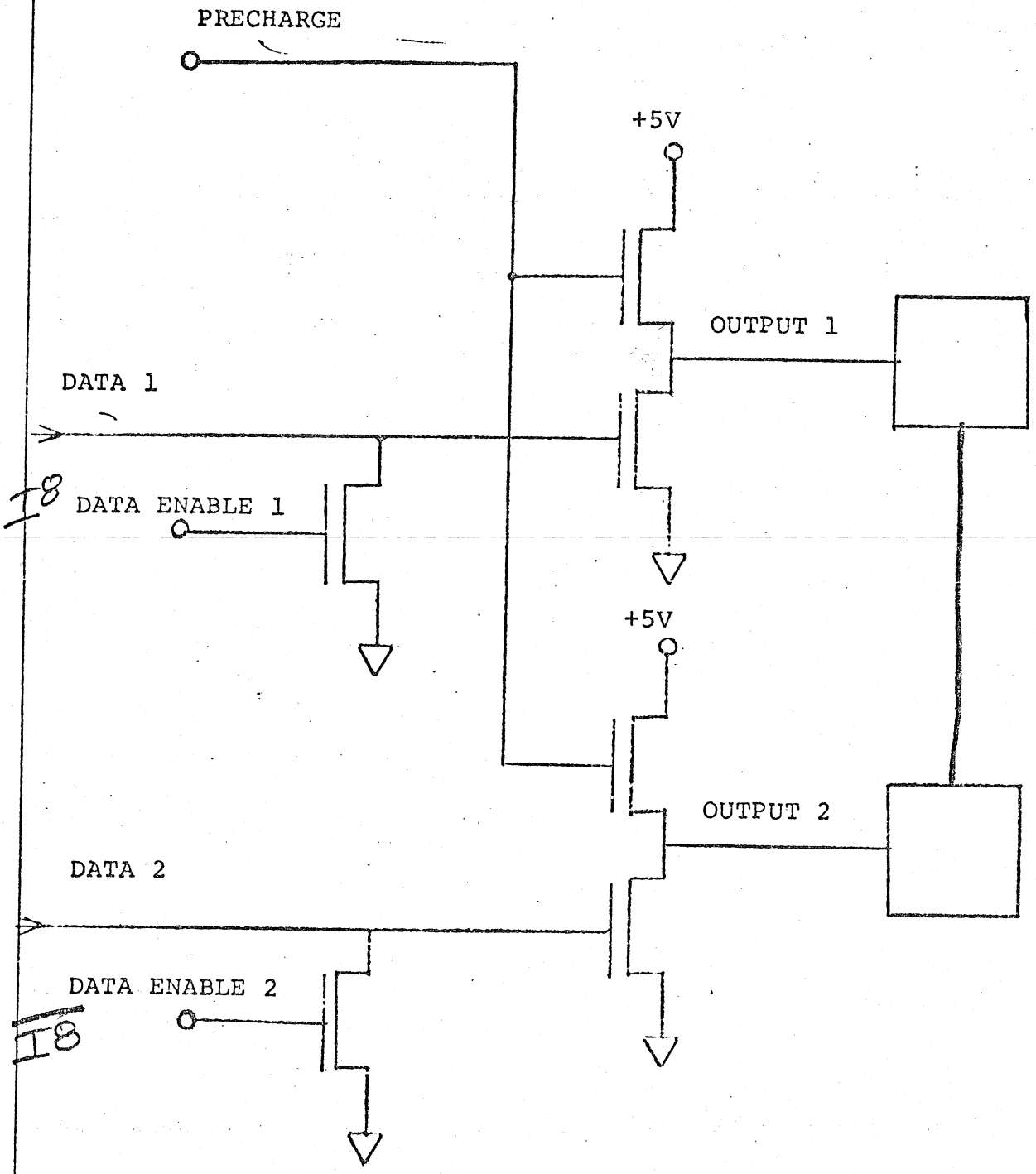
.FOR FURTHER INFORMATION:

CHUCK KINGSFORD-SMITH -- GROUP LEADER

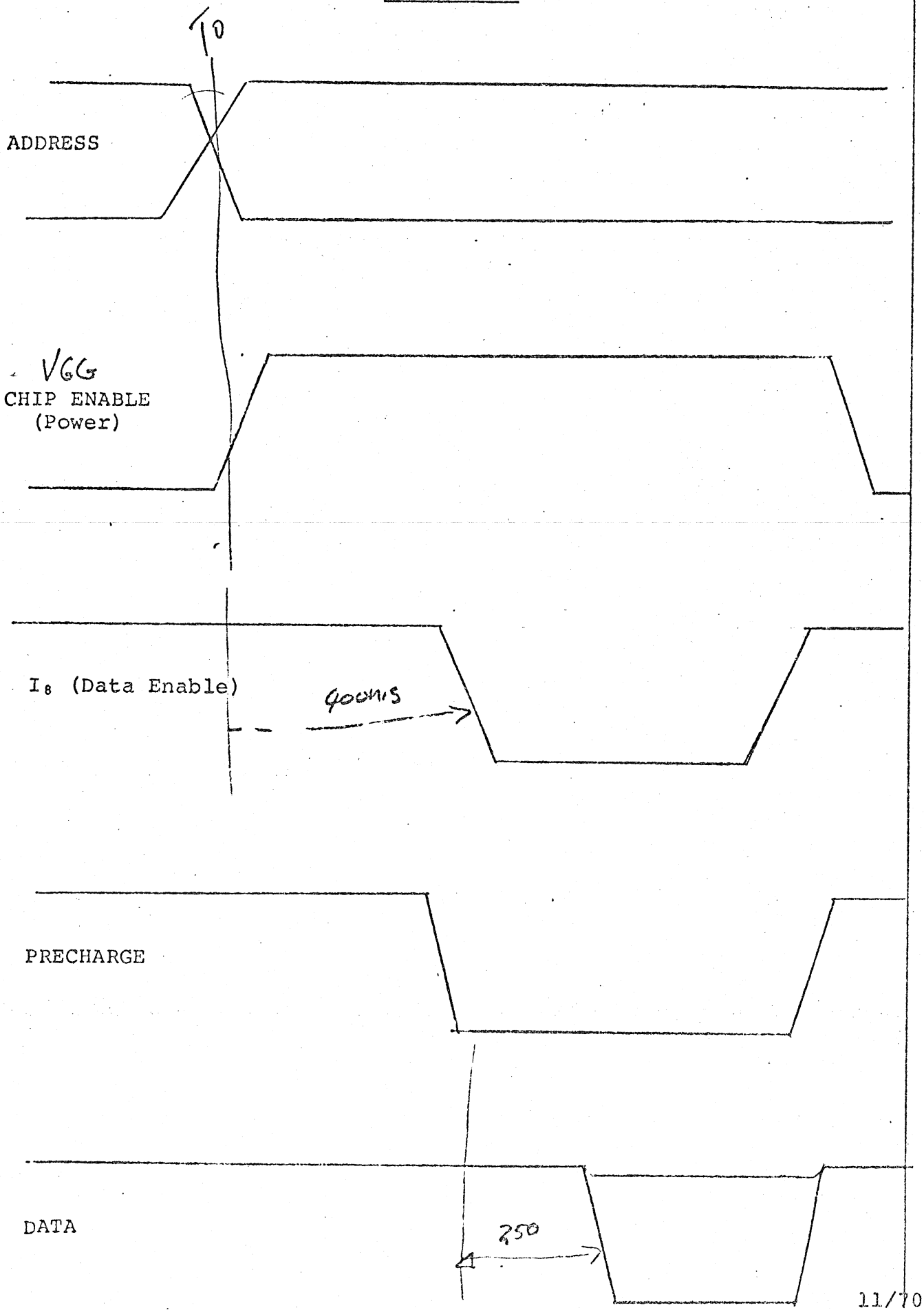
CLARE NELSON -- SOFTWARE

ROGER COX -- PHYSICAL SPECIFICATIONS

ROM OUTPUT


PRECHARGE
+5V
OUTPUT 1
DATA 1
I8
DATA ENABLE 1
+5V
OUTPUT 2
DATA 2
DATA ENABLE 2
I8

ROM TIMING


T0
ADDRESS
VGG
CHIP ENABLE
(Power)
I8 (Data Enable)
400nS
PRECHARGE
DATA
250

ROM SPECIFICATIONS

.ARRAY SIZE: 4096 BITS

.ORGANIZATION: 256 X 16 OR 512 X 8

.POWER 250 mW - CAN BE PULSED

.ACCESS TIME: < 500 nS

.CYCLE TIME: < 1 μs

.POWER SUPPLIES: ±5, +10

.TECHNOLOGY: N-CHANNEL

.CHIP AREA: 110 X 100 MILS^2

.PACKAGE: 24 PIN DUAL CERAMIC IN-LINE FOR 512 X 8; 30 PINS FOR 256 X 16

.OUTPUT PRECHARGE CIRCUITRY - PROGRAMMABLE

.INPUT PULL UP RESISTORS - PROGRAMMABLE

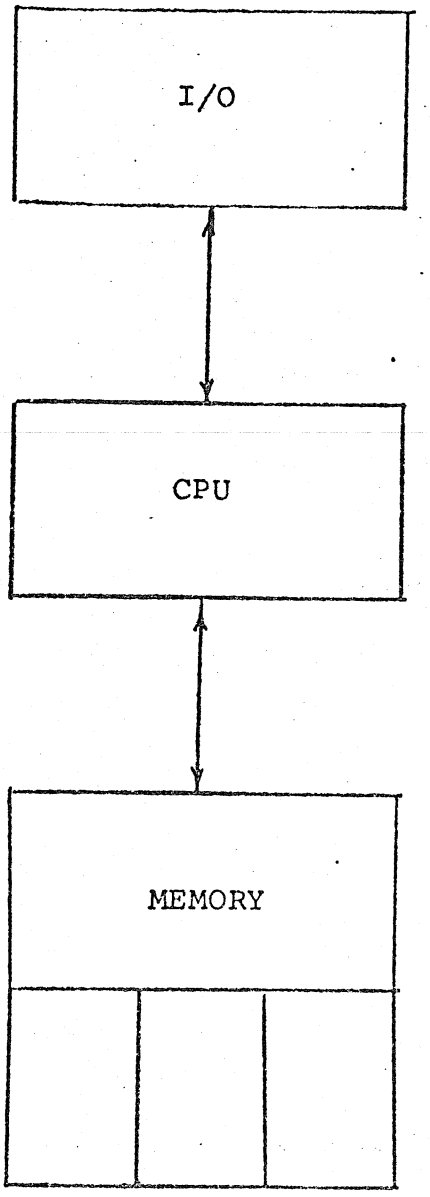
.SINKS 1 TTL LOAD

.TTL COMPATABLE ON INPUT

.$.003/BIT

9820 CALCULATOR

BLOCK DIAGRAM

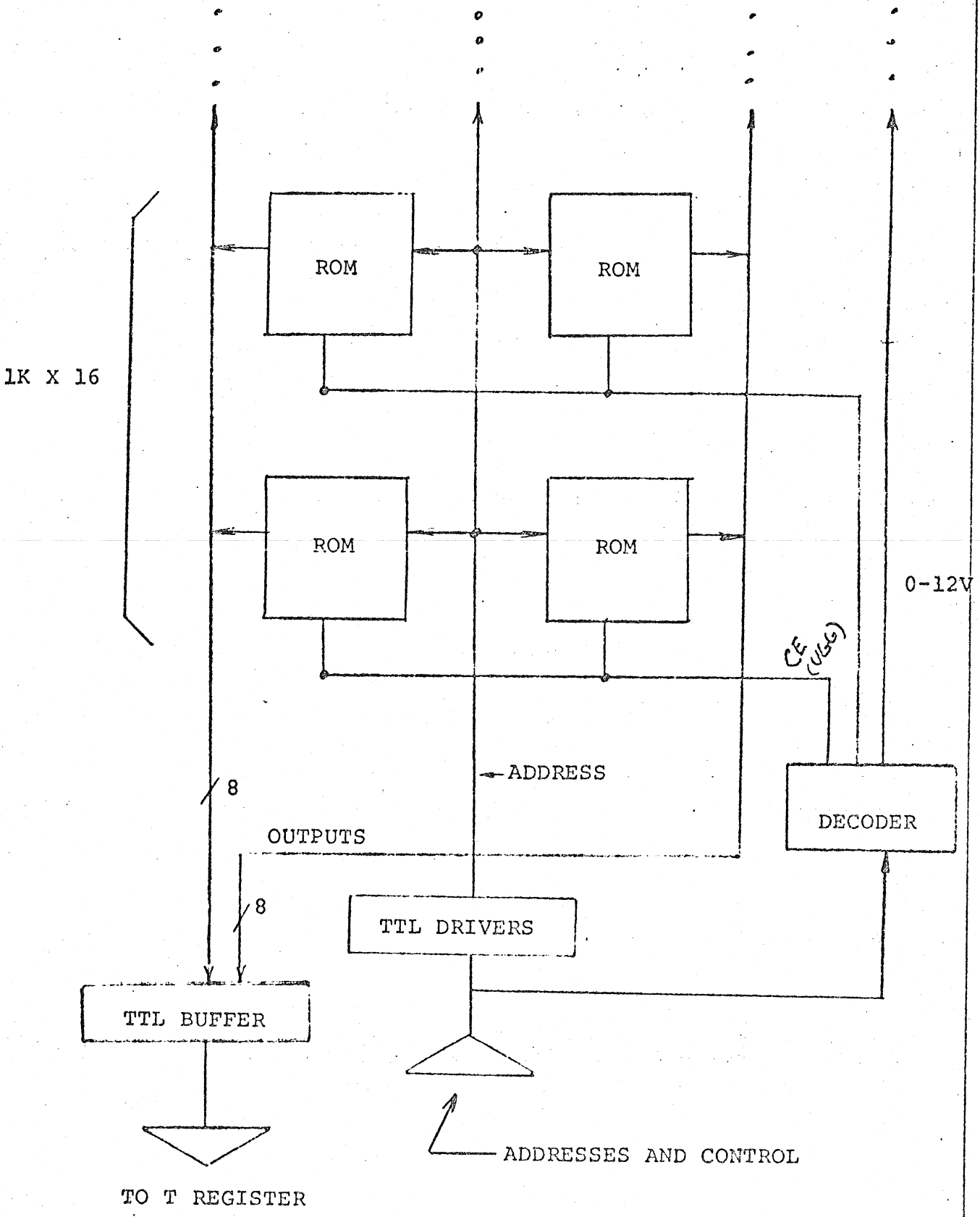


9-1K X 4 BIT SANTA CLARA
BIPOLAR ROM

512-1024 X 16 RWM
4K X 16 MOS ROM

3 ADD-ON BLOCKS
MOS ROM
UP TO 1K X 16 EACH

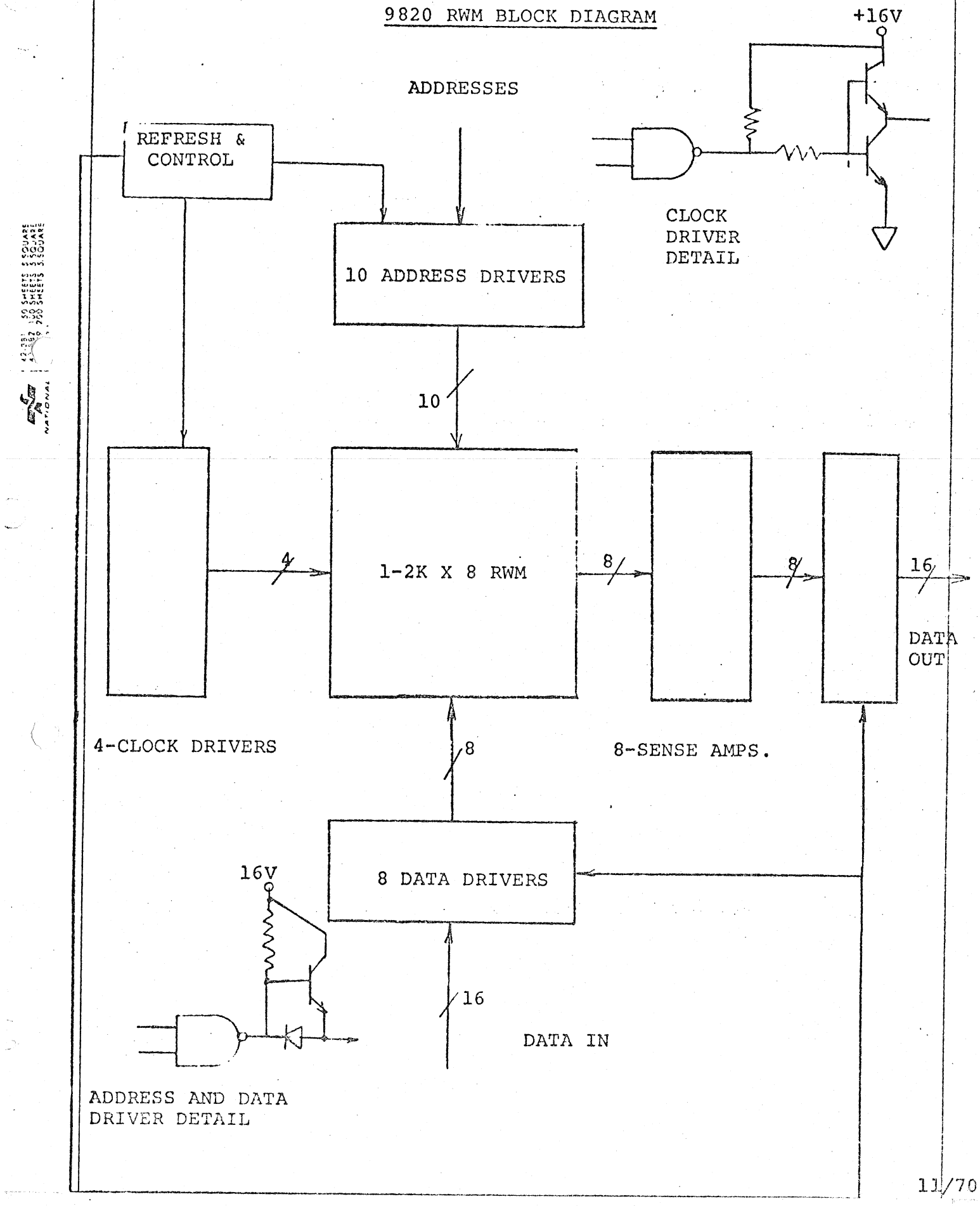
ROM IN 9820


ROM
ROM
ROM
ROM
1K X 16
0-12V
CE (USED)
ADDRESS
8
OUTPUTS
DECODER
8
TTL DRIVERS
TTL BUFFER
ADDRESSES AND CONTROL
TO T REGISTER

INTEL 1103 RWM DESCRIPTION

- SIZE: 1024 X 1 BITS
- DYNAMIC--REFRESHING NECESSARY
- 18 PIN PLASTIC PACKAGE
- POWER SUPPLIES +16, +20
- SENSE AMPS NEEDED ON OUTPUT
- SPEED--580 nS CYCLE TIME
- PRICE--$.01/BIT

9820 RWM BLOCK DIAGRAM



STATUS AT LOVELAND

- EVALUATION OF 4 UNITS
- 8 K X 16 MEMORY FOR CALCULATOR SOFTWARE DEVELOPMENT THIS WEEK
- WORKING PROTOTYPE END OF NOVEMBER
- PLANNED FOR 9810, 9820--OUT IN 1 YEAR
- HAVE HAD 100 X-1102 IN 2 SYSTEMS

INTEL'S PRICING

QUANTITY	PLASTIC	CERAMIC
FIRST 5 K	$20.00	$25.00
NEXT 10 K	15.00	19.00
NEXT 25 K	10.00	13.20
NEXT 50 K	8.00	10.50
NEXT 100 K	7.00	9.00
NEXT 1 M	1.85	3.85

ESTAMATED 1973 PRICE $4.50 to $6.50 IN 50 K QUANTITIES

9820 MEMORY FACTORY COSTS

M REGISTER BOARD	$ 40
T REGISTER BOARD	50
CONTROL BOARD	60
MOTHER BOARD	25
HARDWARE	10
TOTAL	$185

(2)	ROM BOARD - (2 K x 16)	$140 each
(2)	RWM BOARDS - (512 x 16)	$145 each

FURTHER INFORMATION

4096 ROM DAVE MAITLAND

INTEL 1024 APPLICATION CAL FINN

PRELIMINARY*

9-0183

4096 BIT MOS ROM

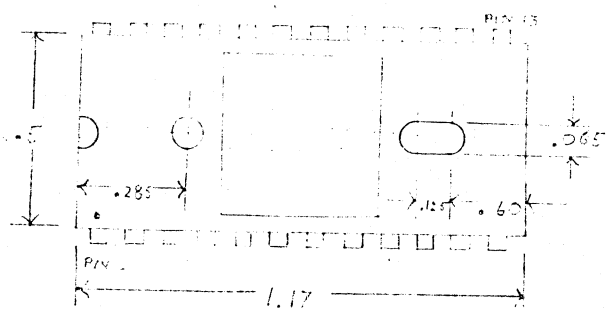
GENERAL DESCRIPTION:

The 9-0183 is a 4096 bit static ROM that can be organized as a 512 x 8 or 256 x 16. The inputs are fully decoded and the outputs can be wire-OR'd. Both the inputs and outputs have programmable pull-up resistors which enable the 9-0183 to be either MOS or TTL compatible.

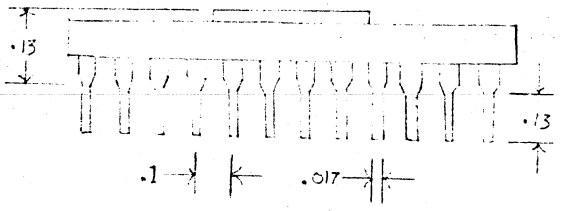
* Subject to change without notice.

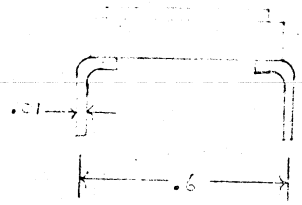
PRELIMINARY*

MECHANICAL DATA



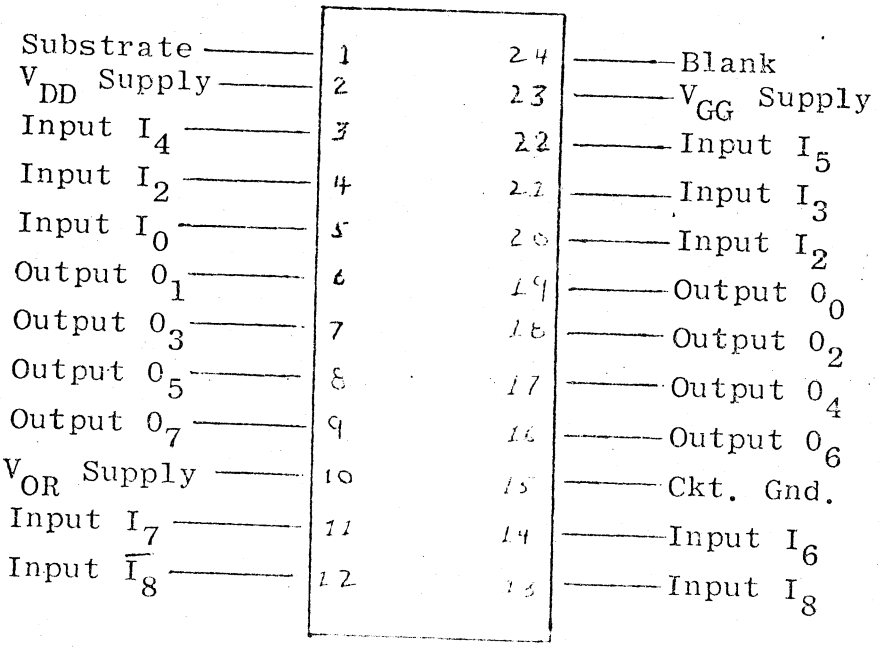
PACKAGE:**
24 lead, ceramic
dual-in-line





PIN CONFIGURATION

TOP VIEW



** For ROM programmed as a 512 x 8.

PRELIMINARY*

MAXIMUM RATINGS

@ 25°C unless otherwise indicated.

CHARACTERISTIC	SYMBOL	MIN	MAX	UNITS
Voltages on all pins**				V
Power Dissipation	P_d			mw.
Operating Temperature	T_o			°C
Storage Temperature	T_s			°C

** Referenced to substrate.

PRELIMINARY*

ELECTRICAL CHARACTERISTICS

Standard Test Conditions (512 x 8):

V_{DD} = +5 volts ±10% Output loads; 200 pf, 100 K to GND.

V_{gg} = +10 volts ±10% T_a = 1 μs (see timing diagram)

V_{BG} = -5 volts ±10% T_o = 25°C

R_L = +10 volts ±10% Input address 111

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Inputs I_{0-8}:						
Logical "0"	V_{in} "0"				V	
Logical "1"	V_{in} "1"				V	
Pullups	R_{in}				KΩ	Programmable
Capacitance	C_{in}				PF	Without pullups
					PF	With pullups
I_8 Capacitance	C_{I8}					
					PF	Without pullups
					PF	With pullups
V_{gg} Capacitance	C_{Vgg}				PF	
Outputs:						
Logical "0"	V_{out} "0"				V	I_{out} = 1.8 MA
Logical "1"	V_{out} "1"				V	
Sink Current	I_{out}					Programmable
					MA	At .4 volts
					MA	At .8 volts

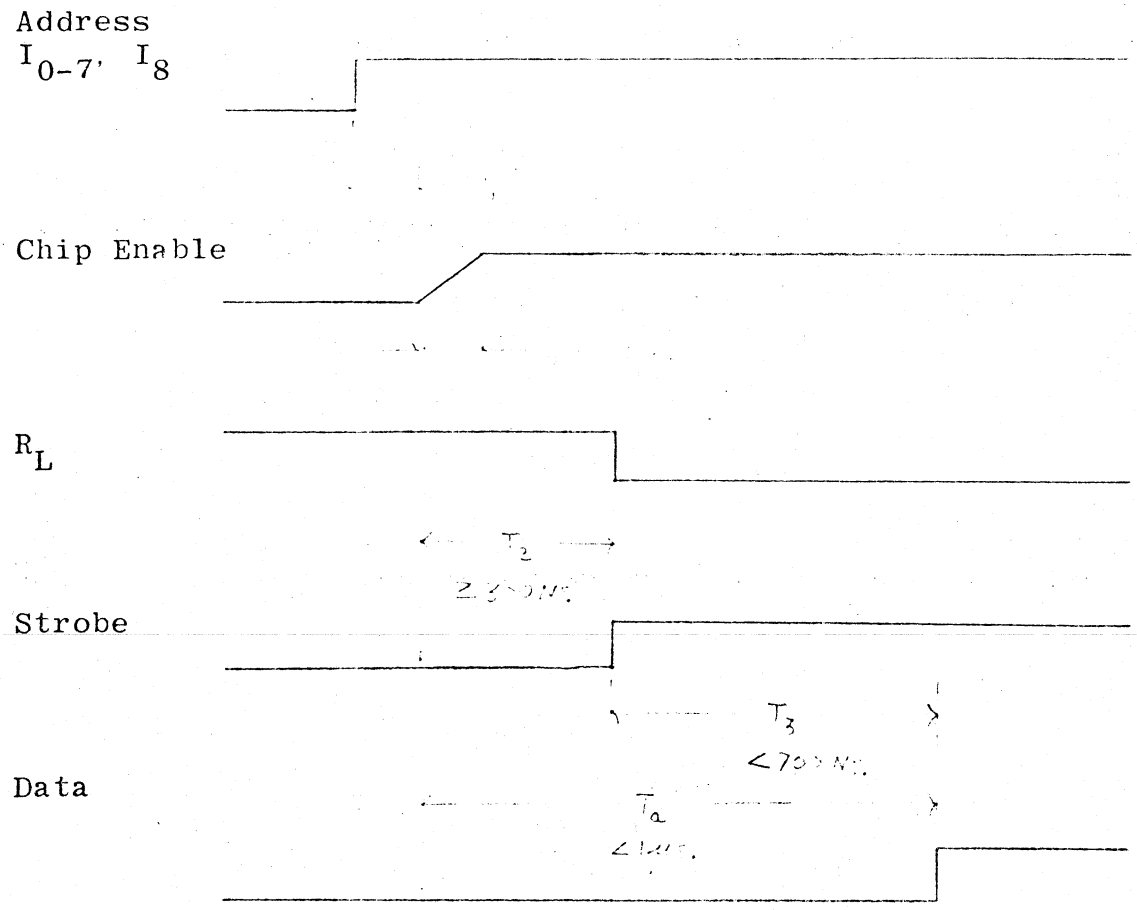
PRELIMINARY*

ELECTRICAL CHARACTERISTICS CONT.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Capacitance	C_{out}				PF	
Pullups	R_{out}					Programmable
					KΩ	At V_{out} = .4 V
					KΩ	At V_{out} = 2.5 V
Access Time	T_a				μs	See timing diagram
Supply Currents:						
V_{DD} Supply	I_{DD}				MA	
V_{gg} Supply	I_{gg}				NA	
V_{BG} Supply	I_{BG}				NA	
R_L Supply	I_L				NA	
Power Dissipation	P_d				MW	

PRELIMINARY*

TIMING DIAGRAM



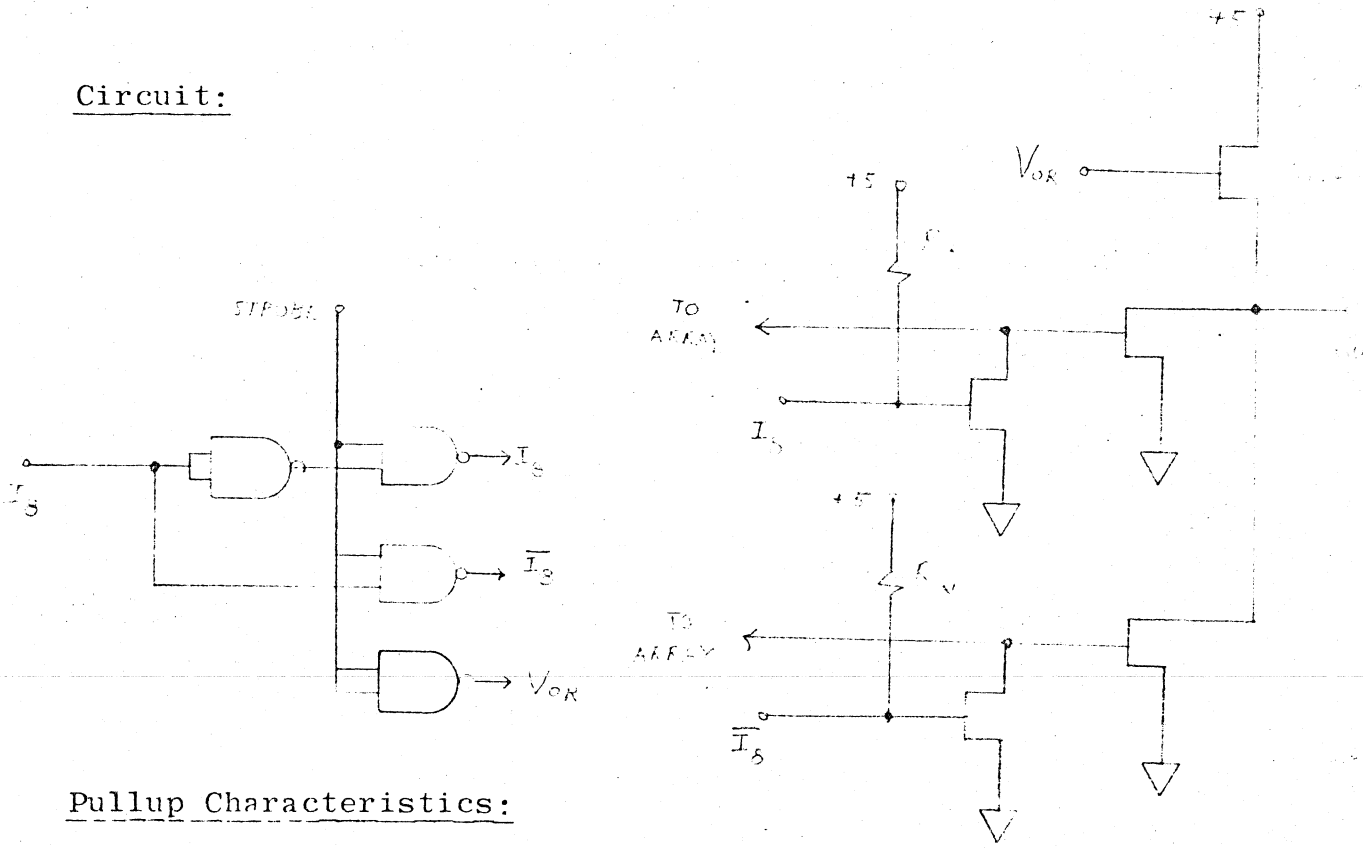
$$T_a = T_2 + T_3$$

PRELIMINARY*

Verwachting

OUTPUT BUFFER UTILIZATION

Circuit:



Pullup Characteristics:

Standard test
Conditions

Note:

1. R_L may be tied to V_{DD} or V_{gg} on the chip.
2. Pullup device may be programmed for .75%, .5% or .25% of the value indicated.

PRELIMINARY*

Power**

Schmoo Plot**

** Standard Test Conditions