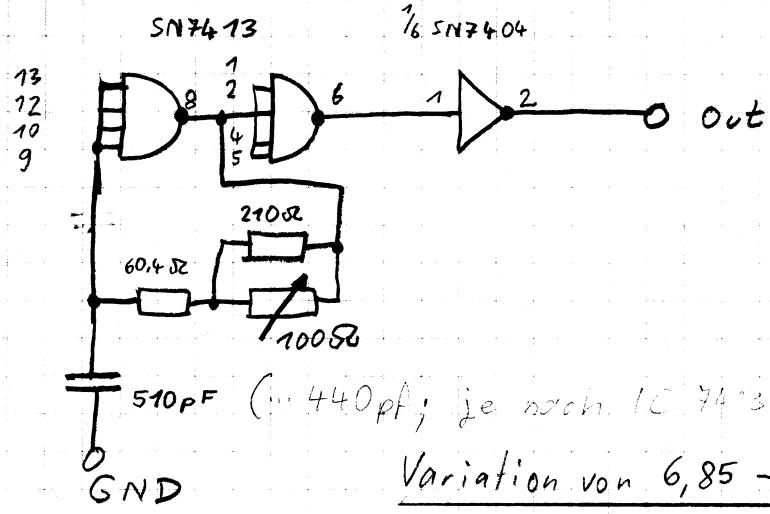
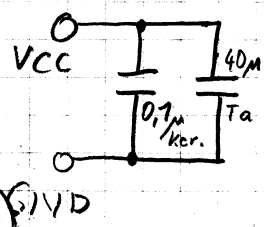
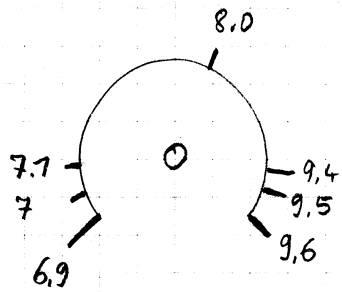
Margin-Clock-Oszillator
für 9810-Calculator

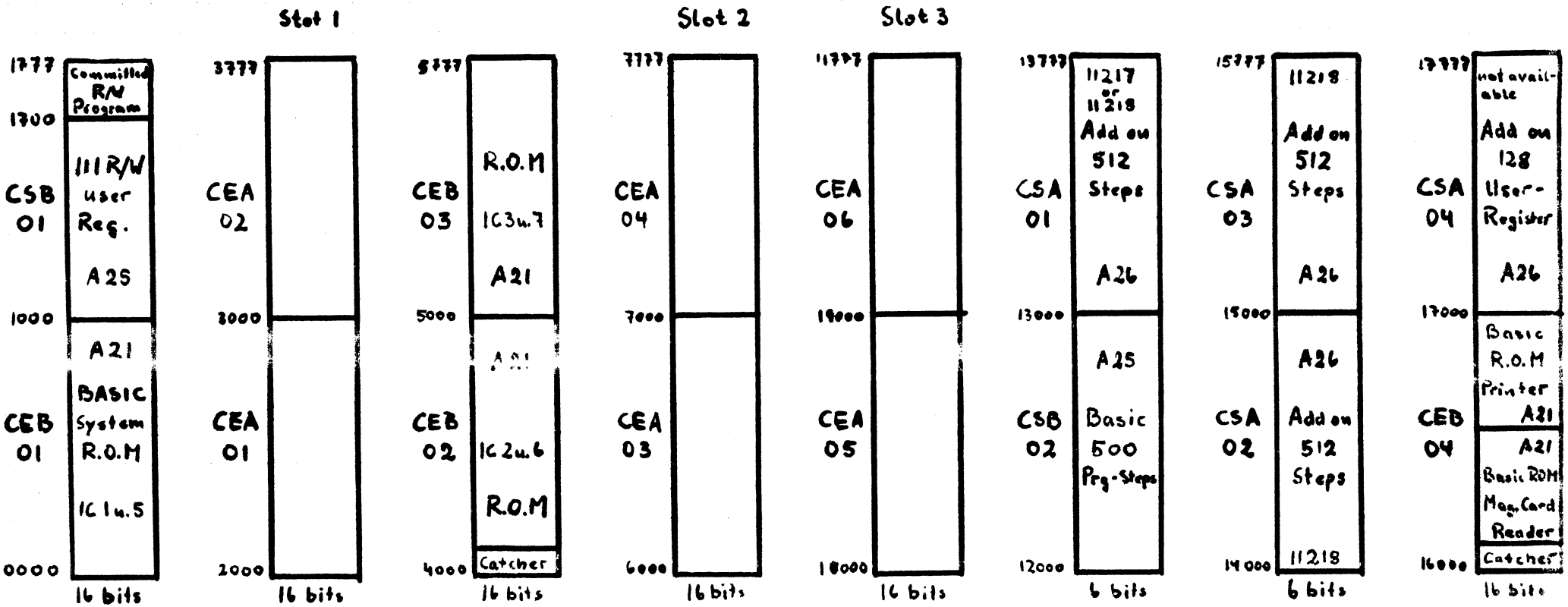




Variation von 6,85 – 9,65 MHz



montiert in Plastikgehäuse ca 70 × 50 × 20
auf IC-Testboard. Anschluß über festgelötetem
10-pin PC-Connector



NOTE:

Catcher = word for a command to send the calculator to monitor-routine.

9810 A Memory Map

Heine 18.4.72

SECONDARY

PRIMARY	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
00	A	B	B	P	P	W	C	D	I	U	B	U	U	F	G	W	P	Q	P	H	J	S	I	SP	K	E	E	Q	P	D	A	Y
01	M	M	M	M	M	U	M	T	M	N	N	N	N	N	U	U	N	U	N	N	P	P	U	J	Q	O	K	P	U	U	Q	L
02	I	E	I	F	F	L	G	W	I	E	Q	H	J	Q	G	W	Q	K	Q	H	J	Q	L	Q	Q	K	L	L	Q	Q	Y	L
03	E	H	W	K	G	Y	J	N	D	D	D	D	D	Y	D	Y	F	I	J	J	U	U	L	T	P	K		K	Q	Q	P	P
04	U	U	U	M	T	M	T	U	T	T	T	T	N	U	U	T	M	M	M	M	N	M	T	T	M	N	N	N	A	A	D	D
05	M	E	E	F	F	F	E	Q	M	H	H	H	H	G	G	G	I	I	I	J	J	J	J	Q	K	K	K	L	L	L	L	L
06	M	P	M	M	M	M	T	U	M	U	M	N	Q	N	Q	U	N	N	N	N	M	U	T	P	P	N	U	P	M	U	P	M
07	B	R	B	C	C	C	C	C	D	U	D	R	N	D	U	G	I	H	G	U	N	N	G	G	U	U	H	H	J	H	SP	SP
10	6	P	P	Q	R	R	S	S	W	U	P	S	U	R		U		M	U	S	N	SP	U	P	W	W	P	S	P	P	S	P
11	U	U	T	S	T	A	W	T	Q	Q	T	S	S	T	S	S	S	G	P	Q	P	P	P	P	W	W	P	P	S	Q	Q	SP
12	U	D	R	D	D	R	N	O	W	D	R	M		W	T	W	Z	P	R	S	R	U	Y	P	S	S	S	M	W	W	S	M
13	N	N	N	N	N	N	R	R	N	N	N	N	N	N	N	N	N	N	N	N	U	Y	W	W	P	U	P	P	W	U	P	Y
14	A	W	W	E	Y	Y	U	S	U	Y	U	U	Y	Y	Y	Y	S	W	U	E	U	U	U	U	U	S	P	P	Y	P	W	U
15	N	N	N	N	N	N	T	D	N	N	N	N	N	N	N	T	N	N	N	N	N	U	U	U	P	W	U	P	U	U	Q	X
16	D	T	O	D	C	D	C	T	P	T	T	S	U	P	C	T	Y	Y	Y	Y	Y	Y	Y	Y	Q	Y	Y	Y	C	U	Y	U
17	A		P	P	Q	A	T	T	U	U	SP	U	R	R	SP	SP	Q	U	Q	Q	P	P	P	P	Q	N	P	P	Q	W	S	A

free

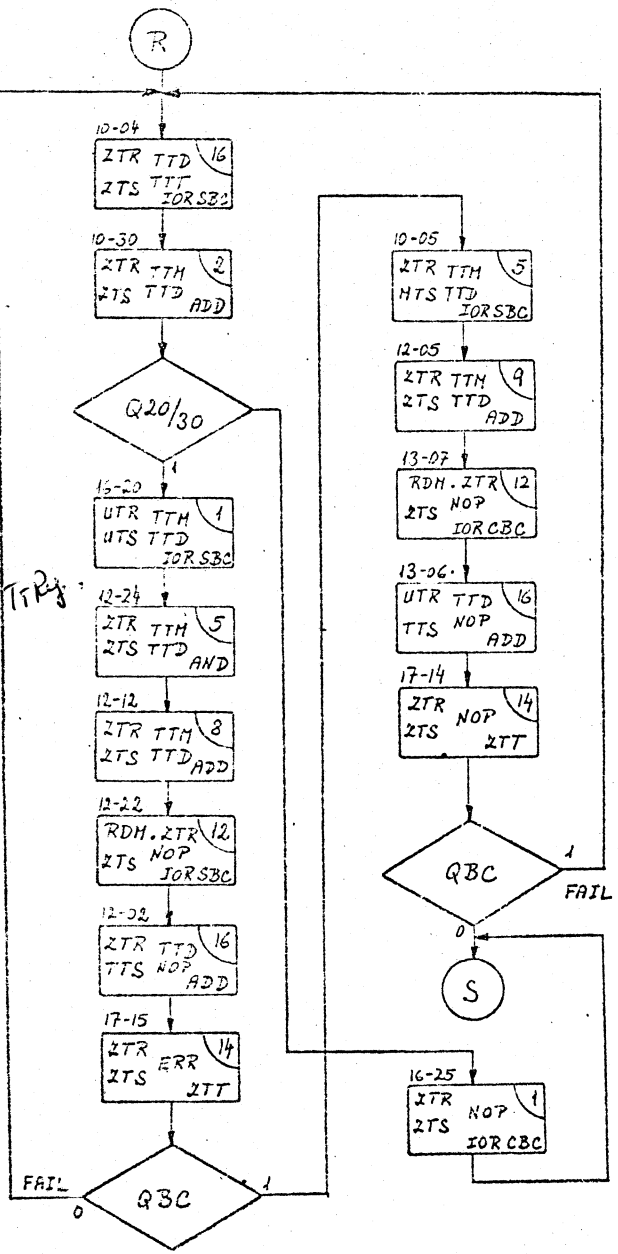
SECONDARY

PRIMARY	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	3	3	3	3	3	3	3	3
00	A	B	B	P	P	W	C	D	I	V	B	U	U	F	G	W	P	Q	P	H	J	W	I	SP	K	E	E	Q	P	D	L	W
01	M	M	M	M	M	U	M	T	M	N	N	N	N	N	U	U	N	U	N	N	P	P	U	J	Q	O	K	P	U	U	Q	L
02	I	E	I	F	F	L	G	W	I	A	Q	H	J	Q	G	W	Q	K	Q	H	J	Q	L	O	O	K	L	L	Q	Q	W	L
03	E	H	W	K	G	W	J	N	D	H	D	D	D	W	D	W	F	I	J	J	U	U	L	T	P	K	W	K	G	X	P	P
04	U	U	U	M	T	M	T	U	T	T	T	T	N	U	U	T	M	M	M	M	N	M	T	T	M	N	N	N	W	W	D	D
05	M	E	E	F	F	F	E	Q	M	H	H	H	H	G	G	G	I	I	I	J	J	J	J	Q	K	K	K	L	L	L	L	L
06	M	P	M	M	M	M	T	U	M	S	N	N	Q	N	Q	U	N	N	N	N	M	U	T	P	P	N	U	P	M	U	P	M
07	B	P	B	C	C	C	C	C	D	U	D	R	N	D	U	G	I	H	G	U	N	N	G	G	U	U	H	H	J	H	SP	SP
10	6	P	P	Q	R	R	S	S	W	U	P	W	U	R	W	U	W	M	U	W	N	SP	U	P	W	W	P	A	P	P	W	P
11	U	U	T	S	T	A	N	T	Q	Q	T	S	S	T	S	S	W	Q	M	Q	P	P	P	P	W	W	P	P	S	Q	Q	SP
12	U	D	R	D	D	P	N	O	W	D	R	N	W	W	T	W	W	P	R	S	R	U	W	P	S	S	S	S	M	W	W	M
13	N	N	N	N	N	N	R	R	N	N	N	N	N	N	N	N	N	N	N	N	U	W	W	W	P	U	P	P	W	U	P	W
14	A	W	W	E	W	W	U	W	U	W	U	U	W	W	W	W	W	W	U	E	U	U	U	U	U	S	P	P	W	P	W	U
15	N	N	N	N	N	N	T	D	N	N	N	N	N	N	N	T	N	N	N	N	N	U	U	U	P	W	U	P	U	U	Q	X
16	D	T	D	D	C	D	C	T	P	T	T	S	U	P	C	T	W	W	W	W	W	W	W	W	G	W	W	W	C	U	W	U
17	A	W	P	P	Q	A	T	T	U	U	SP	U	R	R	SP	SP	Q	U	G	Q	P	P	P	P	Q	W	P	P	Q	W	S	A

9810 DIAGNOSTIC TESTER

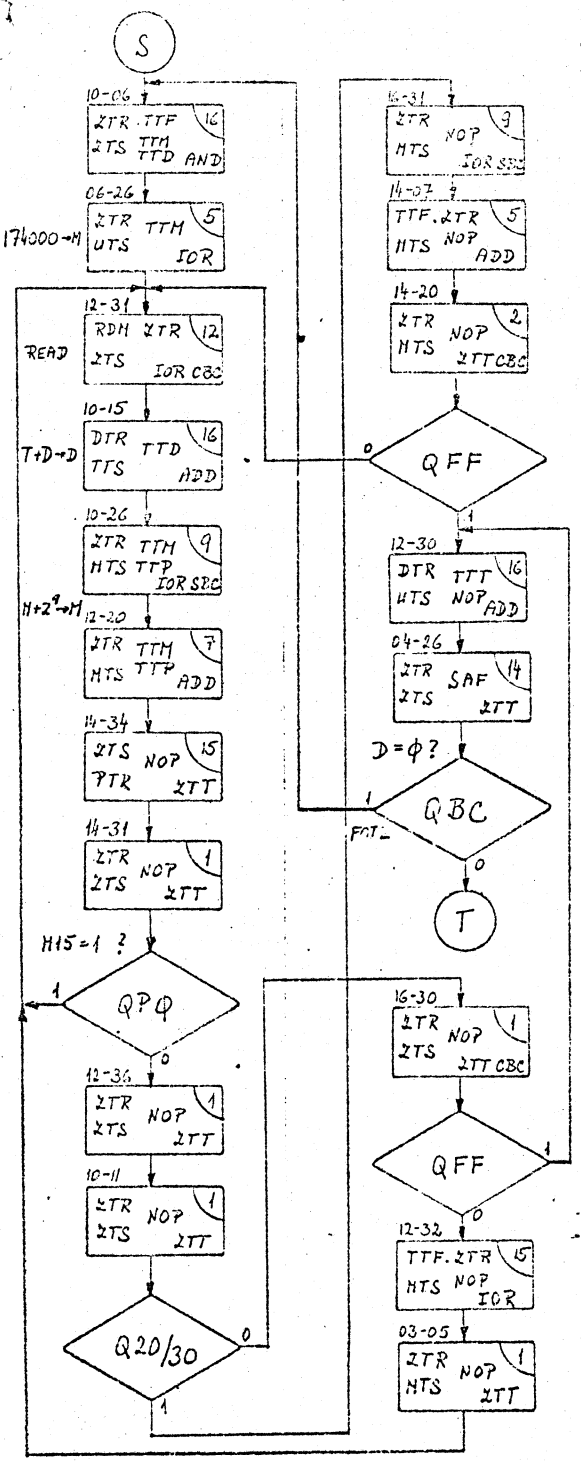
STATE ASSIGNMENTS

TEST 17 READ DRIVERS TEST



Tol405
1" TTR

TEST 18 CHIP ENABLE TEST



9820 A Constants

ΦΦΦΦ	164ΦΦ3
1ΦΦΦ	Φ45723 -
2ΦΦΦ	122625
3ΦΦΦ	Φ2Φ42Φ
4ΦΦΦ	Φ77476 -
5ΦΦΦ	Φ7Φ212
6ΦΦΦ	ΦΦ4115
7ΦΦΦ	Φ3143Φ
16ΦΦΦ	177744
Sum	Φ22614

TEST Block 155164

9821 Constant

174ΦΦΦ	Φ2Φ54Φ	9
175ΦΦΦ	Φ24526	10
ΦΦΦΦ	164ΦΦ3	1
1ΦΦΦ	Φ45723	2
2ΦΦΦ	164763	3
3ΦΦΦ	Φ3172Φ	4
4ΦΦΦ	Φ77476	5
5ΦΦΦ	Φ7Φ212	6
6ΦΦΦ	ΦΦ4115	7
7ΦΦΦ	Φ3143Φ	8
16ΦΦΦ	177744	
Sum.	14354Φ	

TEST Block Φ3424Φ

9830 Constants

ΦΦΦΦ	164121
1ΦΦΦ	ΦΦΦΦΦΦ
2ΦΦΦ	Φ22465
3ΦΦΦ	Φ21473
4ΦΦΦ	Φ2Φ116
5ΦΦΦ	Φ15423
6ΦΦΦ	Φ31453
7ΦΦΦ	Φ7431Φ
1ΦΦΦΦ	Φ6Φ653
11ΦΦΦ	Φ74112
12ΦΦΦ	ΦΦ7ΦΦ2
13ΦΦΦ	Φ66725
14ΦΦΦ	ΦΦΦΦΦ3
15ΦΦΦ	Φ74Φ46
16ΦΦΦ	Φ6273 5
17ΦΦΦ	ΦΦΦΦΦΦ
4ΦΦΦΦ	Φ374ΦΦ
Sum	1Φ4427

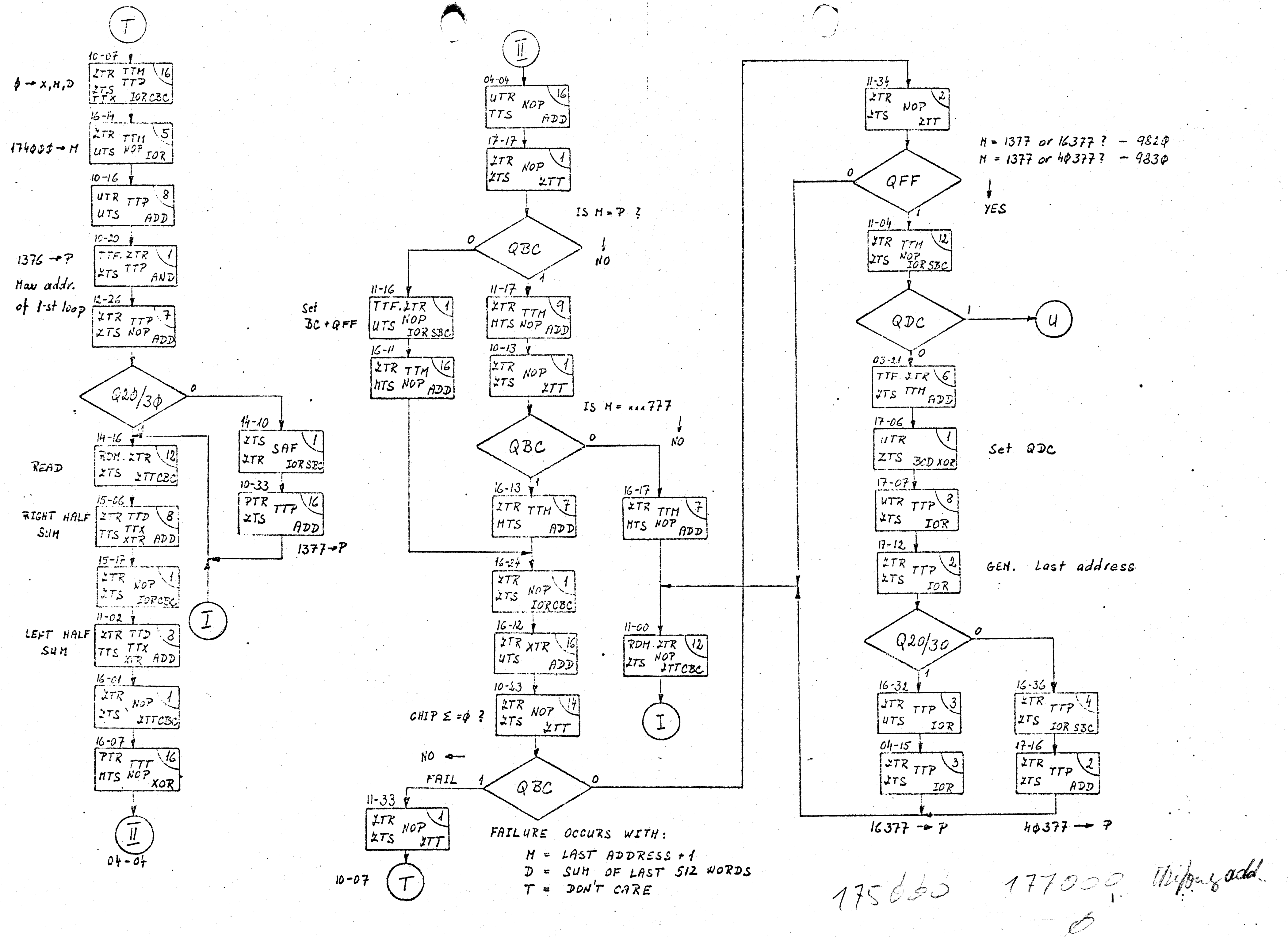
TEST Block Φ73351

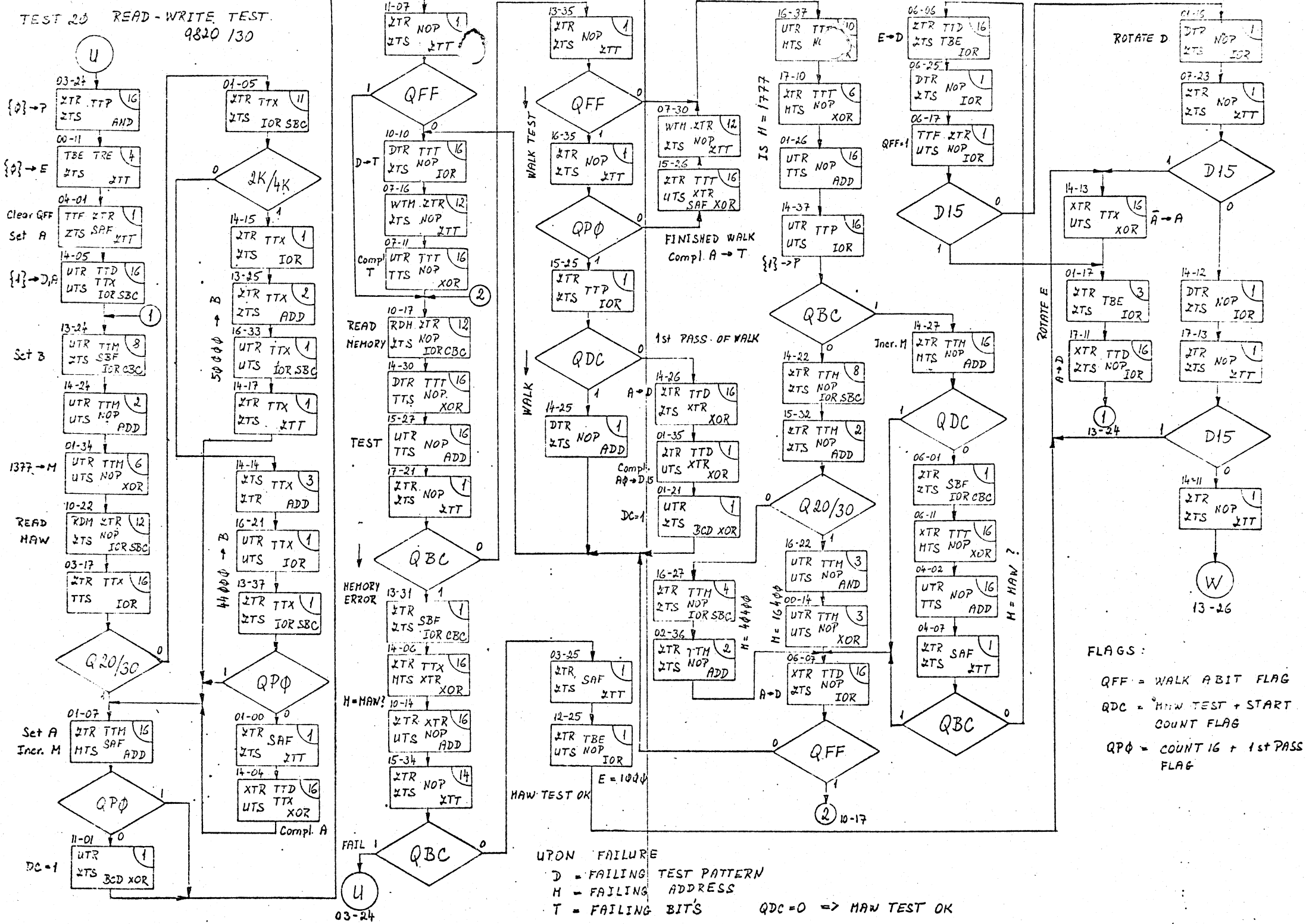
ADD ON ROM CONSTANTS

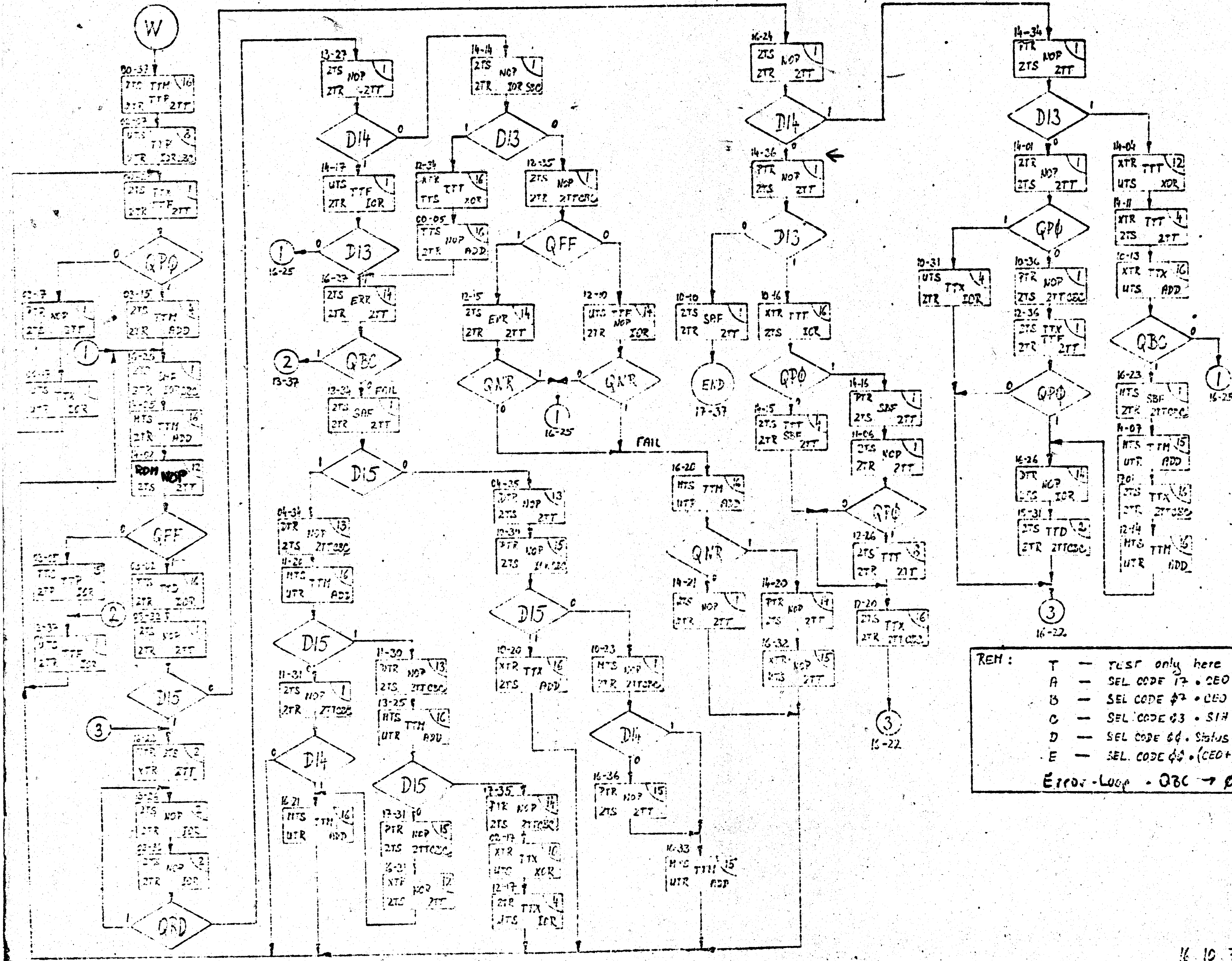
MATH.	ΦΦΦΦΦ2
	Φ25754/Φ31554
USER DEF.	ΦΦΦΦΦ4
	Φ63264
CASS.	ΦΦΦΦΦ7
	Φ21726
PC I.	ΦΦΦΦΦ1
	Φ671Φ6
PC II.	ΦΦΦΦΦ6
	Φ66743

MATR.	ΦΦΦ3Φ1
	Φ35661
Plot.	ΦΦ14ΦΦ
	Φ23524
String	ΦΦ6Φ11
	Φ63Φ3Φ
EXT. I/O	ΦΦΦ215
	Φ45472
TERM 1	ΦΦΦΦ77
	121661
BATCH	ΦΦΦ3ΦΦ
	ΦΦ4476
ADV. PR.	ΦΦΦ137

TEST 19 ROM TEST 982ϕ /3ϕ




TEST 20 READ-WRITE TEST
9820 /130
U
03-24
{0}→P
00-11
{0}→E
04-01
Clear QFF
Set A
{1}→D,A
14-05
1
13-24
Set B
14-24
01-34
1377→M
10-22
READ
HAW
03-17
Q 20/30
01-07
Set A
Incr. M
QPΦ
11-01
DC=1
01-05
2K/4K
14-15
5ΦΦΦ→B
13-25
16-33
14-17
14-14
16-21
4ΦΦΦ→B
13-37
11-07
QFF
10-10
D→T
07-16
07-11
Compl T
2
10-17
READ MEMORY
14-30
15-27
TEST
17-21
QBC
MEMORY ERROR
13-31
14-06
H=MAW?
10-14
15-34
FAIL 1
U
03-24
WALK TEST
13-35
16-35
QPΦ
15-25
QDC
WALK
14-25
1st PASS OF WALK
A→D
14-26
01-35
Compl. AΦ→D,15
01-21
DC=1
07-30
15-26
FINISHED WALK
Compl. A→T
16-37
17-10
01-26
14-37
{13}→P
IS H=1777
03-25
12-25
E=100Φ
MAW TEST OK
16-27
02-36
H=164Φ
H=4ΦΦΦ
A→D
06-06
E→D
06-25
06-17
QFF=1
D15
14-22
15-32
Incr. M
06-01
06-11
04-02
04-07
H=MAW ?
01-16
ROTATE D
07-23
14-13
Ā→A
01-17
ROTATE E
A→D
17-11
14-11
W
13-26
14-12
17-13
FLAGS :
QFF = WALK A BIT FLAG
QDC = MAW TEST + START COUNT FLAG
QPΦ = COUNT 16 + 1st PASS FLAG
UPON FAILURE
D = FAILING TEST PATTERN
H = FAILING ADDRESS
T = FAILING BITS
QDC=0 => MAW TEST OK



M reg	Instr	T reg	Rem
1Ø ØØØ	NOP	ØØØØØØ	
1Ø ØØ1	Preg const.	ØØ5Ø?1	
1Ø ØØ2	OTA Ø1, H	152:4?	
1Ø ØØ3	LIB Ø1, H	Ø22Ø41	T
1Ø ØØ4	OTA Ø1, C	143141	
1Ø ØØ5	MIB Ø1, C	Ø27?41	T
1Ø ØØ6	OTA ØØ, C	153141	
1Ø ØØ7	LIB Ø1, C	Ø23241	T
1Ø Ø1Ø	SFC ØØ, C	1637ØØ	T
1Ø Ø11	STC Ø1, H	1423Ø1	
1Ø Ø12	SFC Ø1, C	1637Ø1	T
1Ø Ø13	SFS Ø1, C	1635Ø1	T
1Ø Ø14	OTA Ø4, H	14214Ø	
1Ø Ø15	SFC Ø1, C	1677Ø1	T
1Ø Ø16	CLF Ø6	143746	
1Ø Ø17	SFC Ø6, C	167306	T
1Ø Ø2Ø	OTA Ø1, H	Ø42141	
1Ø Ø21	STC Ø1, H	1426Ø1	A
1Ø Ø22	SFS Ø4, H	1725Ø4	T
1Ø Ø23	OTA Ø4, H	Ø42144	B
1Ø Ø24	SFC Ø4, C	1735Ø4	T
1Ø Ø25	SFC Ø4, C	1637Ø4	T
1Ø Ø26	SFC Ø1, C	1635Ø1	T
1Ø Ø27	STF Ø1	1527?1	T
1Ø Ø3Ø	OTA Ø1, H	Ø42141	T C
1Ø Ø31	STA	16????	T
1Ø Ø32	OTA Ø1, C	Ø43141	T D
1Ø Ø33	STC Ø1, H	Ø5??Ø1	
1Ø Ø34	OTA Ø1, H	155141	E
1Ø Ø35	STF Ø1	156741	
1Ø Ø36	LIB Ø1, H	Ø72241	
1Ø Ø37	Sum const	ØØ1632	T

REM :

- T — test only here
- A — SEL CODE 17 • CEO → STOP from Interface
- B — SEL CODE Ø7 • CEO → CFI from Interface
- C — SEL CODE Ø3 • SIH → STOP • SSI — " —
- D — SEL CODE ØØ • Status 16 → SSI — " —
- E — SEL. CODE ØØ • (CEO + SIH) → Inverted data and status on DI lines

Error-Loop • QBC → Ø

W

16.10.72 D. Kulka

DT 9820/30

Secondary addr.

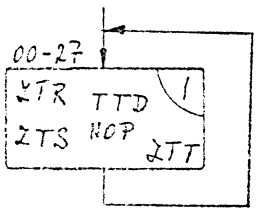
Primary addr.

	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17	20	21	22	23	24	25	26	27	30	31	32	33	34	35	36	37
00	A	B	B	P	P	W	C	D	I	U	B	Sp	U	F	G	W	P	Q	P	H	J	Sp	I	Sp	K	E	E	Q	P	P	A	X
01	U	M	M	M	M	U	M	U	M	N	N	N	N	N	U	U	N	U	N	N	P	P	U	J	Q	O	K	P	U	U	Q	L
02	I	E	I	F	F	L	G	W	I	E	Q	H	J	Q	G	W	Q	K	Q	H	J	Q	L	Q	Q	K	L	L	Q	Q	U	L
03	E	H	W	K	G	S	J	N	D	D	D	D	D	Sp	D	U	F	T	J	J	U	U	L		P	K	I	K	Q	Q	P	P
04	Sp	U	U	M	T	M	Sp	U	W	Sp	Sp	Sp	N	T	M	Sp	M	M	M	M	N	M	S	Sp	M	N	N	N	A	A	D	D
05	M	E	E	F	F	F	E	O	M	H	H	H	H	G	G	G	I	I	I	J	J	J	J	Q	K	K	K	L	L	L	L	L
06	M	U	M	M	M	M	U	U	M	U	M	N	Q	N	Q	U	N	N	N	N	M	U	S	P	P	N	P	P	M	Sp	P	M
07	B	B	B	C	C	C	C	C	D	U	D		N	D	U	G	I	H	G	U	N	N	G	G	U	Sp	H	H	Sp	H	Sp	Sp
10	O	P	P	Q	R	R	S	T	U	S	P	T	U	S	T	U	T	M	U	T	N	Sp	S	P	R	W	P	T	P	P	Sp	P
11	T	U	T	Sp	T	A	W	U	Q	Q	P	Sp	Sp	Sp	T	T	Sp	Q	P	Q	P	P	P	P	W	W	P	T	T	Q	Q	Sp
12	Sp	D	R	D	D	R	N	O	W	D	R	H	Sp	W	Sp	W	S	P	R	Sp	R	U	T	P	S	S	S	H	W	W	S	M
13	N	N	N	N	N	N	R	R	N	N	N	N	N	N	N	N	N	N	N	N	U	U	W	W	P	U	P	P	W	U	P	U
14	A	W	W	E	U	U	U	S	T	U	U	U	U	U	T	U	S	W	U	E	U	U	U	U	U	S	P	P	S	P	W	U
15	N	N	N	N	N	N	T	D	N	N	N	N	N	N	N	T	N	N	N	N	N	U	U	U	P	W	U	P	U	Sp	Q	X
16	D	T	D	D	C	D	C	T	P	T	T	T	T	P	C	T	R	U	U	W	T	R	Q	U	S	S	T	U	C	U	T	U
17	A	Sp	P	P	Q	A	T	T	U	U	T	U	R	R	T	T	Q	U	Q	Q	P	P	P	P	Q	W	P	P	Q	W	Sp	A

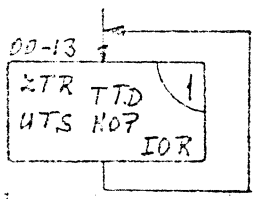
Addresses of ET 5490 Diagnostic tester

Test	Beg. addr.	Error addresses						
A Error simul.	17-37	11-05						
B BC FF test	07-01	00-01	00-02	00-12				
C XOR logic	07-03	16-34	16-04	16-06	16-16			
D Binary ADD	00-07	07-10	07-12	07-15	12-01	12-11	12-03	12-04
=//=		15-07	04-36					
E Preg test	05-06	02-01	02-11	14-03				
F Ereg test	05-03	02-04	02-03					
G Breg test	05-15	02-06	02-16	03-04				
H Areg test	05-14	02-13	02-23	03-01				
I Ereg>Areg	05-20	02-00	02-02	02-10				
J Mreg test	05-23	02-14	02-24	03-06				
K Treg test	05-30	02-21	02-31	03-03				
L Treg>Ereg	05-33	02-33	02-05	02-26				
M Binary ALU	01-02	06-12	06-02	06-03	06-04			
N Binary ALU	01-11	06-22	06-13	06-21	06-23	06-31	06-15	
P BCD ADD test	10-01	17-02	17-03					
Q Dez.ALU test	10-03	17-04						
R Read drivers	10-04	17-15	17-14					
S Chip select	10-06	04-26						
T ROM test	10-07	10-23						
U R/W test	03-24	15-34						
W I/Oreg test	13-26	14-36						
Sp Spec.ROM test	12-00	17-36						

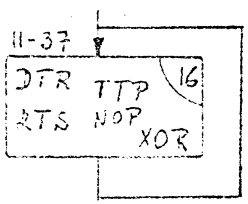
SP DT 09820/30



$\phi \rightarrow$ Dreg



$1 \rightarrow$ Dreg



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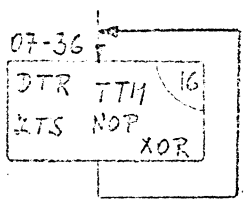

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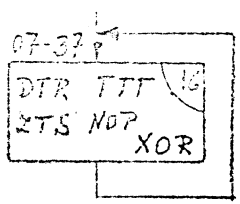
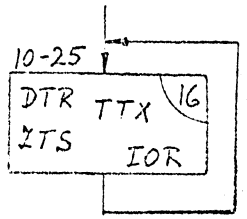
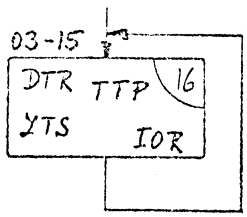


$D \rightarrow T$



$D \rightarrow$ A or B



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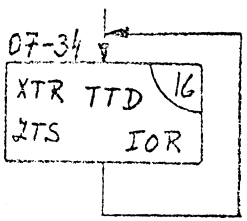
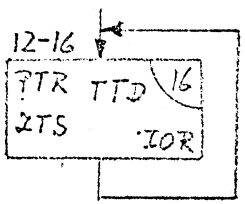


A or B $\rightarrow D$



$P \rightarrow D$

SP