HP 9000 Computer Systems

HEWLETT PACKARD

ASSEMBLY LANGUAGE

Reference Manual

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Assembly Language Reference Manual

92432-90001 November 1988

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HP 9000 Series 800

ASSEMBLY LANGUAGE

Reference Manual

HEWLETT PACKARD
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Preface

This manual describes the use of the HP Precision Architecture Assembler. Although the manual also summarizes the machine instruction set, you should refer to the *Precision Architecture and Instruction Reference Manual* for a complete description of these instructions. You need to be familiar with the machine instructions to use the Assembler.

Because the machine instruction set and Assembler directives were designed to optimize the new HP Precision Architecture, the resulting *assembly language* is tailored more to the needs of the computer rather than the programmer. Thus, we do not encourage using the Assembler for production programming purposes. For those cases, however, where efficiency or control require programming to be done in assembly language, this manual provides the necessary guidelines.

This manual is organized as follows:

Chapter 1 introduces the Assembler for HP 9000 Series 800 computers.

Chapter 2 explains programming the Assembler for HP-UX.

Chapter 3 describes the HP Precision Architecture Assembler control directives.

Chapter 4 summarizes the mnemonics and instruction format for the HP Precision Architecture machine instructions.

Chapter 5 contains several sample assembly language programs.

Chapter 6 describes the *assembly* (as) command and the ways to invoke the HP Precision Architecture Assembler under the HP-UX operating system.

Appendix A lists the error messages that the HP Precision Architecture Assembler may generate.

Appendix B lists the complete machine instruction set sorted alphabetically by mnemonic name.

This manual assumes that you are an experienced assembly language programmer. In addition, you should have detailed understanding of the HP Precision Architecture and hardware features, and a working knowledge of the HP-UX operating system, program structures, procedure calls, and stack unwind procedures. Consult the following manuals for additional details on specific subjects:

- *HP-UX Reference (09000-90009)* -- for information on HP's implementation of the UNIX* operating system.
- *Precision Architecture and Instruction Reference Manual (09740-90014)* -- for information on architecture and the instruction set.
- *Procedure Calling Conventions Manual (09740-90015)* -- for complete information about the use of the procedure calling convention.

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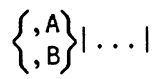
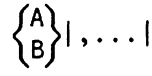
Conventions

NOTATION	DESCRIPTION
UPPERCASE	Within syntax statements, characters in uppercase must be entered in exactly the order shown, though you can enter them in either uppercase or lowercase. For example: SHOWJOB Valid entries are: showjob ShowJob SHOWJOB Invalid entries are: shojwob Shojob SHOW_JOB
italics	Within syntax statements, a word in italics represents a formal parameter or argument that you must replace with an actual value. In the following example, you must replace *filename* with the name of the file you want to release: RELEASE *filename*
punctuation	Within syntax statements, punctuation characters (other than brackets, braces, vertical parallel lines, and ellipses) must be entered exactly as shown.
{ }	Within syntax statements, when several elements within braces are stacked, you must select one. In the following equivalent examples, you must select ON or OFF: SETMSG {ON } {OFF} SETMSG {ON | OFF}
[ ]	Within syntax statements, brackets enclose optional elements. In the following example, brackets around ,TEMP indicate that the parameter and its delimiter are not required: PURGE *filename*[,TEMP] When several elements within brackets are stacked, you can select any one of the elements or none. In the following equivalent examples, you can select *devicename* or *deviceclass* or neither: SHOWDEV [*devicename*] [*deviceclass*] SHOWDEV [*devicename* | *deviceclass*]

Conventions (Continued)

NOTATION	DESCRIPTION

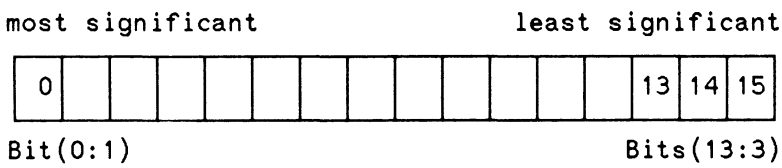
[...]	Within syntax statements, a horizontal ellipsis enclosed in brackets indicates that you can repeatedly select elements that appear within the immediately preceding pair of brackets or braces. In the following example, you can select *itemname* and its delimiter zero or more times, each instance of *itemname* preceded by a comma:
	
	`[,itemname][...]`
	
	If a punctuation character precedes the ellipsis, you must use that character as a delimiter to separate repeated elements. However, if you select only one element, the delimiter is not required. In the following example, the comma does not precede the first instance of *itemname*:
	
	`[itemname][,...]`

|...|	Within syntax statements, a horizontal ellipsis enclosed in parallel vertical lines indicates that you can select more than one element that appears within the immediately preceding pair of brackets or braces. However, each element can be selected only one time. In the following equivalent examples, you must select `,A` or `,B` or `,A,B` or `,B,A` :
	
	`{,A}`
	`{,B}|...|` 
	
	If a punctuation character precedes the ellipsis, you must use that character as a delimiter to separate repeated elements. However, if you select only one element, the delimiter is not required. In the following example, you must select `A` or `B` or `A,B` or `B,A` (the first element is not preceded by a comma):
	
	`{A}`
	`{B}|,...|` 

. . .	Within examples, horizontal or vertical ellipses indicate where portions of the example are omitted.
Δ	Within syntax statements, the space symbol Δ shows a required blank. In the following example, you must separate *modifier* and *variable* with a blank: `SET [(modifier)]Δ(variable);`
KEY	The symbol KEY indicates a key on the terminal's keyboard. For example, RETURN indicates the carriage return key.
CONTROL *char*	CONTROL *char* indicates a control character. For example, CONTROL Y means you must simultaneously press the control key and Y key on the terminal's keyboard.

Conventions (Continued)

NOTATION	DESCRIPTION
base prefixes	The prefixes %, #, and $ specify the numerical base of the value that follows: *%num* specifies an octal number *#num* specifies a decimal number *$num* specifies a hexadecimal number When no base is specified, decimal is assumed.
Bit (*bit:length*)	When a parameter contains more than one piece of data within its bit field, the different data fields are described in the format Bit (*bit:length*), where *bit* is the first bit in the field and *length* is the number of consecutive bits in the field. For example, Bits (13:3) indicates bits 13, 14, and 15:



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Chapter 1
The Assembly Language

This chapter provides an introduction to the assembly language for the HP 9000 Series 800 computers.

The HP 9000 Series 800 Assembly Language represents machine language instructions symbolically, and permits declaration of addresses symbolically as well. The Assembler's function is to translate an assembly language program, stored in a *source file*, into machine language. The result of this translation resides in a *relocatable object file*. The object file is relocatable because it can still be combined with other relocatable object files and libraries. Thus, it is necessary to relocate any addresses that the Assembler chooses for the symbols in the source program. This process of combining object files and libraries is performed by the linker, *ld*. The linker's task is to transform one or more relocatable object files into an executable *program file*. Every program must be linked before it can be executed, even if the source file is complete within itself and does not need to be combined with other files.

Assembler Features

The Assembler provides a number of features to make assembly language programming convenient. These features include:

- **Mnemonic Instructions.** Each machine instruction is represented by a mnemonic operation code, which is easier to remember than the binary machine language operation code. The operation code, together with to output a binary machine instruction to the object file.

- **Symbolic Addresses.** You can select a symbol to refer to the address of a location in virtual memory. The address is often referred to as the *value* of the symbol, which should not be confused with the value of the memory locations at that address. These symbols are called *relocatable symbols* because the actual addresses represented by such symbols are subject to relocation by the linker.

- **Symbolic Constants.** A symbol can also be selected to stand for an integer constant. These symbols are called *absolute symbols* because the values of such symbols are not relocatable.

- **Expressions.** Arithmetic expressions can be formed from symbolic addresses and constants, integer constants, and arithmetic operators. Expressions involving only symbolic and integer constants defined in the current module, or the difference between two relocatable constants, are called *absolute expressions*. They can be used wherever an integer constant can be used. Expressions involving the sum or difference between a symbolic address and an absolute expression are called *relocatable expressions*, or *address expressions*. The constant part of an expression, the part that does not refer to relocatable expressions, may use parenthesized subexpressions to alter operator precedence.

- **Storage Allocation.** In addition to encoding machine language instructions symbolically, storage may be initialized to constant values or simply reserved. Symbolic addresses, or *labels*, can be associated with these memory locations.

- **Symbol Scope.** When two or more object files are to be combined by the linker, certain symbolic addresses can be defined in one module and used in another. Such symbols must be *exported* from the defining module and *imported* into the using module. In the defining module, the symbol has *universal* scope, while in the using module, the symbol is *unsatisfied*. Other symbols declared in the source program that are not exported have *local* scope.

- **Subspaces and Location Counters.** You can organize code and data into separate subspaces, and into separate location counters within each subspace. The programmer can move among the subspaces and location counters, while the Assembler changes the code and data into the correct order.

- **Macro Processing.** A *macro* is a user-defined word which calls a sequence of instructions. Including a macro in a source program causes the sequence of instructions to be inserted into the program wherever the macro appears.

Structure of the Source Program

An assembly language program is a sequence of *statements*. There are three classes of statements:

- Instructions
- Pseudo-operations
- Directives

Instructions represent a single machine instruction in symbolic form. Pseudo-operations cause the Assembler to initialize or reserve one or more words of storage for data, rather than machine instructions. Directives communicate information about the program to the Assembler, but do not generally cause the Assembler to output any machine instructions.

An assembly statement contains four *fields*:

- Label
- Opcode
- Operands
- Comments

Each of these fields is optional, with the exception of the operands field, which cannot appear without an opcode field.

The label field is used to associate a symbolic address with an instruction or data location, or to define a symbolic constant using the .EQU pseudo-operation. This field is optional for all but a few statement types; if present, the label must begin in column one of a source program line. If a label appears on a line by itself, or with a comment only, the label is associated with the next address within the same subspace and location counter.

When the label field begins with the "#" character, it is not treated as a label. If "#" is followed by white space and an integer, the Assembler's line number counter, used when reporting errors, is reset to the value of the integer. Otherwise, the line beginning with "#" is ignored.

The opcode field contains either a mnemonic machine instruction, a pseudo-operation code, or the name of an Assembler directive. It must be separated from the label field by a blank or tab. For certain machine instructions, the opcode field can also contain *completers*, separated from the instruction mnemonic by commas. The completers allowed for each instruction are described in Chapter 4.

The operands field follows the opcode field, separated by a blank or tab. The meaning of the operands depends on the specific statement type, determined by the opcode. Machine instructions require from zero to four operands, which can denote register numbers or memory addresses, depending on the specific instruction.

The comments field is introduced with a semicolon, and causes the Assembler to ignore the remainder of the source line. A comment can also appear on a line by itself.

Figure 1-1 contains several assembly language statements and identifies each of the four fields described above.

```
Label    Opcode    Operands                  Comments

JAN      .EQU      1                         ;declares a symbolic constant
SUM      .WORD     0                         ;reserve a word and set to zero
LOOP     LDW       4(%r1),%r2
         ADD       %r2,%r3,%r4
         STW       %r4,SUM-$global$(%dp)
         BL        LOOP,%r0
```

Figure 1-1. Assembly Language Statements

Statements are normally written on separate lines. It is sometimes useful, especially when using a macro preprocessor, to be able to write several statements on one line. This can be done by separating the statements with the " ! " character. When this feature is used, a label can be placed only on the first statement of the line, and a comment can only follow the last statement on the line. The .LABEL directive can override this condition by providing a means for declaring a label within a multi-statement line. %r is defined in "Registers and Register Mnemonics" later in this chapter.

Symbols and Constants

Both addresses and constants can be represented symbolically. Labels represent a symbolic address except when the label is on an .EQU directive. If the label is on an .EQU directive, the label represents a symbolic constant. These symbols are composed of uppercase and lowercase letters, digits, dollar signs, and underscores. Symbols cannot begin with a digit. The Assembler considers uppercase letters and lowercase letters in symbols to be distinct. The mnemonics for operation codes, directives, and pseudo-operations can be written in either case. There is no explicit limit on the length of a symbol. The following are examples of legal symbols:

```
$START$     _start      PROGRAM
M$3         $global$    $$mulI
main        P_WRITE     loop1
```

The following are examples of illegal symbols:

```
LOOP#1      Contains an illegal character
1st_time    Begins with a digit
```

Integer constants are written in either decimal, octal, or hexadecimal notation. Table 1-1 lists the ranges of these integer constants.

Table 1-1. Integer Constants

	Signed	Unsigned
Decimal	-2147483648 through 2147483647	0 through 4294967295
Octal	020000000000 through 017777777777	0 through 037777777777
Hexadecimal	0x80000000 through 0x7FFFFFFF	0 through 0xFFFFFFFF

The period (.) is a special symbol reserved to denote the current offset of the location counter. It is useful in address expressions to refer to a location relative to the current instruction or data word. This symbol is considered relocatable, and can be used anywhere a relocatable symbol can be used, with the exception of the label field.

NOTE

A symbol whose initial characters are "L$" will not be passed to the linker. Symbols beginning with "L$" may only be used for local code labels and absolute values.

Registers and Register Mnemonics

Series 800 processors have four sets of registers:

- General
- Floating-point
- Space
- Control

General registers are the focus of almost all activity. Data is loaded from memory into general registers and stored into memory from general registers. All arithmetic and logical operations are performed on the contents of the general registers. Each general register is 32 bits wide. There are 32 general registers, denoted %r0 through %r31. General register 0 is special because "writes" into it are ignored, and it always reads as zero. The remaining general registers can be used normally, with the caution that %r1 is the implicit target register for the ADDIL instruction, and %r31 is the implicit link register for the BLE instruction.

The floating-point registers are physically present only on systems with a floating-point coprocessor. On systems without the coprocessor, their presence and behavior is emulated by the HP-UX operating system. There are 16 floating-point registers, each capable of holding either a single or double-precision floating-point number in IEEE format. These registers are denoted %fr0 through %fr15. Registers %fr1, %fr2 and %fr3 are exception registers and are not available to the programmer. Floating-point register 0 contains a permanent floating-point zero when used in an arithmetic operation; when written or read with floating-point loads or stores, the floating-point status register is actually set.

The space registers form the basis of the virtual memory system. Each of the eight space registers can hold a 16 or 32-bit space identifier, depending on the hardware model (the Series 840 uses 16-bit space registers). The space registers are denoted %sr0 through %sr7. Space register 0 is set implicitly by the BLE instruction, and space registers 5 through 7 cannot be modified except by the operating system.

The control registers contain system-state information. There are 25 control registers, denoted %cr0 and %cr8 through %cr31. Of these registers, only %cr11, the shift amount register, and %cr16, the interval timer, are accessible to the user-level programmer.

Register operands are denoted as integer constants since the Assembler can differentiate between general registers, space registers, floating-point registers, and literal values from context. In order to make assembly code more readable, symbolic constants can be defined with the .EQU directive, and used as register operands. In addition, the Assembler has many predefined mnemonic register names that can be used instead of integers. These predefined registers have register types associated with them. The only way to obtain register type checking is to use the .REG directive to assign a predefined register in the operand field to a user-defined name in the label field. This permits type checking on user-defined register names. The following example demonstrates correct usage of the .REG directive:

```
tblptr      .REG      %r20
```

Predefined mnemonic registers are shown in the following tables. All of the mnemonics begin with the % character, so they do not conflict with any programmer-defined symbols.

Table 1-2. General Registers

%r0	%r8	%r16	%r24
%r1	%r9	%r17	%r25
%r2	%r10	%r18	%r26
%r3	%r11	%r19	%r27
%r4	%r12	%r20	%r28
%r5	%r13	%r21	%r29
%r6	%r14	%r22	%r30
%r7	%r15	%r23	%r31

Table 1-3. Floating-Point Registers

%fr0	%fr4	%fr8	%fr12
%fr1	%fr5	%fr9	%fr13
%fr2	%fr6	%fr10	%fr14
%fr3	%fr7	%fr11	%fr15

Table 1-4. Space Registers

%sr0	%sr2	%sr4	%sr6
%sr1	%sr3	%sr5	%sr7

Table 1-5. Control Registers

Registers	Synonyms	Registers	Synonyms
%cr0	%rctr	%cr20	%isr
%cr8	%pidr1	%cr21	%ior
%cr9	%pidr2	%cr22	%ipsw
%cr10	%ccr	%cr23	%eirr
%cr11	%sar	%cr24	%tr0 %ppda
%cr12	%pidr3	%cr25	%tr1 %hta
%cr13	%pidr4	%cr26	%tr2
%cr14	%iva	%cr27	%tr3
%cr15	%eiem	%cr28	%tr4
%cr16	%itmr	%cr29	%tr5
%cr17	%pcsq	%cr30	%tr6
%cr18	%pcoq	%cr31	%tr7
%cr19	%iir		

A few additional predefined register mnemonics are provided in Table 1-5 to match the standard procedure calling convention. This is discussed briefly in Chapter 2. For more detailed information see the *Procedure Calling Conventions Manual.*

Table 1-6. Procedure Calling Convention Registers

Register	Synonyms	Description
%r2	%rp	Return link
%r23	%arg3	Argument word 3
%r24	%arg2	Argument word 2
%r25	%arg1	Argument word 1
%r26	%arg0	Argument word 0
%r27	%dp	Data pointer
%r28	%ret0	Return value
%r29	%ret1 %s1	Return value, static link
%r30	%sp	Stack pointer
%r31	%mrp	Millicode return link
%sr1	%sret %sarg	Return value, argument

Expressions

Arithmetic expressions are often valuable in writing assembly code. The Assembler allows expressions involving integer constants, symbolic constants, and symbolic addresses. These terms can be combined with the standard arithmetic operators shown in Table 1-6.

Table 1-7. Standard Arithmetic Operators

Operator	Operation
+	Integer addition
-	Integer subtraction
*	Integer multiplication
/	Integer division (result is truncated)

The multiplication and division operators have *precedence* over addition and subtraction. That is, multiplications and divisions are performed first from left to right, then additions and subtractions are performed from left to right. Thus, the expression 2+3*4 evaluates to 14.

Expressions produce either an absolute or a relocatable result. Any operation involving only absolute terms yields an absolute result. Relocatable terms are allowed only for the + and - operators. The legal combinations involving relocatable terms are shown in Table 1-7.

Table 1-8. Legal Combinations For Relocatable Terms

Operation	Result
Absolute + Relocatable	Relocatable
Relocatable + Absolute	Relocatable
Relocatable - Absolute	Relocatable
Relocatable - Relocatable (defined locally)	Absolute

NOTE

The combination "relocatable-relocatable+relocatable" is not permitted.

For example, assume the symbols MONTH and YEAR are relocatable, and JANUARY and FEBRUARY are absolute. The expressions MONTH+JANUARY and MONTH+FEBRUARY-4 are relocatable, while the expressions YEAR-MONTH and FEBRUARY-4 are absolute. The expression MONTH+JANUARY*4 is also legal and produces a relocatable result, because JANUARY*4 is evaluated first, producing an absolute intermediate result that is added to MONTH. The expression MONTH+YEAR is illegal, because the sum of two relocatable terms is not permitted.

Because all Series 800 instructions are a single word in length, it is not possible to form a complete 32-bit address in a single instruction. Thus, it is likely that the Assembler (or linker) may not be able to insert the final address of a symbol into the instruction as desired. For example, to load the contents of a word into a register, the following instruction could be used:

```
LDW       START,%r2
```

Because the LDW provides only 14 bits for the address of START, the Assembler or linker prints an error message if the address of START requires more than 14 bits. There are two instructions, LDIL and ADDIL, whose function is to form the leftmost 21 bits of a 32-bit address. The succeeding instruction, by using the target of the LDIL or ADDIL as a base register, needs only 11 bits for the remainder of the address. The Assembler provides special operators, called *field selectors*, that extract the appropriate bits from the result of an expression. With the field selectors L% and R%, the previous example can be recoded as follows:

```
LDIL      L%START,%r1             ;put left part into r1
LDW       R%START(%r1),%r2        ;add r1 and right part
```

The field selectors are always applied to the final result of the expression. They cannot be used in the interior of an expression. The field selectors shown are the two most commonly used. Table 1-8 shows all the available field selectors and their meanings.

Table 1-9. Available Field Selectors

Field Selector	Meaning
F%	Full 32 bits (default)
L%	Right-justified, high-order 21 bits
R%	Low-order 11 bits
LS%	High-order 21 bits after rounding to nearest page
RS%	Low-order 11 bits, sign extended
LD%	Right-justified, high-order 21 bits after rounding to next page
RD%	Low-order 11 bits, with negative sign
LR%	L%value with constant rounded to nearest multiple of 8192
RR%	R%value with constant rounded to nearest multiple of 8192, plus the difference of the constant and the rounded constant.

Since a page is 2048 bytes long, the selectors L%, LS%, and LD% extract a page number, and the corresponding selectors R%, RS%, and RD% extract the offset relative to that page. The distinction is whether the offset is always positive and between 0 and 0x7ff (L%-R%), always negative and between -0x800 and -1 (LD%-RD%), or between -0x400 and 0x3ff (LS%-RS%). The LR% and RR% prefixes are used for accessing different fields of a structure, allowing the sharing of the LR% computation. The distinction is only important when using short addressing near a quadrant boundary, since only the left part is used to select a space register. Chapter 2 explains this further. Each pair is designed to work together just as L% and R% did in the previous example.

The field selectors may also be written F', L', R', LS', RS', LD', RD', LR', and RR'.

Parenthesized Sub-Expressions

The constant term of an expression may contain parenthesized sub-expressions that alter the order of evaluation from the precedence normally associated with arithmetic operators. For example:

```
LABEL1-LABEL2+((6765+(2048-1))/2048)*2048
```

contains a parenthesized sub-expression that rounds a value up to a multiple of 2048.

Absolute symbols may be equated to constant terms containing parenthesized sub-expressions as in the following sequence:

```
BASE    .EQU    0x200
N_EL    .EQU    24
SIZE    .EQU    (BASE+4)*N_EL
```

NOTE

The use of parentheses to group sub-expressions may cause ambiguities in statements where parenthesized register designators are also expected.

Operands and Completers

Machine instructions generally require one, two, or three operands that tell the processor what data to use and where to store the result. Operands can identify a register, a location in memory, or an immediate constant (that is, data that is coded into the instruction itself). The operation code determines how many, and what kinds of operands are required.

The most frequently used machine instructions are those that involve only general registers. Most of these instructions require three register operands that specify two source registers and one target register. Each register operand must be an absolute expression whose value is between zero and 31. Typically, the operand is just an integer constant, which is a symbolic constant that has been equated to a register number, or a register mnemonic.

Register operands may use *typing* by means of a predefined or user-defined register name. Users may define register names with the .REG directive as in the following example:

```
tblptr      .REG      %r20
```

Several instructions also provide access to space and control registers. When a space register is expected, a register mnemonic or absolute expression whose value is between zero and 7 must be given. For a control register, the value must be zero, or between 8 and 31. The following examples show a few machine instructions with register operands:

```
SCRATCH     .EQU      %r18
            ADD       %r3,%r7,%r4          ;r3 + r7 -> r4
            SUB       1,2,3                ;r1 - r2 -> r3
            OR        %r7,%r3,%r8          ;inclusive or of r7,r3 -> r8
            OR        SCRATCH,0,%r7        ;copy r18 to r7 (note: r0 = 0)
            MTCTL     %r2,%sar             ;set shift amount register (cr11)
            MFSP      %sr4,%r10            ;fetch contents of sr4
```

Operands designating memory locations usually consist of an expression and a general register used as a base register. Some instructions also require a space register designation. In general, such operands are written in the form `expr(sr,gr)` or `expr(gr)`, as in the following examples:

```
local_off   .EQU      -64
            LDW       4(%dp),%r2
            STW       %r0,local_off-4(0,%sp)
            LDW       0(%sr3,%r2),%r9
            BLE       $$mulI(%sr7,0)
```

Notice that the space register can be omitted on instructions that require it, as in the first LDW instruction shown in the previous example. If only one register is given, it is assumed to be the general register, and the space register field in the machine instruction is set to zero. Remember that the register mnemonics are equivalent to an integer constant. If the second LDW instruction is written as follows:

```
LDW     0(%r2,%sr3),%r9          ;wrong !
```

an error message is displayed.

The expression in a memory operand is either absolute or relocatable. Absolute expressions are meaningful when the base register contains the address of an array, record, or the stack pointer to which a constant offset is required. Relocatable expressions are meaningful when the base register is r0, or when

the base register contains the left part of a 32-bit address as illustrated in the following example:

```
LDIL        L%glob,r1                   ;set up r1 for STW
STW         %r9,R%glob(%r1)
```

Immediate operands provide data for the machine language instruction directly from the bits of the instruction word itself. A few instructions that use immediate operands are shown below:

```
ADDIL       L%var,%dp
LDIL        L%print,%r1
ADDI        4,%r3,%r5
SUBI        0x1C0,%r14,%ret0
```

Completers are special flags that modify an instruction's behavior. They are written in the opcode field, separated from the instruction mnemonic by a comma. The most common type of completer is a condition test. Many instructions can conditionally trap or nullify the following instruction, depending on the result of their normal operation. For example, notice the completers in the sequence below:

```
ADD,NSV     %r1,%r2,%r3
BL,N        handle_oflo,%r0
OR          %r3,%r4,%r5
```

The ,NSV in the ADD instruction nullifies the BL instruction if no overflow occurs in the addition operation, and execution proceeds with the OR instruction. If overflow does occur, the BL instruction is executed, but the ,N completer on the BL specifies that the OR instruction in its delay slot should not be executed.

Each class of machine instructions defines the set of completers that can be used. These are described with the individual instructions in Chapter 4.

Macro Processing

A macro is a user-defined word that calls a sequence of instructions. Including a macro in a source program causes the sequence of instructions to be inserted into the program wherever the macro appears.

A user may define a word as a macro by using the .MACRO directive.

Detailed information about macro arguments, placement and redefinition of macros, nested macro definitions, and nested macro calls is in Chapter 3 of this manual.

Defining New Instructions With Macros

If you are testing new CPU's or coprocessors, you may need to use opcodes that are unknown to the Assembler. A variant of a macro definition may be used to create a mnemonic for the instruction. After being defined, the new mnemonic instruction can be invoked as easily as a standard instruction.

Opcodes, subopcodes, completers, and operands are encoded into the instruction word in a bit intensive manner because all HP Precision Architecture instructions are one word, or 32-bits, in length. Bit fields do not usually fall on byte or nibble boundaries. A nibble is a half byte.

To write a macro, you must specify explicitly which bit fields are to contain constants and which are to contain macro arguments. The macroprocessor has no built-in knowledge of instruction formats. Defining new instructions through macros is only possible because a convenient way to delimit bit fields has been provided. It is up to the programmer to choose the correct bit field.

Bit positions within the 32-bit word are numbered from zero to 31, from left to right. A bit range is indicated by the starting bit position followed by the ending bit position. The two bit positions should be separated by two periods and enclosed in braces. The bit field beginning at bit position 6 and ending at bit position 10 is represented as:

```
{6..10}
```

If the bit field being assigned from is bigger than the bit field being assigned to, then a warning is issued and the *assigned from* bit field is truncated on the left. When no bit field is specified for the *assigned from* value, low-order bits are used until the value of the *assigned from* bit field becomes the same as the width of the *assigned to* bit field. The *assigned to* bit field must always be specified.

No sign extension is provided by the Macro-assembler when bit fields are generated.

Example

```
PACK    .MACRO              BASE,GREG,SREG,OFFSET
        {0..5}=0x3E{26..31}
        {6..10}=BASE{27..31}
        {11..15}=GREG{27..31}
        {16..17}=SREG{30..31}
        {18..31}=OFFSET{18..31}
       .ENDM
```

The above macro definition defines the macro PACK. The following explanation assumes that PACK is invoked:

```
PACK    %sp,%r19,%sr0,-52
```

Bit field 0 through 5 contains the six low-order bits of the new opcode *0x3E*, or binary 111110, entered as a constant in the macro definition. Bit field 6 through 10 contains general register 30, or binary 11110. These are the five low-order bits of the argument BASE in the macro definition. Bit field 11 through 15 contains general register 19, or binary 10011. These are the five low-order bits of the argument GREG in the macro definition. Bit field 16 through 17 contains space register 0 and represents the five low-order bits of the argument SREG in the macro definition. Bit field 18 through 31 contains binary 11111111001100, the OFFSET -52 which was entered as an argument to the macro definition.

Chapter 2
Programming for HP-UX

The Assembler is a flexible tool for writing programs, but every operating system imposes certain conventions and restrictions on the programs that are intended to run on that system. This chapter discusses the conventions that must be understood in order to write assembly language programs and procedures for the HP 9000 Series 800 HP-UX operating system. Several Assembler directives are mentioned in this chapter to place them in a meaningful context. A full discussion of these directives can be found in following chapters.

Spaces

Virtual addressing on the HP Precision Architecture is based on *spaces*. A virtual address is composed of a space identifier, which is either 16 or 32 bits long (depending on the hardware model), and a 32-bit offset within the space. Thus, each space can contain up to 4 gigabytes, and there is a large supply of spaces.

Every program on an HP-UX system is assigned two spaces when it is loaded for execution by the operating system: one for code, and one for data. The HP-UX operating system makes the code space *read only*, so that it can be shared whenever several processes are executing the same program. The data space is writable by the new process, and is private to that process; that is, every process has a unique data space.

The actual space identifiers assigned to these two spaces can vary from one execution of the program to the next; these numbers cannot be determined at compile time or link time. Generally, programmers do not need to be concerned with the space identifiers, since the operating system places them in two reserved space registers, where they remain for the duration of program execution. The identifier of the code space is placed in space register 4 (`sr4`) and the identifier of the data space is placed in `sr5`.

When writing an assembly language program, declare a space named `$TEXT$` for executable code, and a space named `$PRIVATE$` for modifiable data. Constant data, literals that you do not plan to modify during program execution, can be placed in either space. Placing constant data in the `$TEXT$` space decreases the size of the non-sharable part of your program and improves the overall efficiency of the operating system.

The particular space registers mentioned above play an important role in virtual addressing. While many of the branching instructions, such as `BL`, `BLR`, and `BV`, are capable of branching only within the currently executing code space (called PC-*space*), two of the branching instructions, `BE` and `BLE`, require that you specify a space register as well as an offset. These instructions allow you to branch to code executing in a different space. On HP-UX systems, all code for a program is contained in one space, so all `BE` and `BLE` instructions should be coded to use `sr4`.

In contrast, the memory reference instructions, such as LDW and STW, allow a choice between two forms of addressing: long and short. With long addressing, you can choose any of the space registers 1 through 3 for the space identifier part of the virtual address. The space offset is formed as the sum of an immediate displacement and the contents of a general register. With short addressing, one of the space registers

between 4 through 7 is chosen automatically, based on the high-order two bits of the general register. Each space addressed by these four space registers is effectively divided into four *quadrants*, with a different quadrant of each space accessible via short addressing.

On HP-UX systems, all of a program's code is placed in the first quadrant of the $TEXT$ space (space offsets from 0 through 0x3FFFFFFF). The data is placed in the second quadrant of the $PRIVATE$ space (space offsets from 0x40000000 through 0x7FFFFFFF). Thus, literal data in the code space and modifiable data in the data space can be addressed using the short addressing technique, without any concern for the space registers.

You can define spaces other than $TEXT$ and $PRIVATE$ in a program file by declaring a special kind of space called an *unloadable space*. Unloadable spaces are treated as normal spaces by the linker, but as the name implies, are not actually loaded when a program is executed. Unloadable spaces are typically used by compilers to store extra information within a program file. The most common example of an unloadable space is $DEBUG$, which is used to hold symbolic debugging information.

The *sort key* attribute allows the programmer to control the placement of a space relative to the other spaces. The linker places spaces with lower sort keys in front of spaces with higher sort keys.

The .SPACE directive is used to declare spaces. The assembly language programmer is not required to fill one space before beginning another. When a space is first declared, the Assembler begins filling that space. The .SPACE directive can also be used to return to a previously declared space, and the Assembler continues to fill it as if there had been no intervening spaces.

Subspaces

While a space is a fundamental concept of the architecture, a subspace is just a logical subdivision of a space. The Assembler places the program's code and data into subspaces rather than spaces. Each subspace *belongs* to the space that was current when the subspace was first declared. The linker groups subspaces into spaces as it builds an executable program file. For more details see the *ld* (UTIL) entry in the *HP-UX Reference* manual. When the linker combines several relocatable files, it groups the subspaces from each file by name, so that all subspaces with the same name are placed contiguously in the program.

Subspaces have several attributes. The *alignment* attribute specifies what memory alignment (in bytes) is required in the virtual address space. The alignment can be any power of two, from 1 through 2048, inclusive. Typically, the alignment is 4 or 8 to specify that the beginning of the subspace must be word or double-word aligned. Normally, the alignment attribute is computed automatically by the Assembler from the largest .ALIGN directive used within the subspace.

The *quadrant* attribute assigns the subspace to one of the four quadrants of its space. On HP-UX systems, all subspaces in the code space must be in quadrant 0, and all subspaces in the data space must be in quadrant 1.

The *access rights* attribute specifies the access rights that should be given to each physical page in the subspace. On HP-UX systems, all subspaces in the code space must have access rights of 0x2C (code page executable at any privilege level). All subspaces in the data space must have access rights of 0x1F (data page readable and writable at all privilege levels).

The *sort key* attribute allows the programmer to control the placement of a subspace relative to the other subspaces in its space. The linker places subspaces with lower sort keys in front of subspaces with higher sort keys.

The .SUBSPA directive is used to declare a subspace and its attributes. As with spaces, the assembly language programmer can switch from one subspace to another, and the Assembler will fill each subspace independently as if the source code had been presented one complete subspace at a time. When the .SPACE directive is used to switch spaces, the Assembler remembers the current subspace in each space.

Several additional Assembler directives are provided as shorthand to declare and switch to some standard spaces and subspaces. For example, the .CODE directive switches to the $TEXT$ space and the $CODE$ subspace, and the .DATA directive switches to the $PRIVATE$ space and the $DATA$ subspace.

You can declare as many subspaces as you can use, but the sort key attribute should be used carefully, because the stack unwind mechanism reserves a range of sort keys (56 through 88) for use with the $CODE$ subspace. Some of the standard subspaces and sort keys used by the compilers are shown in Table 2-1. Directives that generate commonly used spaces and subspaces are found in Table 3-4.

Table 2-1. Standard Subspaces and Sort Keys

Space	Subspace	Sort Key	Use
$TEXT$		8	
	$MILLICODE$	8	Millicode library routines
	LIT	16	Literals
	$CODE$	24	Normal code
	$UNWIND_START$	56	Stack unwind
	$UNWIND$MILLICODE$	62	Stack unwind
	$UNWIND$	64	Stack unwind
	$UNWIND_END$	72	Stack unwind
$PRIVATE$		16	
	$GLOBAL$	8	Pascal global variables
	$DATA$	24	Normal global and static data
	$COMMON$	24	FORTRAN BLOCK DATA
	BSS	80	Uninitialized data and common

NOTE

By linker convention, programs should avoid using sort keys less than 8 in either space.

Location Counters

Just as spaces can be divided into subspaces, subspaces can be further divided by using location counters. You can use up to four location counters in each subspace, and the Assembler fills a separate area for each location counter. When the assembly is complete, the subspace is formed by concatenating each of these areas. All references relative to a location counter are relocated so that they are relative to the complete subspace.

Unlike subspaces, however, the use of location counters is completely local to the Assembler. Once the subspace is formed at the end of the assembly, the distinction among the individual areas built by location counters disappears. No further reordering or grouping related to location counters is performed by the linker.

This facility allows you to assemble related data into disjoint pieces of a subspace while keeping the source code in a convenient order.

The `.LOCCT` directive is used to switch from one location counter to another. The Assembler automatically remembers the previous value of each location counter within each subspace. When the `.SUBSPA` directive is used to switch subspaces, the Assembler automatically begins using the location counter that was last in effect in the new subspace.

Compiler Conventions

In order to write assembly language procedures that can both call to and be called from high-level language procedures, it is necessary to understand the standard procedure calling convention and other compiler conventions.

On many computer systems, each high-level language has its own calling convention. Consequently, calls from one language to another are sometimes difficult to arrange, except through assembly code. The architecture generally prescribes very few operations that must be done to effect a procedure call, and there is often a pair of machine-language instructions to call a procedure and return from one. The HP Precision Architecture provides no special procedure call or return instructions. There is, however, a standard procedure calling convention for all high-level languages as well as the Assembler. It is tuned for the architecture, and is designed to make a procedure call with as few instructions as possible.

Besides defining a uniform call and return sequence for all languages, the calling convention is important for other reasons as well. In order to streamline the calling sequence, the return link is not saved on the stack unless necessary and the previous stack pointer is rarely saved on the stack. Thus, it is not usually possible to obtain a stack trace at an arbitrary point in the program without some additional static information about each procedure's stack frame size and usage. For example, you could not obtain a stack trace while debugging or analyzing a core dump, or using the try-recover feature in Pascal. Obtaining a stack trace is made possible by the *stack unwind* mechanism. It uses special *unwind descriptors* that contain the exact static information needed for each procedure. These descriptors are generated automatically by all high-level compilers as well as the Assembler. Each descriptor contains the starting and ending address of a procedure's object code, plus that procedure's stack frame size, and a few flags indicating, among other things, whether the return link is saved on the stack. Given the current program counter and stack pointer, the stack unwind mechanism can determine the calling procedure by finding the return link either in a register or on the stack. Also, it can determine the previous stack pointer by subtracting the current procedure's stack frame size.

The Assembler requires that you follow programming conventions to generate unwind descriptors. The beginning and end of each procedure must be noted with the `.PROC` and `.PROCEND` directives. The `.CALLINFO` directive supplies additional information about the procedure, including the stack frame size. With this information, the Assembler creates the unwind descriptor. It can also generate the standard entry and exit code to create and destroy the stack frame, save and restore the return link (if necessary), and save and restore any necessary registers. These code sequences are generated at the points indicated by the `.ENTER` and `.LEAVE` directives.

Arguments to procedures are loaded into general registers 26, 25, 24, and 23; these registers are named, respectively, `%arg0`, `%arg1`, `%arg2`, and `%arg3`. If more than four words of arguments are required, the remaining arguments are stored in the caller's stack frame in the variable argument list. The return value should be returned in general register 28, called `%ret0`. General register 29, called `%ret1`, is used for the low-order bits of a double-word return value, while `%ret0` contains the high order bits. In addition to the argument and return registers, the procedure can use registers 19 through 22 and registers 1 and 31 as scratch registers. Any other registers must be saved before use at entry and restored before exit.

Chapter 3 contains detailed descriptions of the Assembler directives described above. For a more thorough discussion of the procedure calling conventions, refer to the *Procedure Calling Conventions Manual.*

In order for an assembly language procedure to be callable from another language or another assembly language module, the name of the procedure must be *exported.* The `.EXPORT` directive does this. It also allows you to declare the *symbol type.* For procedure entry points, the symbol type should be `ENTRY`.

The Assembler and linker treat all symbols as case sensitive, while some compilers do not. By convention, compilers that are case insensitive uniformly convert all exported names to lower case. For example, it is possible to declare a procedure that cannot conflict with Pascal procedure names by using upper case letters. However, there is an *aliasing* mechanism in some compilers that allows you to declare a case-sensitive name for external use. See the appropriate language reference manual for more information.

Conversely, the .IMPORT directive allows you to reference a procedure name that is exported from another module, either from the Assembler or the compiler. Once a procedure name has been imported, it can be referenced exactly as if it were declared in the same module.

Data symbols can be exported and imported just like procedure names. However, not all compilers export the names of global variables, or provide a mechanism to reference data symbols exported from an assembly language module. For example, the HP Pascal/HP-UX compiler does not normally do this, while the C/HP-UX compiler does. FORTRAN 77/HP-UX named common blocks are exported, but the names of the variables within the common blocks are not.

It was mentioned before that data is allocated beginning from a virtual space offset 0x40000000. For convenience as well as compatibility with future releases of HP-UX systems, all data in the $PRIVATE$ space must be accessed relative to general register 27, called %dp. Standard run-time startup code, from the file /lib/crt0.o, must be linked with every program. This startup code declares a global symbol called $global$ in the $GLOBAL$ subspace. This code also loads the address of this symbol into the %dp register before beginning program execution. This register must not be changed during the execution of a program. Since the %dp register is known to contain the address of $global$, the following single instruction does the load as long as the displacement from $global$ to the desired location is less than 8 kilobytes:

```
LDW     var-$global$(%dp),%r3
```

If the desired location is not known to be close enough to $global$, the following sequence must be used:

```
ADDIL   L%var-$global$,%dp          ;result in r1
LDW     R%var-$global$(%r1),%r3
```

To access items in the $PRIVATE$ space (global data), the following does not work:

```
LDIL    L%var,%r1                   ;wrong
LDW     R%var(%r1),%r3              ;wrong
```

This assumes that the operating system always allocates data at the same virtual space offset 0x40000000.

Uninitialized areas in the data space can be requested with the .COMM (common) request. By convention, these requests should always be made in the BSS subspace in the $PRIVATE$ space. The BSS should not be used for anything else. Common requests are passed on to the linker, which matches up all requests with the same name and allocates a block of storage equal in size to the largest request. If, however, an exported data symbol is found with the same name, the linker treats the common requests as if they were imports. FORTRAN 77/HP-UX common blocks are naturally allocated in this way: if a BLOCK DATA subprogram initializes the common block, all common requests are linked to that initialized block. Otherwise, the linker allocates enough storage in BSS for the common block. The C/HP-UX compiler also allocates uninitialized global variables this way. In C, however, each uninitialized global is a separate common request.

System Calls

The HP-UX operating system defines a large set of system calls. Refer to the *HP-UX Reference* manual for more information. These system calls can be made indirectly by calling the interface routines in the C run-time library, or they can be made directly from assembly code. All system calls are funneled through a single entry point in the system space, which is identified by space register 7. Each system call is assigned a unique number, which must be loaded into general register 22. The arguments to the system call should be loaded into general registers 26, 25, 24, and 23, as necessary. When the system call returns, a status code is returned in register 22. If the status code is zero, the system call succeeded and the return value, if any, is in register 28. If the status code is nonzero, the system call failed and the error number is found in register 28. A list of the system call numbers as well as the location of the system call entry point is in the standard include file `/usr/include/sys/syscall.h`.

The following example of a code fragment shows a call to the *read* system call:

```
OR      %r0,%r0,%arg0                   ;file descriptor = 0
ADDIL   L%buf-$global$,%dp
LDO     R%buf-$global$(%r1),%arg1       ;buffer address
LDO     10,%arg2                        ;length = 10
LDIL    L%0xC0000004,%r1
BLE     R%0xC0000004(%sr7,%r1)          ;system call entry point
LDO     3,%r22                          ;read system call = 3
```

In the above code, the last instruction loads the constant 3 into register 22, and executes in the delay slot of the BLE instruction.

Assembly Listing

The Assembler's command line option, -l, causes an assembly listing to the standard output. For each line of source code, the listing provides the line number, the subspace offset, the hexadecimal representation of the assembled code (possibly flagged with an asterisk (*) to indicate address relocation), the source text, and any comments.

Following is a line of assembly language as it appears in the source file:

```
        SAVE        LDO        VAL(%r0),%r20        ;retain value
```

The above line would appear in the assembly listing as follows:

```
line no.   offset     hex representation  label opcode  operands        comment

16         0000004c   (341400A)           SAVE  LDO     VAL(%r0),%r20   ;retain value
```

The choice of line number 16 is arbitrary here. At the end of the assembly listing, a symbol table is printed showing the name and value of each symbol in the file. A type field for each symbol, indicating either absolute or relocatable, is included.

Certain types of source lines generate multiple instructions. Macro calls usually expand to several instructions. The .ENTER and .LEAVE directives each generate more than one HP Precision Architecture instruction. The predefined subspace directives, such as .CODE and .DATA, result in a space and a subspace declaration. Procedures in the $CODE$ subspace generate stack unwind descriptors in the $UNWIND$ subspace.

You have the choice of listing a section of assembled code in either the compressed or expanded form. The placement of the .LISTON and .LISTOFF directives determines which code will be expanded during listing. The directive .LISTON tells the Assembler to expand the listing of all subsequent source lines until a .LISTOFF directive is encountered. .LISTOFF stays in effect until the occurrence of a .LISTON directive. The default is .LISTOFF.

The directives .LISTON and .LISTOFF may be placed anywhere in the source text and always go into effect immediately. .LISTON and .LISTOFF may be used as often as desired.

Chapter 3
Assembler Directives and Pseudo-Operations

A set of Assembler directives allow you to take special programming actions during the assembly process. These Assembler directives begin with a period (.) to distinguish them from machine instruction opcodes or extended opcodes.

Table 3-1 lists the Assembler directives described in this chapter. These directives include those that establish the procedure calling convention, declare common, and define spaces and subspaces. Table 3-2 lists those directives that are compiler generated and, therefore, are not used by assembly language programmers. Table 3-3 lists the pseudo-operations that reserve and initialize data areas and generate entry and exit code.

This chapter also includes Table 3-4 under "Programming Aids" which lists the predefined directives for establishing standard spaces and subspaces.

Table 3-1. Assembler Directives

Directive	Function
.ALIGN	Forces location counter to the next larger multiple of the supplied alignment value.
.CALL	Specifies that the next statement is a procedure call.
.CALLINFO	Provides information for generating Entry/Exit code sequences and for creating stack unwind descriptors.
.COMM	Requests common storage for a specified number of bytes.
.COPYRIGHT	Inserts the specified string into the object module as a copyright notice.
.DOUBLE	Initializes a double-word to a floating-point value.
.END	Terminates an Assembly language program.
.ENDM	Marks the end cf a macro definition.
.ENTER	Marks a procedure's entry point and generates standard entry code.

(Continued on next page)

Table 3-1. Assembler Directives (Continued)

Directive	Function
.EQU	Assigns an expression to an identifier.
.EXPORT	Makes a specified symbol available to other modules.
.FLOAT	Initializes a double-word of storage to a floating-point value.
.IMPORT	Specifies that the definition of the given symbol occurs in another module.
.LABEL	Permits a label definition to appear within a sequence of directives that occur on a single line.
.LEAVE	Marks a procedure's exit point and generates standard exit code.
.LISTOFF	Controls listing of expanded Assembler instructions.
.LISTON	Controls listing of expanded Assembler instructions.
.LOCCT	Selects a location counter.
.MACRO	Marks the beginning of macro definitions.
.ORIGIN	Advances the location counter to a relative location from the beginning of the current subspace.
.PROC	Marks the first statement in a procedure.
.PROCEND	Marks the last statement in a procedure.
.REG	Attaches a type and number to a user-defined register name.
.SPACE	Declares a new space or switches back to a previous space.
.SPNUM	Reserves and initializes a word of storage.
.SUBSPA	Declares a new subspace or switches back to a previous subspace.
.VERSION	Inserts the specified string into the current object module as a user-defined version identification string.

Table 3-2. Compiler Generated Directives

Directive	Function
.ENTRY	Marks the entry point of the current procedure.
.EXIT	Marks the return point of the current procedure.

Table 3-3. Pseudo-Operations

Directive	Function
.BLOCK and .BLOCKZ	Reserves a block of data storage.
.BYTE	Reserves 8 bits (byte) of storage and initializes it to the given value.
.HALF	Reserves 16 bits (half word) of storage and initializes it to the given value.
.STRING and .STRINGZ	Reserves the appropriate amount of storage and initializes it to the given string.
.WORD	Reserves 32 bits (a word) of storage and initializes it to the given value.

Assembler Directives

The remainder of this chapter lists the Assembler directives and pseudo-operations in alphabetical order.

NOTE

The similar pseudo-operations, .BYTE, .HALF, and .WORD, are grouped together under "Byte". The .EXPORT and .IMPORT directives are also treated as one. Several of the descriptions include sample assembly code sequences. You can enter these short code sequences, assemble them using the -l option then inspect the offsets and field values to see how that particular directive controls the assembly environment.

The .ALIGN Directive

The .ALIGN directive advances the current location counter to the next specified "boundary."

Syntax

```
.ALIGN  [boundary]
```

Parameters

boundary — An integer value for the byte boundary to which you want to advance the location counter. The Assembler advances the location counter to that boundary. Permissible values must be a power of 2 and can range from one to 2048. The default value is 8 (doubleword aligned).

Example

```
                .CODE
                ADDIL L'$WORDMARK$-$global$,%dp
                B page
                NOP
                .ALIGN 2048
page
                ADDI    1,%r1,%r1
                .DATA
$WORDMARK$
                .WORD   0x0FFF
                .IMPORT $global$,DATA
```

This sample program adds a 21 bit field to the data pointer. Then a branch is taken to the label page that has been page aligned.

The .BLOCK and .BLOCKZ Pseudo-Operations

The .BLOCK and .BLOCKZ pseudo-operations reserve a block of storage.

Syntax

```
.BLOCK[Z]   [num_bytes]
```

Parameters

num_bytes — An integer value for the number of bytes you want to reserve. Permissible values range from zero to 0x7FFFFFFF, although the Assembler uses a default value of zero if you omit specifying a parameter.

Discussion

The .BLOCK pseudo-operation reserves a data storage area but does not perform any initialization. The .BLOCKZ pseudo-operation reserves a block of storage and initializes it to zero.

When you label a .BLOCK pseudo-operation, the label refers to the first byte of the storage area.

NOTE

Under the present implementation of the Assembler, the .BLOCK pseudo-operation also initializes the reserved area to zero.

Example

```
            .SPACE $TEXT$
            .SUBSPA $CODE$
            .BLOCK 64
swap        LDW 0(2),1
            STW 1,4(2)
            .END


            .DATA
word0       .BLOCK      0X20
word8       .WORD       0XFFFF
```

The first example requests the Assembler to reserve 64 bytes of memory in the $CODE$ subspace. This area is then followed by a "Load Word" and "Store Word" instruction. The second example reserves 32 bytes of memory in the $DATA$ subspace followed by one word intended as an end marker.

The .BYTE, .HALF, and .WORD Pseudo-Operations

The .BYTE, .HALF, and .WORD pseudo-operations reserve storage and initialize it to the given value.

Syntax

```
{ .BYTE }
{ .HALF } [init_value] [,init_value]...
{ .WORD }
```

Parameters

init_value	Either a decimal, octal, or hexadecimal number or a sequence of ASCII characters, surrounded by quotation marks. If you omit the initializing value, the Assembler initializes the area to zero.

Discussion

The .BYTE pseudo-operation requests 8 bits of storage; the .HALF pseudo-operation requests 16 bits of storage; and the .WORD pseudo-operation requests 32 bits of storage. If the location counter is not properly aligned on a boundary for a data item of that size, the Assembler advances the location counter to the next multiple of that item's size before reserving the area.

When you label one of these pseudo-operations, the label refers to the first byte of the storage area. Operands separated by commas initialize successive units of storage.

Example

```
E    .BYTE    "["
F    .WORD    -32
     .WORD    0X6eff1234
```

The first pseudo-operation allocates a byte labeled "E" and initializes it to the character "[". The next pseudo-operation advances the current subspace's location counter to a word boundary, allocates a word of storage labeled "F" and initializes that word to negative 32 (2's complement). The last pseudo-operation initializes a word of storage to the hexadecimal number 6EFF1234.

The .CALL Directive

The .CALL directive marks the next branch statement as a procedure call, and permits you to describe the location of arguments and the function return result.

Syntax

```
.CALL [argument_description]
```

Parameters

argument_description Allows you to communicate to the linker the types of registers used to pass floating point arguments and receive floating point return results in the succeeding procedure call. Similarly, this information can be communicated in the .EXPORT directive.

The linker requires this information because the Procedure Calling Convention allows floating point arguments and return values to reside in either general registers or floating point registers, depending on source language convention. At link time, the linker ensures that both the caller and called procedure agree on argument location. If not, the linker may insert code to relocate the arguments (or return result) before control is transferred to the called procedure or a procedure return is completed.

Up to 5 *argument-descriptions* may be present in the .CALL directive; one for each of the four arguments that may be passed in registers (arg0-arg3), and one for a return value (ret0).

The form of the *argument-description* is:

```
ARG  = location
```

where ARG may be:

ARGW0	The first word in the argument list.
ARGW1	The second word in the argument list.
ARGW2	The third word in the argument list.
ARGW3	The fourth word in the argument list.
RTNVAL	The return value for a procedure.

and location may be:

NO	The argument word cannot be relocated. This should be used for all non-floating point arguments; it is the default assumed when an *argument-description* is omitted.
GR	The argument word occurs in a general register.
FR	The argument word occurs in a floating point register.
FU	The argument word occurs in the upper half of a floating point register.

Example

```
;  This program calls printf() with four arguments
;  whose register locations are described in the .CALL directive.
;  The format string goes into arg0, not to be relocated.
;  The string "message" goes into arg1, specified as a general register.
;  The floating-point value 57005.57005 goes into farg2,
;  specified as a floating-point register.
;  The hexadecimal number 0xf00d goes into arg3,
;  specified as a general register.
;  The return value from printf() is not to be relocated.

          .LIT
          .ALIGN  8
          .WORD   1197387154          ; floating-point literal
          .BLOCKZ 12
fp2       .WORD   0
          .CODE
main
          .PROC
          .CALLINFO CALLER,FRAME=24,SAVE_RP
          .ENTER
          LDIL    L'fp2,%r1
          LDO     R'fp2(1),%r31       ; r31 < - floating-point literal address
          FLDWS   -16(0,%r31),%fr4
          LDO     -64(%sp),%r19
          FSTWS   %fr4,0(0,%r19)
          ADDIL   L'61453,0
          LDO     R'61453(%r1),%r20
          STW     %r20,-68(0,%sp)     ; end of stacking floating-point address
          ADDIL   L'string_area-$global$,%dp
          LDO     R'string_area-$global$(%r1),%r21  ; point to "message"
          STW     %r21,-60(0,%sp)     ; stack "message" address
          LDO     -64(%sp),%r22
          FLDWS   0(0,%r22),%fr5
          FCNVFF,SGL,DBL    %fr5,%fr6    ; convert floating-point value
          ADDIL   L'string_area-$global$+8,%dp
          LDO     R'string_area-$global$+8(%r1),%arg0 ;point to format string
          LDW     -60(0,%sp),%arg1    ; load "message" argument
          FSTDS   38,-16(0,%sp)
          FLDWS   -12(0,%sp),%fr6     ; load floating-point argument
          LDWS    -16(0,%sp),%arg3    ; load hexadecimal argument
          LDW     -68(0,%sp),%r1
          STW     %r1,-52(0,%sp)
          .CALL   argw0=no,argw1=no,argw2=fr,argw3=no,rtnval=no
          BL      printf,2
          NOP
          .LEAVE
          .PROCEND
          .EXPORT main,ENTRY
          .IMPORT printf,CODE

          .DATA
string_area
```

```
.ALIGN  8
.STRINGZ          "message"
.STRINGZ          "args = %s,%f,%x\n"
.IMPORT $global$,DATA
```

This example shows the use of the .CALL directive.

The .CALLINFO Directive

.CALLINFO is a required directive that describes the environment of the current procedure. The information it provides is available to the .ENTER and .LEAVE pseudo-operations to control the entry and exit code sequences they generate. Additional information is used by the Assembler to direct the creation of stack unwind descriptors.

Syntax

```
.CALLINFO  [FRAME=number]
           [,NO_UNWIND]  [,SAVE_SP]  [,SAVE_RP]
           [,ENTRY_GR=number]
           [,ENTRY_FR=number]
           [,ENTRY_SR=number]  [,CALLER | CALLS]  [,NO_CALLS]
           [,HPUX_INT]
```

NOTE

The first parameter in the syntax example is not preceded by a comma, but the following parameters are preceded by commas. This example uses FRAME as the first parameter which is an arbitrary choice.

Parameters

FRAME=*number*

Defines the combined size (in bytes) of the local variable area and variable argument area needed by the procedure. The .ENTER pseudo-operation allocates the desired space for local variables below the frame marker and the .LEAVE pseudo-operation deallocates that space.

The *number* parameter must be a multiple of eight bytes. If a .CALLINFO directive lacks this parameter, the Assembler assumes a default frame size of zero.

The stack frame includes space for local variables and the variable argument area. The size specified for the frame should not include space for the stack frame marker or the fixed argument area. Allocation of these areas is controlled by the CALLER and NO_CALLS parameters. The inclusion of the CALLER parameter always allocates space for the stack frame marker and the fixed argument area. (See Figure 3-1.)

A frame marker is required if the assembly routine calls another routine.

Because the frame marker contains 32 bytes and the fixed argument list contains 16 bytes, the frame area is offset from the Stack Pointer by 48 bytes if both of these areas are present. However, the Assembler does not allocate space for the frame marker and fixed argument list if the procedure does not call any other routines (see the NO_CALLS parameter).

When the total frame size for a procedure exceeds 8K bytes, the Assembler uses gr3 to locate the previous frame marker when it encounters an .ENTER or .LEAVE pseudo-operation. Under these circumstances, changing the value of gr3 can cause serious consequences.

NO_UNWIND

This is to be used only in the context of *stand alone code* or any procedure that does not need to be reliably *unwound*.

SAVE_SP

Specifies that the current routine saves the value of Previous_SP in its frame marker at SP-4. Because the Assembler does not automatically save the Stack Pointer when it generates Entry/Exit code sequences, you must explicitly save this value in your program when using this key word. (You can obtain the Previous_SP value from pseudo-register number 64.)

Programming languages, such as Pascal, typically use this value for up-level display pointers to reference local variables.

SAVE_RP

Specifies that the frame marker of the previous routine stores the value of the Return Pointer (RP). The Assembler automatically saves the Return Pointer when it encounters an .ENTER pseudo-operation, and it restores the RP value when it encounters a .LEAVE pseudo-operation. Generally, any procedure that calls other routines should save the RP value.

ENTRY_GR=*number*

Specifies the high end boundary of the Entry/Save register partition. The partition may extend over registers gr3 through gr18. If you omit this parameter, none of the registers are saved.

When a procedure uses these registers, the Assembler saves their values when it encounters an .ENTER pseudo-operation and restores these values when it encounters a .LEAVE pseudo-operation. The called routine saves these registers upon entry and restores them upon exit, so values in Entry/Save registers are preserved across a procedure call.

NOTE

See the previous description of the FRAME parameter regarding the use of gr3.

ENTRY_FR=*number*

Specifies the high end boundary of the Entry/Save floating-point register partition. The partition includes fr12 through fr15. The Assembler automatically saves these registers when it encounters an .ENTER pseudo-operation and restores them when it encounters a .LEAVE pseudo-operation.

ENTRY_SR=*number*

Specifies the high end boundary of the space register partition. The

partition currently contains only sr3. When the .CALLINFO directive includes this parameter, the Assembler automatically saves the Space Register when it encounters an .ENTER pseudo-operation and restores this register when it encounters a .LEAVE pseudo-operation.

CALLER
or
CALLS

Indicates that this procedure calls other routines so it requires space in the stack for a frame marker and a fixed argument list. (When a program is assembled using the -f option, this becomes the default case.) The Assembler allocates this space (48 bytes) when it encounters an .ENTER pseudo-operation and deallocates this space when it encounters a .LEAVE pseudo-operation.

The frame marker and fixed argument list area occur at the top of the stack so you must take this space into account when locating local variables on the stack. You must allocate an area (using FRAME=) for a variable argument list when this area is needed.

CALLER does not imply the existence of the parameter SAVE_RP.

The CALLER and CALLS parameters are equivalent.

NO_CALLS

Indicates that the procedure does not call other procedures and, therefore, does not require a frame marker on the stack. This is the default case unless the program is assembled using the -f option.

HPUX_INT

Specifies that this procedure is an interrupt procedure. This is necessary for the stack unwind mechanism.

A stack frame consists of a pointer to the top of the frame, a frame marker, a fixed argument list, and a variable argument list. Figure 3-1 illustrates these areas as an inverted stack.

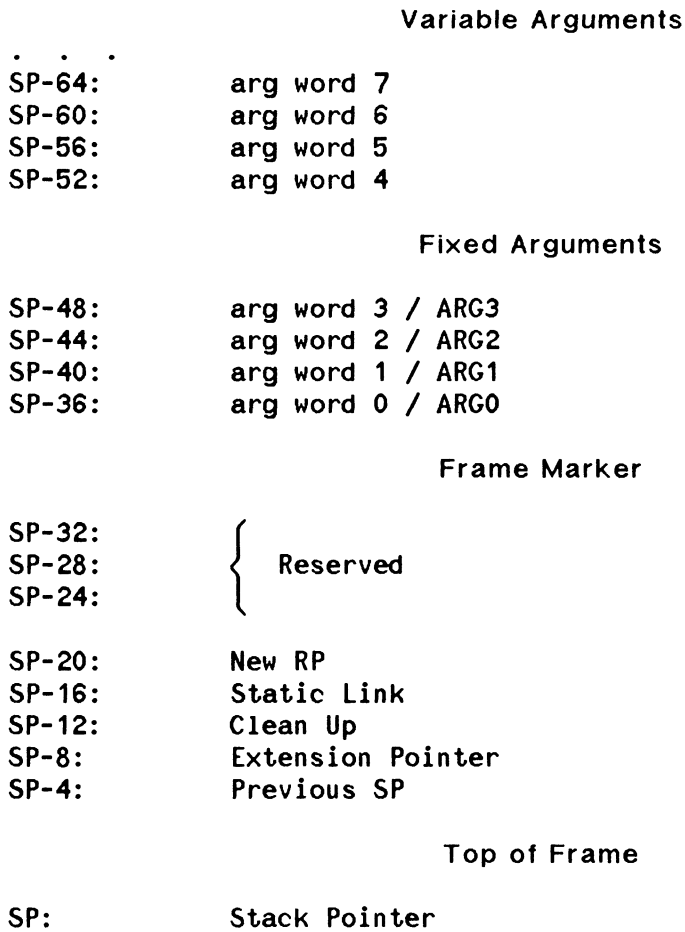

Figure 3-1. Stack Frame

Discussion

When a program uses the .CALLINFO directive, all entry and exit code must follow the Procedure Calling Convention and the Assembler automatically generates the necessary code. The parameters in the .CALLINFO directive govern the generation of the Entry/Exit code sequence (except for SAVE_SP).

Example

```
        .CODE                           ; declare space and subspace
main
        .PROC                           ; delimit procedure entry
        .CALLINFO CALLER,FRAME=0,SAVE_RP    ; no local variables, need return
        .ENTER                          ; insert entry code sequence
        ADDIL  L'stringinit-$global$,27    ; point to data to be printed
        LDO    R'stringinit-$global$(1),26 ; place argument to printf
        .CALL                           ; set up for procedure call
        BL     printf,2                 ; call printf, remembering from where
        NOP
        .LEAVE                          ; insert exit code sequence
        .PROCEND                        ; delimit procedure end

        .DATA                           ; declare space and subspace
stringinit                              ; mark use of global data subspace
        .STRINGZ      "hello world\n"   ; declare some data
        .IMPORT  $global$,DATA          ; get data reference point
        .CODE                           ; re-enter code subspace
        .EXPORT main,ENTRY              ; make routine known to linker
        .IMPORT printf,CODE             ; external procedure declaration
        .END
```

This example uses the C printf routine. It illustrates most of the directives to be used when assembly language programmers follow the standard procedure calling convention.

The .COMM Directive

The .COMM directive makes a storage request for a specified number of bytes.

Syntax

```
label   .COMM   [num_bytes]
```

Parameters

label	Labels the location of the reserved storage.
num_bytes	An integer value for the number of bytes you want to reserve. The Assembler uses a default value of 4 if the .COMM directive lacks a *num_bytes* parameter. Permissible values range from one to 0x7FFFFFFF.

Discussion

The .COMM directive declares a block of storage that may be thought of as a *common block*. You must label every .COMM directive. The linker associates the *label* with the subspace in which the .COMM directive is declared and allocates the necessary storage within that subspace. It is recommended that .COMM appear only in the BSS subspace of the $PRIVATE$ space. If the *label* of a .COMM directive appears in several object modules, the linker uses the maximum size specified in any module when it allocates the necessary storage in the current subspace.

Example

```
            .BSS
mydata      .COMM 16
```

This example reserves 16 bytes of storage for mydata.

The .COPYRIGHT Directive

The .COPYRIGHT directive inserts a company name and date into the object module as a copyright notice.

Syntax

```
.COPYRIGHT  "company name[, date]"
```

Parameters

company name, date — A sequence of ASCII characters, surrounded by quotation marks. The string can contain up to 256 characters. When a comma follows the company name, the next text is expected to be the date. The default date is 1985.

Example

```
            .COPYRIGHT "company name, date"
            .CODE
            .EXPORT main,ENTRY
main
            .PROC
            .CALLINFO
            .ENTER
            LDI     2,%r5
            ADDI    2,%r5,%r6
            .LEAVE
            .PROCEND
```

This program places a copyright notice in the object file. Once the copyright notice is in the object file, the HP-UX utility, *strings*, is used to access it.

NOTE

This directive can appear anywhere in the source file, but may appear only once.

The following is the standard copyright message placed in the copyright header of the object file:

> Copyright *company name, date*. All rights reserved. No part of this program may be photocopied, reproduced, or transmitted without prior written consent of *company name*.

The .DOUBLE Directive

The .DOUBLE directive initializes a double-word to a floating-point value calculated from the parameters provided. If the location counter is not aligned on a word double-word boundary, it is forced to the next multiple of eight. If the statement is labeled, the label refers to the first byte of the storage area.

Syntax

```
.DOUBLE  integer [ .'decimal][ E'[ -']power]
```

Parameters

integer	Specifies the whole number part of a decimal number.
decimal	Specifies the fractional part of a decimal number.
power	Specifies the power of ten to raise a decimal number. To raise the decimal number to a negative power of ten, place a minus sign (-) directly in front of the power specified.

Discussion

Each of the following examples initializes two words of memory to floating-point quantities: 0.00106 and 400000.0 respectively.

Example

```
dec_val1  .DOUBLE 10.6E-4

dec_val2  .DOUBLE 0.4E6
```

The .END Directive

The .END directive terminates an assembly language program.

Syntax

```
.END
```

Discussion

This directive is the last statement in an assembly language program. If a source file lacks an .END directive, the Assembler terminates the program when it encounters the end of the file.

Example

```
            .CODE
            .EXPORT double,ENTRY
            .PROC
double
            .CALLINFO
            .ENTER
            ADD     %arg0,%arg0,%ret0
            .LEAVE
            .PROCEND
            .END
```

A file that omitted the last line of this sample program would produce identical results.

The .ENDM directive

The .ENDM directive marks the end of a macro definition. The macro definition is entered into the macro table and the remaining source lines are read in and assembled. An .ENDM directive must always accompany a .MACRO directive.

Syntax

```
.ENDM
```

Example

```
QUADL   .MACRO  WD1,WD2,WD3,WD4
        .ALIGN  16
        .WORD   WD1
        .ALIGN  16
        .WORD   WD2
        .ALIGN  16
        .WORD   WD3
        .ALIGN  16
        .WORD   WD4
        .ENDM
```

This example defines the macro QUADL; it aligns the data specified in the macro parameters on quad word boundaries.

The .ENDM directive delimits the end of the definition of QUADL.

The .ENTER and .LEAVE Pseudo-Operations

The .ENTER and .LEAVE pseudo-operations mark a procedure's entry and exit points. They instruct the Assembler to generate procedure entry and exit code sequences based on the information provided in the .CALLINFO directive.

Syntax

```
.ENTER

.LEAVE
```

Discussion

The .ENTER pseudo-operation marks an entry point for the current procedure. Every procedure following the standard procedure calling convention must contain one .ENTER pseudo-operation. The .LEAVE pseudo-operation marks a procedure's exit point. Every procedure following the standard procedure calling convention must contain one .LEAVE pseudo-operation.

When the Assembler encounters an .ENTER pseudo-operation, it generates an entry code sequence according to the parameters in the .CALLINFO directive for that procedure. Similarly, when the Assembler encounters a .LEAVE pseudo-operation, it generates an exit code sequence according to the parameters in the .CALLINFO directive for that procedure.

Example

```
        .SPACE $TEXT$
        .SUBSPA $CODE$
    entrypt
        .PROC
        .CALLINFO
        .ENTER
        SH1ADD      %arg0,%arg1,%ret0
        .LEAVE
        .PROCEND
        .EXPORT entrypt,ENTRY
        .END
```

This example shows the placement of the .ENTER and .LEAVE pseudo-operations.

The .ENTRY and .EXIT Directives

.ENTRY and .EXIT are compiler generated directives that mark the entry point and return point of the current procedure.

Syntax

```
.ENTRY

.EXIT
```

Discussion

The .ENTRY directive signifies that the next statement is the beginning of an entry point for the current procedure. The .EXIT directive signifies that the next statement initiates a return from the current procedure. These directives are issued by compilers and are not used by assembly language programmers.

Example

```
        .ENTRY                                  ; proc entry code follows
        STW     2,-20(0,30)                     ; stack the return pointer
        LDO     48(30),30                       ; set up user stack pointer
        ADDIL   L'$THISMODULE$-$global$,27      ; point to printf data
        .CALL                                   ; set up for printf call
        BL      printf,2                        ; call printf thru RP
        LDO     R'$THISMODULE$-$global$(1),26   ; insert argument to printf
L$exit1                                         ; hide from linker
        LDW     -68(0,30),2                     ; get callee RP
        BV      0(2)                            ; exit thru RP
        .EXIT                                   ; end of exit sequence
```

This example shows a sequence of compiler-generated assembly code.

The .EQU Directive

The .EQU directive assigns an expression value to an identifier.

Syntax

```
symbolic_name  .EQU  value
```

Parameters

symbolic_name — Names the identifier to which the Assembler assigns the expression.

value — An integer expression. The Assembler evaluates the expression, which must be absolute, and assigns this value to *symbolic_name*. If the expression references other identifiers, each identifier must be defined before the .EQU directive attempts to evaluate the expression.

NOTE

The Assembler prohibits the use of offset values (instruction labels) and imported symbols as components of an expression.

Example

```
loc1 .EQU  0
loc2 .EQU  loc1+4
     .SPACE $TEXT$
     .SUBSPA $CODE$
     LDW   loc1,%r1
     STW   %r1,loc2
     .END
```

This is a valid assembly program because the definition of loc1 comes before the definition of loc2. Reversing the first two statements, however, produces an error condition.

The .EXPORT and .IMPORT Directives

The .EXPORT and .IMPORT directives allow symbols to be defined in one program but used in other programs.

Syntax

```
.EXPORT  symbol [,type] [,argument-description]
   or
.IMPORT  symbol [,type]
```

Parameters

symbol — The name of an identifier whose definition is being exported or imported.

type — A linker symbol type that can take one of the following values:

ABSOLUTE	Designates an absolute symbol.
DATA	Designates a data symbol.
CODE	Designates a code location. The location can not be a procedure entry.
ENTRY	Designates the entry point of a procedure.
MILLICODE	Locates code for the entry point of a millicode subroutine.
PLABEL	Locates a pointer to a procedure.
PRI_PROG	Designates the primary program entry point. The outerblock of Pascal and the main program in FORTRAN are type PRI_PROG.
SEC_PROG	Designates a secondary program entry point.

argument-description Allows you to communicate to the linker the types of registers used to receive floating point arguments and return floating point return results. Similarly, this information can be communicated in the .CALL directive.

The linker requires this information since the Procedure Calling Convention allows floating point arguments and return values to reside in either general registers or floating point registers depending on source language convention. At link time, the linker ensures that both the caller and called procedure agree on argument location. If not, the linker may insert code to relocate the arguments (or return result) before control is transferred to the called procedure or a procedure return is completed.

The form of the *argument-description* is described in the discussion of the .CALL directive. Refer to the .CALL directive in this chapter for more information.

Discussion

Both the .EXPORT and .IMPORT directives use a series of keywords to define a symbol to the linker. These keywords declare the symbol's type, and its argument relocation information if the symbol is the name of a procedure.

Because the .IMPORT directive specifies that another object module contains this symbol's formal definition, the Assembler does not associate an imported symbol with any particular subspace.

When an .IMPORT directive lacks a *type* parameter, the Assembler assigns the type of the current subspace (either CODE or DATA) to the symbol.

Example

```
.IMPORT symname,CODE
.CODE
LDIL    L'symname,%r1
BLE,n   R'symname(%sr4,%r1)
NOP
.END
```

This example imports the symbol symname, then loads the right part of symname with respect to gr1 into gr26.

The .FLOAT Directive

The .FLOAT directive initializes a double-word of storage to a floating-point value calculated from the parameters provided. If the location counter is not aligned on a word boundary, it is forced to the next multiple of four. If the statement is labeled, the label refers to the first byte of the storage area.

Syntax

```
.FLOAT  integer ['.'decimal]['E'['-']power]
```

Parameters

integer	Specifies the whole number part of a decimal number.
decimal	Specifies the fractional part of a decimal number.
power	Specifies the power of ten to raise a decimal number. To raise the decimal number to a negative power of ten, place a minus sign (-) directly in front of the power specified.

Discussion

Each of the following examples initializes one word of memory to floating-point quantities: 0.00096 and 3400000.0 respectively.

Example

```
factor1  .FLOAT  9.6E-4

factor2  .FLOAT  3.4E6
```

The .LABEL Directive

The .LABEL directive permits a label definition to appear within a sequence of instructions that occur on a single line.

Syntax

```
.LABEL  label_id
```

Parameters

label_id	Names the label identifier.

NOTE

The .LABEL directive is especially useful when using the M4 macroprocessor or the C pre-processor (cpp). You would normally use this directive in a DEFINE macro that includes multiple instructions. However, because the Assembler does not process M4 or cpp style macros, you must run programs that contain the .LABEL directive through the M4 pre-processor or the C pre-processor (cpp).

Example

```
#define Loop(xx) LDO xx(%r0),%r1 ! .LABEL Loop ! ADDI,= -1,%r1,%r1 \
! BL Loop,%r0  ! NOP  ! LDI 1,%ret0 ; macro
          .CODE
step_ten
          .PROC
          .CALLINFO
          .ENTER
          Loop(10)
          .LEAVE
          .PROCEND
          .EXPORT step_ten,ENTRY
```

This example defines a CPP macro named Loop.

The .LISTOFF and .LISTON Directives

The .LISTOFF and .LISTON directives control the expansion of instructions for all macro invocations, all predefined subspace declarations, and the .ENTER and .LEAVE pseudo-operations. .LISTOFF causes the Assembler to cease listing expanded instructions until a .LISTON directive is encountered. .LISTON causes the Assembler to list expanded instructions until a .LISTOFF directive is encountered. The default is .LISTOFF.

Syntax

```
.LISTOFF
.LISTON
```

The following is an example of .LISTON in an assembly listing of a procedure containing a macro invocation.

Example

```
line offset   hexcode  label    opcode            operands (comment)
1                                .LISTON
2                                .CODE
                                 .SPACE $TEXT$,    SPNUM=0,SORT=0
                                 .SUBSPA $CODE$,   QUAD=0,ALIGN=8,ACCESS=0x2c
3                                .PROC
4                      call_DECR                   ;proc label
5                                .CALLINFO         FRAME=0,SAVE_RP
6                                .ENTER
    00000000 (6BC23FD9)          STW               2,-0x14(0,0x1E)
    00000004 (37DE0060)          LDO               0x30(0x1E),0x1E
7   00000008 (2B600000)          ADDIL             L'count-$global$,%dp
8   0000000C (683A0000)          STW               %arg0,R'count-$global$(%r1)
9                                DECR              mark,count;
                                                   macro invocation
    00000010 (2B600000)          ADDIL             L'VAL-$global$,%dp
    00000014 (48340000)          LDW               R'VAL-$global$(%r1),%r20
                       LAB
    00000018 (AE9F3FF5)          ADDIBF,=          -1,%r20,LAB
    0000001C (08000240)          NOP
10                               .LEAVE
    00000020 (4BC23F79)          LDW               -0x44(0,0x1E),2
    00000024 (E840C000)          BV                0(2)
    00000028 (37C03FA1)          LDO               -0x30(0x1E),0
11                               .PROCEND
12                               .EXPORT           call_DECR,ENTRY

13                               DATA
                                 .SPACE $PRIVATE$, SPNUM=1,SORT=16
                                 .SUBSPA $DATA$,   QUAD=1,ALIGN=8
                                                   ACCESS=0x1f
14                               .IMPORT           $global$
15  40000000 (00000000) count    .WORD             0
16                               .LISTOFF
```

In the above example, if .LISTOFF had been used, the macro invocation DECR, and the directives .CODE, .DATA, .ENTER, and .LEAVE, would not have been expanded in the assembly listing.

The .LOCCT Directive

The .LOCCT directive specifies where subsequent code should occur in one of the four location counters of the current subspace. Note that the .LOCCT directive is not permitted within a procedure.

Syntax

```
.LOCCT  [loc_number]
```

Parameters

loc_number	A location counter number of the current subspace. The permissible values are 0, 1, 2, and 3. The default is zero.

Example

```
        .CODE
        .LOCCT  0
ldval1
        LDIL    L'val1,%r19
        LDO     R'val1(%r19),%r19
        .LOCCT  1
val1    .WORD   57005
        .LOCCT  0
ldval2
        LDIL    L'val2,%r20
        LDO     R'val2(%r20),%r20
        .LOCCT  1
val2    .WORD   61453
```

This example uses two location counters to separate code from data. In the assembled code, everything under location counter 0 comes first, followed by everything under location counter 1, and so on.

The .MACRO Directive

The .MACRO directive marks the beginning of macro definitions.

Syntax

```
label .MACRO  [formal_parameter]  [,formal_parameter]...
```

Parameters

formal_parameter — Specifies a string of characters treated as a positional parameter. The *i*th actual parameter in a macro invocation is substituted for the *i*th formal parameter in the macro declaration wherever the formal parameter appears in the body of the macro definition.

Normal Assembler syntax is observed within macro definitions except text substitution is assumed for formal parameters. The following line is an example of a macro declaration:

```
DECR    .MACRO LAB,VAL
```

LAB and VAL are formal parameters. Their actual values are determined by the first and second parameters on any invocation of the macro DECR. On the macro invocation, the parameters are delimited by commas. Successive commas indicate a null parameter, causing the expanded macro to substitute null for one of its formal parameters. When the number of formal parameters exceeds the number of actual parameters, null parameters are inserted for the excess parameter positions. When the number of actual parameters exceeds the number of formal parameters, a warning is issued and the excess parameters are ignored.

Example

```
DECR    .MACRO    LAB,VAL
SETP    ADDIL     L'VAL-$global$,%dp
        LDW       R'VAL-$global$(%r1),%r20
LAB
        ADDIBF,=  -1,%r20,LAB
        NOP
        .ENDM
```

The above macro definition defines a simple counter or timer call DECR. Following is an invocation to DECR:

```
DECR LOOP,COUNT
```

LOOP and COUNT are the actual parameters that are specific to this particular invocation of the macro DECR.

During macro expansion, textual substitution for positional parameters is performed in the body of the macro definition. Substitution is performed on strings of characters that are delimited by blanks, tabs, commas, or semicolons. If the string matches one of the formal parameters, it is replaced with the corresponding actual parameter.

When a macro definition contains a label, the expanded form of the macro adds a unique suffix to the label for each instance the macro is invoked. This unique suffix prevents duplicate symbols from occurring and prevents the label from being referenced from outside the body of the macro definition. This suffix also contains a number that is used as a counter by the Assembler.

Examples

```
PRINT   .MACRO   DATA_ADDR
        ADDIL    L'DATA_ADDR,%dp
        .CALL
        BL       print,%rp
        LDO      R'DATA_ADDR(%r1),%arg0
        .ENDM
```

The above example defines the macro PRINT to call *printf*. The macro parameter DATA_ADDR is used to set up the argument to be passed to *printf*.

```
STORE   .MACRO   REG,LOC
        LDIL     L'LOC-$global$,%r1
        STW      REG,R'LOC-$global$(%r1)
        .ENDM
```

The above example defines the macro STORE. STORE places the contents of the register REG, the first macro parameter, into the memory address LOC, the second parameter.

NOTE

Although there is no upper limit on the number of parameters or arguments in a macro definition, no single macro parameter may exceed 200 characters.

Discussion

Macro definitions may appear wherever and however often as necessary within source code. Macro definitions may occur inside or outside of spaces, subspaces, and procedures.

Since the Assembler always uses the most recently encountered definition, macros may be redefined as often as desired.

NOTE

A macro may not be defined within the body of another macro definition.

Although nested macro definitions are not allowed, nested macro calls are. A nested macro call occurs when one macro is invoked within the definition of another macro. A macro may not be invoked within its own definition. Macros can only be invoked after being defined.

The .ORIGIN Directive

The .ORIGIN directive advances the location counter to the specified location.

Syntax

```
.ORIGIN  [location]
```

Parameters

location

An integer value for the offset you want to advance the location counter. Permissible values range from zero to 0x7FFFFFFF. The default value is zero. The value specified cannot be less than the current value of the location counter.

When the Assembler encounters an .ORIGIN directive, it issues a .BLOCK pseudo-operation of a size calculated to advance the location counter to the requested origin. (See the discussion of the .BLOCK pseudo-operation.)

Example

```
        .CODE
        XOR     %r21,%r22,%r23
        B  idx
        NOP
        .ORIGIN 64
idx     LDWX    %r23(0,0),%r3
       .END
```

This sample program does an exclusive OR operation and advances the location counter to 64 bytes where the label idx is located as a branch target.

The .PROC and .PROCEND Directives

The .PROC and .PROCEND directives bracket the statements within a procedure.

Syntax

```
.PROC

.PROCEND
```

Discussion

The .PROC directive signifies that the next statement is the first statement of a procedure. The .PROCEND directive signifies that the previous statement was the last statement of the procedure. Switching spaces or subspaces within a procedure is not permitted.

Every procedure must contain a .CALLINFO directive and normally contains an .ENTER and .LEAVE pseudo-operation. The only exception to the latter rule occurs in procedures that are either compiler-generated or created by programmers who are writing their own entry and exit code sequences.

NOTE

Because the .ENTER and .LEAVE pseudo-operations guarantee that the stack unwind process works correctly, you should consistently use these directives rather than writing your own entry and exit code sequences.

Example

```
        .CODE
test
        .PROC
        .CALLINFO
        .ENTER
        COMCLR,=        %arg0,%arg1,%ret0
        LDI             1,%ret0
        .LEAVE
        .PROCEND
        .EXPORT test
```

This template shows a procedure that follows the standard procedure calling convention.

The .REG Directive

The .REG directive, which must be labeled, attaches a type and number to a user-defined register name. The new register name may optionally begin with %.

Syntax

```
label .REG [typed_register]
```

Parameters

typed_register	Must either be one of the predefined Assembler registers or a previously defined user-defined register name. All predefined Assembler registers begin with %.

Example

```
shift   .REG %SAR
```

The example above defines the register `shift` with *control* register type and register number eleven. %SAR is a synonym for control register eleven, the shift amount register.

The .SPACE Directive

The .SPACE directive starts a new space or switches back to an old space.

Syntax

```
.SPACE name [,SPNUM=value] [,UNLOADABLE]
            [,NOTDEFINED] [,PRIVATE] [,SORT=<value>]
```

Parameters

name	An identifier that names the new space.
SPNUM=*value*	A space number constant that provides a specific number for the current space. Its use is currently optional and is ignored by the linker. If the first parameter of the .SPACE directive is an integer, it will be interpreted as the space number and any remaining parameters will be ignored.
UNLOADABLE	Specifies that the space resides on disk and is not loadable into main memory. Debugger data is a typical example of an unloadable space.
NOTDEFINED	Specifies that the definition for this space occurs in another object module.
PRIVATE	Specifies that other programs cannot *share* the data in this space. Enforcement of this directive depends on the operating system.
SORT=value	Provides an integer value for the sort key. The linker orders the spaces in the output object module according to this key. It is suggested that the number "8" be used for space $TEXT$ and the number "16" be used for $PRIVATE$.

Discussion

The first time the Assembler encounters a .SPACE directive with a new *name*, it uses that name to declare a new space. As this is the defining occurrence of that space, additional keywords can describe attributes for that space.

If the Assembler encounters subsequent .SPACE directives with that *name*, it continues that space. In this case, where the program is re-entering a previously defined space, the .SPACE directive can only contain the space name; other keywords to describe the space are illegal.

A space can contain from one to four discrete quadrants (See the QUAD parameter of the .SUBSPA directive.) When you divide a space into multiple quadrants, you must define all the subspaces within each quadrant as a group. If subspaces for a quadrant are defined individually, program operation is unpredictable. The Assembler, however, does not check for this condition.

Example

```
.SPACE  $TEXT$
.SUBSPA $CODE$,     QUAD=0,ALIGN=8,ACCESS=0x2c,SORT=24
   .
   .
   .
.SPACE  $PRIVATE$, 1
.SUBSPA $DATA$,     QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=24
.SUBSPA $BSS$,      QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=80, ZERO
   .
   .
   .
.SPACE  $myspace$
.SUBSPA $myspace_ADDRESS$,      ALIGN=4,ACCESS=0x2c,UNLOADABLE
```

The above example shows some of the standard "space" definitions in a typical assembly language program.

The .SPNUM Directive

The .SPNUM directive reserves a word of storage and initializes it with the space number of the space named by the operand. Only one operand is allowed and any label present is offset at the first byte of the storage just initialized.

Syntax

```
.SPNUM name
```

Parameters

name	Specifies the name of a space whose space number is used to initialize a word of storage.

Example

```
            .SPACE    $PRIVATE$,SPNUM=1    SORT=16
            .SUBSPA   $DATA$,QUAD=1,       ALIGN=8,ACCESS=0x1f   SORT=24
data_ref
            .WORD                          0xFFFF
LOG         .SPNUM                         $PRIVATE$
```

In the above example, the space number of $PRIVATE$, 1, is stored as the address of the symbol LOG by the .SPNUM directive.

NOTE

Space numbers are ignored by the linker.

The .STRING and .STRINGZ Pseudo-Operations

The .STRING pseudo-operation reserves storage for a data area and initializes it to ASCII values. The .STRINGZ pseudo-operation reserves storage the same as .STRING, but appends a zero byte to the data. This creates a C language type string. If the statement is labeled, the label refers to the first byte of the storage area.

Syntax

```
.STRING[Z]  "init_value"
```

Parameters

init_value

A sequence of ASCII characters that are surrounded by quotation marks. A string can contain up to 256 characters.

Specifies a sequence of ASCII characters enclosed in quotation marks. The quotation marks are not generated into the storage area. The HP-UX style escape sequences \0, \n, \t, \b, \r, \f, \\, and \" are recognized. In addition, the escape sequences \X or \x followed by two hexadecimal digits can be used to represent any 8-bit character (the HP-UX sequence \0 becomes \X00).

Discussion

The .STRING pseudo-operation requests the required number of bytes to store the string (where each character is stored in a byte). The .STRINGZ pseudo-operation also requests the required storage for the quoted string but then appends a zero byte for compatibility with C language strings.

When you label one of these pseudo-operations, the label refers to the first byte of the storage area.

Examples

```
G   .STRING "A STRING"
```

This pseudo-operation allocates eight bytes, the first of which is labeled "G", then initializes this area with the characters: A, "space", S, T, R, I, N, and G.

```
G   .STRINGZ  "A STRING"
```

This pseudo-operation allocates eight bytes to hold A STRING, allocates an additional byte for the appended zero, and associates the label "G" with the first byte of this storage area.

The .SUBSPA Directive

The .SUBSPA directive declares a new subspace or switches back to an old subspace.

Syntax

```
.SUBSPA name [,QUAD=value]t ,ALIGN=value]
             [,ACCESS=value] [,SORT=value]
             [,FIRST] [,COMMON] [,ZERO] [,DUP_COMM]
             [,CODE_ONLY] [,UNLOADABLE]
```

Parameters

name	An identifier that names the current subspace.
QUAD=*value*	Specifies the quadrant (0 through 3) in which the Assembler should place this subspace. The default value is zero.
FIRST	Specifies that the subspace must be allocated exactly at the end of the specified space. The default is false.
ALIGN=*value*	Specifies a value (which must be a power of 2) on which the Assembler should align the beginning of the subspace. The default value is the largest alignment requested within that subspace, or one if no alignment requests exist.
ACCESS=*value*	Specifies the 7-bit value for the access rights field in the PDIR (Physical Page Directory for virtual address mapping). Must be 0X2C for code, and 0X1F for data subspaces.
SORT=*value*	Provides an integer value for the primary sort key. The linker orders the subspaces in the output object module according to this primary key. If several subspaces share the same primary key value, the linker lists these subspaces in the order in which it processes them. It is suggested that 24 be used for both code and data subspaces.
COMMON	Specifies that this subspace is a common block. The default setting is false.
ZERO	Specifies that this subspace contains all zeros and no data appears in the output file. The default setting is false.
DUP_COMM	Specifies that the initialized data symbols within this subspace may have duplicate names. When you include this parameter, multiple occurrences of a universal data symbol can exist and the linker does not report a "Duplicate Definition" error. The default setting is false.
CODE_ONLY	Specifies that this subspace contains only code. The default setting is false.

UNLOADABLE	Specifies that this subspace is not loadable into memory. The default setting is false. Loadable subspaces must reside in loadable spaces, and unloadable subspaces must reside in unloadable spaces.

Discussion

The first time the Assembler encounters a .SUBSPA directive with a new *name*, it uses that name to declare a new subspace. As this is the defining occurrence of that subspace, optional keywords describe attributes of that subspace.

When the Assembler encounters additional .SUBSPA directives with that *name*, it continues that subspace. In this case, the .SUBSPA directive can only contain the subspace name; other keywords to describe the subspace are illegal.

The $CODE$ subspace uses the stack unwind subspace called $UNWIND$. If other code subspaces have an associated stack unwind subspace, the Assembler identifies them with names of the form: $UNWIND$ *<code_subspace_name>*. For subspaces with names of the form $CODE$<mycode>, the Assembler creates an unwind subspace with the name $UNWIND$<mycode>.

Example

```
.SPACE  $TEXT$,     0
.SUBSPA $CODE$,     QUAD=0,ALIGN=8,ACCESS=0x2c,SORT=24
.SPACE  $PRIVATE$, 1
.SUBSPA $DATA$,     QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=24
```

The above example shows some of the standard "subspace" definitions in a typical assembly language program.

The .VERSION Directive

The .VERSION directive places the designated string in the current object module for version identification.

Syntax

```
.VERSION  "info_string"
```

Parameters

info_string	A sequence of ASCII characters, surrounded by quotation marks. The string can contain up to 256 characters.

Discussion

The Assembler places this string in the current object module. A program may contain multiple .VERSION directives.

Example

```
.CODE
.VERSION "Version 1 of This Simple Sample Program"
SUB      %r19,%r20,%r19
DEP      %r19,14,5,%r22
.END
```

This program inserts version information into the object module, and performs subtract and deposit operations. Once the version information is in the object file, the HP-UX utility, *strings*, is used to access it.

NOTE

This directive can appear anywhere in the source file, and multiple occurrences are permitted.

Programming Aids

The Assembler provides a series of standard space and subspace definitions that you may use to simplify the writing of an assembly program. These definitions are duplicated in the system file *pcc_prefix.s*. Because these files are relatively large and may change with new releases of the Assembler, you can view the most recent version of these files on your terminal screen by typing the command:

```
more /lib/pcc_prefix.s.
```

Table 3-4 lists the predefined directives for establishing standard spaces and subspaces.

Table 3-4. Predefined Spaces and Subspaces

Directive	Space Name	Default Parameters
.FIRST	.space $TEXT$, .subspa $FIRST$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=2048,ACCESS=0x2c, SORT=4,FIRST
.REAL	.space $TEXT$, .subspa $REAL$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x2c, SORT=4,FIRST,LOCK
.MILLICODE	.space $TEXT$, .subspa $MILLICODE$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x2c,SORT=8
.LIT	.space $TEXT$, .subspa LIT,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x2c,SORT=16
.CODE	.space $TEXT$, .subspa $CODE$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x2c,SORT=24
.UNWIND	.space $TEXT$, .subspa $UNWIND$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=4,ACCESS=0x2c,SORT=64
.RECOVER	.space $TEXT$, .subspa $RECOVER$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=4,ACCESS=0x2c,SORT=80
.RESERVED	.space $TEXT$, .subspa $RESERVED$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x73,SORT=82
.GATE	.space $TEXT$, .subspa $GATE$,	SPNUM=0,SORT=8 QUAD=0,ALIGN=8,ACCESS=0x4c, SORT=84,CODE_ONLY

(Continued on next page)

Table 3-4. Predefined Spaces and Subspaces (Continued)

Directive	Space Name	Default Parameters
.GLOBAL	.space $PRIVATE$, .subspa $GLOBAL$, .IMPORT $global$	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=8
.SHORTDATA	.space $PRIVATE$, .subspa $SHORTDATA$,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=16
.DATA	.space $PRIVATE$, .subspa $DATA$,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=24
.PFA_COUNTER	.space $PRIVATE$, .subspa $PFA_COUNTER$,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=4,ACCESS=0x1f,SORT=64
.BSS	.space $PRIVATE$, .subspa BSS,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f, SORT=80,ZERO
.PCB	.space $PRIVATE$, .subspa PCB,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x10,SORT=82
.STACK	.space $PRIVATE$, .subspa $STACK$,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=82
.HEAP	.space $PRIVATE$, .subspa $HEAP$,	PRIVATE,SPNUM=1,SORT=16 QUAD=1,ALIGN=8,ACCESS=0x1f,SORT=82
.PFA_ADDRESS	.space PFA, .subspa $PFA_ADDRESS$,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=64 ALIGN=4,ACCESS=0x2c,UNLOADABLE
.HEADER	.space $DEBUG$, .subspa $HEADER$,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=80 ALIGN=4,ACCESS=0,UNLOADABLE,FIRST
.GNTT	.space $DEBUG$, .subspa $GNTT$,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=80 ALIGN=4,ACCESS=0,UNLOADABLE
.LNTT	.space $DEBUG$, .subspa $LNTT$,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=80 ALIGN=4,ACCESS=0,UNLOADABLE
.SLT	.space $DEBUG$, .subspa SLT,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=80 ALIGN=4,ACCESS=0,UNLOADABLE
.VT	.space $DEBUG$, .subspa VT,	SPNUM=2,PRIVATE,UNLOADABLE,SORT=80 ALIGN=4,ACCESS=0,UNLOADABLE

Chapter 4
The Instruction Set

The HP Precision Architecture instructions fall into the following major categories:

- Memory Reference
- Immediate
- Branch
- Computational
- System Control
- Assist (coprocessor)

In addition, pseudo-instructions are available to perform commonly used functions that are variations of the basic instructions.

Instruction Operands

Table 4-1 lists the instruction operands by class as well as meaning. The table is intended as a reference for the operands used in the instruction tables throughout this chapter.

Table 4-1. Instruction Operands

Operand Class	Meaning
b	base register (0 through 31)
d	14 bit displacement
i	5 or 11 bit immediate value
len	length of bit field
p	bit position indicator
count	shift count
r	source register: • general register (0 through 31) • floating point register (0 through 15) • control register (0 and 8 through 31)
r1 and r2	source register: • general register (0 through 31) • floating point register (0 through 15)
sr	space register (0 through 7)
s	space register (0 through 3)
t	destination register: • general register (0-31) • floating-point register (0-15) • control register (0 and 8-31)
wd	word displacement (12 bit immediate)
x	index register (general register 0 through 31)

Memory Reference Instructions

The memory reference instructions load values from memory into general registers and store values from general registers into memory. The displacement or index values can be used to modify the base offset in a general register.

Memory reference instructions include:

- Load and Store
- Load and Store With Base Register Modification
- Indexed Load
- Short Displacement Load and Store
- Store Bytes Short

Load and Store Instructions

A value is transferred between memory and a general register.

Table 4-2. Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Load Byte	LDB	d(s,b),t
Load Halfword	LDH	d(s,b),t
Load Word	LDW	d(s,b),t
Store Byte	STB	r,d(s,b)
Store Halfword	STH	r,d(s,b)
Store Word	STW	r,d(s,b)

Load and Store with Base Register Modification Instructions

A word is transferred between memory and a general register. The base register is pre-decremented if the displacement is negative; otherwise, the base register is post-incremented.

Table 4-3. Load and Store With Base Register Modification Instructions

Instruction Name	Mnemonic Name	Operands
Load Word and Modify	LDWM	d(s,b),t
Store Word and Modify	STWM	r,d(s,b)

Indexed Load Instructions

A value is read from memory into a general register. The address is formed by the addition of the index register to the base register. Optionally, the index value may be shifted to reflect an offset corresponding to the size of the value being read. The base register may be modified after the address has been formed.

Table 4-4. Indexed Load Instructions

Instruction Name	Mnemonic Name	Operands
Load Byte Indexed	LDBX,cmplt	x(s,b),t
Load Halfword Indexed	LDHX,cmplt	x(s,b),t
Load Word Indexed	LDWX,cmplt	x(s,b),t
Load Word Absolute Indexed *	LDWAX,cmplt	x(b),t
Load and Clear Word Indexed	LDCWX,cmplt	x(s,b),t

* This instruction may be executed only by code running at the most privileged level.

Table 4-5. Indexed Load Completers

cmplt	Description
,S	Shift Index by Data Size, No Base Register Modification
,M	No Index Shift, Base Register Modification
,S,M or ,SM	Shift Index by Data Size, Base Register Modification
none specified	No Index Shift, No Base Register Modification

Short Displacement Load and Store Instructions

A value is transferred between memory and a general register. The address is formed by adding the short displacement to the base register. A short displacement is one that is between -16 and +15 bytes. Optionally, the base register may be modified either before or after the address has been formed.

Table 4-6. Short Displacement Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Load Byte Short	LDBS,cmplt	d(s,b),t
Load Halfword Short	LDHS,cmplt	d(s,b),t
Load Word Short	LDWS,cmplt	d(s,b),t
Load Word Absolute Short *	LDWAS,cmplt	d(b),t
Load and Clear Word Short	LDCWS,cmplt	d(s,b),t
Store Byte Short	STBS,cmplt	r,d(s,b)
Store Halfword Short	STHS,cmplt	r,d(s,b)
Store Word Short	STWS,cmplt	r,d(s,b)
Store Word Absolute Short *	STWAS,cmplt	r,d(b)

* This instruction may be executed only by code running at the most privileged level.

Table 4-7. Short Displacement Load and Store Completers

cmplt	Description
,MB	Modify Before
,MA	Modify After
none specified	No Base Register Modification

Store Bytes Short Instruction

Byte values are written from a general register into memory. The address is formed using the short displacement, the base register, and the completer. The bytes can be aligned to the beginning or the end of the word. Optionally, the base register can be modified after the address has been formed.

Table 4-8. Store Bytes Short Instruction

Instruction Name	Mnemonic Name	Operands
Store Bytes Short	STBYS,cmplt	r,d(s,b)

Table 4-9. Store Bytes Short Completers

cmplt	Description
,B	Beginning case, no modify
,E	Ending case, no modify
,B,M	Beginning case, modify base
,E,M	Ending case, modify base

Immediate Instructions

An immediate value is loaded into a general register. Values are computed from either a 21-bit immediate value, a 21-bit immediate value plus a general register, or a 14-bit immediate value plus a base register.

Table 4-10. Immediate Instructions

Instruction Name	Mnemonic Name	Operands
Load Immediate Left	LDIL	i,t
Add Immediate Left *	ADDIL	i,r
Load Offset	LDO	d(b),t
Load Immediate **	LDI	i,t

* The result of the ADDIL operation is placed in general register one.

** The LDI pseudo-instruction generates an LDO i(0),t instruction.

Branch Instructions

Branch instructions can be conditional or unconditional. Unconditional branches are used to alter the control flow of a program. Conditional branches perform a function and then branch depending upon whether a specified condition has been met.

NOTE

When coding branch instructions, including those with nullification specified, attention should be given to the *following* instruction in the source code. All branch instructions consider the instruction that follows to be in its *delay slot*. An NOP pseudo-operation may be used to fill the delay slot when there is no other useful work to be performed.

Unconditional Branch Instructions

Unconditional branch instructions are used to make control transfers, procedure calls, and procedure returns. Targets for unconditional branches are either local or external. Unconditional *local* branch instructions are used for control transfers within a space (intraspace). Unconditional *external* branch instructions are used for control transfers into another space (interspace).

Table 4-11. Unconditional Branch Instructions

Instruction Name	Mnemonic Name	Operands
Branch External	BE,n	wd(sr,b)
Branch and Link External	BLE,n	wd(sr,b)
Branch and Link	BL,n	target,t
Branch and Link Register	BLR,n	x,t
Branch Vectored	BV,n	x(b)
Gateway	GATE,n	target,t
Unconditional Branch *	B,n	target

* The B pseudo-instruction generates a BL instruction with the link register t equal to GR0.

Conditional Branch Instructions

Local conditional branches include the following instructions:

- Move and Branch
- Compare and Branch
- Add and Branch
- Branch on Bit

A conditional branch is considered *taken* if the condition specified by the condition completer is met by the operands, and/or is met by the results of the function performed.

All conditional branches can be coded with a nullification completer. If nullification is specified, the instruction following either a *taken forward branch* or a *failing backward branch* is nullified. If nullification is not specified, the following instruction is executed before the branch target, especially in the case where a branch instruction occupies the delay slot. See the *Precision Architecture and Instruction Reference Manual* for the definition of "following instruction".

A forward branch is one to an address that is greater than the address of the instruction in the delay slot of the branch. A backward branch is one to an address that is less than or equal to the address of the delay slot. Figure 4-1 identifies which branches are forward branches and which branches are backward branches.

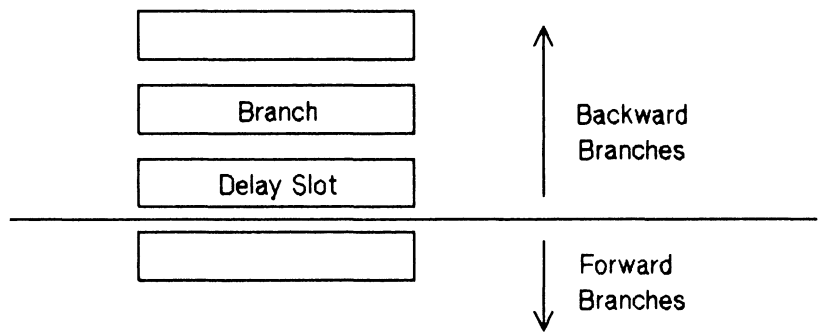

Figure 4-1. Branch Descriptions

Move and Branch Instructions

A general register or an immediate value is copied to a general register. The value copied is used to determine if the specified condition is met.

Table 4-12. Move and Branch Instructions

Instruction Name	Mnemonic Name	Operands
Move and Branch	MOVB, cond, n	r1,r2,target
Move Immediate and Branch	MOVIB, cond, n	i,r,target

Table 4-13. Move and Branch Conditions

cond	Description
	never
=	all bits are equal to 0
<	leftmost bit is equal to 1
OD	rightmost bit is equal to 1
TR	always
<>	at least one bit is equal to 1
>=	leftmost bit is equal to 0
EV	rightmost bit is equal to 0

Compare and Branch Instructions

A general register or an immediate value is compared against a general register. The operands and/or the result of the comparison are used to determine whether the specified condition is met. The COMBT, COMIBT, COMBF and COMIBF instructions use only the non-negated completer conditions (never, =, <, <=, <<, <<=, SV, OD). The COMB and COMIB pseudo-instructions use any of the condition completers.

Table 4-14. Compare and Branch Instructions

Instruction Name	Mnemonic Name	Operands
Compare and Branch If True	COMBT,cond,n	r1,r2,target
Compare Immediate and Branch If True	COMIBT,cond,n	i,r,target
Compare and Branch If False	COMBF,cond,n	r1,r2,target
Compare Immediate and Branch If False	COMIBF,cond,n	i,r,target
Compare and Branch *	COMB,cond,n	r1,r2,target
Compare Immediate and Branch **	COMIB,cond,n	i,r,target

* The COMB pseudo-instruction generates either a COMBT or COMBF instruction depending on the condition.

** The COMIB pseudo-instruction generates either a COMIBT or COMIBF instruction depending on the condition.

Table 4-15. Compare and Branch Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to opd2	
<	opd1 is less than opd2 (signed)	
<=	opd1 is less than or equal to opd2 (signed)	
<<	opd1 is less than opd2 (unsigned)	
<<=	opd1 is less than or equal to opd2 (unsigned)	
SV	opd1 minus opd2 results in overflow (signed)	
OD	result of opd1 minus opd2 is odd	
TR	always	Negated
<>	opd1 is less than or greater than opd2	
>=	opd1 is greater than or equal to opd2 (signed)	
>	opd1 is greater than opd2 (signed)	
>>=	opd1 is greater than or equal to opd2 (unsigned)	
>>	opd1 is greater than opd2 (unsigned)	
NSV	opd1 minus opd2 results in no overflow (signed)	
EV	result of opd1 minus opd2 is even	

Add and Branch Instructions

A general register or an immediate value is added to a general register. The operands and/or the *results* of the addition are used to determine whether the specified condition is met. The ADDBT, ADDIBT, ADDBF and ADDIBF instructions use only the non-negated completer conditions (never, =, <, <=, NUV, ZNV, SV, OD). The ADDB and ADDIB pseudo-instructions uses any of the condition completers.

Table 4-16. Add and Branch Instructions

Instruction Name	Mnemonic Name	Operands
Add and Branch If True	ADDBT,cond,n	r1,r2,target
Add Immediate and Branch If True	ADDIBT,cond,n	i,r,target
Add and Branch If False	ADDBF,cond,n	r1,r2,target
Add Immediate and Branch If False	ADDIBF,cond,n	i,r,target
Add and Branch *	ADDB,cond,n	r1,r2,target
Add Immediate and Branch **	ADDIB,cond,n	i,r,target

* The ADDB pseudo instruction generates either a ADDBT or ADDBF instruction, depending on the condition.

** The ADDIB pseudo-instruction generates either a ADDIBT or ADDIBF instruction, depending on the condition.

Table 4-17. Add and Branch Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to -opd2	
<	opd1 is less than -opd2 (signed)	
<=	opd1 is less than or equal to -opd2 (signed)	
NUV	opd1 + opd2 < 2^{32} (no unsigned overflow)	
ZNV	opd1 + opd2 < 2^{32} or opd1 + opd2 = 0	
SV	opd1 plus opd2 results in overflow (signed)	
OD	result of opd1 plus opd2 is odd	
TR	always	Negated
<>	opd1 is not equal to -opd2	
>=	opd1 is greater than or equal to -opd2 (signed)	
>	opd1 is greater than -opd2 (signed)	
UV	opd1 + opd2 > = 2^{32} (unsigned overflow)	
VNZ	opd1 + opd2 > 2^{32} and opd1 + opd2 not = 0	
NSV	opd1 plus opd2 results in no overflow (signed)	
EV	result of opd1 plus opd2 is even	

Branch on Bit Instructions

The bit specified, either as an immediate or in the shift-amount-register (SAR,CR11), of a general register is tested. The result of the test is used to determine whether the specified condition is met.

Table 4-18. Branch on Bit Instructions

Instruction Name	Mnemonic Name	Operands
Branch on Variable Bit	BVB,cond,n	r,target
Branch on Bit	BB,cond,n	r,p,target

Table 4-19. Branch on Bit Conditions

cond	Description
<	Bit specified is equal to 1
>=	Bit specified is equal to 0

Computational Instructions

Computational instructions are composed of the following:

- Add
- Shift and Add
- Subtract
- Compare and Clear
- Divide Step
- Logical
- Unit
- Shift
- Extract
- Deposit

The instructions in this group are organized by the type of condition that can be specified.

After the computational instructions perform a function, the operands and/or the "results" of the function being performed are used to determine whether the specified condition is met. If the condition is met, the *following* instruction is nullified.

Some of the computational instructions cause interrupt traps to occur based on overflow and/or condition detection.

Refer to the "Instruction Operands" section earlier in this chapter for a description of the instruction operands.

Add Instructions

Two general registers, or an immediate value and a general register, are added together and the result is stored in a general register. The operands and/or the *results* of the addition are used to determine whether the specified condition is met. If the specified condition is met, the following instruction is nullified, except for ADDIT and ADDITO where a trap is taken.

Table 4-20. Add Instructions

Instruction Name	Mnemonic Name	Operands
Add	ADD,cond	r1,r2,t
Add Logical	ADDL,cond	r1,r2,t
Add and Trap on Overflow	ADDO,cond	r1,r2,t
Add with Carry	ADDC,cond	r1,r2,t
Add with Carry and Trap on Overflow	ADDCO,cond	r1,r2,t
Add to Immediate and Trap on Condition	ADDIT,cond	i,r,t
Add to Immediate and Trap on Condition or Overflow	ADDITO,cond	i,r,t
Add to Immediate	ADDI,cond	i,r,t
Add to Immediate and Trap on Overflow	ADDIO,cond	i,r,t

Table 4-21. Add Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to -opd2	
<	opd1 is less than -opd2 (signed)	
<=	opd1 is less than or equal to -opd2 (signed)	
NUV	opd1 + opd2 < 2^{32} (no unsigned overflow)	
ZNV	opd1 + opd2 < 2^{32} or opd1 + opd2 = 0	
SV	opd1 plus opd2 results in overflow (signed)	
OD	result of opd1 plus opd2 is odd	
TR	always	Negated
<>	opd1 is not equal to -opd2	
>=	opd1 is greater than or equal to -opd2 (signed)	
>	opd1 is greater than -opd2 (signed)	
UV	opd1 + opd2 > = 2^{32} (unsigned overflow)	
VNZ	opd1 + opd2 > 2^{32} and opd1 + opd2 not = 0	
NSV	opd1 plus opd2 results in no overflow (signed)	
EV	result of opd1 plus opd2 is even	

Shift and Add Instructions

A general register is left-shifted and added to a general register, and the result is stored in a general register. The operands and/or the results are used to determine whether the specified condition is met. The following instruction is nullified if the specified condition is met. A signed overflow condition can be detected if any of the bits shifted out are different from the resulting left-most bit after the shift.

Table 4-22. Shift and Add Instructions

Instruction Name	Mnemonic Name	Operands
Shift One and Add	SH1ADD,cond	r1,r2,t
Shift One and Add Logical	SH1ADDL,cond	r1,r2,t
Shift One, Add and Trap on Overflow	SH1ADDO,cond	r1,r2,t
Shift Two and Add	SH2ADD,cond	r1,r2,t
Shift Two and Add Logical	SH2ADDL,cond	r1,r2,t
Shift Two, Add and Trap on Overflow	SH2ADDO,cond	r1,r2,t
Shift Three and Add	SH3ADD,cond	r1,r2,t
Shift Three and Add Logical	SH3ADDL,cond	r1,r2,t
Shift Three, Add and Trap on Overflow	SH3ADDO,cond	r1,r2,t

Table 4-23. Shift and Add Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to -opd2	
<	opd1 is less than -opd2 (signed)	
<=	opd1 is less than or equal to -opd2 (signed)	
NUV	opd1 + opd2 < 2^{32} (no unsigned overflow)	
ZNV	opd1 + opd2 < 2^{32} or opd1 + opd2 = 0	
SV	opd1 plus opd2 results in overflow (signed)	
OD	result of opd1 plus opd2 is odd	
TR	always	Negated
<>	opd1 is not equal to -opd2	
>=	opd1 is greater than or equal to -opd2 (signed)	
>	opd1 is greater than -opd2 (signed)	
UV	opd1 + opd2 >= 2^{32} (unsigned overflow)	
VNZ	opd1 + opd2 > 2^{32} and opd1 + opd2 not = 0	
NSV	opd1 plus opd2 results in no overflow (signed)	
EV	result of opd1 plus opd2 is even	

Subtract Instructions

A general register is subtracted from an immediate value or a general register and the result is stored in a general register. The operands and/or the results of the subtraction are used to determine whether the specified condition is met. If the specified condition is met, the following instruction is nullified, except for SUBT and SUBTO where a trap is taken.

Table 4-24. Subtract Instructions

Instruction Name	Mnemonic Name	Operands
Subtract	SUB,cond	r1,r2,t
Subtract and Trap on Condition	SUBT,cond	r1,r2,t
Subtract with Borrow	SUBB,cond	r1,r2,t
Subtract and Trap on Overflow	SUBO,cond	r1,r2,t
Subtract and Trap on Condition or Overflow	SUBTO,cond	r1,r2,t
Subtract with Borrow and Trap on Overflow	SUBBO,cond	r1,r2,t
Subtract from Immediate	SUBI,cond	i,r,t
Subtract from Immediate and Trap on Overflow	SUBIO,cond	i,r,t

Table 4-25. Subtract Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to opd2	
<	opd1 is less than opd2 (signed)	
<=	opd1 is less than or equal to opd2 (signed)	
<<	opd1 is less than opd2 (unsigned)	
<<=	opd1 is less than or equal to opd2 (unsigned)	
SV	opd1 minus opd2 results in overflow (signed)	
OD	result of opd1 minus opd2 is odd	
TR	always	Negated
<>	opd1 is less than or greater than opd2	
>=	opd1 is greater than or equal to opd2 (signed)	
>	opd1 is greater than opd2 (signed)	
>>=	opd1 is greater than or equal to opd2 (unsigned)	
>>	opd1 is greater than opd2 (unsigned)	
NSV	opd1 minus opd2 results in no overflow (signed)	
EV	result of opd1 minus opd2 is even	

Compare and Clear Instructions

An immediate value or a general register is compared against another general register and zero is loaded into a third general register. The operands of the comparison are used to determine whether the specified condition is met. If the specified condition is met, the following instruction is nullified.

Table 4-26. Compare and Clear Instructions

Instruction Name	Mnemonic Name	Operands
Compare and Clear	COMCLR,cond	r1,r2,t
Compare Immediate and Clear	COMICLR,cond	i,r,t

Table 4-27. Compare and Clear Conditions

cond	Description	
	never	Non-negated
=	opd1 is equal to opd2	
<	opd1 is less than opd2 (signed)	
<=	opd1 is less than or equal to opd2 (signed)	
<<	opd1 is less than opd2 (unsigned)	
<<=	opd1 is less than or equal to opd2 (unsigned)	
SV	opd1 minus opd2 results in overflow (signed)	
OD	result of opd1 minus opd2 is odd	
TR	always	Negated
<>	opd1 is less than or greater than opd2	
>=	opd1 is greater than or equal to opd2 (signed)	
>	opd1 is greater than opd2 (signed)	
>>=	opd1 is greater than or equal to opd2 (unsigned)	
>>	opd1 is greater than opd2 (unsigned)	
NSV	opd1 minus opd2 results in no overflow (signed)	
EV	result of opd1 minus opd2 is even	

Divide Step Instruction

A divide step operation is performed using two general registers; the intermediate result is stored in a general register. The operands and/or the results of the divide step operation are used to determine whether the specified condition is met. The divide step can be used with either the add or subtract conditions depending upon the stage of the operation.

Table 4-28. Divide Step Instruction

Instruction Name	Mnemonic Name	Operand
Divide Step	DS,cond	r1,r2,t

See Table 4-21 or 4-25 for the add or subtract conditions, respectively.

Logical Instructions

A logical operation is performed on two general registers and the result is stored in a general register. The result of the logical operation is used to determine whether the specified condition is met. The following instruction is nullified if the specified condition is met.

Table 4-29. Logical Instructions

Instruction Name	Mnemonic Name	Operands
And Complement	ANDCM,cond	r1,r2,t
And	AND,cond	r1,r2,t
Inclusive Or	OR,cond	r1,r2,t
Exclusive Or	XOR,cond	r1,r2,t
Copy *	COPY	r,t
No Operation **	NOP	

* The COPY pseudo-instruction generates the OR r,0,t instruction.

** The NOP pseudo-instruction generates the OR 0,0,0 instruction.

Table 4-30. Logical Conditions

cond	Description	
	never	Non-negated
=	all bits are equal to 0	
<	leftmost bit is equal to 1	
<=	leftmost bit is equal to 1, or all bits are equal to 0	
OD	rightmost bit is equal to 1	
tr	always	Negated
<>	at least one bit is equal to 1	
>=	leftmost bit is equal to 0	
>	leftmost bit is equal to 0, and at least one bit is equal to 1	
EV	rightmost bit is equal to 0	

Unit Instructions

One or two general registers are operated upon and the result is stored in a general register. The results of the operation are used to determine whether a specified condition is met. If the specified condition is met, the following instruction is nullified, except for UADDCMT where a trap is taken.

Table 4-31. Unit Instructions

Instruction Name	Mnemonic Name	Operands
Unit Exclusive Or	UXOR,cond	r1,r2,t
Unit Add Complement	UADDCM,cond	r1,r2,t
Unit Add Complement and Trap on Condition	UADDCMT,cond	r1,r2,t
Intermediate Decimal Correct	IDCOR,cond	r,t
Decimal Correct	DCOR,cond	r,t

Table 4-32. Unit Conditions

cond	Description	
	never	Non-negated
SBZ	some byte zero	
SHZ	some halfword zero	
SCD	some BCD digit carry	
SBC	some byte carry	
SHC	some halfword carry	
TR	always	Negated
NBZ	all bytes nonzero	
NHZ	all halfwords nonzero	
NDC	no BCD digit carry	
NBC	no byte carry	
NHC	no halfword carry	

Shift, Extract, and Deposit Instructions

A shift, extract, or deposit operation is performed and the result is stored in a general register. The results of the operation are used to determine whether a specified condition is met. A variable operation may be performed using the shift-amount-register (SAR, CR 11).

The shift instructions use two general registers to perform a double shift. The amount to be shifted comes either from the operand list or from the SAR.

The extract instructions isolate a field of the specified length in a general register, right shift to position the field, and store the result in a general register. The result may be stored as a sign extended value. The ending position of the field to be extracted may be specified as an operand or from the SAR.

The deposit instructions use an immediate value or a general register to isolate a field of the specified length, left shift to position the field, and merge the result into a general register. The result may be merged with the existing bits of the general register or zeros. The ending position of the result field may be specified as an operand or from the SAR.

Table 4-33. Shift, Extract, and Deposit Instructions

Instruction Name	Mnemonic Name	Operands
Variable Shift Double	VSHD,cond	r1,r2,t
Shift Double	SHD,cond	r1,r2,count,t
Variable Extract Unsigned	VEXTRU,cond	r,len,t
Variable Extract Signed	VEXTRS,cond	r,len,t
Extract Unsigned	EXTRU,cond	r,p,len,t
Extract Signed	EXTRS,cond	r,p,len,t
Variable Deposit	VDEP,cond	r,len,t
Zero and Deposit	ZDEP,cond	r,p,len,t
Deposit	DEP,cond	r,p,len,t
Zero and Variable Deposit	ZVDEP,cond	r,len,t
Zero and Variable Deposit Immediate	ZVDEPI,cond	i,len,t
Variable Deposit Immediate	VDEPI,cond	i,len,t
Zero and Deposit Immediate	ZDEPI,cond	i,p,len,t
Deposit Immediate	DEPI,cond	i,p,len,t

Table 4-34. Shift, Extract, and Deposit Conditions

cond	Description
	never
=	all bits are equal to 0
<	leftmost bit is equal to 1
OD	rightmost bit is equal to 1
TR	always
<>	at least one bit is equal to 1
>=	leftmost bit is equal to 0
EV	rightmost bit is equal to 0

System Control Instructions

System control instructions provide special register moves, system mask control, return from interruption, hash address computation, probe access rights, memory management operations, and implementation-dependent functions.

Some of the memory management instructions use an optional completer to allow the base register to be modified after the address has been formed.

Most of these instructions are executed by code that only runs at the most privileged level.

Table 4-35. System Control Completers

complt	Address Formation
,M	Base Register Modification
none specified	No Base Register Modification

Table 4-36. System Control Instructions

Instruction Name	Mnemonic Name	Operands
Break	BREAK	i1, i2
Return from Interruption	RFI	
Set System Mask	SSM	i, t
Reset System Mask	RSM	i, t
Move To System Mask	MTSM	r
Load Space Identifier	LDSID	(s, b), t
Move To Space Register	MTSP	r, sr
Move To Control Register	MTCTL	r, t
Move To Shift Amount Register *	MTSAR	r
Move From Space Register	MFSP	sr, t
Move From Control Register	MFCTL	r, t
Synchronize Caches	SYNC	
Probe Read Access	PROBER	(s, b), r, t
Probe Read Access Immediate	PROBERI	(s, b), i, t
Probe Write Access	PROBEW	(s, b), r, t
Probe Write Access Immediate	PROBEWI	(s,b), i, t
Load Physical Address	LPA, cmplt	x (s, b), t
Load Hash Address	LHA, cmplt	x (s, b), t
Purge Data Translation Lookaside Buffer	PDTLB, cmplt	x (s, b)
Purge Instruction Translation Lookaside Buffer	PITLB, cmplt	x (sr, b)
Purge Data Translation Lookaside Buffer Entry	PDTLBE, cmplt	x (s, b)

* The MTSAR pseudo-instruction generates an MTCTL r,11 instruction.

Table 4-36. System Control Instructions (Continued)

Instruction Name	Mnemonic Name	Operands
Purge Instruction Translation Lookaside Buffer Entry	PITLBE, cmplt	x (sr, b)
Insert Data Translation Lookaside Buffer Address	IDTLBA	r, (s, b)
Insert Instruction Translation Lookaside Buffer Address	IITLBA	r, (sr, b)
Insert Data Translation Lookaside Buffer Address	IDTLBP	r, (s, b)
Insert Instruction Translation Lookaside Buffer Protection	IITLBP	r, (sr, b)
Purge Data Cache	PDC, cmplt	x (s, b)
Flush Data Cache	FDC, cmplt	x (s, b)
Flush Instruction Cache	FIC, cmplt	x (sr, b)
Flush Data Cache Entry	FDCE, cmplt	x (s, b)
Flush Instruction Cache Entry	FICE, cmplt	x (sr, b)
Diagnose	DIAG	i

Assist (Coprocessor) Instructions

Coprocessor instructions are used to perform data manipulations on attached special purpose processors, while incurring minimum overhead in execution rate. Each instruction must specify a unit identifier between zero and seven to select a coprocessor. The coprocessor instructions include:

- Coprocessor Operation
- Indexed Load and Store
- Short Displacement Load and Store
- The Floating-Point Instruction Set

Coprocessor Operation Instruction

You must explicitly prescribe the binary value for the desired operation as well as the unit number of the coprocessor.

This instruction uses only completers. Operands are not accepted.

Table 4-37. Coprocessor Operation Instruction

Instruction Name	Mnemonic Name
Coprocessor Operation	COPR,uid,sop,n

Table 4-38. Coprocessor Operation Completers

	Completer Description
uid	(0 - 7) Select coprocessor unit number
sop	Provides a 22 bit value that the assembler encodes in the instruction
n	If the value is one and the coprocessor condition is satisfied, the following instruction is nullified.

NOTE

Identify coprocessor is encoded as COPR,uid,0.

Coprocessor Indexed Load and Store Instructions

A value is transferred between memory and a register. The address is formed by the addition of the index register to the base register. Optionally, the index value may be shifted to reflect an address corresponding to the size of the value being transferred and the base register may be modified after the address has been formed.

Table 4-39. Coprocessor Indexed Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Coprocessor Load Word Indexed	CLDWX,uid,complt	x(s,b),t
Coprocessor Load Doubleword Indexed	CLDDX,uid,complt	x(s,b),t
Coprocessor Store Word Indexed	CSTWX,uid,complt	r,x(s,b)
Coprocessor Store Doubleword Indexed	CSTDX,uid,complt	r,x(s,b)

Table 4-40. Coprocessor Indexed Load and Store Completers

complt	Description
,S	Shift Index by Data Size, No Base Register Modification
,M	No Index Shift Base Register Modification
,S,M or ,SM	Shift Index by Data Size Base Register Modification
none specified	No Index Shift, No Base Register Modification

Coprocessor Short Displacement Load and Store Instructions

A value is transferred between memory and a floating-point register. The address is formed by the addition of the short displacement to the base register. Optionally, the base register may be modified either before or after the address has been formed.

Table 4-41. Coprocessor Short Displacement Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Coprocessor Load Word Short	CLDWS,uid,complt	d(s,b),t
Coprocessor Load Doubleword Short	CLDDS,uid,complt	d(s,b),t
Coprocessor Store Word Short	CSTWS,uid,complt	r,d(s,b)
Coprocessor Store Doubleword Short	CSTDS,uid,complt	r,d(s,b)

Table 4-42. Coprocessor Short Displacement Load and Store Completers

complt	Description
,MB	Modify Before
,MA	Modify After
none specified	No Base Register Modification

Floating-Point Instructions

Floating-point instructions are used to perform floating-point arithmetic. The instructions are either executed directly by a floating-point assist coprocessor or by floating-point emulation software. The floating-point instructions include:

- Indexed Load and Store
- Short Displacement Load and Store
- Operations
- Compare and Test

Floating-Point Indexed Load and Store Instructions

A value is transferred between memory and a floating-point register. The address is formed by the addition of the index register to the base register. Optionally, the index value may be shifted to reflect an address corresponding to the size of the value being transferred and the base register may be modified after the address has been formed.

Table 4-43. Floating-Point Indexed Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Floating-point Load Word Indexed	FLDWX,cmplt	x(s,b),t
Floating-point Load Doubleword Indexed	FLDDX,complt	x(s,b),t
Floating-point Store Word Indexed	FSTWX,complt	r,x(s,b)
Floating-point Store Doubleword Indexed	FSTDX,complt	r,x(s,b)

Table 4-44. Floating-Point Indexed Load and Store Completers

complt	Description
,S	Shift Index by Data Size, No Base Register Modification
,M	No Index Shift Base Register Modification
",S,M" or ,SM	Shift Index by Data Size Base Register Modification
none specified	No Index Shift, No Base Register Modification

Floating-Point Short Displacement Load and Store Instructions

A value is transferred between memory and a floating-point register. The address is formed by the addition of the short displacement to the base register. Optionally, the base register may be modified either before or after the address has been formed.

Table 4-45. Floating-Point Short Displacement Load and Store Instructions

Instruction Name	Mnemonic Name	Operands
Floating-point Load Word Short	FLDWS,cmplt	d(s,b),t
Floating-point Load Doubleword Short	FLDDS,complt	d(s,b),t
Floating-point Store Word Short	FSTWS,cmplt	r,d(s,b)
Floating-point Store Doubleword Short	FSTDS,cmplt	r,d(s,b)

Table 4-46. Floating-Point Short Displacement Load and Store Completers

complt	Description
,MB	Modify Before
,MA	Modify After
none specified	No Base Register Modification

Floating-Point Operation Instructions

Floating-point operation instructions include math functions and data format conversions.

Values from one or two floating-point registers are used to perform an operation and the result is stored in a floating-point register.

Table 4-47. Floating-Point Operation Instructions

Instruction Name	Mnemonic Name	Operands
Floating-point Add	FADD,fmt	r1,r2,t
Floating-point Subtract	FSUB,fmt	r1,r2,t
Floating-point Multiply	FMPY fmt	r1,r2,t
Floating-point Divide	FDIV,fmt	r1,r2,t
Floating-point Square Root	FSQRT,fmt	r,t
Floating-point Absolute Value	FABS,fmt	r,t
Floating-point Remainder	FREM,fmt	r1,r2,t
Floating-point Round to Integer	FRND,fmt	r,t
Floating-point Copy	FCPY,fmt	r,t
Floating-point Convert from Fixed-point to Floating-point	FCNVXF,sf,df	r,t
Floating-point Convert from Floating-point to Fixed-point	FCNVFX,sf,df	r,t
Floating-point Convert from Floating-point to Floating-point	FCNVFF,sf,df	r,t
Floating-point Convert from Floating-point to Fixed-point and Truncate	FCNVFXT,sf,df	r,t

Table 4-48. Floating-Point Format Completers

fmt/df/sf	Format or Size Specified
,SGL or <none>	single (32-bit)
,DBL	double (64-bit)
,QUAD	quad (128-bit)

Floating-Point Compare and Test Instructions

A floating-point register is compared against a floating-point register using the format specified. The operands and/or the result of the comparison are used to determine whether the specified condition is met. If the condition is met, the C bit of the floating-point status register is set; otherwise, it is cleared.

A floating-point test instruction is used to nullify the following instruction based on the state of the C bit. If the C bit is set, the next instruction is skipped; otherwise, it is executed.

Table 4-49. Floating-Point Compare and Test Instructions

Instruction Name	Mnemonic Name	Operands
Floating-point Compare	FCMP,fmt,cond	r1,r2
Floating-point Test	FTEST	

For completer format, refer to Table 4-48.

Table 4-50. Floating-Point Compare Conditions

Cond	Relations				Invalid Operation Except if Unordered
	Greater Than	Less Than	Equal To	Unordered	
false? false ? !<=>	F F F F	F F F F	F F F F	F F T T	F T F T
= =T ?= !<>	F F F F	F F F F	T T T T	F F T T	F T F T
!?>= < ?< !>=	F F F F	T T T T	F F F F	F F T T	F T F T
!?> <= ?<= !>	F F F F	T T T T	T T T T	F F T T	F T F T
!?<= > ?> !<=	T T T T	F F F F	F F F F	F F T T	F T F T
!?< >= ?>= !=	T T T T	F F F F	T T T T	F F T T	F T F T
!?= <> != !=T	T T T T	T T T T	F F F F	F F T T	F T F T
!? <=> true? true	T T T T	T T T T	T T T T	F F T T	F T F T

Pseudo Instructions

Table 4-51 lists the commonly used pseudo instructions that are abbreviations for machine instructions. These pseudo instructions can be used instead of machine instructions.

Table 4-51. Pseudo-Instructions

Pseudo-Instruction Code		Standard Format		
B	w	BL	w, 0	
COMB,cond,n	r1,r2,target	COMBT,cond,n COMBF,cond,n	r1,r2,target r1,r2,target	*
COMIB,cond,n	r1,r2,target	COMIBF,cond,n COMIBT,cond,n	r1,r2,target r1,r2,target	*
ADDB,cond,n	r1,r2,target	ADDBT,cond,n ADDBF,cond,n	r1,r2,target r1,r2,target	*
ADDIB,cond,n	r1,r2,target	ADDIBT,cond,n ADDIBF,cond,n	r1,r2,target r1,r2,target	*
COPY	r,t	OR	r,0,t	
LDI	i,t	LDO	i(0),t	
NOP		OR	0,0,0	
MTSAR	r	MTCTL	r,11	

* The supplied completer determines the actual instruction that the Assembler uses in the conditional branch. You can use the completer for any arithmetic condition or its negation with the pseudo-instructions COMB, COMIB, ADDB, and ADDIB. The false form of the corresponding actual instruction is assembled if the completer specifies the negation of a condition. Otherwise, the true form is used.

Chapter 5
Programming Examples

This chapter consists of five programming examples in the assembly language. The first three examples show typical assembly language code sequences; the last two examples show the correspondence between C, a higher-level programming language, and assembly language.

Example 1 calculates the highest bit position set in a passed parameter. A binary search is used to enhance performance.

Example 2 copies bytes from a source location to a destination location. Both locations and the number of bytes to copy are passed in as parameters.

Example 3 uses Divide Step to divide a 64-bit signed dividend by a 32-bit signed divisor.

Example 4 uses a procedure call from a C program to the Assembler to verify that the program is passing the correct argument.

Example 5 shows a C program that generates assembly code to call `printf`.

Binary Search for Highest Bit Position

In Example 1, the Shift Double and Extract Unsigned instructions are used to implement a binary search. Bits shifted into general register 0 are effectively discarded.

Example 1

```
        .CODE
        .EXPORT post
;
; This procedure calculates the highest bit position
; set in the word passed in as the first argument.
; If passed parameter is non-zero, the algorithm
; starts by assuming it is one.
; A binary search for a set bit is then used
; to enhance performance.
;
; The calculated bit position is returned to the caller.
;
        .PROC
post
        .CALLINFO SAVE_RP
        .ENTER
        COMB,=,N    %r0,%arg0,all_zeros    ; No bits set
        LDI         31,%ret0               ; assume 2 to the 0 power
;
; if extracted bits non-zero, fall thru to change assumption
; else set up 16 low order bits and keep assumption
;
        EXTRU,<>    %arg0,15,16,%r0        ; check 16 high order bits
        SHD,TR      %arg0,%r0,16,%arg0     ; left shift arg0 16 bits
        ADDI        -16,%ret0,%ret0        ; assume 2 to the 16 power
;
; if extracted bits non-zero, fall thru to change assumption
; else set up 8 low order bits and keep assumption
;
        EXTRU,<>    %arg0,7,8,%r0          ; check next 8 high order bits
        SHD,TR      %arg0,%r0,24,%arg0     ; left shift arg0 8 bits
        ADDI        -8,%ret0,%ret0         ; assume 8 higher power of 2
;
; if extracted bits non-zero, fall thru to change assumption
; else set up 4 low order bits and keep assumption
;
        EXTRU,<>    %arg0,3,4,%r0          ; check next 4 high order bits
        SHD,TR      %arg0,%r0,28,%arg0     ; left shift arg0 4 bits
        ADDI        -4,%ret0,%ret0         ; assume 4 higher power of 2
```

```
;
; if extracted bits non-zero, fall thru to change assumption
; else set up 2 low order bits and keep assumption
;
       EXTRU,<>      %arg0,1,2,%r0          ; check next 2 high order bits
       SHD,TR        %arg0,%r0,30,%arg0     ; left shift arg0 2 bits
       ADDI          -2,%ret0,%ret0         ; assume 2 higher power of 2
;
; if extracted bit is zero, fall thru and keep assumption
; else make conclusion
;
       EXTRU,=       %arg0,0,1,%r0          ; check next bit
       ADDI          -1,%ret0,%ret0         ; next higher power of 2
       B,N           tally

all_zeros
       LDI           -1,%ret0

tally
       .LEAVE
       .PROCEND
```

Copying a String

Example 2 contains a section of assembly code that moves a byte string of arbitrary length to an arbitrary byte address.

Example 2

```
;
;
; The routine rflect copies bytes from the source location
; to the destination location.
;
; The first parameter is the source address and the second
; parameter is the destination address.
;
; The third parameter is the number of bytes to copy.
;
; For performance, larger chunks of bytes are handled differently.
;
;
        .CODE
        .EXPORT     rflect,ENTRY
rflect
        .PROC
        .CALLINFO   ENTRY_GR=6,SAVE_RP
        .ENTER
        COMB,=,N    %arg2,%r0,fallout       ; done, count is zero
        COMB,<,N    %arg2,%r0,choke         ; caller error, neg count
        OR          %arg0,%arg1,%r6         ; source and dest
        OR          %r6,%arg2,%r6           ; count
        EXTRU,=     %r6,31,2,%r0            ; 2 low order bits = 0?
        B,N         onebyte                 ; yes, skip this branch
        ADDIBT,<,N  -16,%arg2,chekchunk     ; no, skip chunkify if count<0

chunkify
        LDWN        16(%arg0),%r6           ; word 1- > temp1
                                            ; point ahead 4 words  in source
        LDW         -12(%arg0),%r5          ; place mark 3 wds back- >temp2
        LDW         -8(%arg0),%r4           ; place mark 2 wds back- >temp3
        LDW         -4(%arg0),%r3           ; place mark 1 wds back- >temp4
        STW         %r5,4(%arg1)            ; dest wd 2 <-temp2
        STWM        %r6,16(%arg1)           ; dest wd 1 <-temp1
                                            ; point ahead 4 words in dest
        STW         %r4,-8(%arg1)           ; dest wd 3 <-temp3
        ADDIBF,<    -16,%arg2,chunkify      ; loop if count > 0
        STW         %r3,-4(%arg1)           ; dest wd 2 <-temp1
chekchunk
        ADDIBT,<    12,%arg2,exeunt         ; go if count < -12
        COPY        %r0,%ret0               ; clear rtnval
```

```
subchunk
        LDWS,MA     4(%arg0),%r6          ; word- >temp1
                                          ; point ahead 4 bytes in source
        ADDIBF,<    -4,%arg2,subchunk     ; go if count<4
        STWS,MA     %r6,4(%arg1)          ; dest< -temp1
                                          ; point ahead 4 bytes in dest

        B           exeunt                ; all done
        COPY        %r0,%ret0             ; clear rtnval

onebyte
        LDBS,MA     1(%arg0),%r6          ; temp1 < -byte,bump src pointer
onemore
        STBS,MA     %r6,1(%arg1)          ; dest<-temp1,bump dest pointer
        ADDIBF,=,N  -1,%arg2,onemore      ; decrement count
                                          ; compare for 0.
        LDBS,MA     1(%arg0),%r6          ; delay slot
                                          ; temp1 <-byte,bump src pointer
fallout
        B           exeunt
        COPY        %r0,%ret0

choke
        B           exeunt
        LDI         14,%ret0

exeunt
        .LEAVE
        .PROCEND
```

Dividing a Double-Word Dividend

Example 3 contains the code sequence to divide a 64-bit signed dividend by a 32-bit signed divisor using the DS (Divide Step) instruction. Table 5-1 lists the registers that this program uses.

Example 3

```
start
            MOVB,>=         dvdu,rem,check_mag  ; Move upper dividend
                                                ;   check for < 0
            ADD             0,dvdl,quo          ; Move lower dividend always
            SUB             0,quo,quo           ; Get absolute value of
            SUBB            0,rem,rem           ;   the dividend in rem,quo
check_mag
            SUBT,=          0,dvr,tp            ; Check 0, clear carry,
                                                ;   negate the divisor
                                                ;   and trap if dvr = 0
            DS              0,tp,0;             ; Set V-bit to the complement
                                                ;   of the divisor sign
            ADD             quo,quo,quo         ; Shift msb bit into carry
            DS,<<           rem,dvr,rem         , 1st divide step, if carry
                                                ;   out msb of quotient = 0
            B,n             min_ovfl            ; Abs(quotient) > 2**31
                                                ;   deal with elsewhere
            ADDC            quo,quo,quo         ; Shift quo with/into carry
            DS              rem,dvr,rem         ; 2nd divide step
            ; ...
            ;repeat divide step sequence
            ; ...
            ADDC            quo,quo,quo         ; Shift quo with/into carry
            DS              rem,dvr,rem         ; 31st divide step
            ADDC            quo,quo,quo         ; Shift quo with/into carry
            DS              rem,dvr,rem         ; 32nd divide step,
            ADDC            quo,quo,quo         ; Shift last quo bit into quo
            ADDB,>=,n       rem,0,finish        ; Branch if pos. rem
            ADD,<           dvr,0,0             ; If dvr > 0, add dvr
            ADD,tr          rem,dvr,rem         ;   for correcting rem.
            ADDL            rem,tp,rem          ; Else add absolute value dvr
finish
            ADD,>=          dvdu,0,0            ; Set sign of rem
            SUB             0,rem,rem           ;   to sign of dividend
            XOR,>=          dvdu,dvr,0          ; Get correct sign of quo
            SUB             0,quo,quo           ;   based on operand signs
```

Table 5-1. Register Designations

Register Designations	Purpose
dvr	Register holding divisor.
dvdu, dvdl	Pair of registers holding dividend.
tp	Temporary register.
quo	Register holding quotient.
rem	Register holding remainder.

Demonstrating the Procedure Calling Convention

In Example 4, a C program calls an assembly language program to test if .ENTER and .LEAVE are working correctly. The assembly language program checks to see if the C program has passed the value zero in ARG0. The assembly language program then returns the value RET0 to the calling program.

Example 4

C Program Listing

```
#include <stdio.h>
int errorcount = 0;
main ()
{
     int toterr = 0;
     printf("TESTING FEATURE  000");
     fflush(stdout);
     if( feat000(000) != -9 ) ++errorcount;
     printf("         %d errors\n",errorcount);
     toterr += errorcount;
     errorcount = 0;
}
```

Assembly Program Listing

```
; Assembler Module that passes results back to
; the C driver module
myfeat   .EQU    000
success  .EQU    -9
         .CODE
         .IMPORT errorcount,DATA
         .SUBSPA $CODE$
         .EXPORT feat000,ENTRY
         .PROC
         .CALLINFO
feat000 .ENTER
         COMIB,<>  myfeat,arg0,exit
         LDI       0,ret0
         LDI       success,ret0
exit     .LEAVE
         .PROCEND
         .END
```

Output of the cc -S Command

Example 5 shows how a simple C program generates assembly language code. The program calls the `printf` routine. To run the assembled code, you need to link to the file `/lib/crt0.o` and the C library file. Remember that the `ld` command requires that you link the `crt0.o` file first.

Example 5

C Program Listing

```
main ()
{
     printf ("Hello World\n");
}
```

Assembly Program Listing From the C Compiler

```
        .SPACE  $TEXT$
        .SUPSPA $CODE$,QUAD=0,ALIGN=8,ACCESS=44,CODE_ONLY
main                                            ; C runtime interface
        .PROC                                   ; delimit procedure
        .CALLINFO CALLER,FRAME=0,SAVE_RP        ; no locals, need return
        .ENTRY                                  ; proc entry code follows
        STW     2,-20(0,30)                     ; stack the return pointer
        LDO     48(30),30                       ; set up user stack pointer
        ADDIL   L'$THISMODULE$-$global$,27      ; point to printf data
        .CALL   ARGW0=GR                        ; set up for printf call
        BL      printf,2                        ; call printf thru ret pointer
        LDO     R'$THISMODULE$-$global$(1),26   ; insert argument to printf
L$exit1                                         ; hide from linker
        LDW     -68(0,30),2                     ; get callee return pointer
        BV      0(2)                            ; exit thru return pointer
        .EXIT                                   ; end of exit sequence
        LDO     -48(30),30                      ; stack pointer -> stack frame
        .PROCEND

        .SPACE  $TEXT$
        .SUBSPA $LIT$,QUAD=0,ALIGN=8,ACCESS=44
        .SUBSPA $CODE$,QUAD=0,ALIGN=8,ACCESS=44,CODE_ONLY
        .SUBSPA $UNWIND$,QUAD=0,ALIGN=8,ACCESS=44
        .SUBSPA $CODE$
        .SPACE  $PRIVATE$
        .SUBSPA $DATA$,QUAD=1,ALIGN=8,ACCESS=31
```

```
$THISMODULE$                                    ; demarks local data
        .ALIGN  8
        .STRINGZ        "Hello World\n"         ; local data
        .SUBSPA $BSS$,QUAD=1,ALIGN=8,ACCESS=31,ZERO
        .IMPORT $global$,DATA                   ; global data reference point
        .SPACE  $TEXT$
        .SUBSPA $CODE$
        .EXPORT main,PRIV_LEV=3,RTNVAL=GR       ; for linking this routine
        .IMPORT printf,CODE                     ; external proc declaration
        .END
```

Chapter 6
Assembling Your Program

This chapter describes two different ways you can invoke the Assembler and the various command line options controlling its behavior. It also contains a brief description of the interface between the Assembler and linker, and things you should remember to facilitate the running of an assembly program.

Invoking the Assembler

You may invoke the Assembler directly by using the **as** command. Or, you may invoke the Assembler through the **cc** command which processes the assembly source using the C pre-processor. The next two sections describe these pathways.

Using the as Command

The **as** command is the standard command for invoking the Assembler on the HP Precision Architecture system.

Syntax

```
as [ [option] ... [file] ... ] ...
```

The **as** command resides in the `/bin` directory. If your programming environment does not establish a path to this directory, you must include the pathname as the first part of the **as** command. For example:

```
/bin/as -l line.s box.s draw.s
```

Parameters

option Serves as a flag to the Assembler to take some special action. The **as** command supports the following flags:

`-e` Specifies that the Assembler should tolerate one million errors before terminating the assembly process. Without this option, the Assembler terminates a program after 100 errors.

`-f`	Specifies that procedures can call other procedures as the default condition. Normally, the Assembler assumes that procedures do not call other procedures. (See the CALLS and NO_CALLS parameters for the .CALLINFO directive.).
`-l`	Lists the assembled program on the standard output device. This listing shows instruction offsets and the values stored in each field.
`-o` *filename*	Assigns the specified name to the output file.
`-u`	Prevents the Assembler from creating stack unwind descriptors. This option precludes the use of the .ENTER and .LEAVE directives within a program.
`-v` *filename*	Names a file to which the Assembler writes cross-reference information; this includes the source file and the line number for each appearance of all symbols.

file

Names an input or output file. You can include multiple input files to the **as** command. The Assembler converts this stream of input files to a single output file.

Assembler input files must include the suffix **.s**. The name for the output file corresponds to the name of the last input file, except the Assembler changes the suffix of that file's name to **.o**.

Using the cc Command

You can also use the `cc` command to run the Assembler on files that end with a `.s` suffix. The `cc` command appends the system file `pcc_prefix.s` to the front of the file and pipes the file through the C pre-processor before passing the file to the Assembler.

The system file `pcc_prefix.s` contains the following configuration files:

```
hard_reg.h
soft_reg.h
std_space.h
```

These files are in the directory `/usr/include`. Table 6-1 describes the contents of each file.

NOTE

The Assembler automatically supports the different definitions that the `pcc_prefix.s` file contains and provides them as programming aids without requiring that you include this file as an input file to the `as` command. Refer to "Registers and Register Mnemonics" in Chapter 1 and "Programming Aids" in Chapter 3 for more information.

Table 6-1. PCC_PREFIX.S Definition Files

File Name	Contents
hard_reg.h	Set of .EQU's for hardware registers.
soft_reg.h	Set of register definitions that follows the Procedure Calling Convention.
std_space.h	Set of space and subspace definitions that most Assembly programs use.

The cc command normally strips all as command options from the command line. Therefore, when you want to retain one of these options, you must include the flag -wa,<opt>,... on the cc command line (where <opt> names the Assembler option you want to preserve).

You can use the C pre-processor (cpp) with assembly language programs to include C-type macros, including directives. You can use an exclamation point (!) as a statement terminator to include multiple statements in the body of one macro definition. Furthermore, you can use the .LABEL directive to declare labels within a macro definition.

NOTE

If you use cpp, C-style comments should only be used on separate lines.

Error Message Catalog

The operating system stores the text for the Assembler error messages in a file with the pathname:

/lib/as_msgs.cat.

Linking an Assembly Program

The relocatable object file produced by the Assembler must be processed by the linker, ld, before it can be executed. The linker merges relocatable object files, searches libraries for any routines that are referenced by the user's code, assigns final addresses to all program symbols, and produces an executable program file.

For the simplest assembly program, the command:

```
ld myfile.o
```

is all that is required when myfile.o is the name of the relocatable file produced by the Assembler. The linker produces a program file called a.out, provided that myfile.o did not contain any references to imported symbols. To select a program file name other than a.out, the command:

```
ld myfile.o -o myfile
```

can be used. The -o option specifies the name myfile for the program file.

In practice, however, a single stand-alone assembly program is extremely uncommon. Most assembly language code declares procedures that are called from high-level language programs. In addition, assembly language code often calls procedures in high-level languages. In these cases, the link command must include a special start-up file called /lib/crt0.o, as well as additional relocatable object files and the high-level language libraries. For example, a C program that calls some assembly language code should be linked as follows:

```
ld /lib/crt0.o prog.o asm.o -lc -o myprog
```

In this example, prog.o is the output of the C/HP-UX compiler, asm.o is the output of the Assembler, the -lc option tells the linker to search the C library, and the -o option names the program file myprog.

When the assembly language procedures are written to be called from a high-level language, the high-level language compiler is usually the easiest interface to the linker. The above example could also have been linked with the command:

```
cc prog.o asm.o -o myprog
```

The cc command always runs the linker with the appropriate files and options for linking a C program. Similarly, the pc and f77 commands should be used when the main program is in Pascal or FORTRAN 77 respectively.

Appendix A
Error Messages

This appendix lists all error messages that originate from the HP Precision Architecture Assembler.

The Assembler error messages are divided into the following categories:

- **Warning Messages** -- flag conditions that cause errors in program execution.
- **Error Messages** -- cause the assembly process to terminate abnormally.
- **Panic Messages** -- cause the assembly process to abort immediately.
- **User Warnings** -- cause the assembler to produce an object file and possibly to take a specified corrective action.
- **Limit Errors** -- caused by running into assembler limits or running out of memory.
- **Branching Errors** -- prevent the assembler from creating an object file.

The symbol "<operand>" used in the error messages designates the Assembler source element that is the subject of the error. When an error message is printed during assembly operation, the "<operand>" designation is replaced by the appropriate source element.

Warning Messages

1	MESSAGE	`-L option is obsolete and ignored`
	CAUSE	-L appeared as a command line argument.
	ACTION	Remove -L option from command line argument list.
2	MESSAGE	`Value of <operand> for 5-bit field not in [0..31] (truncated)`
	CAUSE	Second operand of EXTRS, BB, or DEP instruction not between zero and 31 inclusive. The Assembler truncates the value to be the <operand> value MOD 32.
	ACTION	To avoid truncation, specify legal value.
3	MESSAGE	`Extract/Deposit field size of <operand> not in [1..32] (set to 32)`
	CAUSE	Operand field 3 of EXTRS or DEP instruction not between 1 and 32 inclusive.
	ACTION	To override the default value of 32, use legal value in operand field 3.
4	MESSAGE	`Value of <operand> for short signed immed. < -16 (set to -16)`
	CAUSE	This message may appear for one of three reasons: 1) First operand of a deposit immediate instruction (DEPI, VDEPI, ZDEPI, or ZVDEPI) or a conditional branch immediate instruction (ADDIBF, ADDIBT, COMIBF, COMIBT, or MOVIB) is less than -16. 2) Address offset of first operand of a load short instruction (LDBS, LDCWS, LDHS, LDWAS, or LDWS) is less than -16. 3) Address offset of second operand of a store short instruction (STBS, STBYS, STHS, STWAS, or STWS) is less than -16.
	ACTION	Change indicated operand so its value falls between -16 and +15 inclusive.

---

5 **MESSAGE** `Value of <operand> for short signed immed. > 15 (set to 15)`

CAUSE This message may appear for one of three reasons:

1) First operand of a deposit immediate instruction (DEPI, VDEPI, ZDEPI, or ZVDEPI) or a conditional branch immediate instruction (ADDIBF, ADDIBT, COMIBF, COMIBT, or MOVIB) is greater than 15.

2) Address offset of first operand of a load short instruction (LDBS, LDCWS, LDHS, LDWAS, or LDWS) is greater than 15.

3) Address offset of second operand of a store short instruction (STBS, STBYS, STHS, STWAS, or STWS) is greater than 15.

ACTION Change above operand to value between -16 and +15 inclusive.

---

6 **MESSAGE** `Keyword <operand> is obsolete and ignored`

CAUSE Keyword DUMMY used with .SPACE directive or keywords ALONE or ATTEND used with .SUBSPACE directive are obsolete.

ACTION Remove obsolete keywords.

---

7 **MESSAGE** `Space characteristics may not be changed after first declaration`

CAUSE New values assigned to keywords for a space previously declared with a .SPACE directive. This message appears whenever a keyword is assigned a value, even if the values remain the same.

ACTION Use desired values for keywords on first declaration of space. Specify keyword values on first declaration of space only.

---

8 **MESSAGE** `Subspace characteristics may not be changed after first definition`

CAUSE New values assigned to keywords for a subspace previously declared with a .SUBSPACE directive.

ACTION Use desired values for keywords on first declaration of subspace. Specify keyword values on first declaration of space only.

9	MESSAGE	`Size omitted - zero assumed`
	CAUSE	`.COMM` directive used without an integer argument.
	ACTION	Use the `.COMM` directive to issue a storage request for the number of bytes desired.
10	MESSAGE	`Alignment omitted - 8 assumed`
	CAUSE	`.ALIGN` directive used without a power of two integer argument.
	ACTION	Use a power of two integer argument with `.ALIGN`.
11	MESSAGE	`Missing value - zero assumed`
	CAUSE	`.ORIGIN` or `.EQU` directive used without an integer argument.
	ACTION	Specify the actual value of the location offset or identifier desired.
12	MESSAGE	`Size omitted - 4 assumed`
	CAUSE	`.BLOCK` directive used without an integer argument.
	ACTION	Specify the actual number of bytes to be reserved for uninitialized storage.
13	MESSAGE	`Use of GR3 when frame>=8192 may cause conflict`
	CAUSE	General register 3 used in an instruction within a procedure where keyword frame set above 8192. Note: `gr3` is used as a base register for large frames.
	ACTION	Use general register other than `gr3`.
14	MESSAGE	`KEEP should not be in force for this statement`
	CAUSE	`.KEEP` directive outside of a procedure.
	ACTION	Remove `.KEEP` directive.

15	MESSAGE	`Procedure makes calls but is not flagged as CALLER in .CALLINFO`
	CAUSE	Missing `CALLER` keyword in a procedure containing `.CALL`.
	ACTION	Add `CALLER` keyword to `.CALLINFO` directive.
16	MESSAGE	`Value for <operand> must be in range 0..3 (set to 3)`
	CAUSE	Illegal privilege level specified.
	ACTION	Change the privilege level specification.
17	MESSAGE	`Existing register name, number, and type are being overwritten`
	CAUSE	Name (label) used with `.REG` directive was previously defined.
	ACTION	Use a different name in the label part to avoid overwriting previous definition.
18	MESSAGE	`Error message file cannot be located`
	CAUSE	Error message catalog is not in the user path.
	ACTION	Ensure `as_msgs.cat` is in the user path or make `/lib/as_msgs.cat` accessible.
19	MESSAGE	`Defining register missing or defining register has no type`
	CAUSE	Parameter to `.REG` is not one of the predefined Assembler registers nor is it a previously defined (with the `.REG` directive) register.
	ACTION	Either use one of the predefined Assembler registers or define register type using the `.REG` directive.

20	MESSAGE	General register expected in this field - <operand>
	CAUSE	Wrong register type used.
	ACTION	Use a general register.
21	MESSAGE	Space register expected in this field - <operand>
	CAUSE	Wrong register type used.
	ACTION	Use a space register.
22	MESSAGE	Control register expected in this field - <operand>
	CAUSE	Wrong register type used.
	ACTION	Use a control register.
23	MESSAGE	Floating point register expected in this field - <operand>
	CAUSE	Wrong register type used.
	ACTION	Use a floating point register.
24	MESSAGE	Location counter must be in range 0..3 (set to 0) - <argument>
	CAUSE	Argument to .LOCCT is not within 0..3 range.
	ACTION	Change argument to .LOCCT to be within 0..3 range.

Error Messages

1000	MESSAGE	`Unterminated quoted string`
	CAUSE	String specified as in `.STRING`, without trailing quotes.
	ACTION	Add trailing quotes to string.

1001	MESSAGE	`Undefined register symbol`
	CAUSE	Parenthesized instruction operand does not have a corresponding `.EQU` directive.
	ACTION	Equate register symbols to values zero through 31.

1002	MESSAGE	`Undefined completer`
	CAUSE	Invalid value in instruction completer field.
	ACTION	Use only those completers specified in the *Precision Architecture and Instruction Reference Manual.*

1003	MESSAGE	`Improper completer specified`
	CAUSE	Completer used with an instruction which does not take completers.
	ACTION	Use completers only with instructions specified for them in the *Precision Architecture and Instruction Reference Manual.*

1004	MESSAGE	`Output file name missing`
	CAUSE	-o option given to Assembler but not followed by a filename.
	ACTION	Place desired output filename after -o option.

1005	MESSAGE	`Unable to open xref file: <operand>`
	CAUSE	A file specified with the -v option is not writable.
	ACTION	Use a different filename.

1006	MESSAGE	`XREF file name missing after -v`
	CAUSE	Filename omitted from command line.
	ACTION	Provide a filename after -v to dump the cross-reference information.

1007	MESSAGE	`Label not allowed here in this expr`
	CAUSE	1) Register specified by identifier. 2) An expression contains the sequence immediate-operator-label.
	ACTION	1) Use integer values for registers. 2) Use labels only as first term when combining with immediate values.

1008	MESSAGE	`Illegal symbol in expression`
	CAUSE	An expression contains a sequence other than label-operator term or term-operator-term.
	ACTION	Place operators +, -, *, / between a label and a term or a term and a term.

1009	MESSAGE	`Field selector not allowed in pc_relative expression`
	CAUSE	Field selector, such as L' or R' used on an expression contained in a branch instruction.
	ACTION	Omit field selector from branch instruction.

1010	MESSAGE	`String not allowed in pc_relative expression`
	CAUSE	String used as the target of a branch instruction.
	ACTION	Target branch to an expression beginning with a label or "."
1011	MESSAGE	`"." allowed in pc_rel expression only`
	CAUSE	"." used as an operand in a nonbranch, external branch or vectored branch.
	ACTION	Use "." only in branch instructions other than branch external or branch vectored.
1012	MESSAGE	`PC_relative expression must begin with . or label`
	CAUSE	Branch target poorly formed.
	ACTION	Use label or "." as first term of branch target expression.
1013	MESSAGE	`Second label not allowed in pc_relative expression`
	CAUSE	Branch target poorly formed: label-operator-label.
	ACTION	Use an offset in place of second label.
1014	MESSAGE	`Labels may not be added - only subtracted`
	CAUSE	Attempt to form an expression using sum of two labels.
	ACTION	Use an offset in place of second label.
1015	MESSAGE	`Unexpected end of expression`
	CAUSE	Nothing follows a +, -, /, or * in an expression.
	ACTION	Place meaningful terms, integers, or labels after operator.

1016	MESSAGE	General register <operand> is out of range
	CAUSE	Register number specified greater than 31.
	ACTION	Use register number between zero and 31.
1017	MESSAGE	Value of <operand> for space register not in [0..3]
	CAUSE	Load or privileged store instruction references a space register greater than 3.
	ACTION	Change space register number to a legal value.
1018	MESSAGE	Value of <operand> for space register not in [0..7]
	CAUSE	Branch or privileged instruction uses space register greater than 7.
	ACTION	Change space register number to a legal value.
1019	MESSAGE	Opcode not defined
	CAUSE	Characters in opcode field do not comprise legal machine instruction or directive.
	ACTION	Starting in column 2, use only defined opcodes and directives.
1020	MESSAGE	Number required for keyword value
	CAUSE	A .CALLINFO keyword is set equal to a nonnumeric argument.
	ACTION	Ensure .CALLINFO keywords are assigned numeric values.
1021	MESSAGE	Unrecognized value for keyword
	CAUSE	Illegal assignment to an ARGW or RTNVAL keyword in .CALL or .EXPORT directive.
	ACTION	Use "NO", "GR", "FR", or "FU" appropriately.

1022	MESSAGE	`This statement must occur within a declared subspace`
	CAUSE	Instruction or directive present before .SUBSPA directive.
	ACTION	Use .SUBSPA directive before issuing instruction or data.

1023	MESSAGE	`Directive not allowed inside a procedure`
	CAUSE	Use of .LOCCT, .SPACE, or .SUBSPA within a procedure.
	ACTION	Do not attempt to change location counter, space or subspace within a procedure.

1024	MESSAGE	`Space name required`
	CAUSE	.SPACE directive not followed by a valid name.
	ACTION	Follow .SPACE directive with a name starting with an alphabetic character.

1025	MESSAGE	`Unrecognized keyword`
	CAUSE	Directive, such as .SPACE, .SUBSPA, or .CALLINFO, followed by a keyword not specified in Assembler manual.
	ACTION	Follow directives with legal keywords separated by commas.

1026	MESSAGE	`Name previously defined`
	CAUSE	Subspace name matches a space name.
	ACTION	Choose subspace names different from space names.

1027	MESSAGE	`This item must be declared within a space`
	CAUSE	A directive, such as .SUBSPA, is used before the first .SPACE directive.
	ACTION	Place .SPACE directive prior to offending directive.

1028	MESSAGE	`Subspace name required`
	CAUSE	.SUBSPA directive parameter list does not begin with a valid name.
	ACTION	.SUBSPA must be followed by name beginning with an alphabetic character or "$".
1029	MESSAGE	`This statement must appear within a procedure`
	CAUSE	Directive, such as .CALLINFO, .ENTER, or .LEAVE, is used outside of a procedure.
	ACTION	Use procedure related directives only within a procedure.
1030	MESSAGE	`Only one .CALLINFO per procedure`
	CAUSE	Multiple .CALLINFO directives between successive .PROC directives.
	ACTION	Place all desired keywords in one .CALLINFO directive for the procedure.
1031	MESSAGE	`Value for <operand> must be >=0`
	CAUSE	In a .CALLINFO directive, FRAME is assigned an identifier equated to a negative value.
	ACTION	Use only nonnegative FRAME values.
1032	MESSAGE	`Value for <operand> must be in range 3..19`
	CAUSE	In a .CALLINFO directive, ENTRY_GR is assigned a value less than 3 or greater than 19.
	ACTION	Assign ENTRY_GR a value between 3 and 19 inclusive. Note: Use of value zero is also legal here.

1033	MESSAGE	`Value for <operand> must be in range 12..31`
	CAUSE	In a .CALLINFO directive, ENTRY_FR is assigned a value less than 12 or greater than 31.
	ACTION	Set ENTRY_FR to a value between 12 and 31 inclusive. Note: Use of value zero is also legal here.
1034	MESSAGE	`ENTRY_SR must be 3 or not specified`
	CAUSE	.CALLINFO contains keyword specifying saved space register other than three.
	ACTION	Omit ENTRY_SR keyword as other space registers do not require saving.
1037	MESSAGE	`Nested .PROC`
	CAUSE	.PROC directive present within .PROC - .PROCEND sequence.
	ACTION	Insert .PROCEND between successive .PROCs or remove any unnecessary .PROCs.
1038	MESSAGE	`Variable name missing`
	CAUSE	Label omitted in .COMM or .EQU directive.
	ACTION	Use label with all .COMM or .EQU directives.
1039	MESSAGE	`Missing string constant`
	CAUSE	.STRING, .STRINGZ, .VERSION, or .COPYRIGHT directive present without a string operand.
	ACTION	Add missing quoted string after directive.

1040	MESSAGE	Only one copyright message permitted
	CAUSE	Multiple copyright directives present.
	ACTION	Combine messages and use one copyright directive.

1041	MESSAGE	Export name required
	CAUSE	.EXPORT directive not followed by an identifier.
	ACTION	Follow .EXPORT directive with a legal identifier that must begin with an alphabetic character, an underscore, or a dollar sign.

1042	MESSAGE	Import name required
	CAUSE	.IMPORT directive not followed by a legal identifier.
	ACTION	Add missing identifier after .IMPORT directive.

1043	MESSAGE	<operand> not permitted for export
	CAUSE	.EXPORT directive not followed by a legal identifier.
	ACTION	Provide appropriate identifier after .EXPORT directive.

1044	MESSAGE	Name required for label definition
	CAUSE	.LABEL directive not followed by legal identifier.
	ACTION	Add missing identifier after .LABEL directive

1045	MESSAGE	Name to be defined by .LABEL must appear as operand.
	CAUSE	Identifier present in column one in a .LABEL directive.
	ACTION	Place identifier after .LABEL, not before it.

1046	MESSAGE	`Duplicate definition of symbol`
	CAUSE	A label was used more than once.
	ACTION	Give labels unique names.

1047	MESSAGE	`Unmatched .PROCEND`
	CAUSE	Two `.PROCEND` directives present without `.PROC` directive in between.
	ACTION	Each procedure should begin with a single `.PROC` and end with a `.PROCEND`.

1048	MESSAGE	`A procedure may not be empty`
	CAUSE	`.PROC` followed by `.PROCEND` with no executable code between.
	ACTION	Use at least `.CALLINFO`, `.ENTER`, and `.LEAVE` within procedure body.

1049	MESSAGE	`Procedure does not have .CALLINFO`
	CAUSE	Missing `.CALLINFO` directive between `.PROC` and `.PROCEND`.
	ACTION	Insert `.CALLINFO` following `.PROC`.

1050	MESSAGE	`Illegal symbol in label position`
	CAUSE	Character present in column one which is not alphabetic, underscore, or dollar sign.
	ACTION	Use only legal identifiers in label field.

1051	MESSAGE	`Illegal symbol in opcode position`
	CAUSE	A sequence of characters starting in column two or beyond does not begin with an alphabetic character or a period.
	ACTION	Use only prescribed opcodes and directives starting in column two or beyond.

1052	MESSAGE	`Directive name not recognized`
	CAUSE	A sequence of characters starting in column two or beyond, beginning with a period, does not correspond to a prescribed directive.
	ACTION	When beginning with a period, use only prescribed directives starting in column two or beyond.
1054	MESSAGE	`Unexpected items at end of line`
	CAUSE	Legal operands are followed by trailing characters or operators.
	ACTION	Examine entire sequence of operands for syntactic integrity.
1055	MESSAGE	`Label must be defined within a declared subspace`
	CAUSE	Label present prior to a .SUBSPA directive.
	ACTION	Place label after issuing .SUBSPA directive.
1056	MESSAGE	`Empty source file(s)`
	CAUSE	No space has been declared.
	ACTION	Use at least one .SPACE directive.
1057	MESSAGE	`Missing .PROCEND`
	CAUSE	Last procedure in program does not end with .PROCEND.
	ACTION	Add .PROCEND directive to last procedure in program.
1059	MESSAGE	`Divide by zero`
	CAUSE	Attempt to perform a division operation with a zero divisor.
	ACTION	Be sure value for divisor can not become equal to zero.

1060	MESSAGE	`Argument 1 or 3 in FARG upper`
	CAUSE	Using the FU value with the ARGW1 or ARGW3 keywords.
	ACTION	Only use the FU value with ARGW0 or ARGW2 keywords.
1061	MESSAGE	`Closing parenthesis is missing in expression`
	CAUSE	Mismatched parenthesis.
	ACTION	Insert closing parenthesis at the end of the expression.
1062	MESSAGE	`Macro parameters must be separated by commas`
	CAUSE	Formal parameters to `.MACRO` or actual parameters to a macro call are not separated by commas.
	ACTION	Insert commas between parameters.
1063	MESSAGE	`Unterminated macro definition`
	CAUSE	A `.MACRO` directive is not matched with an `.ENDM` directive.
	ACTION	Terminate the macro definition with an `.ENDM` directive.
1064	MESSAGE	`Poorly formed macro parameter`
	CAUSE	Formal parameter to the macro definition is not in an Assembler-accepted form.
	ACTION	Change the form of the formal parameter to an acceptable form.
1065	MESSAGE	`Poorly formed .FLOAT or .DOUBLE argument`
	CAUSE	The floating point number that was used as the argument to `.FLOAT` or `.DOUBLE` is not in the right format.
	ACTION	Use the correct floating point format for the argument.

1066	MESSAGE	`Poorly formed bit field specifier`
	CAUSE	Bit field is not being specified in the form {x..y} where x and y are natural numbers.
	ACTION	Specify bit fields in the correct form.
1067	MESSAGE	`Bit field too wide for instruction field`
	CAUSE	Mismatched bit field declaration and use.
	ACTION	Use the same length for both the bit field being assigned to and the bit field being assigned from.
1068	MESSAGE	`Brace outside of macro definition`
	CAUSE	Opening or closing braces are being used outside a macro definition.
	ACTION	Remove opening or closing braces or use them before the `.ENDM`.
1069	MESSAGE	`Equal sign required in bit field assignment`
	CAUSE	Missing operator = for assigning one bit field to another.
	ACTION	Insert equal sign (=) for bit field assignment.
1070	MESSAGE	`Bit range must be within {0..31}`
	CAUSE	Range specified in bit field is not 0..31.
	ACTION	Ensure bit field range is within 0..31.

1071	MESSAGE	`Opening brace expected in bit range designator`
	CAUSE	Missing opening brace to specify a bit field.
	ACTION	Use correct format for bit field specification.
1072	MESSAGE	`Ending brace expected in bit range designator`
	CAUSE	Missing closing brace to specify a bit field.
	ACTION	Use correct format for bit field specification.
1073	MESSAGE	`Unmatched .ENDM`
	CAUSE	No `.MACRO` was recognized as corresponding to the `.ENDM`.
	ACTION	Either remove the unmatched `.ENDM` or insert a `.MACRO` in appropriate position preceding the `.ENDM`.
1074	MESSAGE	`Illegal expression type for plabel`
	CAUSE	More than one label was found in a plabel expression.
	ACTION	Use only one label in a procedure label expression.
1075	MESSAGE	`Undefined field selector`
	CAUSE	Illegal field selector is being used.
	ACTION	Use correct field selector.

Panic Messages

2000	MESSAGE	`Exceeded maximum error count`
	CAUSE	More than 100 errors were detected and the -e option was not invoked.
	ACTION	Use -e option to permit up to a million errors.
2001	MESSAGE	`Bad option - <operand>`
	CAUSE	An option flag was used on the command line that does not correspond to an option in the Assembler manual.
	ACTION	Use only prescribed options.
2002	MESSAGE	`Unable to open input file: <operand>`
	CAUSE	Requested input file is either nonexistent or unreadable.
	ACTION	Check for presence of requested input file and examine read-write permissions.
2003	MESSAGE	`Unable to open output file: <operand>`
	CAUSE	1) Output file exists and is not writable. 2) File system error.
	ACTION	1) Make output file writable. 2) Contact HP-UX system administrator.
2004	MESSAGE	`Free storage exhausted`
	CAUSE	Assembler cannot allocate memory for its internal structures.
	ACTION	Break up the program into smaller modules. If this doesn't work, contact HP-UX system administrator.

2005	MESSAGE	`Internal instruction parsing error on <operand>`
	CAUSE	Assembler has an internal defect.
	ACTION	Contact HP-UX system administrator.
2006	MESSAGE	`Unable to regain access to source file for listing`
	CAUSE	Not able to access source file for reading.
	ACTION	Check for existence of source file and permission to read it.
2007	MESSAGE	`Unable to access temporary file to build listing`
	CAUSE	Not able to write to the temporary listing file. Could be a file system error.
	ACTION	Call HP-UX system administrator.
2008	MESSAGE	`Unterminated macro definition`
	CAUSE	Macro definition is not complete until a `.ENDM` is encountered.
	ACTION	Insert `.ENDM` at the end of the macro definition.

User Warnings

Errors 7100 through 7199 are user warnings. The assembler will proceed, and produce an object file, in some cases taking the described form of corrective action.

7100

MESSAGE `code subspace has no unwind subspace`

CAUSE No unwind subspace was specified for the code subspace.

ACTION Contact HP-UX system administrator.

7101

MESSAGE `Improper completer, <completer>, given for opcode [opcode] - ignored`

CAUSE The completer given is not valid for the opcode.

The assembler generates object code as if the completer were not given.

ACTION You should either remove the completer or give a correct completer.

7102

MESSAGE `Immediate value of <constant> for 5-bit field in <opcode> not in [0..31] (truncated)`

CAUSE The constant was given as an operand for the opcode, and is larger than the 5-bit field allows.

The lower five bits of the given constant are used.

ACTION You should change the value to within the limits (0 through 31) or use a different instruction.

7103

MESSAGE `Extract/deposit of <constant> for field size in [opcode] not in [1..32] (set to 32)`

CAUSE The constant was given as a field size for the extract or deposit instruction with the specified opcode, and is larger than the 5-bit field allows.

The constant is set to 32 unless you take some action.

ACTION You should change the value to within the limits (1 through 32), or use a different instruction.

7104	MESSAGE	Immediate value of <constant> for <opcode> is less than -16 (set to -16)
	CAUSE	The constant was given as an operand for the opcode, and is smaller than the 5-bit signed field allows.
	ACTION	You should change the value to within the limits (-16 through 15), or use a different instruction.

7105	MESSAGE	Immediate value of <constant> for <opcode> is greater than 15 (set to 15)
	CAUSE	The constant was given as an operand for the opcode, and is larger than the 5-bit signed field allows.
	ACTION	You should change the value to within the limits (-16 through 15), or use a different instruction.

7106	MESSAGE	DSR value of <constant> for <opcode> not in [0..3] - truncated
	CAUSE	A data space register value other than 0,1,2, or 3 was given for the specified opcode.
	ACTION	You should change the value to within the limits (0 through 3).

7107	MESSAGE	CSR value of <constant> for <opcode> not in [0..7] - truncated
	CAUSE	A data space register value (constant) other than zero through 7 was given for the specified opcode.
	ACTION	You should change the value to within the limits (0 through 7).

7108	MESSAGE	The value <constant> did not fit into a <field size> bit field at offset <offset> (op code - [opcode])
	CAUSE	During object file generation, a symbol reference (such as branch label or load offset) being resolved to a constant could not be resolved within the field of the referencing instruction. The value of the actual constant being placed into the instruction is given, as well as the size of the field, the offset from the beginning of the subspace of the offending instruction, and the opcode of the offending instruction.
	ACTION	You must remove the reference, or use a different instruction sequence that can accommodate the size of the constant.

7109	MESSAGE	Tried to define the value of non-absolute symbol <symbol-name>
	CAUSE	You used a .EQU directive to define a symbol that was already defined as a non-absolute symbol, such as DATA or ENTRY.
	ACTION	You must either remove or change the symbol name in the .EQU directive, or resolve the inconsistency with the other uses of that symbol.

Limit Errors

Errors 7200 through 7299 are fatal errors that you may be able to work around. They involve running into assembler limits or running out of memory.

7200	MESSAGE	`internal table overflow`
	CAUSE	Too many labels in the object file.
	ACTION	Split the file. Make global variable and procedure names shorter. This should rarely happen.

7201	MESSAGE	`new_slc_block: out of memory`
	CAUSE	The assembler attempted to allocate some dynamic memory, and the system was unable to provide the memory.
	ACTION	1) Check the system limits because other processes that allocate dynamic memory might also be running. More memory might be available at another time. 2) Break your assembly file into smaller pieces, and assemble them separately.

7202	MESSAGE	`init_link: Out of memory`
	CAUSE	The assembler attempted to allocate some dynamic memory, and the system was unable to provide the memory.
	ACTION	1) Check the system limits because other processes might be running that also allocate dynamic memory. More memory might be available at another time. 2) Break up your assembly file into smaller pieces and assemble them separately.

7203	MESSAGE	`allocate_bytes: Out of memory`
	CAUSE	The assembler attempted to allocate some dynamic memory, and the system was unable to provide the memory.
	ACTION	1) Check the system limits because other processes might be running that also allocate dynamic memory. More memory might be available at another time. 2) Break up your assembly file into smaller pieces, and assemble them separately.

7204	MESSAGE	`error in writing to output file.`
	CAUSE	The assembler cannot write to the object file.
	ACTION	Contact HP-UX system administrator to check for file system errors.

Branching Errors

Errors 7400 through 7405 are branching errors that prevent the assembler from creating an object file. You must correct these errors to assemble your program.

7400	MESSAGE	`Procedure number <number> has no label known to linker`
	CAUSE	You used the .PROC directive to specify the beginning of a procedure, but have not exported a procedure label. This is necessary for creating unwind tables.
	ACTION	You need to export a label for the procedure.

7401	MESSAGE	`Attempt to set location counter backward with .ORIGIN value of <constant>`
	CAUSE	You specified a value for the .ORIGIN directive that causes the location of the following item to be earlier than the previous item.
	ACTION	You must either delete items before the .ORIGIN directive to adjust the offset of the immediately preceding item, or adjust the value on the .ORIGIN directive.

7402	MESSAGE	`Procedure call to non entry point: <label name>`
	CAUSE	You used the .CALL directive to mark a procedure call to a label that is not an entry point. It must be marked with either .ENTER or .ENTRY.
	ACTION	You must either remove the .CALL directive, change the target on the .CALL directive, or place a .ENTER or .ENTRY at the target.

7403	MESSAGE	`undefined label - <label name>`
	CAUSE	You used the given label in an expression, such as a branch instruction or a .WORD directive, but the label was never defined.
	ACTION	Remove the reference to the label. Or define it by exporting it or using it as a label on an instruction or data item.

7404	MESSAGE	branch target .-<constant> unresolvable, instruction number <number>
	CAUSE	You specified a negative displacement from the current location, and there is no instruction there.
	ACTION	You must place an instruction at the target of the branch, or change the constant in the branch.

7405	MESSAGE	branch target .+<constant> unresolvable, instruction number <number>
	CAUSE	You specified a branch to the current location plus a constant, but there is no instruction there. The sequence number of the branch instruction within its subspace is given.
	ACTION	You must place an instruction at the target of the branch, or change the constant in the branch.

Appendix B
Instruction Summaries

Table B-1 lists the different Assembler machine instructions, alphabetically, by their mnemonic names.

Table B-1. Instructions Arranged by Mnemonic Name

Mnemonic Name	Operands	Instruction Name
ADD,cond	r1,r2,t	Add
ADDB,cond,n	r1,r2,target	Add and Branch *
ADDBF,cond,n	r1,r2,target	Add and Branch If False
ADDBT,cond,n	r1,r2,target	Add and Branch If True
ADDC,cond	r1,r2,t	Add With Carry
ADDCO,cond	r1,r2,t	Add With Carry and Trap On Overflow
ADDI,cond	i,r,t	Add To Immediate
ADDIB,cond,n	i,r2,target	Add Immediate and Branch *
ADDIBF,cond,n	i,r2,target	Add Immediate and Branch If False
ADDIBT,cond,n	i,r2,target	Add Immediate and Branch If True
ADDIL	i,r	Add Immediate Left
ADDIO,cond	i,r,t	Add To Immediate and Trap On Overflow
ADDIT,cond	i,r,t	Add To Immediate and Trap On Condition
ADDITO,cond	i,r,t	Add to Immediate and Trap On Condition or Overflow
ADDL,cond	r1,r2,t	Add Logical
ADDO,cond	r1,r2,t	Add and Trap On Overflow

*Pseudo instruction.

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
AND,cond	r1,r2,t	And
ANDCM,cond	r1,r2,t	And Complement
B,n	target	Branch *
BB,cond,n	r1,p,target	Branch On Bit
BE,n	wd(sr,b)	Branch External
BL,n	target,t	Branch and Link
BLE,n	wd(sr,b)	Branch and Link External
BLR,n	x,t	Branch and Link Register
BREAK	i1,i2	Break
BV,n	x(b)	Branch Vectored
BVB,cond,n	r1,target	Branch On Variable Bit
CLDDS,uid,cmplt	i(s,b),t	Coprocessor Load Doubleword Short
CLDDX,uid,cmplt	x(s,b),t	Coprocessor Load Doubleword Indexed
CLDWS,uid,cmplt	d(s,b),t	Coprocessor Load Word Short
CLDWX,uid,cmplt	x(s,b),t	Coprocessor Load Word Indexed
COMB,cond,n	r1,r2,target	Compare and Branch *
COMBF,cond,n	r1,r2,target	Compare and Branch If False
COMBT,cond,n	r1,r2,target	Compare and Branch If True
COMCLR,cond	r1,r2,t	Compare and Clear
COMIB,cond,n	i,r2,target	Compare Immediate and Branch *
COMIBF,cond,n	i,r2,target	Compare Immediate and Branch If False
COMIBT,cond,n	i,r2,target	Compare Immediate and Branch If True
COMICLR,cond	i,r,t	Compare Immediate and Clear

*Pseudo instruction.

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
COPR,uid,sop,n		Coprocessor Operation
COPY	r,t	Copy *
CSTDS,uid,cmplt	r,d(s,b)	Coprocessor Store Doubleword Short
CSTDX,uid,cmplt	r,x(s,b)	Coprocessor Store Doubleword Indexed
CSTWS,uid,cmplt	r,d(s,b)	Coprocessor Store Word Short
CSTWX,uid,cmplt	r,x(s,b)	Coprocessor Store Word Indexed
DCOR,cond	r,t	Decimal Correct
DEP,cond	r,p,len,t	Deposit
DEPI,cond	i,p,len,t	Deposit Immediate
DIAG	i	Diagnose
DS,cond	r1,r2,t	Divide Step
EXTRS,cond	r,p,len,t	Extract Signed
EXTRU,cond	r,p,len,t	Extract Unsigned
FABS,fmt	r,t	Floating-point Absolute Value
FADD,fmt	r1,r2,t	Floating-point Add
FCMP,fmt,cond	r1,r2	Floating-point Compare
FCNVFF,sf,df	r,t	Floating-point Convert from Floating-point to Floating-point
FCNVFX,sf,df	r,t	Floating-point Convert from Floating-point to fixed-Point
FCNVFXT,sf,df	r,t	Floating-point Convert from Floating-point to Fixed-point and Truncate
FCNVXF,sf,df	r,t	Floating-point Convert from Fixed-point to Floating-point
FCPY,fmt	r,t	Floating-point Copy

*Pseudo instruction.

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
FDC,cmplt	x(s,b)	Flush Data Cache
FDCE,cmplt	x(s,b)	Flush Data Cache Entry
FDIV,fmt	r1,r2,t	Floating-point Divide
FIC,cmplt	x(sr,b)	Flush Instruction Cache
FICE,cmplt	x(sr,b)	Flush Instruction Cache Entry
FLDDS,cmplt	d(s,b),t	Floating-point Load Doubleword Short
FLDDX,cmplt	x(s,b),t	Floating-point Load Doubleword Indexed
FLDWS,cmplt	d(s,b),t	Floating-point Load Word Short
FLDWX,cmplt	x(s,b),t	Floating-point Load Word Indexed
FMPY,fmt	r1,r2,t	Floating-point Multiply
FREM,fmt	r1,r2,t	Floating-point Remainder
FRND,fmt	r,t	Floating-point Round to Integer
FSQRT,fmt	r,t	Floating-point Square Root
FSTDS,cmplt	r,d(s,b)	Floating-point Store Doubleword Short
FSTDX,cmplt	r,x(s,b)	Floating-point Store Doubleword Indexed
FSTWS,cmplt	r,d(s,b)	Floating-point Store Word Short
FSTWX,cmplt	r,x(s,b)	Floating-point Store Word Indexed
FSUB,fmt	r1,r2,t	Floating-point Subtract
FTEST		Floating-point Test
GATE,n	target,t	Gateway
IDCOR,cond	r,t	Intermediate Decimal Correct
IDTLBA	r,(s,b)	Insert Data Translation Lookaside Buffer Address

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Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
IDTLBP	r,(s,b)	Insert Data Translation Lookaside Buffer Protection
IITLBA	r,(sr,b)	Insert Instruction Translation Lookaside Buffer Address
IITLBP	r,(sr,b)	Insert Instruction Translation Lookaside Buffer Protection
LDB	d(s,b),t	Load Byte
LDBS,cmplt	d(s,b),t	Load Byte Short
LDBX,cmplt	x(s,b),t	Load Byte Indexed
LDCWS,cmplt	d(s,b),t	Load and Clear Word Short
LDCWX,cmplt	x(s,b),t	Load and Clear Word Indexed
LDH	d(s,b),t	Load Halfword
LDHS,cmplt	d(s,b),t	Load Halfword Short
LDHX,cmplt	x(s,b),t	Load Halfword Indexed
LDI	i,t	Load Immediate *
LDIL	i,t	Load Immediate Left
LDO	d(b),t	Load Offset
LDSID	(s,b),t	Load Space Identifier
LDW	d(s,b),t	Load Word
LDWAS,cmplt	d(b),t	Load Word Absolute Short
LDWAX,cmplt	x(b),t	Load Word Absolute Indexed
LDWM	d(s,b),t	Load Word and Modify
LDWS,cmplt	d(s,b),t	Load Word Short
LDWX,cmplt	x(s,b),t	Load Word Indexed

*Pseudo instruction.

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
LHA,cmplt	x(s,b),t	Load Hash Address
LPA,cmplt	x(s,b),t	Load Physical Address
MFCTL	r,t	Move From Control Register
MFSP	sr,t	Move From Space Register
MOVB,cond,n	r1,r2,target	Move and Branch
MOVIB,cond,n	i,r2,target	Move Immediate and Branch
MTCTL	r,t	Move To Control Register
MTSAR	r	Move To Shift Amount Register *
MTSM	r	Move To System Mask
MTSP	r,sr	Move To Space Register
NOP		No Operation *
OR,cond	r1,r2,t	Inclusive OR
PDC,cmplt	x(s,b)	Purge Data Cache
PDTLB,cmplt	x(s,b)	Purge Data Translation Lookaside Buffer
PDTLBE,cmplt	x(s,b)	Purge Data Translation Lookaside Buffer Entry
PITLB,cmplt	x(sr,b)	Purge Instruction Translation Lookaside Buffer
PITLBE,cmplt	x(sr,b)	Purge Instruction Translation Lookaside Buffer Entry
PROBER	(s,b),r,t	Probe Read Access
PROBERI	(s,b),i,t	Probe Read Access Immediate
PROBEW	(s,b),r,t	Probe Write Access
PROBEWI	(s,b),i,t	Probe Write Access Immediate
RFI		Return From Interruption

*Pseudo instruction.

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
RSM	i,t	Reset System Mask
SH1ADD,cond	r1,r2,t	Shift One and Add
SH1ADDL,cond	r1,r2,t	Shift One and Add Logical
SH1ADDO,cond	r1,r2,t	Shift One, Add and Trap On Overflow
SH2ADD,cond	r1,r2,t	Shift Two and Add
SH2ADDL,cond	r1,r2,t	Shift Two and Add Logical
SH2ADDO,cond	r1,r2,t	Shift Two, Add and Trap On Overflow
SH3ADD,cond	r1,r2,t	Shift Three and Add
SH3ADDL,cond	r1,r2,t	Shift Three and Add Logical
SH3ADDO,cond	r1,r2,t	Shift Three, Add and Trap On Overflow
SHD,cond	r1,r2,count,t	Shift Double
SSM	i,t	Set System Mask
STB	r,d(s,b)	Store Byte
STBS,cmplt	r,d(s,b)	Store Byte Short
STBYS,cmplt	r,d(s,b)	Store Bytes Short
STH	r,d(s,b)	Store Halfword
STHS,cmplt	r,d(s,b)	Store Halfword Short
STW	r,d(s,b)	Store Word
STWAS,cmplt	r,d(b)	Store Word Absolute Short
STWM	r,d(s,b)	Store Word and Modify
STWS,cmplt	r,d(s,b)	Store Word Short
SUB,cond	r1,r2,t	Subtract
SUBB,cond	r1,r2,t	Subtract With Borrow
SUBBO,cond	r1,r2,t	Subtract With Borrow and Trap On Overflow

(continued on next page)

Table B-1. Instructions Arranged by Mnemonic Name (continued)

Mnemonic Name	Operands	Instruction Name
SUBI,cond	i,r,t	Subtract from Immediate
SUBIO,cond	i,r,t	Subtract from Immediate and Trap On Overflow
SUBO,cond	r1,r2,t	Subtract and Trap On Overflow
SUBT,cond	r1,r2,t	Subtract and Trap On Condition
SUBTO,cond	r1,r2,t	Subtract and Trap On Condition or Overflow
SYNC		Synchronize Caches
UADDCM,cond	r1,r2,t	Unit Add Complement
UADDCMT,cond	r1,r2,t	Unit Add Complement and Trap On Condition
UXOR,cond	r1,r2,t	Unit Exclusive Or
VDEP,cond	r,len,t	Variable Deposit
VDEPI,cond	i,len,t	Variable Deposit Immediate
VEXTRS,cond	r,len,t	Variable Extract Signed
VEXTRU,cond	r,len,t	Variable Extract Unsigned
VSHD,cond	r1,r2,t	Variable Shift Double
XOR,cond	r1,r2,t	Exclusive Or
ZDEP,cond	r,p,len,t	Zero and Deposit
ZDEPI,cond	i,p,len,t	Zero and Deposit Immediate
ZVDEP,cond	r,len,t	Zero and Variable Deposit
ZVDEPI,cond	i,len,t	Zero and Variable Deposit Immediate

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- **E** Electronic Instruments & Measurement Systems
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