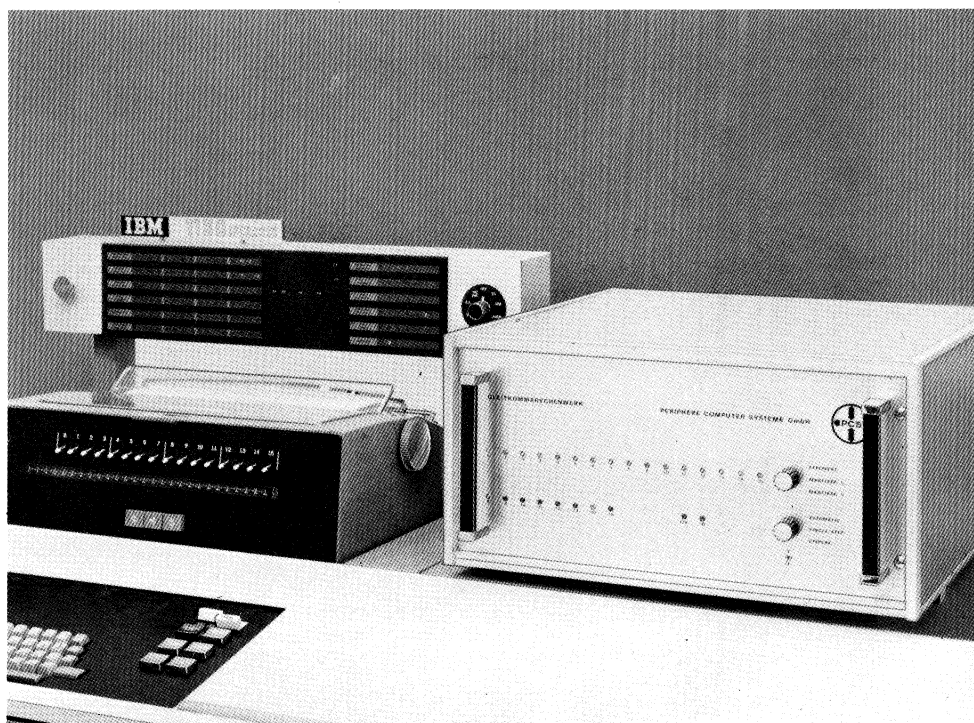


floating point hardware processor

a development of

PCS
PERIPHERE COMPUTER SYSTEME



for IBM 1130
and IBM 1800
with full
software support

FLOATING POINT HARDWARE - WHY?

What a pity!
You have, up to now, lost a lot of money and probably don't even realize it.
As a matter of fact, doing calculations by SOFTWARE means doing it the HARD way, doing it by HARDWARE means doing it the SOFT way.
If you are confronted with the problem of an increasing number of jobs for your IBM 1130 or 1800 (such as e.g. calculations of optical systems, chemical analyses, matrix-operations, Fourier transformations, simulations and so on) and it failed to pack more than 24 hours into a day, and in asking for a more powerful system you have been quoted a delivery time of some 6 months, and you are worried about how to get the finance and ... and ... and ...
Don't get a nervous breakdown! Our FPH will accelerate your computing time and you can switch off your system after 5 hours of run time instead of 24 hours previously. An error? No! Depending on the number of floating point operations, you can save 70 % to 92 % of the running time. That's saving money, right?
If you are already certain, that our FPH can help you to solve your problems — call our representative. If not, think it over and read the following paragraphs too.

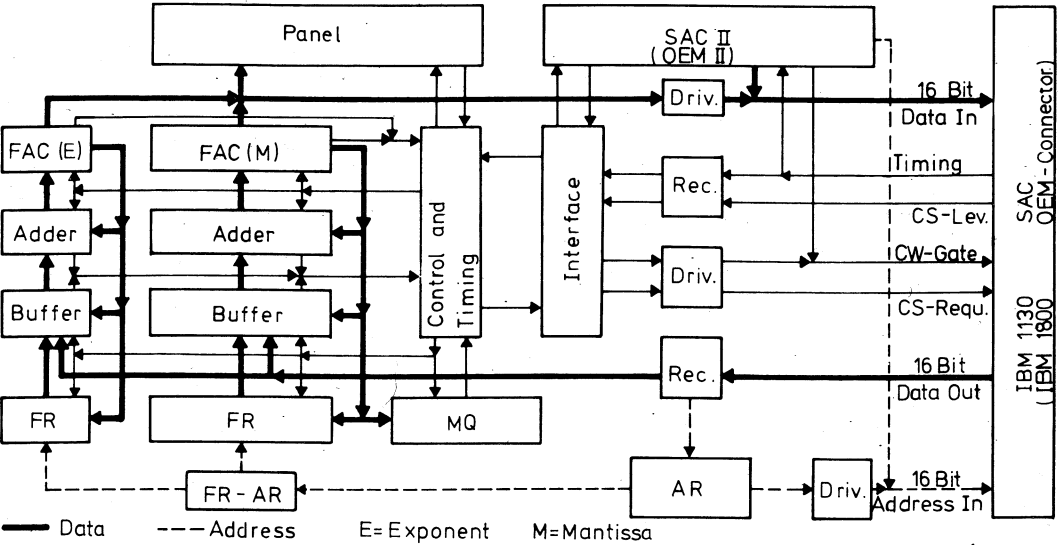


DIAGRAM OF THE FLOATING POINT HARDWARE

BASIC DESCRIPTION

The FPH interface structure allows making an easy connection to the SAC and IBM Multiplexer respectively. There is an SAC II option available also, allowing use of the SAC for other devices. No further steps are required to install the FPH.
DATA FLOW (see diagram):
The control and data lines are fed from the SAC via decoupling receivers into the FPH, thereby controlling and performing the program defined operations. 16 Fast Registers (FR) are provided for chained operations, allowing the storage of intermediate results which may be retrieved within 80 nsec. (Access time = 80 nsec.).

EXAMPLES FOR INSTRUCTIONS

| (altogether 39) | | | |
|-----------------|-------------------------|---|--|
| Instruction | Name of IBM-Subroutines | IBM-Software execution time in μ sec. | PCS-Hardware execution time in μ sec. (including operand transfer) |
| LOAD | FLD | 180 | 14 |
| STORE | FSTO | 180 | 18 |
| ADD | FADD | 460 | 16 |
| SUBTRACT | FSUB | 560 | 16 |
| MULTIPLY | EMPY | 790 | 25 |
| DIVIDE | EDIV | 2.060 | 30 |
| DIVIDE REVERSE | EDVR | 2.520 | 31 |
| SIGN REVERSE | SNR | 80 | 11 |

Since no Subprogram-Calls are necessary, the Hardware time applies directly to the execution of the operation in a FORTRAN-program. No Software set-up times are required.

40-BIT OPTION

The 40-bit option provides the possibility of achieving higher accuracy without extra care and without extensive modification to the Software (the 3 words are already reserved in the IBM Computer). Multiply and divide execution times are increased by about 25 %, but the higher accuracy provides new possibilities especially for handling big matrices.

TECHN. SPECIFICATIONS:

| | |
|--|---|
| Technology: | Fully integrated Modules in TTL-Logic. Wirewrapped frame. |
| Word length: | 32 bit for mantissa (40 bit available) 8 bit for exponent. |
| Fast register: | 16 words à 32 + 8 bit, 80 nsec. access time. |
| Instructions: | 39 different instructions. |
| Connection: | SAC of IBM 1130/OEM-Channel of IBM 1800. |
| Optional SAC II for IBM 1130, OEM II for IBM 1800: | For connection of other units (with priority control for SAC II and OEM II respectively). |
| Dimensions: | Depth 550 mm (21.66") Width 505 mm (19.88") Heigth 270 mm (10.63") |
| Dimensions: | Depth 380 mm (14.96") Heigth 221 mm (8.70") |
| Weight: | 28 kp (61 pounds) |
| Power requirements: | 115 ± 10 %, 220 ± 10 % VAC, 120 watts, 50-60 Hz |
| Cooling: | By air, 1 fan at the rear side. |
| Ambient temperature: | 0—50° C (32—122° F). |

SOFTWARE (IBM 1130)

The FPH may be used in standard 1130-Assembler and FORTRAN-programs. The operation codes in the Assembler may be defined directly in files of DC- definitions or in files of Makro-definitions. 3 other methods are possible in the Assembler as well as in FORTRAN such as:

- Use of altered Arithmetic Subroutines (e.g. FADD) provides an acceleration by a factor of 2–3.
- Use of a Postcompiler, which looks into programs in DSF format and changes Subroutine-Calls for FP-operations into the corresponding in-line codes.
- Additional use of a changed FORTRAN-Compiler; here the compiler already generates in-lines codes. 3 FORTRAN-Phases have been changed.

Additionally all Function Subroutines (like FSIN- FEXP) are provided in a new form, using the PCS-Hardware in an optimal manner. These routines are about 8 times faster than the original ones.

Some routines like MINV from the SSP-Package have also been modified – e.g. Matrix inversions, compared to the new ASM program, are performed about 15 times faster.

SOFTWARE (IBM 1800)

The same Software, with the exception of the modified FORTRAN-Compiler, is available for the IBM 1800:

- the changed Arithmetic Subroutines
- the changed Function Subroutines
- the Postcompiler for TSX
- the Postcompiler for MPX for use of the FPH on one Level.

The PCS-FLOATING POINT HARDWARE has been developed especially for the IBM 1130 and 1800. Our software-packages are well tested and field proven. Please, ask for our reference list.



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Representative: