IBM Maintenance Library

CONTROL MODULE

3340-A2

S N

MLM

VOL. RO1	VOL. RO2	VOL. RO3	VOL. RO4	VOL. RO5	VOL. RO6
INDEX MLX LGND **START** FSI MSG SENSE OLT OPER	MICRO	PANEL SSW* CTL-I DATA	MICFL	DEV-I ACC R/W	DM RPI PWR LOC INST

Volumes RO1, 2, 3, and 4 accompany only Control Modules (A2).

** This section is only with Control Modules that have the string switch feature installed.*

SATELLITE MODULE

3340-Bx

S N

MLM

VOL. RO5	VOL. RO6
DEV-I ACC R/W	DM RPI PWR LOC INST

Volumes RO5 and RO6 accompany every Control Module (A2) and every Satellite Module (B1 or B2). (One set per serial numbered frame.) To ensure proper documentation level, use the volume that goes with the module you are working on.

3340 Disk Storage

BM0010	2747523	440200	440203	440218	440224
Seq. 1 of 2	Part No. ( )	25 Jun 73	2 Nov 73	5 Aug 74	15 Dec 75

PREFACE

MAINTENANCE LIBRARY ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3340 Maintenance Library can be ordered from the San Jose plant by using the *Wiring Diagram/Logic Page Request* (Order No. 120-1679). In the columns headed "Logic Page", enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

Example:

Sequence number — Part number — Latest EC number

3340	**DW0010** Seq. 1 of 2	**2747749** Part No. ( )	**440203** 2 Nov 73	**440204** 21 Dec 73	**440205** 28 Jan 74			

Sheet number

This manual was prepared by the IBM General Products Division, Product Publications, Department G24, San Jose, California 95193.

3340	**BM0010** Seq. 2 of 2	**2747523** Part No. ( )	**440200** 25 Jun 73	440203 2 Nov 73	**440218** 5 Aug 74	**440224** 15 Dec 75		

SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment.

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it: for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

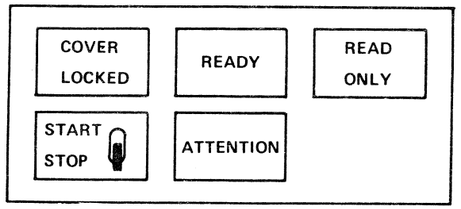
1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)
2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

PANEL CONTENTS

Note: Certain 3340 subsystems have a 3344 drive attached. The 3344 operator panel is not the same as the 3340 operator panel. See the PANEL section in the 3344 MLM. (3344 documentation will be available in May 1976).

3340 OPERATOR PANEL



READY Indicator

Lights when the data module is properly inserted and ready for operation.

START/STOP Switch

With the switch in the start position, the cover is locked, the data module is loaded and the heads are moved to track 0, provided that:

1. The drive power is on.
2. The data module is in place.
3. The cover is closed and latched.

When the switch is placed in the stop position, the data module is unloaded and the cover is unlocked. The data module will not unload while the system is communicating with the drive or when an Attention is pending.

READ ONLY Indicator

Lights when the write function is inhibited after the data module is loaded. Write is inhibited by rotating the read only inset in the data module handle.

COVER LOCKED Indicator

Lights when the drive cover is locked.

ATTENTION Pushbutton

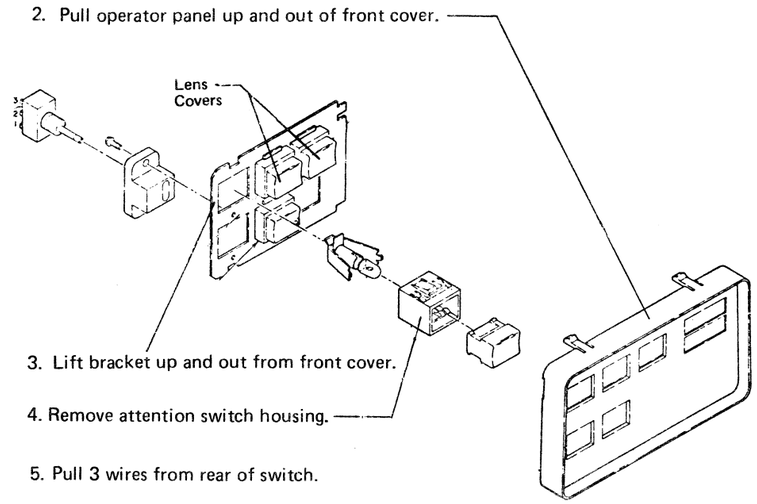
Operating this pushbutton causes the drive to perform a rezero operation:

1. Read/Write heads are moved to track 0.
2. DM (data module) Attention is signaled to the controller.

OPERATOR PANEL SWITCH REPLACEMENT

Removal

1. Remove all lens covers.
2. Pull operator panel up and out of front cover.
3. Lift bracket up and out from front cover.
4. Remove attention switch housing.
5. Pull 3 wires from rear of switch.
6. Loosen lock nut on switch.
   Unscrew and remove switch from housing.

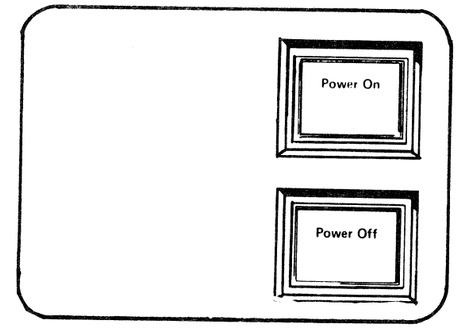


Replacement

Replacement is the reverse of removal.

3340 POWER PANEL (Standard)

A2 Module



POWER ON Switch

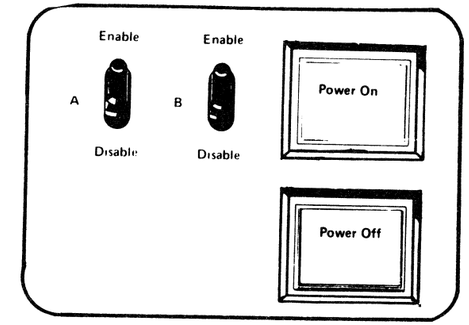
Operation of the Power-on switch allows ac power to be applied to the module provided subsystem power is present. The switch is bypassed by the subsystem sequencing controls during a subsystem power-up operation.

POWER OFF Switch

Operation of the Power-off switch removes ac power from the module when subsystem power is up. During a subsystem power-down operation, this switch is bypassed and power is removed by the subsystem sequencing controls.

3340 POWER PANEL (String Switch)

A2 Module

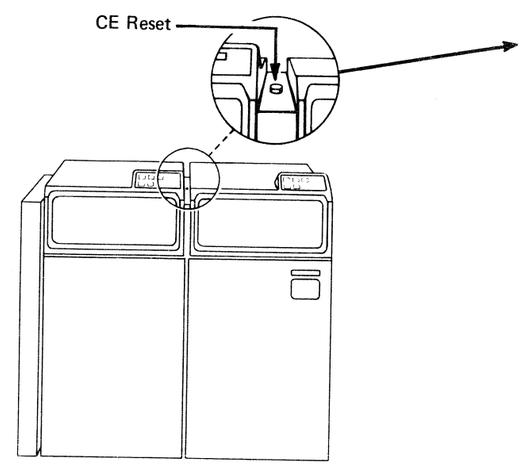


The functions of this power panel are the same as the standard machine (left) except for:

ENABLE/DISABLE Switches

The Enable/Disable switches (A or B) can be used to dedicate the 3340-A2 and associated drives to a single interface. Interlocking is provided.

*Machines without the String Switch feature do not have these switches.



IBM 3340-A2

CE Reset switch

This control is located on the top surface of the frame between the drive covers. See LOC 2 and LOC 12, or PANEL 10. When a drive is in CE mode, CE RESET resets:

1. Check and Attention conditions in the drive
2. Difference Counter
3. Head Address Register
4. Cylinder Register
5. Target Register
6. Cover Locked Latch

When the drive is not in CE Mode, the CE Reset switch:

- Resets a DM Sequencer error if it is in State 0, and initiates another 10 second retry to unload the data module. See Note 1, DM 100 for detailed theory on use of CE Reset for DM Sequence errors.
- Resets the Cover Locked Latch. See Note 4, DM 120 for detailed description of Cover Locked Latch.

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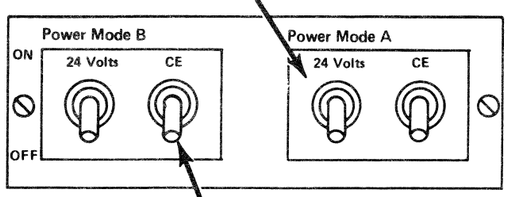
CE CONTROLS

The CE controls allow:

- Communication with the storage control to initiate and control microdiagnostics from the 3340. (See MICRO 10 and 11.)
- Placing a drive in CE Mode.
- Removing the 3340 subsystem from system power sequencing.
- Removing +24 V power from an individual drive.
- Resetting of various drive circuits.

+24 V POWER switches

One for each drive, removes +24 Vdc power from the DM sequence microswitches and edge connectors to allow servicing one drive while the other is in operation if the CE Mode switch is on.



CE MODE switch

One CE Mode Switch for each drive allows a drive to be put in CE mode so it can be selected when a Select Tag accompanied by the Service Select bit on Bus Out is present.

Program Control display and Data display

Allows communication from the storage control to the 3340. For a description of PROGRAM CONTROL displays and their corresponding DATA displays, see MICRO 10 and 11.

Data Entry switches

Used in conjunction with Execute Switch to send information to the storage control. Examples:
1. Microdiagnostic routine and test numbers.
2. Test parameters.
3. Running options.

POWER MODE switch

1. Remote Drive Power sequencing under system control.
2. Local removes the 3340 subsystem from normal system power sequencing. Allows powering down the 3340 subsystem without affecting system operation. Prevents the system from powering up the 3340 during maintenance activity.

Parity Check

CTL-I Tag Bus lamp

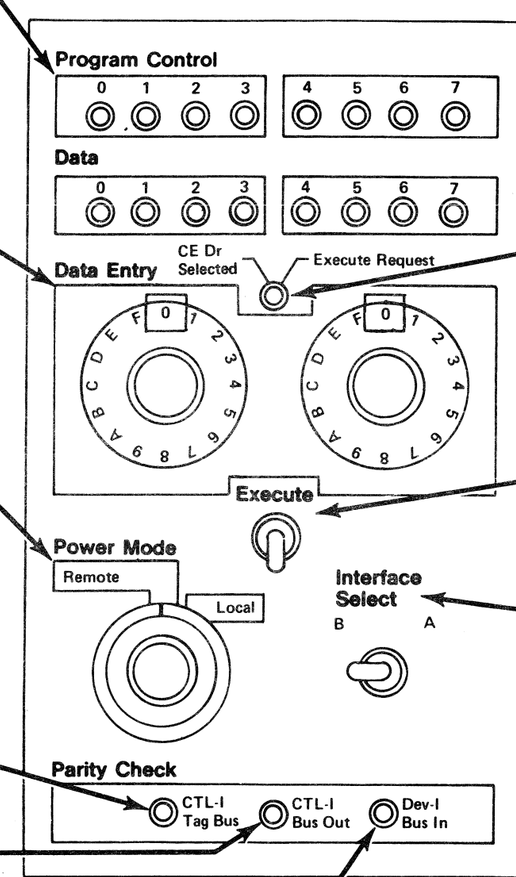
Turned on by control interface tag bus parity error. Reset by execute switch or by power on/off sequence.

CTL-I Bus Out lamp

Turned on by control bus out parity error. Reset by execute switch or by power on/off sequence.

Dev-I Bus In lamp

Turned on by device bus in parity error. Reset by execute switch or by power on/off sequence.



CE Dr Selected/Execute Request lamp

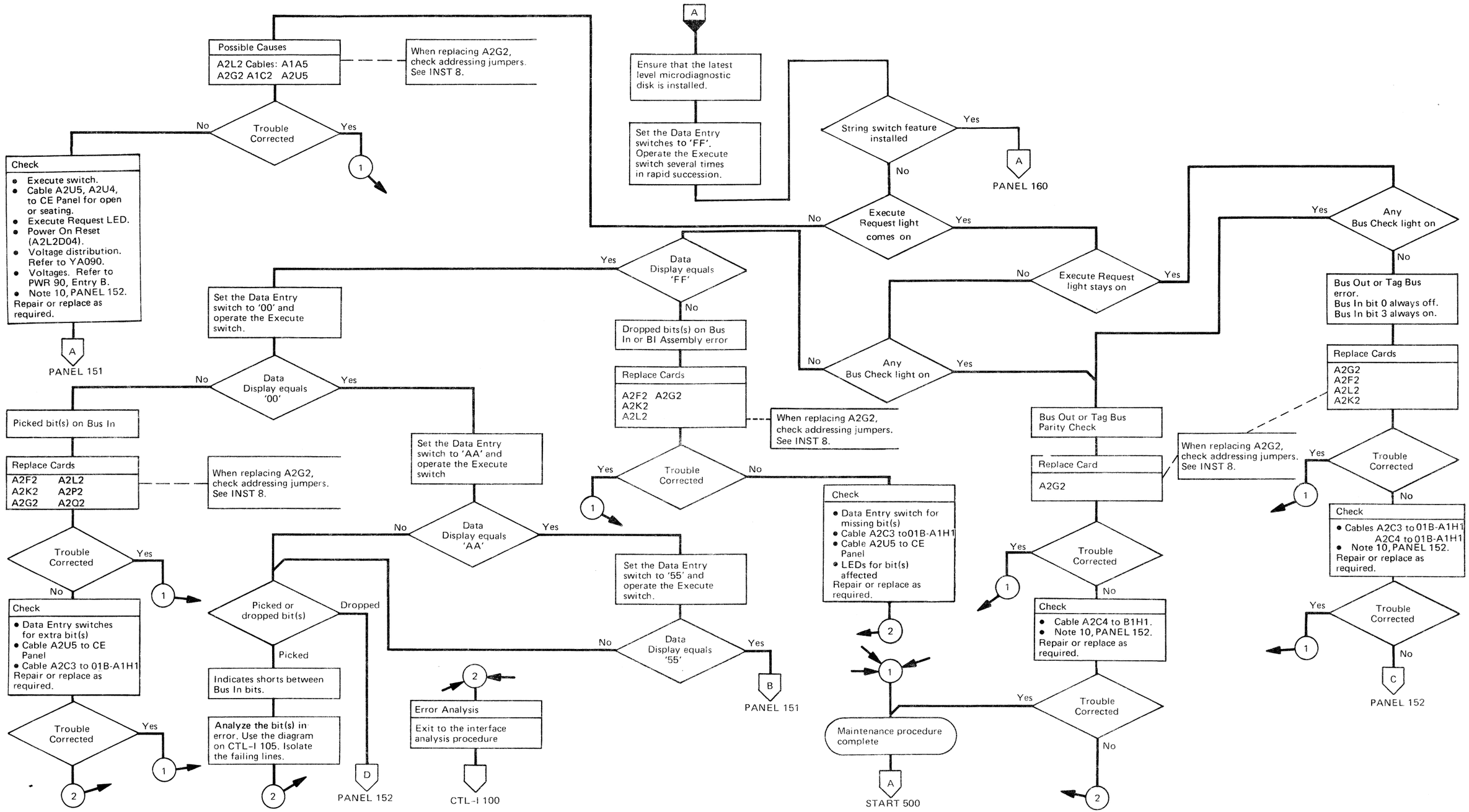
Turns on when execute switch is operated. Reset when operation requested by data entry switches is complete and program control display is set. In CE mode, the lamp turns on when a drive is selected.

Execute switch

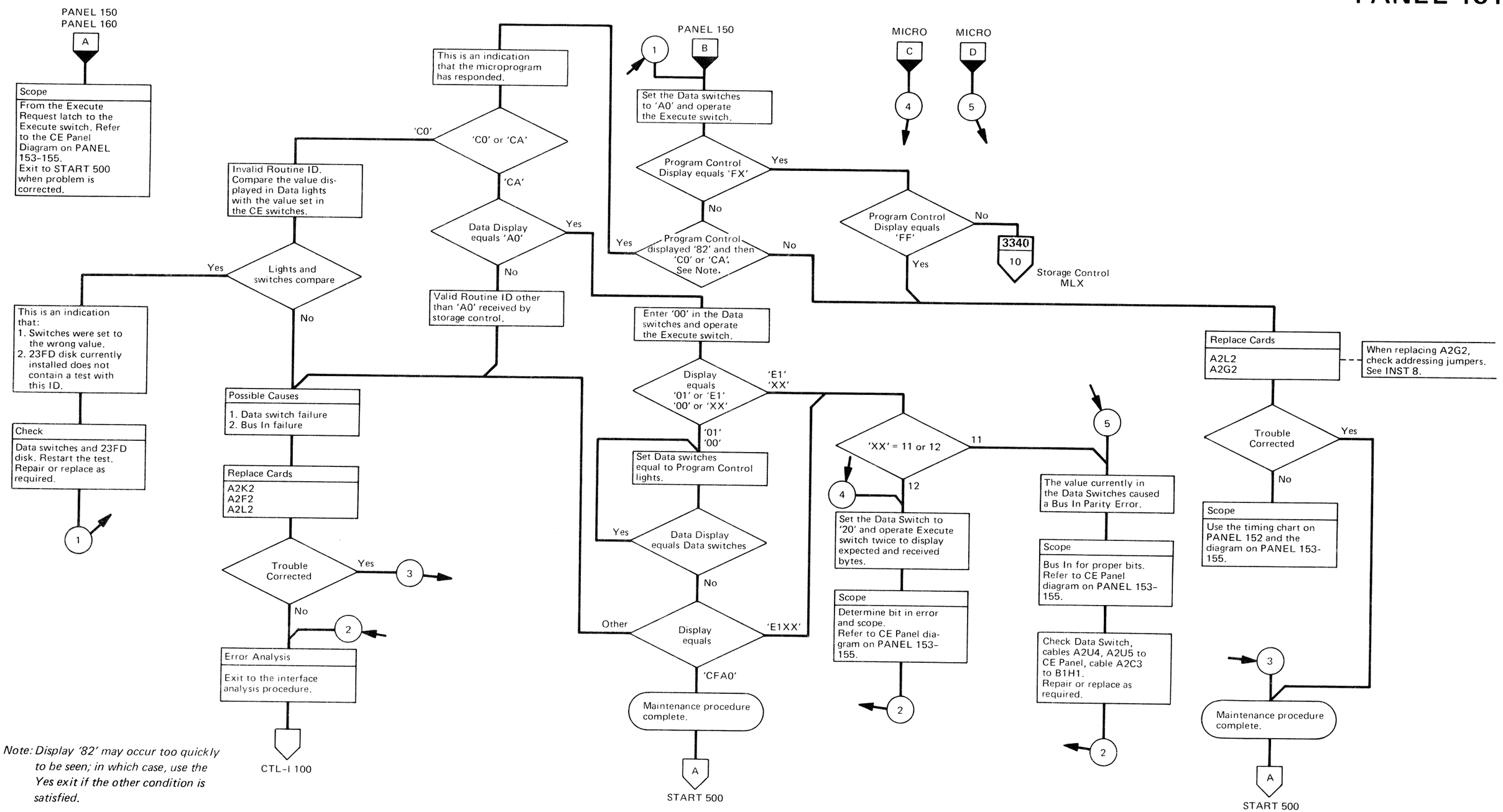
1. Causes control program to read data entry switches.
2. Turns on Execute Request light.
3. Resets bus checks and bus check lights.

Interface Select switch

Selects control interface A or B for CE Panel operation (String Switch Feature).



3340	BN0020 Seq 2 of 2	2747413 Part No. (1)	See EC History	440224 15 Dec 75	440227 14 Sept 76	440241 30 Oct 78			



Note: Display '82' may occur too quickly to be seen; in which case, use the Yes exit if the other condition is satisfied.

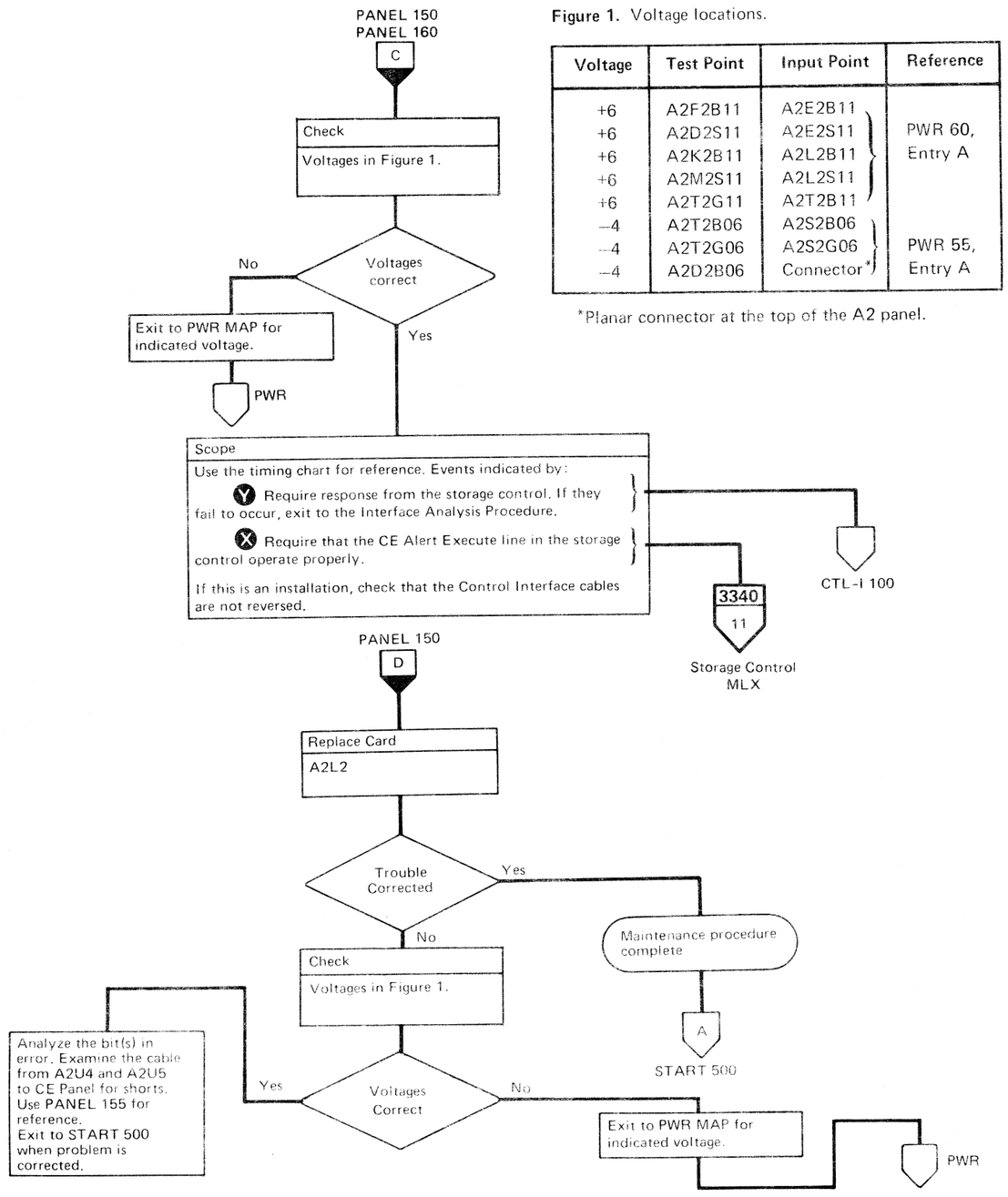
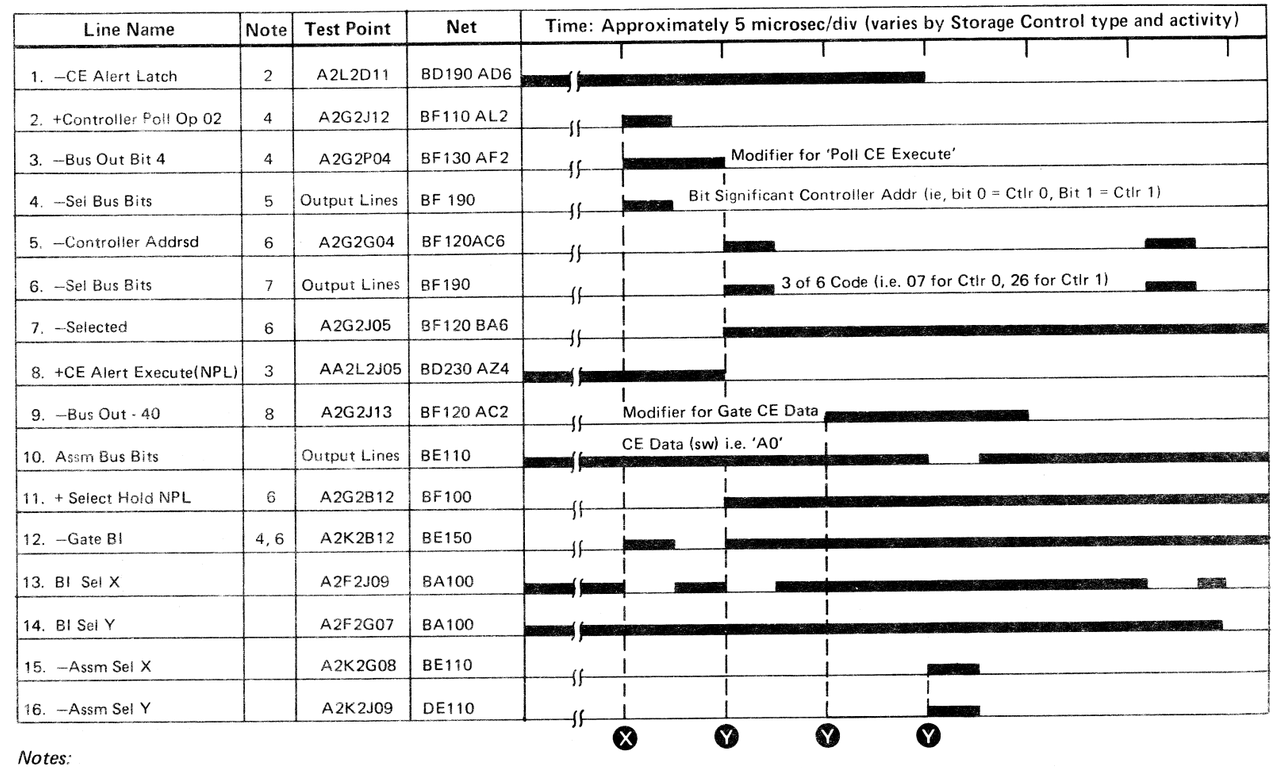


Figure 1. Voltage locations.

Voltage	Test Point	Input Point	Reference
+6	A2F2B11	A2E2B11	PWR 60, Entry A
+6	A2D2S11	A2E2S11	
+6	A2K2B11	A2L2B11	
+6	A2M2S11	A2L2S11	
+6	A2T2G11	A2T2B11	
–4	A2T2B06	A2S2B06	PWR 55, Entry A
–4	A2T2G06	A2S2G06	
–4	A2D2B06	Connector*	

*Planar connector at the top of the A2 panel.

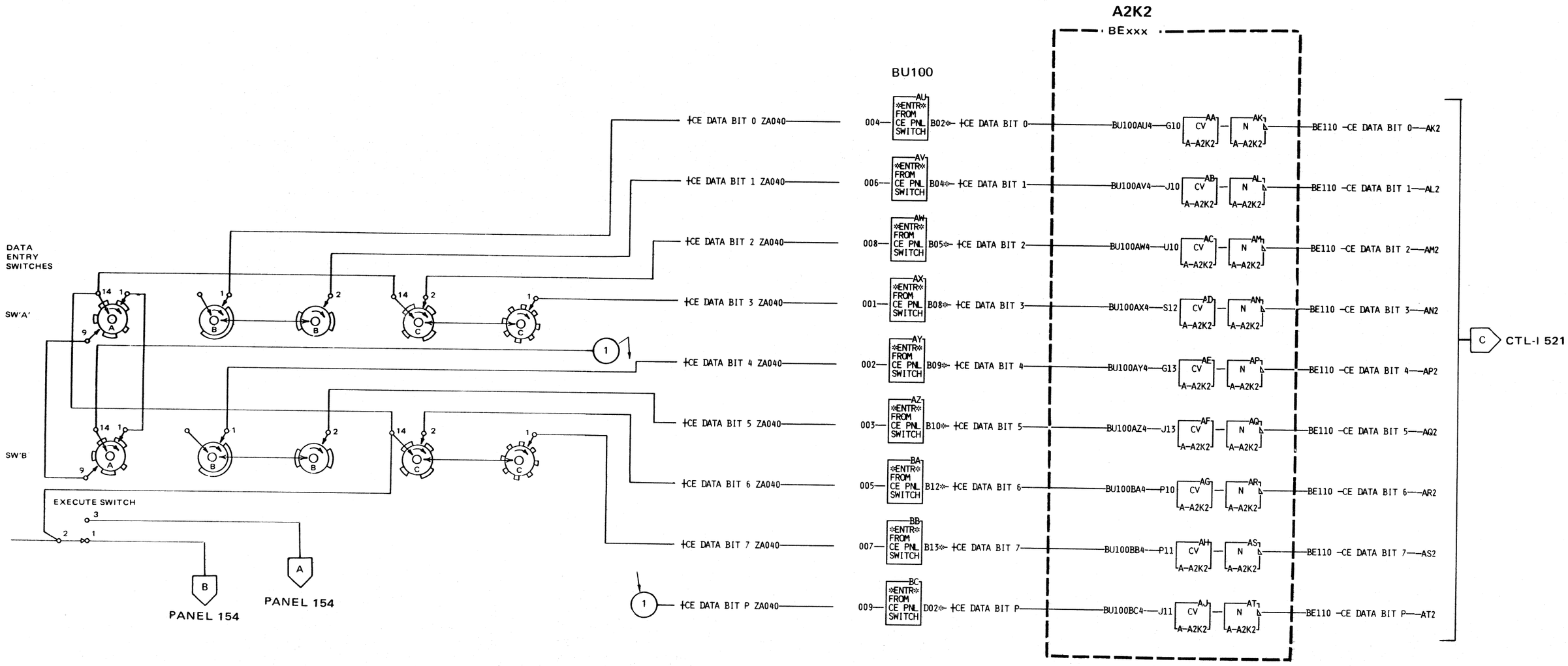


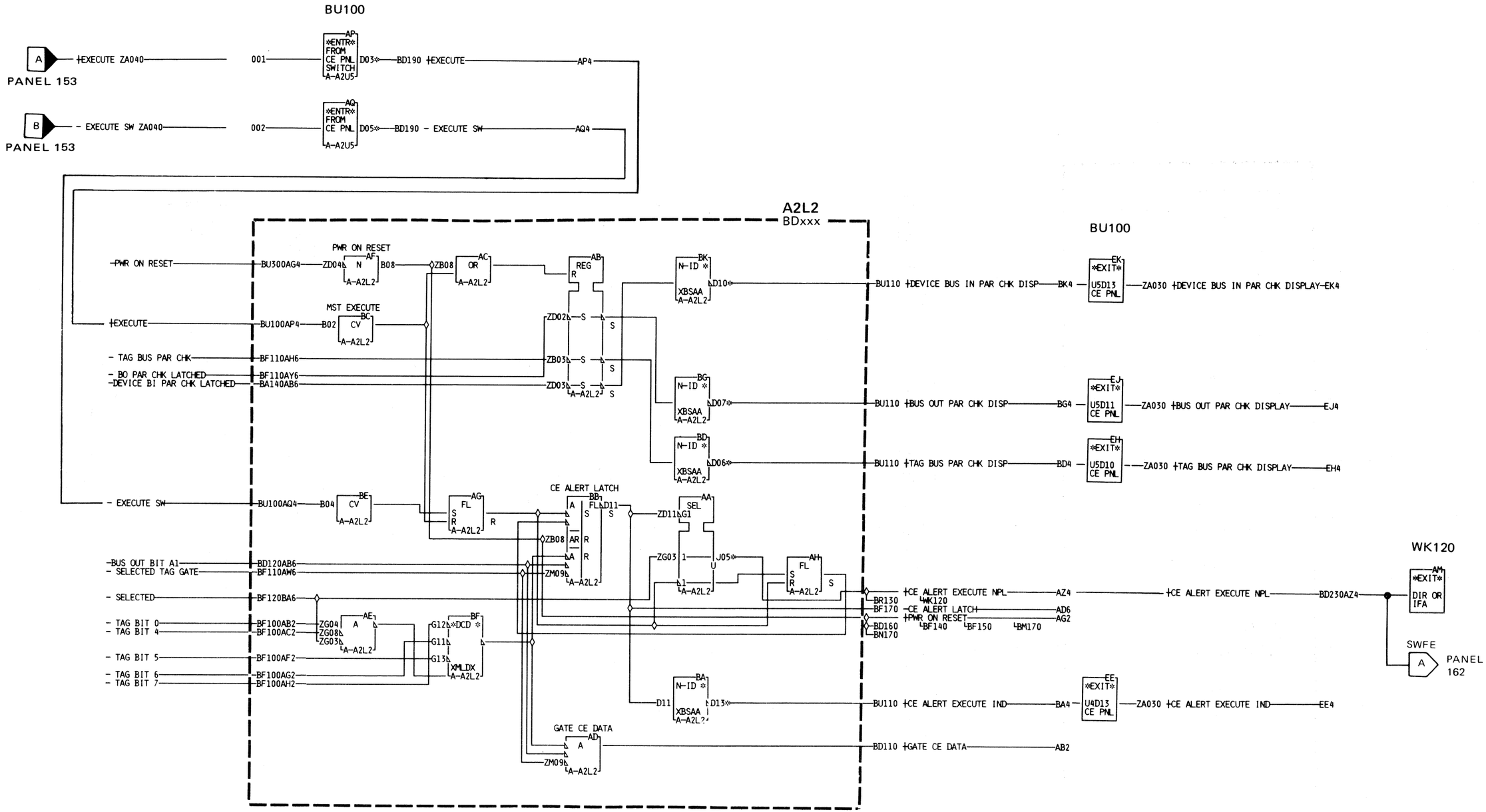
Notes:

1. *Refer to the OPER section for complete Bus and Tag descriptions.*
2. *Execute Request switch, when operated, sets CE Alert Latch. If it fails to set, check the switch cables to CE Panel and latch on A2L2.*
3. *When the controller is not selected, CE Alert Execute (NPL) becomes active. Check Select Hold and the selected latch.*
4. *Storage Control should respond with Controller Poll Op 02 with a Bus Out value hex 08. If not, check interface cables or suspect Storage Control problem.*
5. *The controller responds with a bit-significant physical address, that is, bit 0 equals Controller 0, bit 1 equals Controller 1. Check from Select Bus to controller interface to be sure it happens correctly. Check Gate B1 and B1 Sel and Assm Sel lines.*
6. *The Storage Control then selects the controller based on the information received above. Check Bus Out and Tag Bus if it does not.*
7. *The controller responds to selection by placing a 3-of-6 bit code on Bus In. Bus In equals 07 for Controller 0 and 26 for Controller 1. If it fails to do so, check Gate B1, B1 Sel, and Assm Sel lines.*
8. *The Storage Control then must read CE data from the switches. Since the decode for this function is imbedded on a logic card, check lines 1, 9, 15, 16, and be sure that the Assm Bus bits equal the CE switch setting. CE Alert Latch (line 1) is reset by Gate CE Data Decode.*
9. *Note that Select Latch comes on and stays on throughout the timing chart.*
10. *Where there is more than one controller on the interface and the following combination of conditions exist –*
    a. *The Execute Request light is on continuously on the controller with the higher address as a result of having operated the Execute Request switch.*
    b. *No apparent Execute Request light on the controller with the lower address when the Execute Request switch is operated.*

    – replace cards in the controller with the lower address.

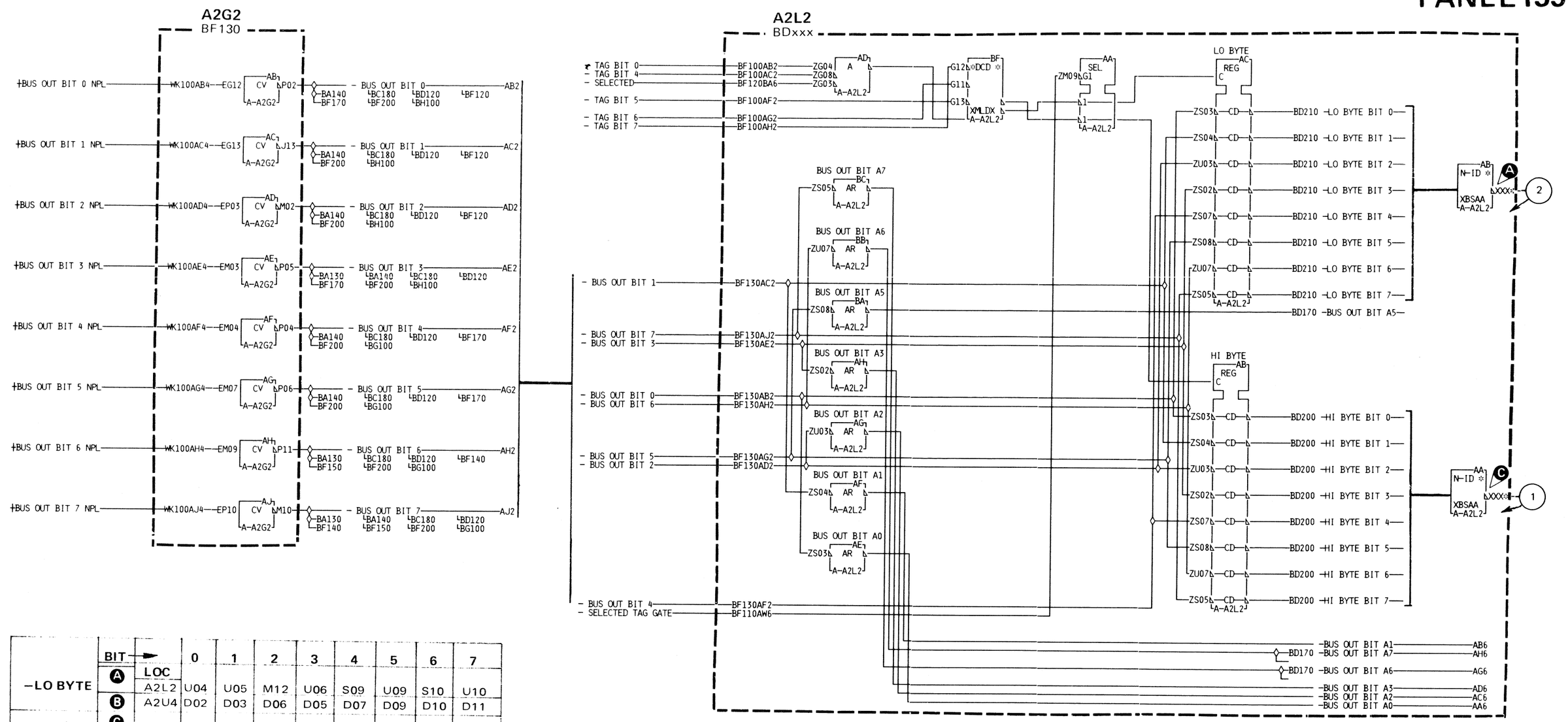
Basic	*A2G2*		
SWFE	*A2D2*	–	*Interface A*
	A2E2	–	*Interface B*





3340

BN0154	2747415	440200	440202	440203	440213			
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	13 May 74			



	BIT →		0	1	2	3	4	5	6	7
		LOC								
-LO BYTE	A	A2L2	U04	U05	M12	U06	S09	U09	S10	U10
	B	A2U4	D02	D03	D06	D05	D07	D09	D10	D11
-HI BYTE	C	A2L2	U11	B05	U02	P12	S13	U12	U13	S12
	D	A2U4	B02	B04	B05	B08	B09	B10	B12	B13

CTL–I CONTENTS

BQ0001	2747417	See	440223	440224	440227			
Seq. 1 of 2	Part No. (1)	EC History	14 Mar 75	15 Dec 75	14 Sept 76			

PHILOSOPHY OF INTERFACE ANALYSIS

If the String Switch feature is installed, go to CTL-I 110.

The recommended approach to interface problems is to replace the designated replaceable unit in the controller and determine if the problem is corrected. The replacements are normally made prior to coming to this page. When successful, this method causes a minimum impact on system operation.

If further action is required, go to the interface checkout procedure for the storage control. If the problem is not resolved, return here.

3830

Execute the CTL Interface Bringup Program. Refer to MICFL 1500 for operation instructions and to CTL-I 101 to CTL-I 105 for scope procedures and diagrams.

370/115-125

Execute the CTL Interface Bringup Program, routine BF. Refer to MICFL 1500 for operation instructions and to CTL-I 101 to CTL-I 105 for scope procedures and diagrams.

370/135

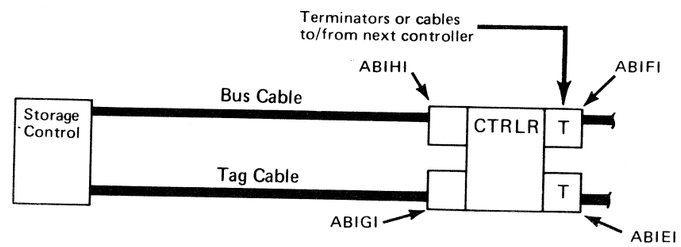
The 370/135 Interface test provides the same function as the CTL Interface Bringup Program. Refer to CTL-I 101 to CTL-I 105 for scope procedures and diagrams.

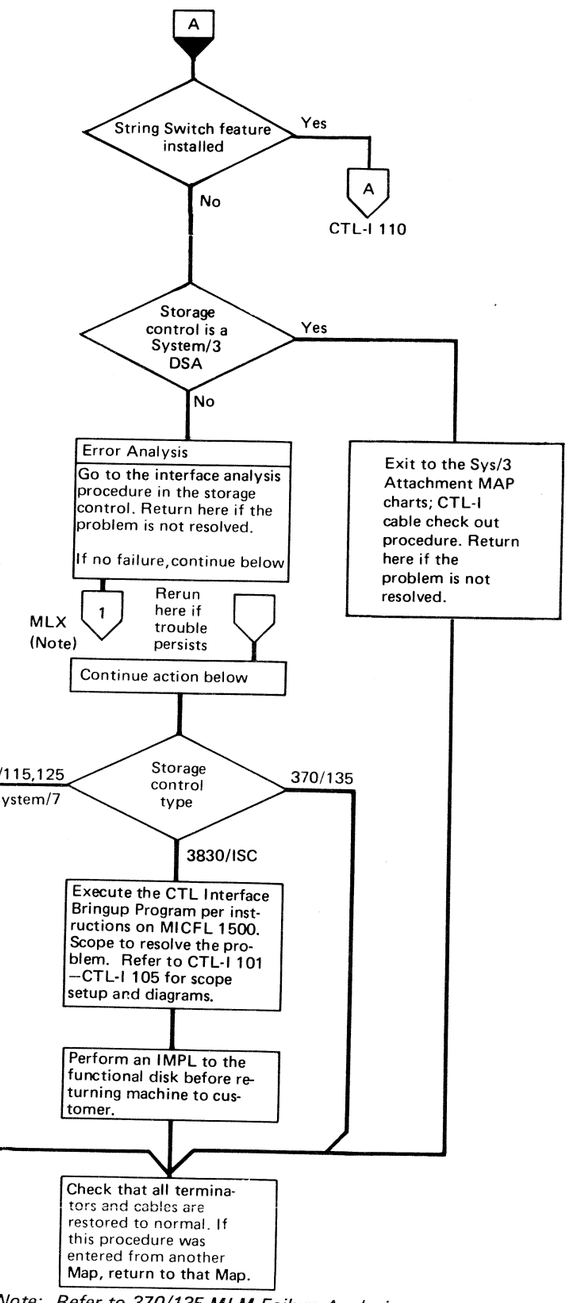
HINTS

1. If more than one controller is attached to the interface, install the terminators in the first controller and check that it functions normally; then proceed to the next controller and continue until all units function normally.
2. Note that the lines listed below require a back panel connection to propagate the signal to the next controller. If a connector is loose at the A2 board in any controller, all controllers may appear to fail. Check that the following connectors in all controllers are securely seated.

Bus Out Bit 3	A2C4
Bus Out Bit 4	A2C4
Tag Bus Bit 6	A2C5
Tag Bus Bit P	A2C5
Bus In Bit 3	A2C3
Bus In Bit 4	A2C3
Error Alert	A2C2
Index Alert	A2C2

3. For new installations, location changes, or whenever cables are removed, the interface cables may be transposed. Verify the cabling. *(See CTL-I 107 for cable checking hints.)*





Note: Refer to 370/135 MLM Failure Analysis page IFA–312.

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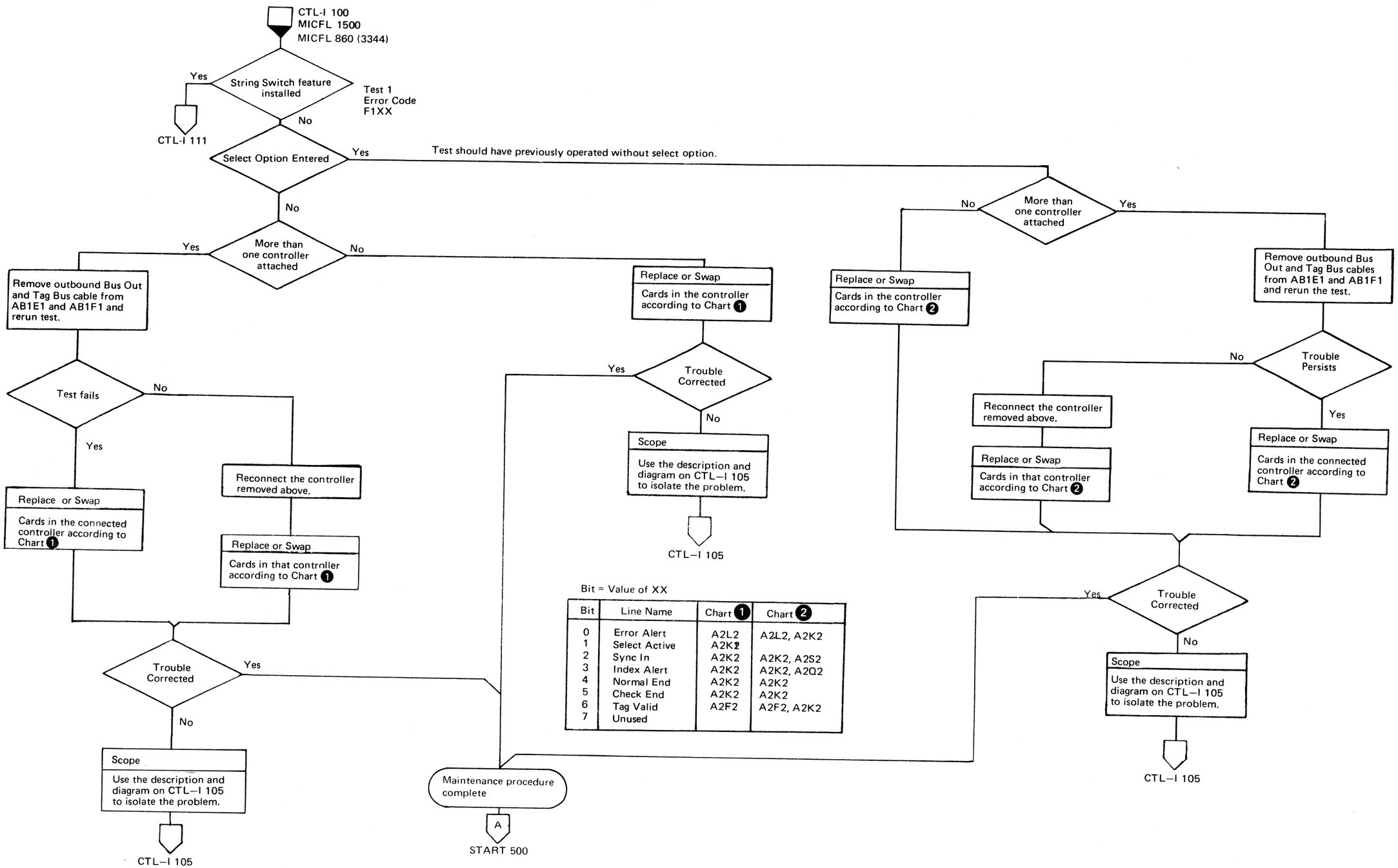
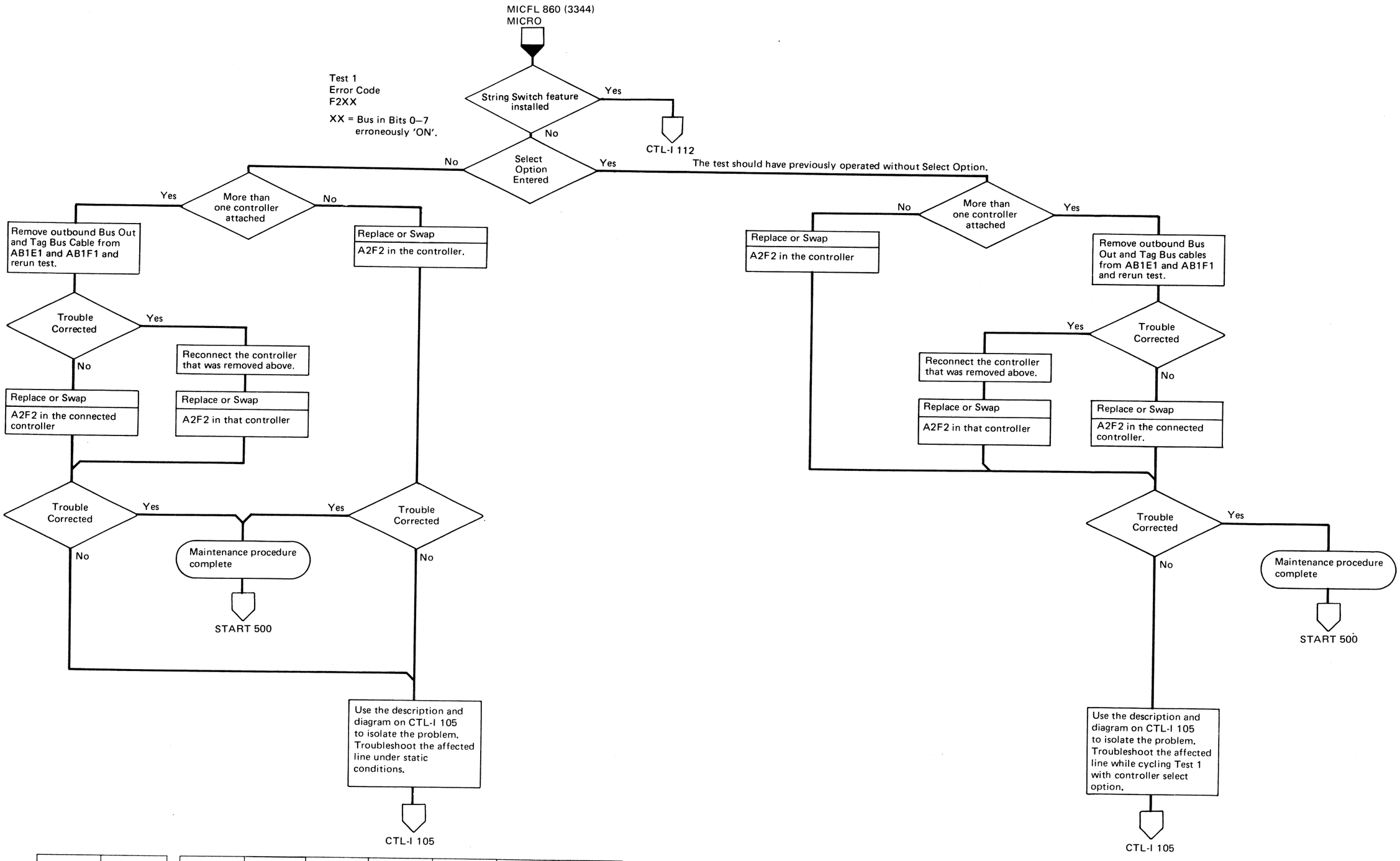


Bit = Value of XX

Bit	Line Name	Chart 1	Chart 2
0	Error Alert	A2L2	A2L2, A2K2
1	Select Active	A2K2	
2	Sync In	A2K2	A2K2, A2S2
3	Index Alert	A2K2	A2K2, A2Q2
4	Normal End	A2K2	A2K2
5	Check End	A2K2	A2K2
6	Tag Valid	A2F2	A2F2, A2K2
7	Unused		



INTERFACE ANALYSIS

Test 2 is an exerciser. Values selected by the CE are cycled on Bus Out or the Tag Bus and then scoped. Below are scope pictures as they should appear while cycling the test. Parameter 3 bits were set to 1s (Tag Bus = '8F' or Bus Out = 'FF') and parameter 4 bits were set to 0s.

If these points are correct and parity errors are present, continue scoping using the ALDs (BF100 for Tag Bus, BF130 for Bus Out).

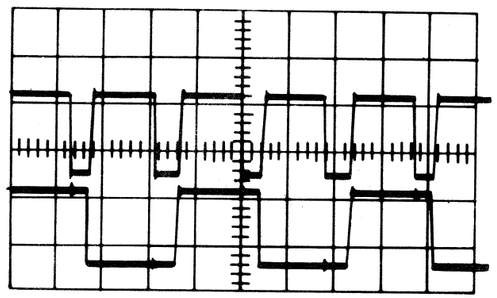
The scope setup for all photos except Number 4 is:

Vertical: 0.2 volts/div X10 probes
Horizontal: 5 us/div
(Timer may vary by storage control type; 3830 is shown)
Internal Sync.

1.

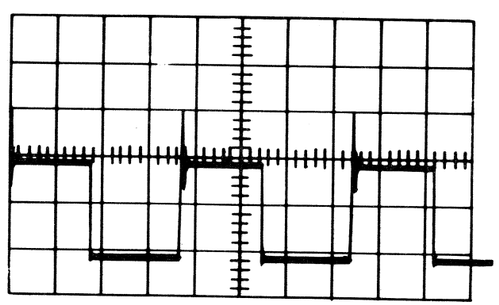
+Tag Gate NPL A2G2J11 (BF130)

+Tag Bus Bit X NPL (BF100)



TAG BUS	
Bit 0	A2G2D13
1	Not used
2	Not used
3	Not used
4	A2G2G02
5	A2G2B03
6	A2G2B05
7	A2G2D04
P	A2G2B04

2.

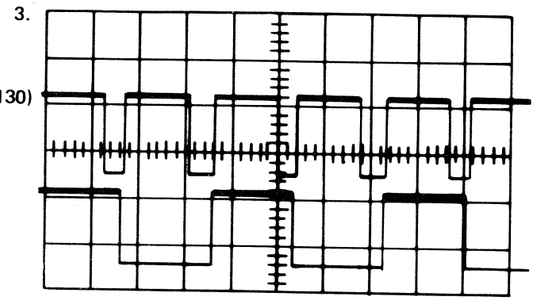


+Bus Out or Tag Bus line which is unterminated. Note the increased amplitude and the ringing on the rise of the pulse.

3.

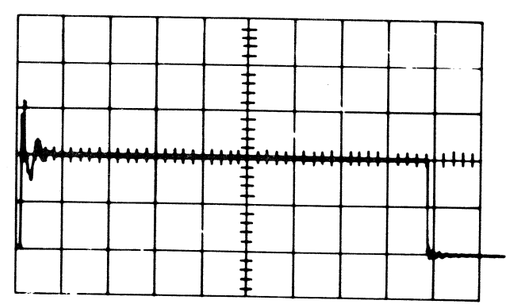
+Tag Gate NPL A2G2J11 (BF130)

+Bus Out Bit X NPL (BF130)



BUS OUT	
Bit 0	A2G2G12
1	A2G2G13
2	A2G2P03
3	A2G2M03
4	A2G2M04
5	A2G2M07
6	A2G2M09
7	A2G2P10
P	A2G2P09

4.



Same as number 2 except that time was changed to 1 us/div to illustrate the ringing on the leading edge.

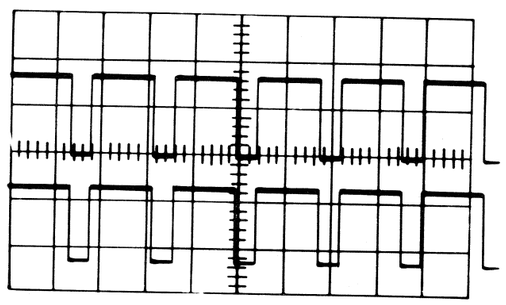
Test 3 exercises:
Select Hold
Tag Gate
Recycle
Below are scope pictures as they should appear while looping the test.

Scope setup:

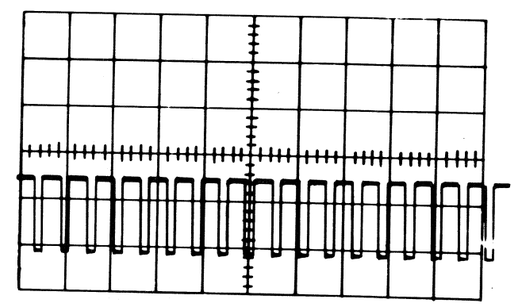
Vertical: 0.2 volts/div
X10 probes
Horizontal: 5 us/div
Time may vary by storage control type (3830 shown).
Sync: Internal

+Tag Gate A2G2J11 (BF130)

+Select Hold A2G2B12 (BF100)



+Recycle A2G2U12 (BF160)

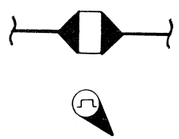


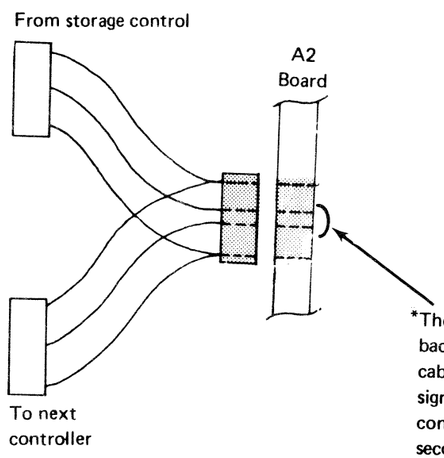
BQ0103 Seq. 2 of 2	2747419 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74		

INTERFACE ANALYSIS

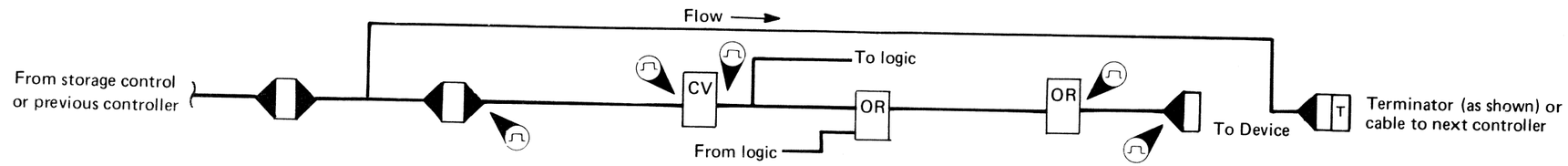
All interface line points shown are NPL levels (nominal ground to +3V) except the output of outbound convert card which is MST.

Terminator part number : 2282675

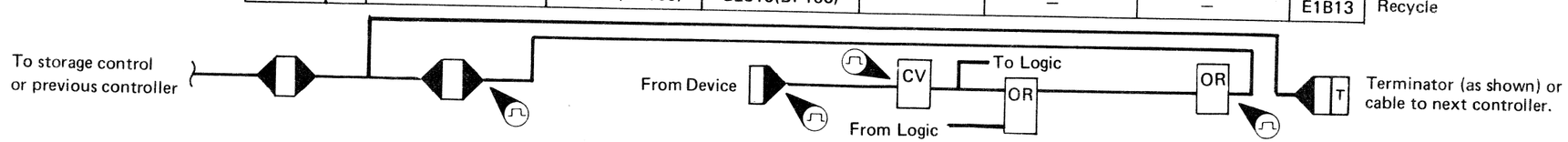




*These pins are tied together on the back of the board. Therefore, if this cable is loose in the first controller, signals do not reach the second controller. If it is loose in the second controller, the lines appear unterminated in the first controller.



Outbound lines		B1		A2	A2	A2		A2	A2	B1	
Bus Out bit	0	H1B04		C4D05(WK100)	G2G12(BF130)	G2P02(BF130)		F2P10(BA110)	V5B02(BU200)	F1B04	0 Bus Out bit
	1	H1D05		C4B05(WK100)	G2G13(BF130)	G2J13(BF130)		F2P12(BA110)	V5B04(BU200)	F1D05	1
	2	H1B06		C4D06(WK100)	G2P03(BF130)	G2M02(BF130)		F2U02(BA110)	V5B05(BU200)	F1B06	2
	3	H1D08		C4B08/B09(WK100)*	G2M03(BF130	G2P05(BF130)		F2S03(BA110)	V5B06(BU200)	F1D08	3
	4	H1B09		C4D09/D10(WK100)*	G2M04(BF130)	G2P04(BF130)		F2S12(BA110)	V5B08(BU200)	F1B09	4
	5	H1D10		C4B10(WK100)	G2M07(BF130)	G2P06(BF130)		F2U12(BA110)	V5B09(BU200)	F1D10	5
	6	H1B11		C4D11(WK100)	G2M09(BF130)	G2P11(BF130)		F2U05(BA110)	V5B10(BU200)	F1B11	6
	7	H1D12		C4B12(WK100)	G2P10(BF130)	G2M10(BF130)		F2U09(BA110)	V5B12(BU200)	F1D12	7
	P	H1D03		C4B02(WK100)	G2P09(BF130)	–		F2M07(BA110)	V5B13(BU200)	F1D03	P
Sync Out		H1B13		C4D13(WK110)	G2B13(BF100)	G2D12(BF100)		–	–	F1B13	Sync Out
Tag Bus bit	0	G1D03		C5B02(WK110)	G2D13(BF100)	G2J03(BF100)		–	–	E1D03	0 Tag Bus bit
	4	G1D05		C5B05(WK110)	G2G02(BF100)	G2J02(BF100)		–	–	E1D05	4
	5	G1B04		C5D05(WK110)	G2B03(BF100)	G2B02(BF100)		L2J10(BD220)	V5D02(BU200)	E1B04	5
	6	G1D08		C5B08/B09(WK110)*	G2B05(BF100)	G2D07(BF100)		L2P03(BD220)	V5D03(BU200)	E1D08	6
	7	G1B06		C5D06(WK110)	G2D04(BF100)	G2B07(BF100)		L2J12((BD220)	V5D05(BU200)	E1B06	7
	P	G1B09		C5D09/D10(WK110)*	G2B04(BF100)	–		L2J04(BD220)	V5D06(BU200)	E1B09	P
Tag Gate		G1D10		C5B10(WK110)	G2J11(BF130)	–		L2J02(BD230)	V5D07(BU200)	E1D10	Tag Gate
Response		G1D12		C5B12(WK100)	G2S03(BF160)	–		–	–	E1D12	Response
Select Hold		G1B11		C5D11(WK110)	G2B12(BF100)	–		L2M03(BD230)	V5D09(BU200)	E1B11	Select Hold
Recycle		G1B13		C5D13(WK110)	G2U12(BF160)	G2S10(BF160)		–	–	E1B13	Recycle



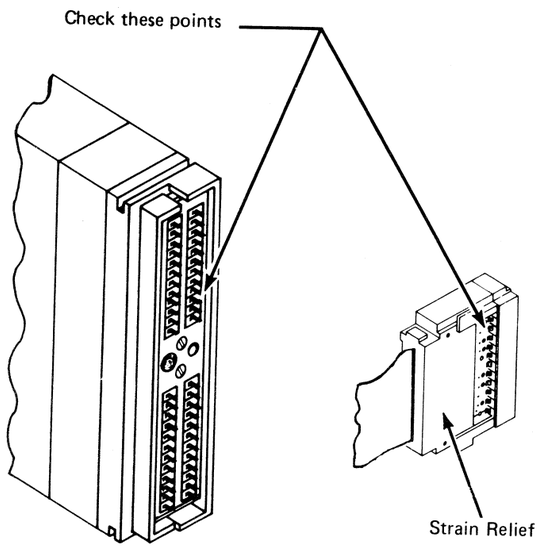
Inbound lines		B1		A2		A2		A2		A2	B1	
Bus In bit	0	H1G04		C3D05(WK120)		V4B02(BU300)		F2B10(BA160)		F2D06(BA150)	F1G04	0 Bus In bit
	1	H1J05		C3B05(WK120)		V4B04(BU300)		F2B07(BA160)		F2B03(BA150)	F1J05	1
	2	H1G06		C3D06(WK120)		V4B05(BU300)		F2G03(BA160)		F2D10(BA150)	F1G06	2
	3	H1J08		C3B08/B09(WK120)*		V4B06(BU300)		F2B09(BA160)		F2D09(BA150)	F1J08	3
	4	H1G09		C3D09/D10(WK120)*		V4B08(BU300)		F2G12(BA160)		F2J02(BA150)	F1G09	4
	5	H1J10		C3B10(WK120)		V4B09(BU300)		F2J04(BA160)		F2J07(BA150)	F1J10	5
	6	H1G11		C3D11(WK120)		V4B10(BU300)		F2G05(BA160)		F2J11(BA150)	F1G11	6
	7	H1J12		C3B12(WK120)		V4B12(BU300)		F2G13(BA160)		F2J03(BA150)	F1J12	7
	P	H1J03		C3B02(WK120)		V4B13(BU300)		F2J13(BA160)		F2J12(BA150)	F1J03	P
Sync In		H1G13		C3D13(WK120)		–		–		K2D04(BE160)	F1G13	Sync In
Select Active		G1J03		C2B02(WK120)		–		–		K2J03(BE160)	E1J03	Select Active
Normal End		G1J05		C2B05(WK120)		–		–		K2D11(BE160)	E1J05	Normal End
Check End		G1G06		C2D06(WK120)		–		–		K2D05(BE160)	E1G06	Check End
Tag Valid		G1G04		C2D05(WK120)		V5D13(BU300)		G2S07(BF160)		K2G05(BE160)	E1G04	Tag Valid
Error Alert		G1J08		C2B08/B09(WK120)*		–		–		L2B09(BD230)	E1J08	Error Alert
Index Alert		G1G09		C2D09/D10(WK120)*		–		–		K2B05(BE160)	E1G09	Index Alert
CE Alert		G1J12		C2B12(WK120)		–		–		L2J05(BD230)	E1J12	CE Alert

CABLE CHECKING HINTS

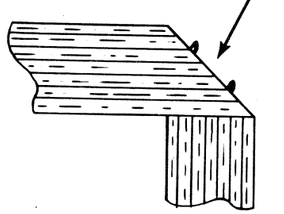
This list contains some (not all) of the items to be considered when checking cables.

REMEMBER: Interface cables must always be connected light (gray) to dark (black). Light to light or dark to dark is wrong (see INST 6).

- Inspect contacts; they may be bent, broken, or pushed in.

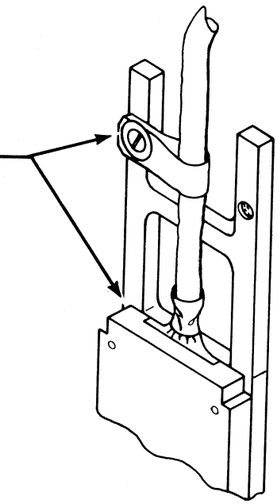


- Inspect at crimps and around strain reliefs for broken wires.
- Inspect SLT paddle cards for cold solder connections, solder splashes, or open land patterns.
- Inspect flat cables at bends for wires breaking through insulation caused by straightening bent cables.



- Inspect for nicks and cuts.

- Inspect wire for evidence of arcing or burning; check especially on paddle cards that carry high current.
- Inspect cables and wires for chafing at rough or sharp pivot points.
- Inspect for interference of strain relief hardware.



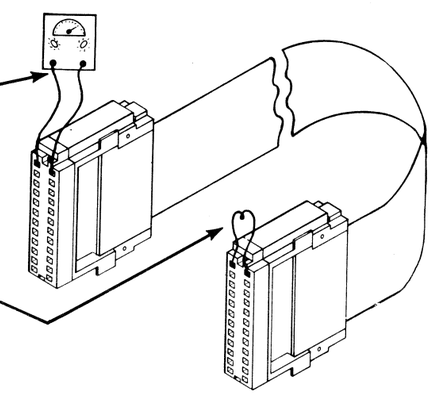
- Check to see if connectors are properly seated and/or mated.
- Where specific lines are suspected or indicated by analysis procedures, use a meter to check for:
  a. Open
  b. Short to ground
  c. Short to adjacent signal line

Possible Action

1. Swap both ends of identical cables (check P/Ns) for isolation (For example: Control Interface cables or Device Interface cables).
2. Use card extenders to swap wires within a cable for isolation or a temporary fix.

Continuity Checks for Long Cables

1. Use the ALDs to verify pin connections.
2. Connect a meter to two pins in the connector.
3. Verify that you have an open circuit.
4. Short the corresponding pins in the other end of the cable.
5. Verify that you now have a short circuit.
6. Meter each signal pin to ground pin D08 to ensure that it is not grounded. Check ALDs to verify any ground connections.

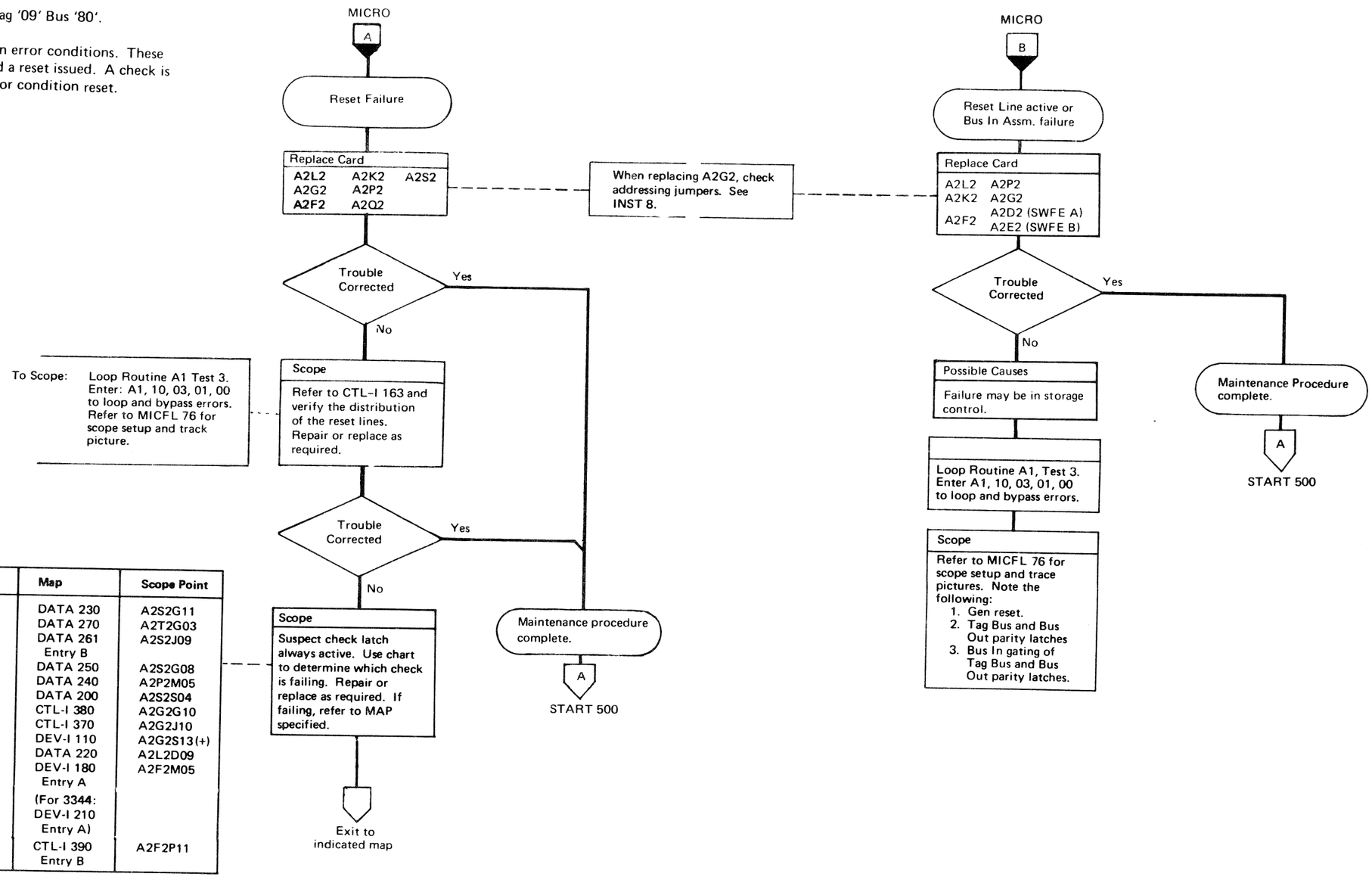


RESET FAILURE

There are two basic resets to the controller:

1. Power On Reset.
   Occurs during the power-on sequence.
2. Controller Reset.
   Occurs as a result of Tag '09' Bus '80'.

Reset is tested by forcing certain error conditions. These conditions are then sampled and a reset issued. A check is then made to verify that the error condition reset.

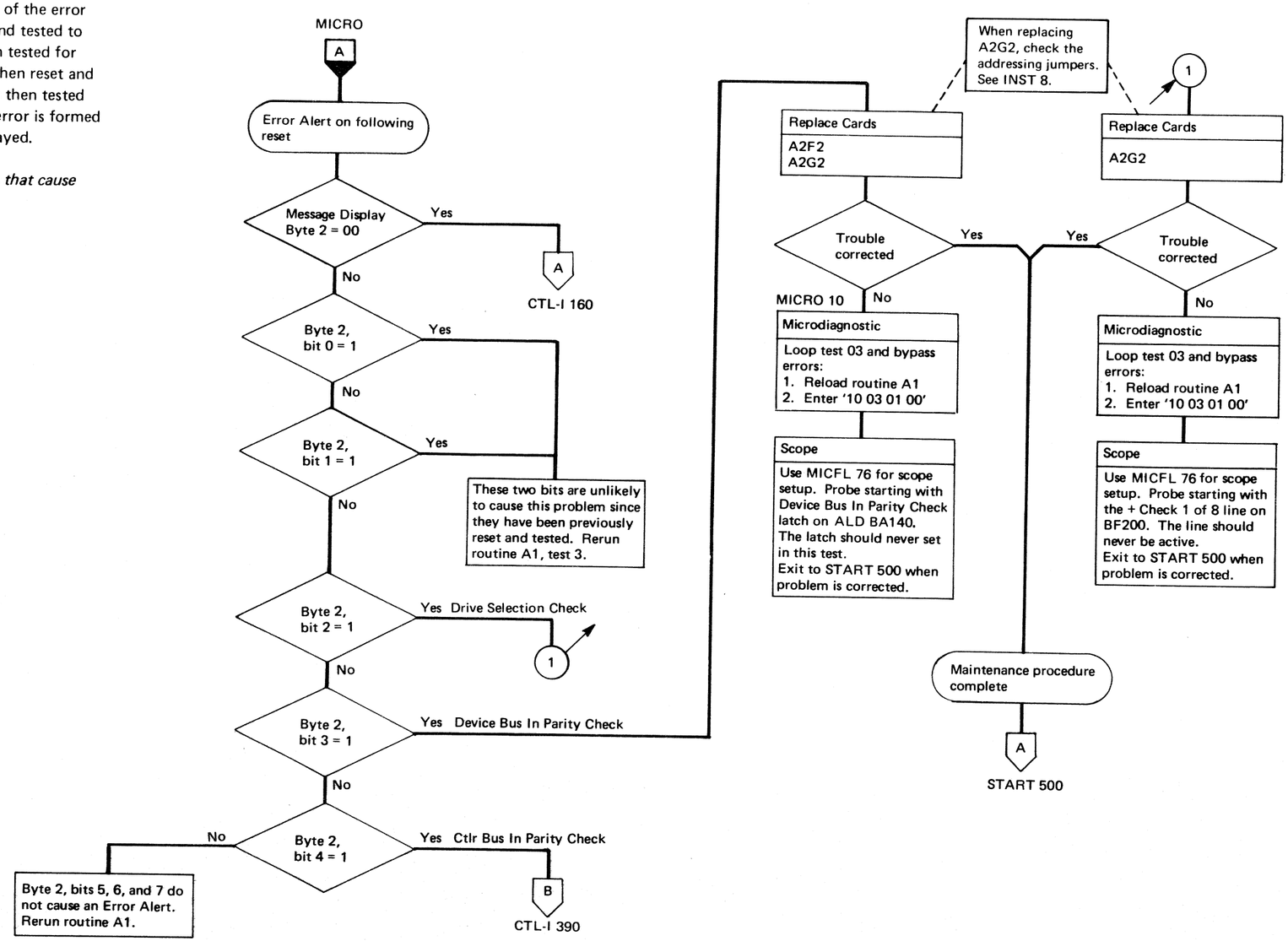


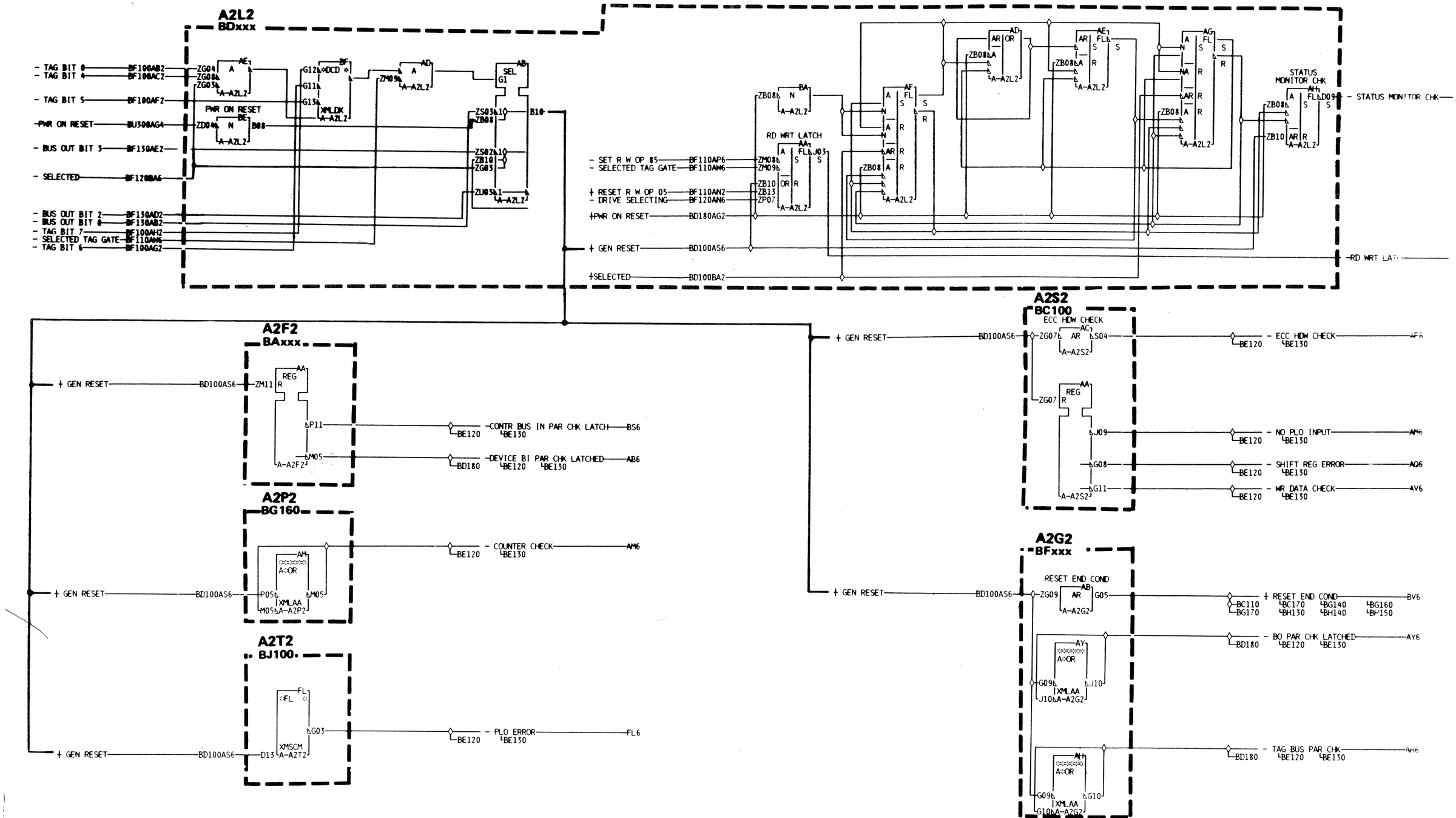
Check Name	Map	Scope Point
Write Data Check	DATA 230	A2S2G11
PLO Error	DATA 270	A2T2G03
No PLO Input	DATA 261 Entry B	A2S2J09
SERDES Shift Reg. Chk	DATA 250	A2S2G08
Counter Chk.	DATA 240	A2P2M05
ECC Hdw. Chk.	DATA 200	A2S2S04
Tag Bus Parity Chk.	CTL-I 380	A2G2G10
Bus Out Parity Chk.	CTL-I 370	A2G2J10
Check 1 of 8	DEV-I 110	A2G2S13(+)
Monitor Chk.	DATA 220	A2L2D09
Dev. Bus in Parity Chk.	DEV-I 180 Entry A (For 3344: DEV-I 210 Entry A)	A2F2M05
Ctl. Bus In Parity Chk.	CTL-I 390 Entry B	A2F2P11

RESET FAILURE (Unexpected Error Alert)

Routine A1 test 3 begins a test of some of the error checkers. The checkers are forced on and tested to see that they are on. Error Alert is then tested for it's aetive state. The check latches are then reset and checked for the off state. Error Alert is then tested for it's inactive state. If it is active, an error is formed and the Controller Error 1 Byte is displayed.

See OPER 260 for a summary of checks that cause Error Alert.



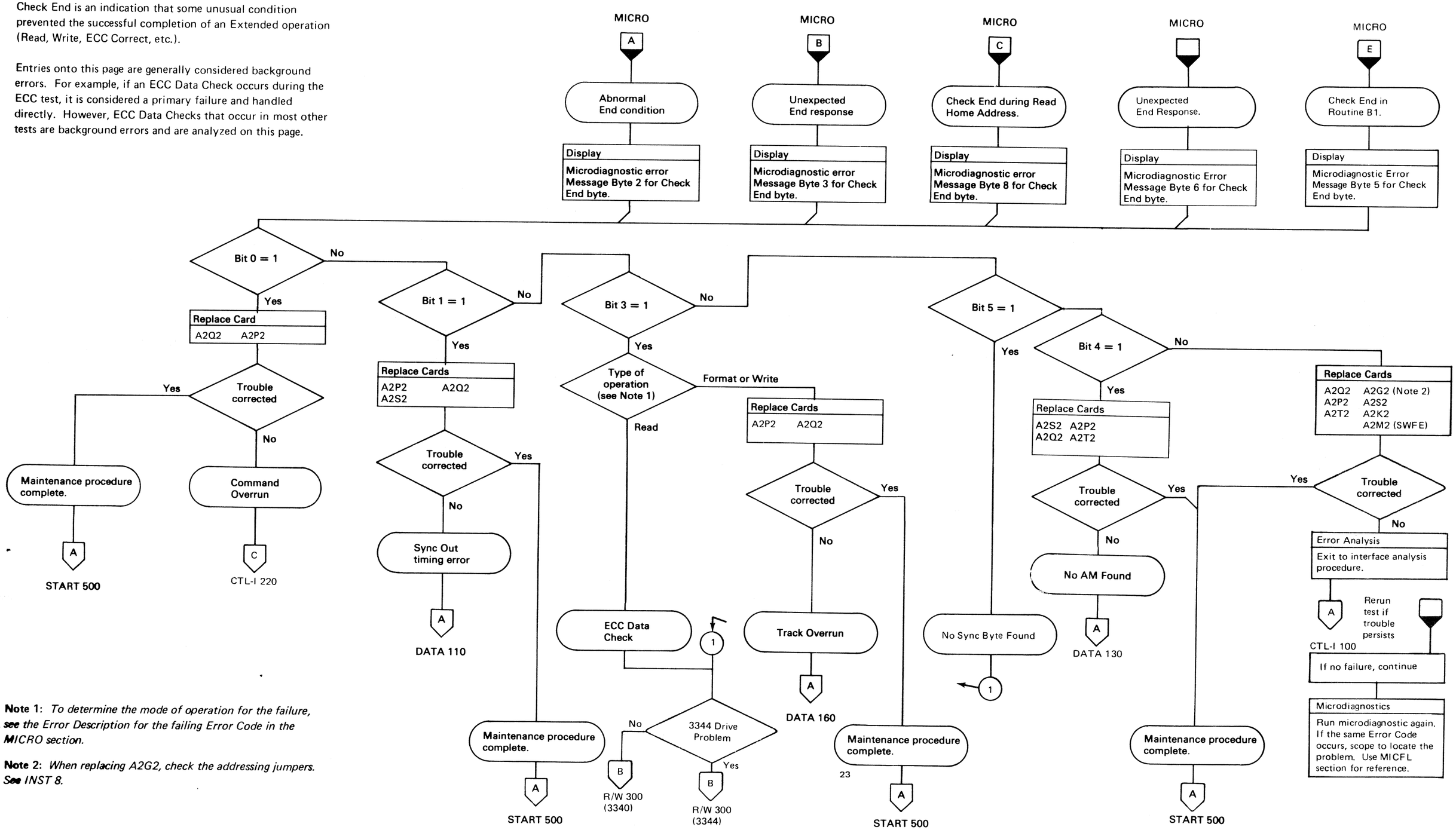


BQ0161 Seq. 2 of 2	2747595 Part No.( )	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74	440224 15 Dec 75		

CHECK END DECISIONS

Check End is an indication that some unusual condition prevented the successful completion of an Extended operation (Read, Write, ECC Correct, etc.).

Entries onto this page are generally considered background errors. For example, if an ECC Data Check occurs during the ECC test, it is considered a primary failure and handled directly. However, ECC Data Checks that occur in most other tests are background errors and are analyzed on this page.

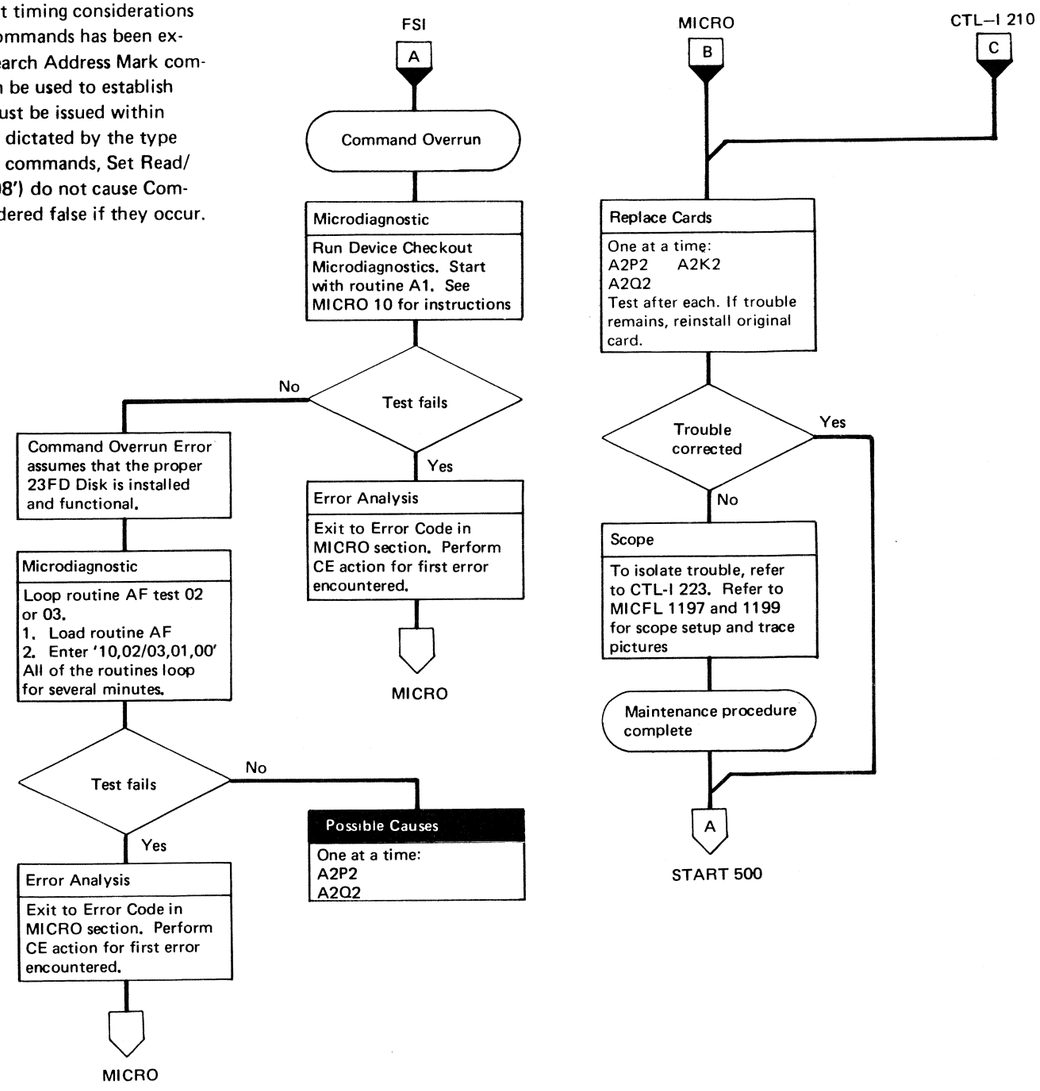


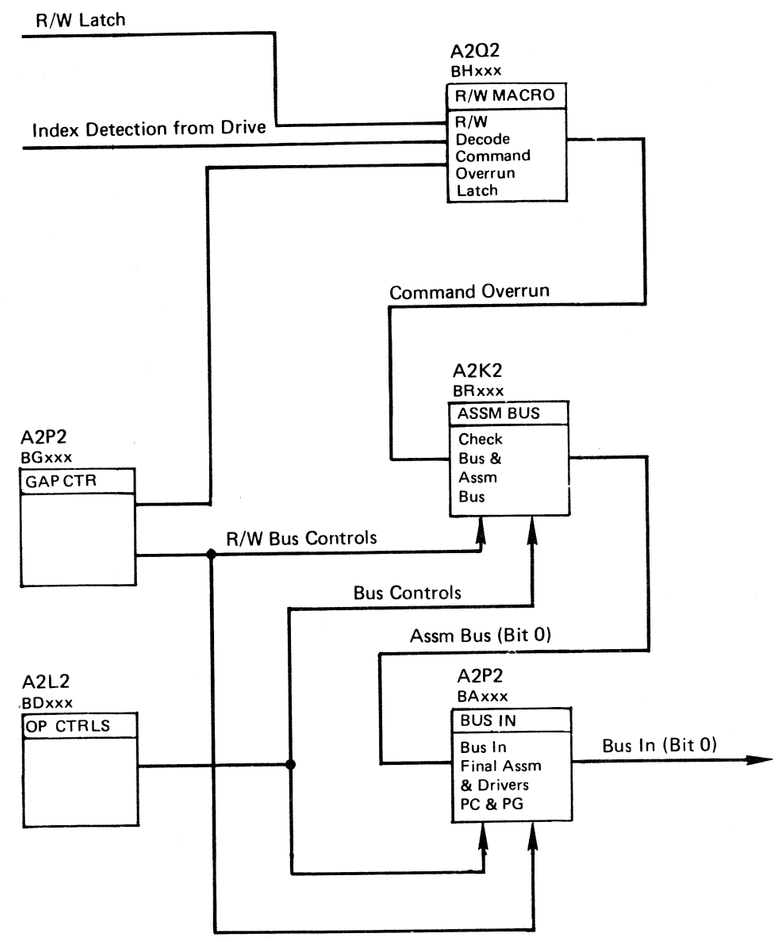
Note 1: *To determine the mode of operation for the failure, see the Error Description for the failing Error Code in the MICRO section.*

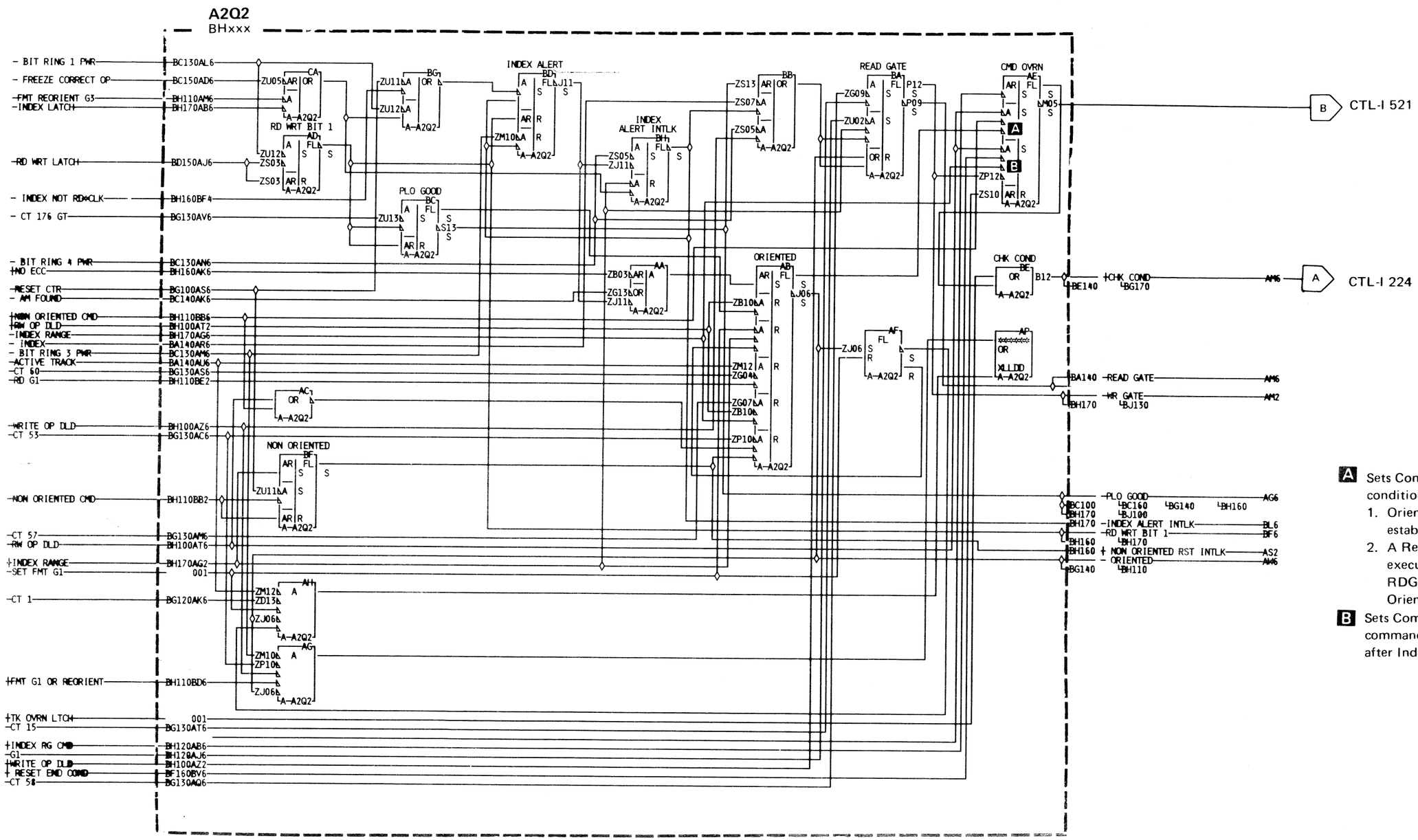
Note 2: *When replacing A2G2, check the addressing jumpers. See INST 8.*

COMMAND OVERRUN

Command Overrun is an indication that timing considerations for a sequence of Read and/or Write commands has been exceeded. The Read, Format G1, and Search Address Mark commands are the only commands that can be used to establish orientation. Subsequent commands must be issued within certain time limits, which are generally dictated by the type of gap and the command involved. G1 commands, Set Read/Write (op '85') and ECC Correct (op '08') do not cause Command Overruns. They should be considered false if they occur.



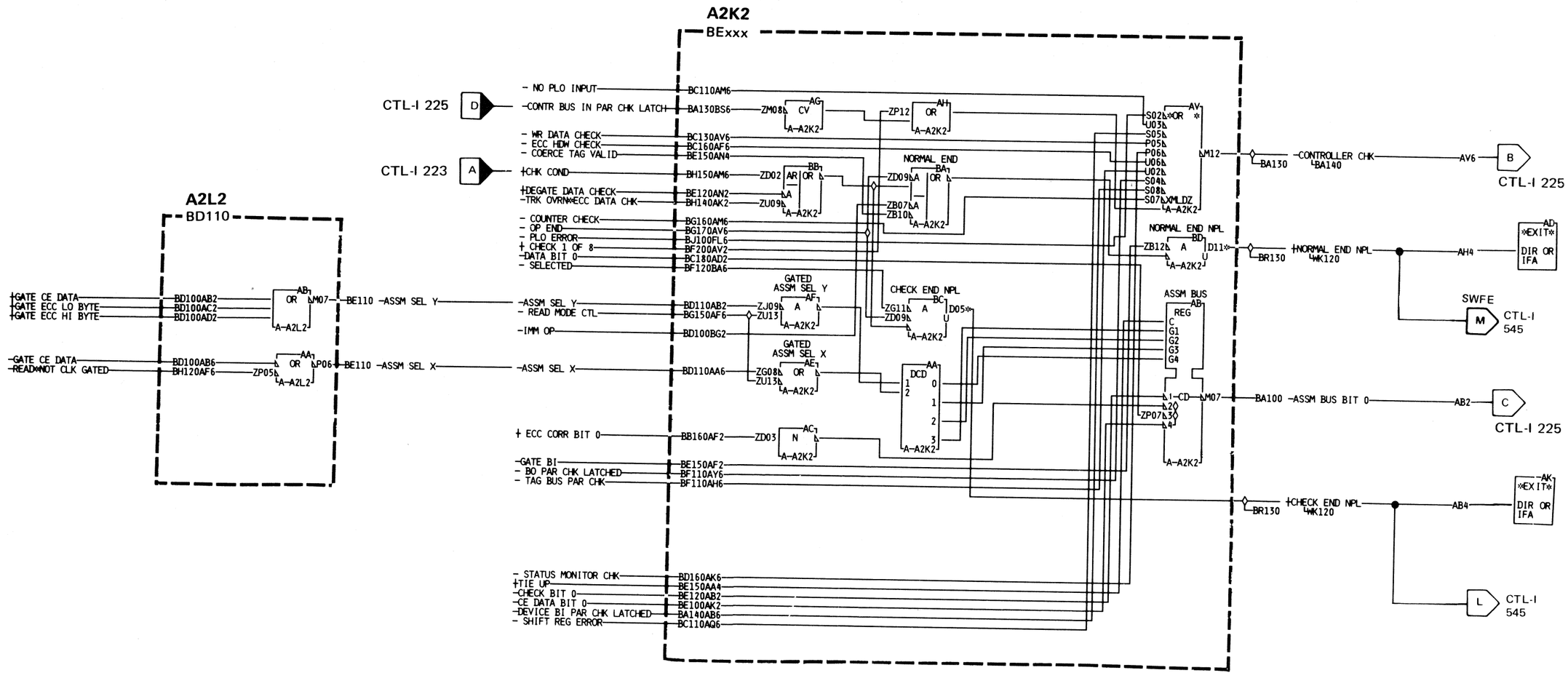




A Sets Command Overrun under these conditions:

1. Orientation should have been established but was not.
2. A Read or Write command was executed. (Only G1 commands and RDG3 commands can establish Orientation)

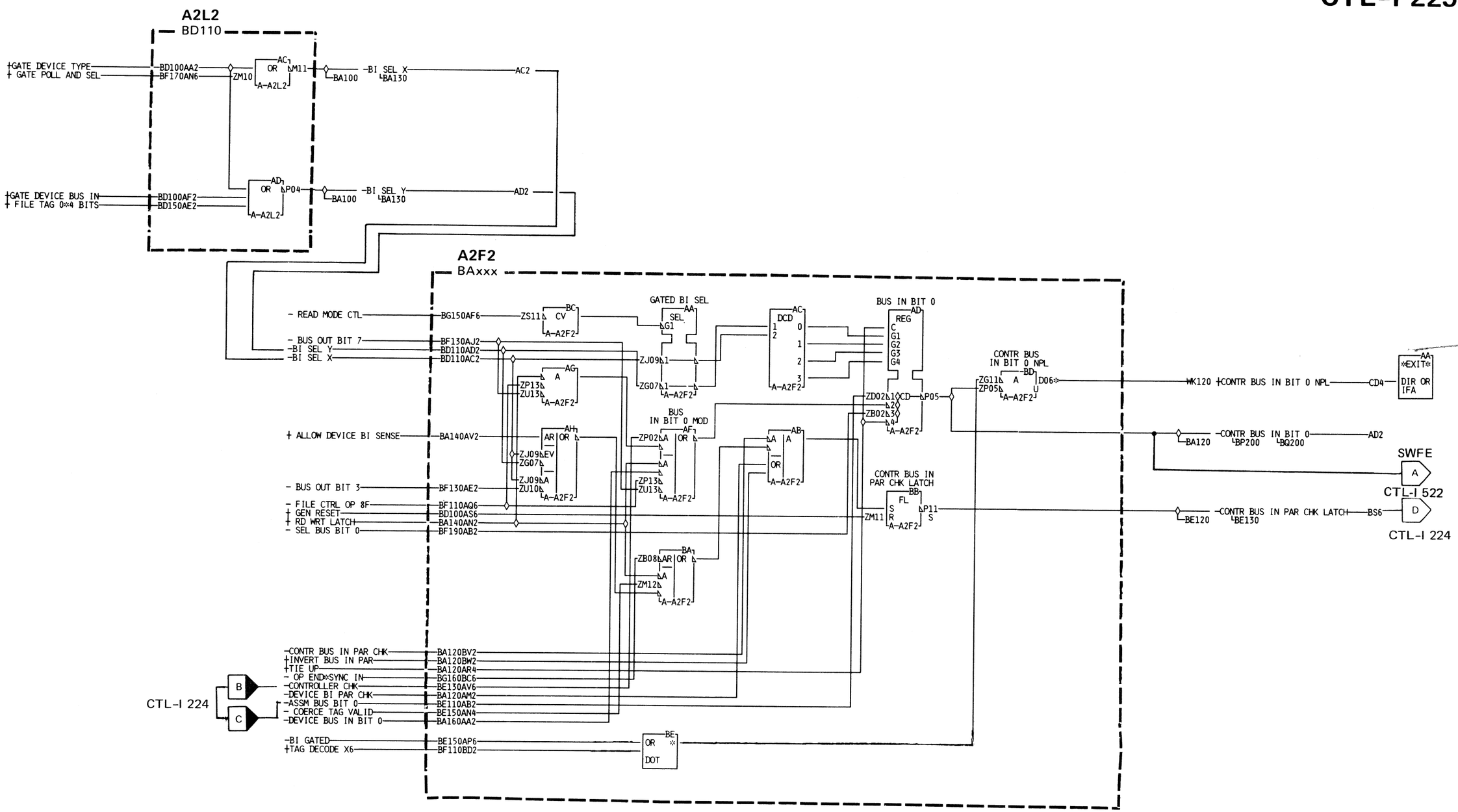
B Sets Command Overrun if a Write command is issued within 57 bytes after Index.



3340

BQ0220	2747422
Seq.2 of 2	Part No.( )

440200	440202	440203	440204	440213	
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	13 May 74	



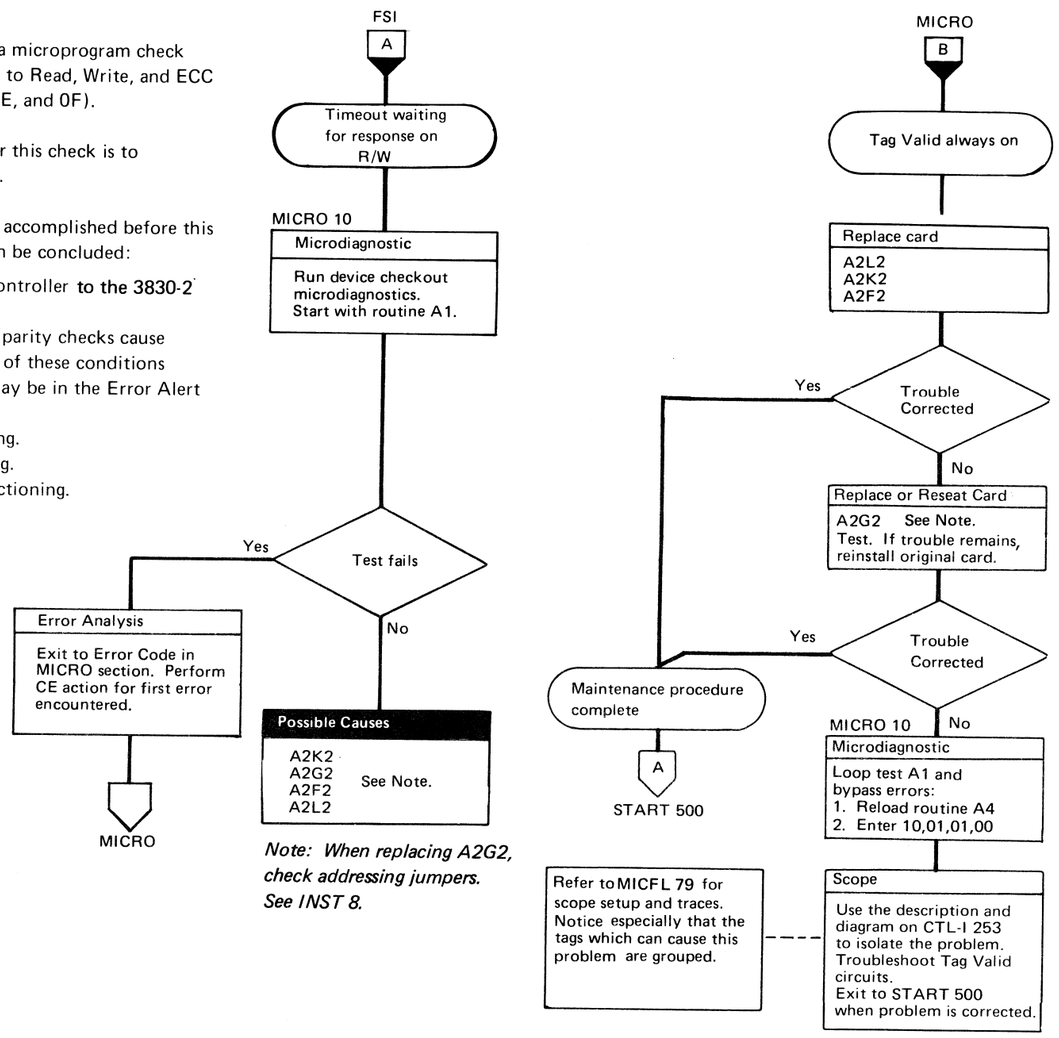
TIME OUT WAITING FOR RESPONSE ON R/W

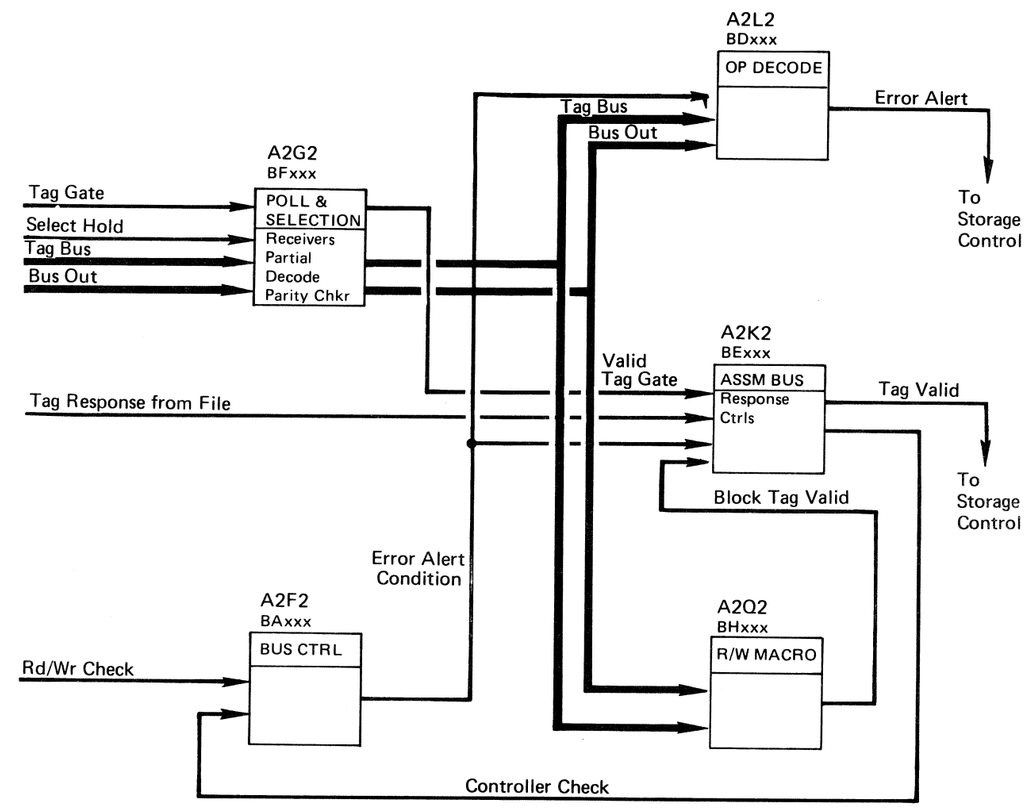
No Tag Valid on Rd/Wr is a microprogram check of controller response time to Read, Write, and ECC operations (Op codes 08, 0E, and 0F).

One of the main reasons for this check is to eliminate 'hang' conditions.

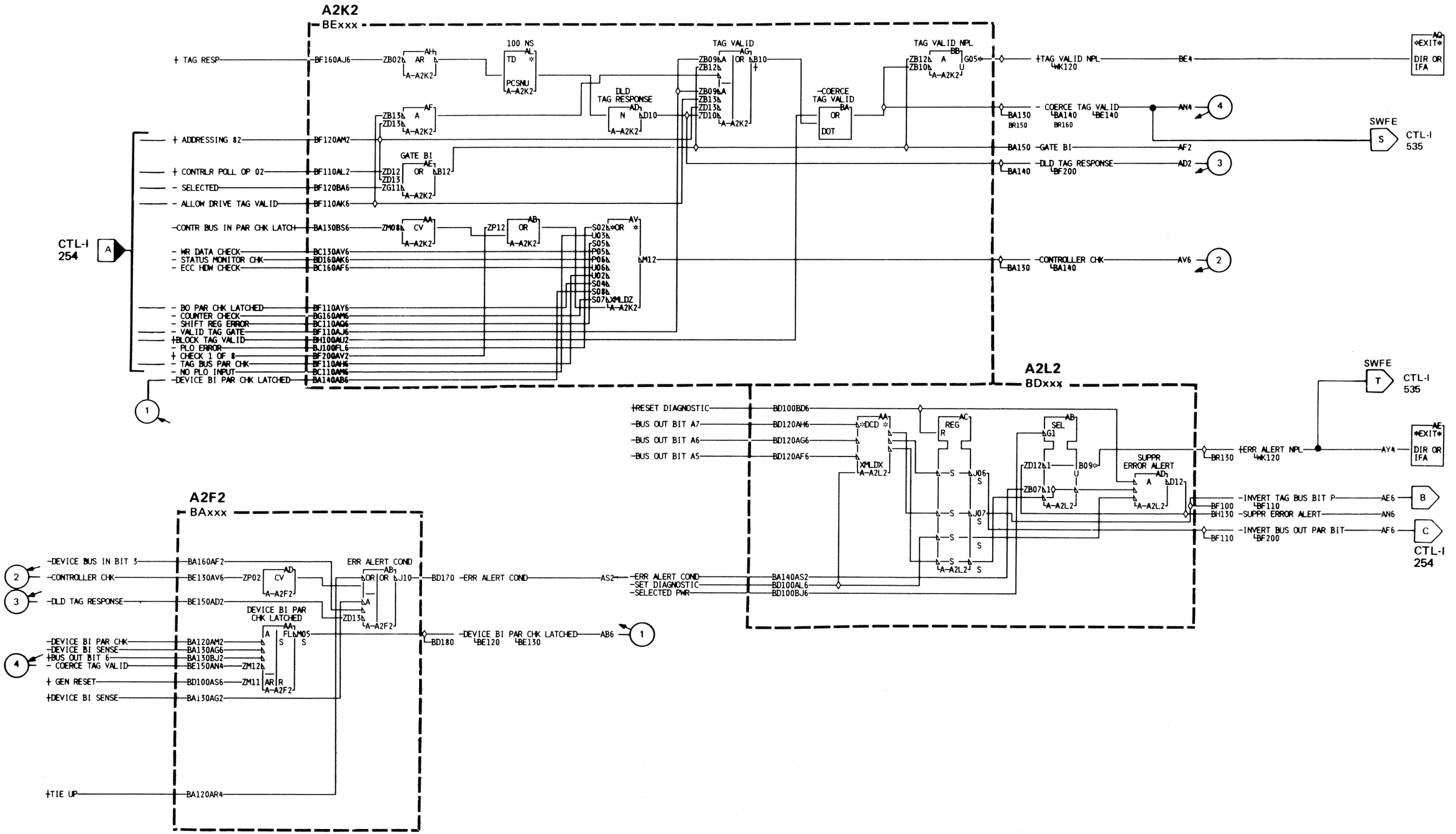
Selection should have been accomplished before this check and the following can be concluded:

1. Tag Valid from the controller to the 3830-2 is functioning.
2. Bus Out and Tag Bus parity checks cause Error Alert. If either of these conditions exists, the problem may be in the Error Alert circuits.
3. Tag Gate is functioning.
4. Selected is functioning.
5. Valid Tag Gate is functioning.

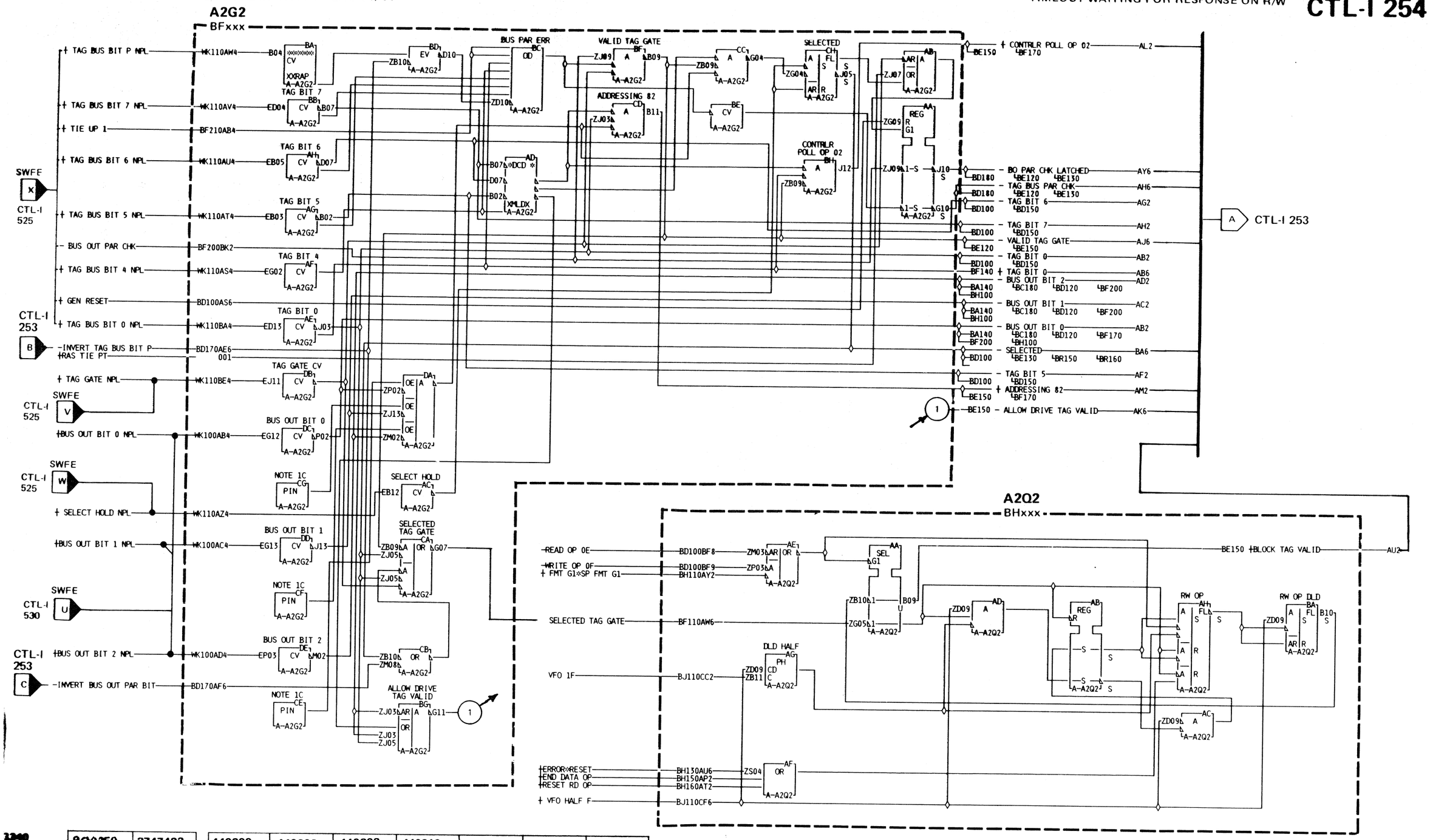




TIMEOUT WAITING FOR RESPONSE ON R/W



TIMEOUT WAITING FOR RESPONSE ON R/W



8C10250 Seq 2 of 2	2747423 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440213 13 May 74			

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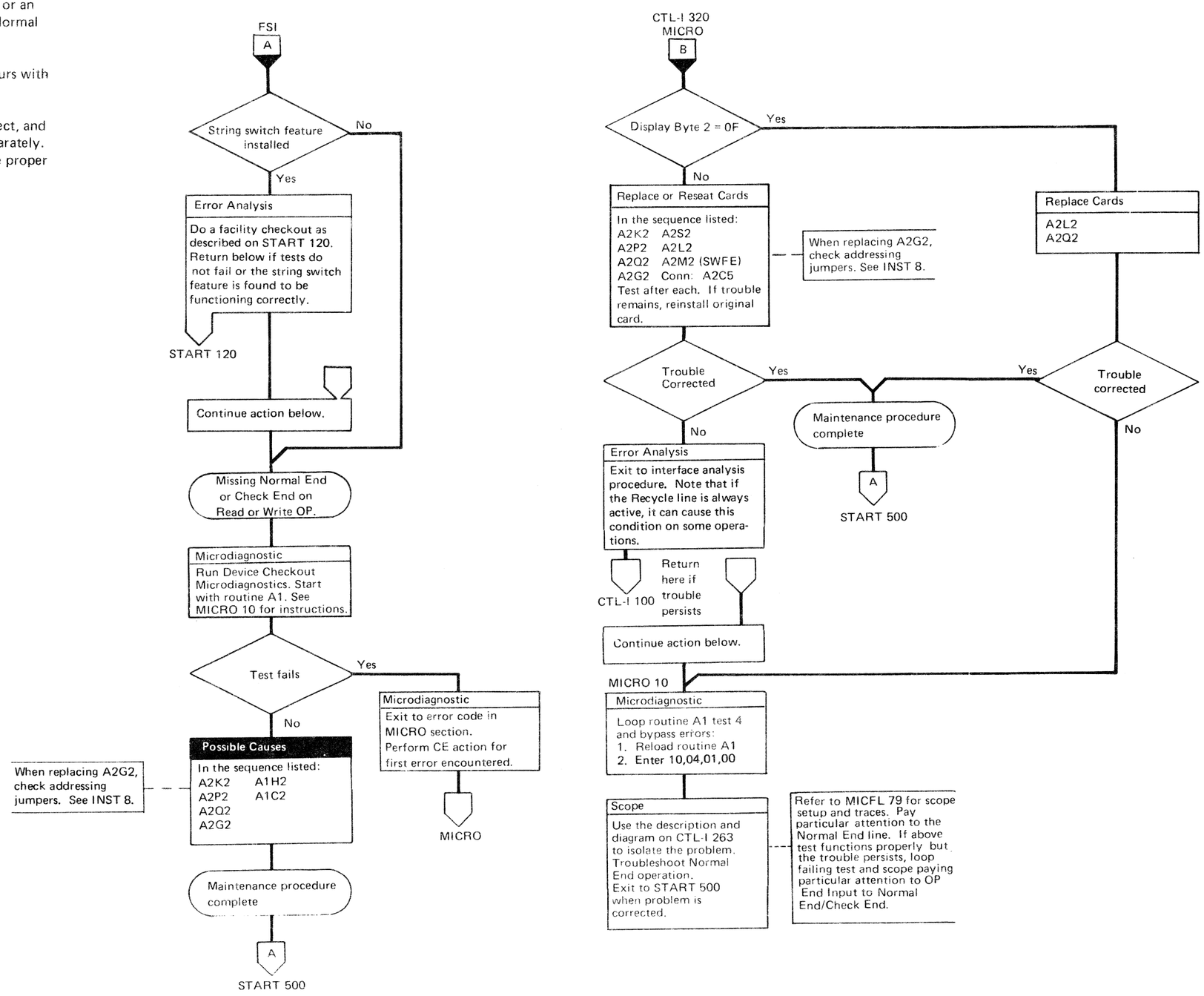
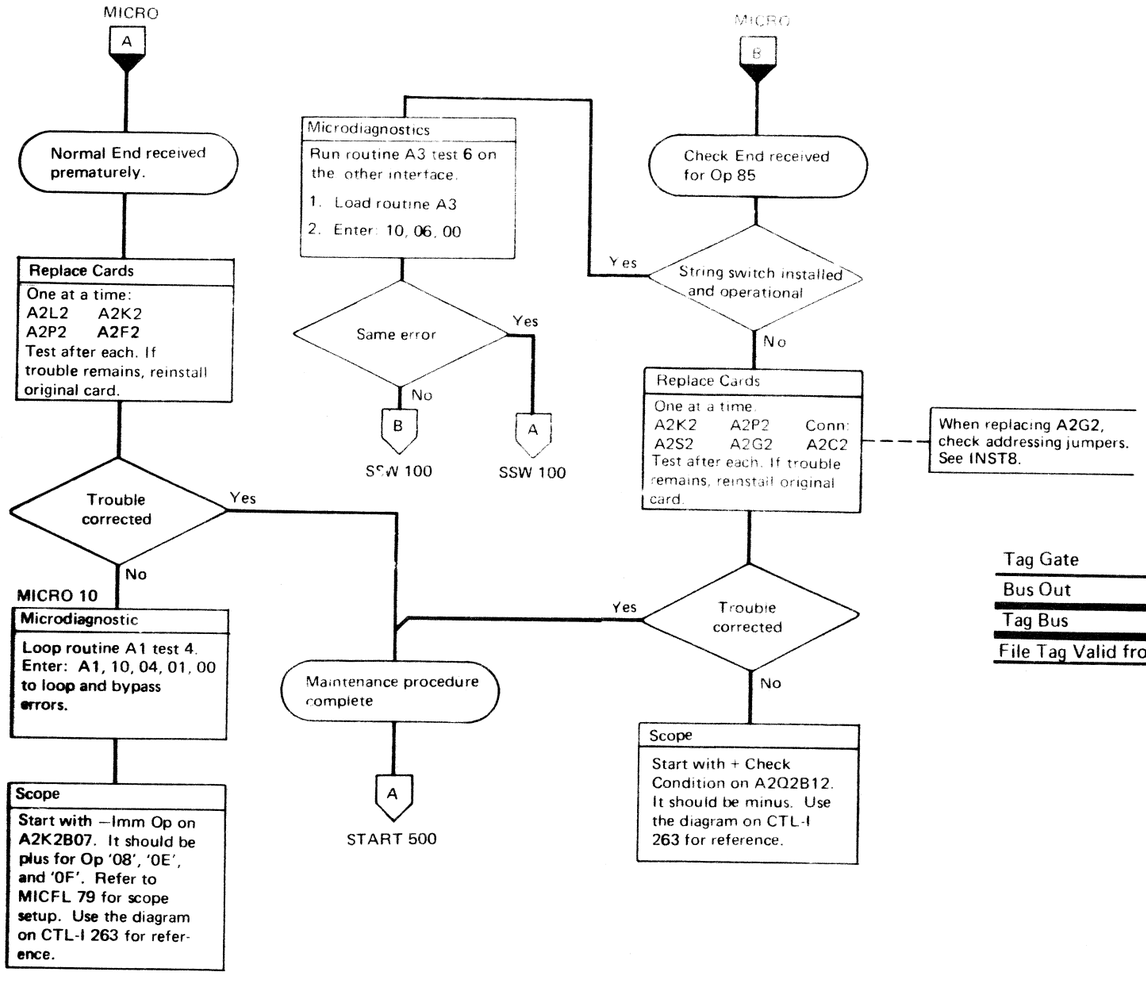
Each operation, whether an Immediate Operation or an Extended Operation, must be terminated with a Normal End or a Check End.

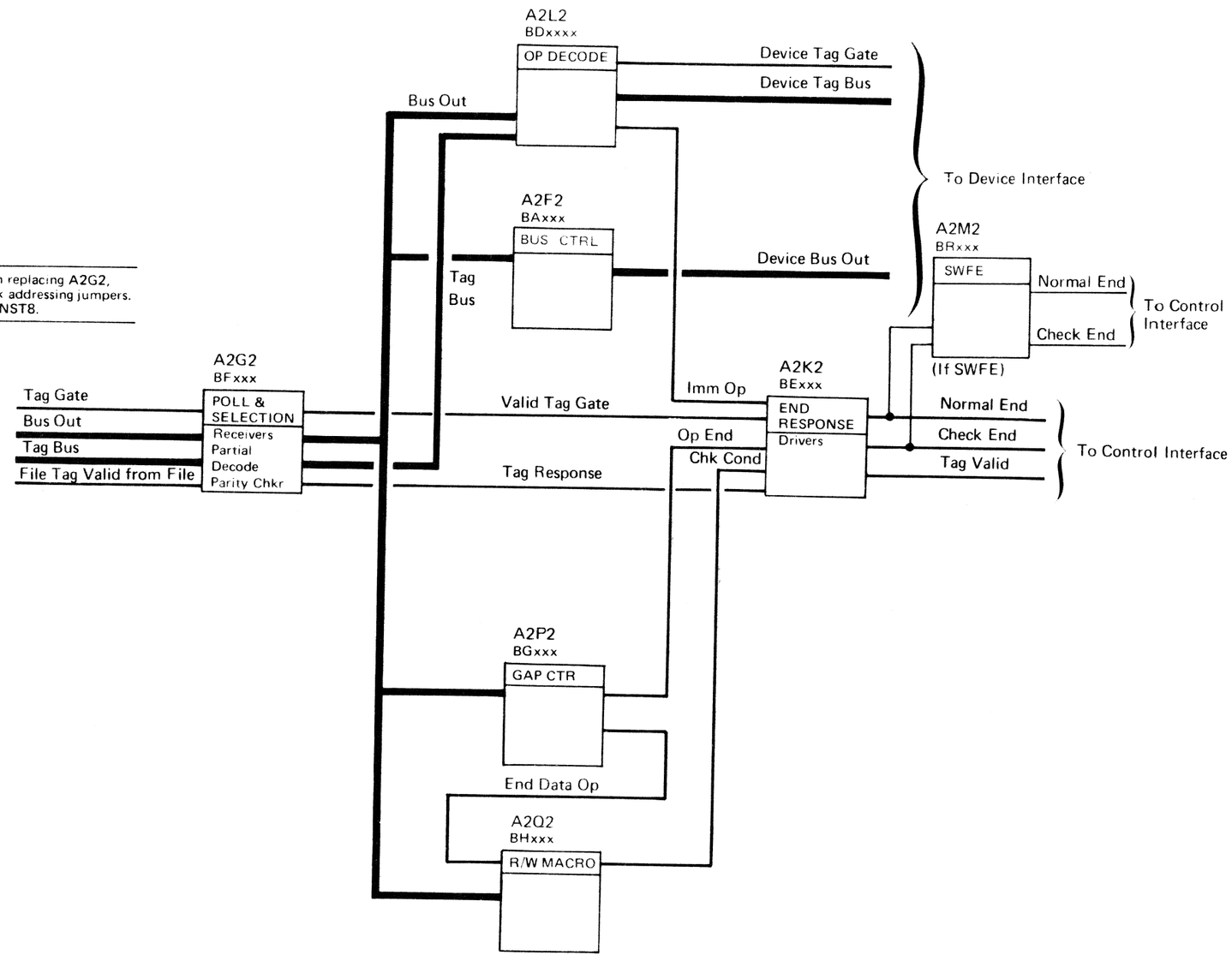
For Immediate Operations, the end condition occurs with Tag Valid.

For Extended Operations, Read, Write, ECC Correct, and Set Read/Write, the end condition is returned separately. If Normal End or Check End is not received at the proper time, an error is posted.



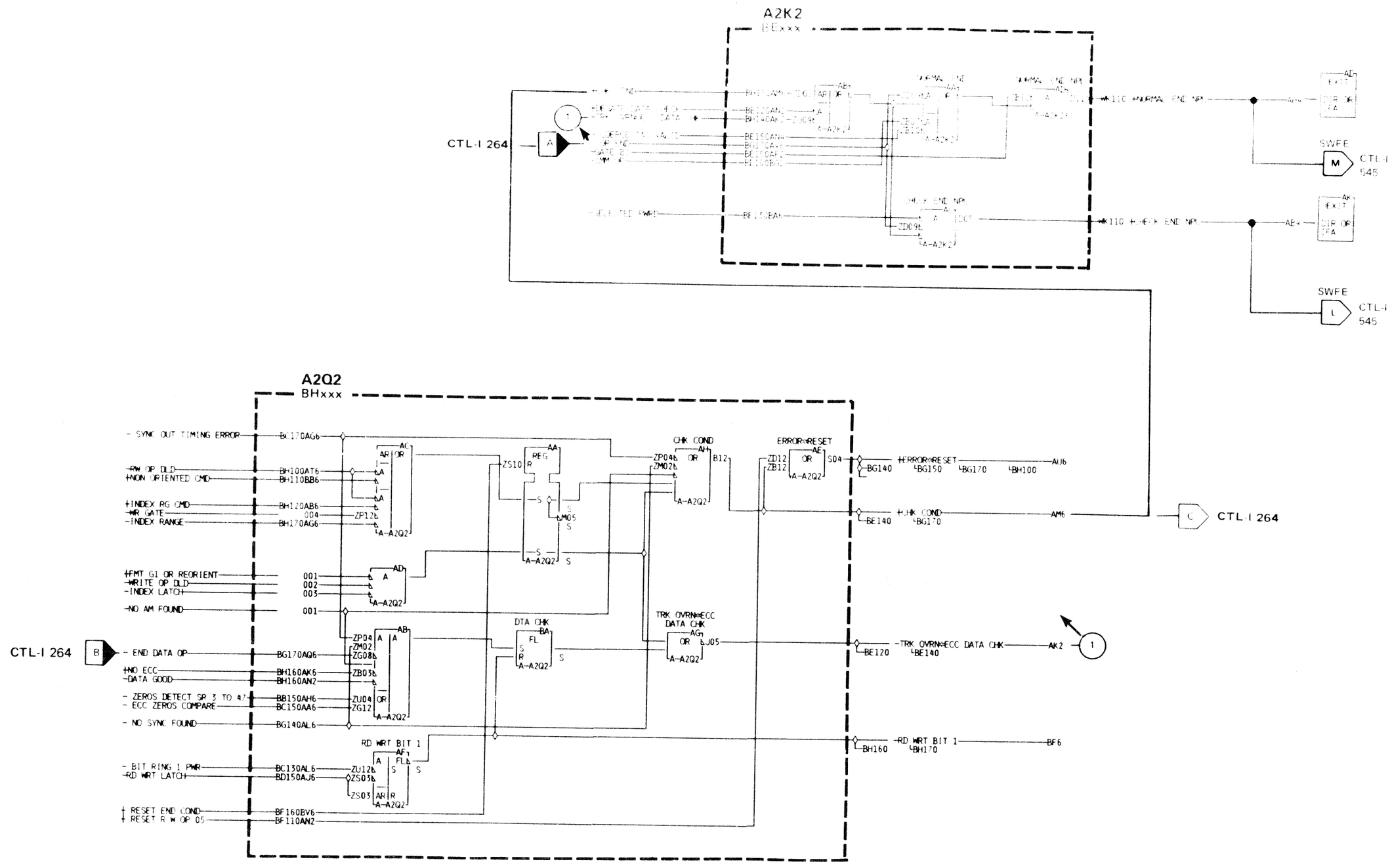
NORMAL END AND CHECK END





BQ0263	2747425	See EC	440218	440219	440224	440227

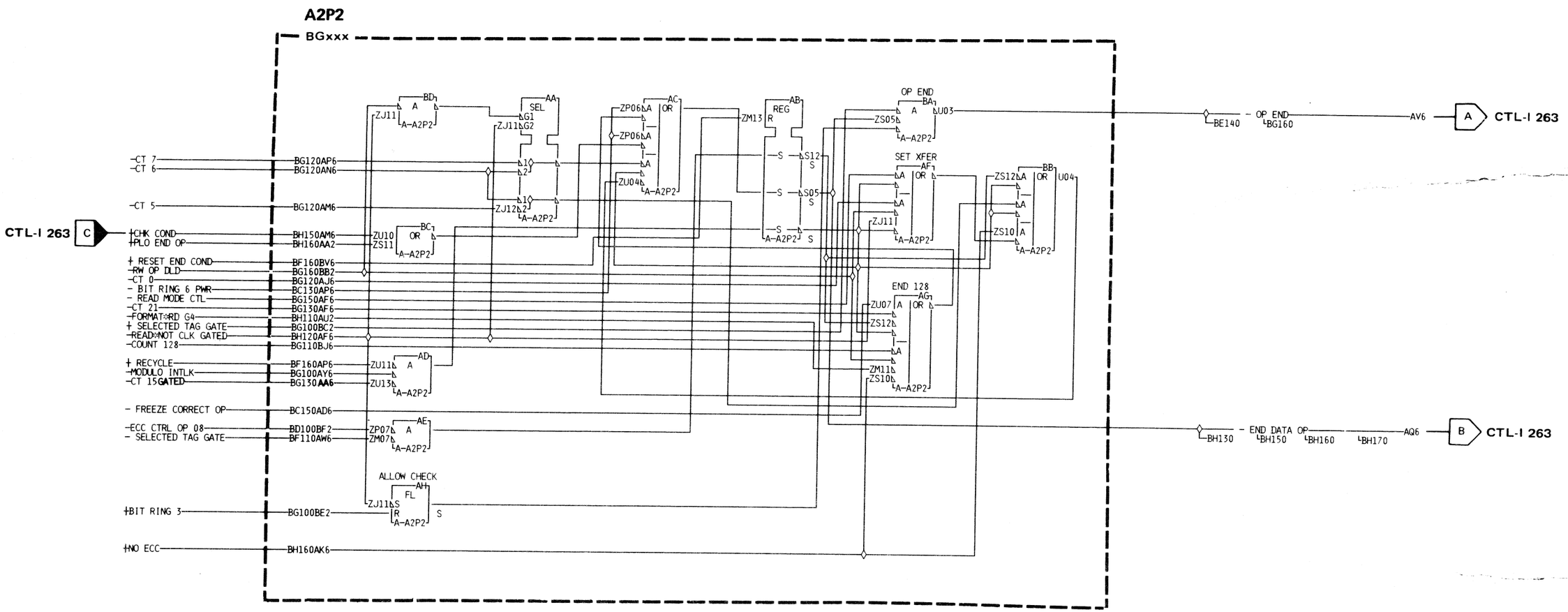
NORMAL END AND CHECK END



3340

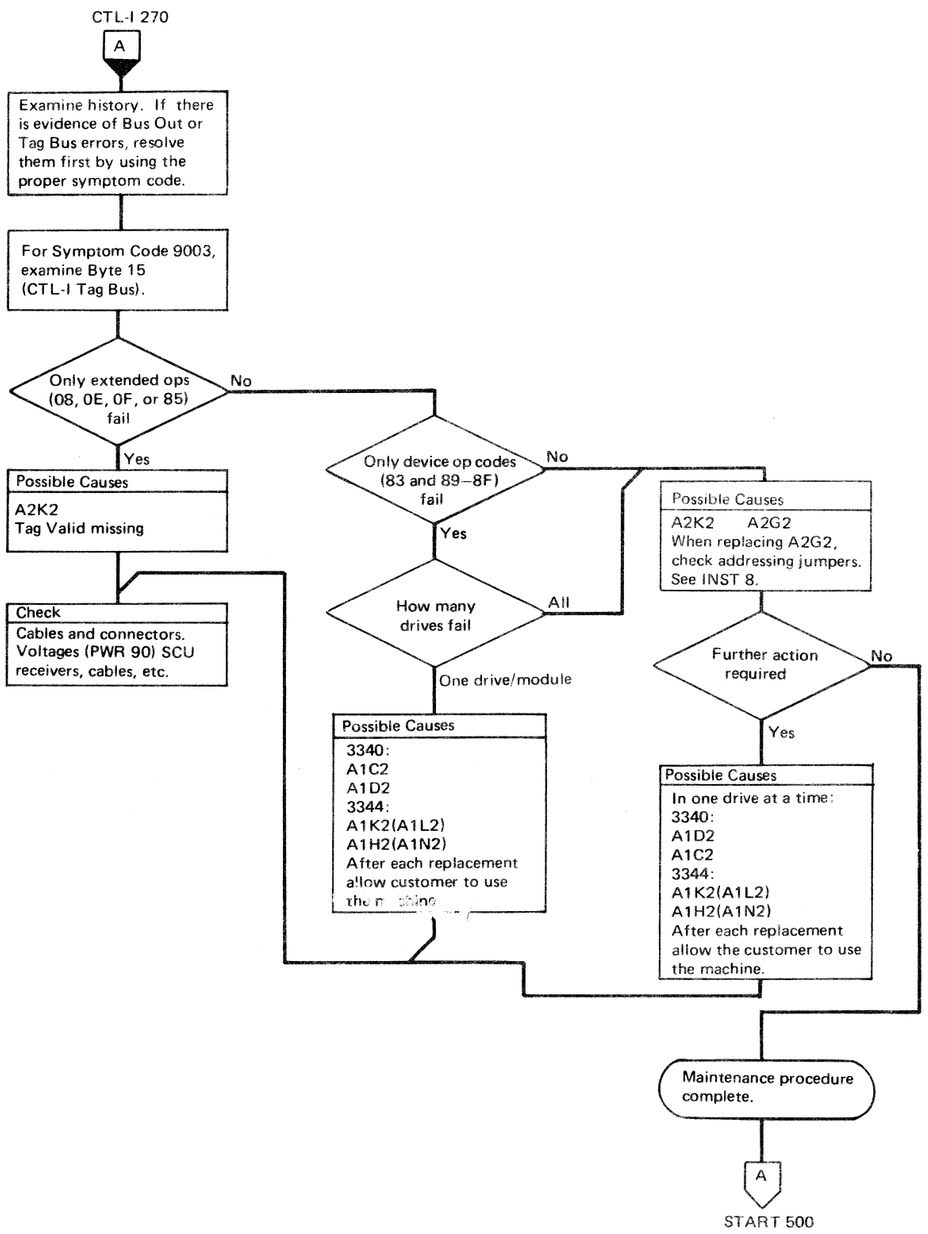
BQ0263	2747425	See EC	440218	440219	440224	440227		
Seq. 2 of 2	Part No. 11	History	5 Aug 74	20 Sept 74	15 Dec 75	14 Sept 76		

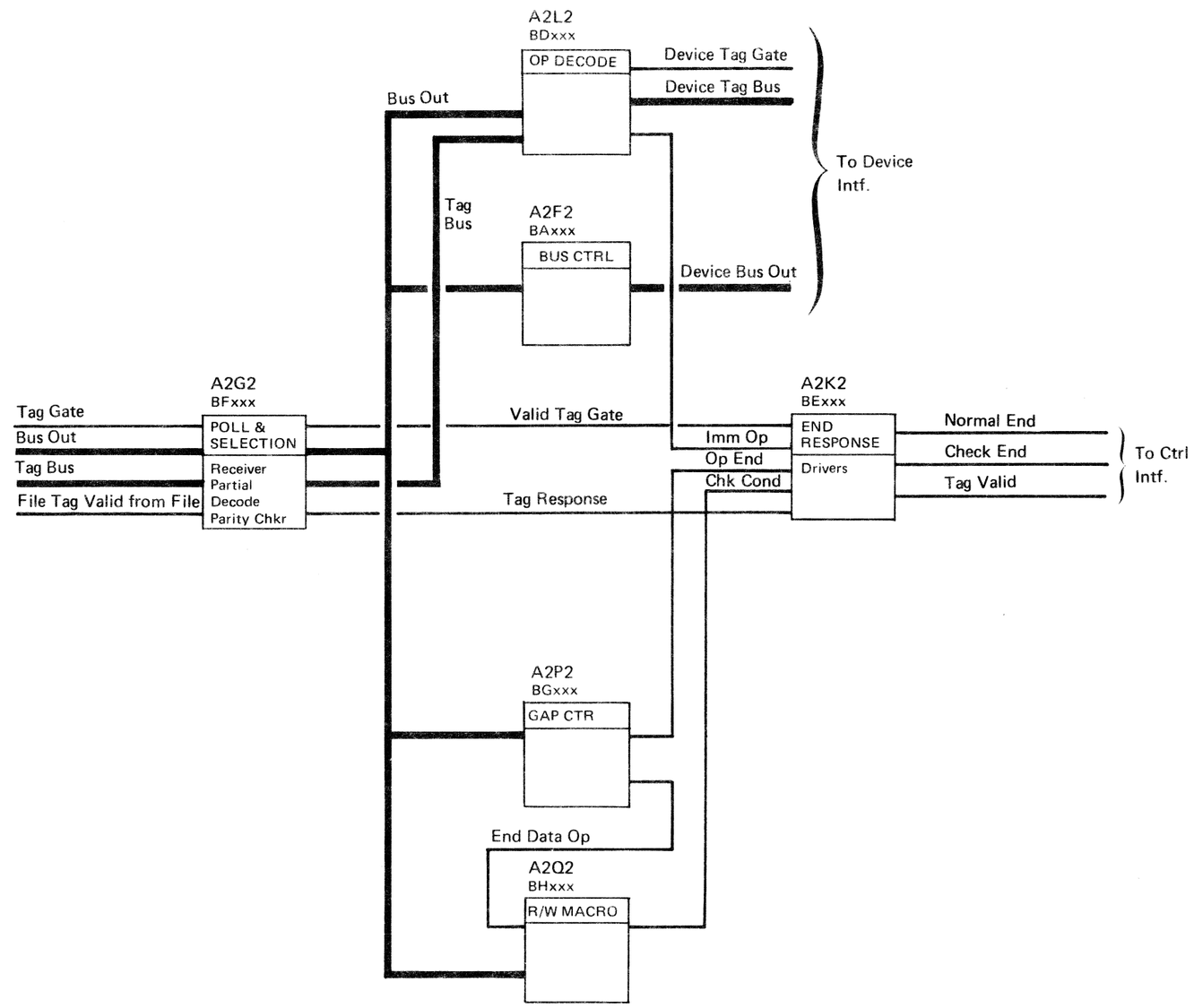
NORMAL END AND CHECK END



BQ0270 Seq. 1 of 2	2747593 Part No.( )	See EC History	440223 14 Mar 75	440224 15 Dec 75			

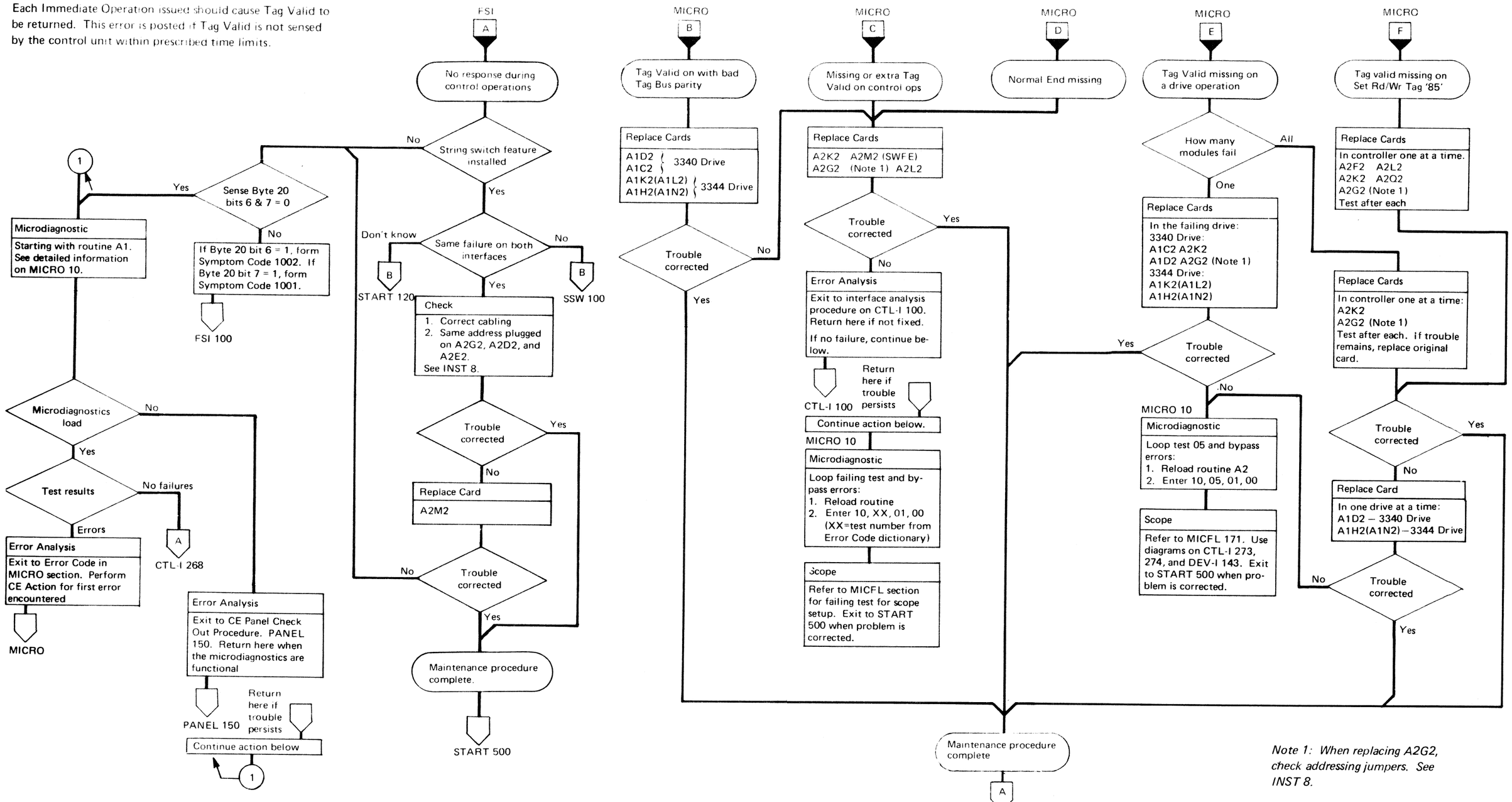
NO RESPONSE DURING CONTROL OPERATIONS



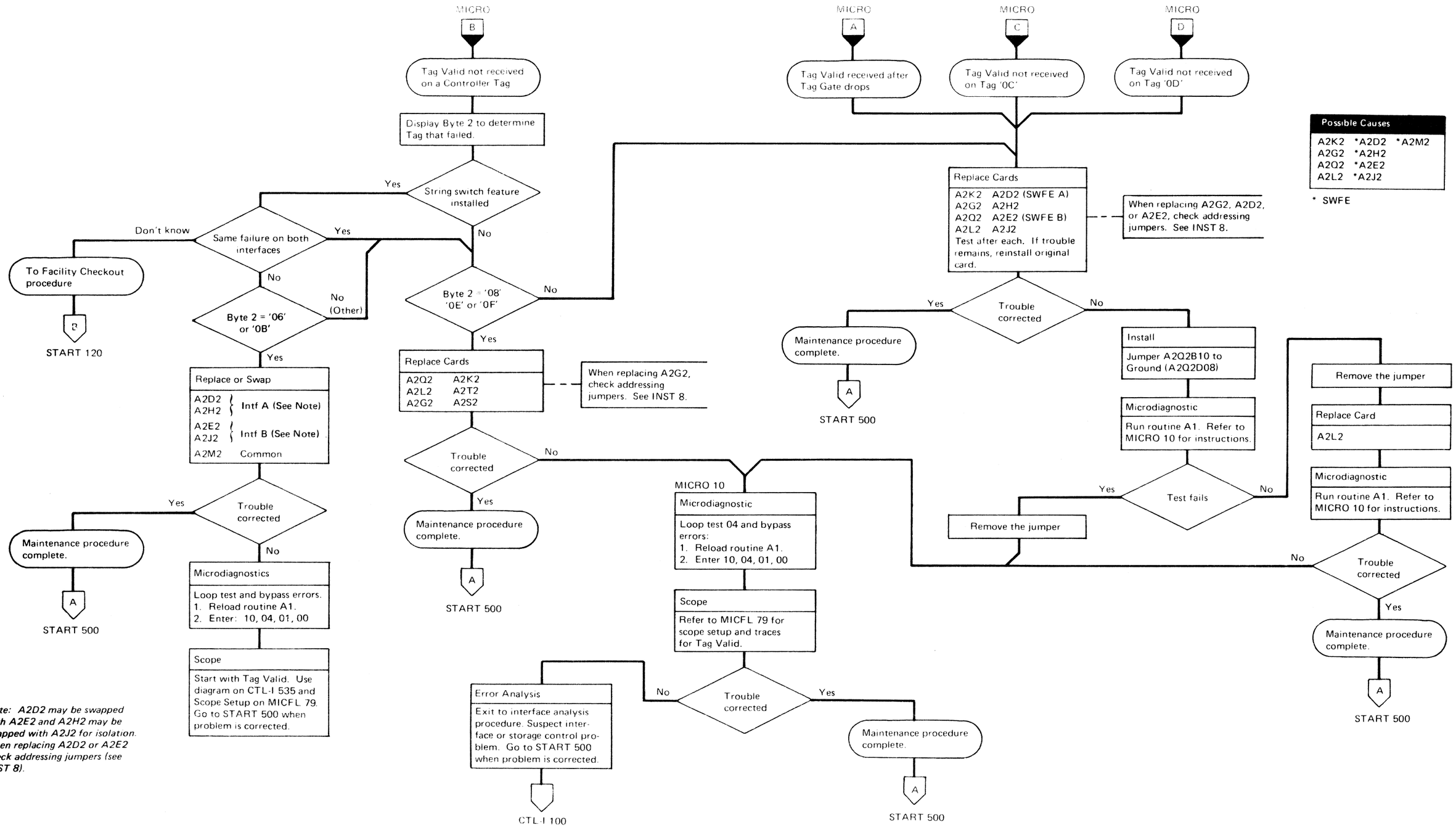


NO RESPONSE DURING CONTROL OPERATIONS

Each Immediate Operation issued should cause Tag Valid to be returned. This error is posted if Tag Valid is not sensed by the control unit within prescribed time limits.

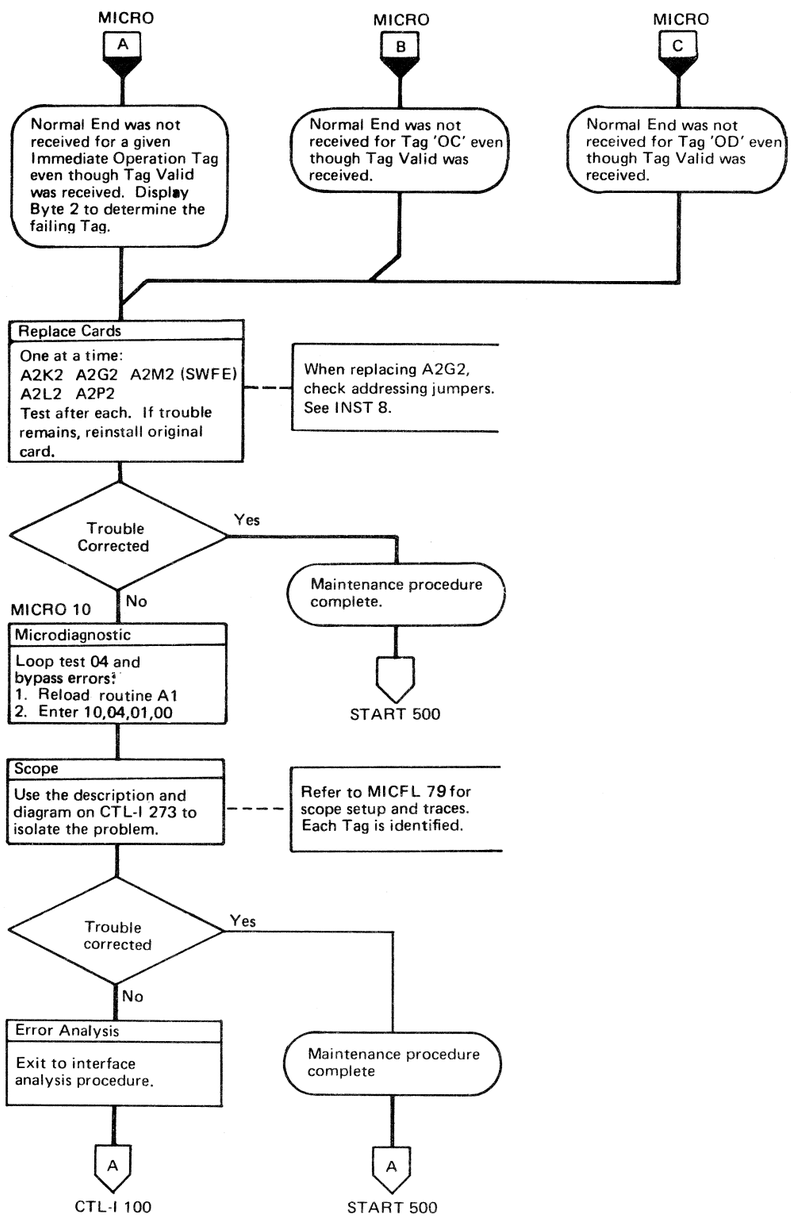


Note 1: When replacing A2G2, check addressing jumpers. See INST 8.



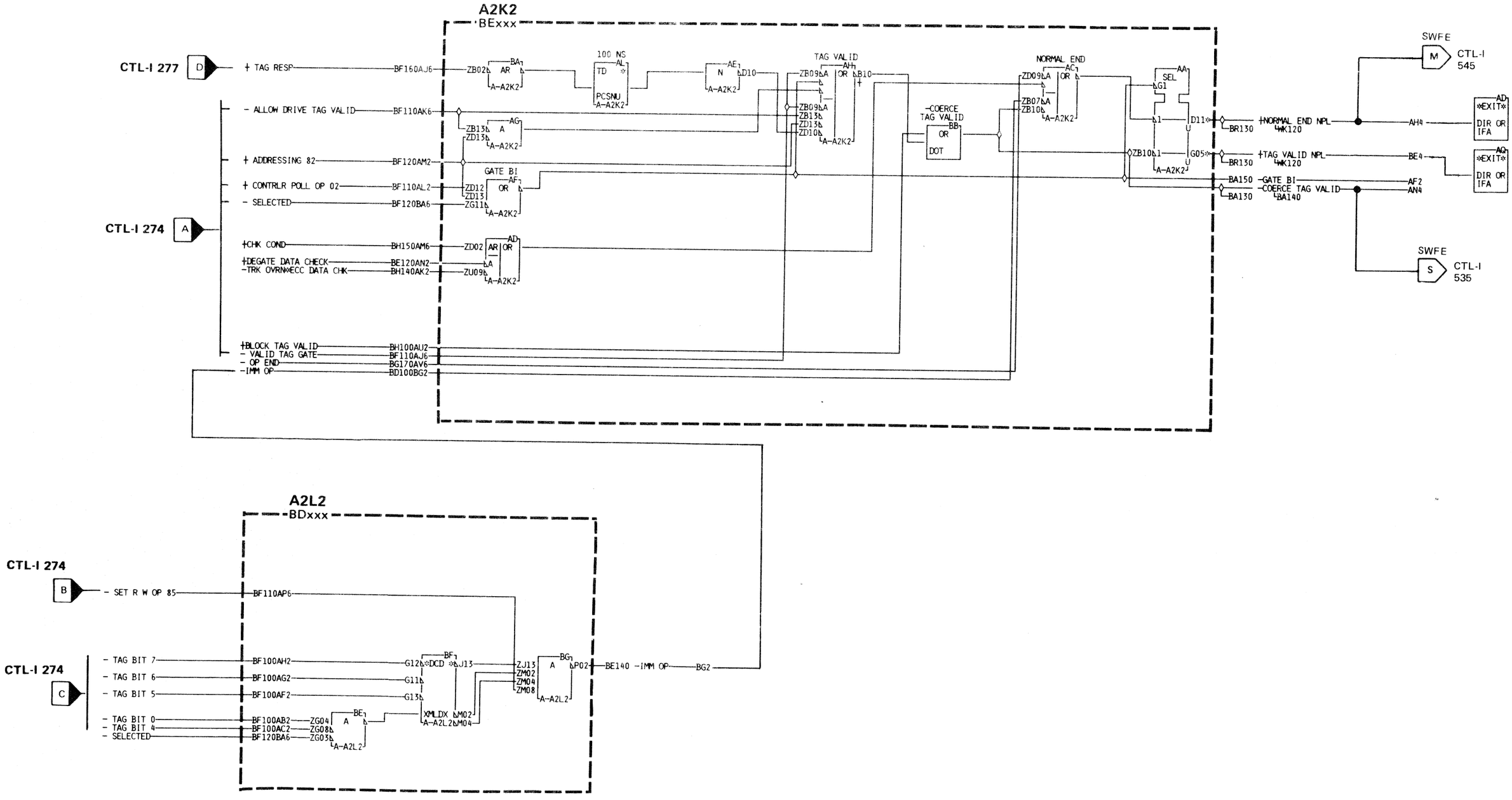
***Note:** A2D2 may be swapped with A2E2 and A2H2 may be swapped with A2J2 for isolation. When replacing A2D2 or A2E2 check addressing jumpers (see INST 8).*

MISSING NORMAL END



Normal End should be presented simultaneously with Tag Valid for all Immediate Operations. The error stops on this page indicate a lack of the Normal End pulse.

NO RESPONSE DURING CONTROL OPERATION

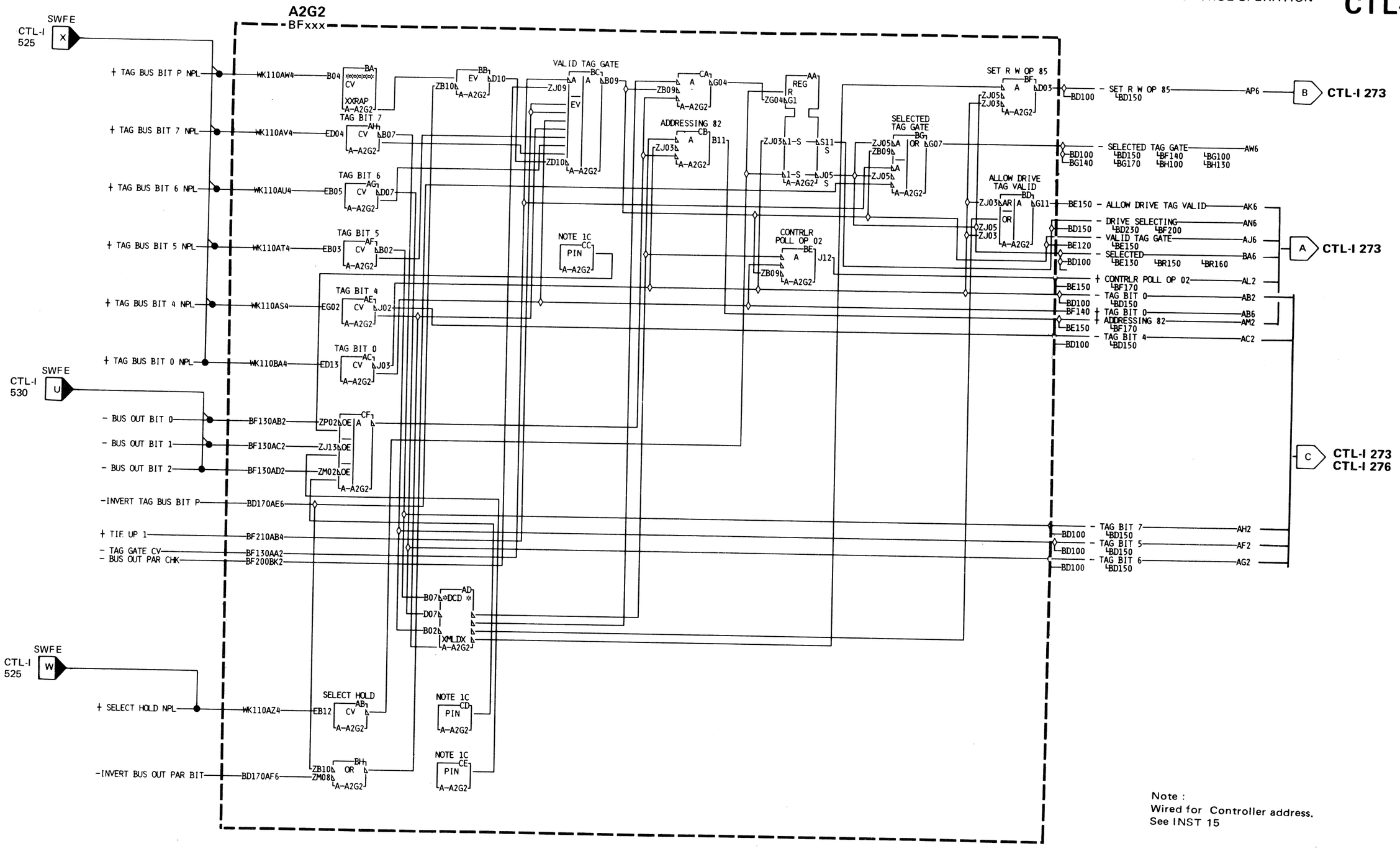


3340

BQ0273 Seq. 2 of 2	2747427 Part No. (1)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440213 13 May 74	440224 15 Dec 75	440227 14 Sept 76	

NO RESPONSE DURING CONTROL OPERATION CTL-I 273

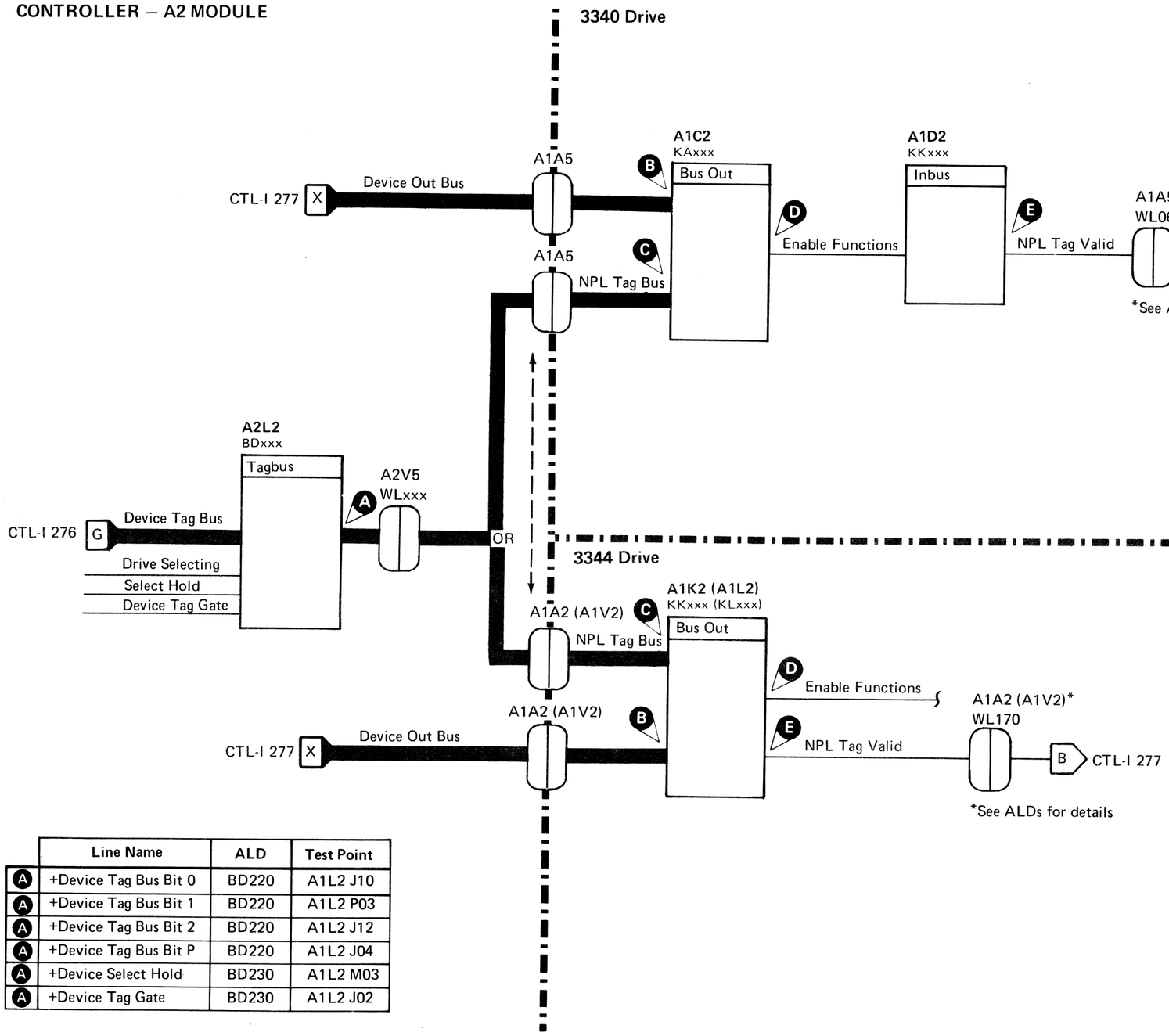
NO RESPONSE DURING CONTROL OPERATION



Note :
Wired for Controller address.
See INST 15

BQ0275 Seq. 1 of 2	2747594 Part No. (1)	440202 7 Sept 73	440203 2 Nov 73	440213 13 May 74	440224 15 Dec 75	440227 14 Sept 76		

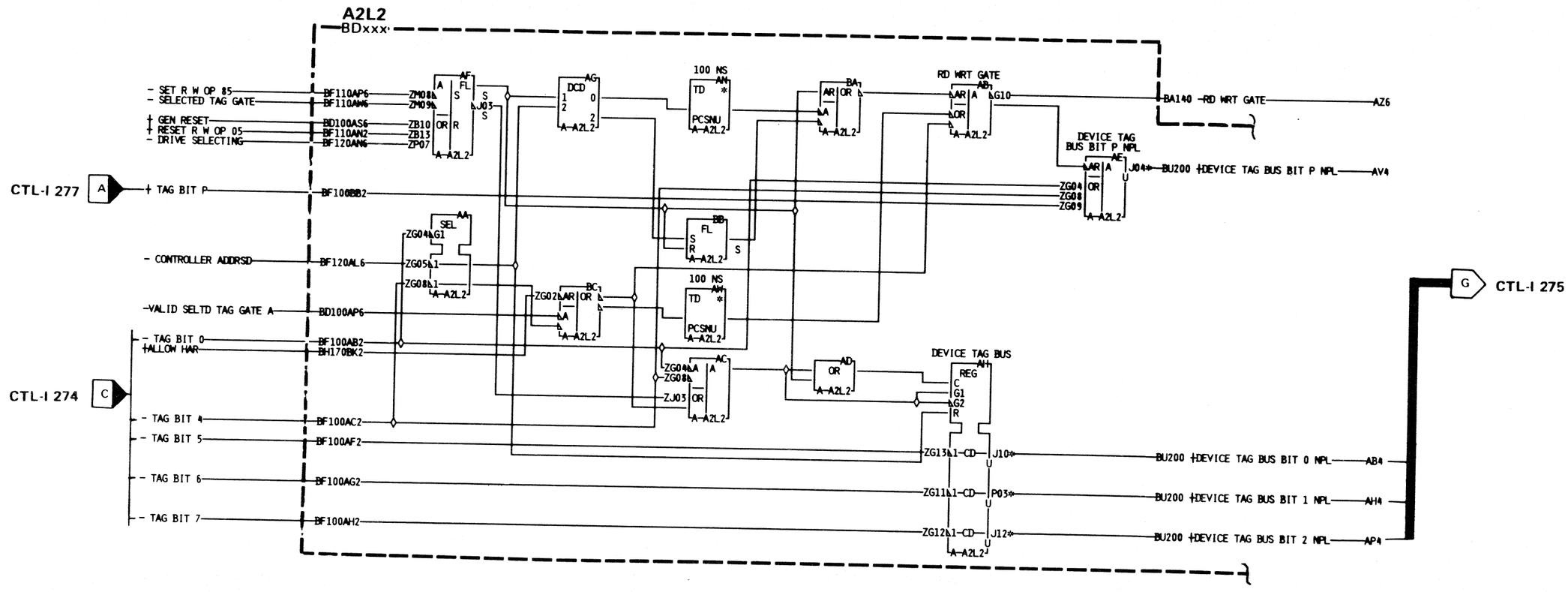
CONTROLLER – A2 MODULE



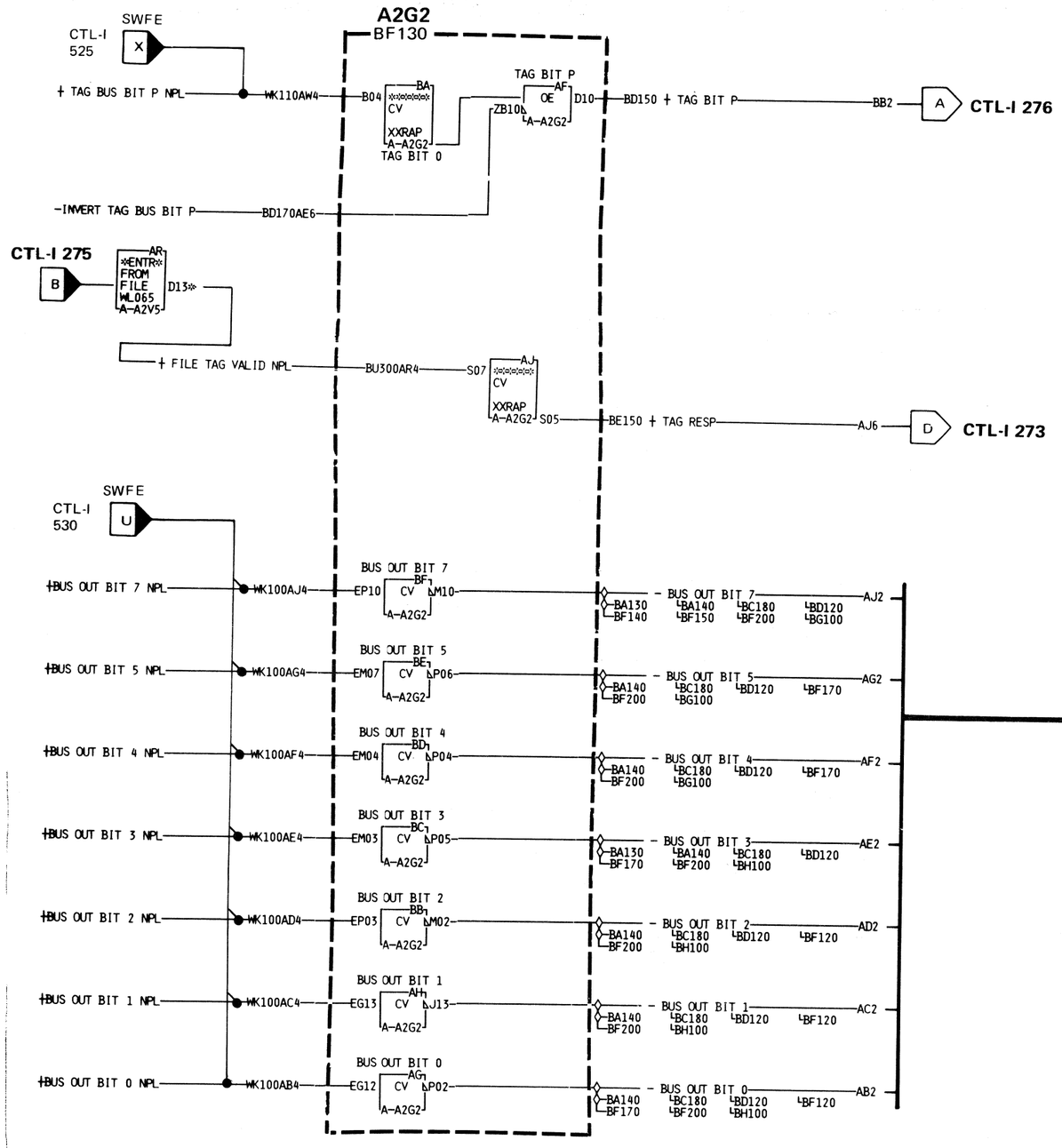
	Line Name	3340 ALD	3340 Test Point	3344 ALD	3344 Test Point
B	+NPL Outbus Bit 0	KA010	A1C2 G09	KK100 (KL110)	A1K2 (A1N2) M07
B	+NPL Outbus Bit 1	KA020	A1C2 B13	KK110 (KL110)	A1K2 (A1N2) U11
B	+NPL Outbus Bit 2	KA020	A1C2 J02	KK110 (KL110)	A1K2 (A1N2) U12
B	+NPL Outbus Bit 3	KA020	A1C2 D13	KK110 (KL110)	A1K2 (A1N2) S11
B	+NPL Outbus Bit 4	KA020	A1C2 B04	KK110 (KL110)	A1K2 (A1N2) U04
B	+NPL Outbus Bit 5	KA020	A1C2 B03	KK110 (KL110)	A1K2 (A1N2) S04
B	+NPL Outbus Bit 6	KA020	A1C2 D03	KK110 (KL110)	A1K2 (A1N2) S02
B	+NPL Outbus Bit 7	KA010	A1C2 J11	KK100 (KL100)	A1K2 (A1N2) M09
C	+NPL Outbus Bit P	KA020	A1C2 D04	KK110 (KL110)	A1K2 (A1N2) U03
C	+NPL Tagbus 0	KA010	A1C2 U03	KK100 (KL100)	A1K2 (A1N2) J05
C	+NPL Tagbus 1	KA010	A1C2 S02	KK100 (KL100)	A1K2 (A1N2) G03
C	+NPL Tagbus 2	KA010	A1C2 U02	KK100 (KL100)	A1K2 (A1N2) G05
C	+NPL Tagbus P	KA010	A1C2 S03	KK100 (KL100)	A1K2 (A1N2) G04
C	+NPL Select Hold	KA010	A1C2 G10	KK100 (KL100)	A1K2 (A1N2) M08
C	+NPL Tag Gate	KA010	A1C2 J10	KK100 (KL100)	A1K2 (A1N2) P09
D	+Enable Functions	KA100	A1C2 B10	KK150 (KL150)	A1K2 (A1N2) G10
E	+NPL Tag Valid	KK020	A1D2 J07	KK140 (KL140)	A1K2 (A1N2) B07

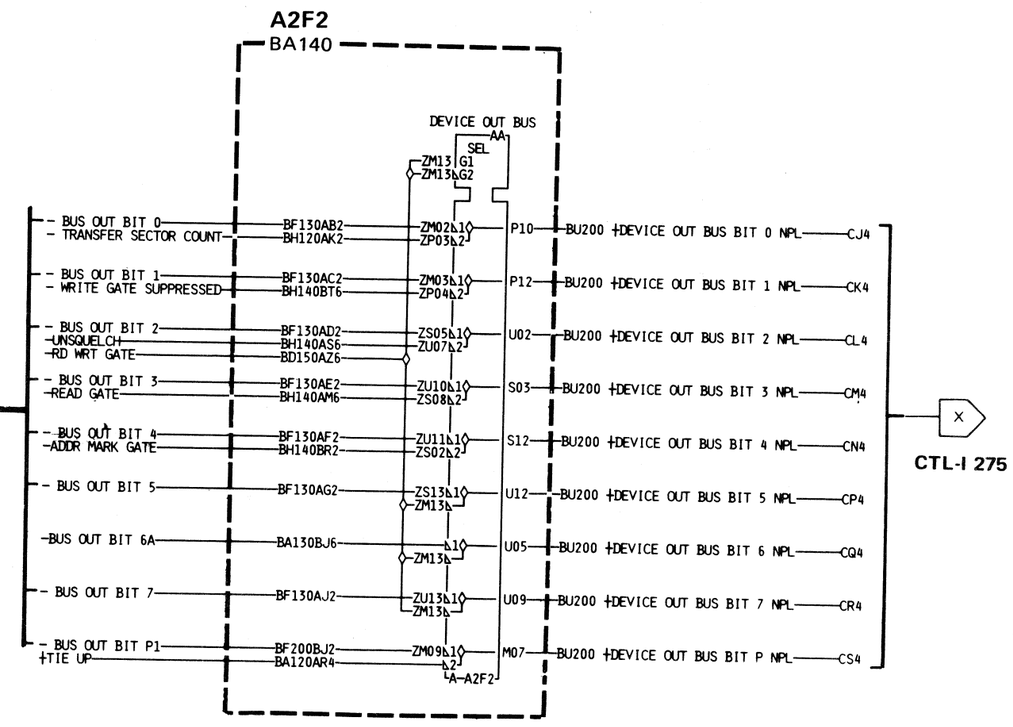
	Line Name	ALD	Test Point
A	+Device Tag Bus Bit 0	BD220	A1L2 J10
A	+Device Tag Bus Bit 1	BD220	A1L2 P03
A	+Device Tag Bus Bit 2	BD220	A1L2 J12
A	+Device Tag Bus Bit P	BD220	A1L2 J04
A	+Device Select Hold	BD230	A1L2 M03
A	+Device Tag Gate	BD230	A1L2 J02

NO RESPONSE DURING CONTROL OPERATION



NO RESPONSE DURING CONTROL OPERATION





BQ0276	2747699	440203	440213	440224				
Seq. 2 of 2	Part No.( )	2 Nov 73	13 May 74	15 Dec 75				

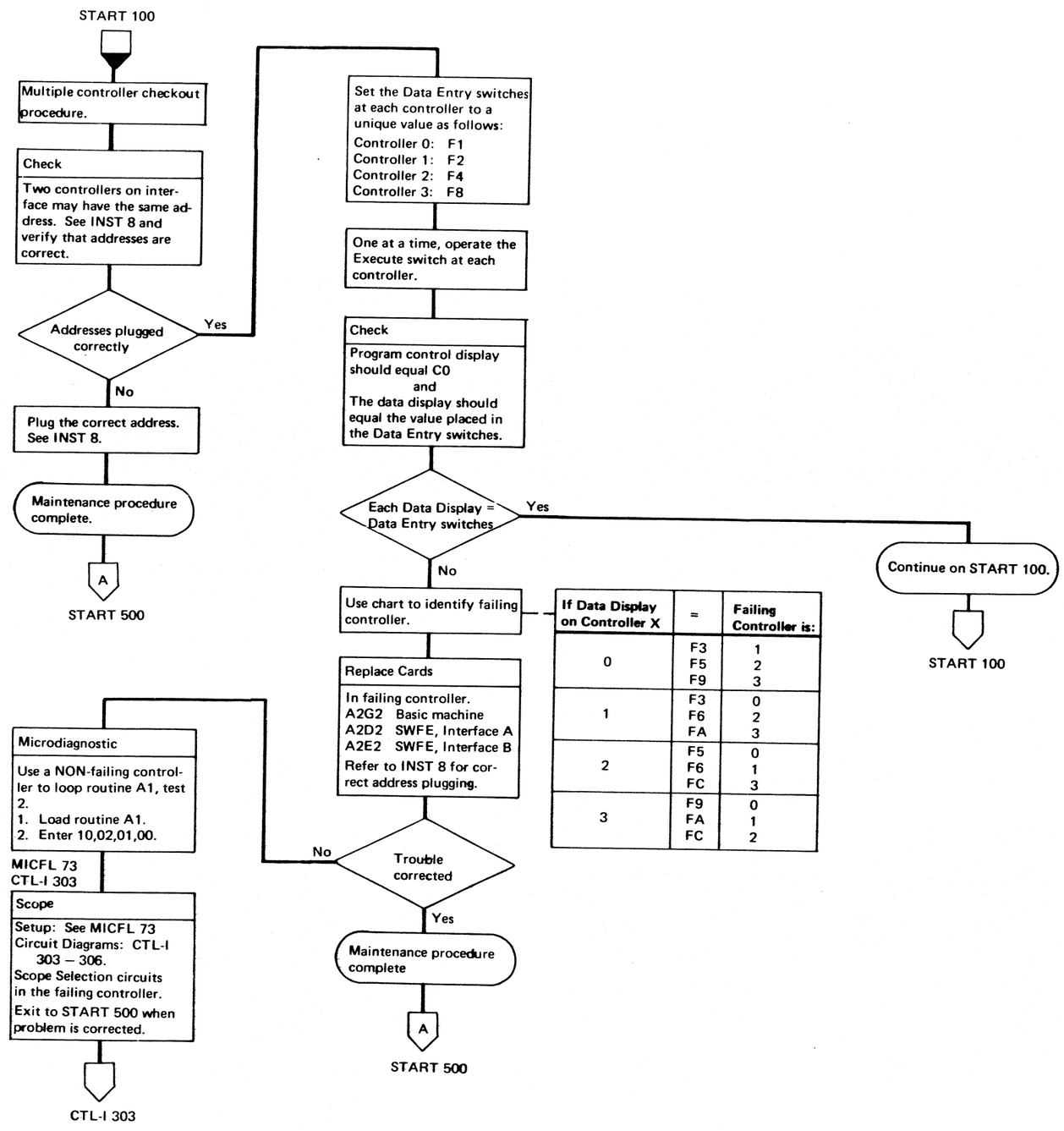
MULTIPLE CONTROLLER CHECKOUT PROCEDURE

When two controllers with the same address respond to selection on the same storage control, their responses are identical. It is impossible for the storage control then to determine that more than one controller responded. Only on some subsequent operation, where different responses are possible, will the condition be detected.

Examples of errors which might be expected with multiple controllers selected are:

1. Invalid DM size bit combination (SC 191E).
2. Storage control detected bus in parity errors.
3. Head switch timer expired (SC 9008).

This procedure establishes controlled conditions so that the results can be decoded to a failing unit(s).



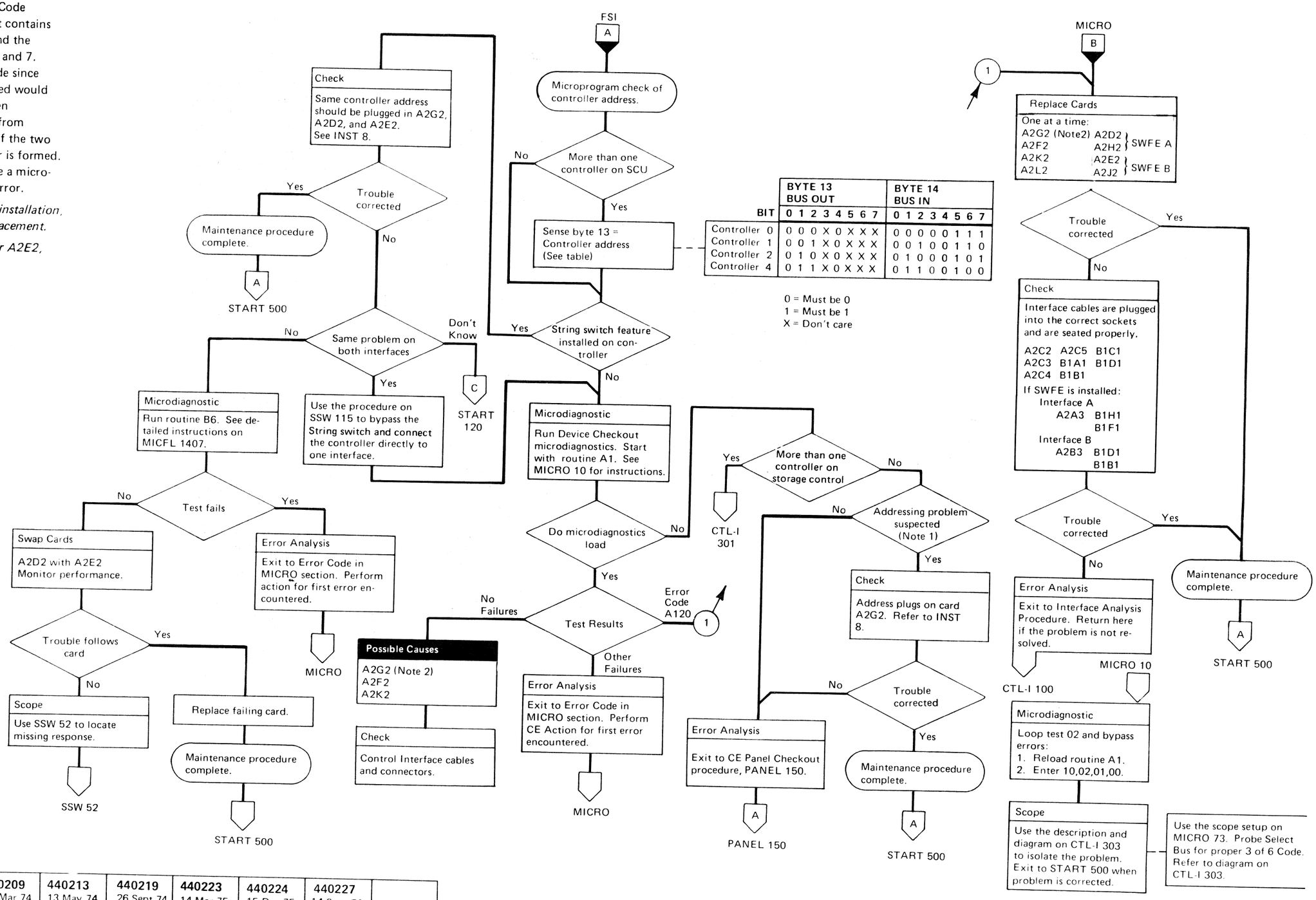
If Data Display on Controller X	=	Failing Controller is:
0	F3	1
	F5	2
	F9	3
1	F3	0
	F6	2
	FA	3
2	F5	0
	F6	1
	FC	3
3	F9	0
	FA	1
	FC	2

MICROPROGRAM CHECK OF CONTROLLER SELECTION

When a Controller is selected by an Op Code of 03 or 83, it responds with a byte that contains the Controller Address in Bits 0, 1, 2, and the complement of the Address in Bits 5, 6, and 7. This byte is referred to as the 3-of-6 Code since for any controller, 3 of the 6 bits involved would always be active. The microprogram then compares the byte received with a byte from storage that is unique for that address. If the two values do not compare, a Format 1 Error is formed. An '06' is encoded in Byte 18 to indicate a microprogram detected Controller Selection Error.

Note 1: Suspect addressing problem on installation, configuration change, or A2G2 card replacement.

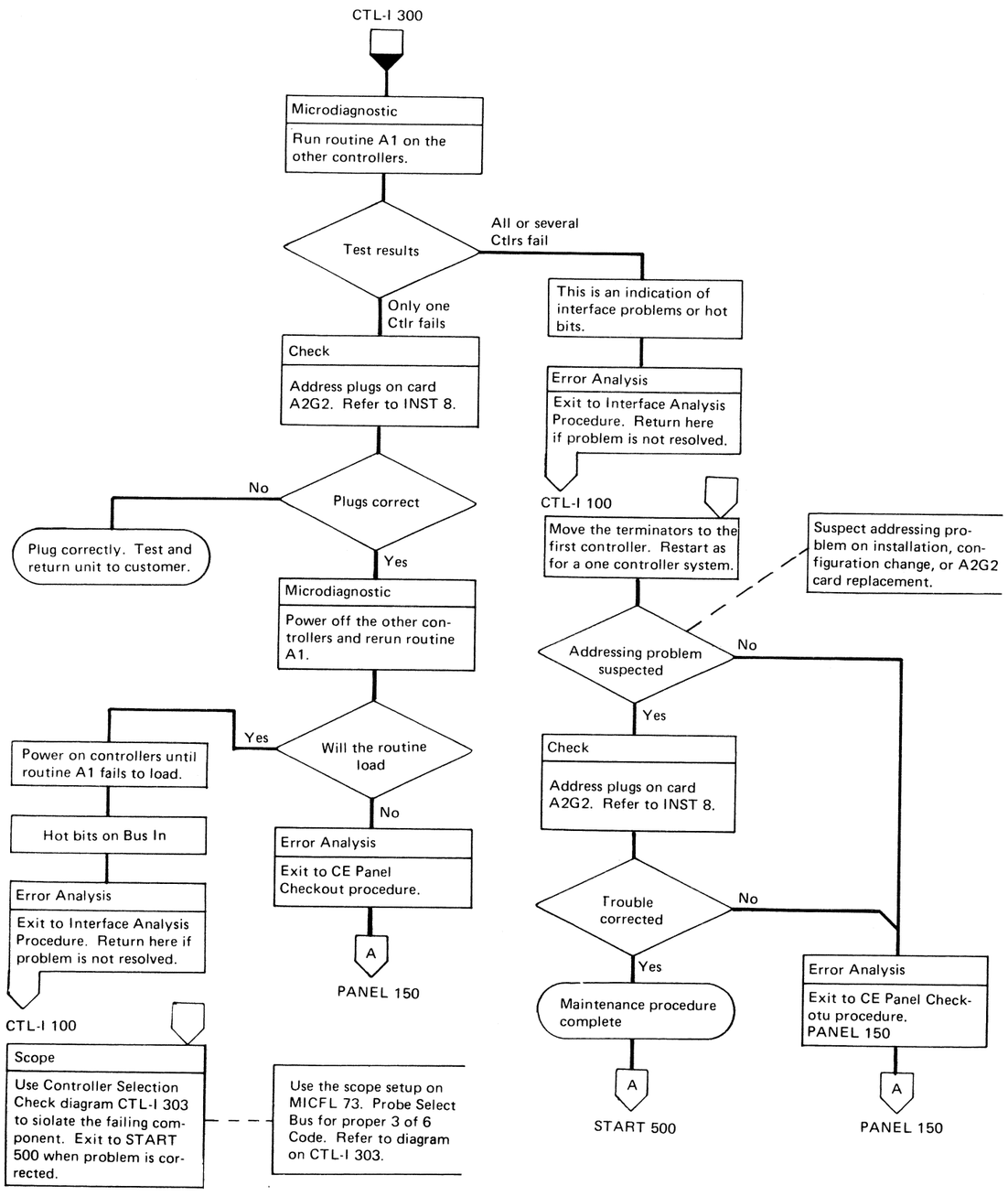
Note 2: When replacing A2G2, A2D2, or A2E2, check addressing jumpers. See INST 8.

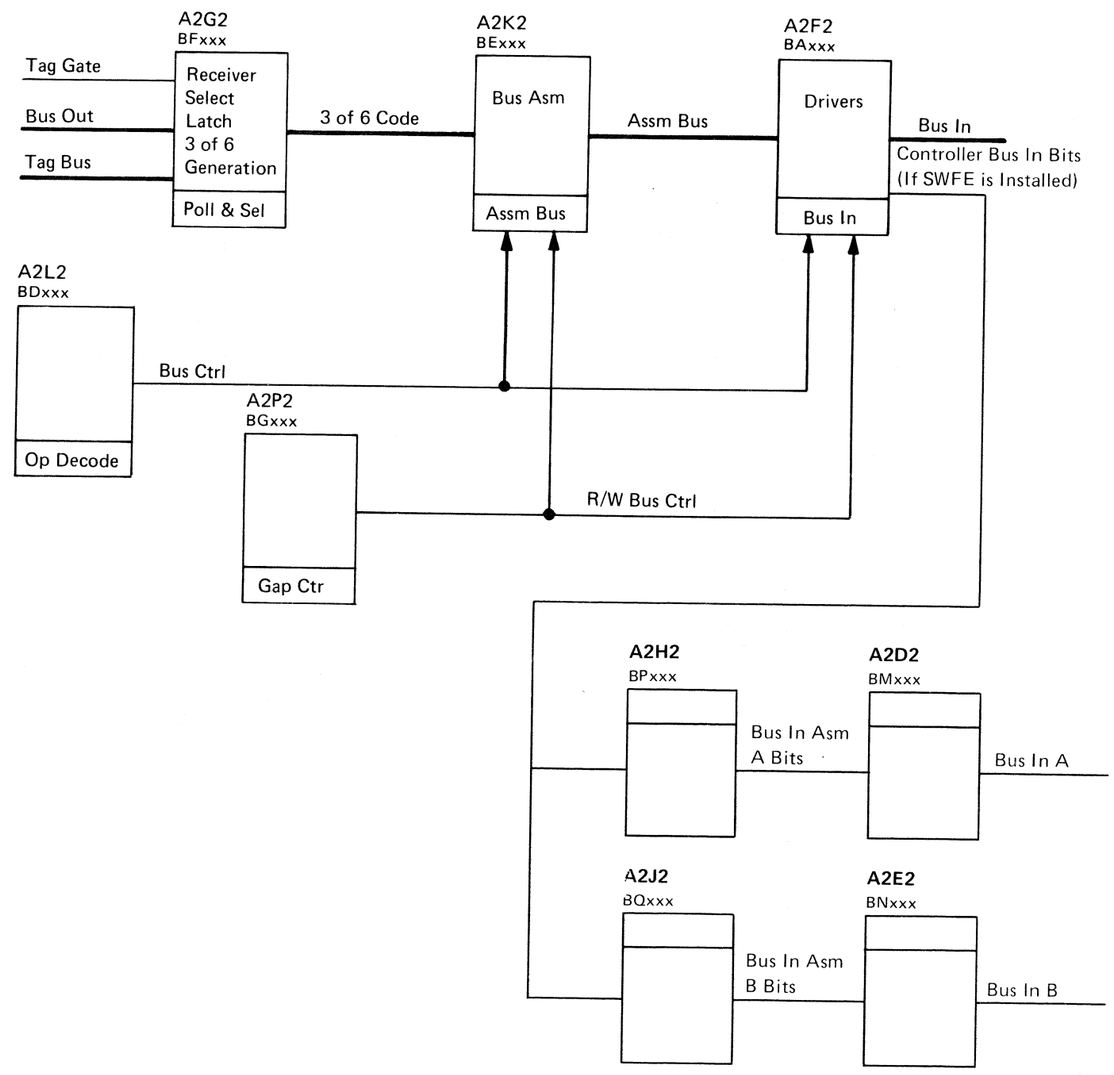


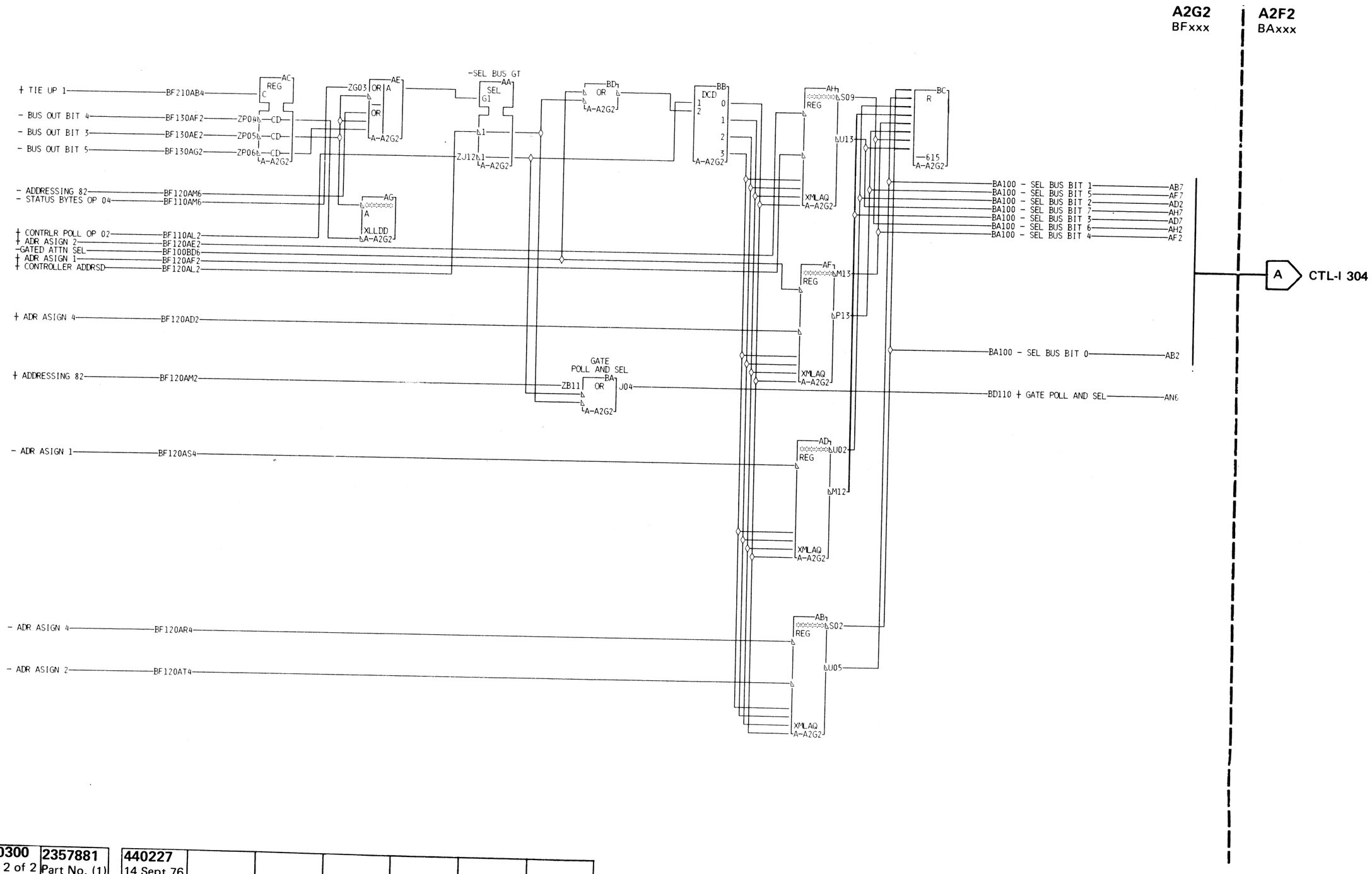
Possible Causes

A2G2
A2D2 (SWFE)
A2E2 (SWFE) (See Note 2)

MICROPROGRAM CHECK OF CONTROLLER SELECTION

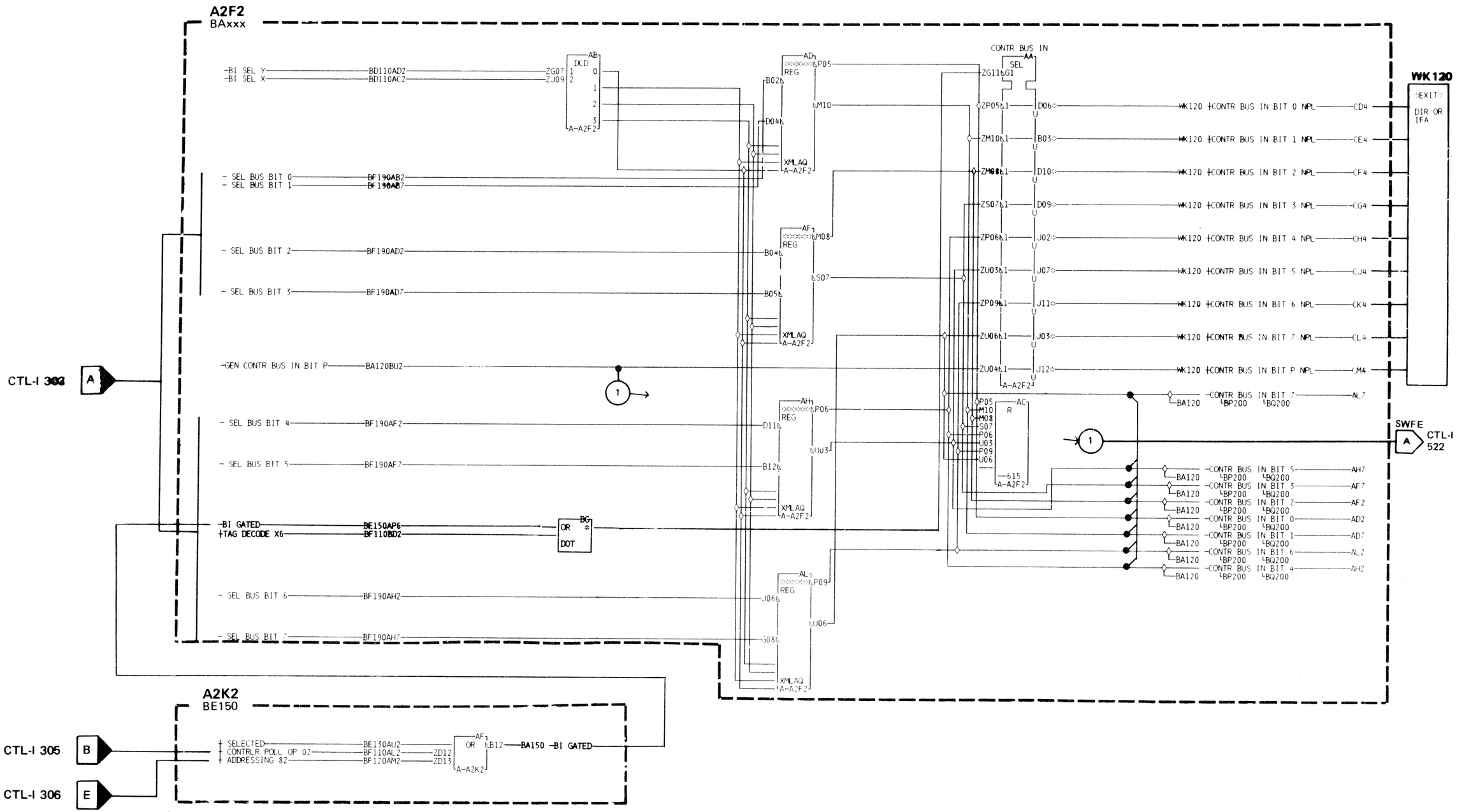


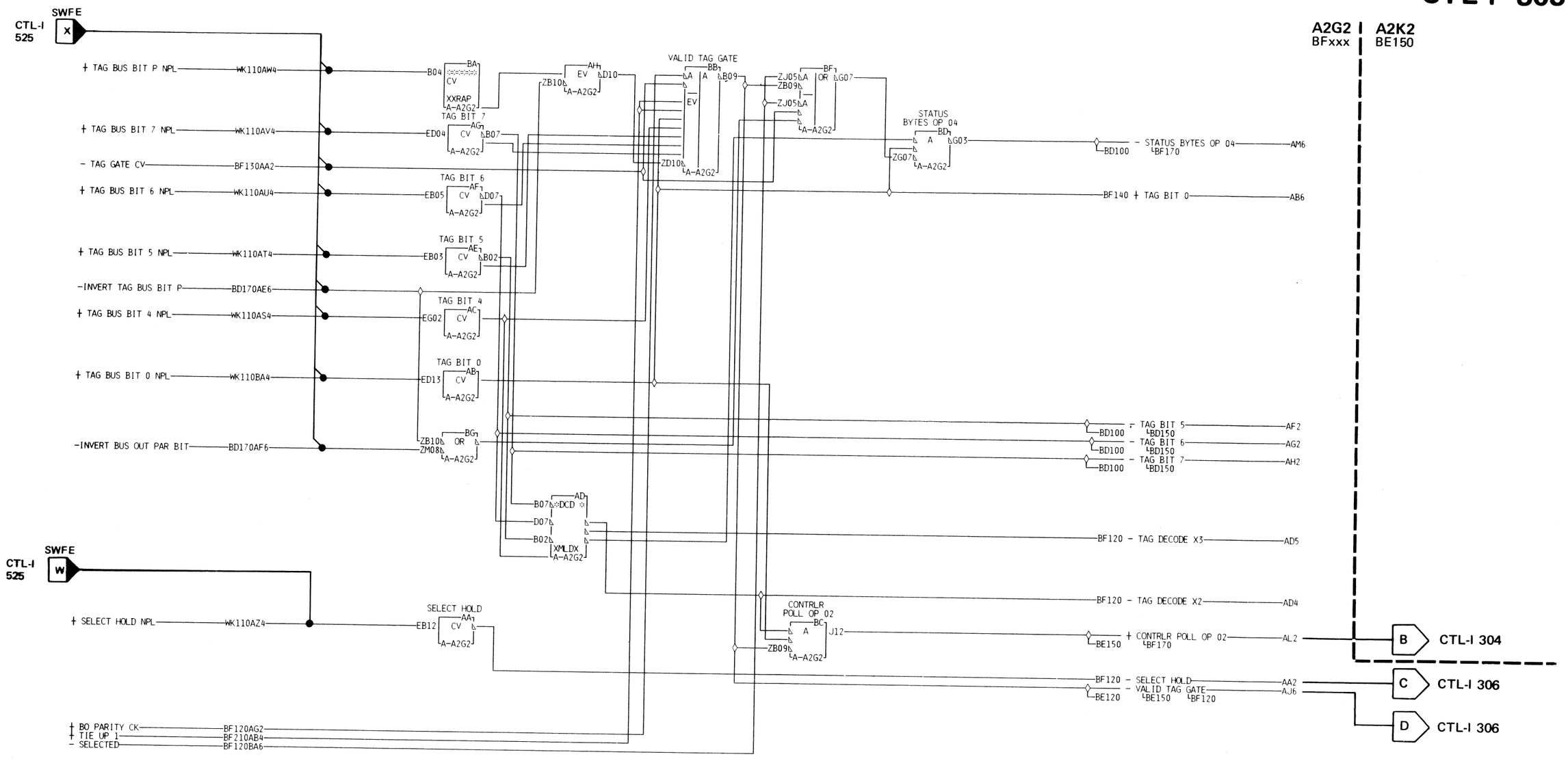




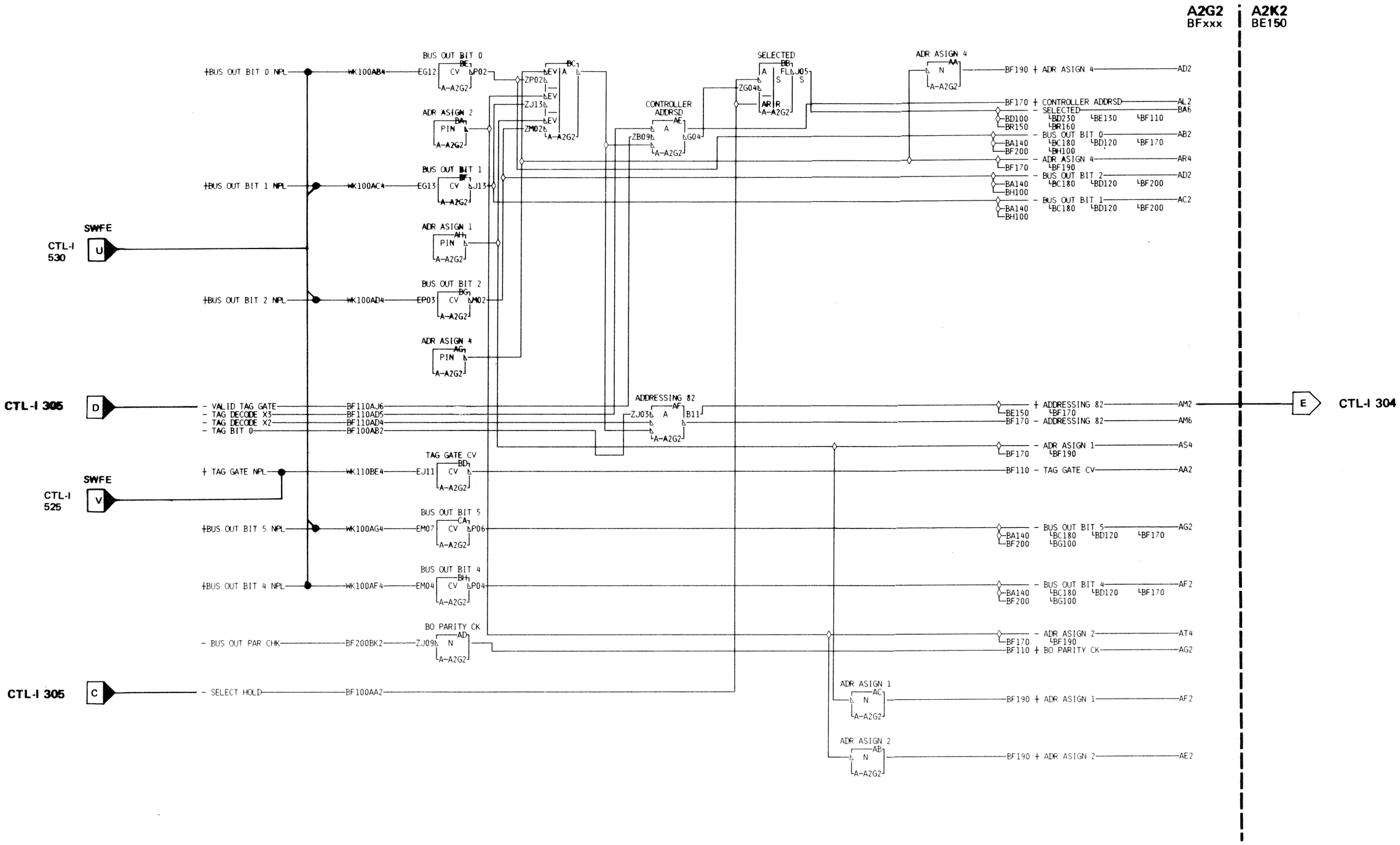
BQ0300	2357881	440227						
Seq. 2 of 2	Part No. (1)	14 Sept 76						

CONTROLLER SELECTION CHECK



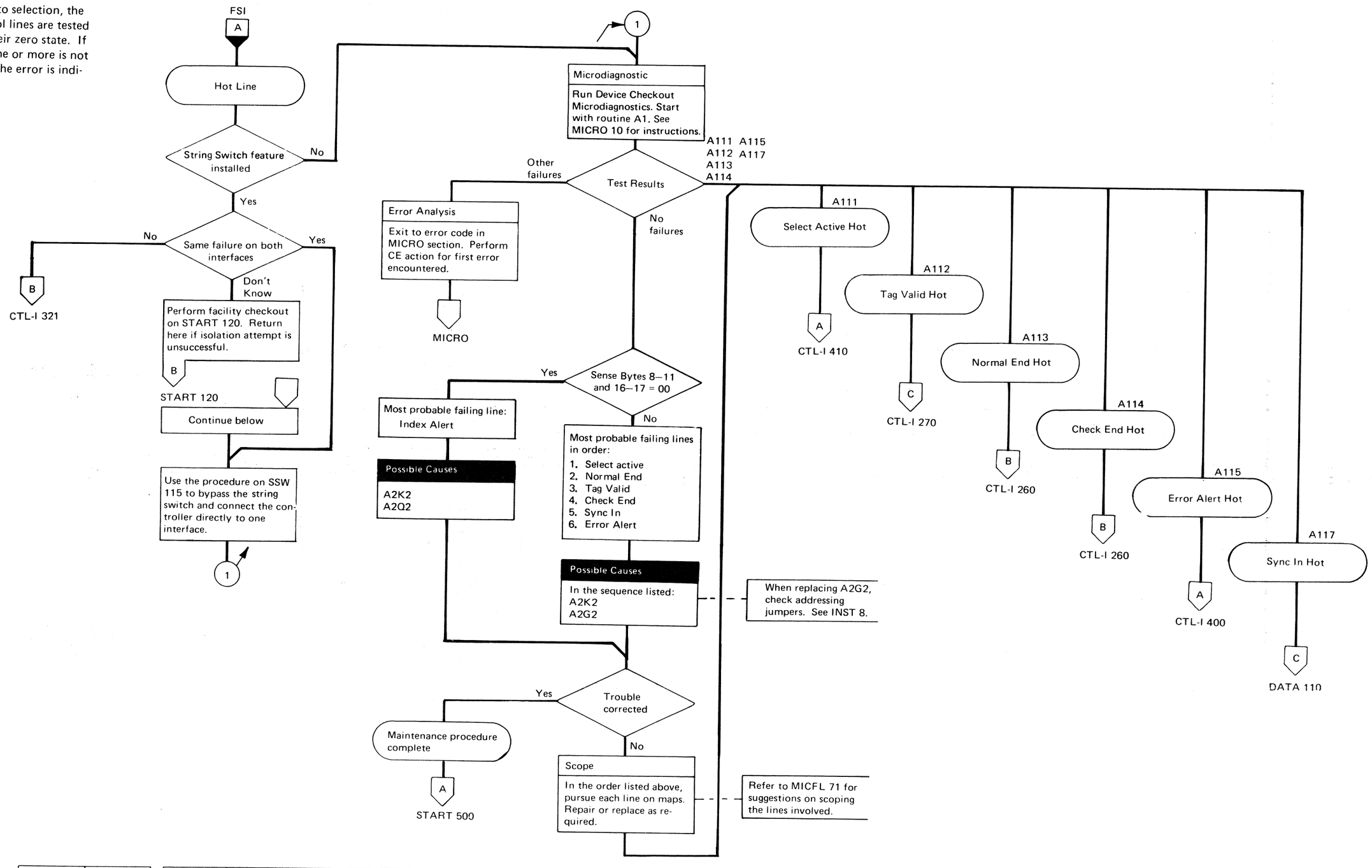


BQ0304	2747429	440200	440203	440204	440213			
Seq. 2 of 2	Part No. ( )	25 Jun 73	2 Nov 73	21 Dec 73	13 May 74			



HOT LINE TEST

Prior to selection, the control lines are tested for their zero state. If any one or more is not zero, the error is indicated.

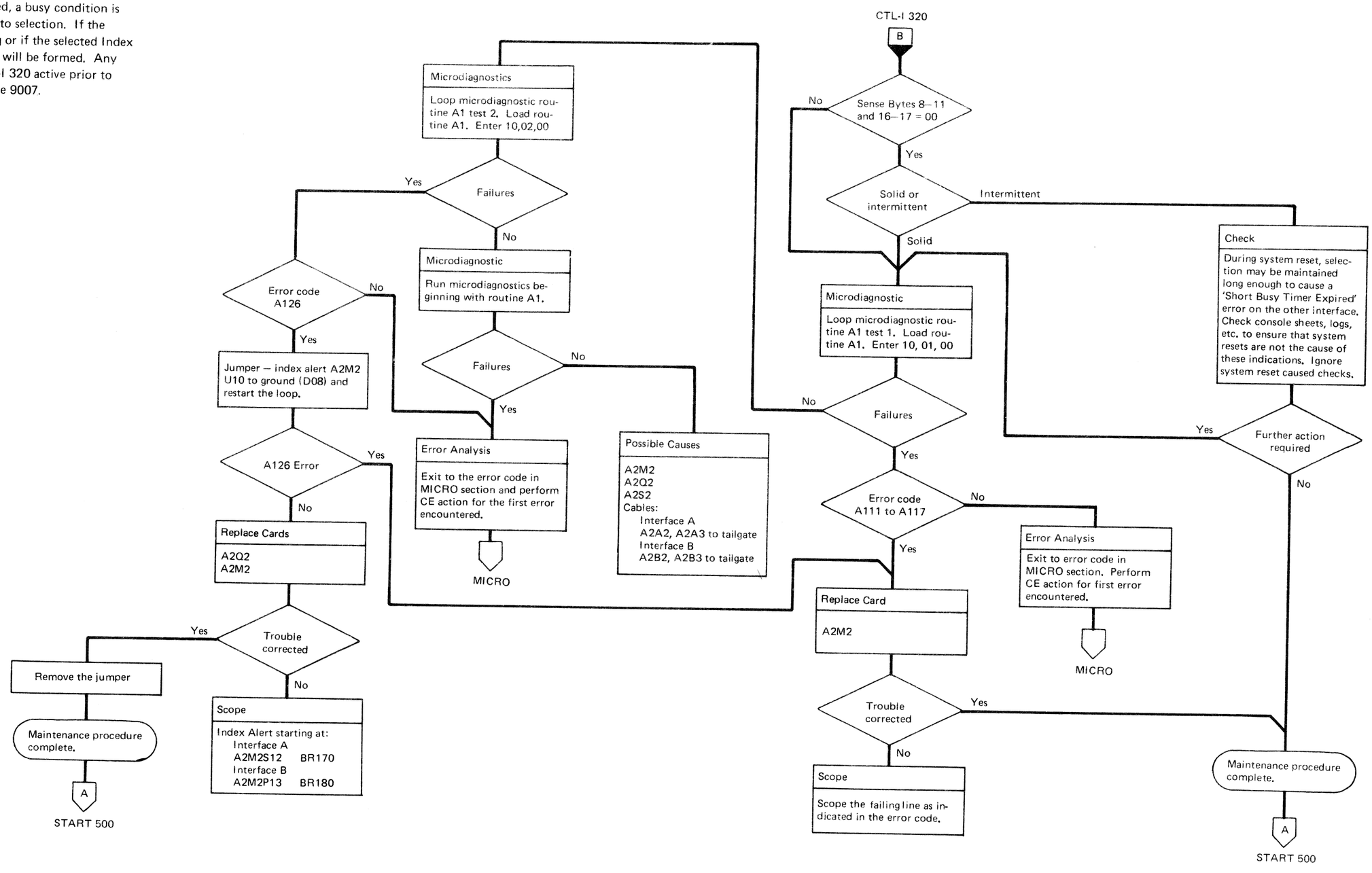


BQ0306	2747430
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440213	440218	440223	440224
25 Jun 73	7 Sept 73	2 Nov 73	13 May 74	5 Aug 74	14 Mar 75	15 Dec 75

HOT LINE OR SHORT BUSY TIMER EXPIRED

With the string switch feature installed, a busy condition is indicated by an Index Alert response to selection. If the busy condition is maintained too long or if the selected Index Alert line is hot, symptom code 9007 will be formed. Any of the control lines indicated on CTL-I 320 active prior to selection will also cause symptom code 9007.

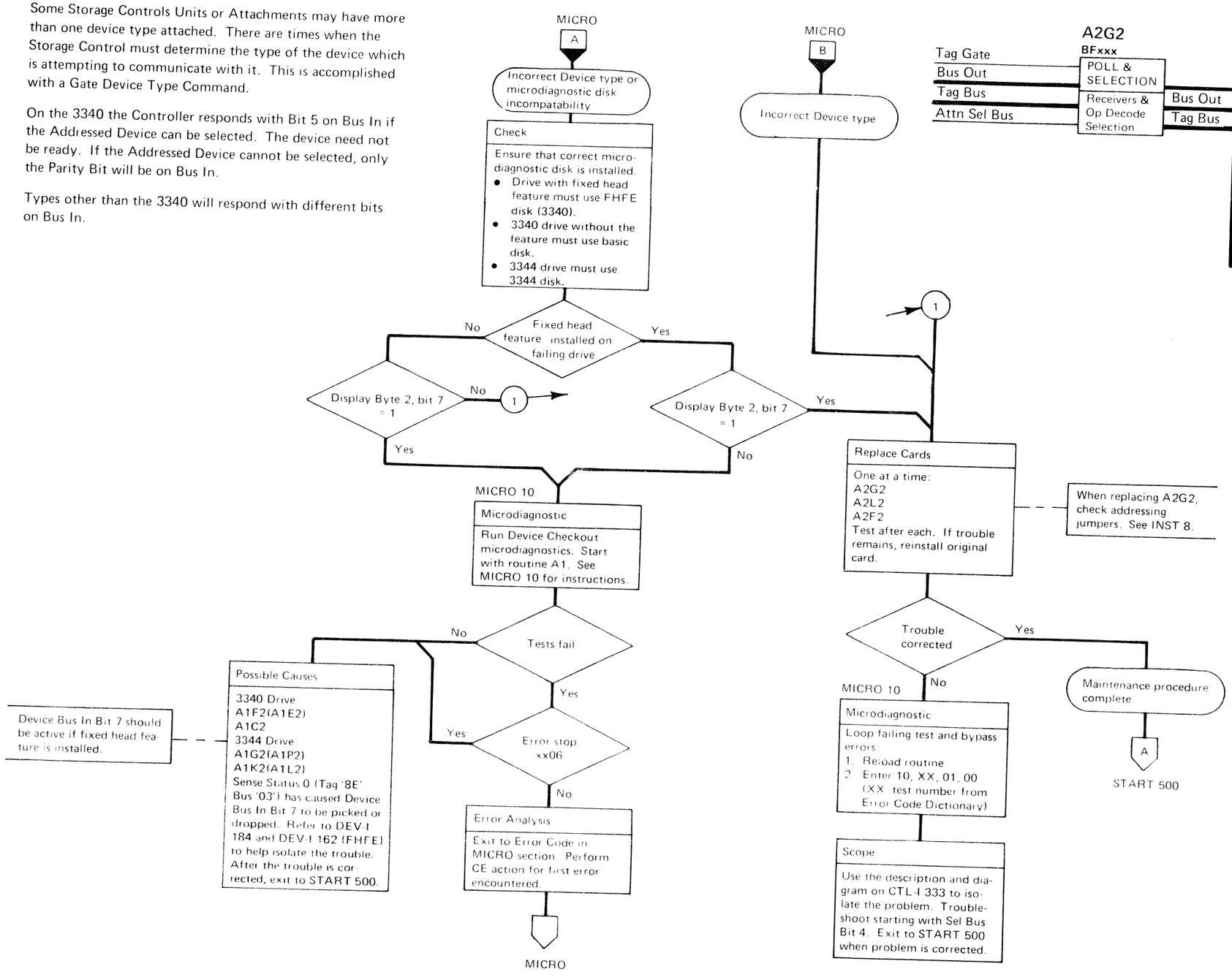


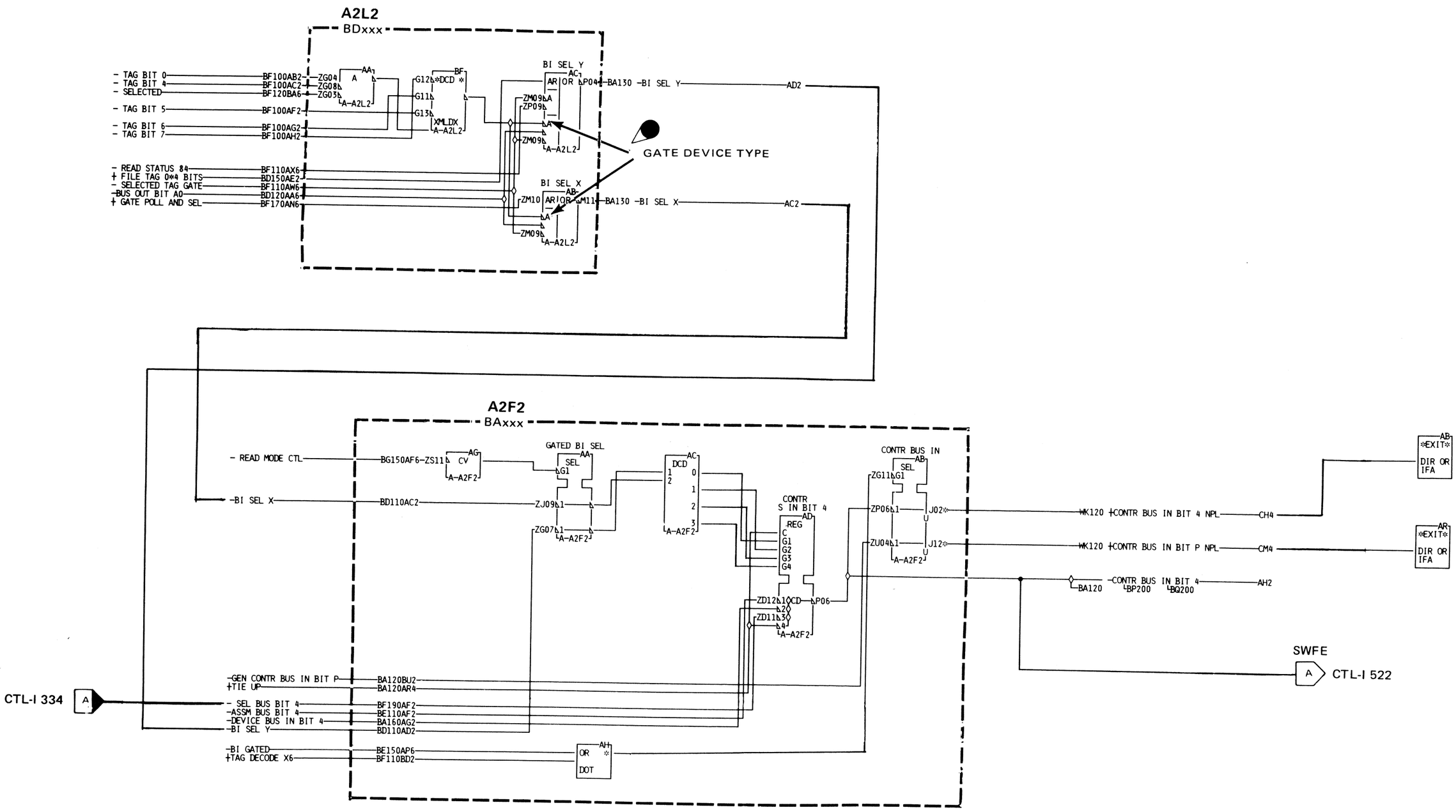
GATE DEVICE TYPE

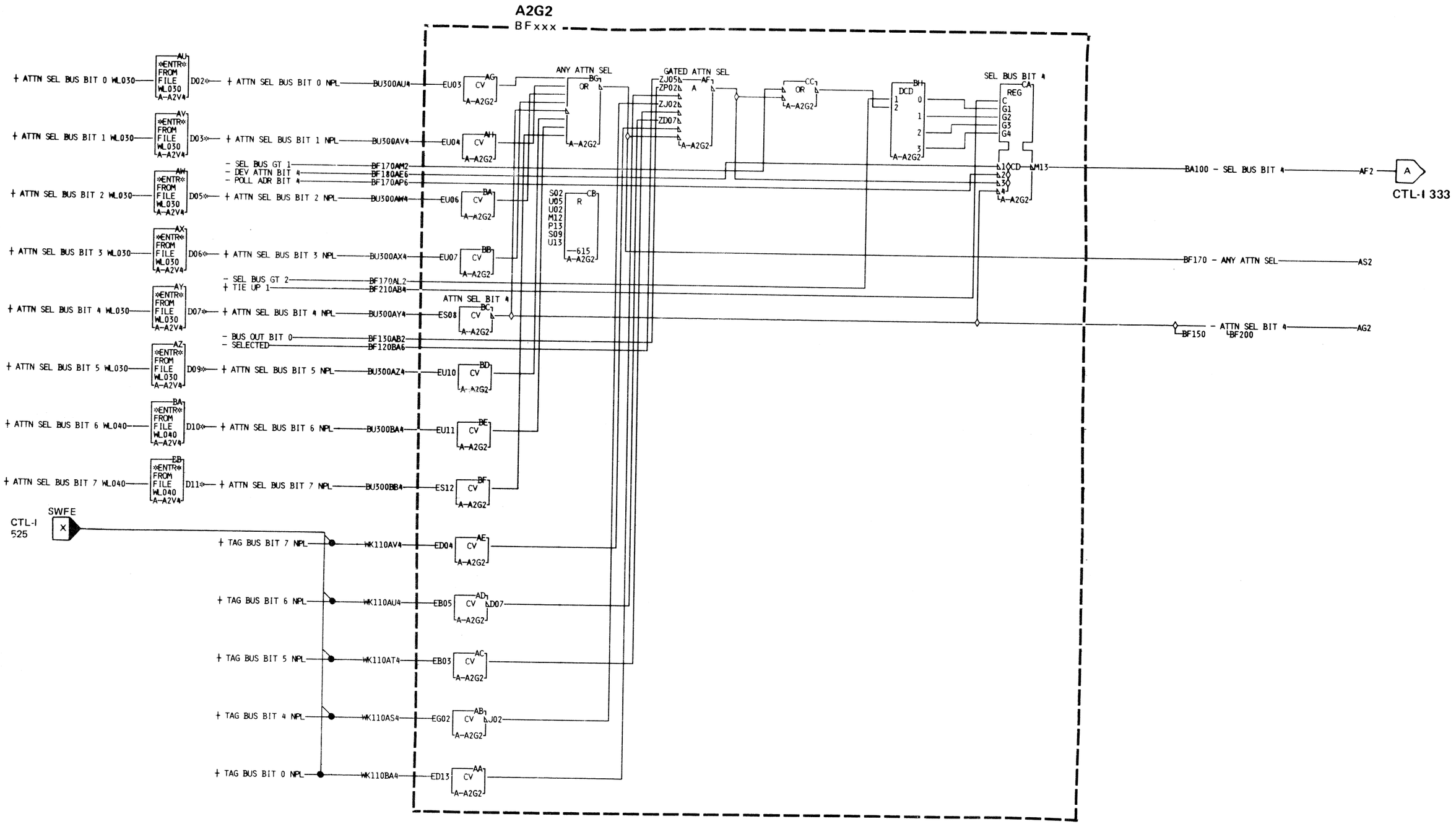
Some Storage Controls Units or Attachments may have more than one device type attached. There are times when the Storage Control must determine the type of the device which is attempting to communicate with it. This is accomplished with a Gate Device Type Command.

On the 3340 the Controller responds with Bit 5 on Bus In if the Addressed Device can be selected. The device need not be ready. If the Addressed Device cannot be selected, only the Parity Bit will be on Bus In.

Types other than the 3340 will respond with different bits on Bus In.







Note: Disregard this page if String Switch feature is installed.

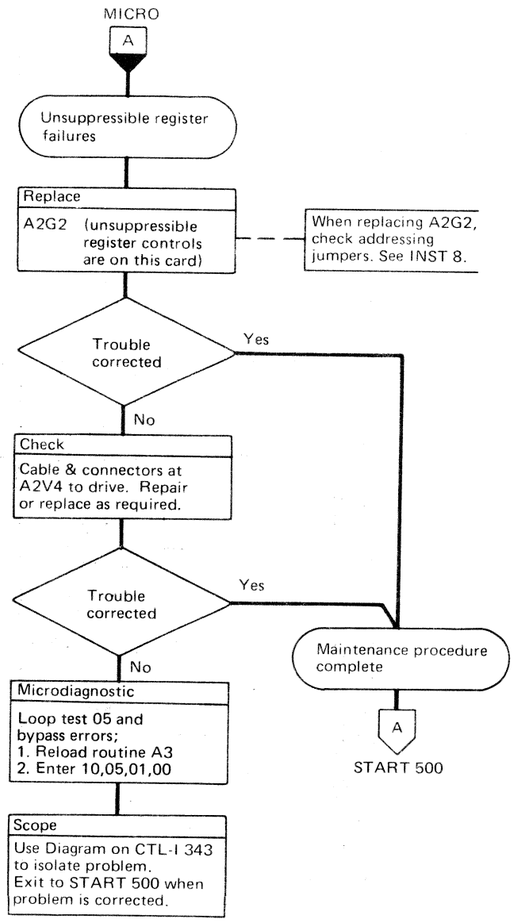
The unsuppressible register is a means by which the control unit can selectively poll for device attentions. The unsuppressible register positions are set and reset individually under control of operation code '01'.

The unsuppressible register has no effect on normal polling during Poll device (op '82') with Bus Out bit 3 equal to 0. When Bus Out bit 3 equals 1, however, only attention bits that are equal to its unsuppressible register position are transmitted to the control unit. For example, if device 5 has an attention bit active and the unsuppressible register position 5 is off, there is no response to a Poll Unsuppressible operation. On the other hand, if the unsuppressible register for position 5 were on, an attention bit 5 is returned to the control unit in response to a Poll Unsuppressible operation.

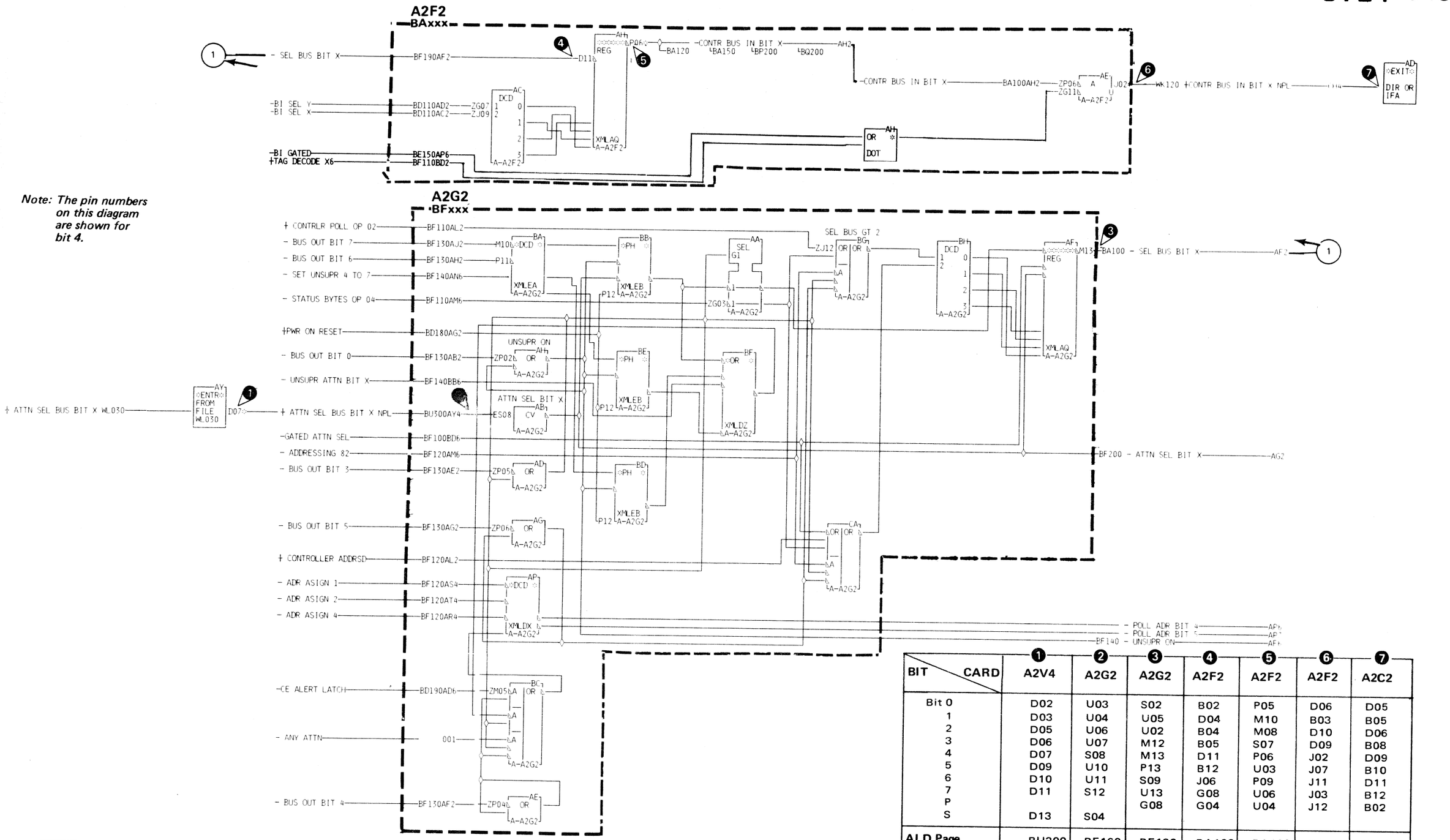
Possible Causes

A2G2 card
A2V4 cable

When replacing A2G2, check addressing jumpers. See INST 8.



BQ0334	2747700	440203	440213	440227			
Seq. 2 of 2	Part No. (1)	2 Nov 73	13 May 74	14 Sept 76			



BIT \ CARD	1 A2V4	2 A2G2	3 A2G2	4 A2F2	5 A2F2	6 A2F2	7 A2C2
Bit 0	D02	U03	S02	B02	P05	D06	D05
1	D03	U04	U05	D04	M10	B03	B05
2	D05	U06	U02	B04	M08	D10	D06
3	D06	U07	M12	B05	S07	D09	B08
4	D07	S08	M13	D11	P06	J02	D09
5	D09	U10	P13	B12	U03	J07	B10
6	D10	U11	S09	J06	P09	J11	D11
7	D11	S12	U13	G08	U06	J03	B12
P			G08	G04	U04	J12	B02
S	D13	S04					
ALD Page	BU300	BF160	BF190	BA100	BA100	BA150	WK110

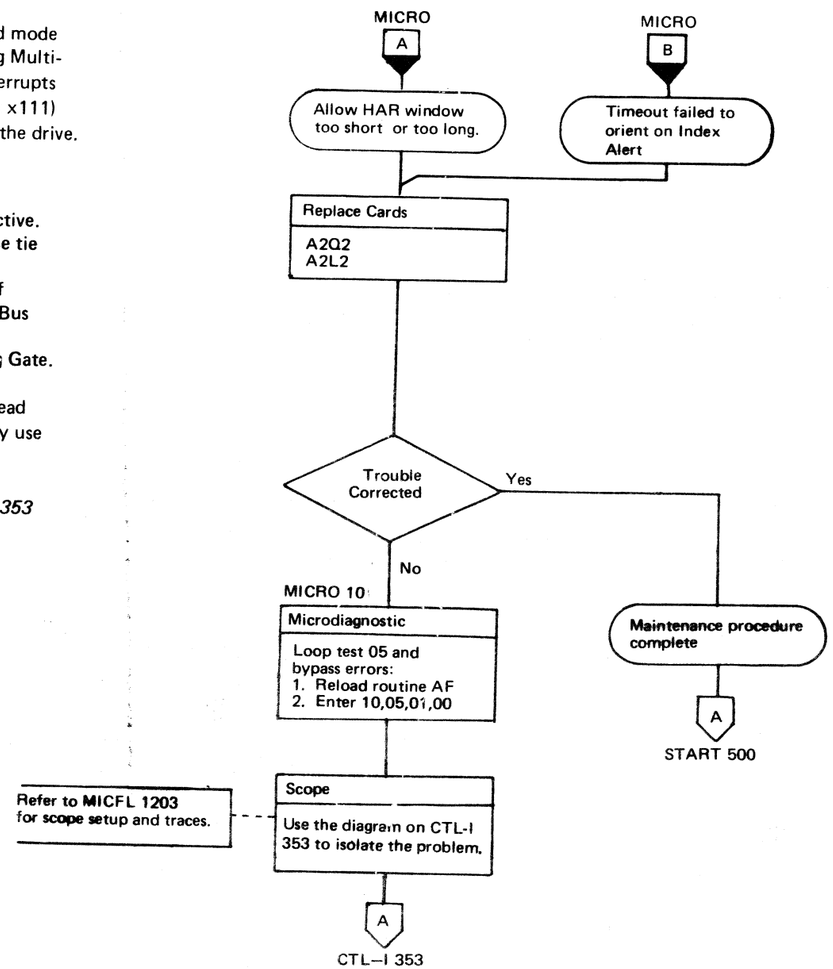
Allow HAR is generated during index range when in read mode to allow the Head Address register to be advanced during Multi-Track and Record Overflow operations. Allow HAR interrupts the Set Read Write values (Dev Tag '07', Bus Out = xxxx x111) and allows the Set HAR bus and tag values to be sent to the drive.

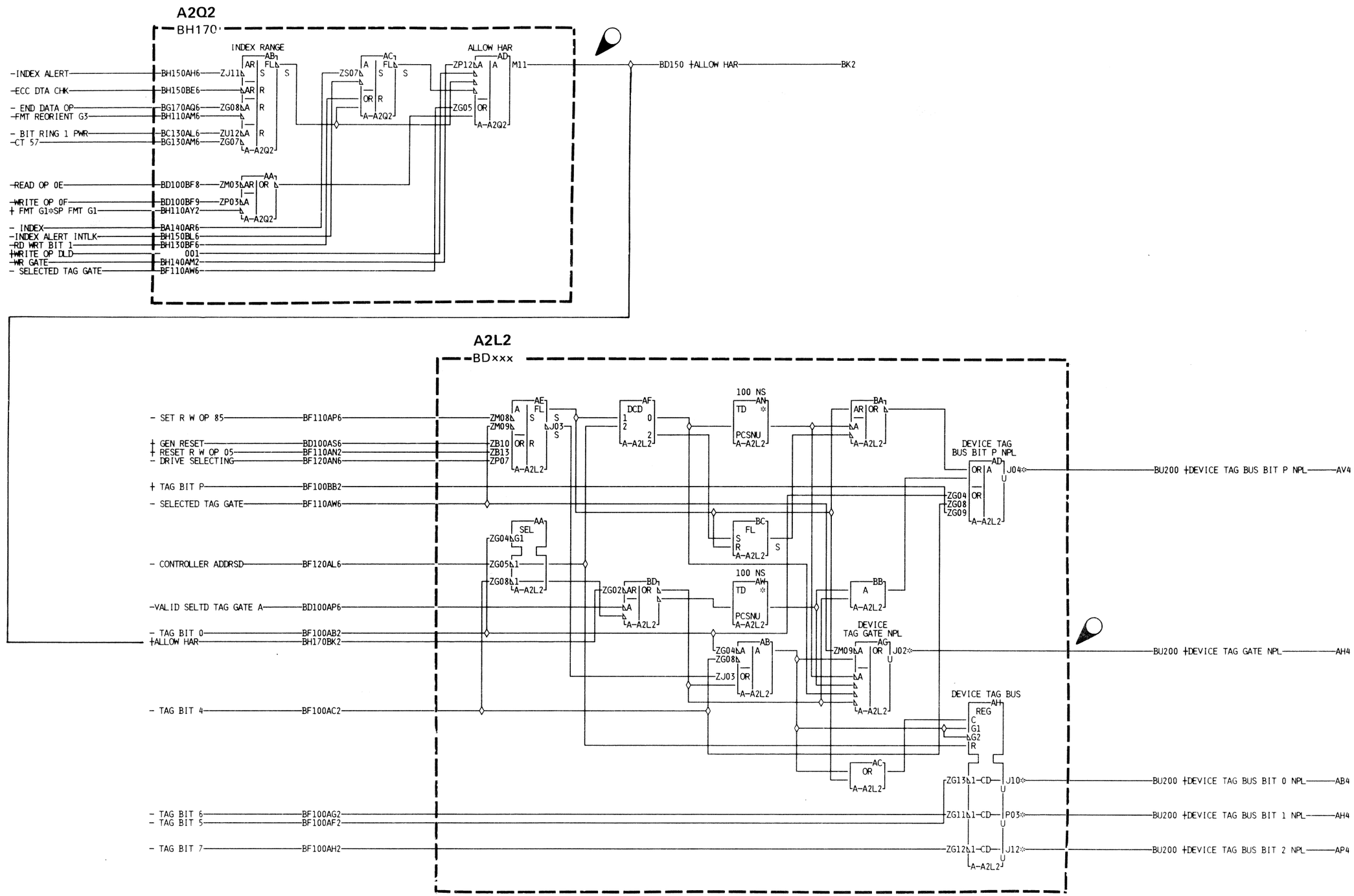
Allow HAR functions:

A. Prevents the RW latch from holding Tag Gate active.
B. Transfers control of the Device Tag Bus from the tie down to the Tag bus bit 5, 6, and 7.
C. Drops Rd Wr Gate which will transfer control of Device Bus Out from the read write controls to Bus Out bits 0-7.
D. Permits Selected Tag Gate to control Device Tag Gate.

These controls would ordinarily be used to advance the head address on a Multi Track or Record Overflow operation by use of Set HAR tag '8B'.

See OPER 101 and 105 for description of tags and CTL-I 353 for logic diagram.





Check Circuits

The Bus Out Parity Check monitors the bits on the Control Bus Out. While Tag Gate is active, an even number of bits perform the following actions:

1. Set Bus Out Parity Check latch.
2. Block Tag Valid.
3. Inhibit Normal End.
4. Set Bus Our Parity Check display latch.
5. Activate Error Alert and Controller Check.

During a selection sequence, a Bus Out Parity Check prevents selection of the Controller by blocking the Valid Tag Gate signal.

Indicator (Control Module CE Panel)

The Bus Our Parity Check lamp indicates until reset by the Execute Switch or Power On Peset. Microdiagnostic Routine A1 Test 3 tests the Bus Out Parity Check latch. The Bus Out Parity Check indicator should be on after running the test and remain on until reset.

Possible Intermittent Failures

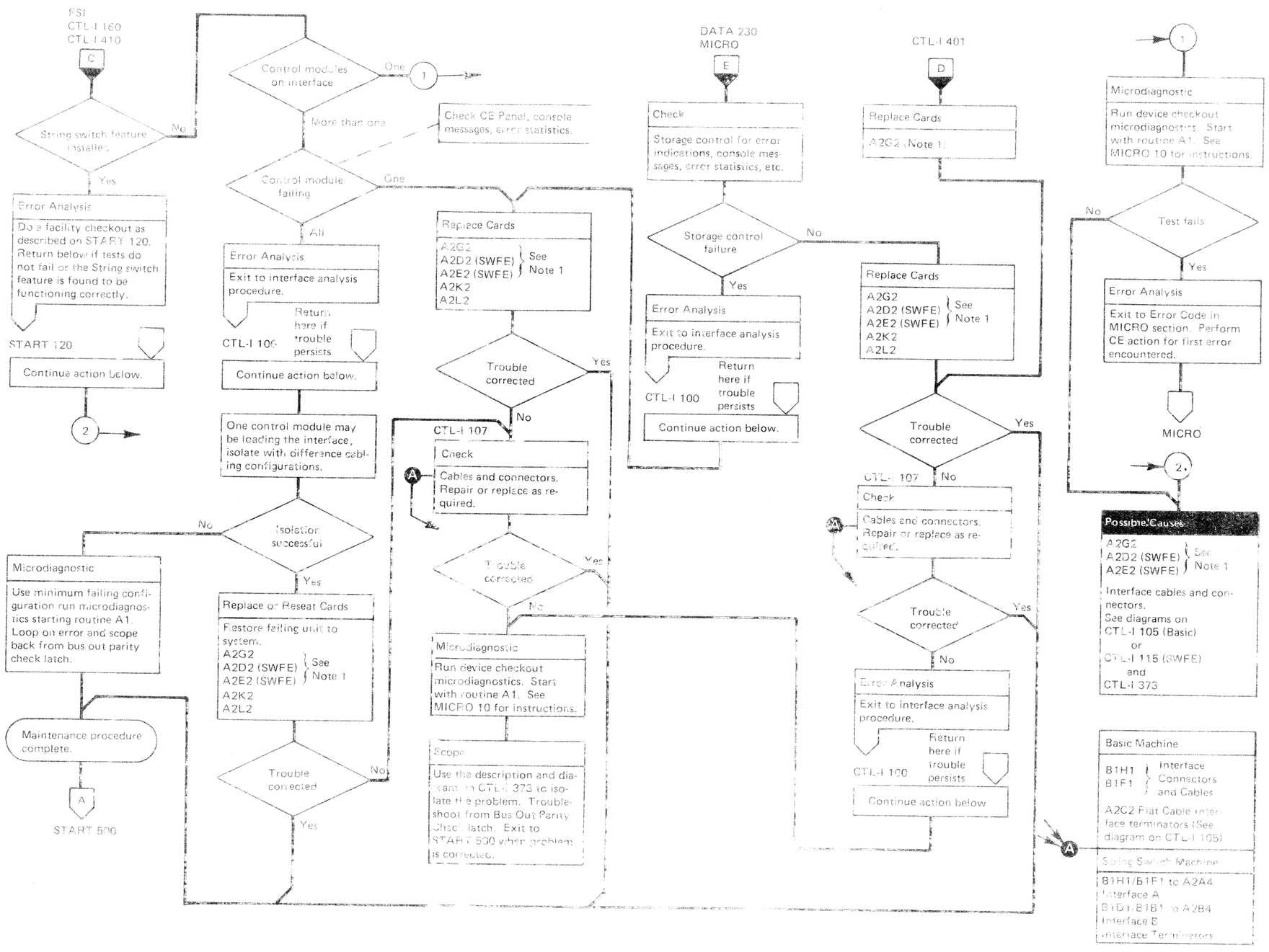
ALL CONTROL MODULES FAIL

1. The storage control unit.
2. Cable or connector from storage control to the first control module.
3. A line held inoperable by a cable or connector short or ground anywhere on the interface.

SINGLE UNIT FAILS

1. Card, voltage, back panel wiring, etc. in the failing unit.
2. Cable or connector fault at the input to failing unit.

Note 1: When replacing A2G2, A2D2, or A2E2, check addressing jumpers. See INST 8.



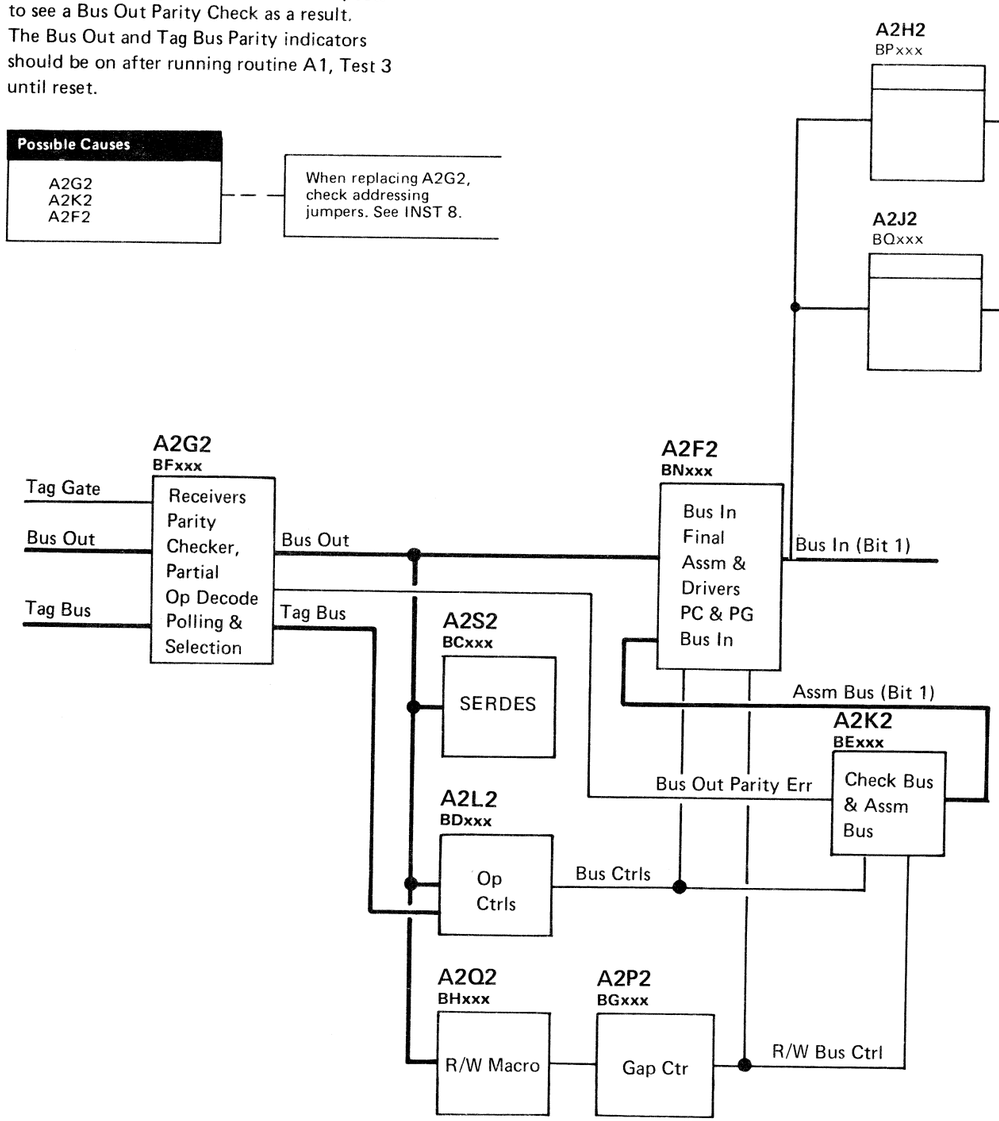
MISSING BUS OUT PARITY CHECK

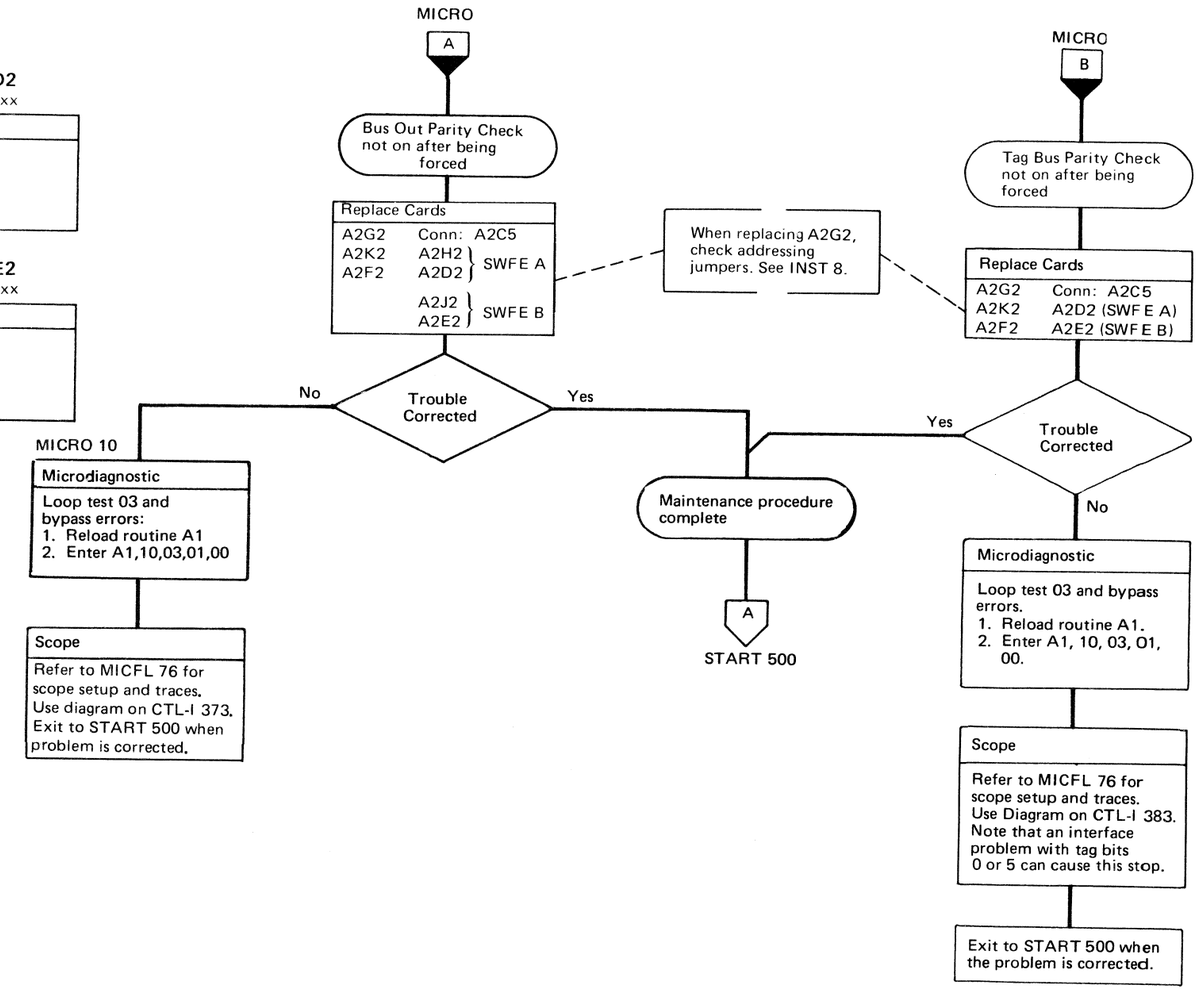
The microprogram changes the value on Bus Out while Tag Gate is active and expects to see a Bus Out Parity Check as a result. The Bus Out and Tag Bus Parity indicators should be on after running routine A1, Test 3 until reset.

Possible Causes

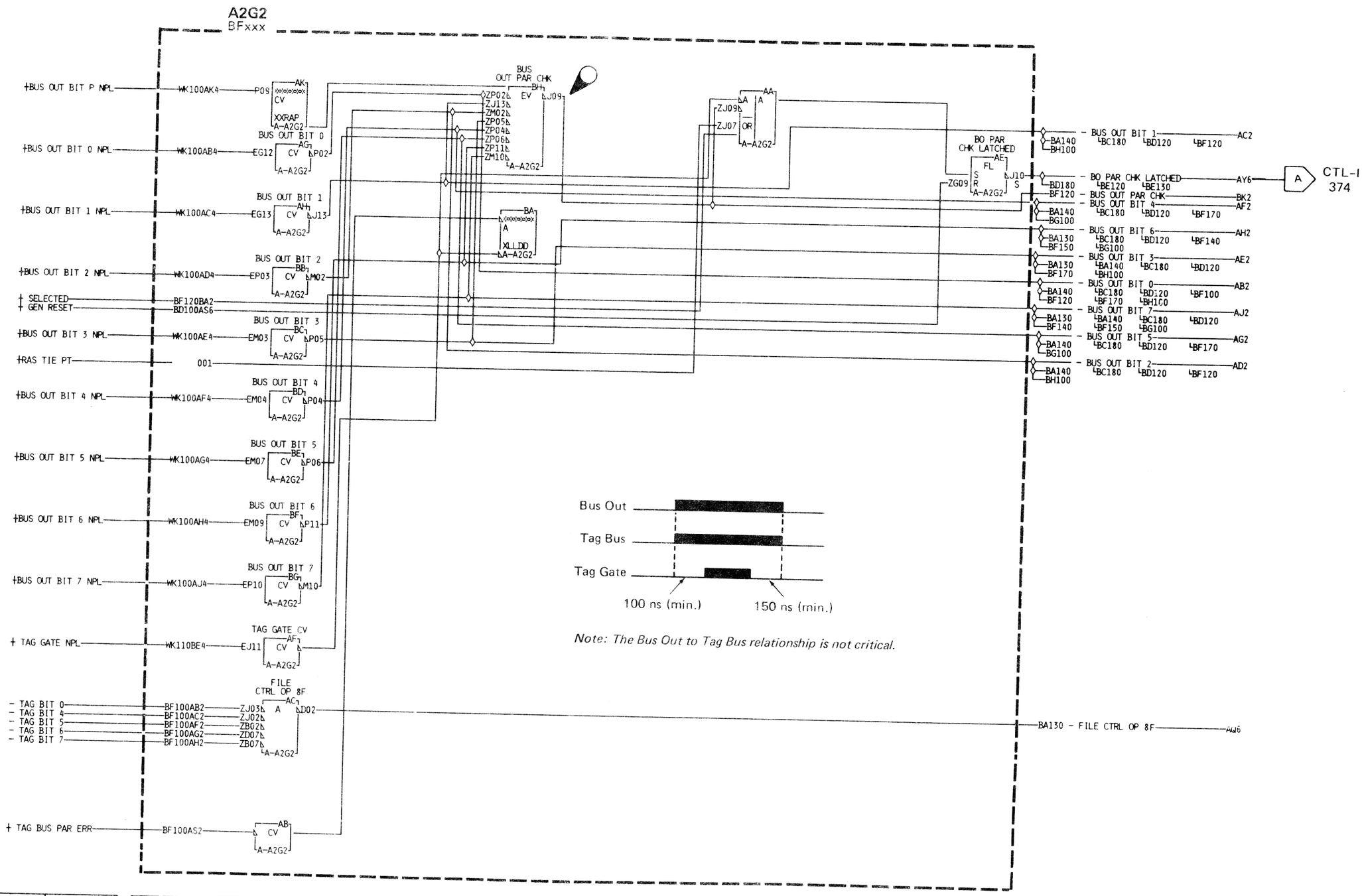
A2G2
A2K2
A2F2

When replacing A2G2, check addressing jumpers. See INST 8.





BQ0371	2747529	See EC History	440224	440227				
Seq. 1 of 2	Part No. (1)		15 Dec 75	14 Sept 76				

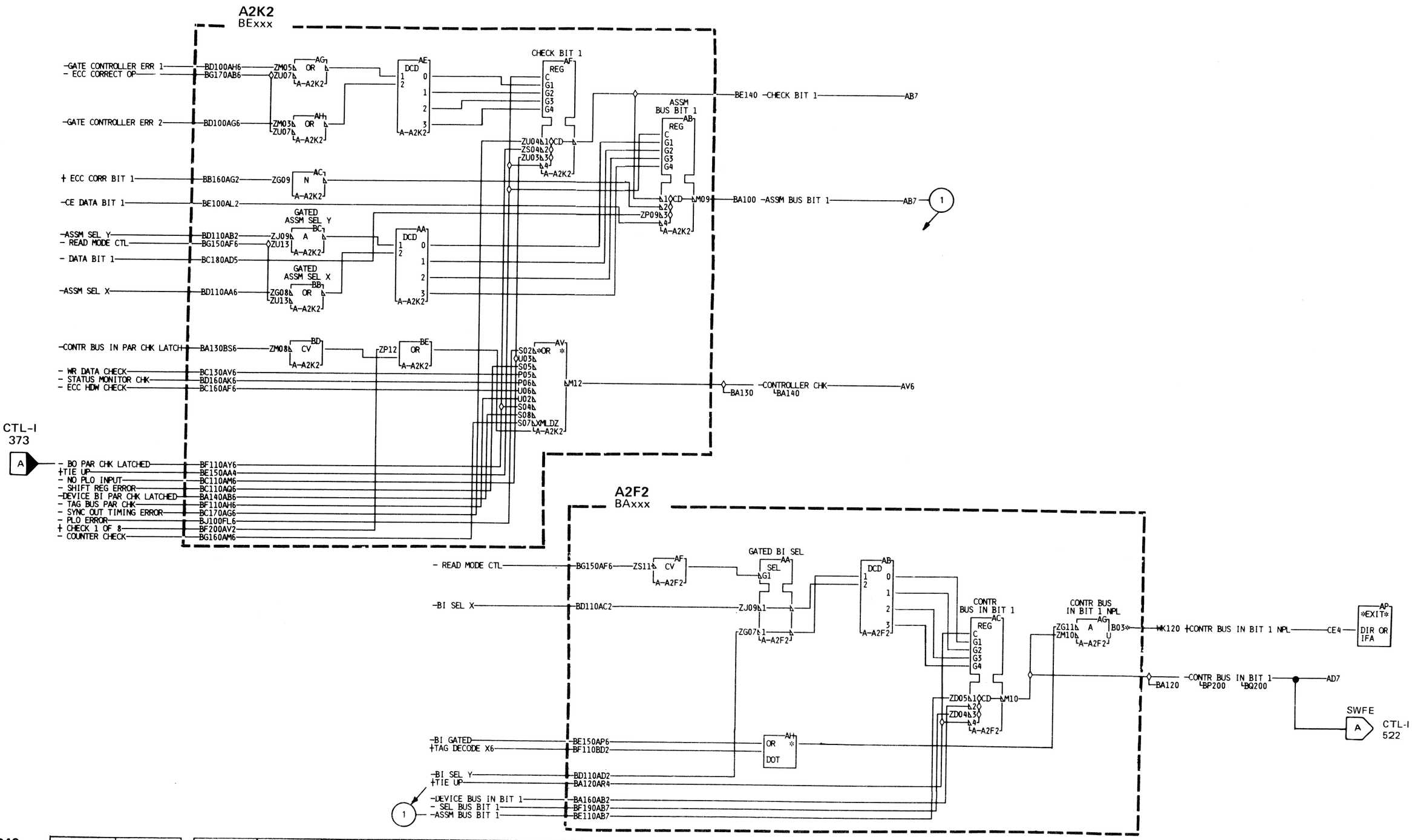


Note: The Bus Out to Tag Bus relationship is not critical.

3340

BQ0371	2747529	See EC History	440224	440227			
Seq. 2 of 2	Part No. (1)		15 Dec 75	14 Sept 76			

BUS OUT PARITY CHECK



BQ0377 Seq. 1 of 2	2747690 Part No. (1)	See EC History	440223 14 Mar 75	440227 14 Sept 76			

Check Circuits

The Tag Bus Parity Check monitors the bits on the Control Tag Bus. While Tag Gate is active an even number of bits perform the following actions:

1. Set Tag Bus Parity Check latch.
2. Block Tag Valid.
3. Inhibit Normal End.
4. Set Tag Bus Parity Check display latch.
5. Activate Error Alert and Controller Check.

During a selection sequence, a Tag Bus Parity Check prevents selection of the Controller by blocking the Valid Tag Gate signal.

Indicator (Control Module CE Panel)

The Tag Bus Parity Check lamp indicates until reset by the Execute Switch or Power On Reset. Microdiagnostic Routine A1 Test 3 tests the Tag Bus Parity Check latch. The Tag Bus Parity Check indicator should be on after running the test and remains on until reset.

Possible Intermittent Failures

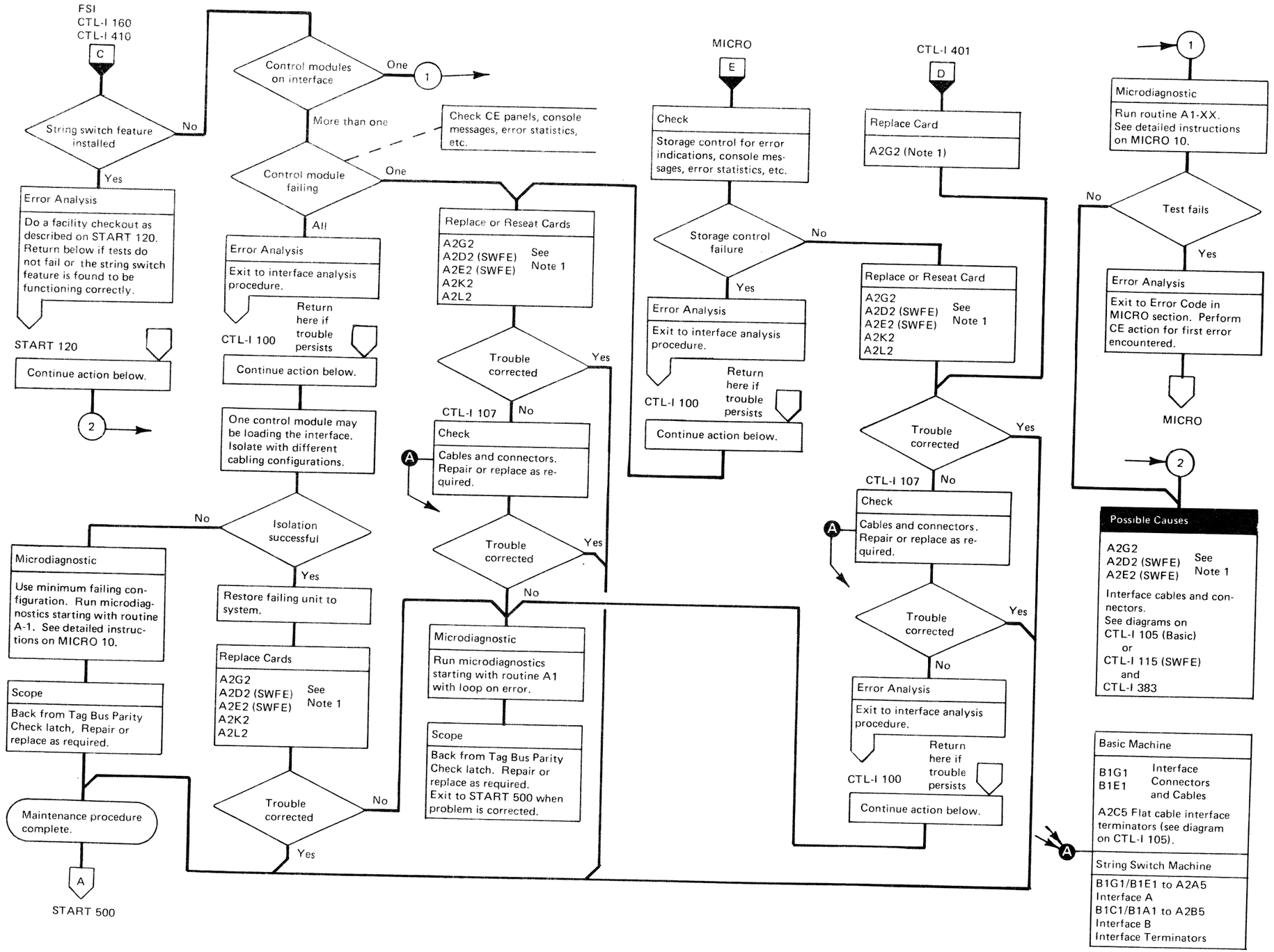
ALL CONTROL MODULES FAIL

1. The storage control unit
2. Cable or connector from storage control to the first control module.
3. A line held inoperable by a cable or connector short or ground anywhere on the interface.

SINGLE UNIT FAILS

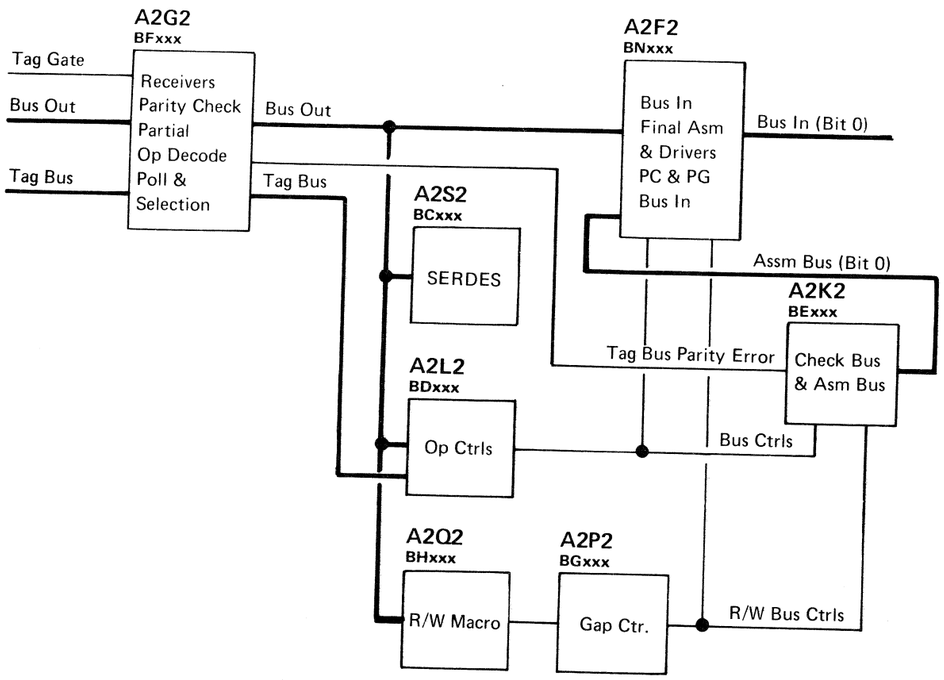
1. Card, voltage, back panel wiring, etc. in the failing unit.
2. Cable or connector fault at the input to failing unit.

Note 1: When replacing A2G2, A2D2, or A2E2 check addressing jumpers. See INST 8.

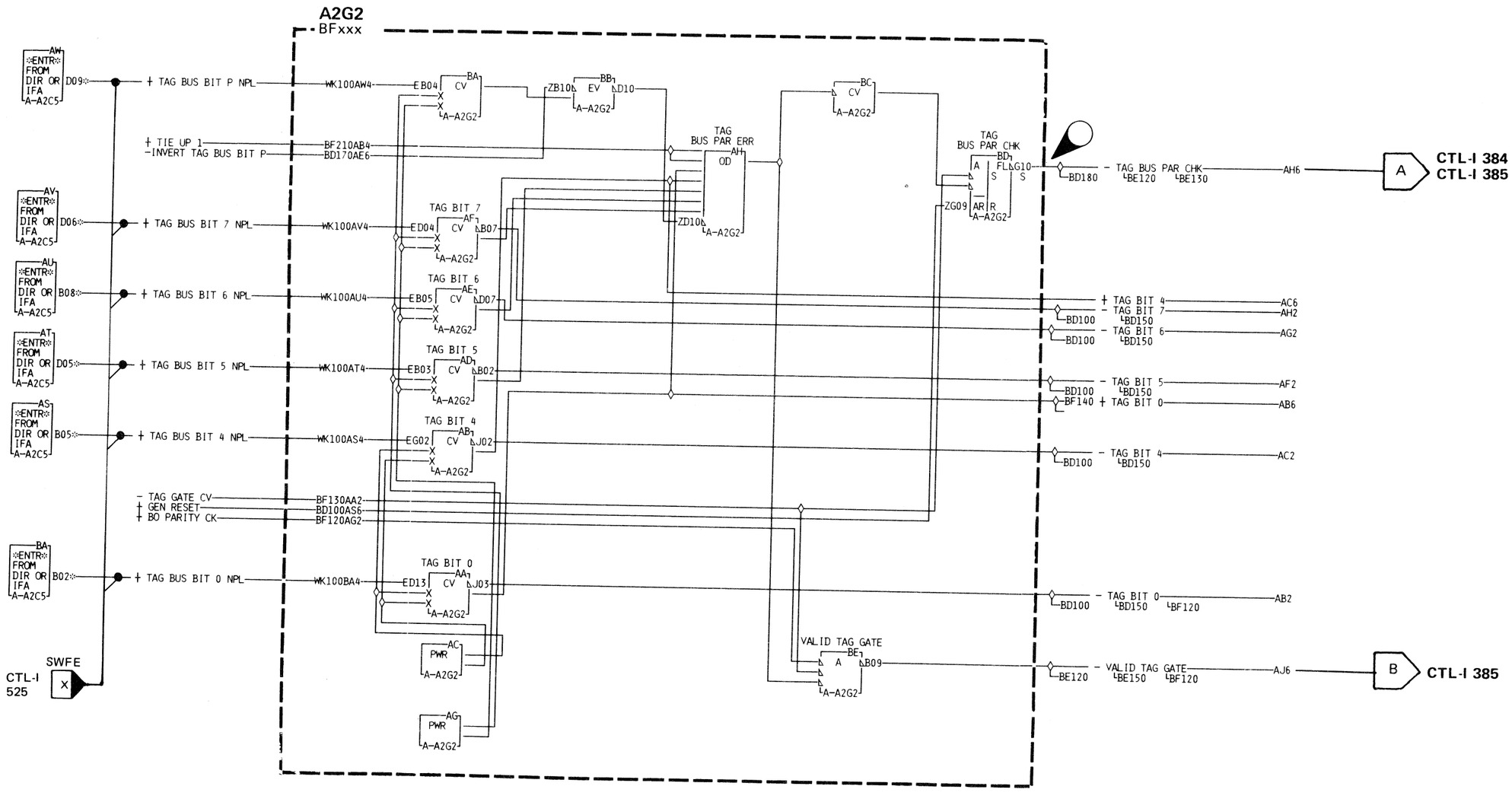


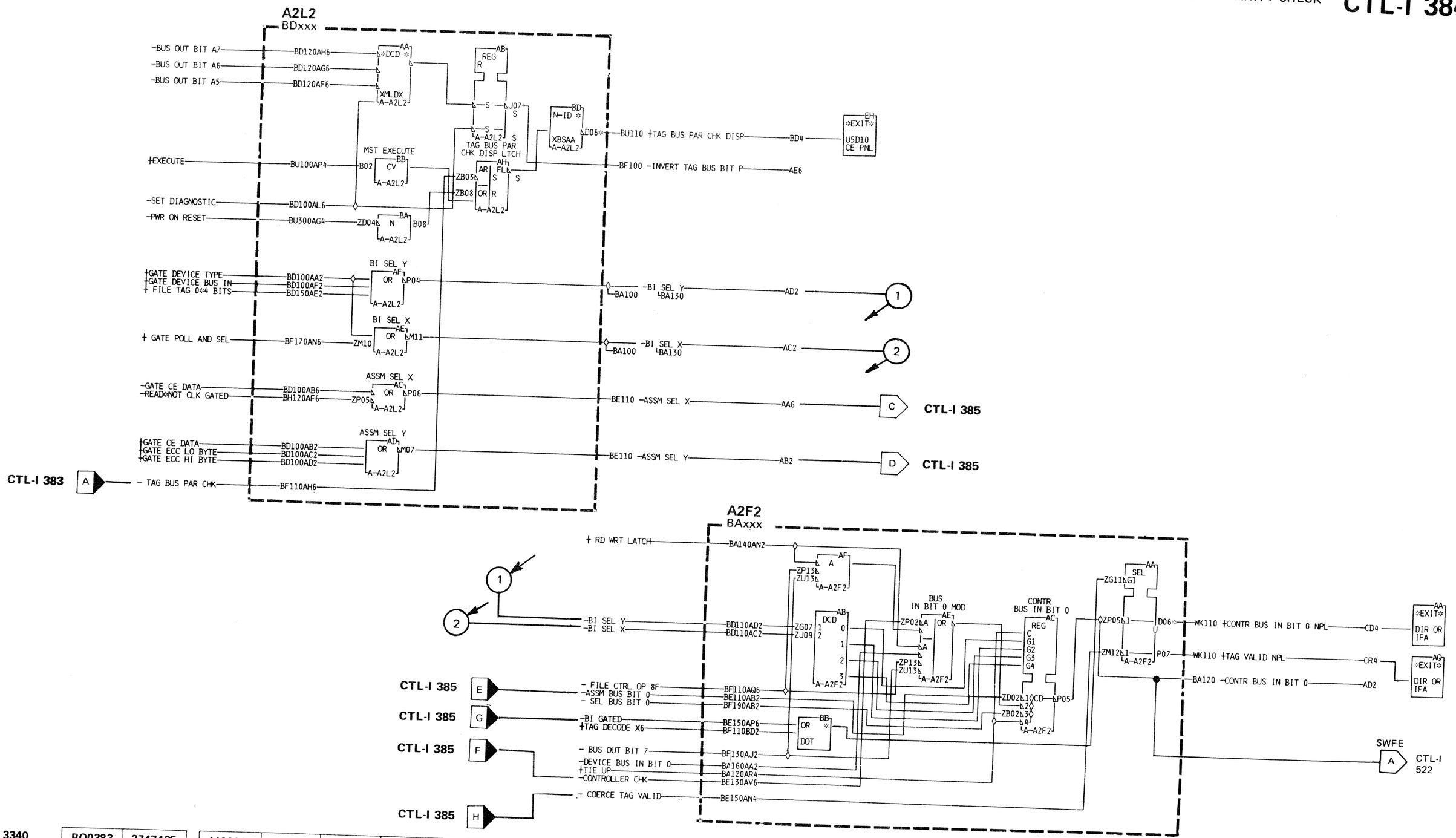
BQ0377	2747690	See EC History	440223	440227				
Seq. 2 of 2	Part No. (1)		14 Mar 75	14 Sept 76				

CONTROL TAG BUS PARITY CHECK



TAG BUS PARITY CHECK

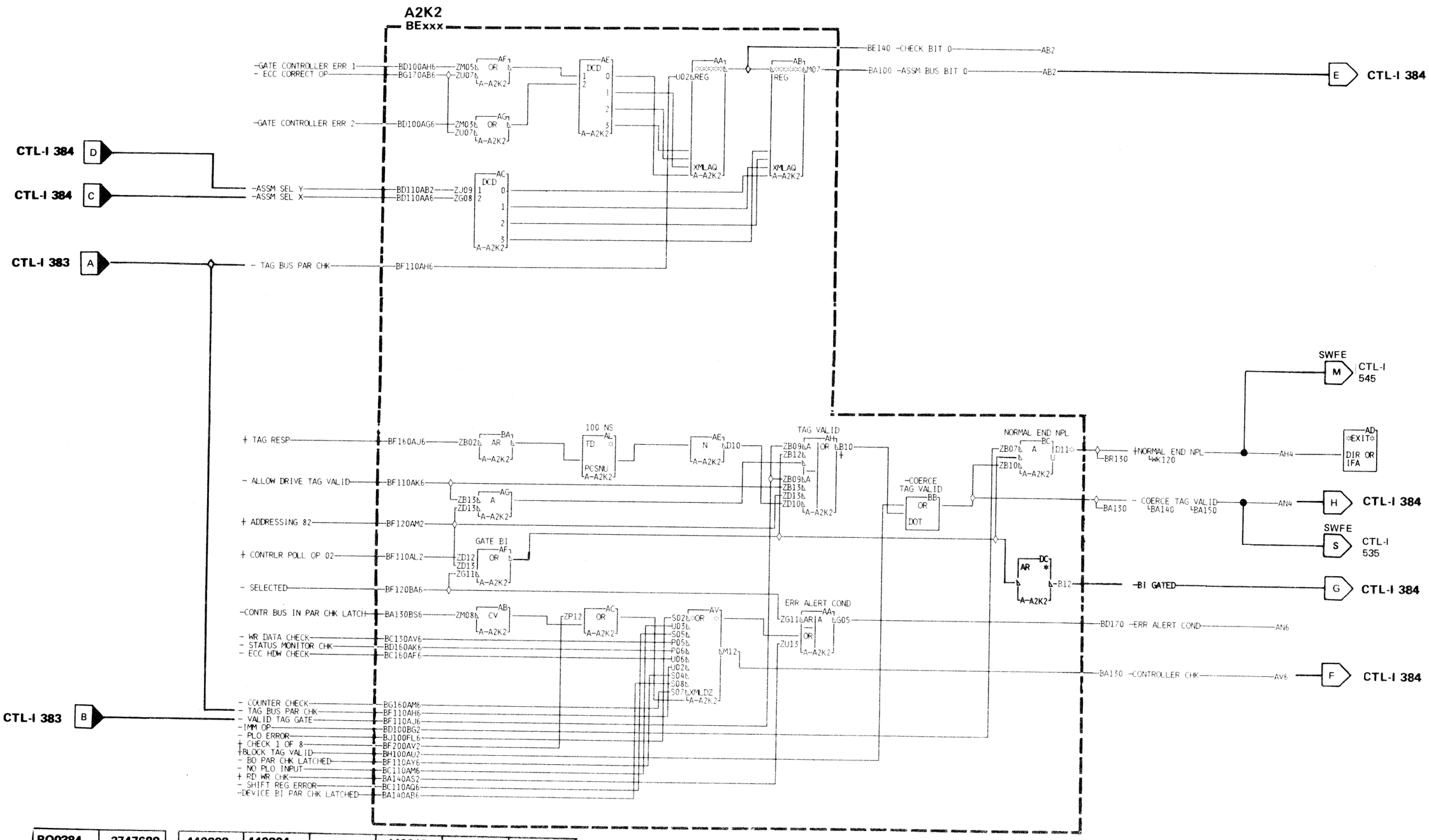




3340

BQ0383	2747435	440200	440203	440204	440213	440227		
Seq. 2 of 2	Part No. (1)	25 Jun 73	2 Nov 73	21 Dec 73	13 May 74	14 Sept 76		

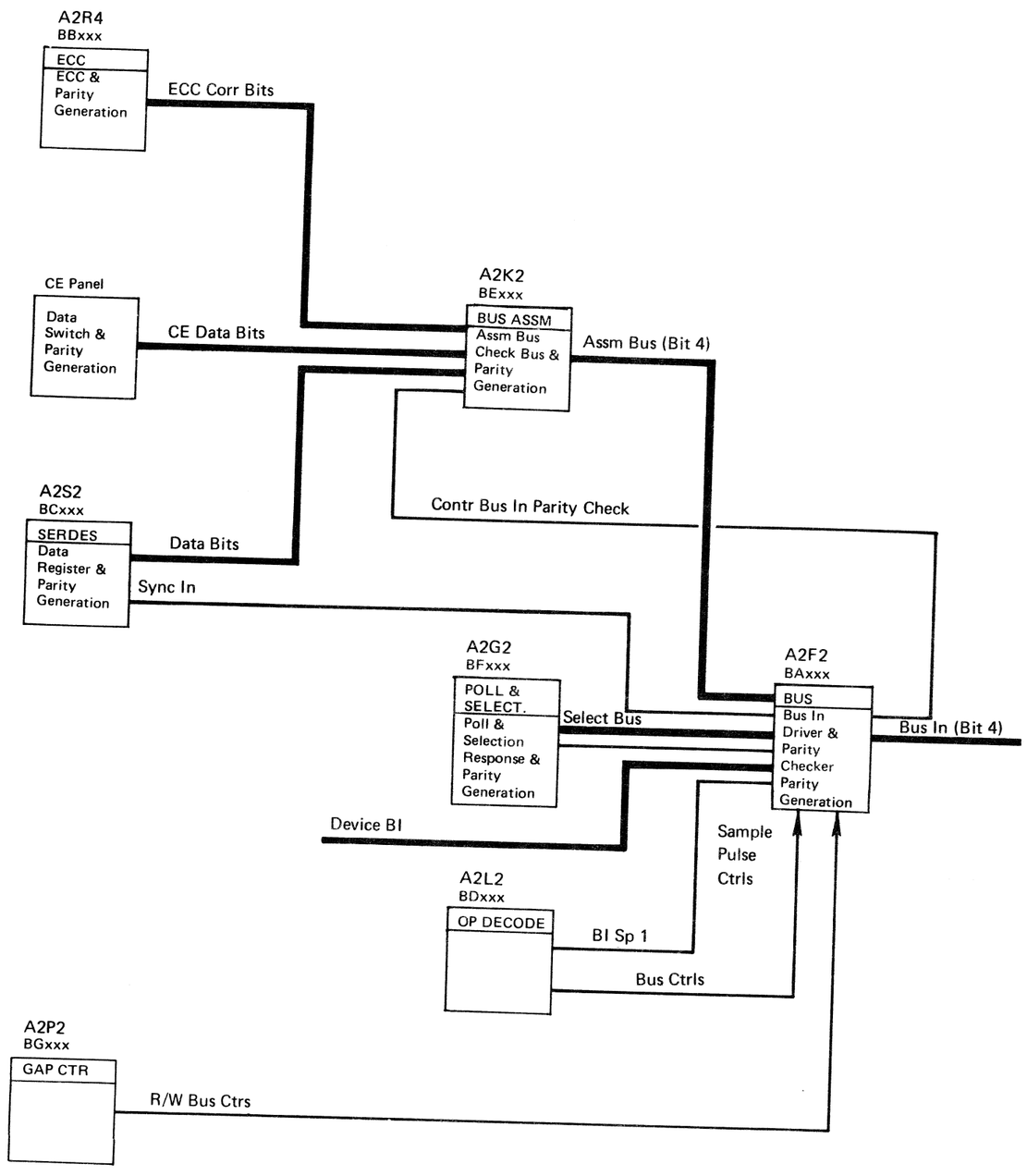
TAG BUS PARITY CHECK



3340

BQ0384 Seq. 1 of 2	2747689 Part No.( )	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440213 13 May 74		

CONTROLLER BUS IN PARITY CHECK



3340

BQ0384	2747689	440203	440204	440209	440213			
Seq. 2 of 2	Part No. ( )	2 Nov 73	21 Nov 73	25 Mar 74	13 May 74			

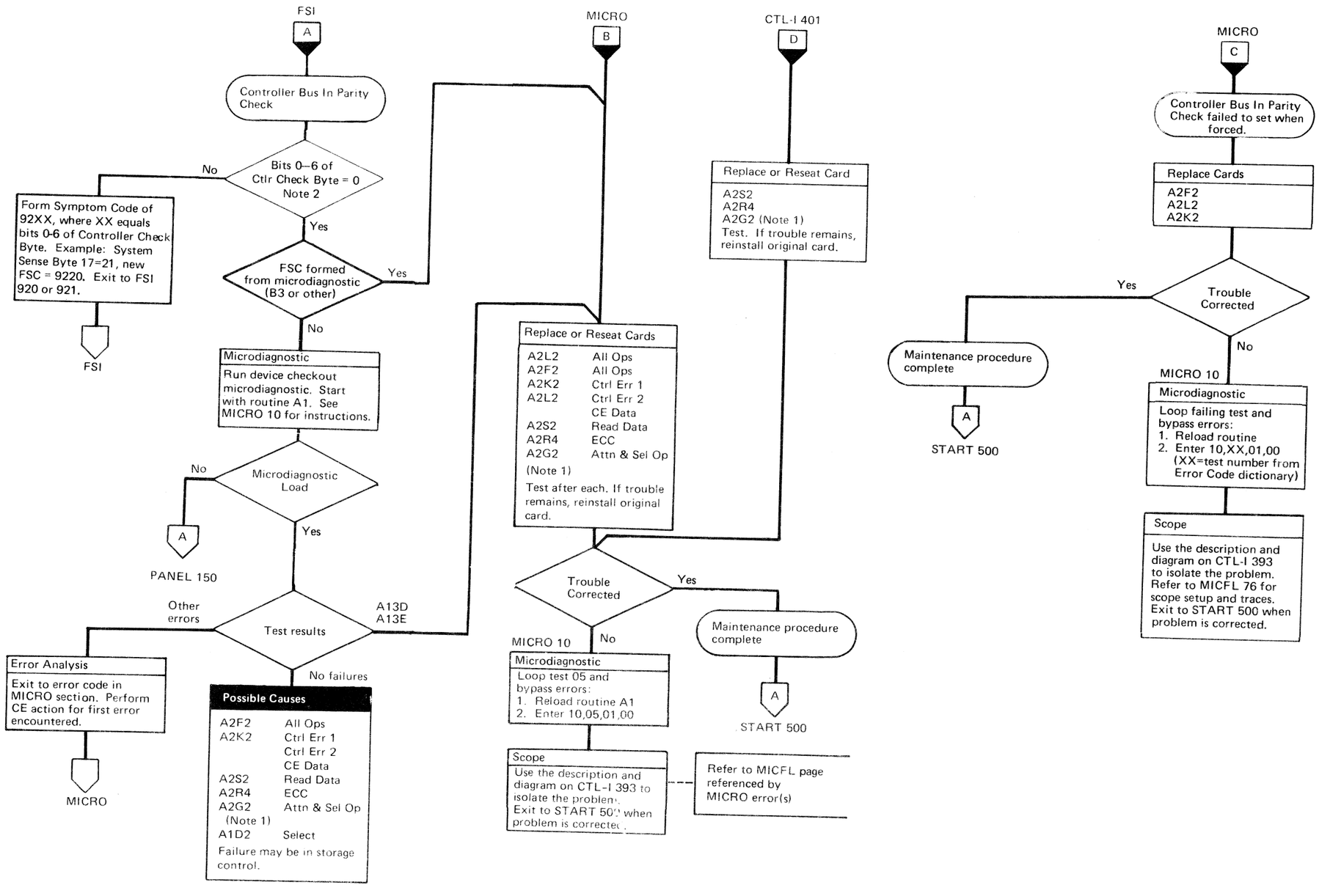
CONTROLLER BUS IN PARITY CHECK

For operations where the data or the control interface Bus In must contain good parity, the inputs to the Bus In drives are checked for proper parity. The parity bit on Bus In is generated to prevent error propagation.

An analysis of the sense bytes (Bytes 13 & 15) or the Error Code Dictionary descriptions indicate the type of operation in progress when the error occurred.

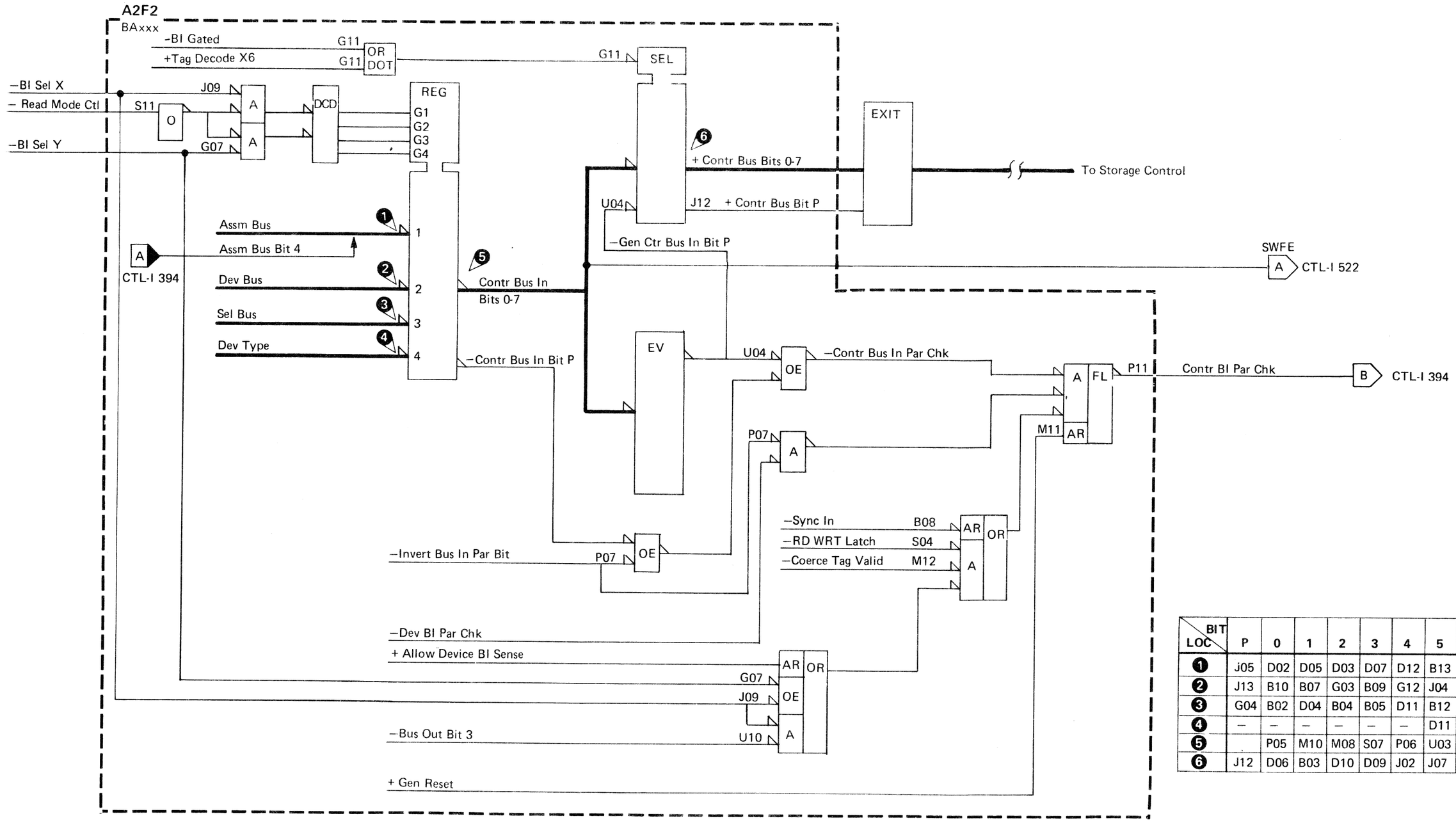
Card A2F2 must be the primary suspect since it contains the Parity Checker as well as the final assembler, which is the input to the Checker. It also contains the device Bus In receivers. The order of subsequent replacement depends upon the failing operation(s).

See CTL-I 107 for cable checking hints.



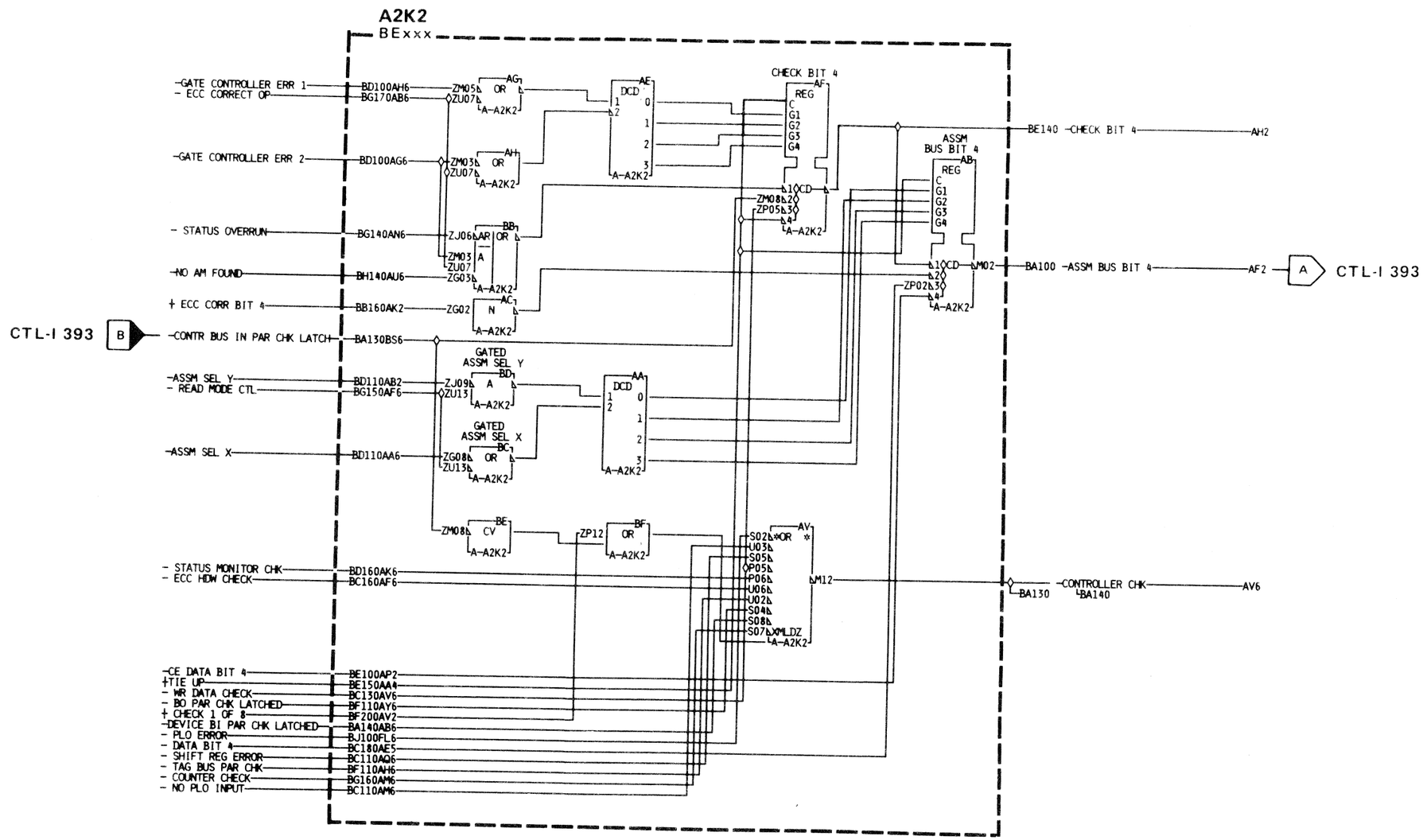
Note 1: When replacing A2G2, check addressing jumpers. See INST 8.

Note 2: Controller Check Byte equals:
System Sense Byte 17 (SENSE 101)
Routine B3 Message Display
Byte 10 (FSI 65)



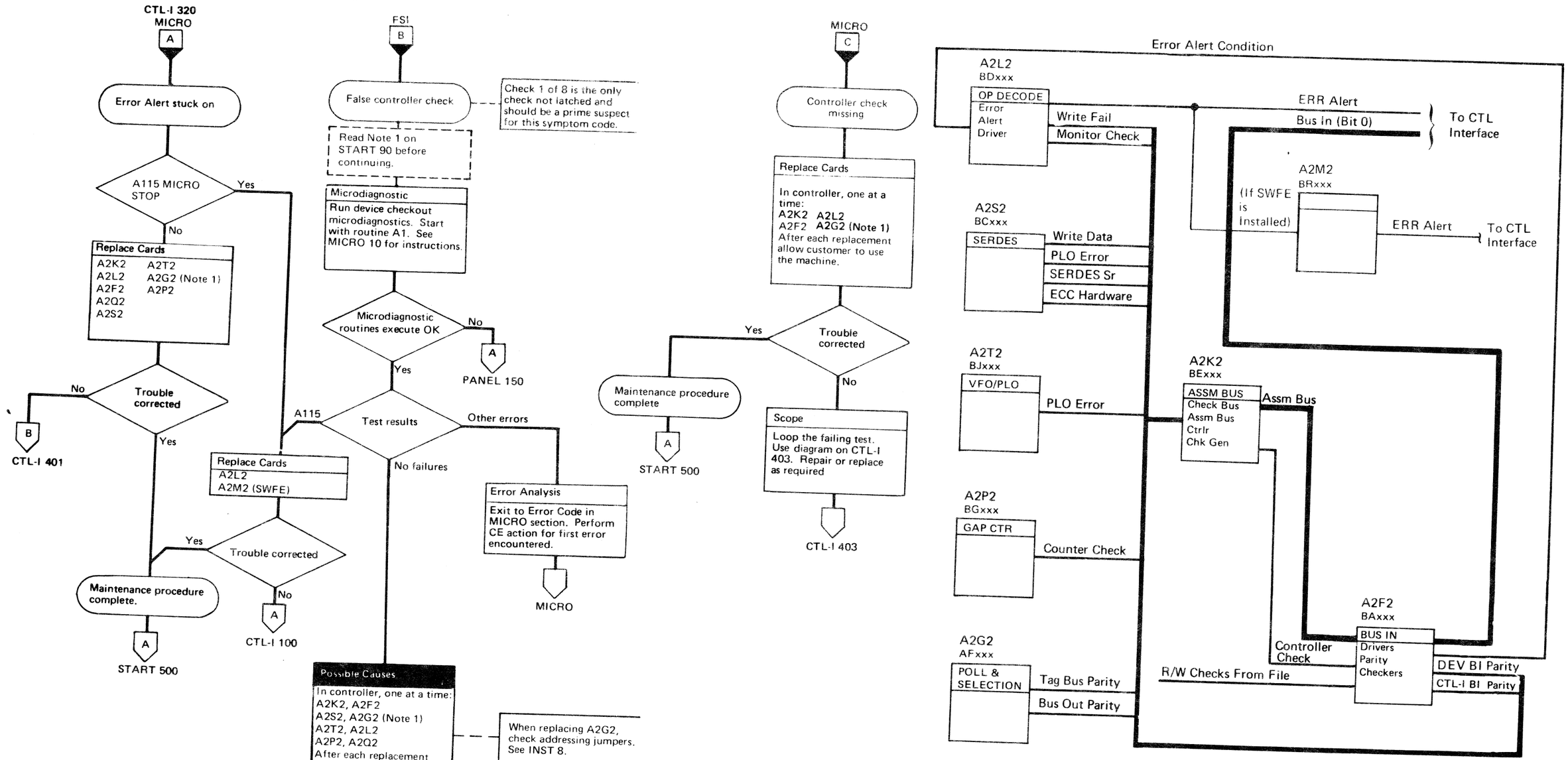
LOC \ BIT	P	0	1	2	3	4	5	6	7
1	J05	D02	D05	D03	D07	D12	B13	G02	G10
2	J13	B10	B07	G03	B09	G12	J04	G05	G07
3	G04	B02	D04	B04	B05	D11	B12	J06	G08
4	–	–	–	–	–	–	D11	–	–
5		P05	M10	M08	S07	P06	U03	P09	U06
6	J12	D06	B03	D10	D09	J02	J07	J11	J03

CONTROLLER BUS IN PARITY CHECK



BQ0393	2747437	See EC History	440224	440227				
Seq 1 of 2	Part No. (1)		15 Dec 75	14 Sept 76				

See OPER 260 for Controller Errors that cause Error Alert.



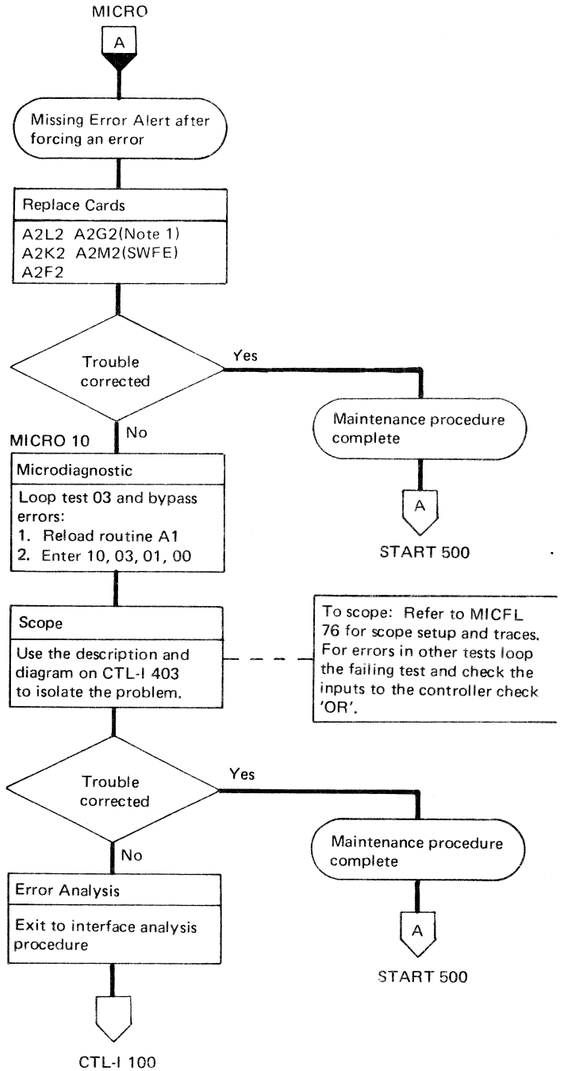
Note 1: When replacing A2G2, check addressing jumpers. See INST 8.

BQ0393	2747437
Seq. 2 of 2	Part No. (1)

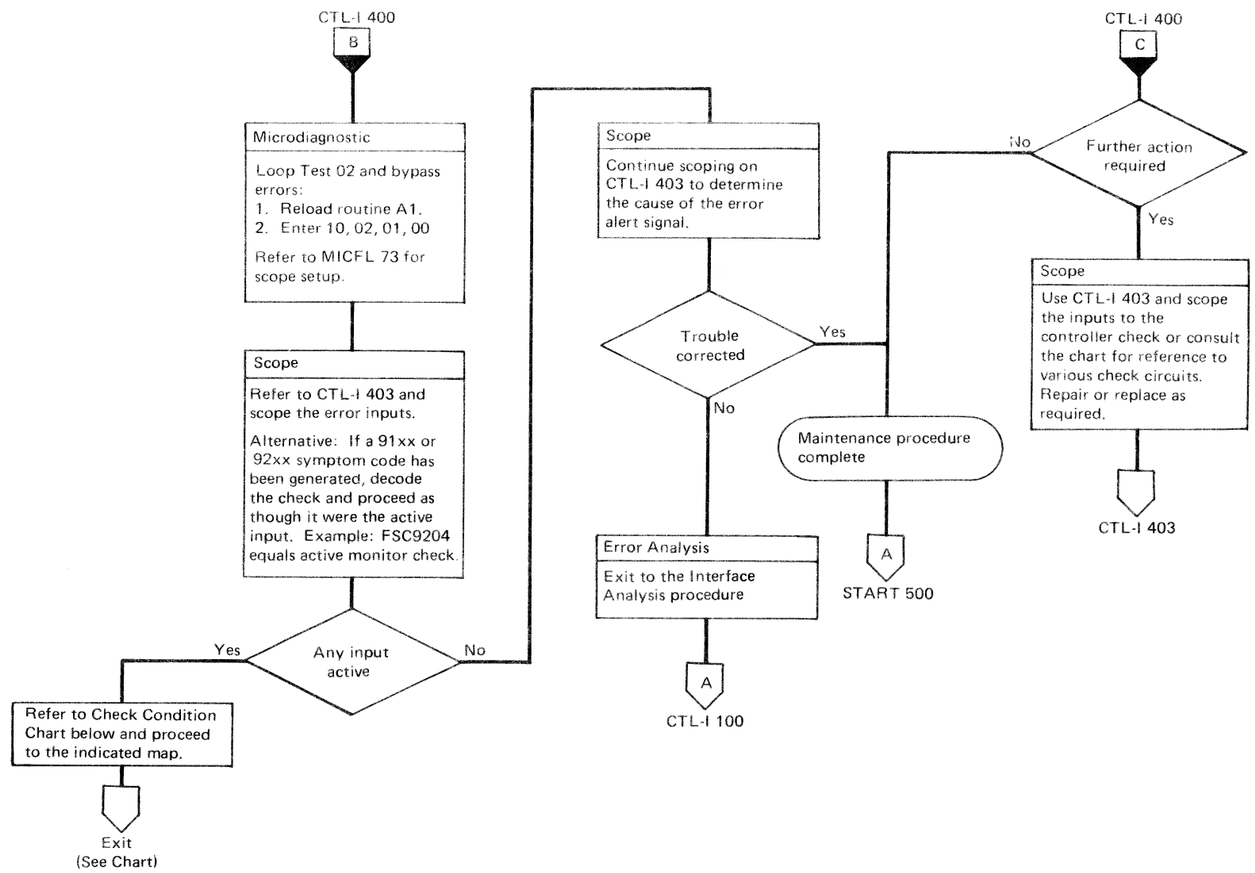
See EC History	440224 15 Dec 75	440227 14 Sep 76				

CONTROLLER CHECK – MISSING ERROR ALERT

See OPER 260 for Controller Errors that cause Error Alert.



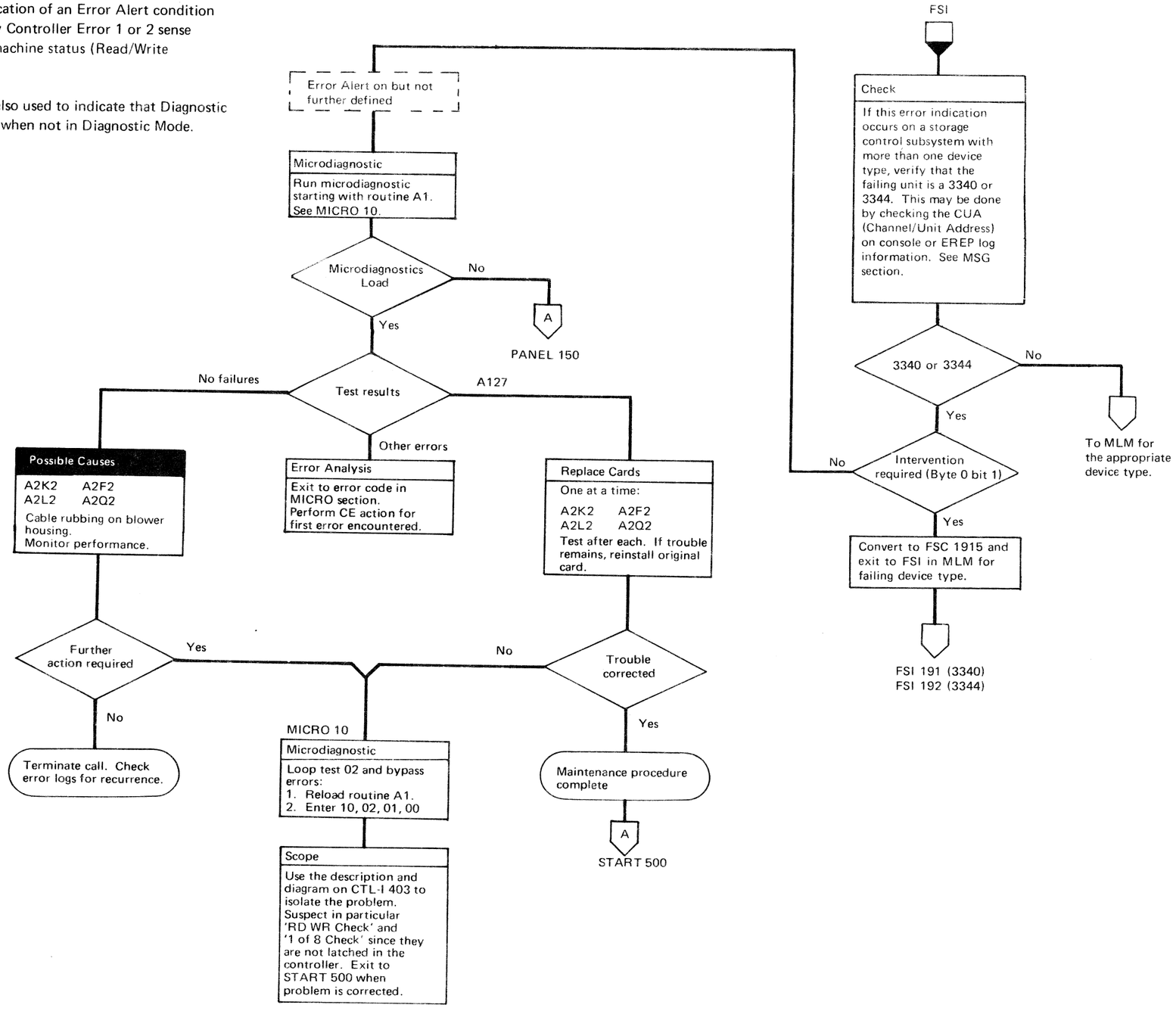
Note 1: *When replacing A2G2, check addressing jumpers. See INST 8.*



FSC	Check Condition	MAP	Scope Point
9108	Ctl. Bus In Parity check	CTL-I 390 Entry D	A2F2P11
9110	Device Bus In Parity check	DEV-I 180 Entry A	A2F2M05
9120	Check 1 of 8	3340: DEV-I 110 Entry A 3344: DEV-I 112 Entry A	
9140	Bus Out Parity check	CTL-I 370 Entry D	A2G2J10
9180	Tag Bus Parity check	CTL-I 380 Entry D	A2G2G10
9202	ECC hardware check	DATA 200 Entry C	A2S2S04
9204	Monitor check	DATA 220 Entry A	A2L2D09
9208	Write Data check	DATA 230 Entry B	A2S2G11
9210	Counter check	DATA 240 Entry A	A2P2M05
9220	SERDES SR check	DATA 250 Entry B	A2S2G08
9240	No PLO input	DATA 261 Entry B	A2S2J09
9280	PLO error	DATA 270 Entry B	A2T2G03

A false Error Alert is an indication of an Error Alert condition that is not further defined by Controller Error 1 or 2 sense information, or by bit 3 of machine status (Read/Write Check) from the device.

An undefined Error Alert is also used to indicate that Diagnostic Suppress Write Gate is active when not in Diagnostic Mode.

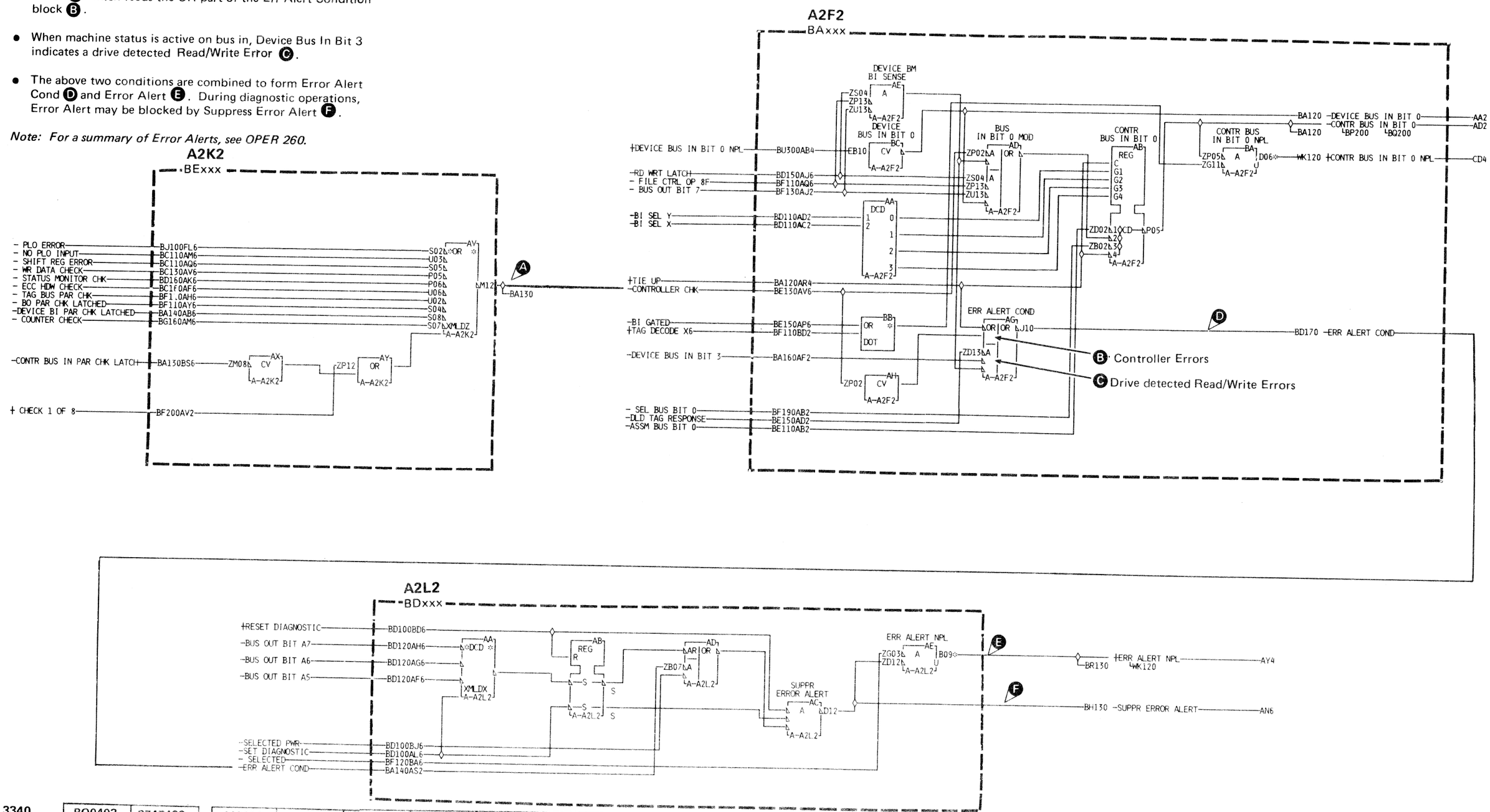


CONTROLLER CHECK

ERROR ALERT

- Controller detected errors are combined to form Controller Check Ⓐ which feeds the OR part of the Err Alert Condition block Ⓑ.
- When machine status is active on bus in, Device Bus In Bit 3 indicates a drive detected Read/Write Error Ⓒ.
- The above two conditions are combined to form Error Alert Cond Ⓓ and Error Alert Ⓔ. During diagnostic operations, Error Alert may be blocked by Suppress Error Alert Ⓕ.

Note: For a summary of Error Alerts, see OPER 260.



BQ0403 Seq 1 of 2	2747439 Part No. (1)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440227 14 Sept 76

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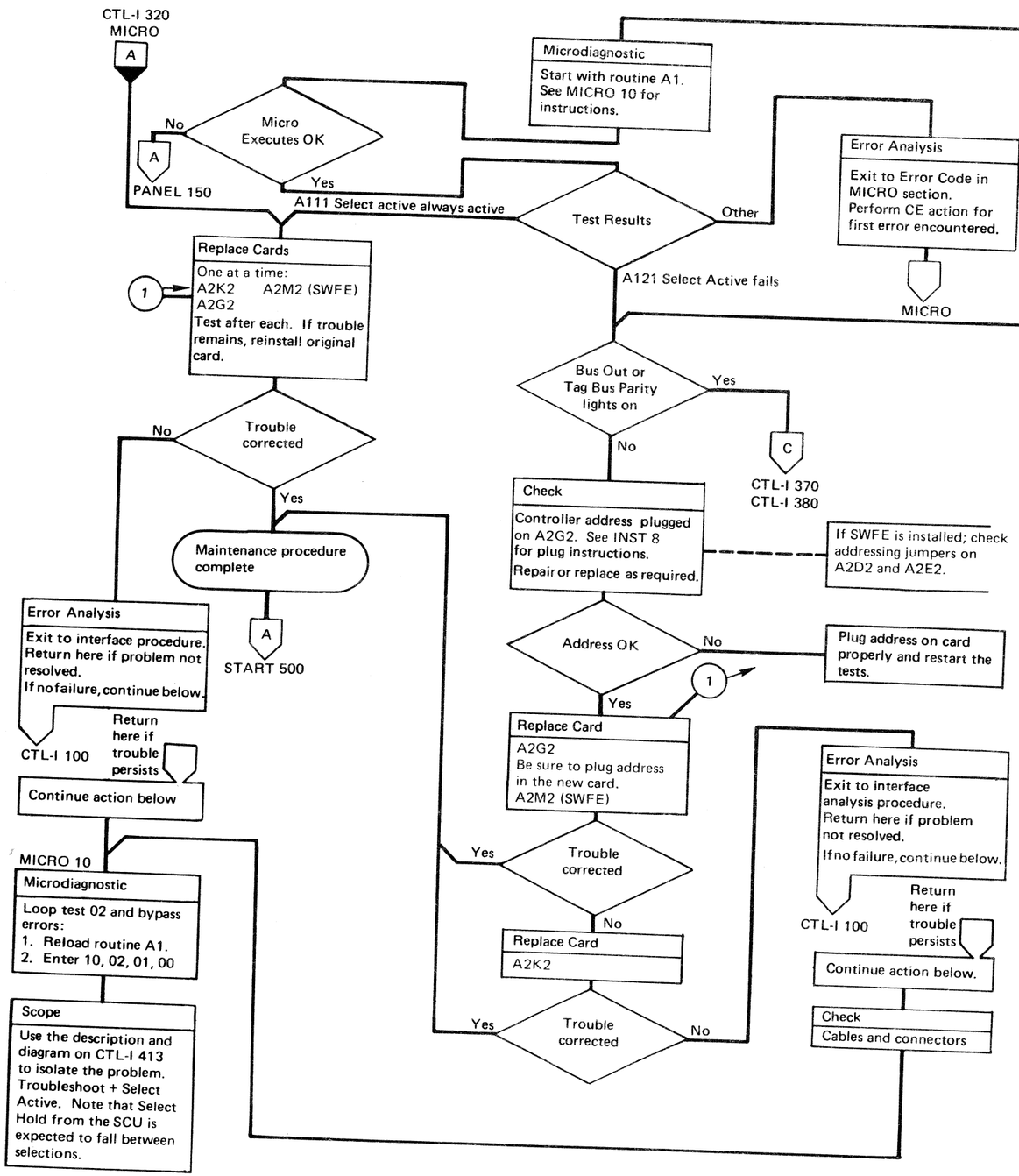
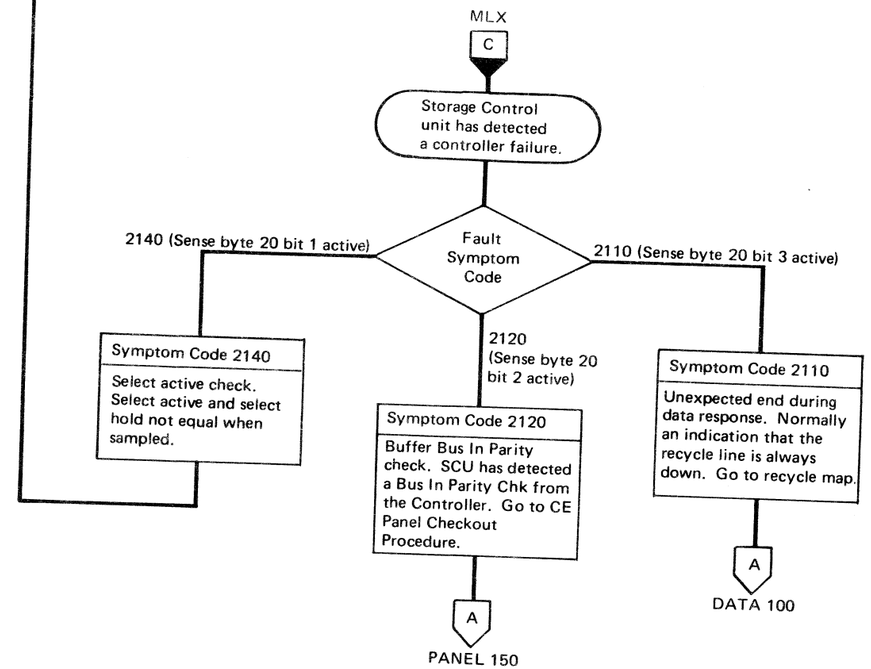
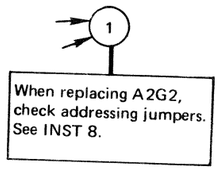
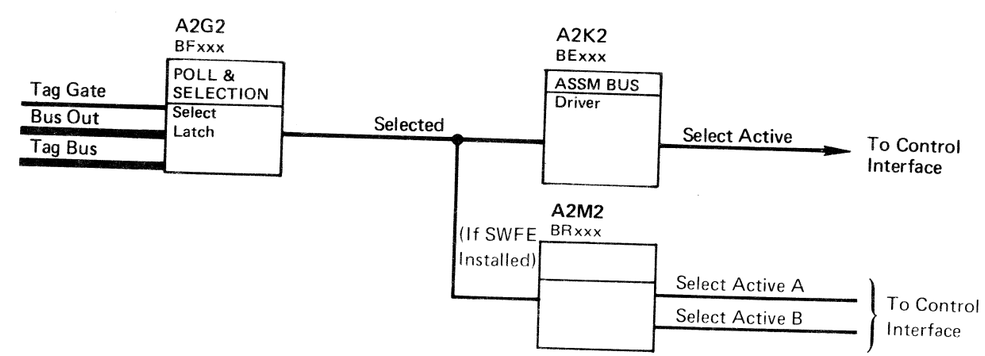
SELECT ACTIVE

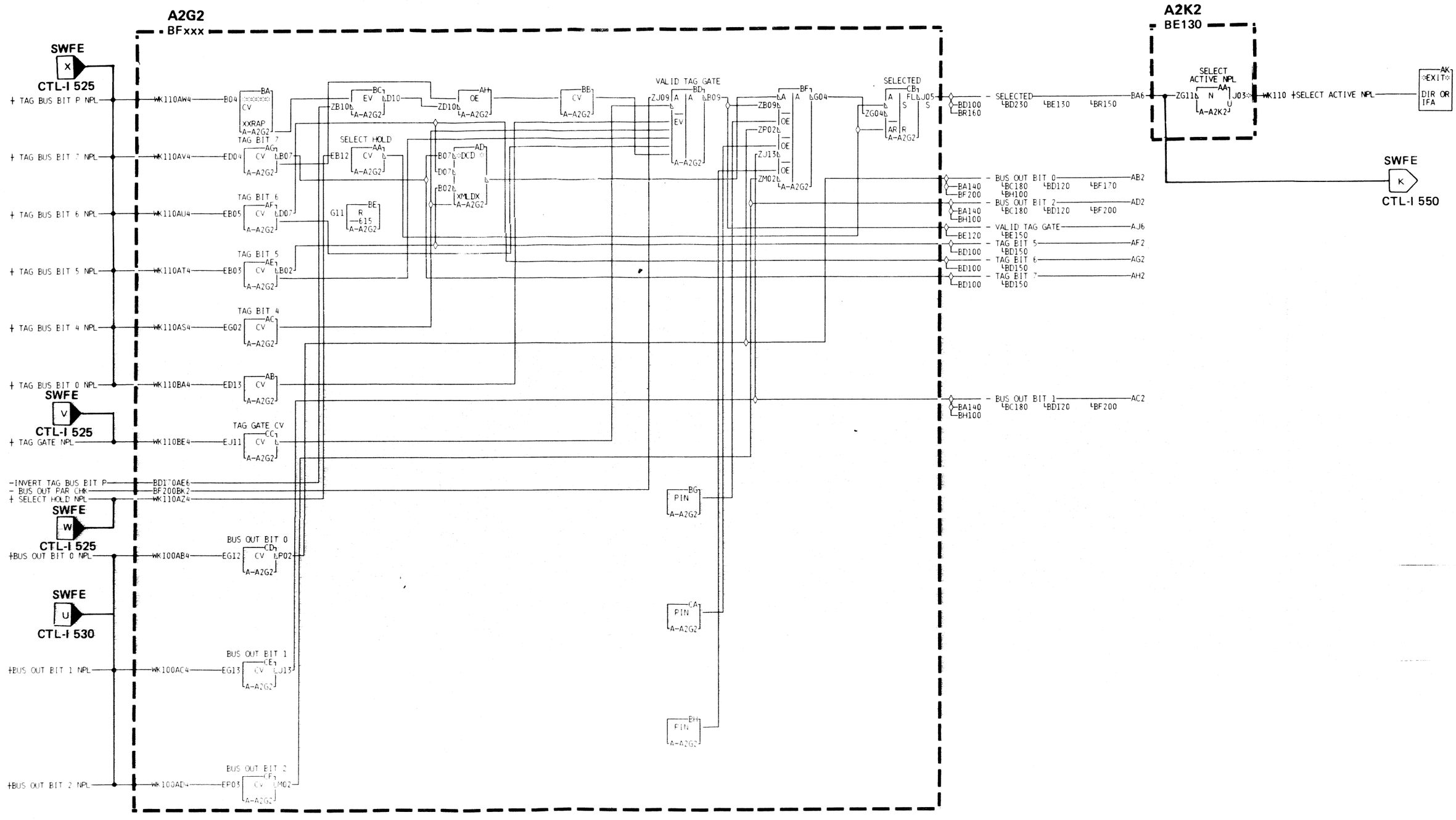








BQ0403 Seq 2 of 2	2747439 Part No. (1)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440227 14 Sept 76

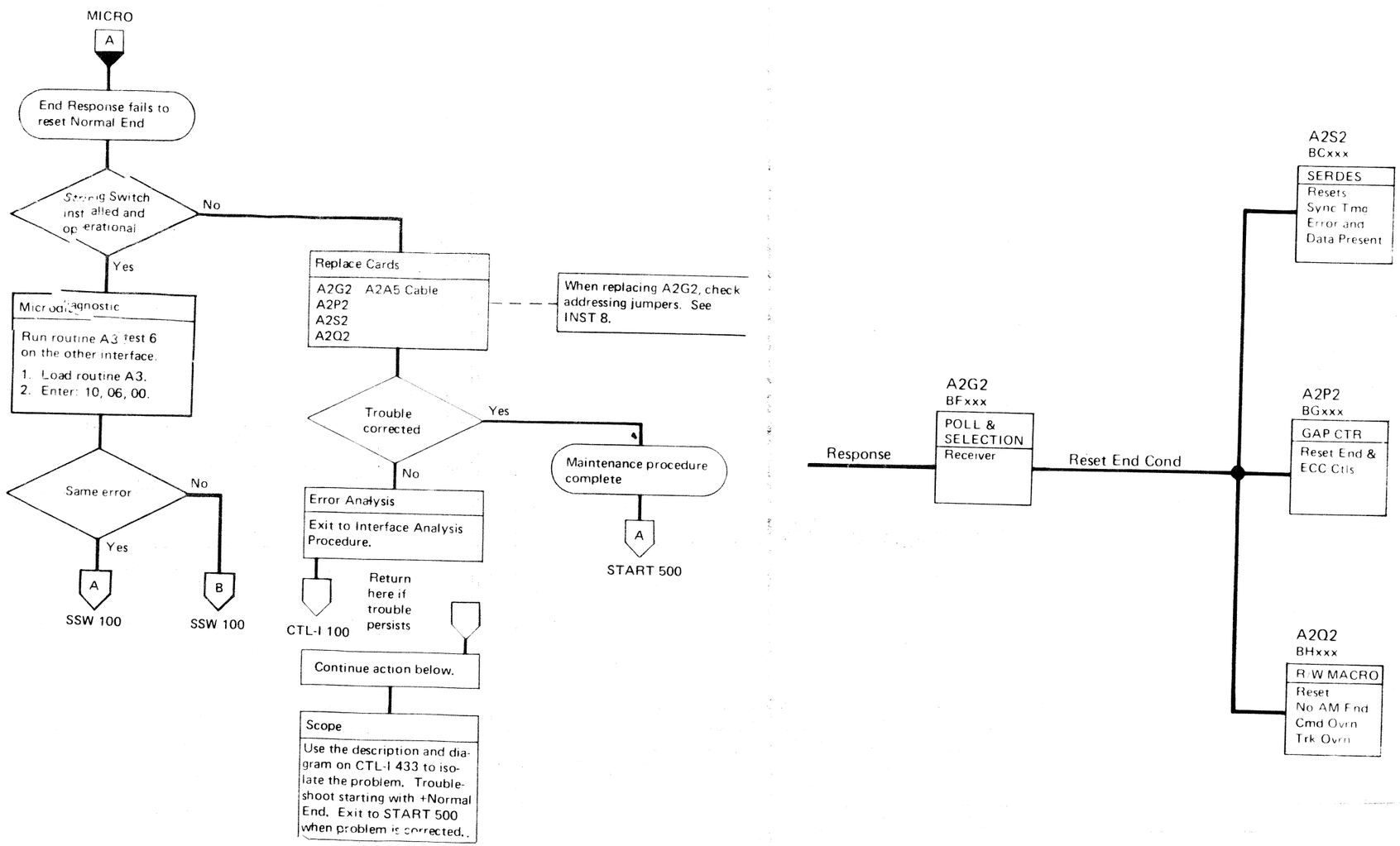


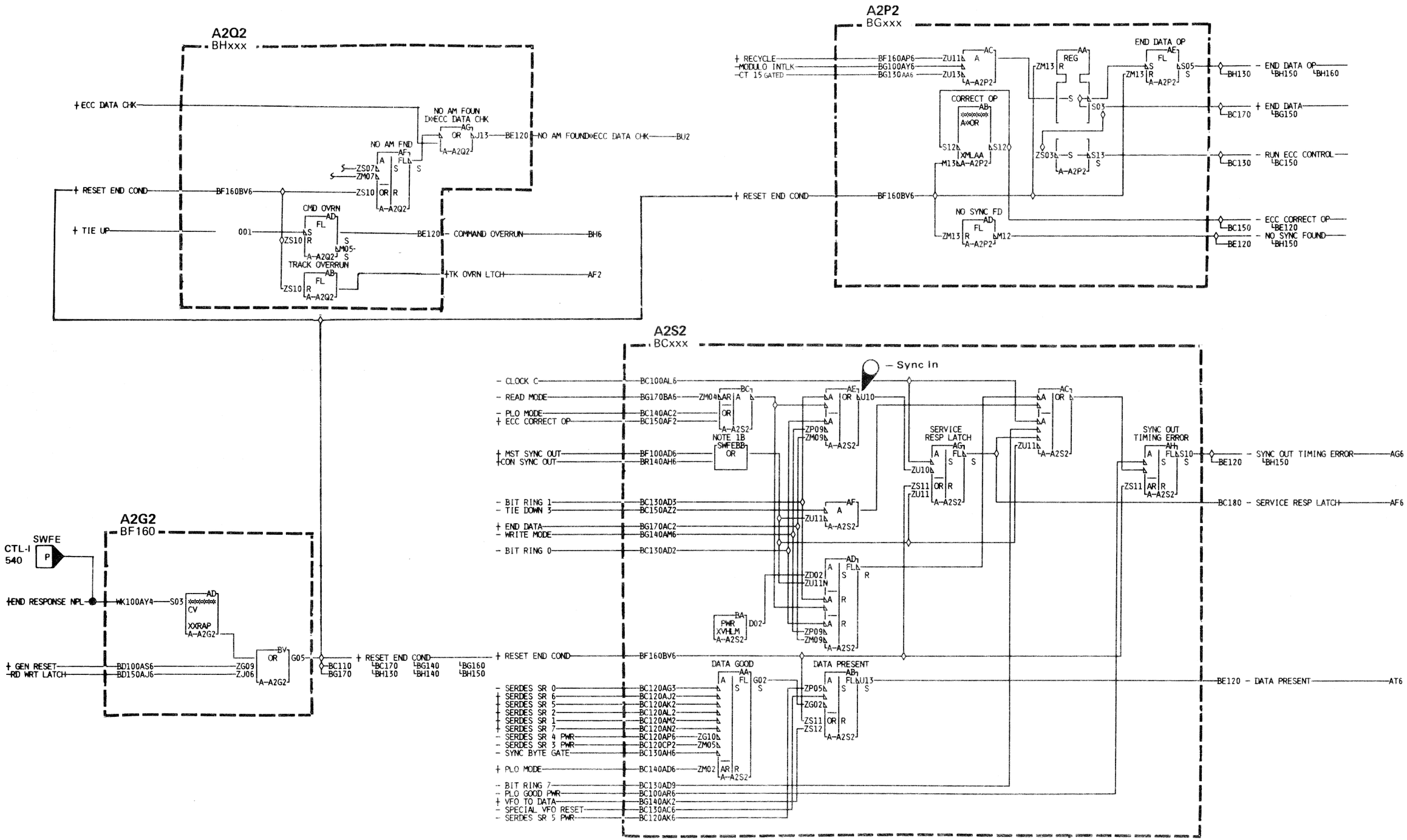
BQ0413	2747540	440200	440203	440209	440213	440224		
Seq. 1 of 2	Part No. ( )	25 Jun 73	2 Nov 73	25 Mar 74	13 May 74	15 Dec 75		

END RESPONSE FAILURE

The End Response signal from storage control signifies to the controller that there is no further need for any of the several conditions or check latches and that these should be reset.

Failure to receive End Response is recognized if one or more of these latches fail to reset when End Response is issued.

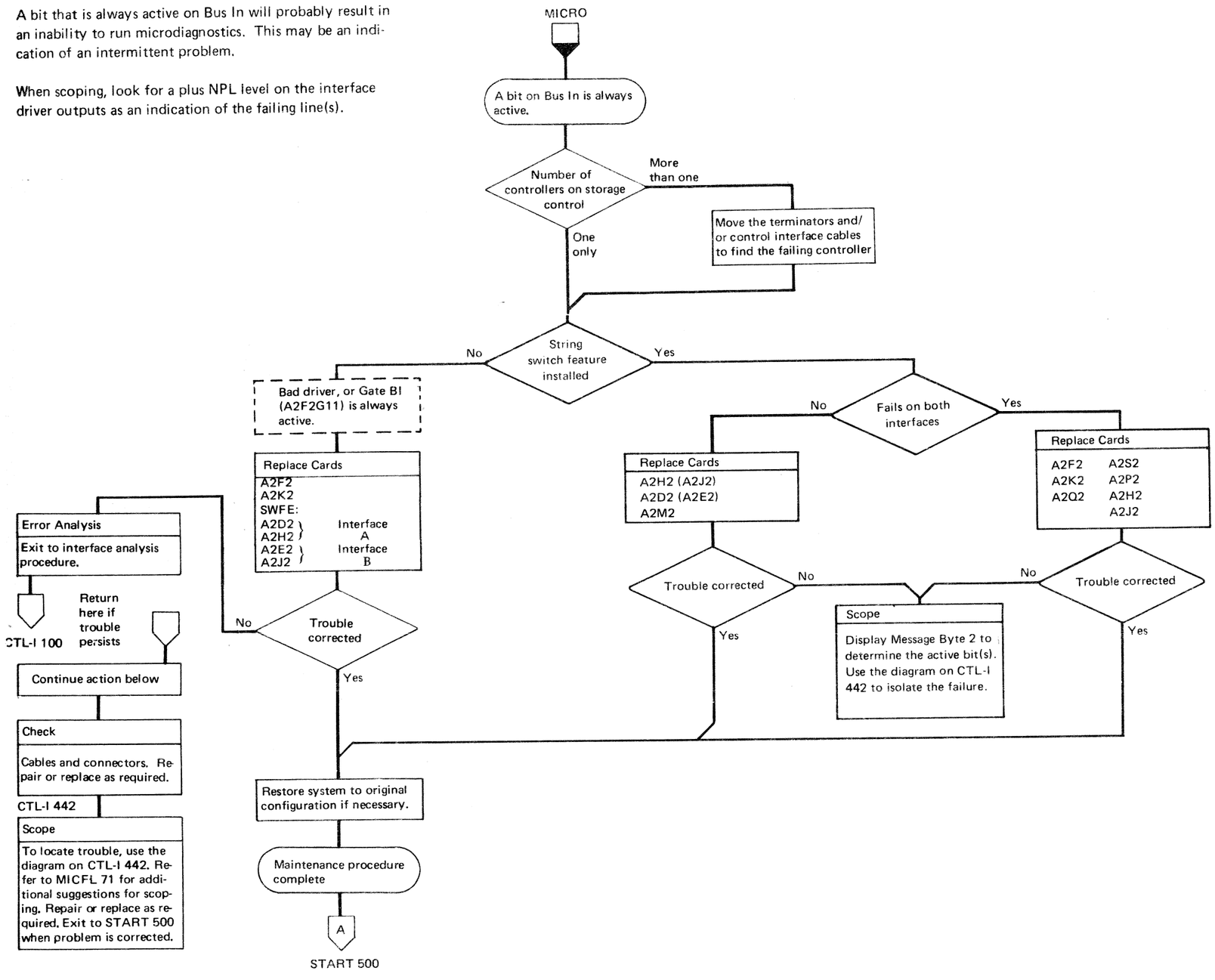




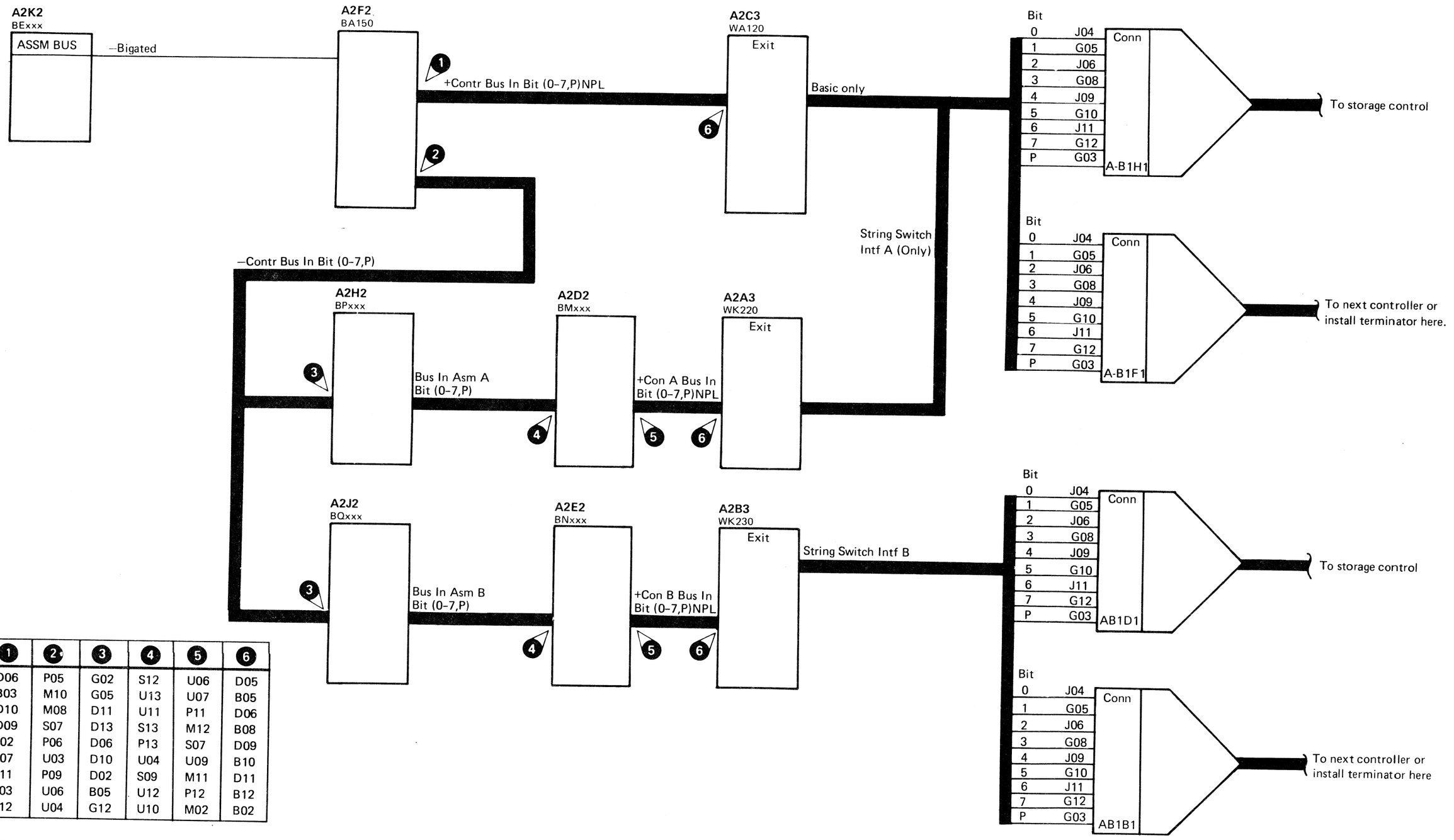
ACTIVE BUS IN BIT

A bit that is always active on Bus In will probably result in an inability to run microdiagnostics. This may be an indication of an intermittent problem.

When scoping, look for a plus NPL level on the interface driver outputs as an indication of the failing line(s).



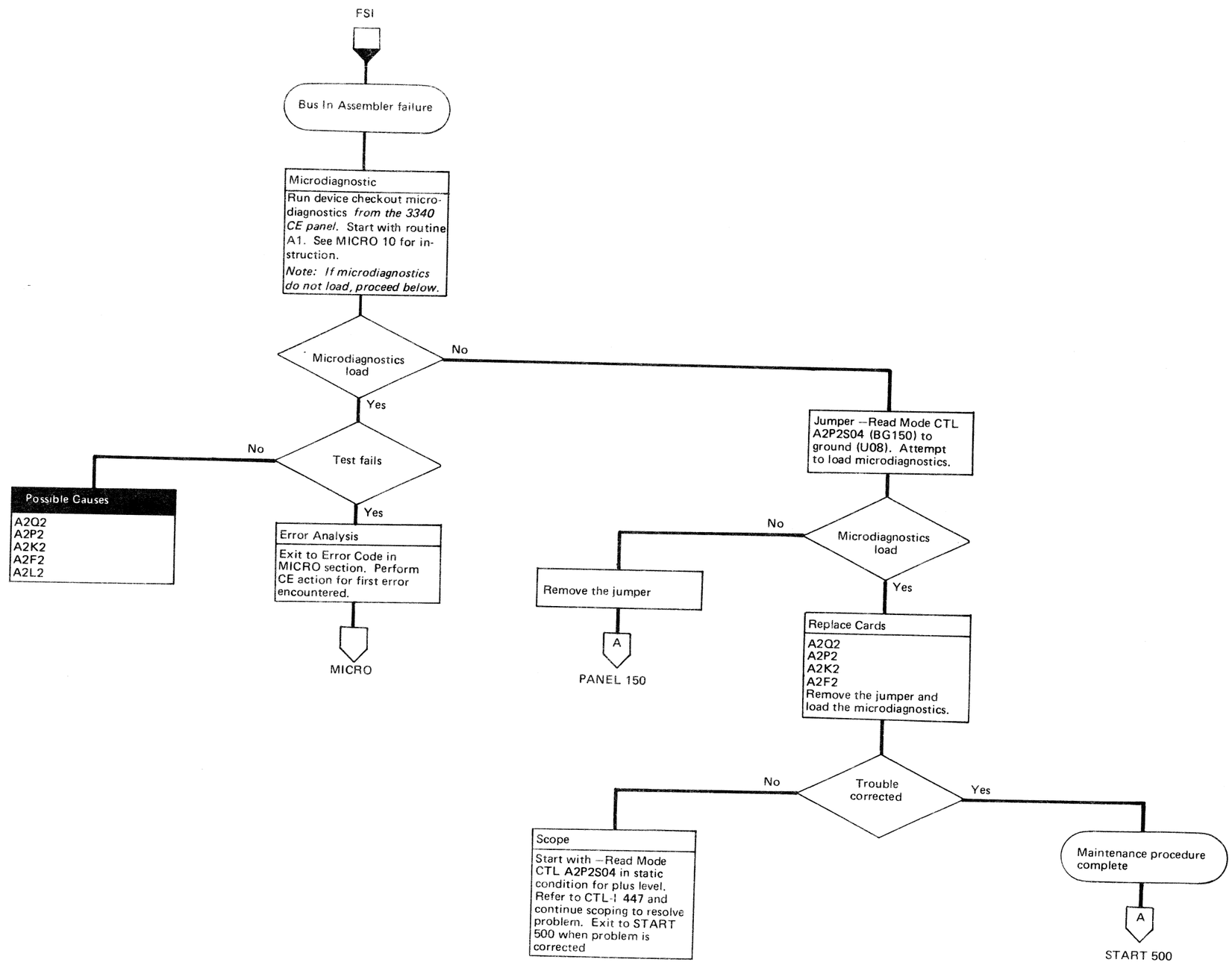
BQ0430 Seq. 2 of 2	2747541 Part No. (1)	See EC History	440219 26 Sept 74	440227 14 Sept 76		



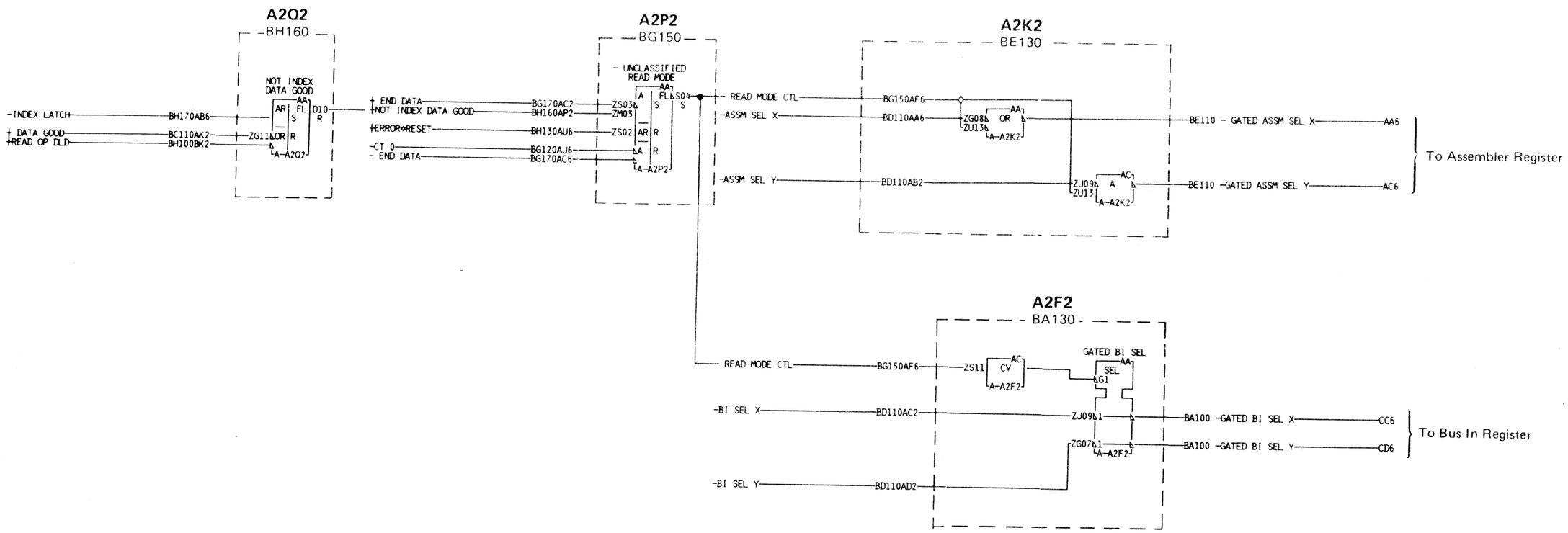
	1	2	3	4	5	6
Bit 0	D06	P05	G02	S12	U06	D05
Bit 1	B03	M10	G05	U13	U07	B05
Bit 2	D10	M08	D11	U11	P11	D06
Bit 3	D09	S07	D13	S13	M12	B08
Bit 4	J02	P06	D06	P13	S07	D09
Bit 5	J07	U03	D10	U04	U09	B10
Bit 6	J11	P09	D02	S09	M11	D11
Bit 7	J03	U06	B05	U12	P12	B12
Bit P	J12	U04	G12	U10	M02	B02

BUS IN ASSEMBLER FAILURE

To ensure data integrity on Read operations, redundant controls are on the registers that assemble the Bus In bits. A malfunction in this area could cause the SERDES Data Register to be gated to Bus In during non-Read operations. This condition is recognized by observing that Sense Bytes 8 through 12 are 'FF'.

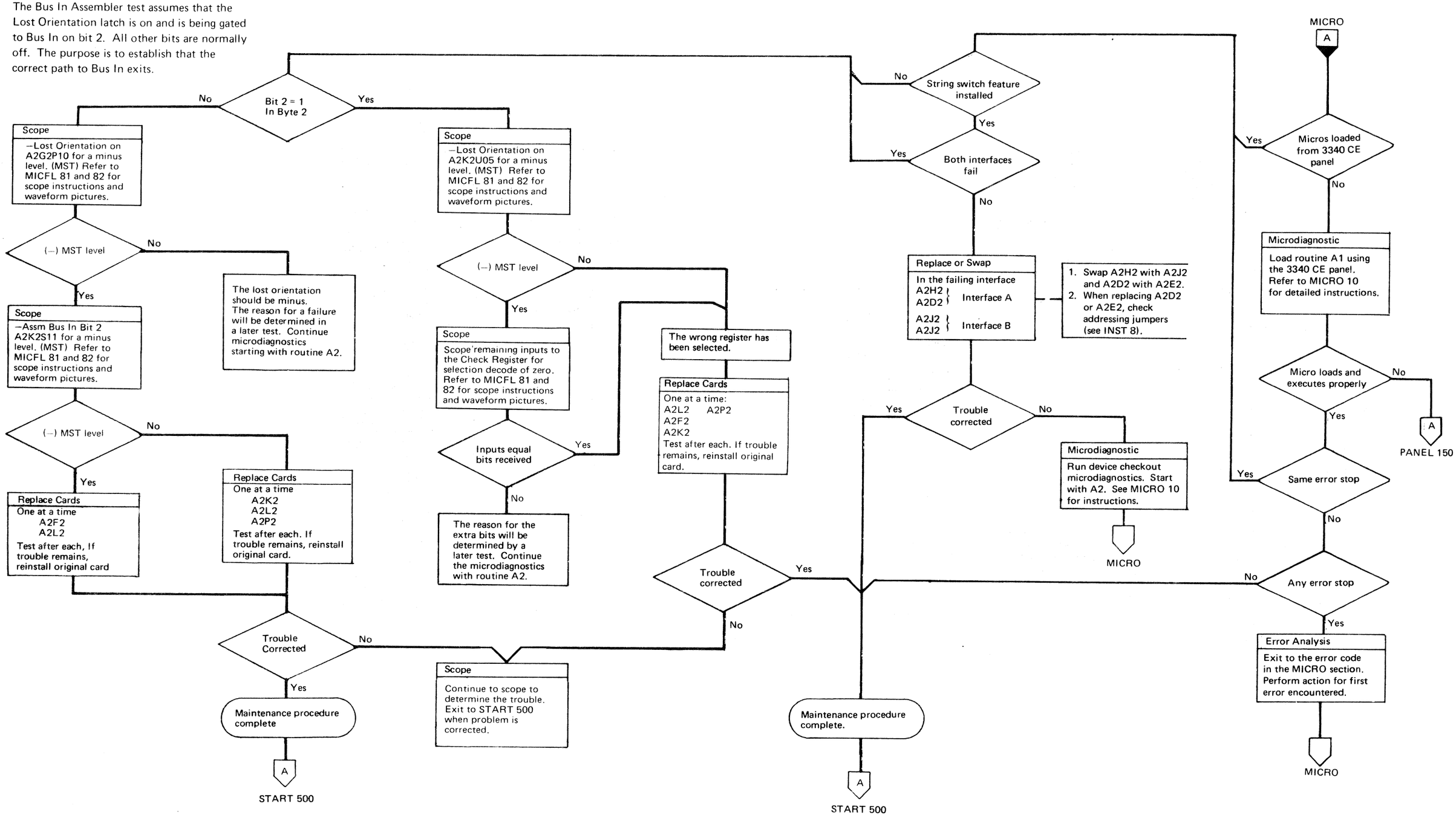


BUS IN ASSEMBLER FAILURE



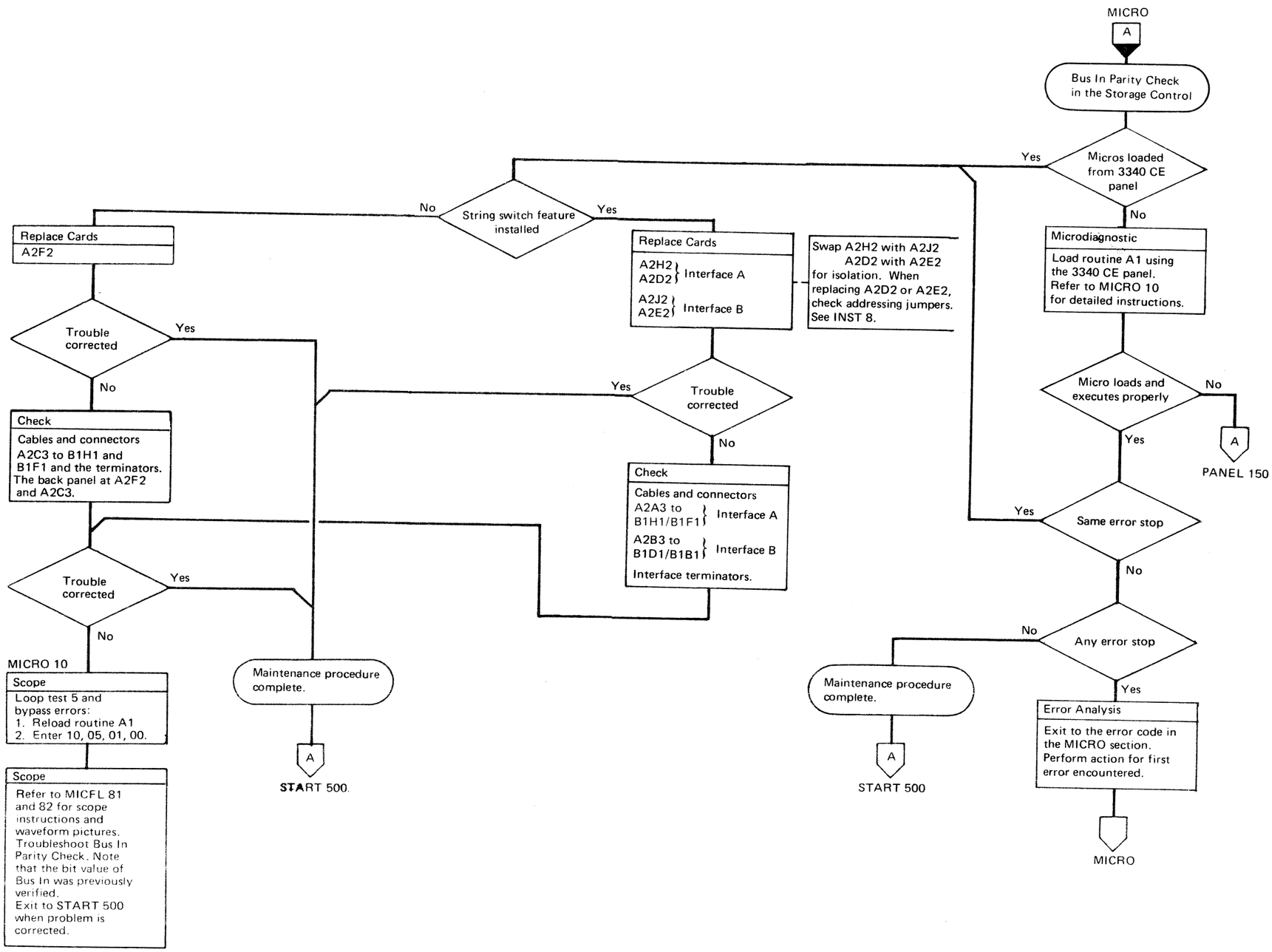
BUS IN ASSEMBLER TEST

The Bus In Assembler test assumes that the Lost Orientation latch is on and is being gated to Bus In on bit 2. All other bits are normally off. The purpose is to establish that the correct path to Bus In exits.



BUS IN ASSEMBLER TEST

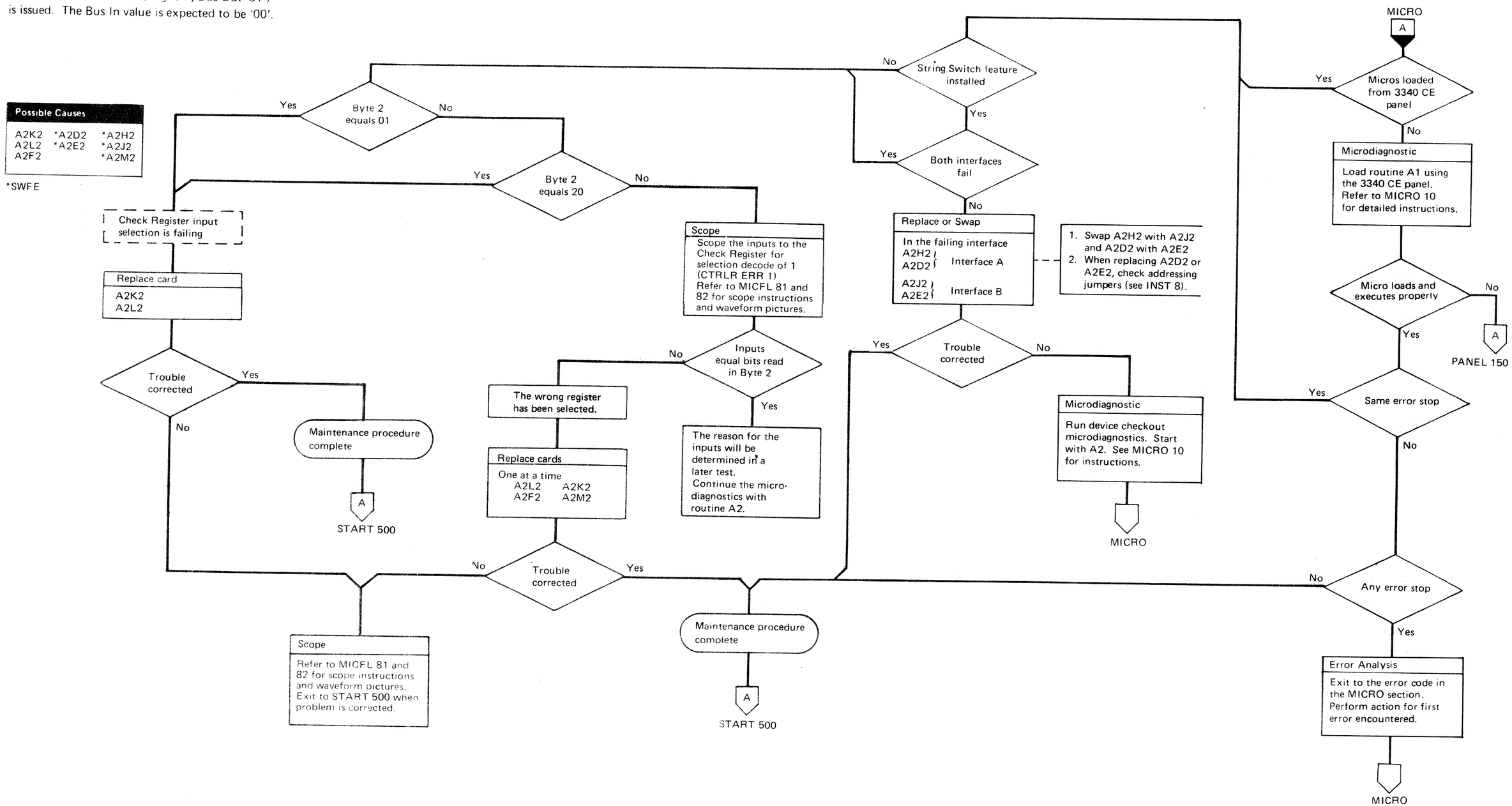
The bits on Bus In are checked and then Parity is checked in the Storage Control. A Bus In Parity Check in the Storage Control indicates that the Parity generator is not functioning properly or that some external force is affecting the Parity bit.



3340	BQ0450 Seq. 2 of 2	2747597 Part No. ( )	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440224 15 Dec 75			

BUS IN ASSEMBLER TEST

Sense Controller Error 1 (Tag '04', Bus Out '01') is issued. The Bus In value is expected to be '00'.

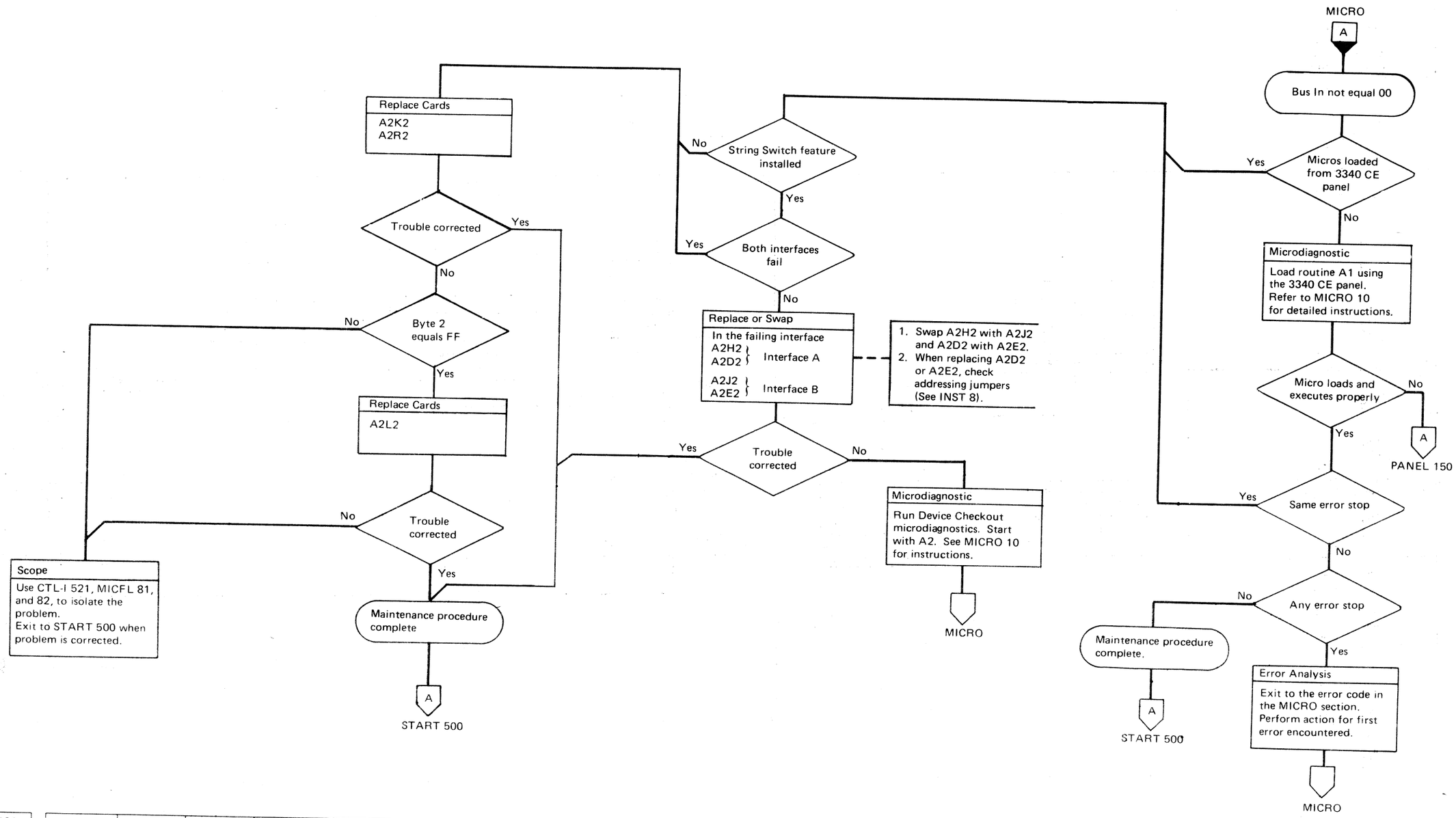


On successive operations, the two ECC Pattern bytes are sensed (Tag '04', Bus '8D' and Tag '04', Bus '40'). Since the ECC Shift Register, which supplies the pattern bytes, is normally reset to zeroes, zeroes are expected on Bus In for both bytes.

Possible Causes

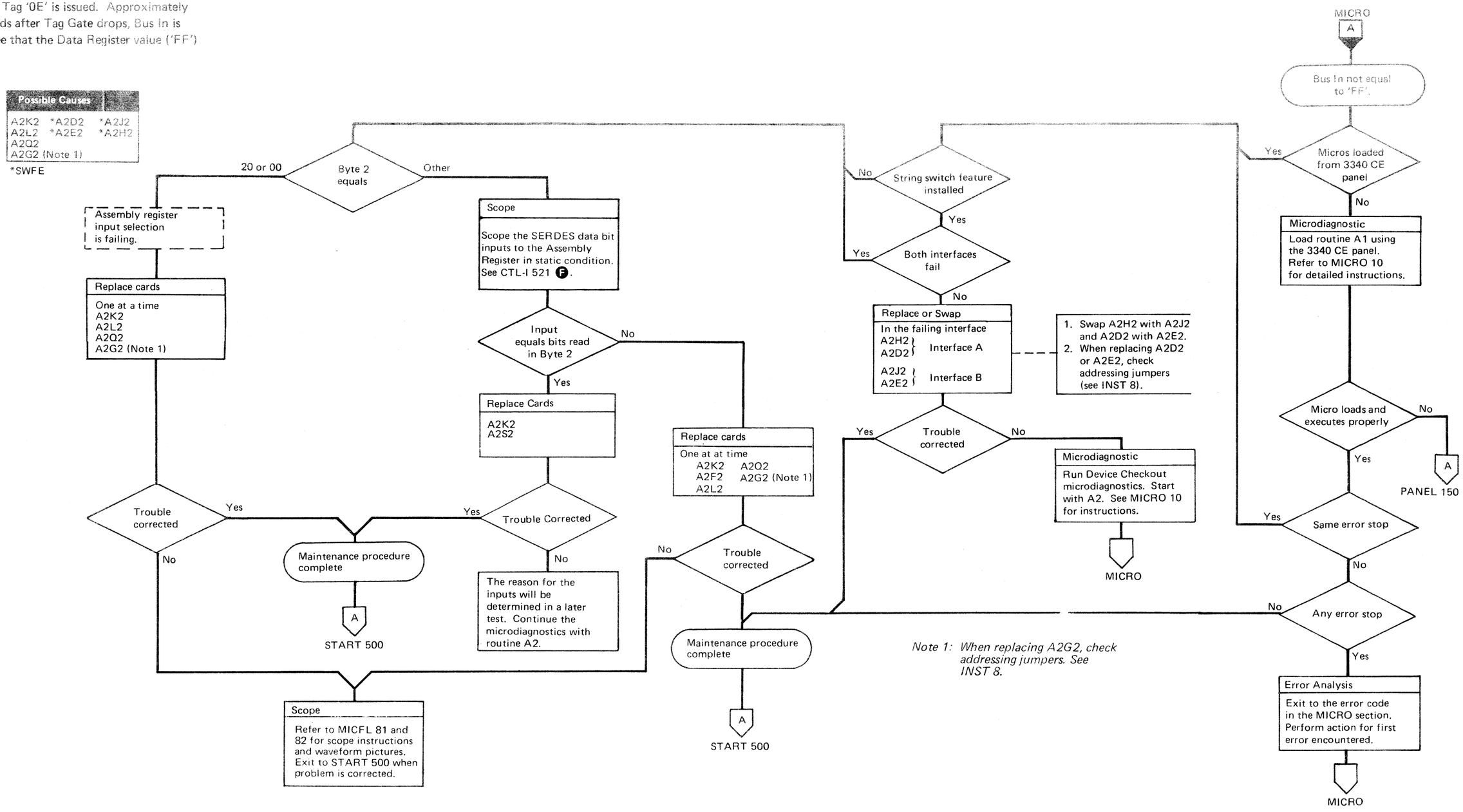
A2K2	*A2E2	*A2H2
A2L2	*A2J2	*A2M2
*A2D2	A2R2	

*SWFE

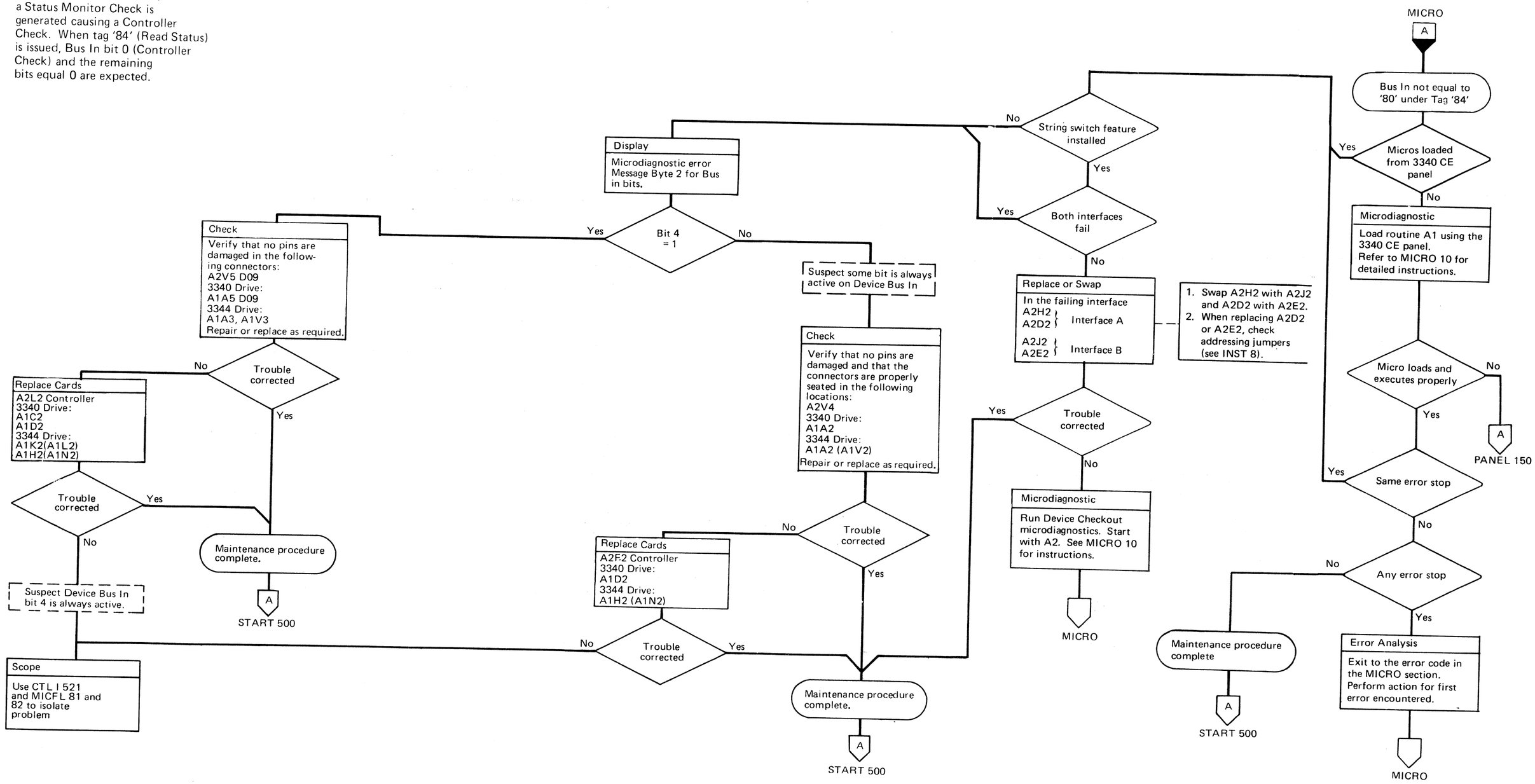


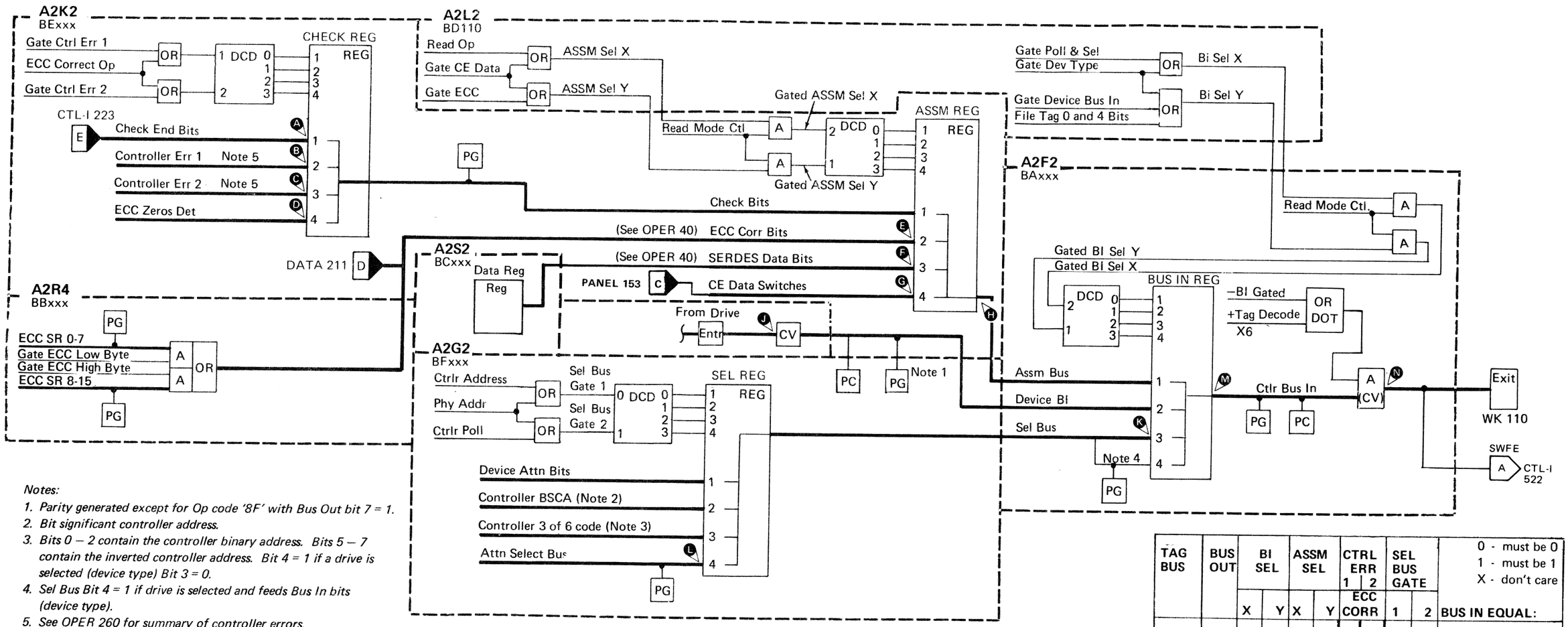
BUS IN ASSEMBLER TEST

The Data Register is normally reset to all bits on ('FF'). Read Tag '0E' is issued. Approximately 2 microseconds after Tag Gate drops, Bus In is checked to see that the Data Register value ('FF') is present.



During Routine A1 Test 5, a Status Monitor Check is generated causing a Controller Check. When tag '84' (Read Status) is issued, Bus In bit 0 (Controller Check) and the remaining bits equal 0 are expected.





Notes:

1. *Parity generated except for Op code '8F' with Bus Out bit 7 = 1.*
2. *Bit significant controller address.*
3. *Bits 0 – 2 contain the controller binary address. Bits 5 – 7 contain the inverted controller address. Bit 4 = 1 if a drive is selected (device type) Bit 3 = 0.*
4. *Sel Bus Bit 4 = 1 if drive is selected and feeds Bus In bits (device type).*
5. *See OPER 260 for summary of controller errors.*

		Check End (A)	Ctrlr Err 1 (B)	Ctrlr Err 2 (C)	ECC Zero Detect (D)	ECC Corr Bits (E)	Serdes Data (F)	CE Data Sws. (G)	Assm Bus (H)	Dev Bus In (J)	Sel Bus (K)	Attn Sel (L)	Contr Bus In (M)	Contr Bus In (N)	
Card Loc	A2K2	A2K2	A2K2	A2K2	A2K2	A2K2	A2K2	A2K2	A2F2	A2F2	A2G2	A2F2	A2F2		
Bit 0	S03	U02	S02	–	D03(+)	P07	G10	M07	B10 see logic	B02	U03	P05	D06		Bit 0
Bit 1	U04	S04	U03	–	G09(+)	P09	J10	M09	B07	D04	U04	M10	B03		Bit 1
Bit 2	U05	P12(+)	S05	–	J12(+)	S10	U10	S11	G03	B04	U06	M08	D10	plus	Bit 2
Bit 3	U09	S08	S07	–	U11(+)	U12	S12	S13	B09	B05	U07	S07	D09	NPL	Bit 3
Bit 4	G03	M08	P05	–	G02(+)	P02	G13	M02	G12 plus	D11	S08	P06	J02	at	Bit 4
Bit 5	P03	–	P06	–	J05(+)	P04	J13	M04	J04 NPL	B12	U10	U03	J07	inter	Bit 5
Bit 6	B03/See logic	–	U06	–	B04(+)	M10	P10	M11	G05	J06	U11	P09	J11	face	Bit 6
Bit 7	G04/	–	S09	S09	J04(+)	P13	P11	M13	G13	G08	S12	U06	J03		Bit 7
Bit P	Gen	Gen	Gen	Gen	G12(+)	J07	J11	G09	J13	G04	S04(S Bit)	U04	J12		Bit P

TAG BUS	BUS OUT	BI SEL X	BI SEL Y	ASSM SEL X	ASSM SEL Y	CTRL ERR 1 ECC CORR	CTRL ERR 2	SEL BUS GATE 1	SEL BUS GATE 2	BUS IN EQUAL:
–	–	0	0	0	0	0	0	X	X	Check End
04	02	0	0	0	0	0	1	X	X	Controller Err 2
04	01	0	0	0	0	1	0	X	X	Controller Err 1
08	–	0	0	0	0	1	1	X	X	ECC Zero Det.
04	80	0	0	0	1	X	X	X	X	ECC Lo Byte
04	40									ECC Hi Byte
0E	–	0	0	1	0	X	X	X	X	SERDES Data Byte
0A	40	0	0	1	1	X	X	X	X	CE Data Switches
84 & 89 to 8F	–	0	1	X	X	X	X	X	X	Device Bus In
82	–	1	0	X	X	X	X	0	0	Device Attn Bit
02	–	1	0	X	X	X	X	0	1	Controller BSCA
03 to 83	–	1	0	X	X	X	X	1	0	Controller CA·$\overline{CA}$
04	10	1	0	X	X	X	X	1	1	Attn Sel Bits
0A	80	1	1	X	X	X	X	X	X	Device Type

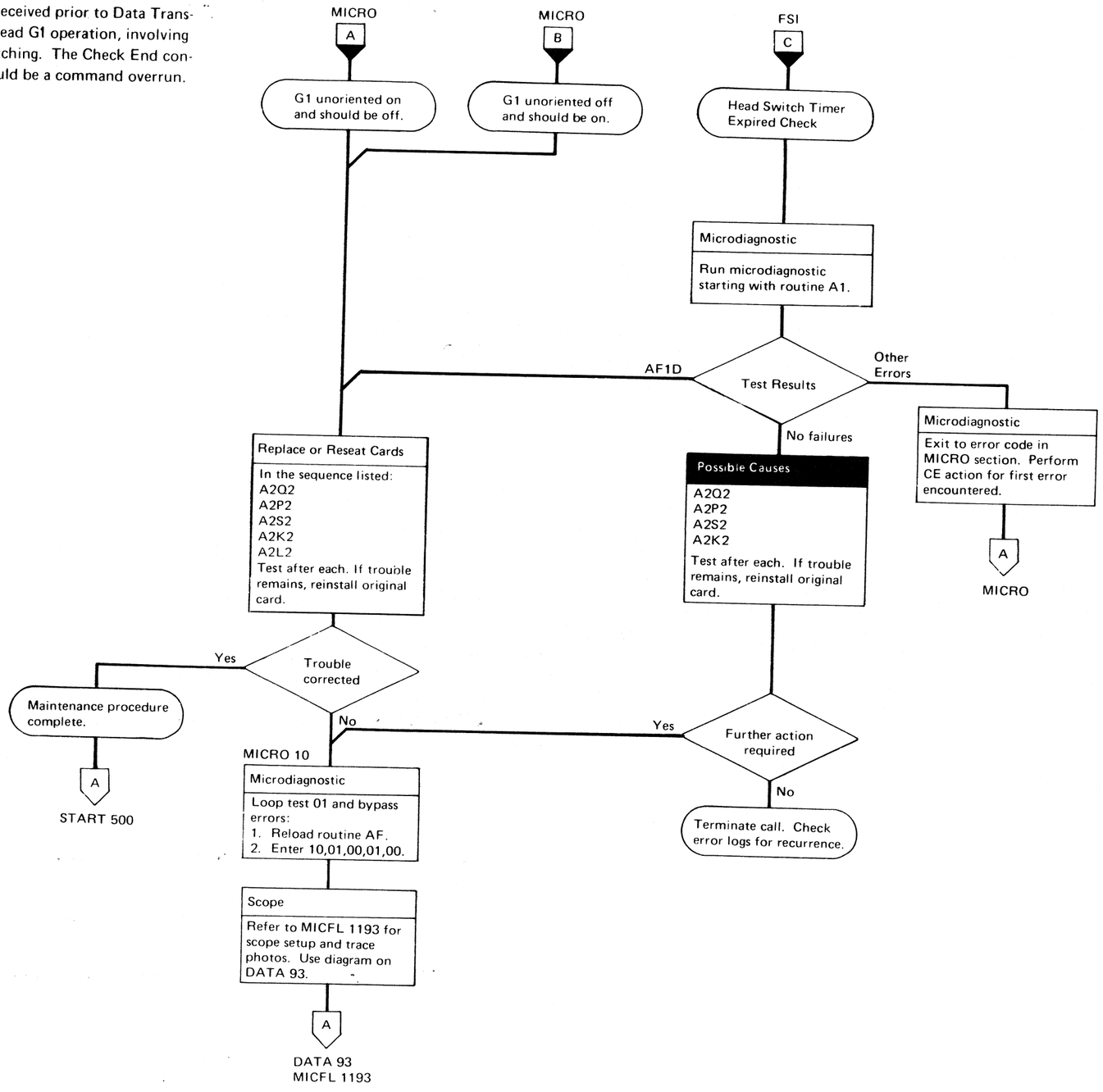
0 - must be 0
1 - must be 1
X - don't care

3340

BQ0800	2747543	440200	440202	440203	440204	440213		
Seq. 1 of 1	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	13 May 74		

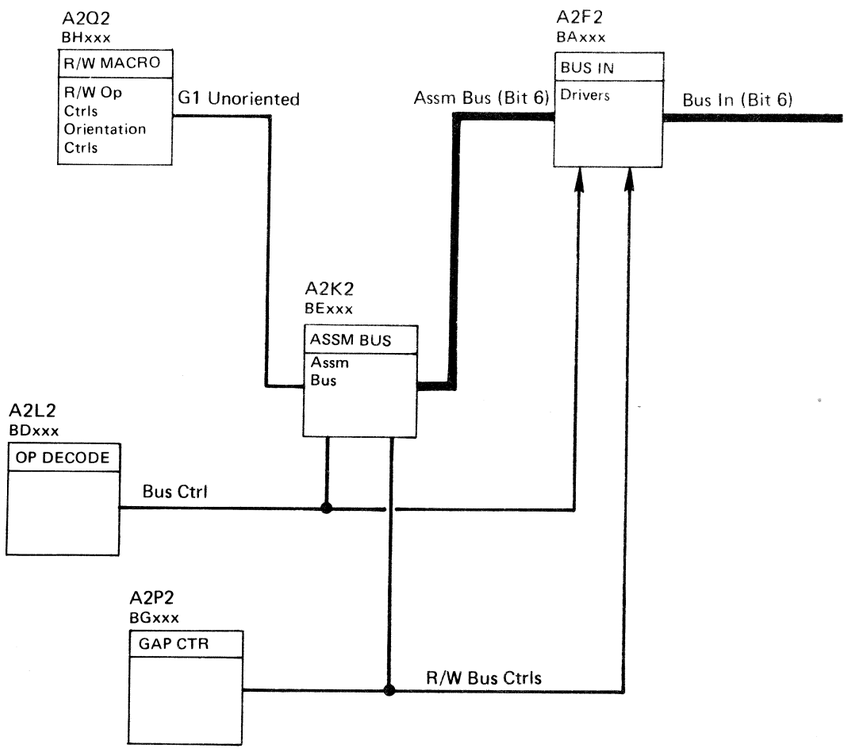
DATA CONTENTS

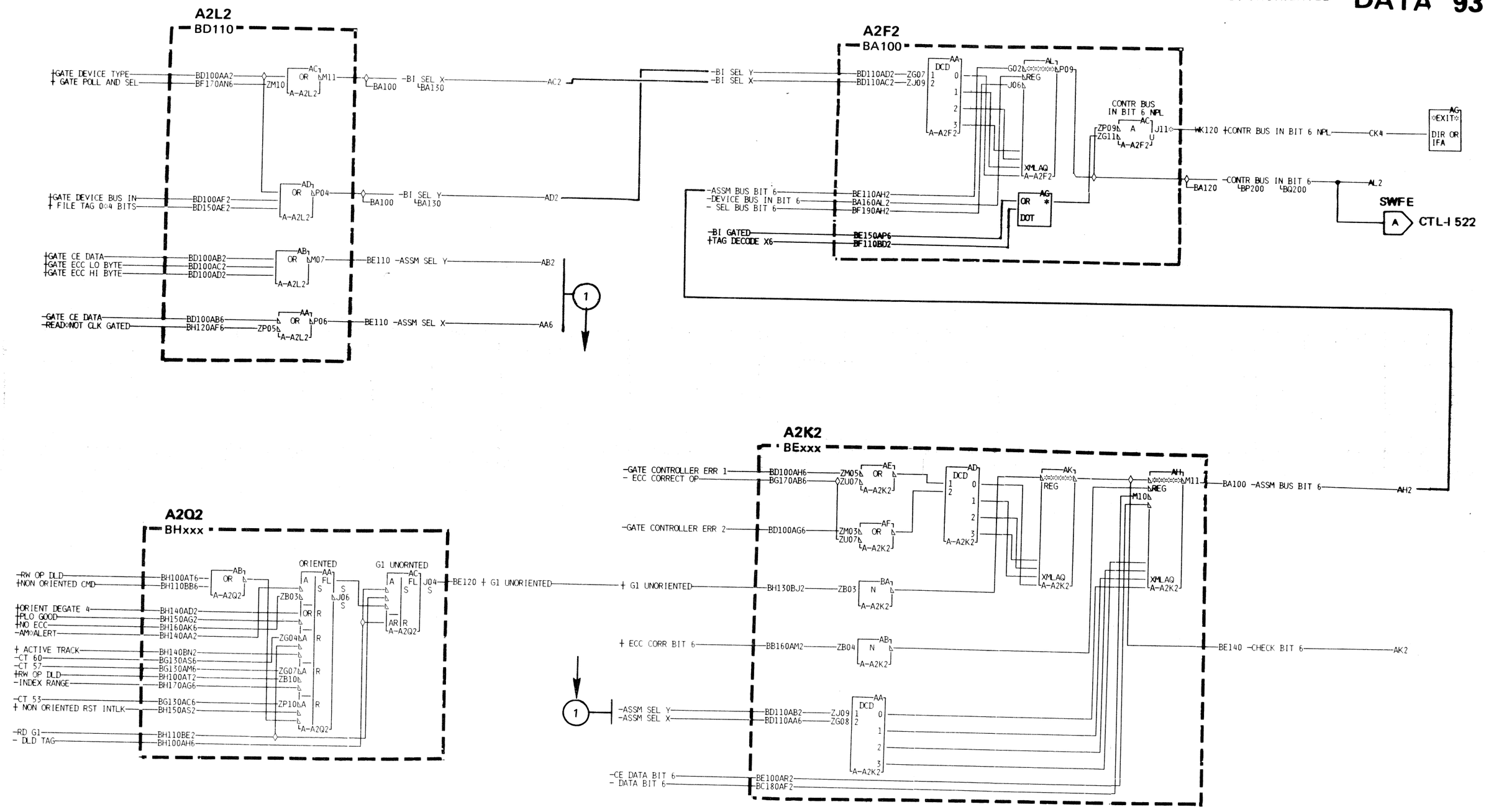
This stop indicates that a Check End has been received prior to Data Transfer on a Read G1 operation, involving Head Switching. The Check End condition would be a command overrun.



EARLY CHECK END DATA 90

EARLY CHECK END





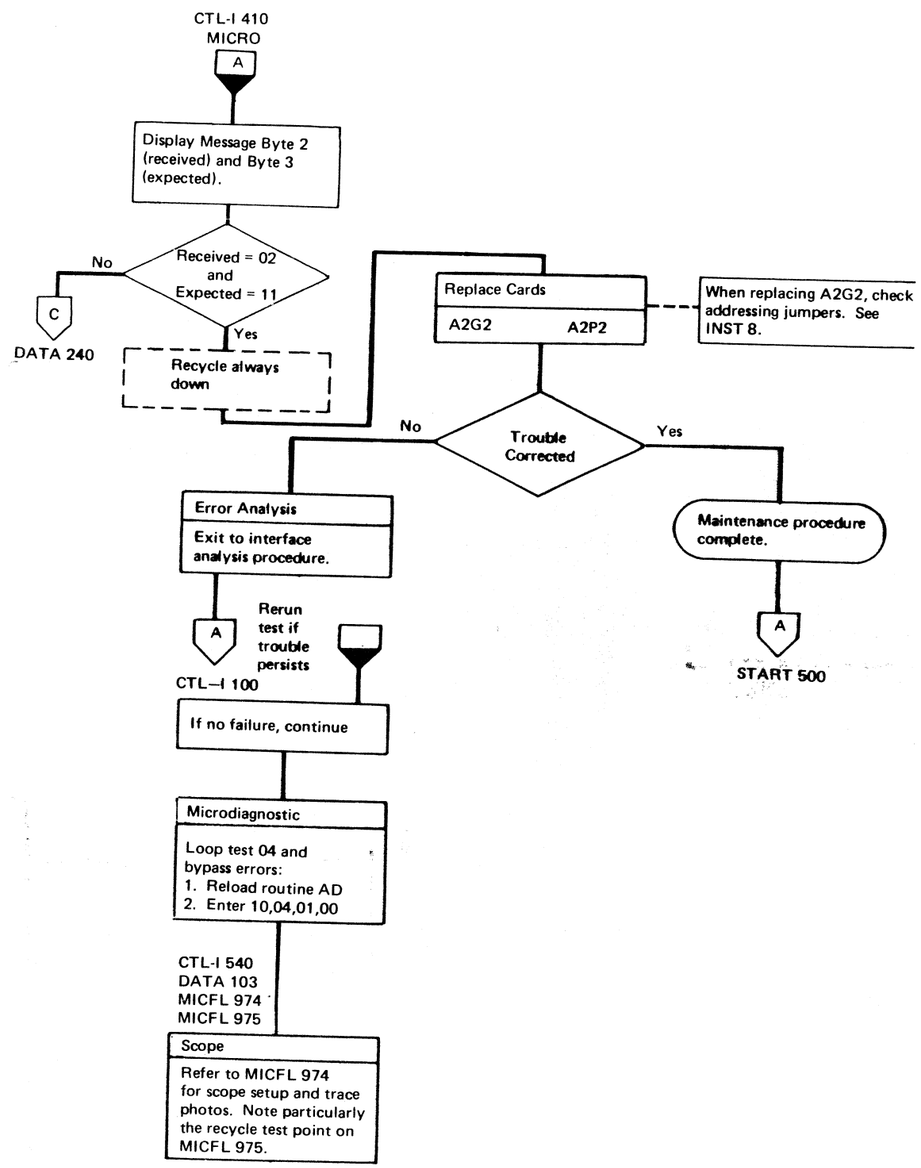
3340

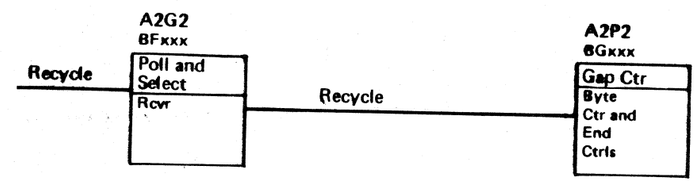
BT0100 Seq. 1 of 2	2747545 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74		

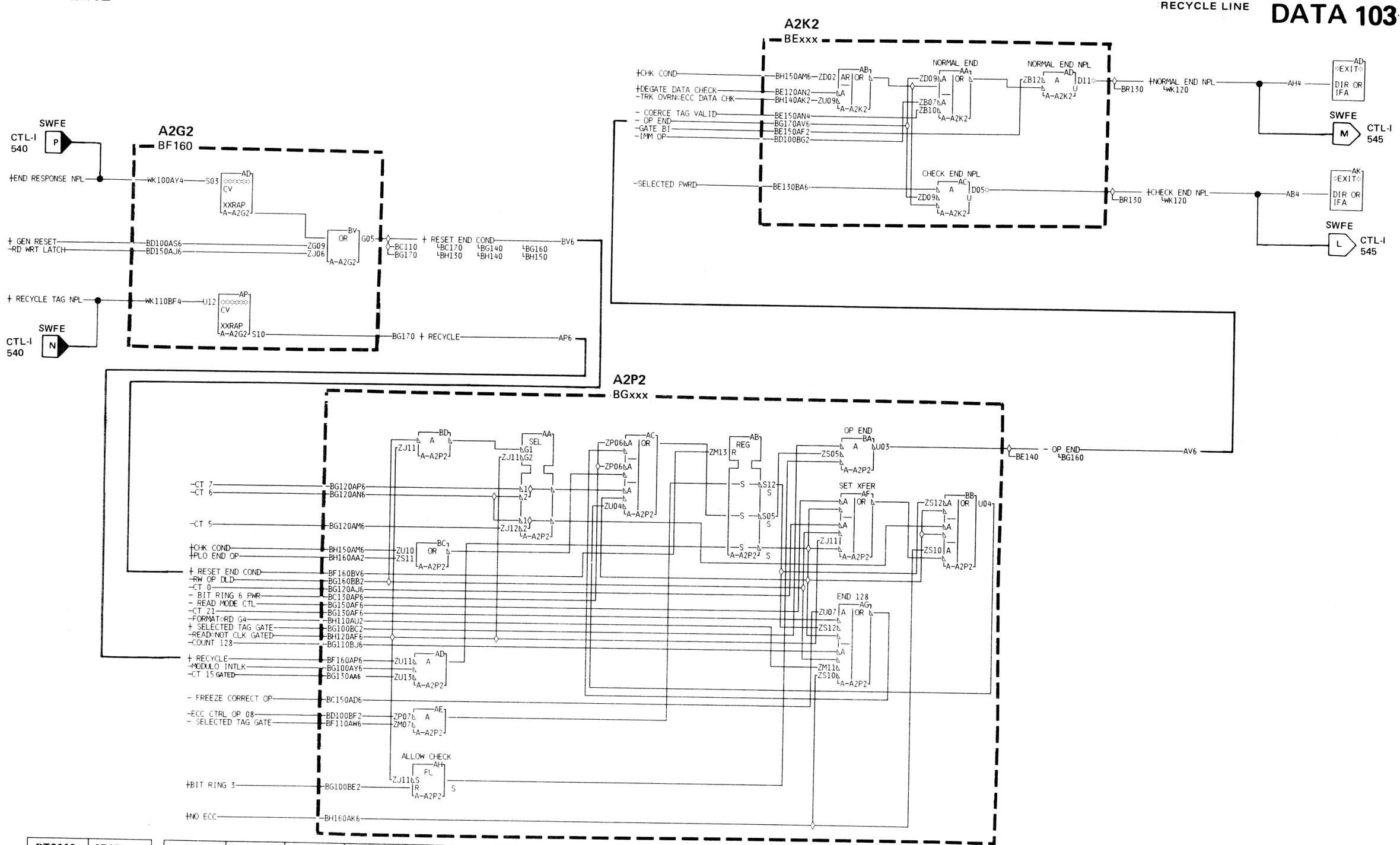
RECYCLE LINE

The Recycle line, in conjunction with the counter in Modulo 16 mode, determines when the interface operations are terminated. The Recycle line is raised by storage control to signal that more than 16 byte-times of interface operation is required. The Recycle line is dropped when less than 8 byte-times remain. If less than 16 byte times are required, Recycle is not raised.

The counter equal to 15 and Recycle line down set the End Data latch. End Data latch in turn starts an ending sequence in the controller. A premature or delayed ending may indicate Recycle line failure.





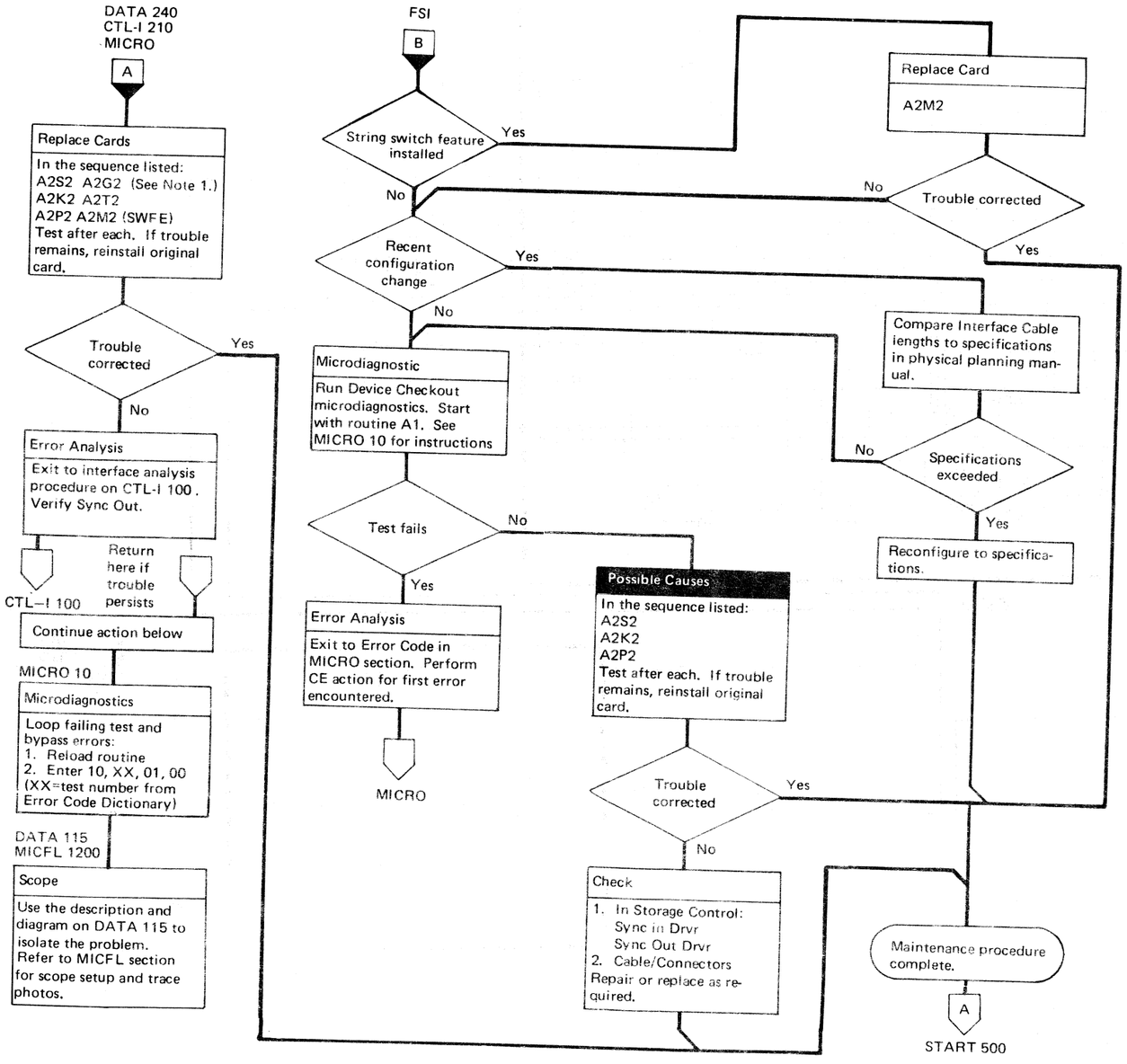


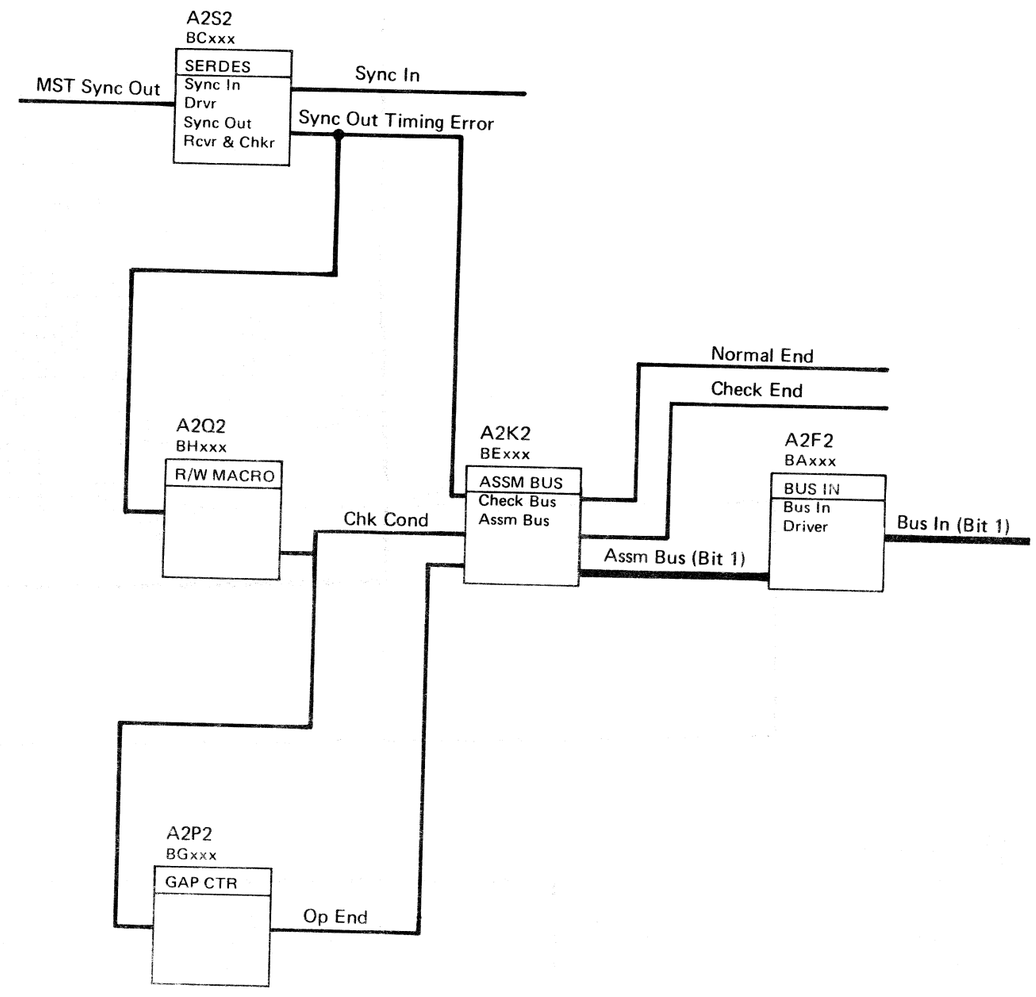
3340

BT0110	2747546	See EC History	440224	440227			
Seq. 1 of 2	Part No. (1)		15 Dec 75	14 Sept 76			

Sync Out Timing error check ensures that one and only one Sync Out is received for each Sync In. It also ensures that Sync Out is received within proper time limits. The time limits are approximately 885 ns for Read and 750 ns for Write.

Note: Cable lengths exceeding specifications can cause this problem.





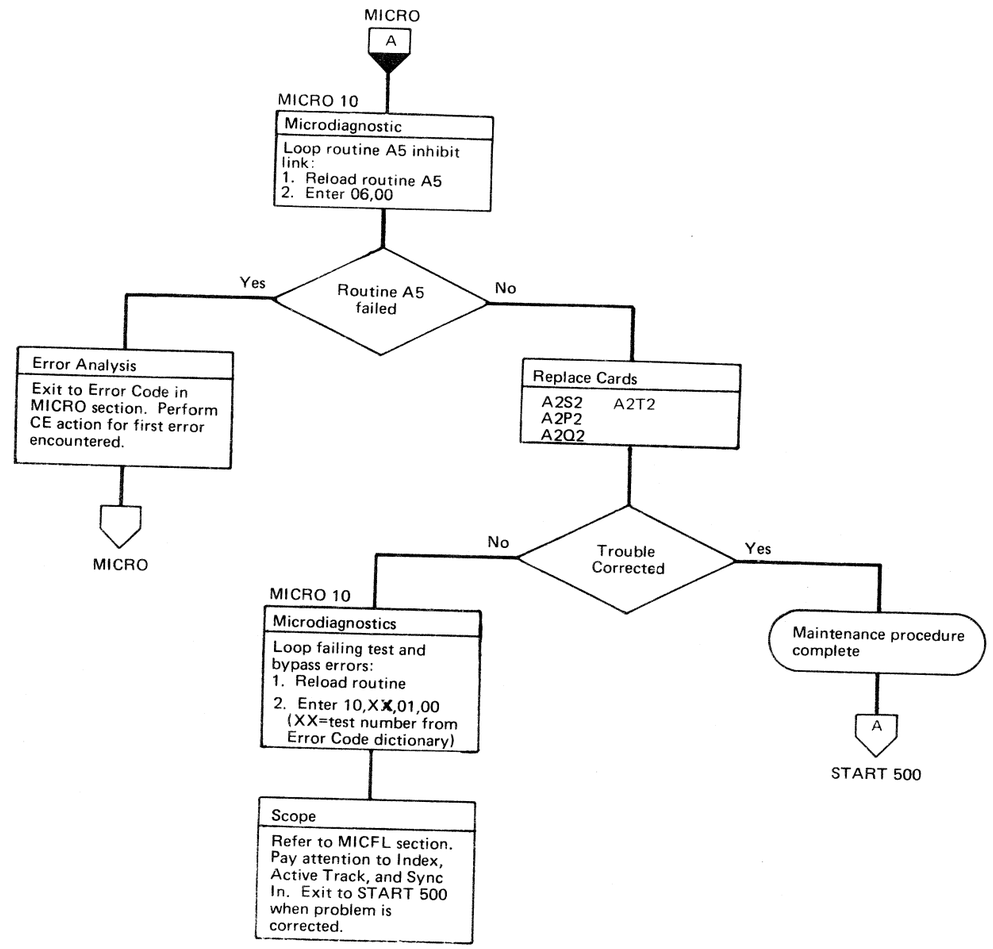
Note 1: When replacing A2G2, check addressing jumpers. See INST 8.

BT0110	2747546	See EC History	440224	440227				
Seq. 2 of 2	Part No. (1)		15 Dec 75	14 Sept 76				

TIMEOUT WAITING FOR RESPONSE FROM CONTROLLER

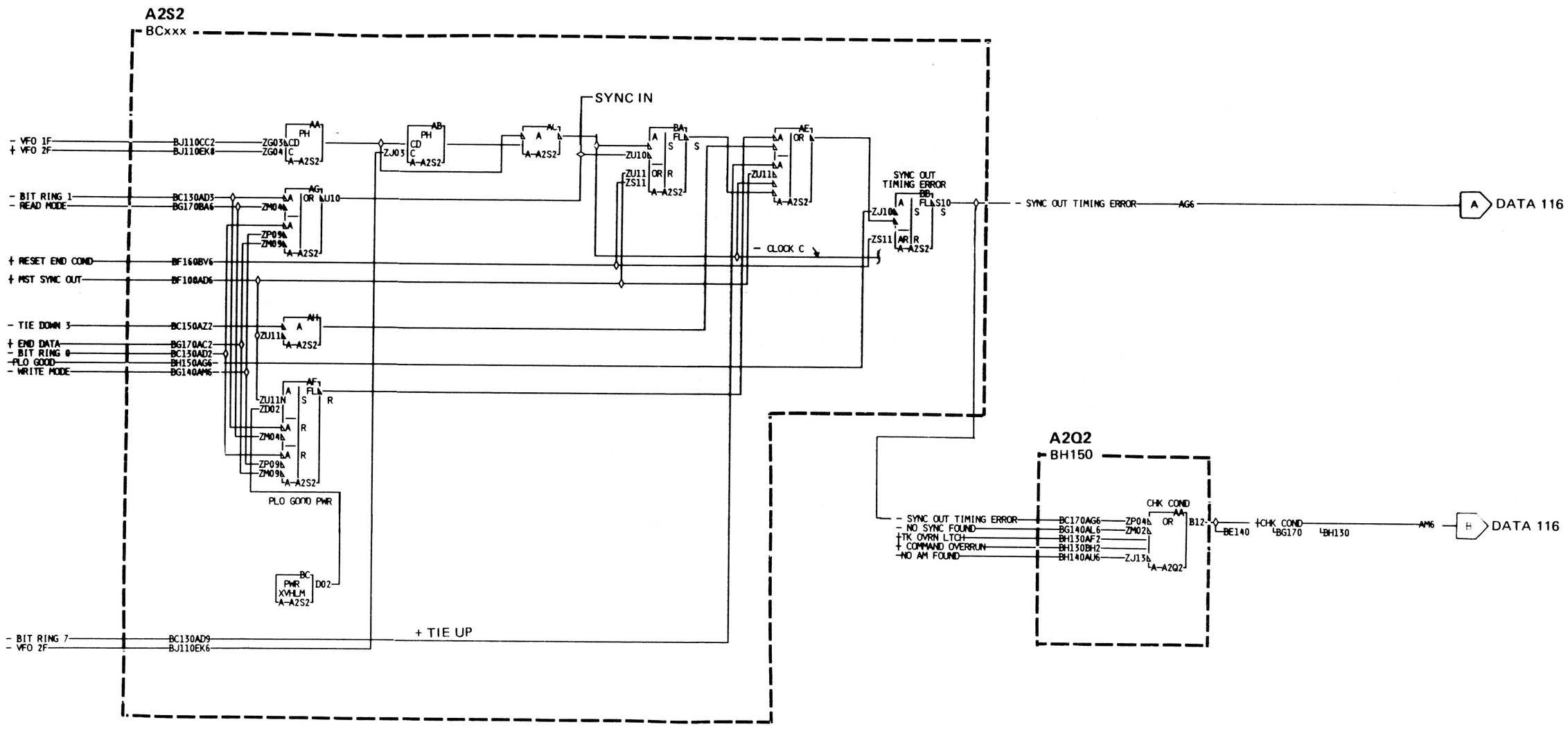
This indication is caused by a time-out condition in the Storage Control to indicate that the Controller has not responded in a specified period of time. This condition is most commonly caused by a failure to recognize Index or Active Track which is required to establish orientation on a Read or Write Operation.

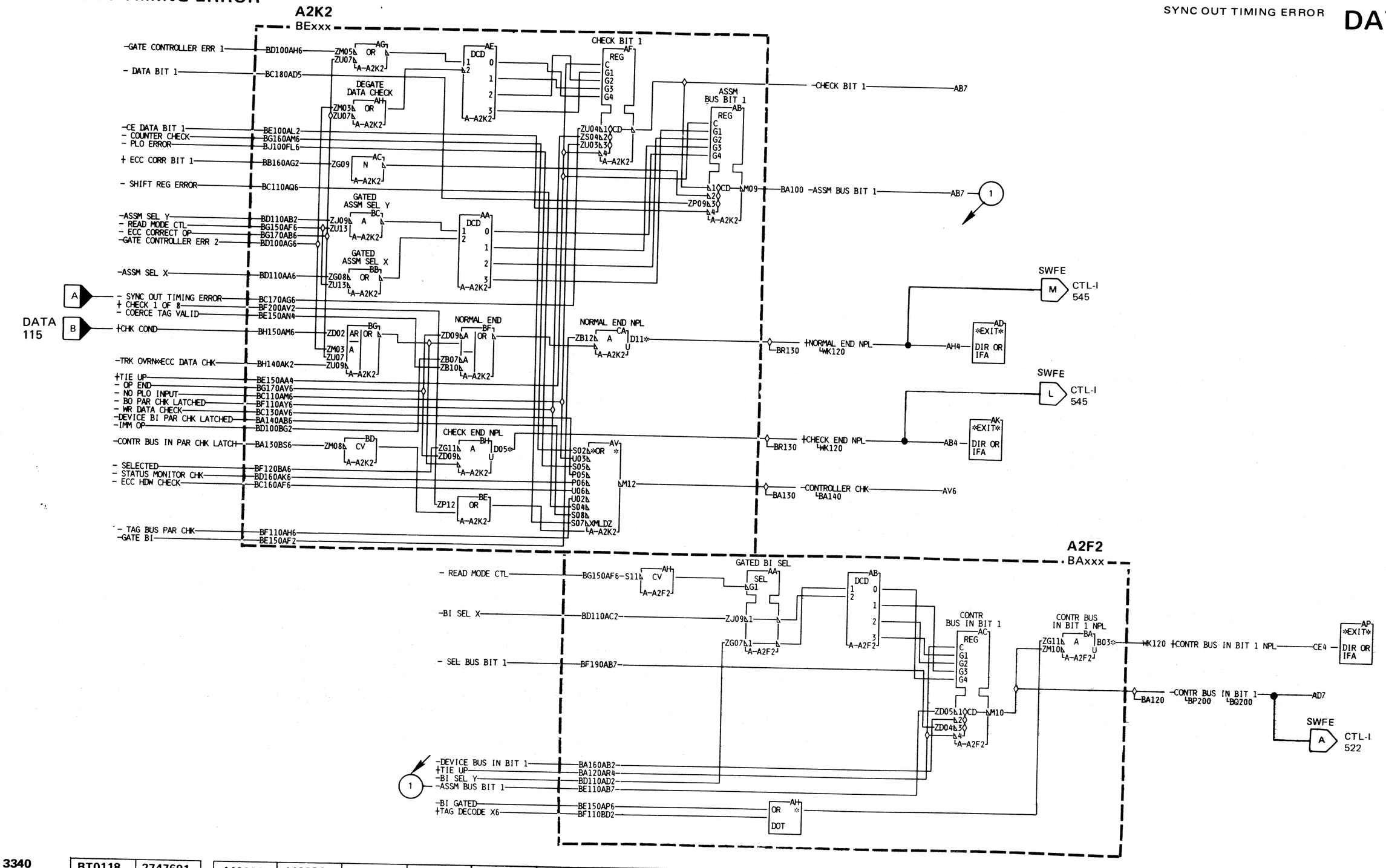
Since routine A5 (the Index and Sector Test) should already have been run. Suspect an intermittent Index or Active Track problem. If routine A5 has not been run, do so at this time.



SYNC OUT TIMING ERROR

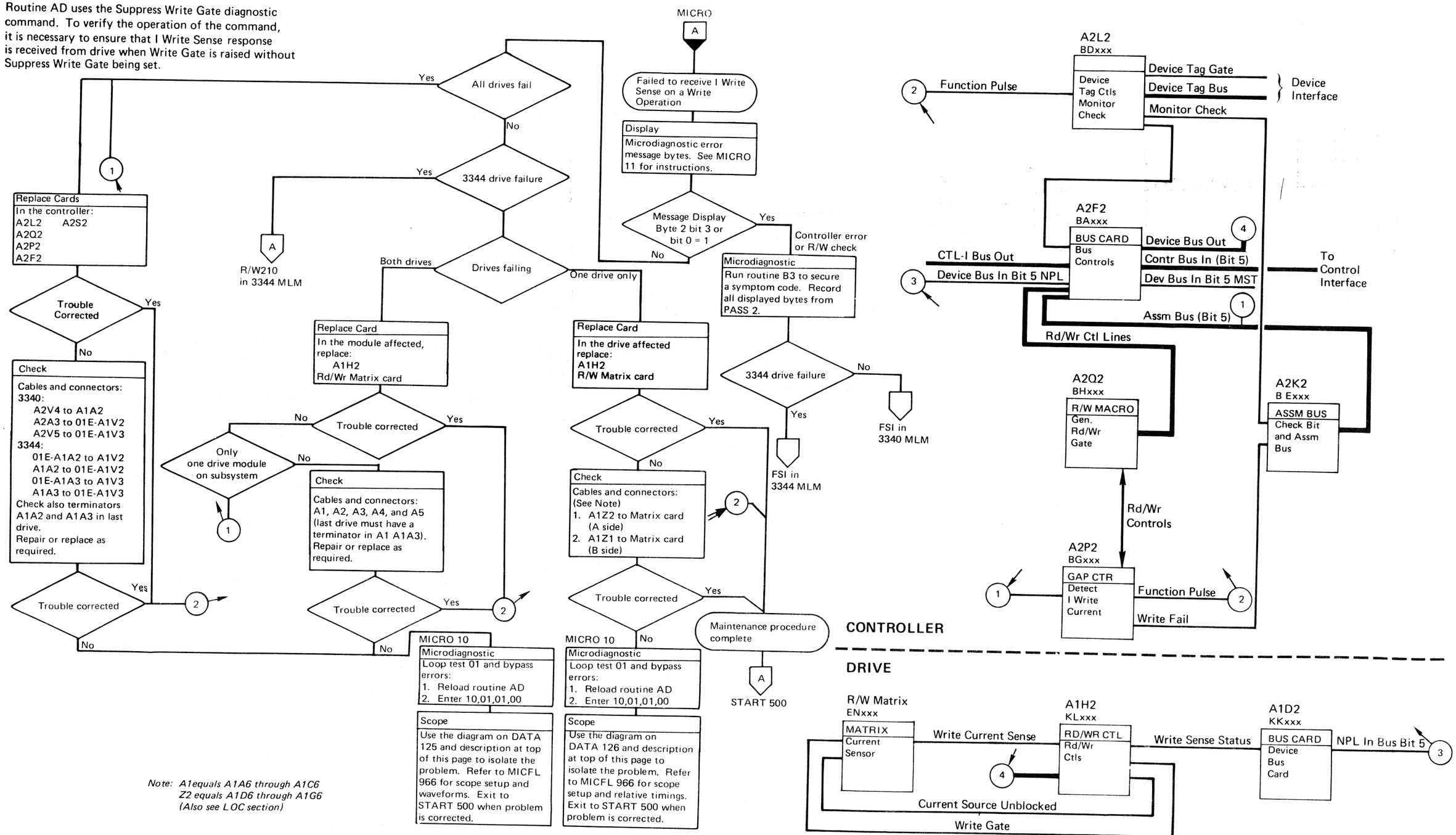
The Sync Out Timing Error Check ensures that one *and only one* Sync Out is received for each Sync In. It also ensures that Sync Out is received within proper time limits. The time limits are approximately 885 ns for Read and 750 ns for Write.





I WRITE SENSE FAILURE

Routine AD uses the Suppress Write Gate diagnostic command. To verify the operation of the command, it is necessary to ensure that I Write Sense response is received from drive when Write Gate is raised without Suppress Write Gate being set.



Note: A1equals A1A6 through A1C6
Z2 equals A1D6 through A1G6
(Also see LOC section)

3340

BT0118	2747691	440203	440204	440209	440213	440224	440227	
Seq. 2 of 2	Part No. (1)	2 Nov 73	21 Dec 73	25 Mar 74	13 May 74	15 Dec 75	14 Sept 76	

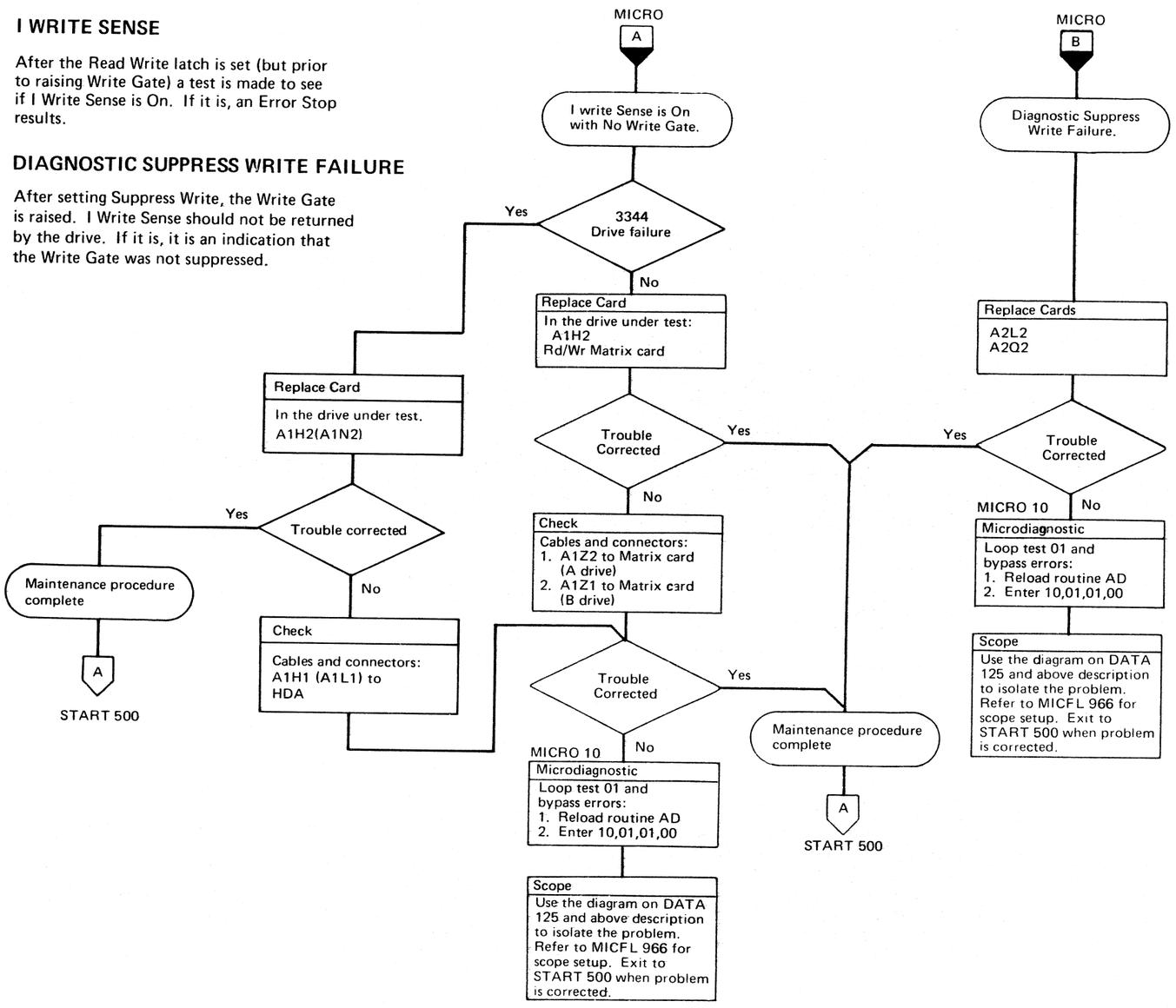
I WRITE SENSE AND SUPPRESS WRITE

I WRITE SENSE

After the Read Write latch is set (but prior to raising Write Gate) a test is made to see if I Write Sense is On. If it is, an Error Stop results.

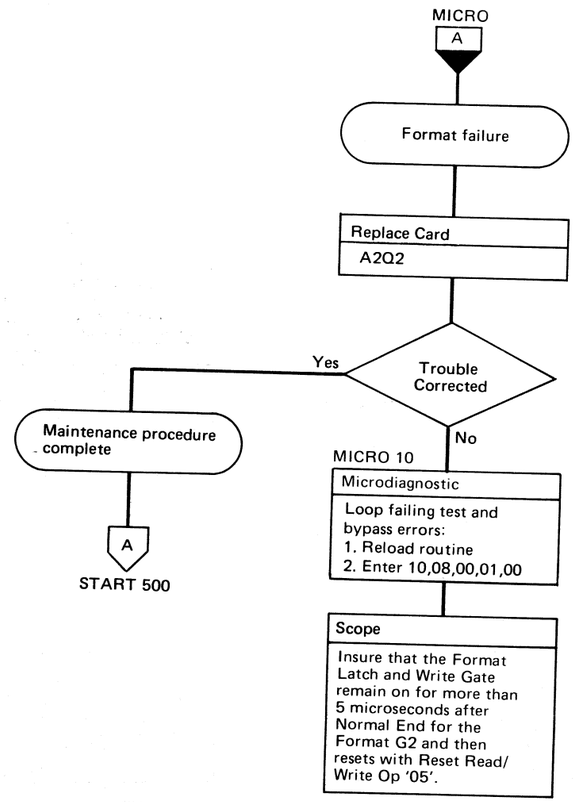
DIAGNOSTIC SUPPRESS WRITE FAILURE

After setting Suppress Write, the Write Gate is raised. I Write Sense should not be returned by the drive. If it is, it is an indication that the Write Gate was not suppressed.



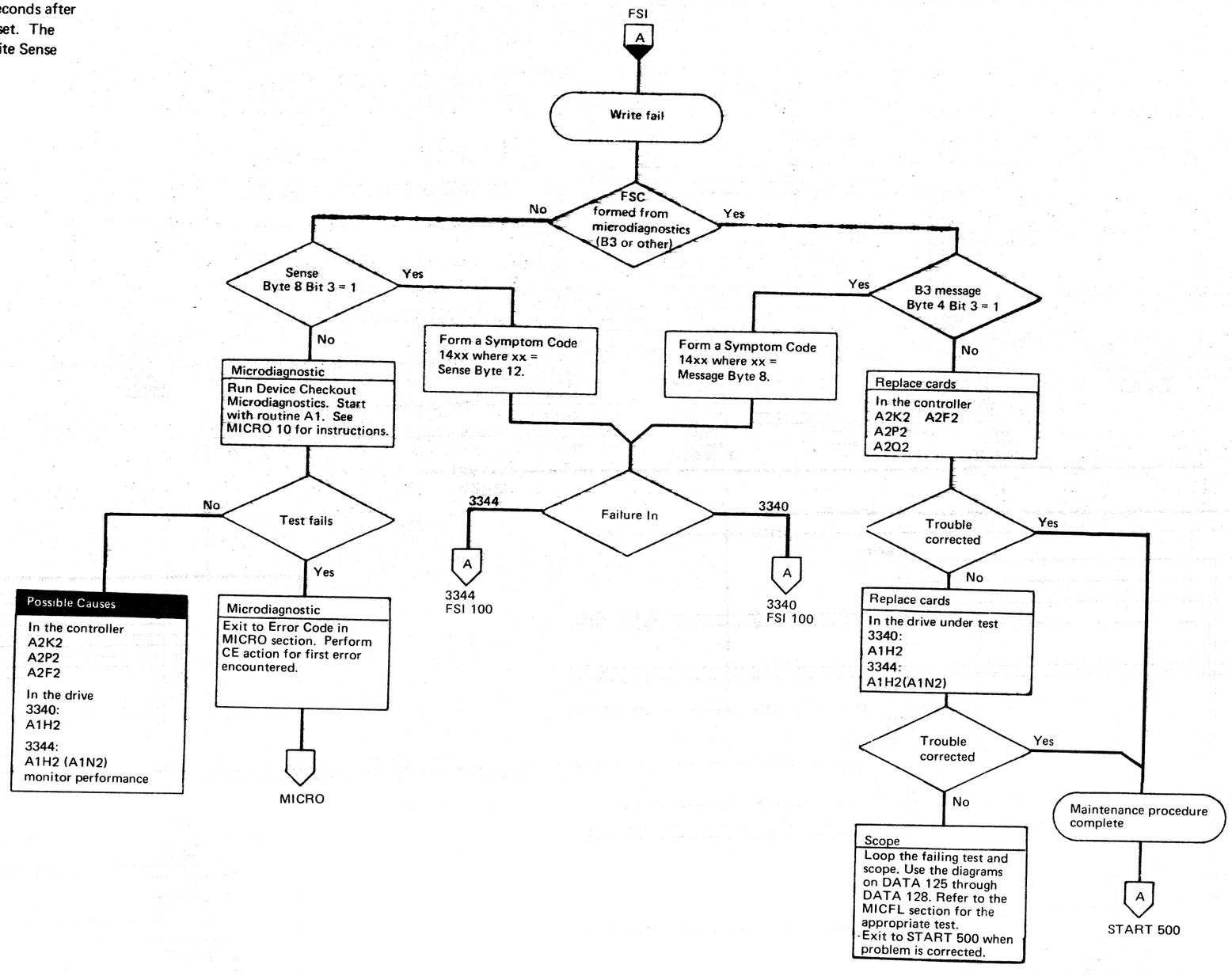
ROUTINE AF TEST 8 CHECKS

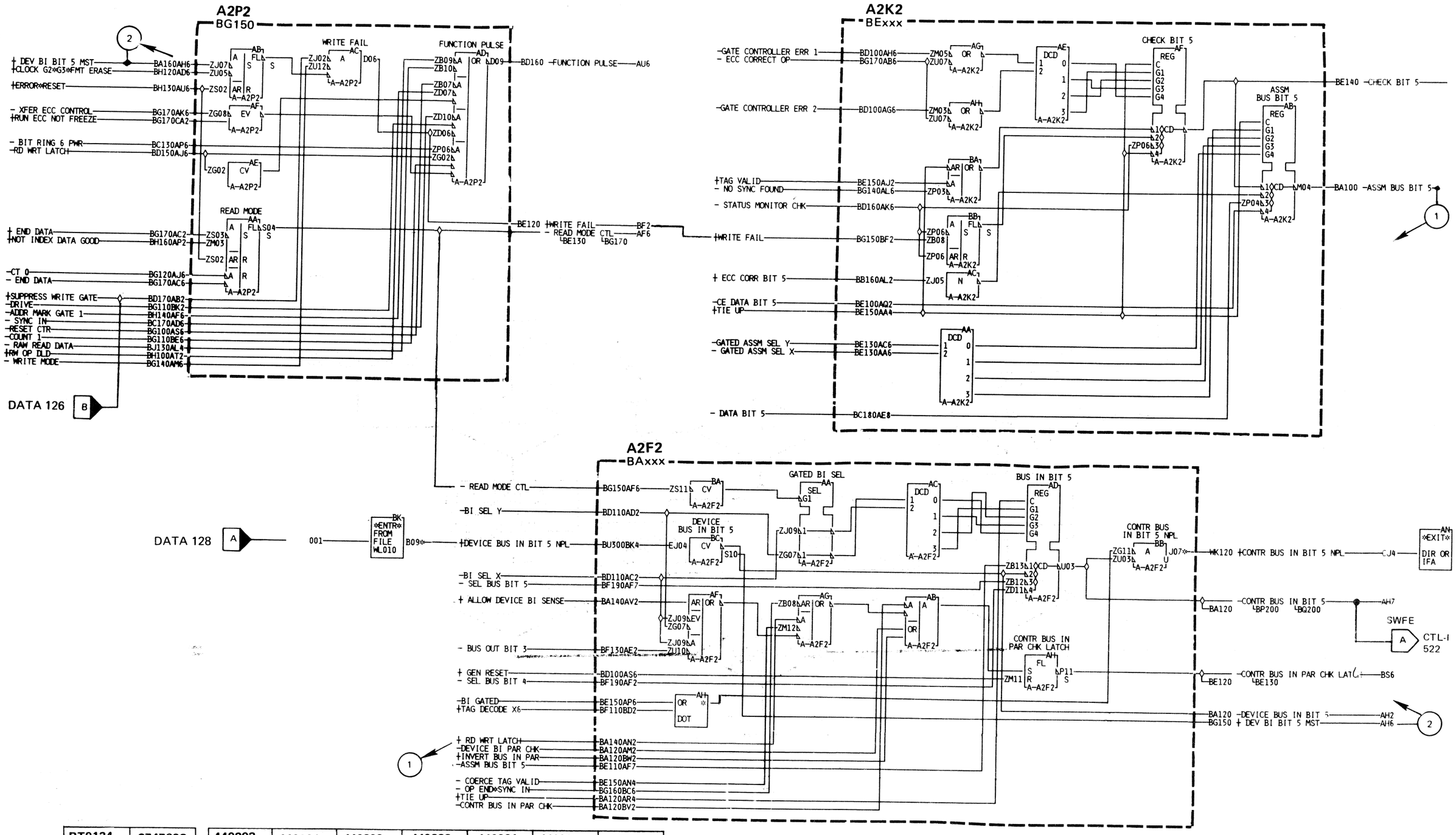
- Padding takes place on format operations by checking that I Write Sense is still on after data and ECC are complete (AF84).
- Padding ceases with Reset Read/Write Command (AF85).
- These are tests of the format latch operation.



WRITE FAIL

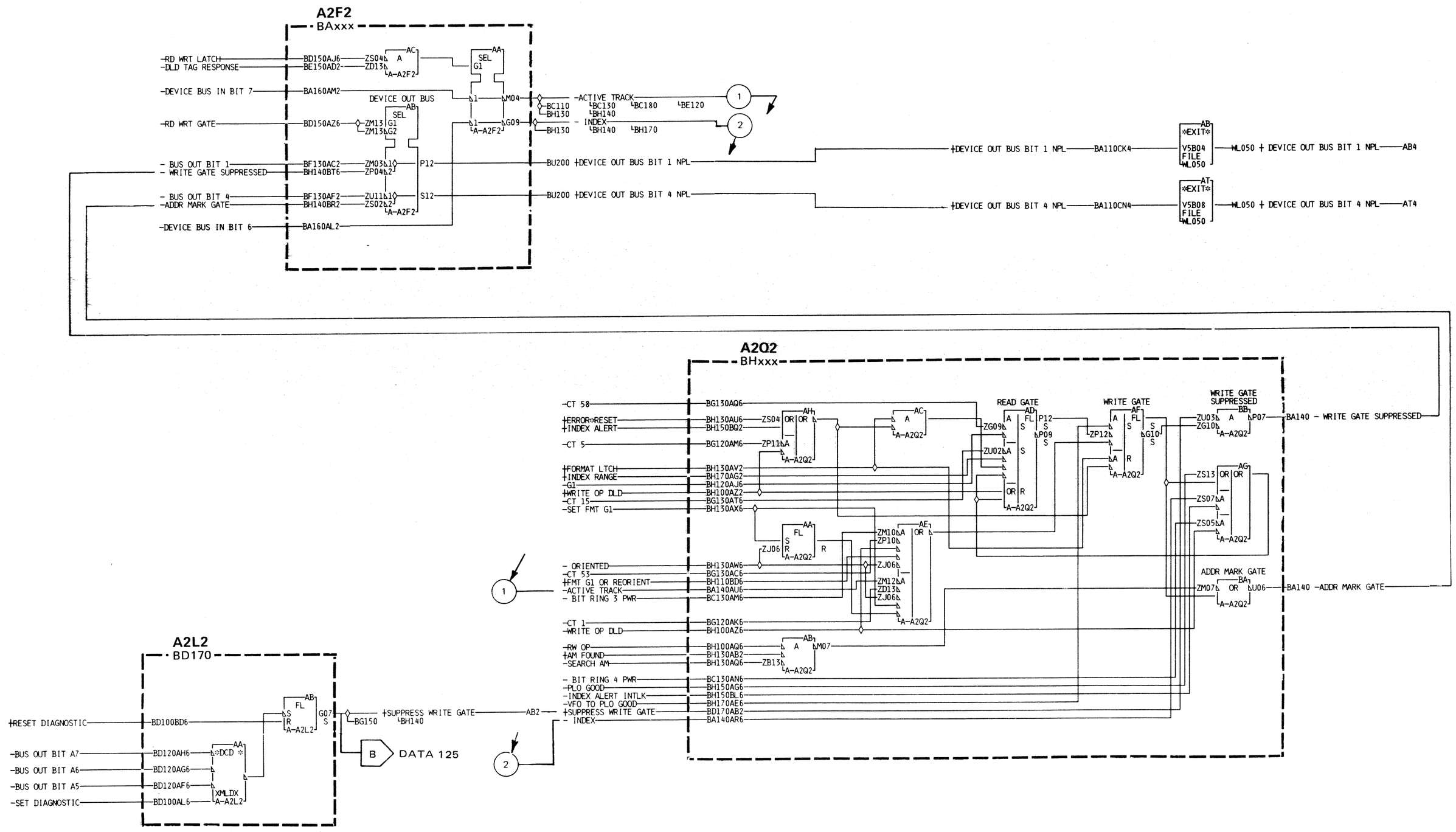
If I Write Sense (Device Bus In bits) is not received by the controller within approximately nine microseconds after the rise of Write Gate, the Write Fail latch is set. The Monitor Check also sets as a result of an I Write Sense failure.



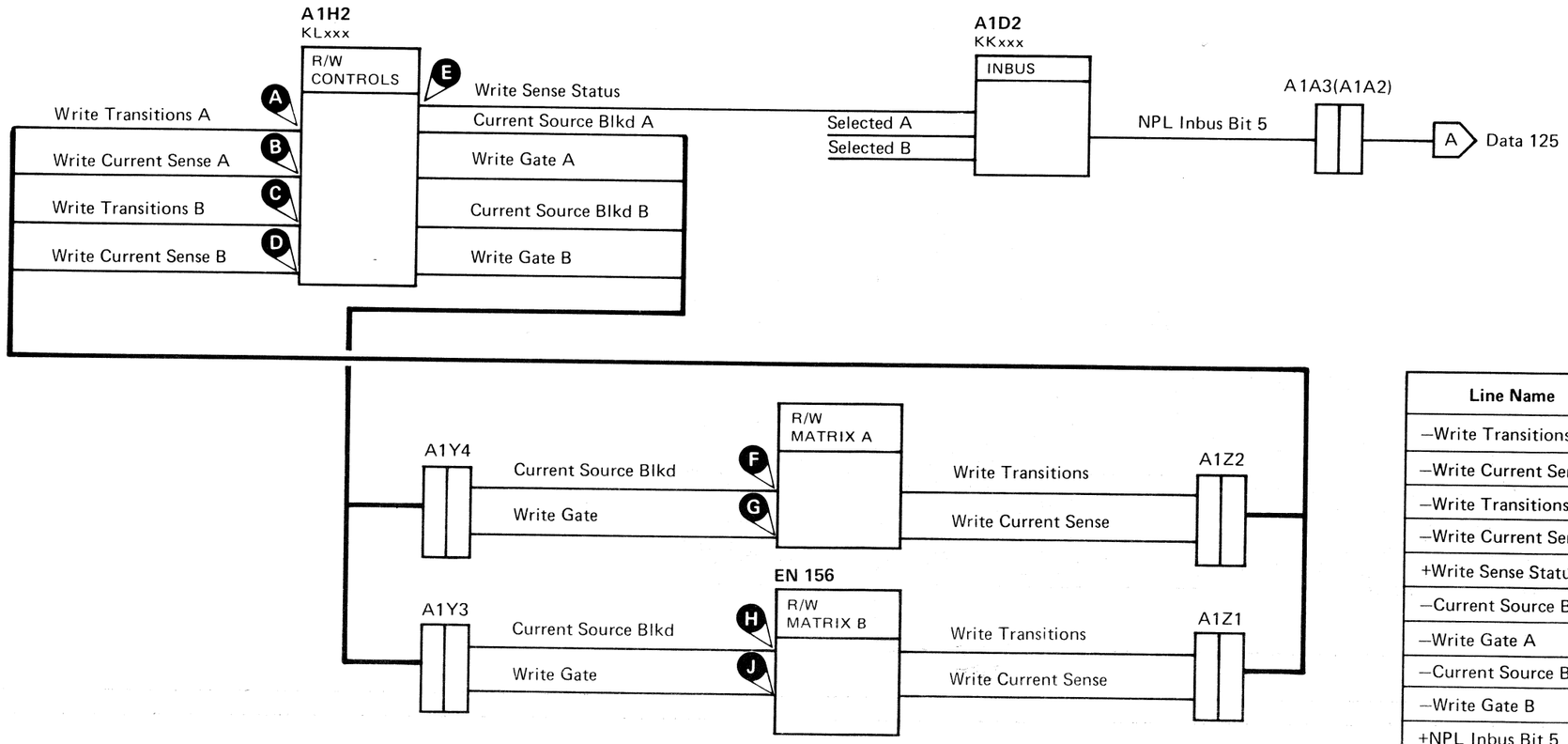


BT0124	2747692	440203	440204	440209	440223	440224	440227
Seq. 2 of 2	Part No.(1)	2 Nov 73	21 Dec 73	25 Mar 74	14 Mar 75	15 Dec 75	14 Sept 76

3340

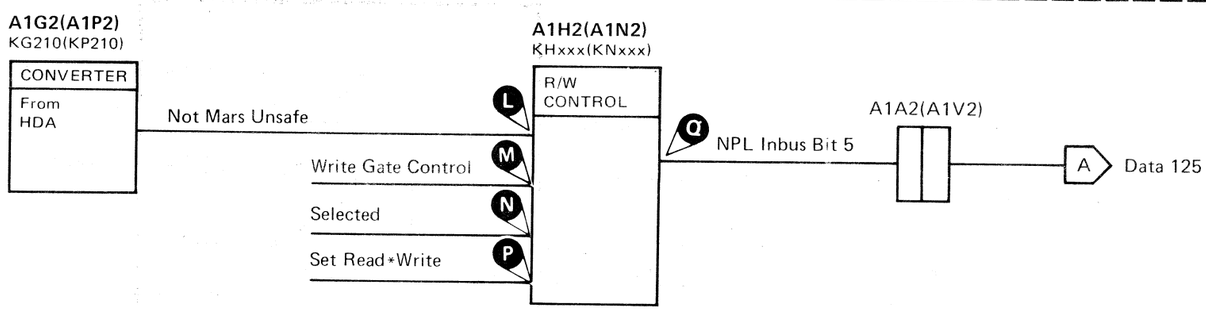


3340



Line Name	ALD	Test Point	
–Write Transitions A	KL090	A1H2 PO4	A
–Write Current Sense A	KL120	A1H2 PO5	B
–Write Transitions B	KL090	A1H2 MO4	C
–Write Current Sense B	KL120	A1H2 PO6	D
+Write Sense Status	KL020	A1H2 UO7	E
–Current Source Blkd A	EN155	R/W Matrix A B12	F
–Write Gate A	EN155	R/W Matrix A D11	G
–Current Source Blkd B	EN156	R/W Matrix B B12	H
–Write Gate B	EN156	R/W Matrix B D11	J
+NPL Inbus Bit 5	KK020	A1D2 PO9	K

3344



Line Name	ALD	Test Point	
Not –Mars Unsafe	KH210 (KN210)	A1H2(A1N2)M08	L
–Write Gate Control	KH110 (KN110)	A1H2(A1N2)G12	M
+Selected	KH100 (KN100)	A1H2(A1N2)MO5	N
+Set Read * Write	KH140 (KN140)	A1H2(A1N2)S13	P
+NPL Inbus Bit 5	KH200 (KN200)	A1H2(A1N2)DO2	Q

NO AM FOUND

NO AM FOUND

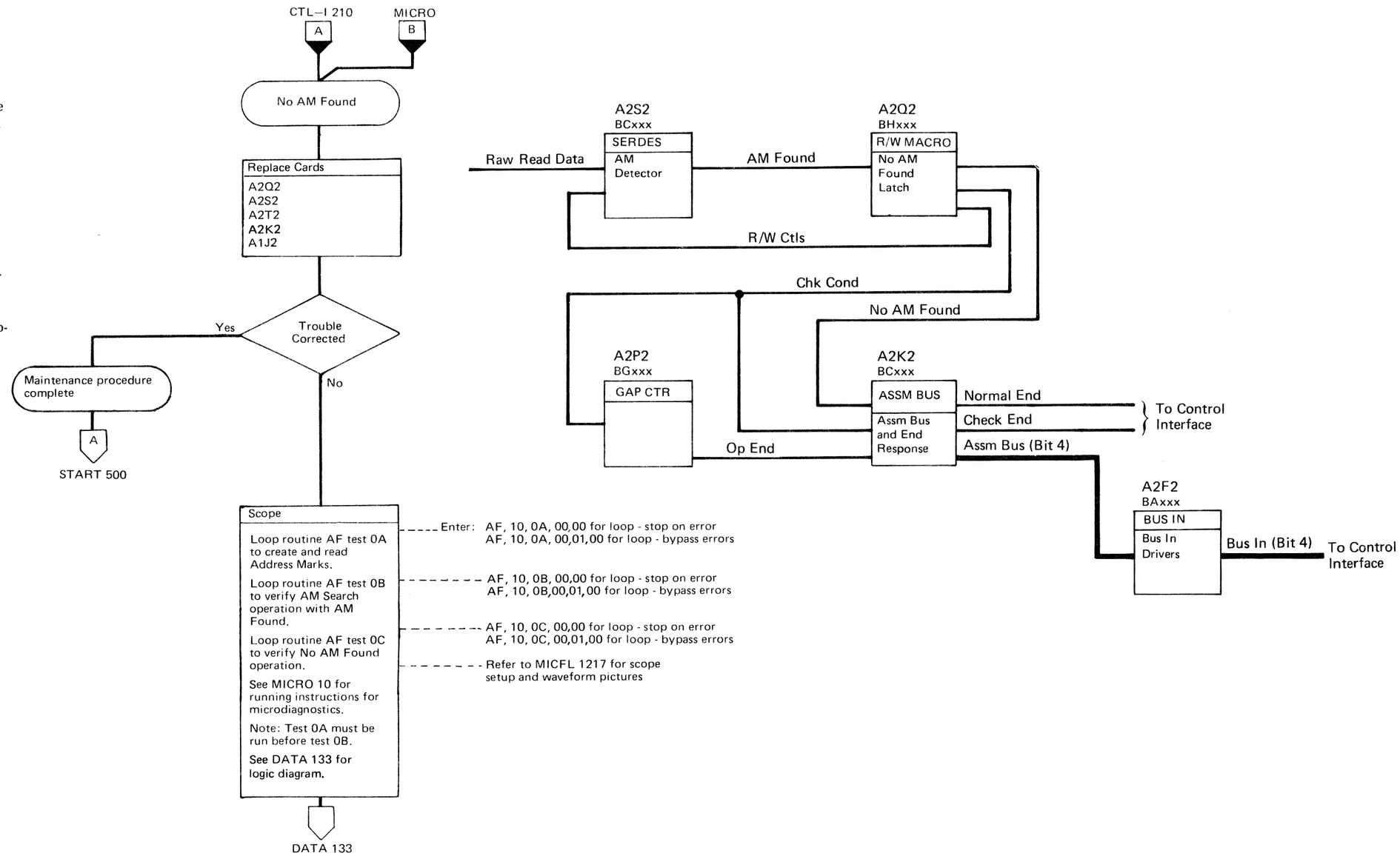
No AM Found is an indication that during an Address Mark Search operation, Index Mark was encountered before an Address Mark. This is not an error or check condition but normal operation, in most cases, since AM Search is used to establish orientation. When Index is encountered, it is used to establish orientation. Degraded throughput would be one reason to suspect AM Search problems, since the only orientation point would be Index. This causes additional rotational latency.

Routine AF tests Address Mark creation, AM Search, and No AM Found circuits.

No AM Found causes a Check End and is defined by Bus In bit 4. Bit 4 is also used as a redundant ECC Data Check bit. Following all Read operations, except RD G3 AM Search, bit 3 and/or bit 4 identifies an ECC Data Check. In this case, bit 4 on alone is an ECC Hardware Check and an Equipment Check is posted.

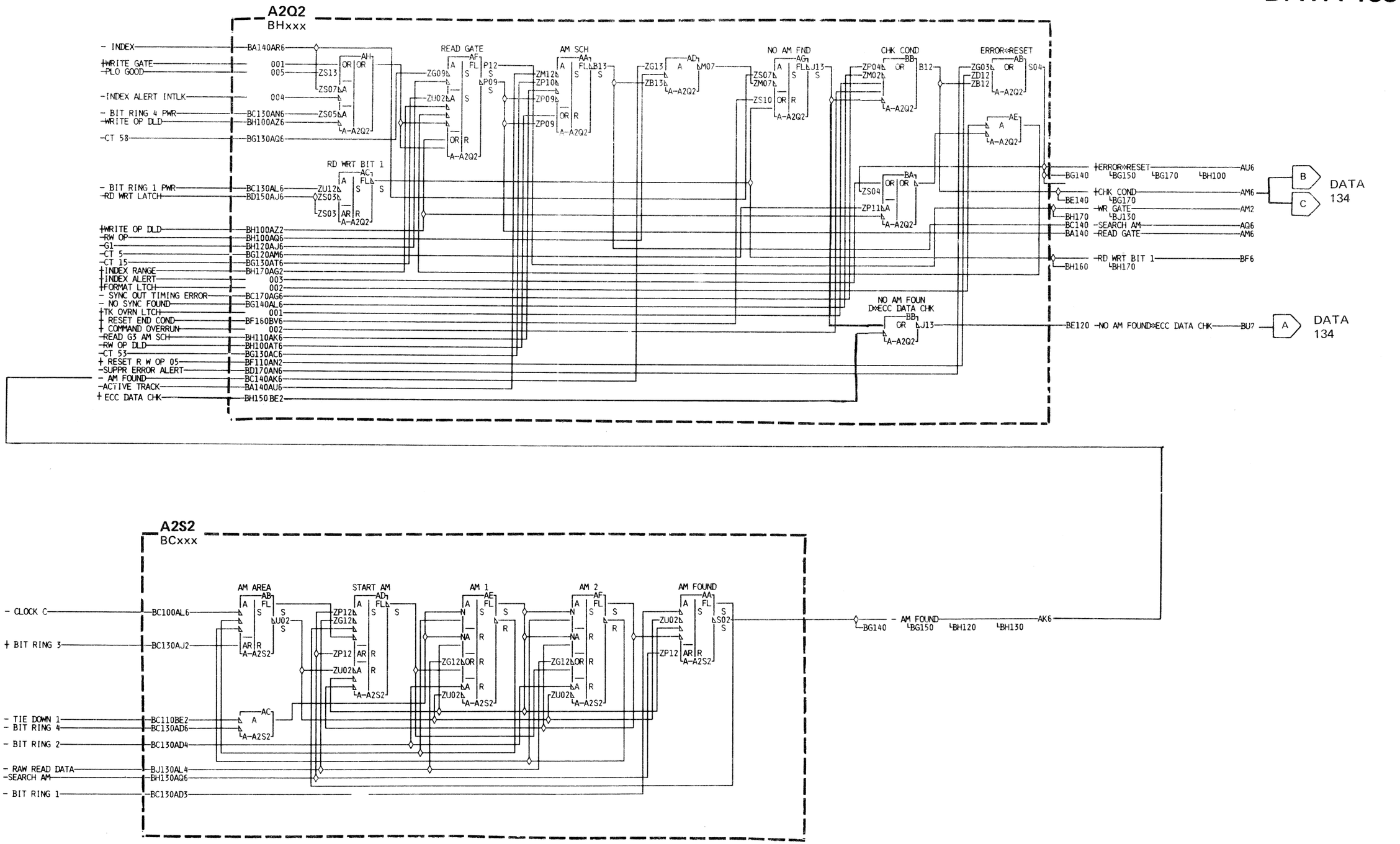
Following a Read G3 AM Search, further analysis is performed by the microprogram to determine the significance of bit 4. If no data has been transferred, bit 4 means No AM Found. If data has been transferred, bit 4 means an ECC Data Check. In the latter case bit 4 on without bit 3 is an ECC Hardware Check and an Equipment Check is posted.

See OPER 230 for description of Read operations.

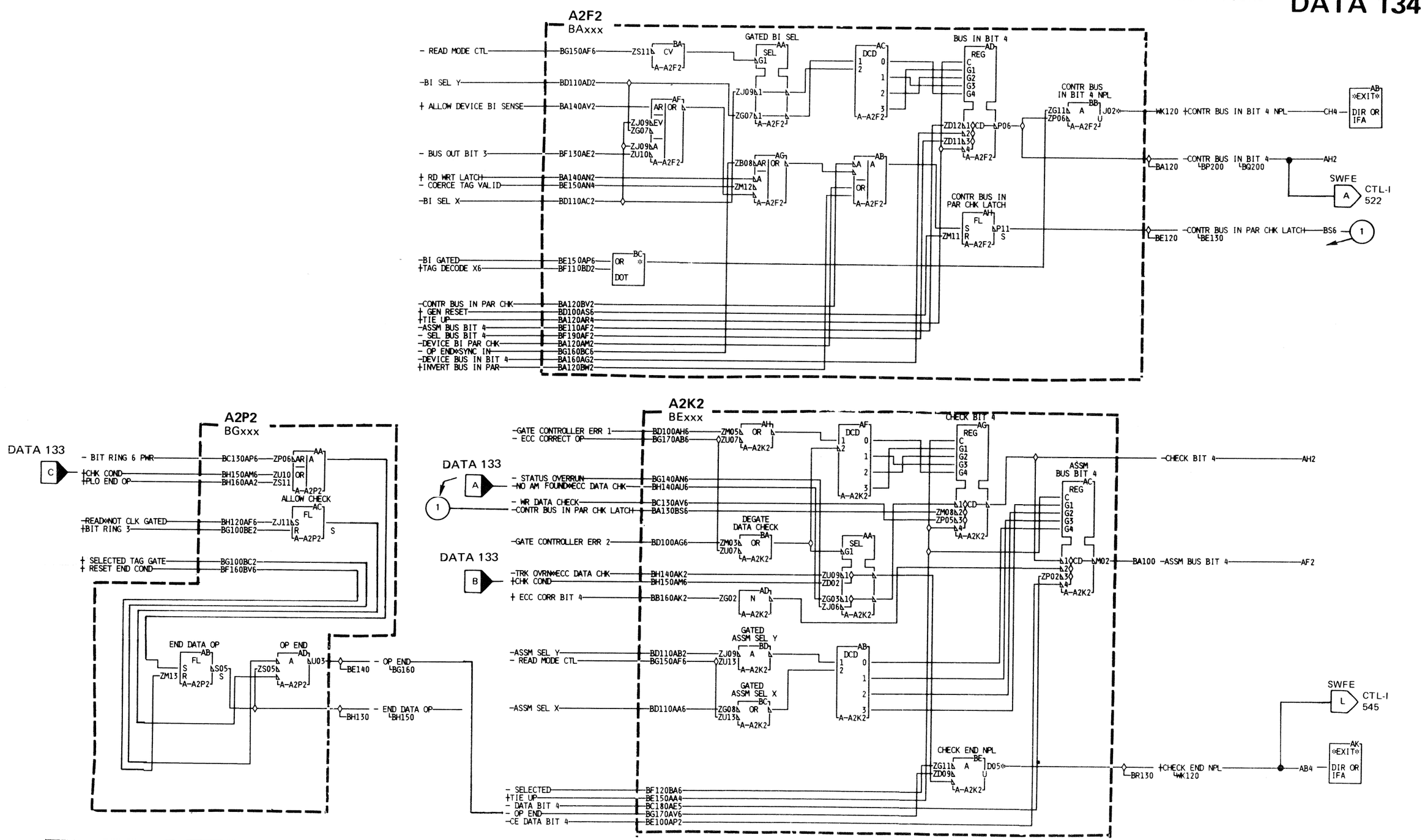


NO AM FOUND

DATA 133



BT0130	2747548	See EC History	440218	440224	440227			
Seq. 2 of 2	Part No.(1)		5 Aug 74	15 Dec 75	14 Sept 76			


A2F2
BAxxx
- READ MODE CTL
-BI SEL Y
+ ALLOW DEVICE BI SENSE
- BUS OUT BIT 3
+ RD WRT LATCH
- COERCE TAG VALID
-BI SEL X
-BI GATED
+TAG DECODE X6
-CONTR BUS IN PAR CHK
+ GEN RESET
+TIE UP
-ASSM BUS BIT 4
- SEL BUS BIT 4
-DEVICE BI PAR CHK
- OP END*SYNC IN
-DEVICE BUS IN BIT 4
+INVERT BUS IN PAR
GATED BI SEL
BUS IN BIT 4
CONTR BUS IN BIT 4 NPL
CONTR BUS IN PAR CHK LATCH
+CONTR BUS IN BIT 4 NPL
-CONTR BUS IN BIT 4
-CONTR BUS IN PAR CHK LATCH
SWFE
CTL-I 522
DATA 133
A2P2
BGxxx
- BIT RING 6 PWR
+CHK COND
+PLO END OP
-READ*NOT CLK GATED
+BIT RING 3
+ SELECTED TAG GATE
+ RESET END COND
ALLOW CHECK
END DATA OP
OP END
- OP END
- END DATA OP
A2K2
BExxx
-GATE CONTROLLER ERR 1
- ECC CORRECT OP
- STATUS OVERRUN
-NO AM FOUND*ECC DATA CHK
- WR DATA CHECK
-CONTR BUS IN PAR CHK LATCH
-GATE CONTROLLER ERR 2
-TRK OVRN*ECC DATA CHK
+CHK COND
+ ECC CORR BIT 4
-ASSM SEL Y
- READ MODE CTL
-ASSM SEL X
- SELECTED
+TIE UP
- DATA BIT 4
- OP END
-CE DATA BIT 4
CHECK BIT 4
ASSM BUS BIT 4
DEGATE DATA CHECK
GATED ASSM SEL Y
GATED ASSM SEL X
CHECK END NPL
-CHECK BIT 4
-ASSM BUS BIT 4
+CHECK END NPL
SWFE
CTL-I 545

NO SYNC BYTE FOUND

The sync byte ('19'), identifies the start of every field written on the disk. No Sync Found is an indication that a sync byte was not found at the proper place on the disk. This would be a normal condition if the field did not exist. It is an error if the field exists but the Sync Byte cannot be determined.

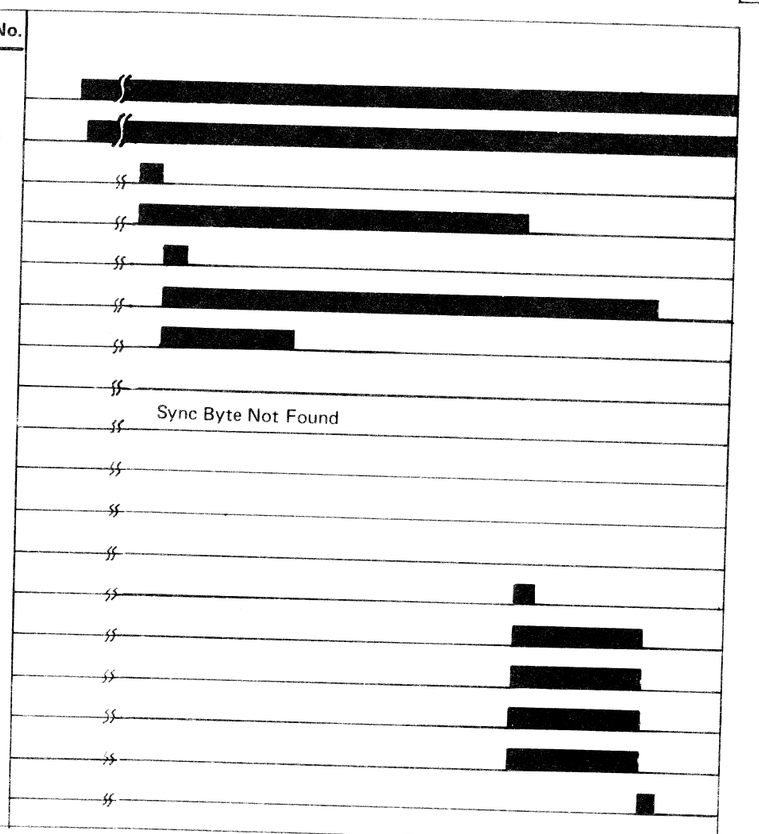
The No Sync Found latch causes a Check Condition which sets the End Data Op latch. End Data Op combined with Check Condition causes a Check End to be sent to storage control.

See OPER 43 for Sync Byte Found descriptions.

Bus In bit 5 on during Check End indicates no sync byte is found. The No Sync Found latch and the End Data Op latch are reset by the End Response signal from storage control. The Data Present latch monitors the data area near the sync byte. If data is found but a sync byte cannot be decoded, the Data Present latch is set and indicated by Bus In bit 6 during Check End. Storage control analyzes No Sync Found and Data Present to determine the status of the field involved. A No Sync Found in a data field causes a Data Check (Format 4, Message 7) regardless of the condition of the Data Present latch. A No Sync Found in the key field causes a Data Check (Format 4, Message 6) regardless of the condition of the Data Present latch.

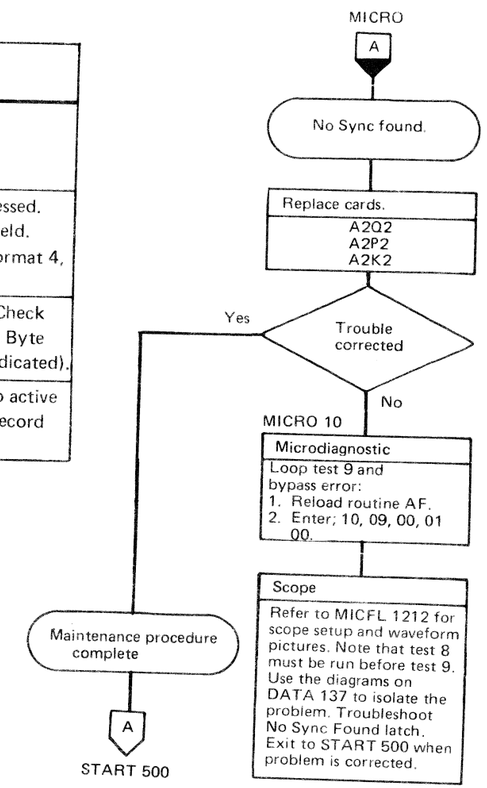
Read Operation With No Sync Found

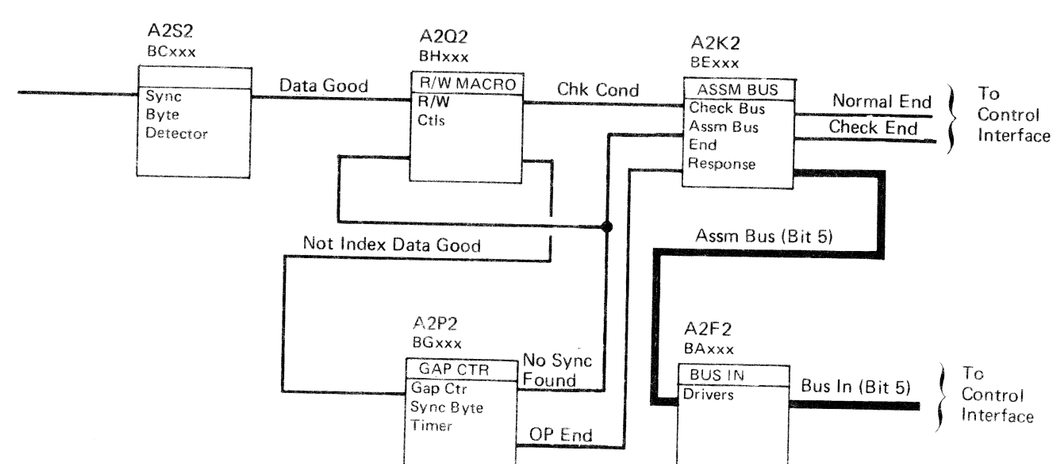
Line Name	ALD	Pin or Net No.
−Read	BH100	AP6
−Read * Not Clock Gated	BH120	A1Q2D06
−Reset Gap Counter	GH140	AG2
−Pre-R/W Mode	BG140	AP6
+VFO to Data	BG140	A2P2J13
−Locked to Data	BC140	AC6
+VFO Fast Sync Latch	BC140	AP2
+Special VFO Reset	BC130	A2S2M11
+Data Good	BC110	A2S2G02
−Read Mode Control	BG150	A2P2S04
−Sync In	BC170	A2S2U10
+Run Modulo	BG100	AR6
−CT 21	BG130	AF6
−No Sync Found	BG140	A2P2M12
+Chk Cond	BH150	A2Q2B12
−End Data Op	BG170	A2P2S05
−Check End	BE140	AE6
+End Response NPL	BF160	A2G2S03

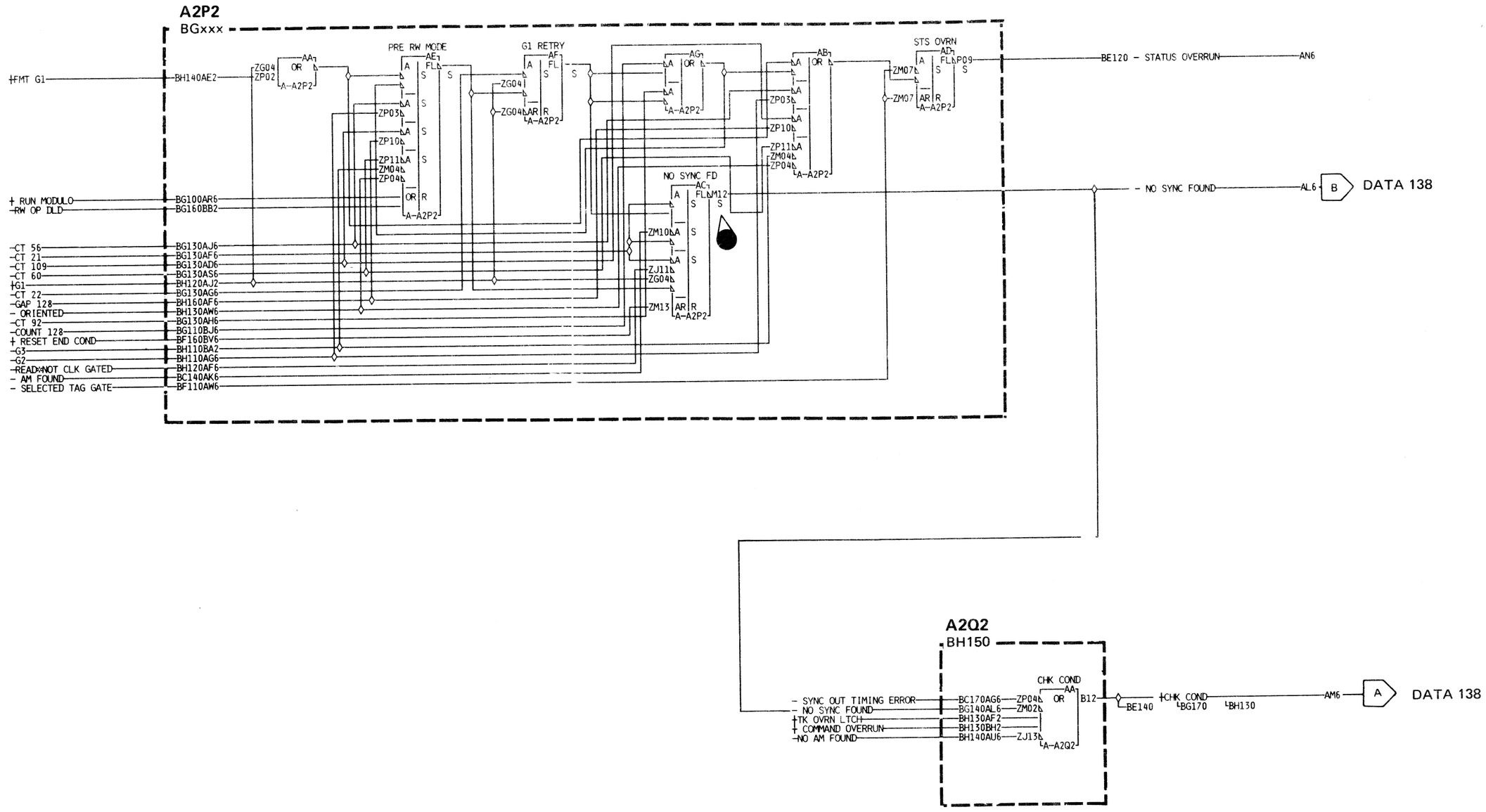


Examples:

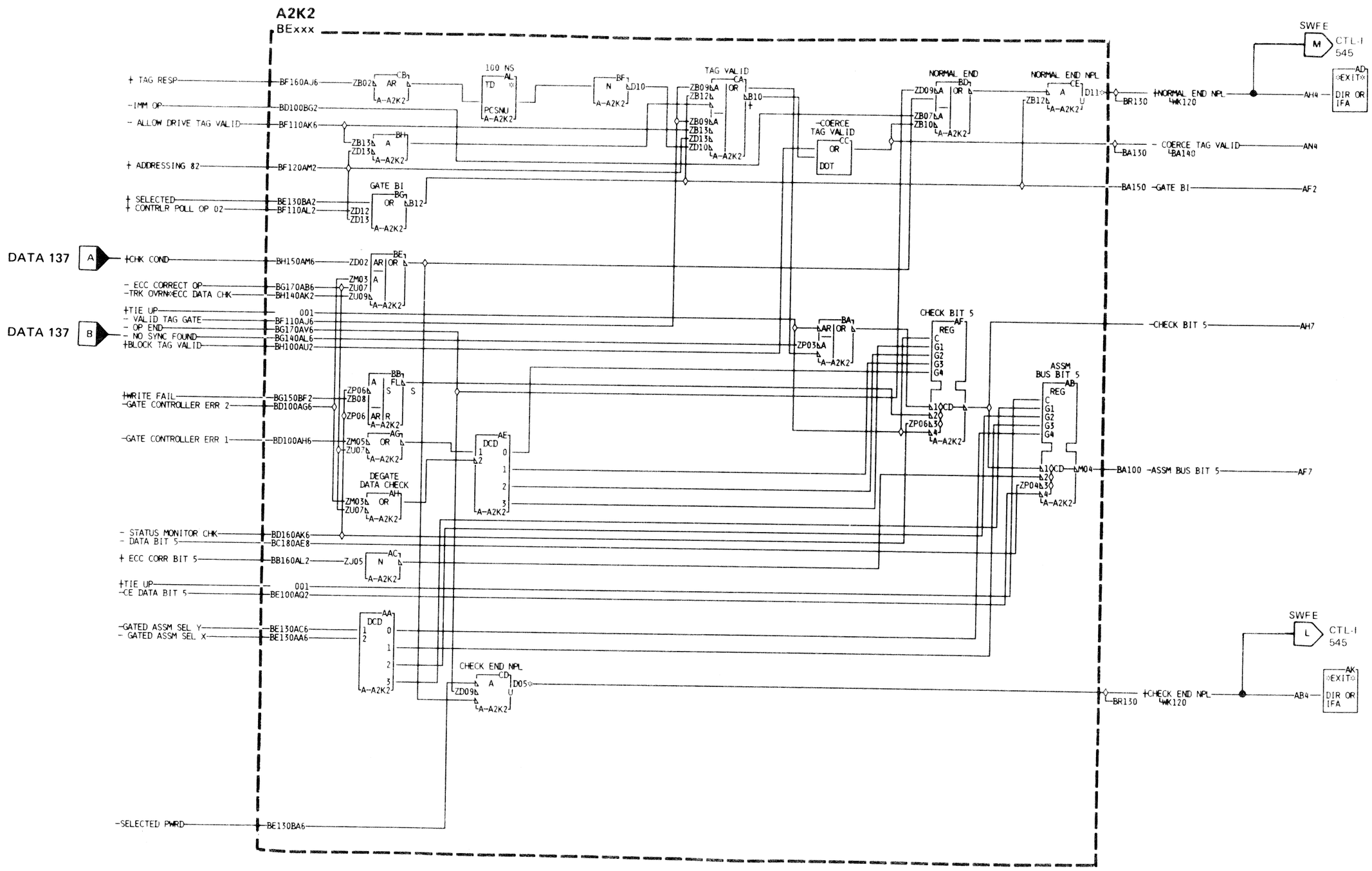
Records on Track	Operation	No Sync Found	Data Present	Results
5	SCHIDEQ R5 TIC RD CKD	OFF ON	OFF OFF	Record does not exist. R0 is read.
6	SCHIDEQ R5 TIC RD CKD	OFF ON	OFF ON	Record 6 cannot be processed. Data Check with Count field. No Sync Byte Found (Format 4, Message 5 is indicated).
6	SCHIDEQ R6 TIC etc.	ON –	ON –	Search terminated. Data Check with Count Field No Sync Byte (Format 4, Message 5 is indicated).
5	SCHIDEQ R6 TIC etc.	ON –	OFF –	Search continues until two active Track Indexes and a No Record Found is posted.







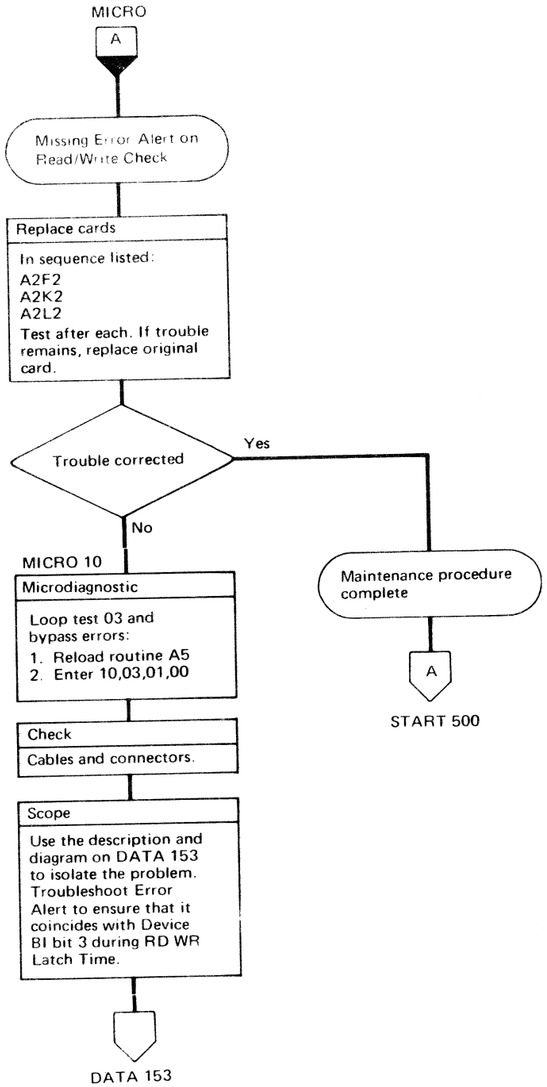
BT0140	2747601	440202	440203	440204	440209	440218		
Seq 2 of 2	Part Number	7 Sept 73	2 Nov 73	21 Dec 73	25 Mar 74	5 Aug 74		

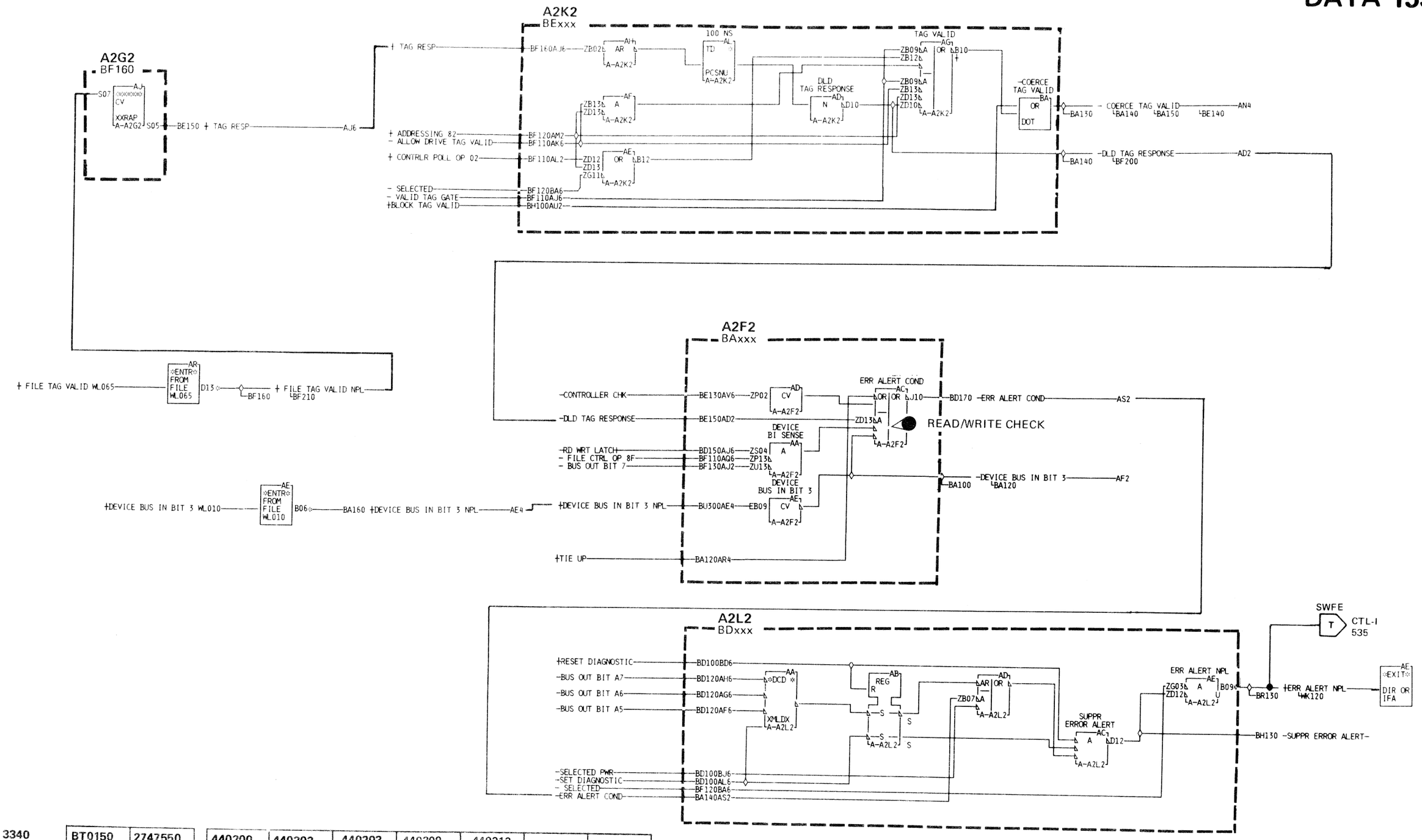


BT0143	2747549	440200	440202	440203	440213	440224		
Seq. 1 of 2	Part No.( )	25 Jun 73	7 Sept 72	2 Nov 73	13 May 74	15 Dec 75		

READ/WRITE CHECK

See OPER 260 for Drive Errors that cause Error Alert.

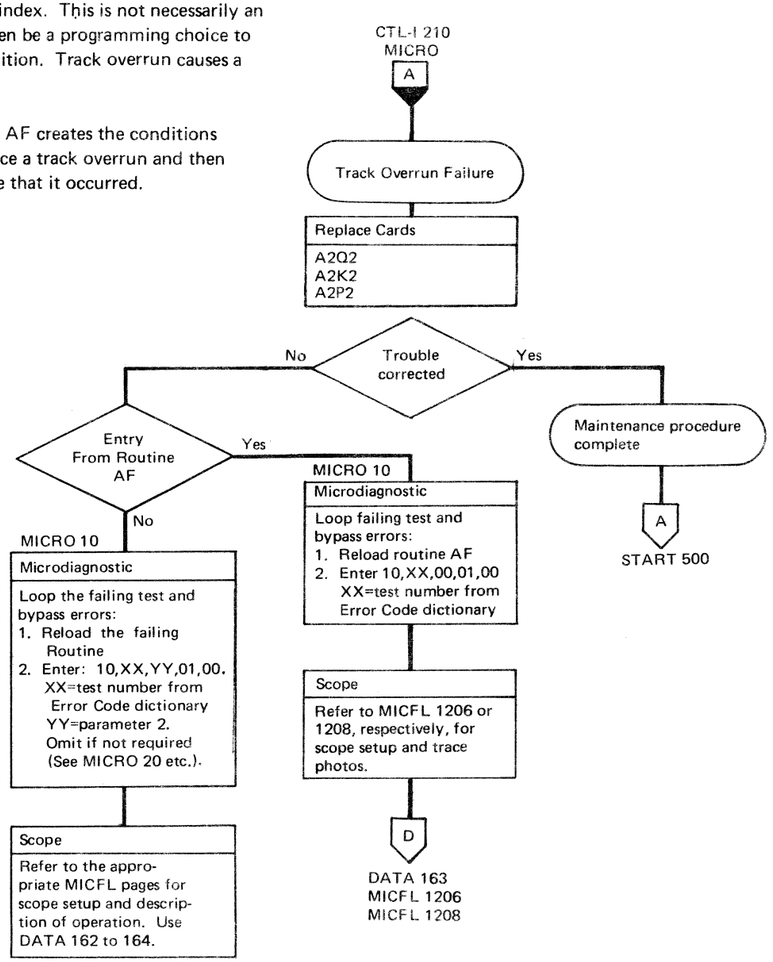


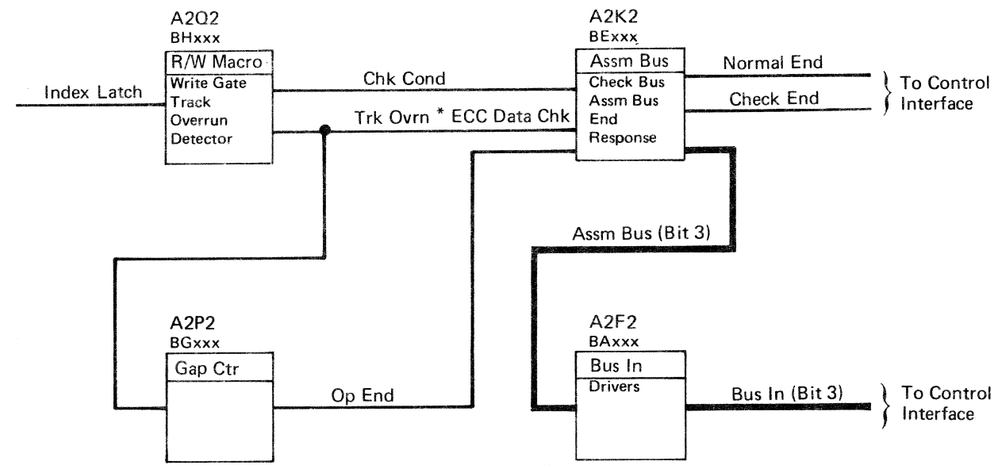


TRACK OVERRUN FAILURE

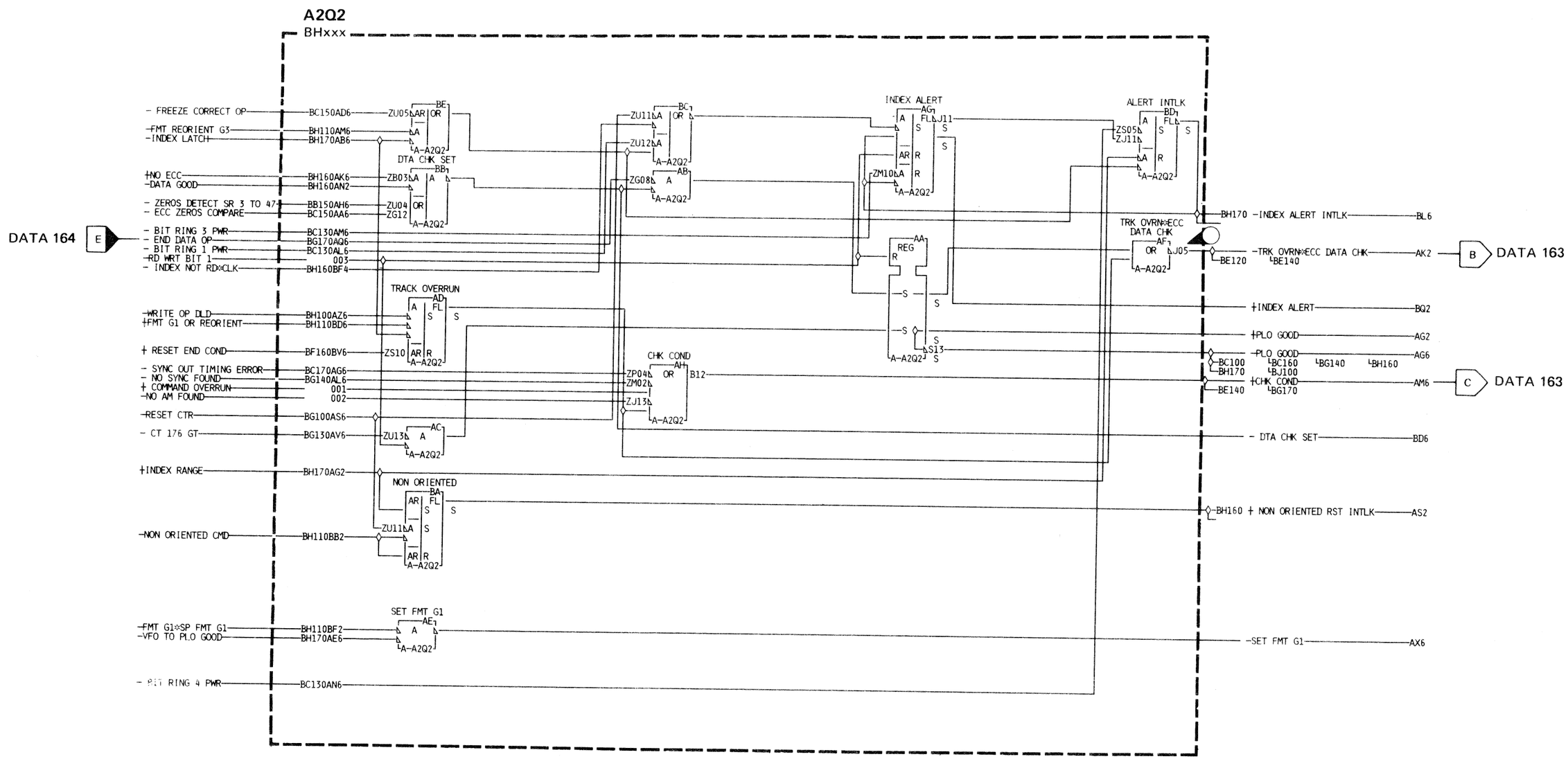
Track overrun is an indication of an attempt to write data past index. This is not necessarily an error; it may even be a programming choice to create this condition. Track overrun causes a check end.

Microdiagnostic AF creates the conditions necessary to force a track overrun and then checks to ensure that it occurred.

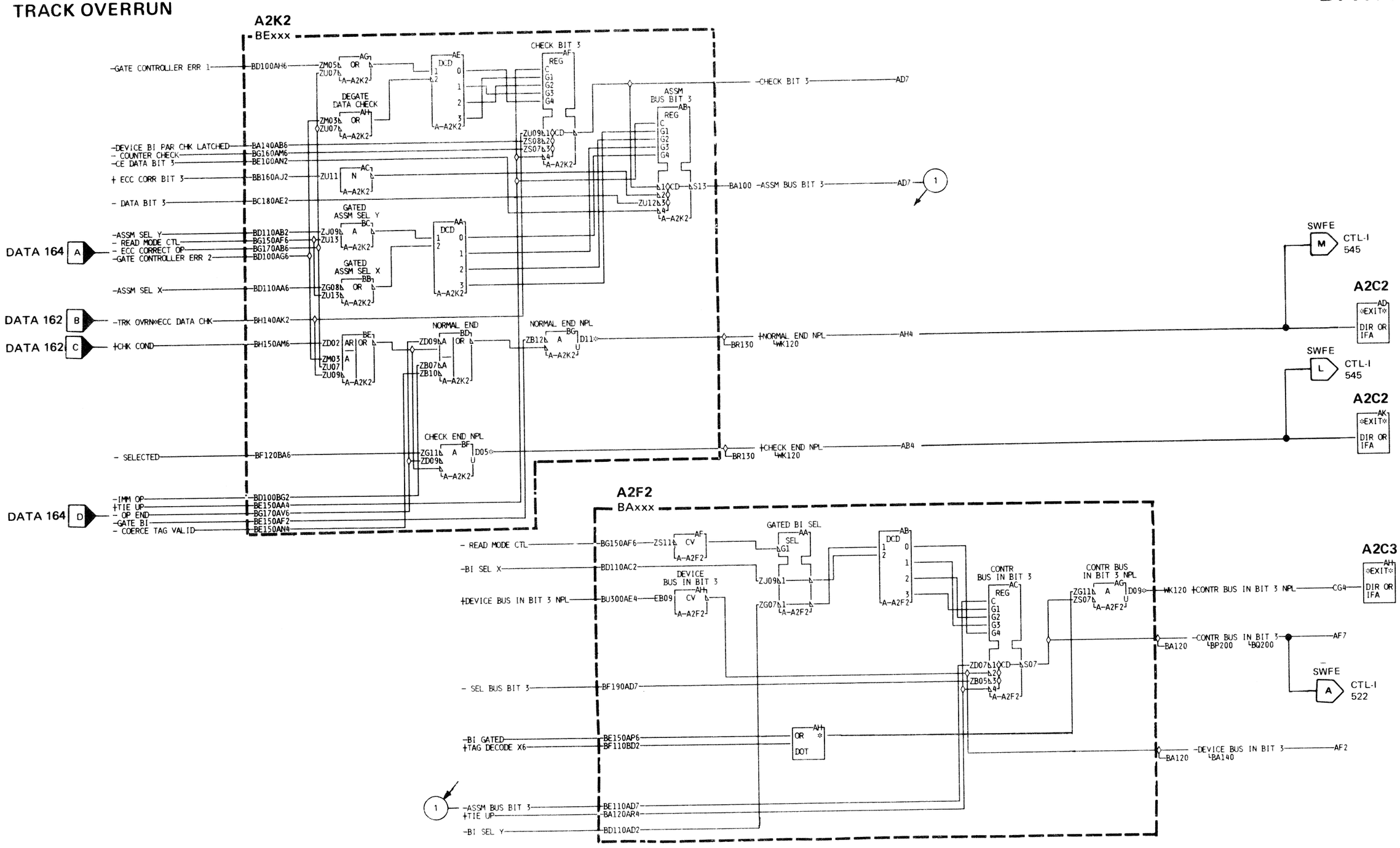


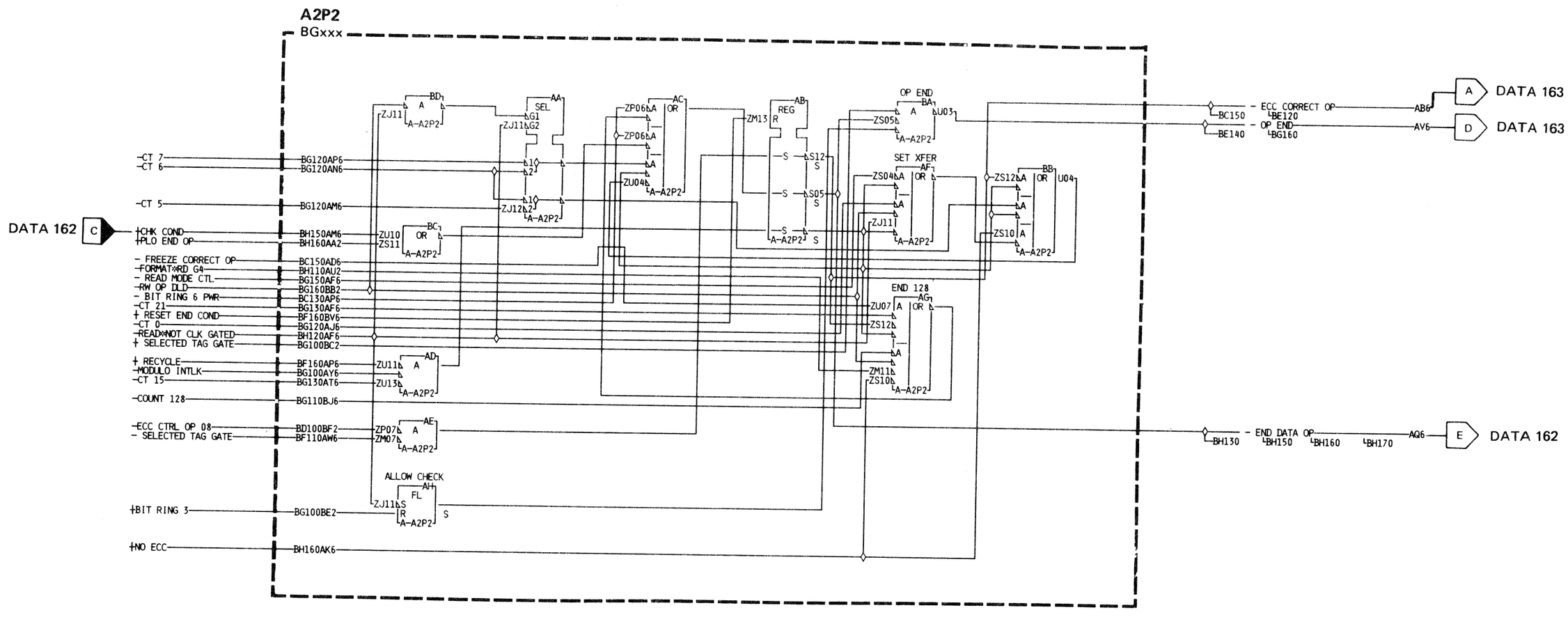


BT0150	2747550	440200	440202	440203	440209	440213	
Seq. 2 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	13 May 74	


A2Q2
BHxxx
DATA 164
E
- FREEZE CORRECT OP
-FMT REORIENT G3
-INDEX LATCH
+NO ECC
-DATA GOOD
- ZEROS DETECT SR 3 TO 47
- ECC ZEROS COMPARE
- BIT RING 3 PWR
- END DATA OP
- BIT RING 1 PWR
-RD WRT BIT 1
- INDEX NOT RD*CLK
-WRITE OP DLD
+FMT G1 OR REORIENT
+ RESET END COND
- SYNC OUT TIMING ERROR
- NO SYNC FOUND
+ COMMAND OVERRUN
-NO AM FOUND
-RESET CTR
- CT 176 GT
+INDEX RANGE
-NON ORIENTED CMD
-FMT G1*SP FMT G1
-VFO TO PLO GOOD
- BIT RING 4 PWR
BC150AD6
BH110AM6
BH170AB6
BH160AK6
BH160AN2
BB150AH6
BC150AA6
BC130AM6
BG170AQ6
BC130AL6
003
BH160BF4
BH100AZ6
BH110BD6
BF160BV6
BC170AG6
BG140AL6
001
002
BG100AS6
BG130AV6
BH170AG2
BH110BB2
BH110BF2
BH170AE6
BC130AN6
ZU05
DTA CHK SET
ZB03
ZU04
ZG12
TRACK OVERRUN
ZS10
ZU11
ZU12
ZG08
CHK COND
ZP04
ZM02
ZJ13
B12
NON ORIENTED
SET FMT G1
INDEX ALERT
ZM10
REG
S13
ALERT INTLK
ZS05
ZJ11
TRK OVRN*ECC DATA CHK
J05
BH170 -INDEX ALERT INTLK
BL6
-TRK OVRN*ECC DATA CHK
BE120
BE140
AK2
B
DATA 163
+INDEX ALERT
BQ2
+PLO GOOD
AG2
-PLO GOOD
AG6
BC100
BC160
BG140
BH160
BH170
BJ100
+CHK COND
BG170
AM6
C
DATA 163
- DTA CHK SET
BD6
-BH160 + NON ORIENTED RST INTLK
AS2
-SET FMT G1
AX6

TRACK OVERRUN



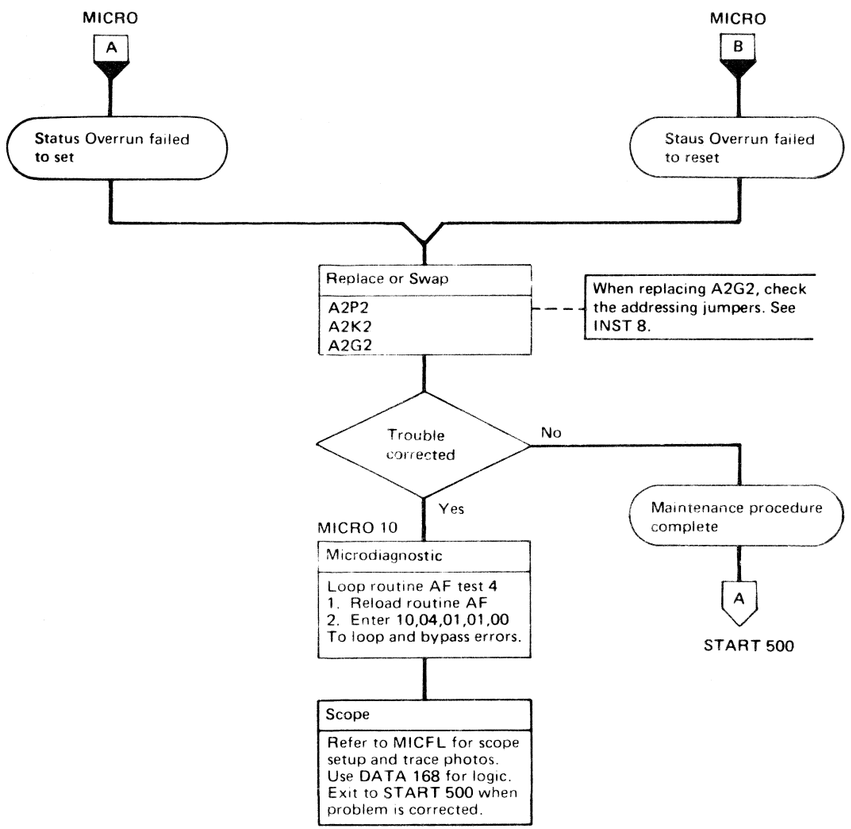

A2P2
BGxxx
DATA 162
C
-CT 7
-CT 6
-CT 5
+CHK COND
+PLO END OP
- FREEZE CORRECT OP
-FORMAT*RD G4
- READ MODE CTL
-RW OP DLD
- BIT RING 6 PWR
-CT 21
+ RESET END COND
-CT 0
-READ*NOT CLK GATED
+ SELECTED TAG GATE
+ RECYCLE
-MODULO INTLK
-CT 15
-COUNT 128
-ECC CTRL OP 08
- SELECTED TAG GATE
+BIT RING 3
+NO ECC
BG120AP6
BG120AN6
BG120AM6
BH150AM6
BH160AA2
BC150AD6
BH110AU2
BG150AF6
BG160BB2
BC130AP6
BG130AF6
BF160BV6
BG120AJ6
BH120AF6
BG100BC2
BF160AP6
BG100AY6
BG130AT6
BG110BJ6
BD100BF2
BF110AW6
BG100BE2
BH160AK6
ZJ11
A-A2P2
BD
A
SEL
AA
G1
G2
ZJ12
ZP06
AC
OR
ZU04
ZM13
AB
REG
R
S12
S05
ZU10
ZS11
BC
ZU11
ZU13
AD
ZP07
ZM07
AE
ALLOW CHECK
AH
FL
OP END
BA
U03
ZS05
SET XFER
AF
ZS04
ZS12
BB
U04
ZS10
END 128
AG
ZU07
ZM11
ZS10
BC150
BE140
- ECC CORRECT OP
BE120
- OP END
BG160
ABG
AV6
A
D
DATA 163
DATA 163
BH130
BH150
BH160
BH170
- END DATA OP
AQ6
E
DATA 162

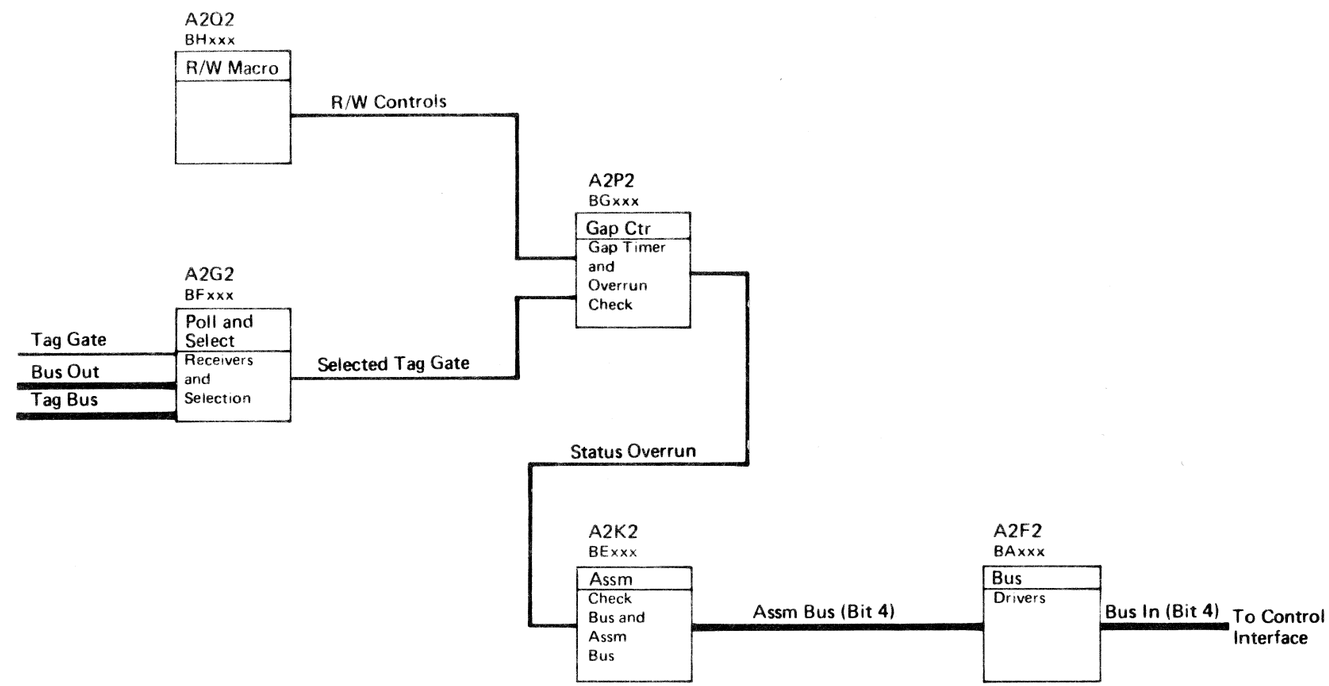
STATUS OVERRUN

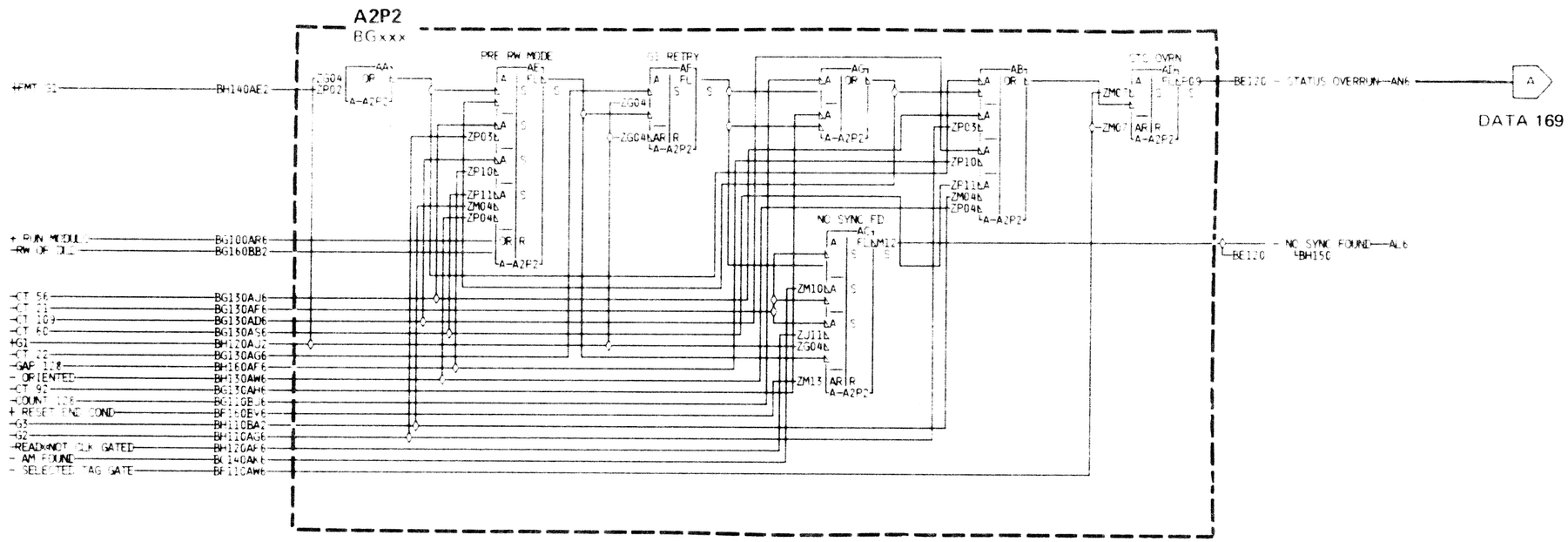
During selection or chained reselection, the storage control interlocks the channel sequence with the control interface sequence. After receiving Command Out, the storage control decodes the command and:

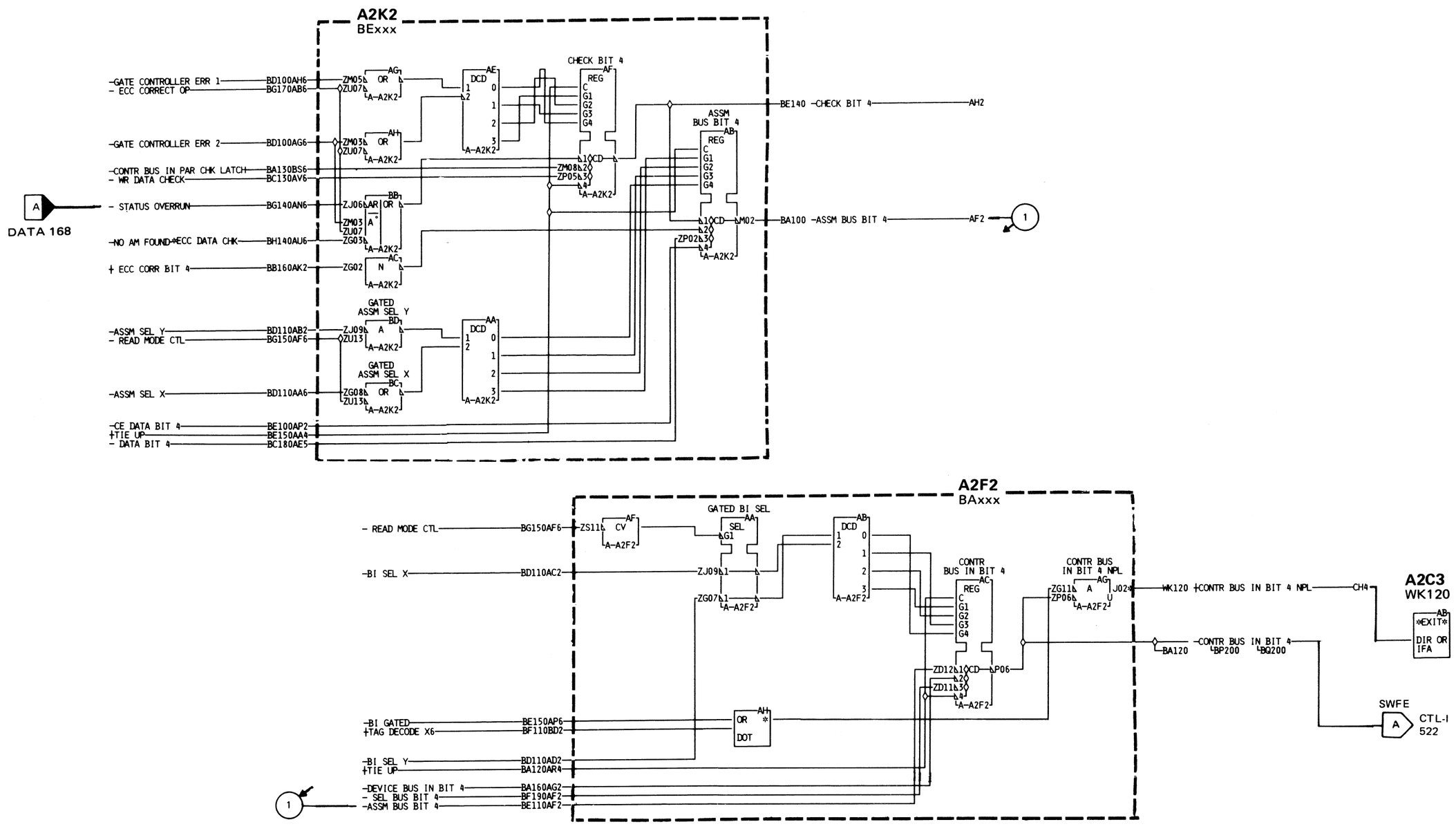
1. Sends an operation code to the controller over the control interface.
2. Sends Status In to the channel.
3. Holds Tag Gate active on the control interface until the channel responds with service out.

If a chained reselection is in process and the disk is oriented, Tag Gate must drop before a specified time to avoid an overrun condition. If it does not drop in time, the Status Overrun latch is set to indicate that the channel did not respond to Status In in time.





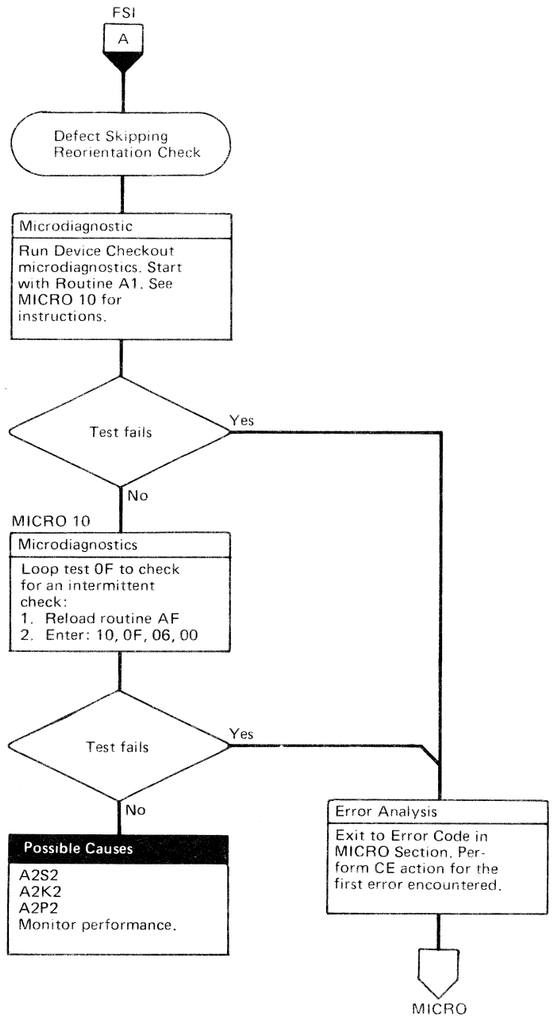


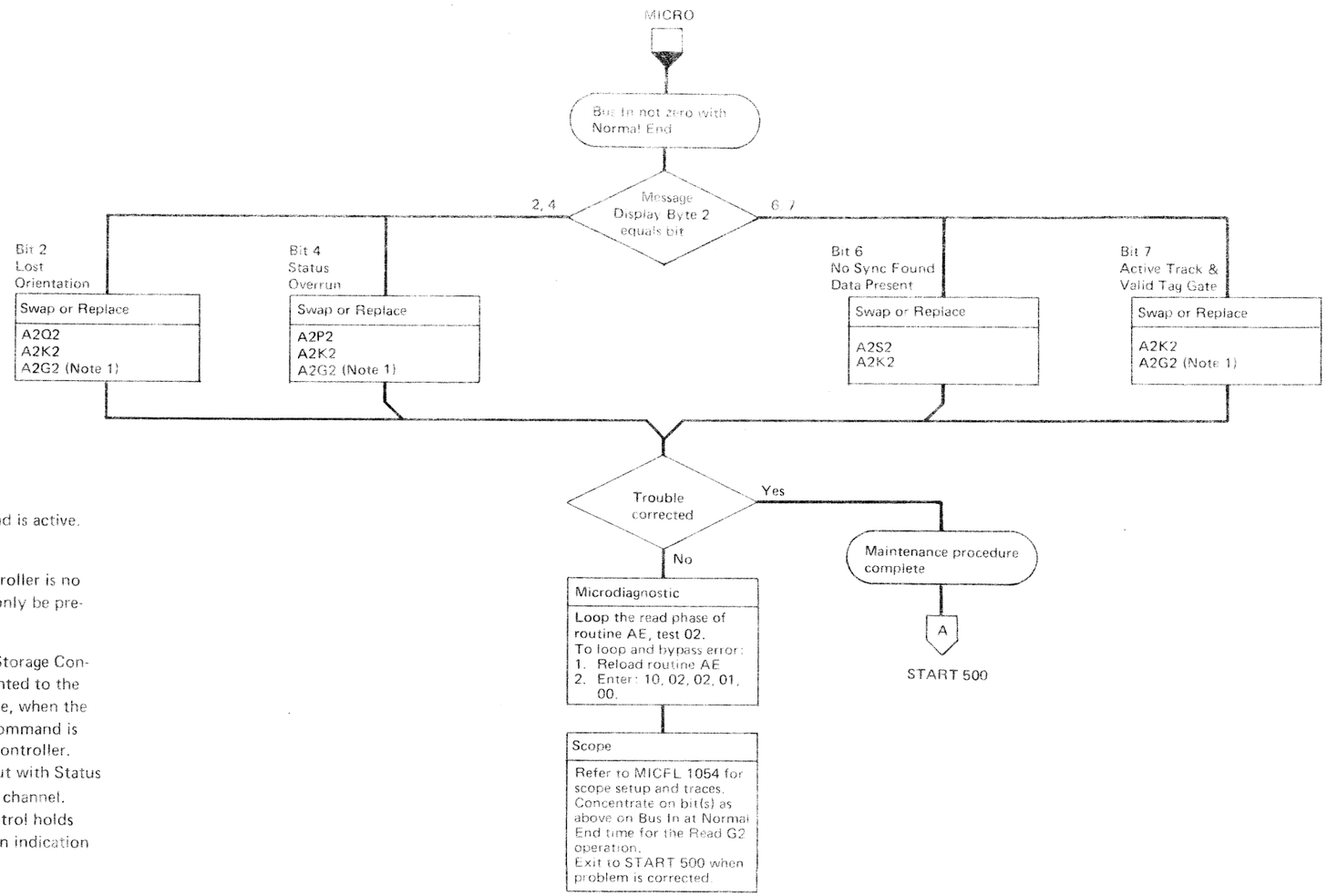

A2K2
BExxx
-GATE CONTROLLER ERR 1
- ECC CORRECT OP
-GATE CONTROLLER ERR 2
-CONTR BUS IN PAR CHK LATCH
- WR DATA CHECK
- STATUS OVERRUN
-NO AM FOUND*ECC DATA CHK
+ ECC CORR BIT 4
-ASSM SEL Y
- READ MODE CTL
-ASSM SEL X
-CE DATA BIT 4
+TIE UP
- DATA BIT 4
BD100AH6
BG170AB6
BD100AG6
BA130BS6
BC130AV6
BG140AN6
BH140AU6
BB160AK2
BD110AB2
BG150AF6
BD110AA6
BE100AP2
BE150AA4
BC180AE5
DATA 168
CHECK BIT 4
ASSM BUS BIT 4
BE140 -CHECK BIT 4
AH2
BA100 -ASSM BUS BIT 4
AF2
GATED ASSM SEL Y
GATED ASSM SEL X
A2F2
BAxxx
- READ MODE CTL
-BI SEL X
-BI GATED
+TAG DECODE X6
-BI SEL Y
+TIE UP
-DEVICE BUS IN BIT 4
- SEL BUS BIT 4
-ASSM BUS BIT 4
BG150AF6
BD110AC2
BE150AP6
BF110BD2
BD110AD2
BA120AR4
BA160AG2
BF190AF2
BE110AF2
GATED BI SEL
CONTR BUS IN BIT 4
CONTR BUS IN BIT 4 NPL
WK120 +CONTR BUS IN BIT 4 NPL
CH4
A2C3
WK120
EXIT
DIR OR IFA
-CONTR BUS IN BIT 4
BA120
SWFE
CTL-I
522

DEFECT SKIPPING REORIENTATION CHECK

This message is generated by the storage control if Check End is received from the controller during a Reorient operation. The Sync Out timing error is the most likely cause of this failure due to the large number of bytes that must be counted to reorient.

The Format Reorient operation is described on OPER 103.





Bus In should always be zero when Normal End is active. Routine AE test 02 tests for zero.

Lost Orientation is an indication that the controller is no longer synchronized with the disk. It should only be presented at Tag Valid time.

Status Overrun is normally used to signal the Storage Control that a Command Overrun should be presented to the channel. During a chained reselection sequence, when the Storage Control receives Command Out, the command is decoded and an operation code is sent to the controller. The Storage Control responds to Command Out with Status In and expects to receive Service Out from the channel. While waiting for Service Out, the Storage Control holds up Tag Gate. If Tag Gate is up too long, it is an indication that the channel is late with Service Out.

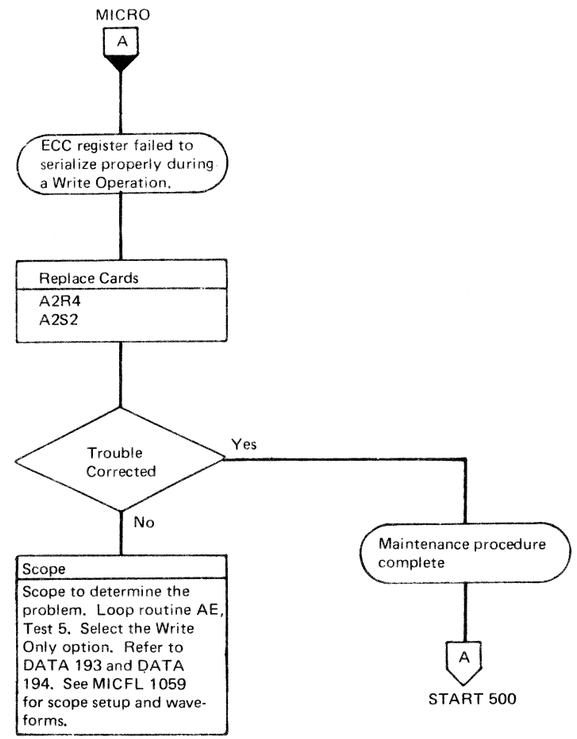
No Sync Found and Data Present is used by the microprogram to determine the reason for the No Sync Byte Found indication.

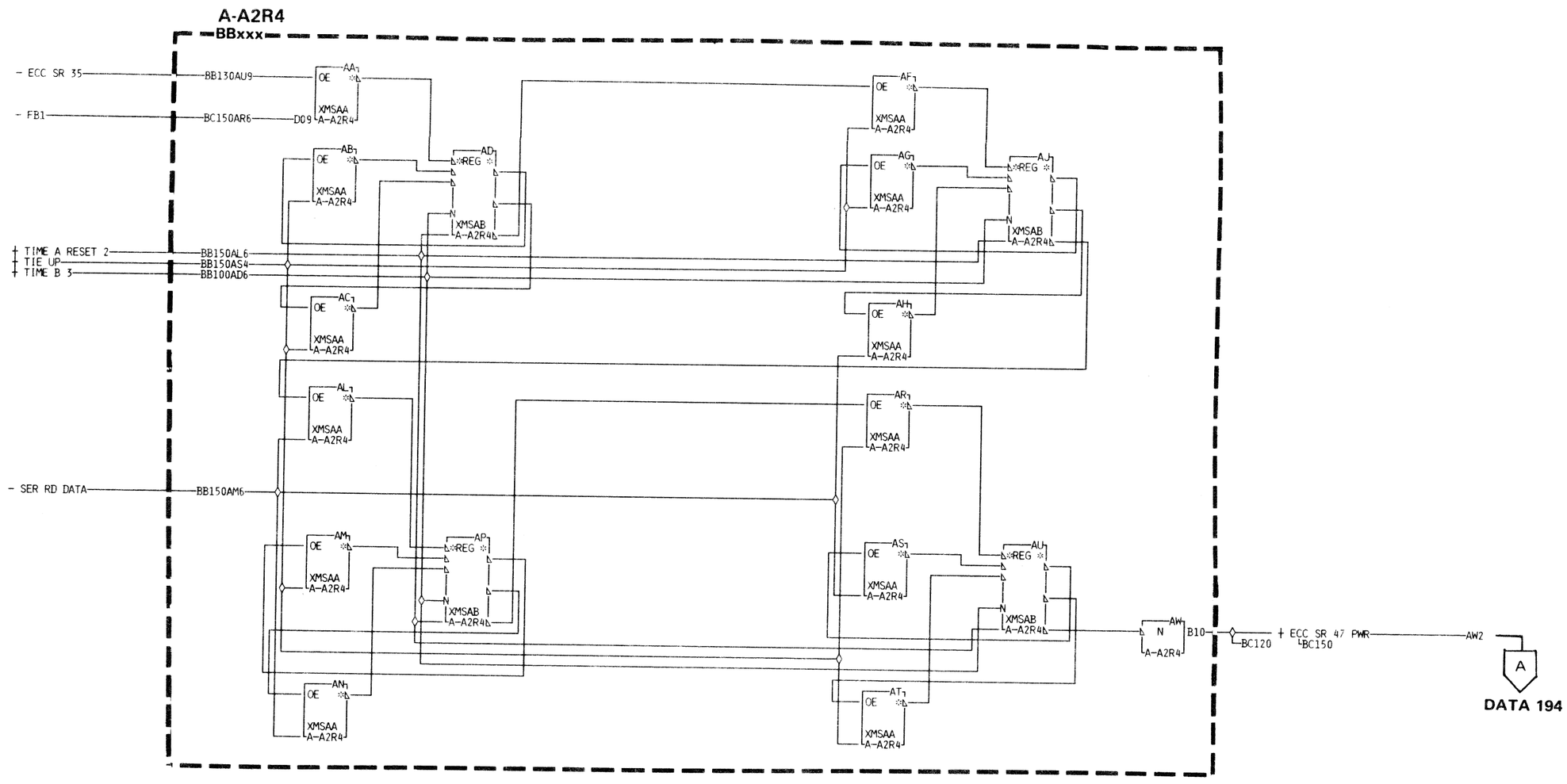
Active Track and Valid Tag Gate indicates Active Track at Tag Gate time.

Note 1: When replacing A2G2, check addressing jumpers. See INST 8.

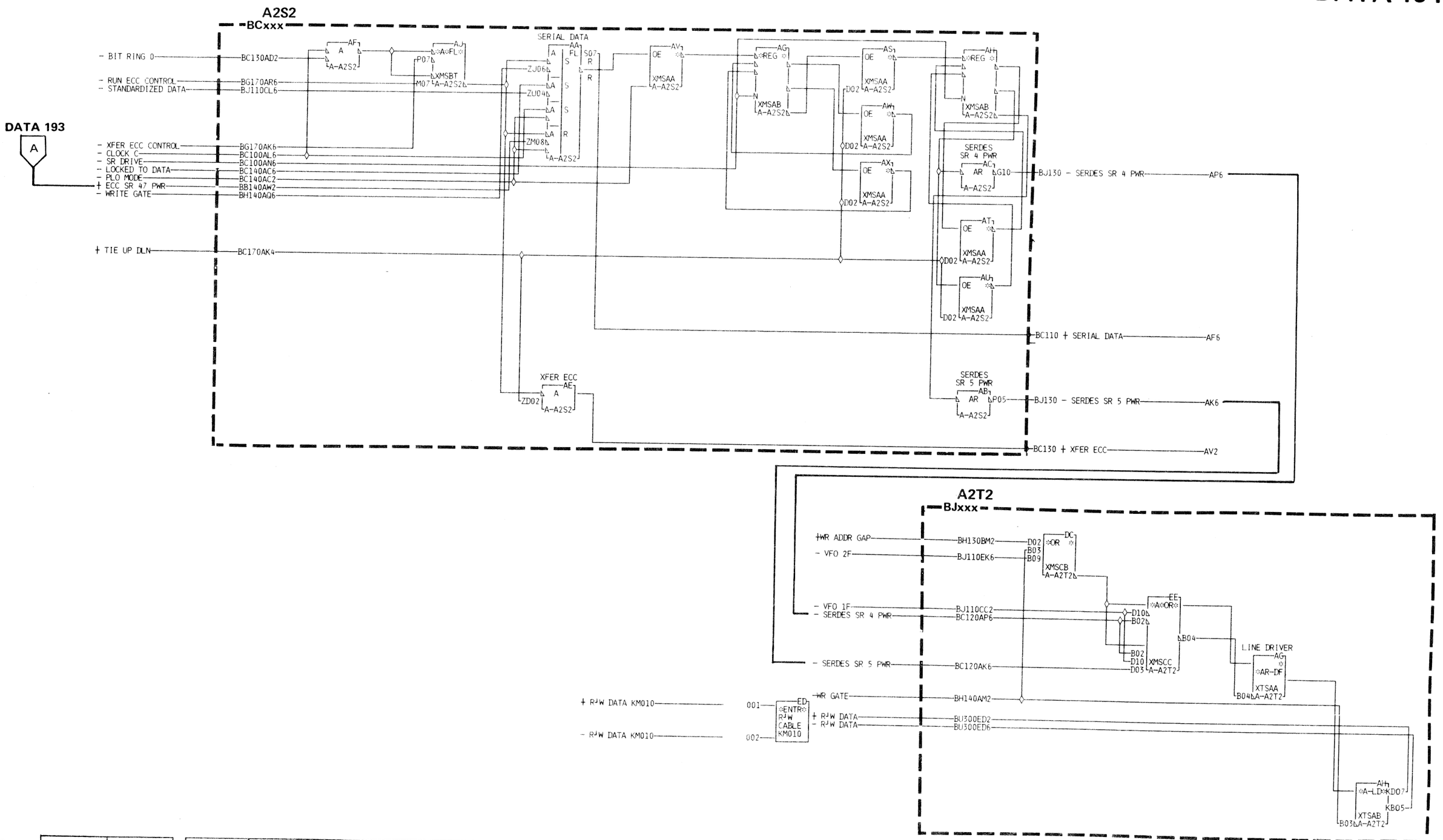
ECC REGISTER FAILURE

This test writes a two byte record of zeros. The ECC bytes which follow equal six bytes of 'FF'.
The record is then read back as an 8-byte record and the Data Check is ignored. The data read is compared with the expected value. A noncompare indicates a failure to write the ECC bytes properly.





ECC REGISTER FAILURE

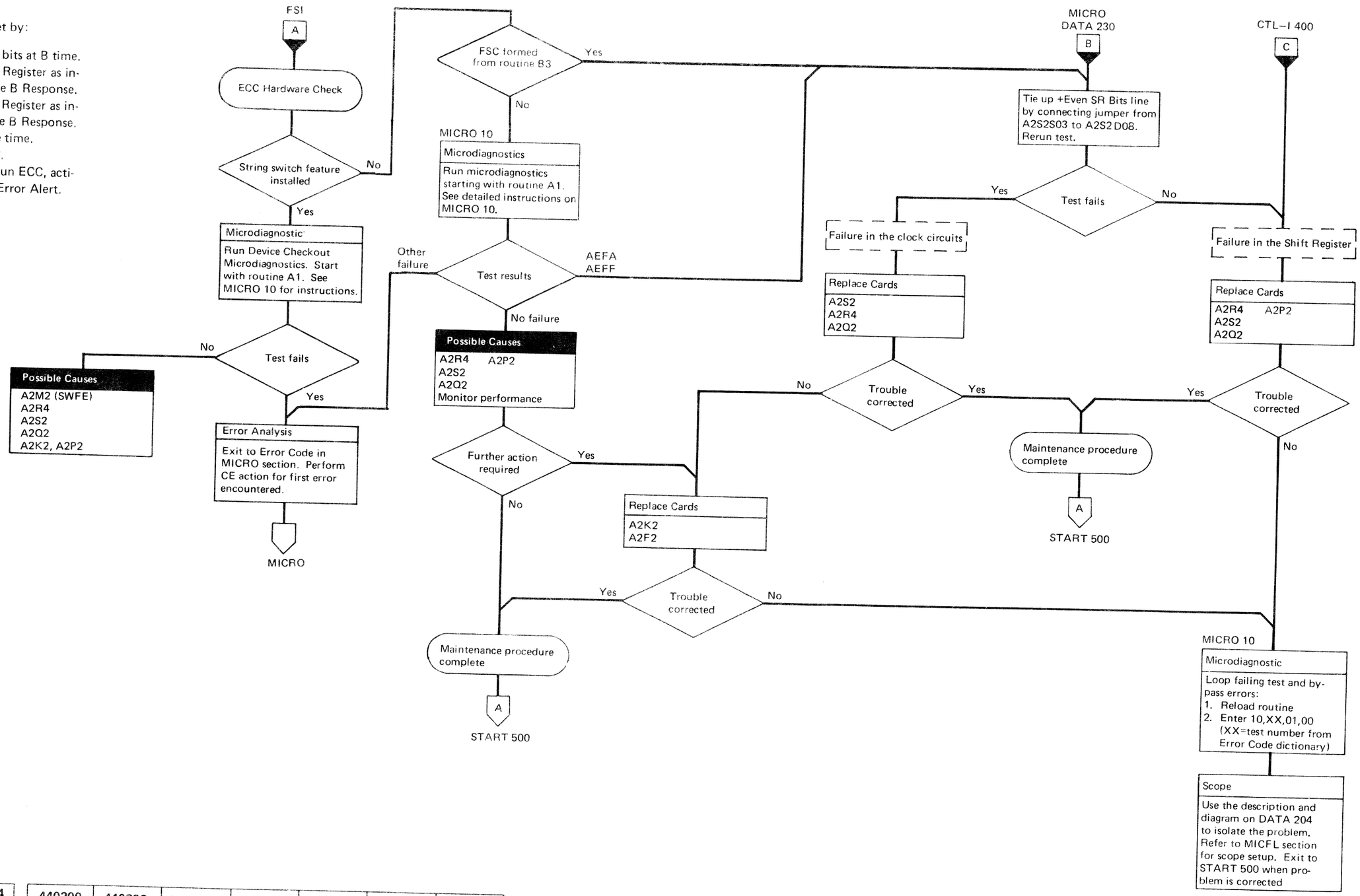


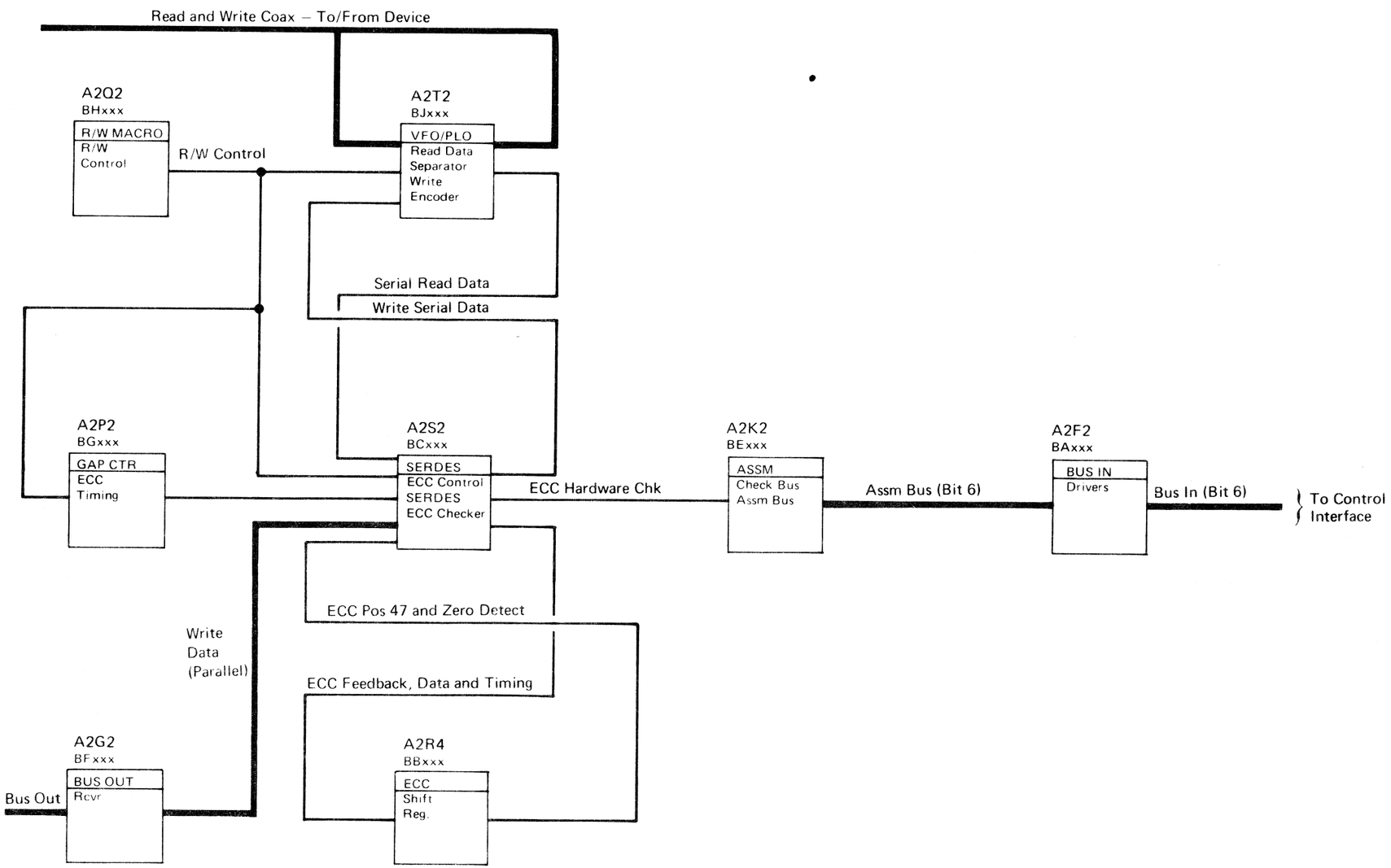
ECC HARDWARE CHECK

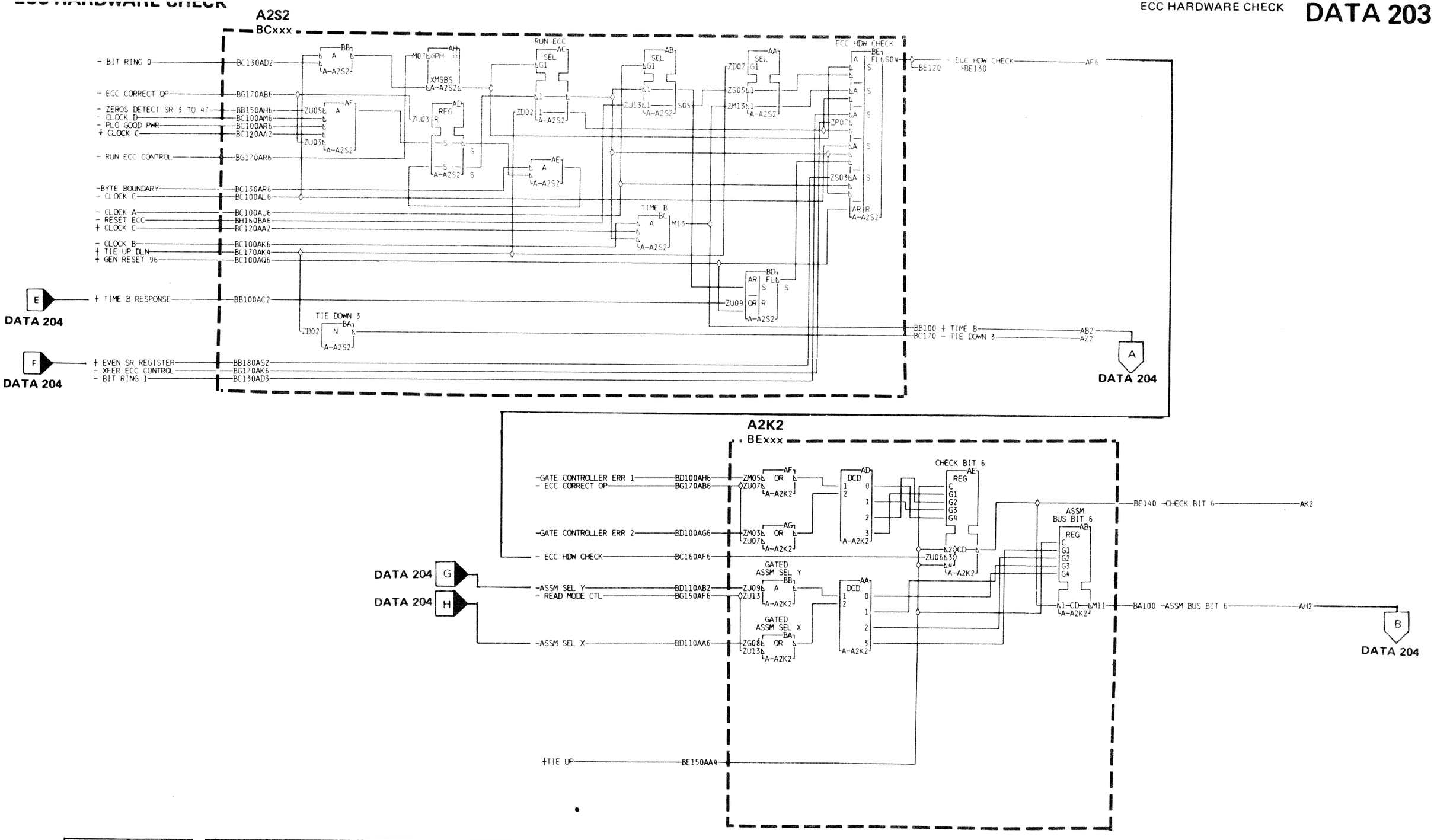
ECC HARDWARE CHECK

The ECC Hardware Check is set by:

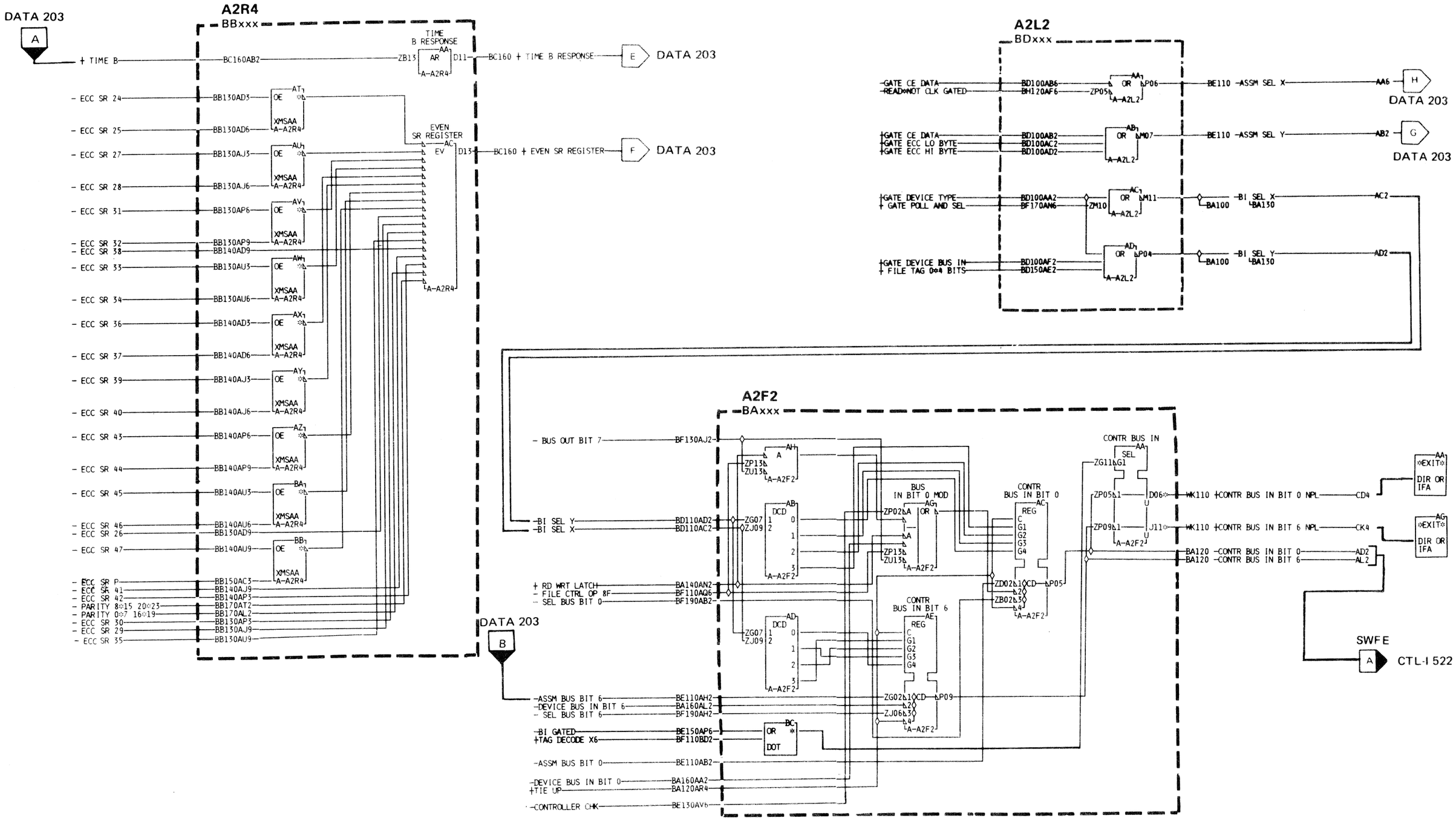
1. An odd number of ECC SR bits at B time.
2. Missing C pulse to the Shift Register as indicated by the lack of +Time B Response.
3. Missing B pulse to the Shift Register as indicated by the lack of +Time B Response.
4. +Time A Reset active all the time.
5. Failure to activate Run ECC.
6. Transfer ECC On Without Run ECC, activates Controller Check and Error Alert.




Read and Write Coax – To/From Device
A2Q2
BHxxx
R/W MACRO
R/W
Control
R/W Control
A2T2
BJxxx
VFO/PLO
Read Data
Separator
Write
Encoder
Serial Read Data
Write Serial Data
A2P2
BGxxx
GAP CTR
ECC
Timing
A2S2
BCxxx
SERDES
ECC Control
SERDES
ECC Checker
ECC Hardware Chk
A2K2
BExxx
ASSM
Check Bus
Assm Bus
Assm Bus (Bit 6)
A2F2
BAxxx
BUS IN
Drivers
Bus In (Bit 6)
To Control
Interface
ECC Pos 47 and Zero Detect
Write
Data
(Parallel)
ECC Feedback, Data and Timing
A2G2
BFxxx
BUS OUT
Rcvr
Bus Out
A2R4
BBxxx
ECC
Shift
Reg.



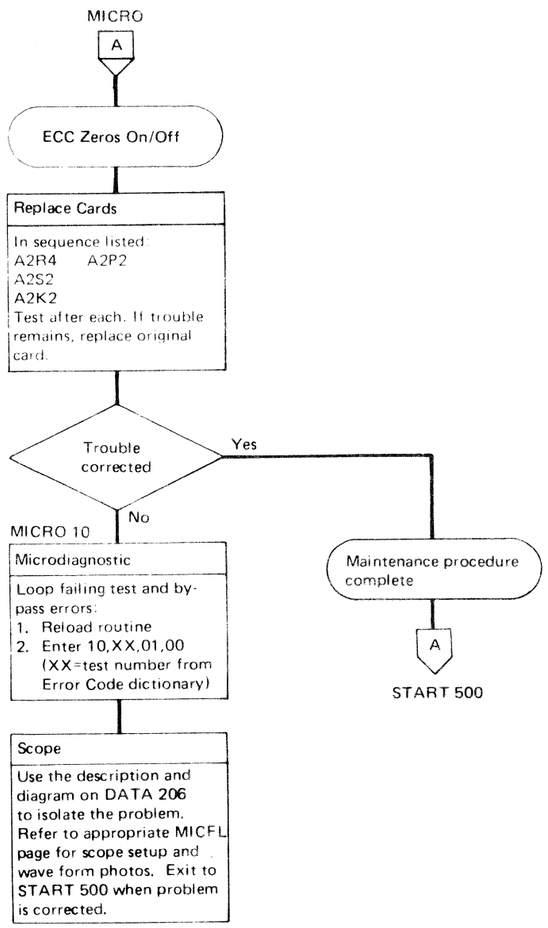
ECC HARDWARE CHECK

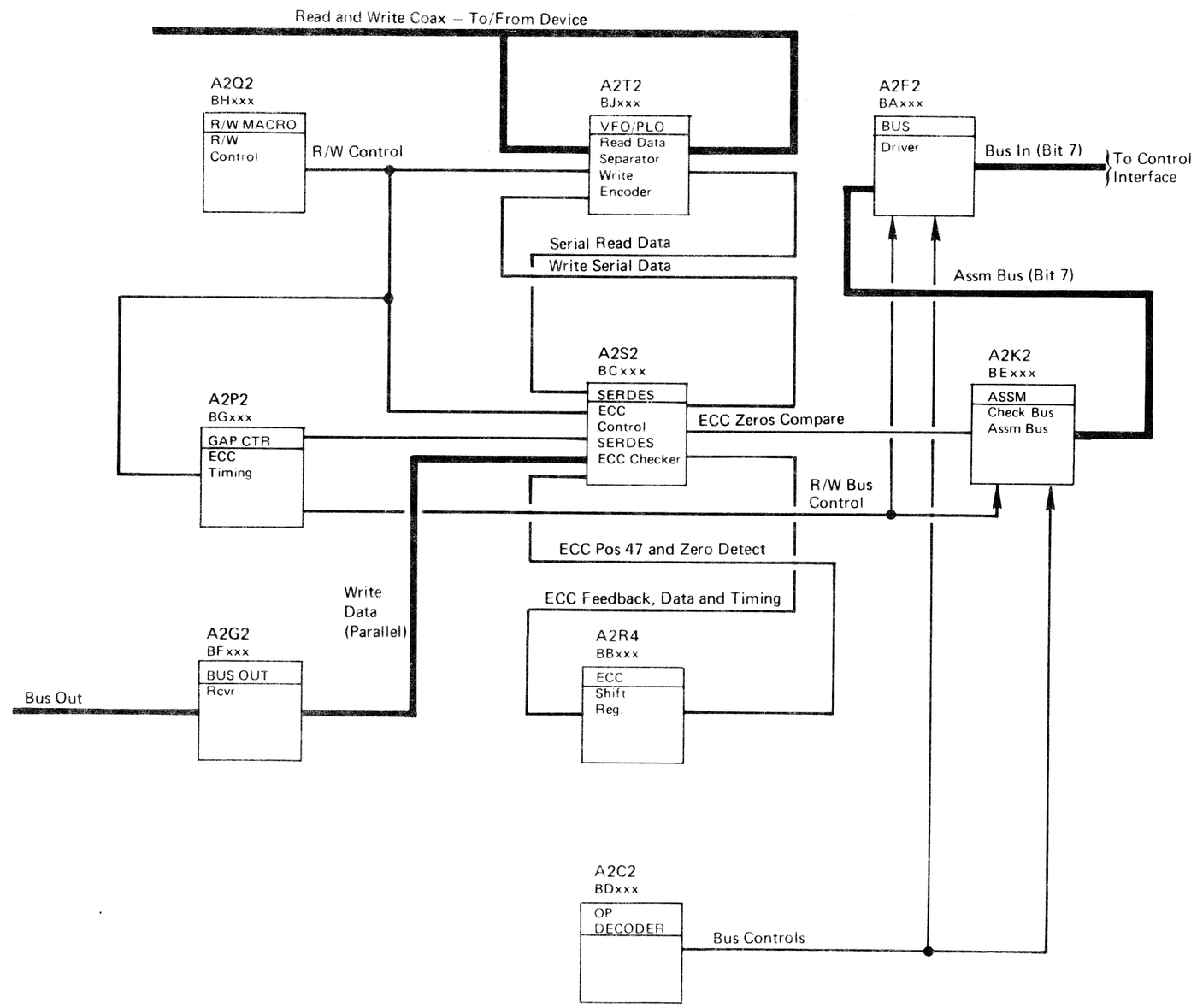


ECC Zeros Compare results if:

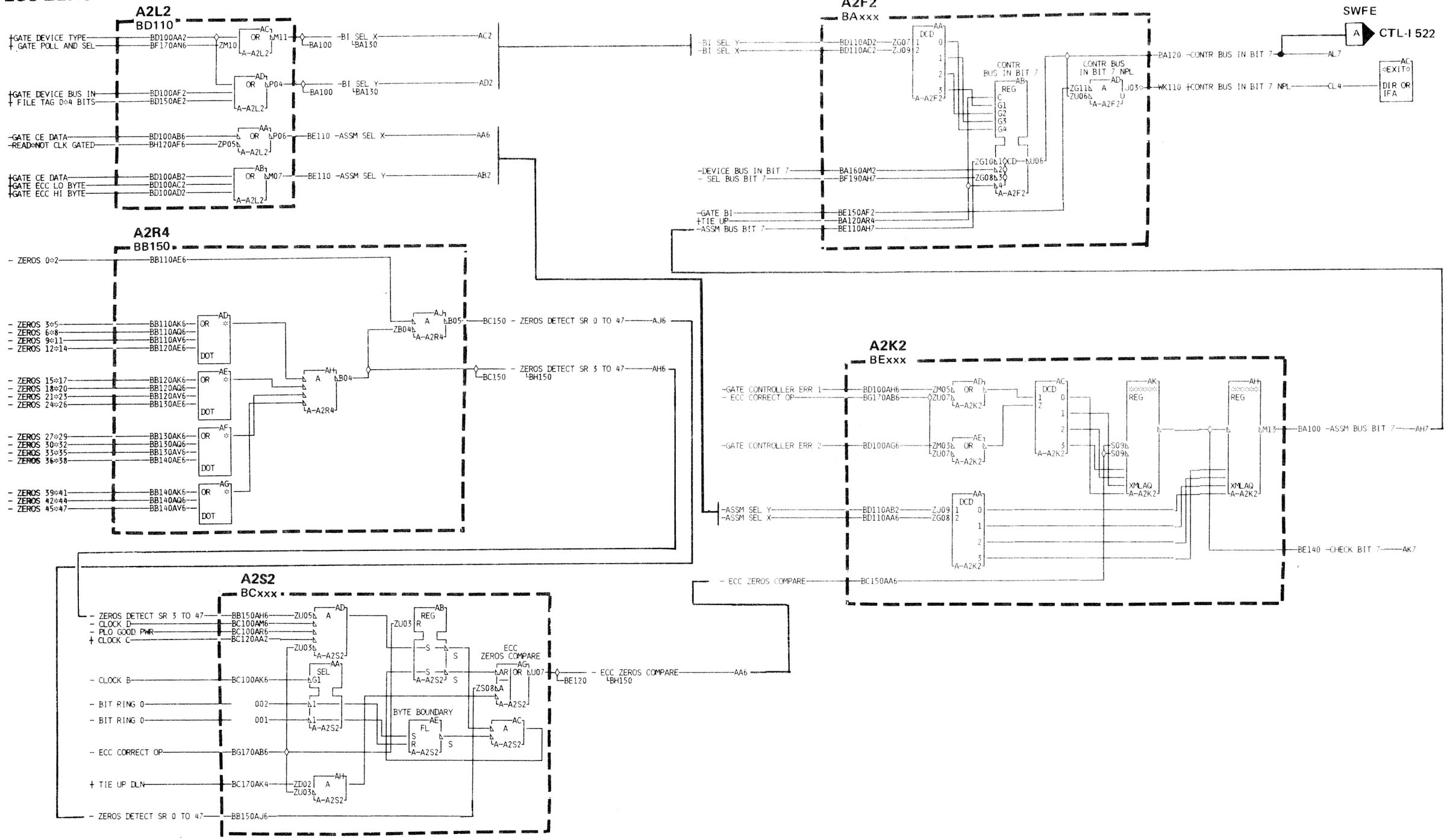
A. All positions of the ECC Shift Register are off or a logical zero, except during an ECC Correct Operation.
B. The first byte boundary after the ECC Shift Register positions 3 to 47 were all off or a logical zero, during an ECC Correct Operation.

In the case of B above, the correction pattern is in ECC Shift Register positions 0 to 15. The pattern can be gated to the storage control by Gate ECC Low Byte for bits 0 to 7 and Gate ECC Hi Byte for bits 8 to 15. It would be an error for both the Hi and Lo bytes to be zero at the end of an ECC Correct Op for a correctable Data Check since zeros exclusive ORed with any value do not change that value.





ECC ZEROS COMPARE



BT0206 Seq. 1 of 2	2747557 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440218 5 Aug 74	440223 14 Mar 75	

3340

ECC DATA CHECK

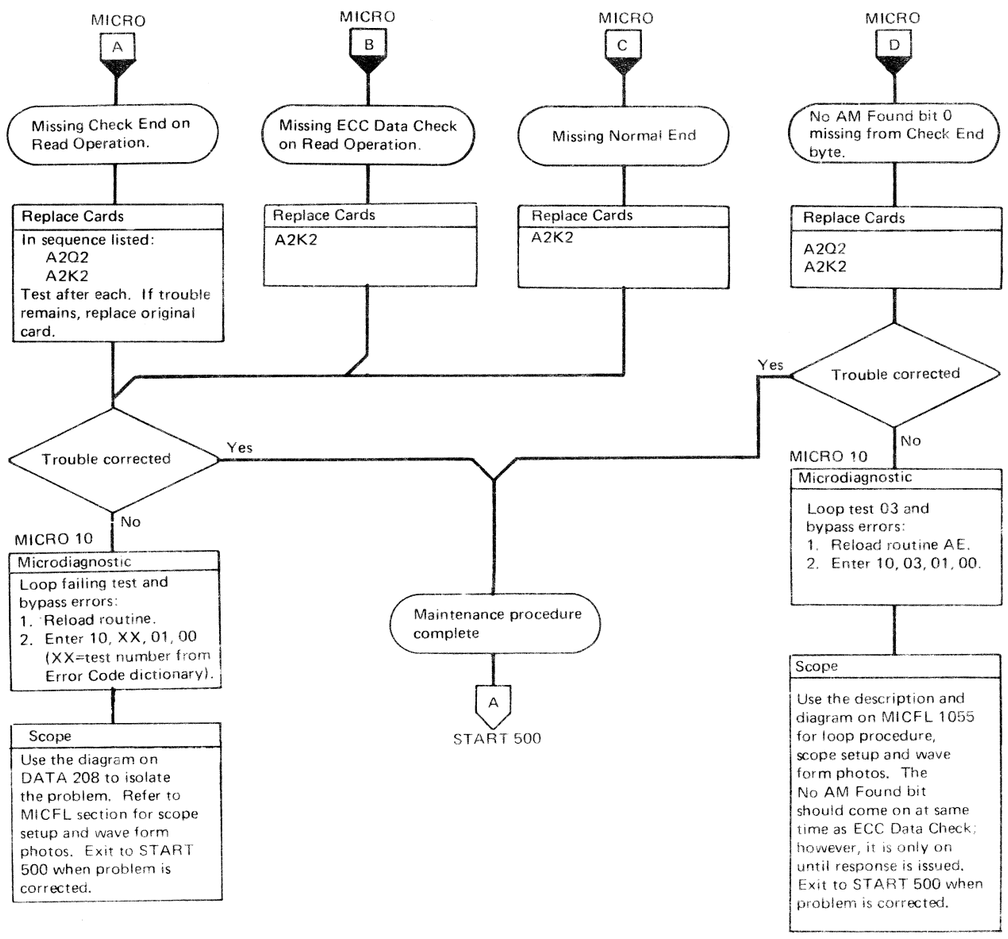
The ECC control allows the serial data bits read from the disk to be shifted through the ECC Shift Register until the end of the data field.

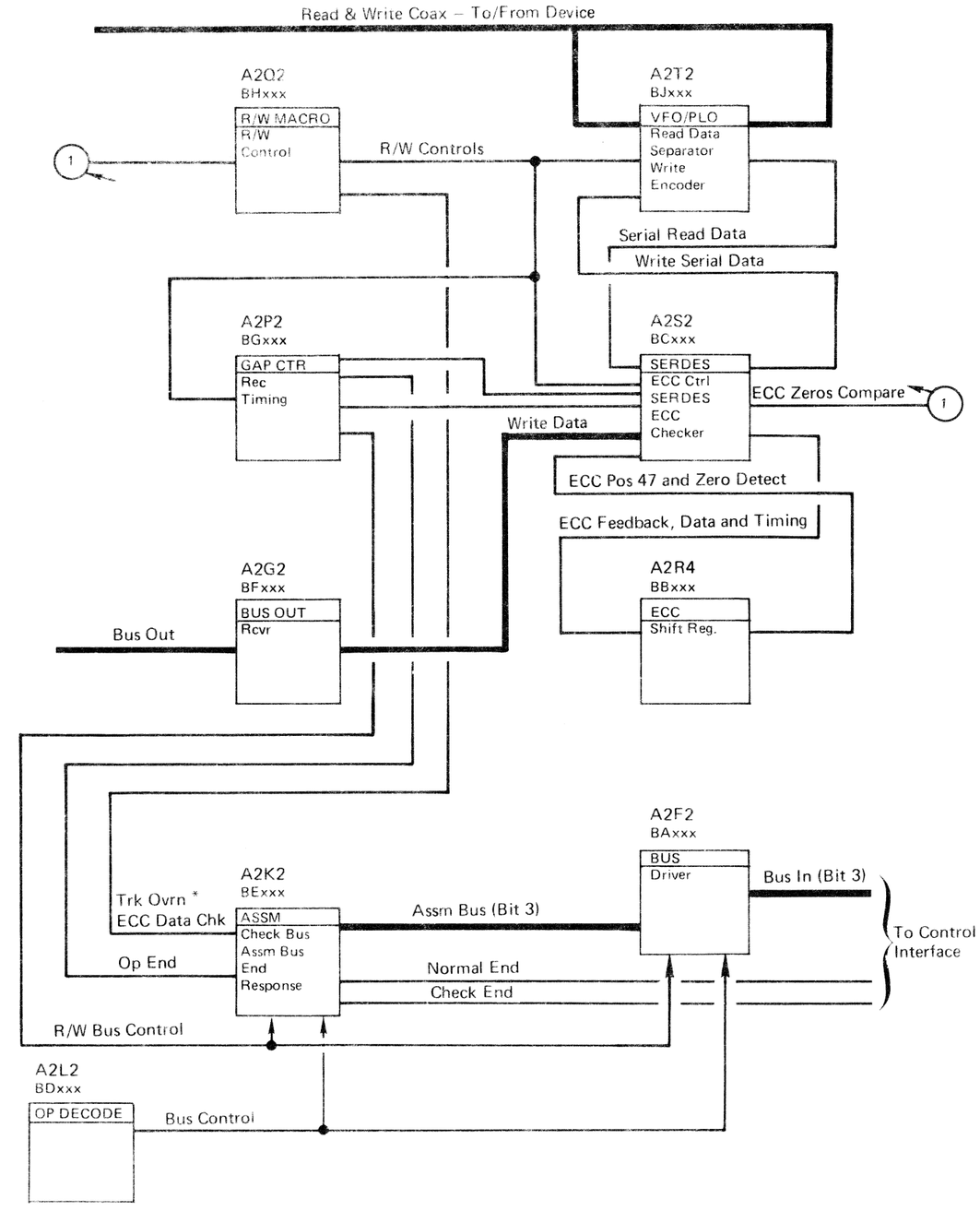
After the end of data is reached, the six ECC bytes are shifted through the ECC Shift Register. If there are no data errors, the ECC Shift Register is zero and ECC Zeros Compare is active.

The absence of ECC Zeros Compare at the end of a Read operation sets the ECC Data Check latch causing Check End to be generated.

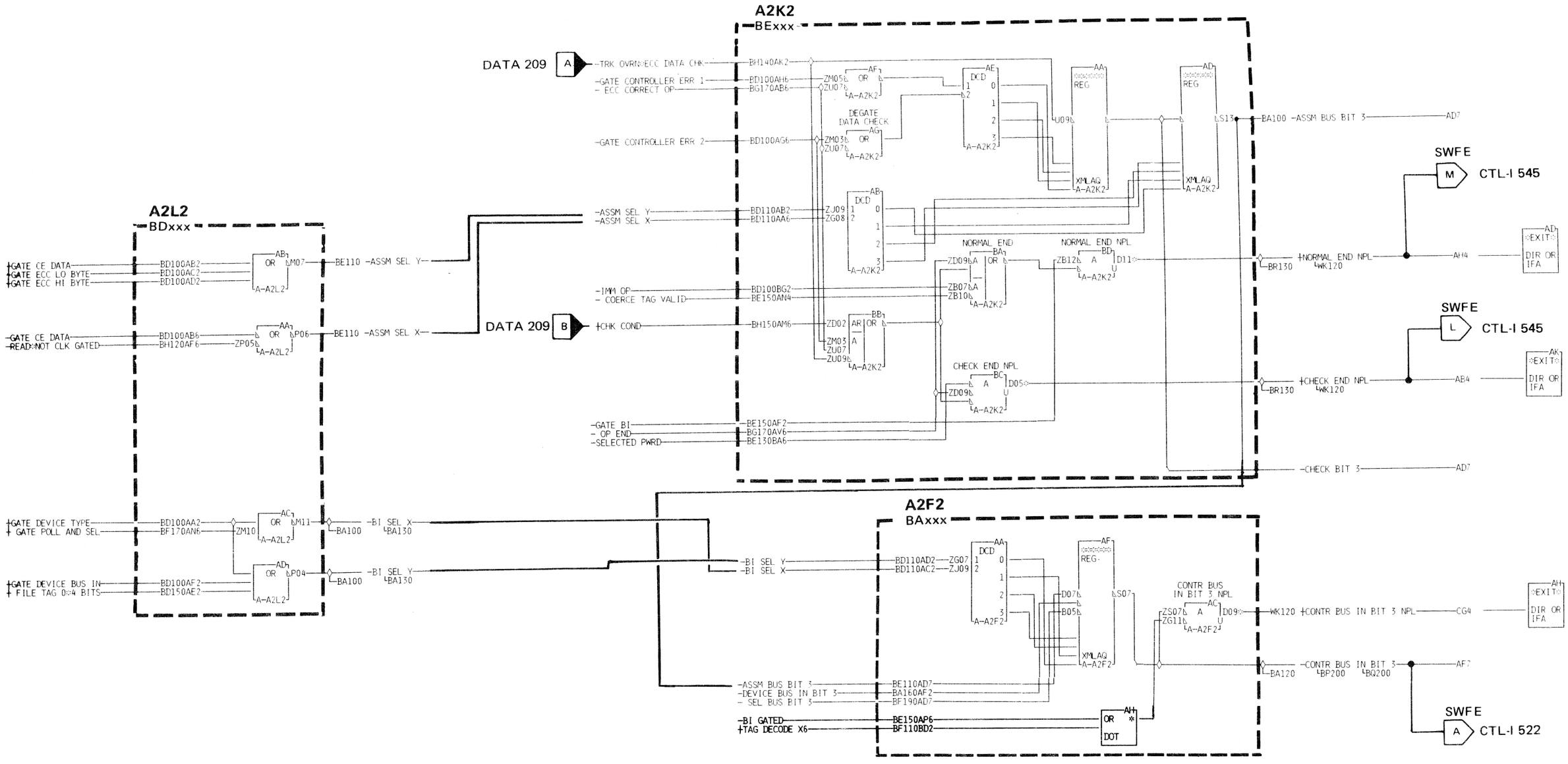
When Check End is indicated, Bus In bit 3 indicates ECC Data Check.

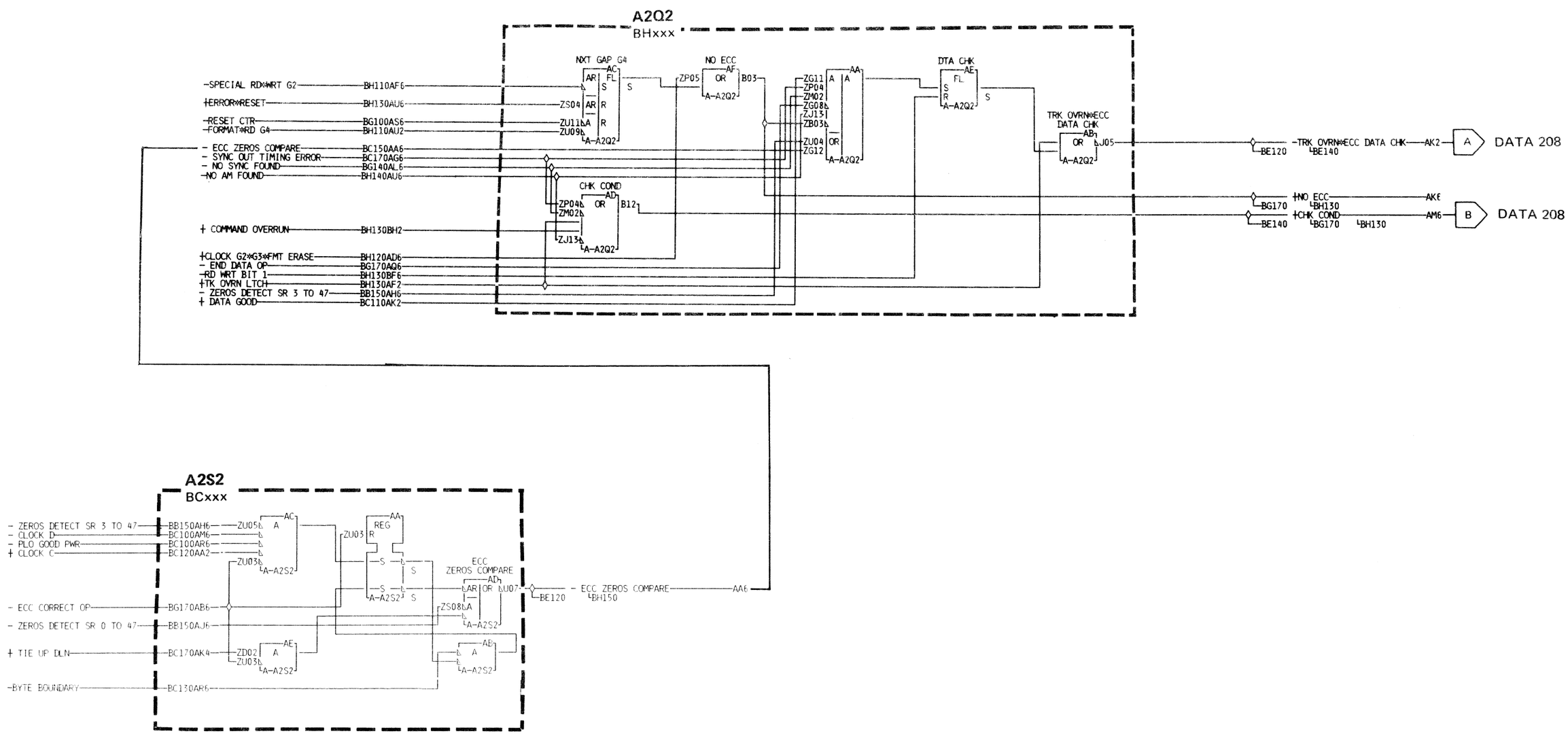
See OPER 242 for description of Error Correction.



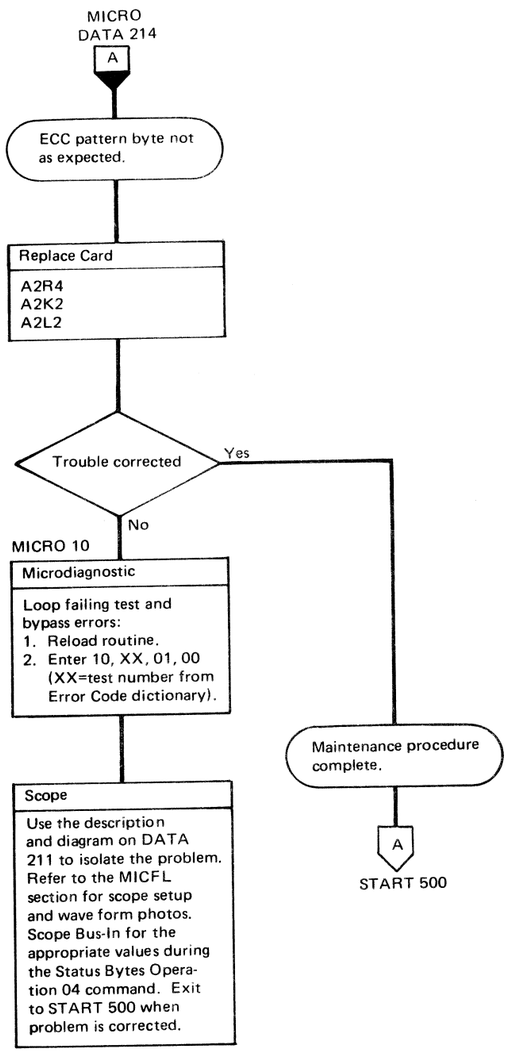


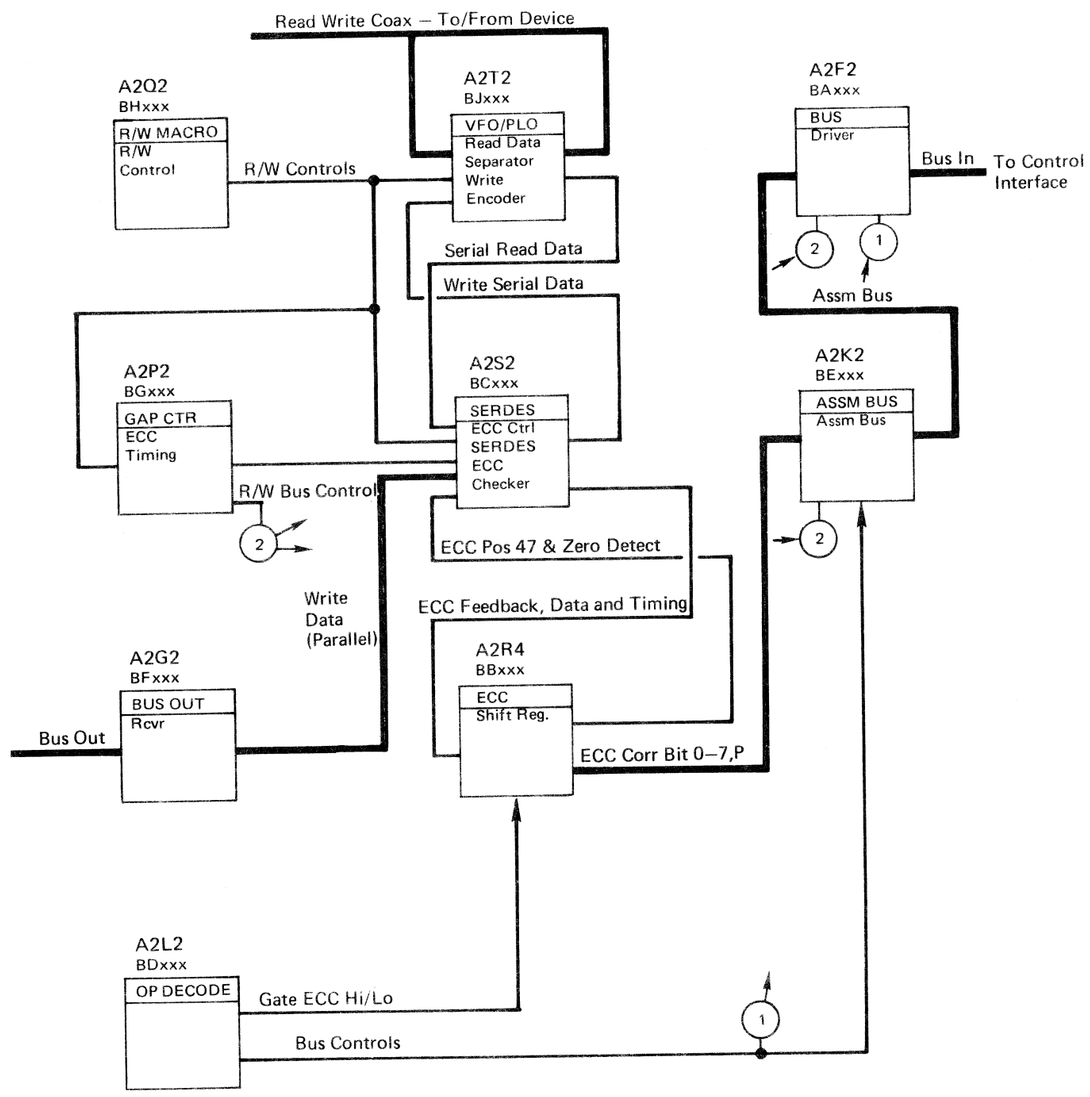
ECC DATA CHECK

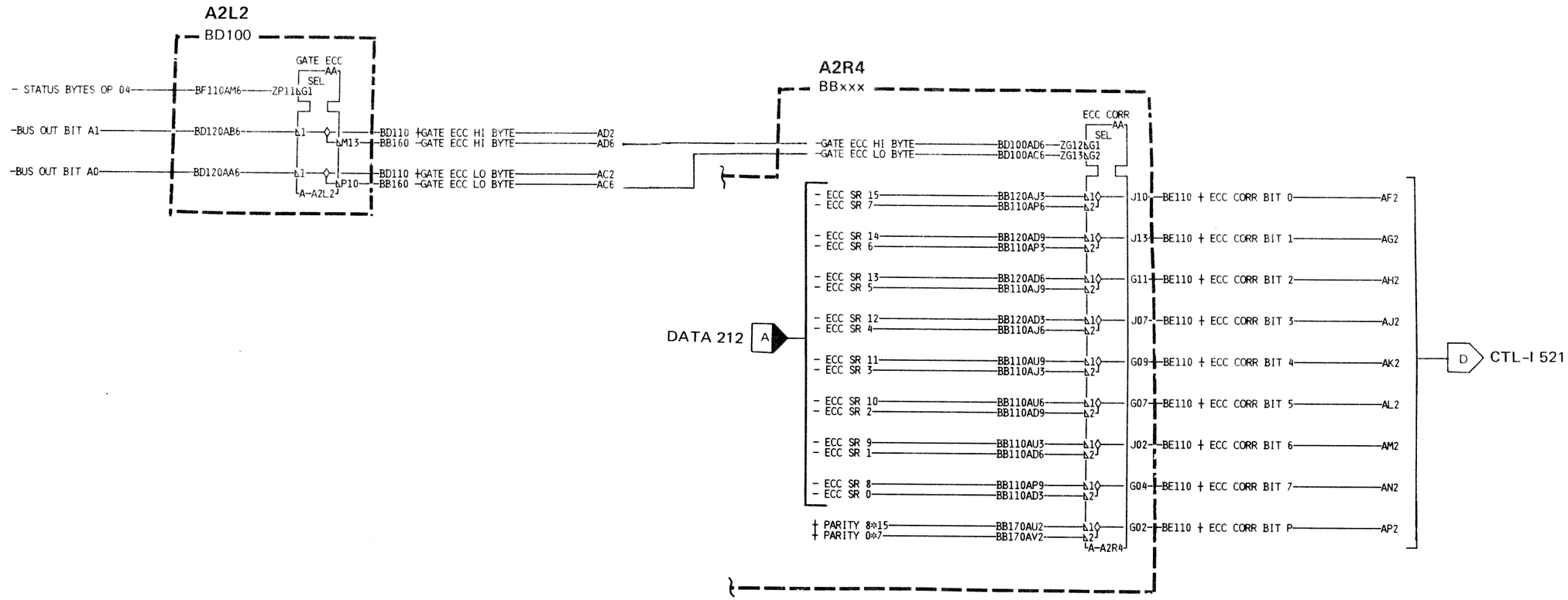




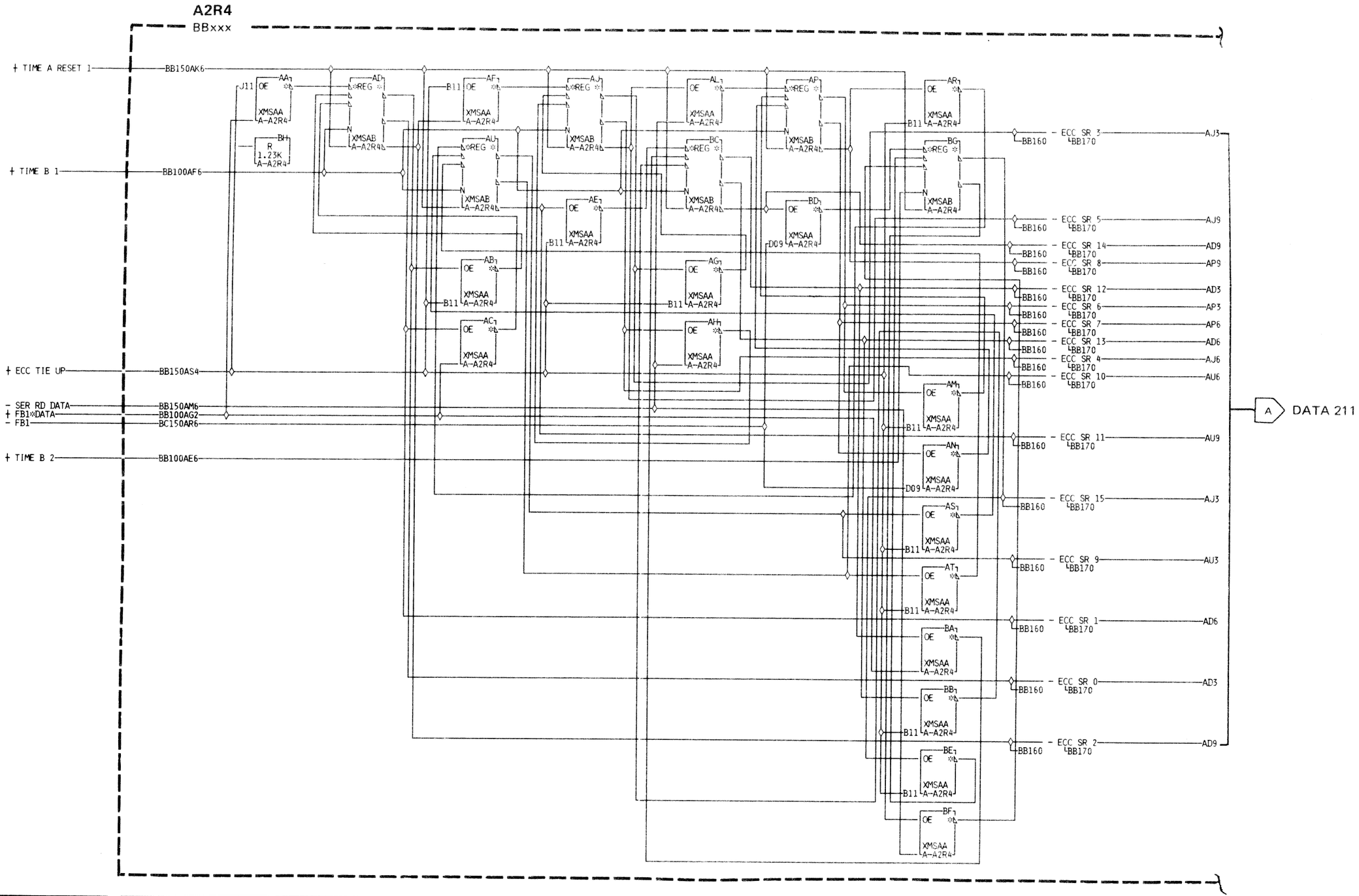
ECC PATTERN BYTE ERRORS







BT0210 Seq. 2 of 2	2747559 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74			



MICROPROGRAM DETECTED ECC HARDWARE CHECK

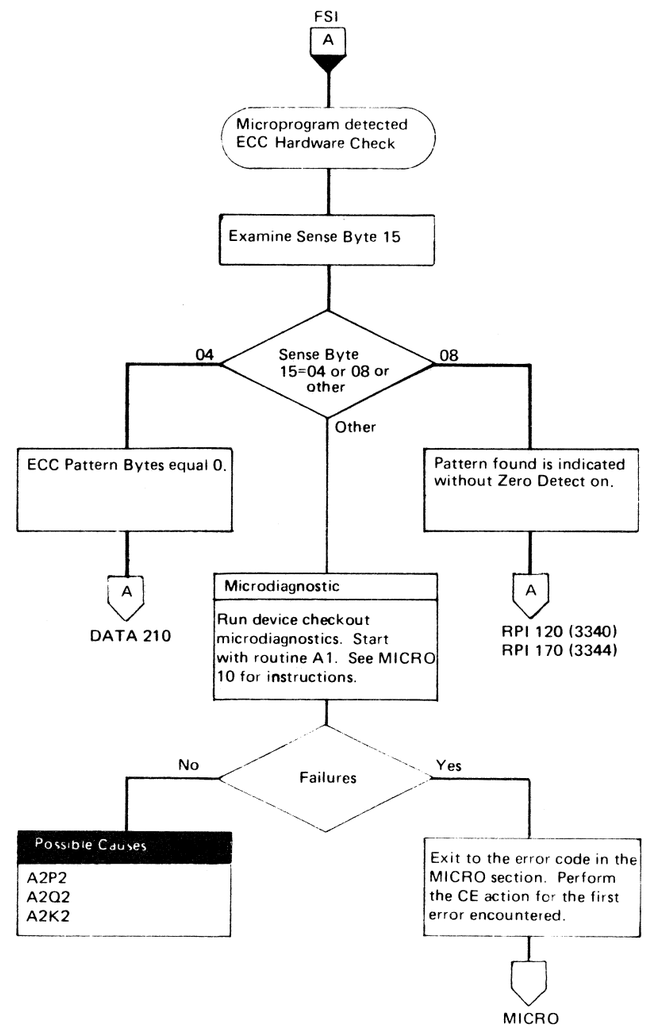
When the controller is performing an ECC Correct operation (Tag '08'), and Index Alert indicates that a correctable pattern has been found. When Index Alert is received by the microprogram, a check is made to ensure that Zero Detected is on. If Zero Detected is not on, an error is indicated.

If Zeros Detected is present, the ECC pattern bytes are sensed (Tag '04'). If both bytes are 0, an error is indicated.

If No AM Found bit is on with a Check End following a data transfer, the ECC Data Check bit must be on also. No AM Found (bit 4) is used as a redundancy check.

Either of these errors is indicated as microprogram detected error 05 (Byte 18, Hex 05) or Symptom Code 9005.

See OPER 242 for a description of ECC Correct operation.



The Monitor Check is a check of the Bit Ring and Gap Counter operation along with a check that an Address Mark Search operation is progressing satisfactorily. Failures in these areas could result in a hang condition.

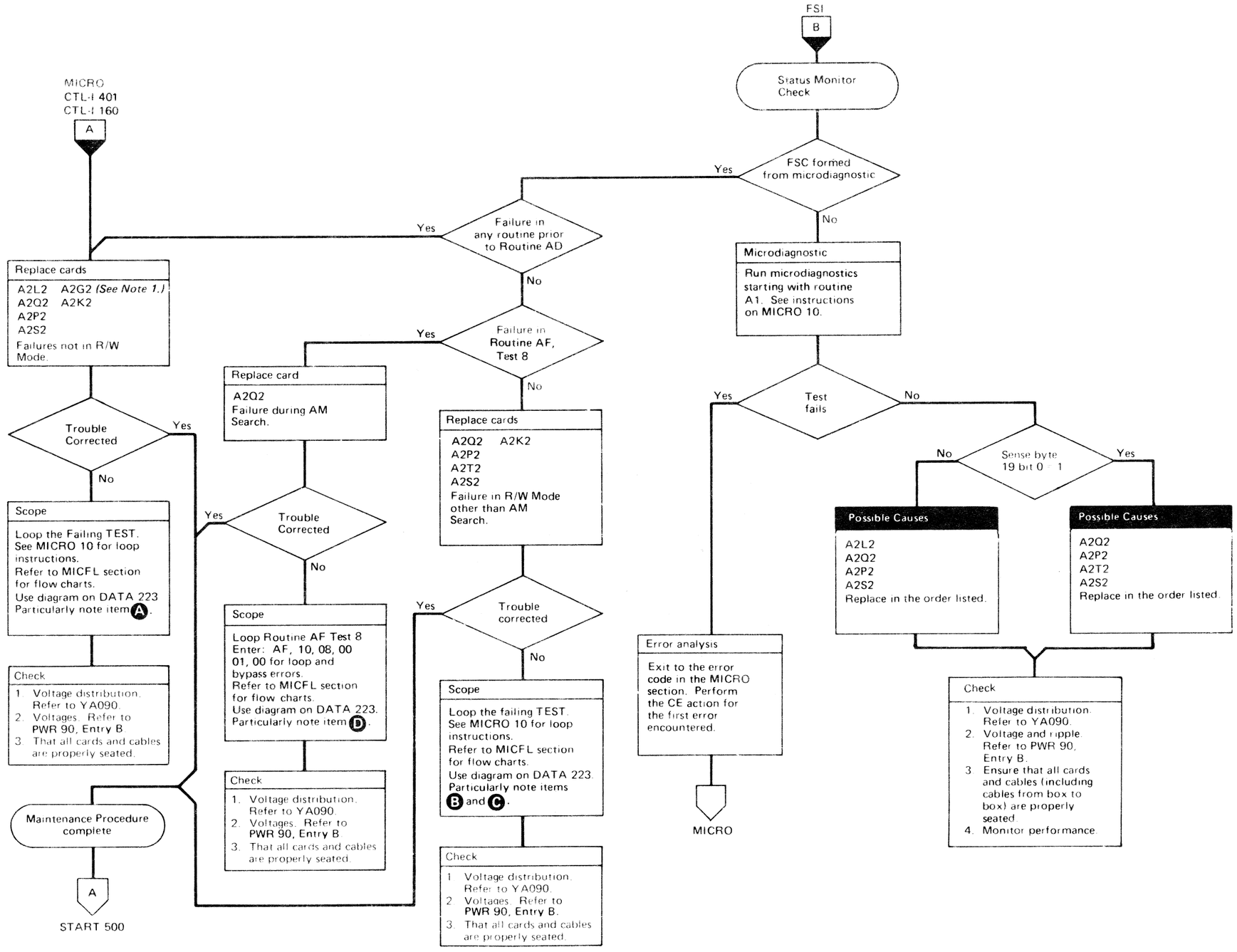
Monitor Check is also used to indicate that I Write Sense was not received from the drive during a Write operation. The lack of I Write Sense during Write Mode blocks the generation of Function pulses.

Various operations produce Function pulses at various frequencies. At least one Function pulse must be generated for every four PLO pulses (eight byte times) when the controller is selected. This is accomplished through a series of AND circuits that generate Function pulses in the following four categories:

A. Idle
B. Data Correct Op, or Format Erase Reorient.
C. ECC Transfer or Gaps.
D. Address Mark Search.

For example: During an Address Mark Search, Raw Read Data pulses are used to generate Function pulses. When an Address Mark is being read it would be normal not to receive Raw Read Data for 3 bytes times, therefore no Function pulses. It would be an error, however, for Raw Read Data to be missing for eight or more bytes, therefore the Monitor Check latch would be set.

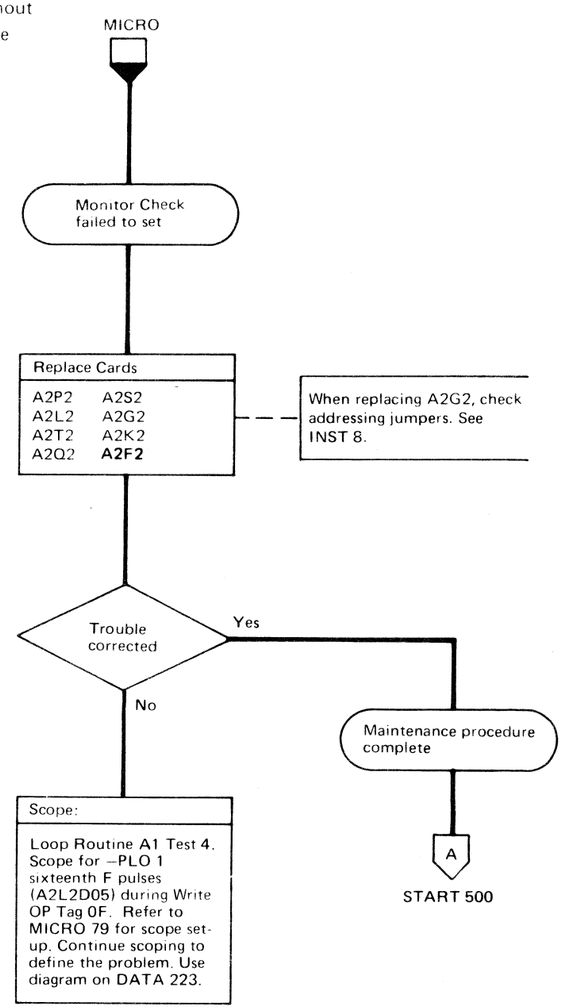
Note 1: When replacing A2G2, check addressing jumpers. See INST 8.

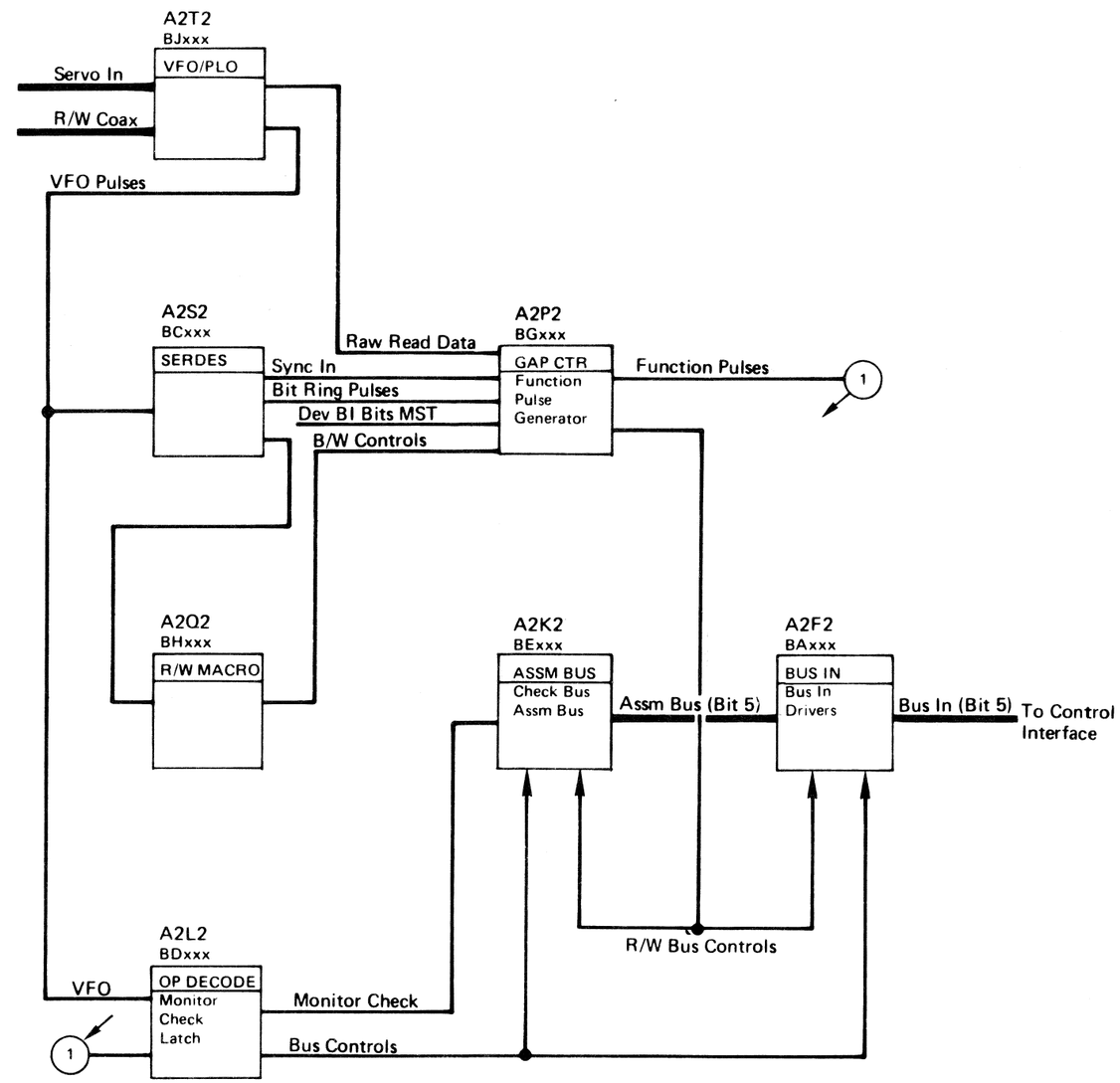


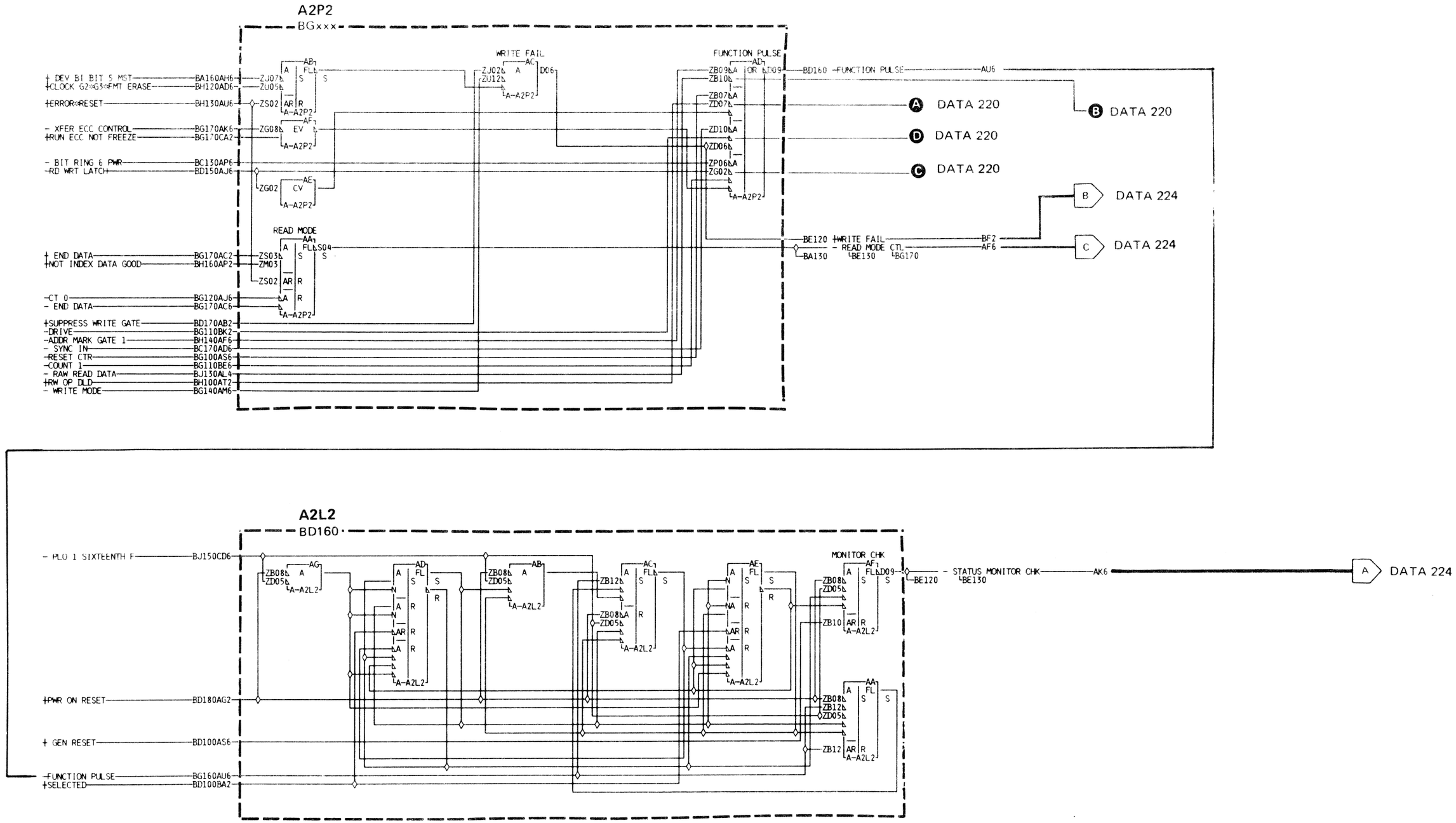
BT0214	2747560	See	440223	440224				
Seq 2 of 2	Part No. ( )	EC History	14 Mar 75	15 Dec 75				

MONITOR CHECK CHECKER

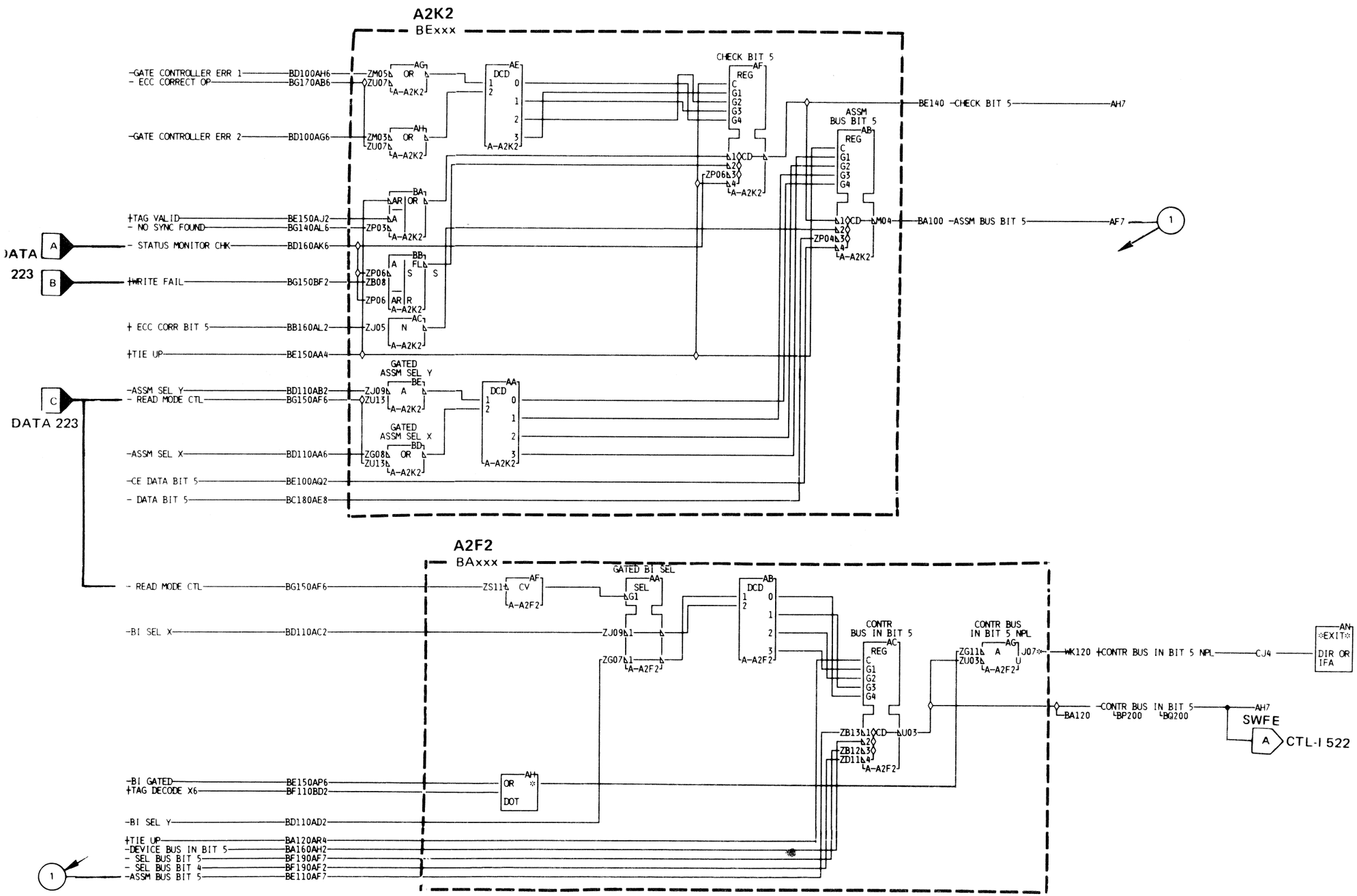
Read and Write Tags are issued in routine A1 test 4 without first issuing a Set Read/Write OP. This unusual sequence should result in the Monitor Check latch being set. The latch is then checked to ensure that it is set.







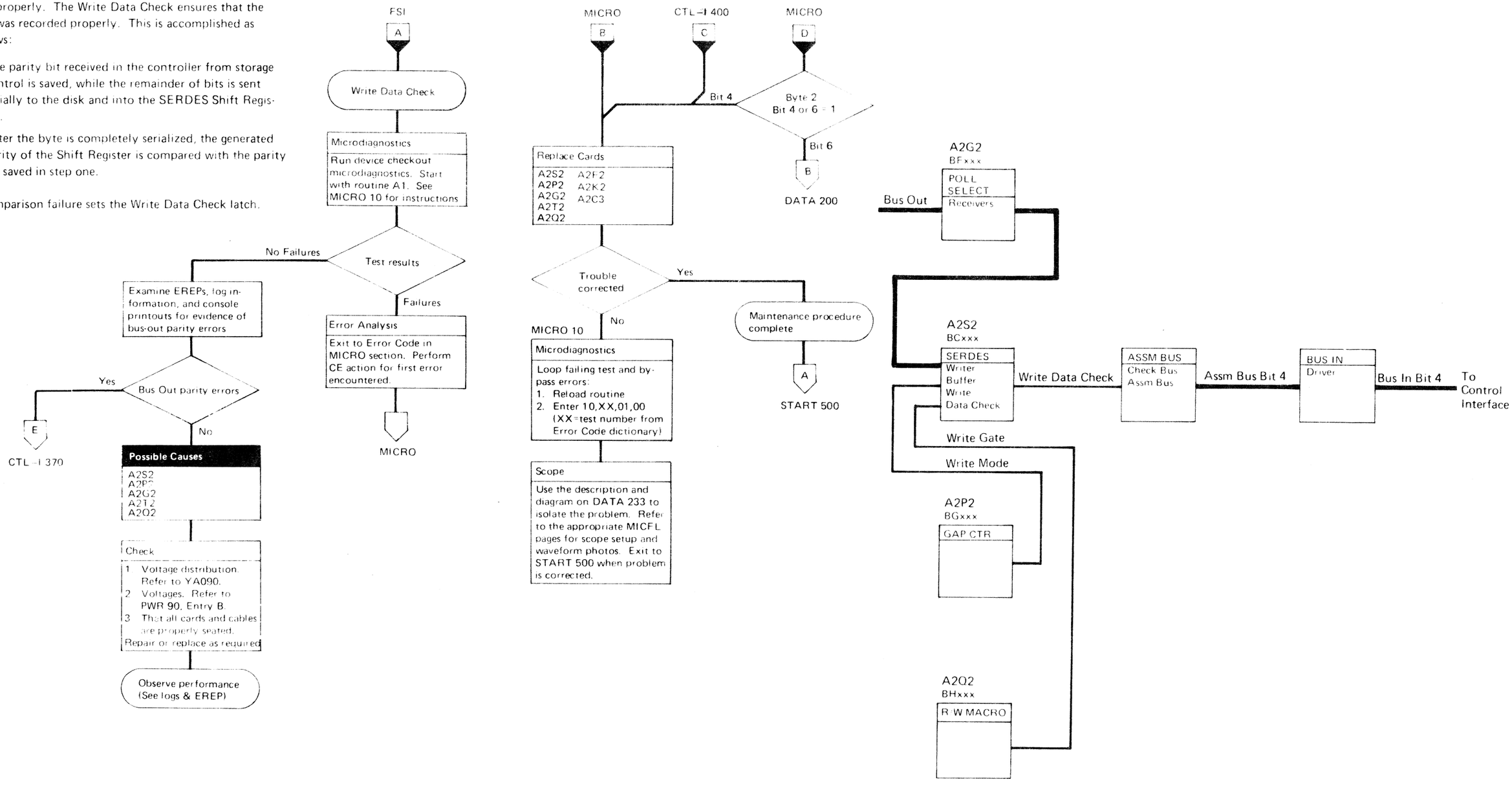
BT0221	2747605	440202	440203	440209	440224			
Seq. 2 of 2	Part No.( )	7 Sept 73	2 Nov 73	25 Mar 74	15 Dec 75			

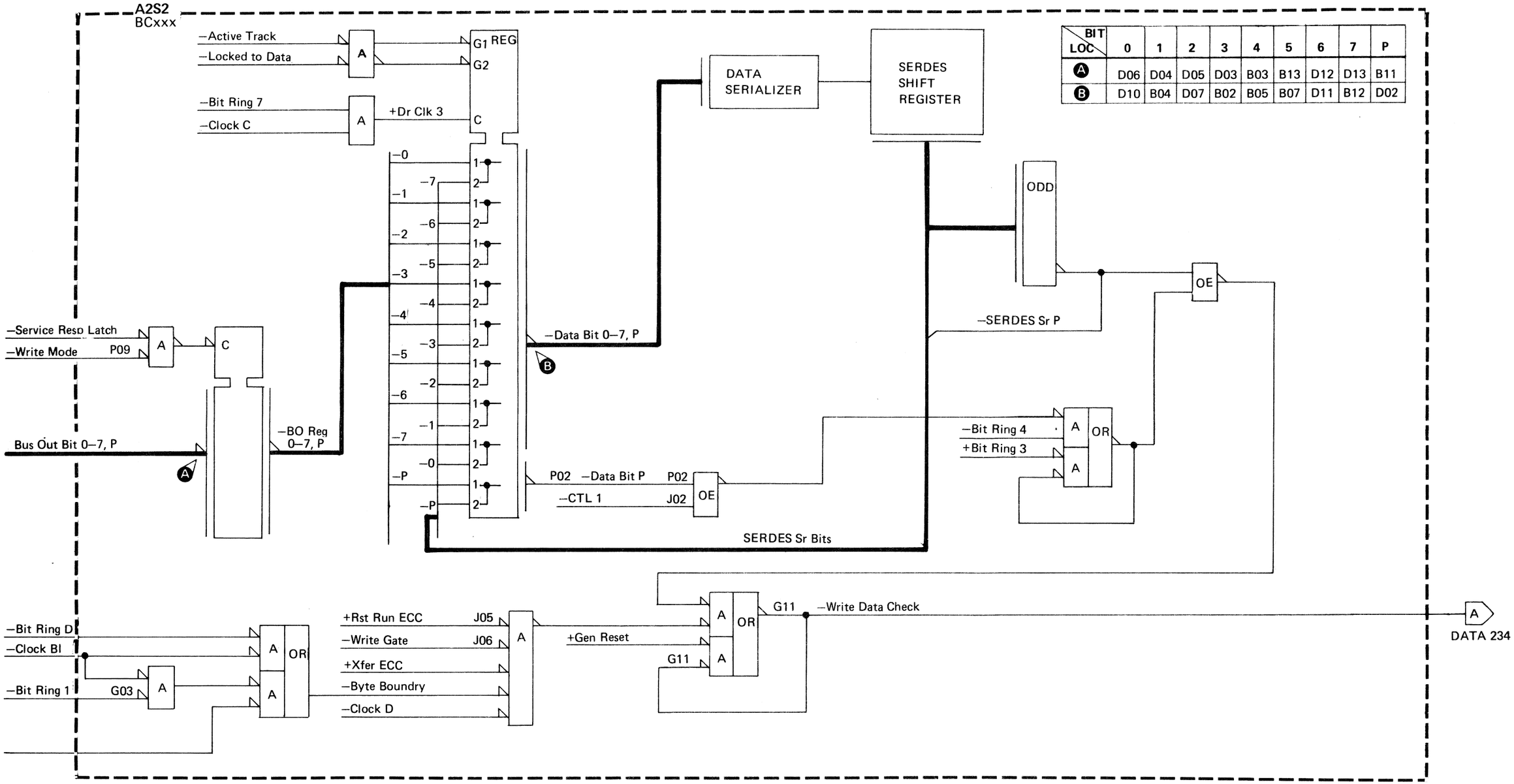

A2K2
BExxx
-GATE CONTROLLER ERR 1
- ECC CORRECT OP
-GATE CONTROLLER ERR 2
+TAG VALID
- NO SYNC FOUND
- STATUS MONITOR CHK
+WRITE FAIL
+ ECC CORR BIT 5
+TIE UP
-ASSM SEL Y
- READ MODE CTL
-ASSM SEL X
-CE DATA BIT 5
- DATA BIT 5
BD100AH6
BG170AB6
BD100AG6
BE150AJ2
BG140AL6
BD160AK6
BG150BF2
BB160AL2
BE150AA4
BD110AB2
BG150AF6
BD110AA6
BE100AQ2
BC180AE8
CHECK BIT 5
BE140 -CHECK BIT 5
AH7
ASSM BUS BIT 5
BA100 -ASSM BUS BIT 5
AF7
GATED ASSM SEL Y
GATED ASSM SEL X
DATA 223
A2F2
BAxxx
GATED BI SEL
- READ MODE CTL
-BI SEL X
-BI GATED
+TAG DECODE X6
-BI SEL Y
+TIE UP
-DEVICE BUS IN BIT 5
- SEL BUS BIT 5
- SEL BUS BIT 4
-ASSM BUS BIT 5
BG150AF6
BD110AC2
BE150AP6
BF110BD2
BD110AD2
BA120AR4
BA160AH2
BF190AF7
BF190AF2
BE110AF7
CONTR BUS IN BIT 5
CONTR BUS IN BIT 5 NPL
+CONTR BUS IN BIT 5 NPL
CJ4
EXIT
DIR OR IFA
BA120
-CONTR BUS IN BIT 5
BP200
BG200
AH7
SWFE
CTL-I 522

The 3340 does not record parity bits on the disk surface. The Error Correction Code ensures that recorded data is read properly. The Write Data Check ensures that the data was recorded properly. This is accomplished as follows:

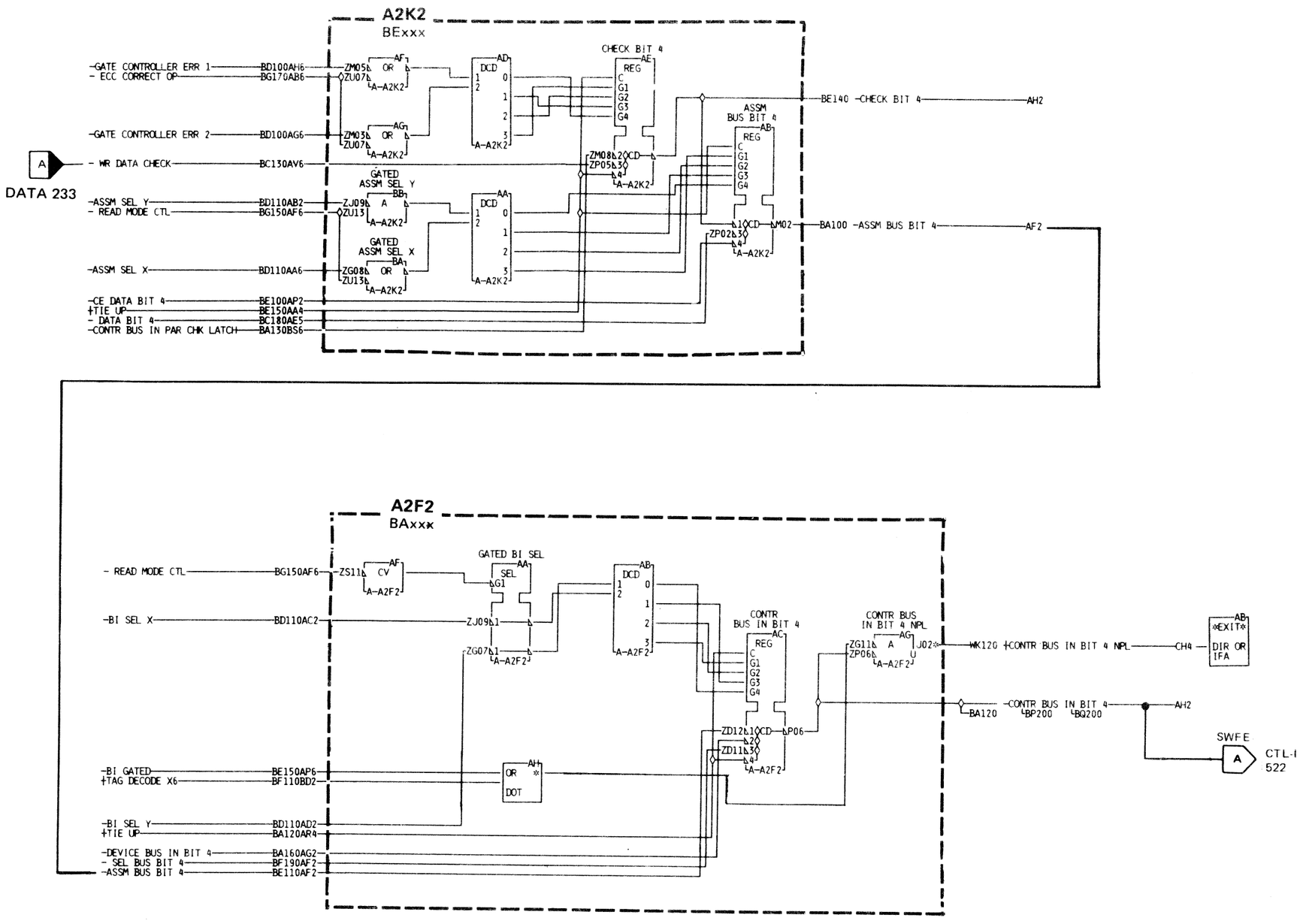
- The parity bit received in the controller from storage control is saved, while the remainder of bits is sent serially to the disk and into the SERDES Shift Register.
- After the byte is completely serialized, the generated parity of the Shift Register is compared with the parity bit saved in step one.

A comparison failure sets the Write Data Check latch.





BIT / LOC	0	1	2	3	4	5	6	7	P
A	D06	D04	D05	D03	B03	B13	D12	D13	B11
B	D10	B04	D07	B02	B05	B07	D11	B12	D02



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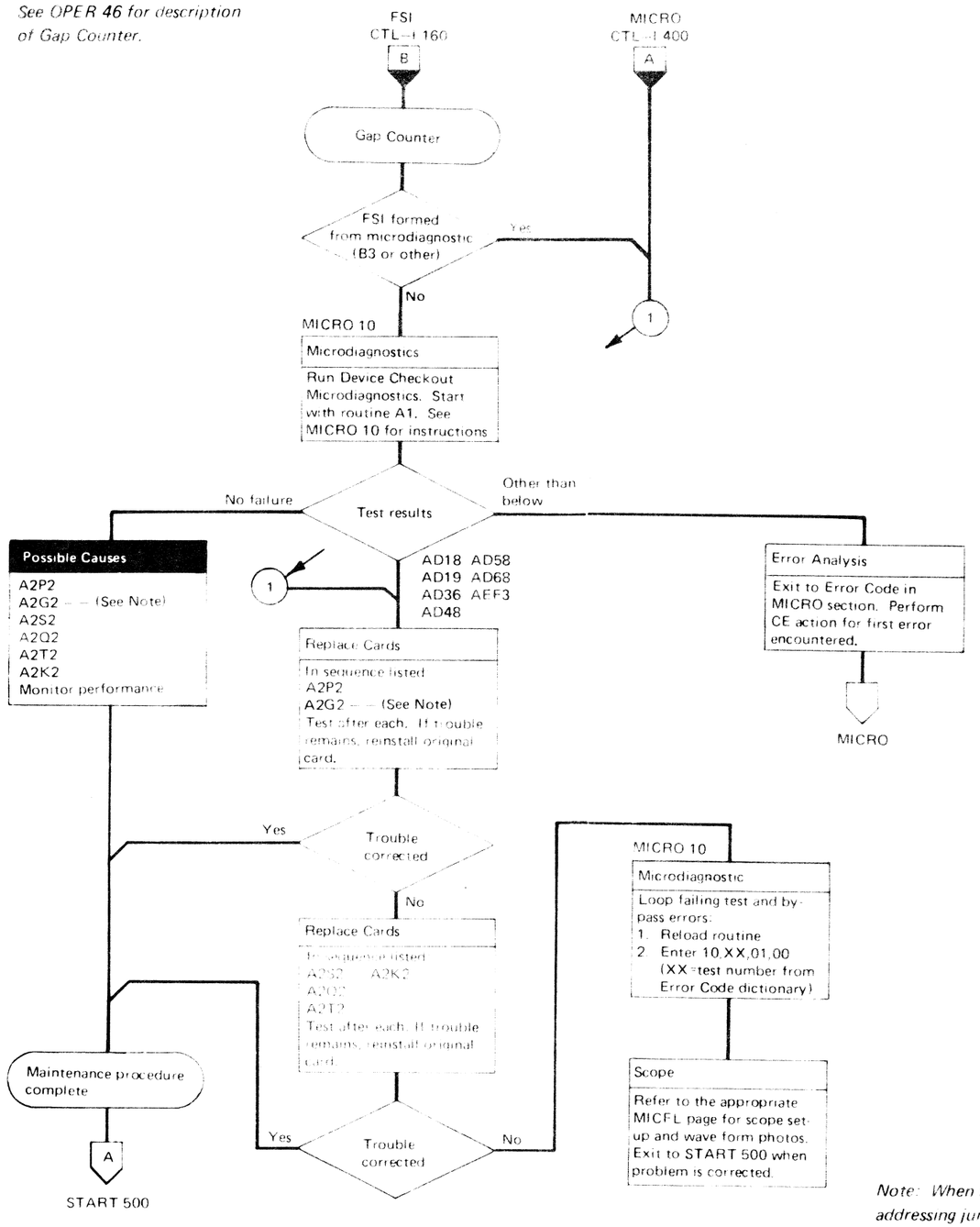
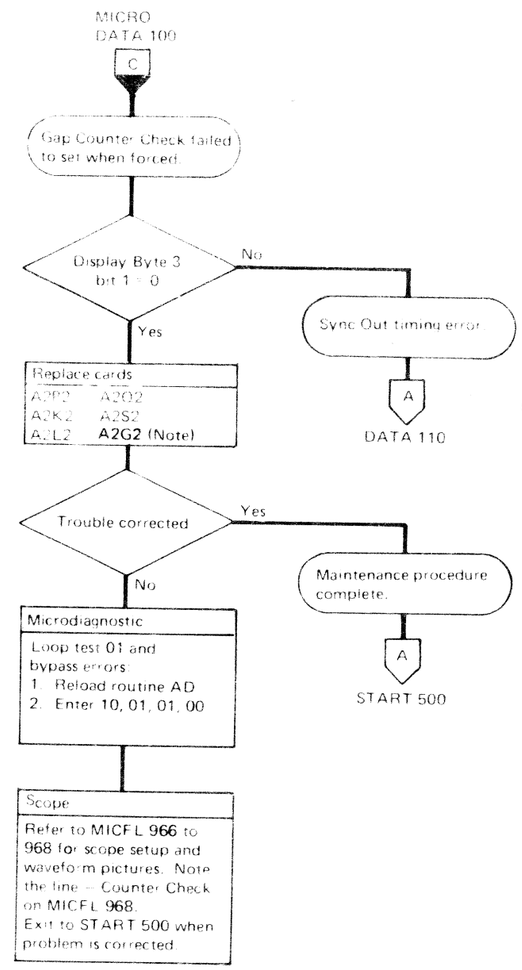
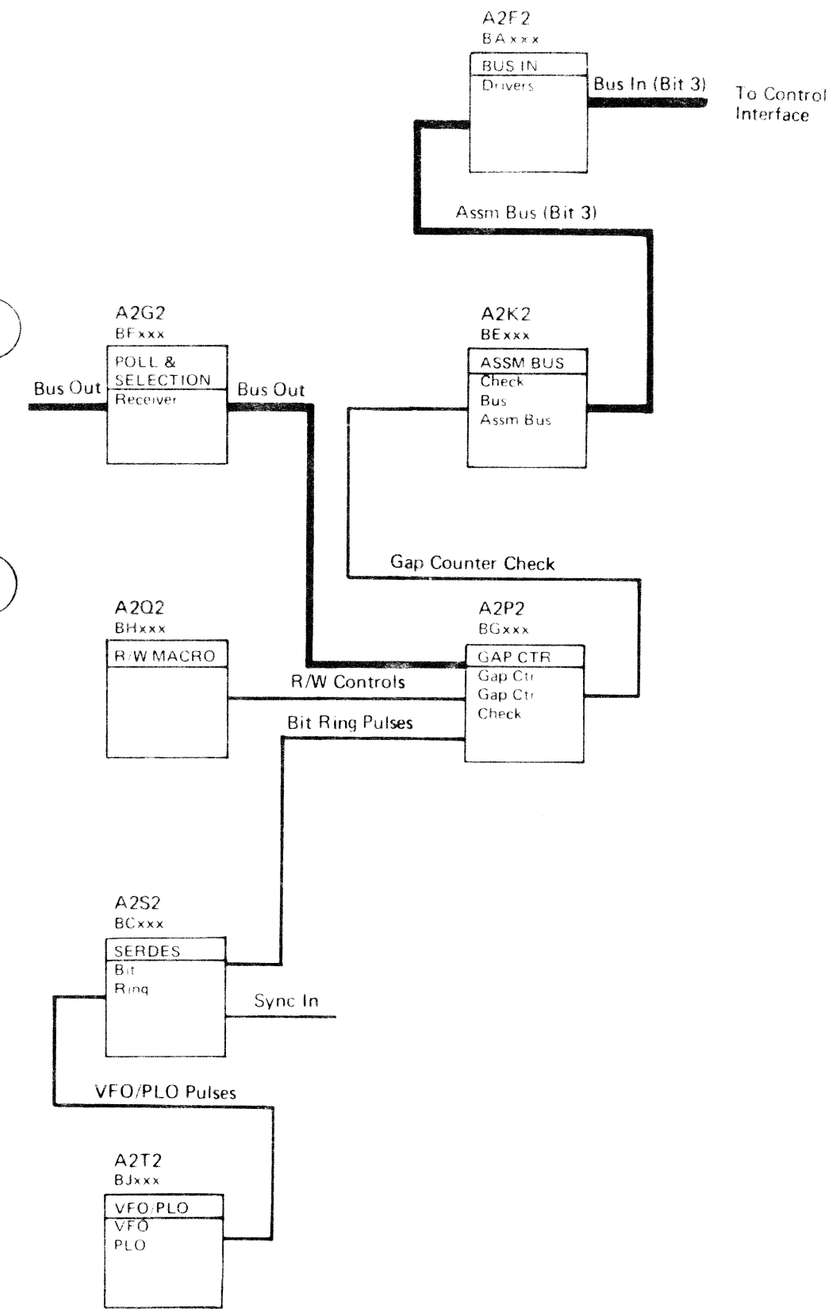
BT0237	2747697	440203	440209	440218	440223	440224		
Seq 1 of 2	Part No	2 Nov 73	25 Mar 74	5 Aug 74	14 Mar 75	15 Dec 75		

See OPER 46 for description of Gap Counter.







Note: When replacing A2G2, check addressing jumpers. See INST 8.

GAP COUNTER TOLERANCE

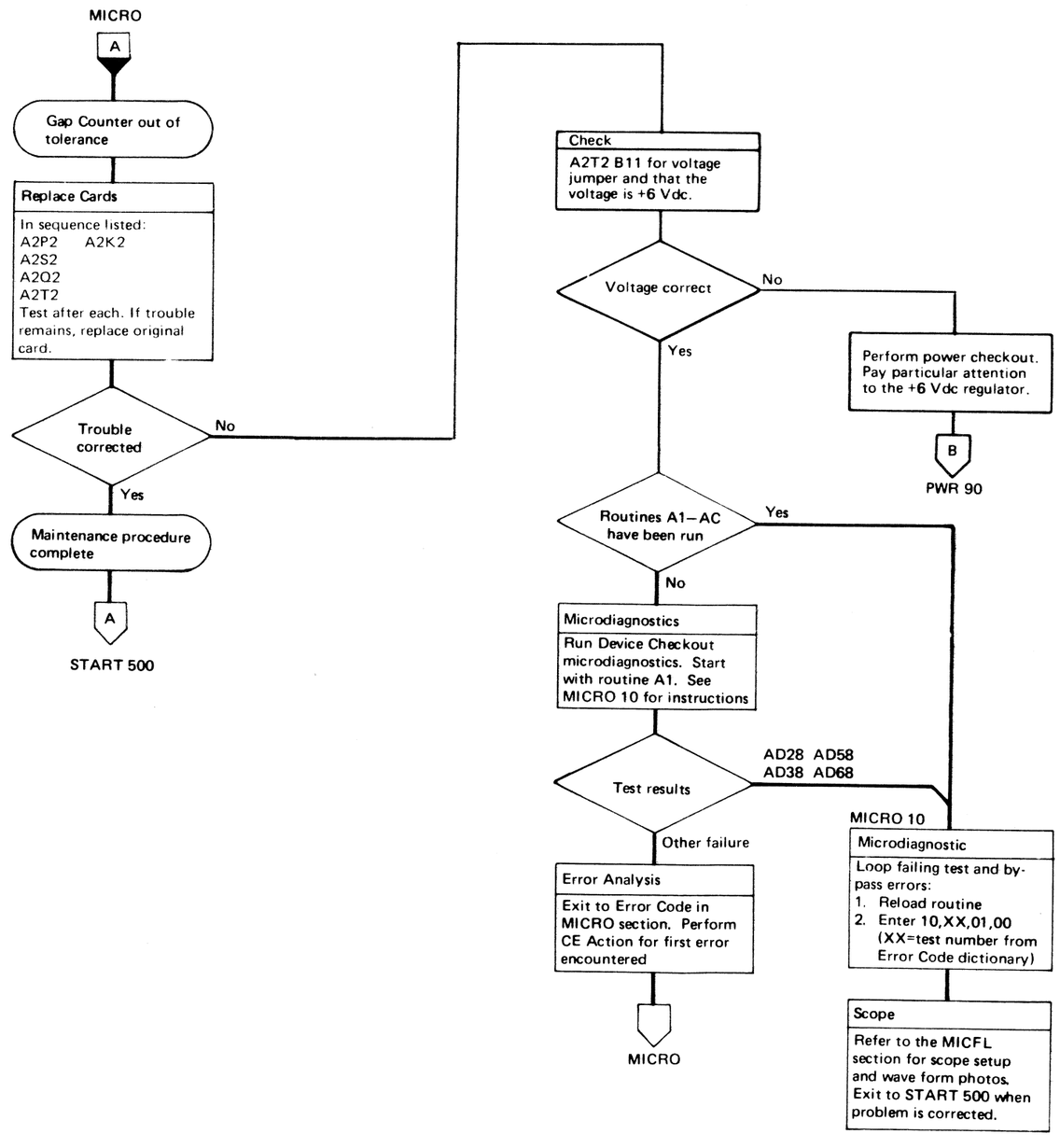
The Gap Counter test measures the duration of the various gaps. If the duration (time) is within 3 percent of normal, the Gap Counter is assumed to be operating properly.

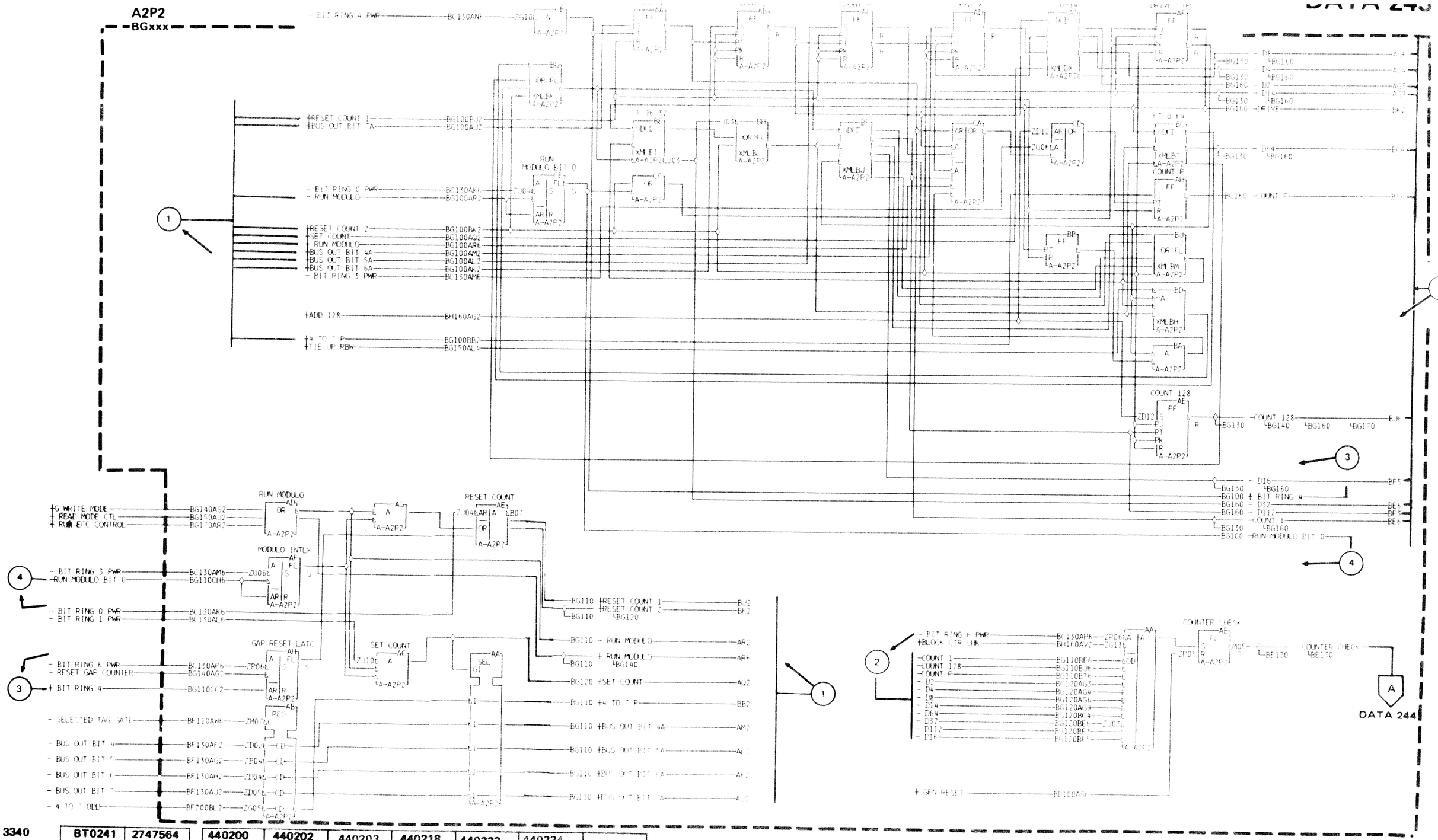
Out of tolerance indications should point to troubles in:

- Gap Counter or output decode.
- Bit Ring that provides the drive.
- A2P2 card that controls the write operation.

It is imperative that Sync In and other basic circuits are operative prior to running this test.

See OPER 46 for description of Gap Counter.

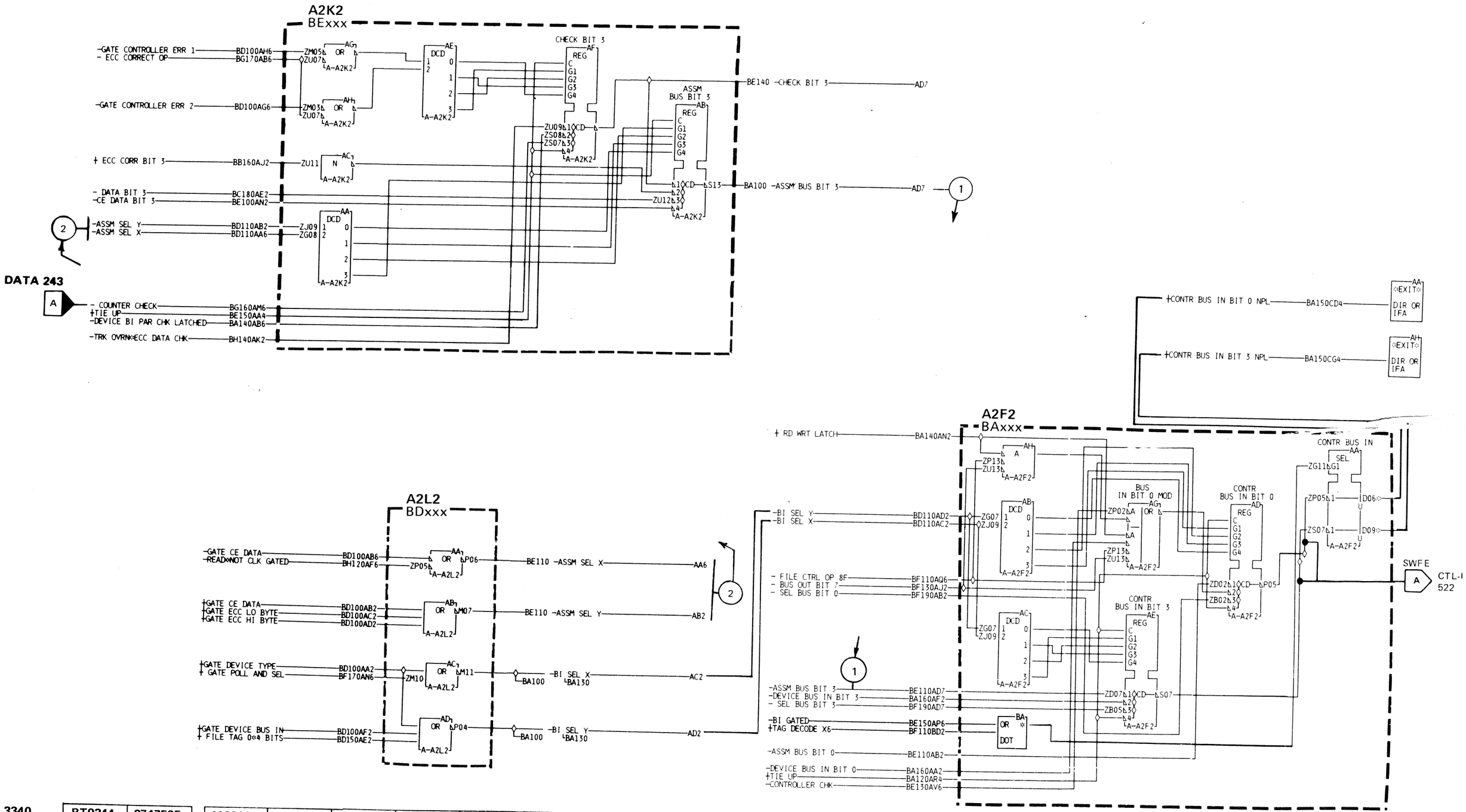




BT0241	2747564	440200	440202	440203	440218	440223	440224
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74	14 Mar 75	15 Dec 75

3340

GAP COUNTER

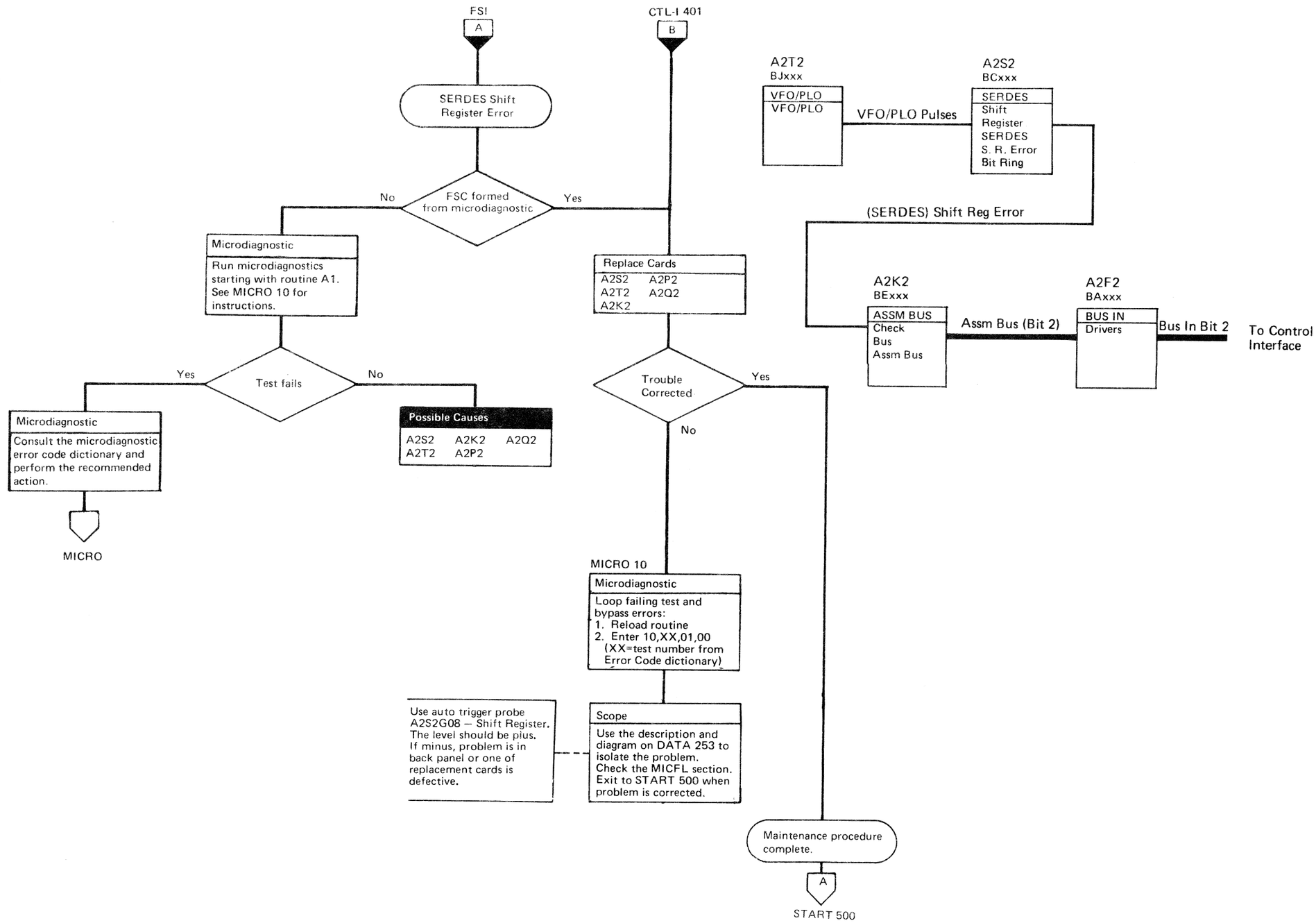


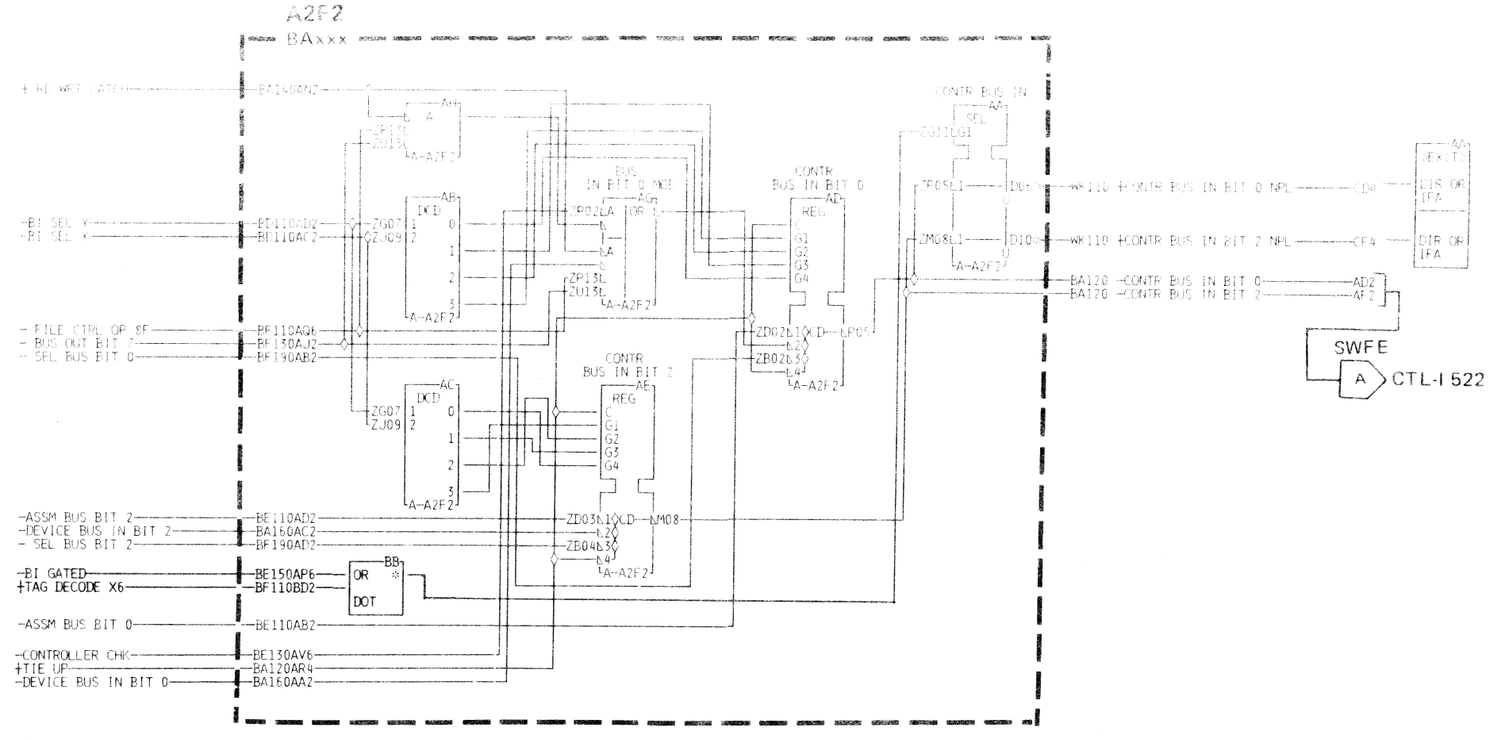
SHIFT REGISTER ERROR

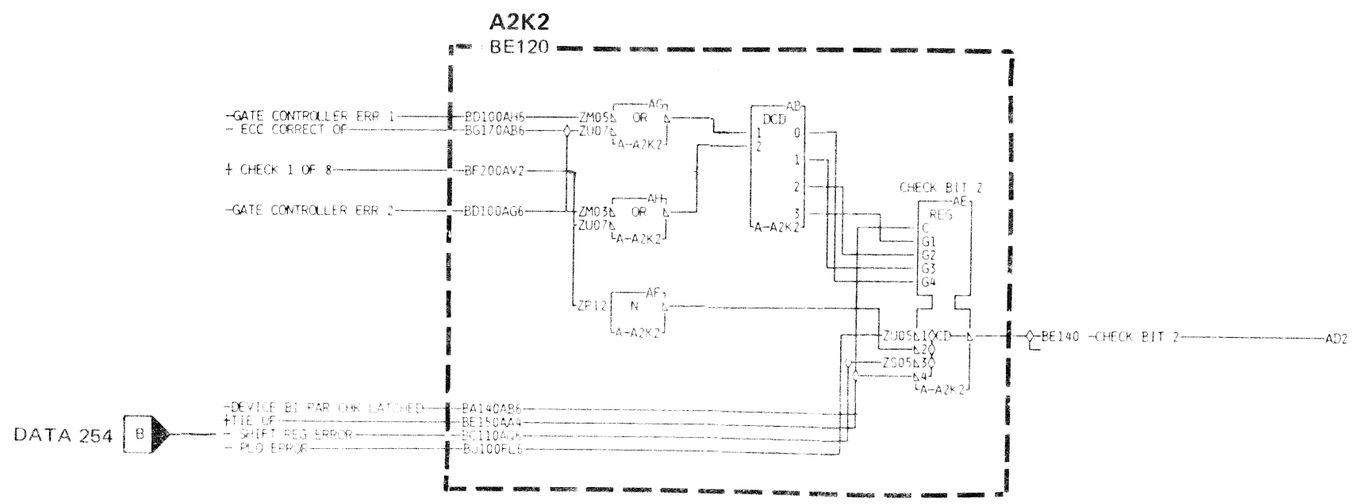
SHIFT REGISTER ERROR

Set by any Shift Register position or SERDES Parity Latch failure. Activates Controller Check and Error Alert.

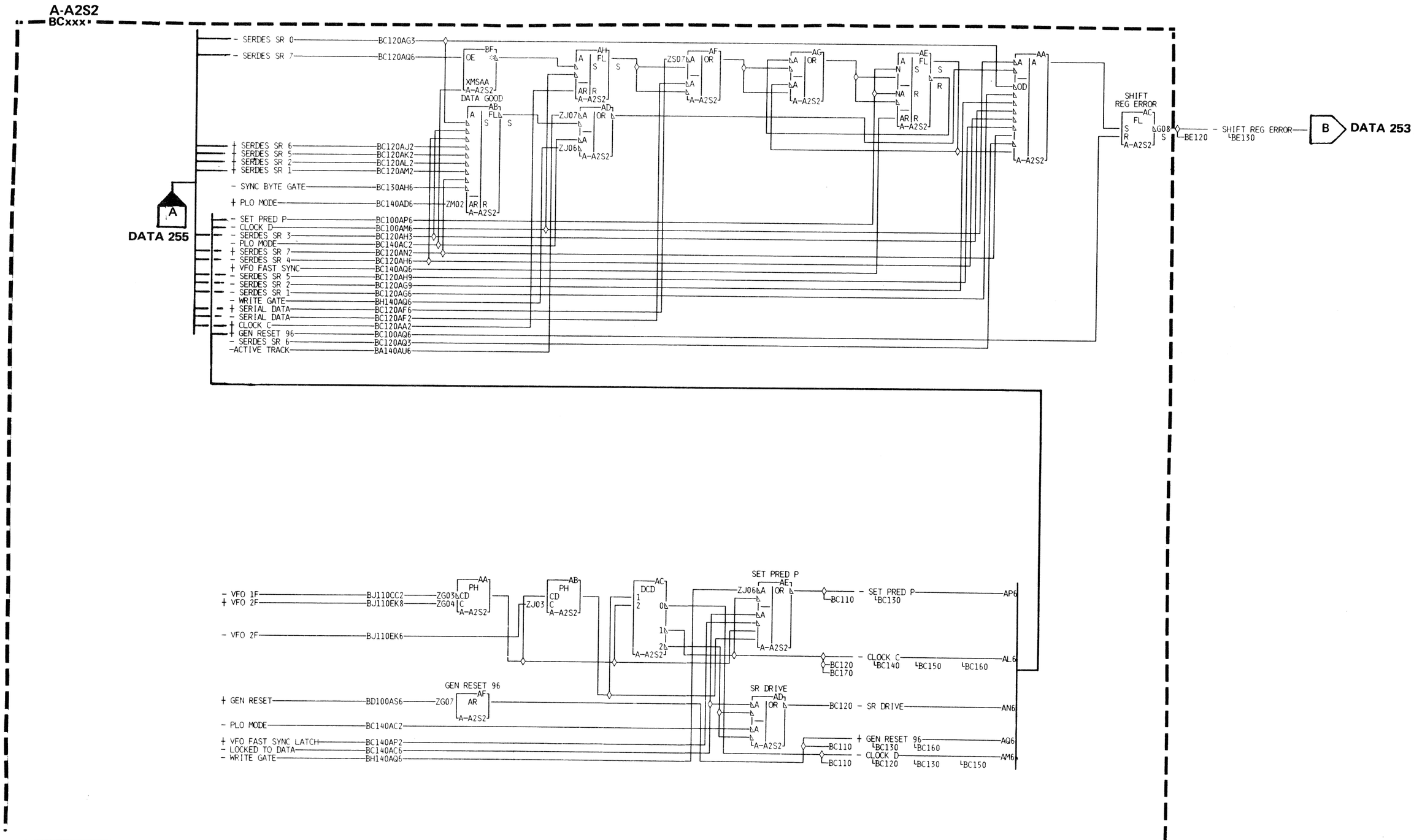
Assume that a hex '19' (0001 1001) followed by hex 0s is read. The data enters Shift Register (SR) position 0 and shifts one position each bit time. The input is also exclusive ORed with the output of SERDES SR 7 to operate the SERDES Parity latch. The SERDES Parity latch flips each time another bit enters the Shift Register unless one shifts out the end as indicated by the SERDES SR 7 line. The SERDES Shift Register outputs are fed to a parity generator to produce the line SERDES SR P. SERDES SR P and the SERDES Parity latch are compared every bit time. The failure of any Shift Register position or SERDES Parity latch turns on the SERDES SR Check latch during the cycle in which the failure occurred. SERDES Shift Register operation is dependent on the proper functioning of the bit ring. See OPER 41, 226 and 231 for bit ring theory.

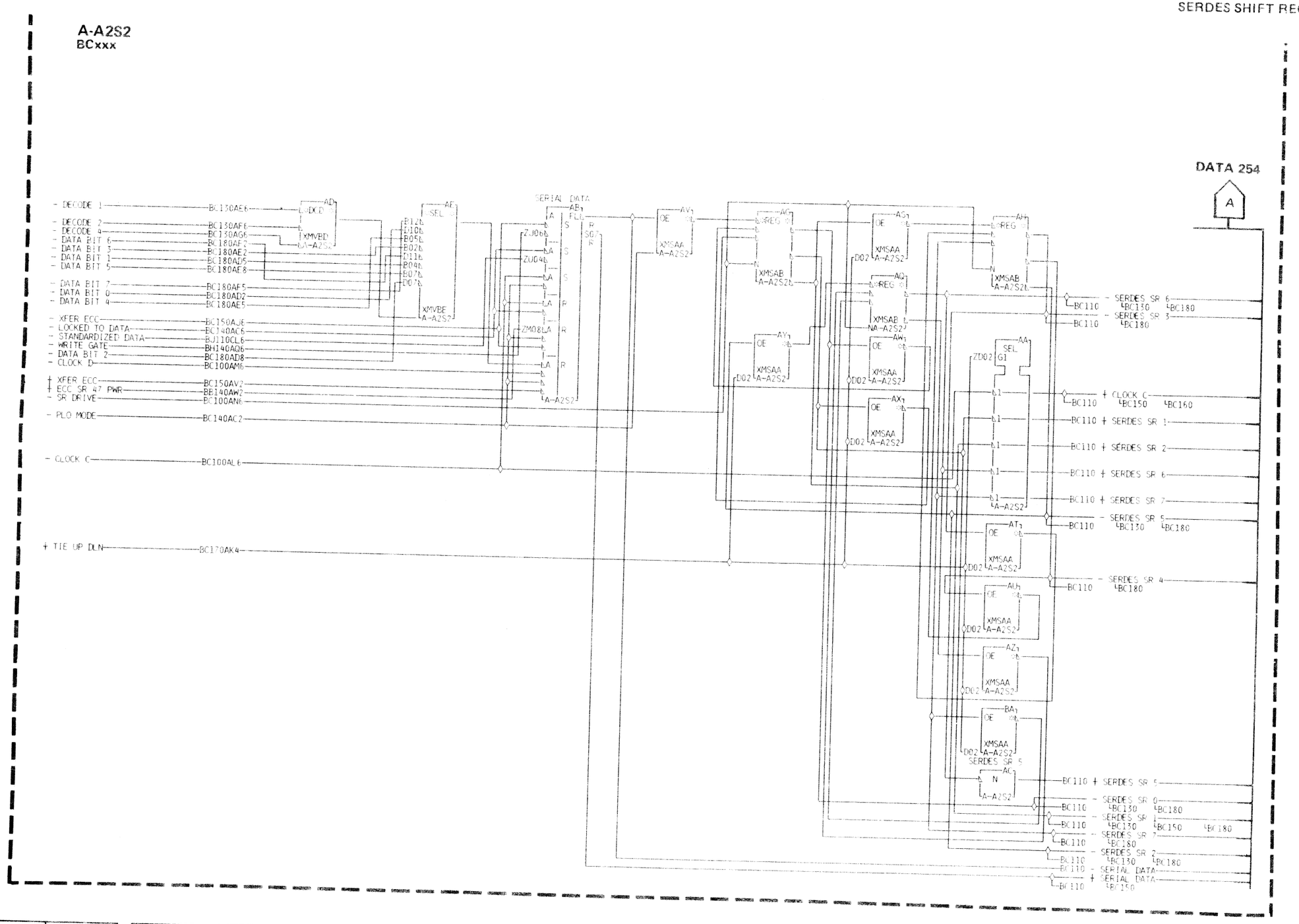






BT0250 Seq.2 of 2	2747566 Part No. (1)	See EC History	440224 15 Dec 75	440227 14 Sept 76				


A-A2S2
BCxxx
- SERDES SR 0 BC120AG3
- SERDES SR 7 BC120AQ6
+ SERDES SR 6 BC120AJ2
+ SERDES SR 5 BC120AK2
+ SERDES SR 2 BC120AL2
+ SERDES SR 1 BC120AM2
- SYNC BYTE GATE BC130AH6
+ PLO MODE BC140AD6
- SET PRED P BC100AP6
- CLOCK D BC100AM6
- SERDES SR 3 BC120AH3
- PLO MODE BC140AC2
+ SERDES SR 7 BC120AN2
- SERDES SR 4 BC120AH6
+ VFO FAST SYNC BC140AQ6
- SERDES SR 5 BC120AH9
- SERDES SR 2 BC120AG9
- SERDES SR 1 BC120AG6
- WRITE GATE BH140AQ6
+ SERIAL DATA BC120AF6
- SERIAL DATA BC120AF2
+ CLOCK C BC120AA2
+ GEN RESET 96 BC100AQ6
- SERDES SR 6 BC120AQ3
-ACTIVE TRACK BA140AU6
DATA 255
DATA GOOD
SHIFT REG ERROR
- SHIFT REG ERROR
DATA 253
- VFO 1F BJ110CC2
+ VFO 2F BJ110EK8
- VFO 2F BJ110EK6
+ GEN RESET BD100AS6
- PLO MODE BC140AC2
+ VFO FAST SYNC LATCH BC140AP2
- LOCKED TO DATA BC140AC6
- WRITE GATE BH140AQ6
GEN RESET 96
SET PRED P
SR DRIVE
- SET PRED P AP6
- CLOCK C AL6
- SR DRIVE AN6
+ GEN RESET 96 AQ6
- CLOCK D AM6

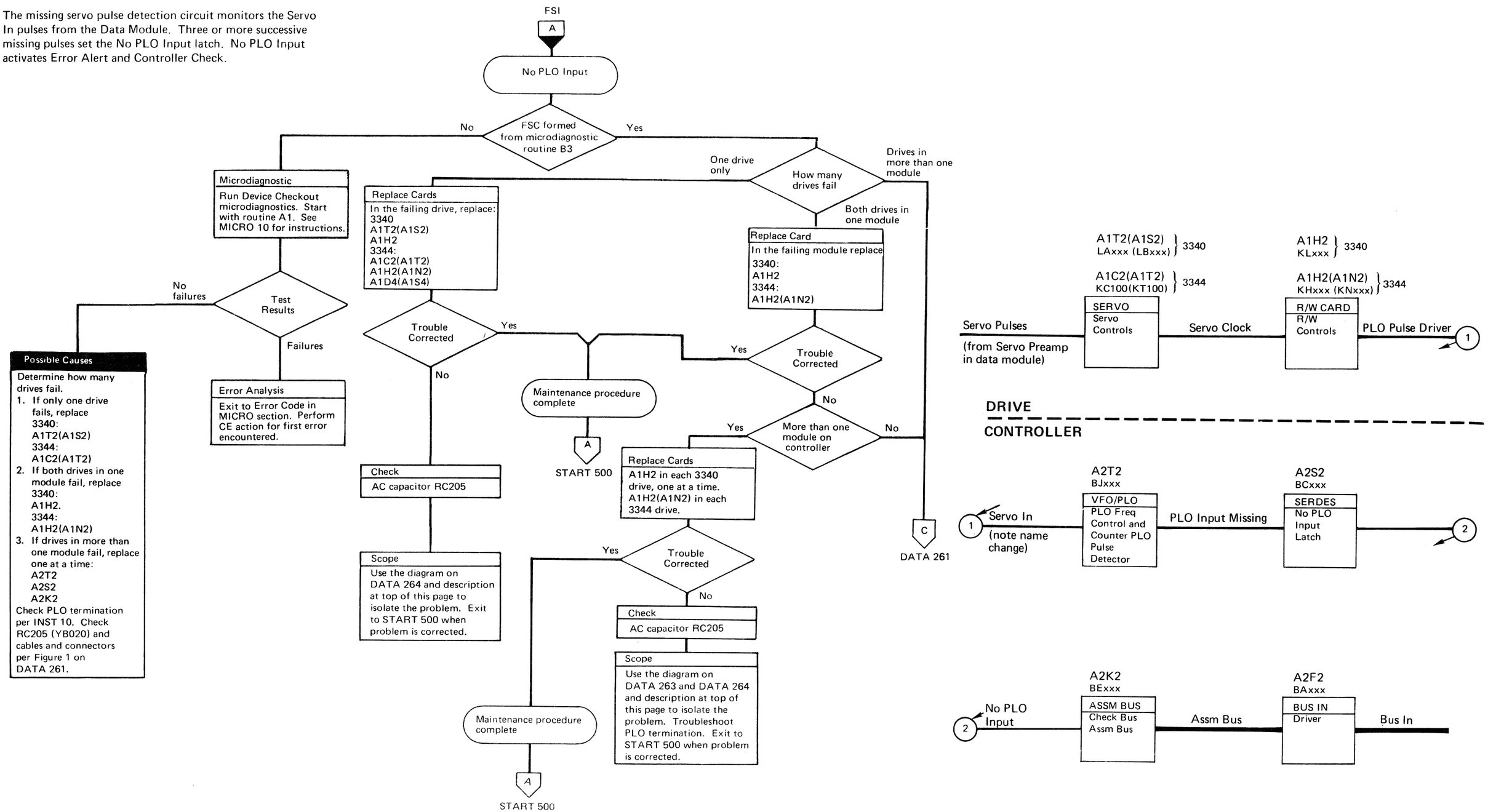


3340

BT0254 Seq.2 of 2	2747567 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73				

NO PLO INPUT

The missing servo pulse detection circuit monitors the Servo In pulses from the Data Module. Three or more successive missing pulses set the No PLO Input latch. No PLO Input activates Error Alert and Controller Check.



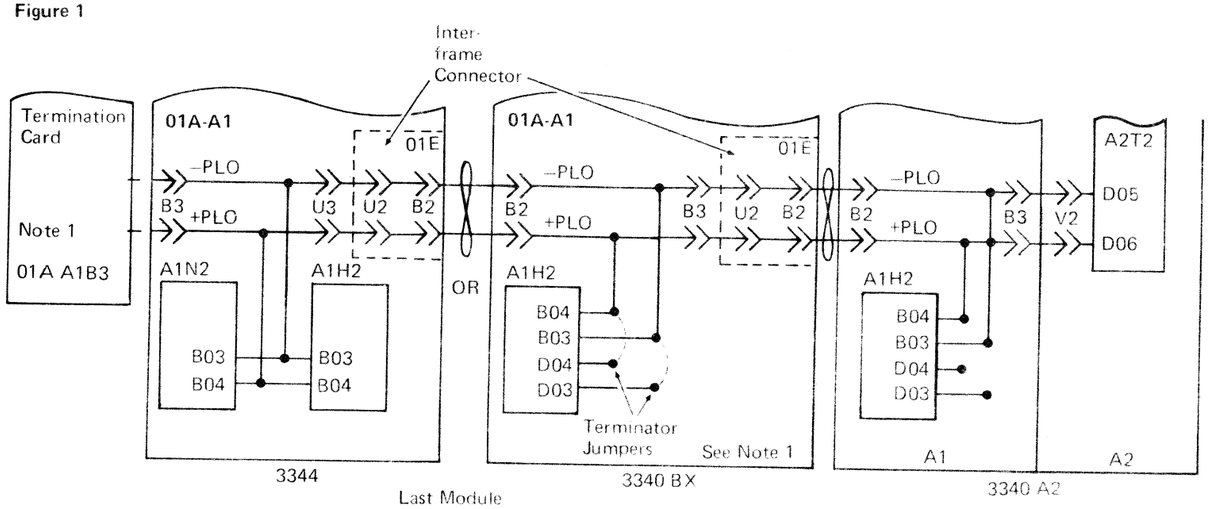
PLO

Servo pulses from the data module are used to control seeking, track following, write, and clocking functions. The Servo pulses are recorded at prescribed intervals and are used to regulate the frequency of the Phase Lock Oscillator (PLO) to the speed of the disk.

Missing servo pulses would result in a change of frequency of the oscillator. Therefore, a circuit has been incorporated to detect missing servo pulses at critical times.

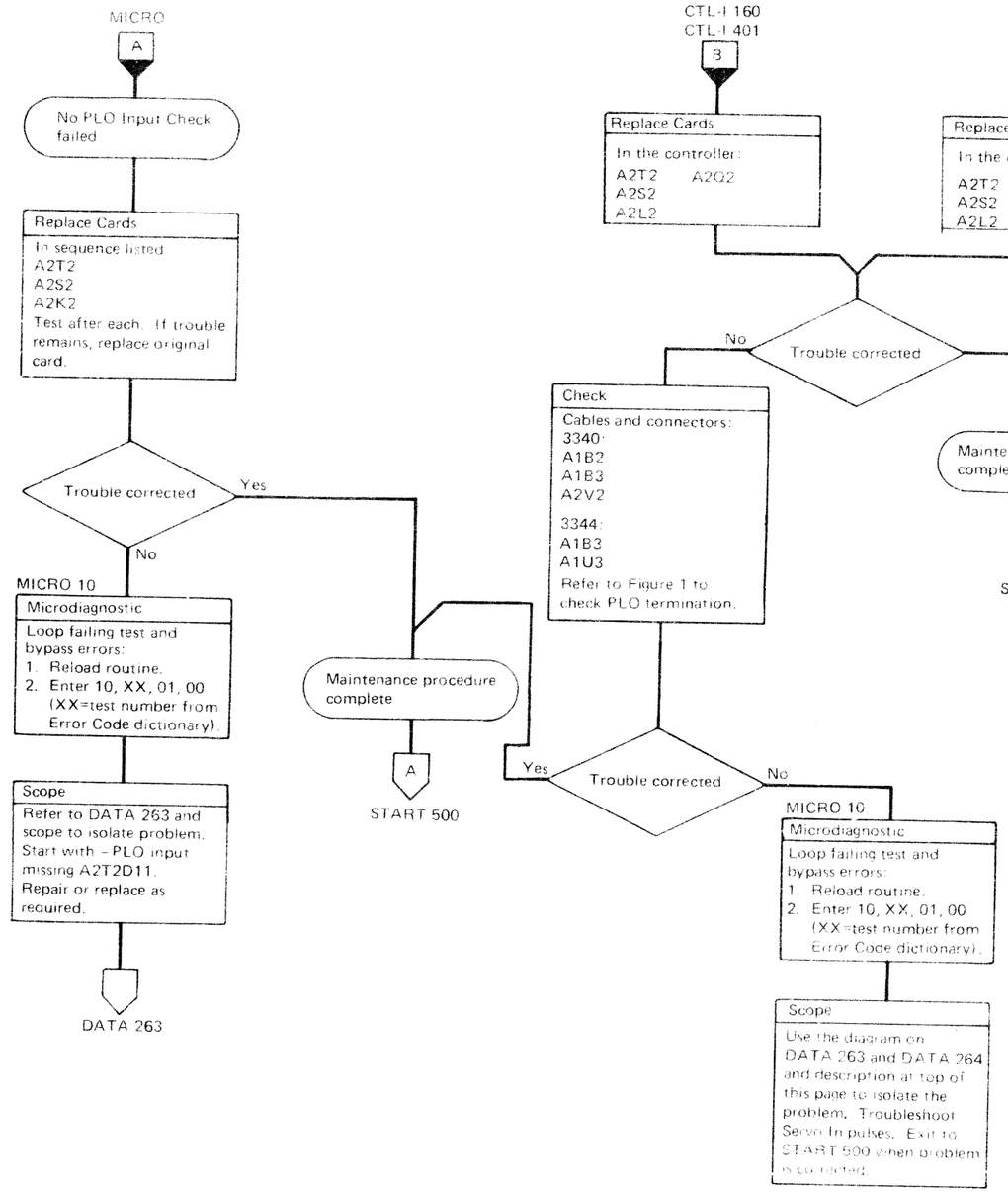
The output of the oscillator (PLO 1F pulses) operates a binary counter (2, 4, 8, 16). Each Count 16 attempts to set or step the three position Missing Servo Pulse Detector triggers. A servo pulse resets the triggers. A missing servo pulse allows the triggers to step. Three successive missing servo pulses causes the No PLO Input Check latch to be set.

Figure 1

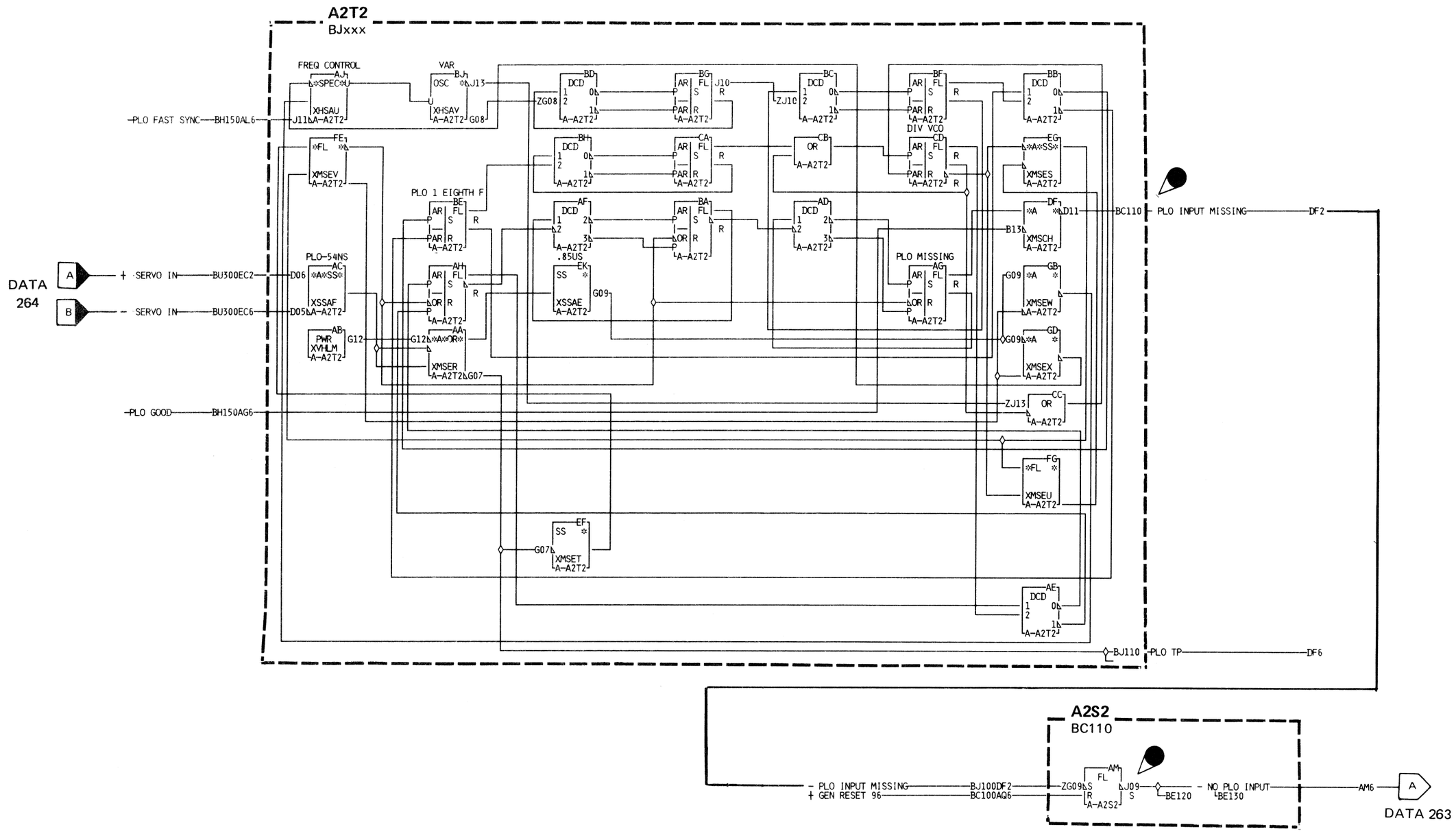


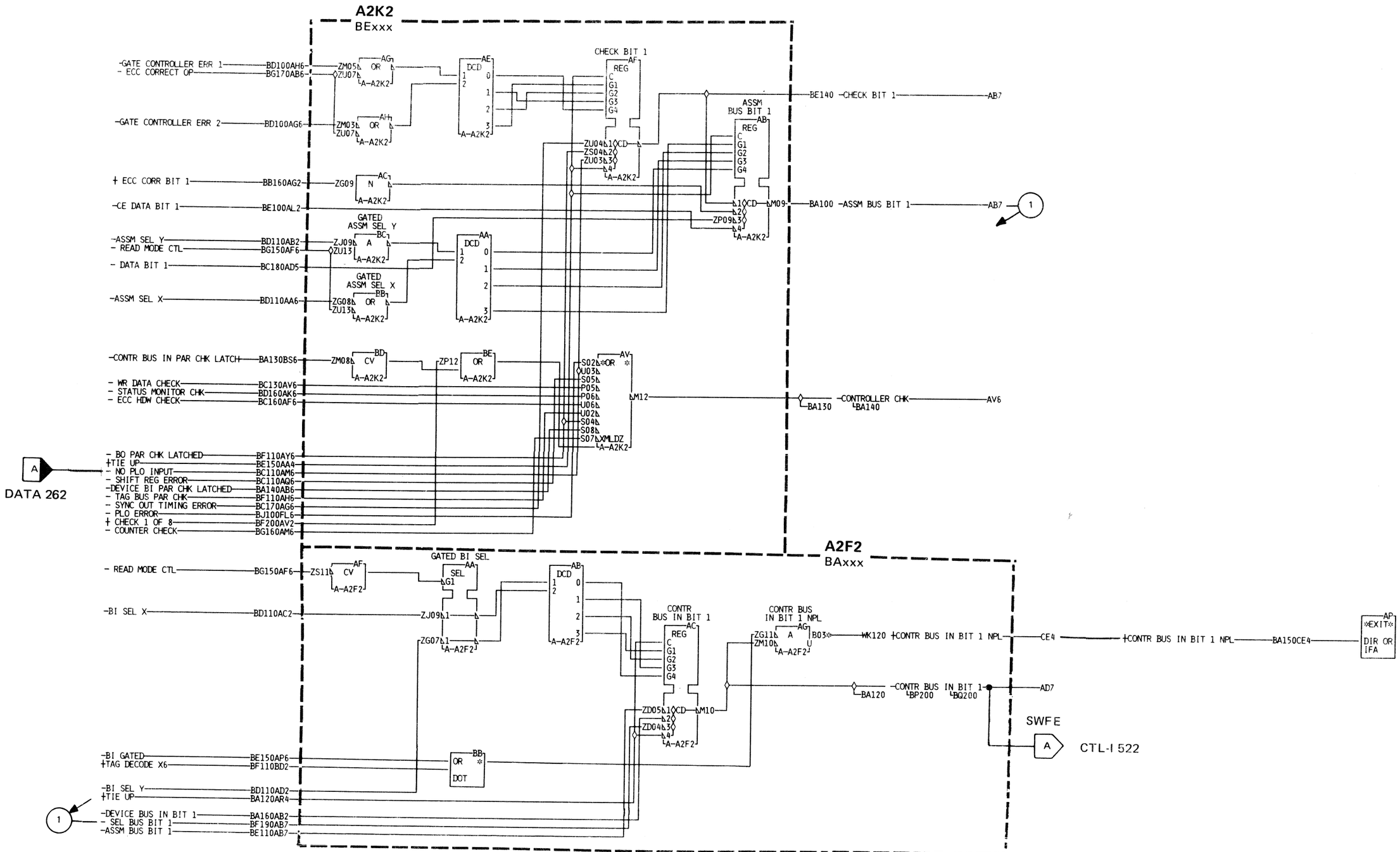
Note 1: If the last module in the string is a 3340, terminate PLO with jumpers as shown in Figure 1.

If the last module in the string is a 3344, use terminator card in card location 01A-A1B3 and remove any PLO terminator jumpers on previous modules.



BT0260	2747568	440200	440202	440203	440209	440224	440227
Seq. 2 of 2	Part No. (1)	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	15 Dec 75	14 Sept 76

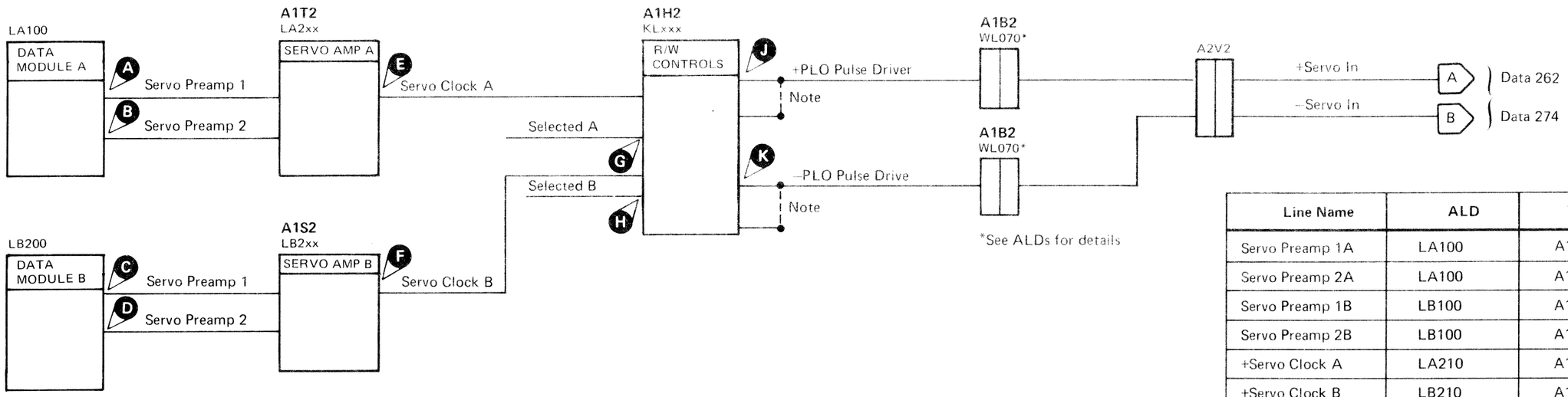

A2T2
BJxxx
FREQ CONTROL
VAR
PLO FAST SYNC
BH150AL6
PLO 1 EIGHTH F
PLO-54NS
DIV VCO
PLO MISSING
DATA 264
SERVO IN
BU300EC2
BU300EC6
PLO GOOD
BH150AG6
PLO INPUT MISSING
DF2
BC110
PLO TP
DF6
A2S2
BC110
PLO INPUT MISSING
GEN RESET 96
BJ100DF2
BC100AQ6
NO PLO INPUT
AM6
DATA 263



3340

BT0263	2747569	440200	440203	440204	440209			
Seq. 2 of 2	Part No.( )	25 Jun 73	11 Nov 73	21 Dec 73	25 Mar 74			

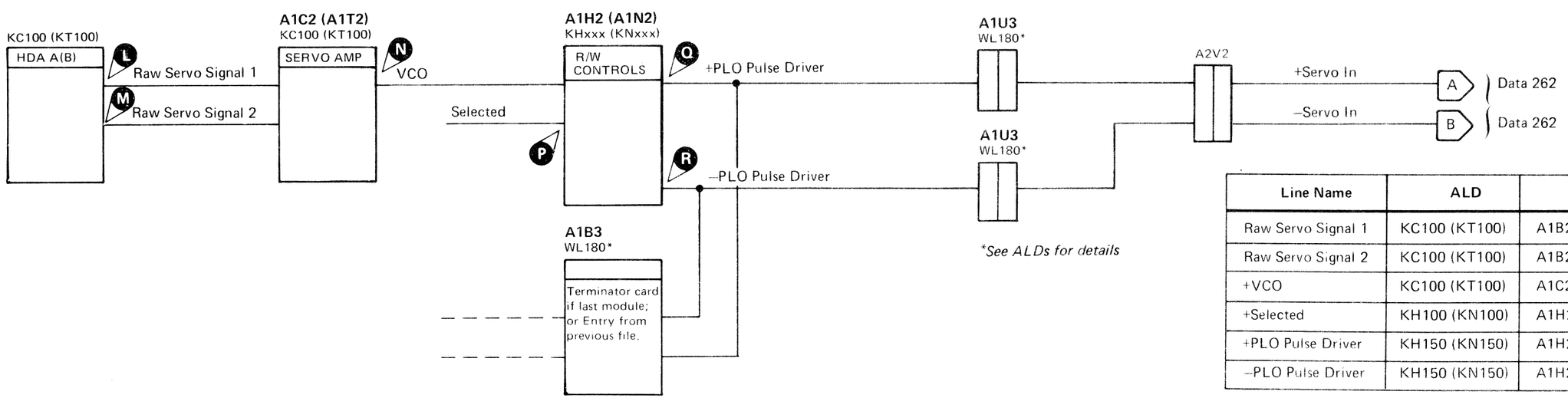
3340



Note: Terminator jumpers on last module. If 3340, see below for terminator if last module is 3344.

Line Name	ALD	Test Point	
Servo Preamp 1A	LA100	A1V2 D13	A
Servo Preamp 2A	LA100	A1V2 D09	B
Servo Preamp 1B	LB100	A1U2 D13	C
Servo Preamp 2B	LB100	A1U2 D09	D
+Servo Clock A	LA210	A1T2 J11	E
+Servo Clock B	LB210	A1S2 J11	F
+Selected A	KL010	A1H2 D10	G
+Selected B	KL010	A1H2 B07	H
+PLO Pulse Driver	KL080	A1H2 B04	J
–PLO Pulse Driver	KL080	A1H2 B03	K

3344



Line Name	ALD	Test Point	
Raw Servo Signal 1	KC100 (KT100)	A1B2(A1U2)B12	L
Raw Servo Signal 2	KC100 (KT100)	A1B2(A1U2)D12	M
+VCO	KC100 (KT100)	A1C2(A1T2)D04	N
+Selected	KH100 (KN100)	A1H2(A1N2)M05	P
+PLO Pulse Driver	KH150 (KN150)	A1H2(A1N2)B03	Q
–PLO Pulse Driver	KH150 (KN150)	A1H2(A1N2)B04	R

PLO CHECK

The PLO error indicates that two successive PLO pulses were out of phase with the VFO oscillator on a Write operation.

PLO single frequency pulses are used as input to the VFO at all times except during Read-type operations. VFO pulses operate a counter to generate 1/2, 1/4, 1/8, and 1/16 frequency pulses. The 1/16 Frequency Counter off becomes a window during which the next Servo (–PLO) pulses must fall. If the PLO pulse is late, the PLO Late latch sets and prevents the set of the Late Reset latch. The PLO Late latch also flips the 1st Late latch for the first late pulse. The 2nd Late latch is reset on so that the second consecutive PLO pulse that is late:

- Sets PLO Latch
- Flips 1st Late Latch
- Flips 2nd Late Latch
- Makes the AND to set PLO Error.

VFO Fast Sync sets the VFO 1F latch on and resets the 1/4, 1/8, and 1/16 th latches off to initialize the check circuits. It also prevents a PLO Check during the sync period.

Figure 1

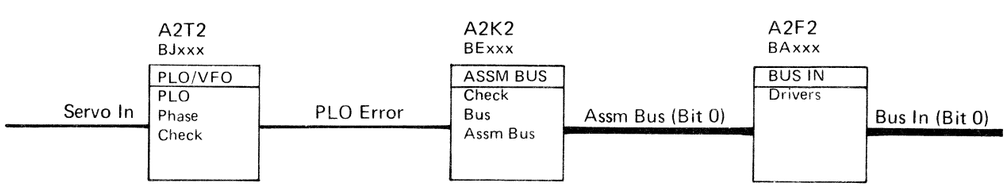
3340

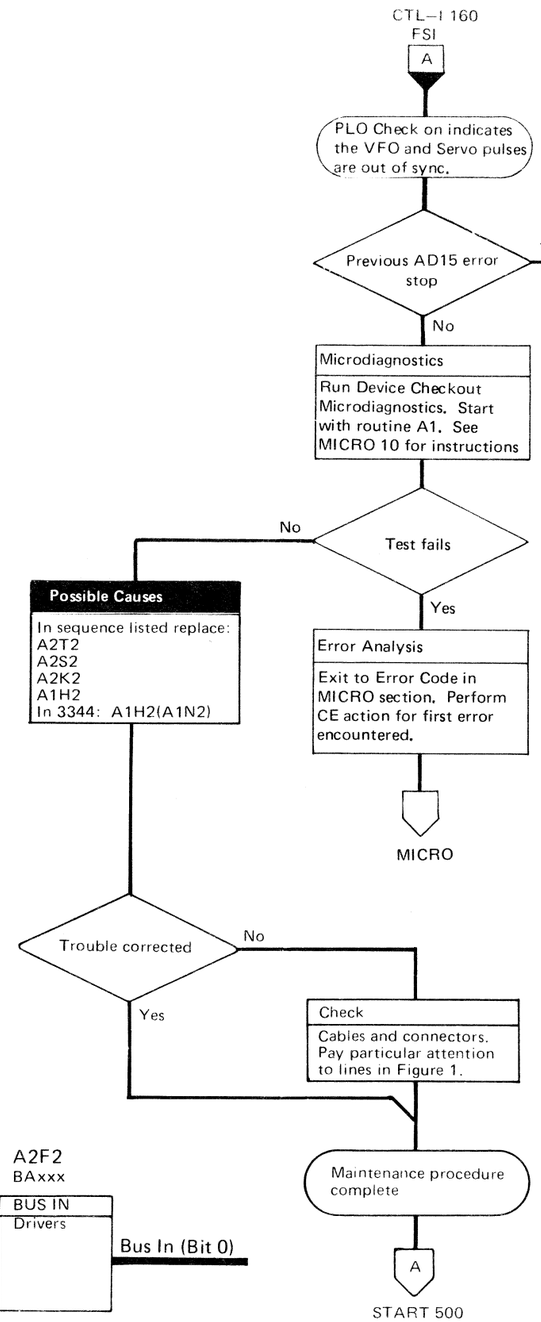
Name	01A		01E*	01A
–PLO Pulse Driver	A1B3 D02	A1B2 D02	A1U2/A1B2	A2V2 D02
+PLO Pulse Driver	A1B3 D03	A1B2 D03	A1U2/A1B2	A2V2 D03

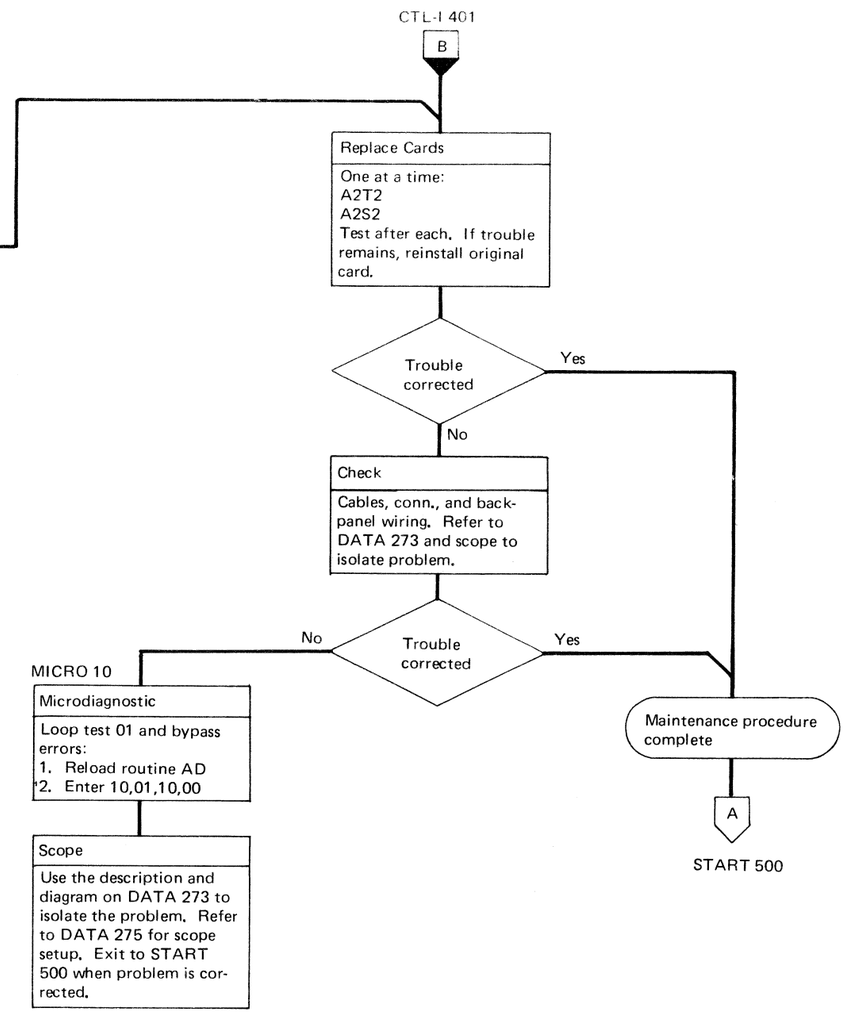
3344

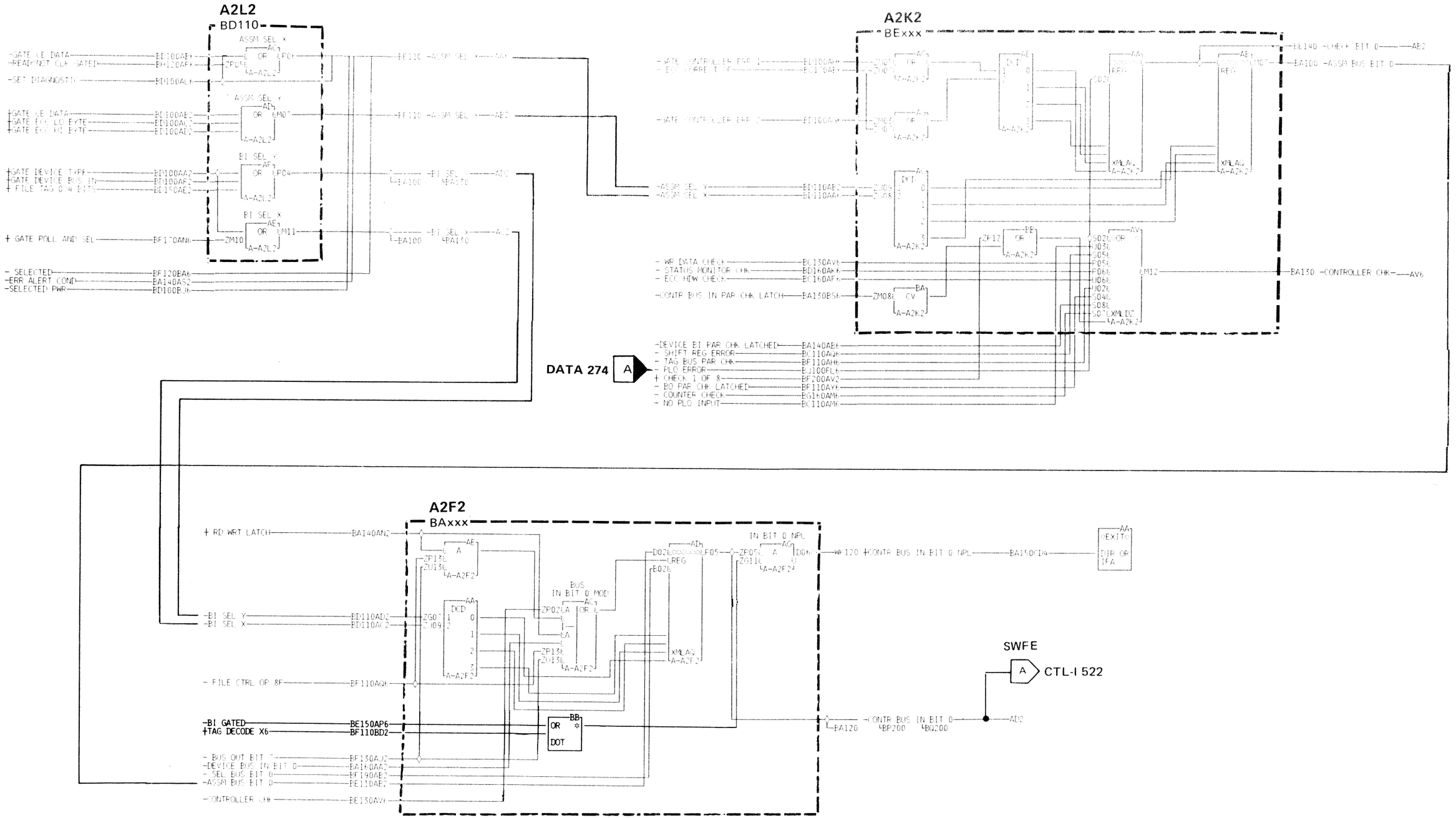
Name	01A		01E*	
–PLO Pulse Driver	A1B3 D02	A1U3 D02	A1U2/A1B2	To next 3340 or 3344
+PLO Pulse Driver	A1B3 D03	A1U3 D03	A1U2/A1B2	

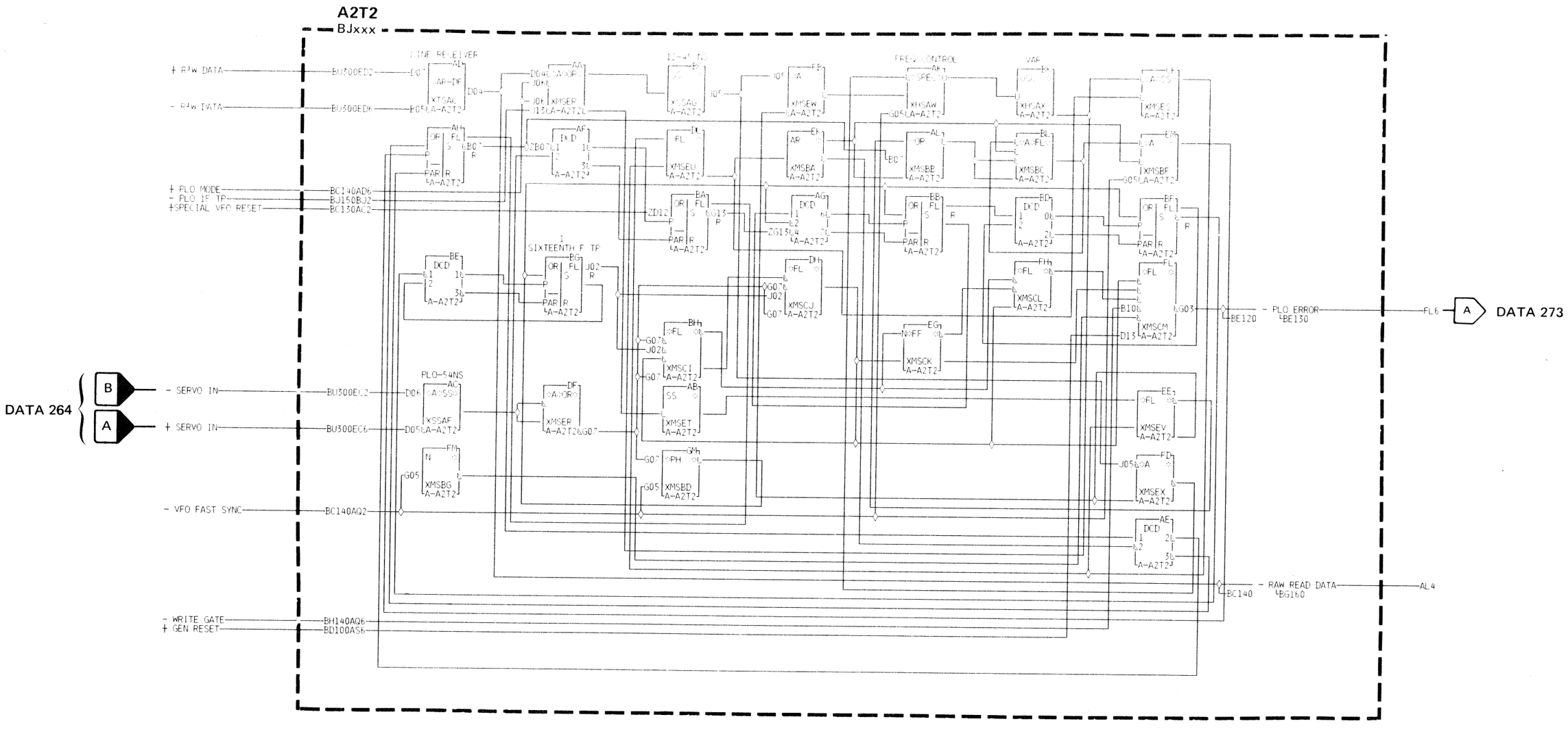
*Frame to frame connector (optional on 3340).










A2T2
BJxxx
+ RJW DATA
- RJW DATA
+ PLO MODE
- PLO IF TP
+SPECIAL VFO RESET
- SERVO IN
+ SERVO IN
- VFO FAST SYNC
- WRITE GATE
+ GEN RESET
DATA 264
B
A
- PLO ERROR
- RAW READ DATA
DATA 273
LINE RECEIVER
SIXTEENTH F TP
PLO-54NS
FREQ CONTROL
VAF

The accompanying photo shows the relationship between the '1 sixteenth F' pulses and the PLO pulses. If the PLO pulse should shift into the minus '1 sixteenth F' pulse area for three consecutive pulses the PLO Check Latch would be set.

Sync: Internal on –PLO TP A2T2G07

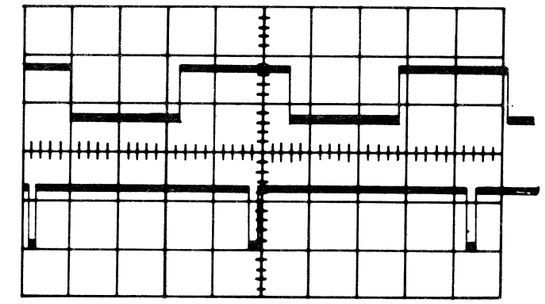
Time: 0.5 μs/div

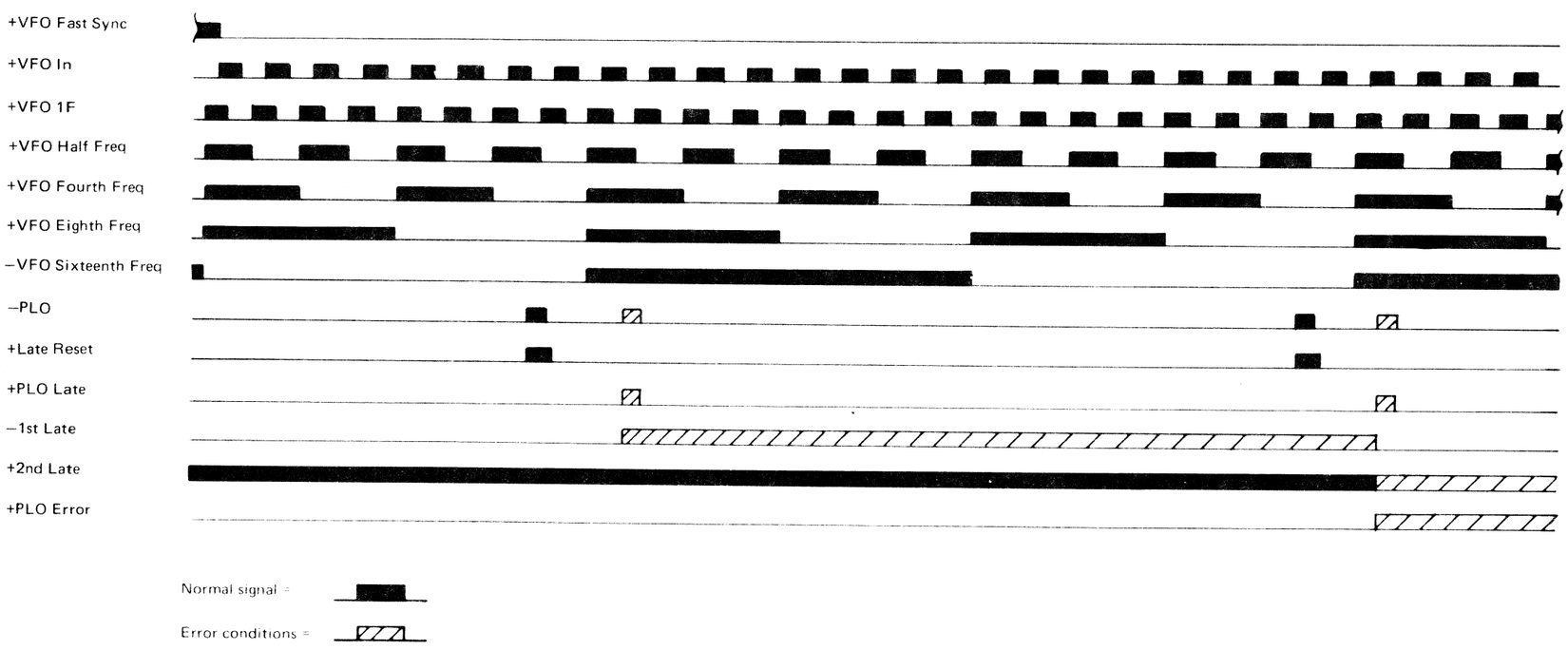
Vertical: 0.1 volt/div X10 probes

Loop Routine AD Test 1

–1 Sixteenth F A2T2J02

– PLO TP A2T2G07





BT0274	2747571	440200	440202	440203	440209	440227		
Seq. 2 of 2	Part No. (M)	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	14 Sept 76		