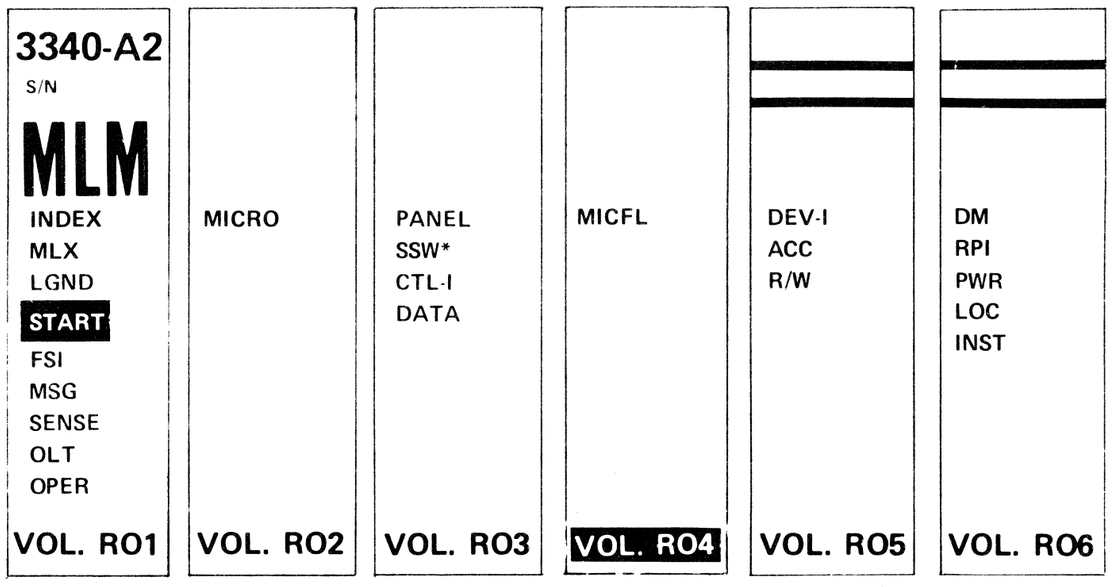
IBM Maintenance Library

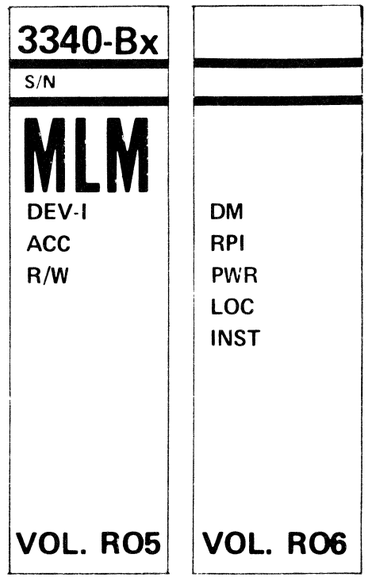
CONTROL MODULE



Volumes R01, 2, 3, and 4 accompany only Control Modules (A2).

** This section is only with Control Modules that have the string switch feature installed.*

SATELLITE MODULE



Volumes RO5 and RO6 accompany every Control Module (A2) and every Satellite Module (B1 or B2). (One set per serial numbered frame.) To ensure proper documentation level, use the volume that goes with the module you are working on.

3340 Disk Storage

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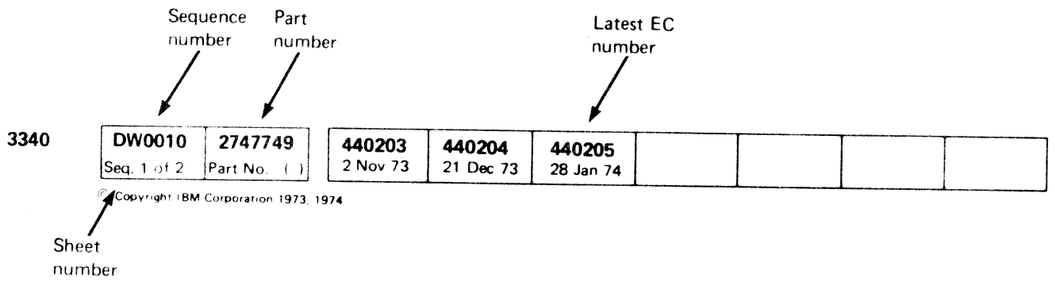
PREFACE

MAINTENANCE LIBRARY ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3340 Maintenance Library can be ordered from the San Jose plant by using the *Wiring Diagram/Logic Page Request* (Order No. 120-1679). In the columns headed "Logic Page", enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

Example:



This manual was prepared by the IBM General Products Division, Product Publications, Department G24, San Jose, California 95193.

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3340

BZ0010	2747524	440200	440203	440218	440224			
Seq. 2 of 2	Part No. ( )	25 Jun 73	2 Nov 73	5 Aug 74	15 Dec 75			

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CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment.

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. **REMEMBER – THEY ARE YOUR EYES.**
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it, for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment – eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)

2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

MICFL CONTENTS

Microdiagnostic Overview – – – – – MICFL 3

Defines the microdiagnostic philosophy, how the microdiagnostics are used, and the routines that may be linked together to appear as a single routine.

Microdiagnostic Flowchart Legend – – MICFL 5

General Routines – – – – – – – – – – MICFL 10–20

Common routines used by all flowcharts

Microdiagnostic Flowcharts – – – – – MICFL 25–1510

Grouped by routine. Each group contains a routine description, the microdiagnostic flowcharts in test number order, and scope pictures and/or routine timing diagrams.

Routine Descriptions

A0 – – – – – – – – – – MICFL 25
A1 – – – – – – – – – – MICFL 40
A2 – – – – – – – – – – MICFL 100
A3 – – – – – – – – – – MICFL 200
A4 – – – – – – – – – – MICFL 300
A5 – – – – – – – – – – MICFL 450
A6 – – – – – – – – – – MICFL 525
A7 – – – – – – – – – – MICFL 600
A8 – – – – – – – – – – MICFL 650
A9 – – – – – – – – – – MICFL 720
AA – – – – – – – – – – MICFL 750
AB – – – – – – – – – – MICFL 790
AC – – – – – – – – – – MICFL 815
AD – – – – – – – – – – MICFL 900
AE – – – – – – – – – – MICFL 1000
AF – – – – – – – – – – MICFL 1100
B0 – – – – – – – – – – MICFL 1230
B1 – – – – – – – – – – MICFL 1250
B2 – – – – – – – – – – MICFL 1299
B3 – – – – – – – – – – MICFL 1350
B4 – – – – – – – – – – MICFL 1400
B7 – – – – – – – – – – MICFL 1475
CTL-I Bringup Prog – – – – MICFL 1500

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3340 MICRODIAGNOSTIC OVERVIEW

PHILOSOPHY

Purpose of Microdiagnostics:

The microdiagnostic package is designed to aid the CE in maintaining the 3340 Disk Storage Controller and Drive. This package can be used in the following ways:

- FRU List

  The number of possible field replaceable units (FRUs) can be greatly reduced by a microdiagnostic that re-creates the failing condition.

- Degraded Performance

  The microdiagnostic package resolves failures in hard ware that create a degraded product performance; for example, excessive seek errors in a particular drive.

- Adjustments

  Adjustments in the servo area can be verified with microdiagnostics. The velocity gain can be adjusted entirely with a microdiagnostic, eliminating the need for a scope.

- Verification of Repair Action

  The microdiagnostic package can be used to check out the 3340 Controller and Drive after repair. This ensures a correct repair before returning the machine to the customer.

Building Block Concept

The Building Block concept tests the hardware in a logical, orderly, progressive sequence starting with the controller interface and working progressively toward the most complex areas of the machine. This type of testing first proves that a complete path from the attachment through the device is operative before attempting to test the more complex functions of the machine. This achieves a high degree of confidence in the information received in further testing of a variety of increasingly complex operations.

DEPENDENCIES

Hardcore

The hardcore of any system or subsystem is defined as the minimum amount of hardware that must be operative to execute a diagnostic and analyze the results of execution with a high degree of confidence. Because of the many attachment configurations possible with the 3340, the assumption that the hardware on the attachment side of the interface is operative must be made. This hardware, a part of the hardcore, is tested by diagnostics designed for the particular attachment, for example, the 3830-2, ISC, DDA, IFA, etc. The 3340 CTL Interface consists of:

- Controller Interface Line Drivers and Receivers.
- Tag Bus and Bus Out.
- Select Hold and Tag Gate.
- Unselected Alert Line (CE Alert).
- Execute Switch and Associated Latch.
- CE Panel Switches, Registers, and Lamps.

If any of the above 3340 hardware is inoperative, it can be diagnosed from the attachment side of the interface by the CTL Interface Bringup program and its associated MAPS. To further diagnose the CE panel hardware, use Routine A0, CE panel test.

IMPLEMENTATION

Microdiagnostic Error Detection Methods.

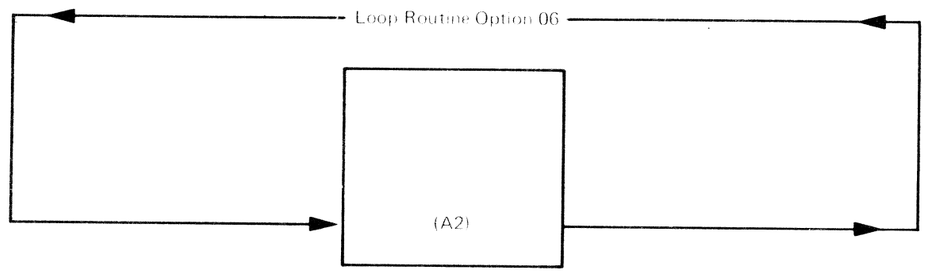
Whenever a microdiagnostic uses an error detection circuit within the building block scheme, the circuit is first checked for correct operation before using it to test the circuit, an error condition is forced on, and verified. The error is then reset and the reset condition verified before continuing the test. The microdiagnostic package detects errors in the following ways:

- An operation is performed and the data received is compared to the expected or normal data. If the received and expected data do not compare, an error is indicated.
- An event or series of events is timed with a micro program controlled timer. The actual measured time is compared to an engineering specification. If the measured time is not within the limits of the engineering specification, an error is indicated.
- An operation is performed and the resultant state of an error check is tested to verify correct or incorrect operation.

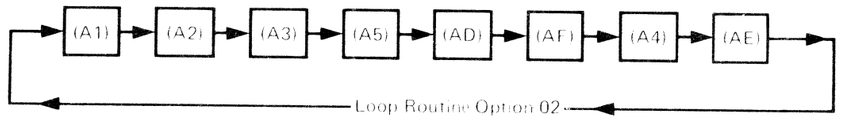
3340 Linked Series Microdiagnostics

The 3340 Building Block concept consists of 8 routines linked together to appear as a single routine. This is known as Linked Series 1. If an error in Linked Series 1 indicates a problem in the servo area, the CE is instructed to run Linked Series 2. Linked Series 2 consists of 2 routines linked together to appear as a single routine. Linked Series 1 and 2 are illustrated below.

Linked Series 1 With Loop Options

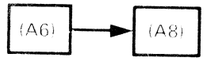


Note: Option 06 inhibits linking to Routine A3 and continues to loop Routine A2 until stopped by an error or by the run control option 00.



Note: Loop routine Option 02 starts with Routine A1 and links to A2, A2 to A3, etc. Until AE is completed. Routine AE now links back to A1 and this process continues until stopped by detection of an error or run control option 00.

Linked Series 2



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MICRODIAGNOSTIC FLOWCHART LEGEND

SYMBOL	DESCRIPTION
DECREMENT COUNT BY (XX)	PROGRAM PROCESS
S2 ← SELECT CONTROLLER / TAG'03'_BUS'XX' (CC101AK2)	TAG SEQUENCE TAG AND BUS OUT VALUES ARE SHOWN ON BOTTOM LINE (IN HEX). IF BUS VALUE IS VARIABLE XX IS USED. THE SCOPE SYNC OR SCOPE TEST POINT MAY BE INDICATED BY ALD NET REFERENCE BELOW BLOCK. A BLACK CIRCLE WITH A WHITE S PLUS A NUMBER INDICATES A SYNC POINT. THAT SYNC POINT CARRIES THE SAME NUMBER WHEREVER IT APPEARS IN A PARTICULAR TEST. SCOPE POINT IS NOT ALWAYS INDICATED.
ERROR STOP DISPLAY (MICFL 20) ERROR-CODE 8ABE → ○	AN ERROR DETECTED BY THE PROGRAM IS INDICATED BY ANY ONE OF THE THREE BLOCKS AT LEFT. THE SCOPE SYNC POINT FOR LOOPING ON THE ERROR IS SHOWN IN A NOTE BLOCK APPEARING ELSEWHERE ON THE PAGE. THE NOTE BLOCK IS REFERRED TO BY A BLACK CIRCLE OR SQUARE CONTAINING THE NOTE NUMBER. THE NOTE BLOCK USUALLY APPEARS AT THE BOTTOM OF THE PAGE. IF THE BLACK SQUARE DOES NOT CONTAIN A NUMBER, THEN A CORRESPONDING NOTE OR SINK POINT DOES NOT EXIST. THE BLACK SQUARE IS USED ONLY AS A FLAG TO HELP THE READER LOCATE THE ERROR STOP BLOCK ON THE PAGE. THE POINT WHERE THE SYNC IS ISSUED CAN BE FOUND BY FOLLOWING THE FLOW CHART BACK UNTIL A BLOCK IS FOUND WITH A SYNC INDICATION. SEE SCOPE SYNC POINT DESCRIPTION BELOW. THE SUBROUTINE THAT DISPLAYS THE ERROR CODE IS DESCRIBED ON MICFL 10. GENERAL NOTES ARE IDENTIFIED WITHIN THE CIRCLE BY A NUMBER.
ERROR STOP DISPLAY (MICFL 20) ERROR-CODE 8A2E → 2	
DYNAMIC DISPLAY (MICFL 20) ERROR-CODE 8A2E → 3	
SET UP DISPLAY FOR ERROR NUMBER='XX' ERROR-CODE 8A2E/8A2F → 4	
1 ← NOTE INFORMATION GOES IN THIS BOX	
2 ← SYNC POS CTLR J2D11 +SELECT ACTIVE ALD REF CC101AK2 → S2	SCOPE SYNC POINT IS INDICATED WITH POLARITY (POS OR NEG); BOX (CTLR OR DRV); AND PIN, WITH ITS LOGIC NAME AND ALD NET.

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C01
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SYMBOL	DESCRIPTION
NO ← ERROR OCCURRED → YES	ANY DECISION SCOPE POINT MAY BE INCLUDED AS IN TAG SEQUENCE BLOCK.
INLINE CHECK (MICFL 20)	PREDEFINED PROCESS. A SUBROUTINE THAT IS DESCRIBED ELSEWHERE IN THE MICFL SECTION. THE PAGE NUMBER WITHIN OR ABOVE THE BLOCK IS WHERE THE SUBROUTINE IS DESCRIBED.
8DB A1 ↓	OFF-PAGE CONNECTOR - ENTRY CHART ID IS DESIGNATED ON FIRST LINE (8DB). ENTRY BLOCK CONNECTOR ID IS DESIGNATED ON SECOND LINE (A1).
8DB A1 ↓	OFF-PAGE CONNECTOR - EXIT 'TO' CHART ID IS DESIGNATED ON FIRST LINE (8DB). 'TO' BLOCK CONNECTOR ID IS DESIGNATED ON SECOND LINE (A1).
B2 ↓	INTERNAL PAGE CONNECTOR - EXIT THE EXIT CONNECTOR CONTAINS THE COORDINATE DESIGNATION OF THE NEXT BLOCK TO BE ENTERED. COORDINATES ARE A-K VERTICALLY AND 1 - 0 HORIZONTALLY.
B2 ↓	INTERNAL PAGE CONNECTOR - ENTRY THE ENTRY CONNECTOR CONTAINS THE COORDINATE DESIGNATION OF THE BLOCK TO BE ENTERED. THE COORDINATE CHARACTERS MUST MATCH BETWEEN THE EXIT AND ENTRY SYMBOLS TO VERIFY THE CORRECT ENTRY.
	ABBREVIATIONS MSEC = MILLISECOND USEC = MICROSECOND CTLR = CONTROLLER DRV = DRIVE '12' = SINGLE QUOTES AROUND 'A3' A NUMBER OR SERIES OF NUMBERS INDICATE A HEXADECIMAL VALUE.
	THE BLOCK TO THE RIGHT IS USED ONLY BY THE WRITER TO IDENTIFY THE PARTICULAR CHART BEFORE IT IS AFFIXED TO THE FINAL MLM PAGE. IT HAS NO MEANING IN THE FLOW DIAGRAM AND SHOULD BE IGNORED BY THE CE.

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440200	440202	440203	440205	440219	440227	
25 Jun 73	7 Sept 73	2 Nov 73	28 Jan 74	26 Sept 74	14 Sept 76	

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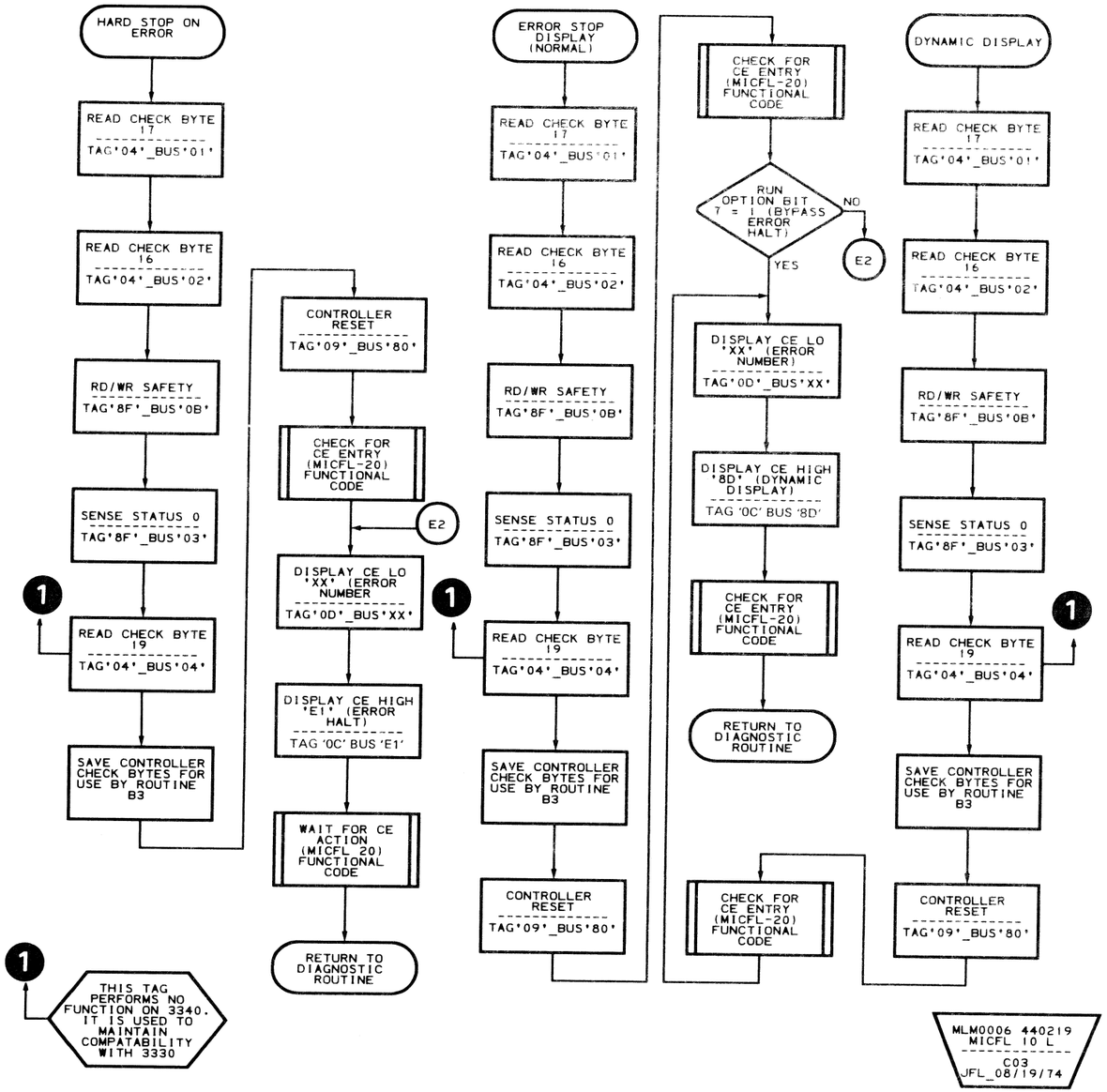

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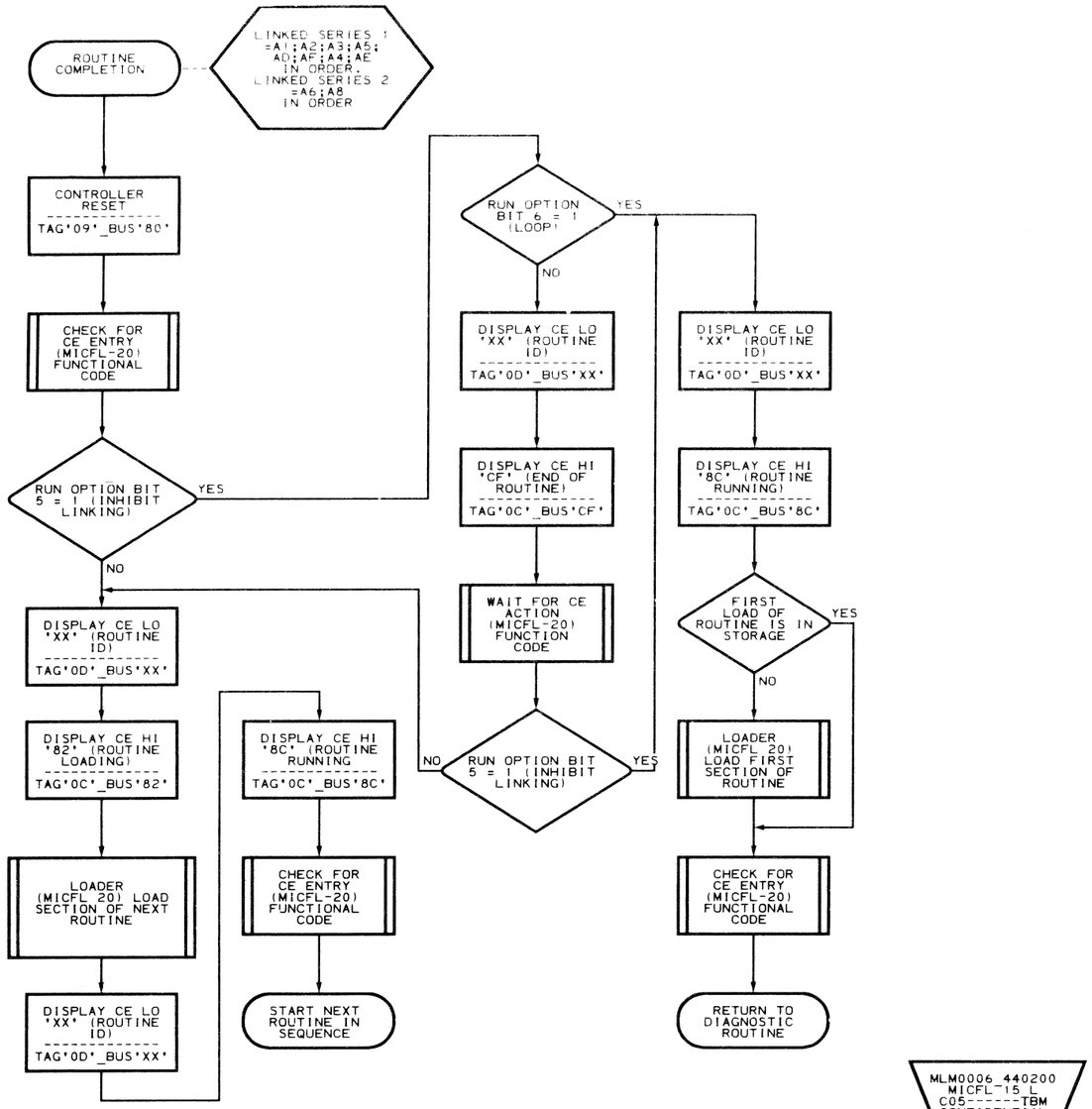

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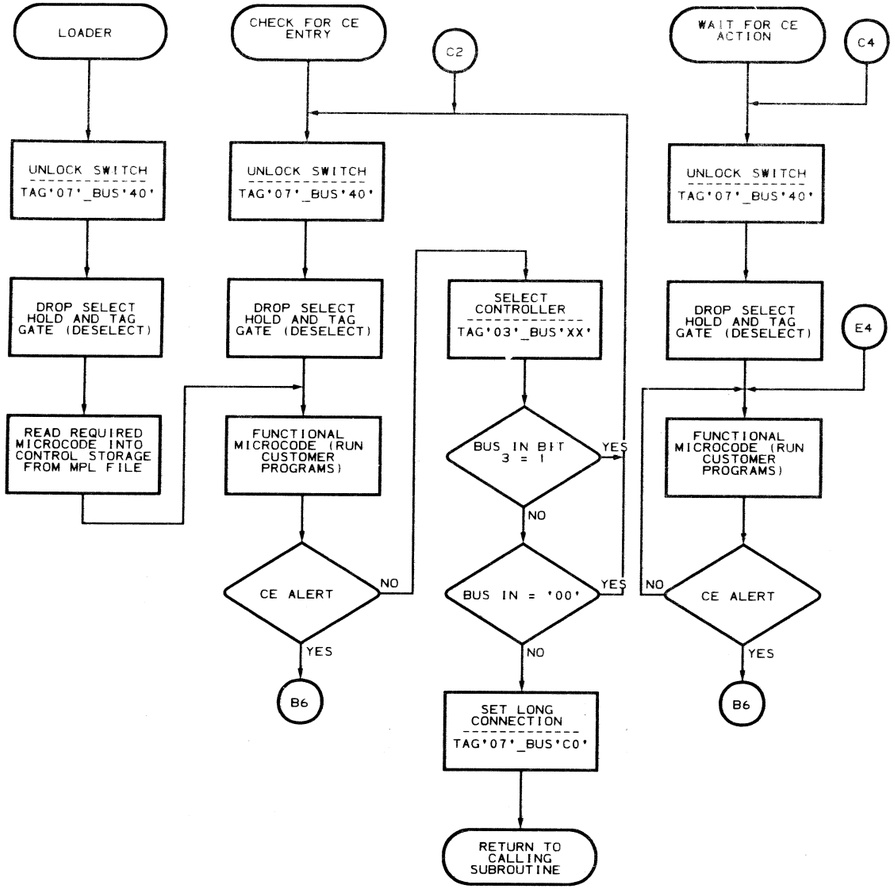
GENERAL ROUTINES



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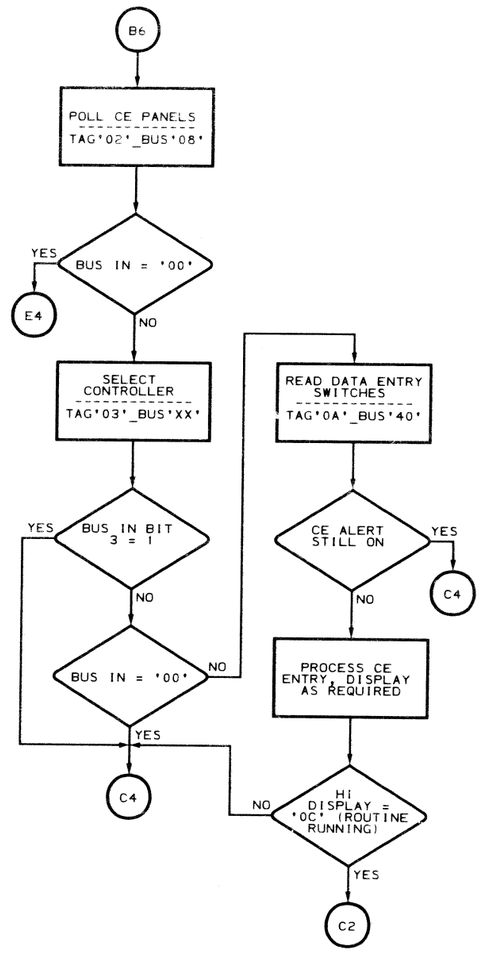

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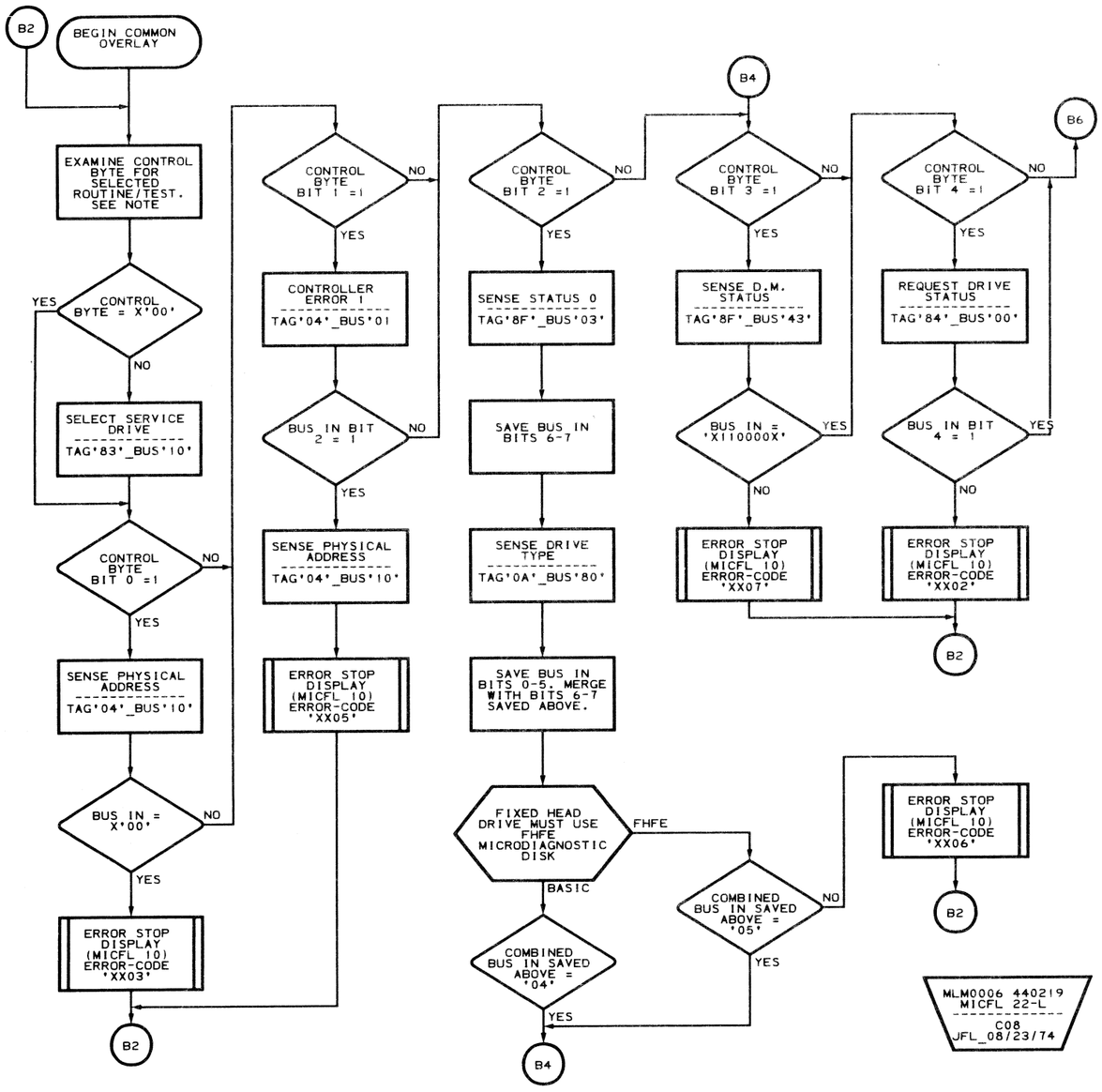
COMMON PREREQUISITE TESTS FOR ALL ROUTINES



NOTE: THE CONTROL BYTE IS A PROGRAM-DEFINED BIT-SIGNIFICANT BYTE WHICH DESCRIBES PREREQUISITES FOR EACH ROUTINE/TEST. A 1 IN ANY POSITION INDICATES THAT THE SPECIFIC PREREQUISITE TEST IS TO BE MADE. BITS ARE DEFINED AS FOLLOWS:

BIT	DESCRIPTION	ERROR NUMBER
0	PHYSICAL ADDRESS RETURNED	03
1	MULTISELECTION	05
2	DRIVE TYPE/FEATURE COMPATABILITY	06
3	DM SEQUENCE COMPLETE	07
4	ON LINE	02
5	READ ONLY	04
6	NOT USED	--
7	NOT USED	--

CONTROL BYTE DEFINITION BY ROUTINE/TEST NUMBER

ROUTINE	TEST	BITS 0123 4567
A0,A1	ALL	0000 0000
A2	1,4	0000 0000
	2,3,5 TO 11	1100 0000
A3	1,5,6,7	1110 0000
	2,3	1111 0000
	4	1111 1000
	8	1110 1000
A4	ALL	1111 1000
A5	ALL	1110 1000
A6,A7,A8	ALL	1111 0000
A9,AA,AB	ALL	1110 1000
AC	ALL	1110 0000
AD,AE,AF,B0	ALL	1110 1100
B1	ALL	1110 1000
B2	ALL	1110 1100
B3,B4	ALL	1110 0000
B6	ALL	1110 1100
B7	ALL	1110 0000

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ROUTINE A0 – CE PANEL TEST

DESCRIPTION

The purpose of Routine A0 is to test the CE panel hardware. The hardware to be tested consists of the Data Entry switches, the Program Control and Data Display lamps, and their associated registers. Prompting is used in this test by displaying the received and next-expected switch values simultaneously. This is done by displaying the switch value just read in the Data Display lamps, and by incrementing this value by 1 and displaying the next-expected value in the Program Control lamps. The Prompting continues throughout the test until each and every position of both Data Entry switches has been tested. The program ends execution when the Data Entry switches complete the entire sequence, which is the time when the switches are set from '0F' to '00'. The program can be restarted at any time by using the '00' run control option.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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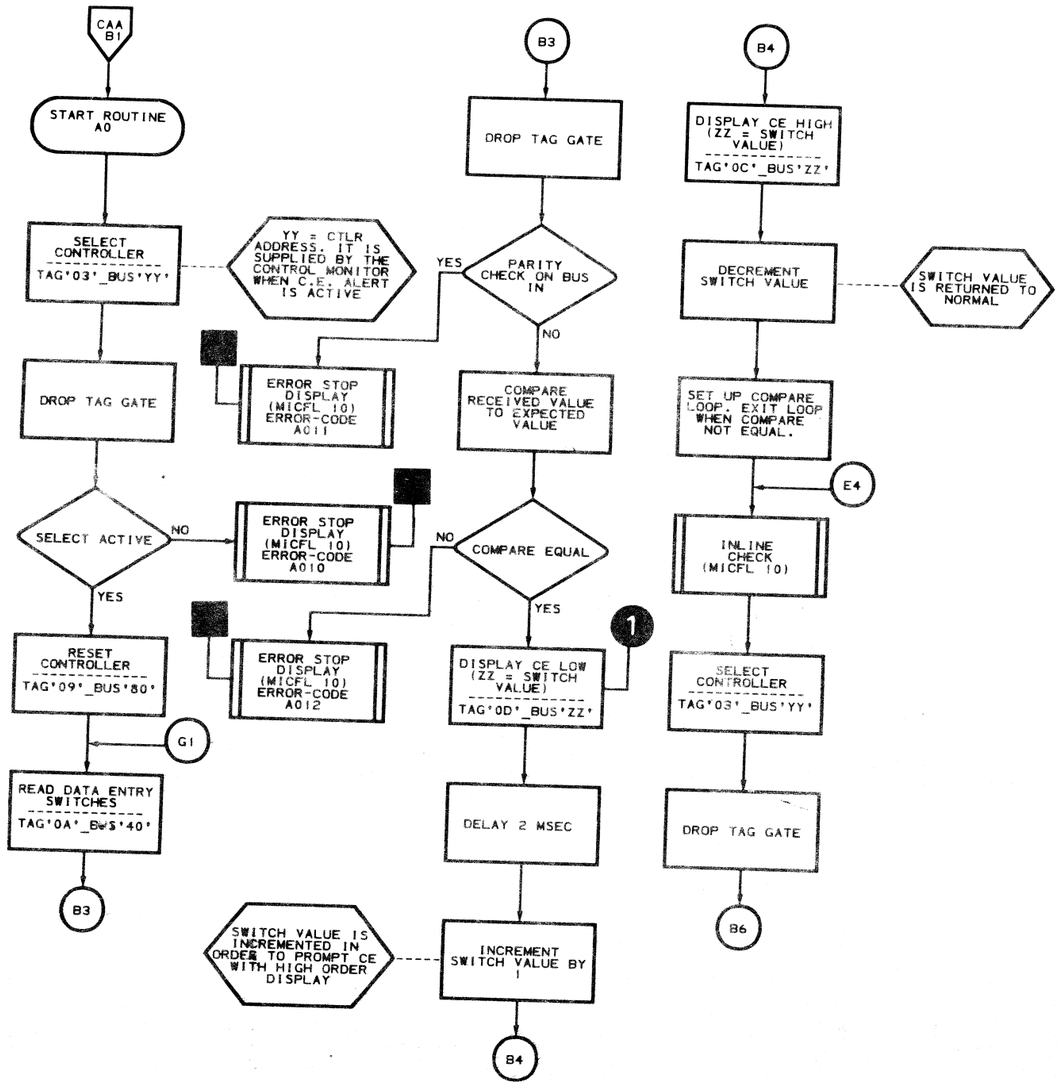
ROUTINE A0



CA0030	2747032	440200	440202	440203	440214			
Seq. 1 of 1	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	17 Jun 74			

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ROUTINE A1 – 3340 CONTROLLER INTERFACE AND LOGIC TESTS

DESCRIPTION

Test 01. Controller Preselection

Test 01 verifies that there are no active lines between the 3340 controller and storage control or IFA prior to controller selection.

Test 02. Controller Selection

Test 02 verifies that certain lines between the 3340 controller and storage control remain inactive while others become active following controller selection. It also verifies that a valid 3-of-6 code is returned upon controller selection.

Test 03. Controller Tag Bus, Bus Out, and Bus In Parity Check

Test 03 verifies that the following parity checks in the 3340 controller can be forced on and then reset by a Reset Controller command:

Tag Bus Parity Check
Bus Out Parity Check
Bus In Parity Check

Tag Bus Parity Check is forced on by an invalid controller tag (Tag '94' Bus '00').

Bus Out Parity Check is forced on by varying the Bus Out value with Tag Gate still active.

Bus In Parity Check is forced on by a special diagnostic command (Tag '09' Bus '20').

Test 04. Controller Tag Valid/Normal End

Test 04 verifies that the storage control receives Tag Valid and Normal End for all the Immediate Op Tags (01-02, 04-07, and 09-0D) and that Tag Bus and Bus Out parity checks are inactive. It also verifies that the storage control receives Tag Valid and no Normal End for all the Extended Op Tags (08, 0E, and 0F) and that the Tag Bus and Bus Out parity checks are inactive. In addition, the test forces a Monitor Check and ensures that it can be reset following a Reset Controller command.

Test 05. Bus In Assembler

Test 05 verifies that the correct Bus In information is gated under control of the Bus In selection bits. There are four buses that are gated through the Bus In Assembler. The test also verifies that a parity check is not generated in the storage control or IFA. The controller Bus In Parity Check is also tested by the diagnostic command Invert Bus In Parity (Tag '09' Bus '20').

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedure.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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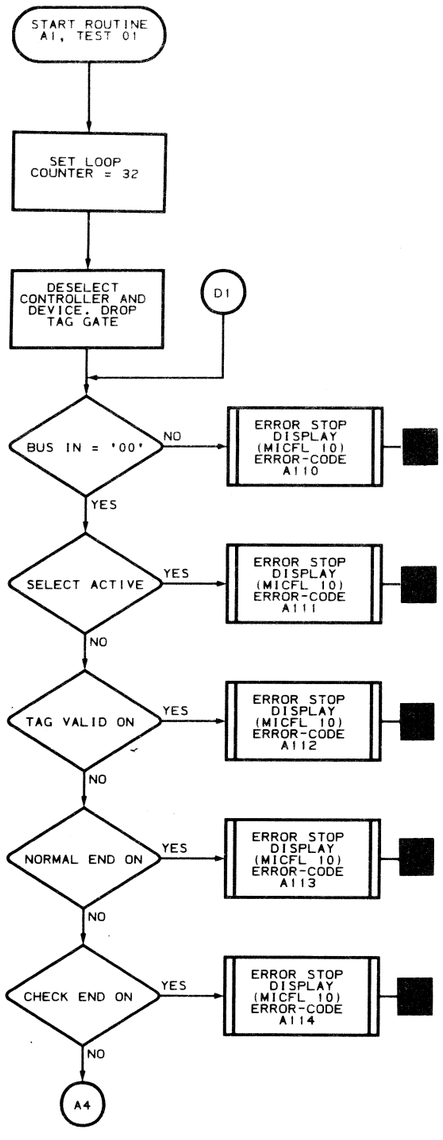
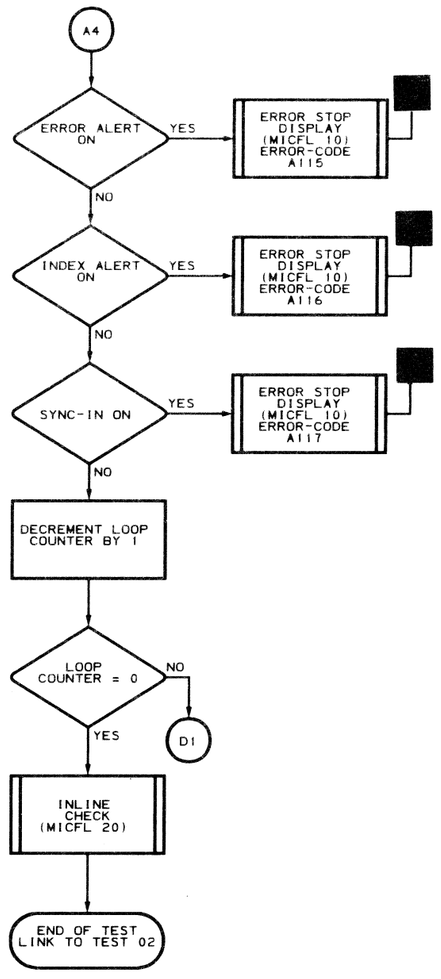
CONTROLLER INTERFACE AND LOGIC TEST (Routine A1)





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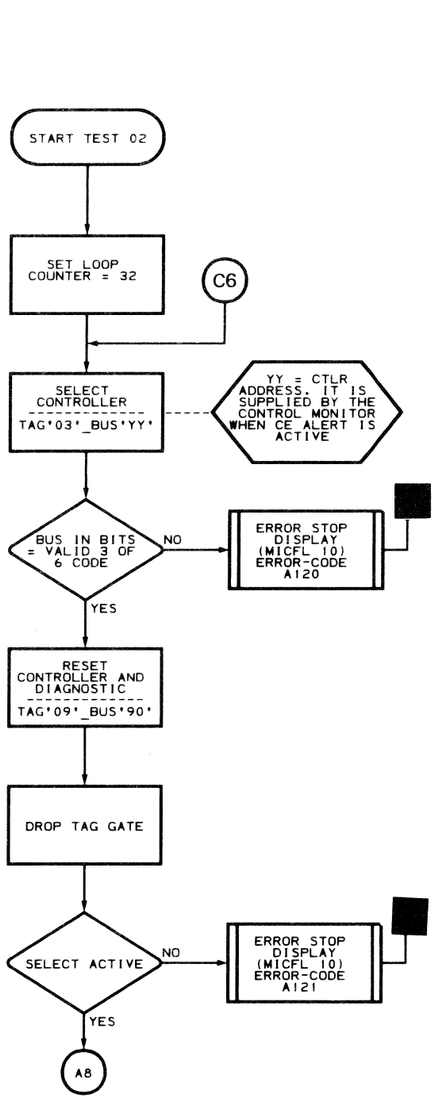
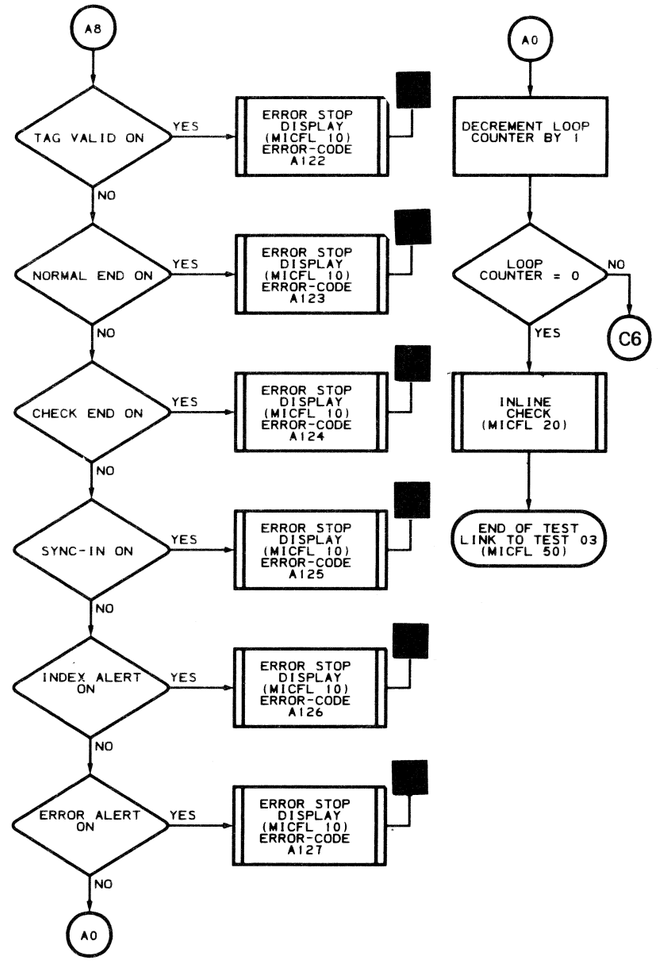
JFL_03/22/74





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CAD
JFL_03/22/74

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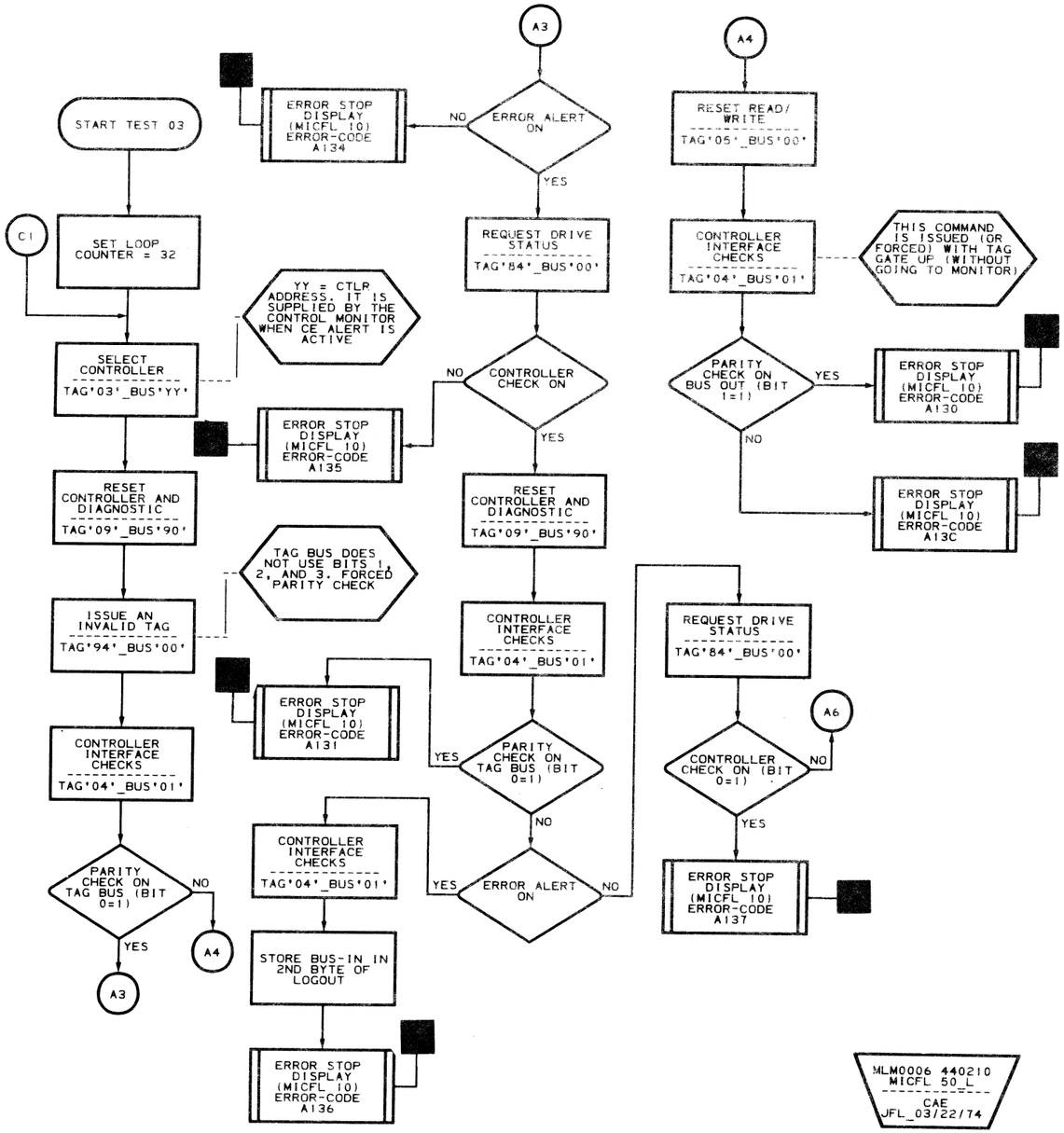
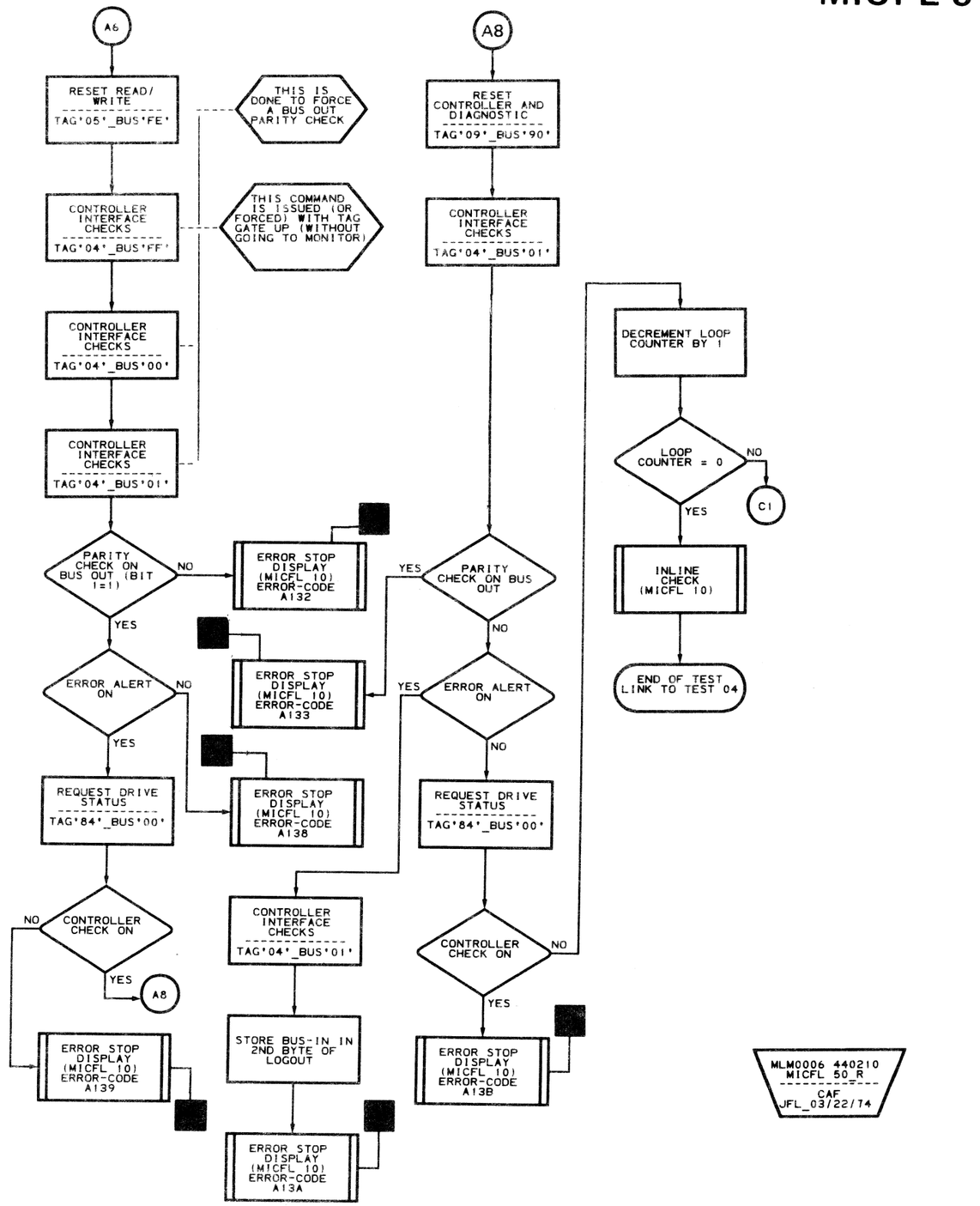
CONTROLLER INTERFACE AND LOGIC TEST (Routine A1)





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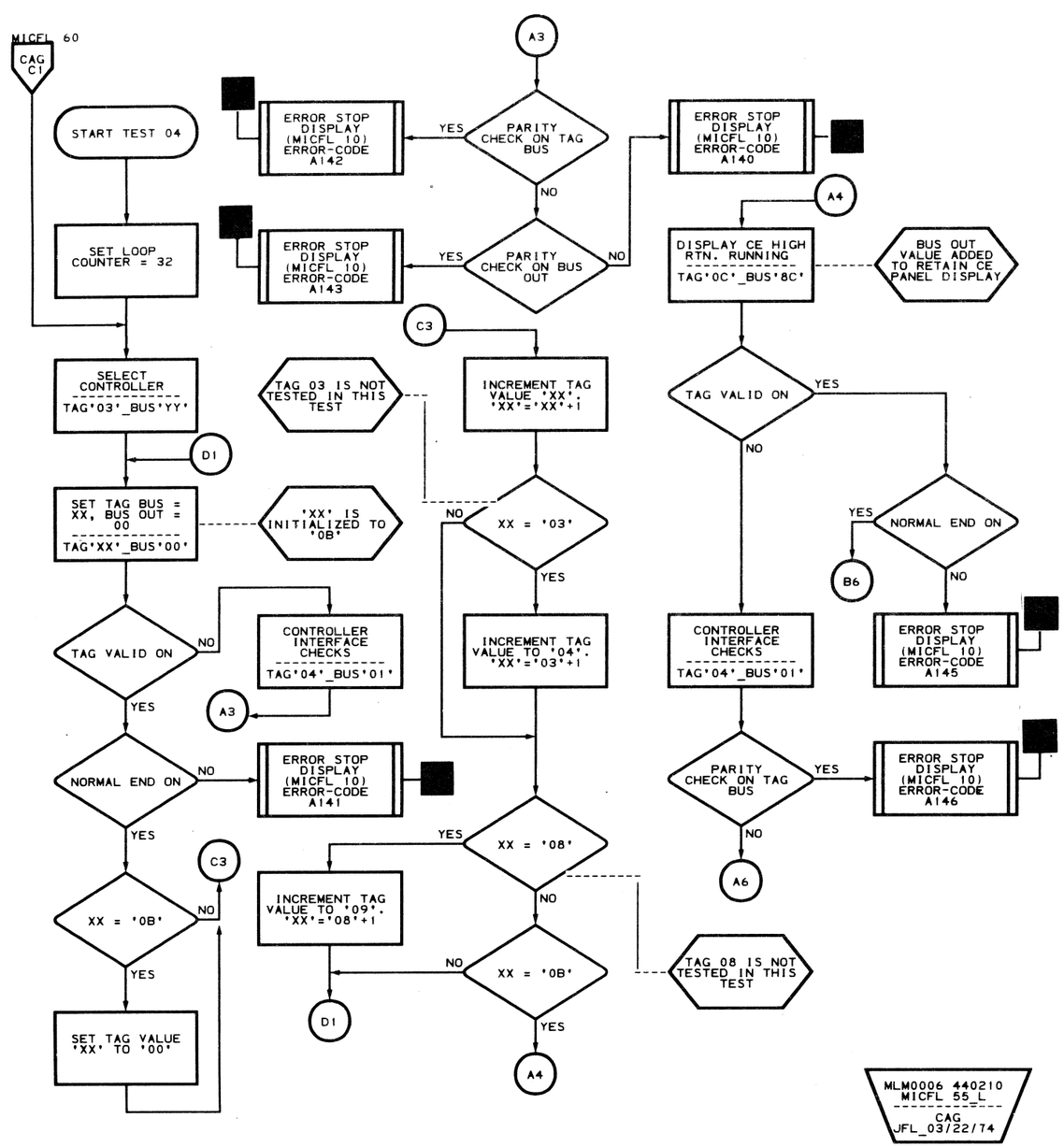

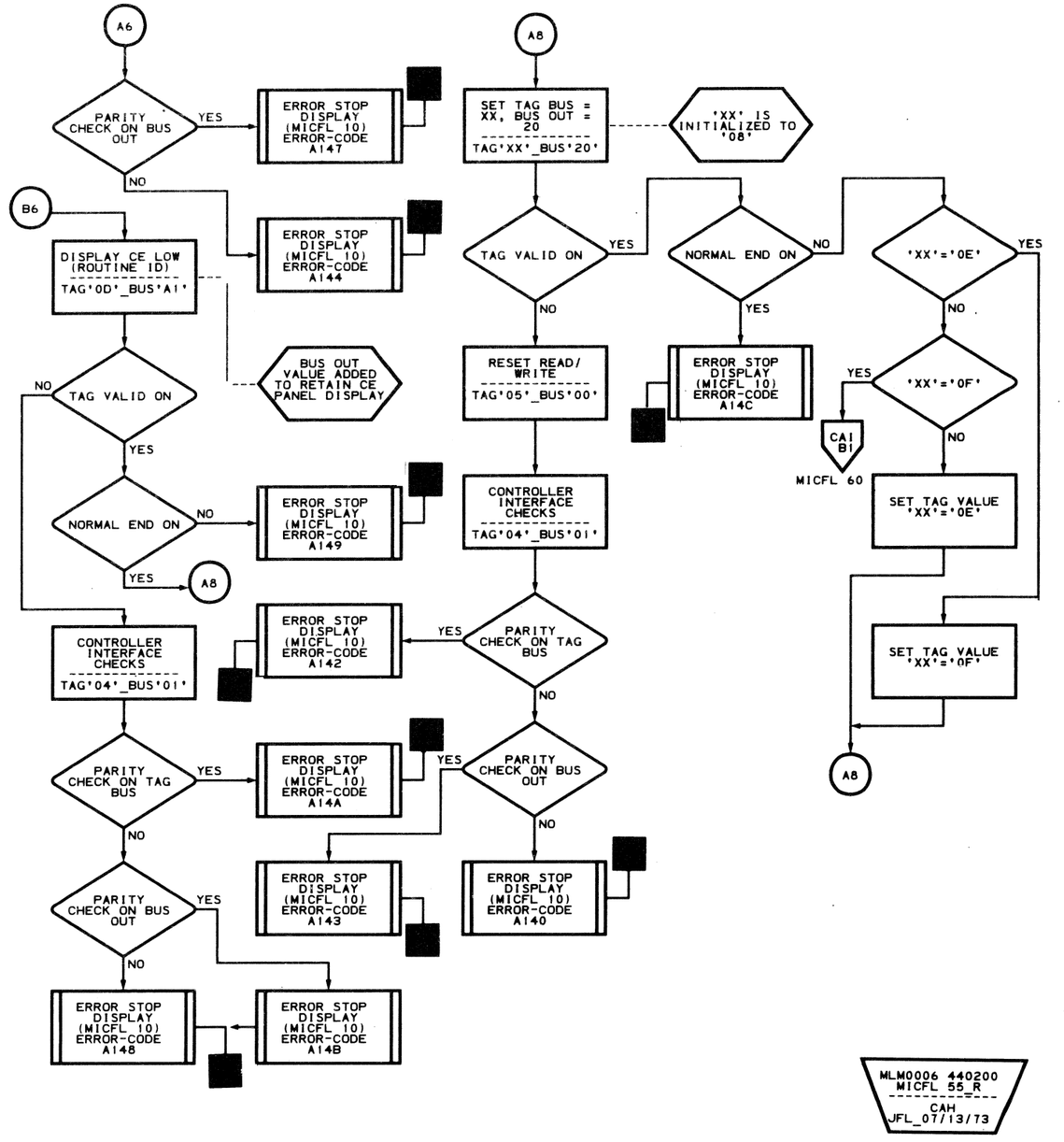

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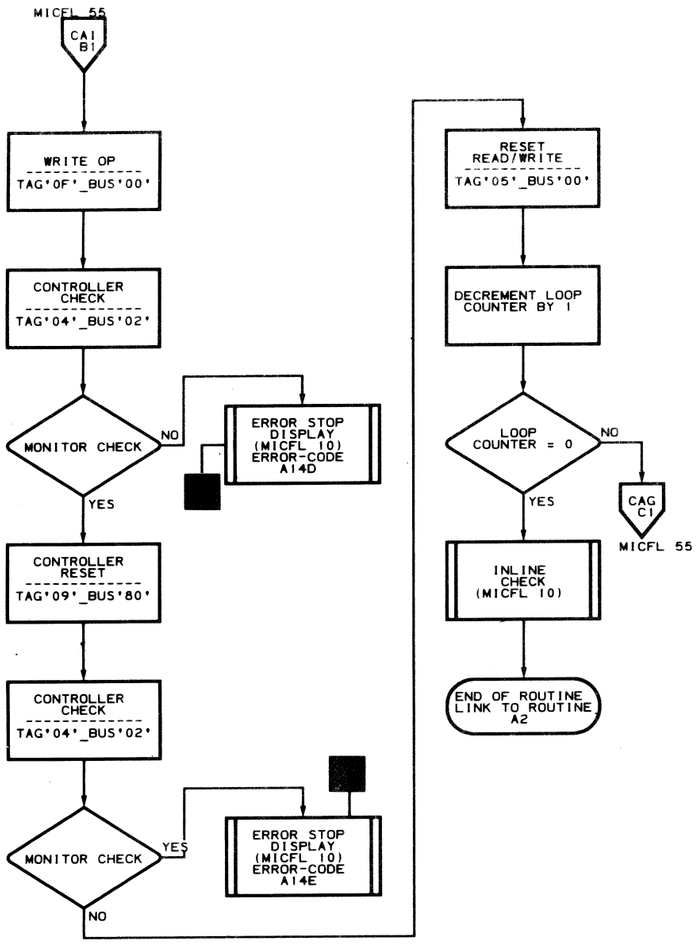

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JFL_03/22/74

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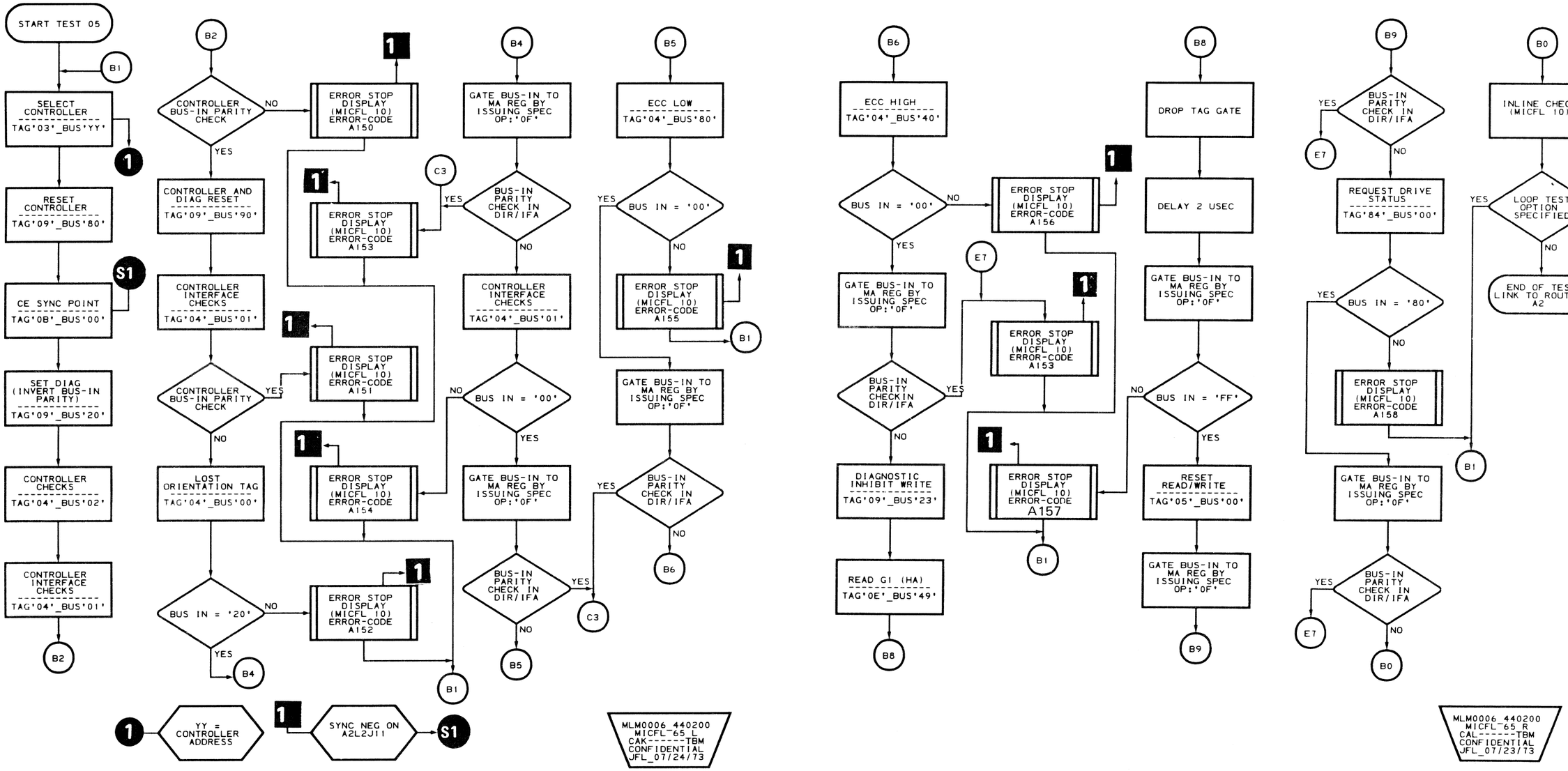

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ROUTINE A1 TEST 1 SCOPING PROCEDURES

Test 1 does not select a controller. It merely gates the Bus In and the control lines into the stroage control and ensures that none of the lines are active.

To scope:

1. Be sure that no controller on the string is operating, since the problem is either on the control interface or very near the control interface.
2. Set scope trigger to auto and adjust triggering level to achieve a stable trace. A suitable sweep speed is 20 microseconds per division.
3. For all bus and control lines except Normal End and Tag Valid, probe the appropriate point, as indicated by logics or diagrams. The program need not be looping. The level must be a minus NPL level (ground) in a static condition. See Note.
4. For Normal End and Tag Valid, scope for pulses – not a solid plus level – since the stroage control is polling and Normal End and Tag Valid are correct responses to poll. A solid +NPL level is an indication of an erroneously active line. See Note.

Note: If more than one controller is attached, it is necessary to isolate to a single controller. Power-off all controllers except the one being tested. Test each controller with power removed from other controllers in the group. Isolation may also be done by removing the control interface cables to succeeding units. It may be necessary to determine if the storage control can be stopped in order to make a proper determination of Normal End and Tag Valid problems without polling in progress. When feasible, stop the storage control and continue with the analysis.

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ROUTINE A1 TEST 2 SCOPING PROCEDURES

Routine A1 Test 2 selects the controller and checks for Select Active and for the proper 3-of-6 code. The test also checks that specified control lines from the controller to the storage control are not active.

The sync point for scoping on this page is +Select Hold NPL. This point is selected because at this stage of testing virtually none of the controller has been tested and, therefore, cannot be relied upon to function properly. Furthermore, error stops that require looping this test render the controller inoperative to online operation in most instances. If there is more than one controller on the string, it may be desirable to use Selected as a sync if it is functioning properly.

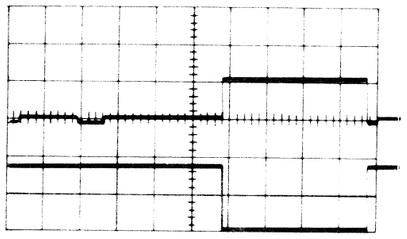
Note: If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.

Sync (+): +Select Hold NPL
A2G2B12 (BF100)
Alternate sync (–): –Selected
A2G2J05 (BF120)

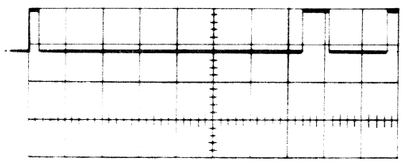
20 μs/div Pulse duration may vary due to storage control type

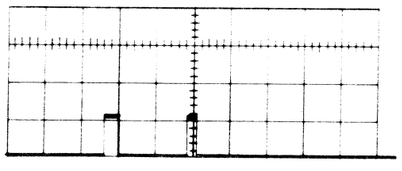
–Selected
A2G2J05 (BF120)
0.1 volt/div
X10 probes

+Select Hold NPL
A2G2B12 (BF100)
0.2 volts/div
X10 probes



–Select Bus Bits (BF190)
As scoped at the output of the Select Bus on BF190. The active bits must be a valid 3-of-6 code for the controller under test; that is, 07 for Ctlr 0 or 26 for Ctlr 1, etc.

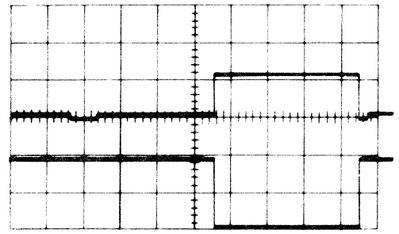




+Gen Reset
A2L2B10 (BD100)

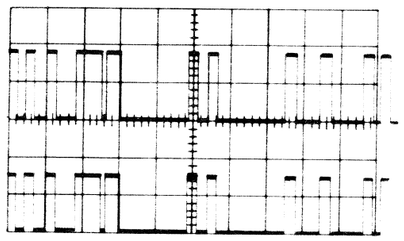
–Selected
A2G2J05 (BF120)
0.1 volts/div
X10 probe

–Select Active
A2K2J03 (BE160)
0.2 volts/div
X10 probe



+ Normal End NPL
A2K2D11 (BE160)
0.2 volts/div
X10 probe

+ Tag Valid NPL
A2K2G05 (BE160)
0.2 volts/div
X10 probe



Normal End and Tag Valid apply to the following tag sequence:

Tag	Bus	Function
03	Ctlr Addr	Select
07	–	Unused
06	–	Unused
03	Ctlr Addr	Select
09	80	Reset
07	–	Unused

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ROUTINE A1 TEST 3 SCOPING PROCEDURES

Test 3 checks the Tag Bus and Bus Out parity checkers and verifies that Error Alert condition and Controller Check are generated.

The sync point shown was selected because at this stage of testing, virtually none of the controller has been tested and therefore, cannot be relied upon to function properly. Furthermore, error stops which would require looping this test would render the controller inoperative to online operation in most instances.

Note: If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is re-started is not valid.

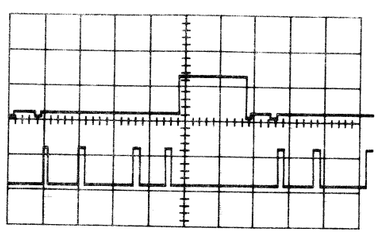
Sync (–): –Selected
A2G2J05(BF120)
Time: 50 µs/div
Pulse duration varies according to storage control type.

Reset is issued 4 times:

1. Initial reset
2. Resets Tag Bus Parity Error
3. Resets Bus Out Parity Error
4. For housekeeping

–Selected
A2G2J05 (BF120)
(Alternate: A2L2G03 (BD100))

0.1 volts/div X10 probe



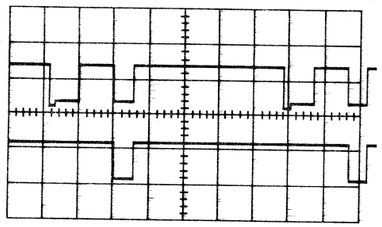
+Gen Reset
A2L2B10 (BD100)
(Alternate: A2F2M11 (BA130))

0.1 volts/div X10 probe

A Tag Bus Parity Check is forced by issuing a Tag Value of 94. The first pulse is the primary failure.

–Tag Bus Parity Check
A2G2G10 (BF110)

0.1 volts/div X10 probe



Bus Out Parity Check is forced by changing the value on Bus Out while Tag Gate is active.

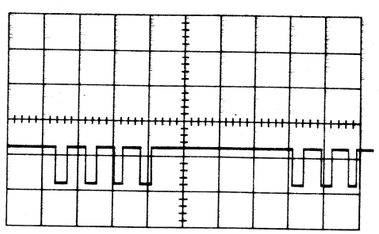
–Bus Out Parity Check
A2G2J10 (BF110)

0.1 volts/div X10 probe

This represents the times that the forced Parity Check and Reset functions are tested.

–Status Bytes Op 04
A2G2G03 (BF110)

0.1 volts/div X10 probe



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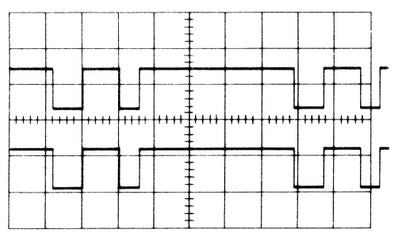
ROUTINE A1 TEST 3 SCOPING PROCEDURES (continued)

Controller Check and Error Alert Condition should follow the Tag Bus and Bus Out Parity Check Latches.

Scope setup as on previous page.

–Controller Chk
A2K2M12 (BE130)

–Err Alert Cond
A2F2J10 (BA140)

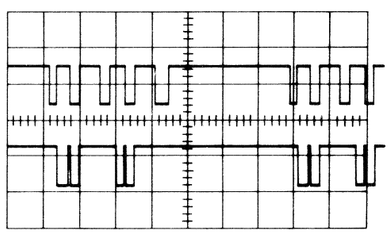


Read Status 84 is used to Gate Controller Check on to Bus In Bit 0. Notice that the first pulse is an erroneous decode of Tag 94 and occurs at the time that Tag Bus Parity Check Sets. Subsequent pulses occur alternately when the Controller Check is active and then inactive.

Controller Bus In Bit 0 represents, alternately, Tag Bus Parity Check under Op 04 and Controller Check under Op 84.

–Read Status 84
A2G2D09 (BF110)

–Contr Bus In Bit 0
A2F2P05 (BA100)



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond thepoint of the error are not valid.

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ROUTINE A1 TEST 4 SCOPING PROCEDURES

Routine A1 Test 4 issues all Controller Tags and checks for:

1. Tag Valid for all Ops.
2. Normal End for all Immediate Ops and no Normal End for Ops 08, 0E, or 0F.
3. No Tag Bus or Bus Out Parity Check.

The tag sequence (refer to Coerce Tag Valid trace) is as follows:

1. 0B – Used as sync for all pictures.
2. 01
3. 02
4. 04
5. 05
6. 06
7. 07
8. 09
9. 0A
10. 0C
11. 0D

All of the above should produce a Normal End pulse. An error stop is created if they do not.

12. 08
13. 0E
14. 0F

The above tags are Extended Op and should not produce a Normal End Op in this test. An error stop is created if they do.

15. 05
16. 09
17. 09
18. 07

The above tags are redundant and are used in housekeeping.

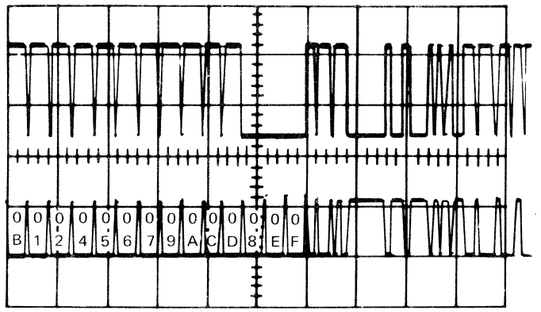
The remaining pictures show representative pulses that may be used to establish timing relationships.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Time: 50 μs/div

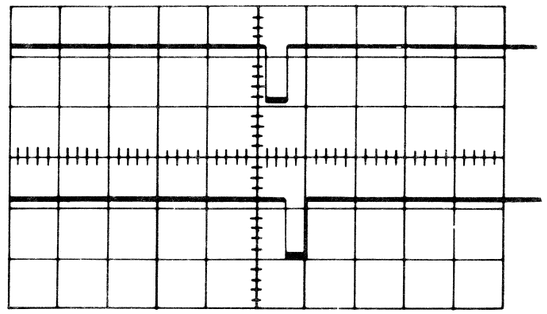
+Normal End NPL
A2K2D11 (BE160)
0.2 volts/div X10 probe

–Coerce Tag Valid
A2K2B10 (BE150)
0.1 volts/div X10 probe
Tag Bus values are indicated with the appropriate pulse.



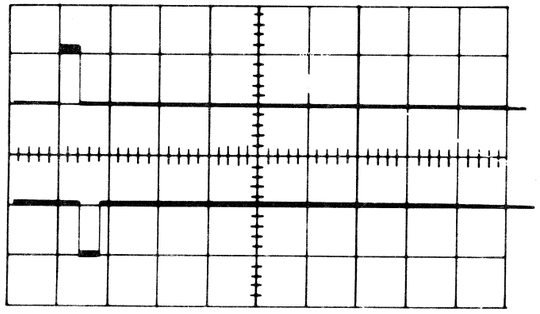
–Read Op OE
A2L2M02 (BD100)

–Write Op OF
A2L2M04 (BD100)

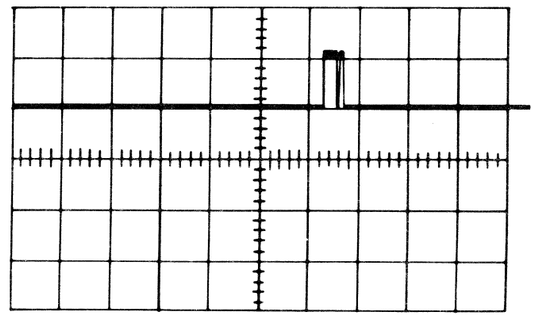


+Contr Poll Op 02
A2G2J12 (BF110)

–Status Bytes Op 04
A2G2G03 (BF110)

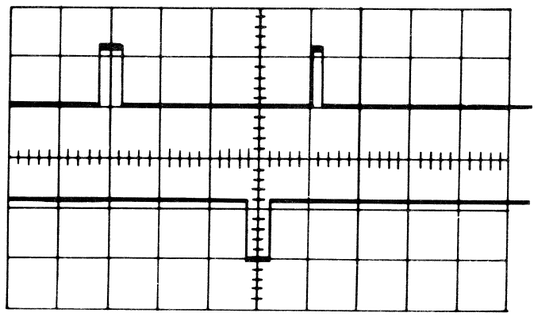


+Gen Reset
A2L2B10 (BD100)



+Reset RW Op 05
A2G2D05 (BF110)

–ECC CTRL Op 08
A2L2J13 (BD100)



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ROUTINE A1 TEST 5 SCOPING PROCEDURES

Routine A1 Test 5 is a test of the registers that form Bus In. The test attempts to gate certain nominal values onto Bus In and then test for those values.

If the nominal values are not present but the register gating is correct, continue on with the other routines. If the register gating is not correct resolve the problem before continuing.

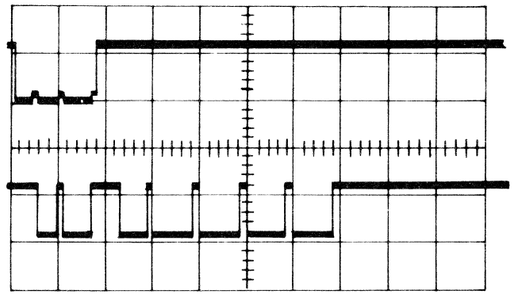
To loop test and bypass errors:
1. Load routine A1.
2. Enter: '10 05 01 00'.

To scope Bus In values which do not compare, see the next page.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

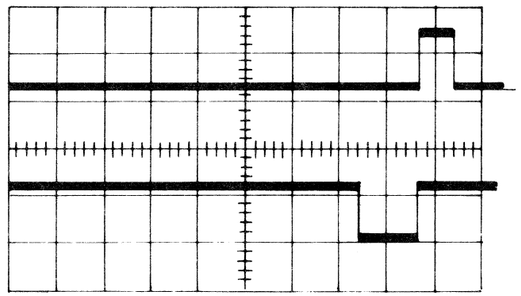
Sync Ext (–): –RASTP
A2L2J11 (BD100)
Time: 20 us/div
Vertical: 0.1 volts/div x 10 probes.

–Controller Bus Par Chk Latch A2F2P11 (BA130)



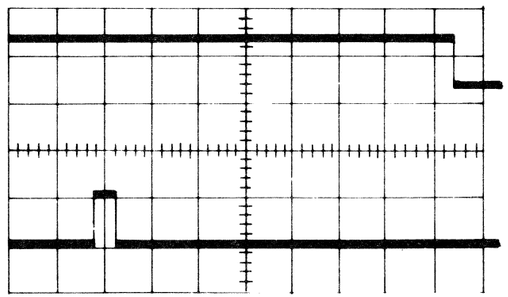
–Status Bytes OP 04
A2G2G03 (BF110)

+Reset R/W OP 05
A2G2D05 (BF110)



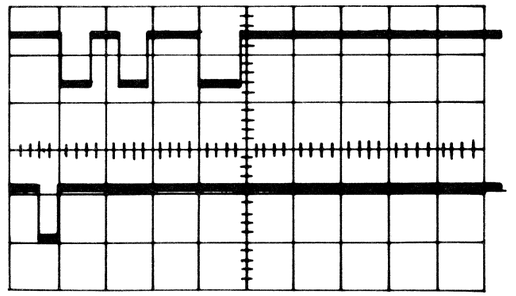
–Read OP 0E
A2L2M02 (BD100)

–Read Status 84
A2G2D09 (BF110)



+Gen Reset
A2L2B10 (BD100)
Alternate: A2F2M11 (BA130)

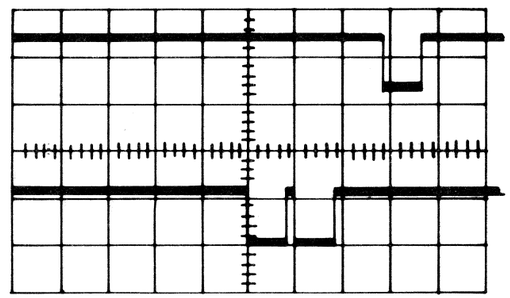
–Gate Controller ERR 1
A2K2M05 (BE120)



–Gate Controller ERR 2
A2K2M03 (BE120)

Note: –ECC Correct OP A2K2U07 (BE120) is never active in this test.

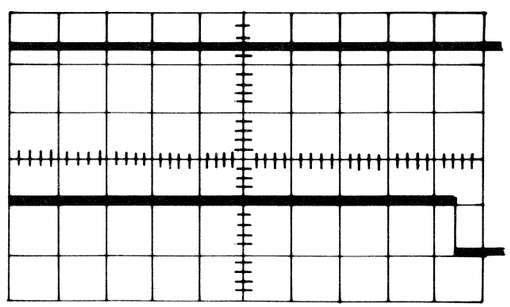
–Assm Sel X
A2K2G08 (BE130)



–Assm Sel Y
A2K2J09 (BE130)

Note: –Read Mode CTL A2K2U13 (BE130) is never active in this test.

–BI Sel X
A2F2J09 (BA130)



–BI Sel Y
A2F2G07 (BA130)

Note: –Read Mode CTL A2F2S11 (BA130) is never active in this test.

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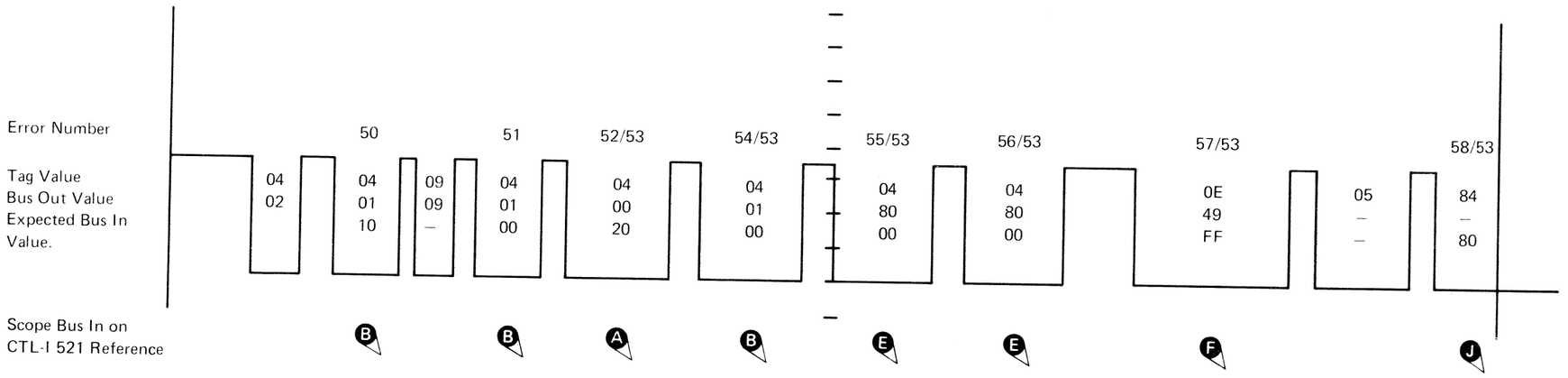
ROUTINE A1 TEST 5 SCOPING PROCEDURES (continued)

Establish the time relationship for the error received and scope using CTL-I 521 for reference. Starting with the referenced points. If the value in Message Byte 2 equals the value scoped, continue the tests starting with Routine A2. For example: for Error Code A152 – if the Message Byte 2 displays 28 instead of 20, scope the designated points on CTL-I 521. If the value at that point is 28, continue with Routine A2. If the value is not 28, replace the cards specified by the appropriate MAP or continue scoping.



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE A2 – 3340 DRIVE INTERFACE AND LOGIC TESTS

DESCRIPTION

Test 01. Drive Selection

Test 01 verifies that a 3340 Drive can be selected by returning a Tag Valid response and a physical address when the drive is in CE mode. It also ensures that Drive Selection Error and Monitor Check are both inactive upon entry.

Test 02. Tag Bus and Bus Out Parity Check

Test 02 verifies that Tag Bus Parity check and Bus Out Parity check can be forced on and then reset when a Device Interface Check command is issued. It also verifies that Drive Interface check is forced on when either Tag Bus or Bus Out Parity check is active.

Both parity checks are forced on by special diagnostic commands.

Tag '09' Bus '21' inverts Tag Bus Parity in the drive.
Tag '09' Bus '22' inverts Bus Out Parity in the drive.

Test 03. Bus Out/Bus In Wrap

Test 03 verifies that a data path exists between Bus Out and Bus In on the 3340 Drive. The test uses the Difference Counter for testing the integrity of the data path. If a failure occurs in the Difference Counter, the test automatically switches to the Head Address Register (HAR) and uses it as the test vehicle. If both HAR and Difference Counter fail, the test halts with an error.

The following values are placed on Bus Out:

a. All 0s
b. All 1s
c. A sliding 1s pattern

Test 04. Drive Selection/Rejection

Test 04 verifies that a drive cannot be selected when Bus Out Bit 4 is active during a selection operation (Tag '83'). This bit prevents a physical address from being returned to the storage control for any drive. The test also forces a Drive Selection Error by selecting the CE drive and any one of eight customer drives (two drives simultaneously selected).

Test 05. Drive Tag Valid/Normal End

Test 05 verifies that the storage control receives a Tag Valid response and Normal End for all of the 3340 Drive tags except Tag '85'. If Tag Valid is not received for a given tag, the test examines Tag Bus and Bus Out Parity checks to see if either one is active.

Test 06. Drive No Tag Valid

Test 06 verifies that Tag Valid is not returned for drive Tags '8A' – '8F' when Tag Bus Parity has been inverted. Tag Bus Parity is inverted by a diagnostic command (Tag '09' Bus '21').

Test 07. Drive Bus In Parity Check

Test 07 verifies that drive Bus In Parity checks can be forced on and then reset with the Reset Controller command. The drive Bus In Parity check is inverted by a diagnostic command (Tag '09' Bus '20').

Test 08. Head Address Register

Test 08 verifies that the Head Address Register (HAR) can be set to any value. The HAR is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 2s pattern. Every time HAR is sensed, Bus In is examined for a parity check.

Test 09. Difference Counter Test (Part 1)

Test 09 verifies that the Difference Counter can be set to any value. The Difference Counter is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 2s pattern. Every time the Difference Counter is sensed, Bus In is examined for a parity check.

Test 10. Difference Counter Test (Part 2)

Test 10 verifies that the Difference Counter can be decremented properly by a special diagnostic command (Tag '8A' Bus '01').

Test 11. Optional Cylinder Address Register

Test 11 verifies that the Cylinder Address Register (CAR) can be set to any value. The CAR is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 2s pattern. Every time the CAR is sensed, Bus In is examined for a parity check.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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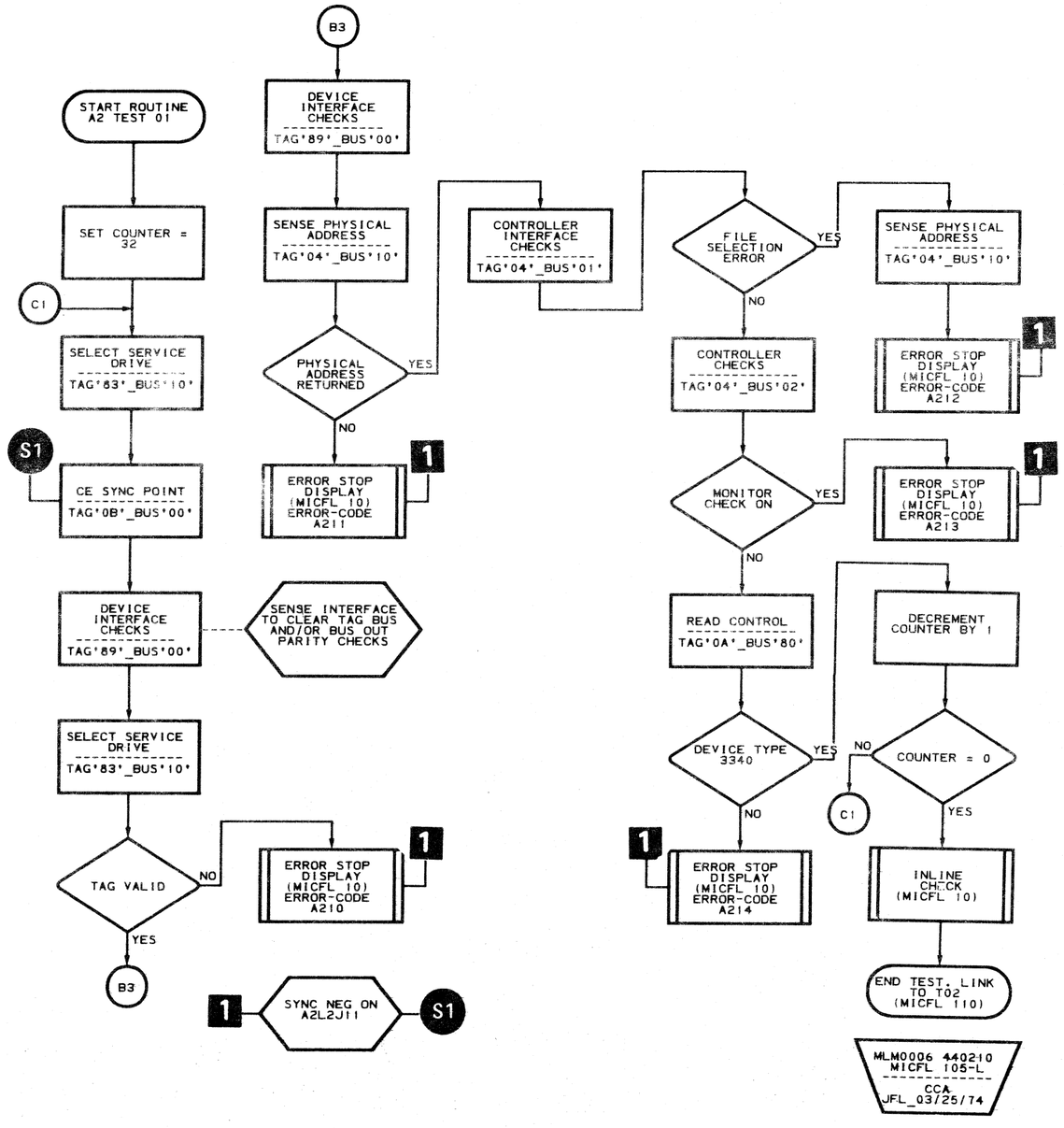
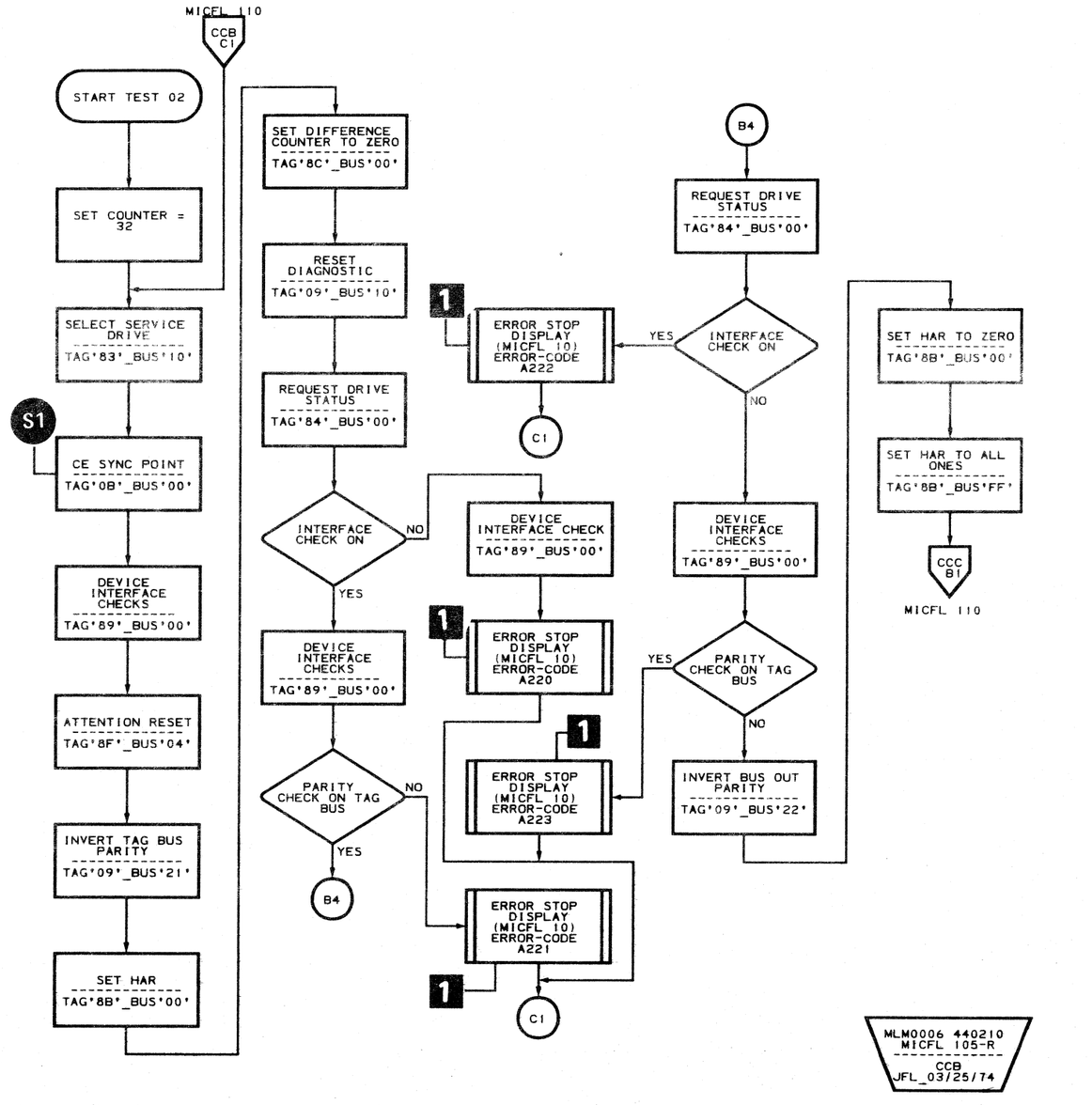
DRIVE SELECTION TEST/PARITY CHECKER TEST (Routine A2)





CA0105	2747039	440200	440202	440203	440210	440214		
Seq. 1 of 1	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	15 Apr 74	17 Jun 74		

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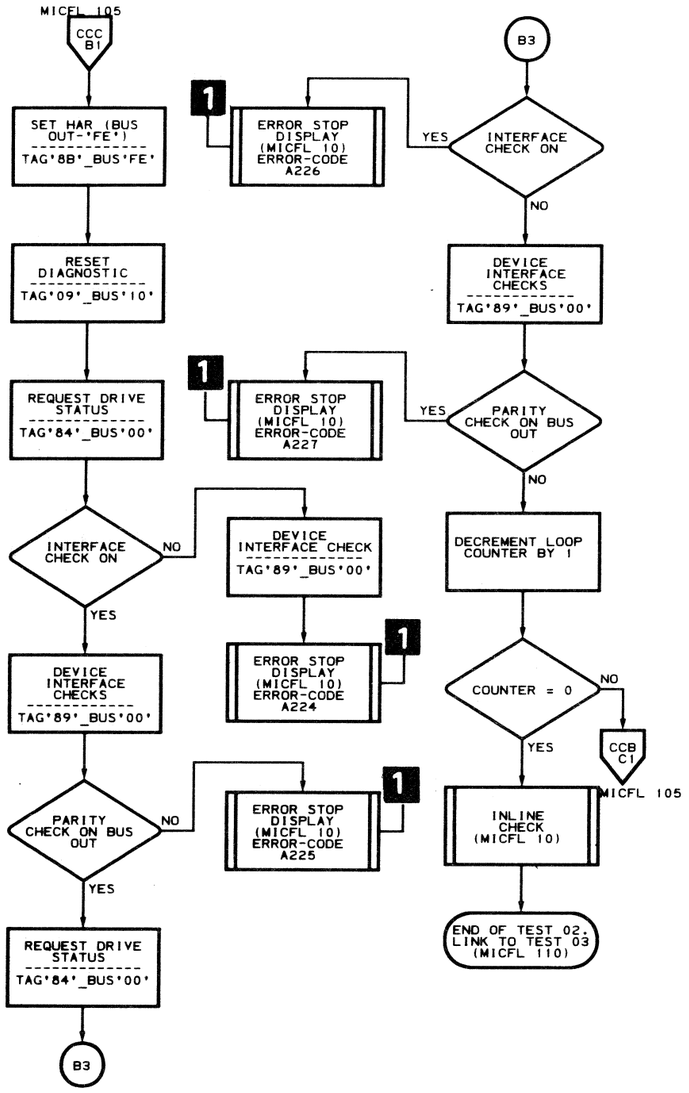
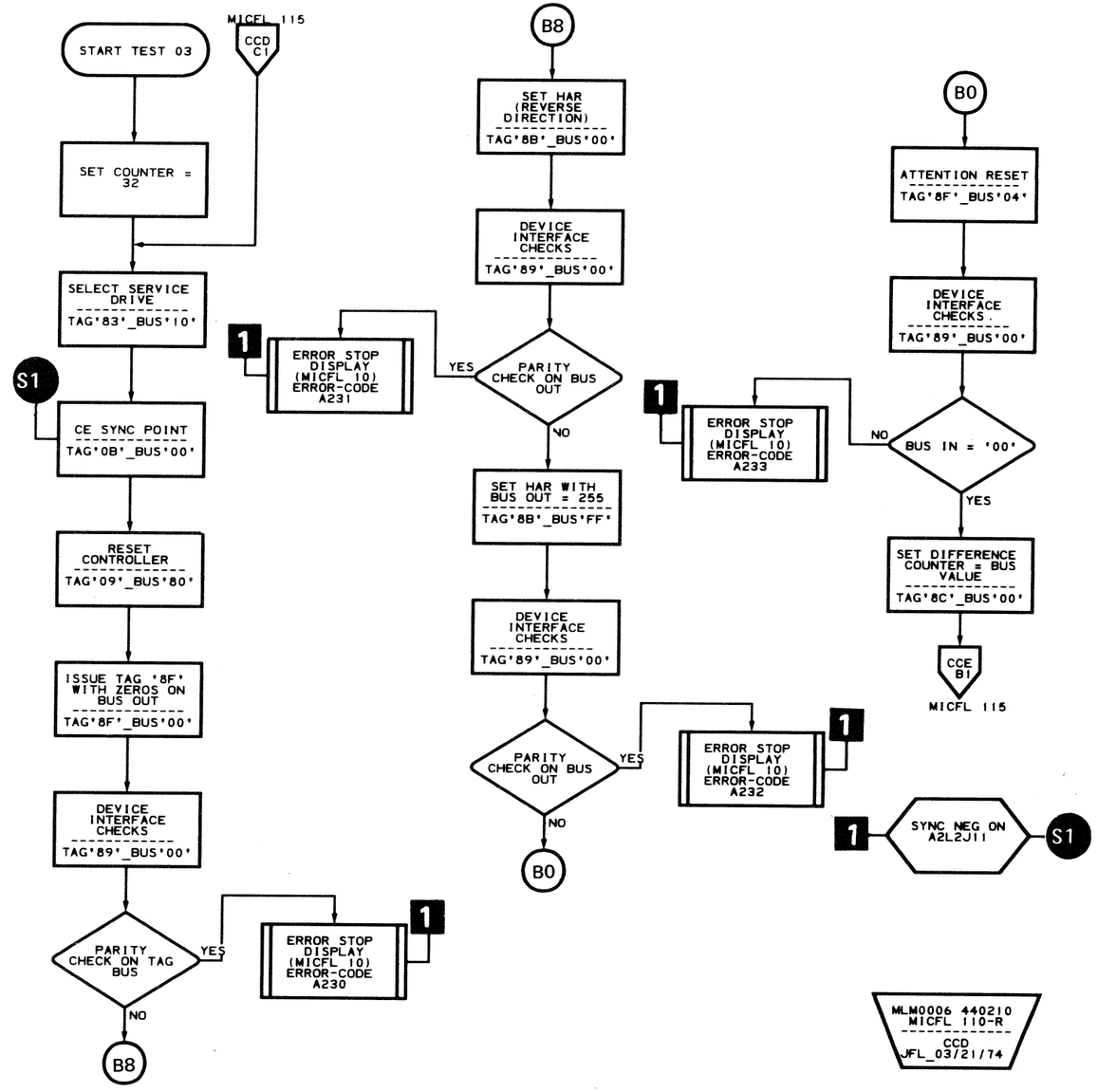
PARITY CHECKER TEST/BUS OUT/BUS IN WRAP TEST (Routine A2)



1 THE SAME TAG IS ISSUED THREE TIMES WITH DIFFERENT BUS OUT VALUES. THE DIFFERENT BIT PATTERNS TEST THE PARITY BIT

MLM0006 440210
MICFL 110-L
CCC
JFL_03/21/74



MLM0006 440210
MICFL 110-R
CCD
JFL_03/21/74

CA0110	2747040	440200	440202	440203	440210			
Seq. 1 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	15 Apr 74			

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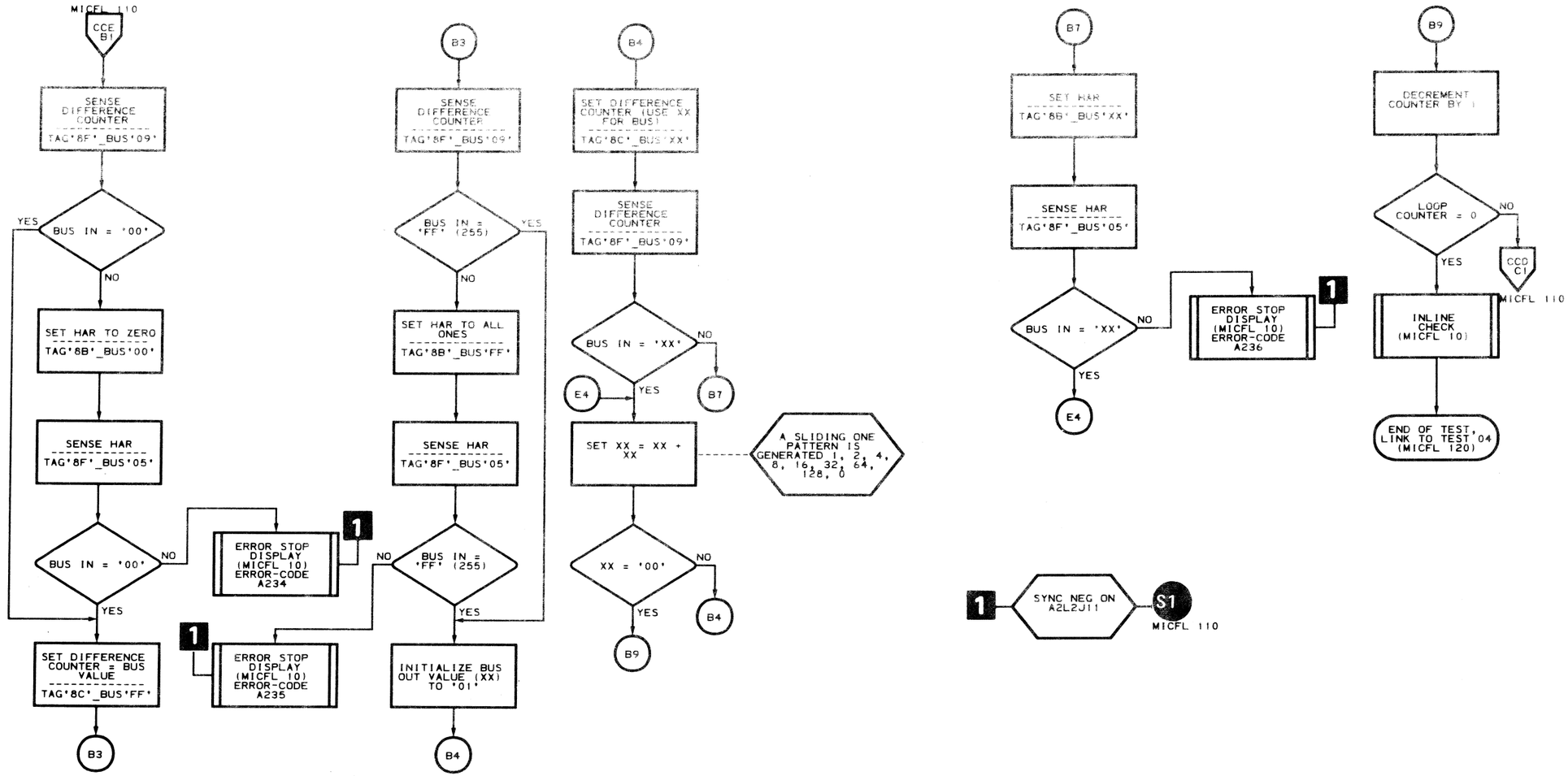

MLM0006 440200
MICFL 115-L
CCE
JFL_03/21/74

MLM0006 440210
MICFL 115-R
CCF
JFL_03/21/74

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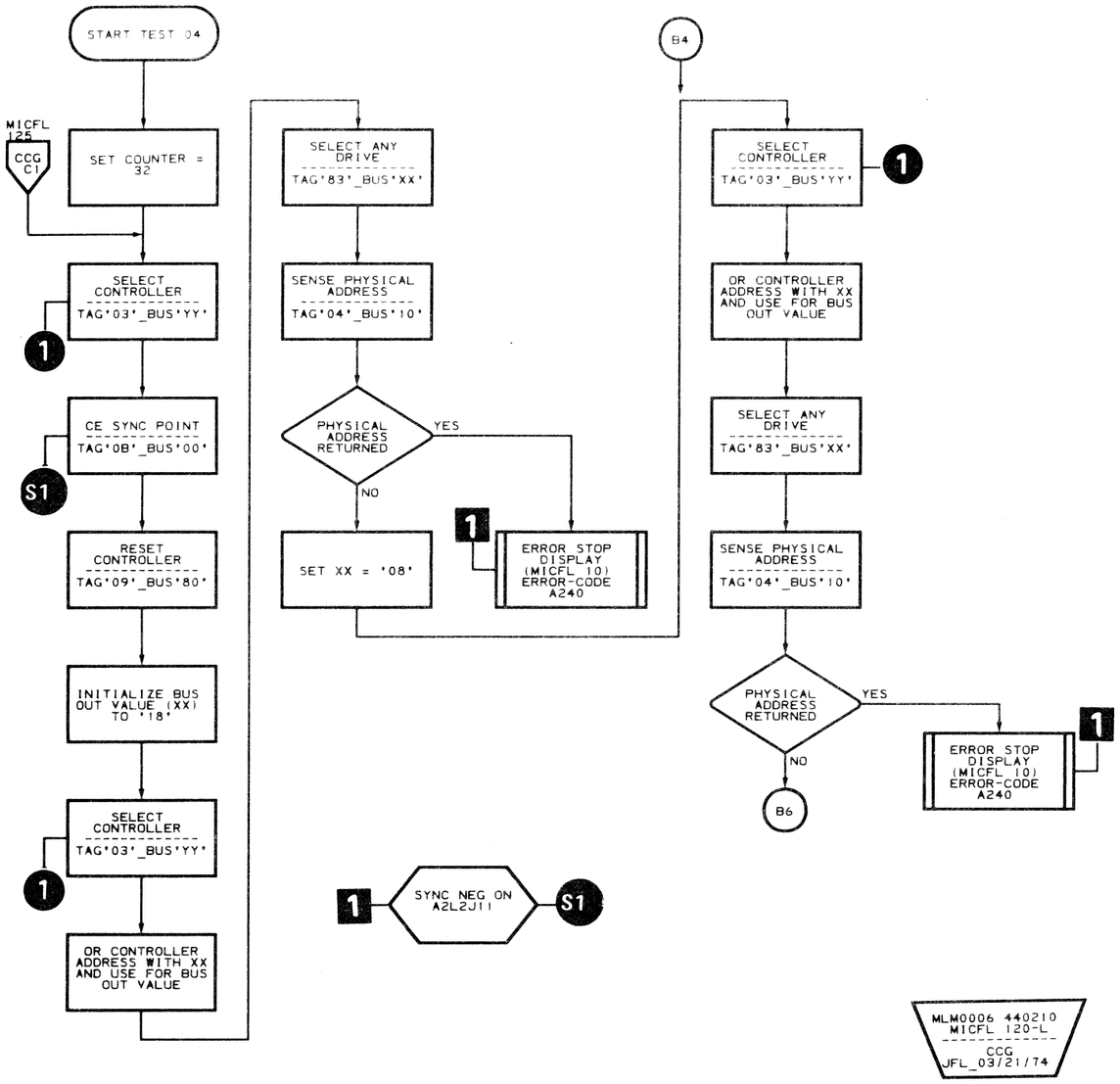
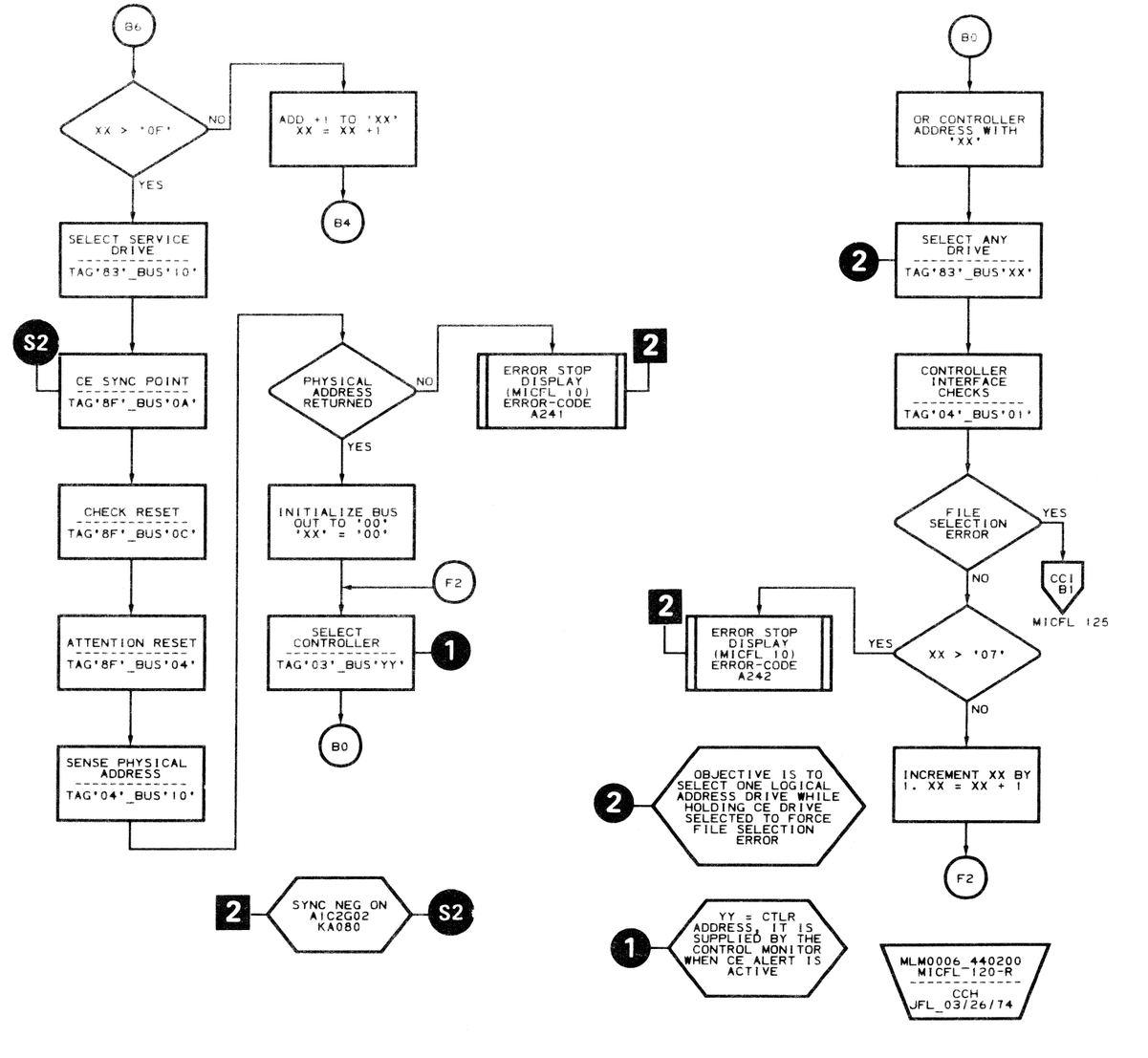
DRIVE SELECTION/REJECTION TEST (Routine A2)





CA0120 Seq. 1 of 2	2747041 Part No.(N)	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440227 14 Sept 76		

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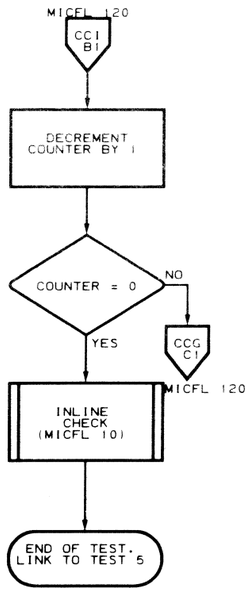

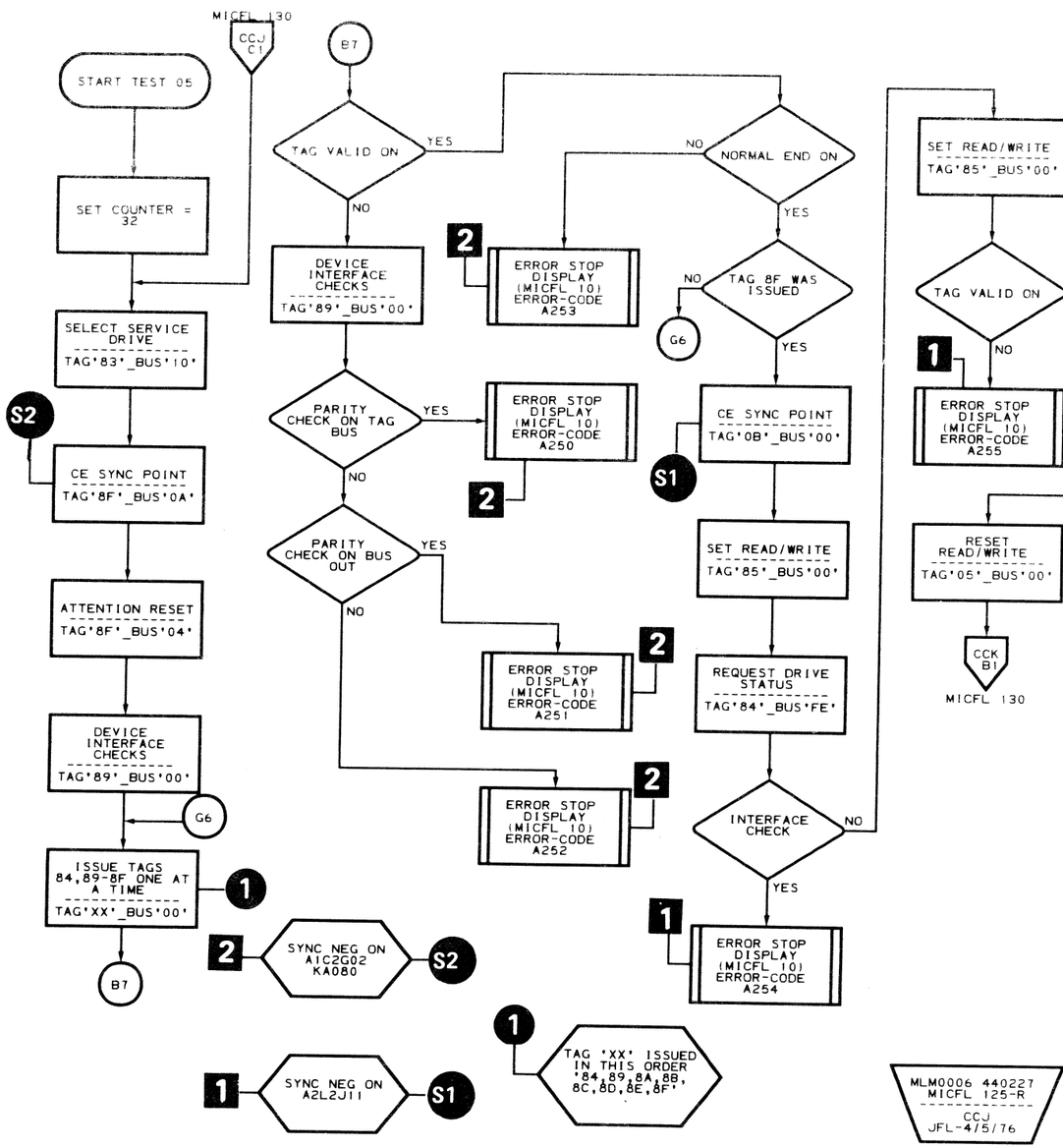

MLM0006 440210
MICFL 125-L
CCI
JFL_03/21/74

MLM0006 440227
MICFL 125-R
CCJ
JFL-4/5/76

CA0120 Seq. 2 of 2	2747041 Part No.(N)

440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440227 14 Sept 76		

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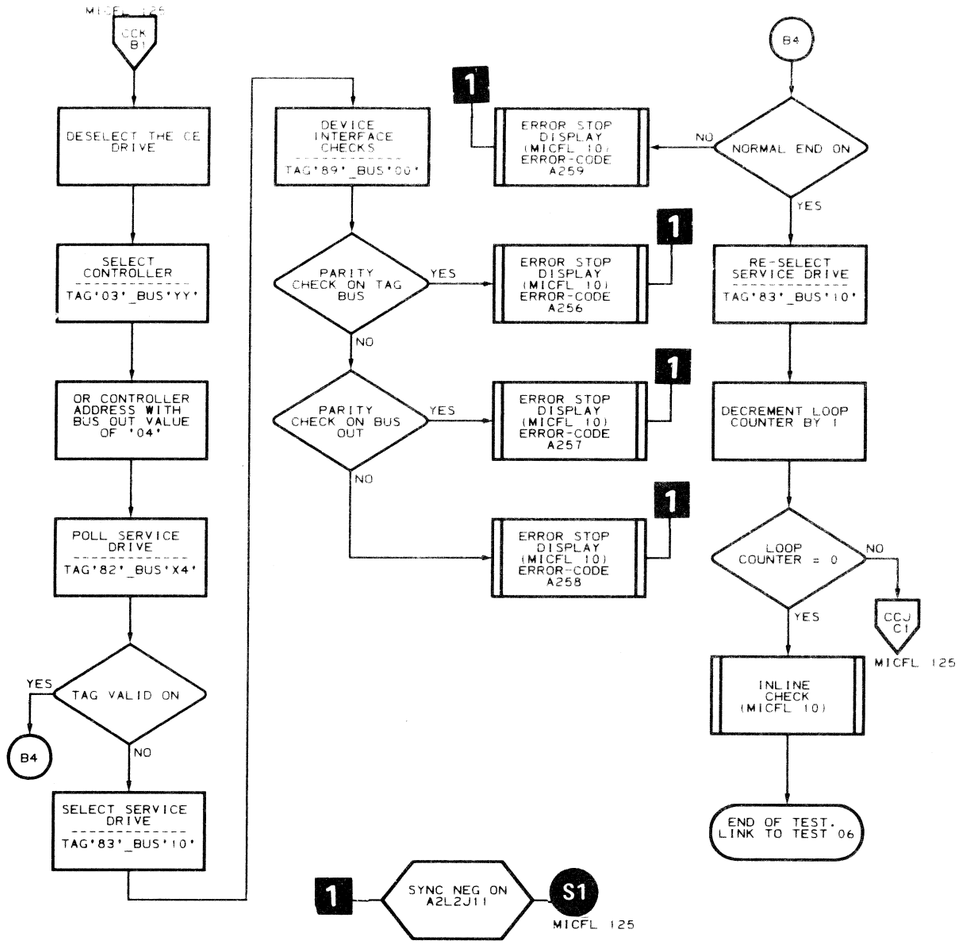
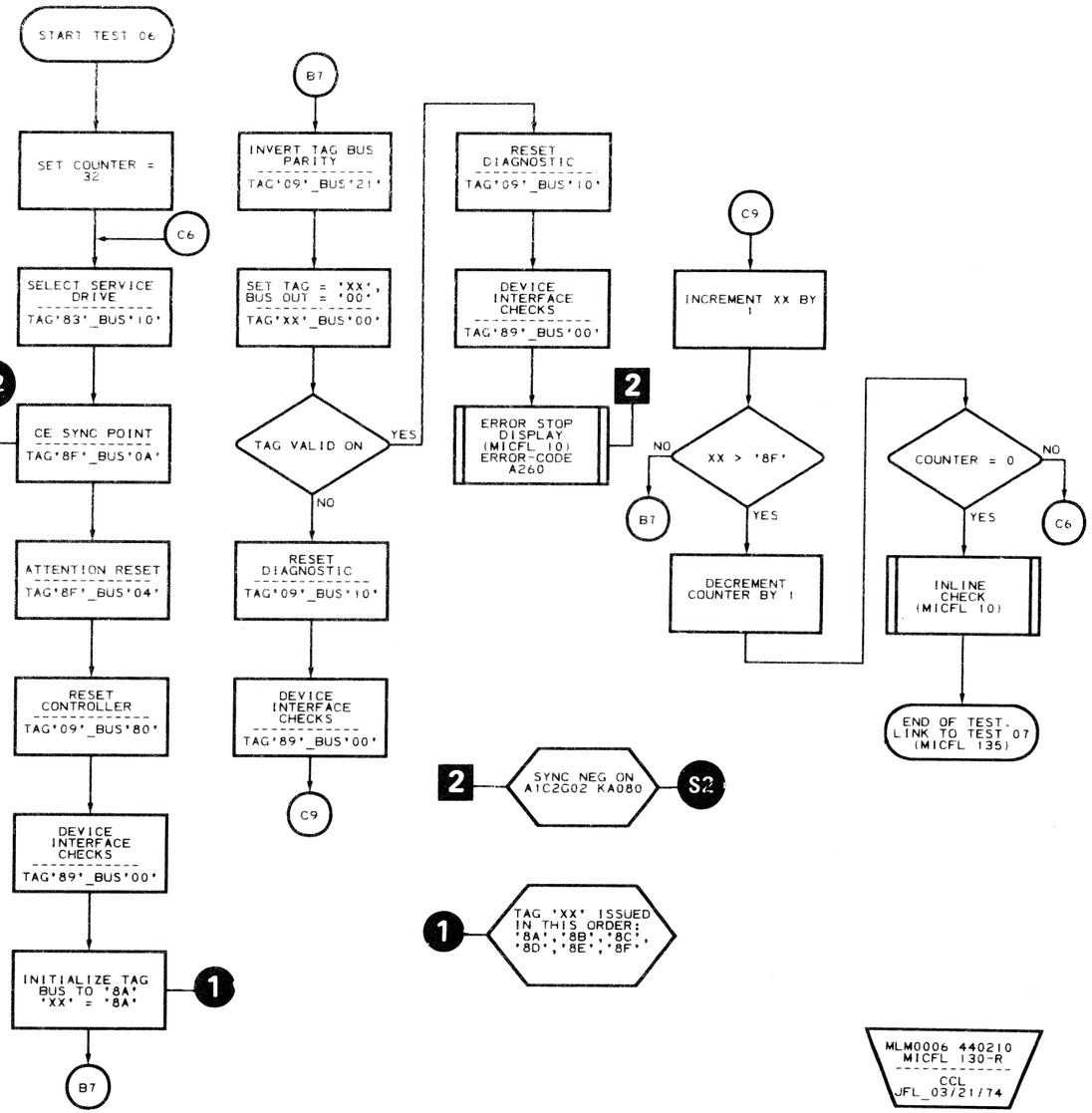
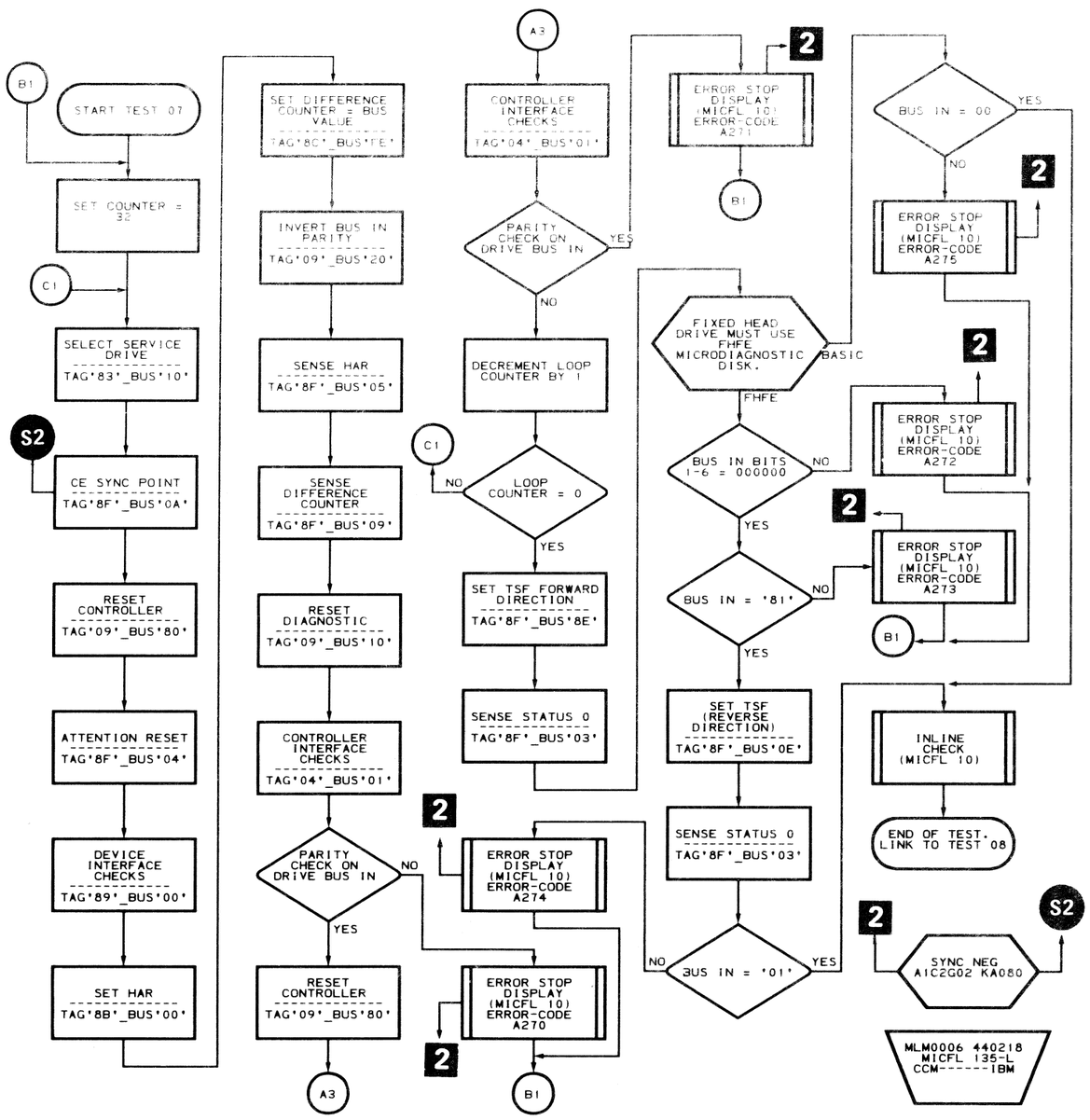
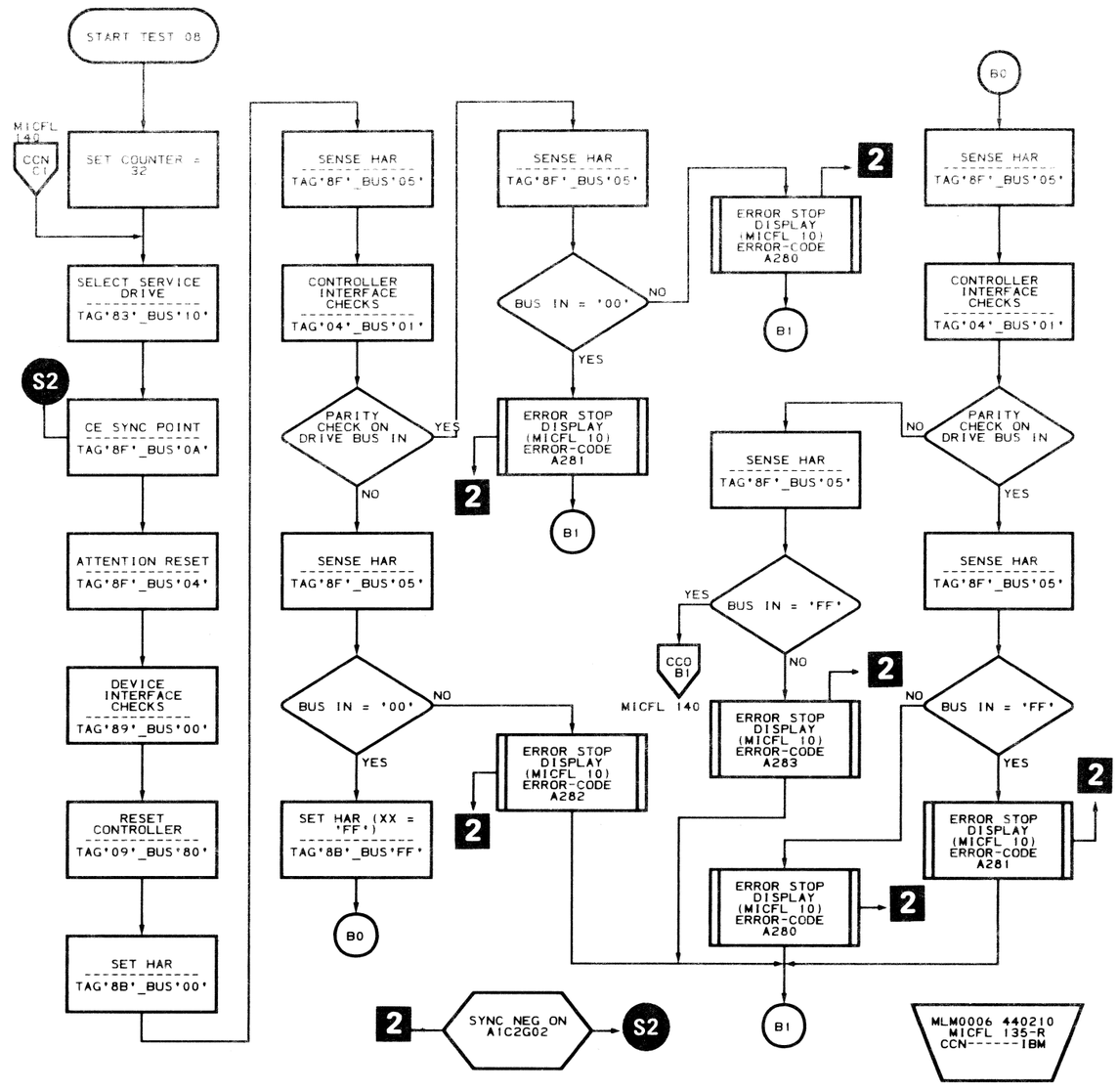




CA0130	2747042	440200	440202	440203	440210	440214	440218
Seq. 1 of 2	Part No. ( )	25 June 73	7 Sept 73	2 Nov 73	15 Apr 74	17 Jun 74	5 Aug 74

BUS IN PARITY CHECK/HEAD ADDRESS REGISTER (Routine A2)





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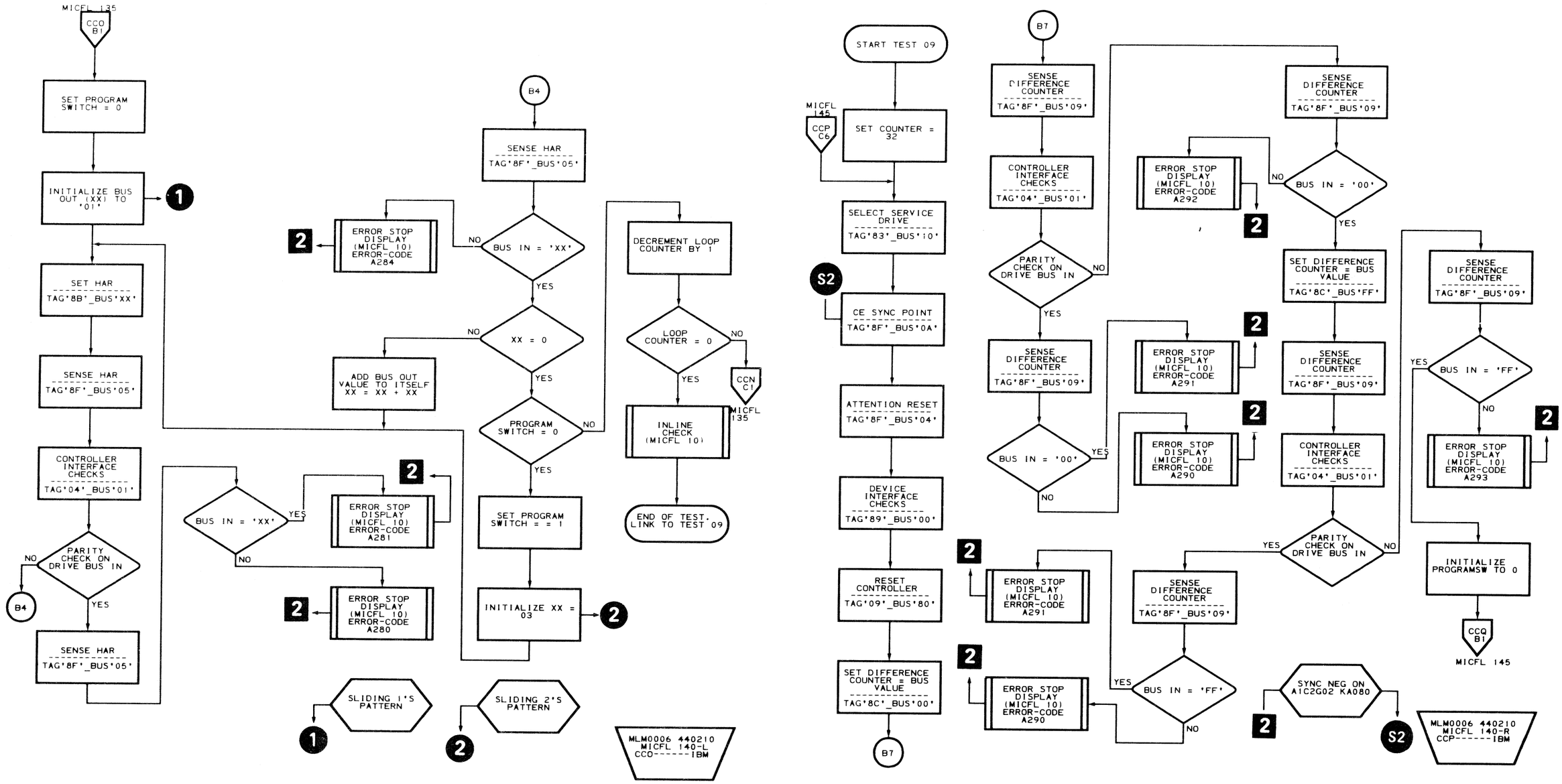
HEAD ADDRESS REGISTER/DIFFERENCE COUNTER (Routine A2)



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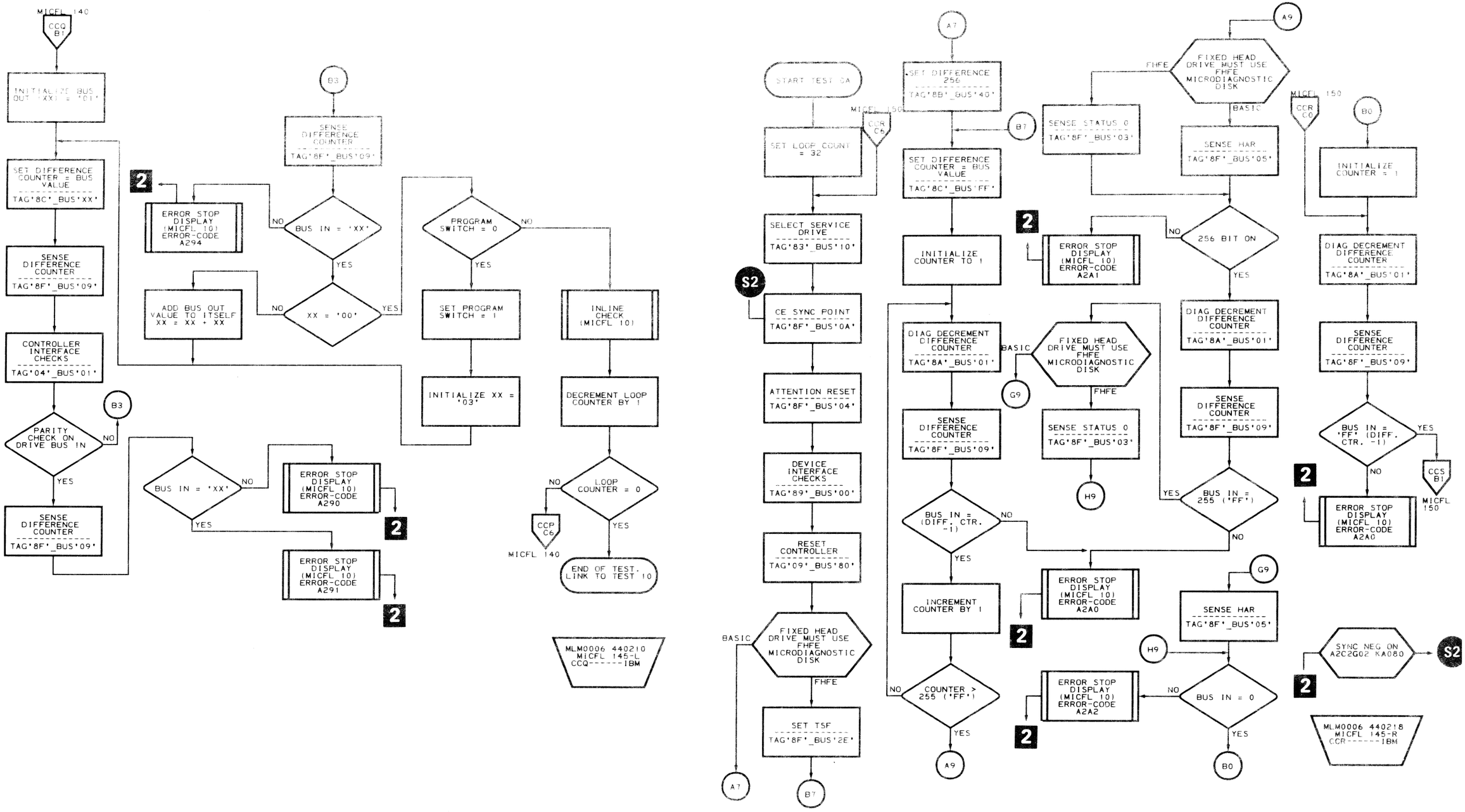

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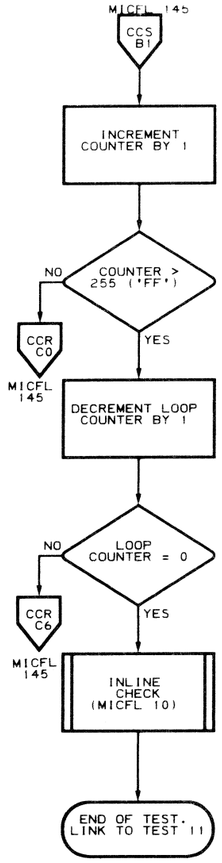

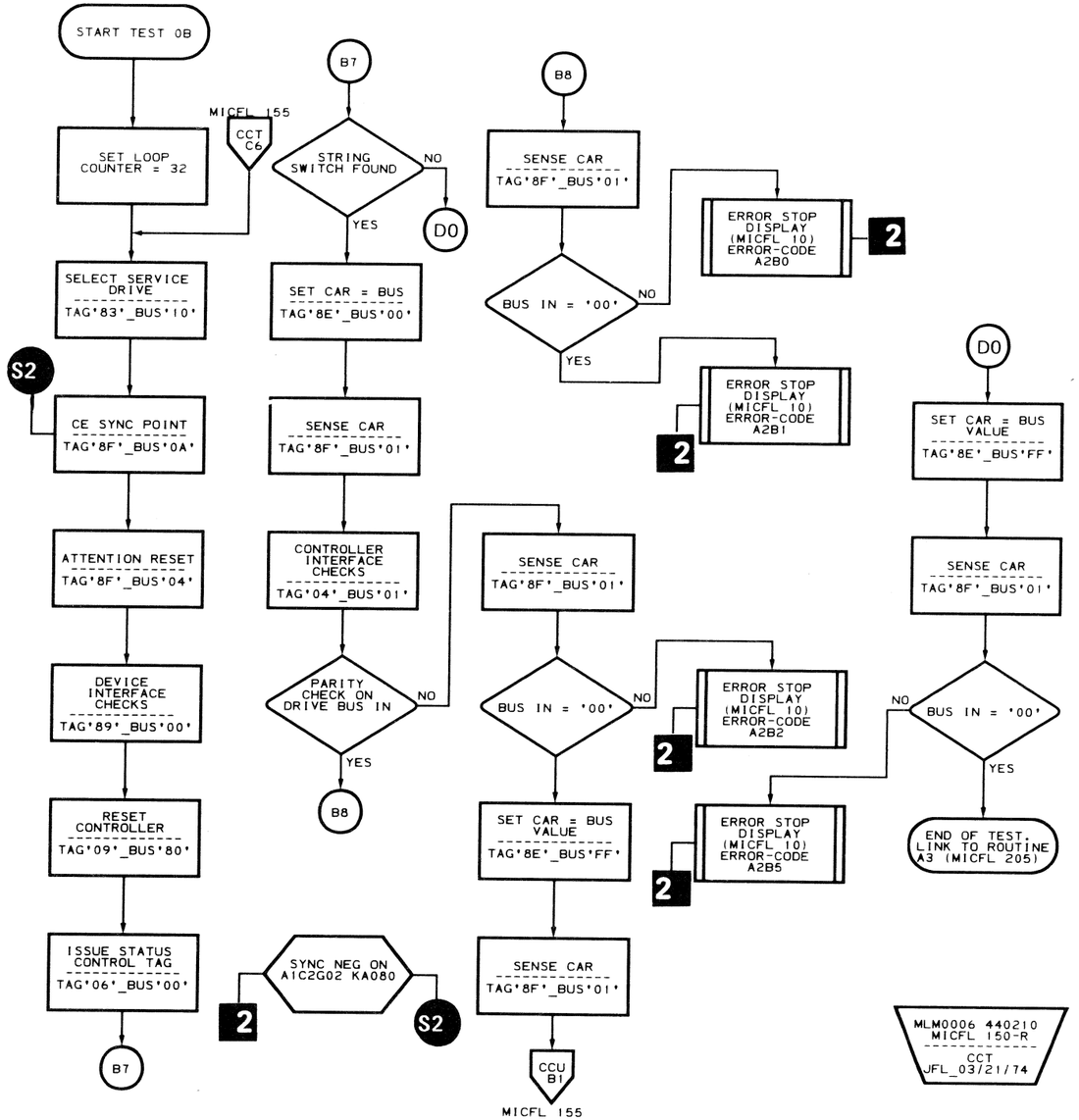

MLM0006 440210
MICFL 150-L
CCS
JFL_03/21/74

MLM0006 440210
MICFL 150-R
CCT
JFL_03/21/74

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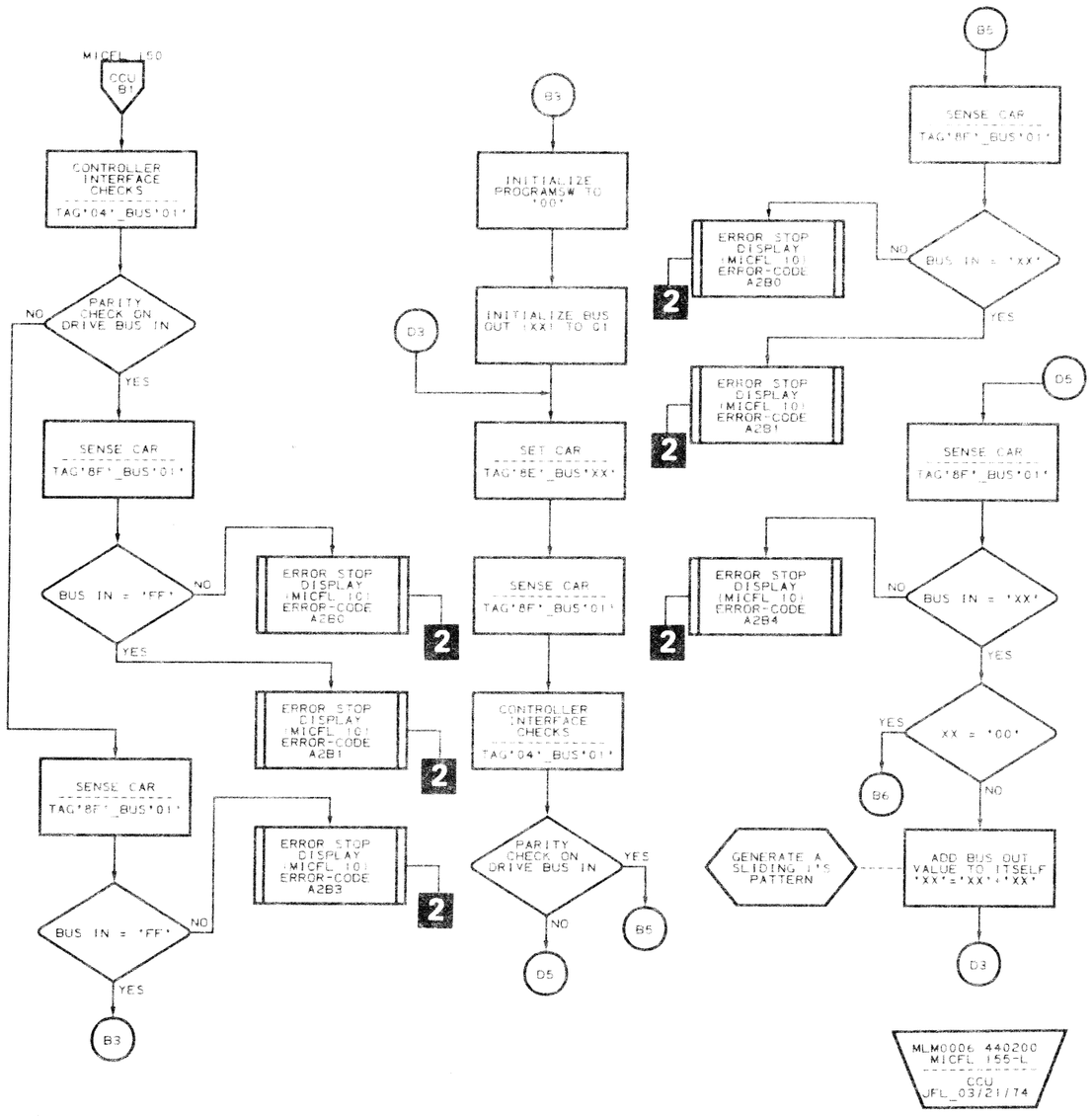

MICFL 150
CCU B1
CONTROLLER INTERFACE CHECKS
TAG'04'_BUS'01'
PARITY CHECK ON DRIVE BUS IN
NO
YES
SENSE CAR
TAG'8F'_BUS'01'
BUS IN = 'FF'
NO
YES
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B0
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B1
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B3
SENSE CAR
TAG'8F'_BUS'01'
BUS IN = 'FF'
NO
YES
B3
B3
INITIALIZE PROGRAM SW TO '00'
INITIALIZE BUS OUT 'XX' TO '01'
D3
SET CAR
TAG'8E'_BUS'XX'
SENSE CAR
TAG'8F'_BUS'01'
CONTROLLER INTERFACE CHECKS
TAG'04'_BUS'01'
PARITY CHECK ON DRIVE BUS IN
YES
NO
B5
D5
B5
SENSE CAR
TAG'8F'_BUS'01'
BUS IN = 'XX'
NO
YES
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B0
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B1
ERROR STOP DISPLAY (MICFL 10) ERROR-CODE A2B4
D5
SENSE CAR
TAG'8F'_BUS'01'
BUS IN = 'XX'
NO
YES
XX = '00'
YES
NO
B6
GENERATE A SLIDING 1'S PATTERN
ADD BUS OUT VALUE TO ITSELF 'XX'='XX'+'XX'
D3
MLM0006 440200
MICFL 155-L
CCU
JFL_03/21/74
B6
PROGRAM SWITCH = 0
YES
NO
DECREMENT LOOP COUNTER BY 1
SET PROGRAM SWITCH = TO 1
LOOP COUNTER = 0
NO
YES
INITIALIZE XX TO '03'
CCT C6
MICFL 150
D3
END OF TEST, LINK TO ROUTINE A3 (MICFL 205)
SYNC NEC ON A102002 *A080
S2
MICFL 150
MLM0006 440210
MICFL 155-R
CCV
JFL_03/21/74

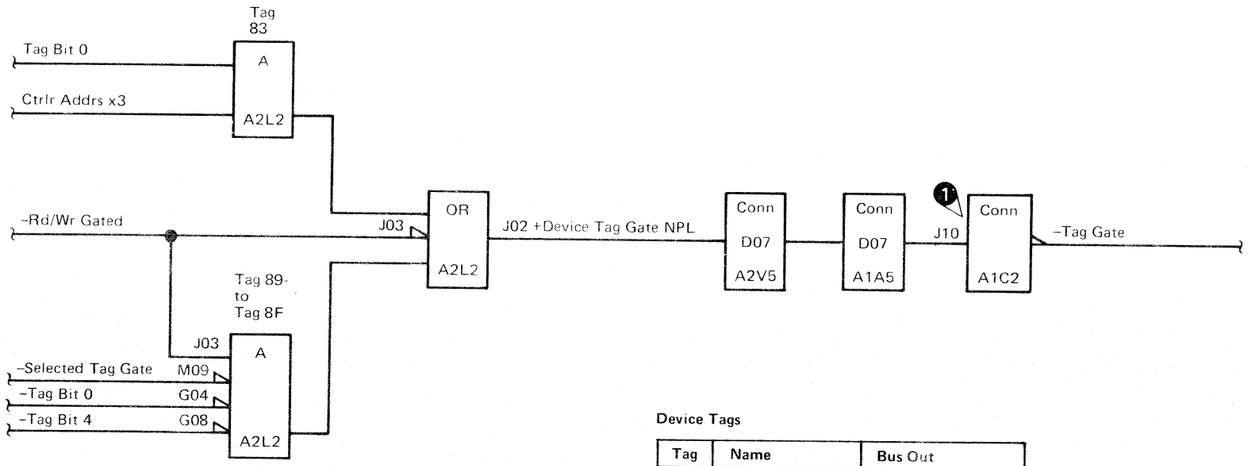
ROUTINE A2 SCOPING PROCEDURE

Loop the failing test by manually entering the test number in the parameter byte. (See MICRO 10 for procedure) Bypass errors using control option '01'; this allows the test to loop and display the error code. The test may now be started and stopped by using control option '00'.

Sync the scope externally as indicated by the MAP or the timing diagrams on MICFL 162-180. Display + NPL Tag Gate ❶ on one trace and use the other trace to display the desired scope point.

The timing diagrams on MICFL 162-180 help relate the events in the test to specific tags. Use the chart below to select the appropriate timing diagram. After an error occurs, the microprogram drops Select Hold, terminates the test, and restarts the test at the beginning.

Error Code	Timing Diagram
A210	MICFL 162
A211	MICFL 162
A212	MICFL 162
A220	MICFL 164
A221	MICFL 164
A222	MICFL 164
A223	MICFL 164
A224	MICFL 164
A225	MICFL 164
A226	MICFL 164
A227	MICFL 164
A230	MICFL 166
A231	MICFL 166
A232	MICFL 166
A233	MICFL 166
A234	MICFL 166
A235	MICFL 167
A240	MICFL 168
A242	MICFL 168
A254	MICFL 171
A270	MICFL 174
A2A0	MICFL 180



Device Tags

Tag	Name	Bus Out
'83'	Select Drive	Drive Address
'89'	Sense Interface	'00'
'8A'	Diagnostic Set	Diagnostic Control
'8B'	Set HAR	Value
'8C'	Set Diff Counter	Value
'8D'	Set Target Reg	Value
'8E'	Set CAR	Value
'8F'	Control	Control Function

Refer to OPER 100-106 for additional information.

Tag '8F' Control Function

Bus Out	Control Function
'01'	Sense CAR
'02'	Rezero
'X3'*	Sense Status
'04'	Attention Reset
'05'	Sense HAR
'08'	Seek Start
'09'	Sense Diff Ctr
'0A'	Drv Sync Tag
'0C'	Chk Reset
'0D'	Sense Target

*X = Status to be sensed

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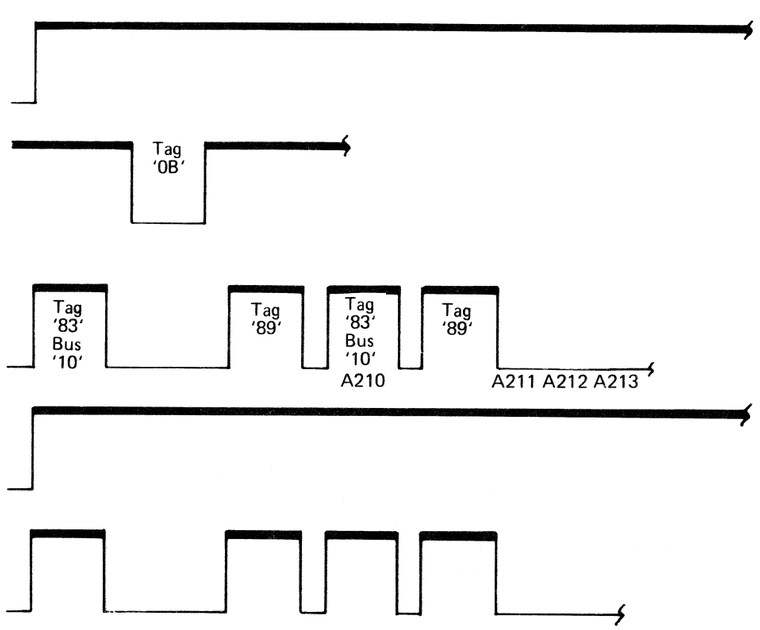
ROUTINE A2 TIMING DIAGRAM

TEST	ERROR STOP	TIMING DIAGRAMS
01 The purpose of this test is to ensure that the drive in CE Mode can select without errors.	**A210** **A211** **A212**	Sync: 10 us/div. + NPL Sel Hold A1C2G10 – MST RAS Sync Tag A2L2J11 + NPL Tag Gate A1C2J10 Associated Error Code + NPL Attn/Sel Response A1D2B03 - Drv A A1D2D07 - Drv B + NPL Tag Valid A1D2J07



* When the SCU brings up Select Hold, the Select Hold line activates all drives in the string. Therefore, Select Hold does not provide a good sync when operating in in-line mode.

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

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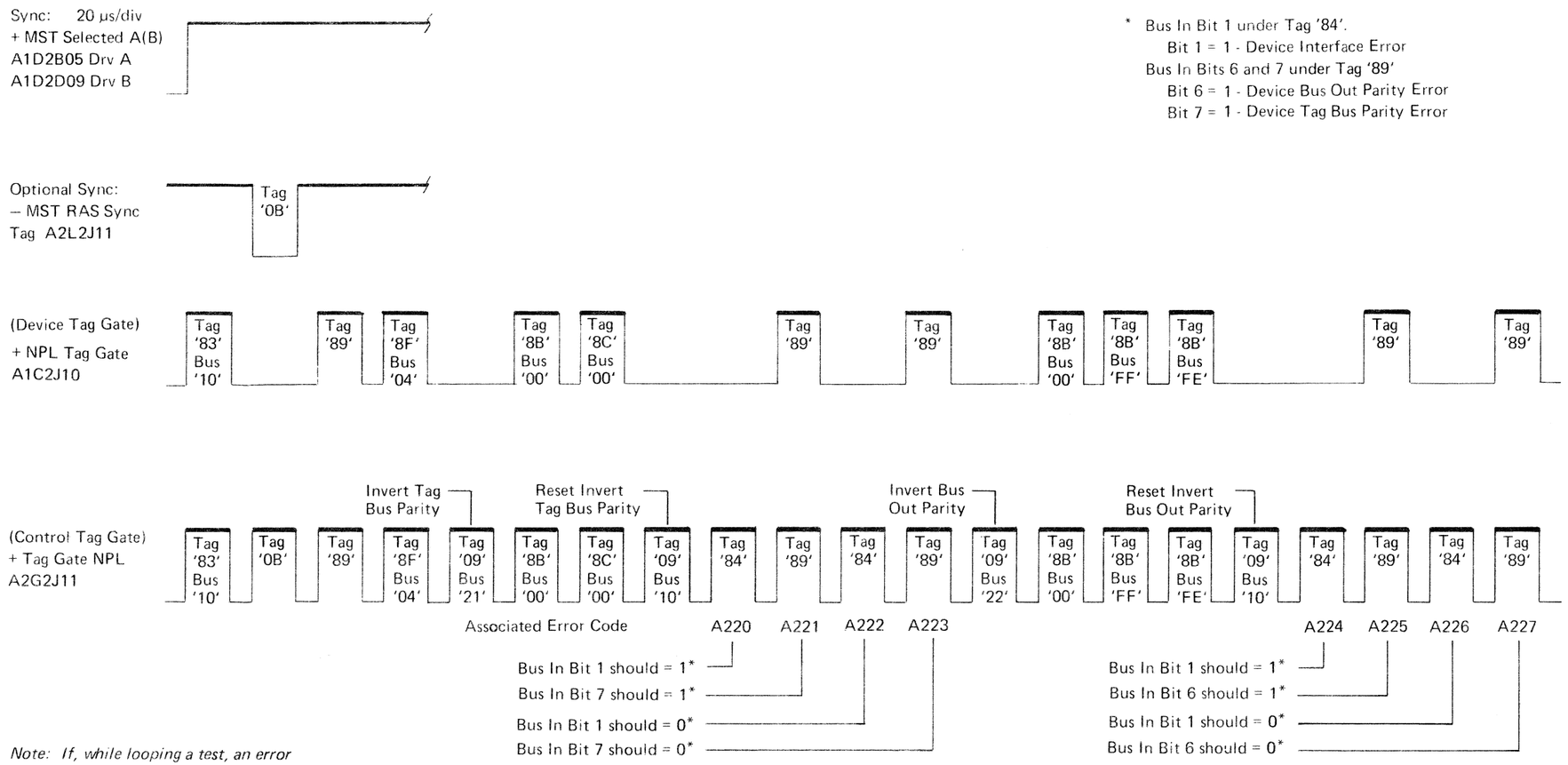
Test	Error Stop
02 The purpose of this test is to force and reset: 1. Dev. Intf. Error 2. Dev Tag Bus Parity Error 3. Dev Bus Our Parity Error	**A220** **A221** **A222** **A223** **A224** **A225** **A226** **A227**

Timing Diagram



* Bus In Bit 1 under Tag '84'.
Bit 1 = 1 - Device Interface Error
Bus In Bits 6 and 7 under Tag '89'
Bit 6 = 1 - Device Bus Out Parity Error
Bit 7 = 1 - Device Tag Bus Parity Error

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

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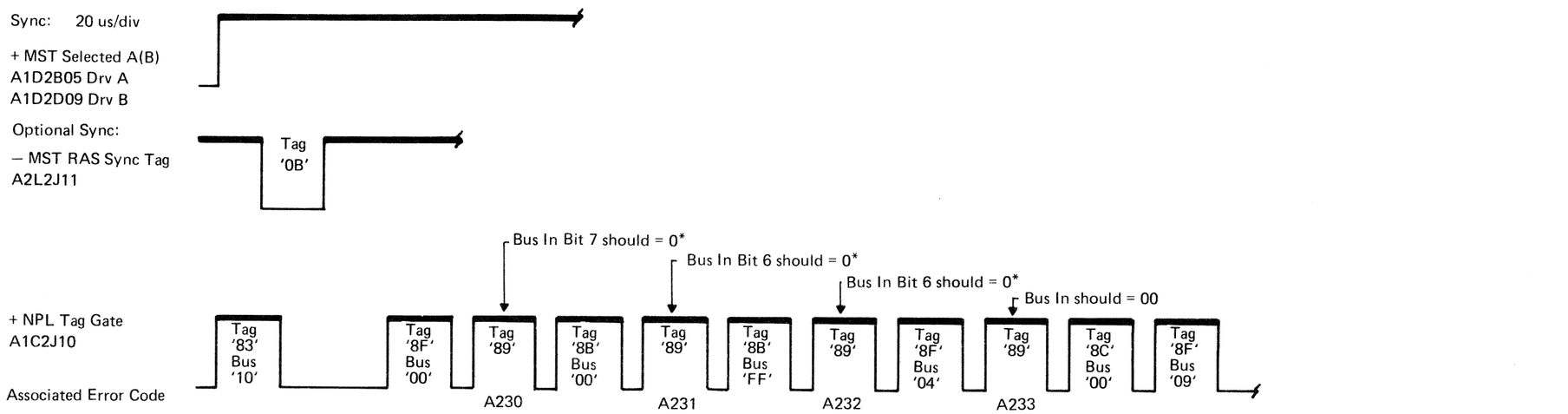
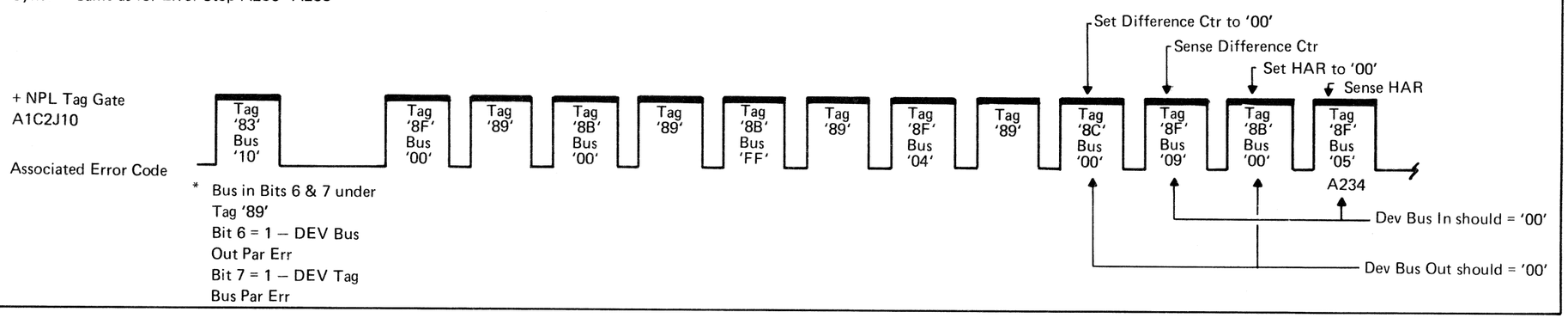
ROUTINE A2 TIMING DIAGRAM

TEST	ERR STOP	TIMING DIAGRAMS
03 The purpose of this test is to ensure that: 1. Device Tag Bus 2. Device Bus Out 3. Device Bus In are functioning properly.	**A230** **A231** **A232** **A233**	
	A234	

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

CA0166 Seq. 1 of 2	2747047 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74			

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TEST	ERROR STOP	TIMING DIAGRAMS
03	A235	Sync: Same as for Error Stop A230–A233 + NPL Tag Gate A1C2J10 Associated Error Code Tag '83' Bus '10' Tag '8F' Bus '00' Tag '89' Tag '8B' Bus '00' Tag '89' Tag '8B' Bus 'FF' Tag '89' Tag '8F' Bus '04' Tag '89' Tag '8C' Bus '00' Tag '8F' Bus '09' Tag '8C' Bus 'FF' Tag '8F' Bus '09' Tag '8B' Bus 'FF' Tag '86' Bus '05' A235 Set Diff Ctr to 'FF' Sense Diff Ctr Set HAR to 'FF' Sense HAR Dev Bus In should = 'FF' Dev Bus Out should = 'FF'

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

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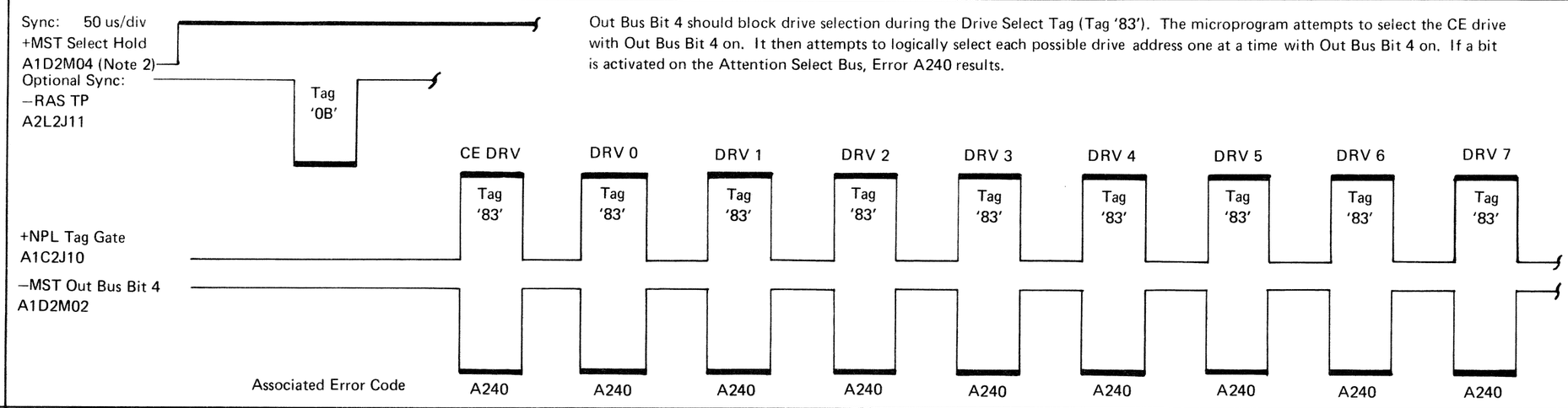
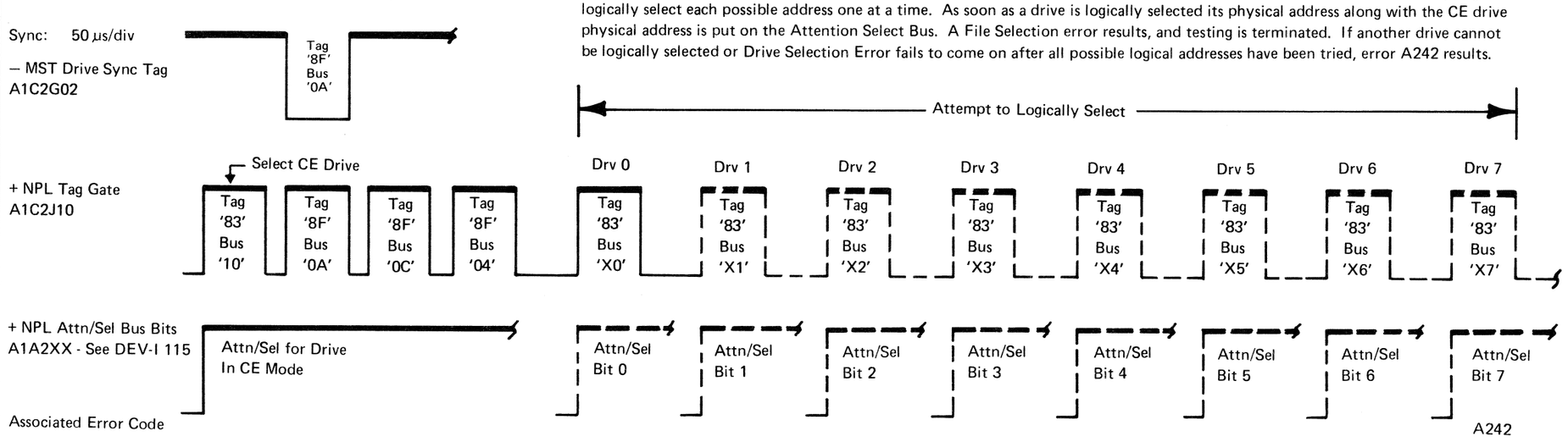
ROUTINE A2 TIMING DIAGRAM

TEST	ERROR STOP	TIMING DIAGRAM
04 The purpose of this test is to ensure that: 1. Drive selection can be blocked. 2. File selection error can be forced.	**A240**	 Out Bus Bit 4 should block drive selection during the Drive Select Tag (Tag '83'). The microprogram attempts to select the CE drive with Out Bus Bit 4 on. It then attempts to logically select each possible drive address one at a time with Out Bus Bit 4 on. If a bit is activated on the Attention Select Bus, Error A240 results.
	A242	 The microprogram attempts to force a File Selection Error (1 of 8 Check) by selecting the drive in CE Mode and then attempting to logically select each possible address one at a time. As soon as a drive is logically selected its physical address along with the CE drive physical address is put on the Attention Select Bus. A File Selection error results, and testing is terminated. If another drive cannot be logically selected or Drive Selection Error fails to come on after all possible logical addresses have been tried, error A242 results.

Note 1: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

Note 2: When the storage control brings up Select Hold, the Select Hold line becomes active in all drives in the string. Therefore, Select Hold does not provide a good sync when operating in inline mode.

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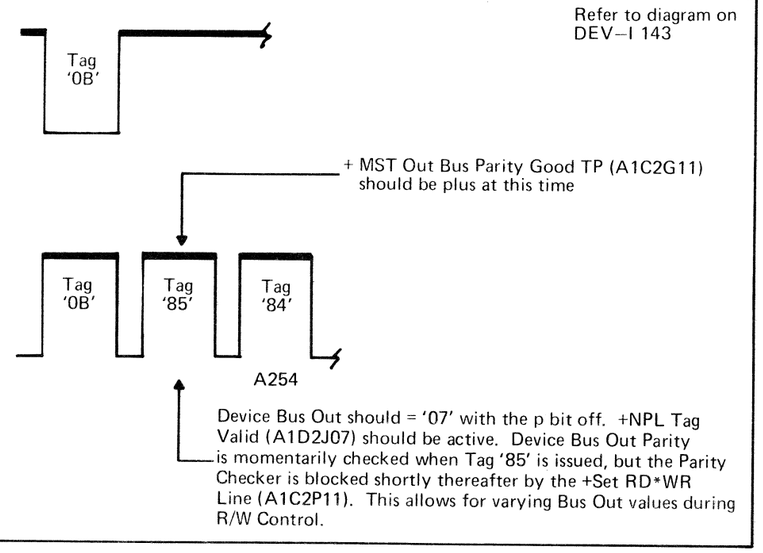
ROUTINE A2 TIMING DIAGRAM

TEST	ERROR STOP	TIMING DIAGRAM
05	A254	Sync 10 µs/div A2L2J11 –MST RAS Sync Tag + Tag Gate NPL A2G2J11



Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

CA0168 Seq. 2 of 2	2747048 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74			

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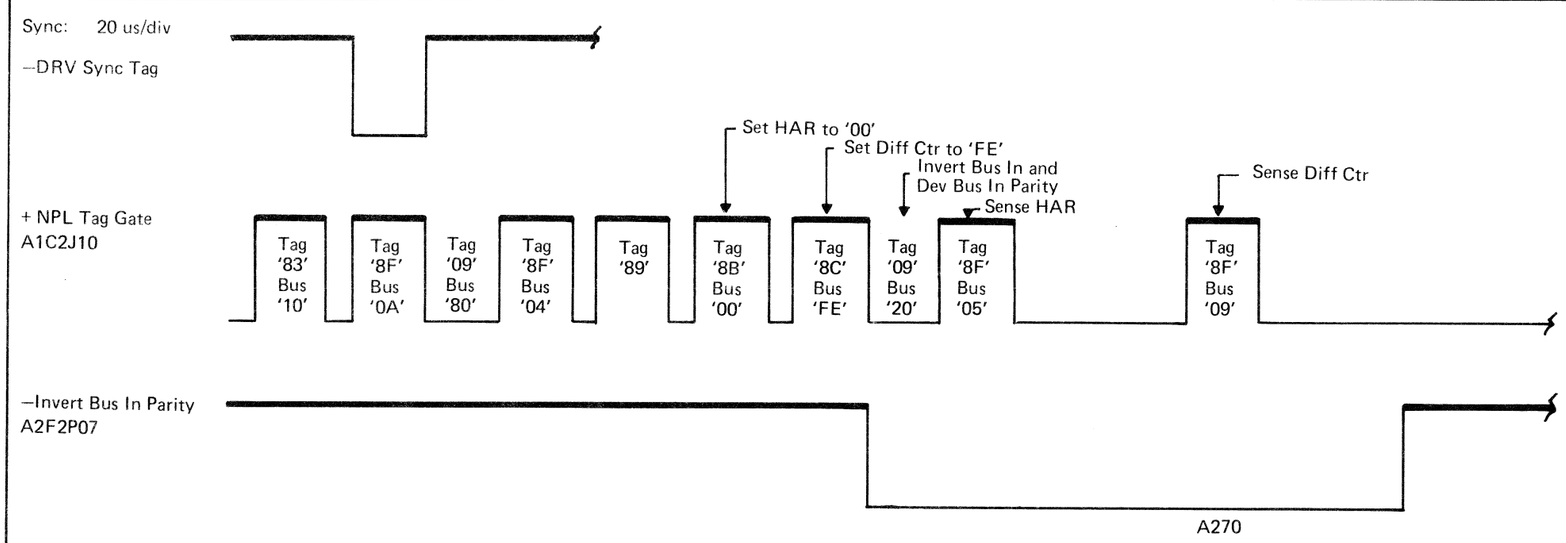
ROUTINE A2 TIMING DIAGRAM

TEST	ERROR STOP	TIMING DIAGRAMS
07 The purpose of this test is to ensure that Device Bus In Parity Check can be forced and reset.	A270	

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

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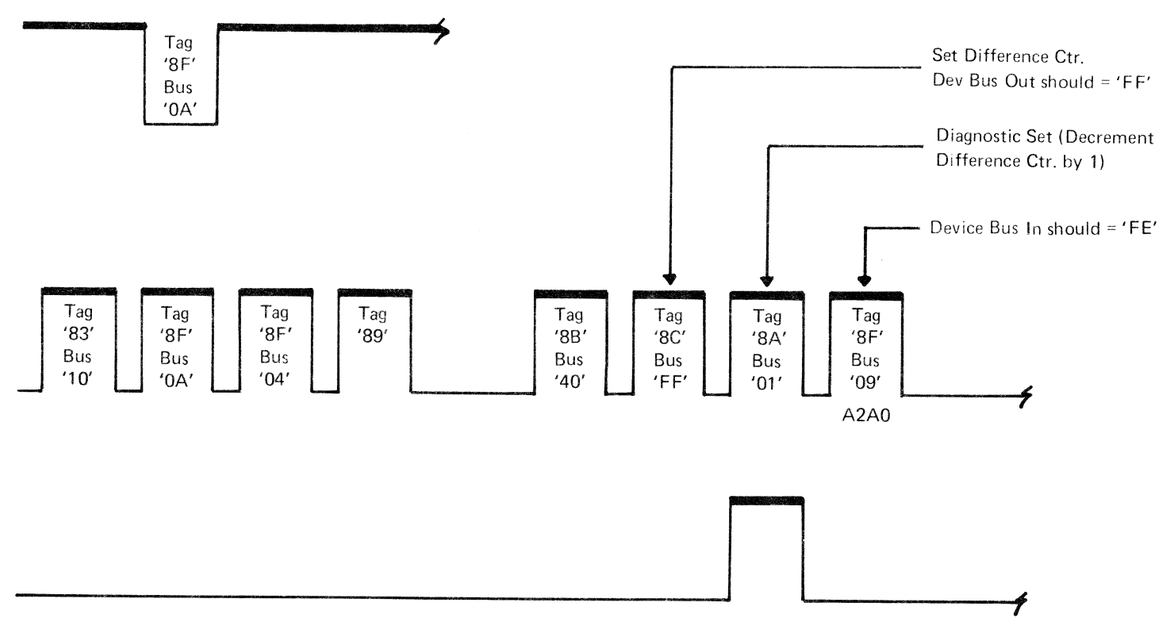
ROUTINE A2 TIMING DIAGRAM

TEST	ERROR STOP	TIMING DIAGRAM
0A The purpose of this test is to ensure that the diagnostic set command decrements the Difference Counter	**A2A0**	

Note: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

CA0174 Seq. 2 of 2	2747049 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74			

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ROUTINE A3 – DATA MODULE CONTROL LOGIC TESTS

DESCRIPTION

Test 01. Data Module Status

Test 01 verifies that correct status (X'60') is returned after mounting a data module on the 3340 Drive and that there are no outstanding attentions after issuing an Attention Reset command to the drive.

Test 02. Access Timer Accuracy

Test 02 verifies that the Access Timeout check is active if a Seek Start command is issued where the access control is forced into zero mode. The access timer starts running and times-out in 180 milliseconds, plus or minus 40 milliseconds. The test also verifies that correct status is generated by the access timeout condition.

Test 03. Recalibration

Test 03 verifies that the 3340 Drive does rezero when Busy status is received during the Rezero operation and that Seek Complete status is received 220 milliseconds after the Rezero command has been issued. The test also verifies that the Rezero command resets to zero both the Head Address Register (HAR) and the Difference Counter.

Test 04. No-Motion Seek

Test 04 verifies that a Seek Complete status is present immediately after issuing a Seek Start command with the HAR and the Difference Counter both set to zero. The test also verifies that an Attention from the Seek Complete is generated when polling the device (Tag '82' Bus 'X4').

Test 05. Unsuppressible Register

Test 05 verifies that when sensing for the physical address, the device address returned matches that returned from a polling device operation with the Unsuppressible Register active. The test first checks to see if the Unsuppressible Register was set on by the customer prior to executing the test. If so, the register is reset, tested, and then restored to its original value. If the Unsuppressible Register is off, then the test sets it on, tests it, and then restores it to the original value.

Test 06. Set Read/Write Tag

Test 06 verifies that Set Read/Write Tag '85' operates error-free and a Normal End response is received 500 microseconds after issuing the tag. The test also verifies that Normal End is reset with a Response.

Test 07. Force No-PLO Input Error

Test 07 verifies that the No-PLO Input error can be forced on and then reset. The test also tests for other errors caused by the No-PLO Input error condition.

Test 08. Servo Off-Track Error Verification

Test 08 verifies that the Servo Off-Track error check logic is operable. This error generates a Drive Check, a Read/Write Capable/Enable, and a Read/Write check. The test also verifies that Index check is present when forcing the Servo Off-Track error (method 1). The test uses two methods for forcing a Servo Off-Track error:

1. Set Read/Write latch on with access not on-track by issuing a Rezero command.
2. Set the Read/Write latch on with the servo in zero mode.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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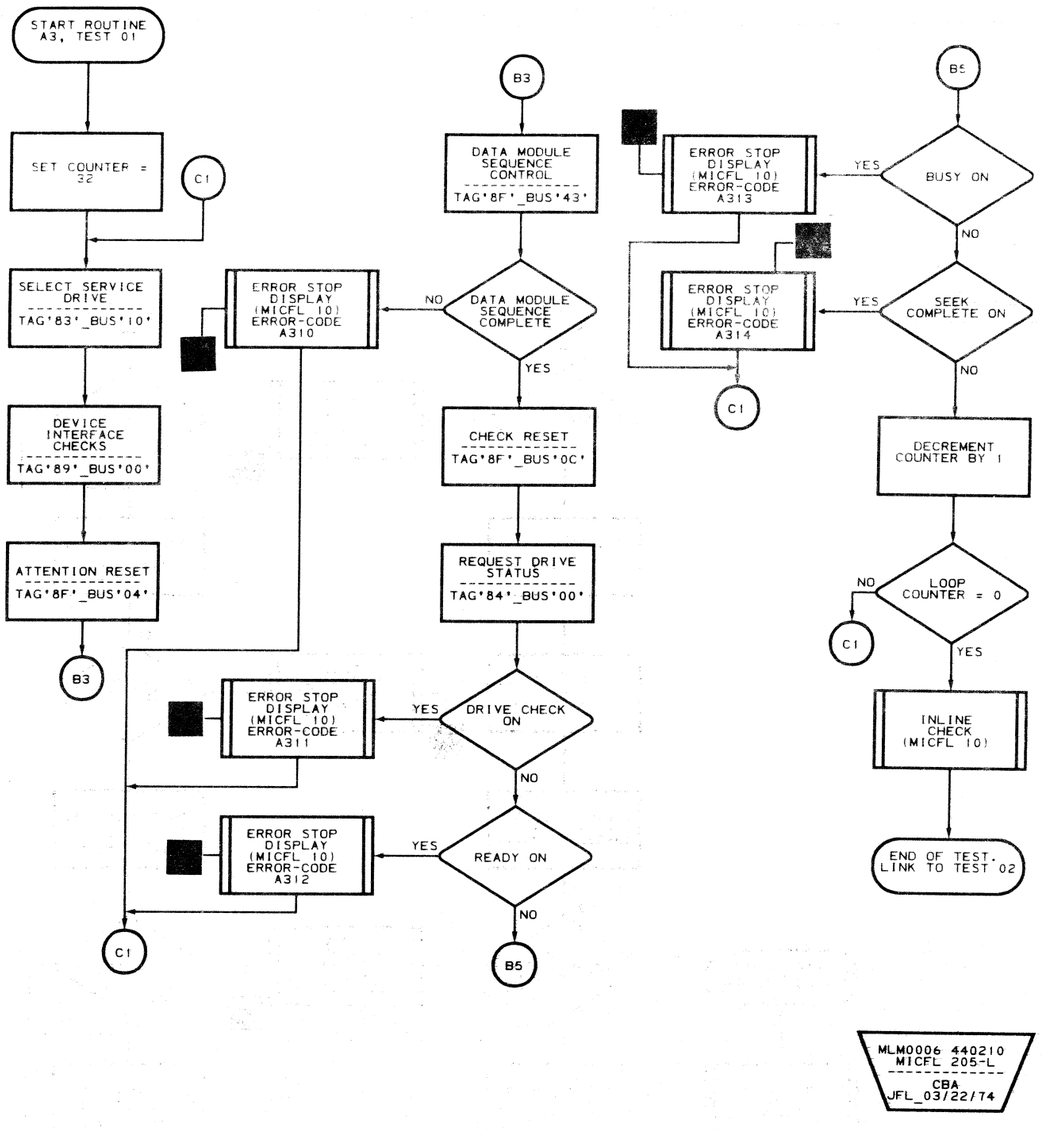
DATA MODULE STATUS (Routine A3)



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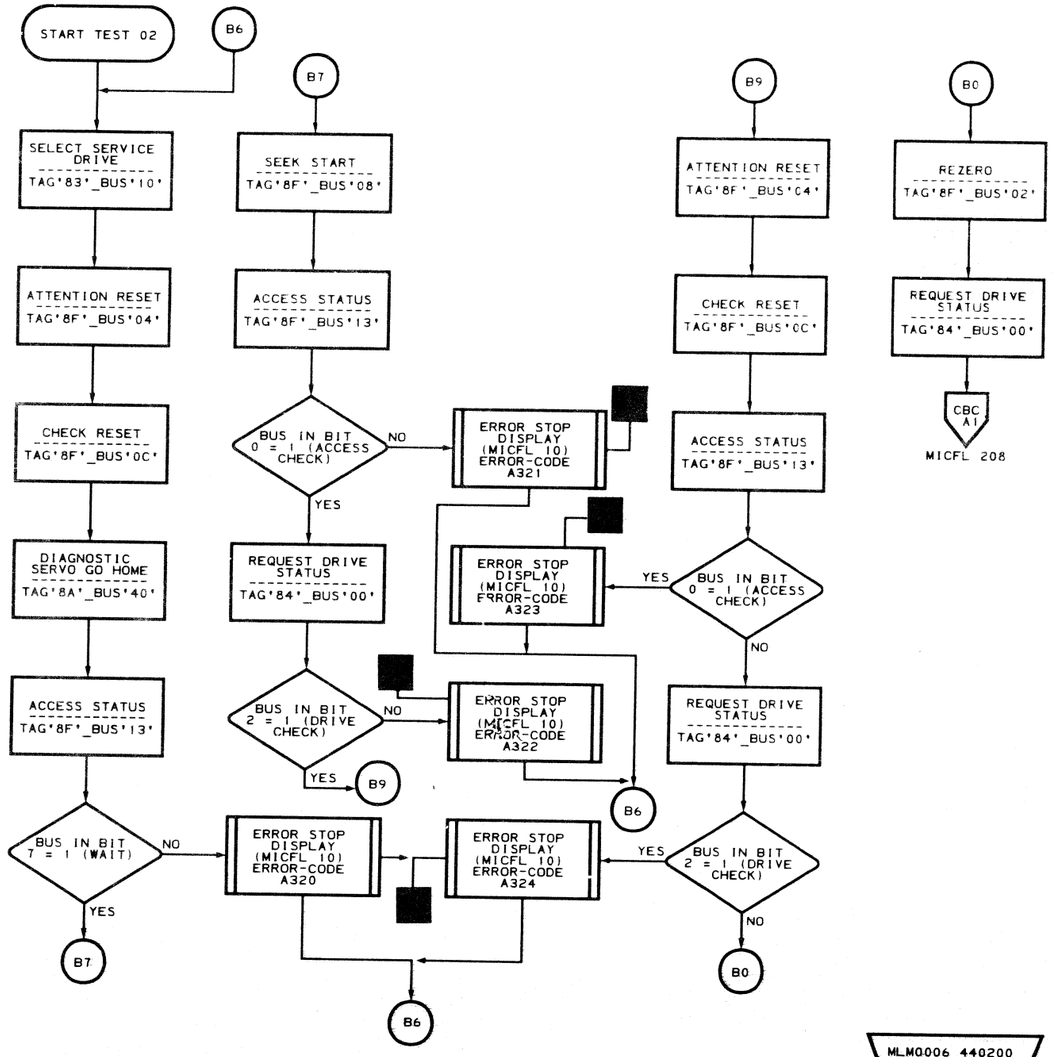
JFL_03/22/74



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CBB
JFL_03/22/74

CA0205 Seq. 1 of 2	2747050 Part No.( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74			

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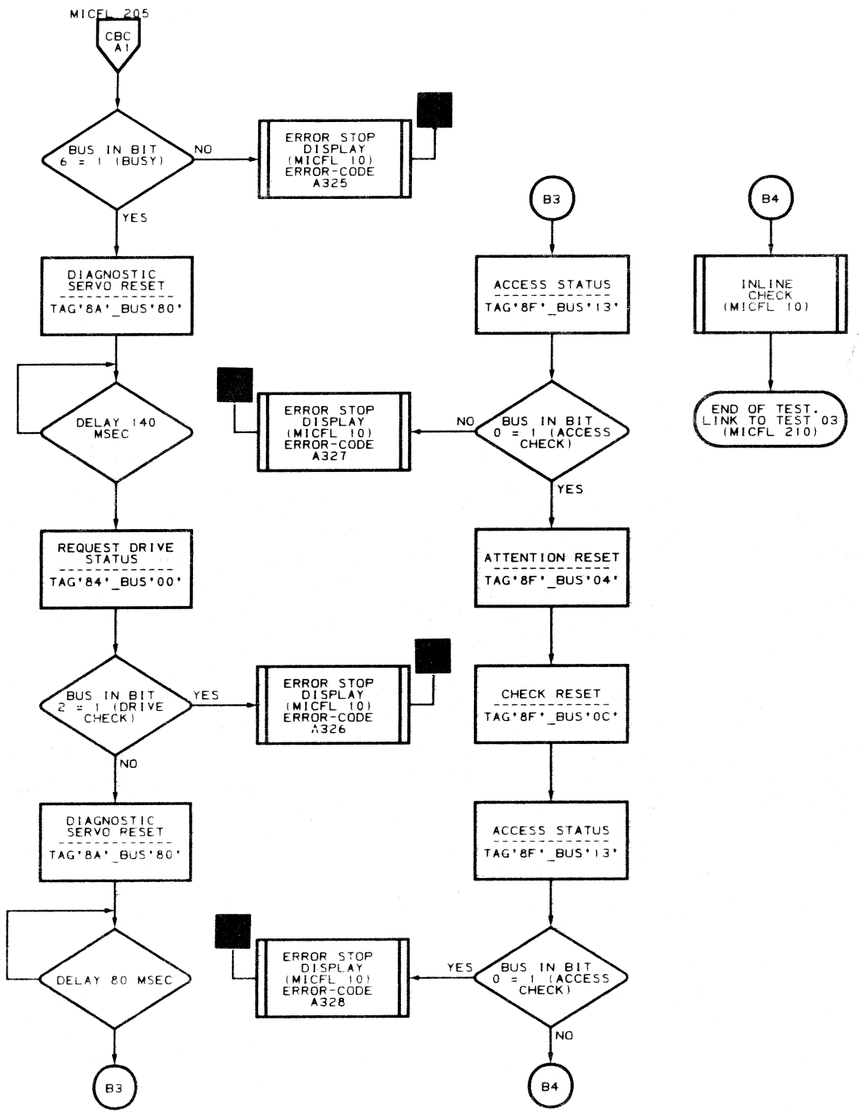
DATA MODULE STATUS (Routine A3)



MLM0006 440200
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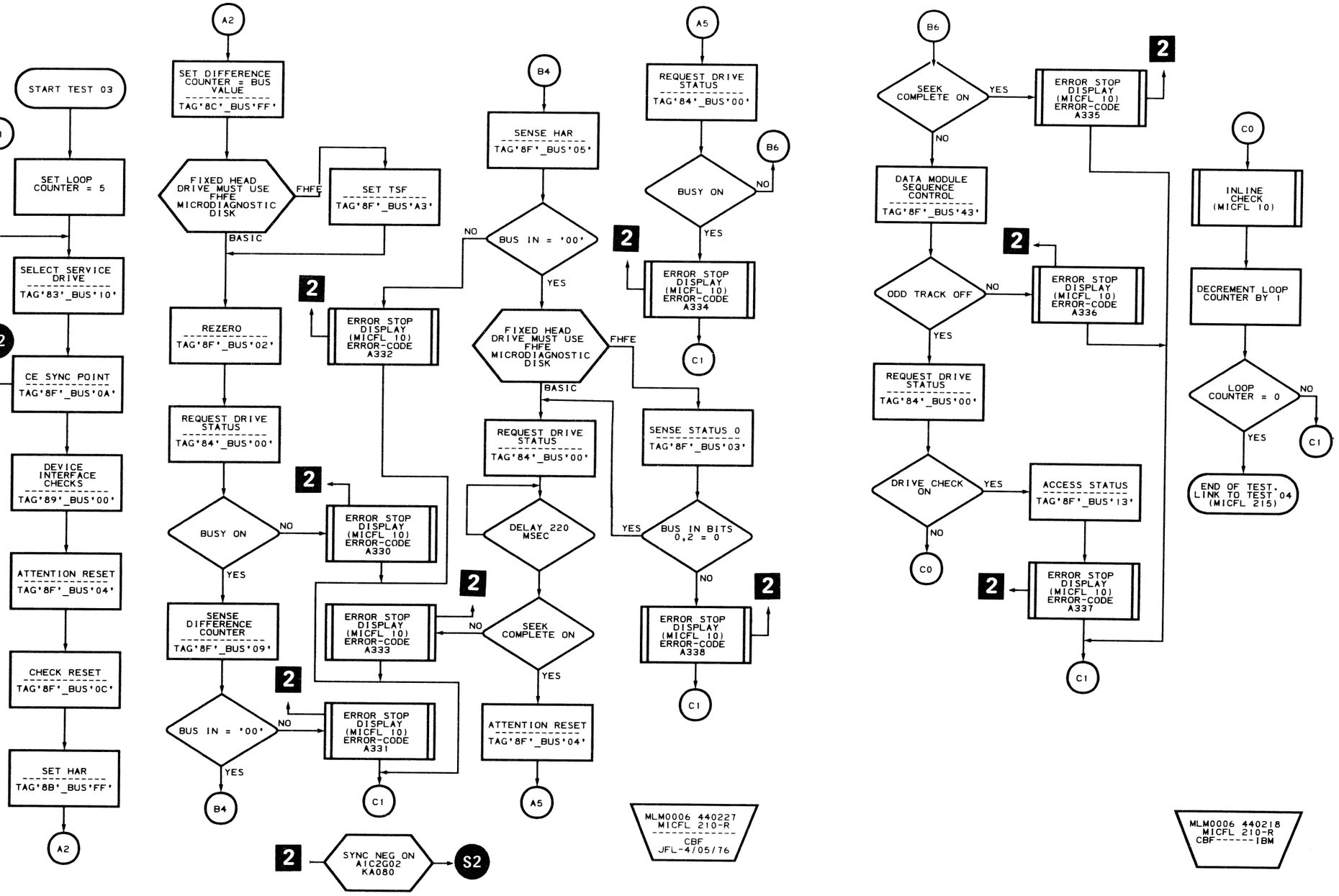
RECALIBRATE (Routine A3)



CA0210 Seq. 1 of 2	2747052 Part No.(N)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440218 5 Aug 74	440227 14 Sept 76	

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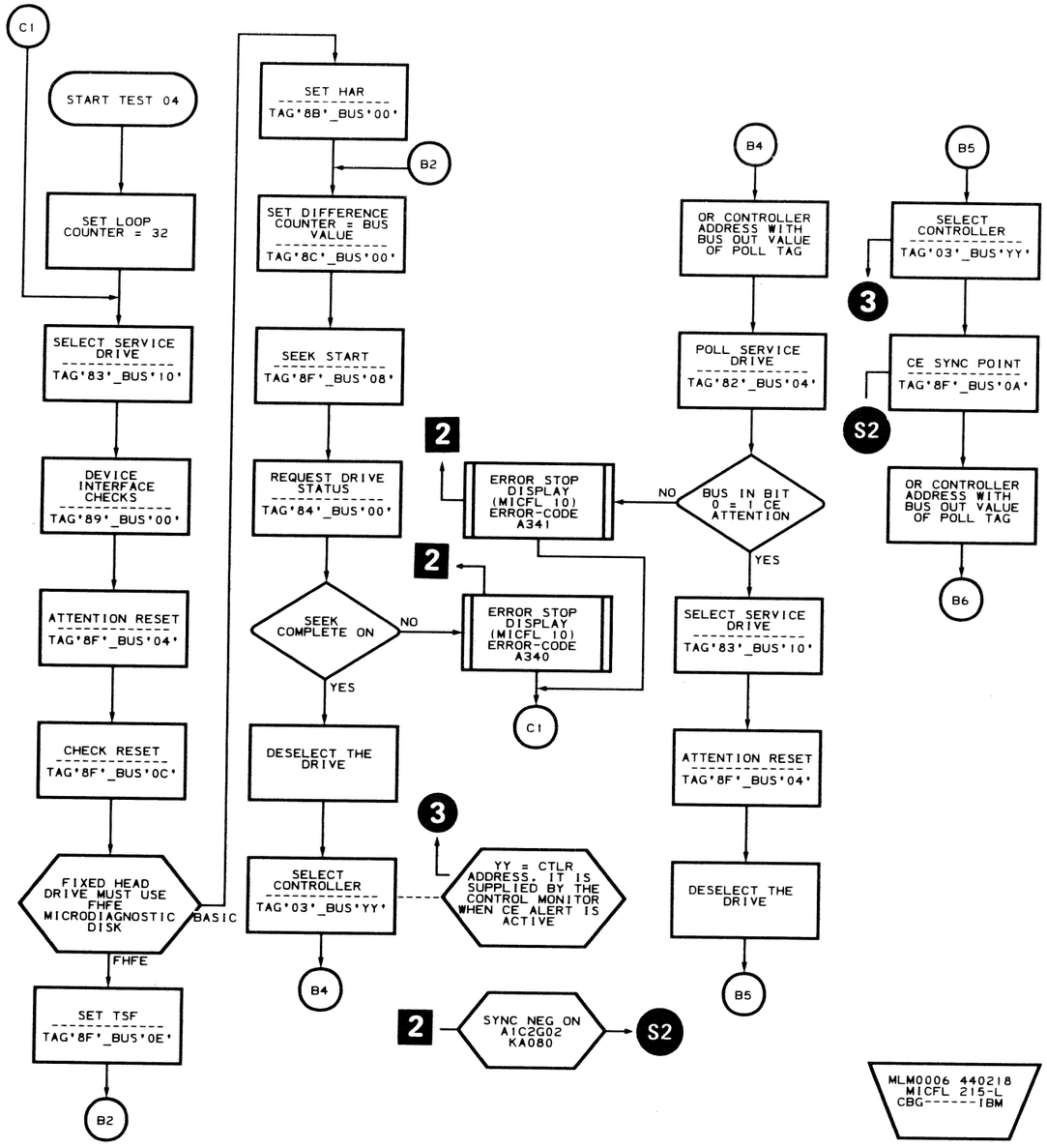
NO MOTION SEEK (Routine A3)



CA0210 Seq. 2 of 2	2747052 Part No.(N)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440218 5 Aug 74	440227 14 Sept 76	

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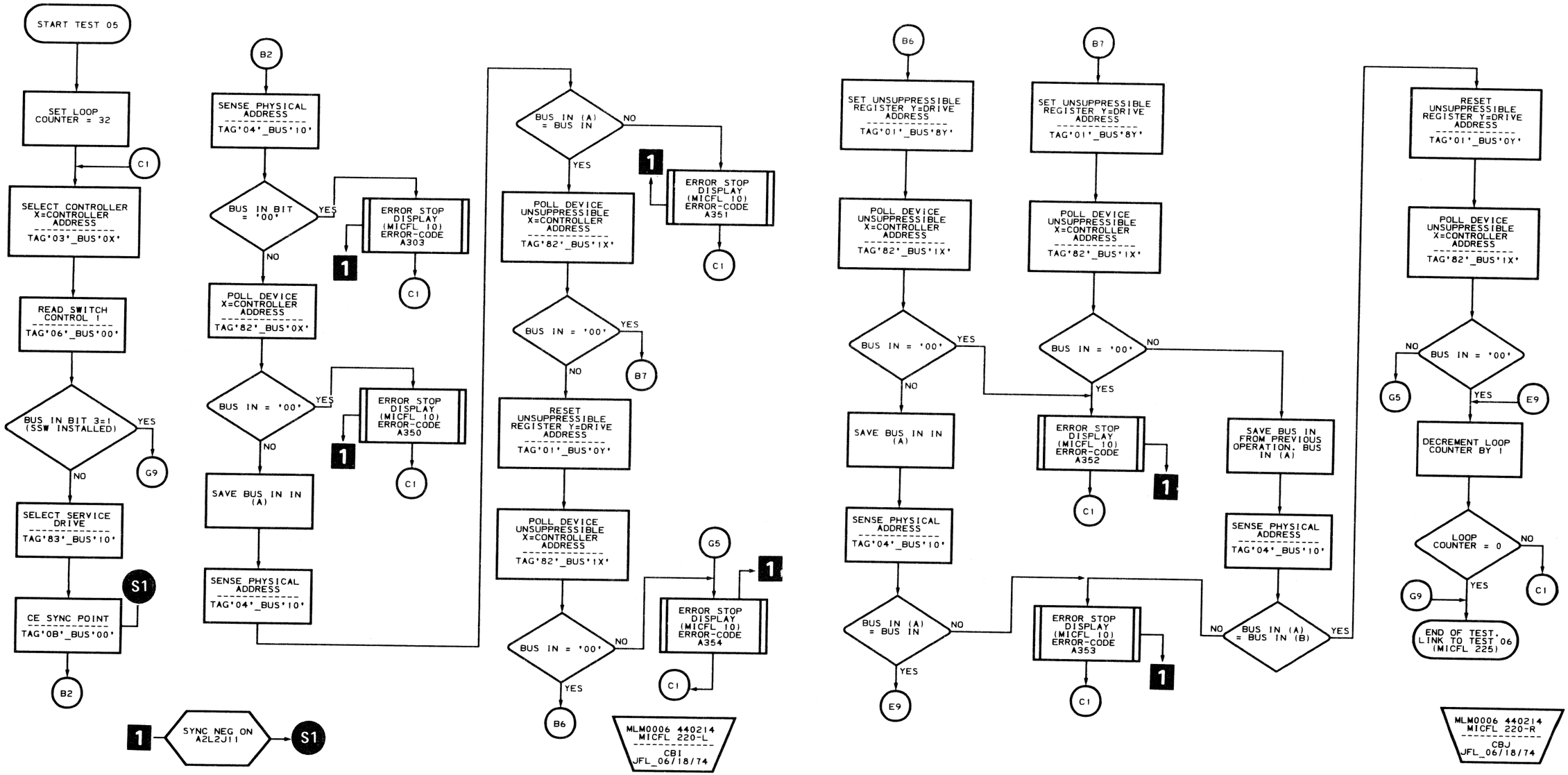
UNSUPPRESSABLE REGISTER TEST (Routine A3)



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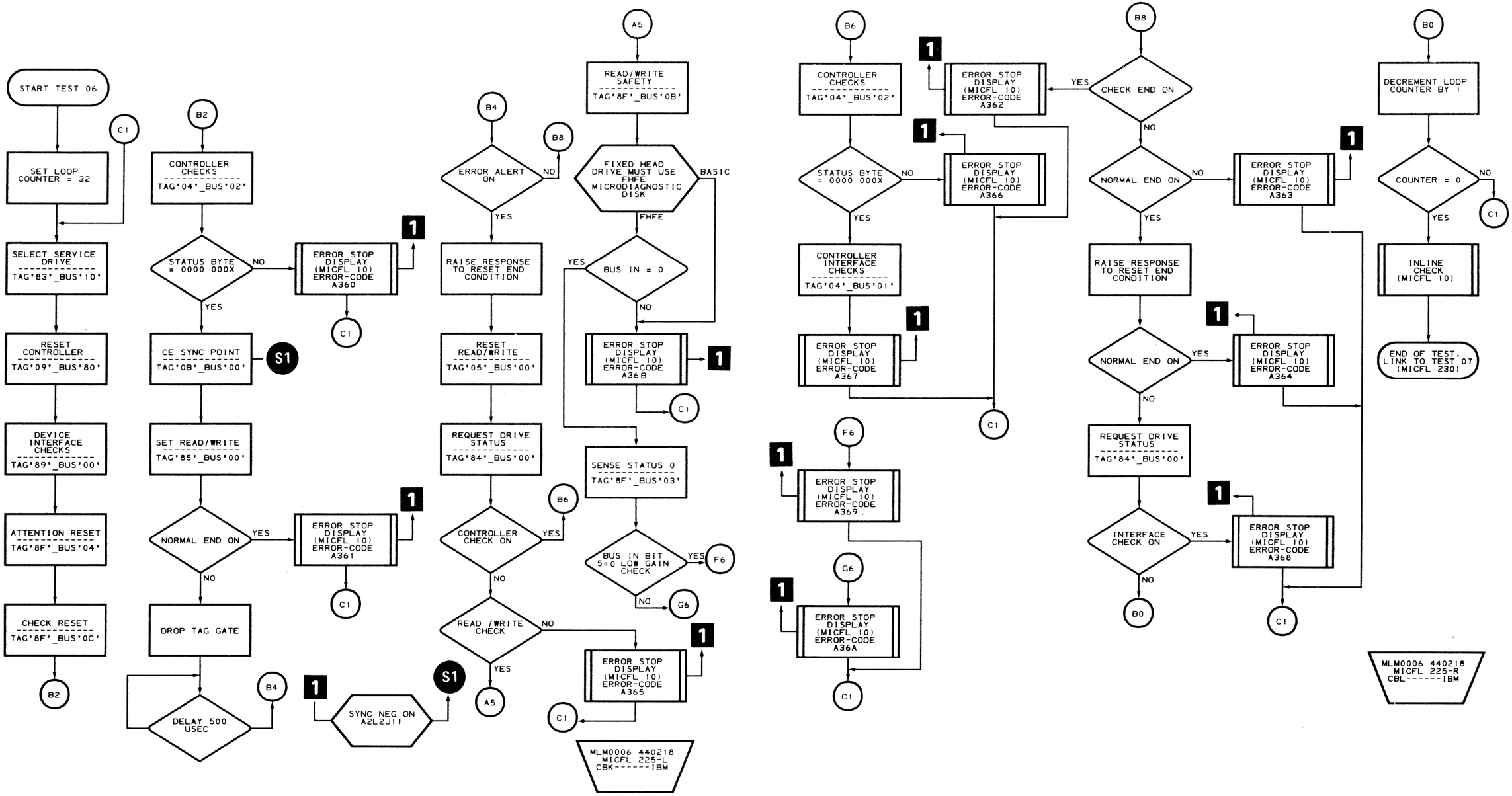

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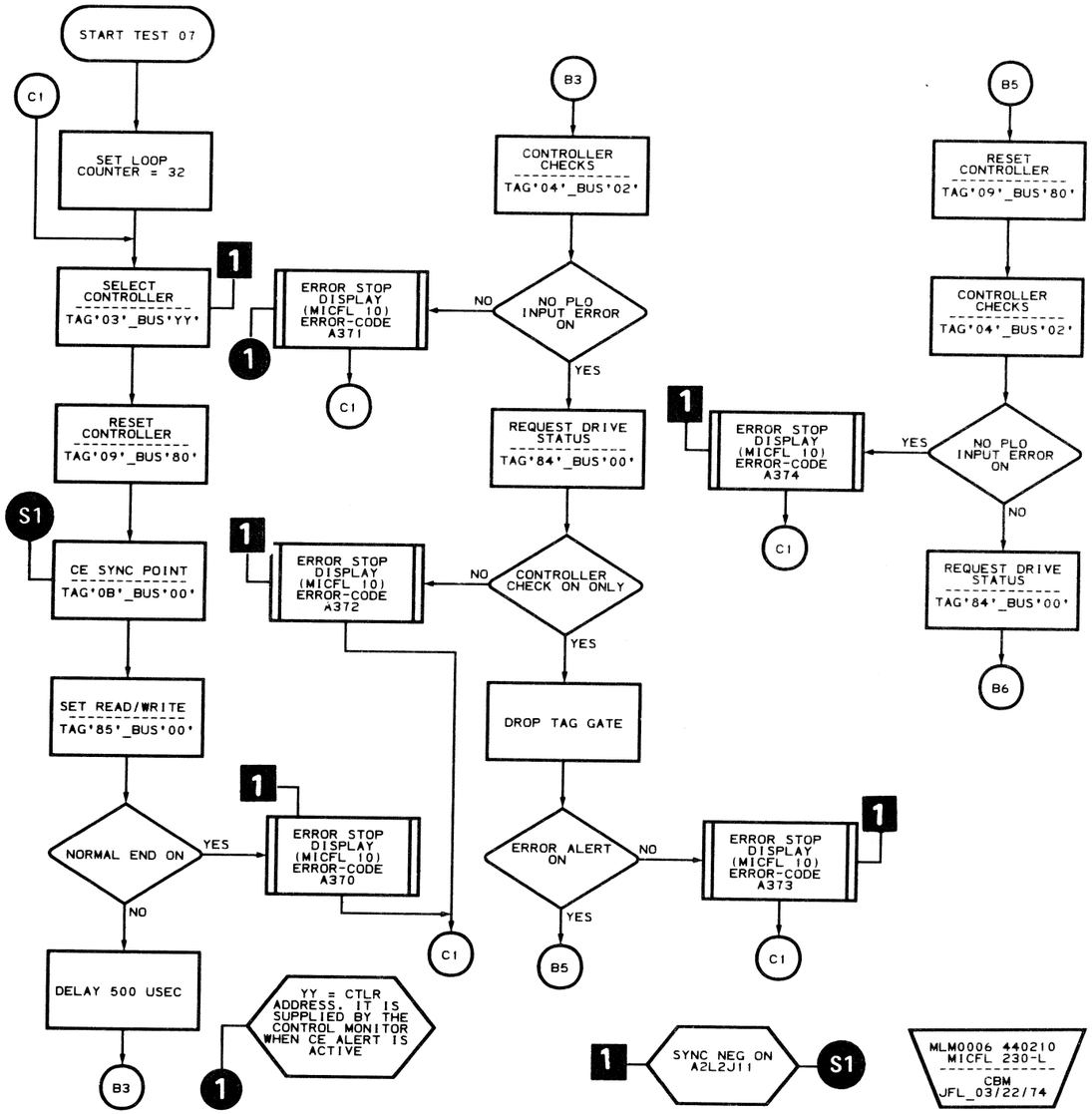
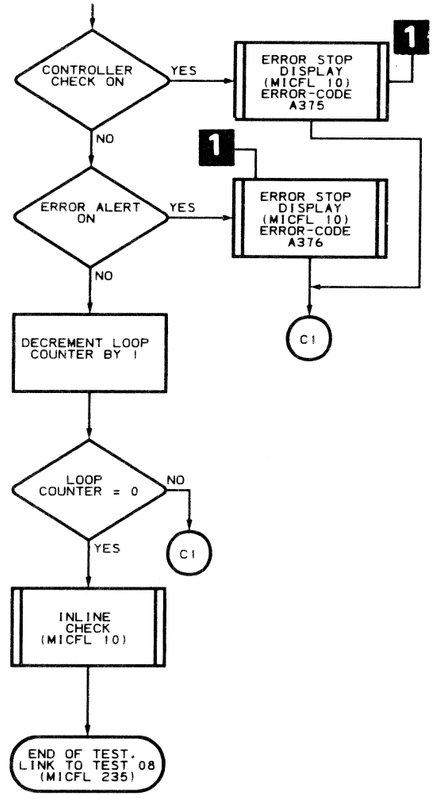
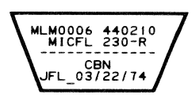
'NO PLO INPUT' CHECKER TEST (Routine A3)







CA0230 Seq. 1 of 2	2747054 Part No.(N)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440227 14 Sept 76		

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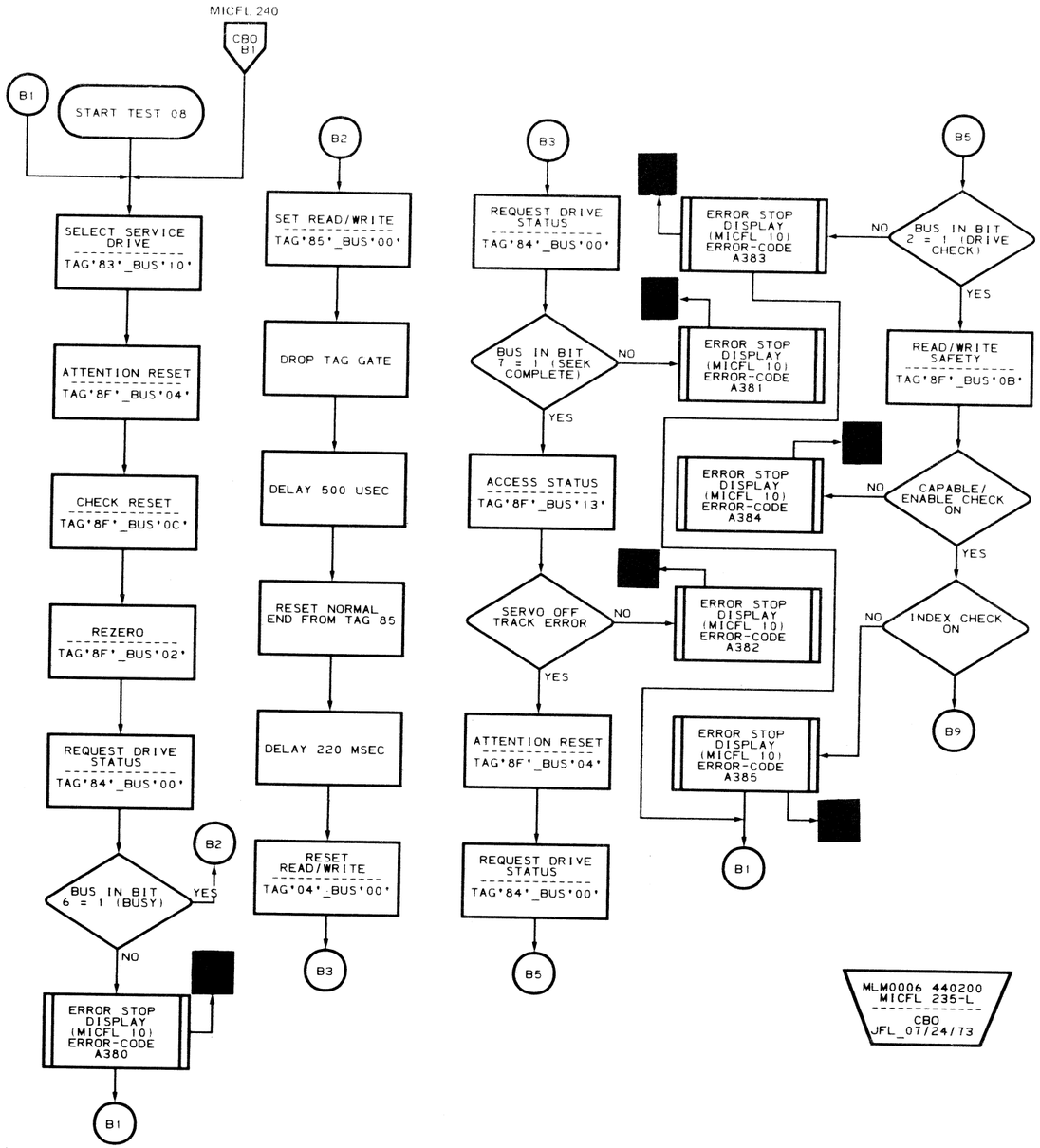
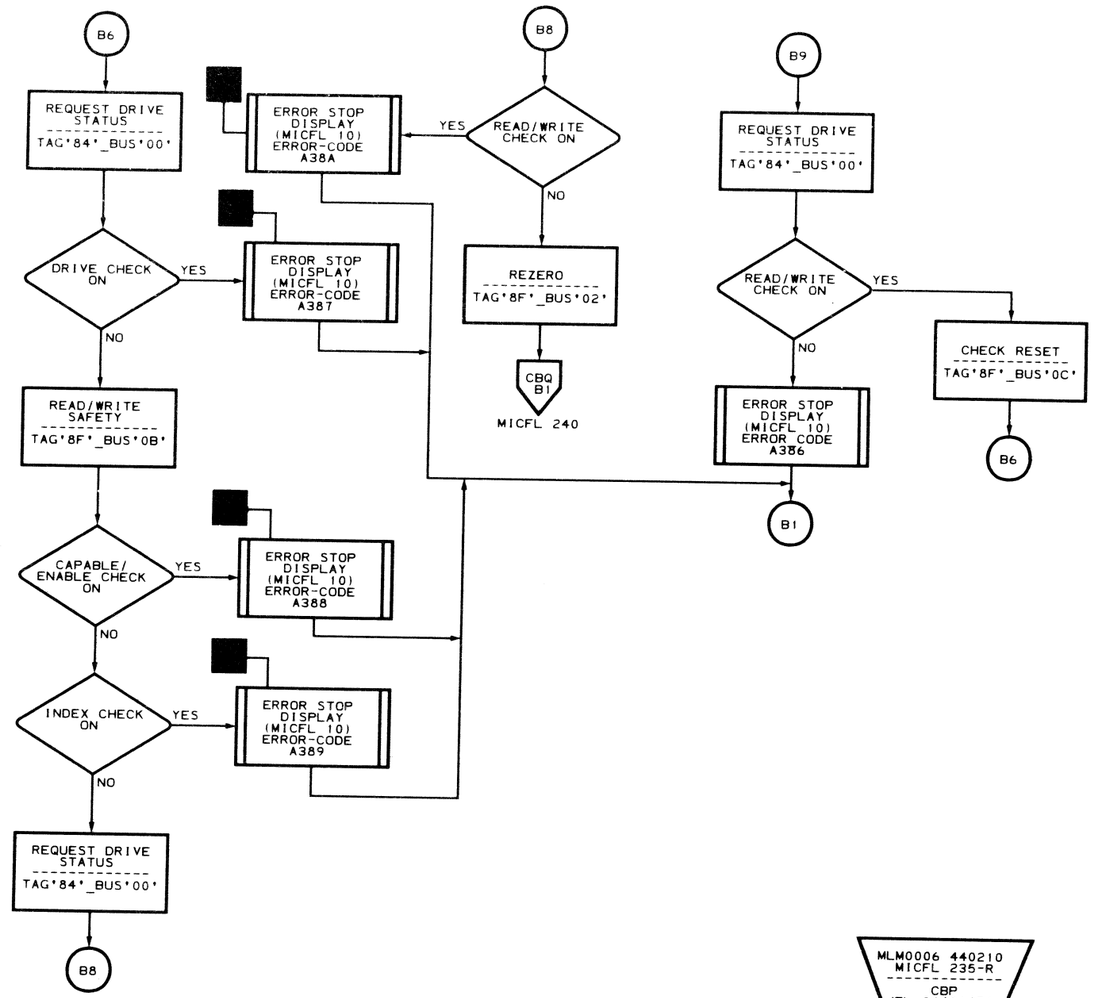
SERVO OFF – TRACK ERROR VERIFICATION (Routine A3)





CA0230 Seq. 2 of 2	2747054 Part No.(N)	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440227 14 Sep 76	440227 14 Sept 76	

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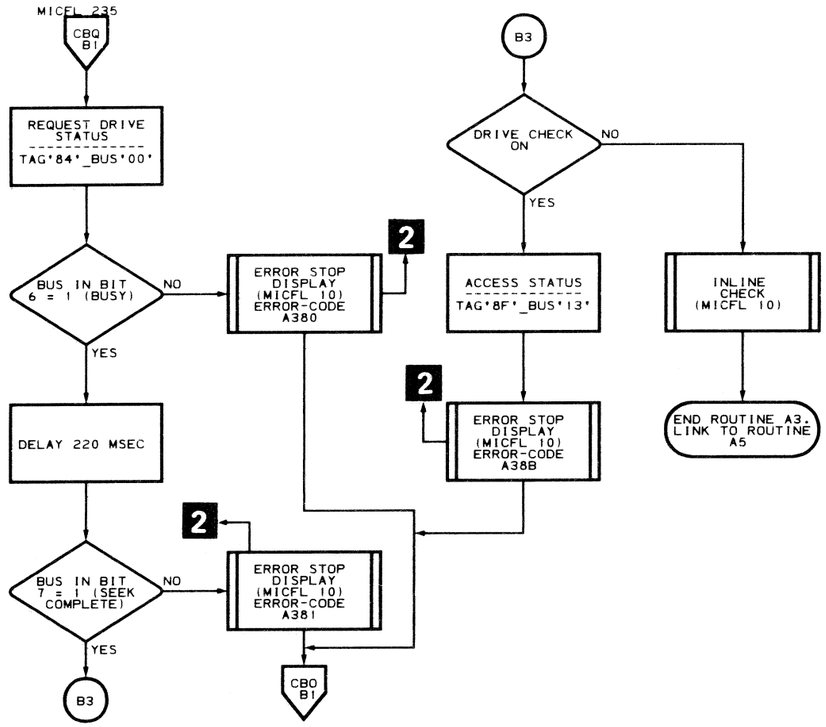
TEST 08 (Routine A3)

MICFL 240



MICFL 235

CA0240 Seq. 1 of 2	2747055 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440218 5 Aug 74		

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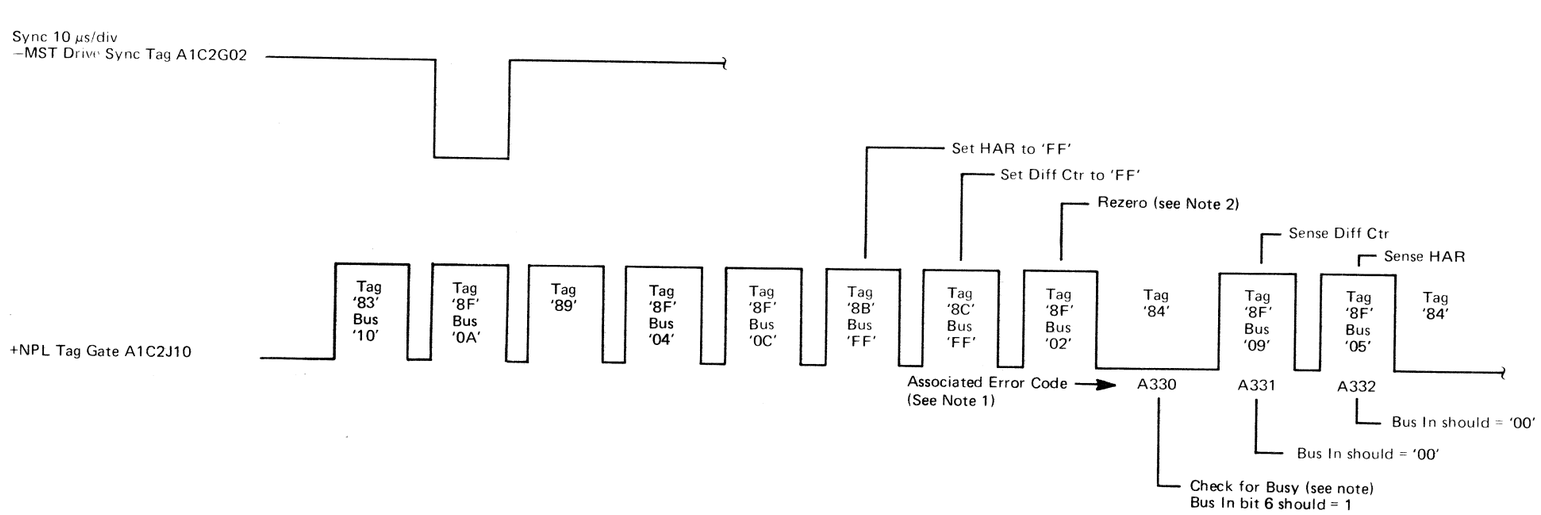
MICFL 240

ROUTINE A3 TEST 3 SCOPING PROCEDURE

1. Load routine A3.
2. Loop test 3 and bypass errors. Enter 10, 03, 01, 00. This allows the test to loop and display the error code. The test may be started and stopped by using control option '00'.
3. Sync the scope externally as indicated in the MAP or on the timing diagram below.
4. Display +NPL Tag Gate on one trace and use the other trace to display the desired scope point. The timing diagram helps relate the events in the test to specific tags. After an error occurs, the test is terminated and the microprogram drops Select Hold. Go back to the beginning of the test and start over again.

Routine A3 Test 3 Timing Diagram



Note 1: If, while looping a test, an error occurs, the microprogram drops Select Hold and terminates the test. The test is then started over again from the beginning. If any Tag Gate pulses appear after an error occurs and before the test is restarted, they are not applicable to this diagram.

Note 2: Rezero activates Busy and resets HAR and the Difference Counter.

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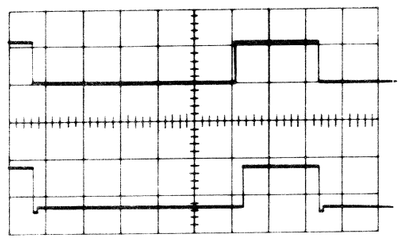
Test 6 performs a Set Read/Write Op 85 and then tests to ensure that it is handled as an Extended Operation; that is, Normal End is not received at Tag Valid Time but is received at the proper time.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Time: 0.1 ms/div

–Set Rd Wr Op 85
A2G2D03 (BF110)
0.1 volts/div X10 probe

–Rd Wr Latch
A2L2J03 (BD150)
0.1 volts/div X10 probe

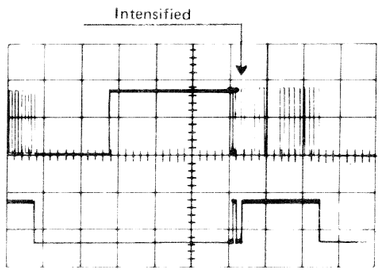


Normal End becomes active (positive) approximately 200 microseconds after the Read/Write latch is set.

After checking is done by the microprogram, an End Response is issued to reset the End Condition. The intensified area shows the time of the End Response.

+Normal End NPL
A2K2D11 (BE160)
0.2 volts/div X10 probe

+Reset End Cond
A2G2G05 (BF160)
0.1 volts/div X10 probe

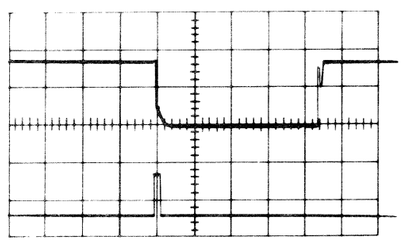


This picture is the intensified area expanded with Delayed Sweep. The pulse on the Reset End Condition is a result of the End Response Signal from the Control Unit. Normal End resets as a result of the Reset End Condition. The next positive pulse on Normal End is a result of a subsequent operation.

Time as above with delayed Sweep Set to 2 μs/div

+Normal End NPL
A2K2D11 (BE160)
0.2 volts/div X10 probe

+Reset End Cond
A2G2G05 (BF160)
0.1 volts/div X10 probe



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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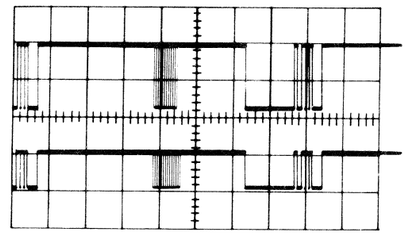
Since Op 85 is issued asynchronously with regard to the disk in this test. The Allow HAR function occasionally occurs during the execution of this test and is indicated by the pulse at the fourth vertical division. The Allow HAR function causes Device Tag Gate to drop which results in a corresponding action on the Tag Response Line. Note that Device Tag Gate follows the Read/Write latch timing and not the Tag Gate from the Storage Control.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

0.1 ms/div

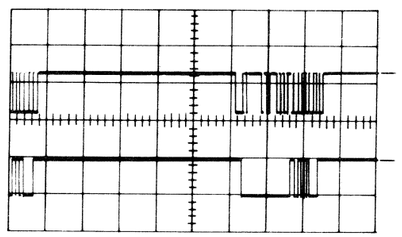
+Device Tag Gate NPL A2L2J02 (BD230)	0.2 volts/div X10 probe
+Tag Response A2G2S05 (BF160)	0.1 volt/div X10 probe



Tag Response from the drive – delayed 100 nansoeconds – causes Tag Valid to be generated to the Storage Control as long as Tag Gate from the Storage Control is active.

0.1 ms/div

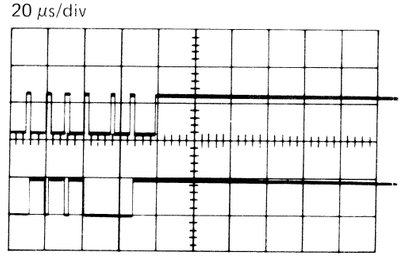
–Coerce Tag Valid A2K2B10 (BE150)	0.1 volts/div X10 probe
+Tag Response A2G2S05 (BF160)	0.1 volts/div X10 probe



Same as above except that the time is changed to show more accurate the relationship of the two pulses.

20 μs/div

–Coerce Tag Valid A2K2B10 (BE 150)	0.1 volts/div X10 probe
+Tag Response A2G2S05 (BF160)	0.1 volts/div X10 probe



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE A3 TEST 7 SCOPING PROCEDURES

Routine A3 Test 7 selects the Controller but does not select a drive. Since no drive is selected, no PLO pulses are received at the Controller. A set Read/Write OP is issued and after a delay a test is made to see if the No PLO Input Error Latch is set.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

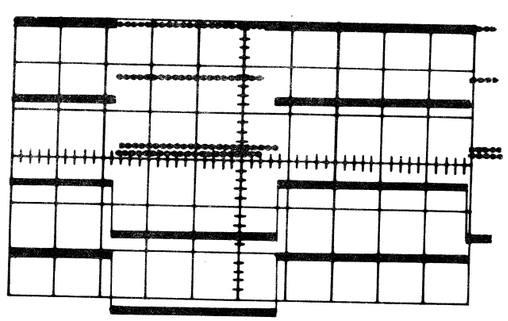
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Time: 0.1 ms/div
Vertical: 0.1 volts/div X10 probes

–PLO Input missing
A2T2D11 (BJ100)

–No PLO Input
A2S2J09 (BC110)

–Suppress Error Alert
A2L2D12 (BD170)

–Controller Check
A2K2M12 (BE130)



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ROUTINE A3 TEST 7
SCOPING PROCEDURE **MICFL 274**

ROUTINE A4 – 3340 DYNAMIC SERVO TESTS PART I

DESCRIPTION

Routines A4, A6, and A8 are dynamic servo tests. Routine A4 consists of ten tests designed to test the servo area in a progressive building-block fashion. Access positioning is verified by reading the Home Address (using Head 0) in all tests except Tests 03 and 04.

Test 01. Rezero, Read Home Address

Test 01 issues the Rezero command, testing to ensure that Busy becomes active, waiting for a maximum delay of 220 milliseconds, and then testing for Seek Complete. When Seek Complete is received, a test for Drive Check is made to ensure that no access errors have occurred. An Attention Reset is issued to reset Seek Complete and the Home Address is read to verify correct access positioning on cylinder 0. Test 01 is repeated 10 times before linking to Test 02 in normal operation.

Test 02. No Motion Seek, Read Home Address

Test 02 verifies correct operation of a No Motion Seek operation by setting the Difference Counter to 0 and issuing a Seek Start command. A test is immediately made for Seek Complete. If Seek Complete is not active, the test is delayed for 3 milliseconds and tested again. If Seek Complete is not active, a Late Seek Complete error is posted. If the first Seek Complete is successful, a test for Drive check is made to ensure no access errors occurred. The HAR Forward Direction bit is alternately set and reset prior to issuing the Seek Start command to ensure that no access motion occurs. If all of the checks are successful, the Home Address is read to verify correct access positioning on cylinder 0. Test 02 is repeated 10 times before linking to Test 03 in normal operation.

Test 03. Overshoot Check

Test 03 verifies correct operation of the Overshoot check circuitry. Overshoot check is forced on by three different methods and the resulting Drive check is verified in each case. The three methods are performed in sequence as follows:

Method 1:

The first method begins by setting the Difference Counter to '80' (128 decimal), and issuing a Seek Start command (128 cylinder seek). After a delay of 2.5 milliseconds to allow access motion to start, the Difference Counter is reset. The test enters a subroutine that samples the off-to-on transitions of the track-crossing pulse (Bit 3 under access status). A check is made to ensure that Overshoot check did not become active on the first on-to-off transition of the track crossing pulse. A second check is made to ensure that Overshoot check became active on the third off-to-on transition of the track crossing pulse. A test for Drive check is then made to ensure that it is active. Attention and check resets are performed and the reset condition of the error latches is verified. A Rezero command is issued to restore the access to cylinder 0 before starting Method 2.

Method 2:

The second method starts with the access at cylinder 0 and uses the Diagnostic Servo Reset command (Tag '8A' Bus '80') to force an Overshoot check. The Diagnostic Servo Reset command is held active for 60 milliseconds, after which a check is made to ensure that Drive check and Overshoot check are active. Attention and check resets are performed and the reset condition of the error latches is verified. A Rezero command is executed to restore the access before starting Method 3.

Method 3:

The third method starts with the access at cylinder 0 and issues repetitive 1-cylinder seeks in the forward direction until the Carriage Home switch is made. The number of seeks required to make Carriage Home is a variable for different Drive and Data module combinations due to mechanical tolerances. If a Drive check occurs before the Carriage Home switch is made, an access error occurred and must also be checked. When the Carriage Home switch is made, Drive check and Overshoot check are verified followed by attention and check resets. Reset condition of the error latches is then performed. A Rezero command followed by attention and check resets is performed before linking to Test 04 in normal operation.

Test 04. Timer Verification

The objective of Test 04 is to measure the elapsed time from the leading edge of the first track crossing pulse to the setting of the control latch in the servo. The time measured must be greater than 2 milliseconds.

This test issues a 1-cylinder forward Seek and enters a timer subroutine to wait for the leading edge of the first track crossing pulse (bit 3 under access status). When this is found, the elapsed time from this point to the setting of the control latch (bit 6 under access status) is accumulated in a counter. When the control latch becomes active, the test compares the accumulated time to a specification of 2 milliseconds. The measured time must be greater than the specification or an error stop occurs. This test is repeated 10 times before linking to Test 05 in normal operation.

Test 05. Incremental Seek (Increment = 1)

Test 05 seeks from cylinder 0 to cylinder 349 and back to cylinder 0 in 1-cylinder increments. The access position is verified after each Seek by reading the Home Address with Head 0. A comparison is made between the actual status of Odd Track (bit 7 under data module sequence control) and the expected type of track (odd or even). An error stop occurs if a noncompare results. This test links to Test 06 when the access has returned to cylinder 0 in normal operation.

Test 06. Incremental Seek (Increment = 2)

Test 06 seeks from cylinder 0 to cylinder 348 and back to cylinder 0 in 2-cylinder increments. Conditions tested are identical to those in Test 05. This test links to Test 07 when the access has returned to cylinder 0 in normal operation.

Test 07. Incremental Seek (Increment = 50)

Test 07 seeks from cylinder 0 to cylinder 300 and back to cylinder 0 in 50-cylinder increments. Conditions tested are identical to those in Test 05. This test links to Test 08 when the access has returned to cylinder 0 in normal operation.

Test 08. Incremental Seek (Increment = 116)

Test 08 seeks from cylinder 0 to cylinder 348 and back to cylinder 0 in 116-cylinder increments. Conditions tested are identical to those in Test 05. This test links to Test 09 when the access has returned to cylinder 0 in normal operation.

Test 09. Incremental Seek (Increment = 174)

Test 09 seeks from cylinder 0 to cylinder 348 and back to cylinder 0 in 174-cylinder increments. Conditions tested are identical to those in Test 05. This test links to Test 10 when the access has returned to cylinder 0 in normal operation.

Test 10. Rezero, Read Home Address, Seek 12 Cylinders, and Read Home Address

Test 10 rezeros, and reads the Home Address to verify access positioning on cylinder 0; then seeks 12 cylinders and again reads the Home Address to verify access positioning on cylinder 12. The test is repeated 10 times before linking to Routine AE in normal operation.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry

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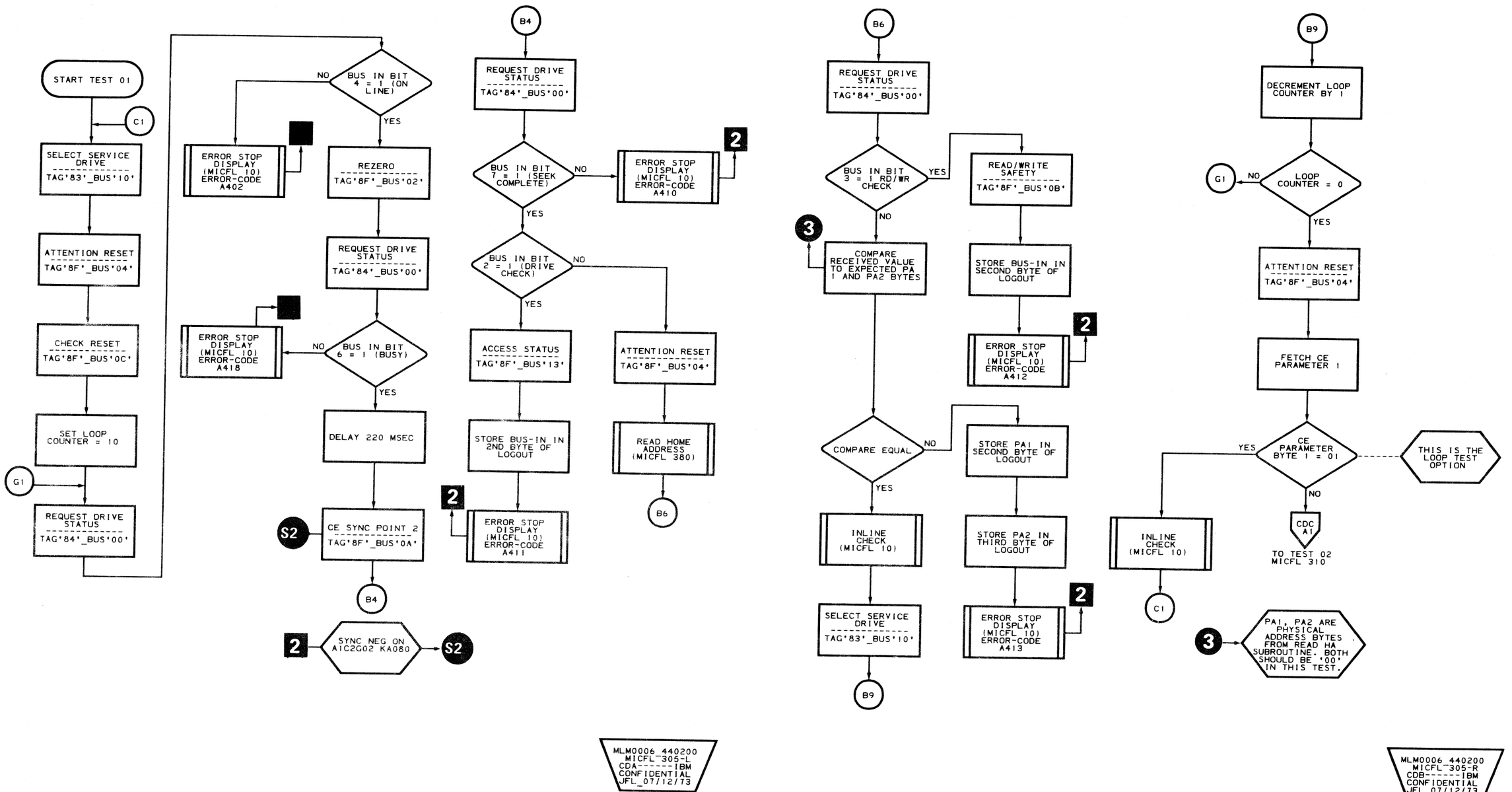

MLM0006_440200
MICFL_305-L
CDA------IBM
CONFIDENTIAL
JFL_07/12/73

MLM0006_440200
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CDB------IBM
CONFIDENTIAL
JFL_07/12/73

CC0305	2747058	440200	440202	440203				
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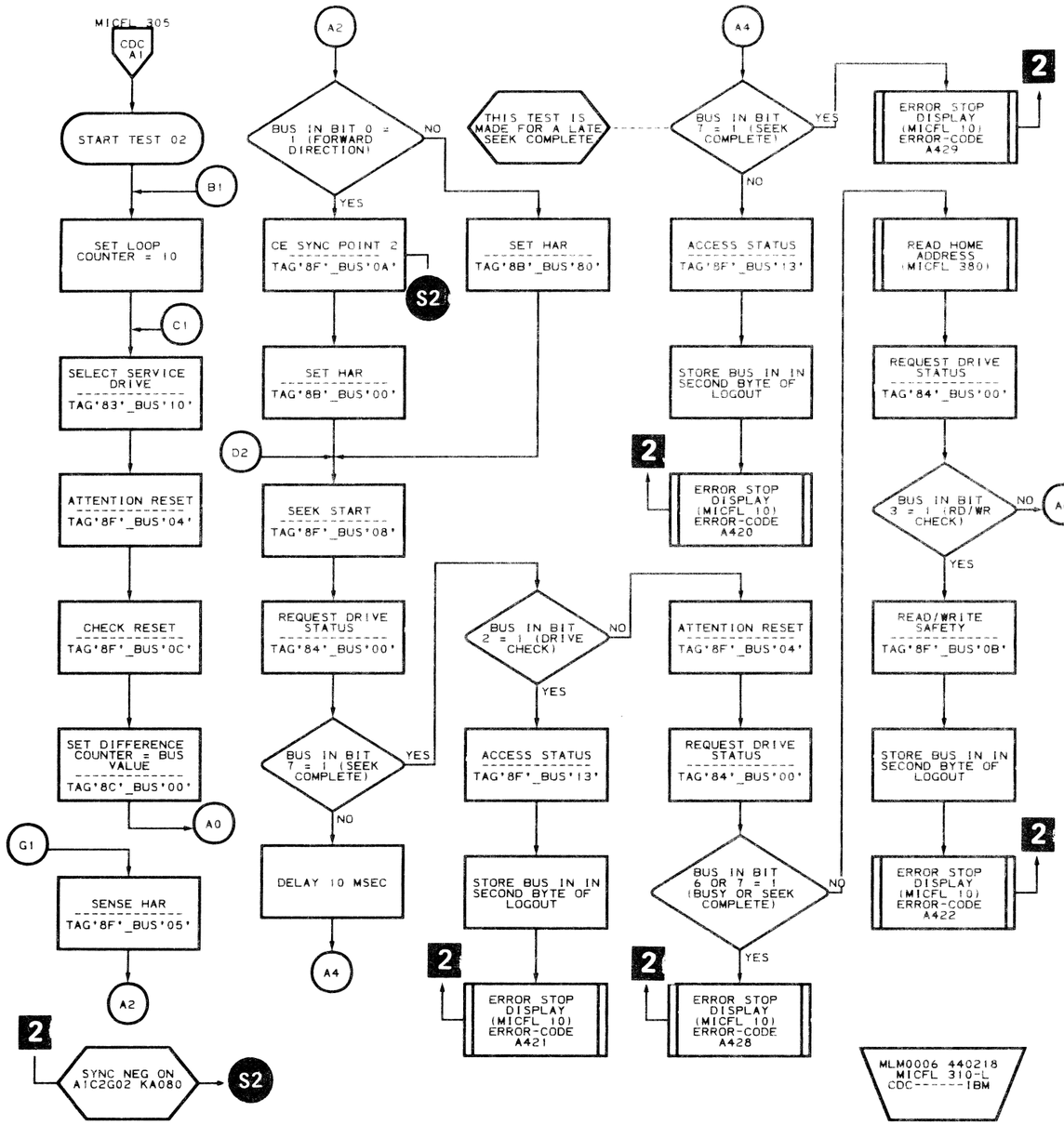
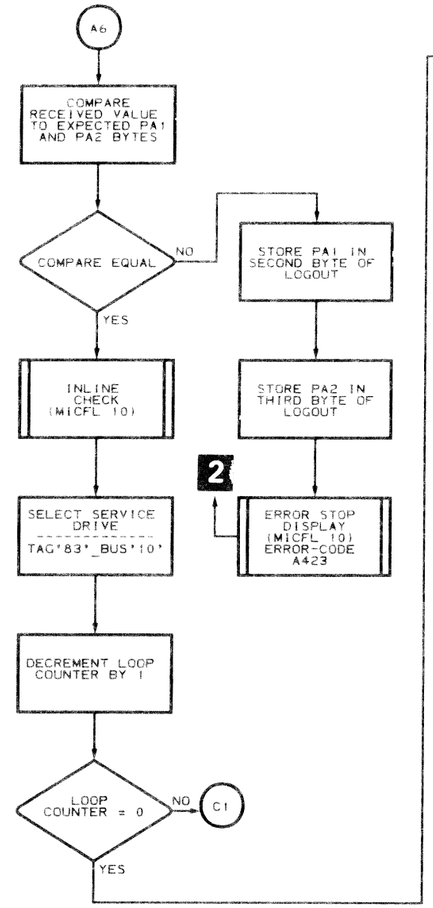
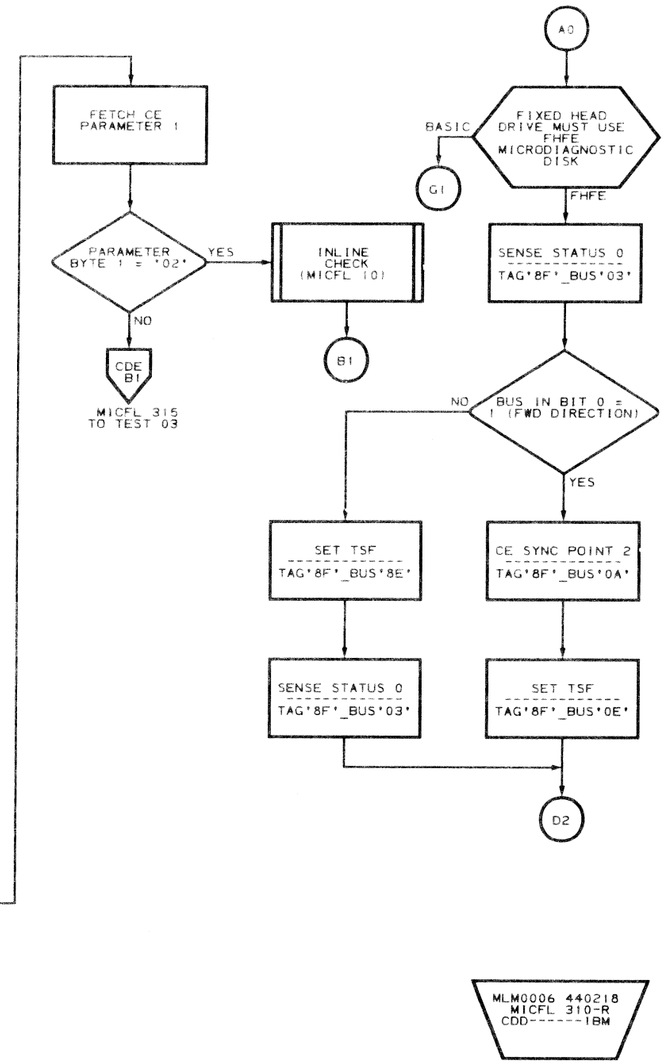
NO MOTION SEEK (Routine A4)







CC0310	2747059	440200	440202	440203	440204	440214	440218	440227
Seq. 1 of 2	Part No. (N)	25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	17 Jun 74	5 Aug 74	14 Sept 76

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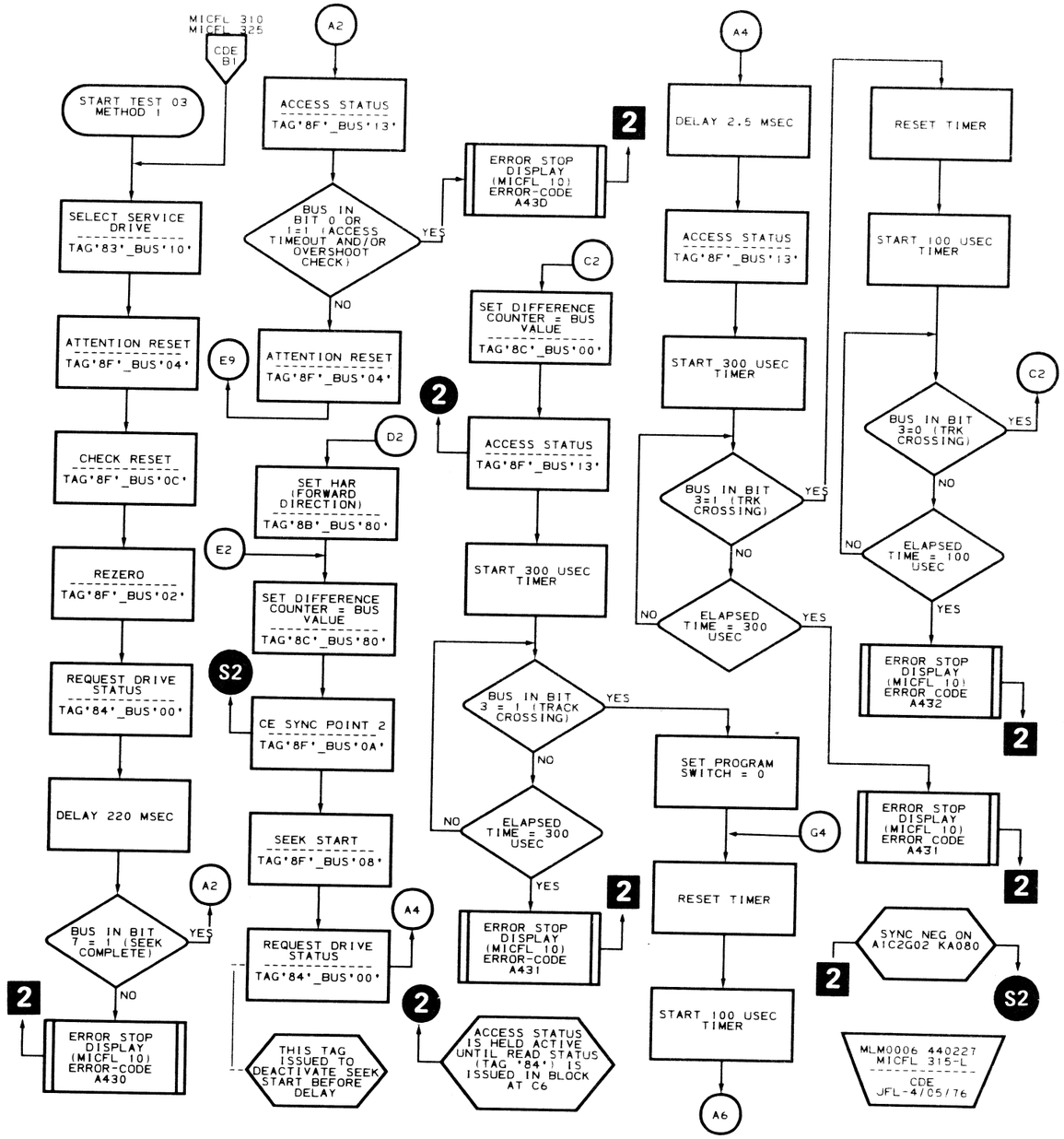
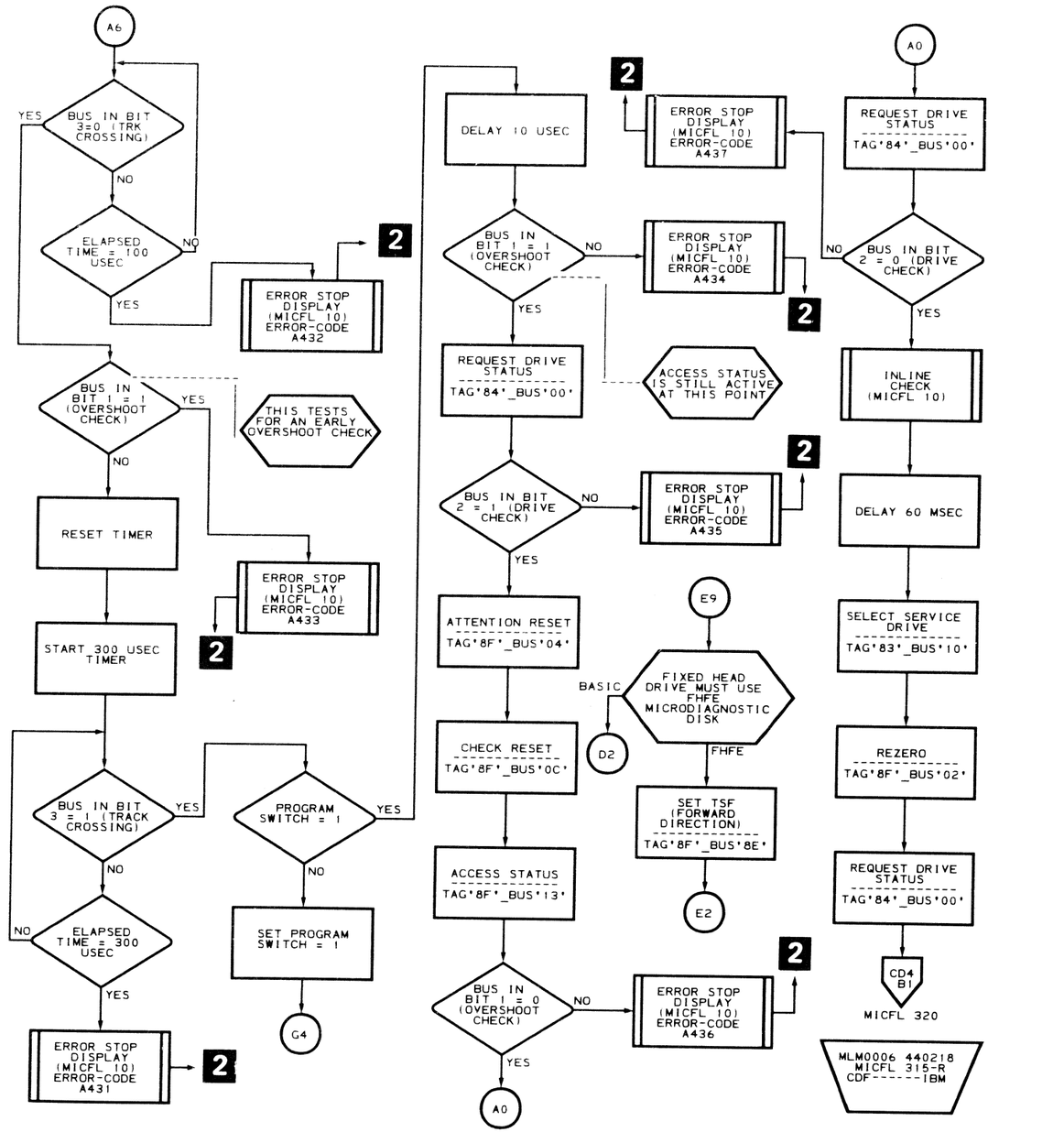
OVERSHOOT CHECK (Routine A4)





CC0310	2747059
Seq. 2 of 2	Part No.(N)

440200	440202	440203	440204	440214	440218	440227
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	17 Jun 74	5 Aug 74	14 Sept 76

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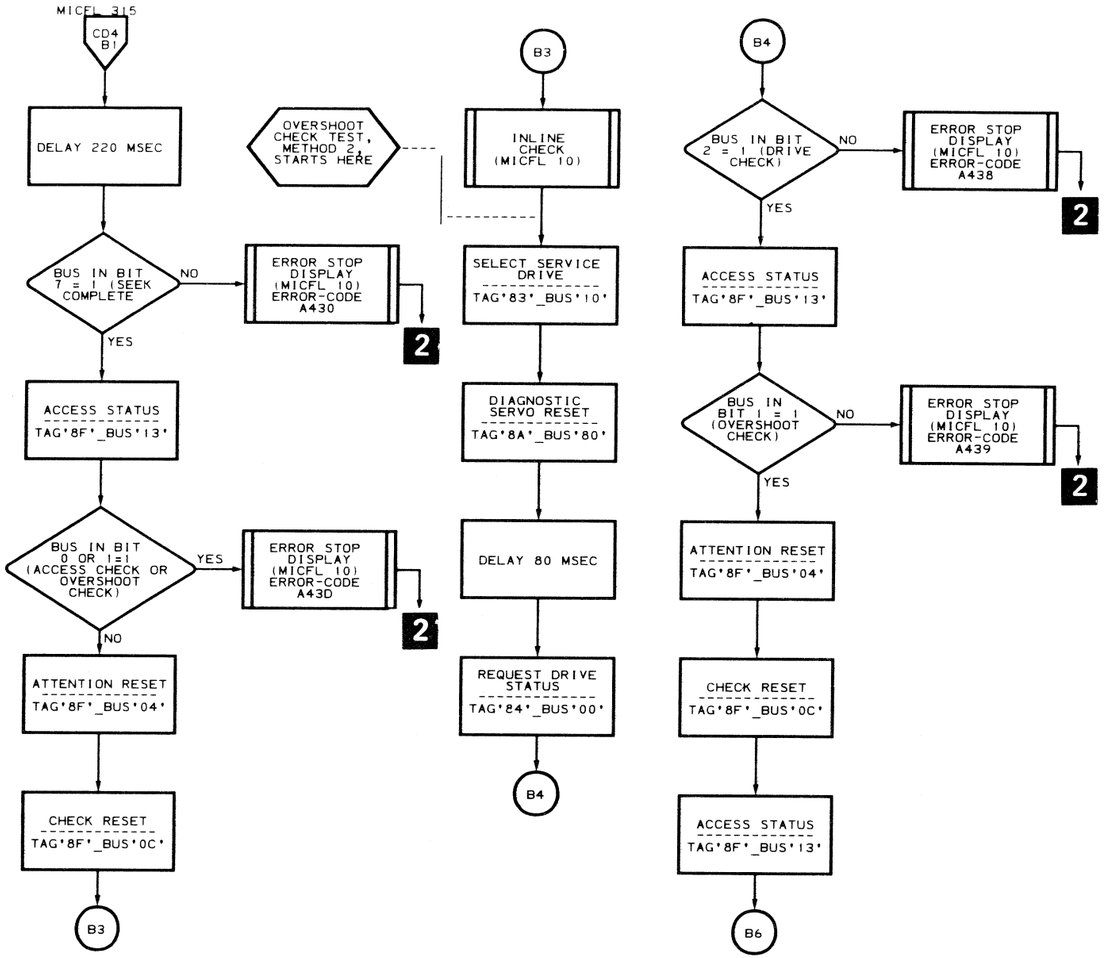
OVERSHOOT CHECK (Routine A4)



MLM0006 440218
MICFL 320-L
CD4------IBM

MLM0006 440200
MICFL 320-R
CD5------IBM

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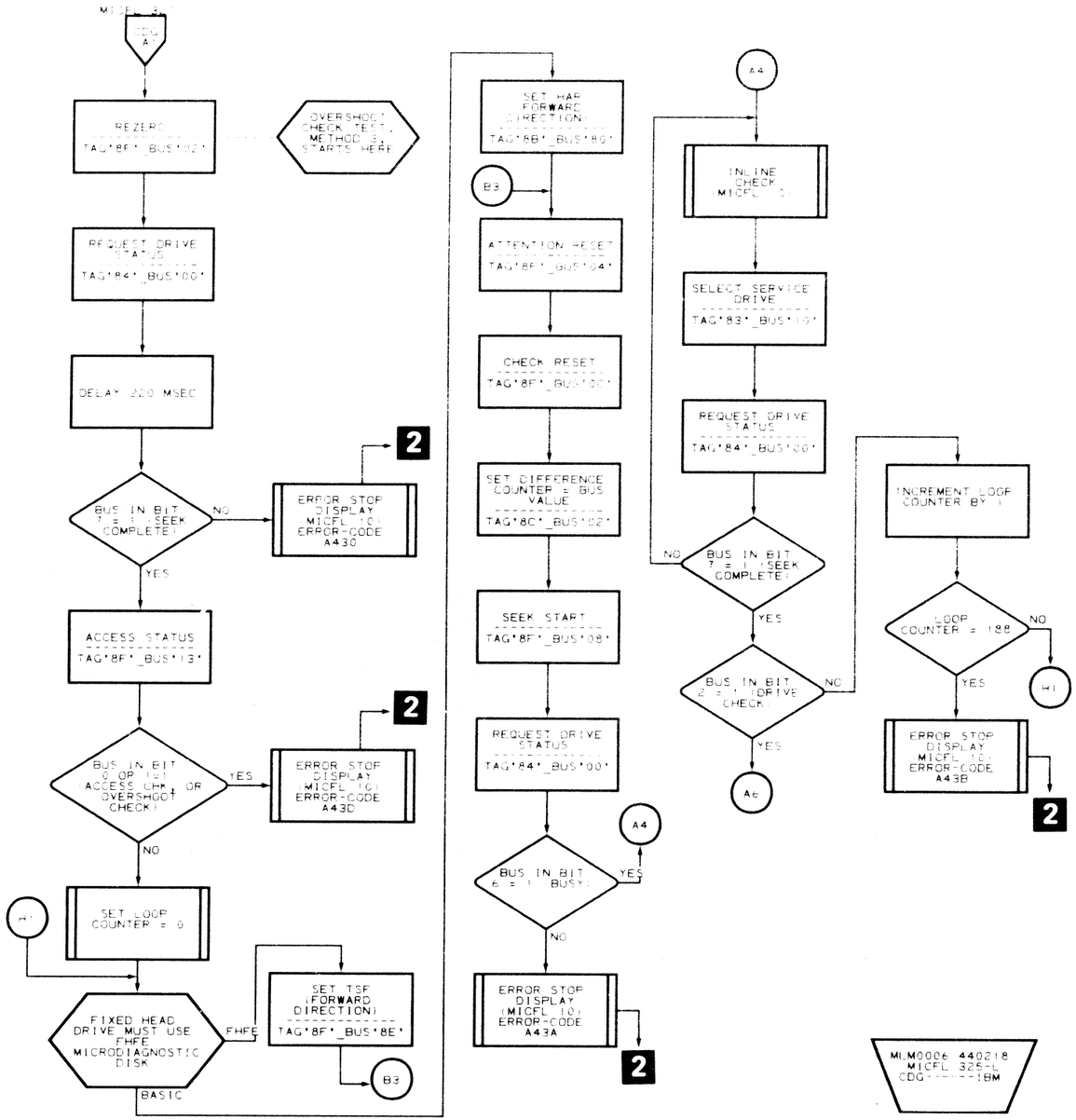

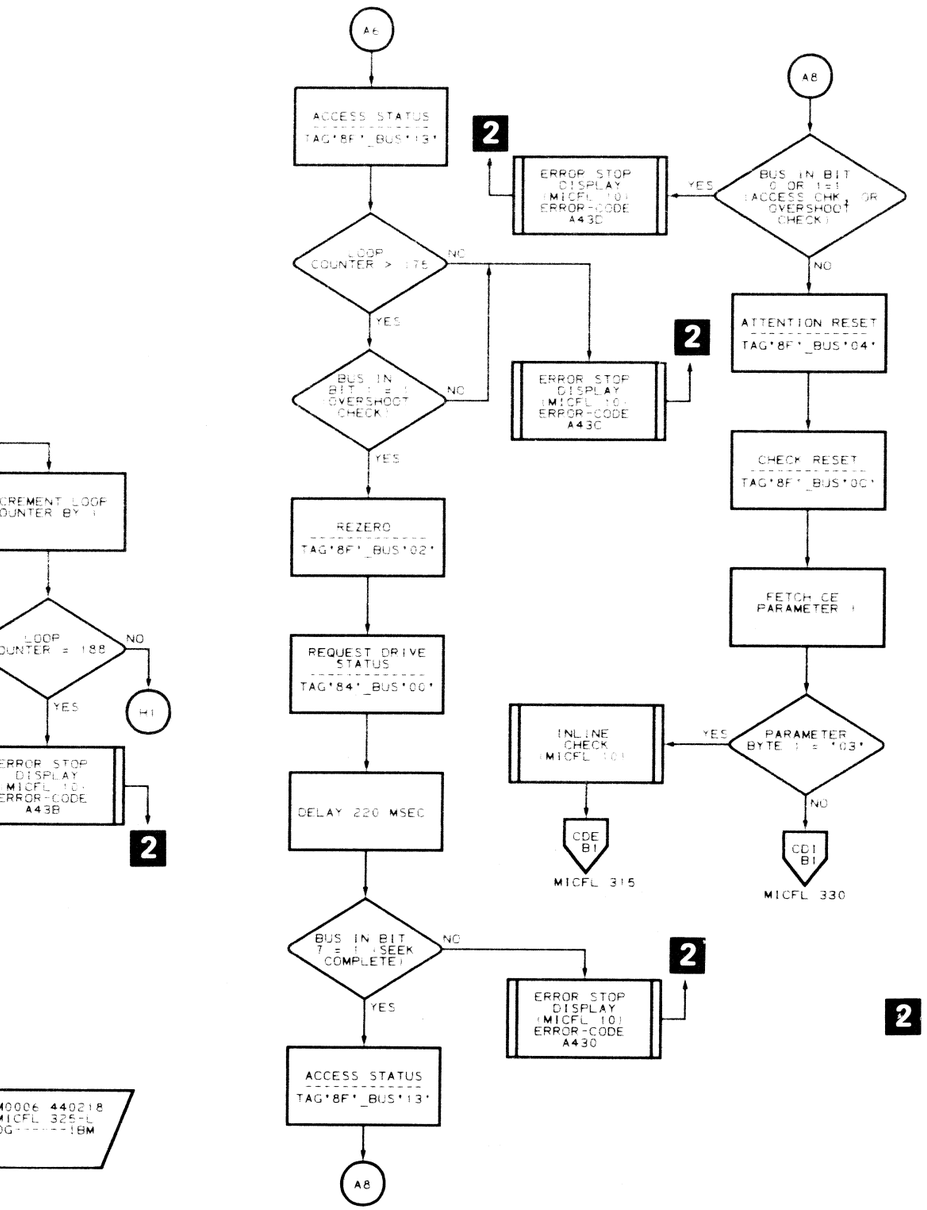

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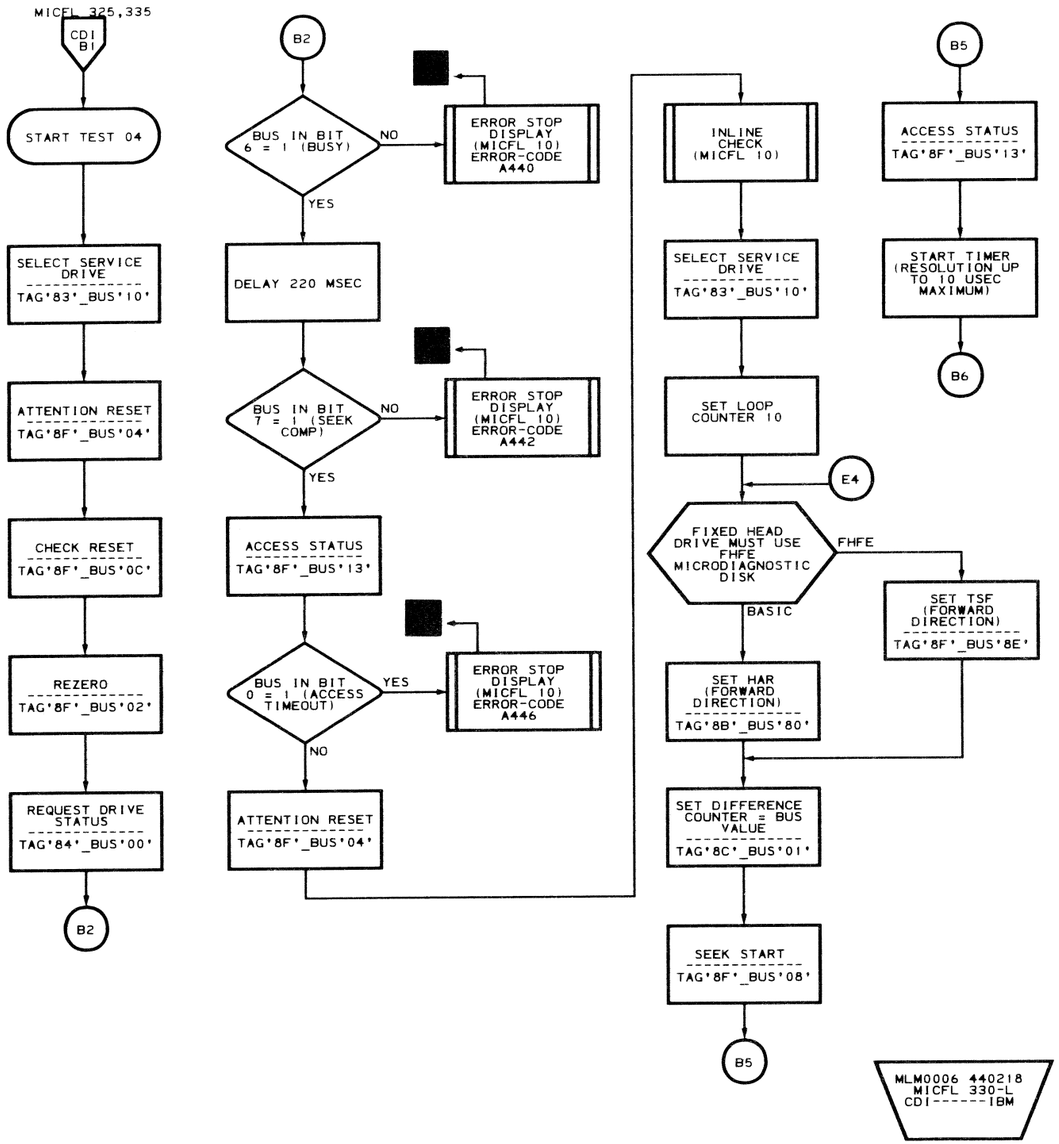
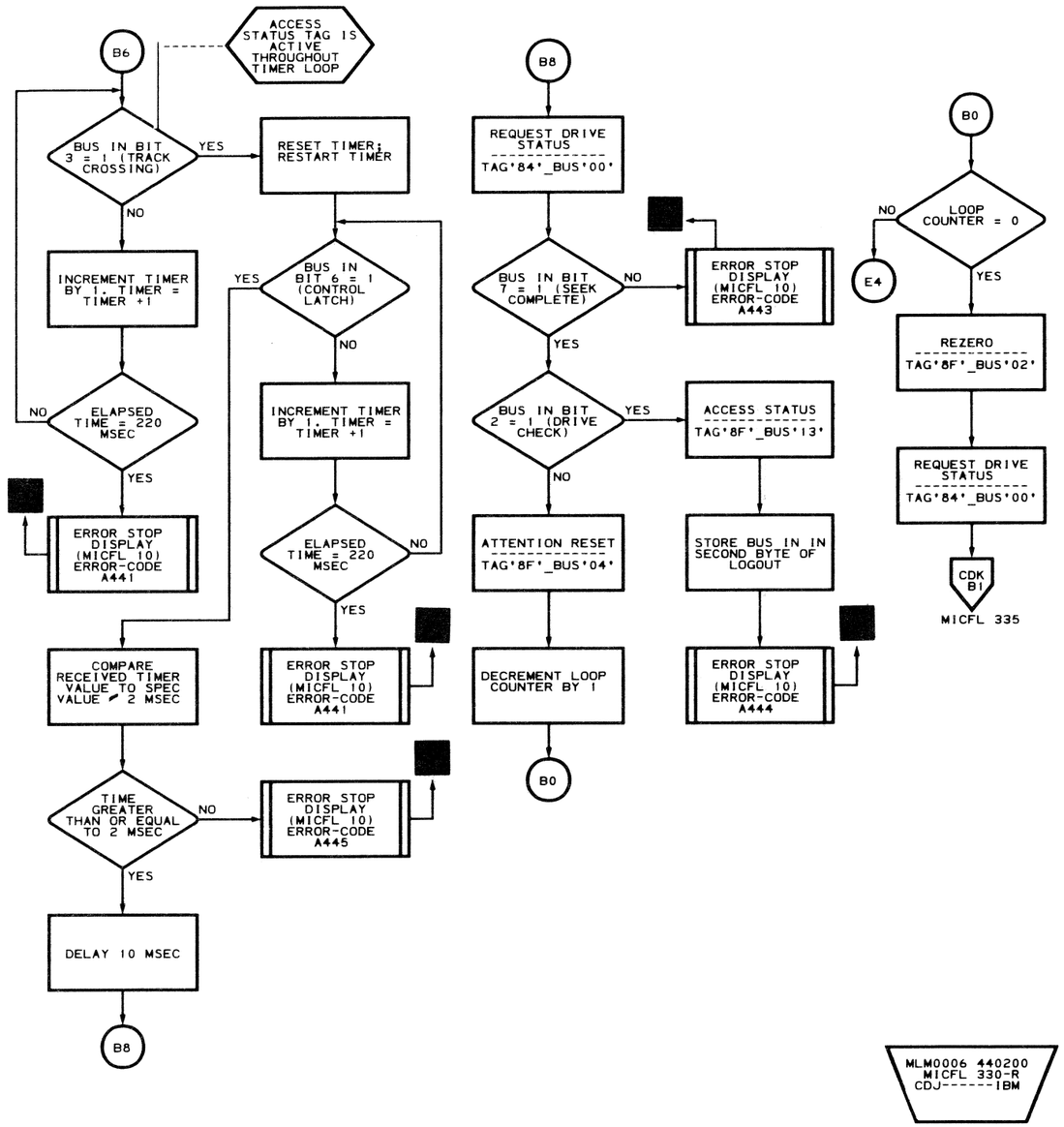
TIMER VERIFICATION (Routine A4)





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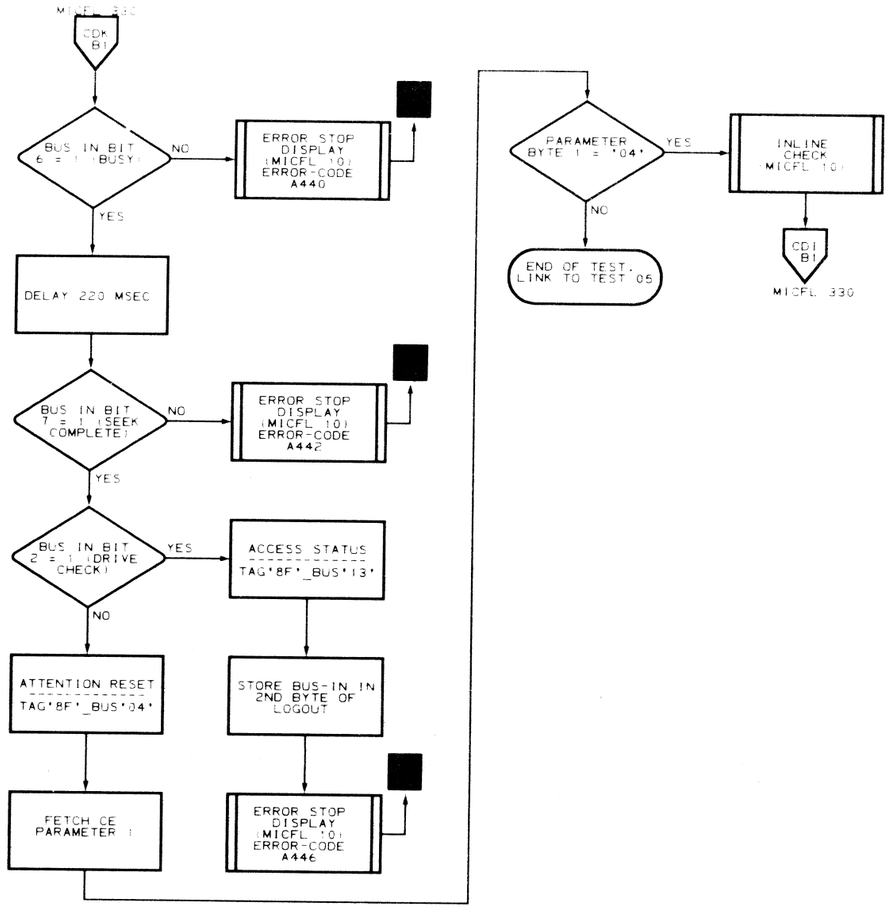

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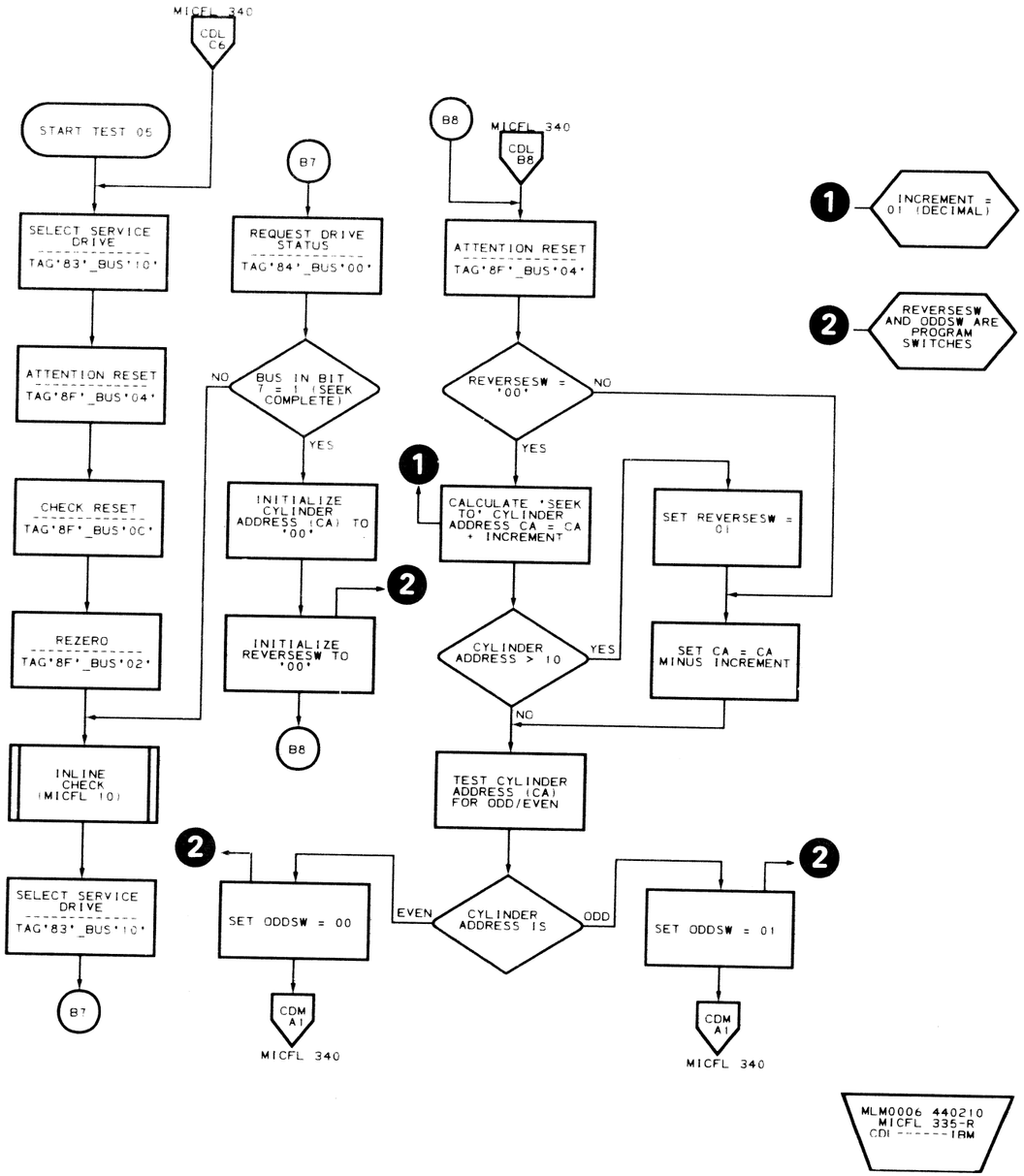
MICFL 335-L
CDK------IBM



MLM0006 440210
MICFL 335-R
CDI------IBM

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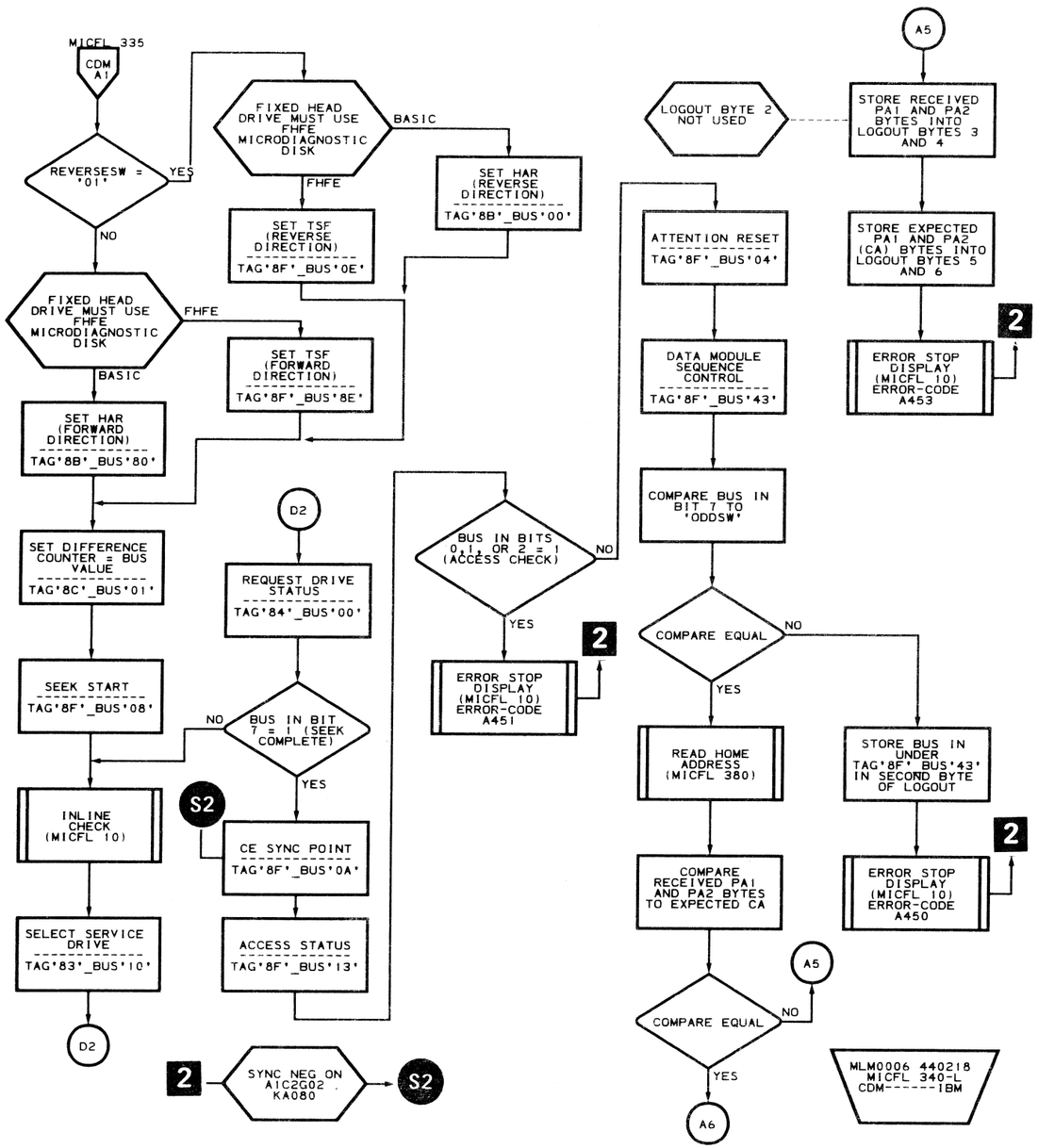
INCREMENTAL SEEK (Routine A4)



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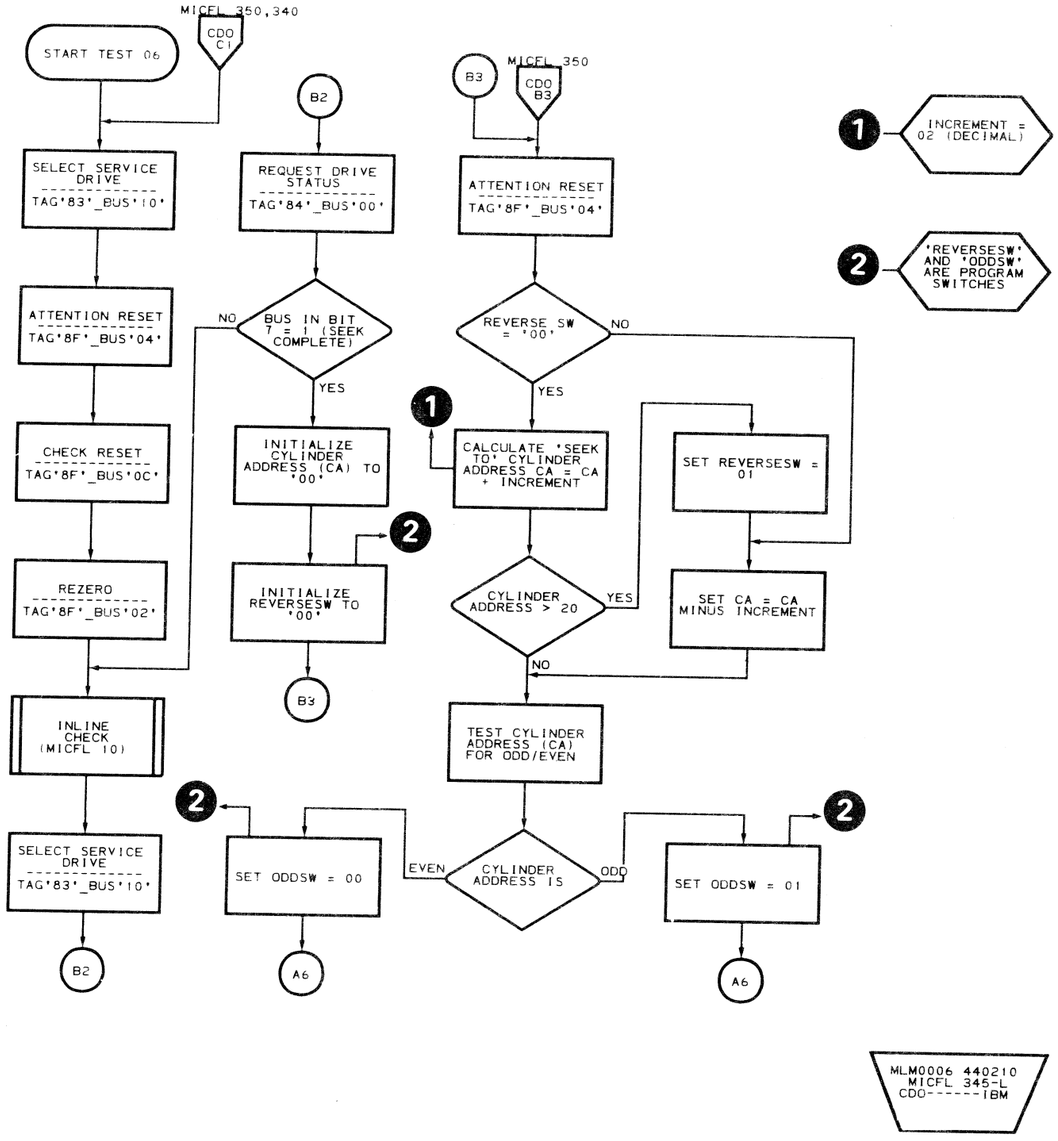
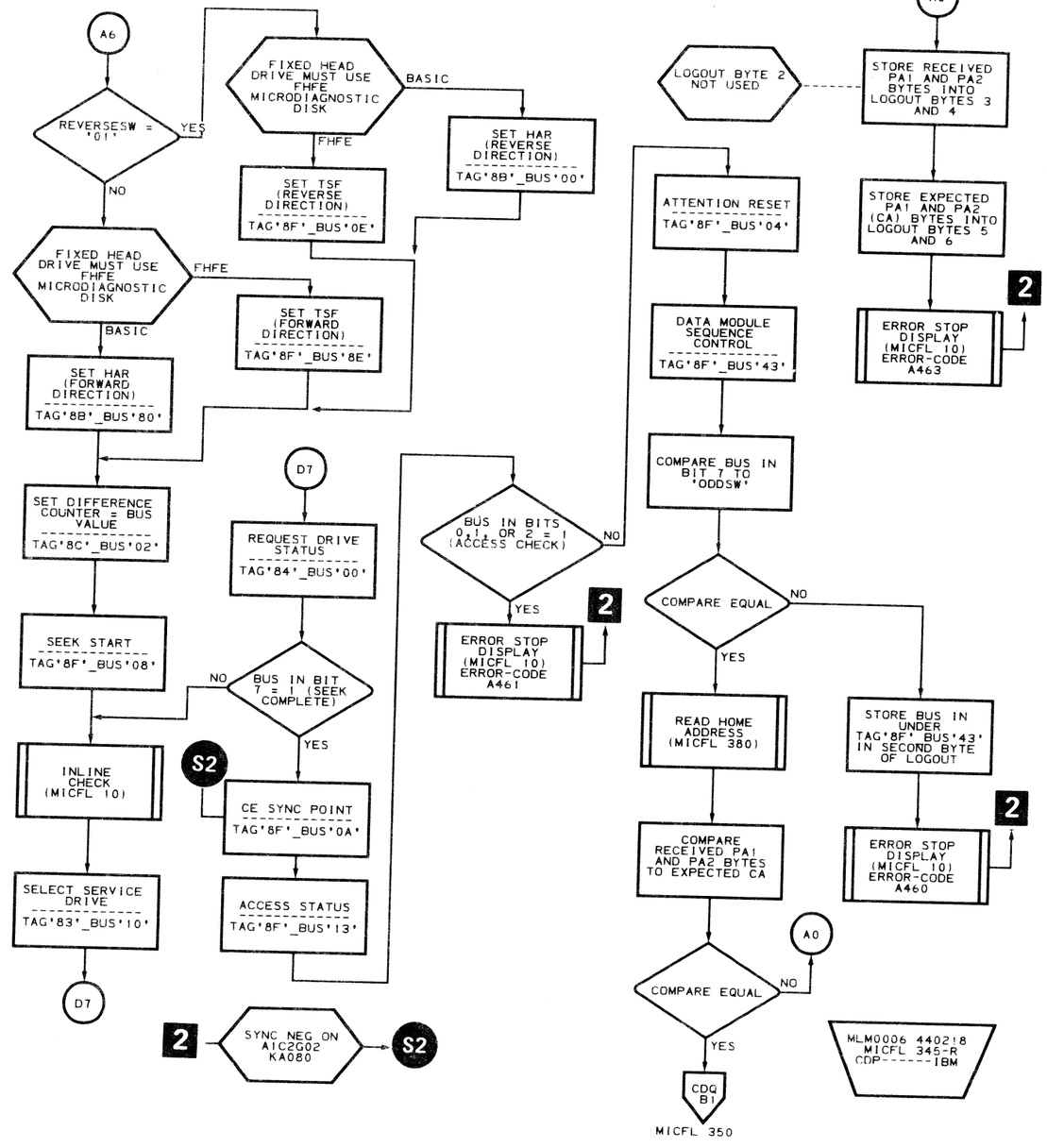
INCREMENTAL SEEK (Routine A4)





CC0340 Seq.2 of 2	2747062 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440214 17 Jun 74	440218 5 Aug 74	

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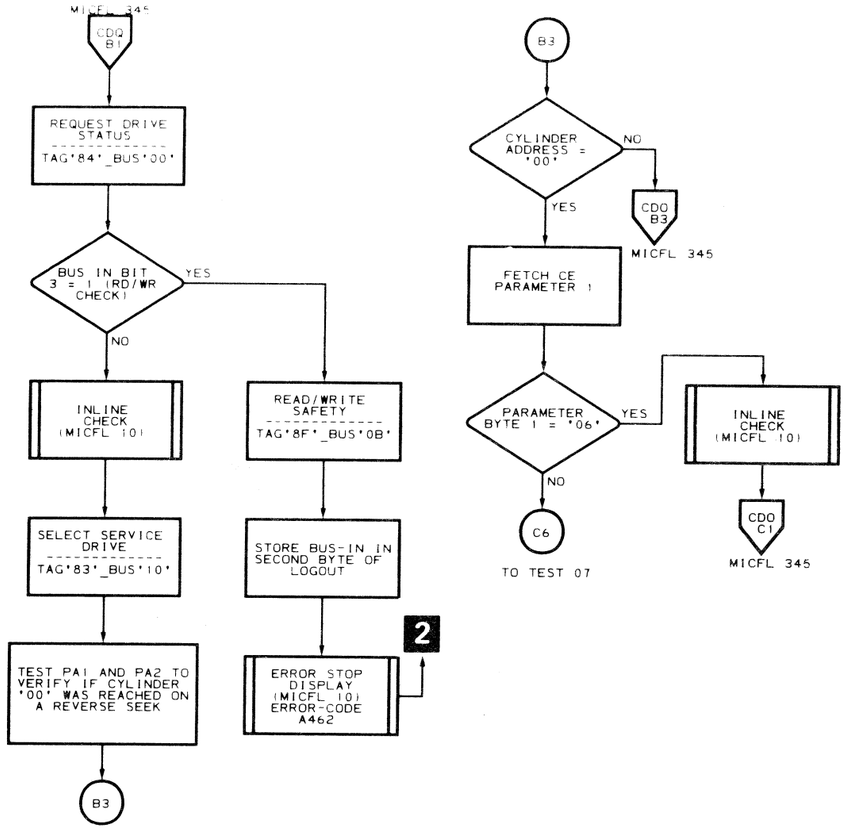
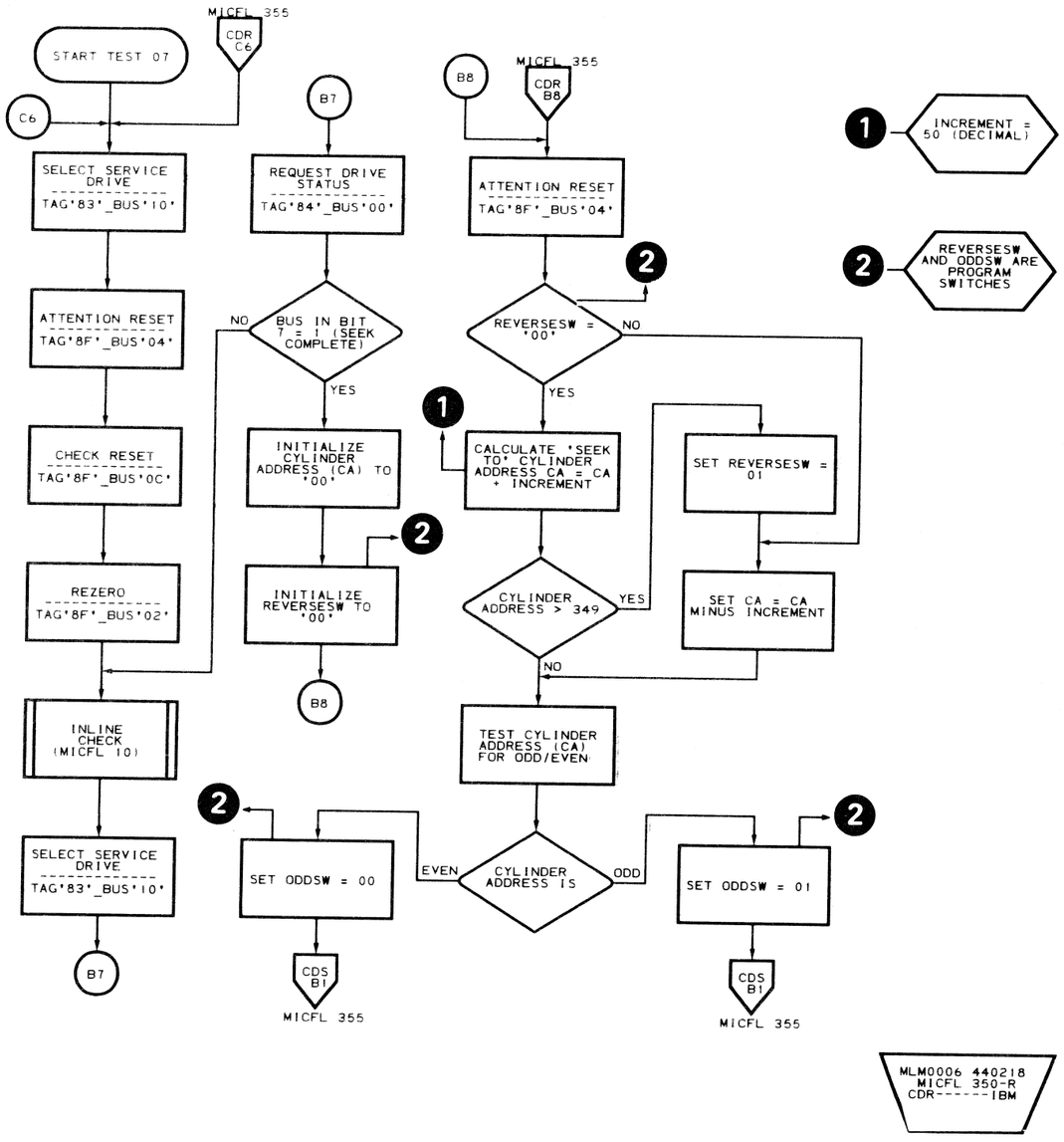
INCREMENTAL SEEK (Routine A4)





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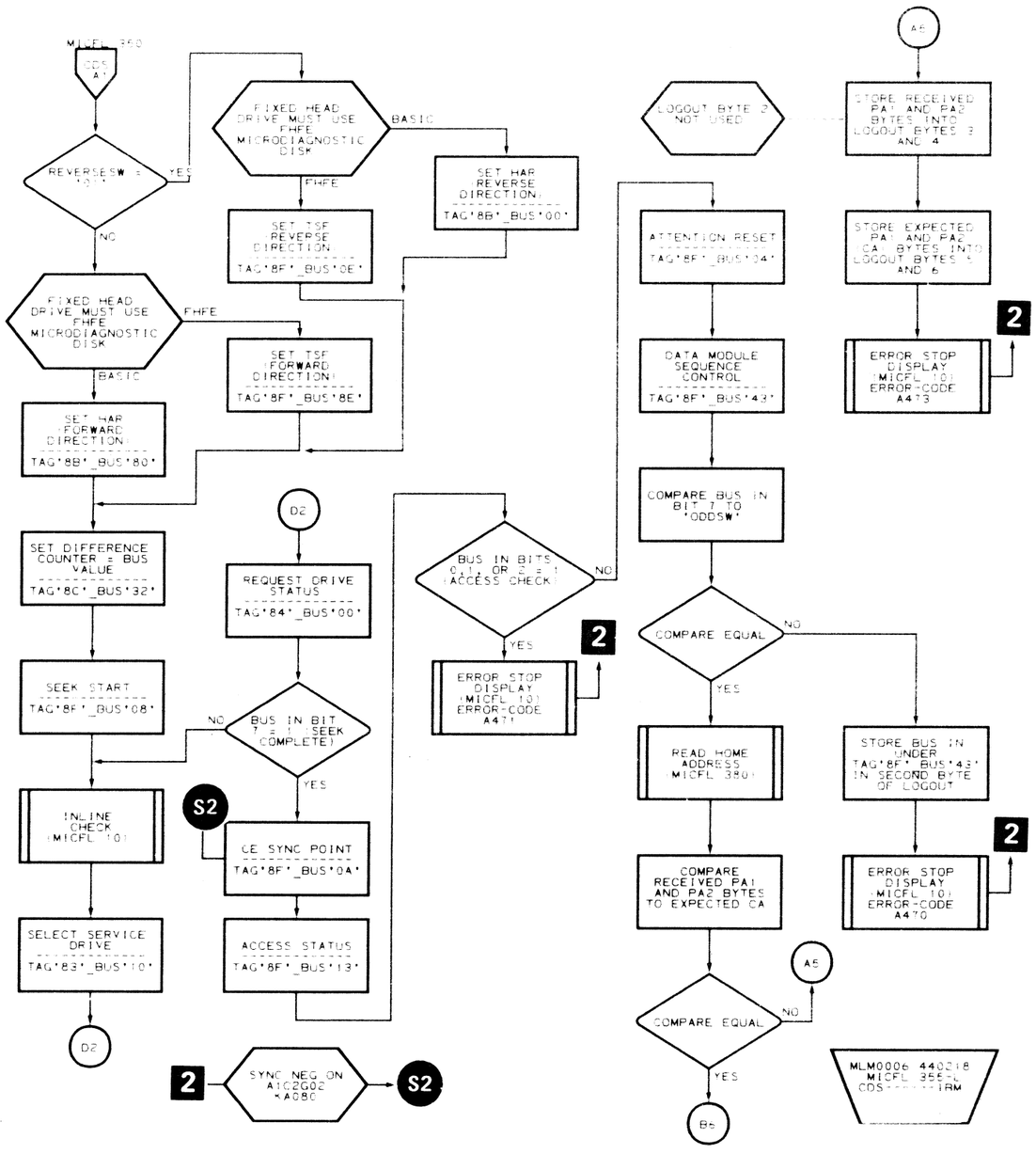
CDQ------IBM

MLM0006 440218
MICFL 350-R
CDR------IBM



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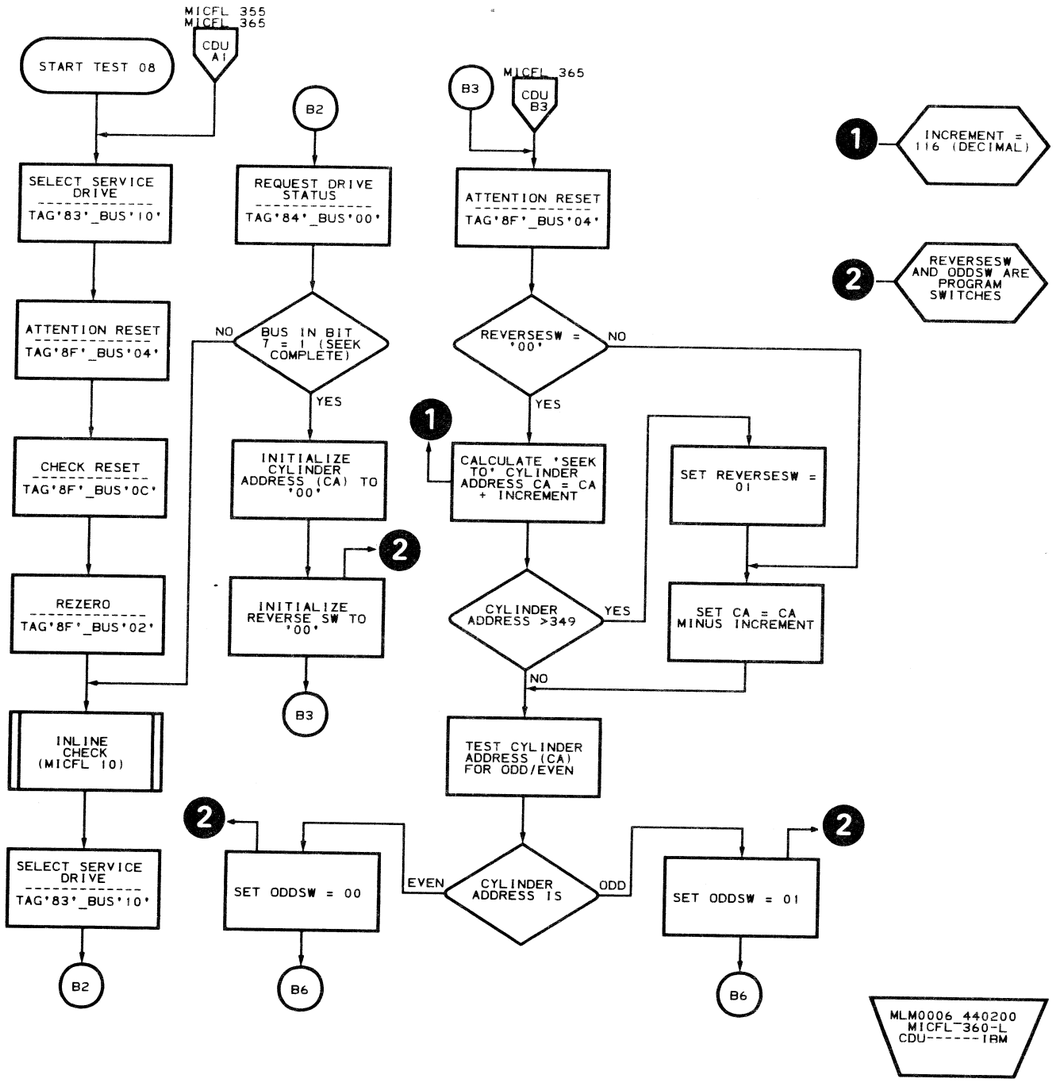
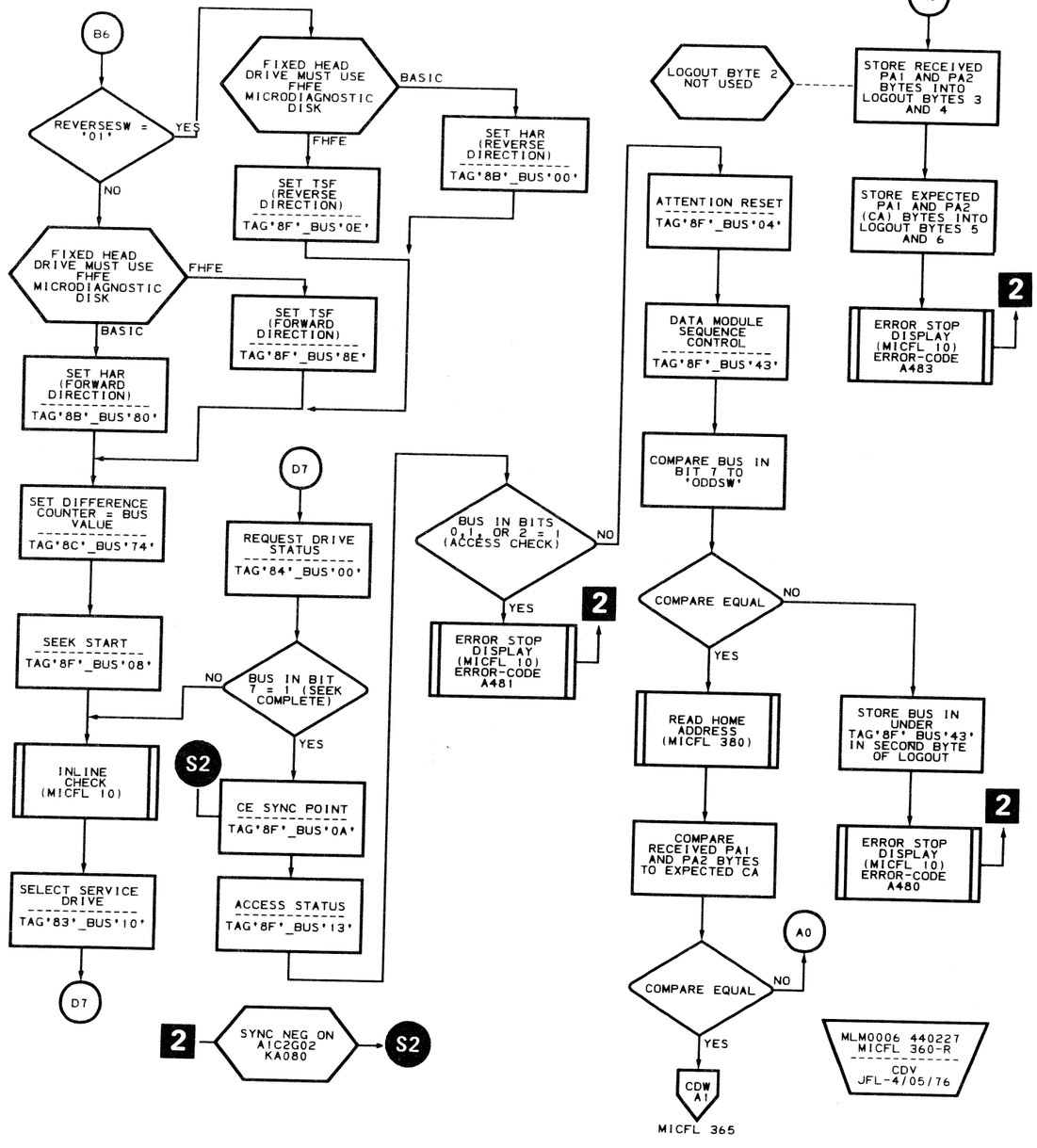
INCREMENTAL SEEK (Routine A4)





CC0360	2747064
Seq. 1 of 2	Part No.(N)

440200	440202	440203	440214	440218	440227	
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74	14 Sep 76	

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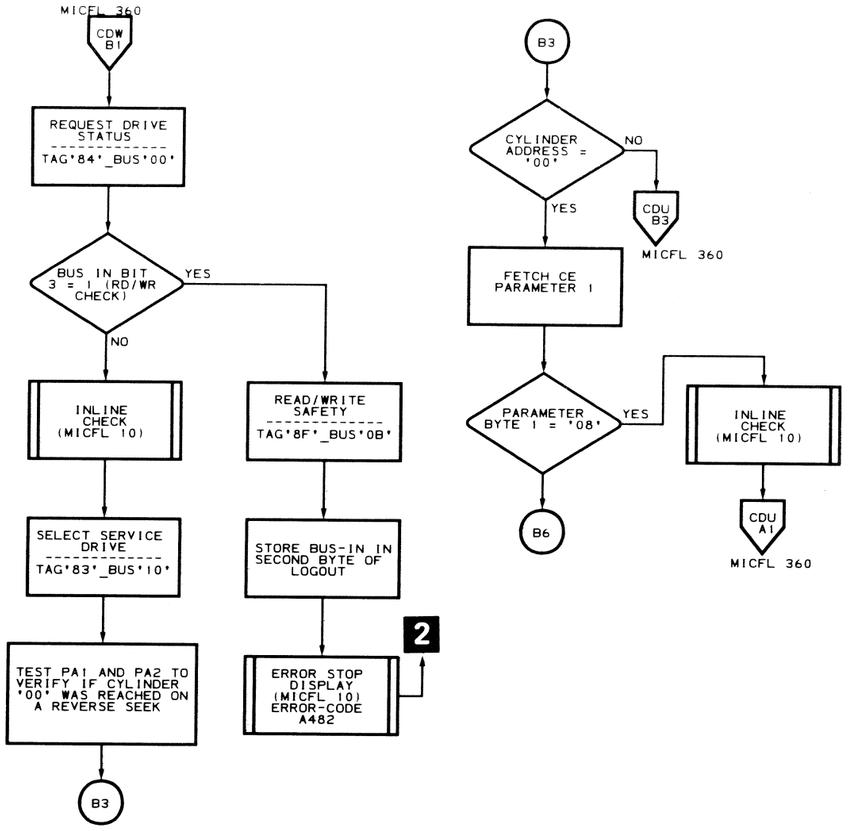
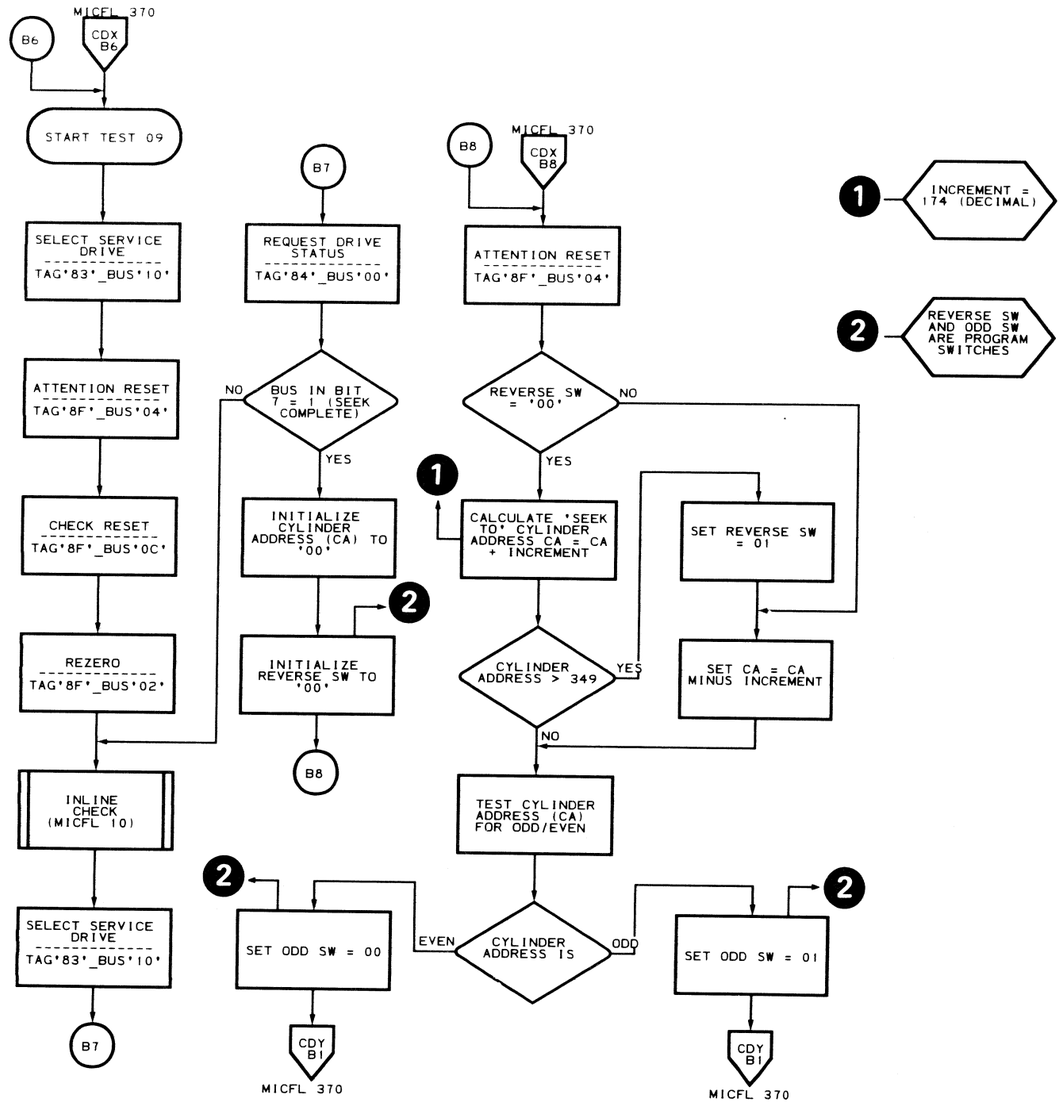
INCREMENTAL SEEK (Routine A4)





MLM0006_440200
MICFL-365-L
CDW------IBM

MLM0006_440218
MICFL-365-R

CC0360	2747064
Seq. 2 of 2	Part No.(N)

440200	440202	440203	440214	440218	440227	
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74	14 Sept 76	

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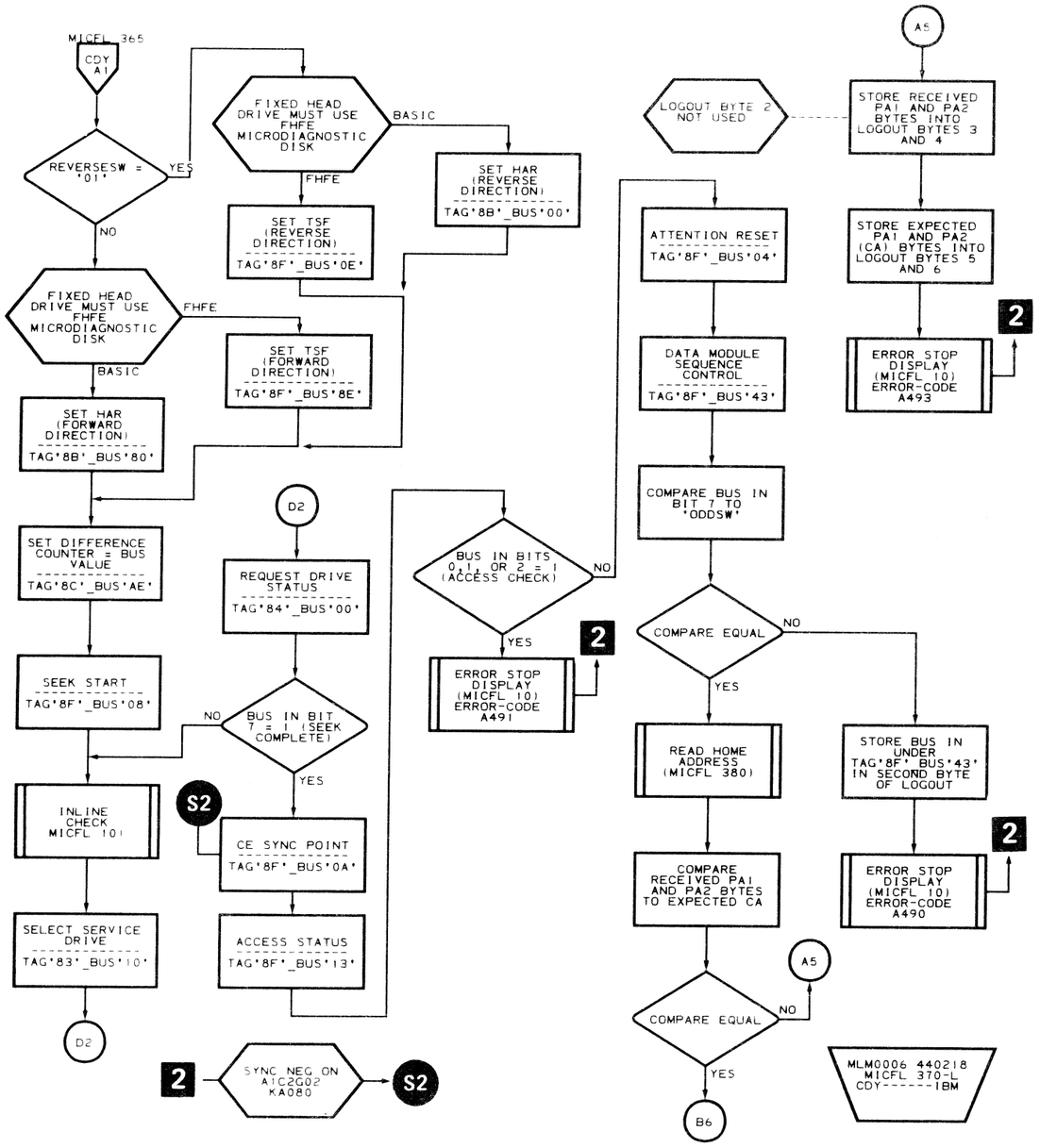
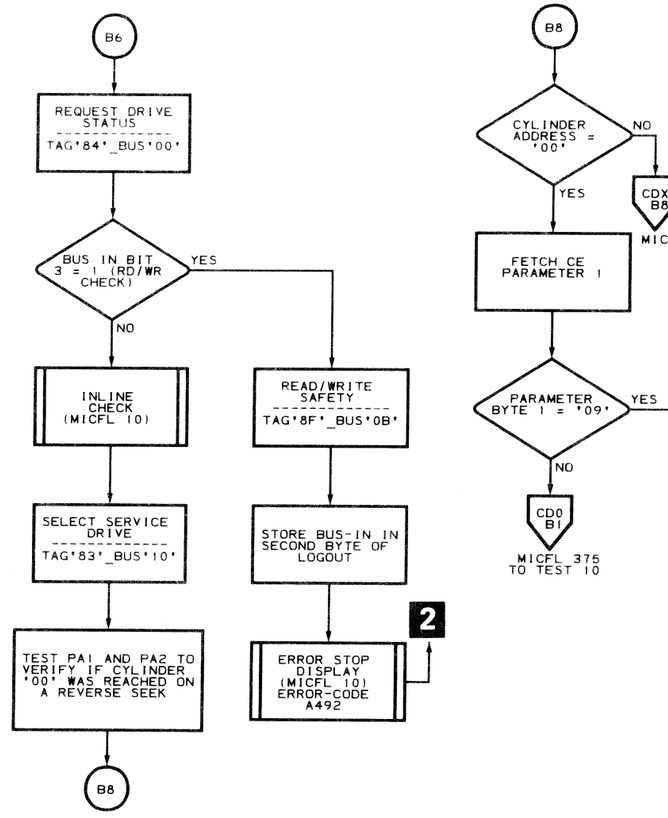
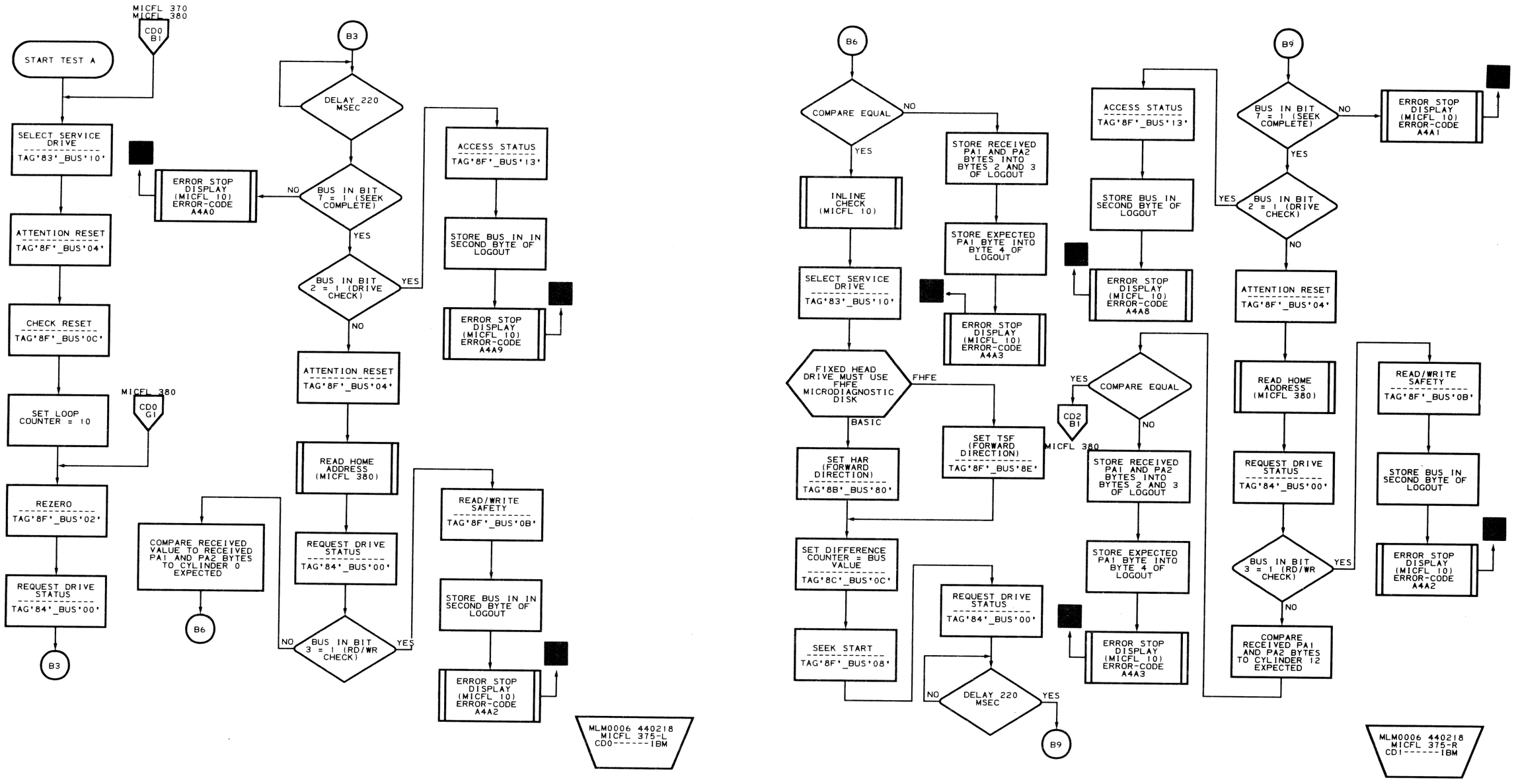
INCREMENTAL SEEK (Routine A4)







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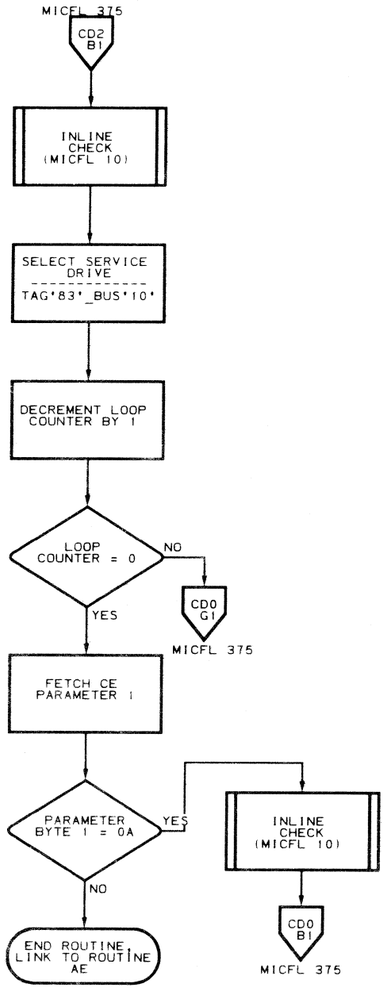
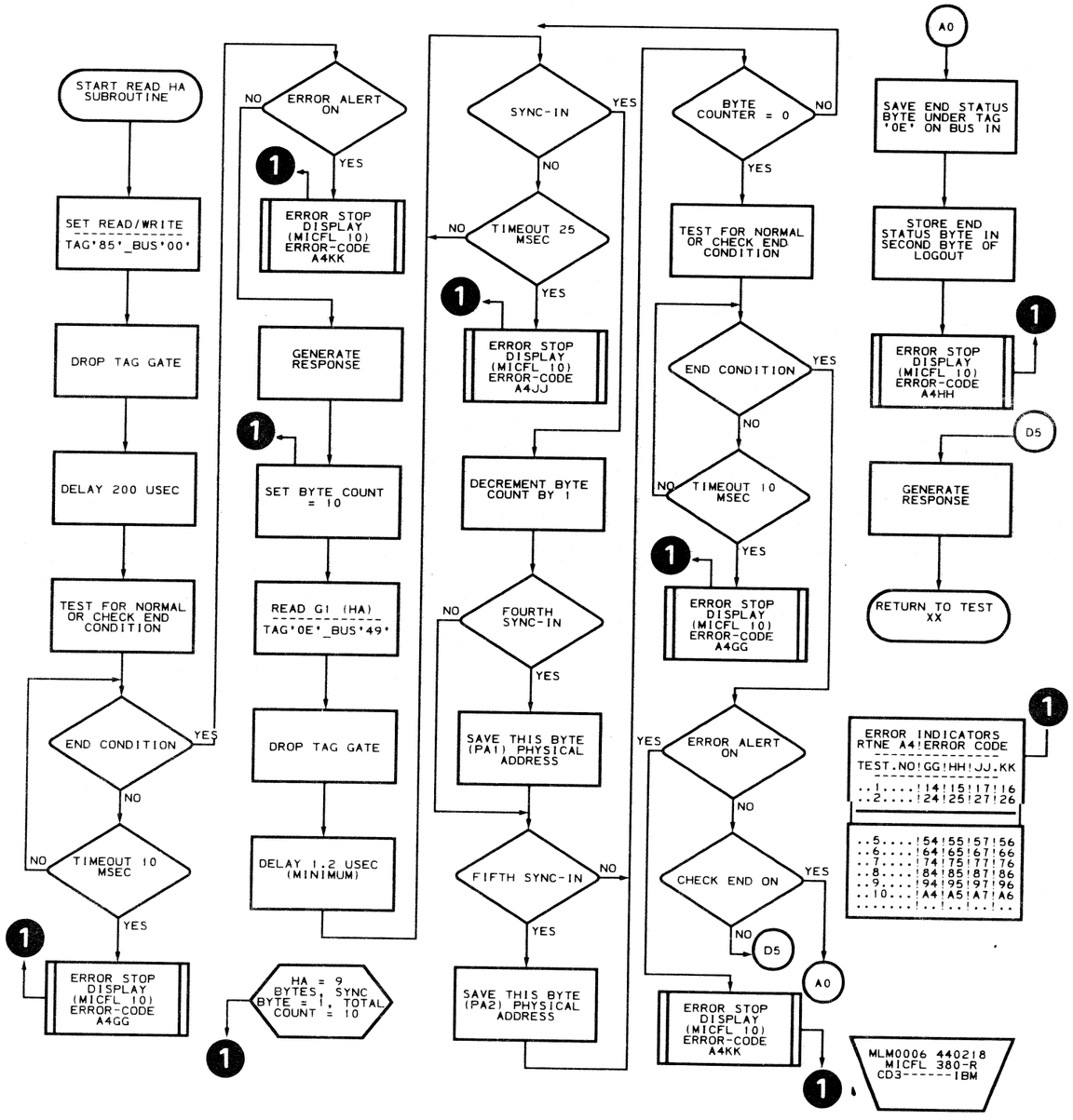
REZERO, SEEK 12 CYL./READ HA SUBROUTINE (Routine A4)





MLM0006 440200
MICFL 380-L
CD2------IBM

MLM0006 440218
MICFL 380-R
CD3------IBM

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ROUTINE A5 – 3340 DRIVE INDEX AND SECTOR TESTS

DESCRIPTION

Test 01. Target Register

Test 01 first checks the 3340 Drive for the RPS feature bit. If found, a Target register test is run. The test sets the Target Register to all 0s, all 1s, a sliding 1s pattern, and a sliding 2s pattern. Every time the Target Register is sensed, Bus In is examined for a parity check.

Test 02. Index

Test 02 performs the following functions:

1. Measures the width of the index pulse as seen by the drive and verifies that the width is between 8 and 10 microseconds.
2. Measures the time between two Index Marks as seen by the drive and verifies that it is between 9.8 and 10.4 milliseconds.
3. Verifies that the active track follows HAR bit 7.
4. Verifies that the Index Mark, as seen by the controller, follows Index Mark in the drive.

Test 03. Force Multihead Check

Test 03 forces a Multihead check by selecting an odd physical head and issuing a special diagnostic command (Tag '8A' Bus '02') which forces even head selection. The test verifies that Read/Write Check comes on because more than one head is selected. If a fixed head data module is mounted, the test is repeated using an odd physical fixed head.

Test 04. Force Sector Compare Check

Test 04 verifies that a Sector Compare check can be forced on and then reset. The test also verifies that an Attention is generated by the Sector Compare check when polling the drive.

Test 05. Sector Compare Attention

Test 05 verifies that an Attention is generated from a Sector Compare when polling the drive. The test also verifies that Busy is received in response to a Set Target command.

Test 06. Sector Compare

Test 06 verifies that Sector Compare is received for sectors 0, 1, 2, 4, 8, 16, 32, 64, and 128. It also performs the following functions:

1. Measures the duration of the Sector Compare and verifies it to be between 153 and 163 microseconds. This applies to all of the previously mentioned sectors except sector 127.
2. Verifies that the Transfer Sector command transfers the contents of the Sector Counter to the Target Register for sectors 0 and 127.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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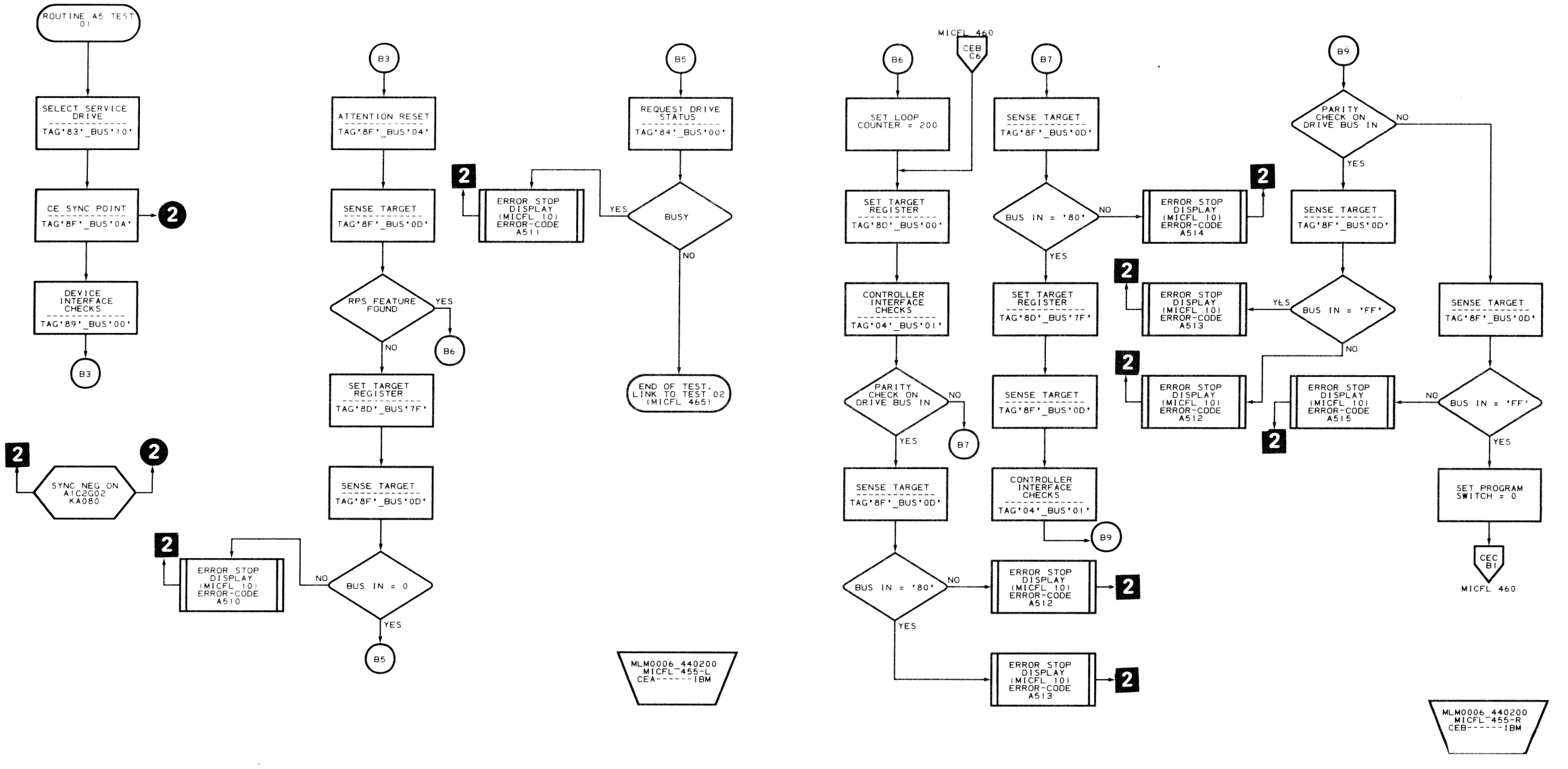
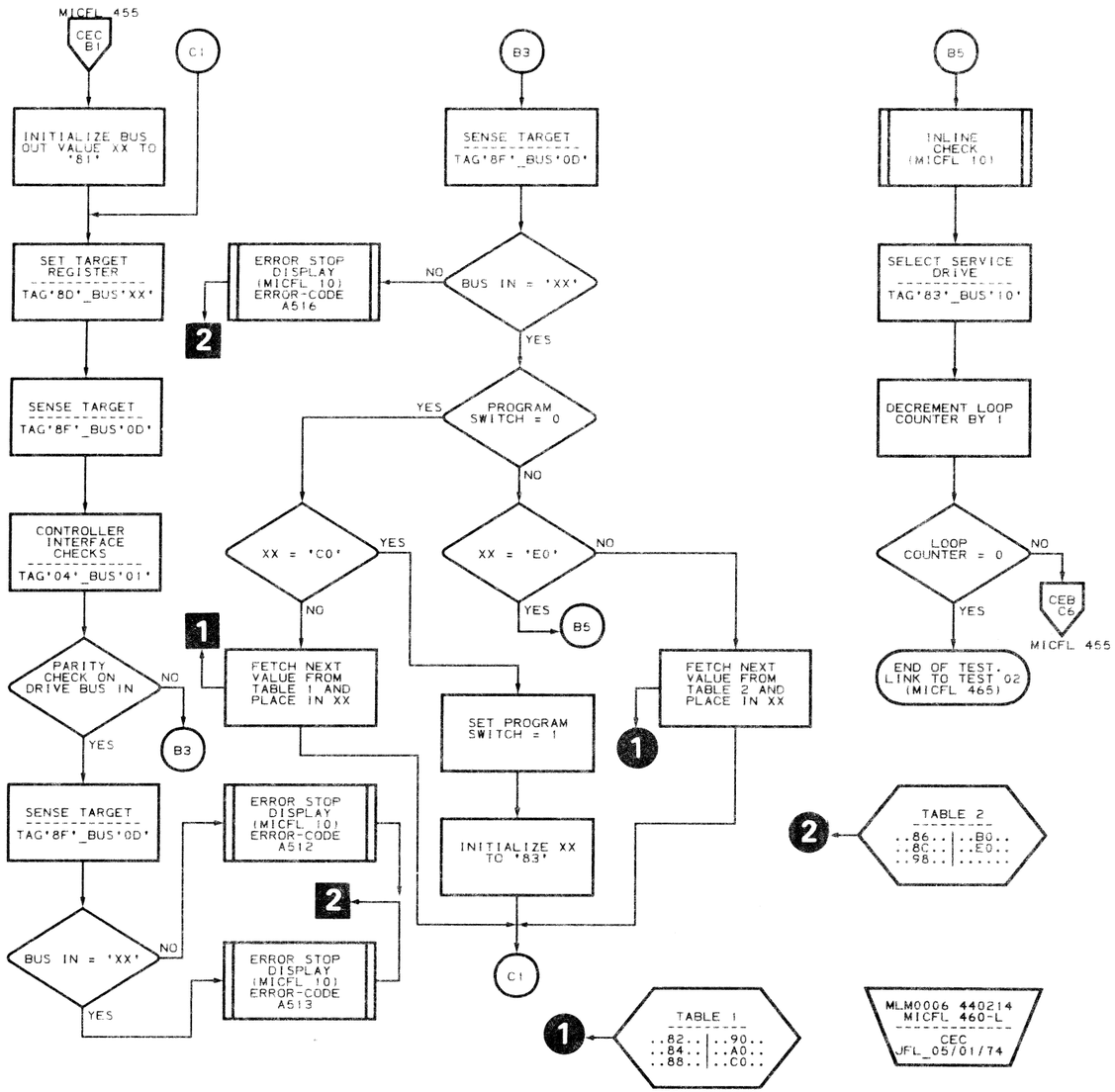
TARGET REGISTER TEST (Routine A5)



TARGET REGISTER TEST (Routine A5)



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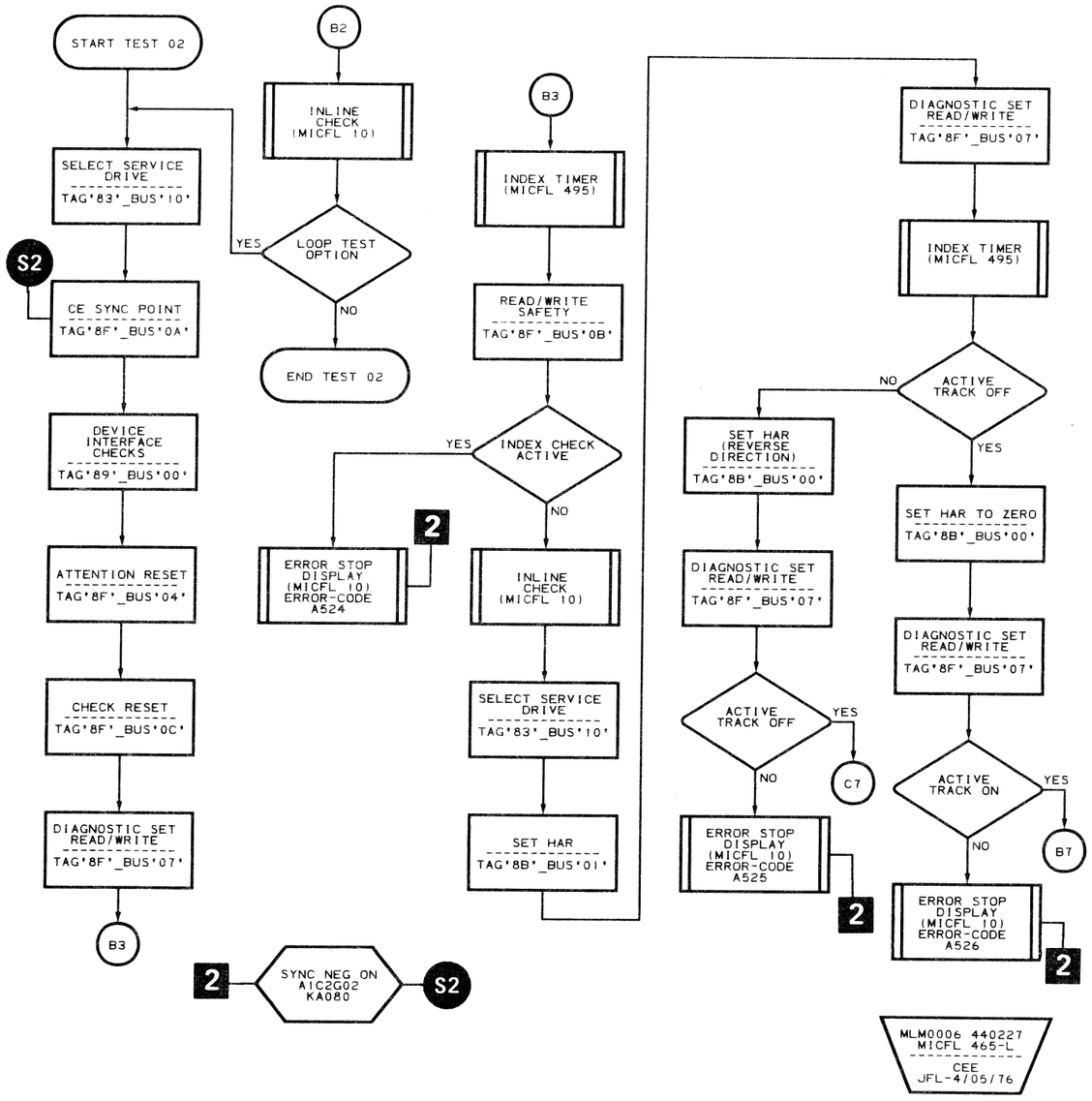
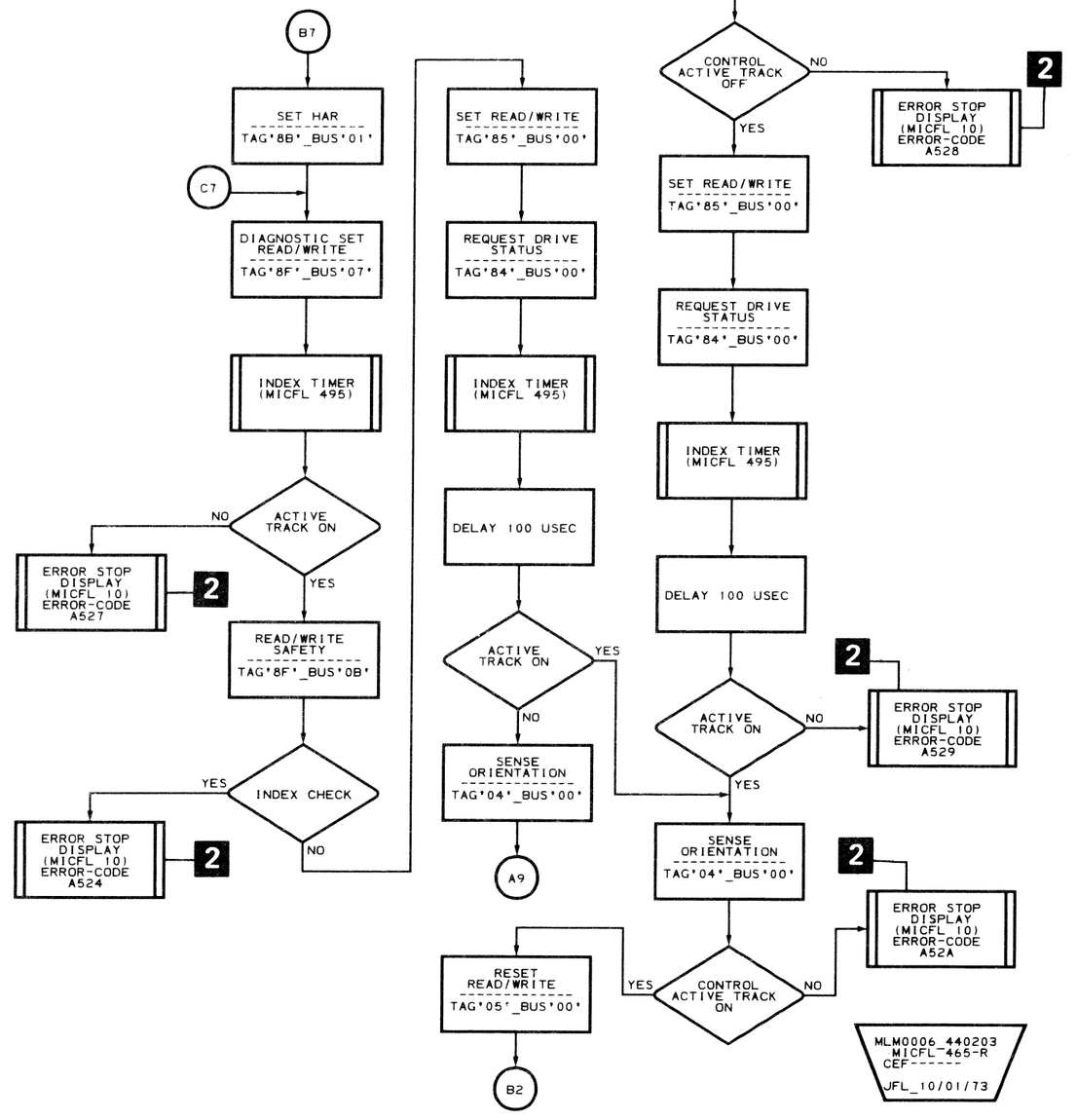
INDEX TEST (Routine A5)





CC0460	2747068
Seq. 1 of 2	Part No.(N)

440200	440202	440203	440214	440218	440227	
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74	14 Sep 76	

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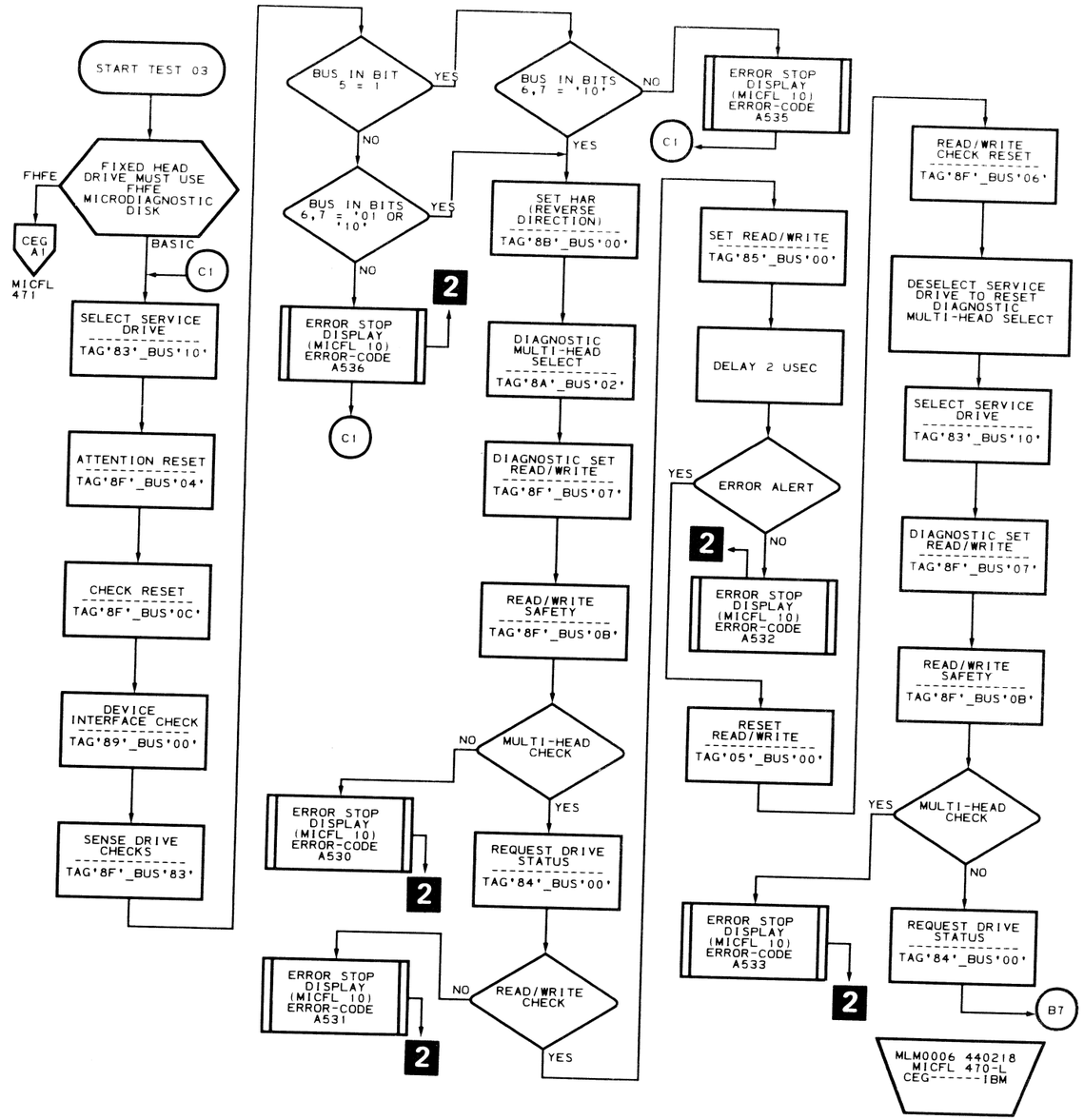
FORCE MULTI-HEAD CHECK (Routine A5)



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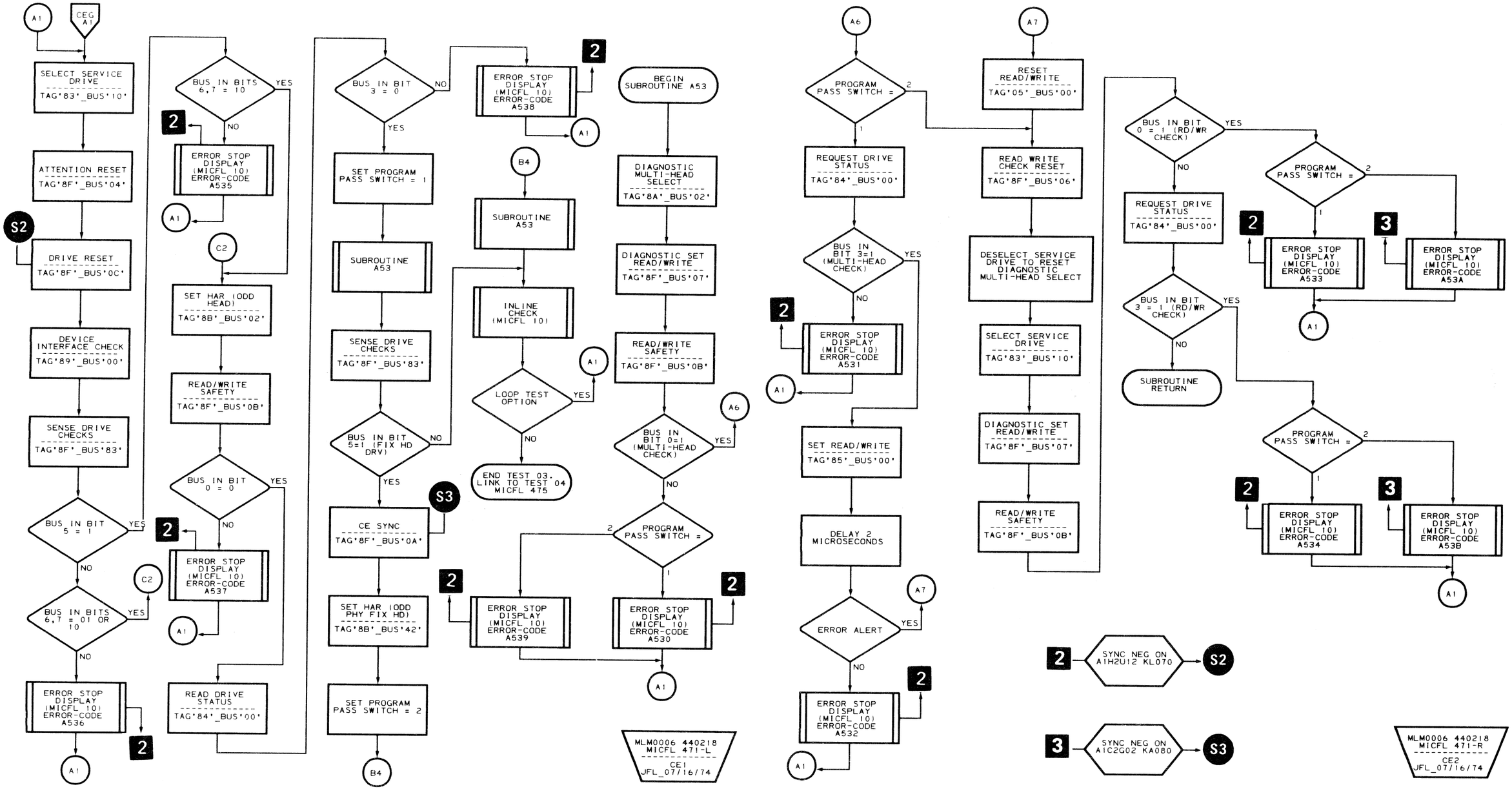
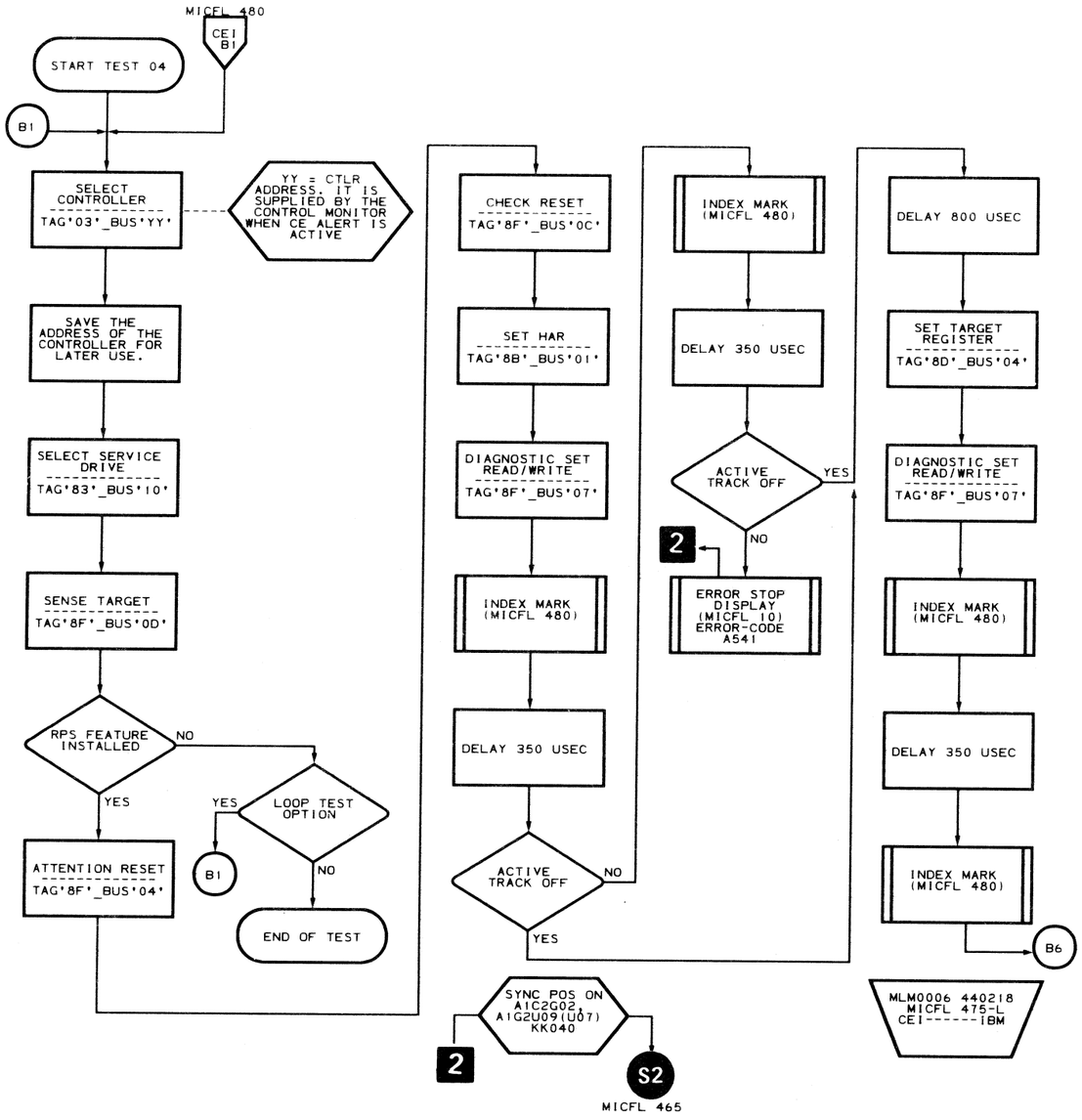
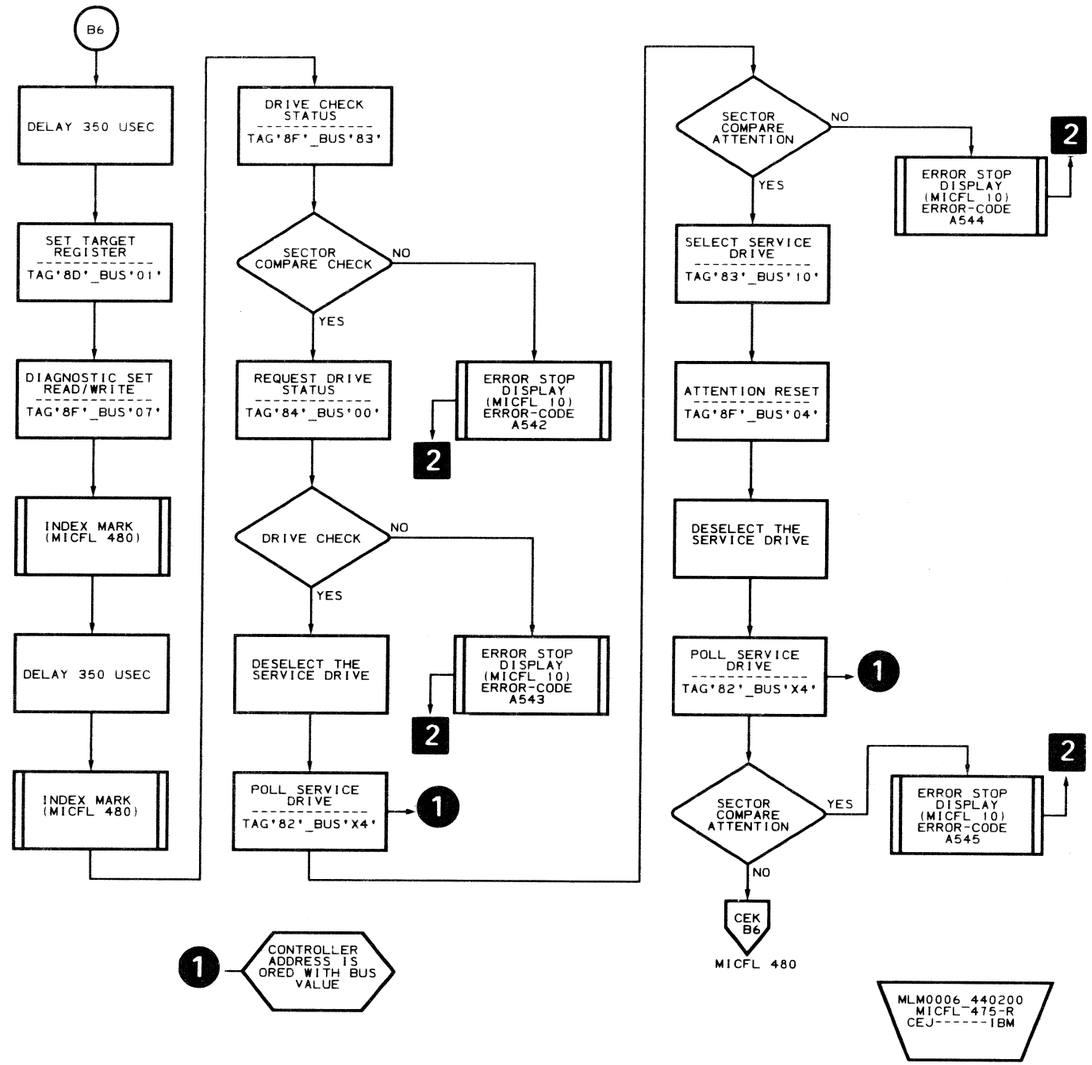
FORCE MULTI-HEAD CHECK (Routine A5)



3340	CC0470	2747069	440200	440202	440203	440214	440218	
	Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74	

FORCE SECTOR COMPARE CHECK (Routine A5)





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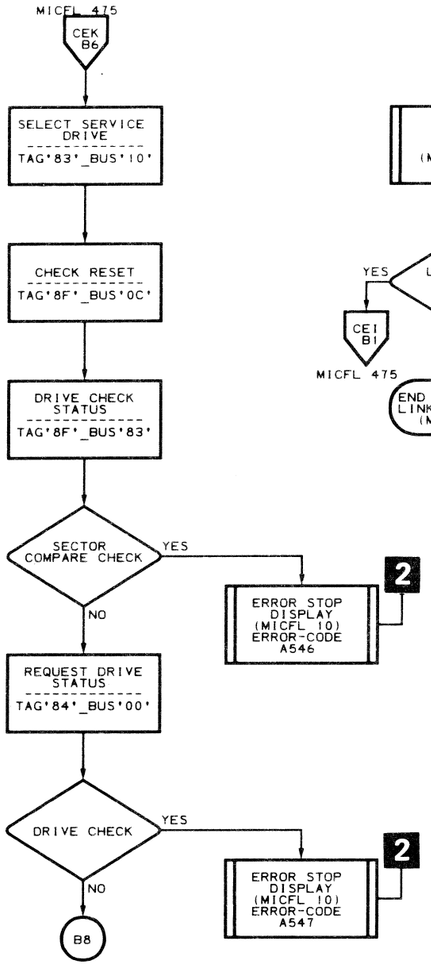
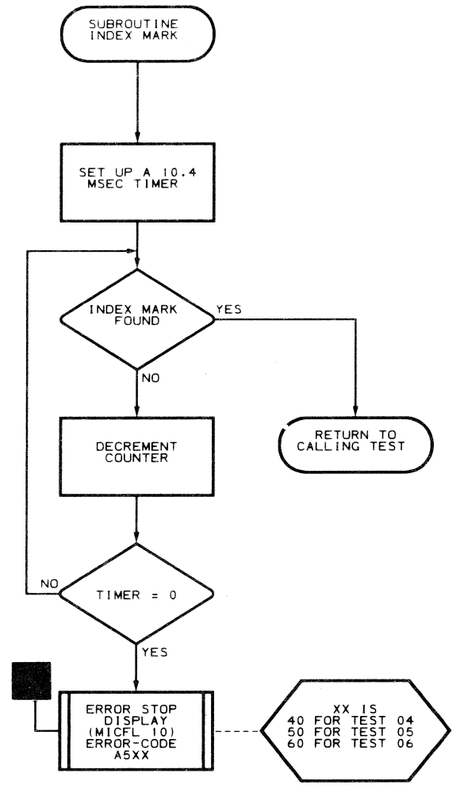
FORCE SECTOR COMPARE CHECK (Routine A5)





MLM0006 440200
MICFL 480-L
CEK
JFL_07/12/73

MLM0006 440200
MICFL 480-R
CEL
JFL_07/12/73

CC0480 Seq. 1 of 2	2747070 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74			

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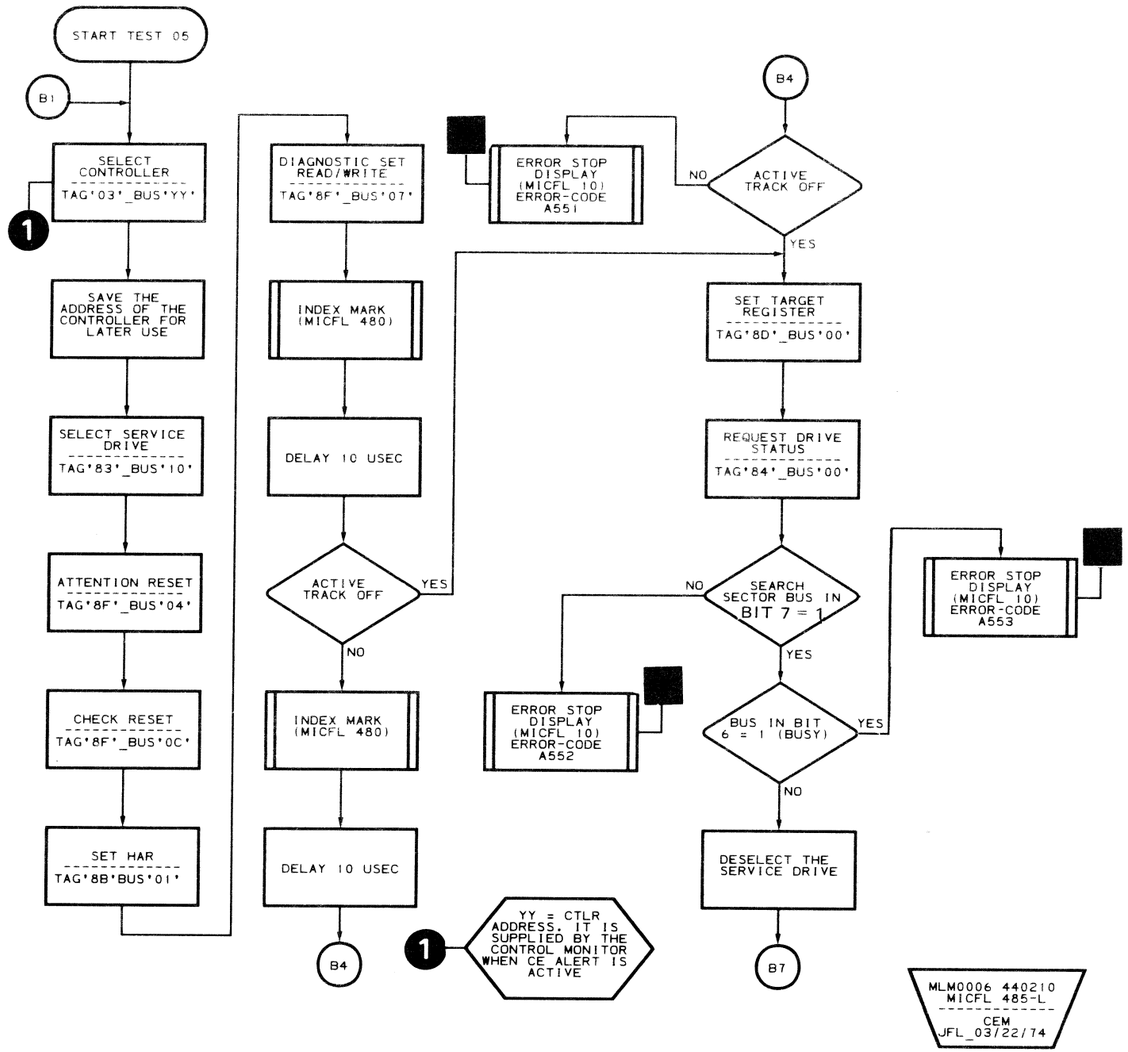

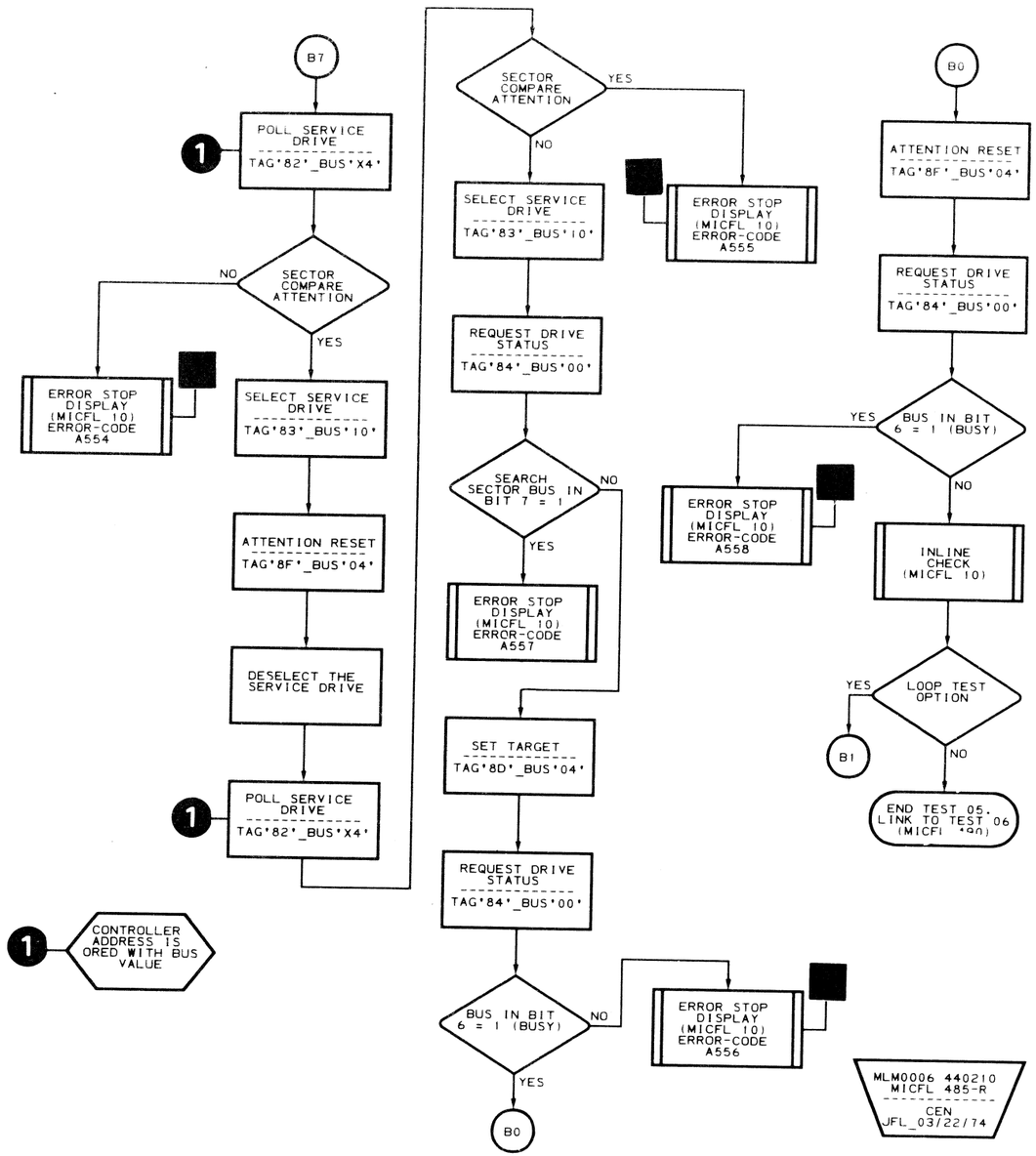

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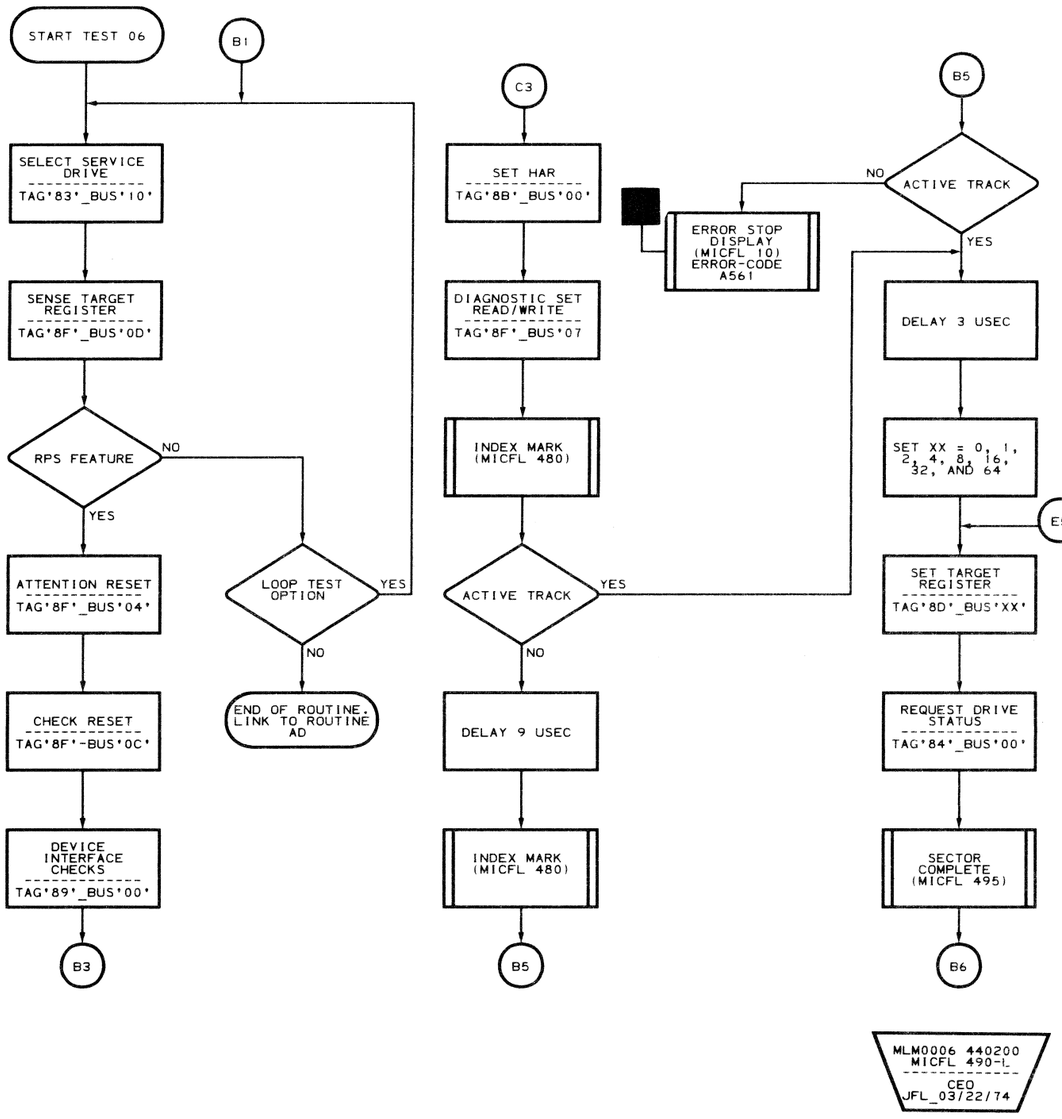

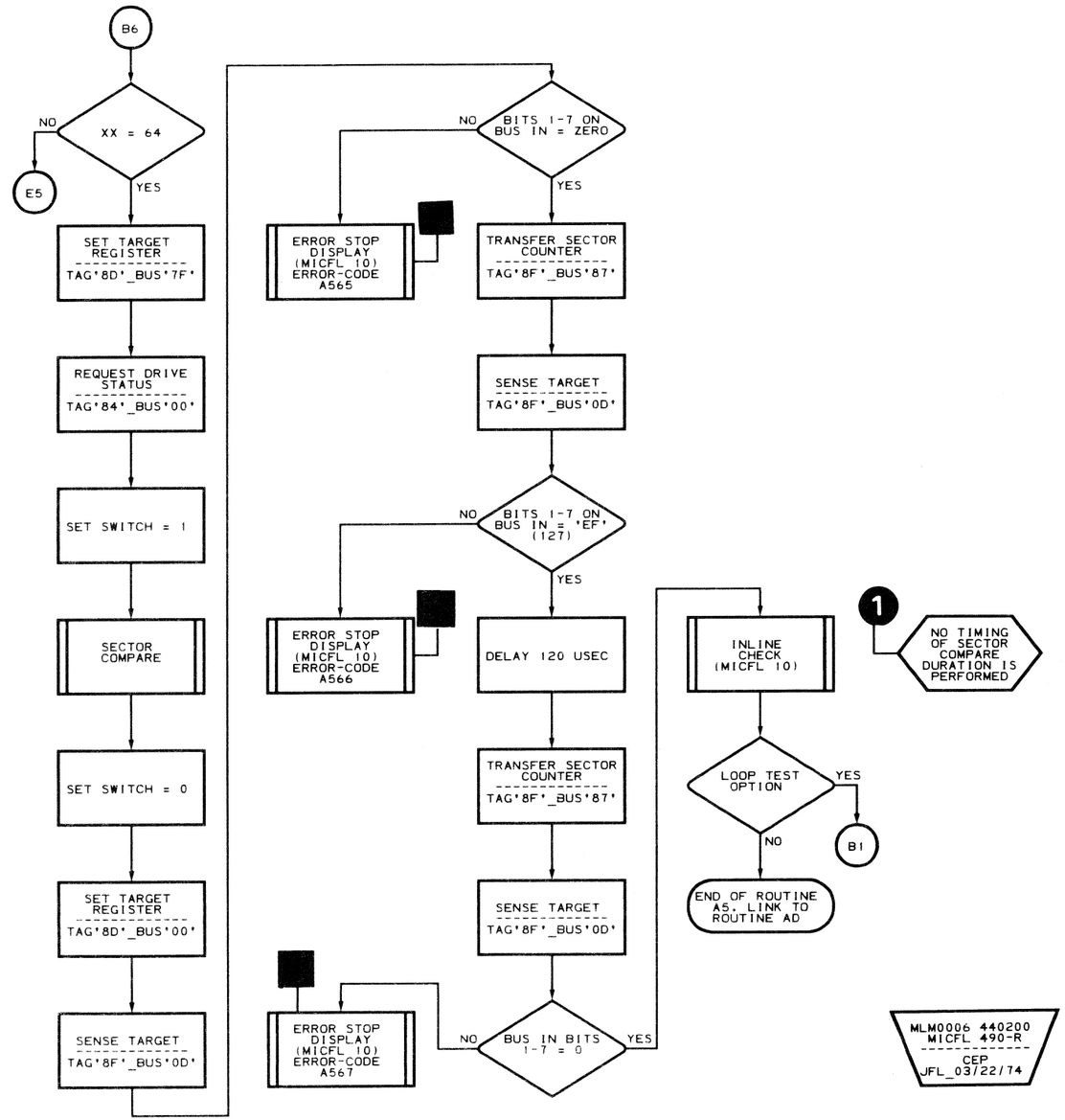

CC0490	2747071	440200	440202	440203	440210	440227		
Seq. 1 of 2	Part No.(N)	25 June 73	7 Sept 73	2 Nov 73	15 Apr 74	14 Sept 76		

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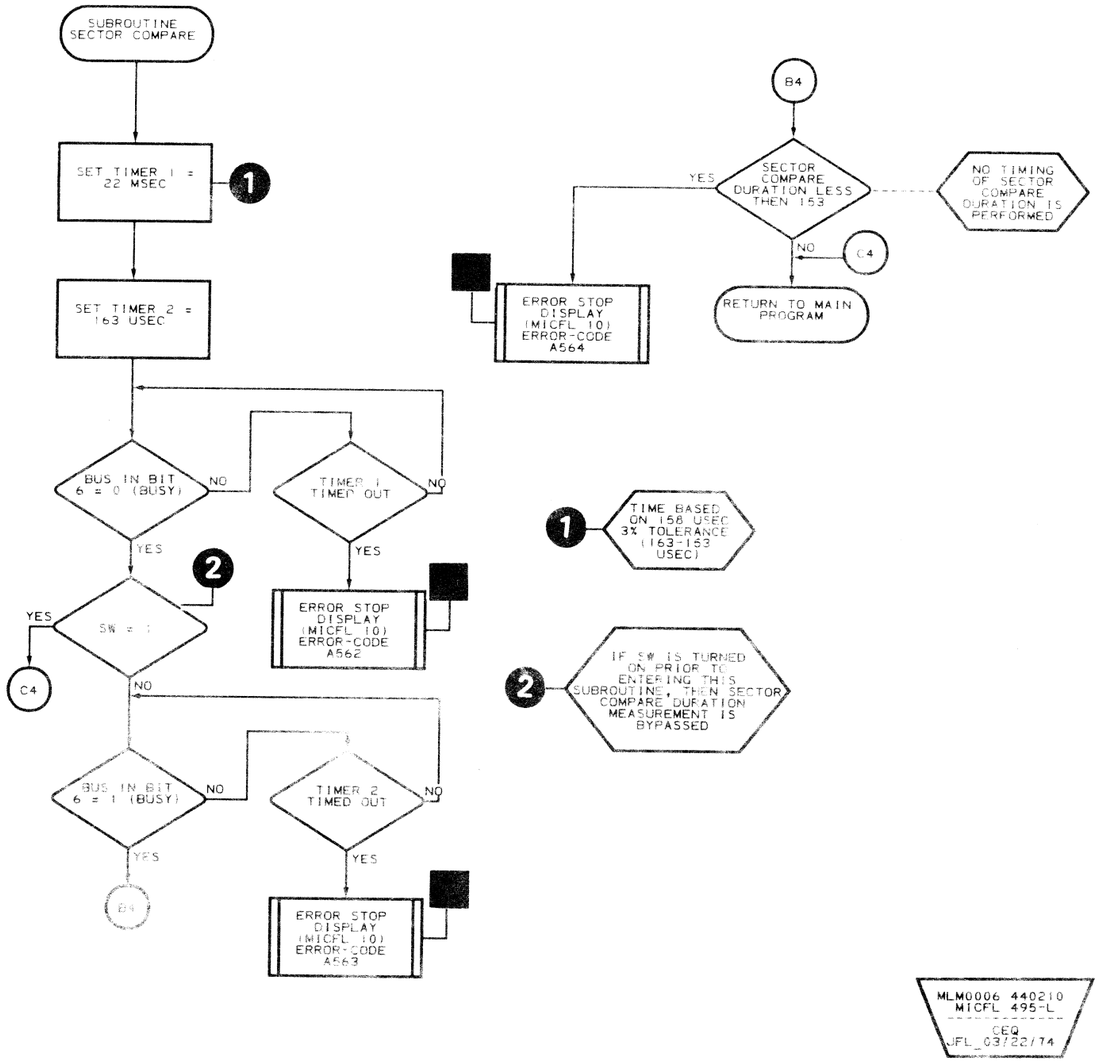

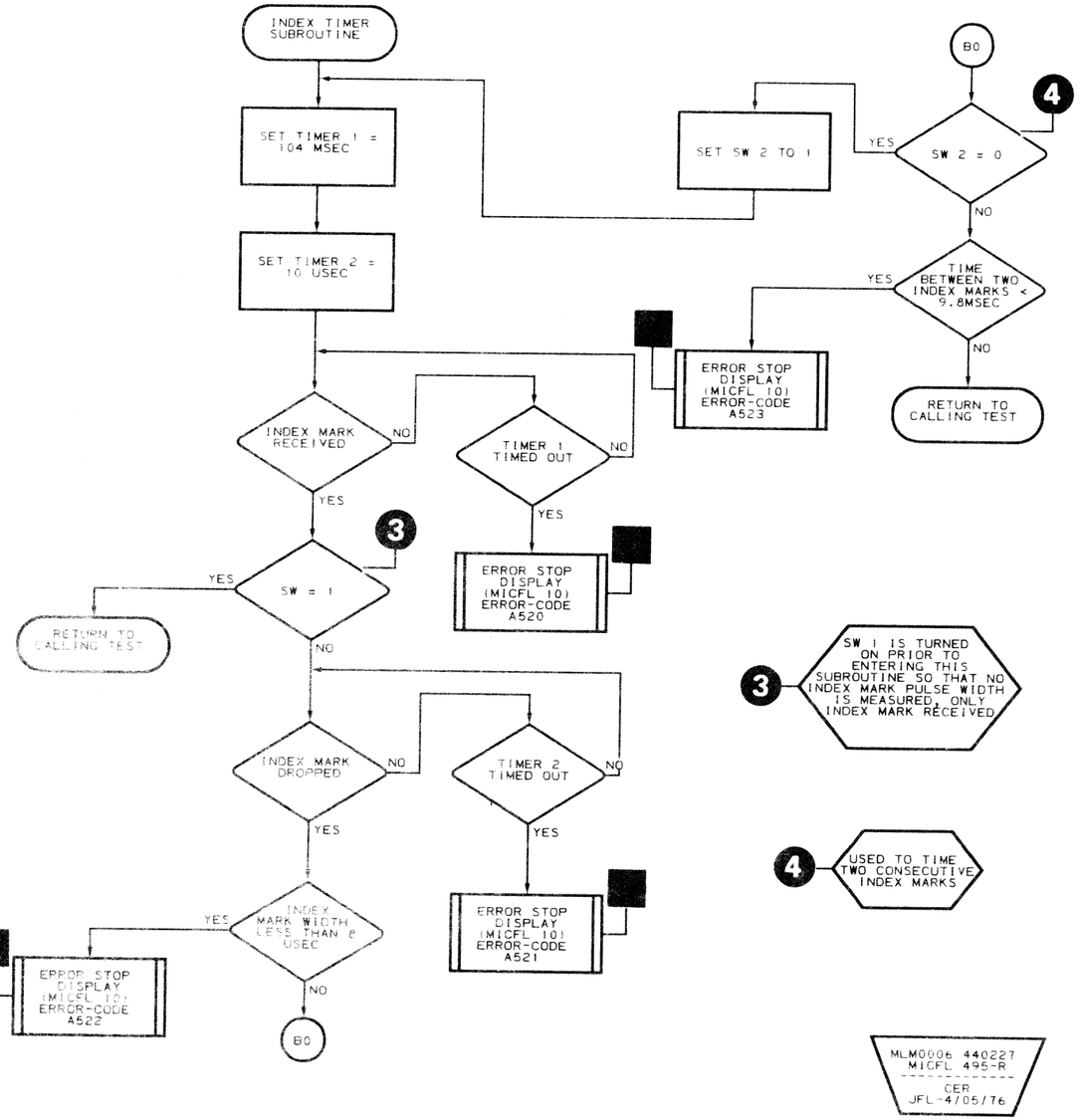

CC0490	2747071
Seq. 2 of 2	Part No. (N)

440200	440202	440203	440210	440227		
25 June 73	7 Sept 73	2 Nov 73	15 Apr 74	14 Sep 76		

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ROUTINE A6 – DYNAMIC SERVO TESTS PART II

DESCRIPTION

Routines A4, A6, and A8 are dynamic servo tests. The purpose of Routine A6 is to verify the correct operation of the servo during a Recalibrate operation. The routine consists of six tests ('01'–'06').

Test 01. Access Timer Accuracy

The purpose of Test 01 is to verify the operation of the Access Timer. A Recalibrate tag is issued and followed by a Diagnostic Servo Reset to stop the Recalibrate operation. This allows the Access Timer to time out. The test checks that the Access Timer times out in 180±40 milliseconds.

Test 02. Open Loop Servo

Test 02 verifies that carriage movement can be detected after a Recalibrate instruction and that the measured acceleration is indicative of a closed loop servo operation. This is done by issuing a Diagnostic Go Home command to move the access to the inner crash stop, after which a Recalibrate command is used to start access motion to the outer crash stop.

While the access is moving, the track-crossing bit in the access status byte is monitored. The times for two sets of 10 track crossing pulses are measured. These times are subtracted from one another and compared with a known specification.

Test 03. Coarse Velocity Gain Adjustment Check

Test 03 measures the recalibrate velocity and compares it with a known specification by using the Diagnostic Go Home tag to move the access to the inner crash stop. The Recalibrate tag is then issued to start access motion. Once access motion has started, the track crossing bit in access status is monitored to measure the velocity. The time samples are taken as follows:

1. Delay 20 tracks to gain speed.
2. Measure the time for 10 tracks.
3. Skip 40 tracks.
4. Repeat steps 2 and 3 four times.
5. Measure 10 more tracks for the sixth sample.
6. Sum all measurements and compare the results with the specification.

Test 04. Rezero Pattern Area Detection

Test 04 verifies that the servo can detect the rezero pattern area and the advance from State 0 to State 2. It uses the Diagnostic Servo Go Home tag to move the access to the inner crash stop. A Recalibrate command is issued to start access motion. After access motion is started, the track crossing bit in access status is monitored for a pulse width greater than a normal track (the rezero pattern area is reflected in the track crossing bit as an extra wide track). The The Access State latch should have advanced from State 0 to State 2.

Test 05. Rezero From Outer Crash Stop

Test 05 verifies that the servo advances from State 2 to State 6 and that the approach velocity to track 0 is correct. It uses the same method as Test 04 to obtain access motion. The track crossing bit in access status is used to determine the approach velocity.

Test 06. Rezero On-Track Verification

Test 06 is used to verify that the servo captures on track 0 during a Recalibrate operation. The method of obtaining access motion is the same as Test 04. The Track Crossing latch and state bits in access status are monitored to determine when the servo has reached the correct state, after which the Home Address is read to verify the access position.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedure.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

CC0525	2747506	440200	440203					
Seq. 1 of 1	Part No. ( )	25 Jun 73	2 Nov 73					

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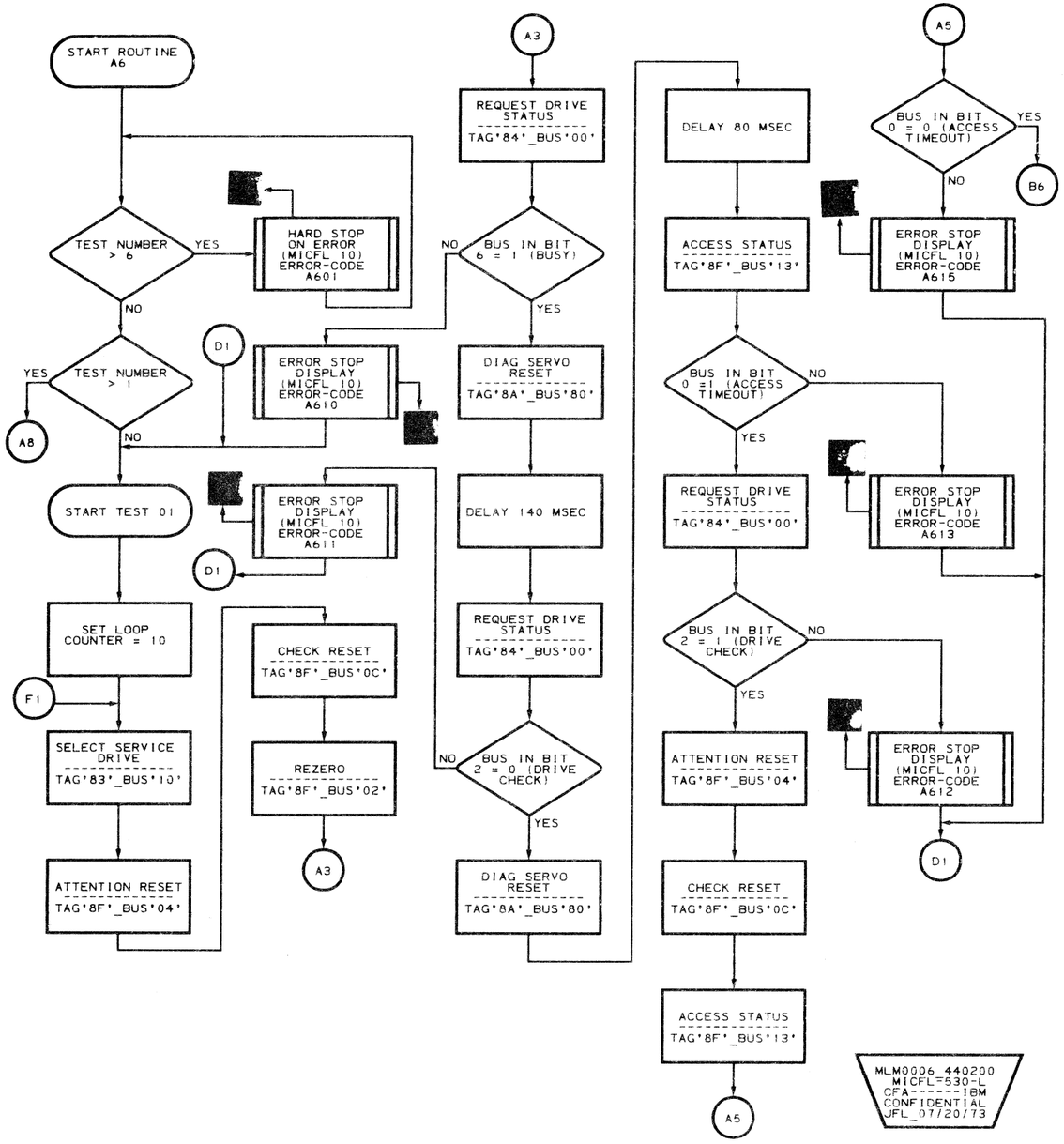
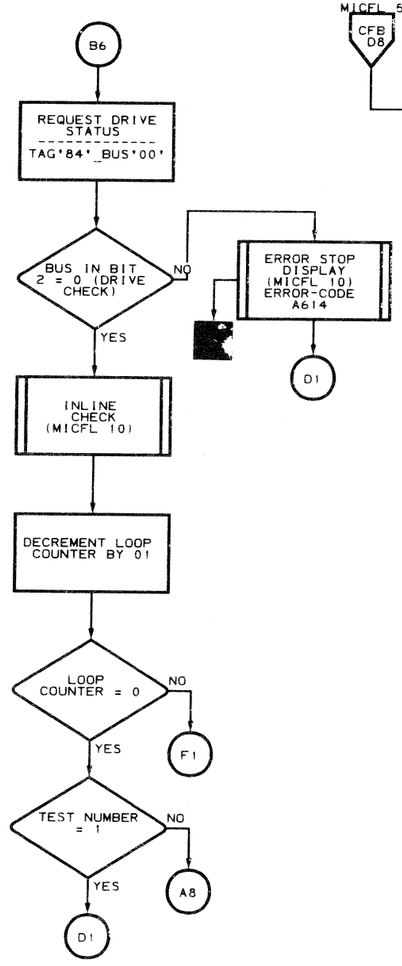
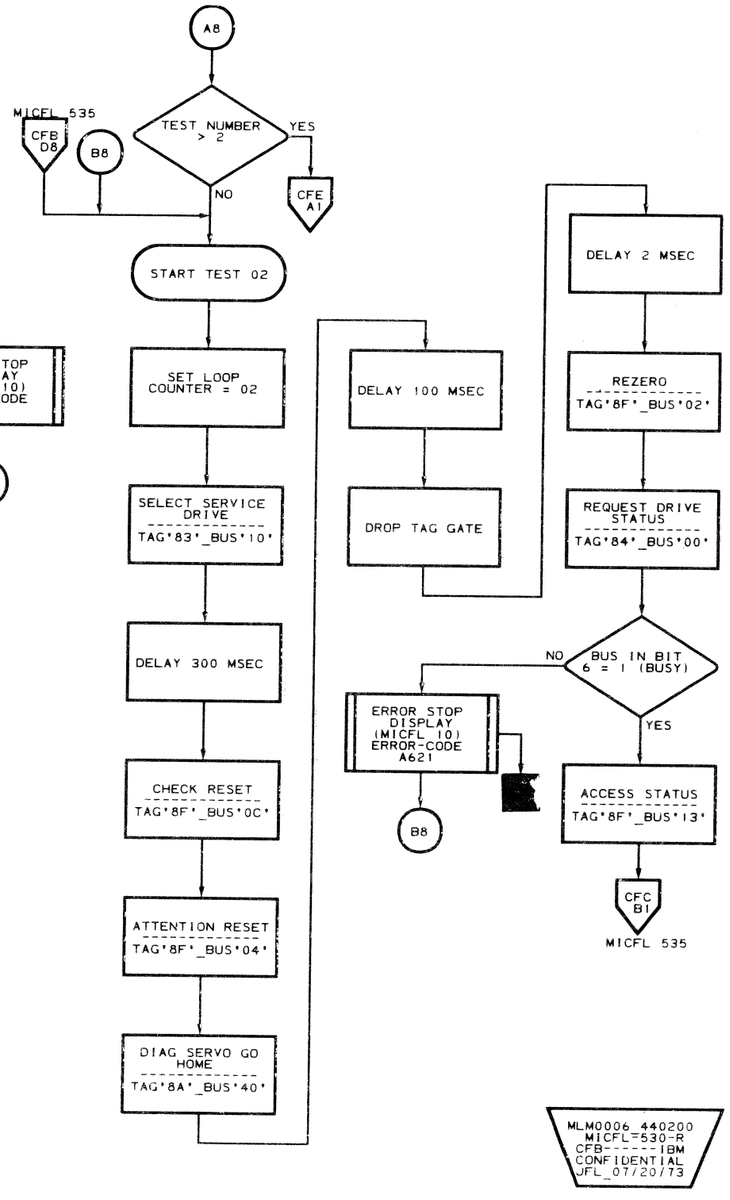
UNTIL DECEMBER 1973

DYNAMIC SERVO (TEST 1) (Routine A6)







CC0530	2747072
Seq. 1 of 2	Part No.( )

440200	440202	440203				
25 Jun 73	7 Sept 73	2 Nov 73				

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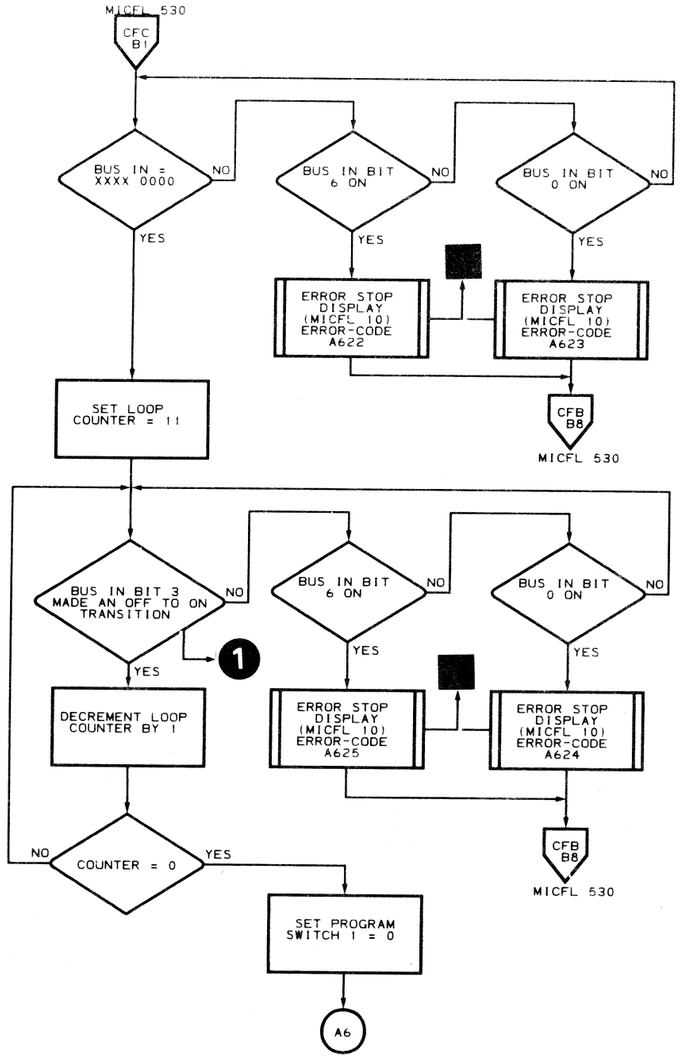
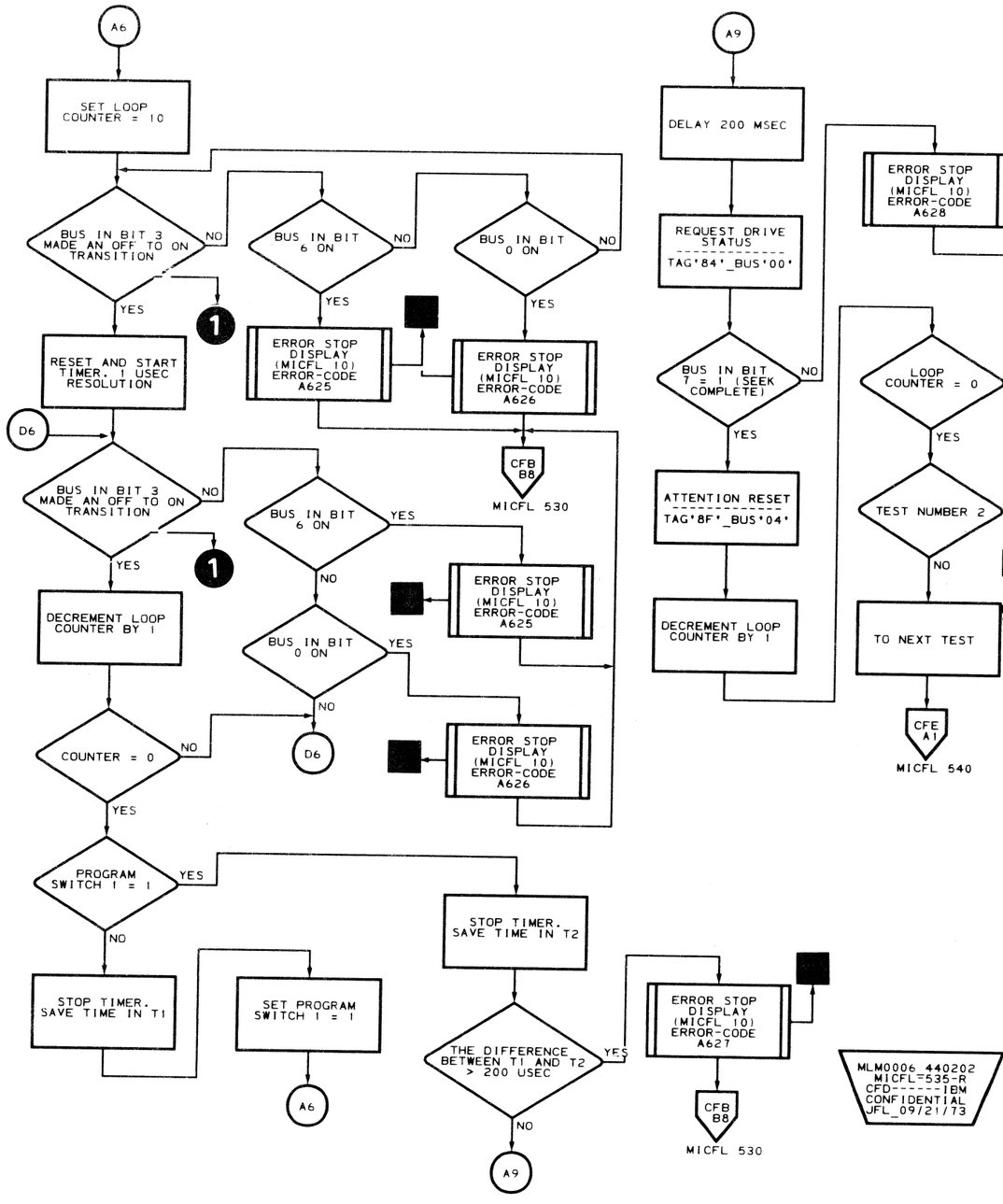
UNTIL DECEMBER 1973



1 BUS IN BIT 3 IS THE TRACK CROSSING LATCH UNDER ACCESS STATUS TAG

MLM0006_440200
MICFL=535-L
CFC------IBM
CONFIDENTIAL
JFL_07/23/73



MLM0006_440202
MICFL=535-R
CFD------IBM
CONFIDENTIAL
JFL_09/21/73

CC0530 Seq. 2 of 2	2747072 Part No.( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73				

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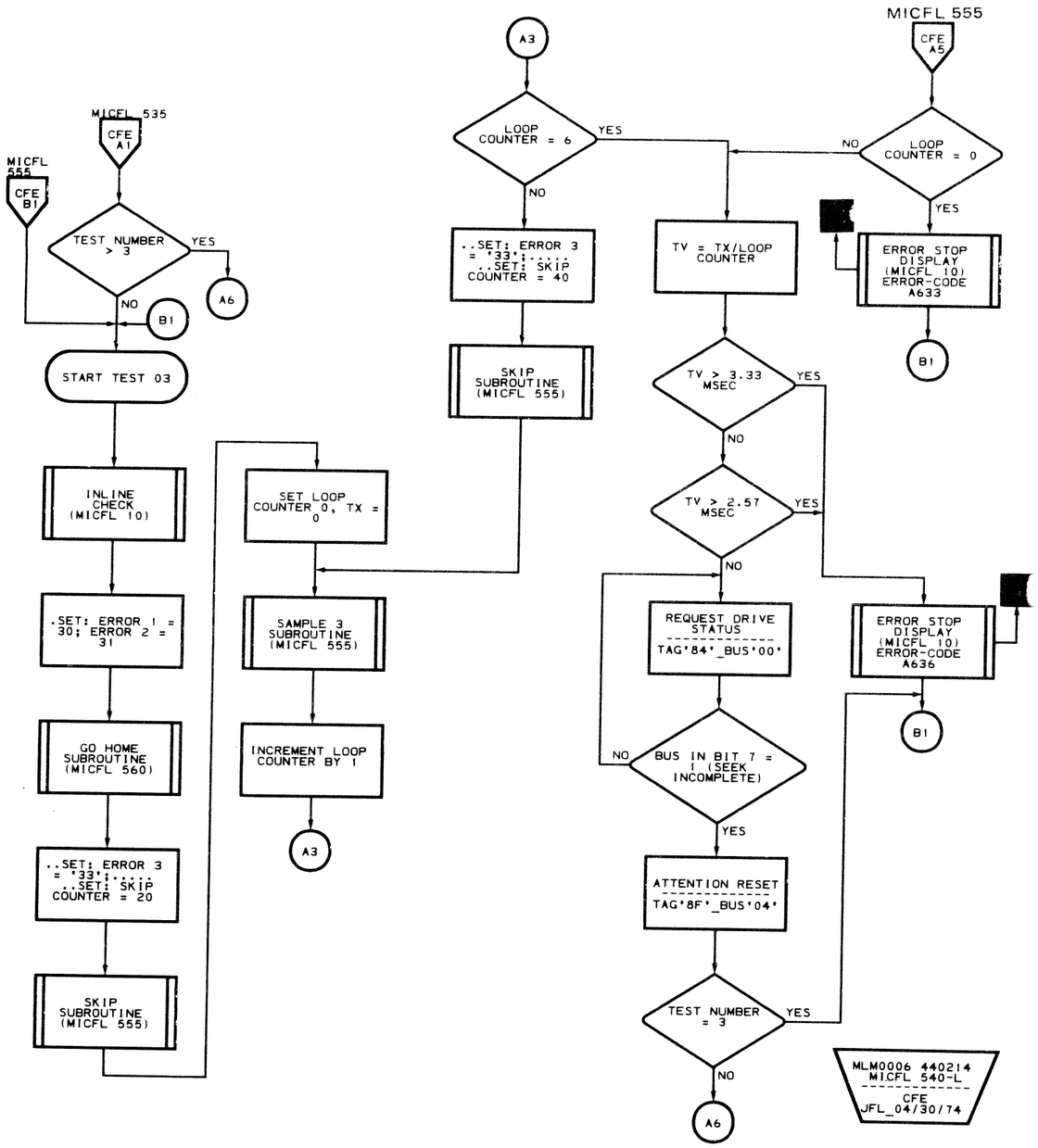
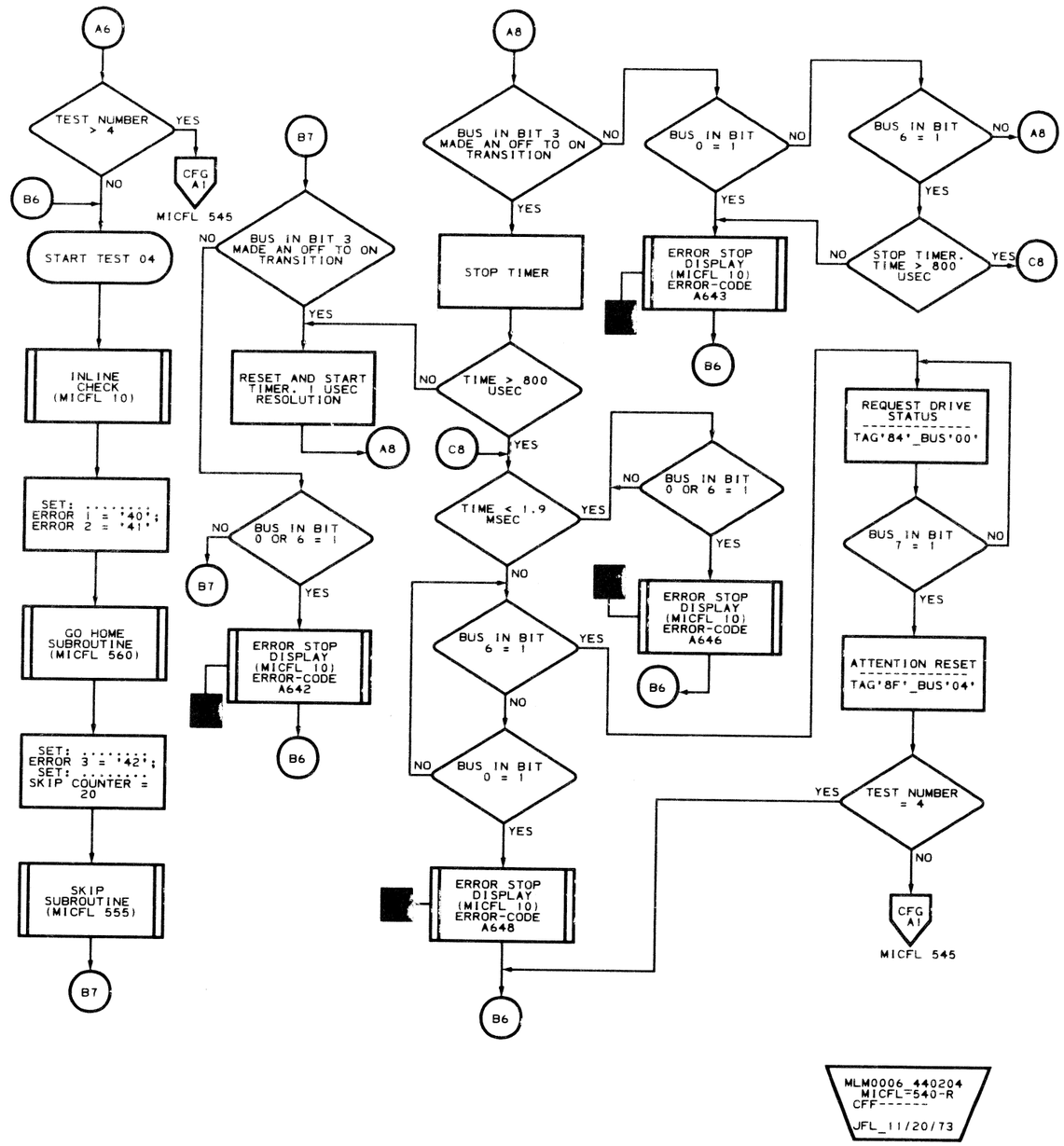
UNTIL DECEMBER 1973

DYNAMIC SERVO (TESTS 3 AND 4) (Routine A6)





CC0535	2747073
Seq. 1 of 2	Part No.( )

440200	440202	440203	440204	440205	440214	
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	28 Jan 74	17 Jun 74	

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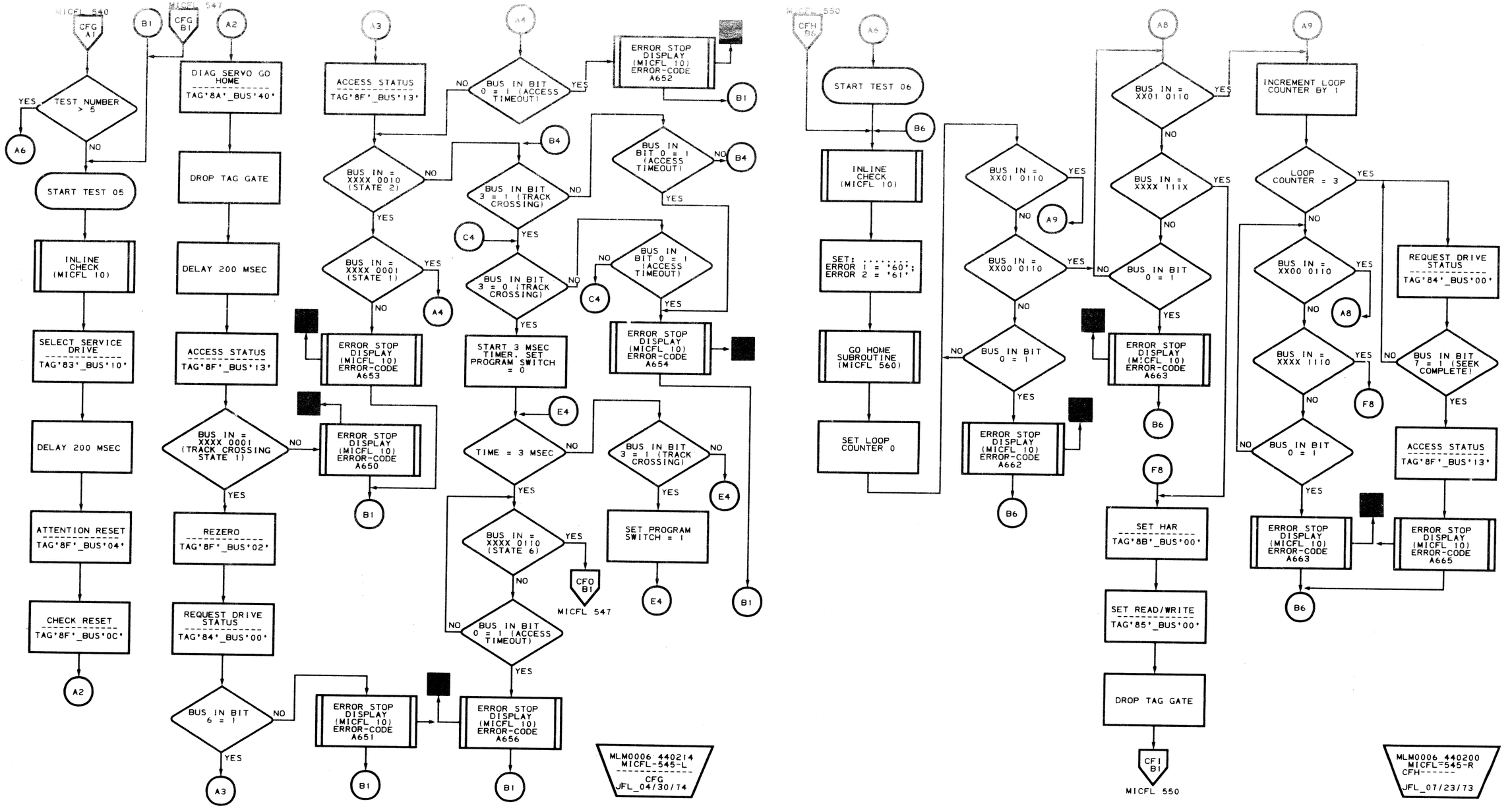
DYNAMIC SERVO (TEST 5 AND 6) (Routine A6)



CC0535	2747073
Seq. 2 of 2	Part No.( )

440200	440202	440203	440204	440205	440214	
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	28 Jan 74	17 Jun 74	

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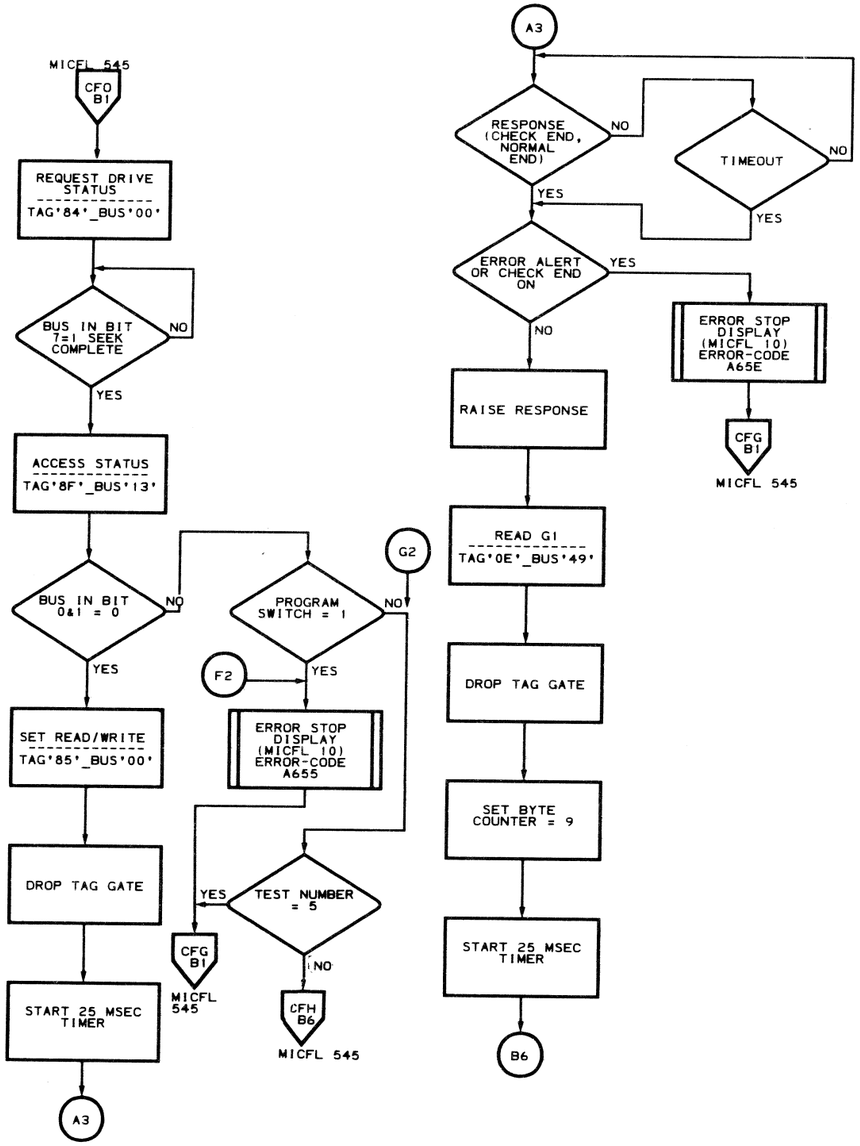
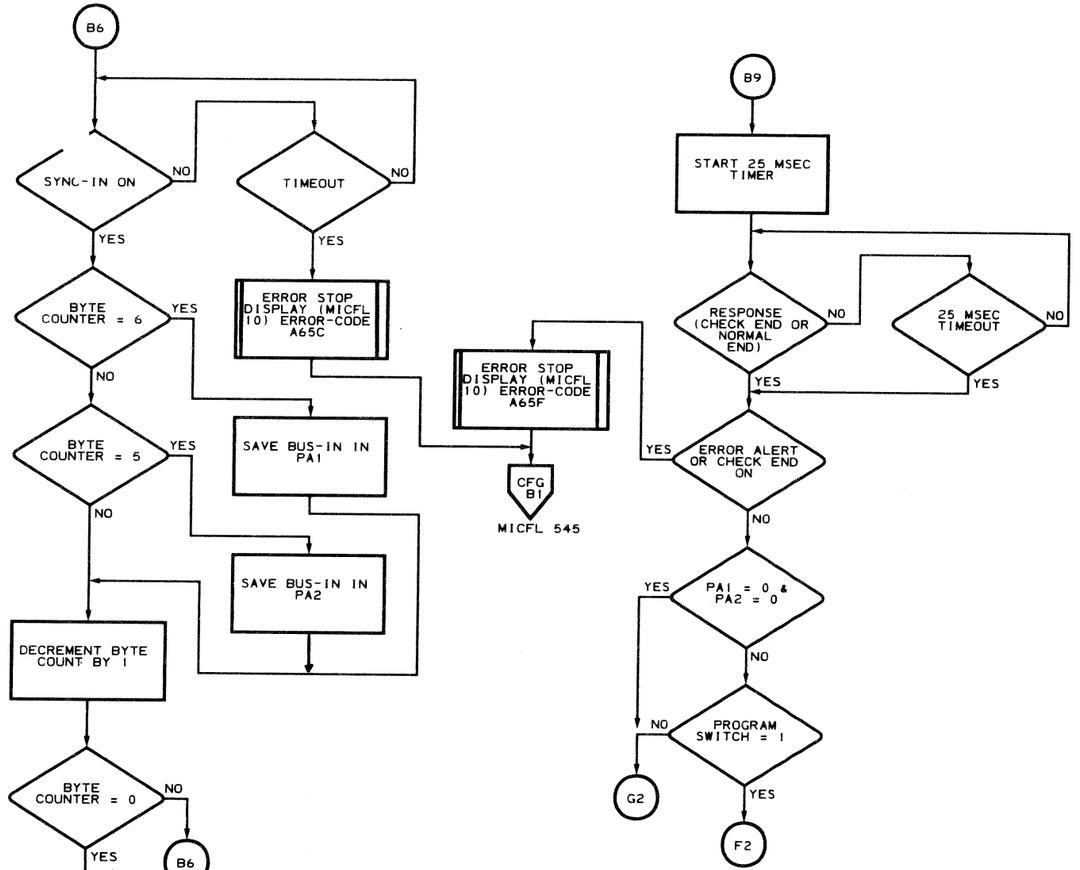
DYNAMIC SERVO (TESTS) (Routine A6)





MLM0006_440214
MICFL-547-L
CFO
JFL_04/30/74

MLM0006_440202
MICFL-547-R
CFP------
JFL_09/21/73

CC0545	2747074
Seq. 1 of 2	Part No.( )

440200	440202	440203	440214			
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74			

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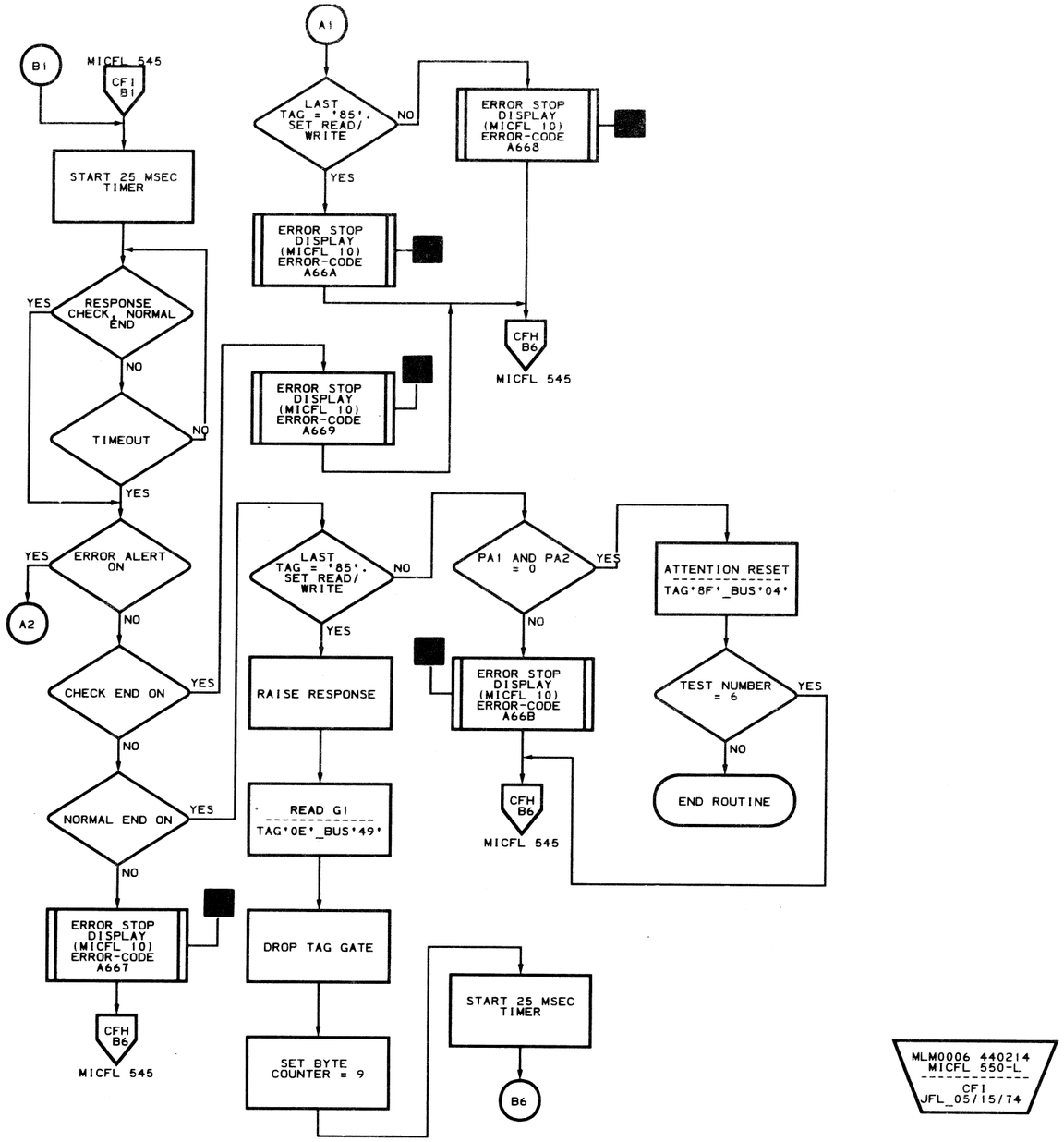
DYNAMIC SERVO (TEST 6) (Routine A6)



CC0545 Seq. 2 of 2	2747074 Part No.( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74			

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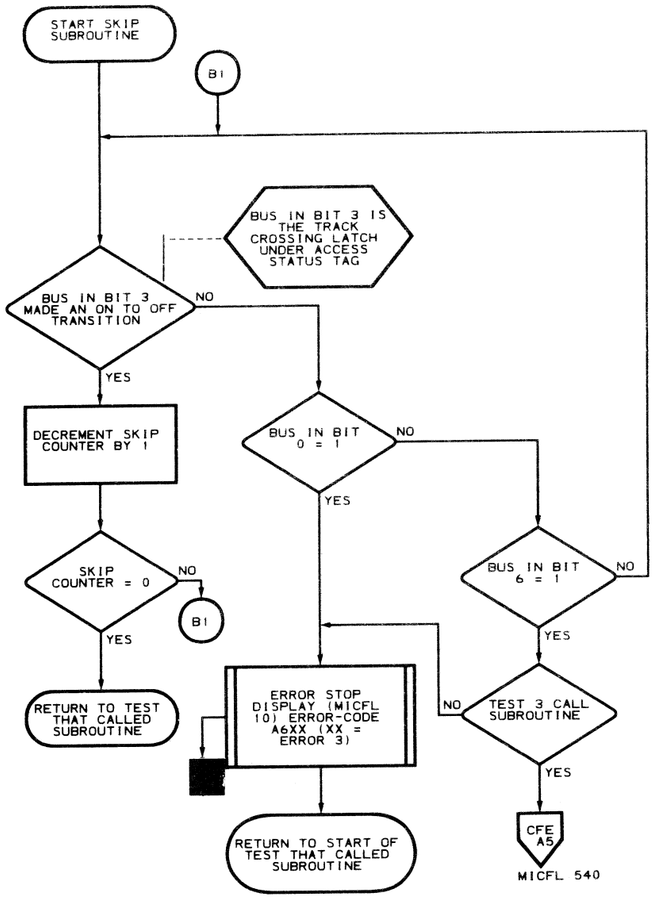
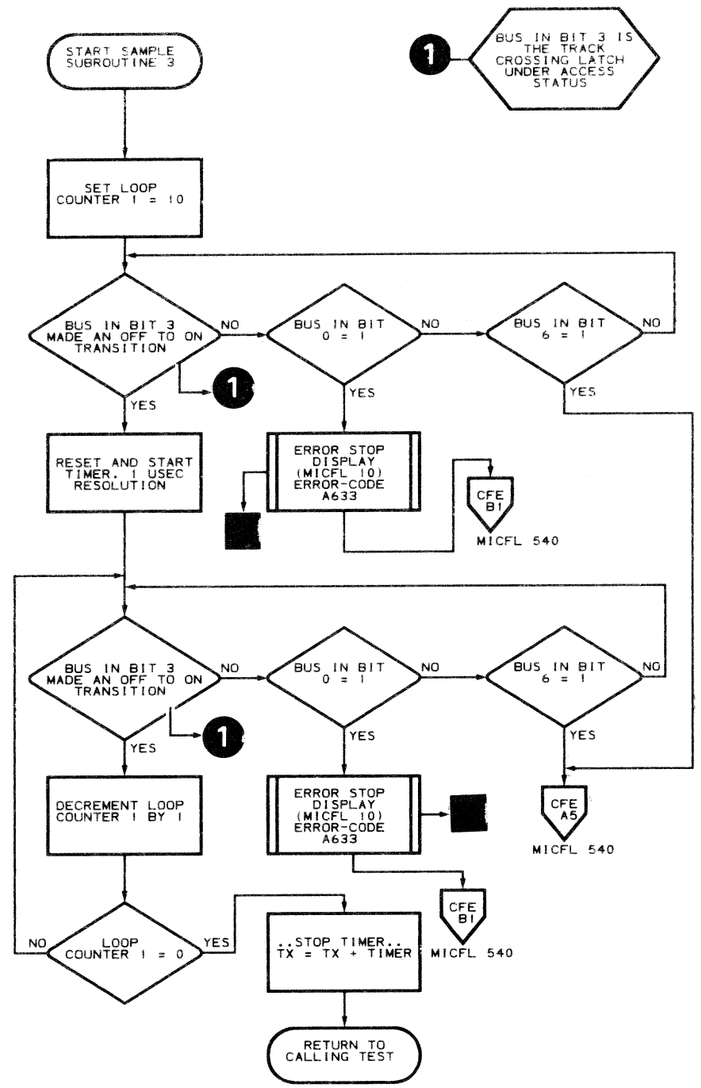
DYNAMIC SERVO SKIP / SAMPLE SUBROUTINE 3 (Routine A6)





MLM0006 440214
MICFL 555-L
CFK
JFL_04/30/74

MLM0006_440200
MICFL=555-R
CFL------
JFL_07/23/73

CC0555	2747075	440200	440202	440203	440214	440223		
Seq. 1 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	14 Mar 75		

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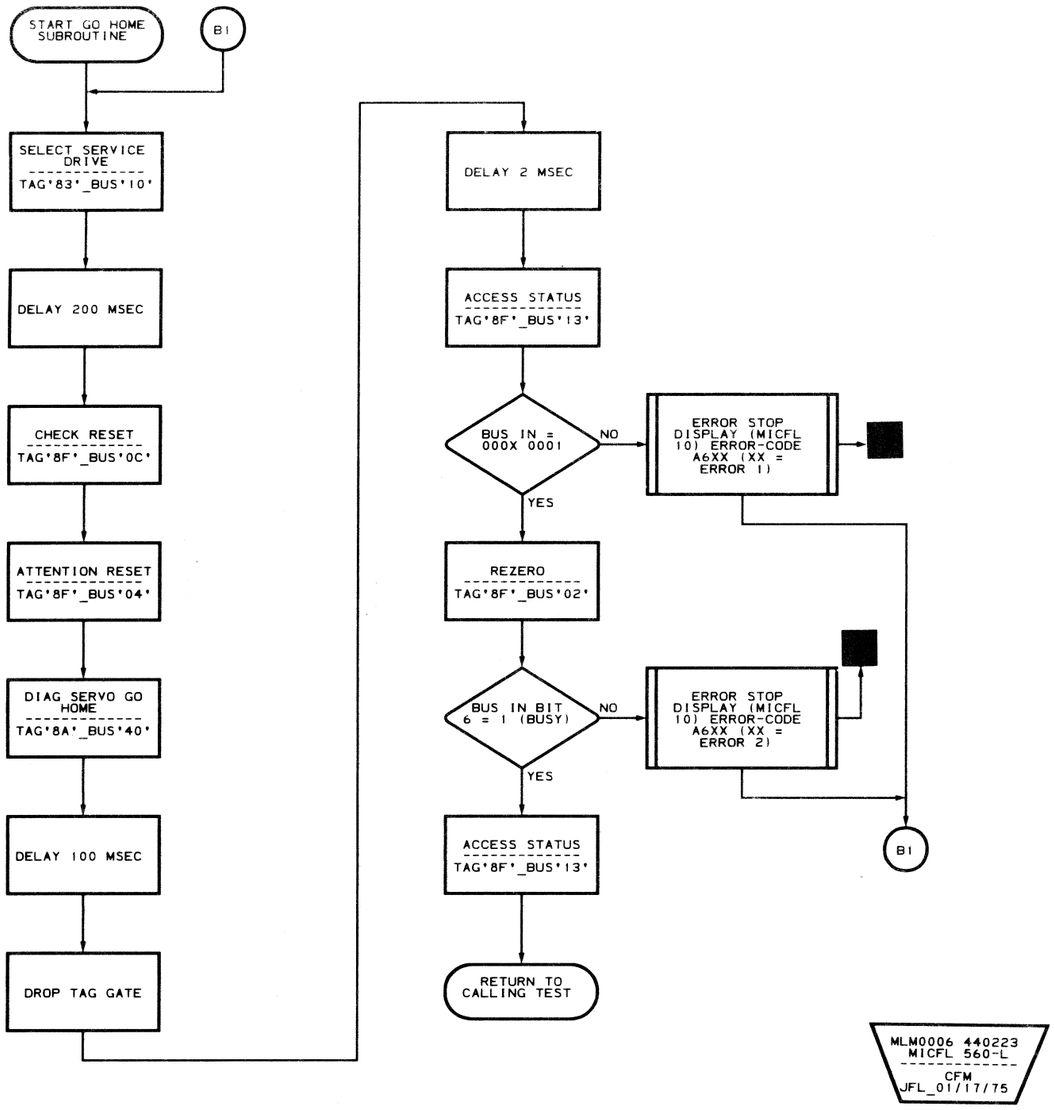

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ROUTINE A7 — 3340 DYNAMIC SERVO ADJUSTMENT PROGRAM

DESCRIPTION

The purpose of Routine A7 is to enable a complete servo adjustment under microprogram control. The servo velocity can be fine tuned with this program and the entire procedure performed without the aid of an oscilloscope. The program is designed to operate in two modes, verification and adjustment. The default mode of operation is verification mode where only Test 02 is run and the specification tolerance is 450±50 microseconds. In adjustment mode, Test 01 is run first and must reach successful completion before it links to Test 02. The specification tolerance of Test 02 is decreased to 450±10 microseconds. The amount of maladjustment of the servo velocity has no effect on successful execution of the program unless hardware failures are detected during execution of the test. The drive servo adjustment ensures compatibility with all IBM 3348 data modules, thus it is to be accomplished using any IBM 3348 data module, including IBM System/3 CE data module if appropriate.

Test 01. Coarse Adjustment

Note: This test is executed when adjustment mode is requested (Parameter 1 = 01).

Test 01 samples the data collected from six areas or bands across the disk during a Rezero operation from the home position to cylinder 0. The access is forced to home position by issuing a Diagnostic Servo Go Home command (Tag '8A' Bus '40'). This tag is held active for 130 milliseconds before being dropped. When it is dropped, a minimum delay of 5 milliseconds allows for voice coil motor current decay. A Rezero operation is then initiated to ensure linear access motion. A total of 40 track crossing pulses are passed before data collection beings. The data is collected by measuring the elapsed time for four track crossing pulse transitions (leading edge to leading edge). The measured elapsed time is compared to a low specification of 0.9 milliseconds and a high specification of 1.6 milliseconds. If this high/low specification is passed, the sample is added to an accumulator. If the specification is not passed, an error halt occurs. When the first sample is accumulated, thirty track crossing pulses are traversed before collecting the second sample. This procedure is repeated until six samples have been accumulated. The accumulated total is averaged and compared to a specification of 1.16±0.11 milliseconds. If this specification is not met, an error halt occurs. The amount of deviation (in microseconds) is displayed in Byte 2 of the logout. Proper adjustment procedures can be found in the ACC section. Test 01 may be restarted by using the '00' run control option. Successful completion of this test results in linking to Test 02.

Test 02. Fine Adjustment

Note: Test 02 runs in the following two modes:

(A) Verification mode is the default mode of operation (specification = 450± 50 microseconds).

(B) Adjustment mode is selected by entering parameter 1 = 01 (specification = 450±10 microseconds)

Test 02 issues a 128-cylinder seek, starting from cylinder 0. Clocking begins from the leading edge of the first track crossing pulse after the Seek Start command to the leading edge of the 118th track crossing pulse. A timer subroutine collects the elapsed time from the leading edge of the 118th track crossing pulse to the leading edge of the 120th track crossing pulse. This elapsed time is measured as the Difference Counter decrements from 0A to 08 during deceleration. This measured time is then compared to specification (A) or (B), above.

Failure of the measured time to meet the specification results in an error. If in verification mode, the error dictionary suggests rerunning the test in adjustment mode. If in adjustment mode, the amount of deviation (in microseconds) can be displayed in byte 2 of the logout. If the specification is met, the test is repeated 10 times before normal completion. The test may be restarted as often as desired using the '00' run control option. Loop control is defined as follows:

(A) Verification Mode:

1. Loop Test 2 only — Use run control option '02'.
2. Run Test 02 first; link back to Test 01; repeat indefinitely, or until error is encountered. Use run control option '06'.

Note: Test 01 can be run without selecting adjustment mode.

(B) Adjustment Mode:

1. Loop Test 02 only — Use run control option '02'.
2. Run Test 01 first; link to Test 02; repeat indefinitely, or until error is encountered. Use run control option '06'.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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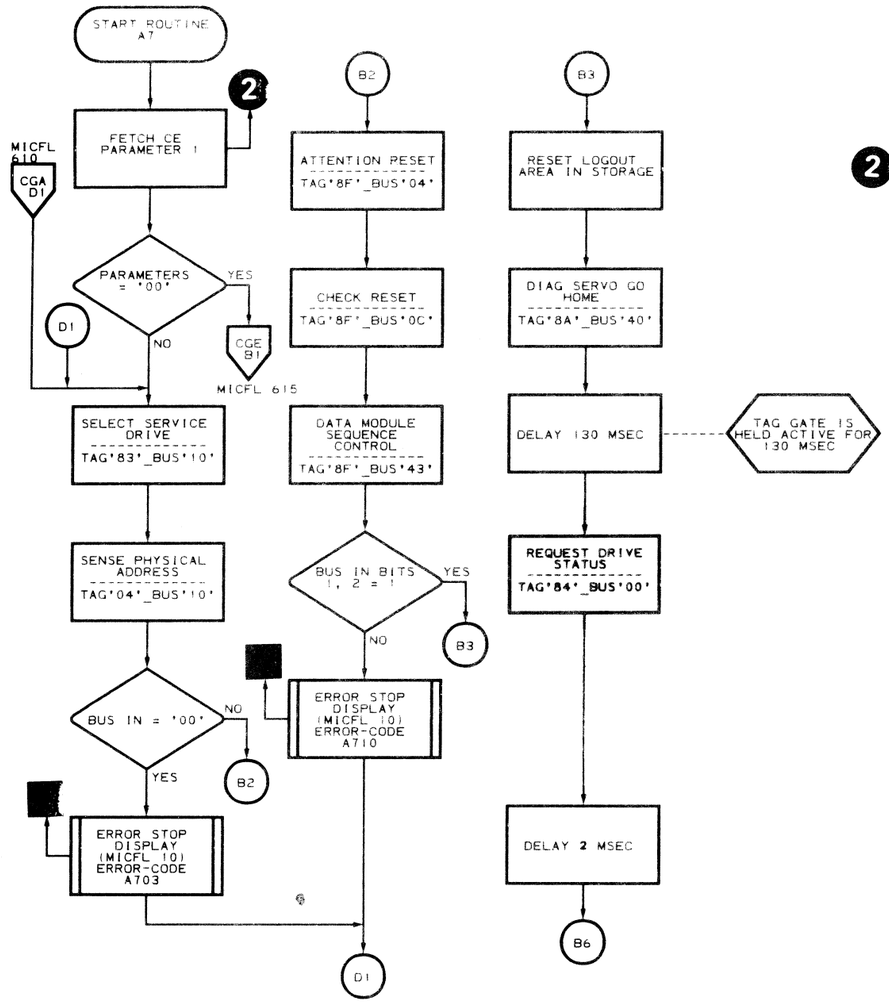
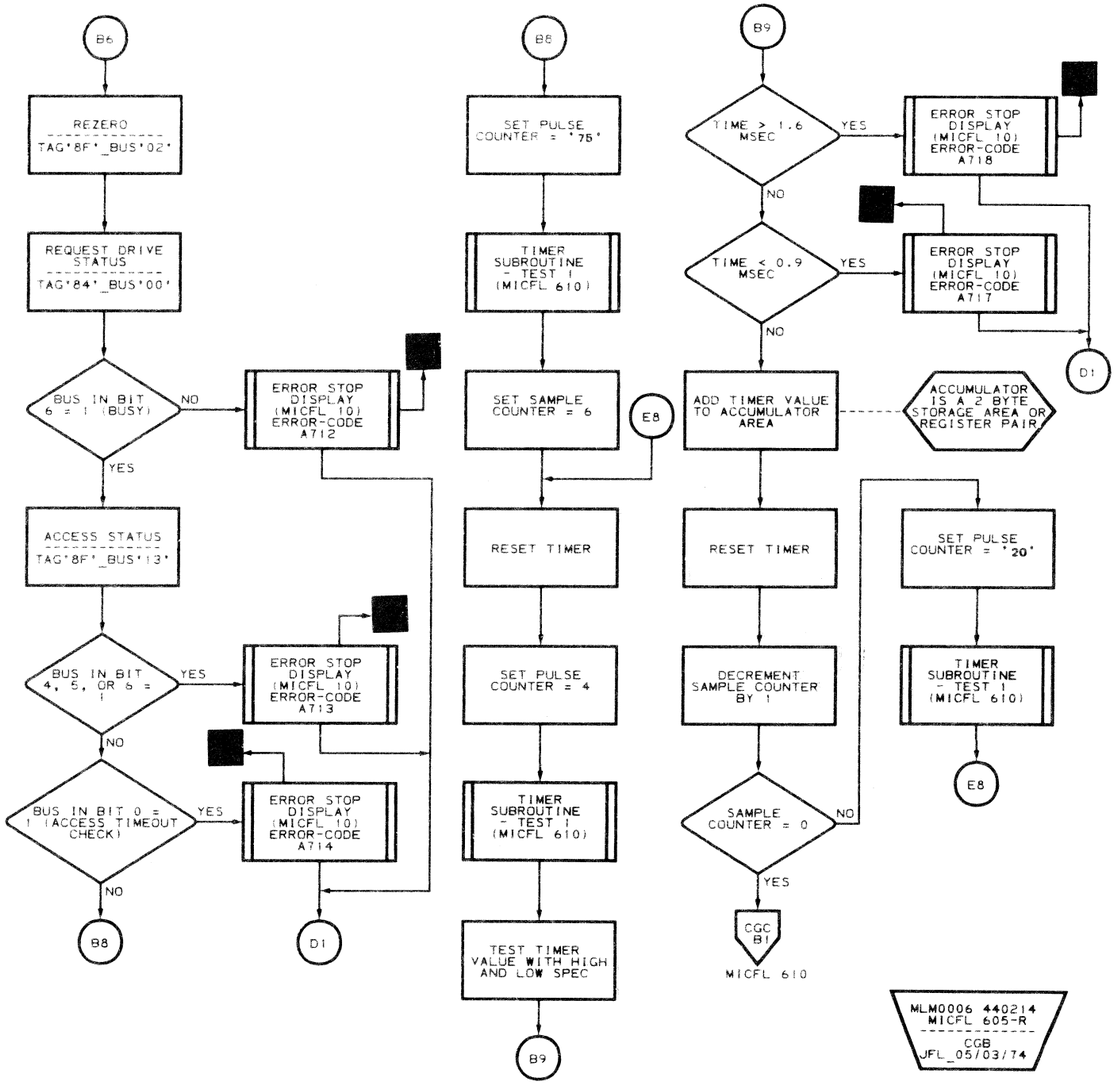
COARSE ADJUSTMENT (Routine A7)





MLM0006 440214
MICFL 605-L
CGA
JFL_05/01/74

MLM0006 440214
MICFL 605-R
CGB
JFL_05/03/74

CE0605	2747077	440200	440202	440203	440214	440223		
Seq. 1 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	14 Mar 75		

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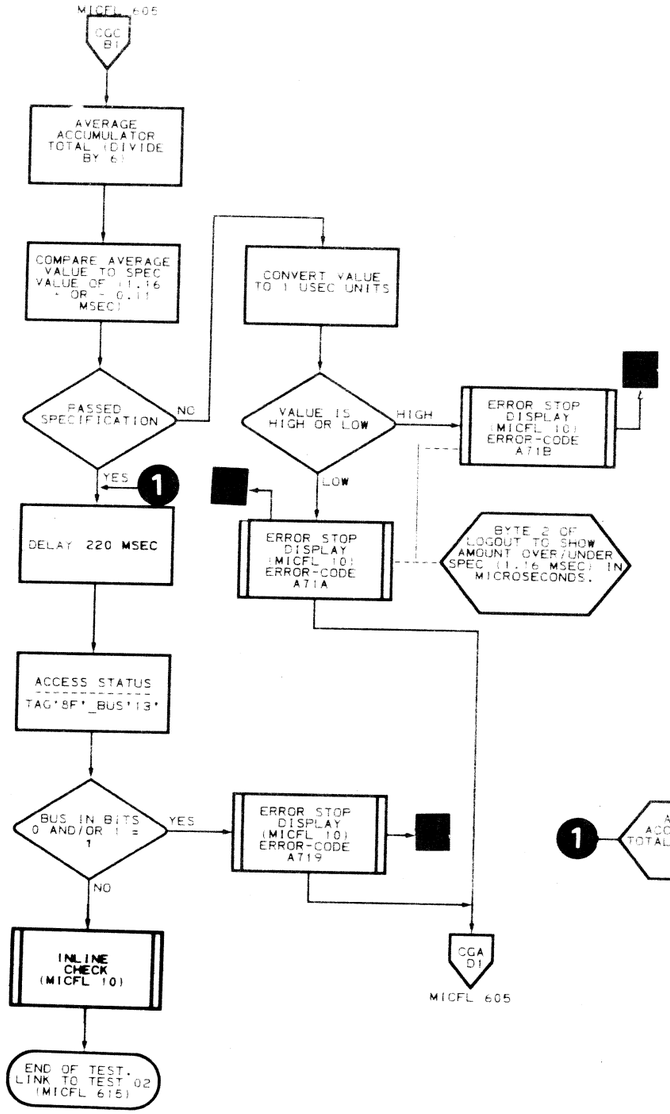
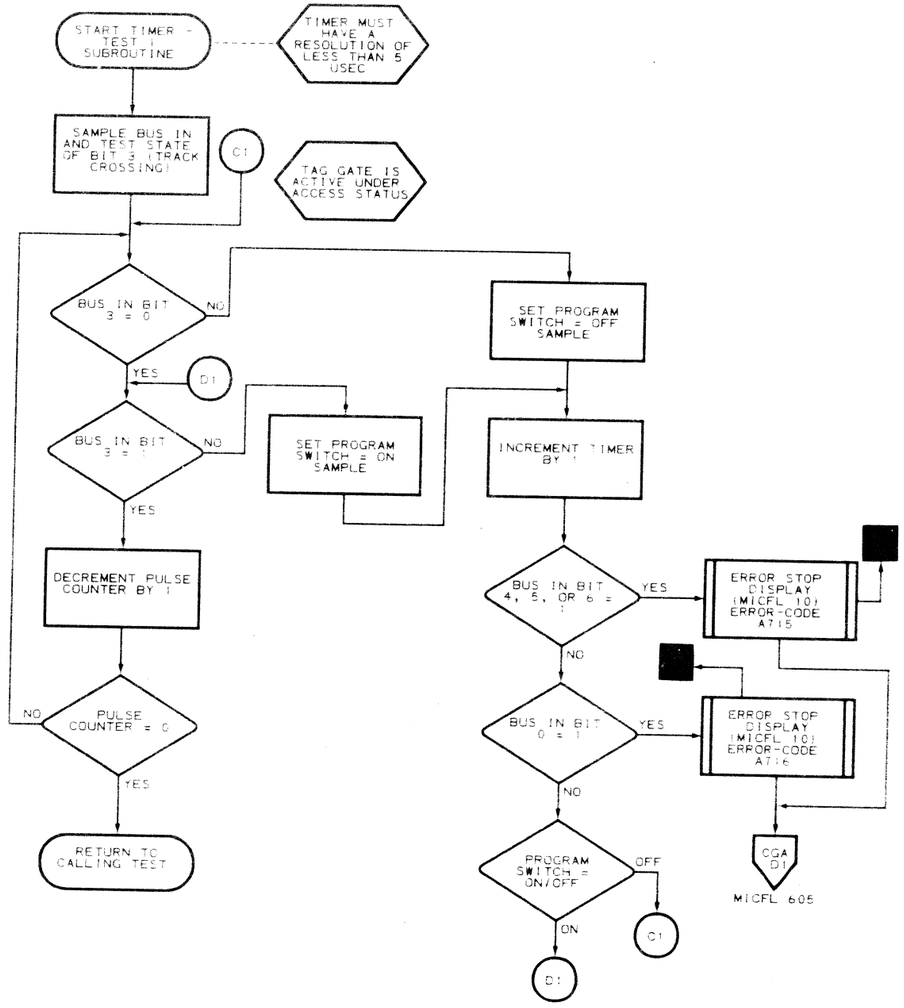
COARSE ADJUSTME. 7/TIMER SUBROUTINE (Routine A7)





MLM0006 440223
MICFL 610-L
CGC
JFL_12/05/74

MLM0006_440200
MICFL-610-R
CGD------
JFL_07/17/73

CE0605 Seq. 2 of 2	2747077 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74	440223 14 Mar 75		

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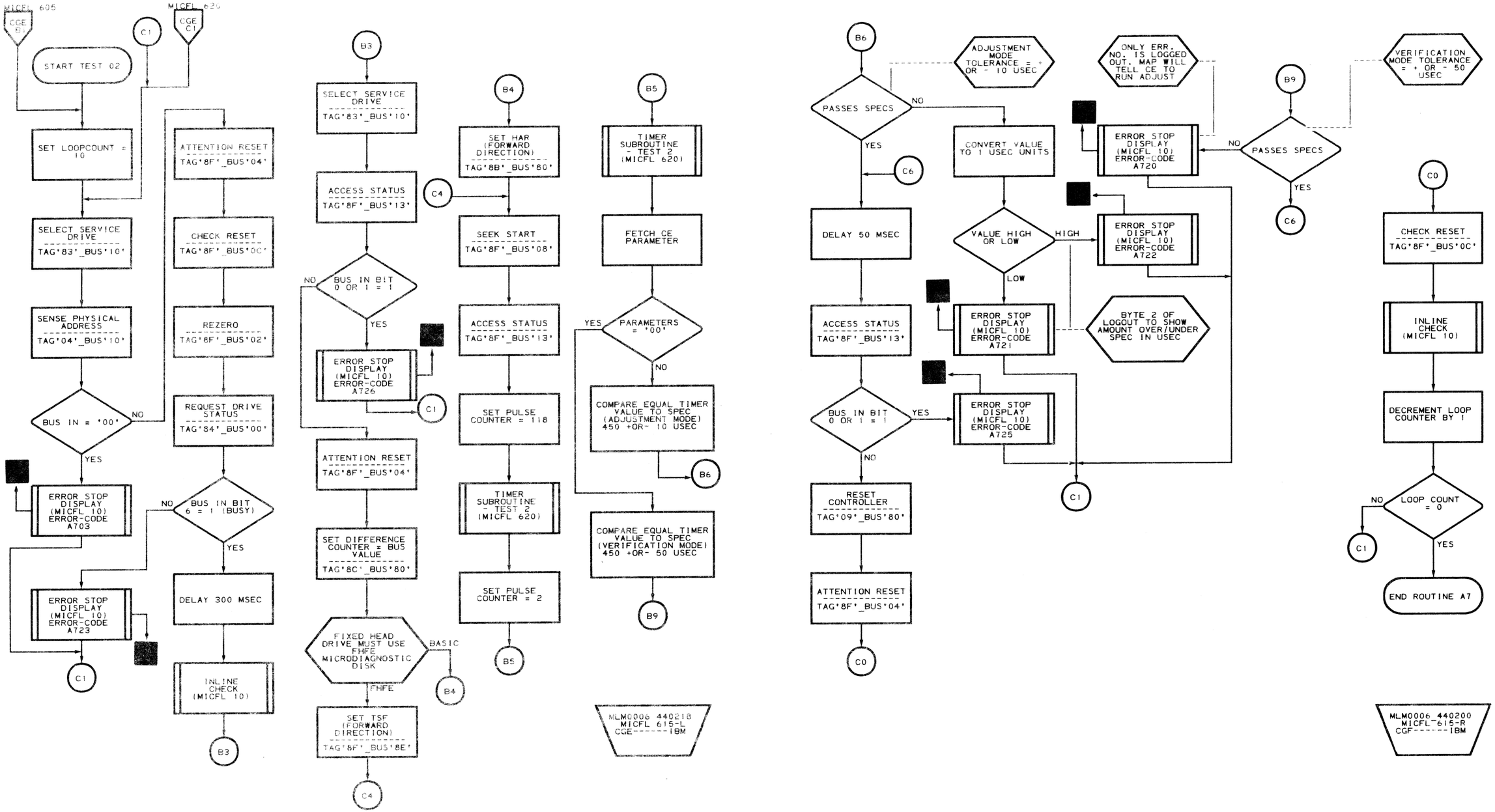
FINE ADJUSTMENT (Routine A7)



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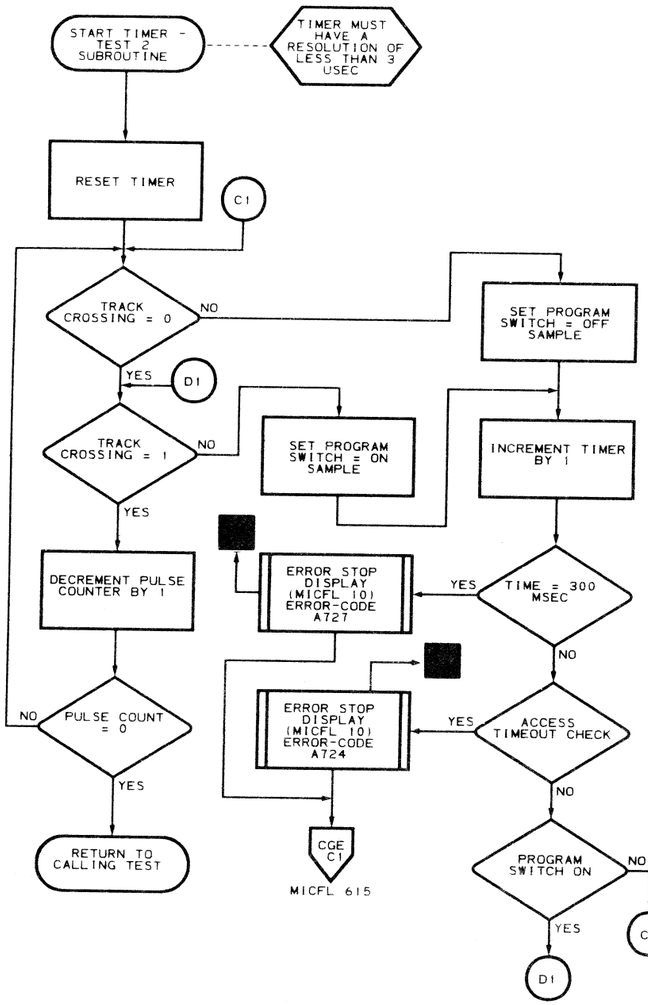
TIMER SUBROUTINE TEST (Routine A7)



MLM0006 440200
MICFL-620-L
CGG------IBM

ROUTINE A8 – DYNAMIC SERVO TESTS PART III

DESCRIPTION

The purpose of Routine A8 is to verify the correct operation of the servo during a Seek operation.

Test 01. Access Mode Selection

Test 01 verifies that carriage movement can be initiated by a Seek Start command as follows:

1. Rezero the access.
2. Issue a Seek Start command and wait 10 milliseconds for the track crossing bit in access status to change states.

Test 02. Difference Counter Verification (Basic)

Test 02 verifies that the Difference Counter decrements with each track crossing pulse by issuing a Seek command for 128 tracks and monitoring the track crossing bit in access status. Each time a track is crossed, the Difference Counter is checked for the correct value.

Test 03. Access Mode Acceleration

Test 03 is issued to verify the operation of the digital to analog converter (DAC) ladder by measuring the accelerate response time for different seek lengths.

The accelerate response time is measured by timing the duration of access State A, which is then compared with known values to determine if they are correct.

Test 04. Target Track Capture

Test 04 verifies that the servo captures on the target track by issuing a Seek command for 128 tracks. After a Seek Complete is received, the Home Address is read to verify the access position. If the Home Address is incorrect, the expected and received Home Addresses are logged out along with the approach velocity. Approach velocity is the time required for the Difference Counter to go from 0 to 1.

Test 05. Difference Counter Verification (Advanced)

Test 05 is the same as Test 02 except that a range of seek lengths are used (1, 2, 4, 8, 16, 32, 64, 128, 256 tracks).

If any forward seek receives a Drive Check and the Difference Counter is correct, a Rezero is issued and the next seek length is executed. If the Drive Check is received on the reverse seek, the same procedure is used. If the failure occurred on the last seek, a Rezero is issued and the test is ended normally.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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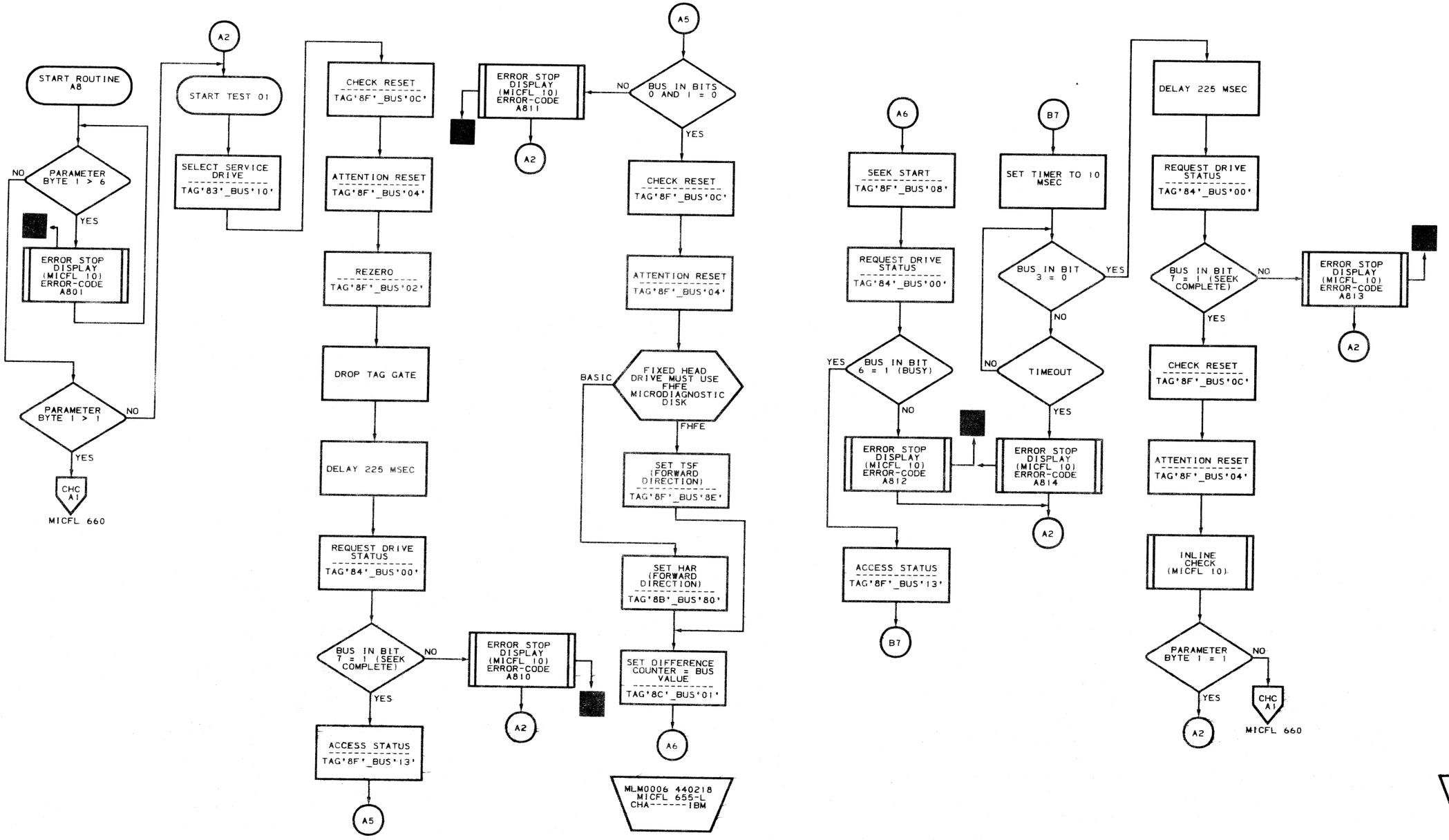
ACCESS MODE SELECTION (Routine A8)



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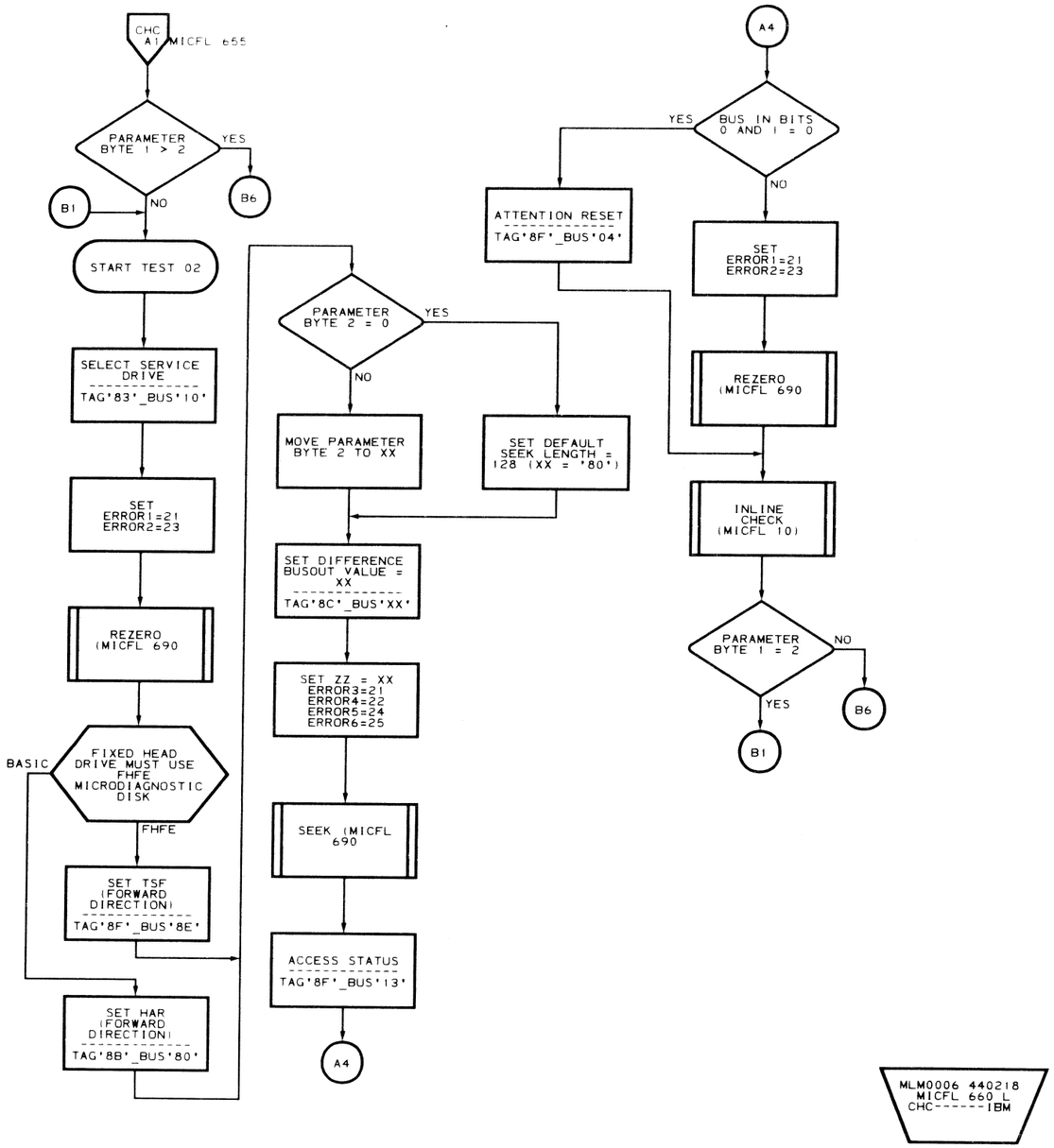
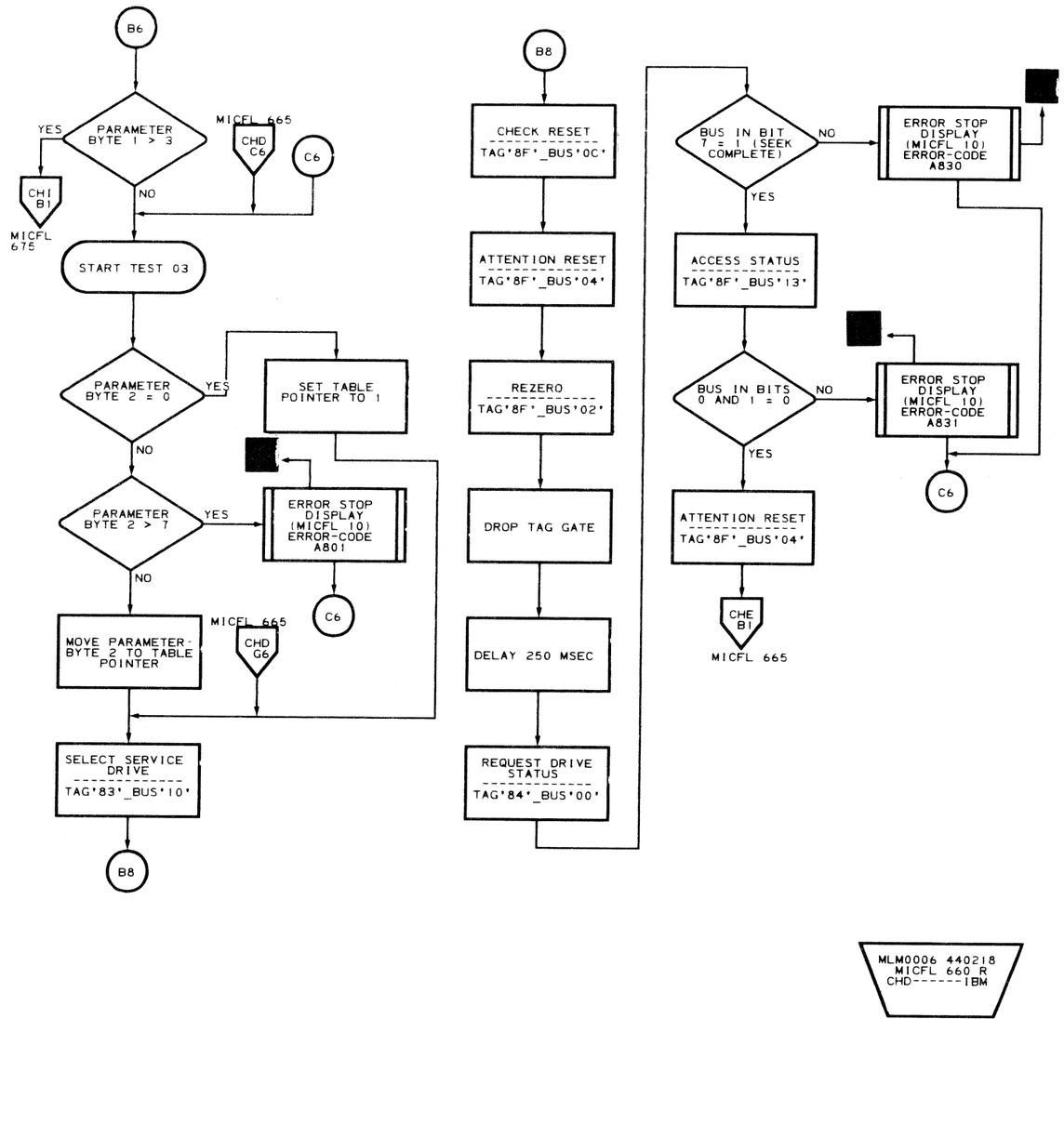
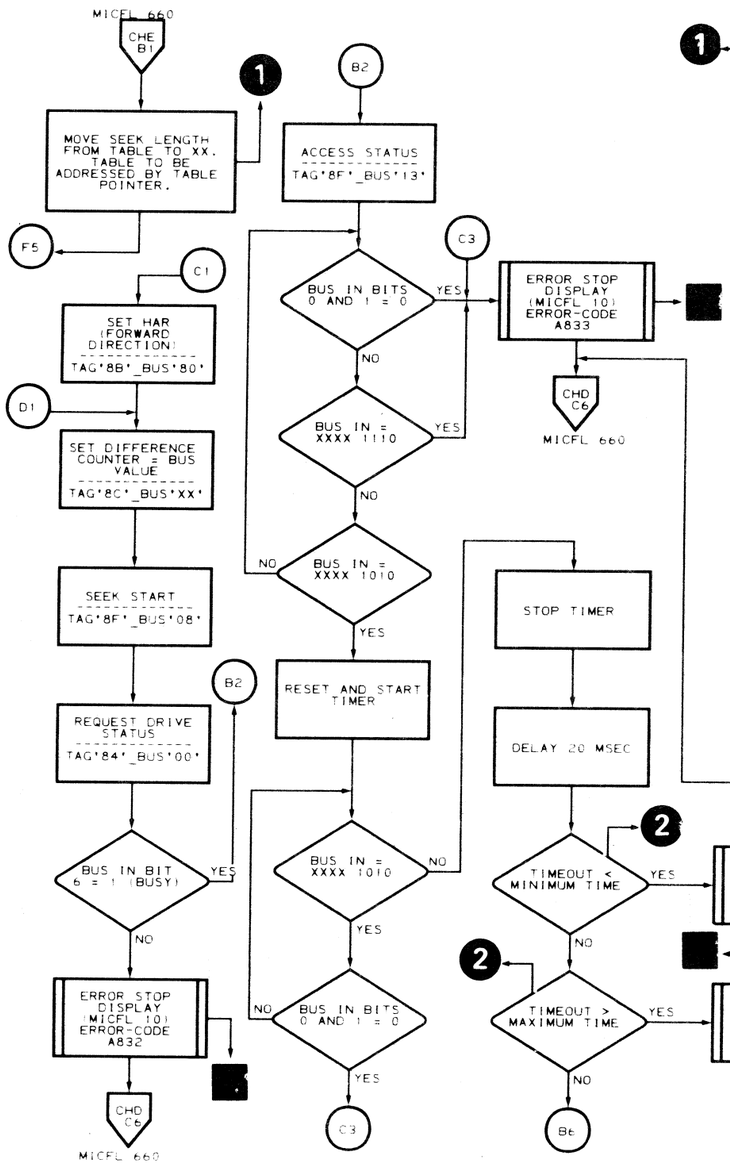
DIFFERENCE COUNTER VERIFICATION/ACCESS MODE ACCELERATION (Routine A8)





ACCESS MODE ACCELERATION (Routine A8)



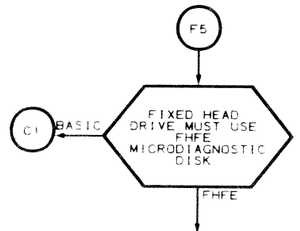
Note 1: If Table Pointer = 1, then Seek length = 128.

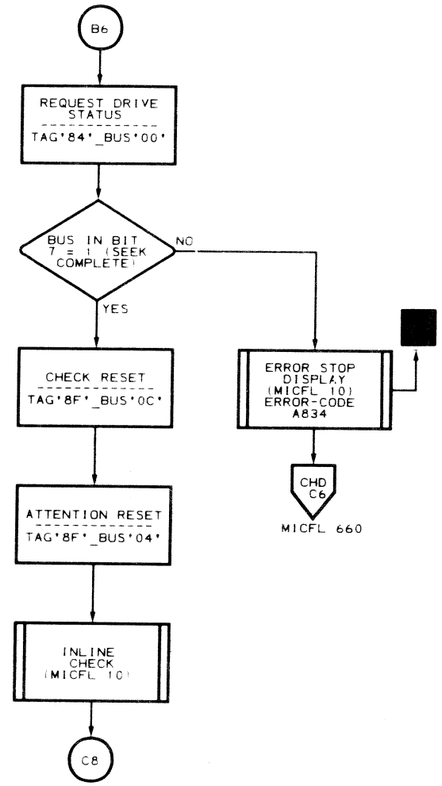
SEEK TIME TABLE

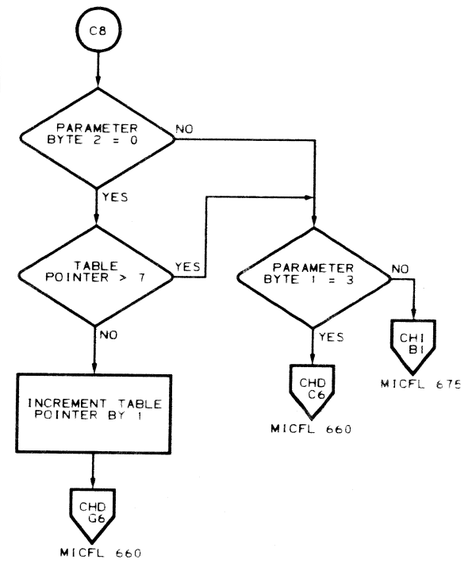
Table Pointer	Seek Lng	Minimum Time	Maximum Time
1	128	6.92 ms	12.8 ms
2	32	3.78 ms	5.42 ms
3	16	2.49 ms	3.61 ms
4	8	1.72 ms	2.48 ms
5	4	1.24 ms	1.753 ms
6	2	740 ms	1.10 ms
7	1	460 us	700 µs

Minimum and maximum times are selected by the table pointer value.

If table pointer = 2,
Minimum time = 3.78 ms
Maximum time = 5.42 ms







MLM0006_440202
MICFL_665_R
CHF
JFL_10/10/73

CE0660	2747081	440200	440202	440203	440214	440218		
Seq. 2 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74		

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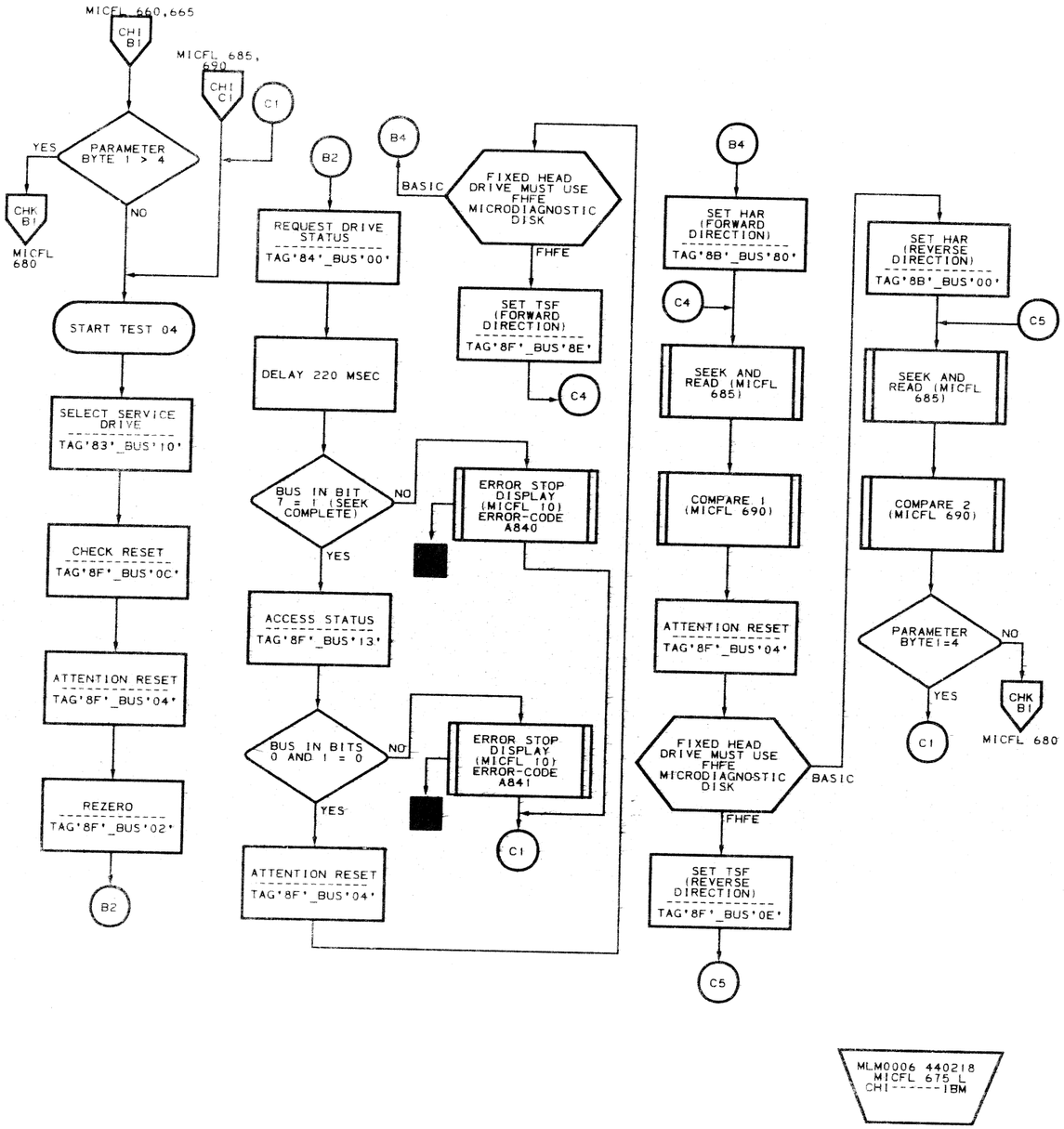
TARGET TRACK CAPTURE (Routine A8)



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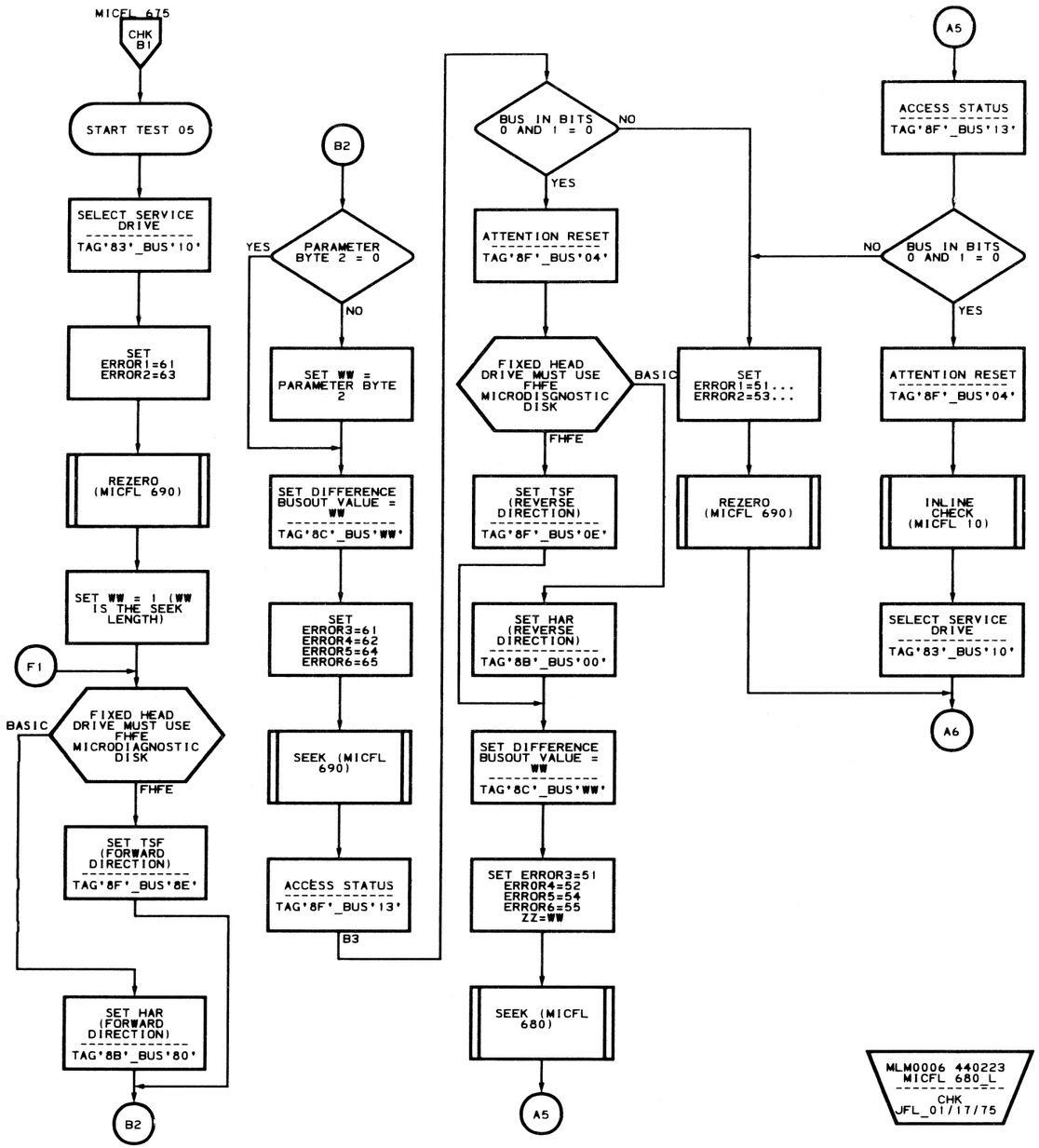
DIFFERENCE COUNTER VERIFICATION (Routine A8)



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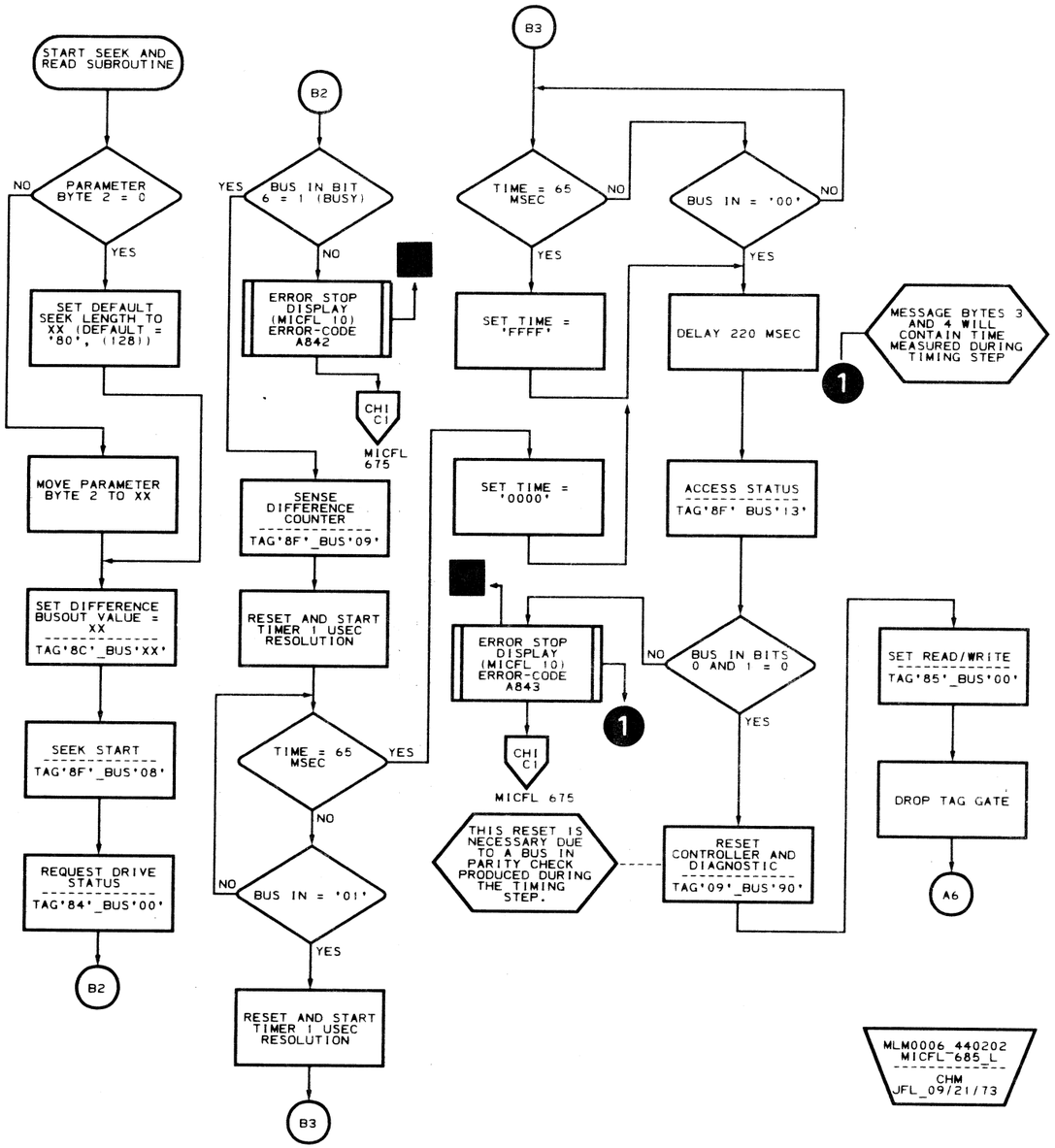
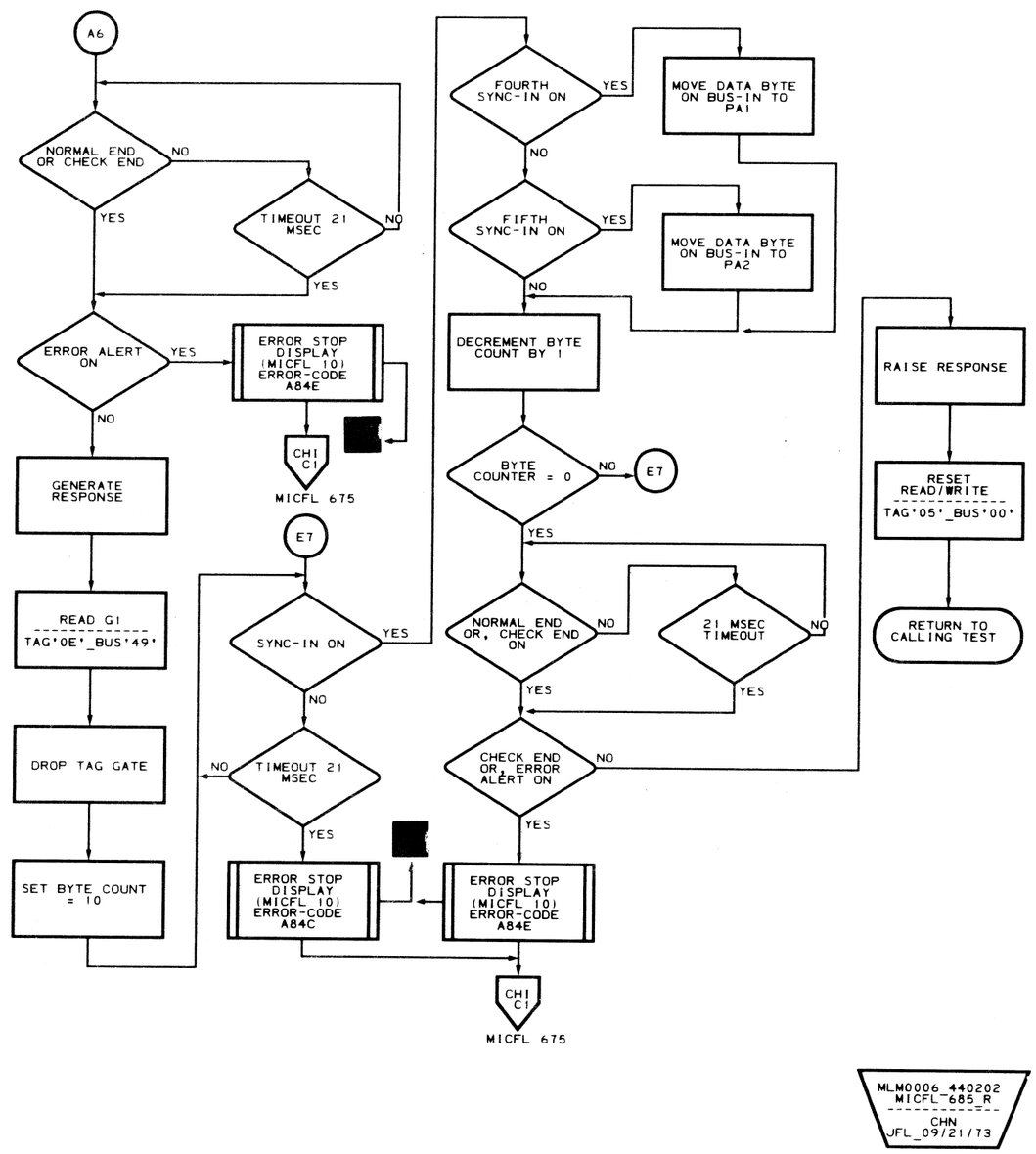
SEEK AND READ SUBROUTINE (Routine A8)





CE0680	2747083	440200	440202	440203	440218	440223		
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74	14 Mar 75		

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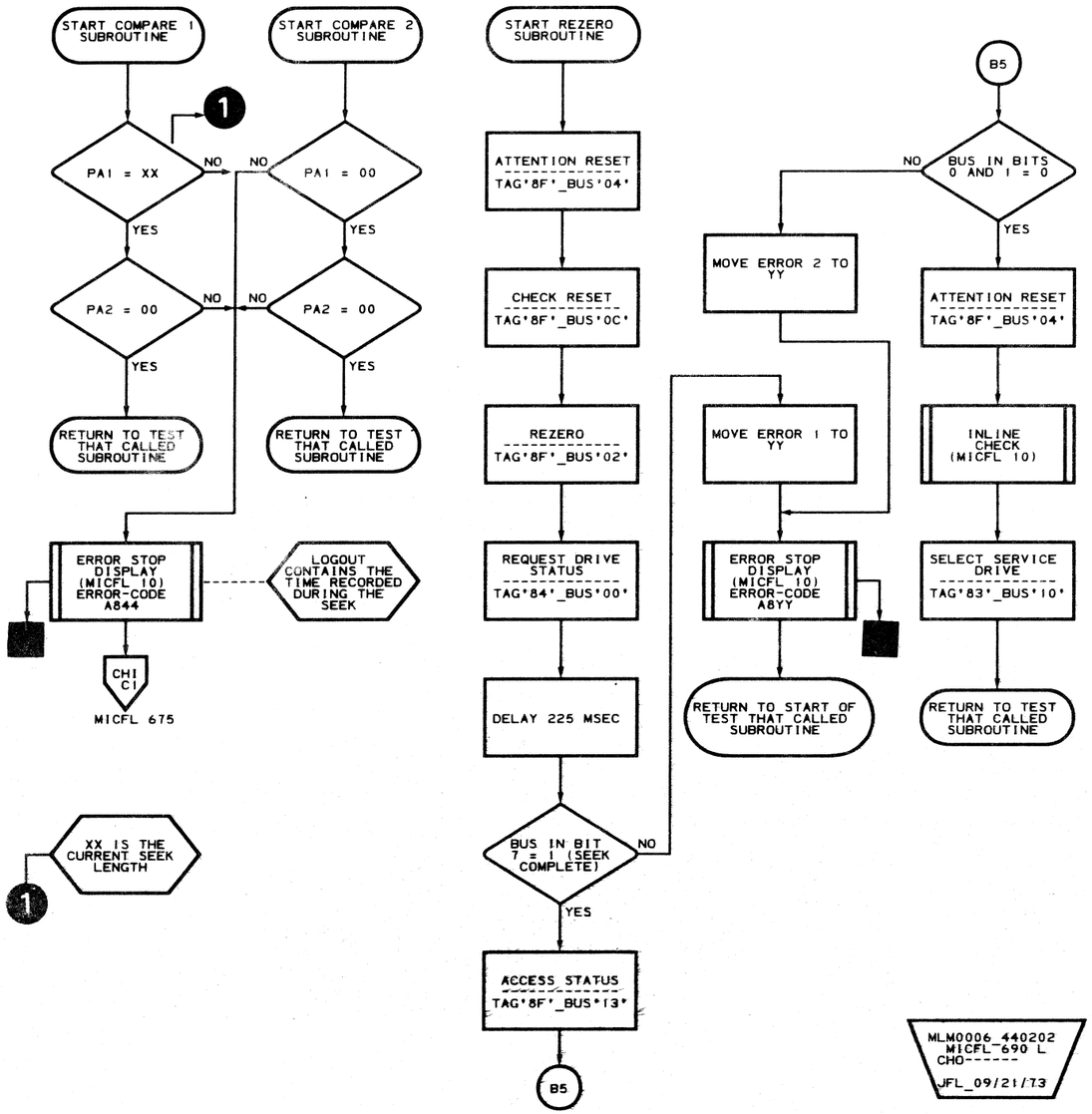
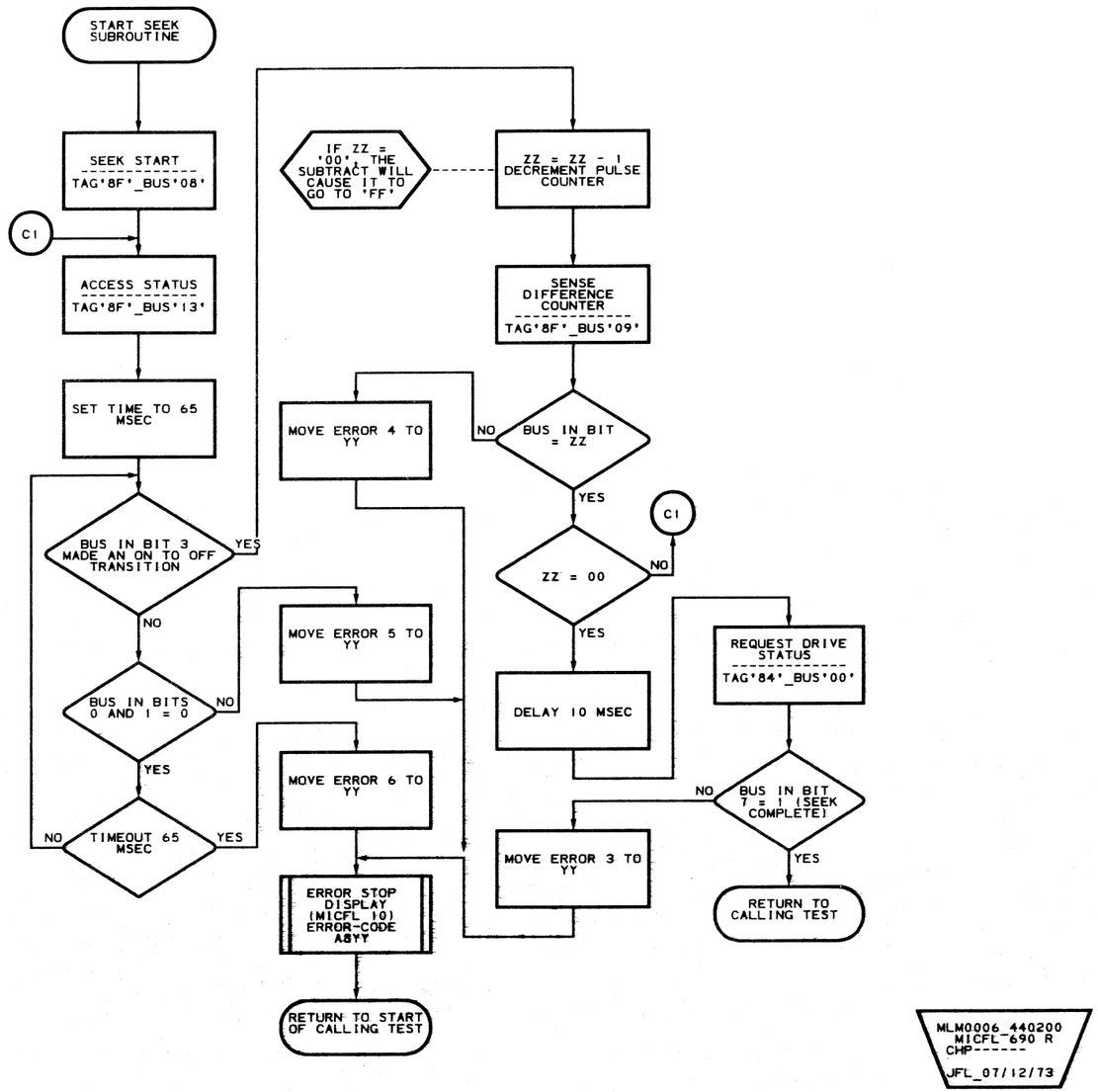
COMPARE 1 AND COMPARE 2 SUBROUTINES/START SEEK ROUTINE





CE0690 Seq. 1 of 1	2747084 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74			

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ROUTINE A9 – INCREMENTAL SEEK TEST

DESCRIPTION

Routine A9 is designed to allow the CE to enter any seek increment between '01' and 'FF'. Starting at cylinder 0, the access takes multiple seeks forward in increments of the number of cylinders specified. When the maximum allowable limit in this direction is reached, reverse seeks of the same increment take place until cylinder 0 is reached.

The operation is repeated until terminated, as described in MICRO 10.

If no seek increment is specified, the test defaults an increment of one cylinder. An increment of '00' is not allowed in this test.

Access arm position is verified by reading the Home Address. If an error occurs, the test performs a Rezero operation and continues.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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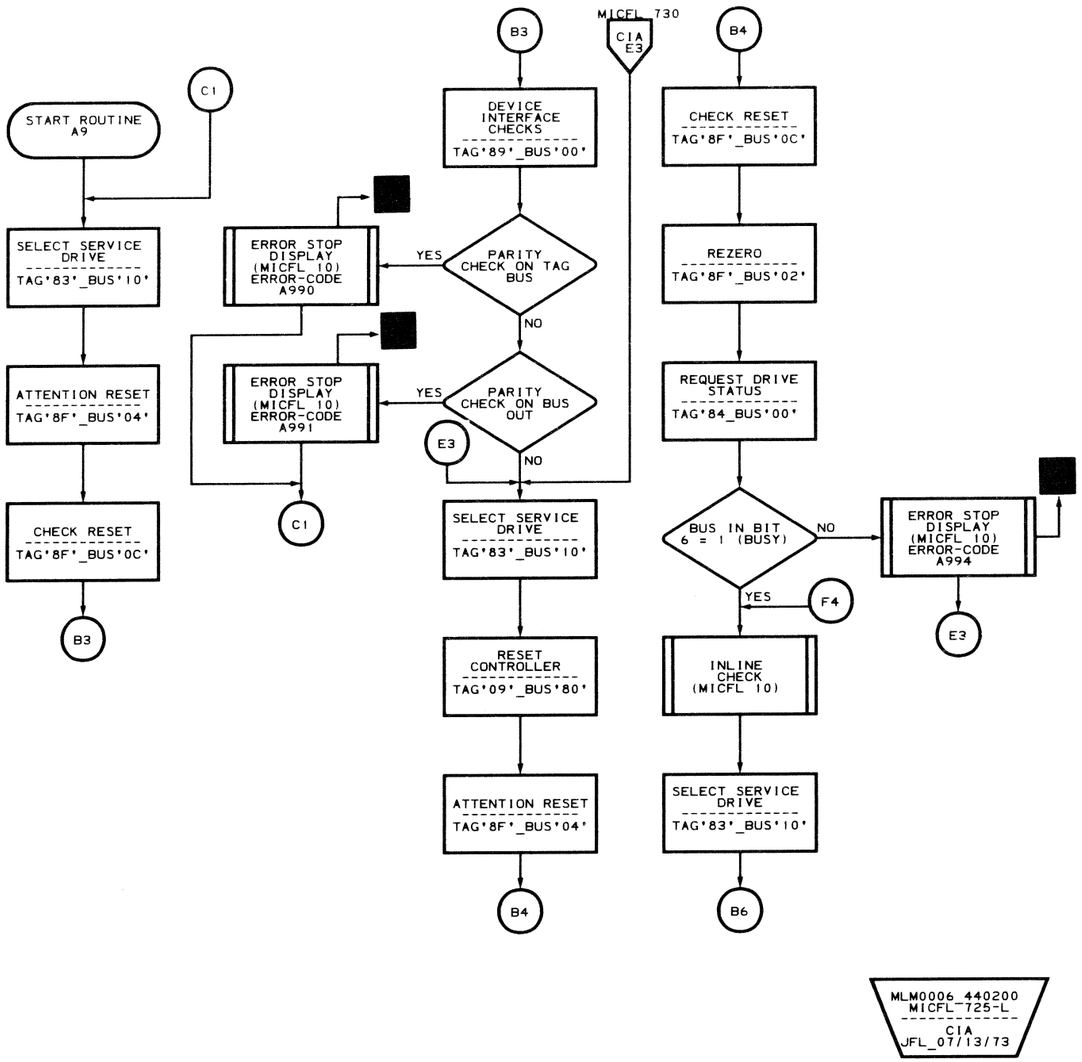
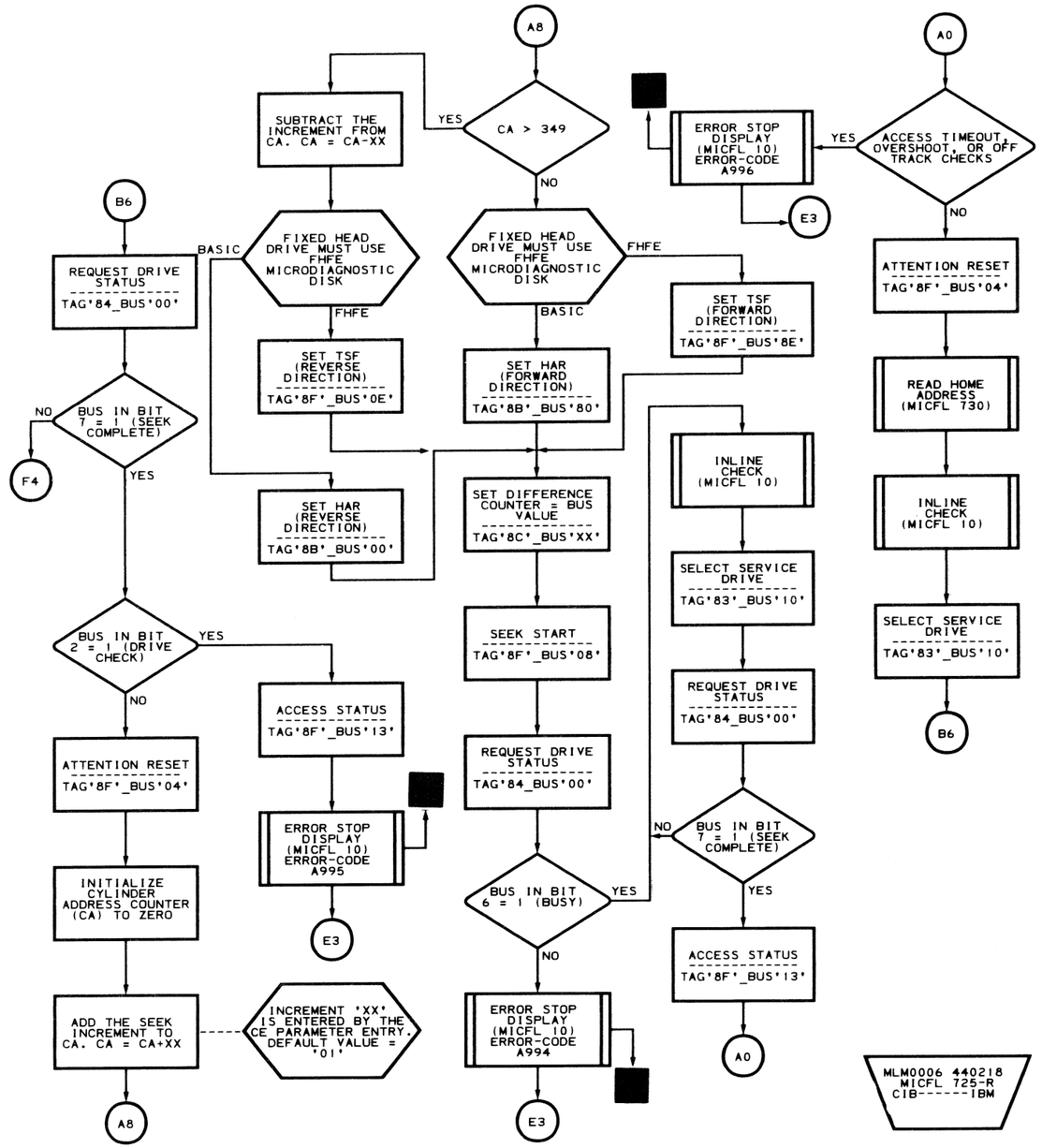
INCREMENTAL SEEK TEST (Routine A9)





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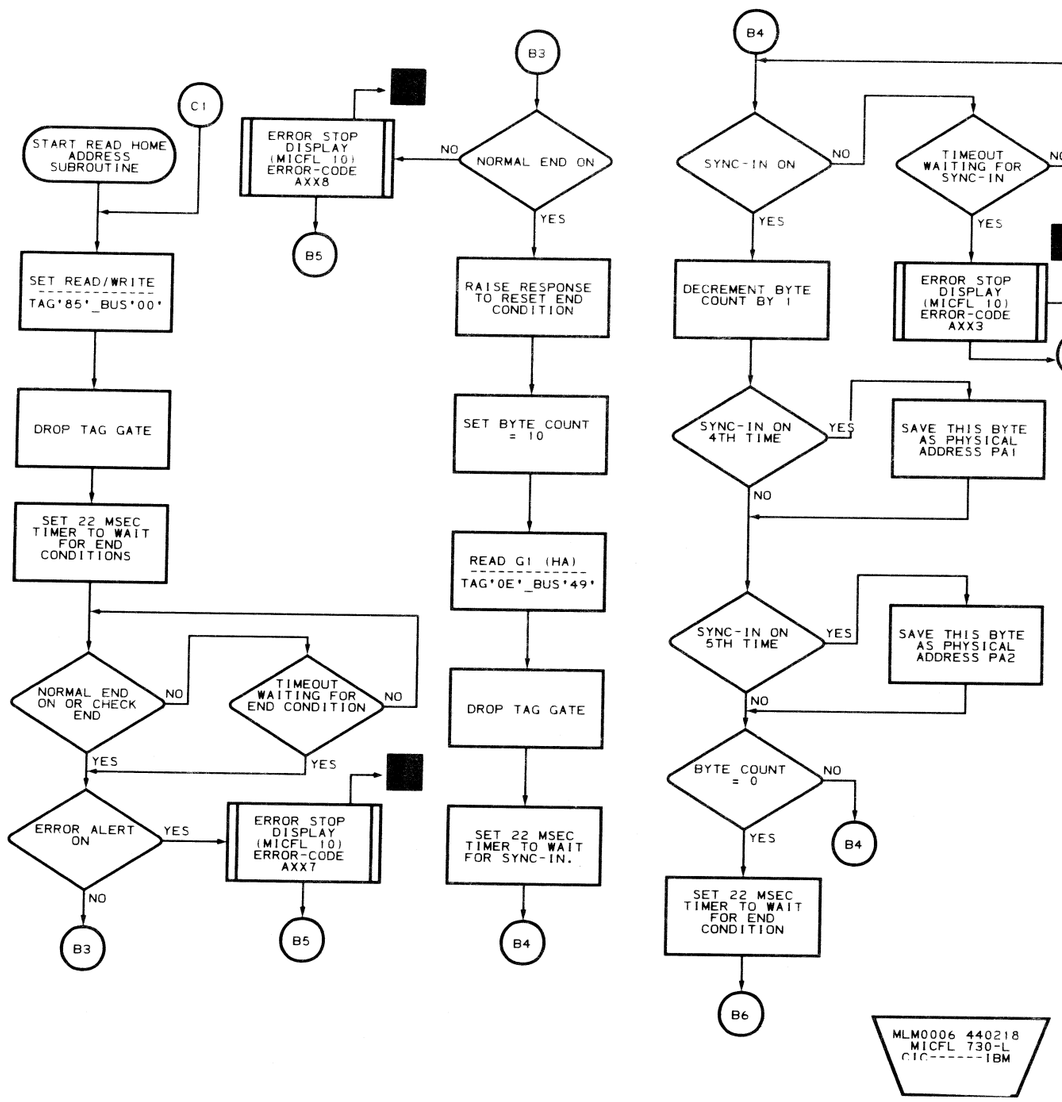
READ HOME ADDRESS SUBROUTINE (Routine A9)



MLM0006 440218
MICFL 730-L
CID------IBM

MLM0006 440200
MICFL-730-R
CID------IBM

CE0725	2747085	440200	440202	440203	440214	440218		
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74		

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ROUTINE AA – CYLINDER SEEK TEST

DESCRIPTION

Routine AA is designed to seek continuously between any two cylinders using any heads specified by the CE.

Any valid physical cylinder address between 0 and 349 (decimal) and any valid logical head for a specific data module can be entered by the CE. However, the head value selected in the From Cylinder and To Cylinder must be the same.

Refer to the chart at right for a description of possible head values for different data modules.

Routine AA acts as a no motion seek if the two cylinder addresses selected are identical.

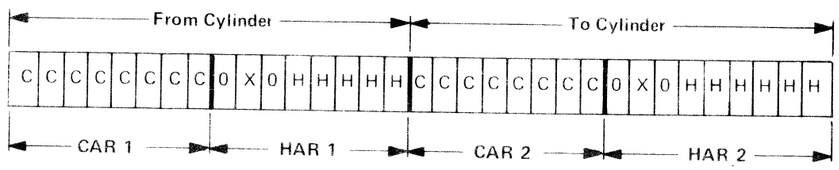
The access arm position is verified by reading Home Address. If an error occurs, the test rezeros and continues.

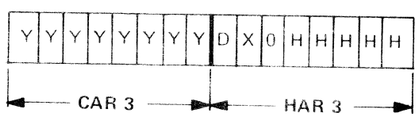
PREREQUISITES

Refer to micordiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.





Symbol	Description
C	Cylinde. Address (Physical)
X	'256' Bit
H	Head Value (Physical)
Y	Difference between From Cylinder and To Cylinder
D	Direction of Seek

Physical Head Value in Decimal	Logical Head Address for a Given Index	
	Index	
	Even	Odd
0	0	1
1	2	3
2	4	5
3	6	7
4	8	9
5	A	B
6	C	D
7	E	F
8	10	11
9	12	13
10	14	15
11	16	17

35 MB Data Module

70 MB Data Module

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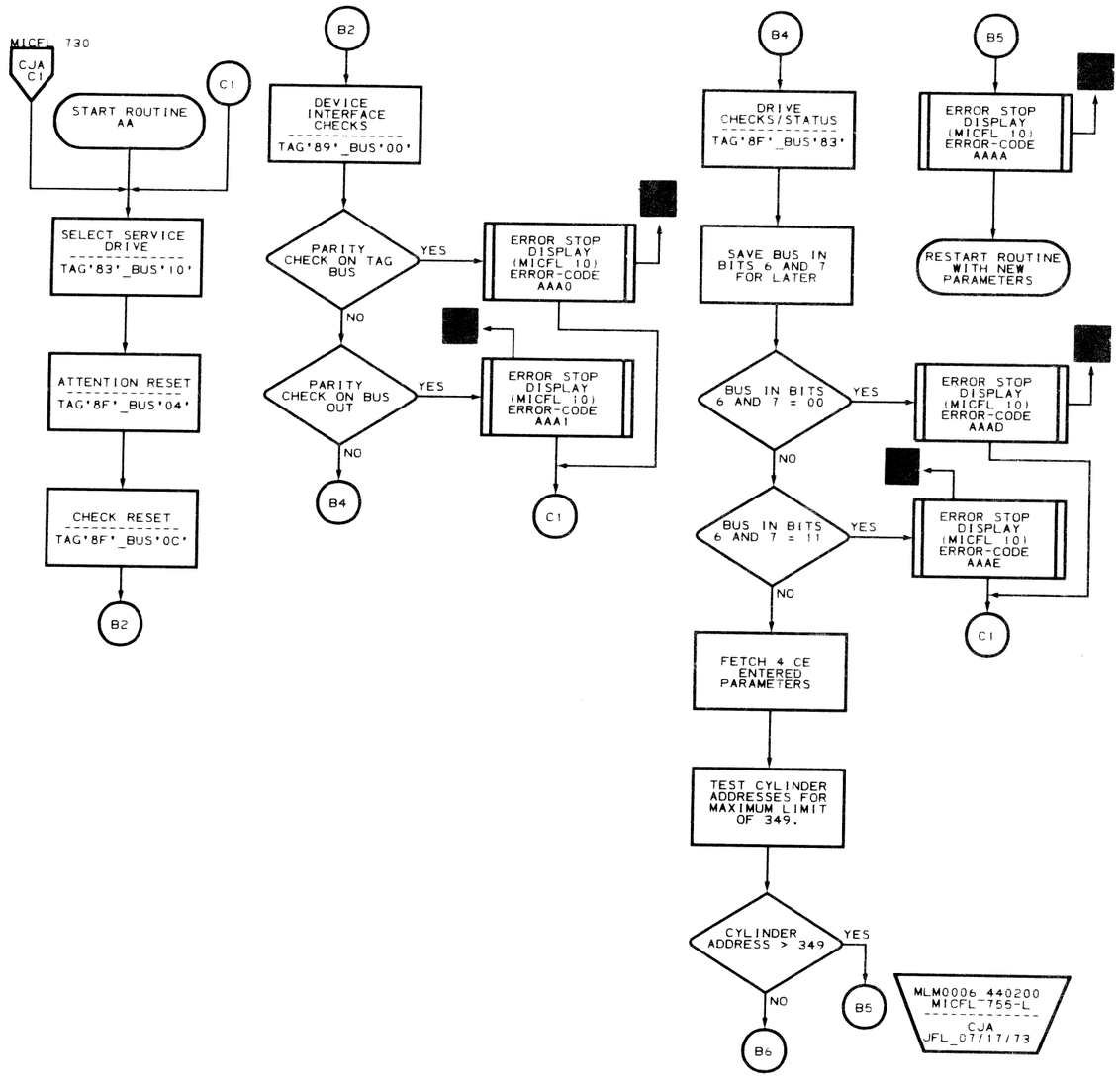
CYLINDER SEEK TEST (Routine AA)



CE0755	2747087	440200	440202	440203	440214	440218		
Seq. 1 of 1	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74		

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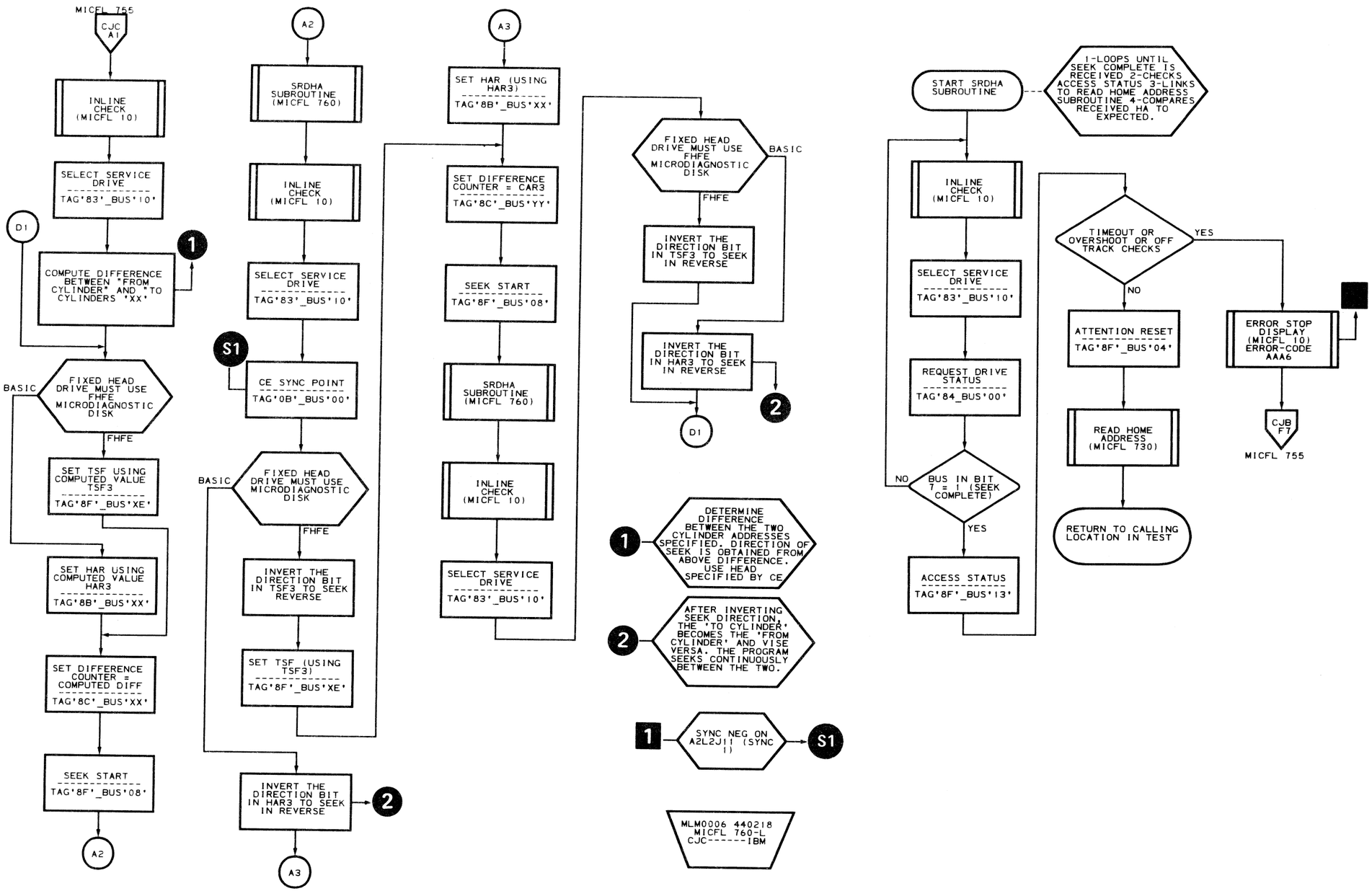
CYLINDER SEEK TEST (Routine AA)



CE0760 Seq.1 of 2	2747088 Part No.( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74			

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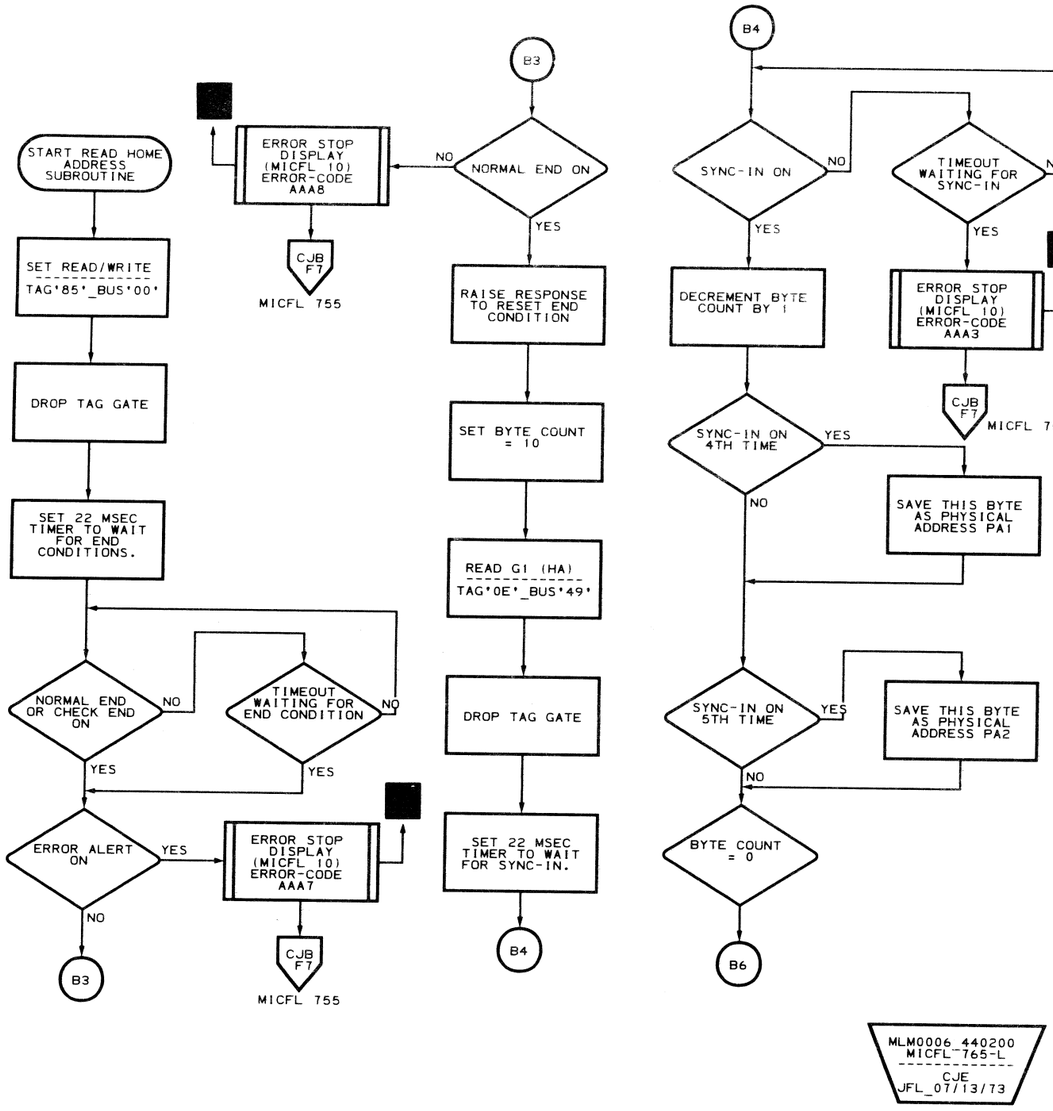
READ HOME ADDRESS SUBROUTINE (Routine AA)



MLM0006_440200
MICFL-765-L
CJE
JFL_07/13/73

MLM0006_440200
MICFL-765-R
CJF
JFL_07/13/73

CE0760	2747088
Seq.2 of 2	Part No.( )

440200	440202	440203	440218			
25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74			

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ROUTINE AB – RANDOM SEEK TEST

DESCRIPTION

Routine AB generates 1792 random seek addresses and seeks to each cylinder. Numerous forward and reverse seeks and no motion seeks are produced. The test automatically terminates after executing the last seek.

The access arm position is verified by reading Home Address using head 0 only. If an error occurs, the test is restarted from the beginning causing a Rezero operation.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

CE0790	2747511
Seq. 1 of 1	Part No. ( )

440200	440203
25 Jun 73	2 Nov 73

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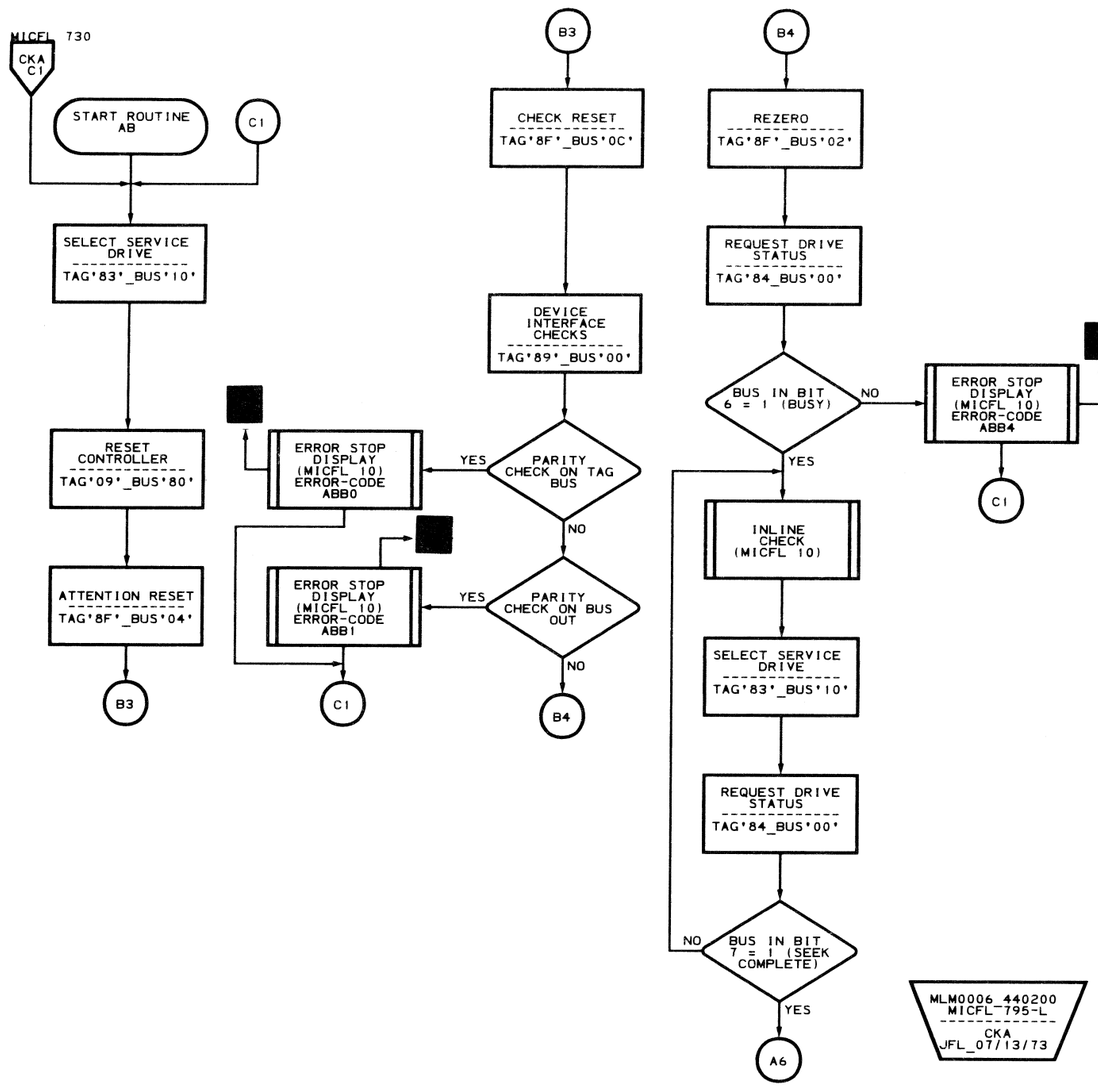
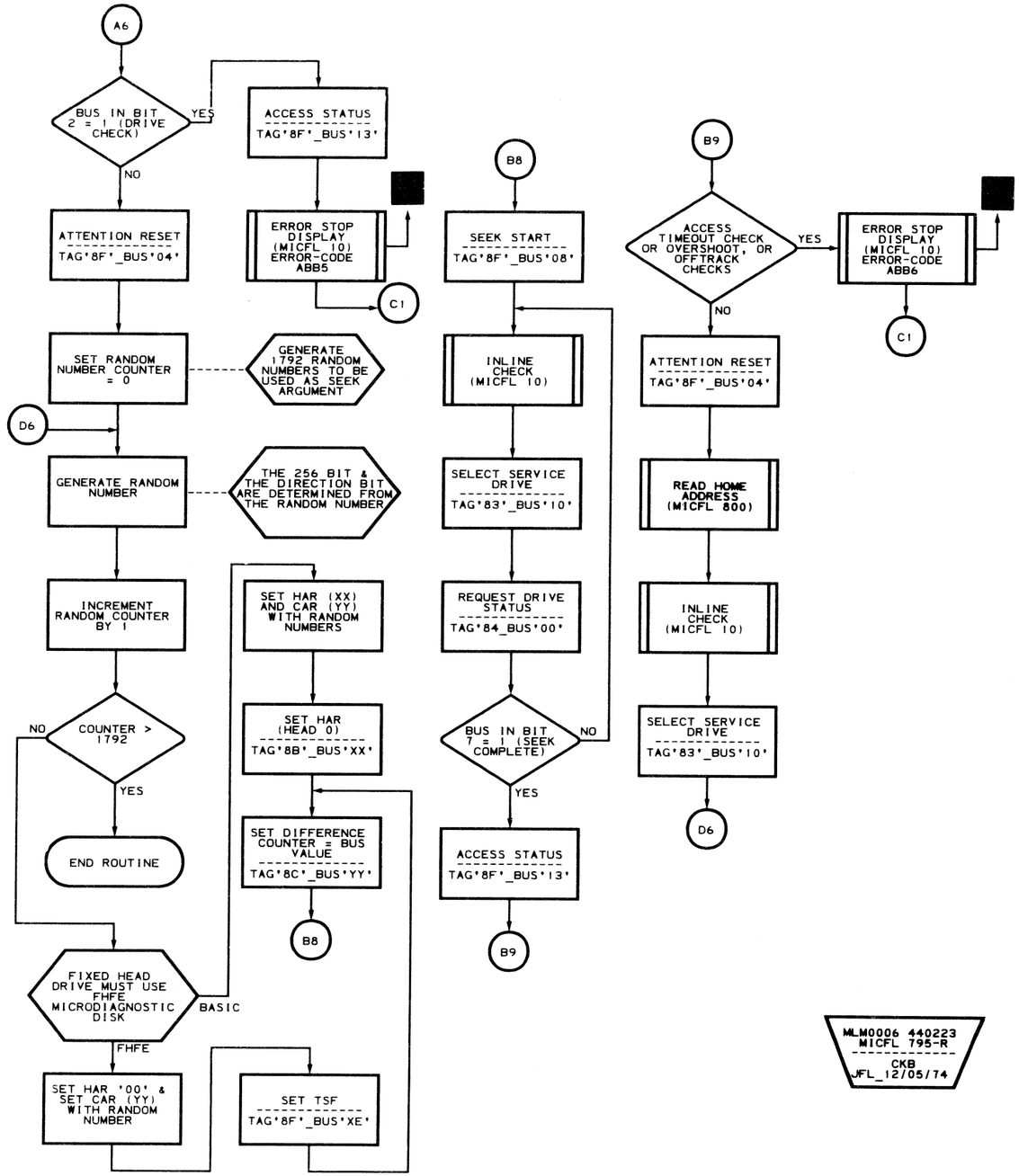
RANDOM SEEK TEST (Routine AB)





CE0795 Seq. 1 of 2	2747089 Part No.( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74	440223 14 Mar 75		

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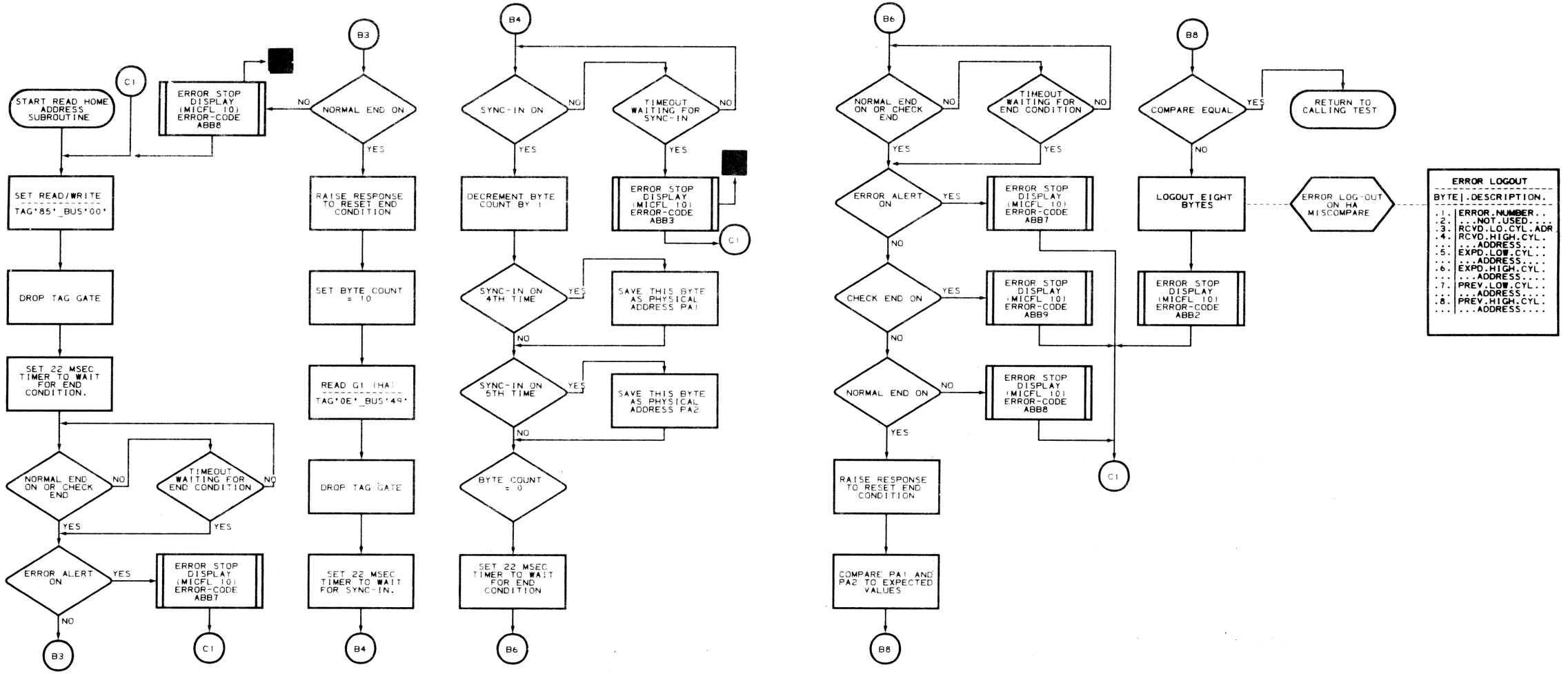

MLM0006_440200
MICFL_800-L
CKC
JFL_07/13/73

MLM0006 440223
MICFL_800-R
CKD
JFL_12/05/74

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ROUTINE AC – DATA MODULE STATE ANALYSIS

DESCRIPTION

Routine AC analyzes data module sequncer load/unload failures by examining certain bits in the error status bytes in a prescribed sequence. Unique error numbers are produced, based upon the values contained within these bytes. Refer to the routine flowchart for detailed sequence of analysis of specific bytes/bits.

Drive Checks Status	(Tag '8F' Bus '83')
DM Sequence Control	(Tag '8F' Bus '43')
Load Switch Status	(Tag '8F' Bus '23')
Access Status	(Tag '8F' Bus '13')

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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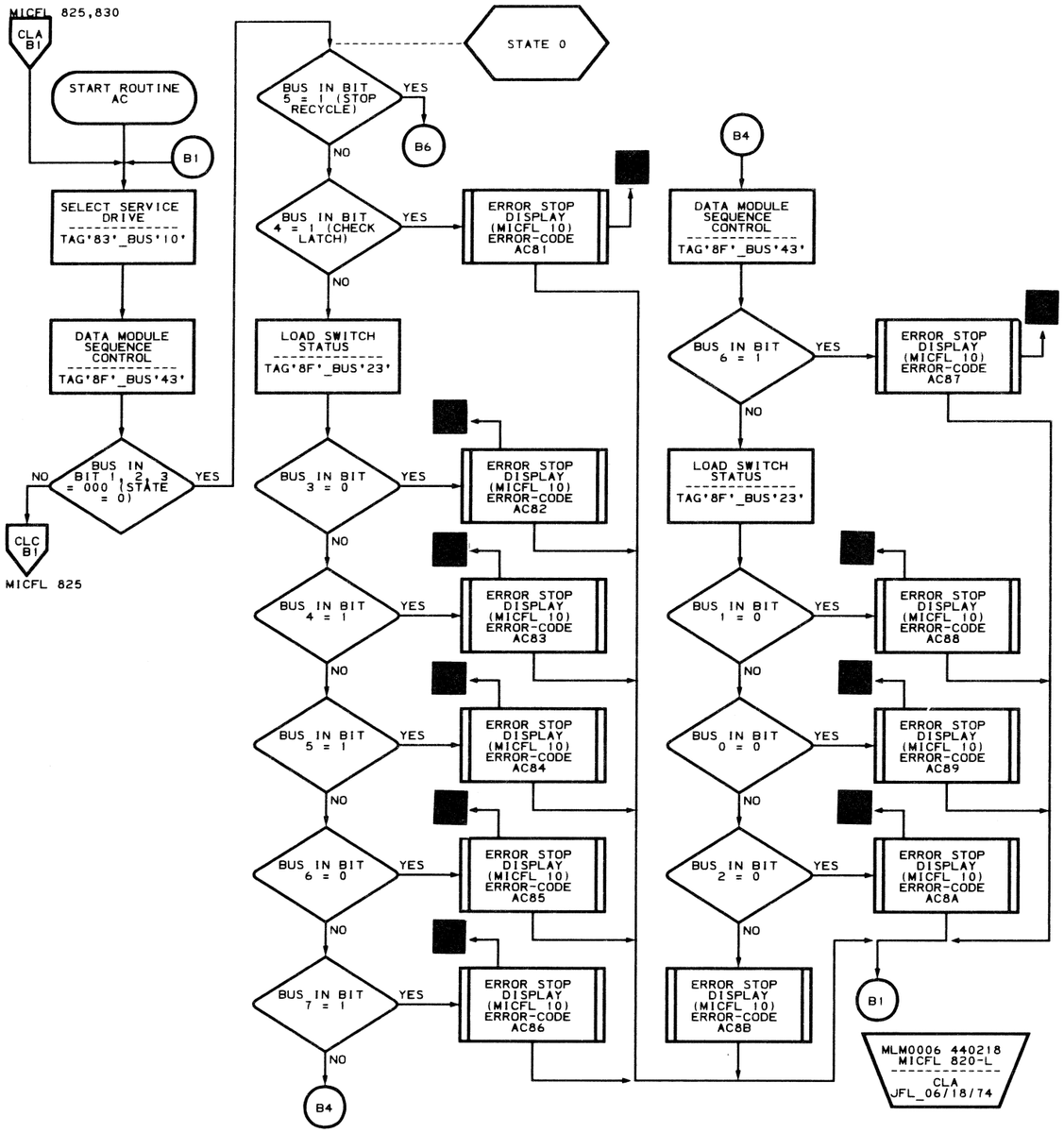

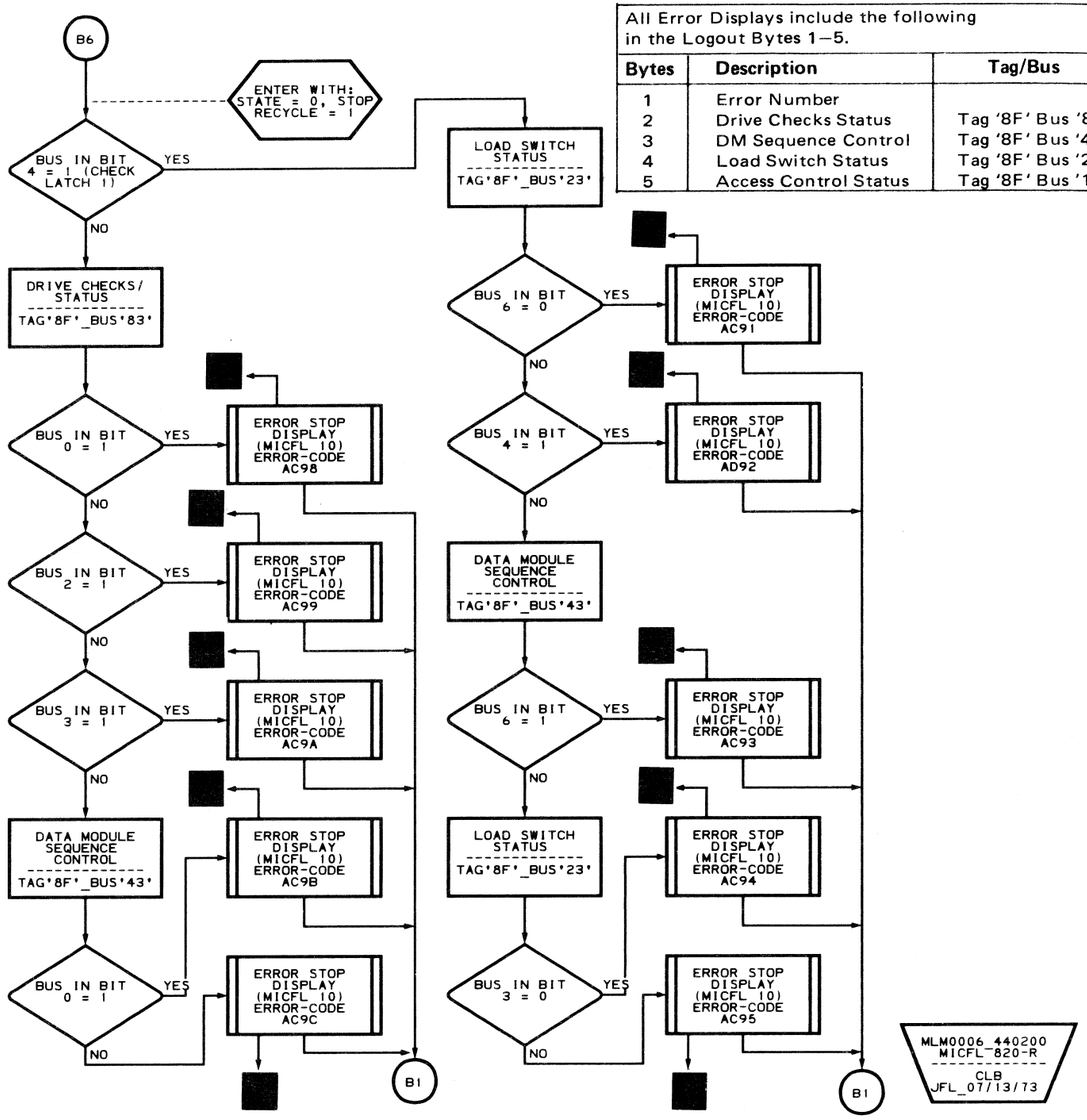

All Error Displays include the following in the Logout Bytes 1–5.

Bytes	Description	Tag/Bus
1	Error Number	
2	Drive Checks Status	Tag '8F' Bus '83'
3	DM Sequence Control	Tag '8F' Bus '43'
4	Load Switch Status	Tag '8F' Bus '23'
5	Access Control Status	Tag '8F' Bus '13'

CE0820	2747091
Seq. 1 of 2	Part No.( )

440200	440202	440203	440218			
25 June 73	7 Sept 73	2 Nov 73	5 Aug 74			

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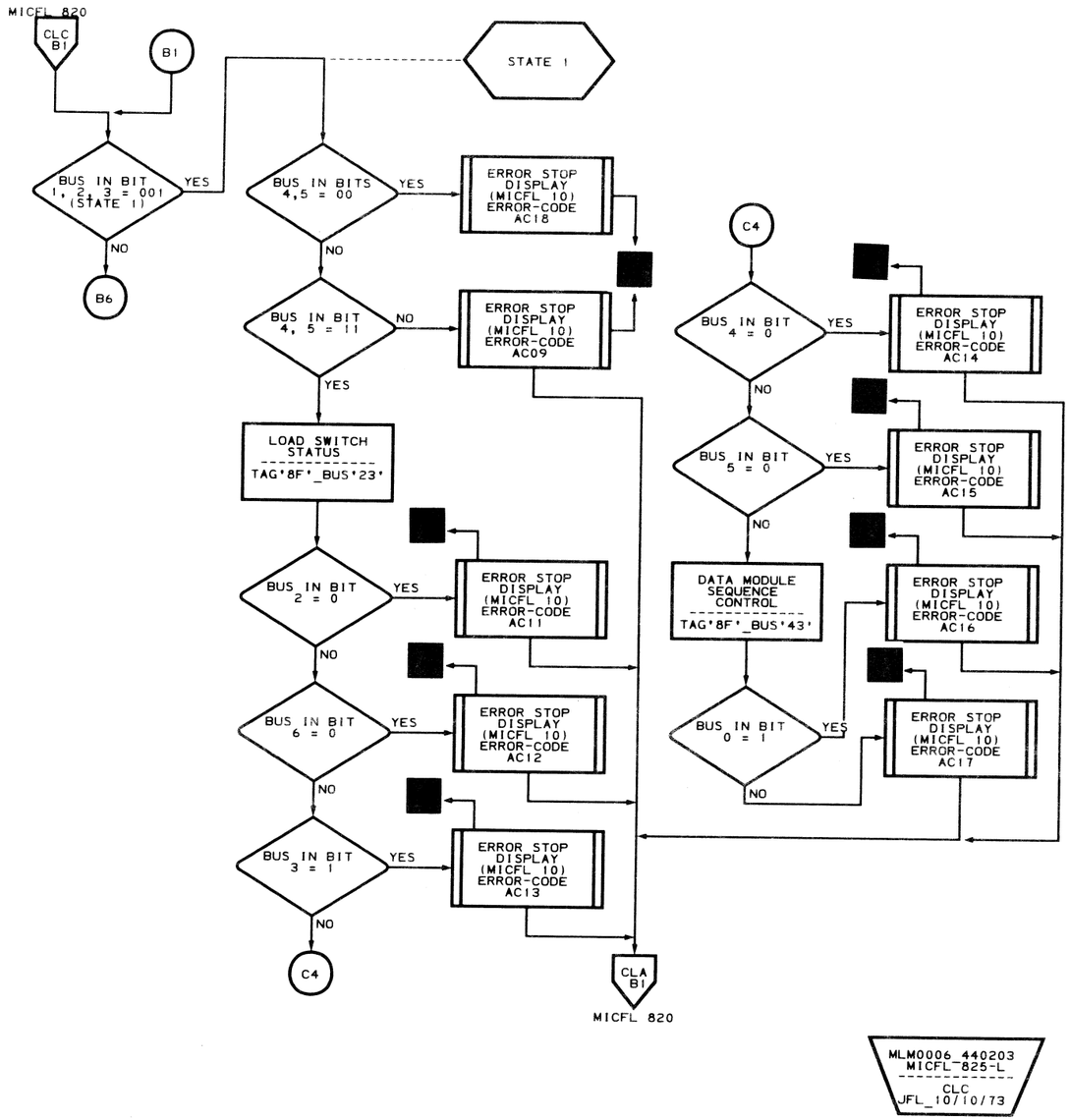

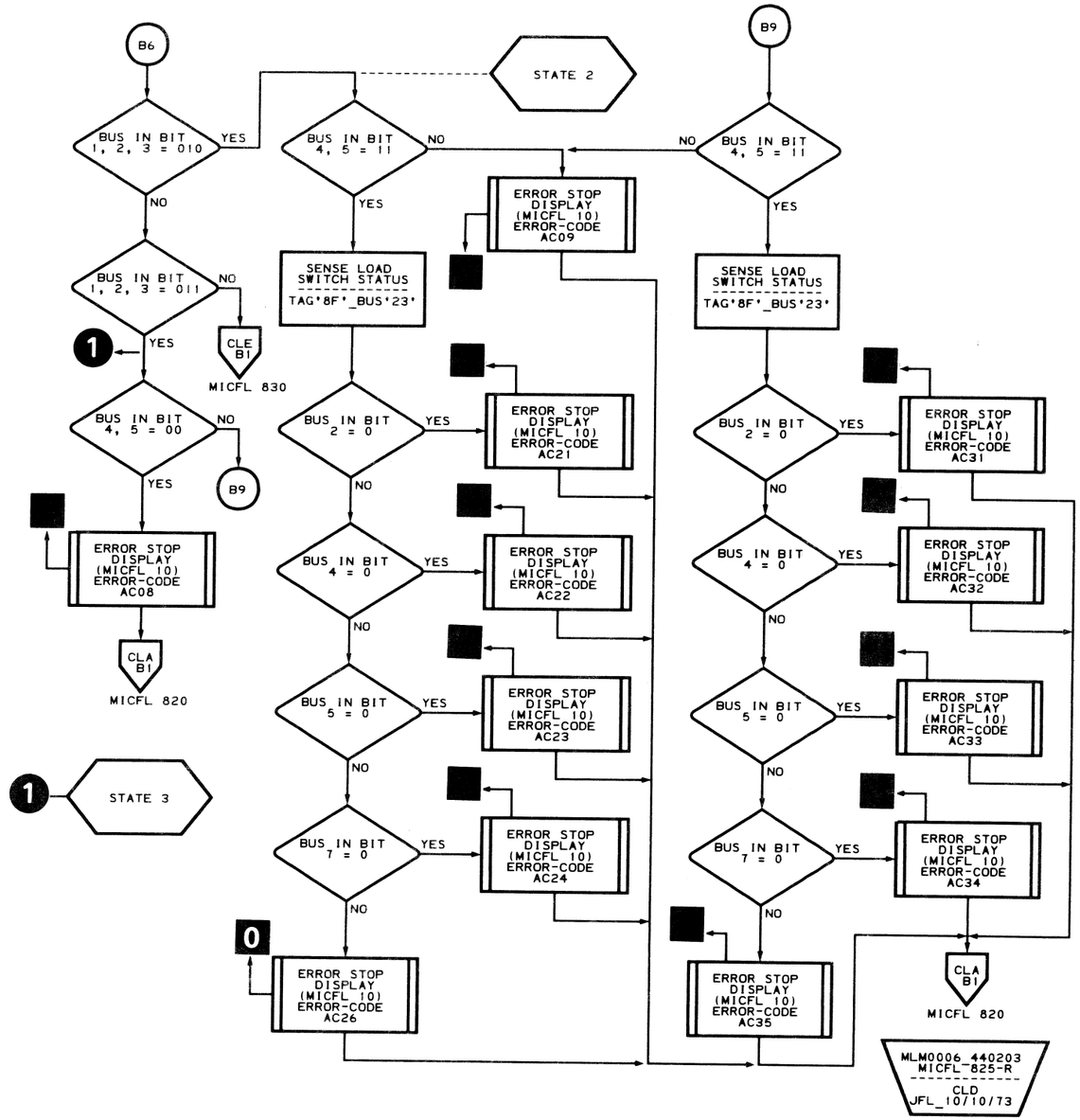

CE0820	2747091	440200	440202	440203	440218			
Seq. 2 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	5 Aug 74			

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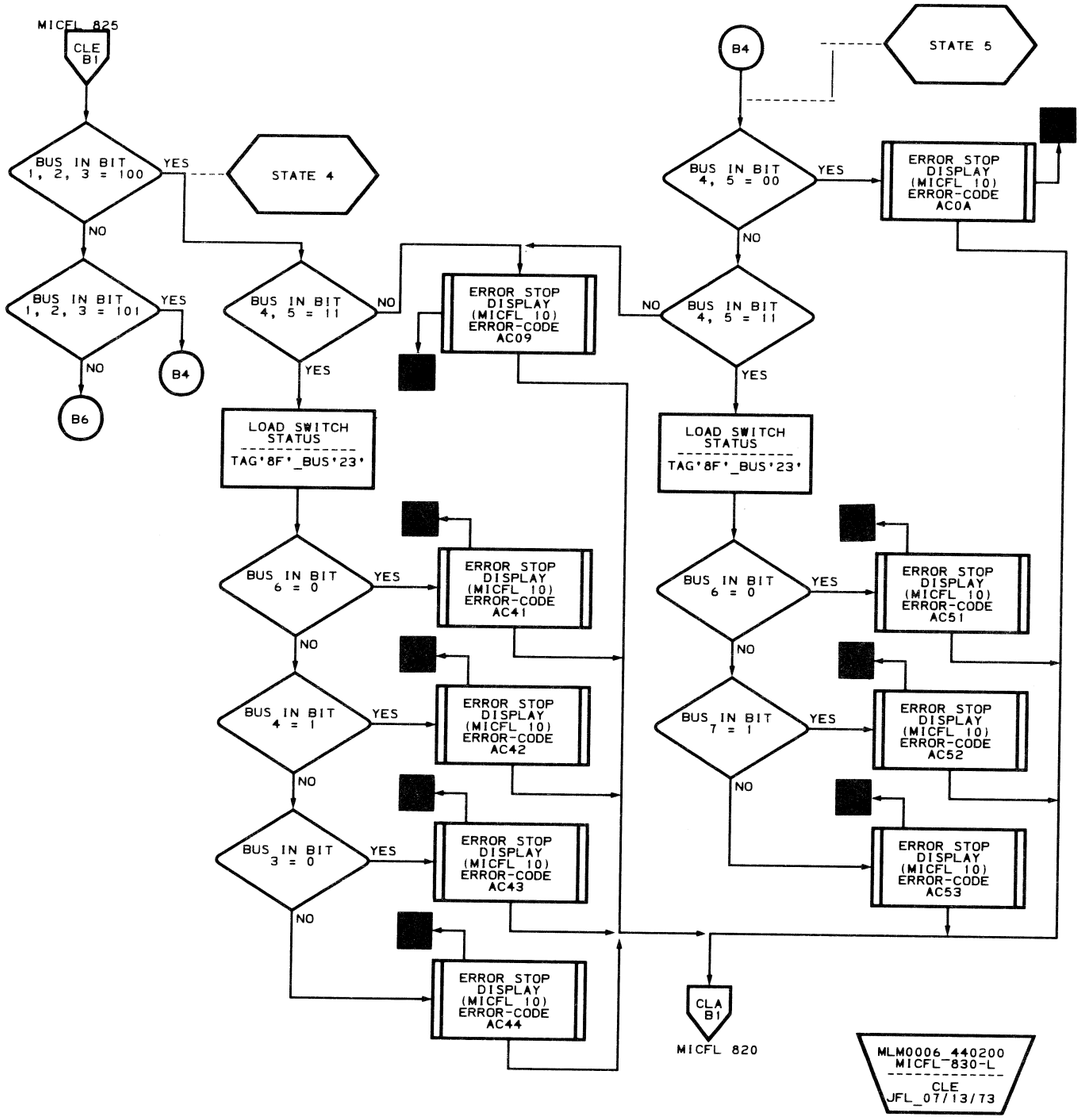

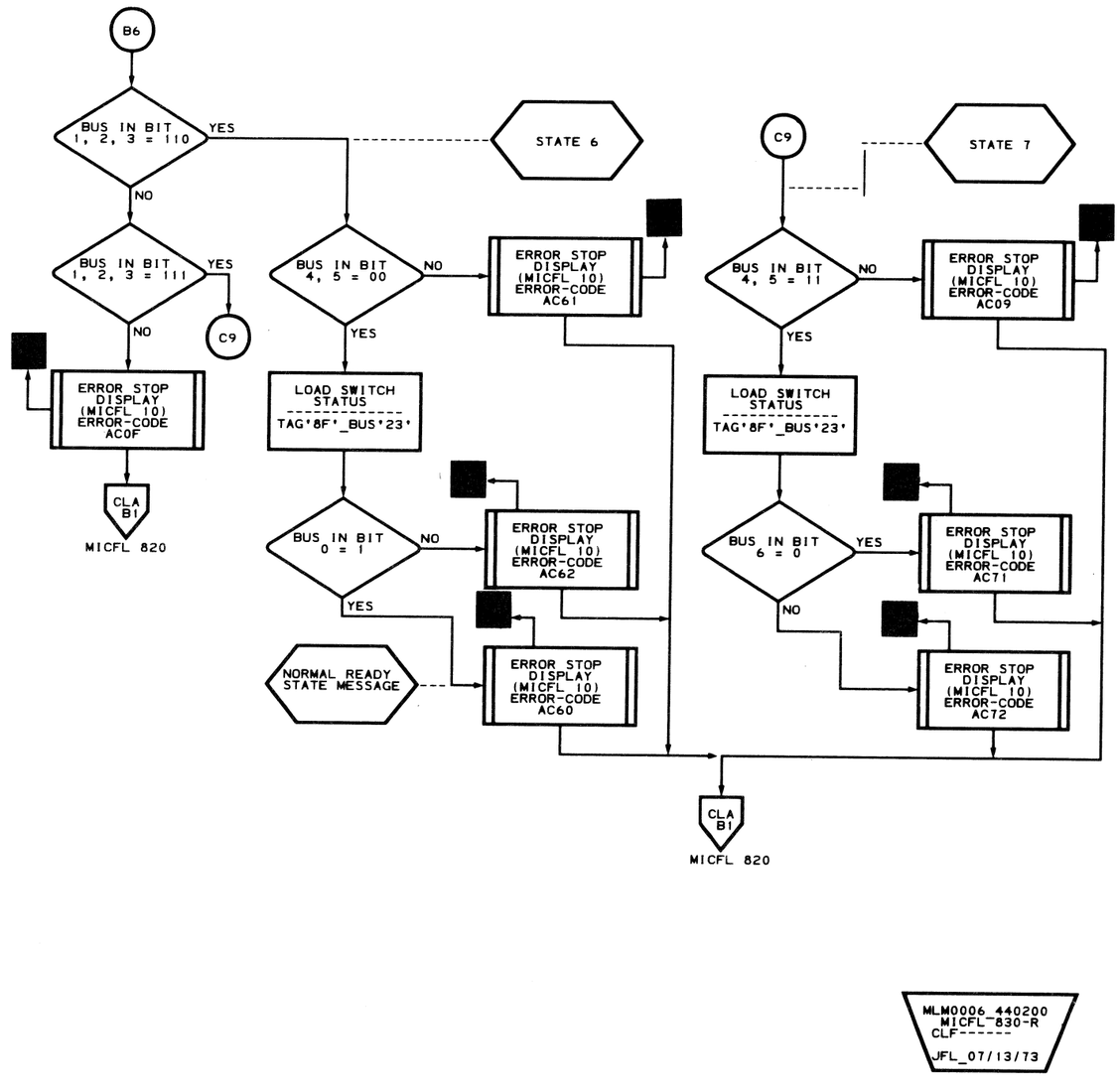

CE0825	2747092	440200	440202	440203	440214			
Seq. 1 of 1	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74			

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ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS

DESCRIPTION

Routine AD checks the Gap Counter and associated drive and controller circuitry. In normal operation (default parameter 1 = '00'), all tests are executed in sequence.

Optional parameter entry may be used to restrict operation to a single test. If a single test is selected, it loops indefinitely until halted by the CE or an error halt.

All tests are performed using physical cylinder 349, head 1.

Test ALL Initialization

Prior to the start of any/all tests, this step verifies that the CE parameter, if any, is valid.

Routine AD verifies that:

- The CE drive is online and Write Enabled.
- A Set Read/Write operation generates a Normal End response within 500 microseconds without an Error Alert 1.
- Index and Active Track are present within 21 milliseconds.

The routine then rezeros the access mechanism, checking for Busy to become active. The routine checks for normal completion of the operation within 300 milliseconds. After completion, drive status includes no Drive Check, not Busy, and Seek Complete.

The routine initiates a series of 349 1-cylinder seek operations and checks for no Error Alert and drive status following each Seek operation. After each operation, drive status includes: no Drive Check, not Busy, and Seek Complete.

Test 01. Data Transfer Checkers Check
Check Diag Inhibit Write Mode
Force Gap Ctr Parity Error
Force Write Data Check

Test 01 checks that Diagnostic Inhibit Write Gate Mode operates as follows:

1. Reads drive status
2. Looks for I Write Sense = 0 (Bit 5)
3. Orients on the Inactive Track Index
4. Initiates a Format G1 operation
5. Orients on the Active Track Index
6. Waits approximately 10 microseconds
7. Reads drive status
8. Checks for I Write Sense = 1 (Bit 5)

The preceding sequence is repeated with Diagnostic Inhibit Write Gate Mode = 1 and the test checked for I Write Sense = 0.

Test 01 looks for no Gap Counter error, initiates a Write G1 operation with Diagnostic Inhibit Write Gate and Diagnostic Invert Bus Out Parity modes active. It checks for Gap Counter error, Write Data Check and Controller Error status. The test initiates a Controller Reset operation and checks for no Gap Counter error. The test then issues a Check Reset operation to reset any errors in the drive.

Test 02. G1 Gap Tolerance

Test 02 measures the length of the G1 Gap by orienting on the Inactive Track Index, initiating a Write G1 operation, orienting on the Active Track Index, and measuring the time to the first Sync In. The measured time is checked for optimum value of 105 byte-times (118 microseconds). Tolerance is ±3.0%. Valid range = 114–121 microseconds.

Test 03. Extended G1 Gap Tolerance

Test 03 measures the length of an extended G1 Gap by orienting on Inactive Track Index, initiating a Write Extended G1 operation, orienting of the Active Track Index, and measuring the time to the first Sync In. The measured time is checked for an optimum value of 233 byte-times (262 microseconds). Tolerance is ±3.0%. Valid range = 253–269 microseconds.

Test 04. Modulo-16 Counter Function

Test 04 checks the operation of the four bit positions of the Modulo-16 Counter and the Recycle line by initiating a Write G1 operation with Diagnostic Inhibit Write Gate Mode active. Byte counts used for the Modulo-16 Counter test are 1, 2, 4, 8, and 17. The test counts the number of Sync Ins until receipt of an end condition. Any abnormal ending conditions resulting from this technique are ignored.

Test 05. G2 Gap Tolerance

Test 05 measures the length of a G2 Gap by orienting on the G1 (HA) field, initiating a Write G2 operation with Diagnostic Inhibit Write Gate Mode active, and counting the time to the first Sync In. The measured time is checked for optimum value of 67 byte-times (75 microseconds). Tolerance is ±3.0%. Valid range = 72–79 microseconds.

Note: The normal G2 length is 69 byte-times (77.28 microseconds). During a Write operation, the first Sync In is presented two byte-times earlier at byte 67 time.

Test 06. G3 Gap Tolerance

Test 06 measures the length of a G3 Gap by orienting on the G1 (HA) field, starting a Write G3 operation with Diagnostic Inhibit Write Gate Mode active, and counting the time to the first Sync In. The measured time is checked for an optimum value of 71 byte-times (79.72 microseconds). Tolerance is ±3.0%. Valid range = 77–82 microseconds.

Note: Normal G3 gap length is 73 byte-times. During a Write operation, the first Sync In is presented 2 byte-times earlier at byte 71 time.

Test 07. Data Transfer

Test 07 initiates a Write G1 operation with Diagnostic Inhibit Write Gate Mode active, using a data pattern of 'EB6DB6DB'. At the end of the operation, this test verifies that no ECC Check and no Write Data Check were received.

Test 08. Write Safety Checkers Check
Force Control Check
Force Write Ovrn Check
Force Transition Check
Force Write I Check

Test 08 verifies that a Check Reset resets Read/Write Check, Control Check, Write Overrun Check, Transition Check, and Write I Check. The test forces Control Check by raising Read Gate and Write Gate simultaneously.

The test forces Write Overrun Check by orienting near the end of the Active Track, raising Write Gate to the drive and holding it up through Index. The test forces Transition Check and Write I Check by raising Write Gate to the drive without bus out bit 4 = 1. This inhibits Current Source Unblocked. The test checks that each of the above conditions forces Read/Write Check and that it is reset by a Check Reset.

Test 09. Force Low Gain Check (FHFE Only)

Test 09 verifies proper operation of the Low Gain Check circuit. First, the test issues a Check Reset and verifies that No Low Gain Check and No Read/Write Check are active. The test then forces a Low Gain Check through use of a diagnostic command and verifies that Low Gain Check and Read/Write Check become active.

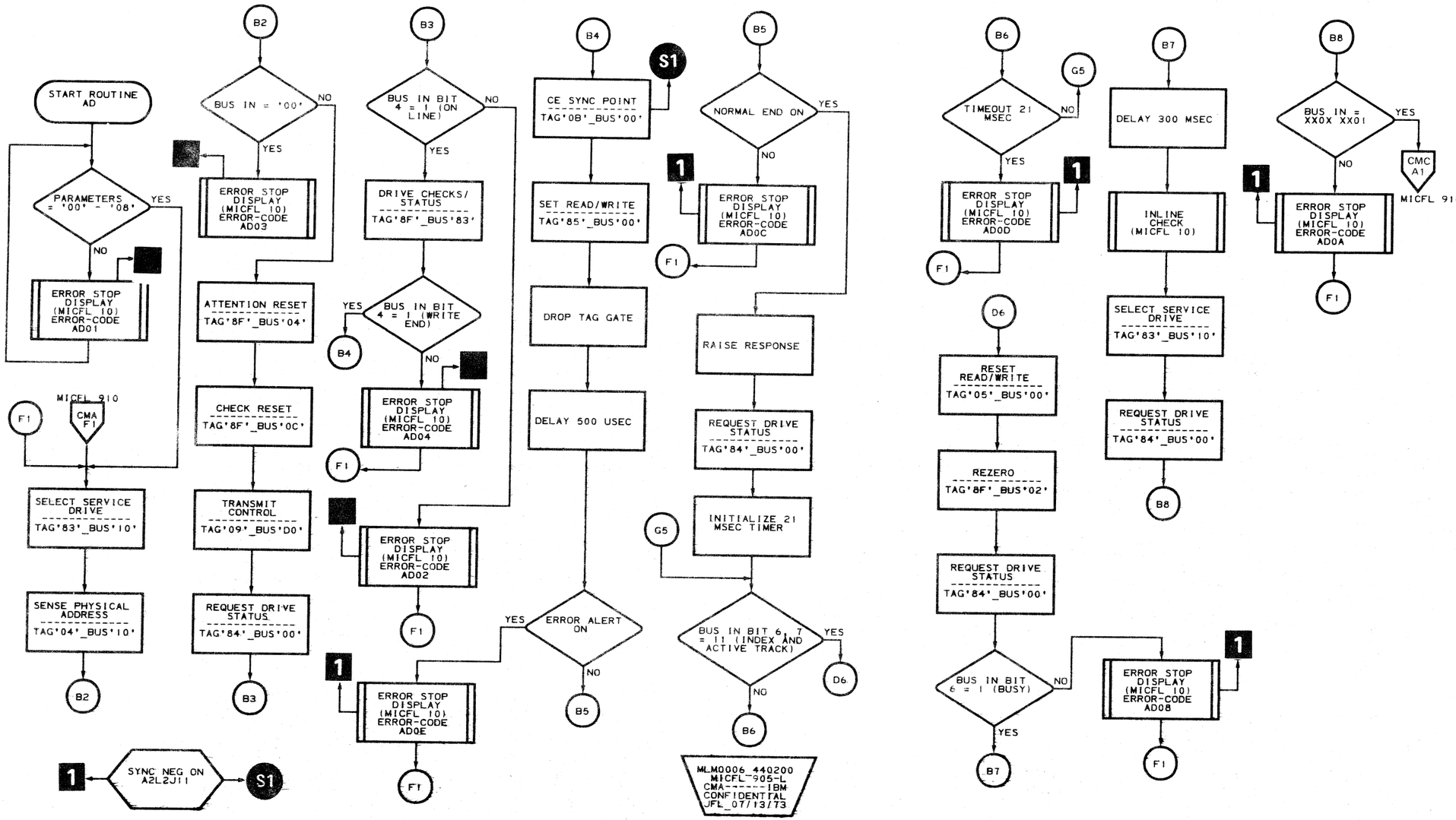
The test then issues a Check Reset and verifies that Low Gain Check and Read/Write Check are both reset.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.



CE0905	2747093	440200	440202	440203	440227			
Seq. 1 of 1	Part No.(N)	25 June 73	7 Sept 73	2 Nov 73	14 Sept 76			

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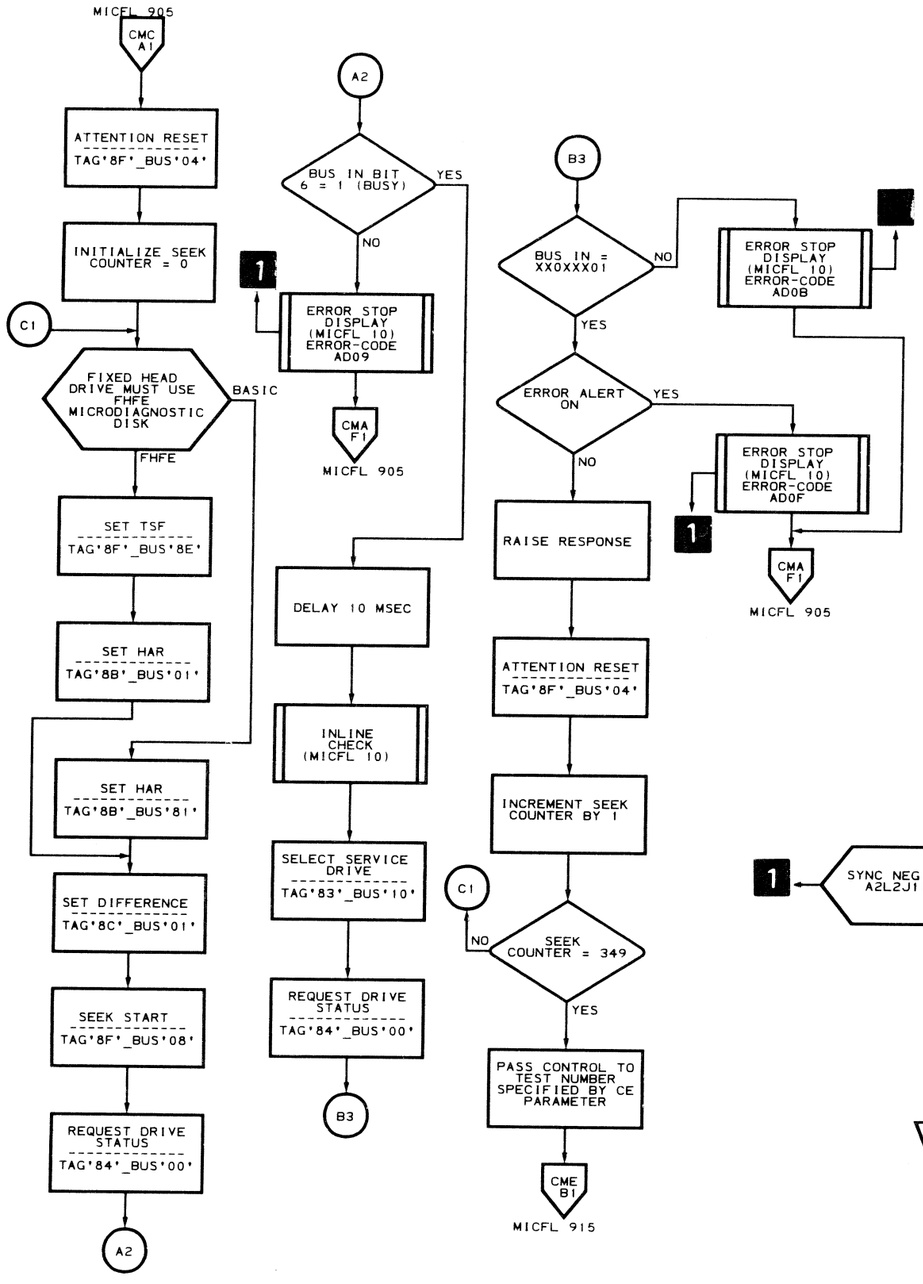
GAP COUNTER AND DATA TRANSFER (Routine AD)



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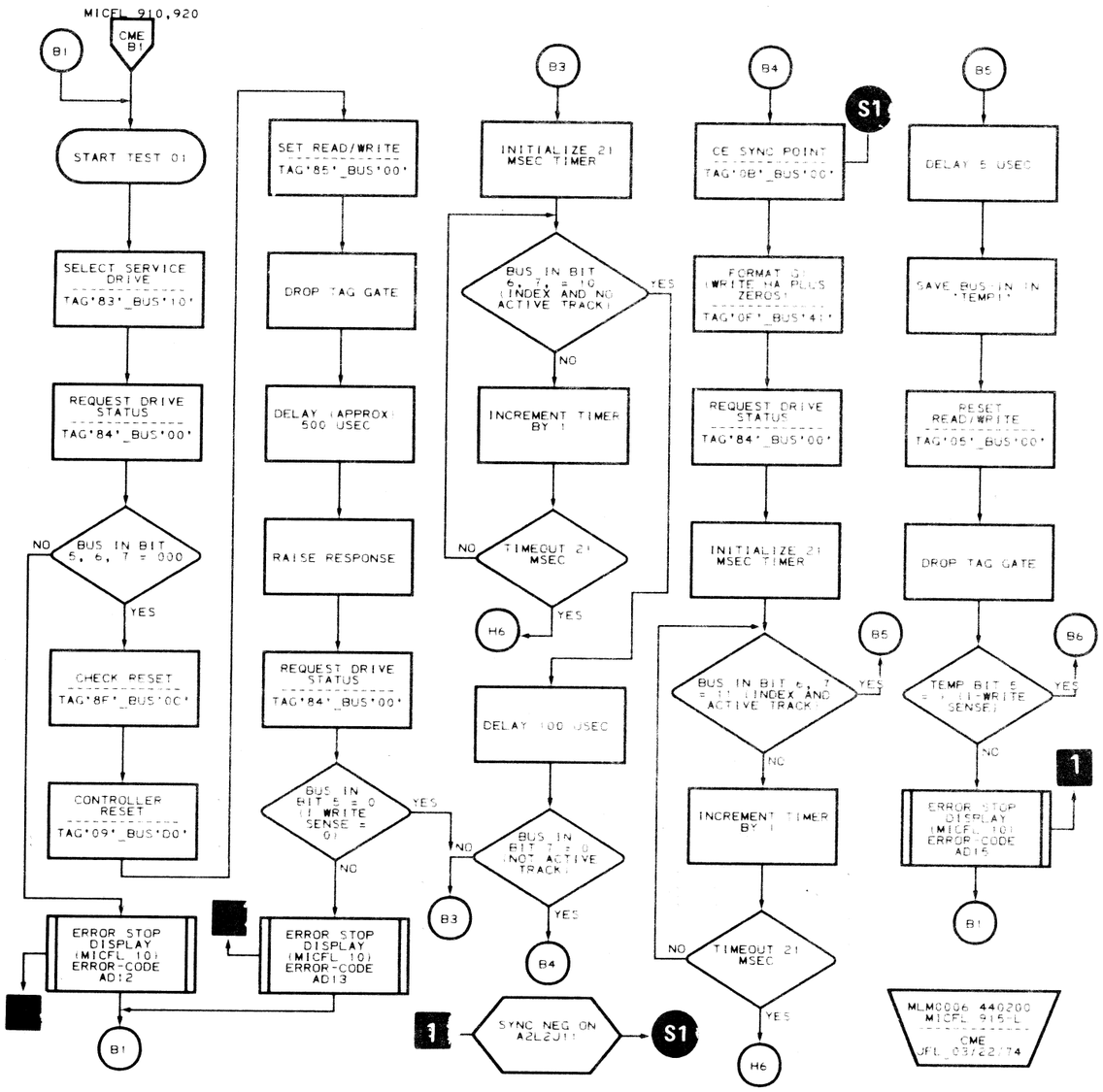
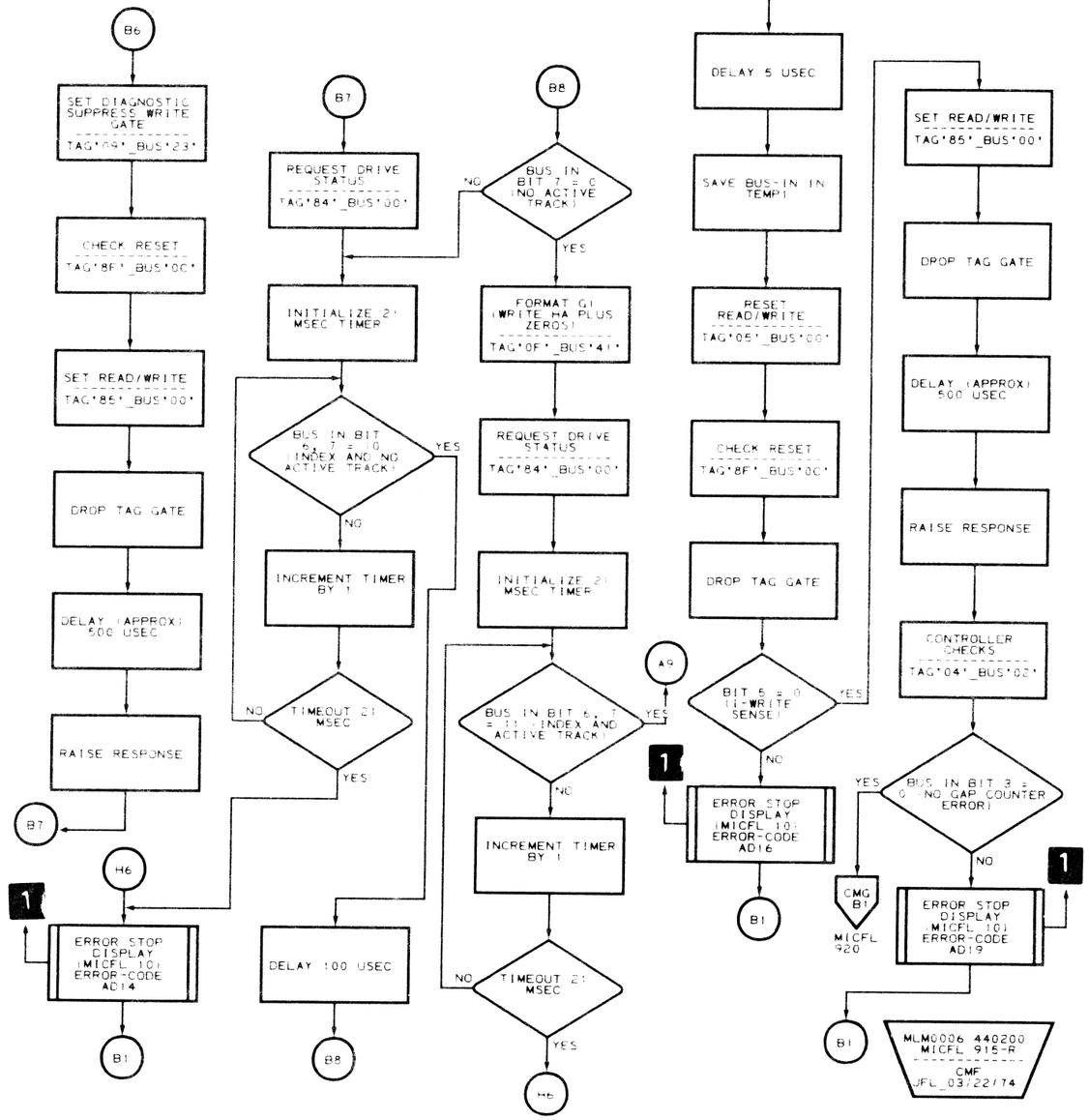
DATA TRANSFER CHECKERS CHECK (Routine AD)





CE0910	2747094	440200	440202	440203	440210	440218	440227	
Seq. 2 of 2	Part No.(N)	25 Jun 73	7 Sept 73	2 Nov 73	15 Apr 74	5 Aug 74	14 Sept 76	

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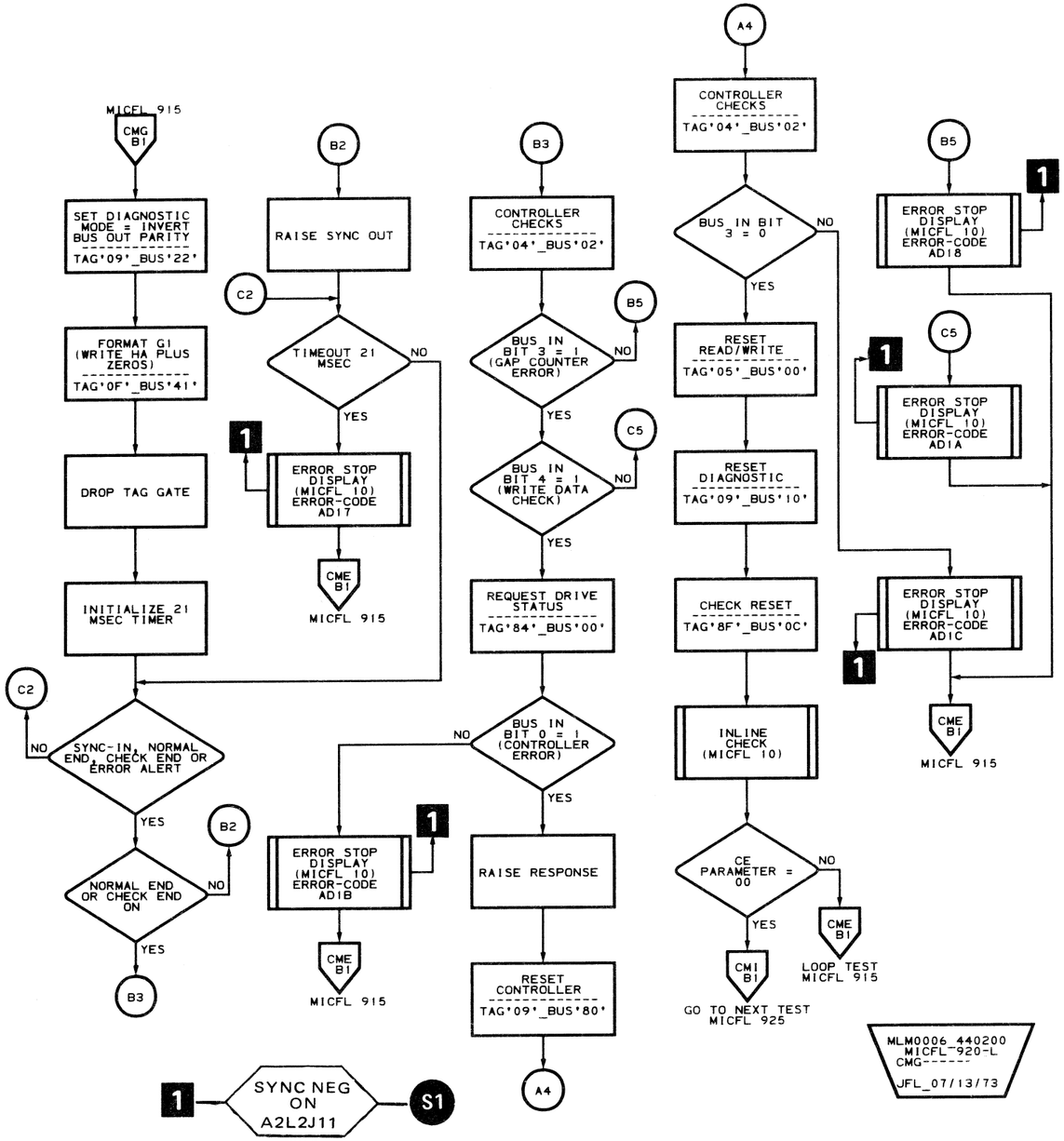

CE0920 Seq. 1 of 2	2747095 Part No.( )

440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74	440223 14 Mar 75		

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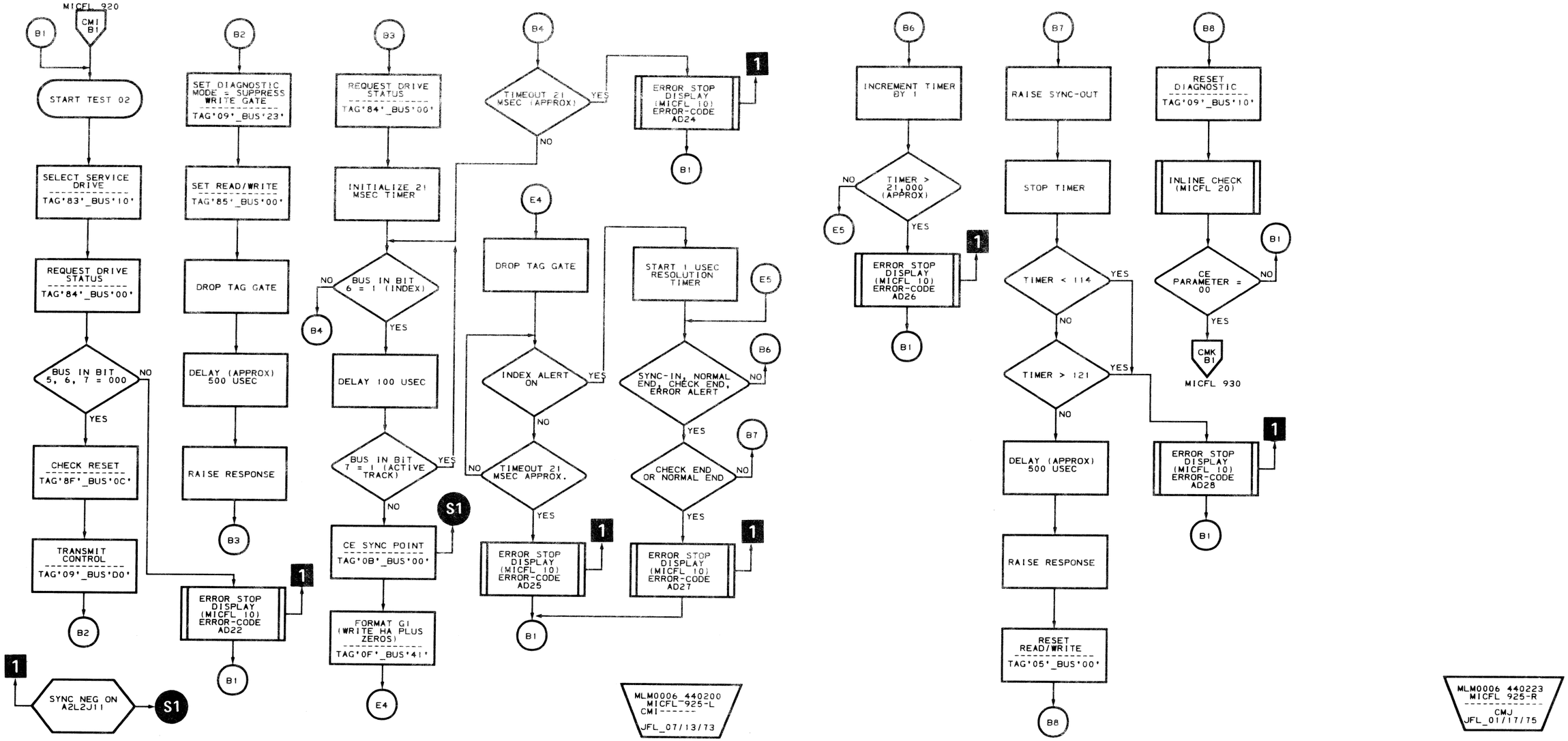

CE0920 Seq. 2 of 2	2747095 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74	440223 14 Mar 75		

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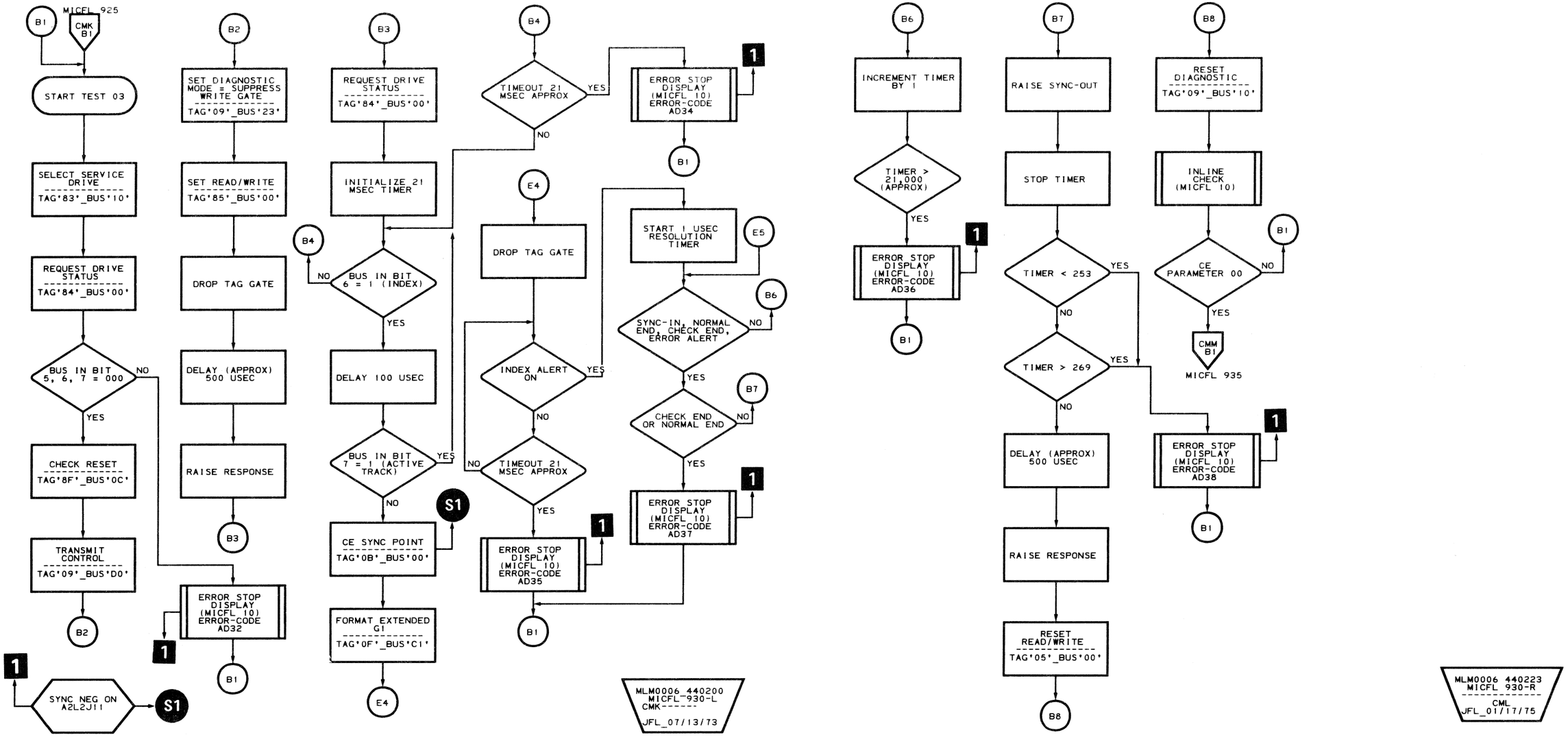

CE0930	2747096
Seq. 1 of 2	Part No.(N)

440200	440202	440203	440214	440219	440223	440227
25 June 73	7 Sept 73	2 Nov 73	17 Jun 74	26 Sept 74	14 Mar 75	14 Sept 76

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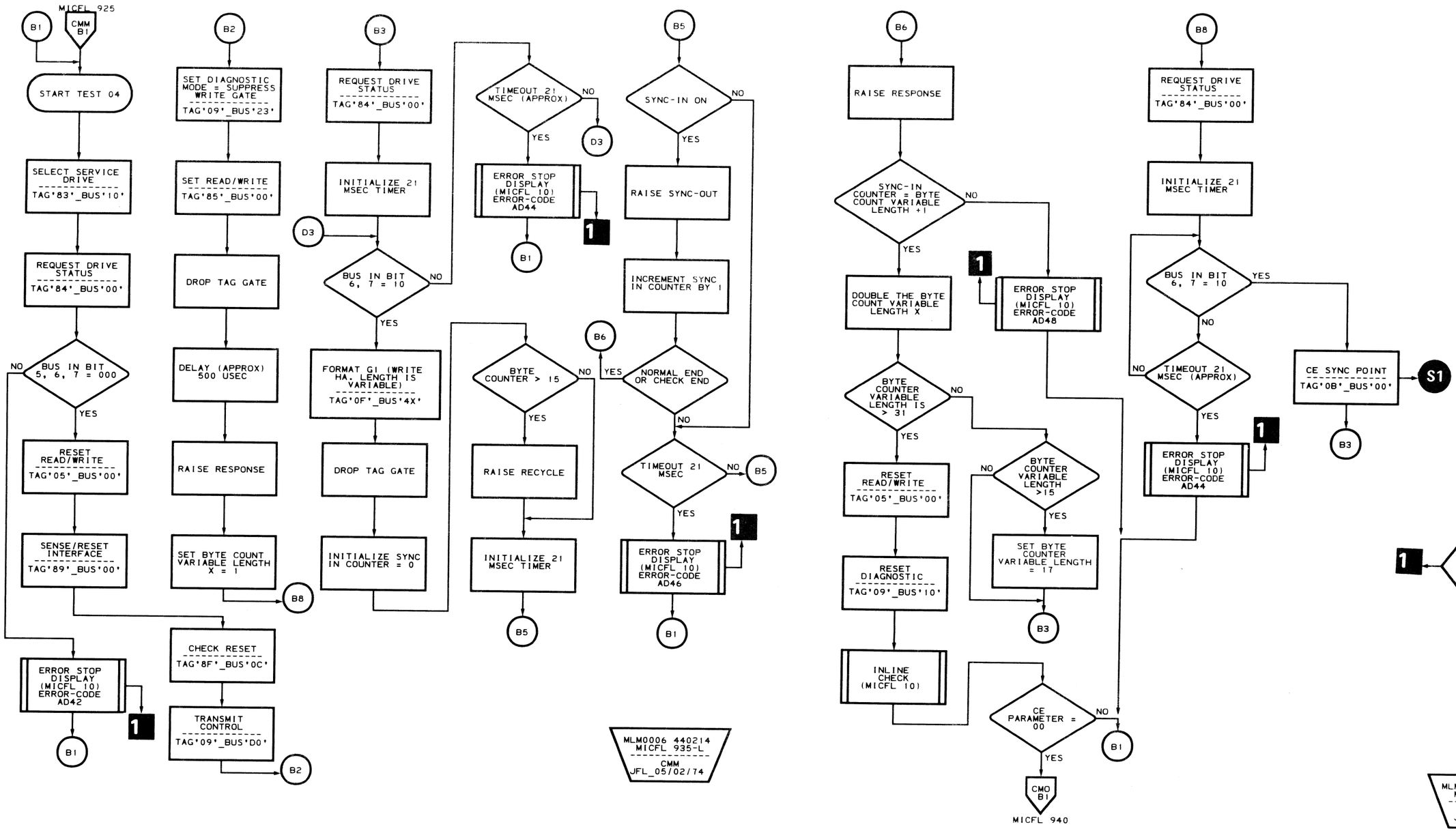

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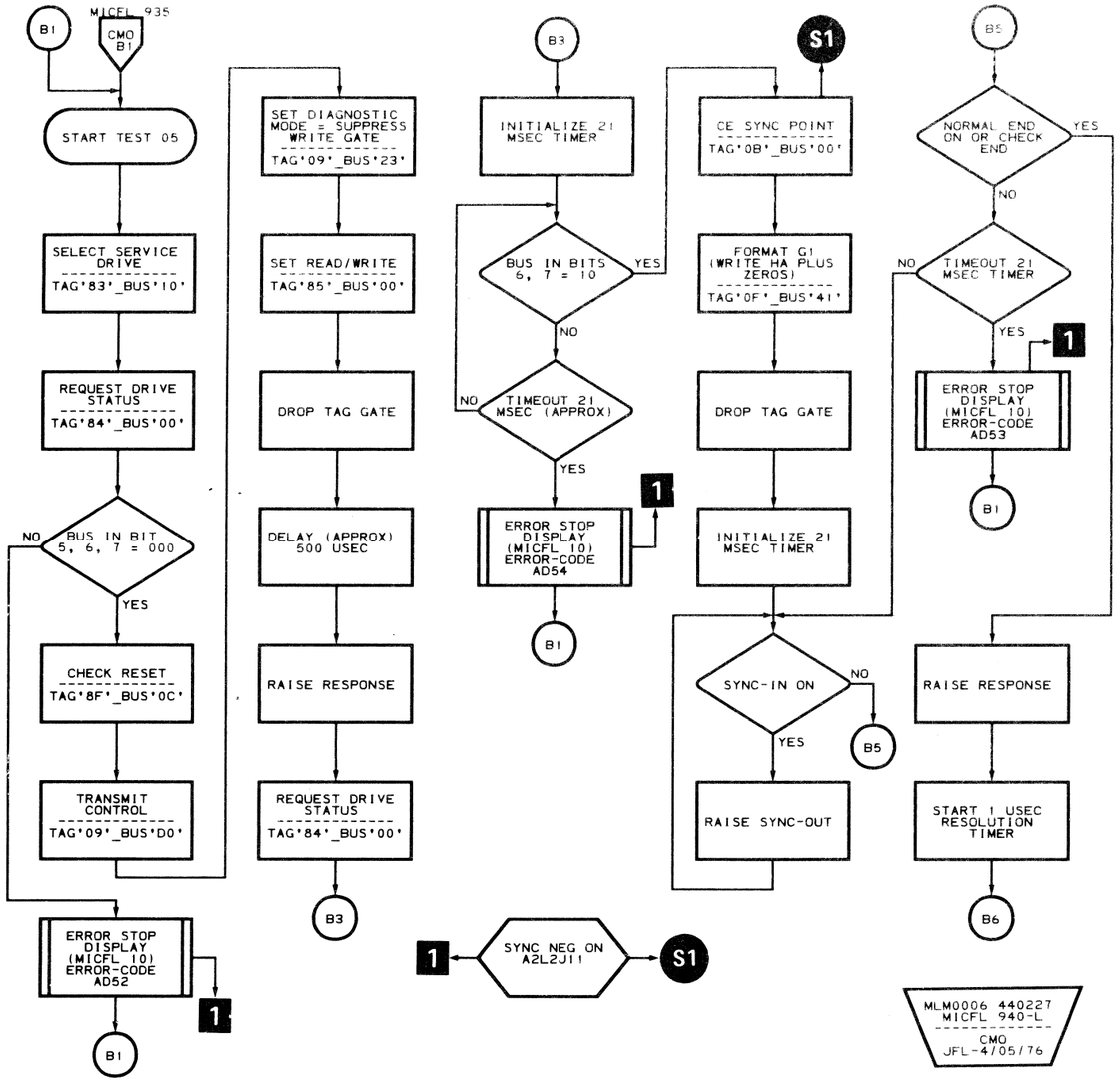

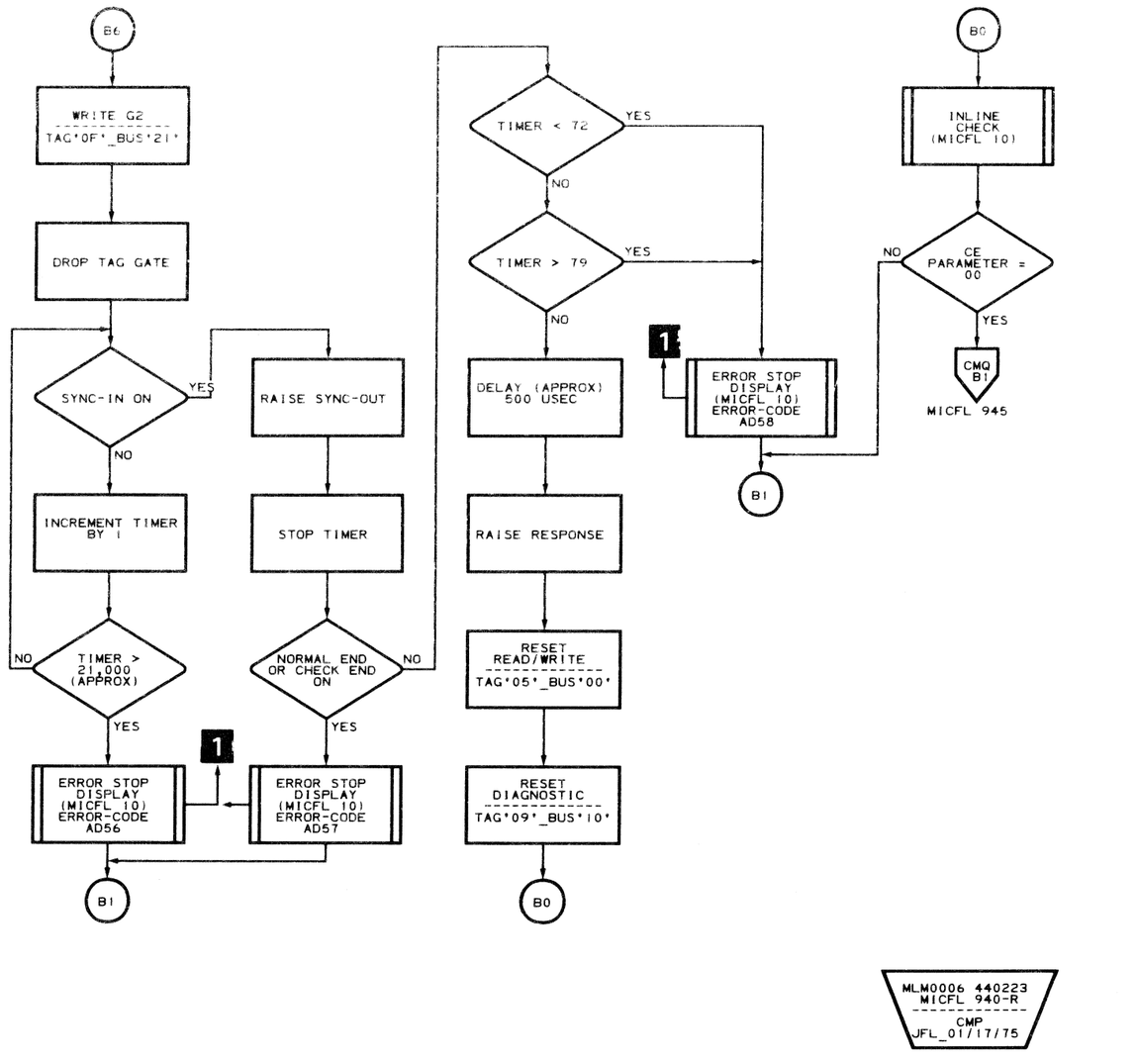

CE0940	2747097
Seq. 1 of 2	Part No.(N)

440200	440202	440203	440223	440227		
25 June 73	7 Sept 73	2 Nov 73	14 Mar 75	14 Sept 76		

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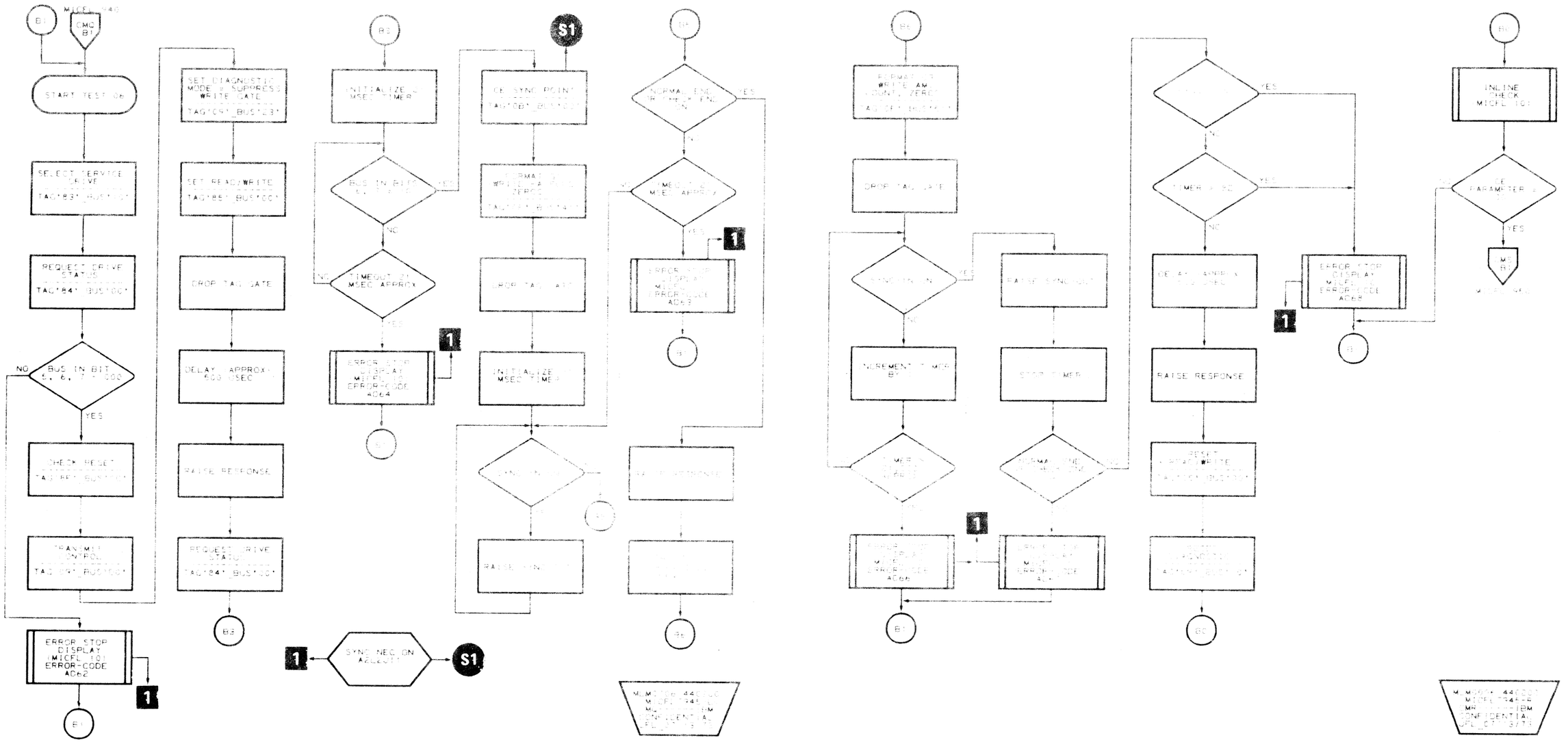

CE0940 Seq. 2 of 2	2747097 Part No.(N)	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440223 14 Mar 75	440227 14 Sept 76	

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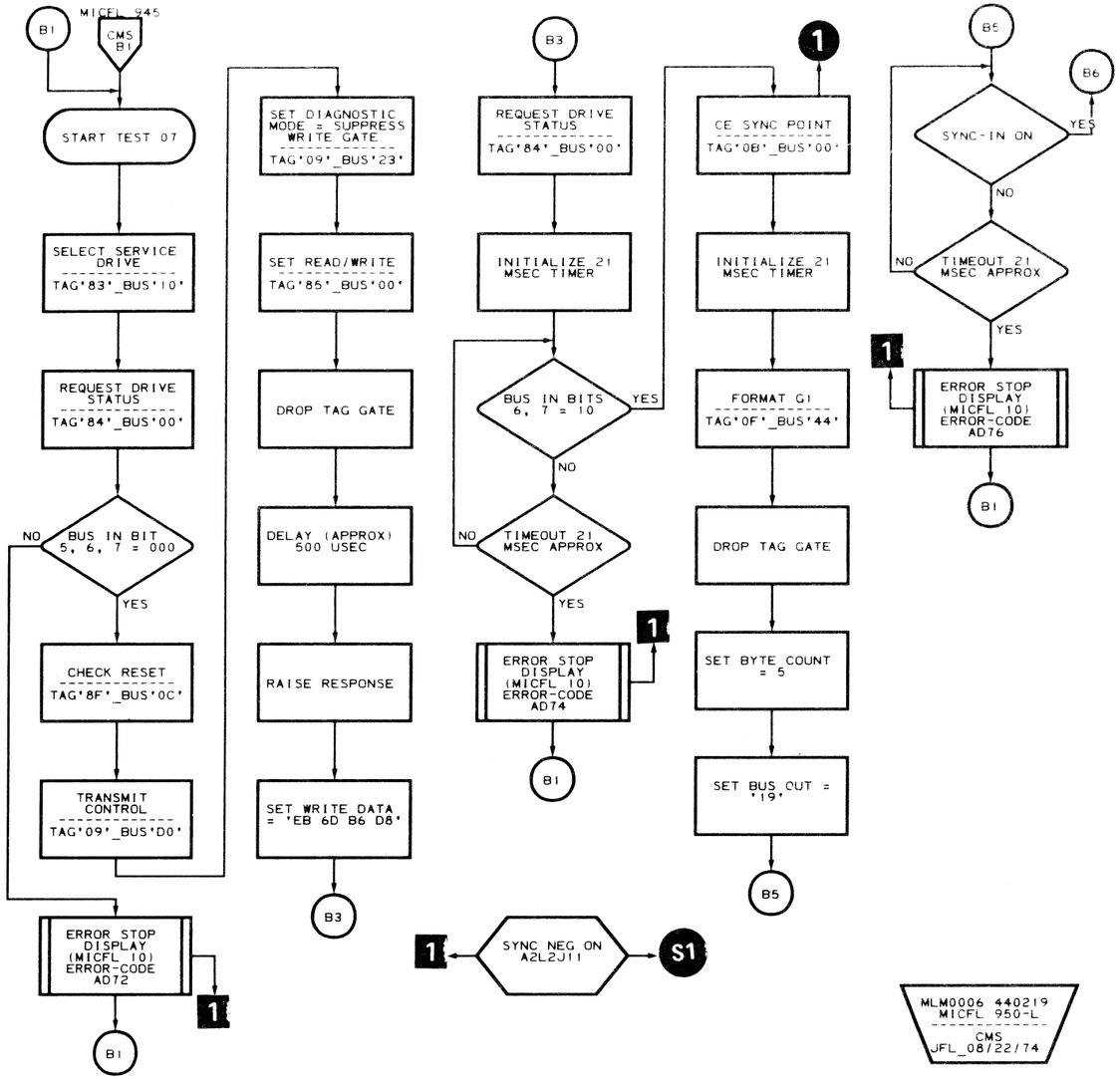

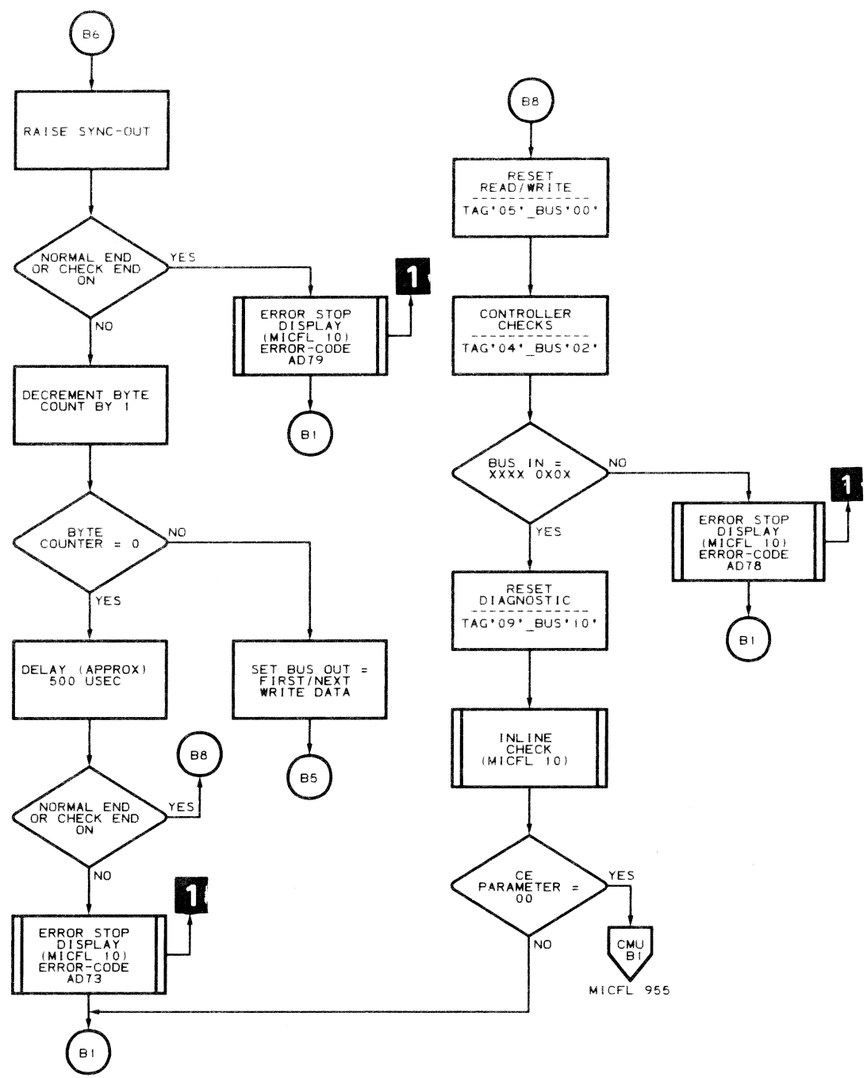

CE0950 Seq. 1 of 2	2747098 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440214 17 Jun 74	440219 26 Sept 74	

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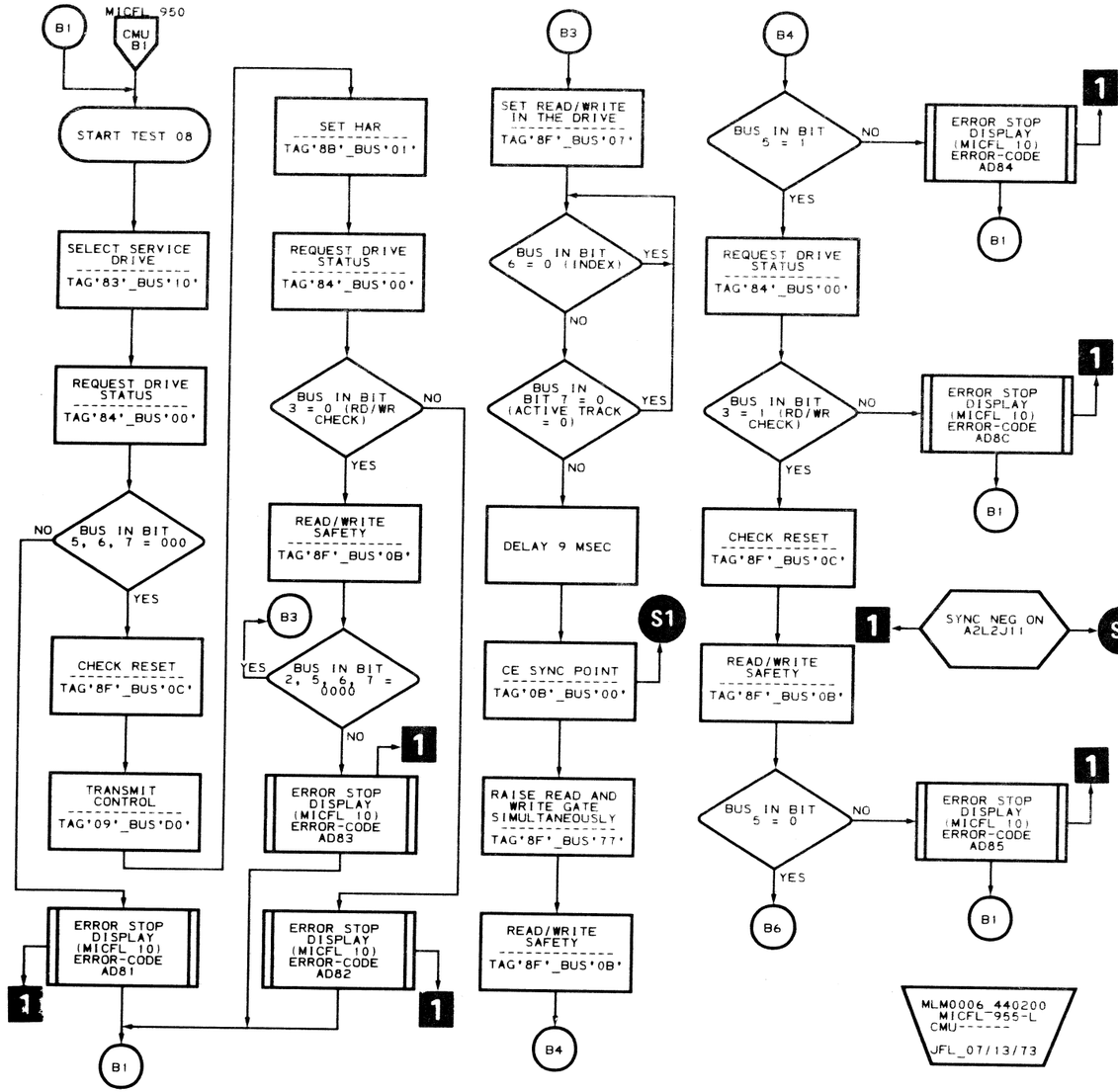

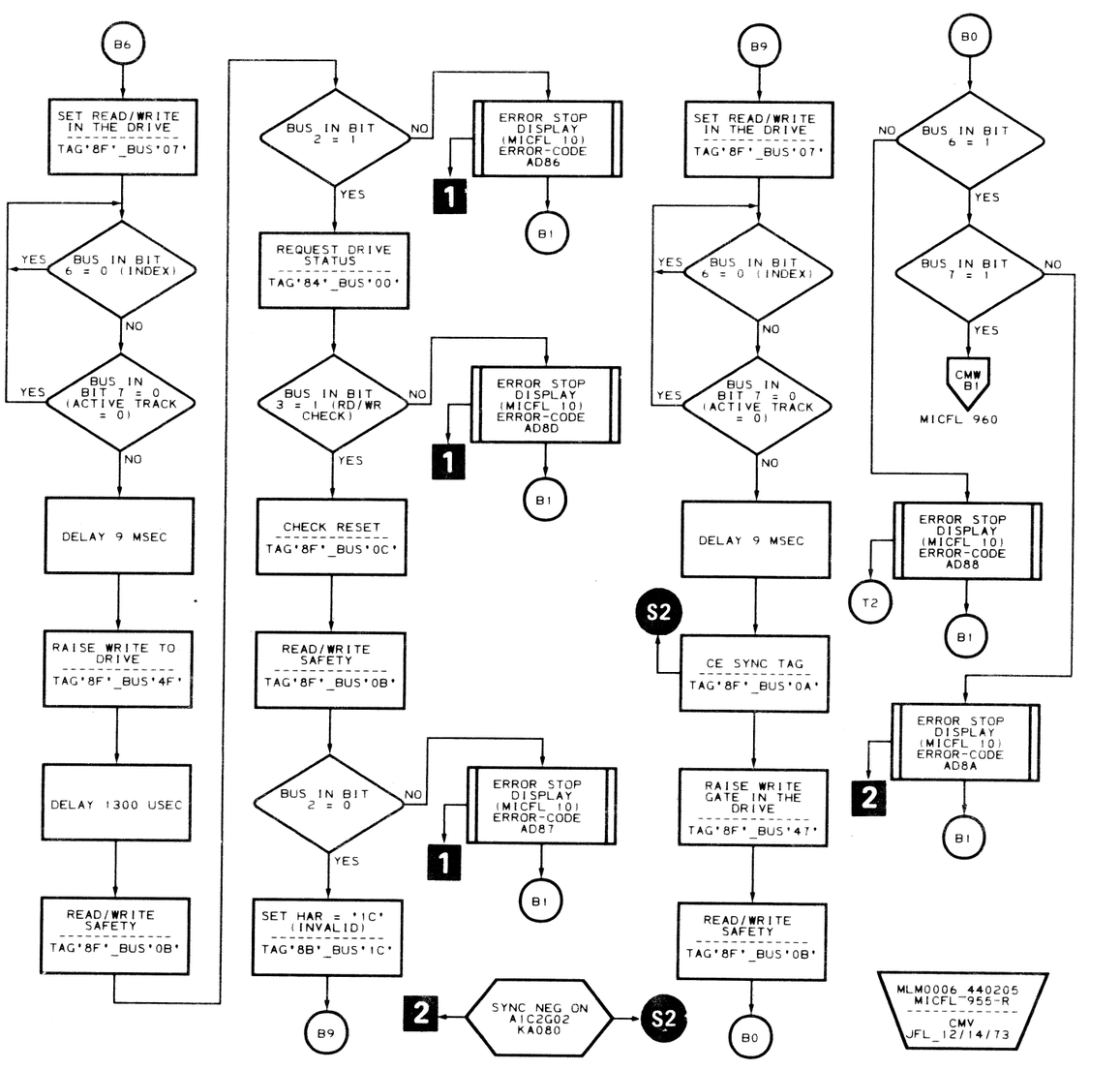

CE0950	2747098	440200	440202	440203	440205	440214	440219	
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	28 Jan 74	17 Jun 74	26 Sept 74	

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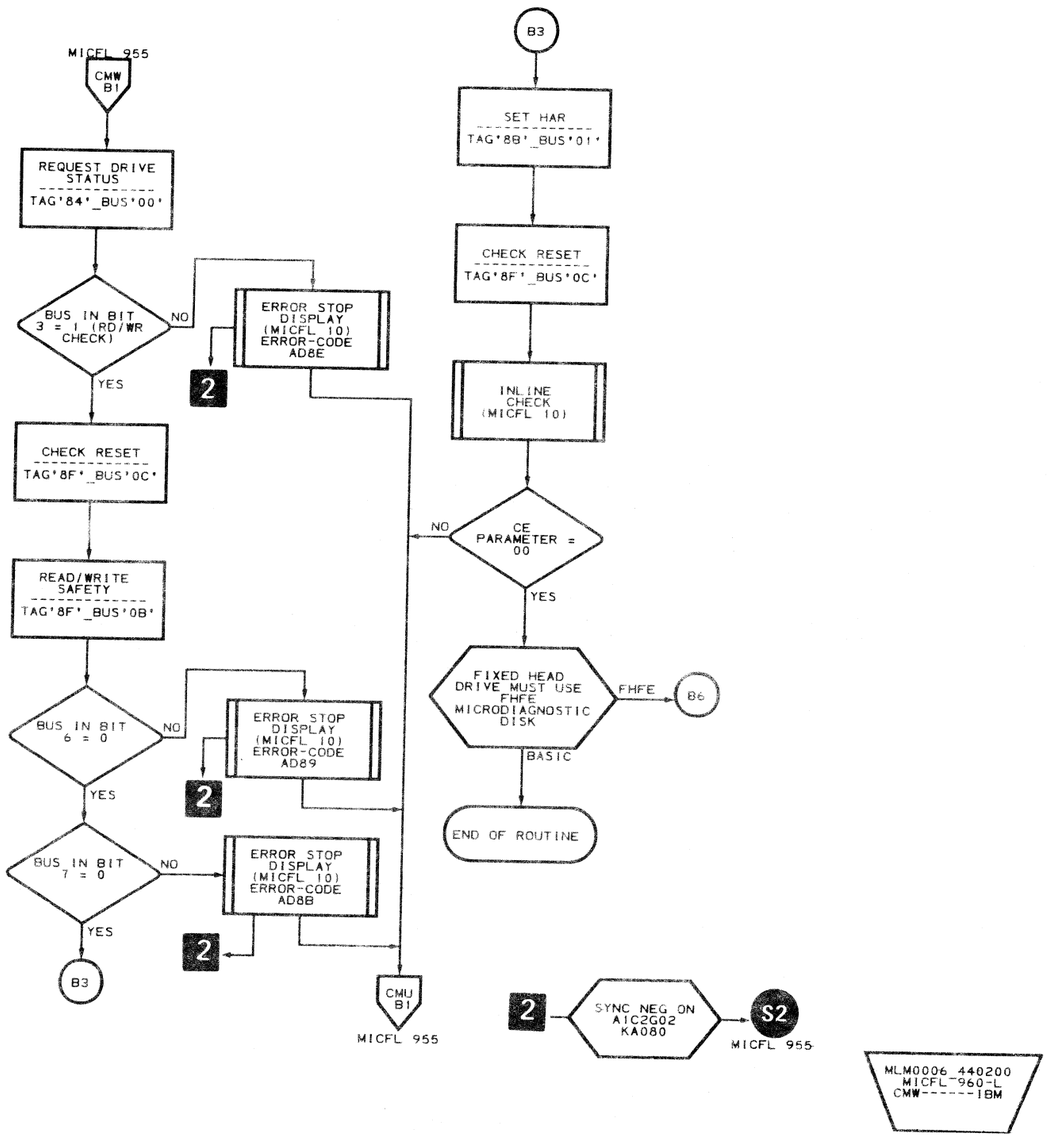
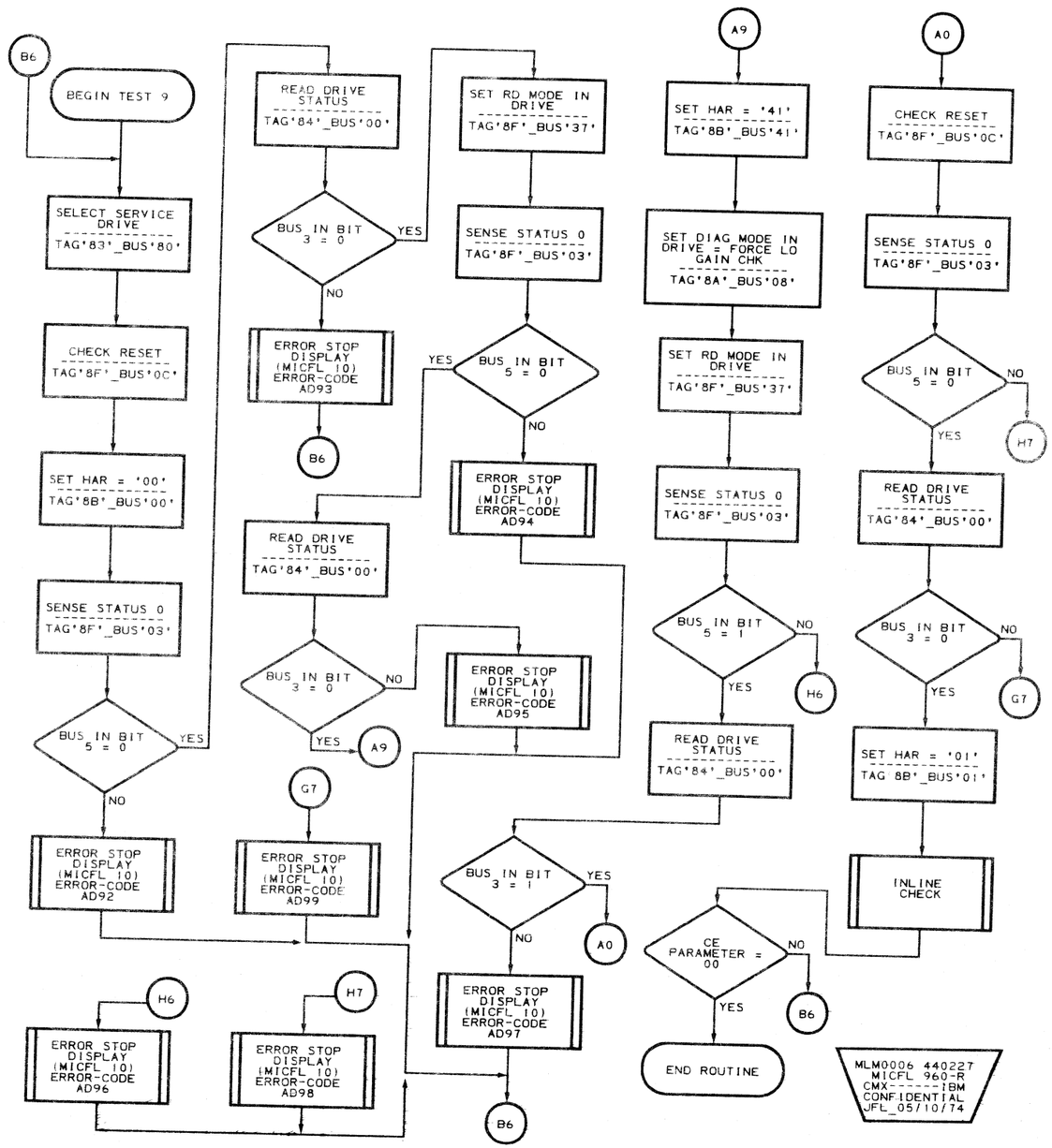
DATA TRANSFER CHECKERS CHECK (Routine AD)





CE0960	2747099
Seq. 1 of 1	Part No.(N)

440200	440202	440203	440218	440227		
25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74	14 Sept 76		

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ROUTINE AD TEST 1 SCOPING PROCEDURES

Routine AD test 1 verifies the following conditions:

(A) If Write Gate is raised without Suppress Write, I Write Sense is returned.

(B) If Write Gate is raised with Suppress Write, I Write Sense is not returned.

(C) The I Write Sense line is not always active.

(D) The Gap Counter and Write Data Check latches function normally.

Note: I Write Sense is referred to in the Controller as DEV BI bit 5 MST.

The sequence of pictures on this page illustrates Item A above. Note that Write Gate Suppressed is active with Write Gate if Suppress Write Gate is not active.

The Addr Mark Gate is used in the drive as a redundancy check of Write Gate.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Time: 5 ms/div

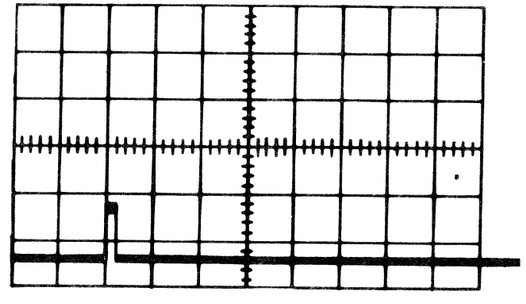
Using triggered delayed sweep as described below with delay time as indicated.

Vertical all pictures 0.1 volts/div X10 probes

Unless otherwise indicated.

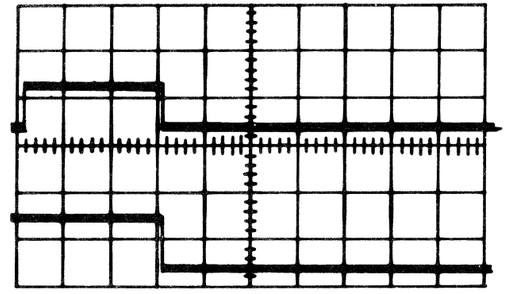
+FMT G1 – A intensified during B
A2Q2M13 (BH140) 0.1 volts/div
Alternate: A2P2P02 (BG140)
Delay Time 5 μs/div

This is the first FMT G1 after the sync.



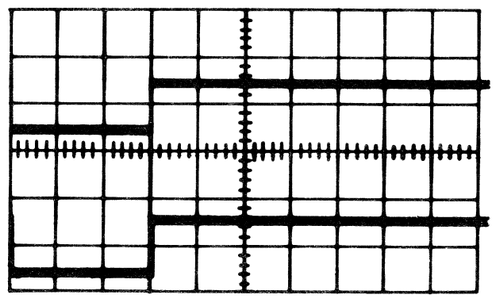
Delayed Sweep

+Dev B1 bit 5 MST
A2F2S10 (BA160)



+FMT G1
A2Q2M13 (BH140)
Alternate: A2P2P02 (BG140)

–Write Gate Suppressed
A2Q2P07 (BH140)



–Addr Mark Gate
A2Q2U06 (BH140)

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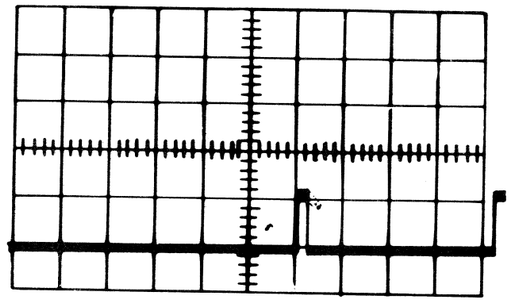
ROUTINE AD TEST 1 SCOPING PROCEDURES

This sequence of pictures illustrates Item B from the previous page. Note that Write Gate Suppressed is blocked by Suppress Write Gate. + Device BI Bit 5 MST (I Write Sense) would also be at it's inactive level. If not, it is being held active.

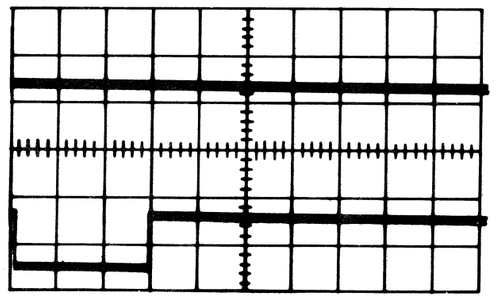
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Vertical: 0.1 volts/div X10 probe
Time: 5 ms/div using triggered delayed sweep as described below with delay time as indicated.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

+ FMT G1 A intensified during B
A2Q2M13 (BH140)
Alternate: A2P2P02 (BG140)
Delay Time: 5 μs/div
This is the second FMT G1



– Write Gate Suppressed (At + level)
A2Q2P07 (BH140)



–Address Mark Gate
A2Q2U06 (BH140)

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AD – TEST 1 SCOPING PROCEDURES

AD – TEST 1 SCOPING PROCEDURES

This sequence of pictures illustrates how (with Invert Bus Out Parity active) the Gap Counter Check and Write Data Check are forced. Gap Counter Check is activated as follows:

1. Line 4 to 7 odd is inverted with the Invert Bus Out Parity diagnostic function.
2. At Write Mode time (see right), where modulo count is set into the Gap Counter with Inverted Parity, causing a Gap Counter Check.

The Write Data Check is activated as follows:

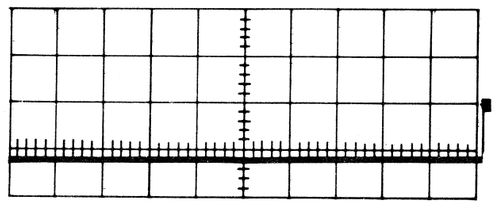
1. Bus Out Parity Bit is inverted using the Invert Bus Out Parity diagnostic function as data is transferred to the SERDES Buffer.
2. After the data byte is serialized, the generated parity from the SERDES Shift Register is compared with the Inverted Parity Bit which results in a miscompare and sets the Write Data Check.

End Data Op and Normal End complete the operation.

Note: When scoping, be aware that once an error is detected, further testing is suspended and the error message is generated. Therefore, the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

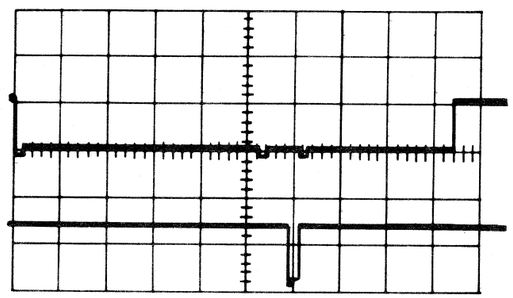
+FMT G1 A intensified during B
A2Q2M13 (BH140)
Alternate: A2P2P02 (BG140)
This is the third FMT G1
Delay Time: 5 μs/div



Delayed Sweep

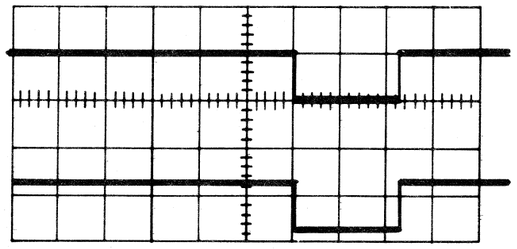
–Write Gate
A2Q2G10 (BG140)

–Write Mode
A2P2U12 (BH140)



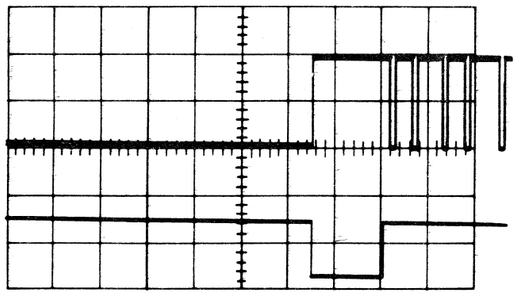
–Counter Check
A2P2M05 (BG160)

–WR Data Check
A2S2G11 (BC130)



+Normal End NPL 0.2 volts/div X10 probes
A2K2D11 (BE160)

–End Data Op
A2P2S05 (BG170)



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AD – TEST 2 SCOPING PROCEDURES

AD – TEST 2 SCOPING PROCEDURES **MICFL 970**

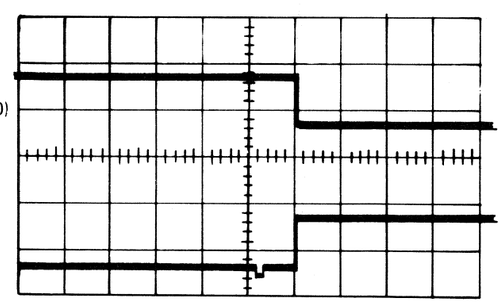
This test verifies the generation of a G1 Gap. It measures from the Index represented here by the rise of +FMT G1 to the first Sync In pulse. Note that this time is just less than 6 divisions or approximately 118 microseconds.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Vertical: 0.1 volts/div X10 probes

Time: 5 ms/div using triggered delayed sweep with trigger on + FMT G1 (A2Q2M13 (BH140)) and delayed time of 20 μs/div.

+ FMT G1
A2Q2M13 (BH140)
Alternate:A2P2P02 (BG140)

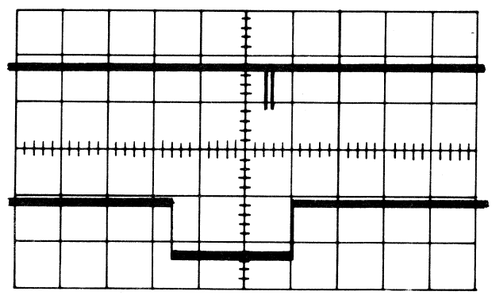
–Write Gate
A2Q2G10 (BH140)



Note: When scoping, be aware that once an error is detected, further testing is suspended and the error message is generated. Therefore, the signals beyond the point of the error are not valid.

–Sync In
A2S2U10 (BC170)

–Transfer Sector Count
A2Q2J07 (BH120)



CE0968	2747101	440200	440203	440213	440223			
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ROUTINE AD TEST 3 SCOPING PROCEDURES

Routine AD test 3 tests the generation of a special G1 Gap, that is, a G1 Gap that has been extended by 128 bytes to skip a defect in the home address area.

The operation begins at Index just as a G1 operation. The Gap Counter, which is reset to zero at Index, counts to byte 53 time. At Count 53, the Add 128 pulse causes the count to immediately jump to a value of 181. Since this is beyond all of the G1 controls, the counter must wrap from 255 back to zero and the controls are activated the second time around.

The program measures the time from Index, represented here by the rise of +FMT G1 to the first Sync In. Note that the time is more than 5 divisions at 50 μs/div or approximately 262 microseconds.

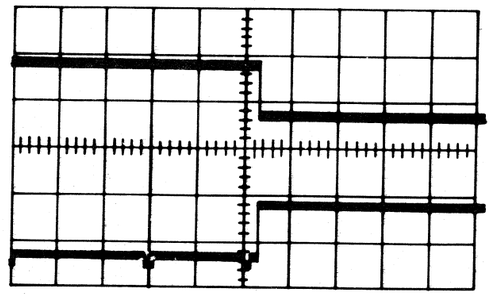
Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 1 volts/div X10 probe

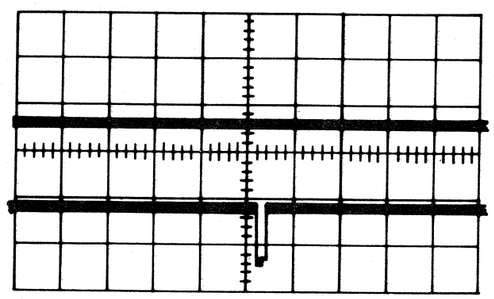
Time: 5 ms/div using triggered delayed sweep with trigger on +FMT G1 (A2Q2M13(BH140)) and delayed time of 50 μs/div.

+FMT G1
A2Q2M13 (BH140)
Alternate: A2P2P02(BG140)



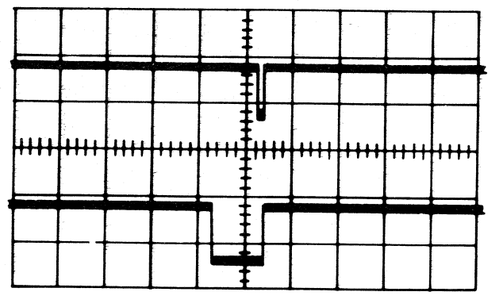
–Write Gate
A2Q2G10 (BH140)

+Add 128
A2Q2P13 (BH160)



–Write Mode
A2P2U12 (BG140)

–Sync In
A2S2U10 (BC170)



–Transfer Sector Count
A2Q2J07 (BH120)

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ROUTINE AD TEST 4 SCOPING PROCEDURES

This test checks the Gap Counter in modulo 16 mode; that is, while it is counting bytes written or read, as opposed to Gap Counter Mode as in the previous tests. On successive revolutions of the disk, G1 records of 1, 2, 4, 8, and 16 bytes are written, the program verifies the number of bytes transferred. These pictures show Write Mode in relation to sync. in pulses. Note that there is always one more sync in than there is count. The extra pulse is for the sync byte and is the first pulse.

The first picture shows Write Mode pulses for the 5 test values each one revolution apart. The succeeding pictures, using delayed sweep, display the sync in pulses in relation to the Write Mode Pulse. An additional picture shows relation of the recycle line to the sync in pulses.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

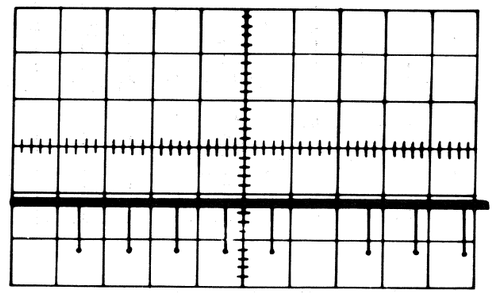
Sync Ext. (–): –RAS TP
A2L2J11 (BD 100)

Vertical: 0.1 volts/div X10 probes

Time : 20 ms/div using triggered delayed sweep triggering on +FMT G1 (A2Q2M13 (BH140)). The delay is advanced to display the successive Write times. Start with delay time multiplier set to minimum.

–Write Mode
A2P2U12 (BG140)

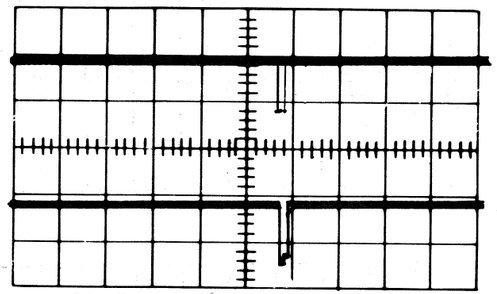
Note: First 5 pulses.
Delay not used for this photo.



Delay Time: 20 μs/div

–Sync In
A2S2U10 (BC170)

Note: There are 2 pulses.



–Write Mode
A2P2U12 (BG140)

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ROUTINE AD TEST 4 SCOPING PROCEDURES (continued)

These pictures illustrate the actions for Modulo counts of 2, 4, 8, and, 16 respectively. The last picture shows the action of the recycle line from the Storage Control. Adjust the delay time multiplier to view the succeeding operations.

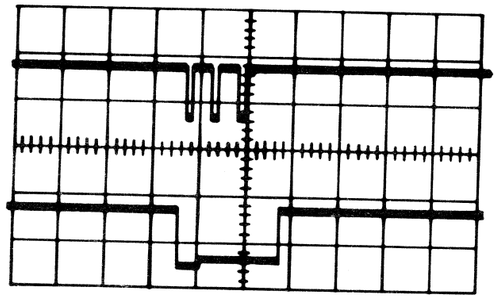
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

0.1 volts/div X10 probes

Time: 20 ms/div using triggered delayed sweep triggering on + FMT G1 (A2Q2M13 (BH140)). The delay is advanced to display the Successive Write times. Start with delay time multiplier set to minimum.

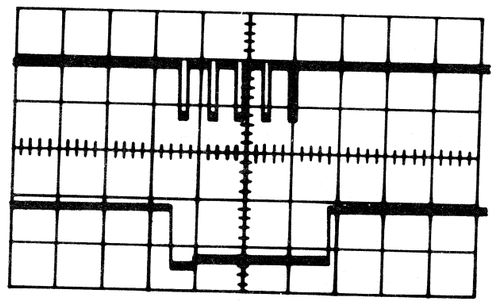
–Sync In - Modulo Count Equals 2
A2S2U10 (BC170)

–Write Mode
A2P2U12 (BG140)



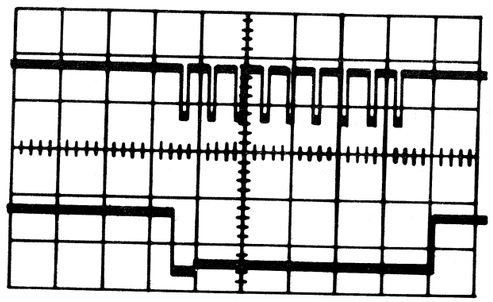
Modulo Count = 4
A2S2U10 (BC170)

–Write Mode
A2P2U12 (BG140)



Modulo Count = 8
A2S2U10 (BC170)

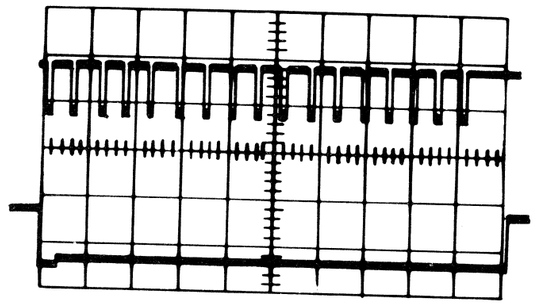
–Write Mode
A2P2U12 (BG140)



Note: When scoping, be aware that once an error is detected futher testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

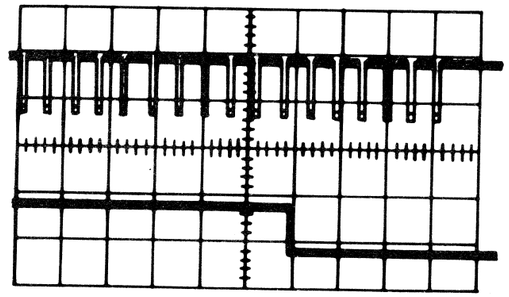
Modulo Count = 16
A2S2U10 (BC170)

–Write Mode
A2P2U12 (BG140)



– Sync In (as above)
A2S2U10 (BC170)

+ Recycle
A2G2S10 (BF160)



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ROUTINE AD TEST 4 (CONTINUED)
SCOPING PROCEDURES
MICFL 975

ROUTINE AD TEST 5 SCOPING PROCEDURES

Routine AD test 5 verifies the gap length of a G2 Gap by measuring the time from Normal End of a previous operation (WR GI) to the first Sync In on the Write G2 operation.

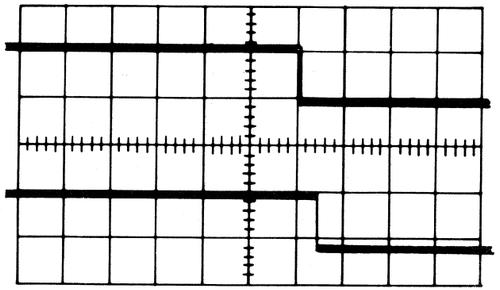
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes unless otherwise noted.

Time: 20 ms/div using triggered delayed sweep triggering on +FMT GI A2Q2M13 (BH140). Delay time 20 μs/div.

+FMT GI
A2Q2M13 (BH140)
Alternate: A2P2P02 (BG140)

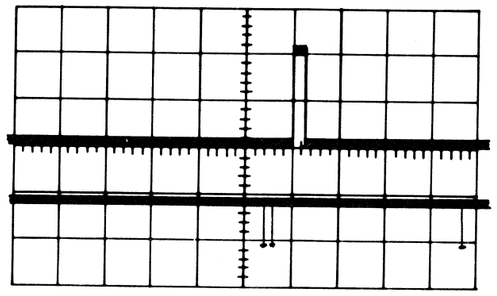
–G2
A2Q2D05 (BH110)



This picture contains the critical timing relation. The time from the rise of Normal End to the second group of Sync In pulses must be 75 to 79 ms.

+Normal End
A2K2D11 (BE160)
0.2 volts/div X10 probes

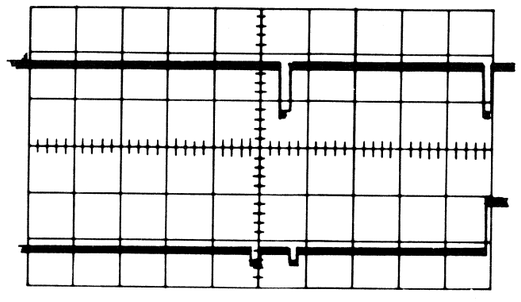
–Sync In
A2S2U10 (BC170)



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

–Write Mode
A2P2U12 (BG140)

–Write Gate
A2Q2G10 (BH140)



Note: Turn off of Write Gate is not critical in this test so long as it includes Write Mode time.

ROUTINE AD TEST 6 SCOPING PROCEDURES

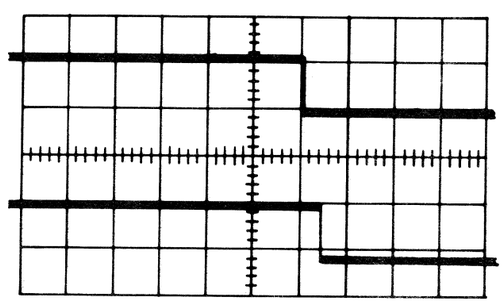
Routine AD Test 6 verifies the gap length of a G3 Gap by measuring the normal time of a previous Op (WR GI) to the first Sync In on the Write G3 operation.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

Time: 20 ms/div using triggered delayed sweep triggering on + FMT GI A2Q2M13 (BH140). Delay time at 20 μs/div.

+FMT GI
A2Q2M13 (BH140)

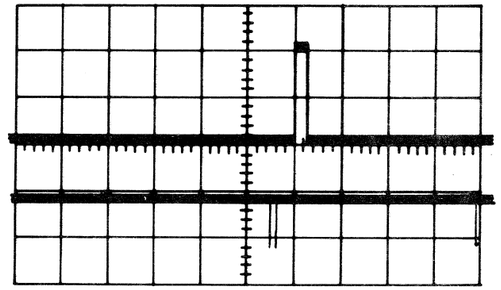


–G3
A2Q2D02 (BH110)

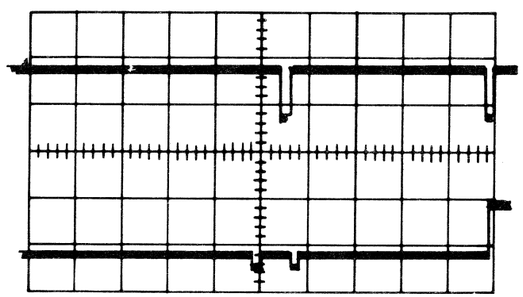
This picture contains the critical timing relationship of this test. The time from the rise of Normal End to the second set of Sync In pulses must be 77 to 82 microseconds.

+Normal End
A2K2D11 (BE160)
0.2 volts/div X10 probes

–Sync In
A2S2U10 (BC170)



–Write Mode
A2P2U12 (BG140)



–Write Gate
A2Q2G10 (BH140)

Note: When scoping, be aware that once an error is detected, further testing is suspended and the error message is generated. Therefore, the signals beyond the point of the error are not valid.

Note: Turn off of Write Gate is not critical in this test as long as it includes Write Mode time.

CE0980	2747104
Seq. 1 of 1	Part No. ( )

440200	440202	440203	440209			
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74			

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ROUTINE AE – ECC LOGIC TEST

DESCRIPTION

Each time this routine is selected, the following initialization occurs:

1. Put CE Drive online.
2. Install Write Enable Plug.
3. Rezero the access.
4. Seek to the CE Write Track.
5. Check for Test Selection and begin execution at the correct point.

Test 01. ECC Reset

Test 01 issues a Read G1 command with a short byte count (byte count = 4). This operation allows the ECC hardware to begin check character generation in the data area and causes an ECC Data Check to occur. The ECC Zeros Detect bit is checked to be sure that the ECC registers are loaded.

Another Read G1 is issued and allowed to proceed to Gap-54 time (the ECC registers are reset at Gap 53). A Sense Controller Error 2-Tag is issued and the Zeros Detect bit is checked to be sure that the ECC registers are reset.

Test 02. ECC Read Normal Data

Test 02 ensures that the ECC hardware can read an error-free data pattern and produce the correct ending conditions. The ECC write functions are not tested during this phase. During step 1 an 8-byte data pattern is written in the G2 position on the CE track. The 8-byte pattern consists of 2 bytes of data and 6 bytes of simulated ECC data.

During step 2, the 2 data bytes are read back and the ECC hardware generates the check characters from the remaining 6 bytes. The ending conditions are then checked for the proper results.

Test 03. ECC Read Correctable Data Check

The first two steps of Test 03 are similar to Test 02 except that the data pattern used is one that produces a correctable data check.

After the pattern has been written, read back, and the ending status checked, an ECC Correct Op Tag is issued. The correct operation is allowed to proceed to some end condition. After the end condition is received, the displacement counter, pattern registers, and ending status are checked for proper results.

Test 04. ECC Read Uncorrectable Data Check

Test 04 is the same as Test 03, except that an uncorrectable data pattern is used.

Test 05. ECC Write Burst (ECC Check Pattern)

During Test 05, the ability of the ECC hardware to gate the check character bytes to the serializer is checked by writing a 2-byte data pattern. This allows the ECC hardware to gate the 6 predetermined check bytes to the serializer. The 8-byte data and check pattern is read back (ECC Data Check is ignored) and compared byte-for-byte with what was written.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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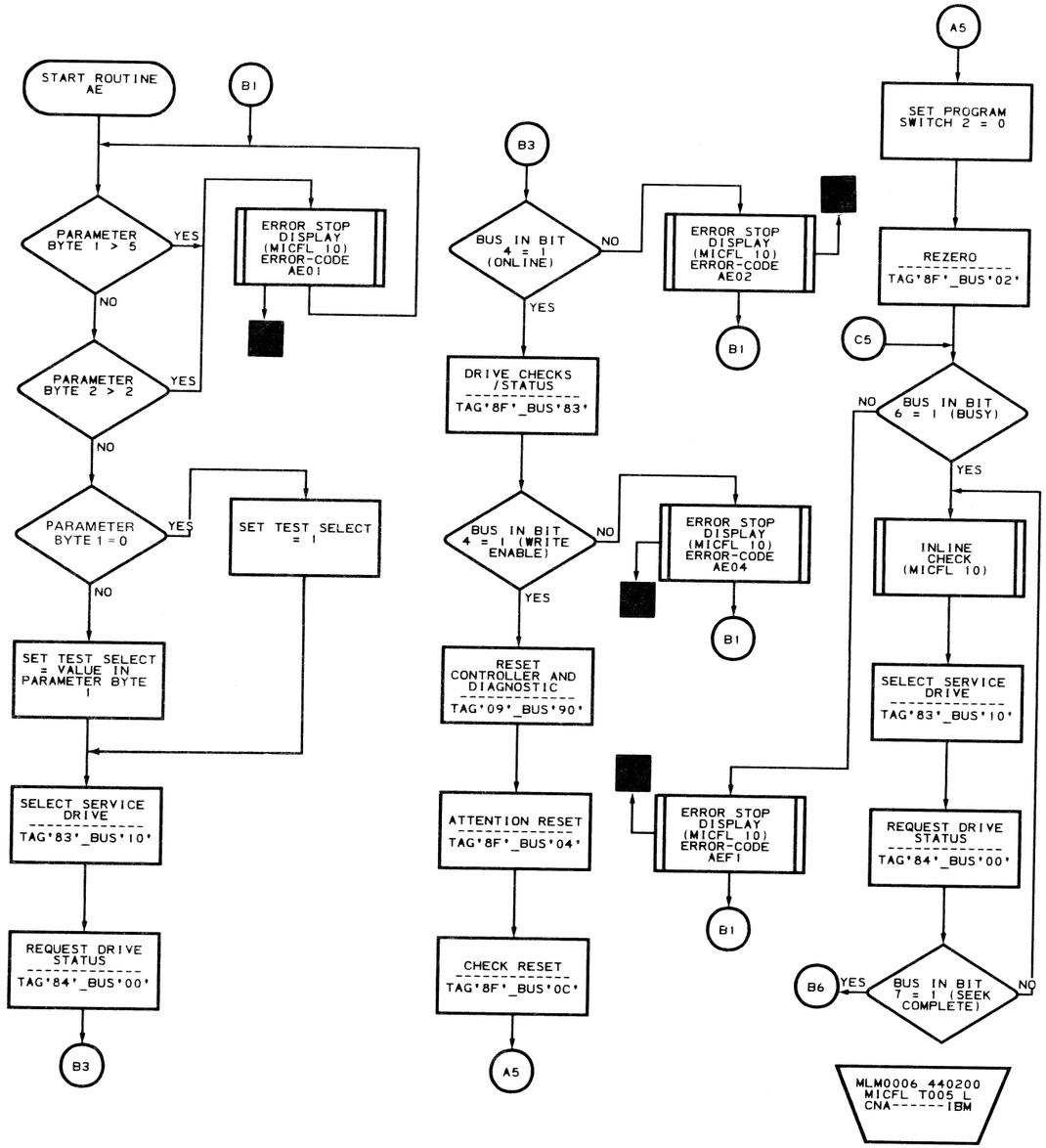
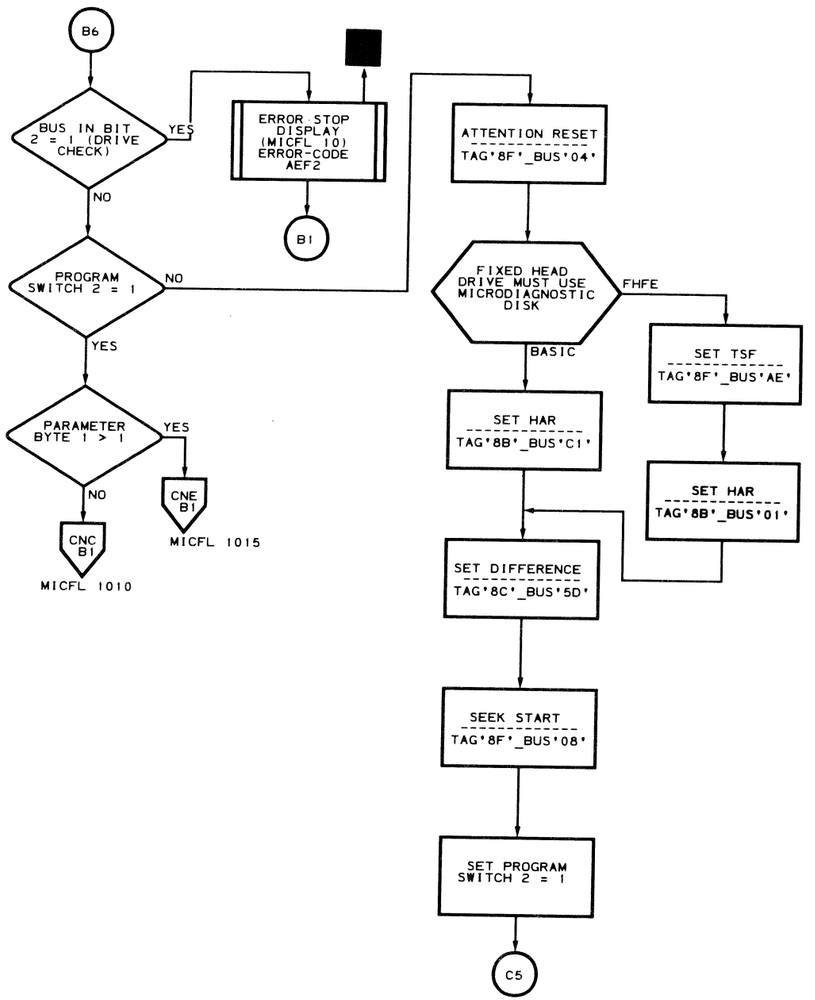
ERROR CORRECTION CODE (Routine AE)





CE1005 Seq.1 of 1	2747105 Part No.(N)

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74	440218 5 Aug 74	440223 14 Mar 75	440227 14 Sept 76

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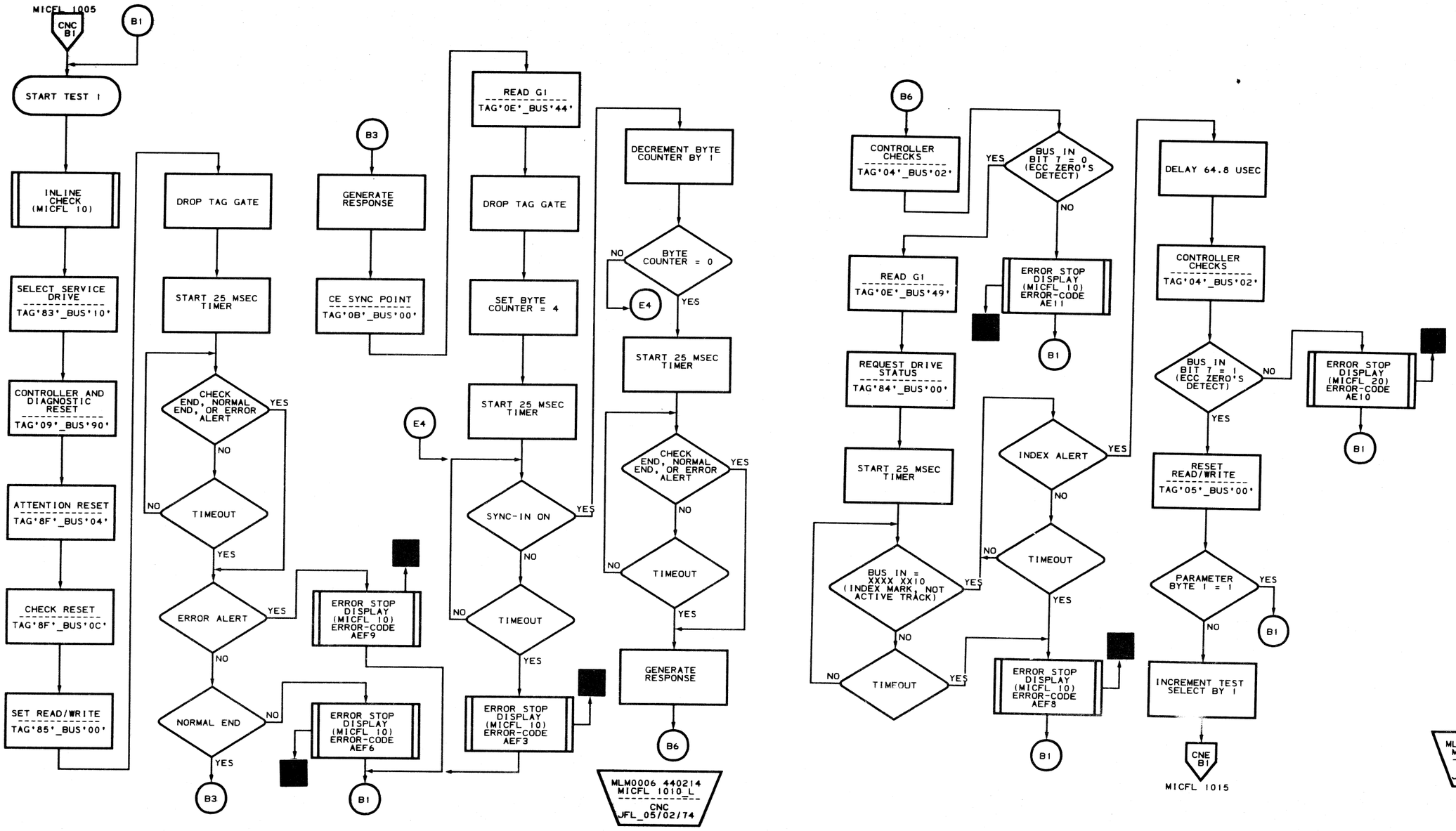
ECC DIAGNOSTIC (TEST 1 RESETS) (Routine AE)



CE1010 Seq. 1 of 2	2747106 Part No.( )

440200	440202	440203	440204	440214		
25 June 73	7 Sept 73	2 Nov 73	21 Dec 73	17 Jun 74		

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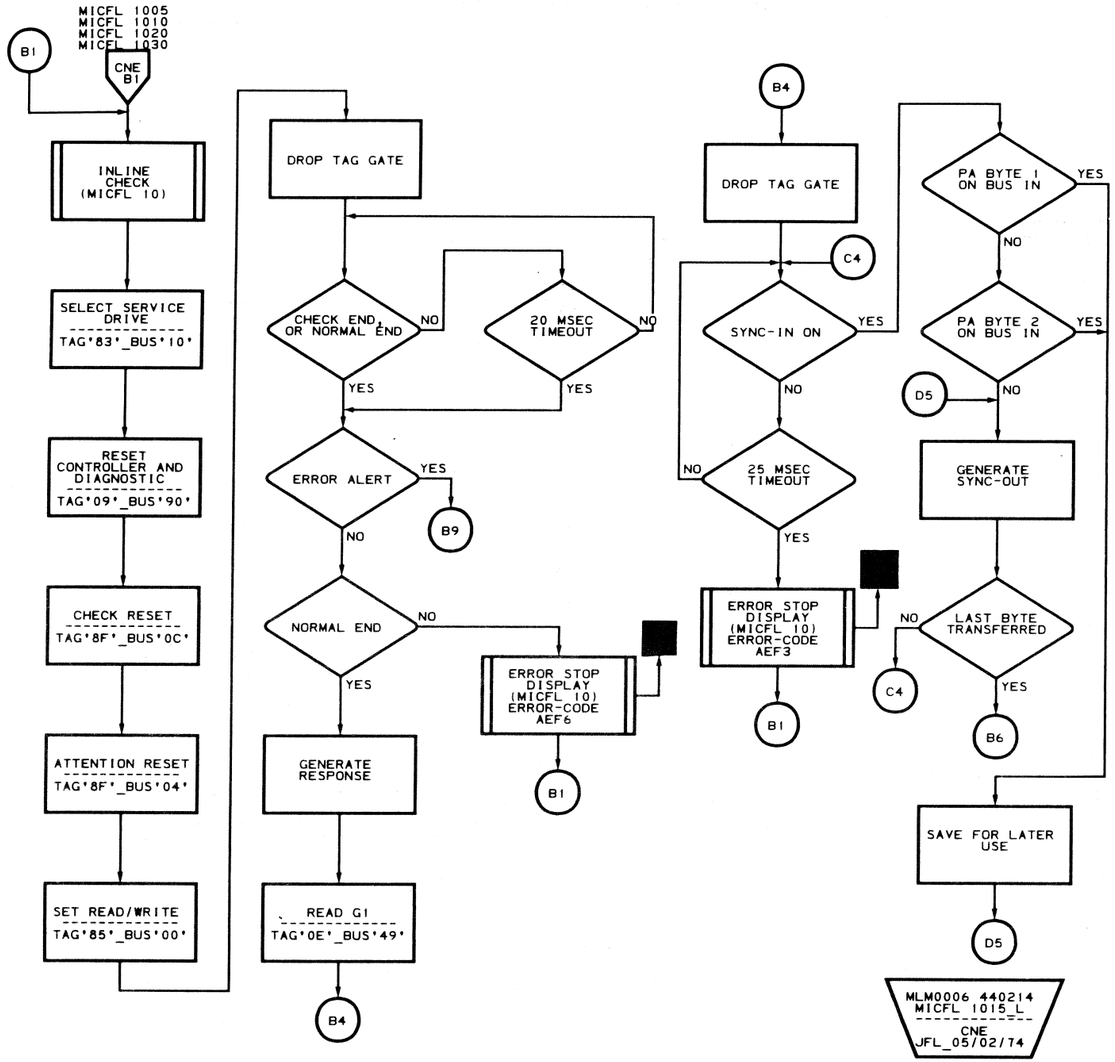

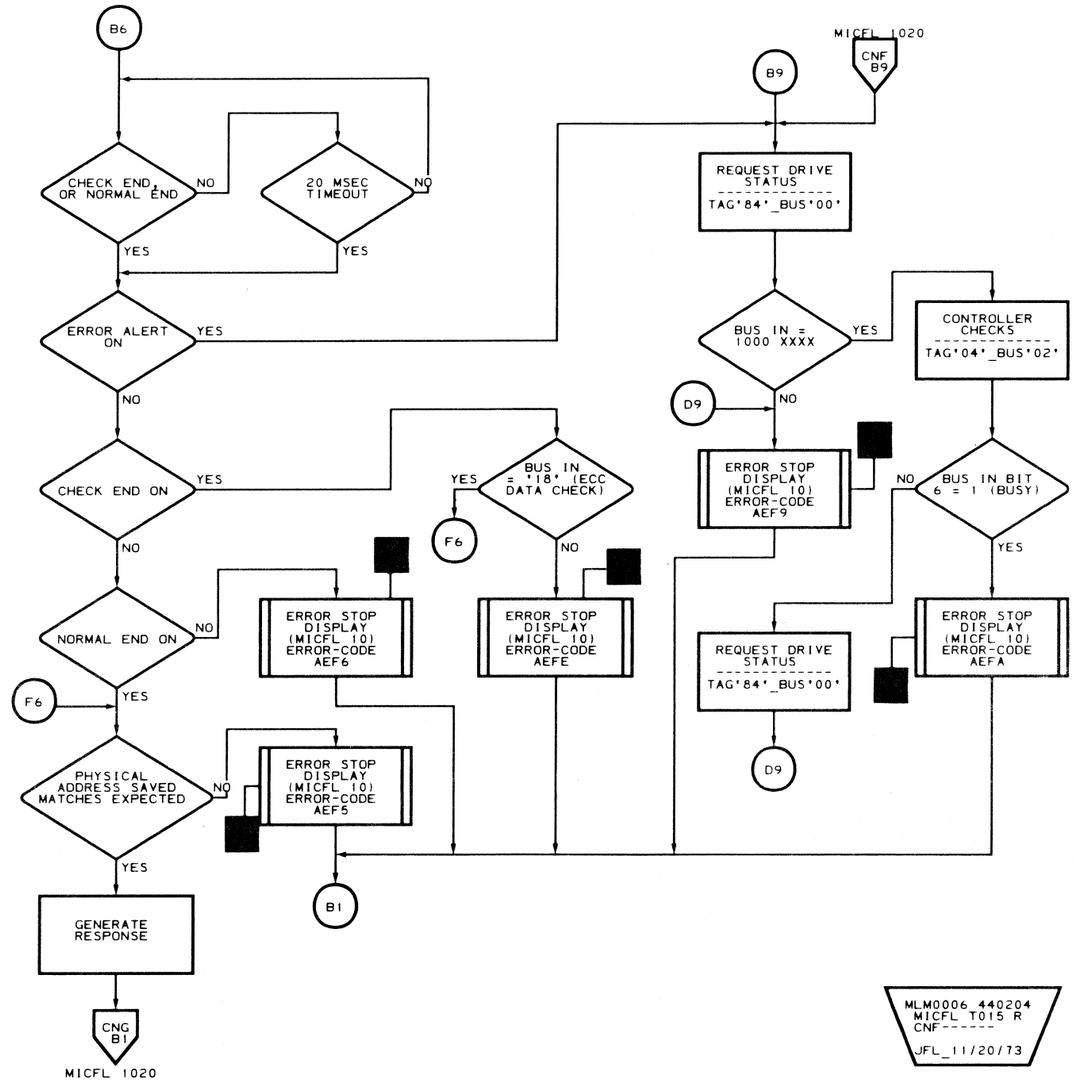

CE1010 Seq. 2 of 2	2747106 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440214 17 Jun 74		

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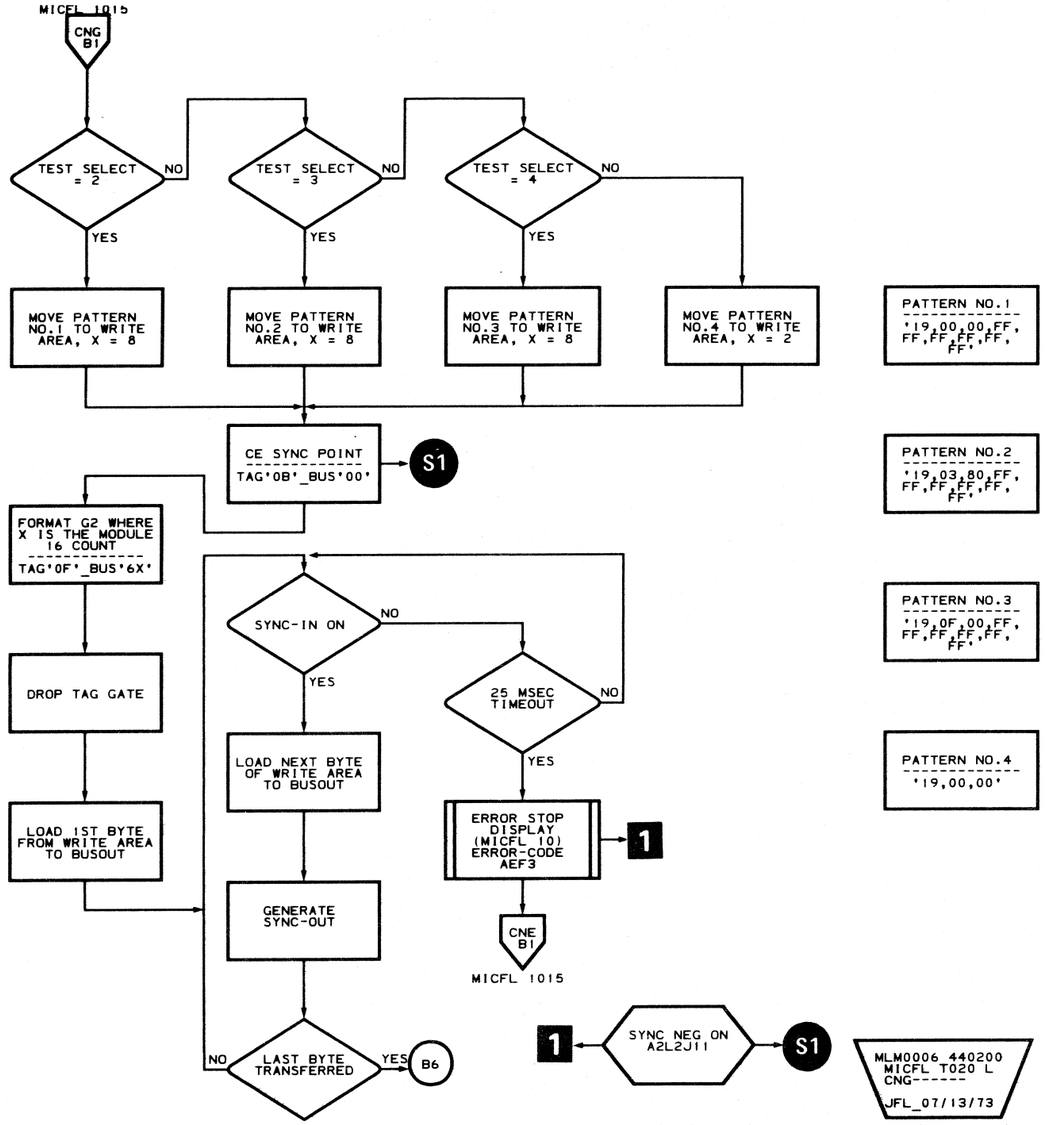
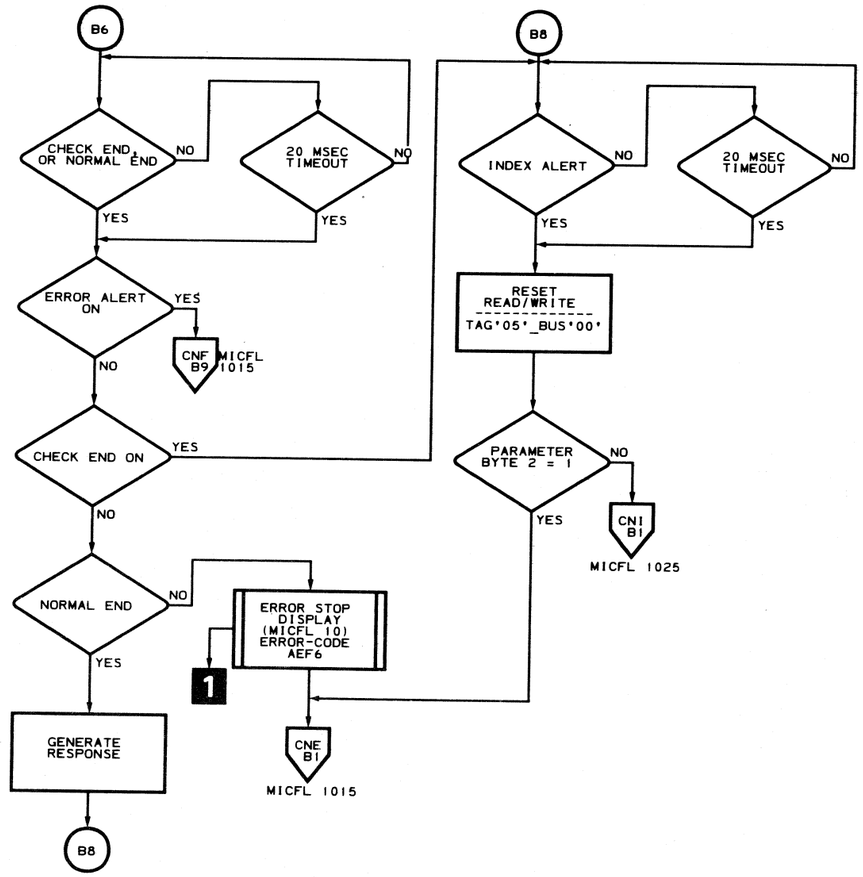
ECC DIAGNOSTIC (WRITE TEST PATTERNS) (Routine AE)





MLM0006 440214 MICFL 1020_R
CNH
JFL_05/02/74

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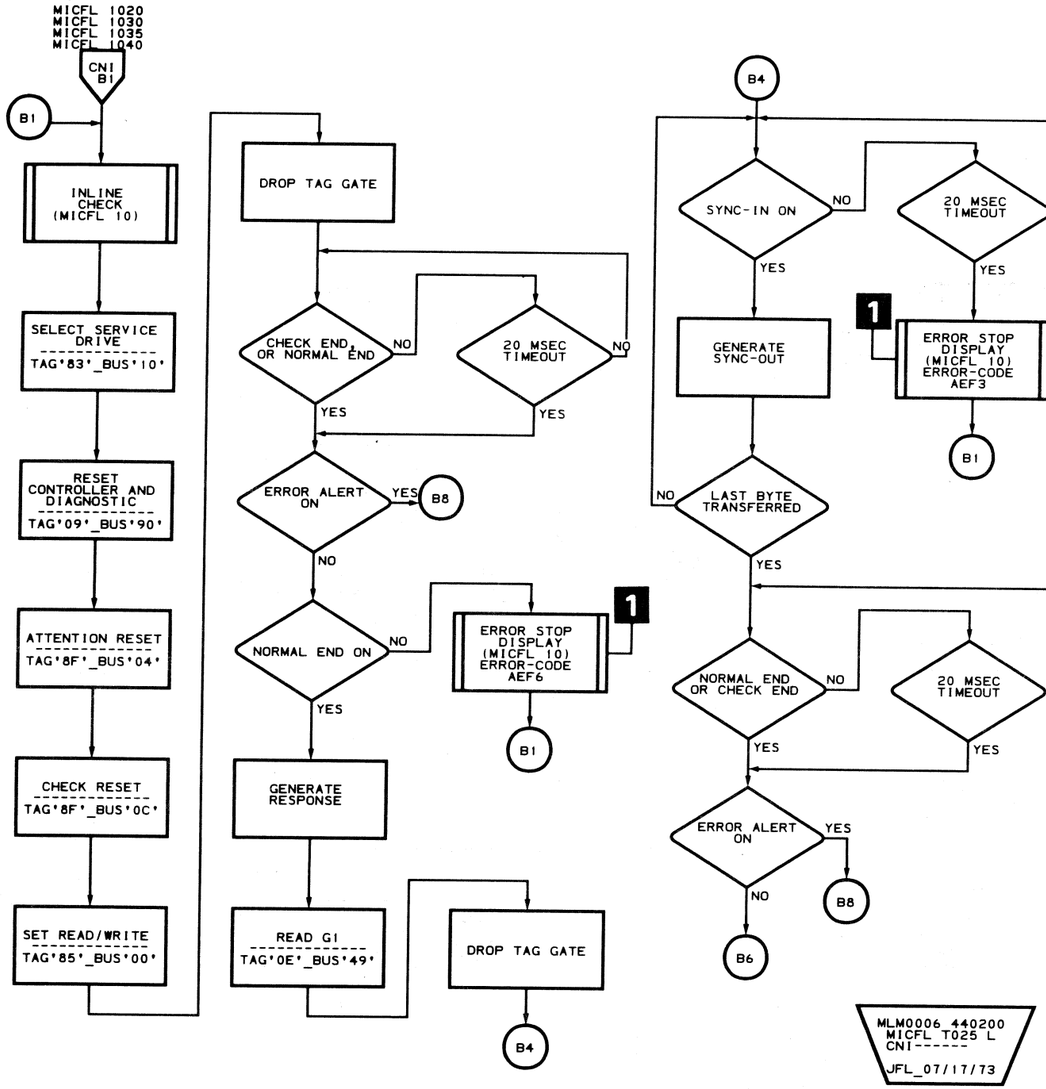
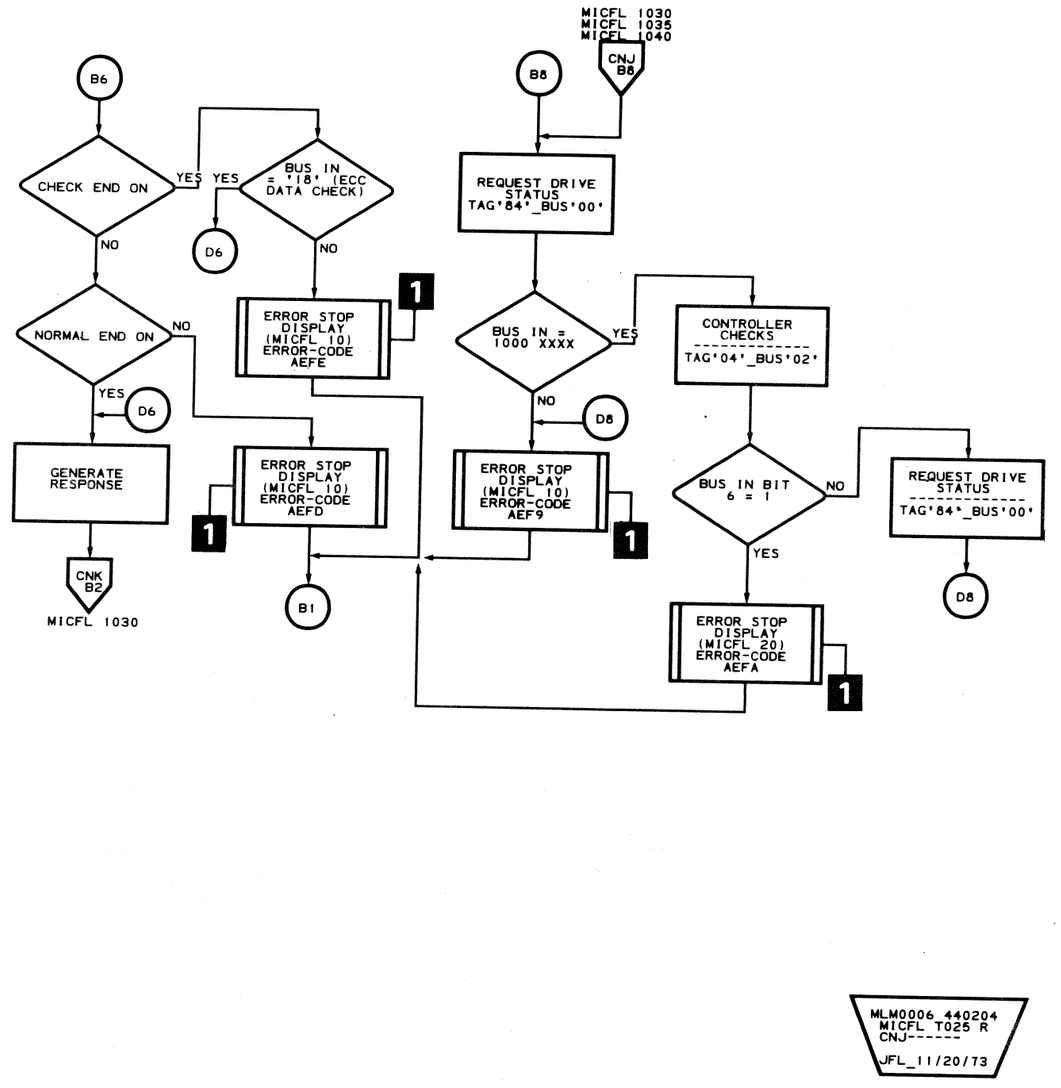
ECC DIAGNOSTIC (PRETEST–READ HA) (Routine AE)





CE1020 Seq. 2 of 2	2747107 Part No.( )

440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440214 17 Jun 74		

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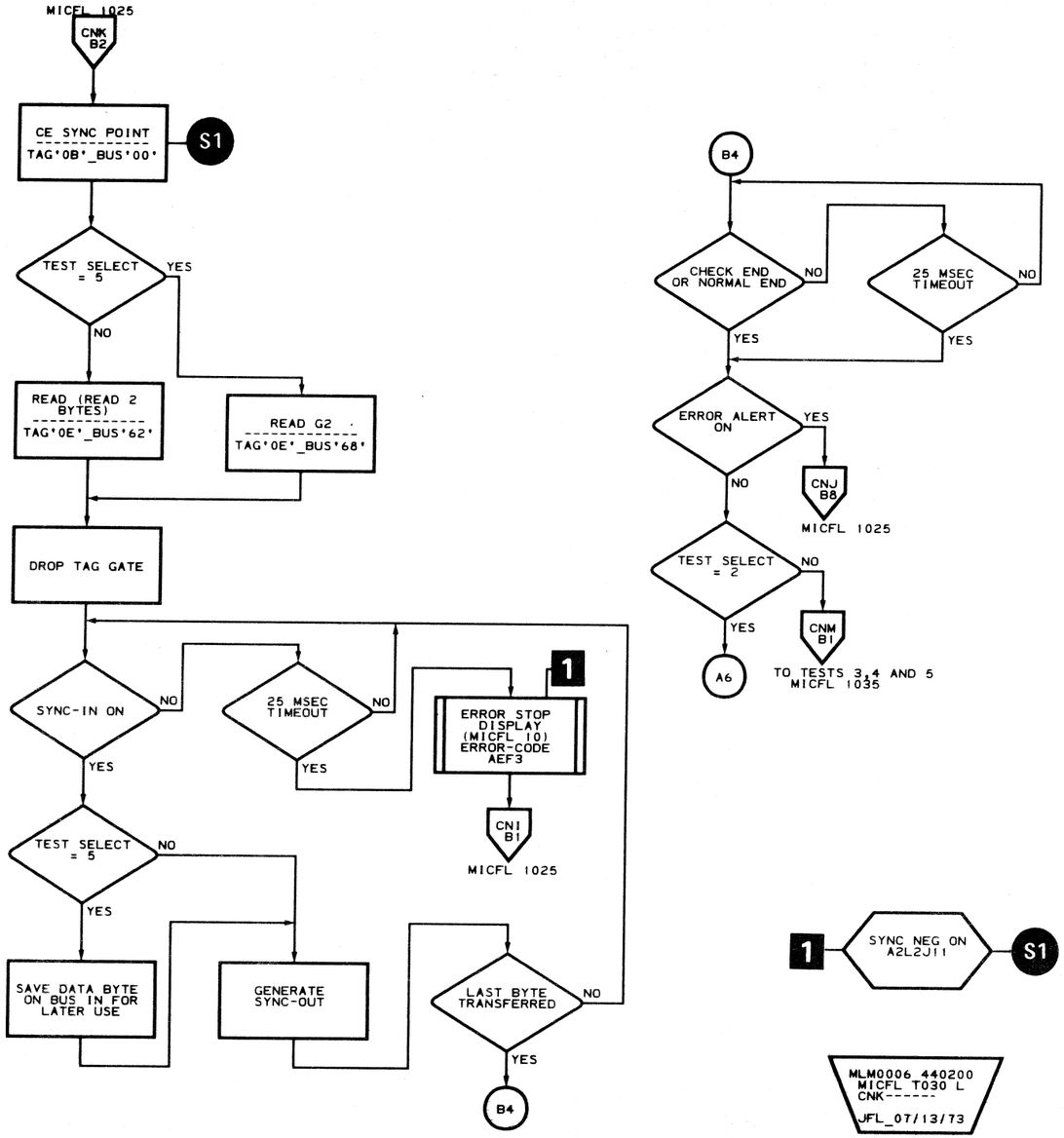
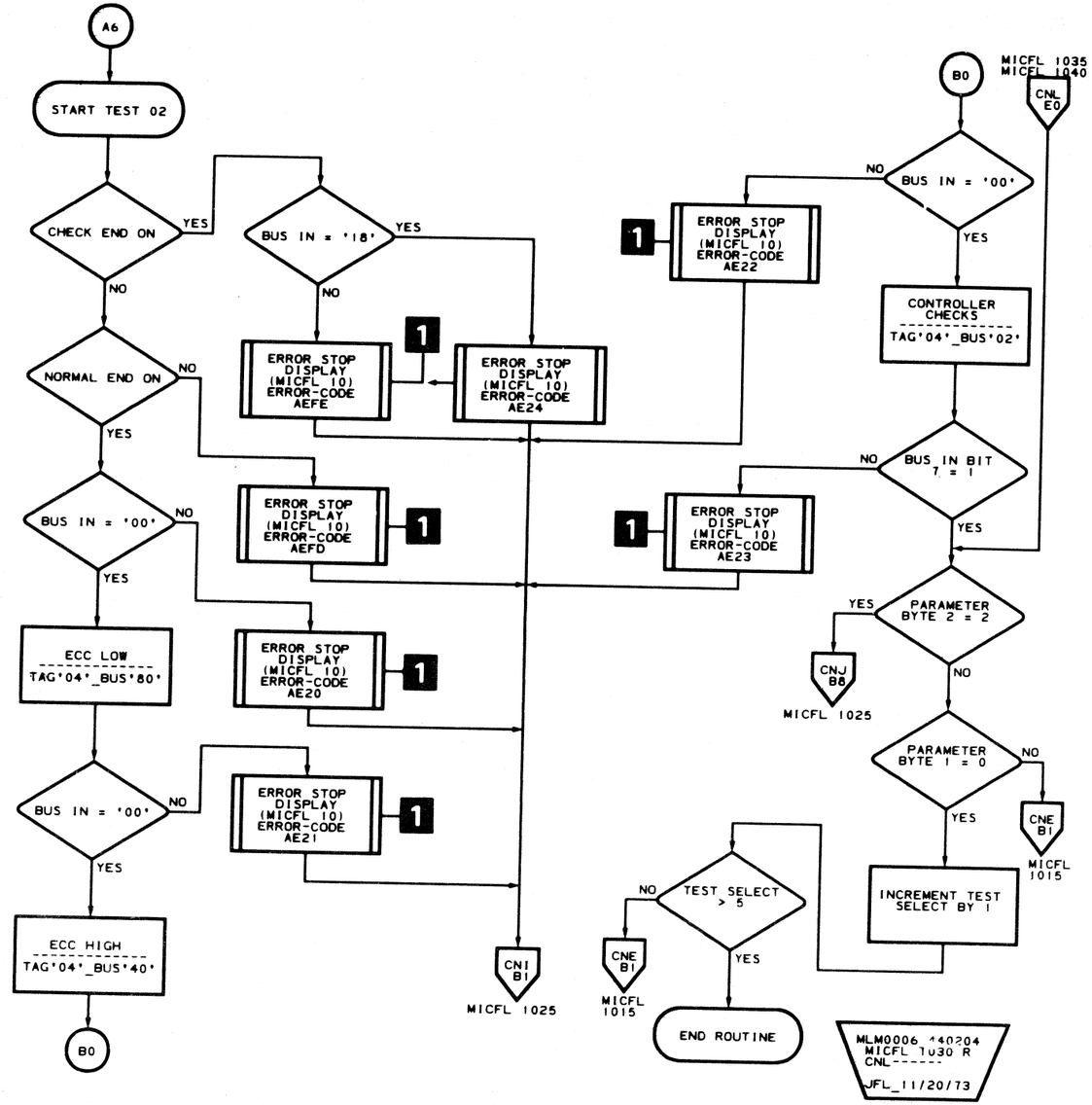
ECC DIAGNOSTIC (PRETEST READ TEST PATTERN) (Routine AE)





CE1030 Seq. 1 of 2	2747108 Part No.( )

440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440214 17 Jun 74		

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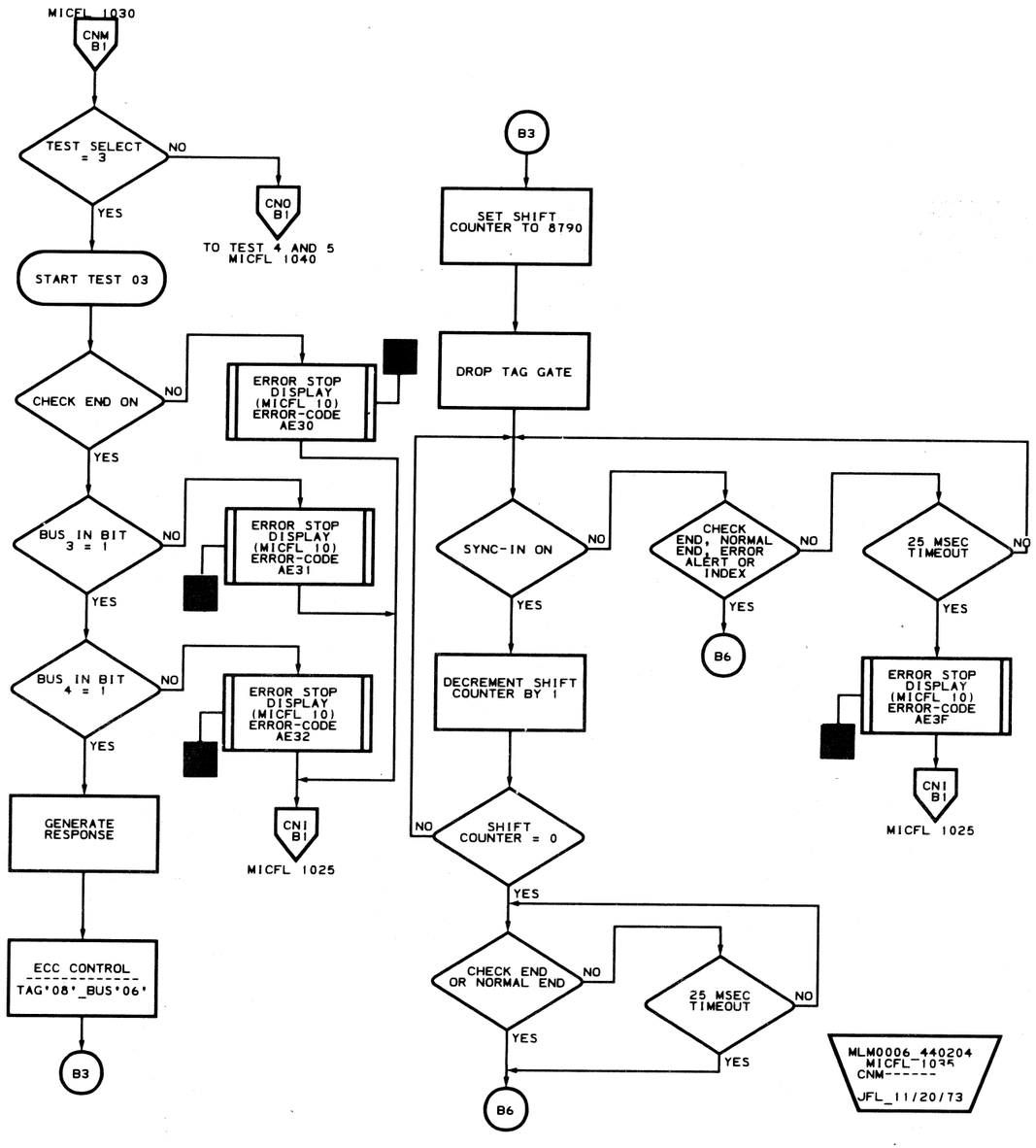

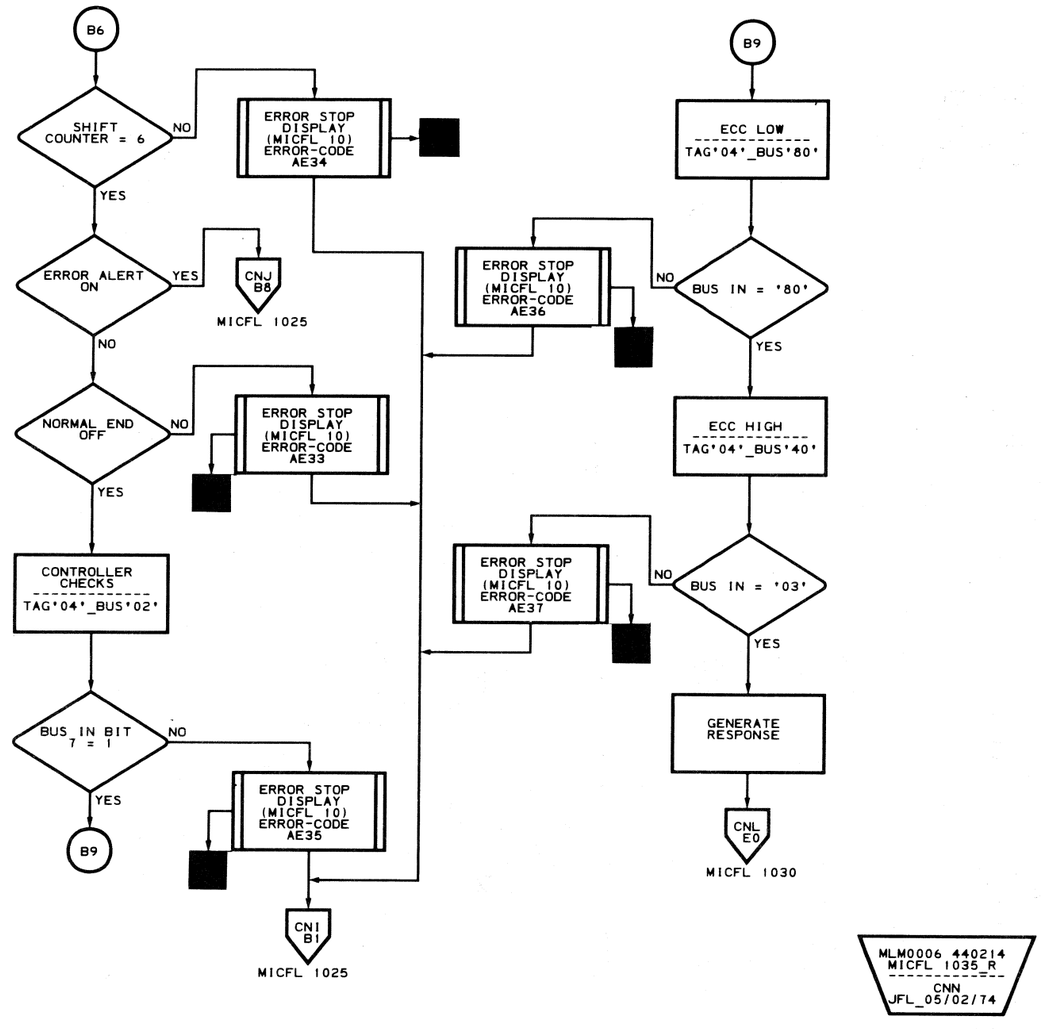

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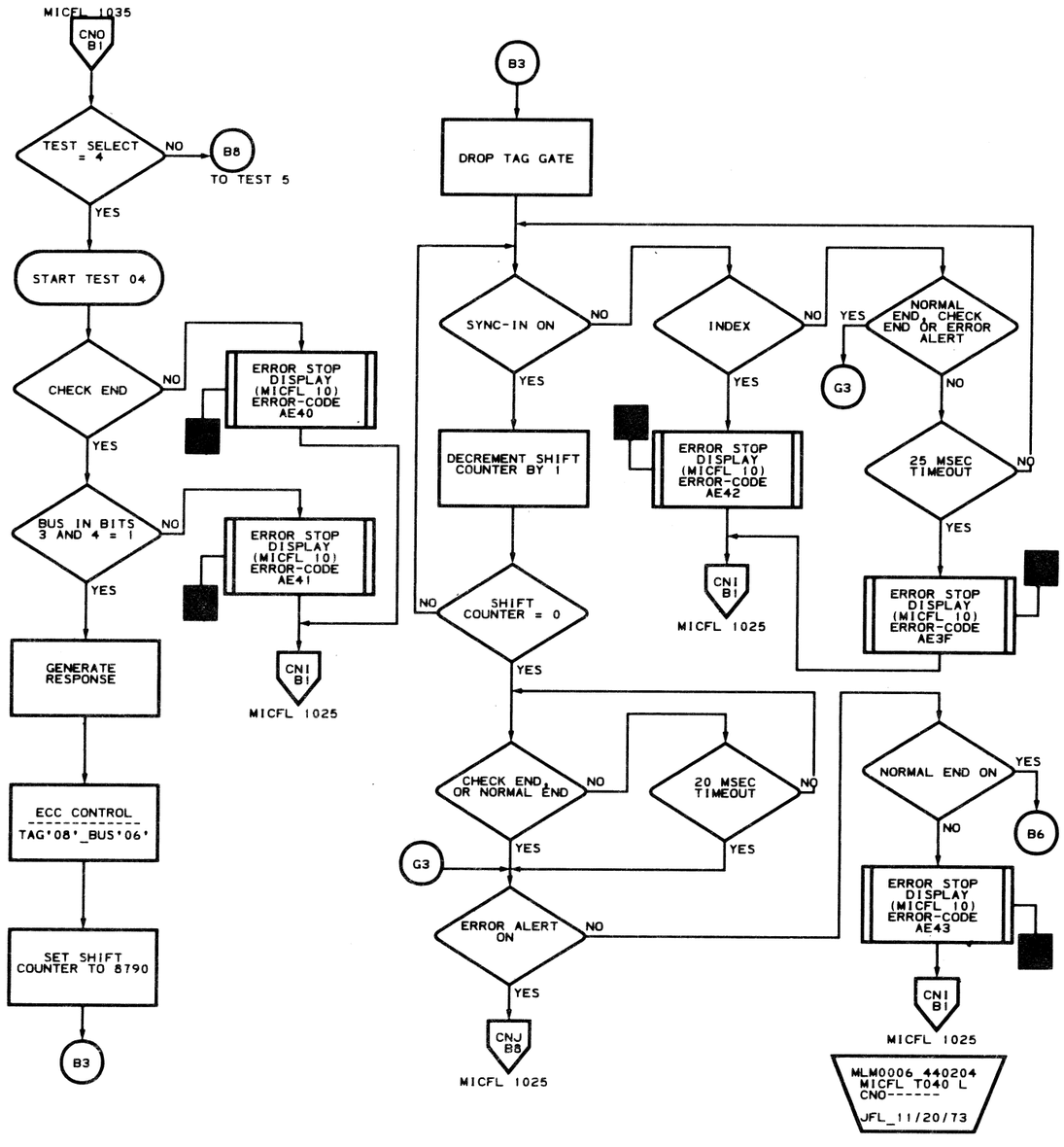
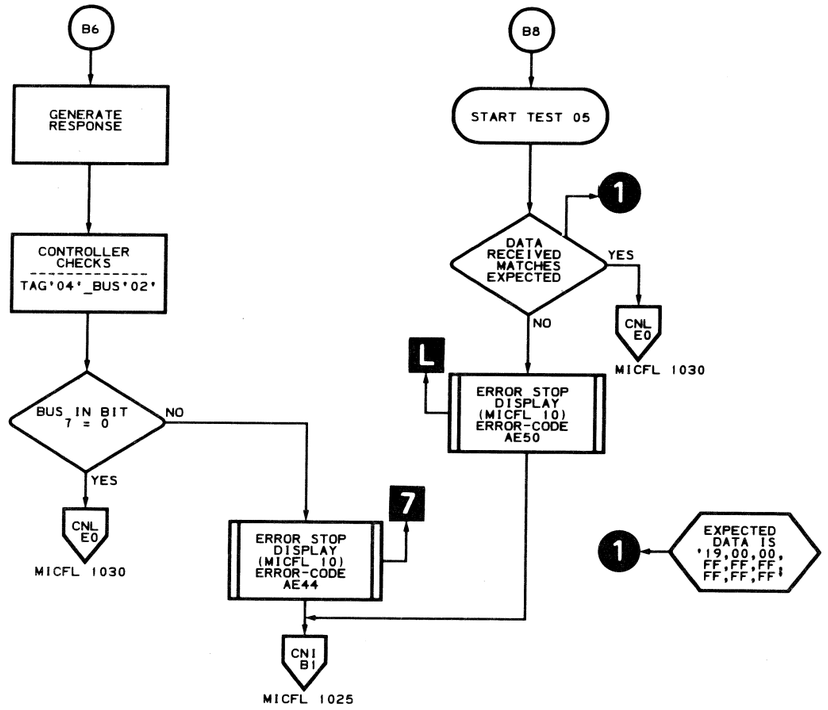
ECC DIAGNOSTIC (TESTS 4 AND 5) (Routine AE)





CE1040 Seq. 1of 1	2747109 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440214 17 Jun 74		

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ROUTINE AE TEST 2 SCOPING PROCEDURES

Test 2 writes a data field of 8 bytes consisting of '00 00 FF FF FF FF FF FF'. When read back with a byte count of two, the above pattern appears as 2 bytes of '00' with a correct ECC pattern.

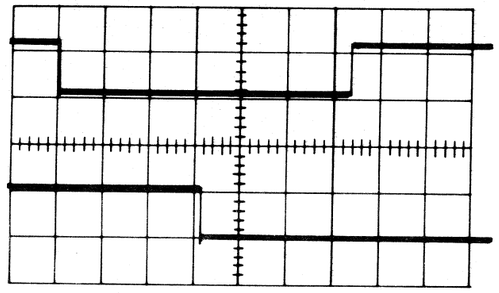
These pictures were taken while looping the write phase of Test 2. Enter: 'AE', '10', '02', '01', '01', '00'.

When assured that the Write phase is operating properly, proceed to the Read phase description on the next page.

– G2
A2Q2D05 (BH110)

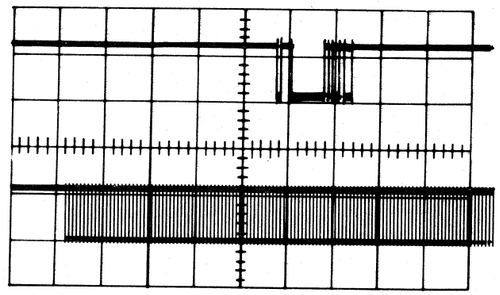
– Write Gate
A2Q2G10 (BH140)

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Vertical: 0.1 volt/div
Time: 10 μs/div



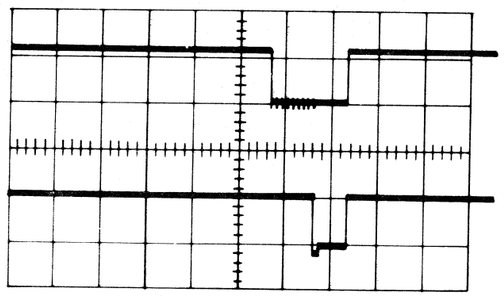
–SERDES Sr 5 Pwr
A2S2P05 (BC120)

– Wr Data TP
A2T2B04 (BJ130)



– Run ECC Ctrl.
A2P2S13 (BG170)

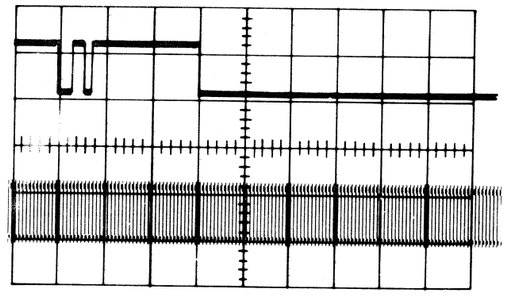
– Xfer ECC Ctrl.
A2P2G08 (BG170)



Setup as above using triggered delay on
– Run ECC Ctrl.
A2P2S13 (BG170) with delay time of 1 μs/div

–SERDES Sr 5 Pwr
A2S2P05 (BC120)
Data equal 19, 00, 00, FF...FF

– Wr Data TP
A2T2B04 (BJ130)



Note: When scoping, be aware that once an error is detected futher testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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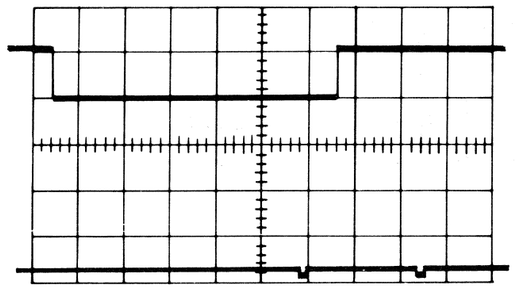
ROUTINE AE TEST 2 SCOPING PROCEDURES

The read phase reads back the information written during the write phase. The byte count is two. No bits shift into or out of the ECC Shift Register. Therefore, ECC Zeros Compare is continuously active.

These pictures show looping the read phase of test 2.
Enter: 'AE', '10', '02', '02', '01', '00'.

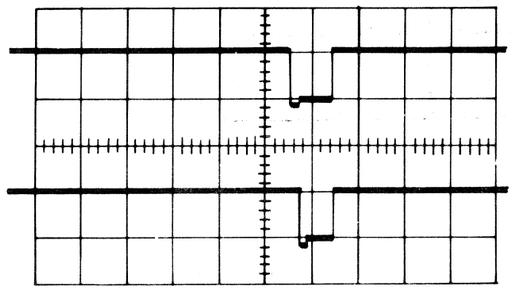
Sync Ext.(–): –RAS TP
A2L2J11 (BD100)
Vertical: 0.1 volts/div
Time: 10 μs/div

– G2
A2Q2D05 (BH110)



– Read Gate (– Level)
A2Q2P09 (BH140)

– Run ECC Control
A2P2S13 (BG170)

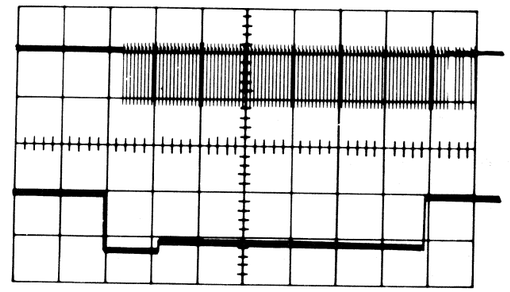


– Xfer ECC Control
A2P2G08 (BG170)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

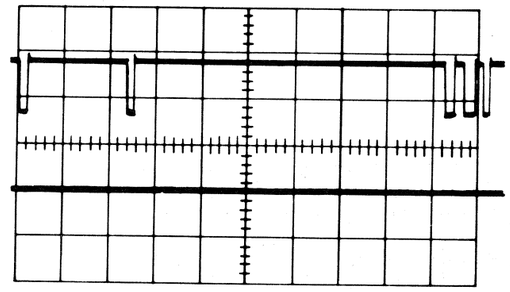
Set up as at left using triggered delay on – Run ECC Control (A2P2S13) with delay time of 1 μs/div.

–Standardize Data
A2T2G02 (BJ110)



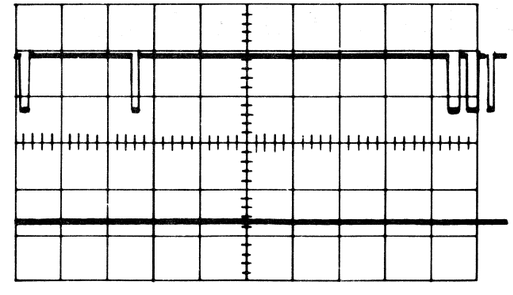
– Xfer ECC Control
A2P2G08 (BG170)

– ECC Ser Rd Data
A2S2P04 (BC150)
The first two pulses are switching spikes and not data



– FB 1 (+ level)
A2S2P11 (BC150)

– Change ECC Parity
A2S2M10 (BC150)
The first two pulses are switching spikes and not change parity signals.



– ECC Zeros Compare
(– Level)
A2S2U07 (BC150)

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ROUTINE AE TEST 3 SCOPING PROCEDURES

Test 3 writes a data field of 8 bytes consisting of '0380 FF FF FF FF FF FF'. When read back with a count of two, the above pattern appears as an ECC Data Check.

The first picture was taken while looping the Write phase of test 3. Enter: 'AE', '10', '03', '01', '01', '00'.

The other two pictures were taken during the Read Back phase of test 3. Enter 'AE', '10', '03', '02', '01', '00'.

Note: The various controls that affect this test, such as – G2, – Write Gate. The ECC Controls are the same as for Test 2.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

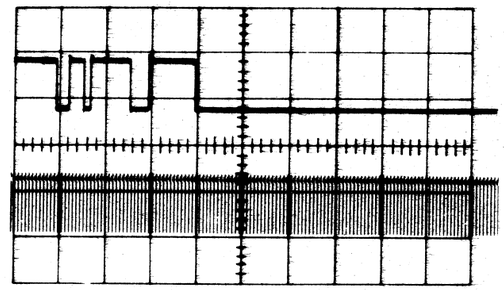
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Using triggered delayed sweep triggering on – Run ECC control A2P2S13 (BG170).

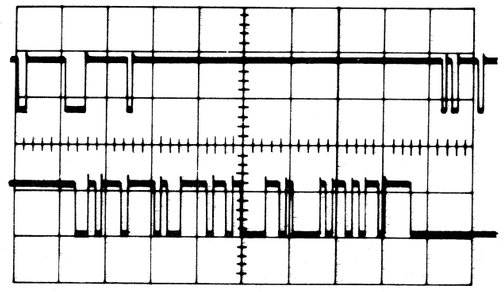
Delay time is 1 μs/div

–SERDES Sr 5 Pwr
A2S2P05 (BC120)

Data equals
190380 FF....FF

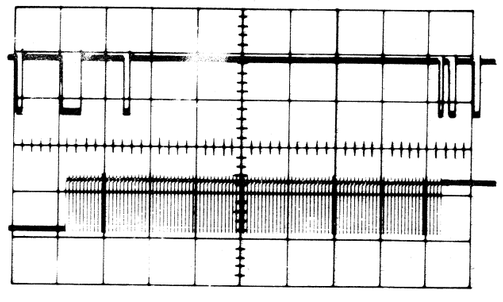


– Write Data TP
A2T2B04 (BJ130)



– ECC Ser Rd Data
A2S2P04 (BC150)

–FB 1
A2S2P11 (BC150)



– Change ECC Parity
A2S2M10 (BC150)

– ECC Zeros Compare
A2S2U07 (BC150)

Note that at the end of Read – ECC Zeros Compare is OFF. This condition causes an ECC Data Check.

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ROUTINE AE TEST 3 SCOPING PROCEDURES

Test 3 proceeds with an ECC Correct Operation. When using the data in this test, the Data Check is correctable.

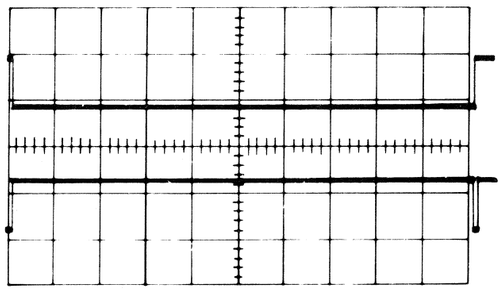
The picture below shows the proper duration of the Correct Operation. The intensified portion is shown expanded in the photos at right. Since the delayed sweep was not triggered, the timing varies somewhat (normally less than one division).

During the last 2 negative pulses of Status Bytes Op 04 the pattern bytes are on Bus In. The hex values should be '80' and '03', respectively.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div

Time: 1 ms/div with A intensified during B.
Delay time is 10 μs/div.

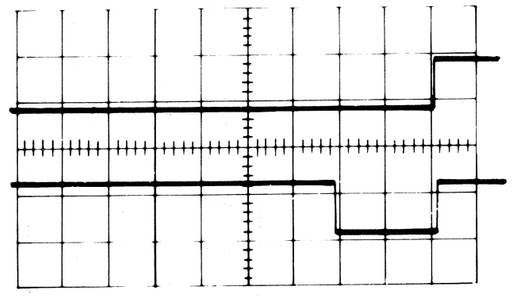


– ECC Correct Op
A2P2S12 (BG170)

– ECC Zeros Compare
A2S2U07 (BC150)

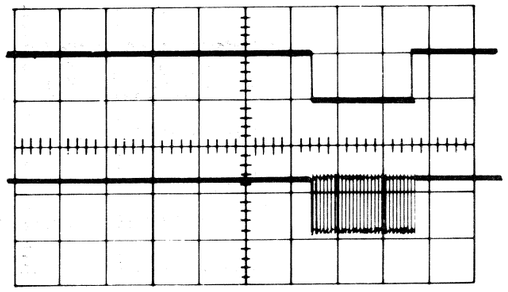
Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

– ECC Correct Op
A2P2S12 (BG170)



– ECC Zeros Compare
A2S2U07 (BC150)

– Freeze Correct Op
A2S2P03 (BC150)

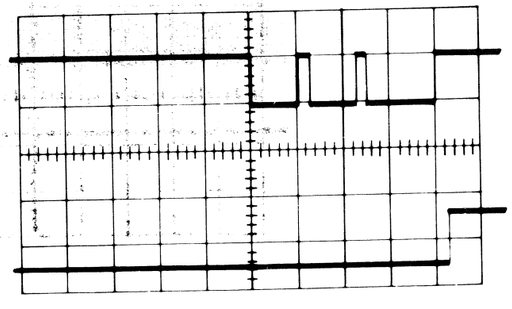


– Index Alert
A2Q2J11 (BH150)

– Status Bytes Op 04
A2G2G03 (BF110)

Adjust the delay time multiplier to obtain this timing.

– Trk Ovrn * ECC Data Check
A2Q2J05 (BH140)



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ROUTINE AE TEST 4 SCOPING PROCEDURES

Test 4 writes a data field of 8 bytes consisting of '0F 00 FF...FF'. When read back with a byte count of 2, an Uncorrectable Data Check should result.

The picture below shows the generation of the record used for this test.

The pictures at right show the read back controls.

The ECC Correct Op ends with a Normal End indicating that the Data Check is uncorrectable.

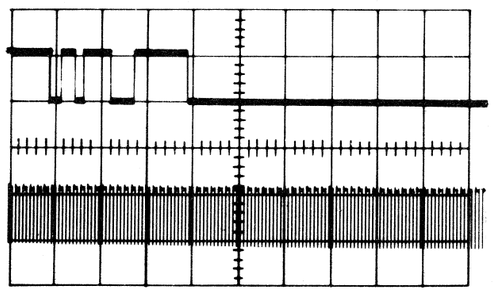
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

Time: 10 μs/div

–SERDES Sr 5 Pwr
A2S2P05 (BC120)

– Wr Data TP
A2T2B04 (BJ130)

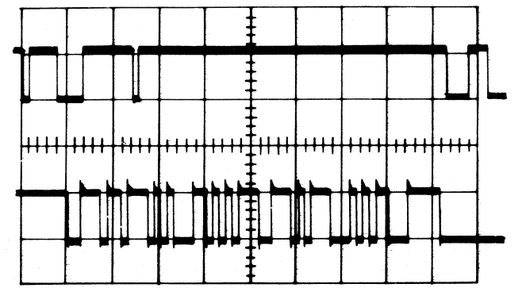


Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

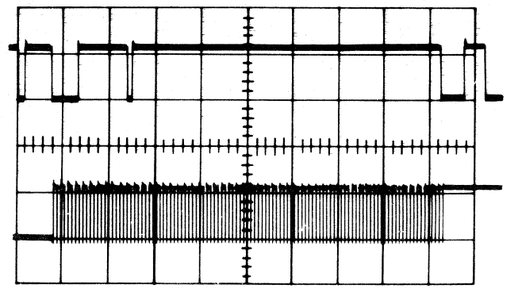
–ECC Ser Rd Data
A2S2P04 (BC150)

Data: 0F00 FFFF ....FF
Ignore the two small pulses

– FB 1
A2S2P11 (BC150)



– Change ECC Parity
A2S2M10 (BC150)



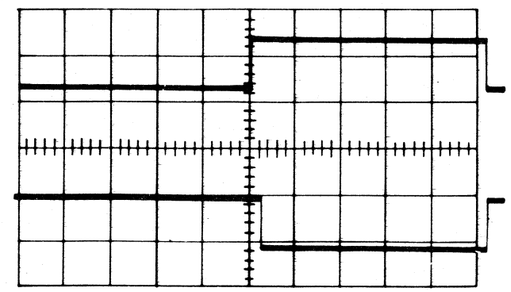
–ECC Zeros Compare
A2S2U07 (BC150)

Note that the operation ends with no ECC zeros. This constitutes an ECC data check. An ECC correct op follows.

Time: 2 ms/div

– ECC Correct Op
A2P2S12 (BG170)

– ECC Zeros Compare
A2S2U07 (BC150)



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UNTIL DECEMBER 1973

ROUTINE AE TEST 5 SCOPING PROCEDURES

Test 5 writes 2 bytes of data. The data bytes equal '00' '00'. The machine writes the check characters normally. During the Read phase a byte count of 8 is used so the data byte and the check characters are transmitted to the storage control for a bit-by-bit examination. ECC Data Check at the end is ignored.

The picture below shows some key points in the generation of the record. To loop enter: 'AE', '10', '05', '01', '01', '00'.

The pictures at right show some key points in the Read phase. To loop enter: 'AE', '10', '05', '02', '01', '00'.

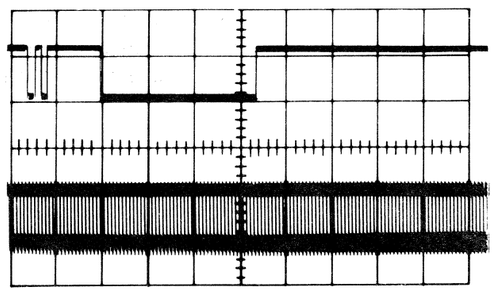
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

Time: 10 μs/div using triggered delayed sweep triggering on – Run ECC Control. A2P2S13 (BG170).

Delay time: 2 μs/div

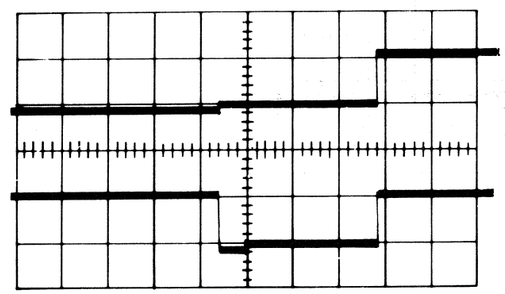
–SERDES Sr 5 Pwr
A2S2P05 (BC 120)
Note: 19 00 00 FF... FF



– Wr Data TP
A2T2B04 (BJ130)

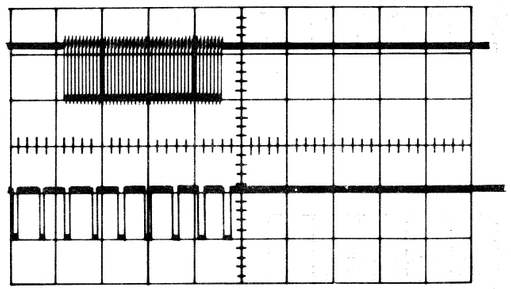
Setup: Same as left

–Run ECC Control
A2P2S13 (BG170)



–Xfer ECC Control
A2P2G08 (BG170)

– Standardized Data
A2T2G02 (BJ110)



– Sync In
A2S2U10 (BC170)

Sync in pulses 2 through 9 strobe data on Bus In.
The data equal '00 00 FF... FF'.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE AE TEST 5
SCOPING PROCEDURES
MICFL 1059

ROUTINE AF – FORMAT READ/WRITE TESTS

DESCRIPTION

Routine AF, which checks the hardware associated with Read and Write commands, consists of 15 tests ('01' through '0F'). In normal operation (default Parameter 1 = '00'), all tests are executed in sequence.

Optional parameter entry may be used to restrict operation to a single test. If a single test is selected, it loops indefinitely until halted by the CE or an error halt occurs.

All tests use physical cylinder 349, Physical Head 0, odd track, with the exception of the initial seek verification (Read G1), which uses Physical Head 1, even track, of the same cylinder.

Test ALL Initialization

Prior to the start of any of the tests, this step verifies that the CE parameter 1 entry is valid. The routine verifies that the CE drive is Online and Write Enabled. It initiates a Rezero operation, verifies that the drive becomes Busy, and that normal completion of the operation occurs within 300 milliseconds. The routine initiates a series of 349 cylinder seek operations (head 01 selected), checks for normal completion of the operation within 10 milliseconds, and checks for drive status after each operation to include: No Drive Check, No Busy, and Seek Complete.

The routine verifies that Index and Active Track are present within 21 milliseconds. If Index and Active Track are present, the routine attempts to verify that the seek to the CE cylinder was performed correctly by reading Home Address from the Read Only track at head 02. It then compares Bytes PA1 and PA2 for validity. If the comparison is successful, the routine logs out an appropriate error message. The CE has the option of retrying the verification (by entering '00' to retry) or bypassing further verification of the Seek operation and going direclty to the specified test through use of parameter 2.

Note: Extreme caution must be used in exercising the option to continue the tests. It is possible to destroy customer data if a hardware malfunction occurs that prevents successful Seek operation.

If the routine cannot successfully verify head position with a Read G1 (Home Address) operation, the password parameter allows the CE to bypass the seek verification and continue the Write G1 test for restoration of the Home Address.

Note: This password parameter must be used very carefully and only when there is no possibility of destroying customer data. The pack must be Backed Up by the customer.

If all criteria for restrictive use of parameter 2 are met, restart Routine AF by inserting Parameter 1 = Test number (format Write G1 Test = '0E') and Parameter 2 = Password (Valid Password = '5D').

The routine executes the Seek and Verify operations and the Stopping with Error command indicates that the verification failed. Enter '00'; this forces the routine to reset the HAR = 01. Continue to the selected test. After the G1 (HA) field is successfully restored, the CE must manually stop Test '0E', restart routine 'AF', and specify the desired (or default) test. If parameters are entered by the CE, Parameter 2 should be set to '00' (default), which gives maximum protection against inadvertent destruction of customer data.

Test 01. Read G1 Unoriented Status, Read and Verify Home Address Physical Address Bytes

Test 01 verifies that Read G1 Unoriented status is not on continuously by orienting on Index and Active Track, then initiating a Read G1 operation, looking for Bus In bit 6 = 0 while Tag Gate is active. The test initiates a Read G1 operation and checks the 4th and 5th bytes for '5D' and '41', respectively (Cylinder 349 head 01). The test also verifies that Read G1 Unoriented can be set on by initiating another Read G1 after orientation has been lost and checking for the unoriented status condition on Bus In with Tag Valid status.

Test 02. Oriented/Unoriented Borderline

Test 02 attempts to locate the borderline between Oriented and Unoriented by initiating a Read G1 operation. It delays a maximum allowable time without losing orientation (50 microseconds), then initiates a Read G2 operation, and checks for no Command Overrun and no Unoriented status.

The test repeats the above sequence of events using a delay large enough to force loss of orientation (54 microseconds) and checks for Command Overrun ending status.

Test 03. Force Command Overrun and Check End

Test 03 forces Command Overrun in both Read and Write modes by orienting on Index and Active Track. It then initiates a Write G2 operation (with the Diagnostic Inhibit Write Gate Mode active) and checks for a Check End response with Command Overrun ending status.

The test orients again and initiates a Read G2 operation and looks for Check End response with Command Overrun ending status.

Test 04. Force Sync Out Timing Error and Force Status Overrun Error

Test 04 forces a Sync Out timing error by initiating a Write G1 operation (with Diagnostic Inhibit Write Gate mode active). It responds to only the first Sync In (inhibits Sync Out) and checks for a Check End response with Sync Out timing error ending status.

This test checks that Status Overrun can be set on by initiating a Write G2 operation, holding Tag Gate active for 100 microseconds, then looking for Bus In bit 4 = 1. The test then drops Tag Gate and looks for Bus In bit 4 = 0.

Test 05. Allow Head Address Register (HAR) and Transfer Sector Counter

Test 05 examines the Allow HAR function during Transfer Sector Counter and Read/Write mode of operation.

Set HAR = '00'.
Sense HAR, check that HAR = '00'.
Set Read/Write.
Orient on Active Track Index.
Wait approximately 20 microseconds (into the center region of the Allow HAR window).
Set HAR = '01'.
Wait approximately 100 microseconds (beyond the Allow HAR window).
Initiate a set HAR = '02' operation and reset Read/Write.
The test performs a sense HAR and checks for HAR = '01'
If HAR does not = '01', an error has occurred.
If HAR = '00', HAR failed to set within the Allow HAR window.
If HAR = '02', the HAR was allowed to set outside the Allow HAR window during Read/Write mode.

The test verifies that the Transfer Sector Counter logic works properly by setting the Target Register to '7F', then initiating a dummy Read G1 operation. It then checks the Target Register for a value of '80' (RPS = 1, Sector = 00).

Test 06. Write Full Track G2 Field

Test 06 clocks through the HAR (G1) field, initiates a Write G2 operation and writes a full track (R0 count field) of 8631 bytes. The test checks for no Error Alert and no Check End response after each operation.

Test 07. Write G2, Force Track Overrun

Test 07 clocks through the HA (G1) field, initiates a Write G2 operation and then initiates a Write G2 operation of greater-than-maximum track capacity (8832 bytes). The test checks for no Error Alert and Check End response with Track Overrun ending status following the Write G2 operation.

Test 08. Write G2/Format Write G2

Test 08 clocks through the HA (G1) field, initiates a Write G2 operation followed by a Format Write G2 operation. The test looks for no Error Alert and no Check End response following each operation. After the end response is received following the Format G2 operation, the test waits 5 milliseconds, reads drive status, and checks for I Write Sense (Bit 5) = 1. The test initiates a Reset Read/Write operation, again reads drive status, and checks for I Write Sense = 0.

Test 09. Read G2/Clock G2, Force No Sync Found

Note: Test 09 depends upon successful completion of Test 08.

Test 09 clocks through the HA (G1) field, initiates a Read G2 operation and checks for no Error Alert and no Check End response. The test then initiates a Clock G2 operation and checks for no Error Alert and no Check End response. The test then initiates a Read G2 operation on a non-existent G2 field, checks for no Error Alert and a Check End response with no Sync Found ending status.

Test 0A. Format Write G3/Read G3

Test 0A clocks through the HA (G1) field, initiates a Format Write G3 operation and checks for no Error Alert and no Check End response. The test again clocks through the HA field, initiates a Read G3 operation, reading the G3 field just written, and checks for no Error Alert and no Check End response.

Test 0B. Clock G3/Read G3 Address Mark Search

Note: Test 0B depends upon successful completion of Test 0A.

Test 0B clocks through the HA (G1) field, initiates a Clock G3 operation, reads the G3 field written by the previous test, and checks for no Check End response. The test again clocks through the HA field, initiates a Read G3 AM search operation, and checks for no Check End response.

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ROUTINE AF – FORMAT READ/WRITE TESTS

Test 0C. Format Erase, Force No Address Mark Found

Test 0C clocks through the HA (G1) field, initiates a Format Erase operation, and checks for no Error Alert and no Check End response. The test again clocks through the HA field, initiates a Read G3 AM Search operation, and checks for Check End response with No Address Mark Found ending status.

Test 0D. Special Format Write G1/Read G1

Test 0D initiates a Special Format Write G1 operation and checks for no Error Alert and no Check End response. The test writes a valid G1, including a logical cylinder number and head number based on data module size.

The test initiates a Read G1 operation, to read the G1 field just written, and checks for no Error Alert and no Check End response.

Test 0E. Format Write G1/Read G1

Test 0E initiates a Format Write G1 operation and checks for no Error Alert and no Check End response. The test writes a valid G1 including a logical cylinder number and head number based on data module size.

The test initiates a Read G1 operation and checks for no Error Alert and no Check End response.

Test 0F. Skip Displacement Fields
Format Reorient
Special Write G2
Special Read G2
Special Write G4
Read G4

Test 0F ensures that a record can be written and read with an embedded G4 gap (simulating a defect within a data field). It ensures that a G3 record is on the track by clocking through the HA (G1) field, initiating a Format Write G3 operation, and checking for no Error Alert and no Check End response.

The test writes a data record around the simulated defect by initiating the following operations which check for no Error Alert and no Check End response after each operation:

Read G1, Read G3, Format Reorient, Format G3, Special Write G2, and Special Format G4.

The test attempts to read back the record just written by initiating the following operations and checks for no Error Alert and no Check End following each operation:

Read G1, Read G3, Special Read G2, and Read G4.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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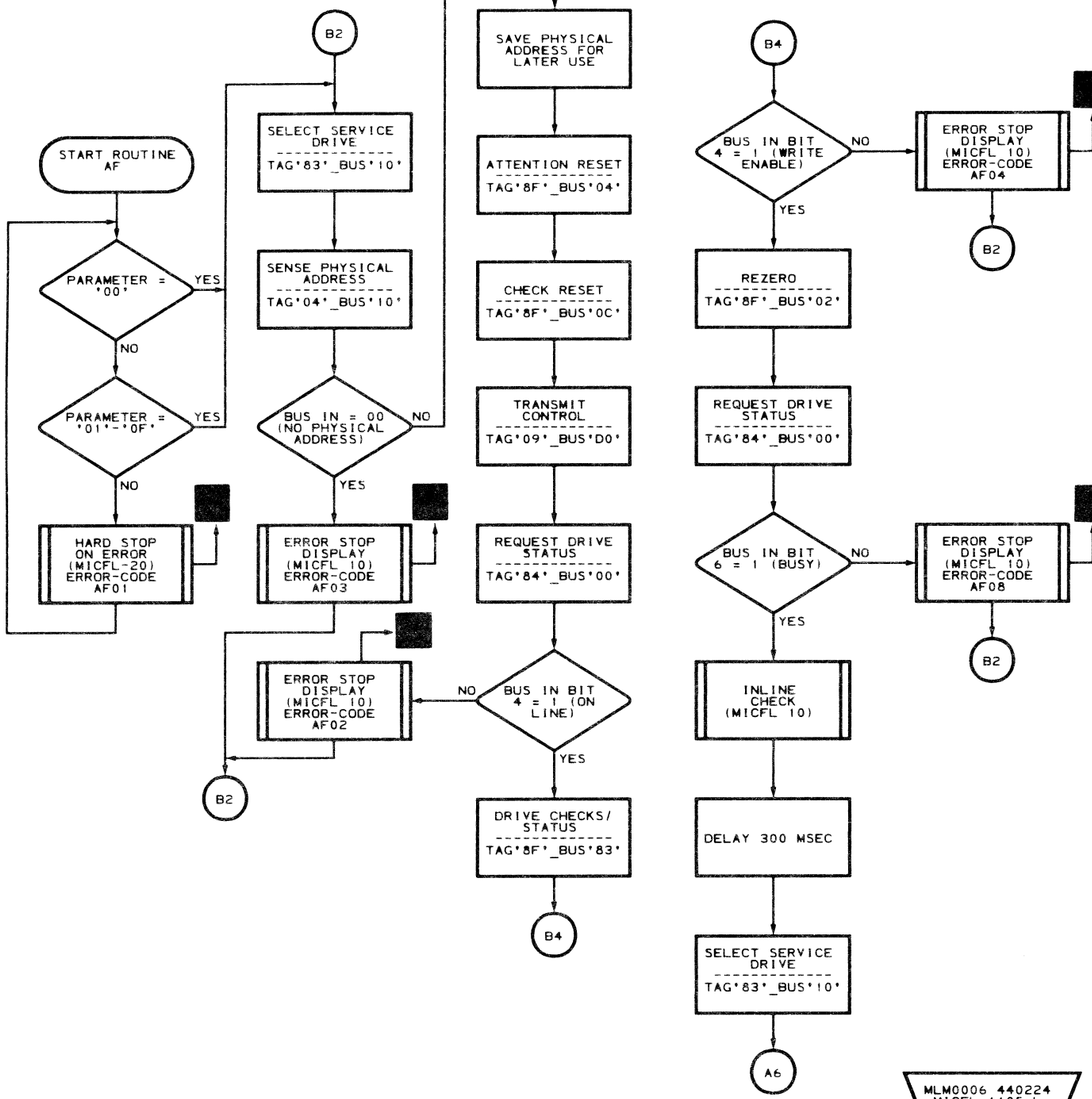
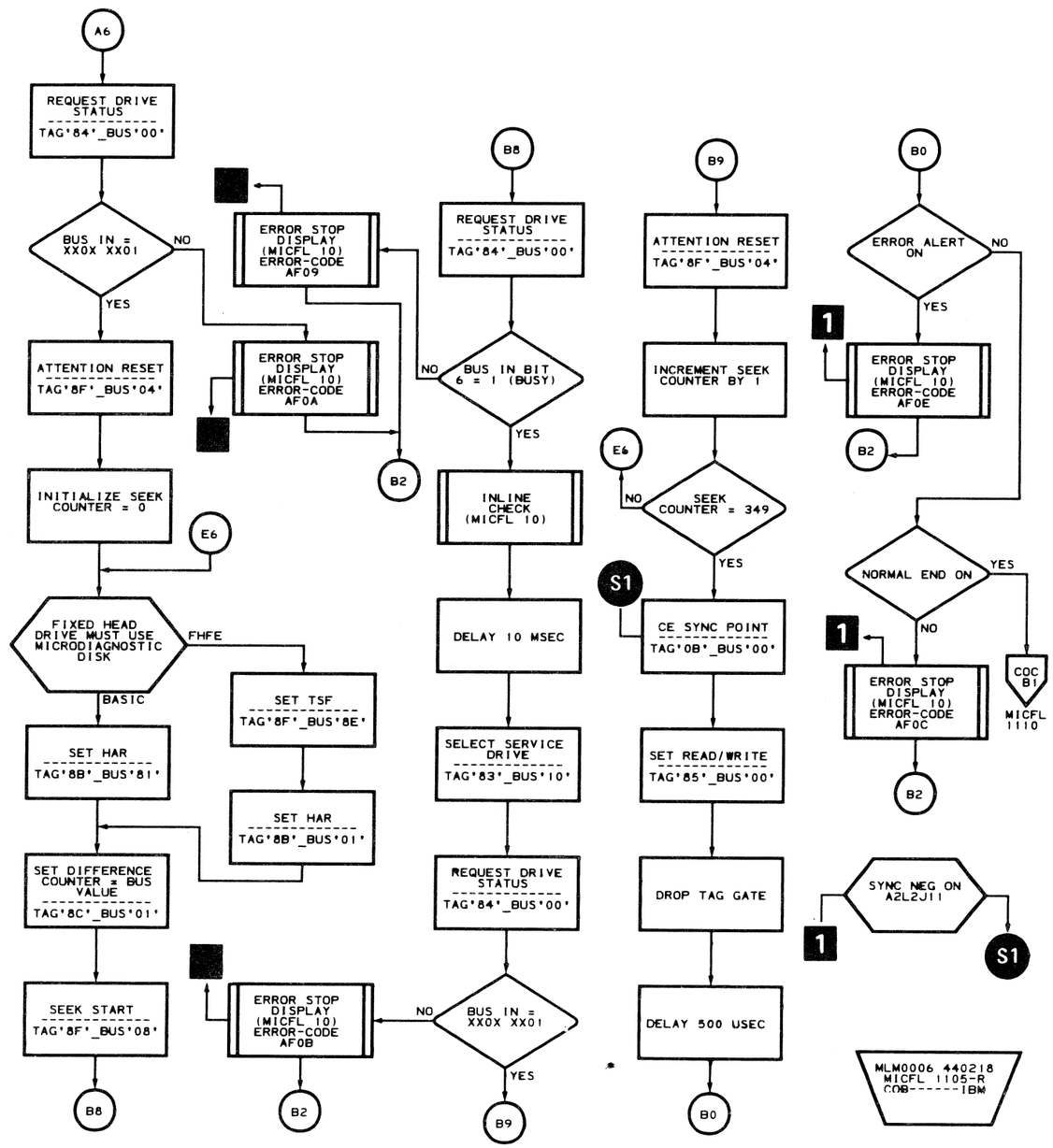
FORMAT READ/WRITE TEST (Routine AF)





CG1105 Seq.1 of 1	2747110 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440214 17 Jun 74	440218 5 Aug 74	440223 14 Mar 75	440224 15 Dec 75

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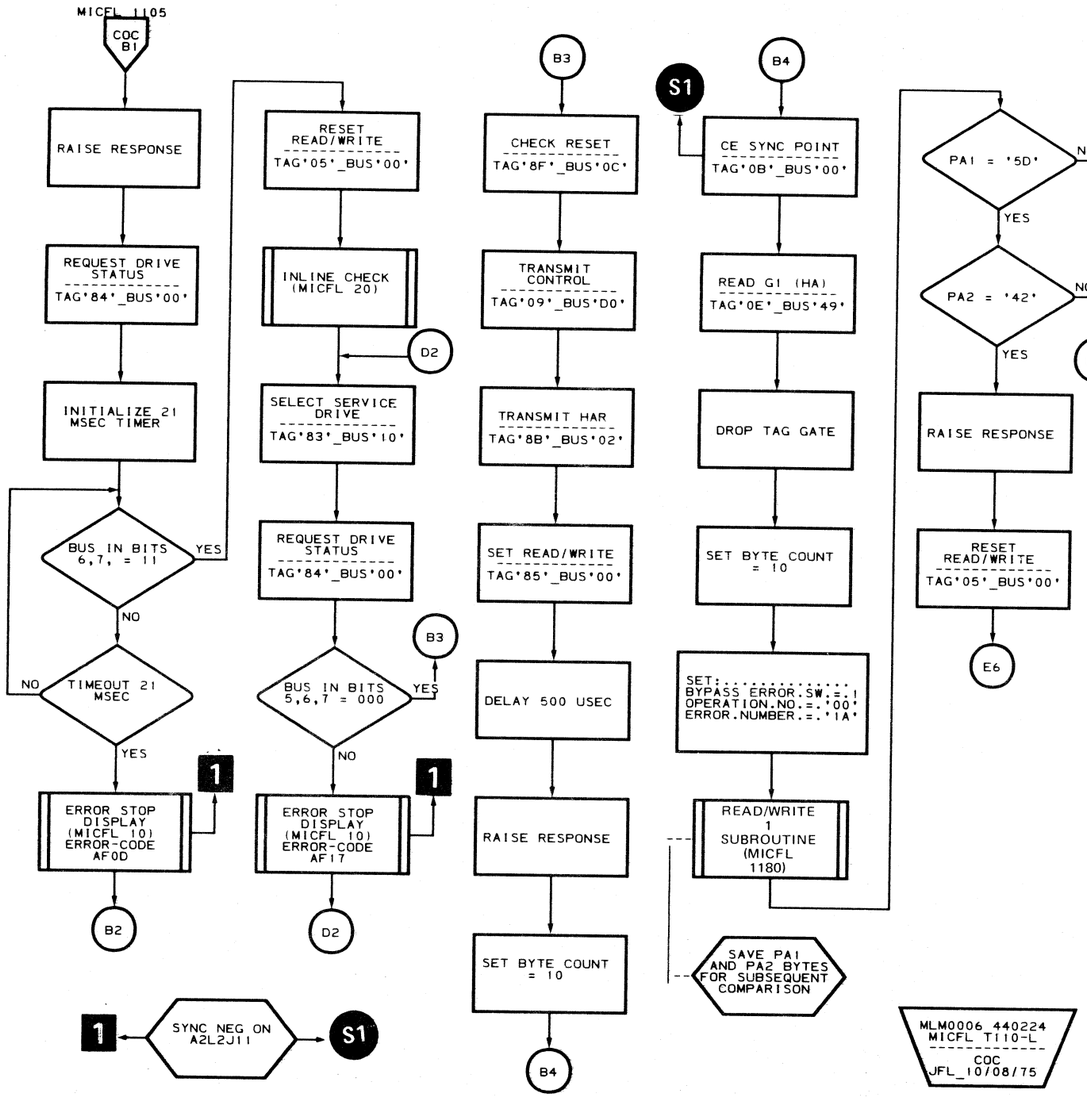
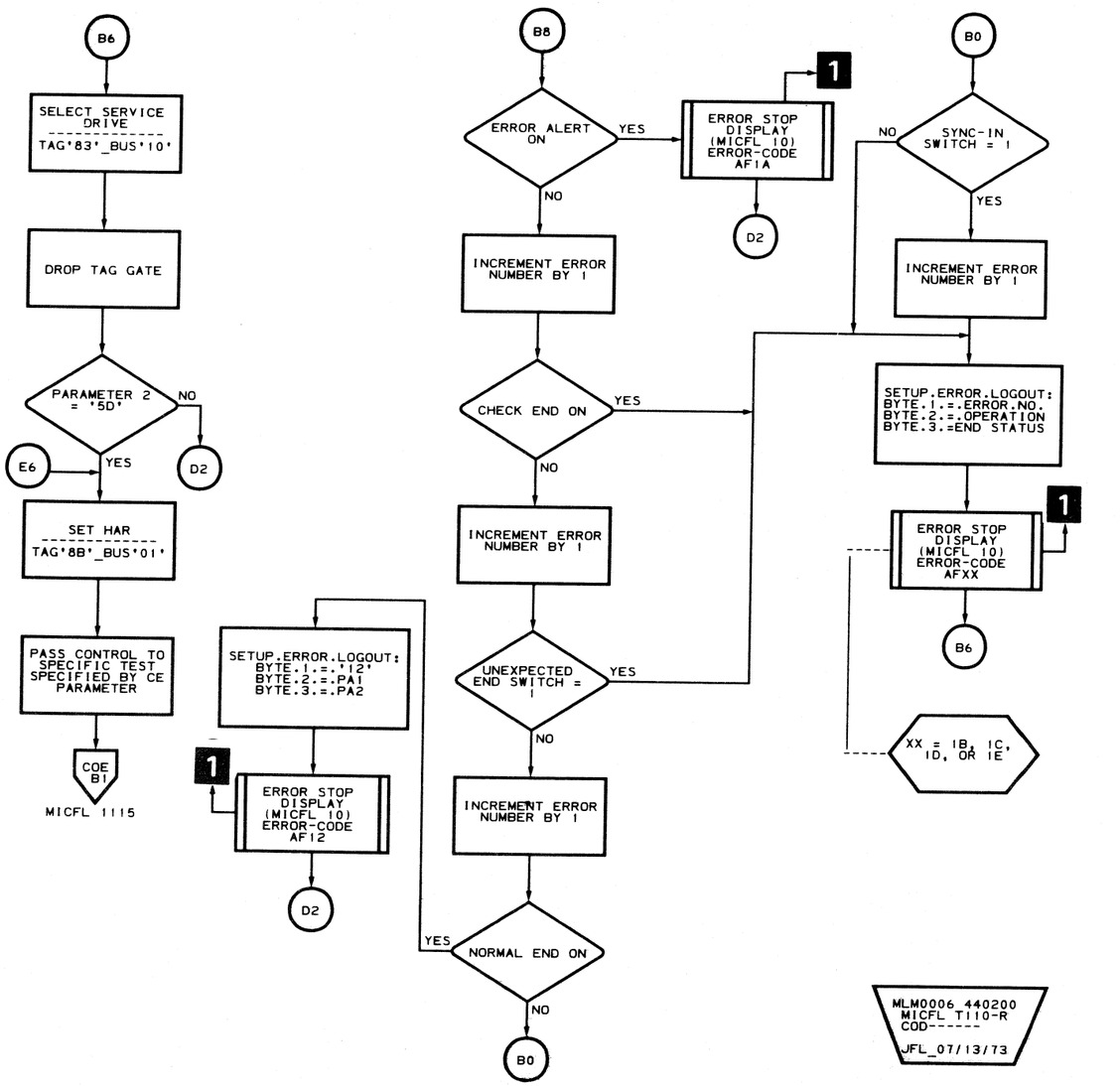
Routine AF





CG1110	2747111
Seq. 1 of 2	Part No.(N)

440200	440202	440203	440214	440223	440224	440227
25 June 73	7 Sept 73	2 Nov 73	17 Jun 74	14 Mar 75	15 Dec 75	14 Sept 76

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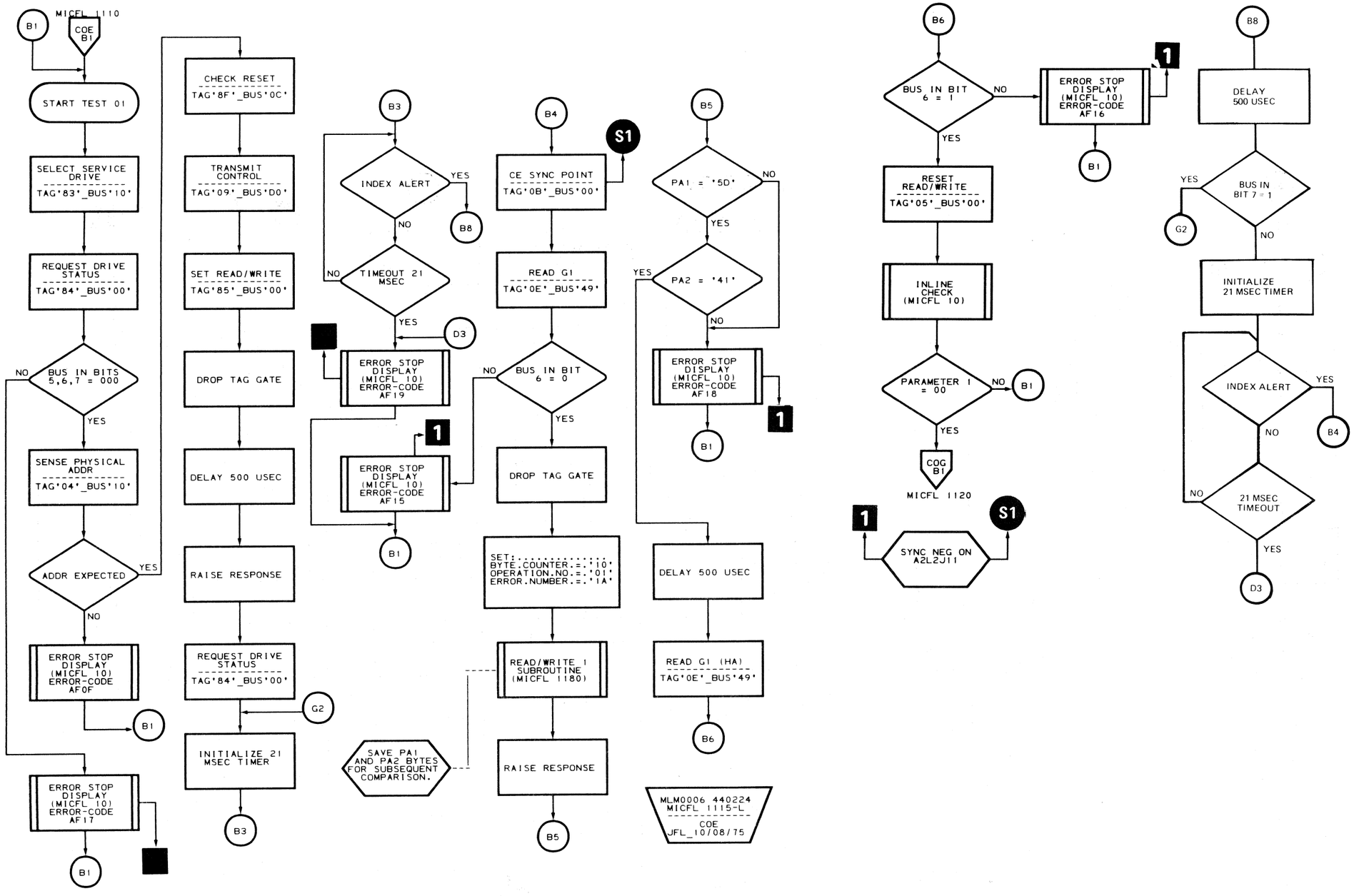

CG1110	2747111	440200	440202	440203	440214	440223	440224	440227
Seq 2 of 2	Part No. (N)	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	14 Mar 75	15 Dec 75	14 Sept 76

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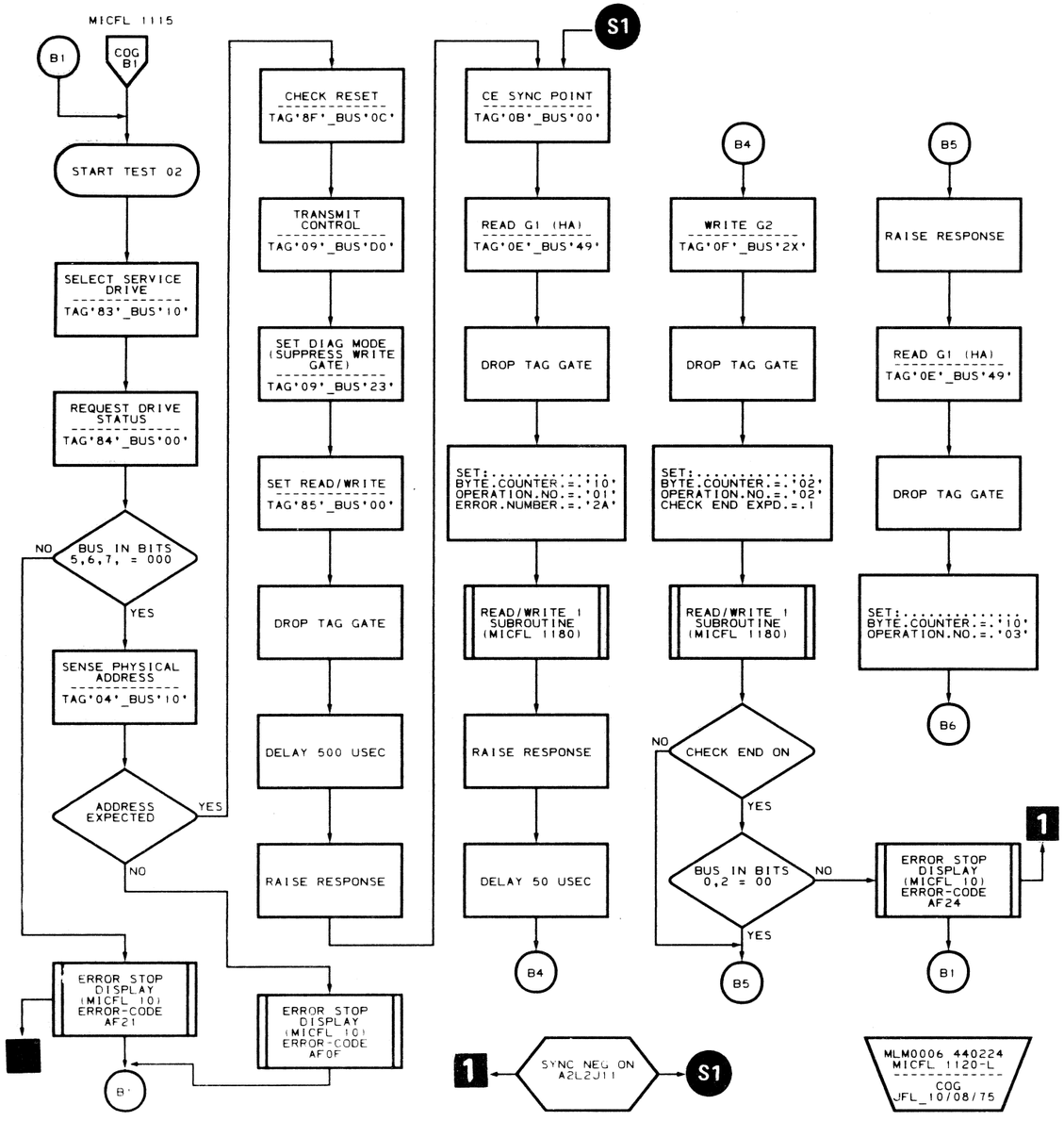
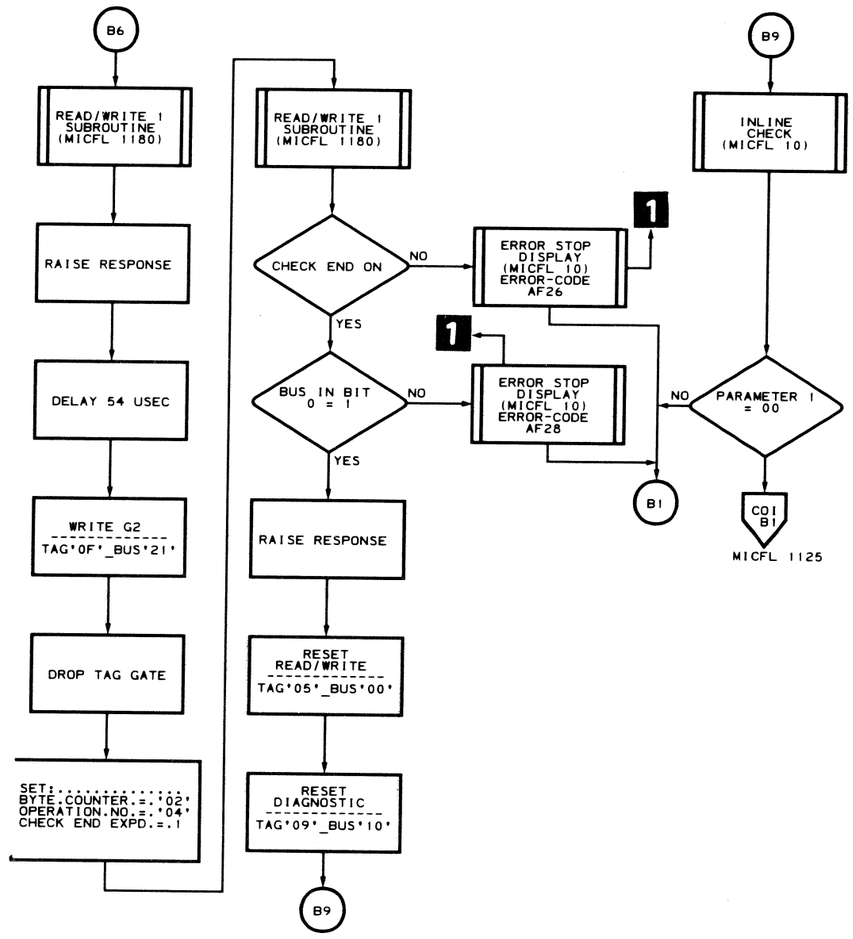
TEST 02 (Routine AF)





CG1120	2747112	440200	440202	440203	440214	440224		
Seq. 1 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	17 Jun 74	15 Dec 75		

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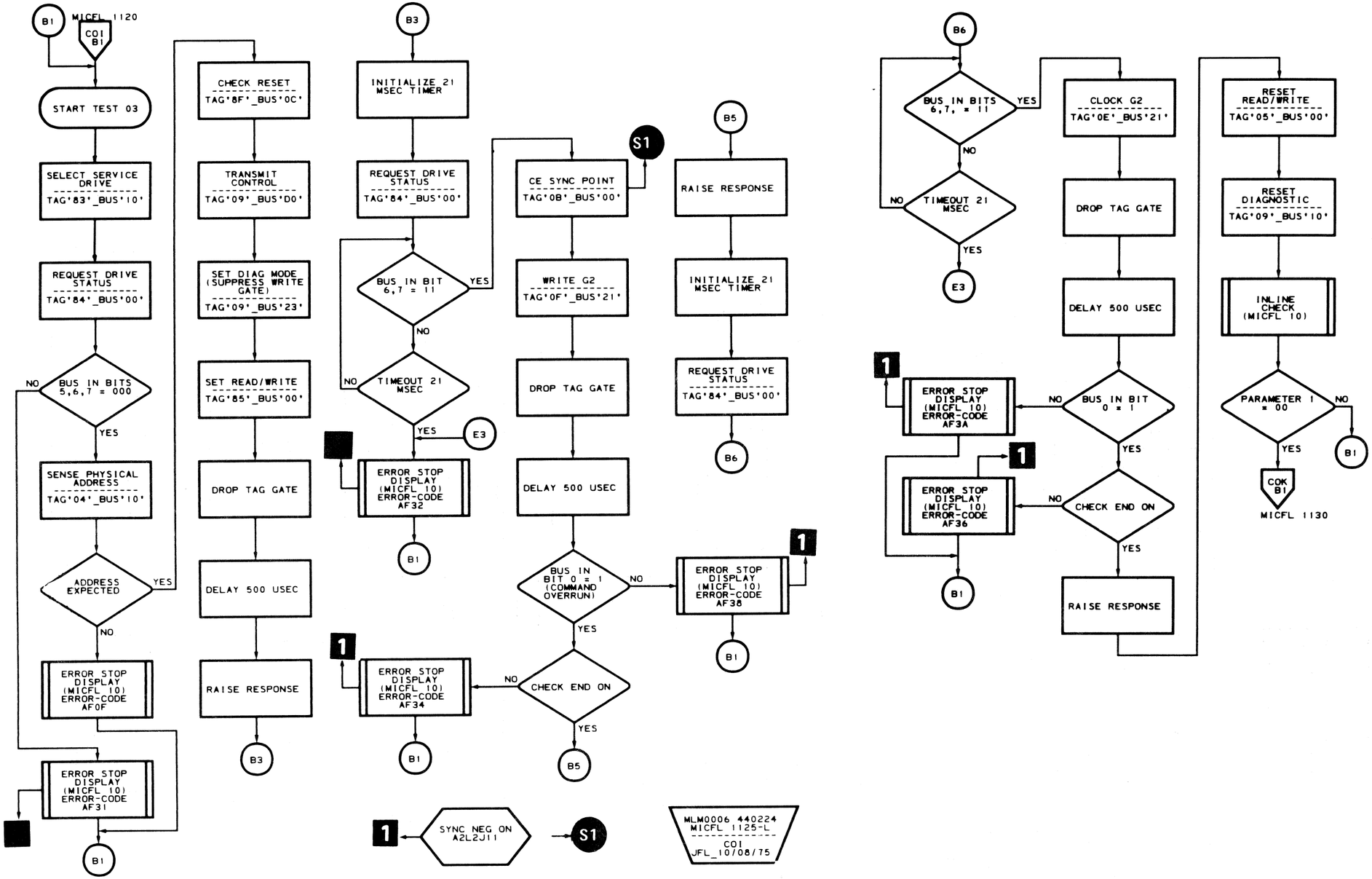

CG1120	2747112
Seq. 2 of 2	Part No.( )

440200	440202	440203	440214	440224		
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	15 Dec 75		

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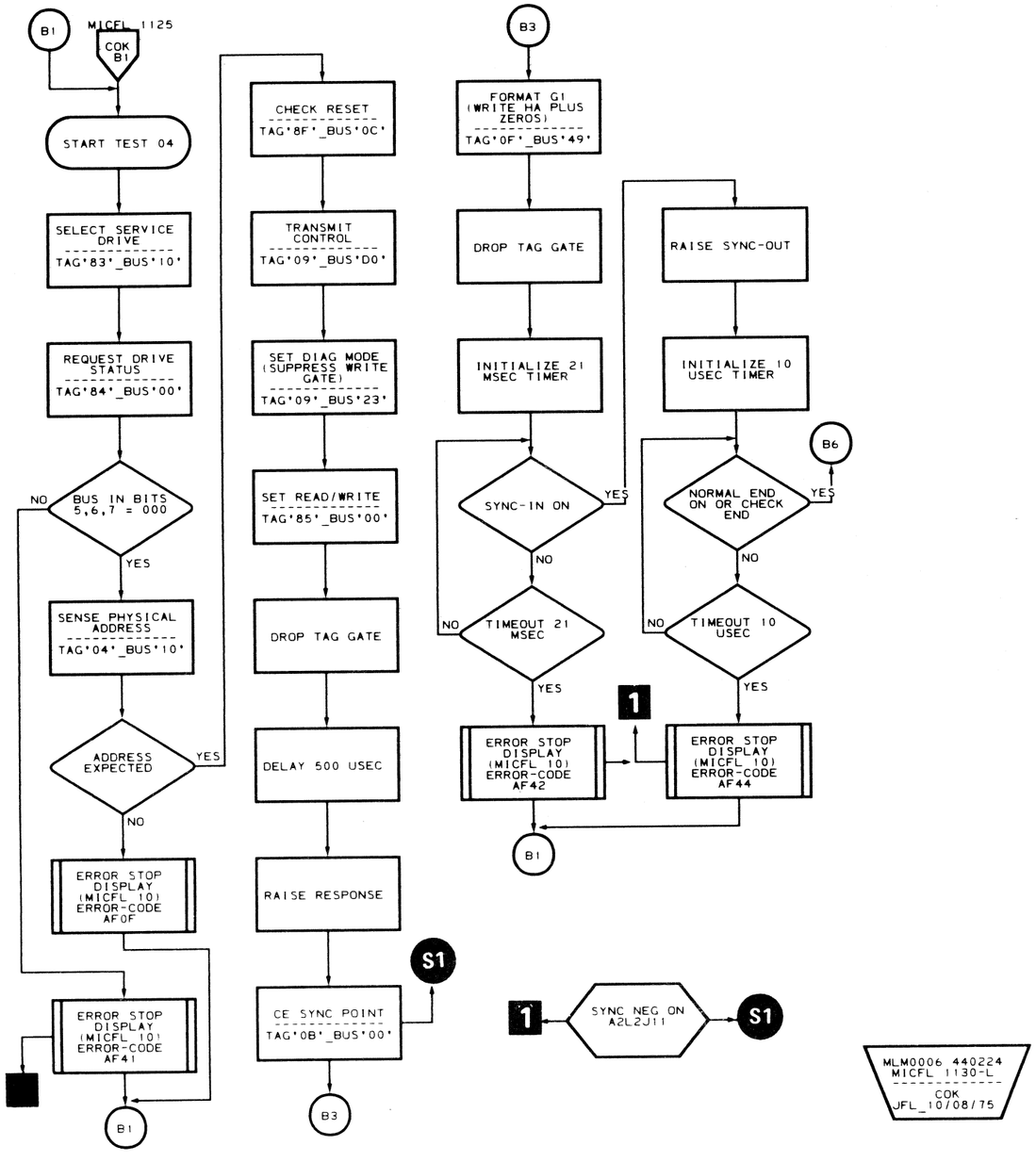
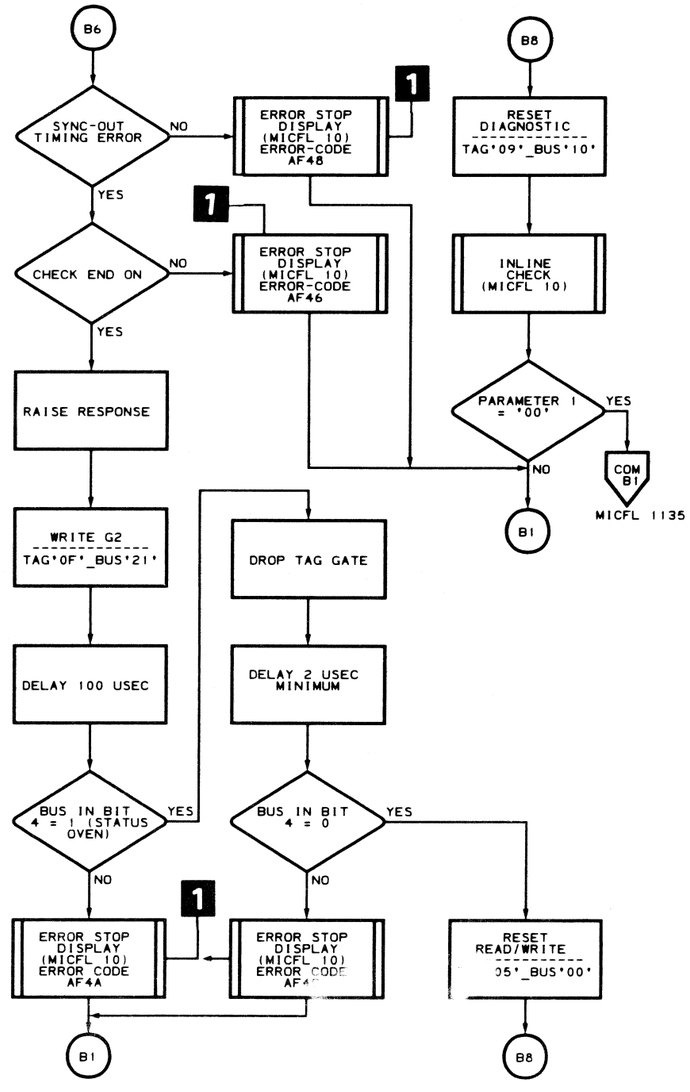
SYNC OUT TIMING ERROR (Routine AF)





CG1130 Seq. 1 of 2	2747113 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440210 15 Apr 74	440224 15 Dec 75		

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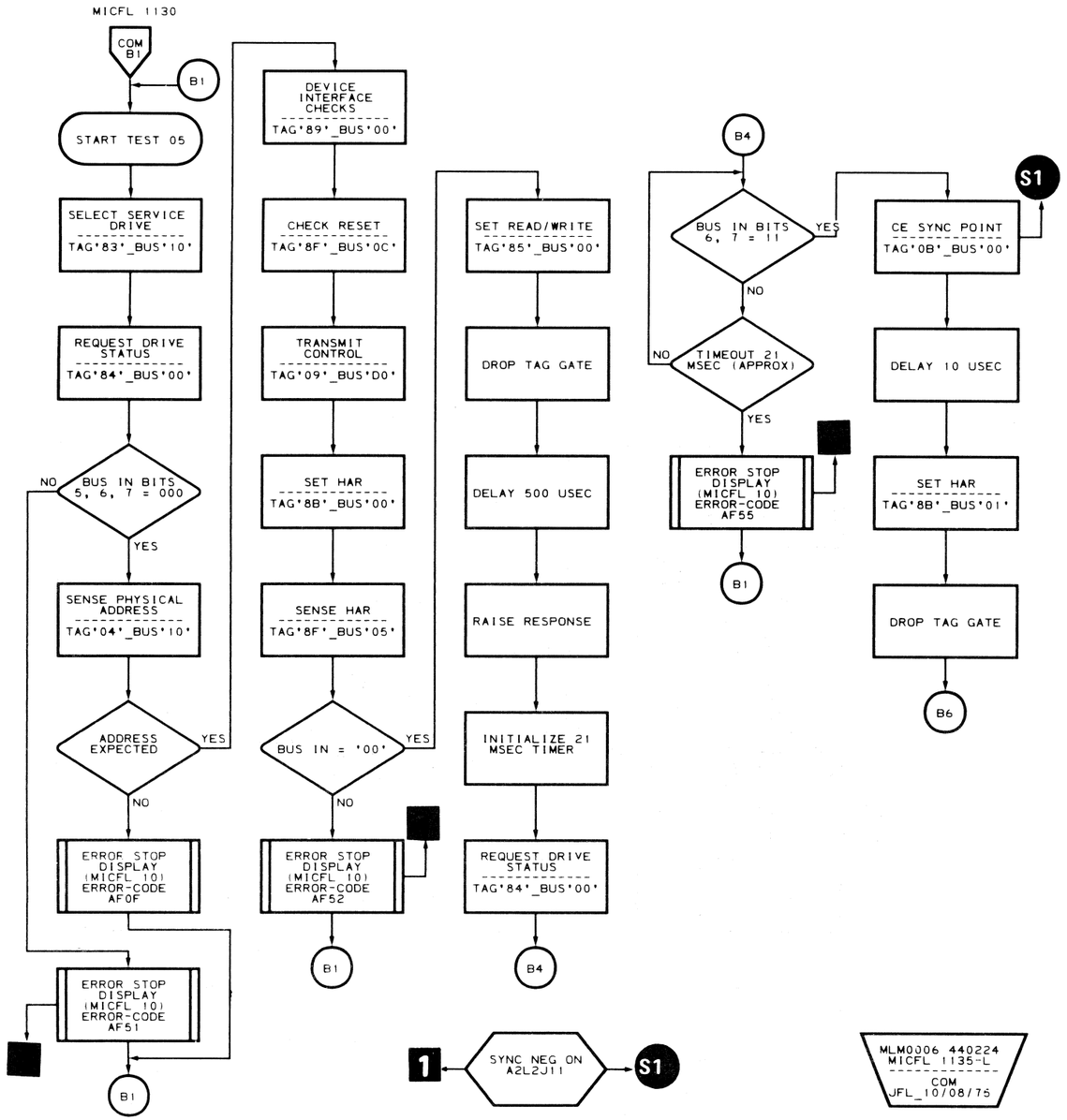
ALLOW HAR TEST (Routine AF)



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MICFL 1135-L
COM
JFL_10/08/75

MLM0006 440210
MICFL 1135-R
CON
JFL_03/22/74

CG1130	2747113	440200	440202	440203	440210	440224		
Seq. 2 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	15 Apr 74	15 Dec 75		

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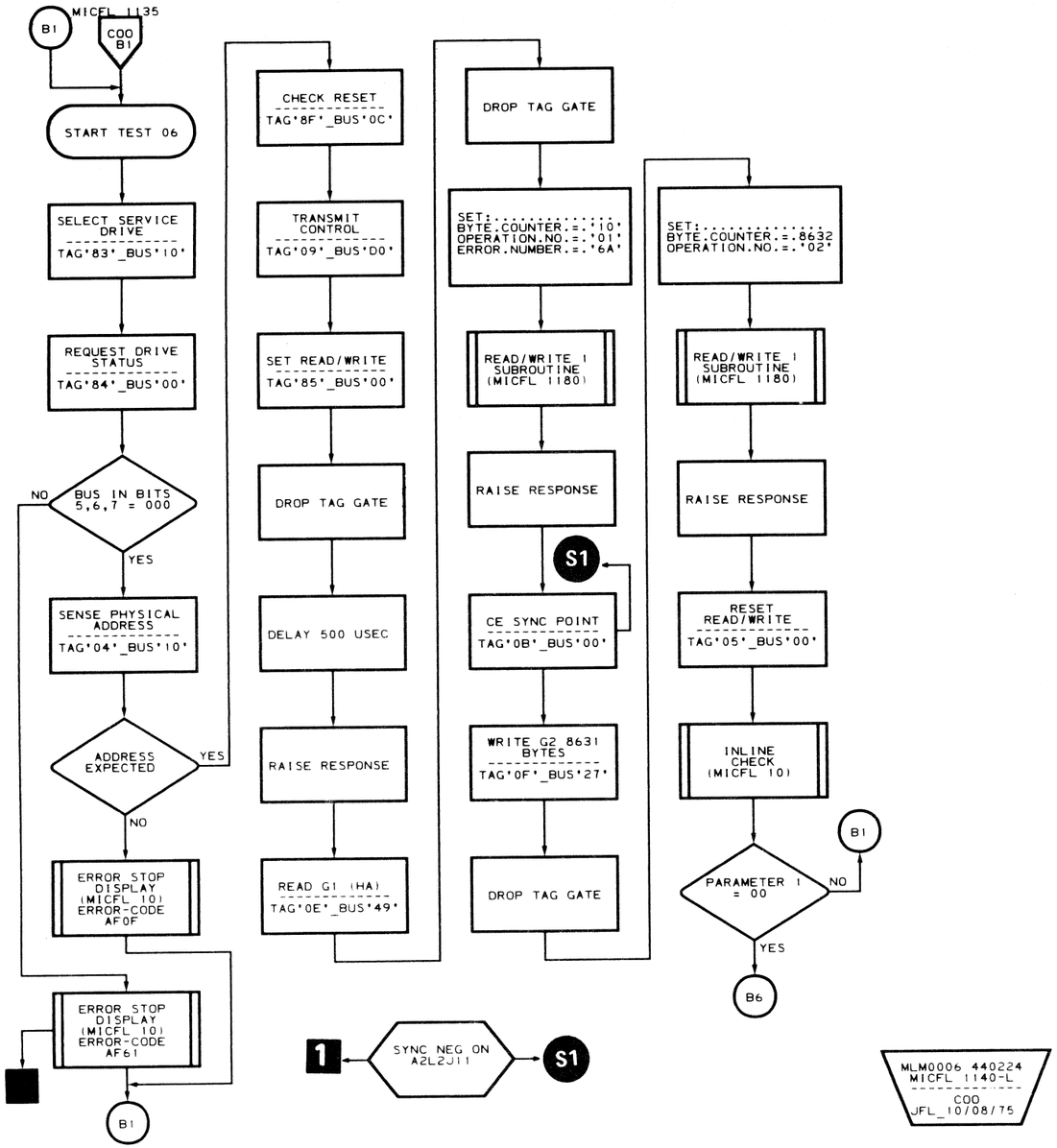

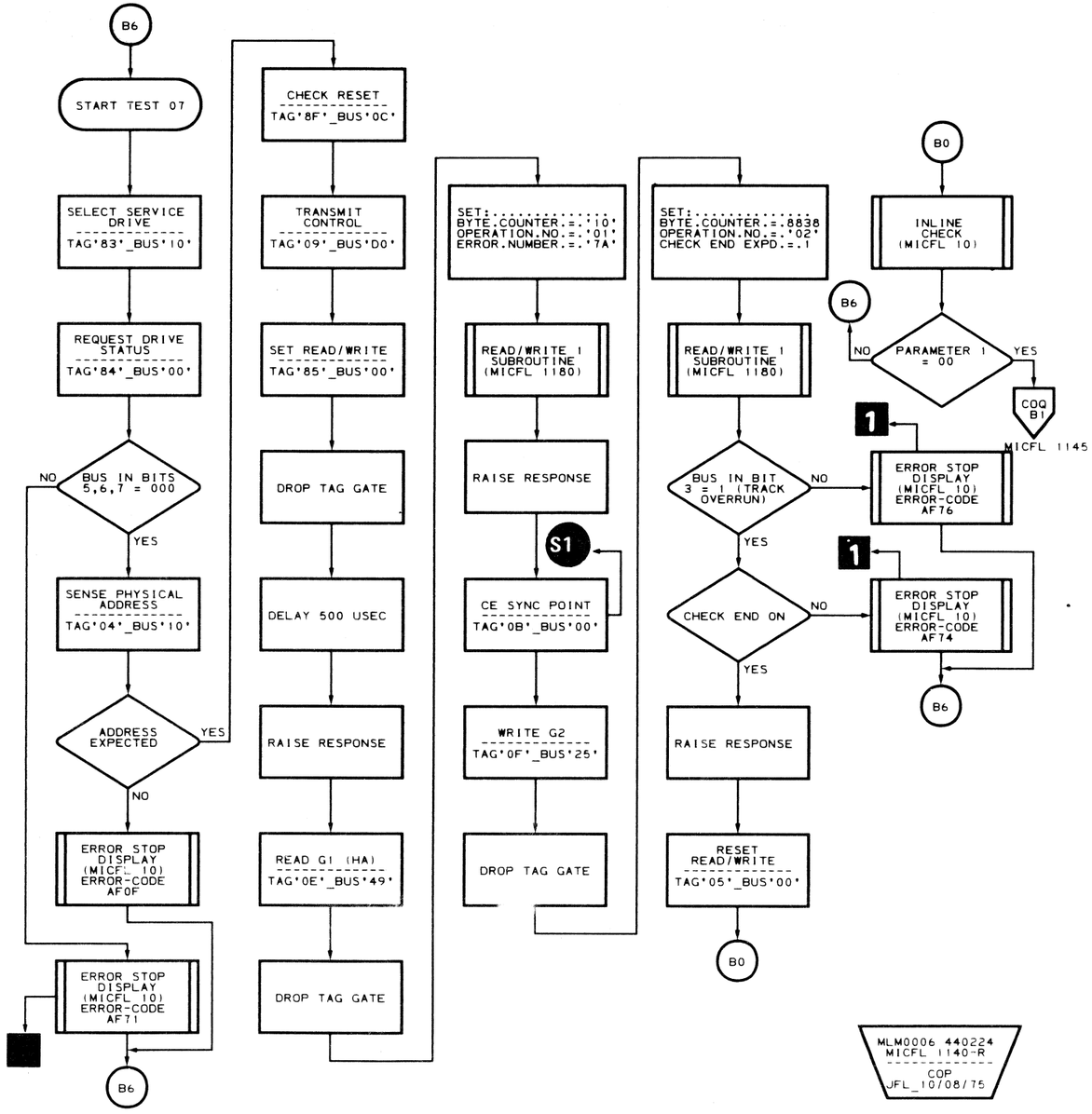

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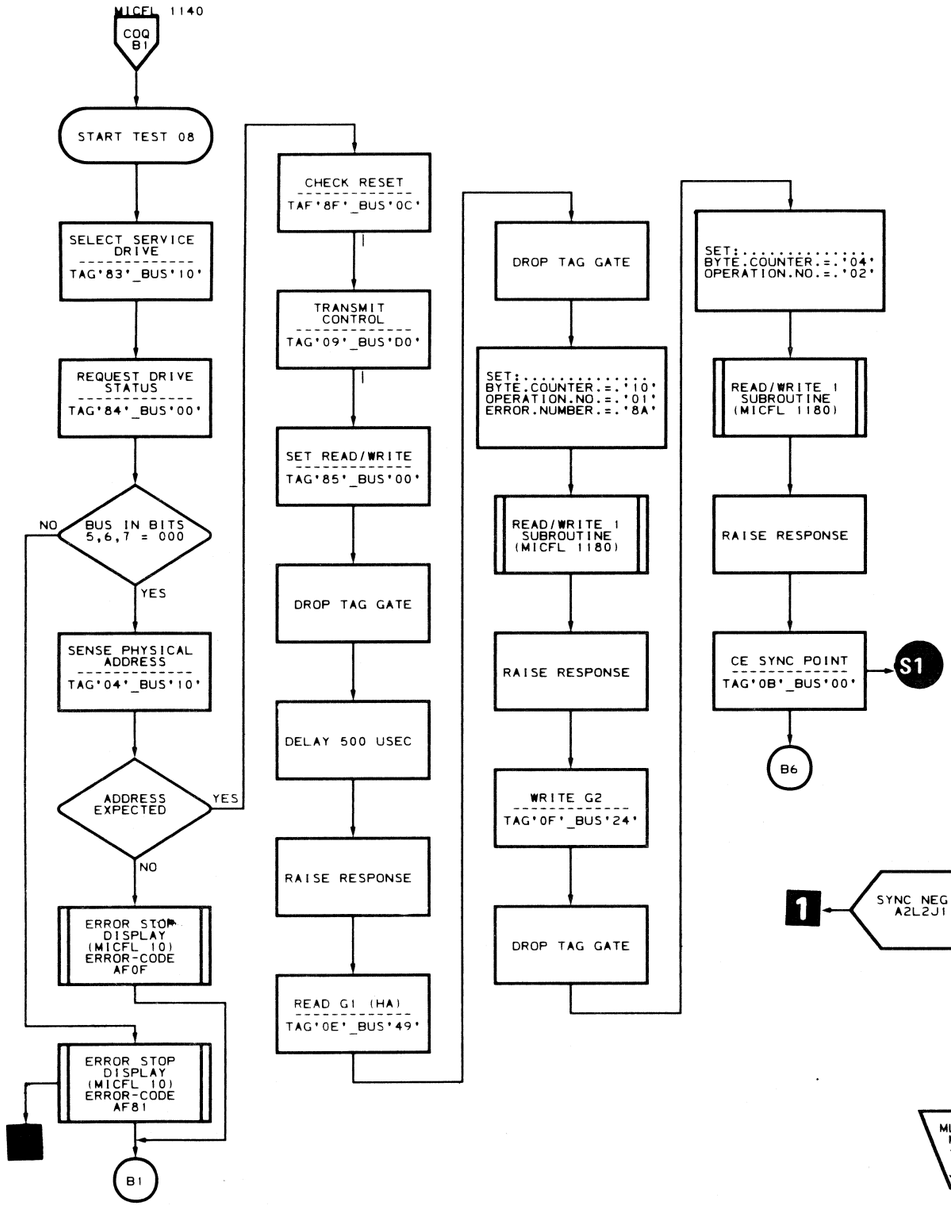

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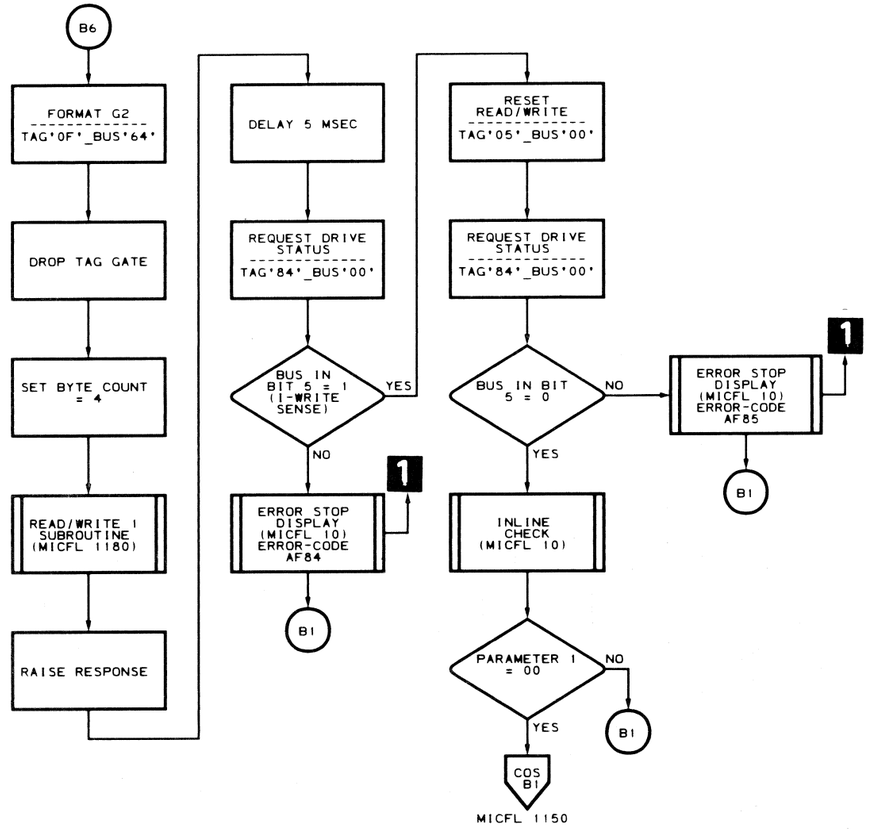
COQ
JFL_10/08/75



MLM0006_440200
MICFL_T145-R
COR
JFL_07/13/73

CG1140 Seq. 2 of 2	2747114 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440224 15 Dec 75			

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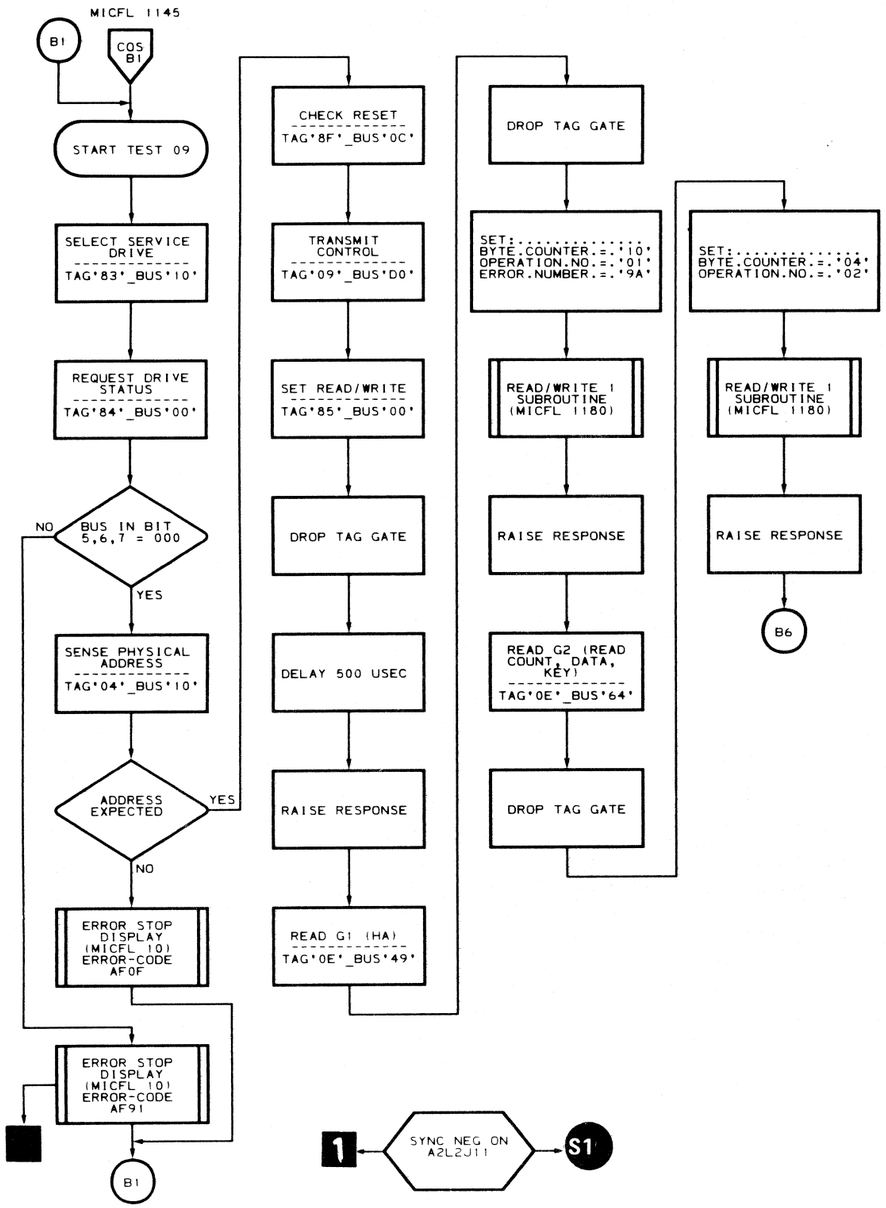

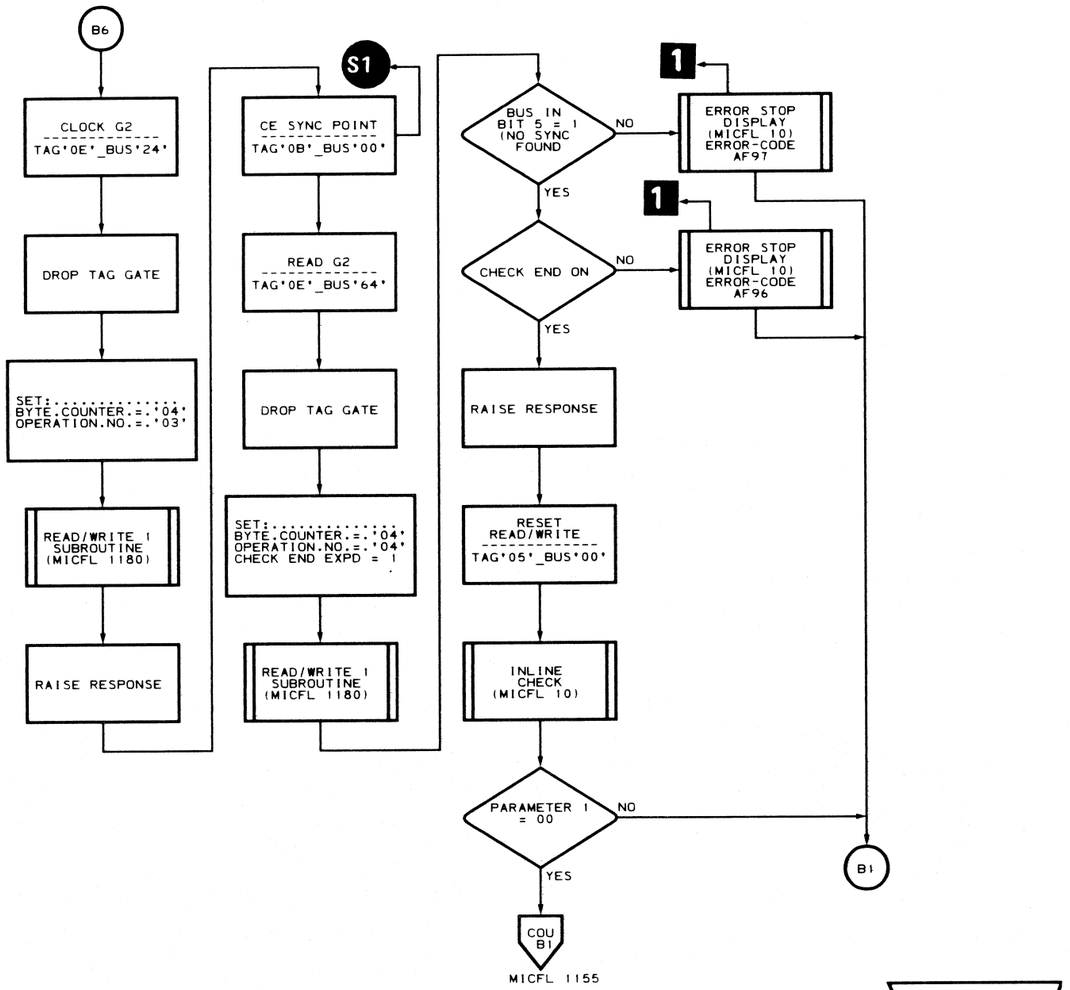

MLM0006 440224
MICFL 1150-L
COS
JFL_10/08/75

MLM0006 440200
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JFL_07/13/73

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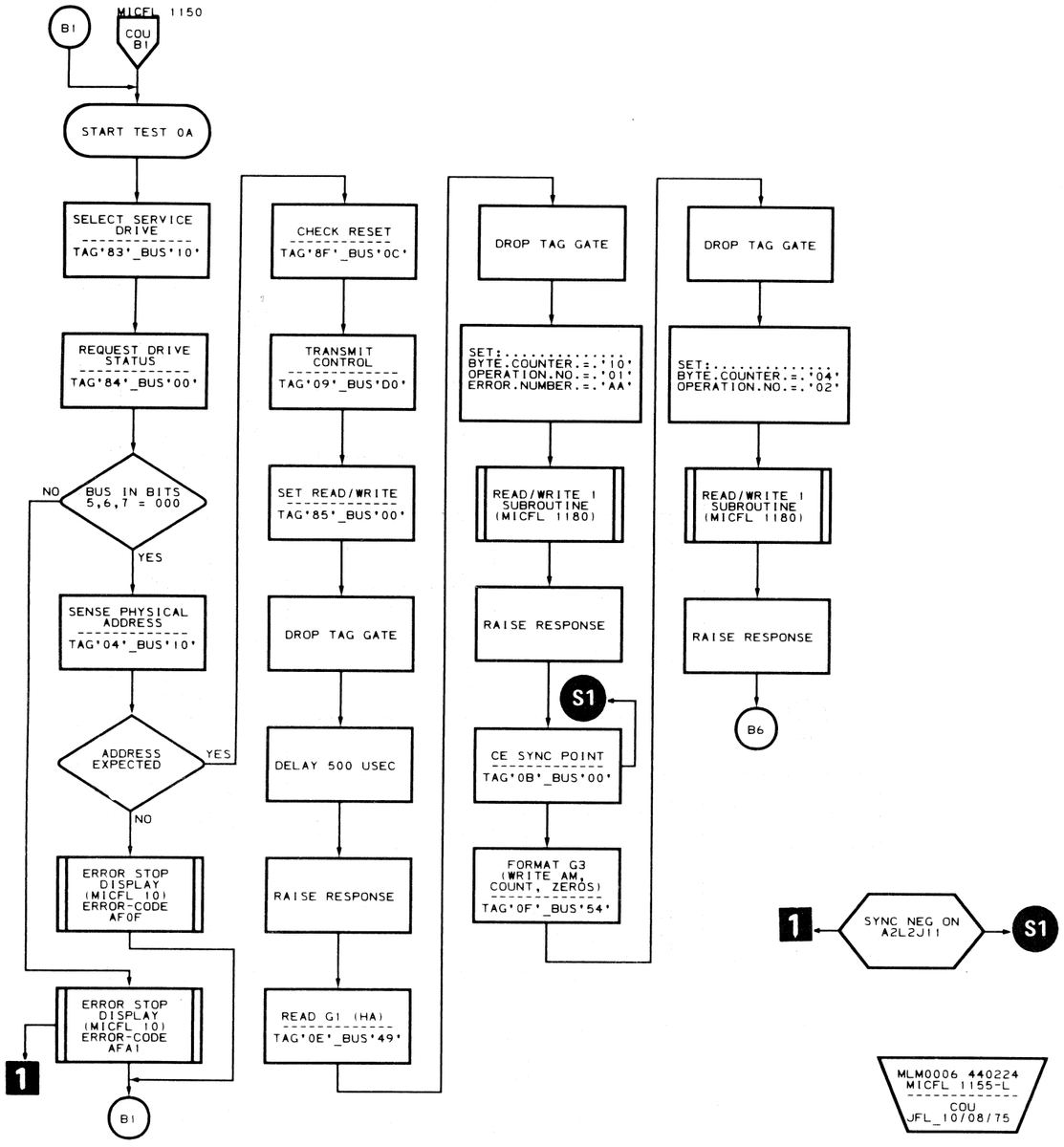
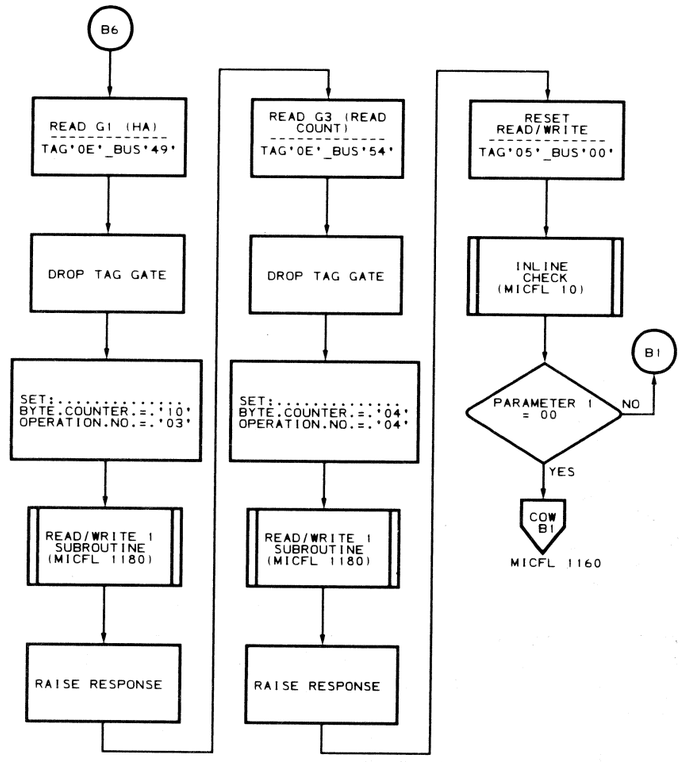
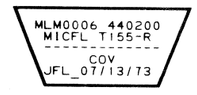
TEST 0A (Routine AF)







CG1150	2747115	440200	440202	440203	440224			
Seq. 2 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	15 Dec 75			

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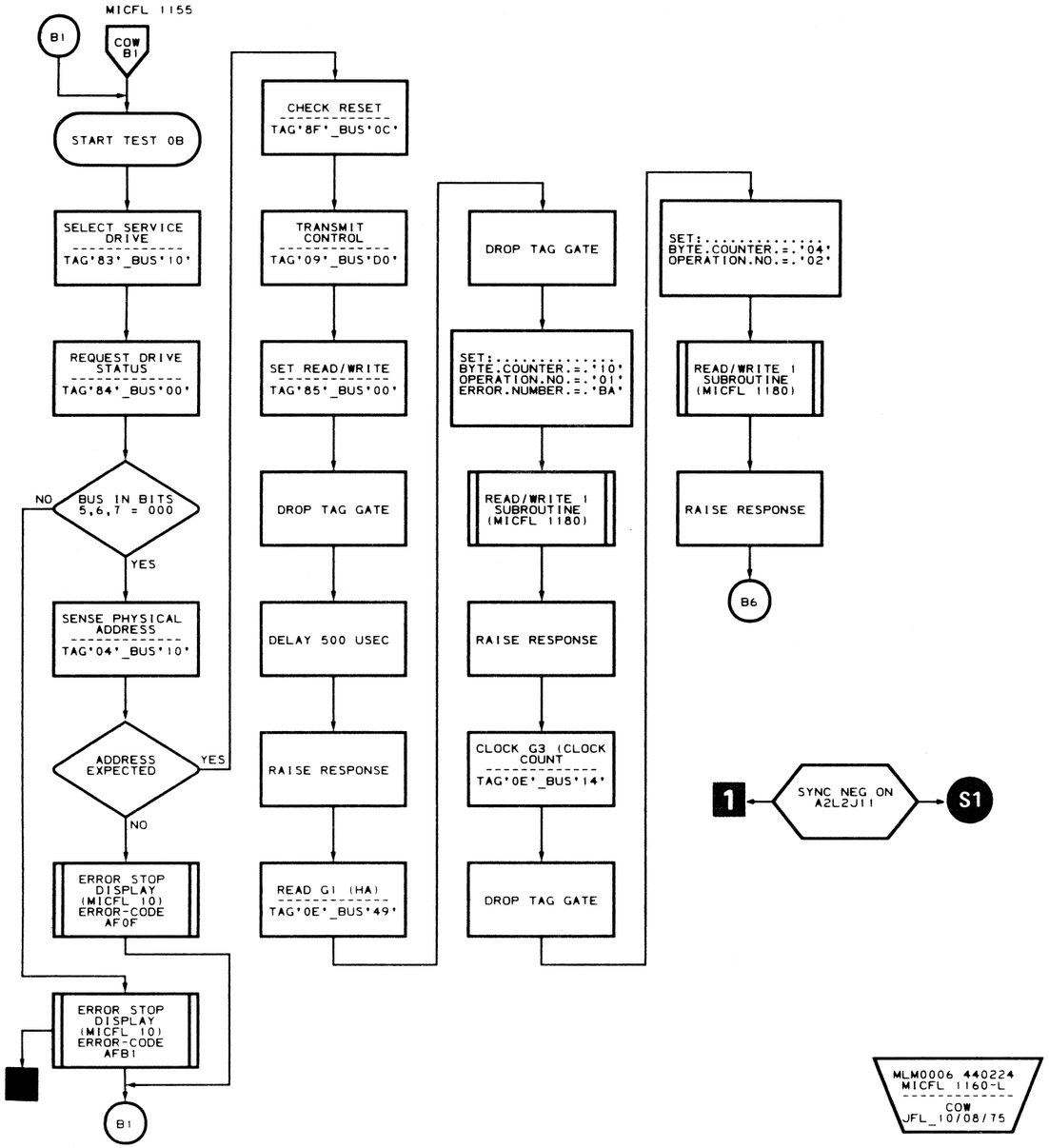
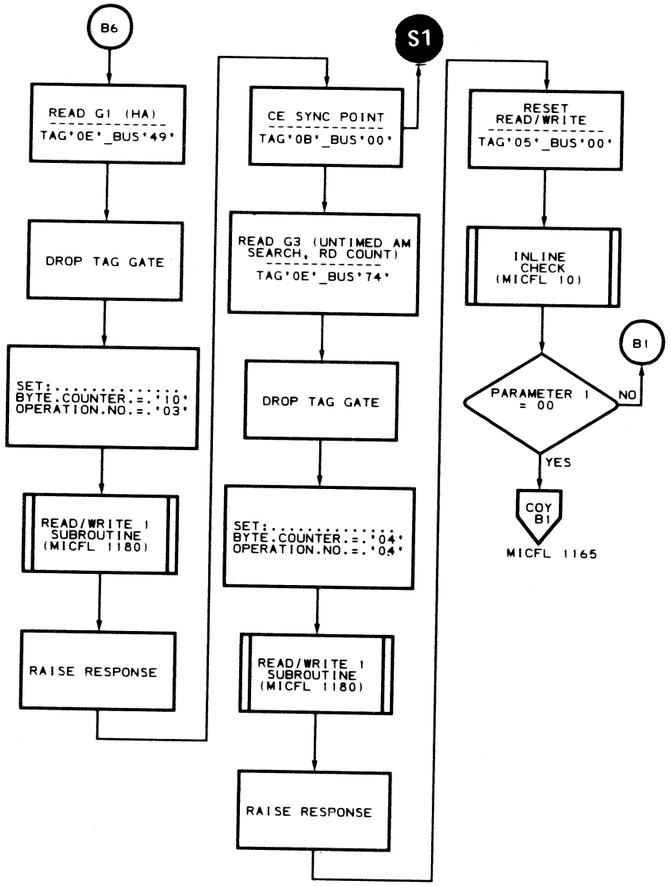
TEST 0B (Routine AF)





MLM0006 440224
MICFL 1160-L
COW
JFL_10/08/75

MLM0006_440200
MICFL T160-R
COX
JFL_07/13/73

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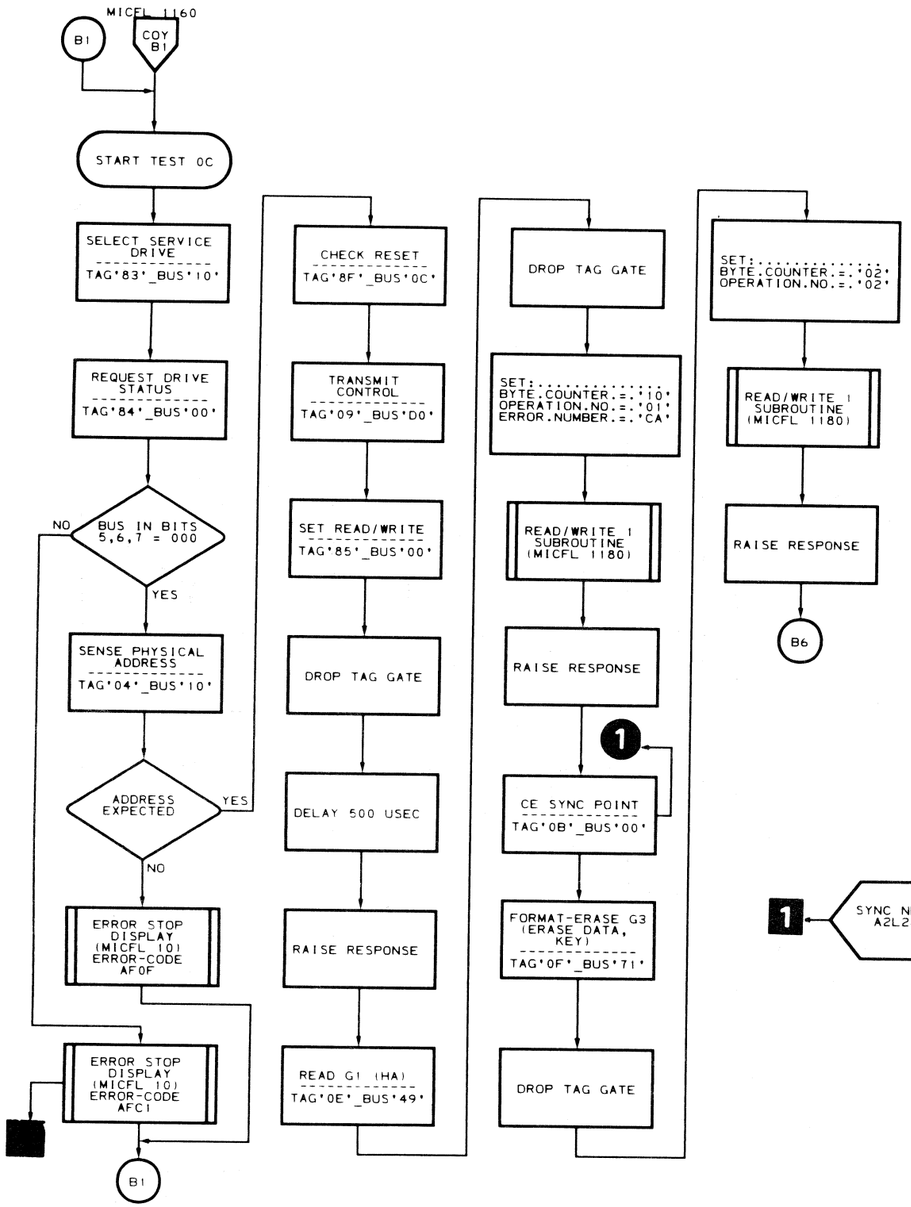

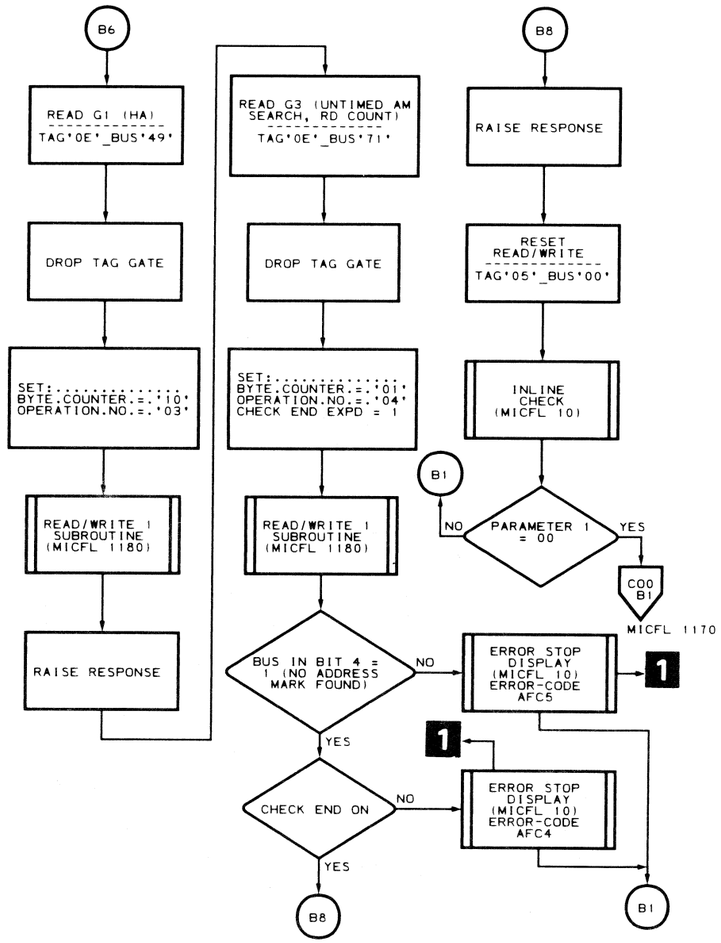

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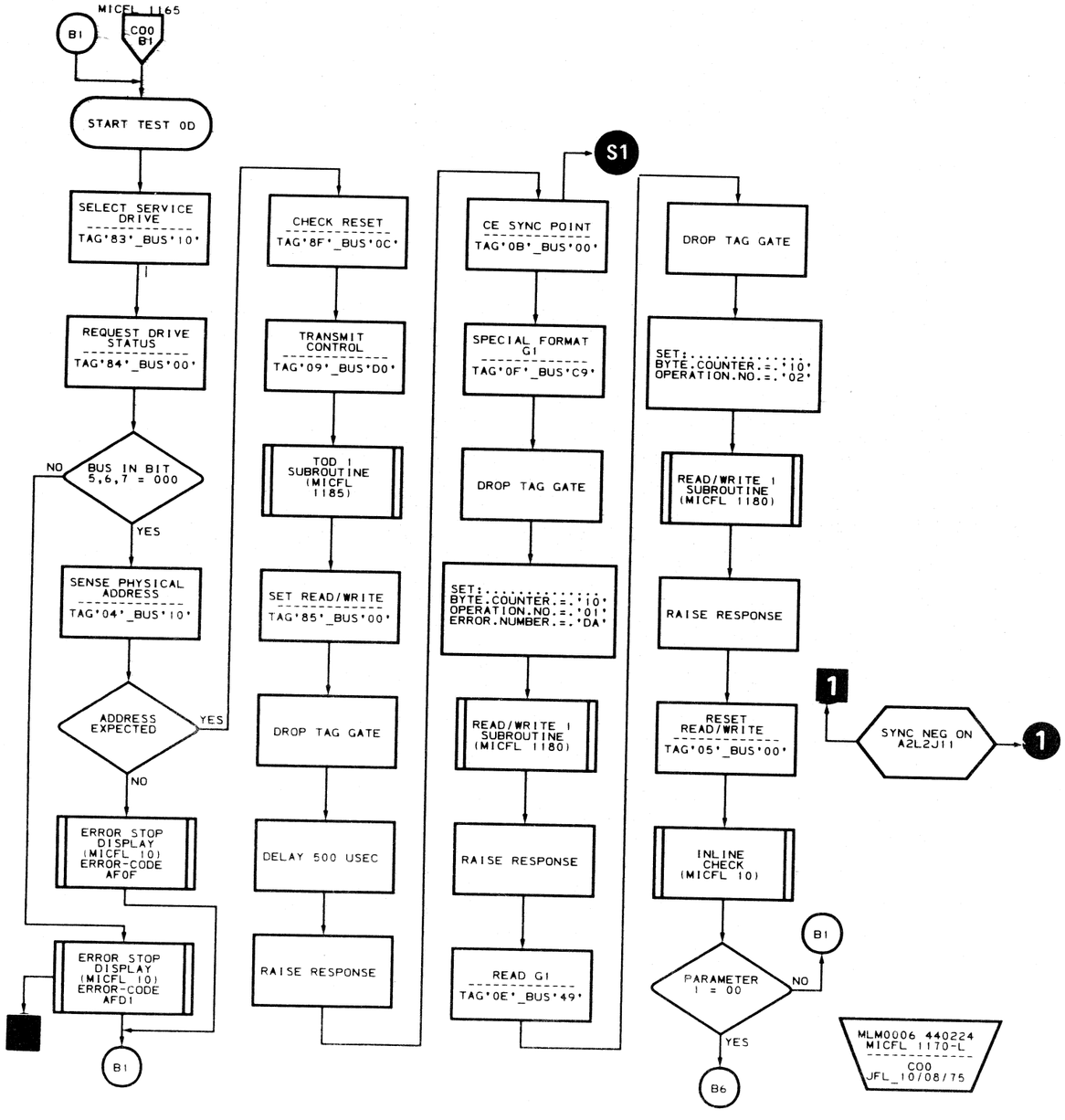
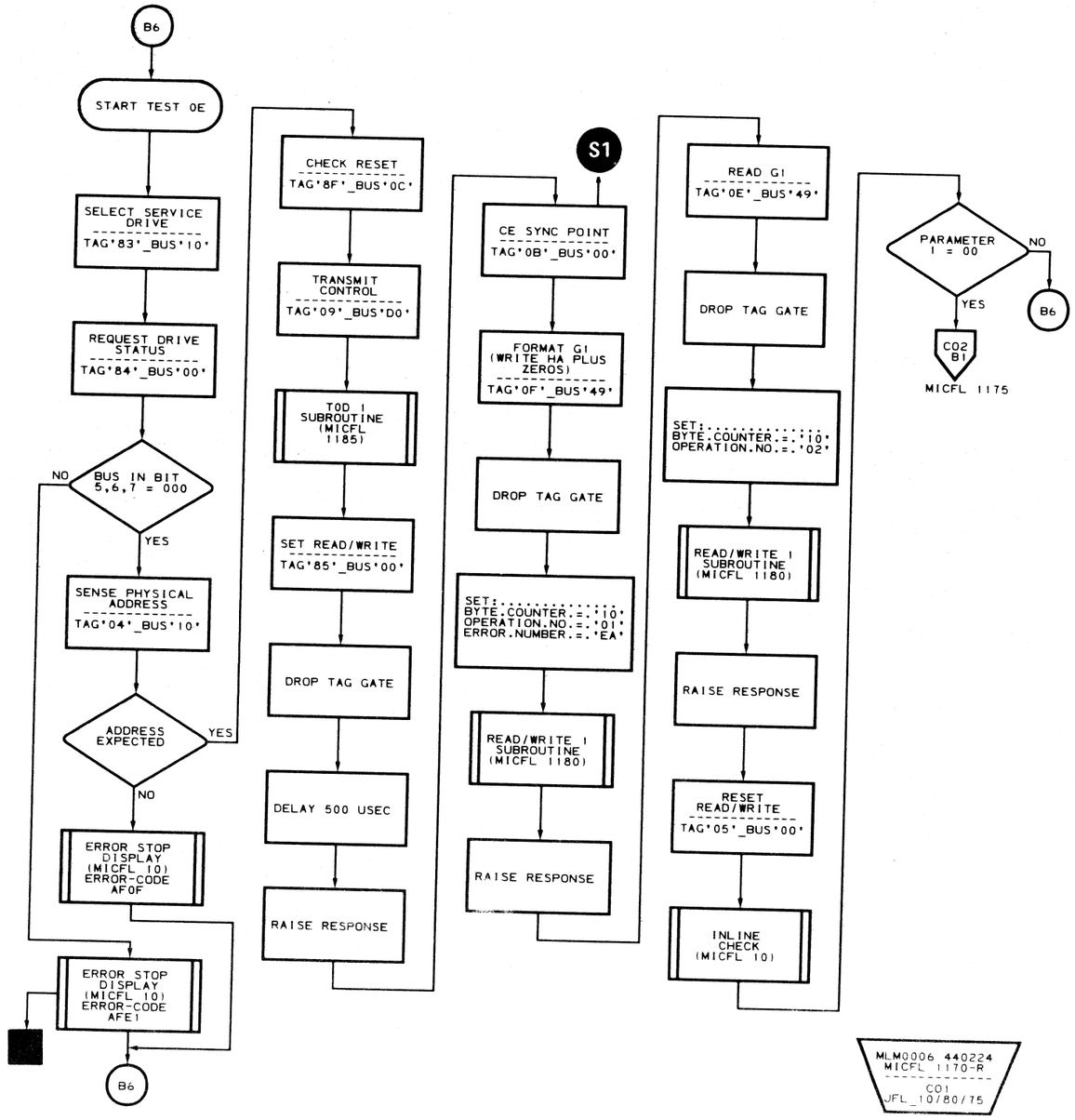
TEST 0D and 0E (Routine AF)





CG1170 2747117 Seq. 1 of 2 Part No.( )	440200 25 June 73	440202 7 Sept 73	440203 2 Nov 73	440223 14 Mar 75	440224 15 Dec 75		

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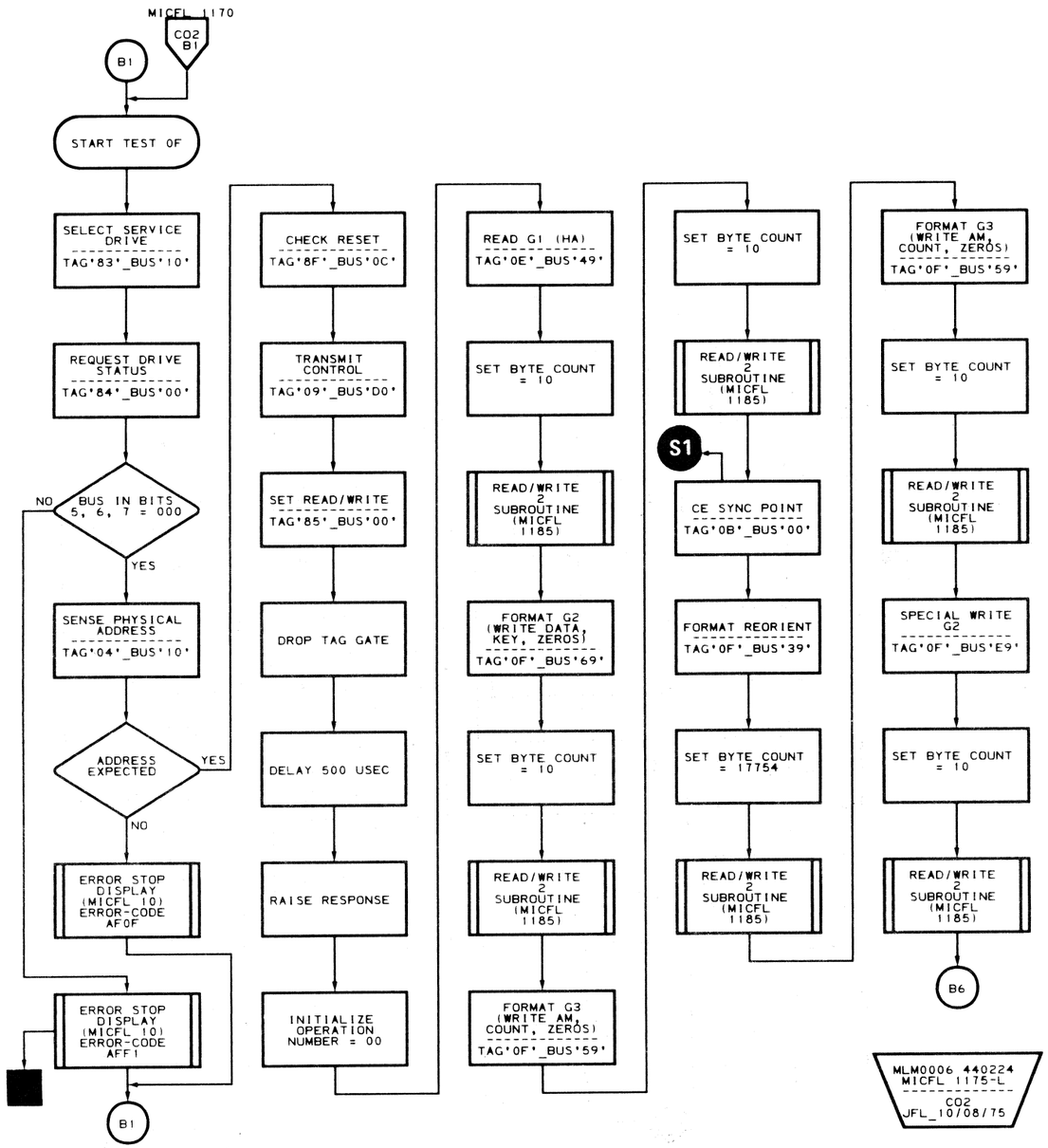

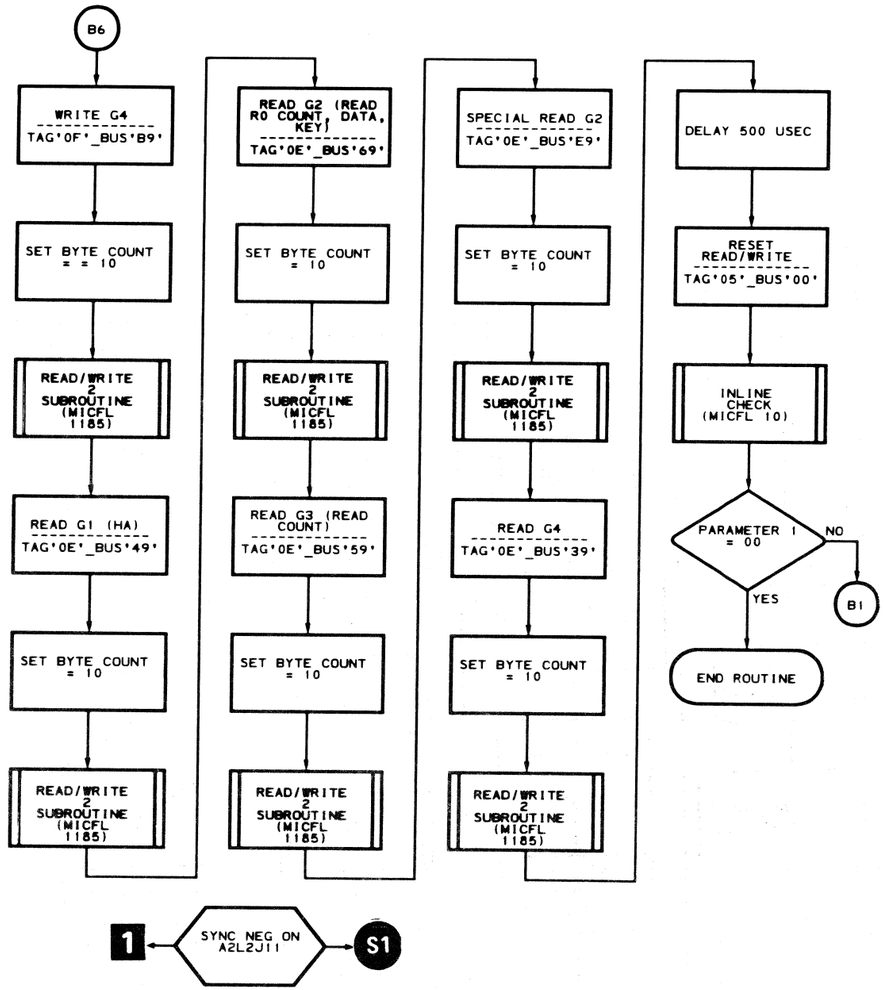

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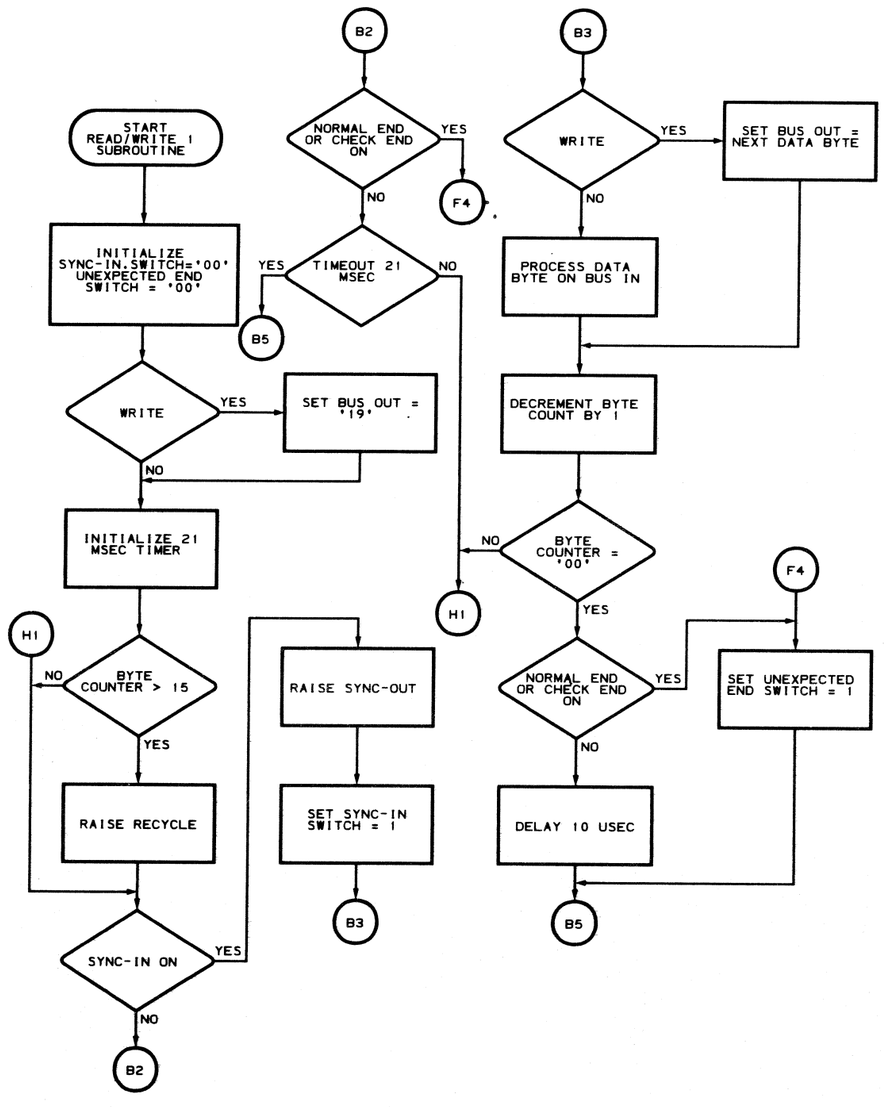
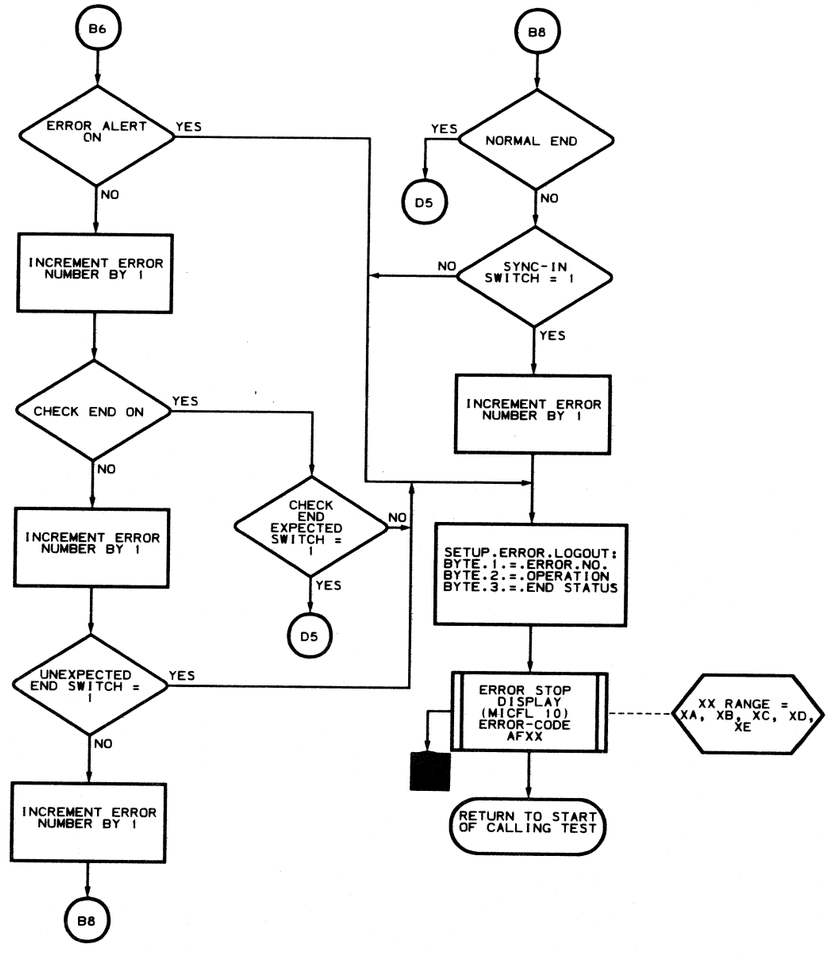
READ/WRITE 1 SUBROUTINE (Routine AF)



MLM0006 440200
MICFL T180-L
C04------
JFL_07/13/73



MLM0006 440200
MICFL T180-R
C05------
JFL_07/13/73

CG1180	2747118	440200	440202	440203	440214			
Seq. 1 of 2	Part No.( )	25 June 73	7 Sept 73	2 Nov 73	17 Jun 74			

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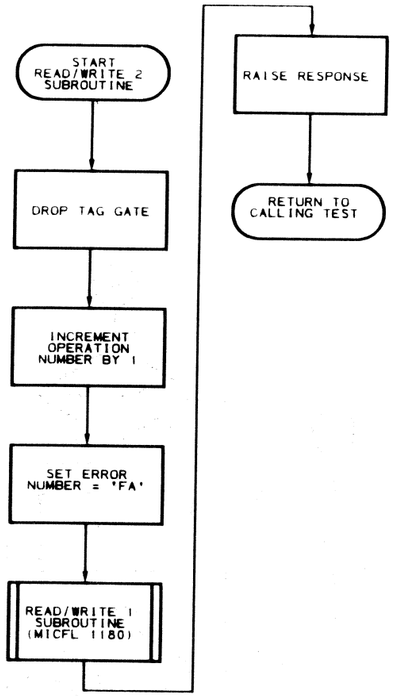
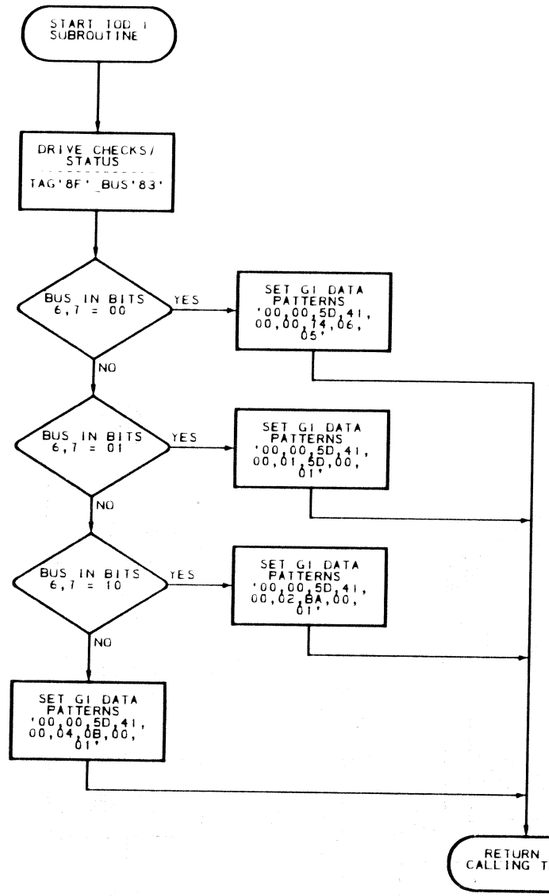


MLM0006 440200
MICFL T185-L
C06------
JFL 07/13/73



MLM0006 440200
MICFL T185-R
C07------
JFL 07/17/73

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ROUTINE AF SCOPING PROCEDURES

Routine AF tests the ability of the Controller to control Read/Write operations and check certain hardware and programming errors. The test contains an initialization program which seeks to the CE Cylinder, verifies the Seek by reading the physical address on head 2, and makes a comparision to the physical address expected (5042). This portion of the program loops only if an error exists. In this case, the machine was forced to select head 0 instead of head 2 to simulate an error condition. While in actual operation, any of several conditions could cause a physical address miscompare. Examples are:

HAR Failure
Matrix Card Failure
Seek Failure
Difference Counter Failure
Servo Problems

The pictures also depict, mostly in chronological order, the key events in a Read operation.

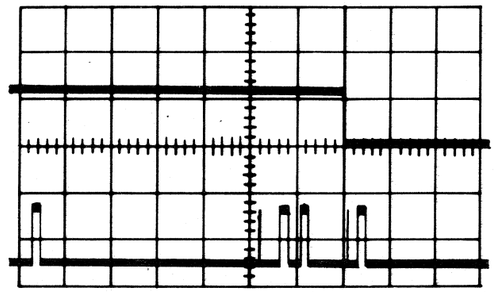
Note: When scoping, be aware that once an error is detected, further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

Time: Select an appropriate time/div to display 2 +G1 pulses (1 ms to 5 ms). Use Triggered Delayed Sweep, triggering on the second +G1 pulse. Delay time used was 20 µs/div.

+ G1
A2Q2J09 (BH120)
Alternate: A2P2G04 (BG140)

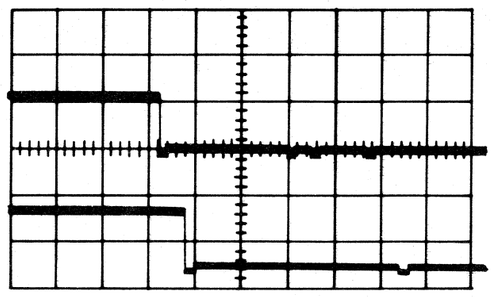


+ Reset Fast Sync
A2P2U09 (BG140)

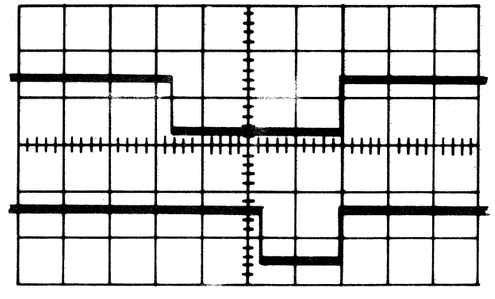
Read Gate and Unsquelch go to the drive to condition read circuits. Transfer Sector Count preserves the Sector Count at the start of the operation if a subsequent read Sector operation is executed (RPS feature only).

–Read Gate
A2Q2P09 (BH140)

–Unsquelch
A2Q2M09 (BH140)



–Transfer Sector Count
A2Q2J07 (BH120)



PLO mode is the opposite of read data, therefore, the inactive level would indicate read time.

+ PLO Mode
A2S2M02 (BC140)

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ROUTINE AF SCOPING PROCEDURES (continued)

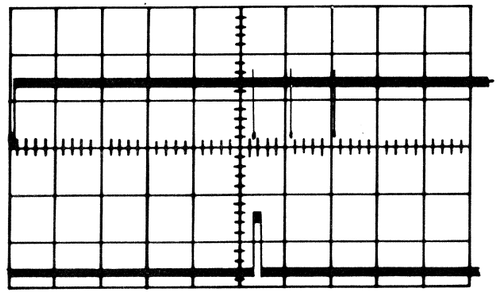
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

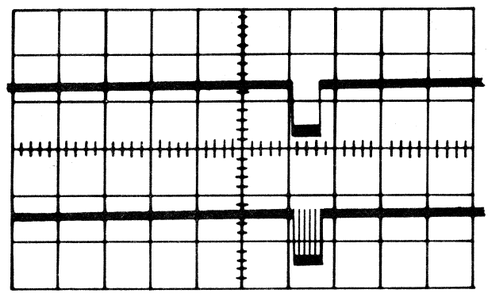
Time: 1 ms/div using triggered delayed sweep triggering on the second + G1. Delay time of 20 μs/div.

–Reset Ctr
A2P2B07 (BG100)

Note 4 Pulses. One is at Index, one at Count 90 at Sync Byte found time before counting bytes, and one after ECC processing.

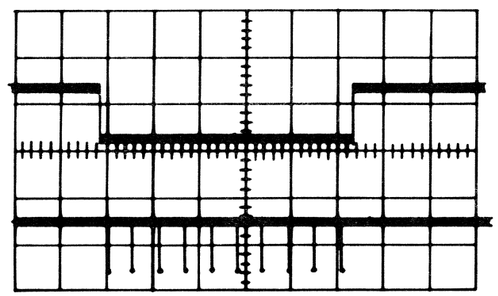


+ VFO to Data
A2P2J13 (BG140)



–Read Mode
A2P2U02 (BG170)

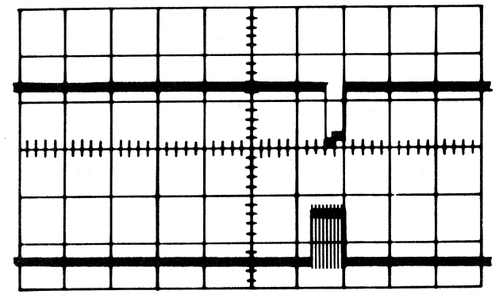
–Sync In Ten Pulses – See Below
A2S2U10 (BC170)



Time same as above except X 10
–Read Mode
A2P2U02 (BG170)

Time same as above except X 10
–Sync In
A2S2U10 (BC170)

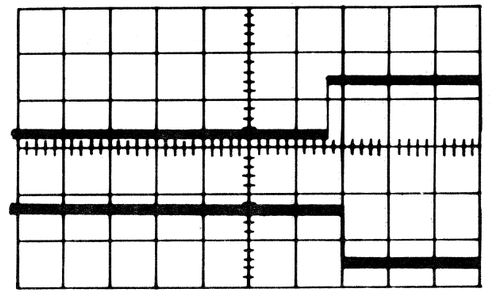
–Xfer ECC
A2P2G08 (BG170)



–ECC Zeros Compare
A2S2U07 (BC150)

If ECC Zeros compare is not minus at the end of the operation, it is a data check.

+ End Data
A2P2S03 (BG170)



–End Data Op
A2P2S05 (BG170)

Note: When scoping, be aware that once an error is detected, further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE AF SCOPING PROCEDURES (continued)

This series of pictures in an analysis of a Read G1 operation. Not Index Data Good is a result of having successfully decoded the sync byte. The sync byte is represented by the first 3 pulses on standardized data. The sync byte is referred to as a '19'. In this case, the sync byte is followed by 2 bytes of hex '0D' for skip displacement. The following pulses represent a hex '5040' (for this test, 5042 is expected).

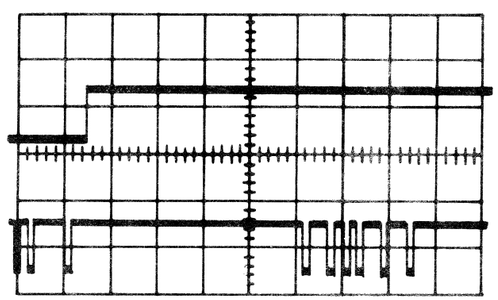
Scope Setup

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes

Time: 1 ms/div using triggered delayed sweep triggering on + VFO to data A2P2J13 and delay time of 5 μs/div and times 10 magnifier.

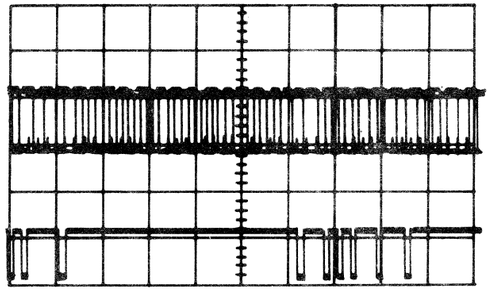
+ Not Index Data Good
A2Q2D10 (BH160)



–Standardized Data
A2T2G02 (BJ110)

The Raw Read Data from which the standardized data was derived is shown in relation to standardized data.

–Raw Read Data
A2T2D04 (BJ130)

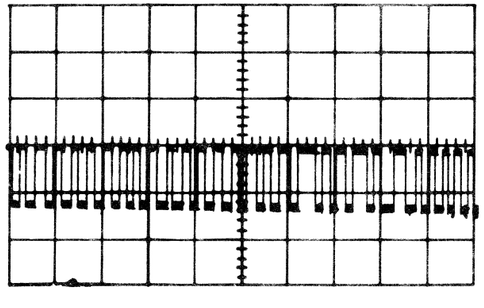


–Standardized Data
A2T2G02 (BJ110)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Read Write Data (Coaxial input)

A2T2B05 (BJ130)
A2T2D07 (BJ130)



Inputs added – One input inverted.
Trace may be inverted depending on the input arrangement and which input is inverted.

CG1192	2747120
Seq. 1 of 1	Part No. ( )

440200	440202	440203	440204			
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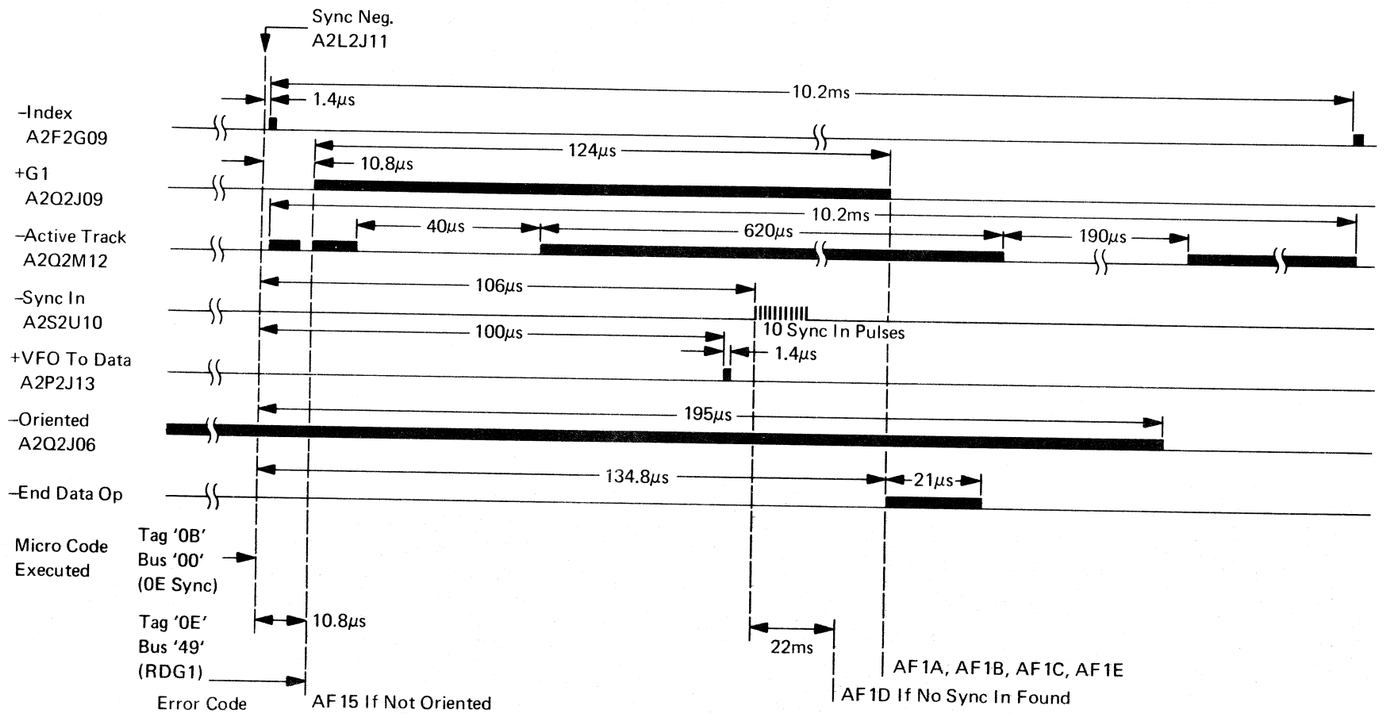
ROUTINE AF TEST 1 TIMING CHART



CG1193 Seq. 1 of 2	2747396 Part No. ( )	440204 21 Dec 73						

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ROUTINE AF TEST 1 SCOPING PROCEDURES

Routine AF Test 1 verifies that the Read G1 command can be executed and the physical address read to 5041 – the CE track and head used for this test. As a part of this test, the Read G1 Unoriented latch is also tested.

Most parts of this test are identical to the physical address verification performed in the initialization load. It is preferable to use this test for intermittent problems because looping is easier.

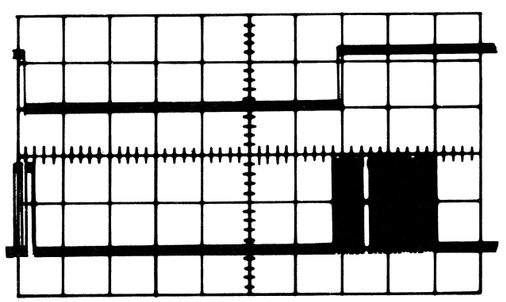
Scope Setup

Sync Ext(–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div X10 probes
Except as noted

Time: 0.1 ms/div

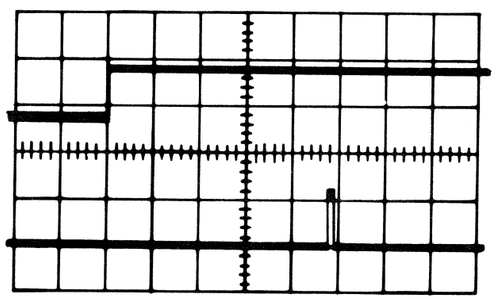
–Read OP OE
A2L2M02 (BD100)



+Tag Gate NPL
A2G2J11 (BF130) 0.2 volts/div X10 probes

During Tag Gate for the Read G1 command, the Oriented latch is sampled. If the Oriented latch is off, + G1 Unoriented latch is set and presented on Bus In under Tag Valid. If the Oriented latch is set, + G1 Unoriented is not formed. The pictures at the right show correct operation.

–Oriented
A2Q2J06 (BH130)



+G1 Unoriented
A2Q2J04 (BH130)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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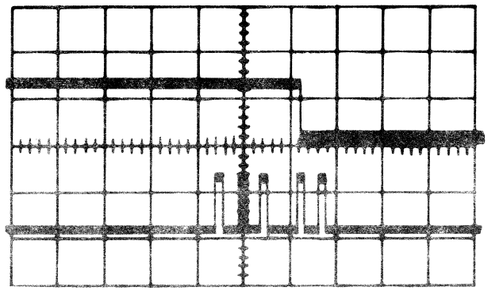
ROUTINE AF TEST 1 SCOPING PROCEDURES (continued)

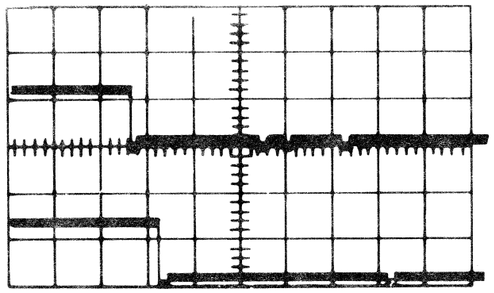
These pictures show key points in a Read G1 operation. The test points are arranged in more or less chronological order. A magnified view of the Read Mode area is shown on MICFL 1196.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

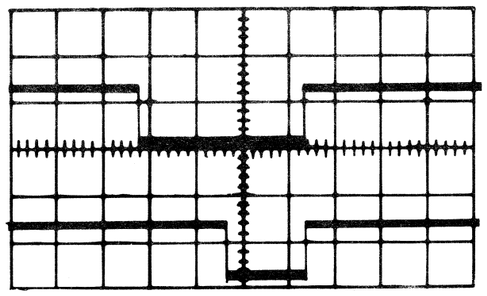
Sync Ext (–): –RAS TP
A2L2J11 (BD100)
Use triggered delayed sweep triggering
+G1 A2Q2J09 (BH120)
Time: 2 ms/div
Delayed Time: 20 µs/div
Vertical: 0.1 volts/div X10 probes
+G1 A2Q2J09 (BH120)
Alternate: A2P2G04 (BG140)
+Reset Fast Past Sync
A2P2U09 (BG140)



–Read Gate
A2Q2P09 (BH140)

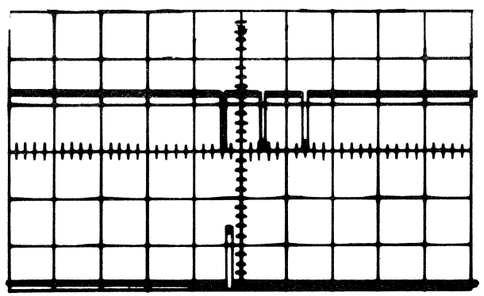


–Unsquelch
A2Q2M09 (BH140)



–Transfer Sector Count
A2Q2J07 (BH120)

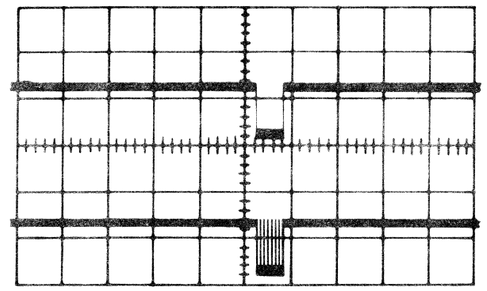
+PLO Mode
A2S2M02 (BC140)



–Reset Ctr.
A2P2B07 (BG100)

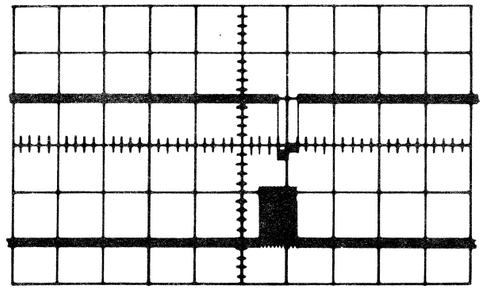
+VFO to Data
A2P2J13 (BG140)

–Read Mode
A2P2U02 (BG170)



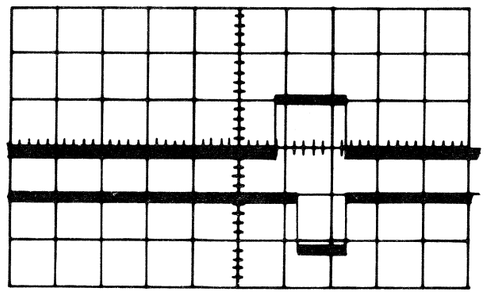
–Sync In
A2S2U10 (BC170)

–Xfer ECC Control
A2P2G08 (BG170)



–ECC Zeros Compare
A2S2U07 (BC150)

+End Data
A2P2S03 (BG170)



–End Data OP
A2P2S05 (BG170)

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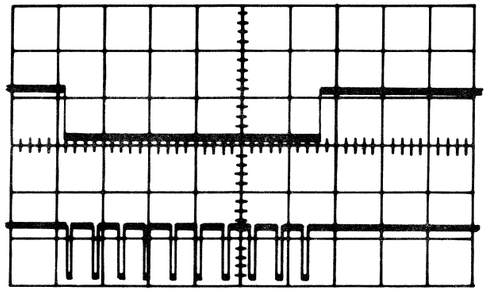
ROUTINE AF TEST 1 SCOPING PROCEDURES (continued)

To facilitate physical address verification problems, the data area has been magnified further for greater detail.

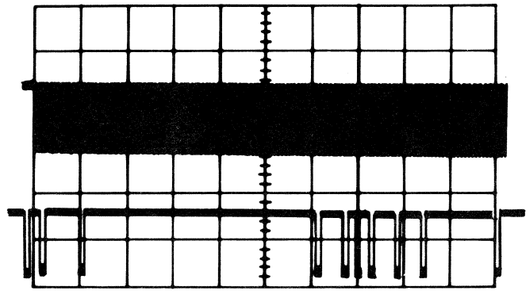
Sync Ext.(–): –RAS TP
A2L2J11 (BD100)
Vertical: 1 volts/div
Time: 2 ms/div using triggered delayed sweep, triggering on + G1 A2Q2J09 (BH120). Delayed time equal 20 μs/div times ten was used.

–Read Mode
A2P2U02 (BG170)



– Raw Read Data
A2T2D04 (BJ130)

Setup: Same as lower left

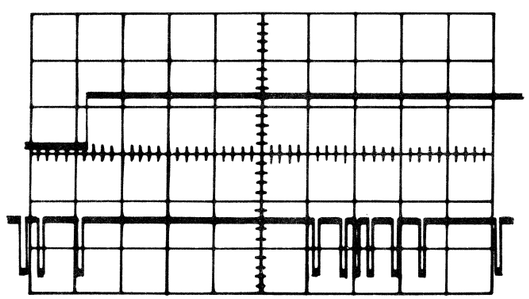


–Sync In
A2S2U10 (BC170)

– Standardized Data
A2T2G02 (BJ110)

Setup: Same as left

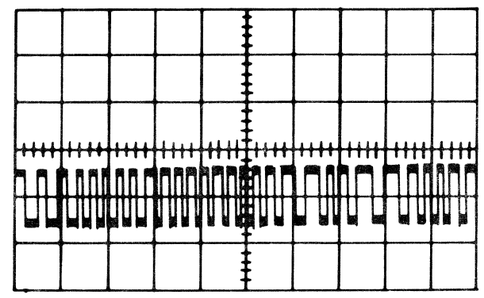
Sync Ext.(–): –RAS TP
A2L2J11 (BD100)
Vertical: 2 ms/div using triggered delayed sweep, triggering on + VFO to data A2P2J13 (BG140). Delay time of 5 μs/div with times 10 magnifier.



RW Data
A2T2B05 (BJ130)
A2T2D07 (BJ130)

Inputs added one input inverted
0.1 volts/div X10 probes

Note: Trace may appear inverted depending upon input arrangement and on which pulse is inverted.



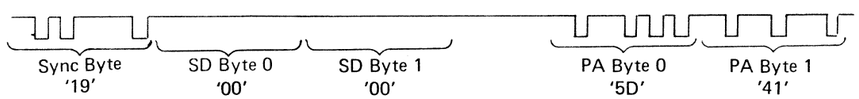
+ Not Index Data Good is active when a sync byte has been detected by the deserializer.

+ Not Index Data Good
A2Q2D10 (BH160)

–Standardized Data
A2T2G02 (BJ110)

The first three pulses on the Standardized Data line are decoded as a sync byte – HEX 19.

Following the sync byte are two bytes of HEX 00 which are the skip displacement bytes. The next pulses are the physical address bytes. Below right is a diagram with the bits decoded.



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE AF TEST 2 SCOPING PROCEDURES

Test 2 checks the Command Overrun circuit, and, indirectly, the Unoriented latch by executing a Read G1 operation and issuing a Write G2 at the latest permissible time. The program checks for No Command Overrun. The program again performs a Read G1 operation and, after a slightly longer wait, issues a Write G2 operation and expects to find a Command Overrun.

Note that Command Overrun is a result of a Write G2 operation that occurred following the turn-off of Oriented.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

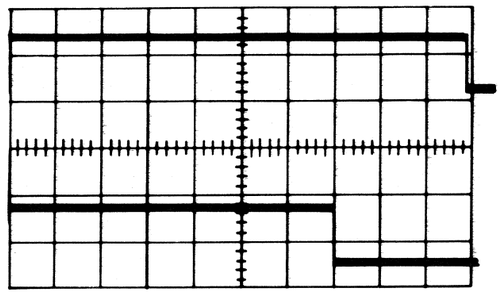
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volts/div

Time: 5 ms/div using triggered delayed sweep triggering on the second + G1 pulse A2Q2J09. Delay time is 20 μs/div.

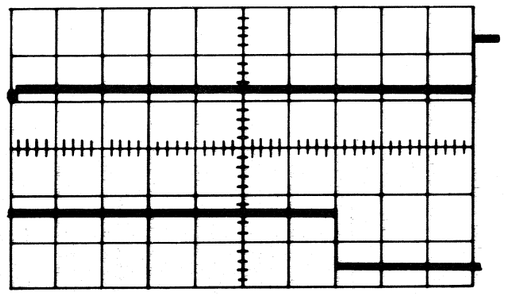
–G2
A2Q2D05 (BH110)

+ G1
A2Q2J09 (BH120)



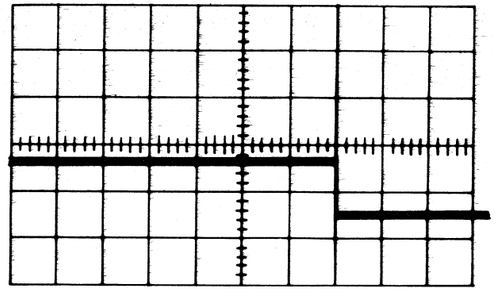
Same as above except that the delay time multiplier is changing to trigger on the fourth +G1 pulse.

– Oriented
A2Q2J06 (BH130)



– Command Overrun
A2Q2M05 (BH130)

+ G1
A2Q2J09 (BH130)



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ROUTINE AF TEST 3 SCOPING PROCEDURES

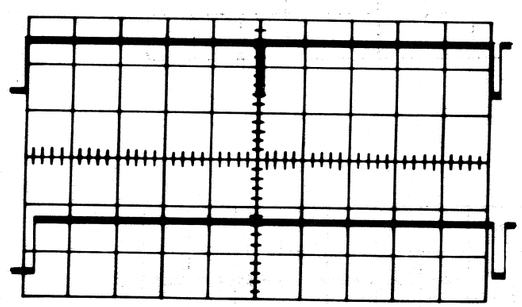
Test 3 checks that Command Overrun is activated if a nonorienting command is issued at Index Range Time. Command Overrun is tested to ensure that it turns on when a Write G2 and a Read G2 command are issued on successive revolutions at Index time.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond thepoint of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
Vertical: 0.1 volts/div X10 probes
Time : 2 ms/div

–Oriented
A2Q2J06 (BH130)

–Command Overrun
A2Q2M05 (BH130)



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ROUTINE AF TEST 4 SCOPING PROCEDURES

Test 4 checks that Storage Control turns around a Sync In pulse to produce a Sync Out pulse. On the next Sync In pulse, the Storage Control does not respond to Sync In with a Sync Out pulse. This causes the Sync Out Timing Error latch to set which, in turn, causes an ending condition by forcing Op End.

The test then issues a Write G2 operation and holds Tag Gate active for 100 microseconds and checks for Status Overrun. Tag Gate is then dropped and a check is made that Status Overrun is reset.

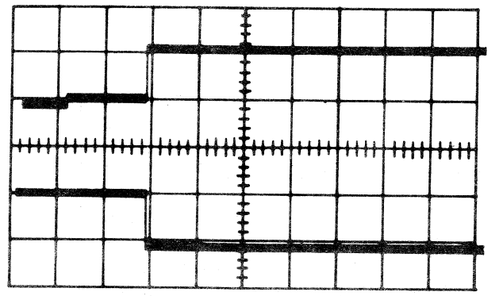
Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Vertical: 0.1 volt/div X10 probes

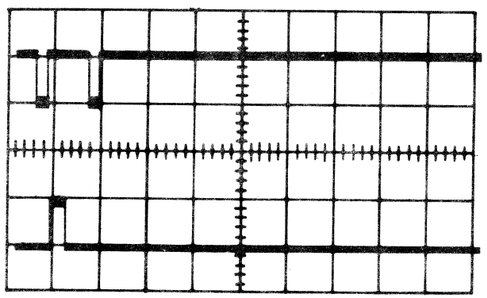
Time: 2 ms/div using triggered delayed sweep triggering on – Write Mode A2P2U12 (BG140). Delay time is 1 μs/div.

–Write Mode
A2P2U12 (BG140)
Alternate: A2Q2D11 (BH160)



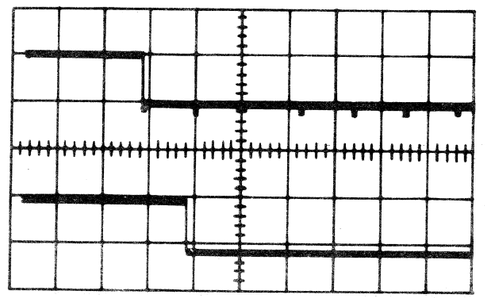
+ FMT G1
A2Q2M13 (BH140)

–Sync In
A2S2U10 (BC170)



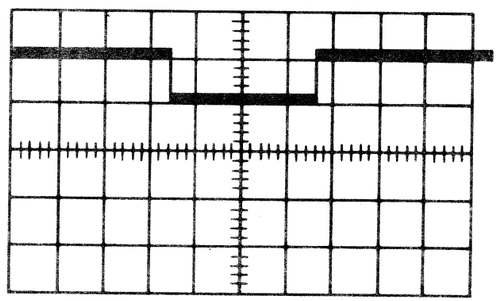
+ MST Sync Out
A2S2U11 (BC170)

–Sync Out Timing Error
A2S2S10 (BC170)



–OP End
A2P2U03 (BC170)

–Status Overrun
A2P2P09 (BG140)



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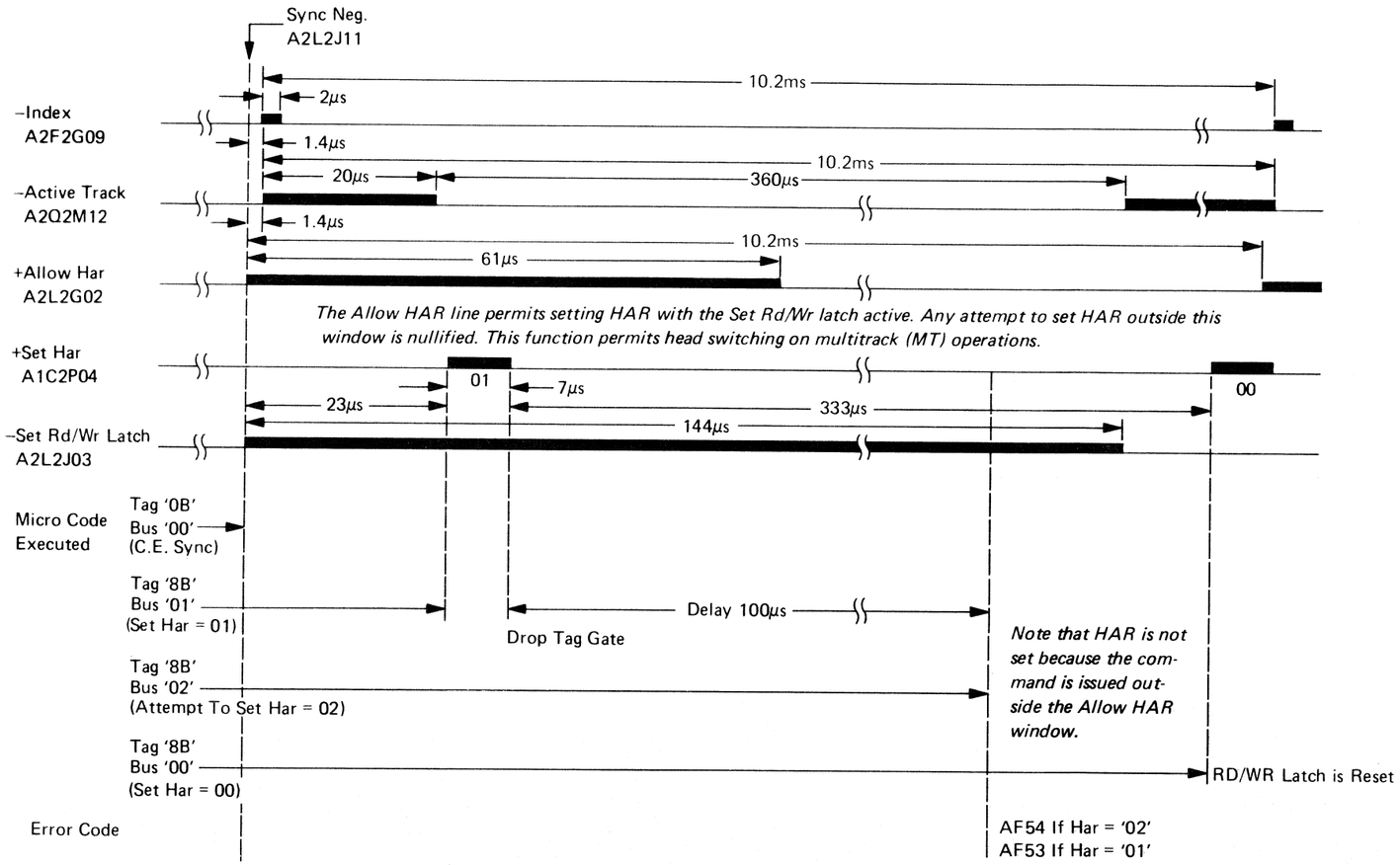
ROUTINE AF TEST 5 TIMING CHART



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ROUTINE AF TEST 5 SCOPING PROCEDURES

On Record Overflow and Multitrack operations, the setting of the Head Address Register must be adjusted immediately following Index (Allow HAR is the signal used). Test 05 attempts to change the Head Address Register twice. The first attempt shown in the picture must be successful. The second attempt that comes too late must not be successful.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

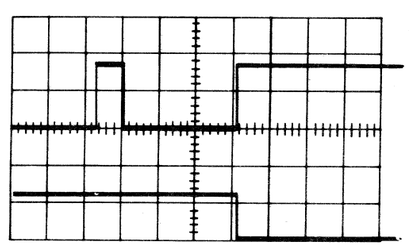
10 μs/div.

+Device Tag Gate NPL
A2L2J02 (BD230)

0.2 volts/div X10 probe

+Allow HAR
A2Q2M11 (BH170)

0.1 volts/div X10 probe



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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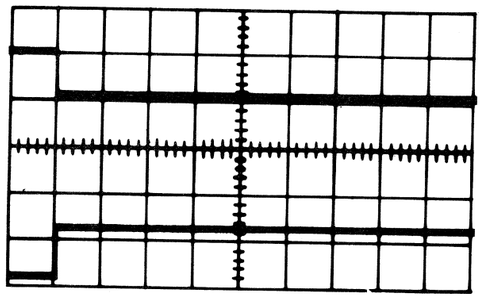
ROUTINE AF TEST 5
SCOPING PROCEDURE
MICFL 1203

ROUTINE AF TEST 6 SCOPING PROCEDURES

Test 6 writes a full track Record 0 Count field. It must successfully complete without a Track Overrun indication (prior to Index time).

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

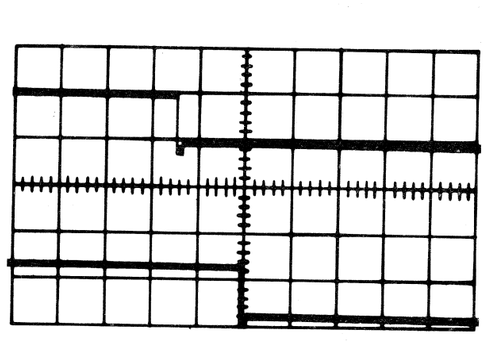
10 μs/div



–G2
A2Q2D05 (BH110)

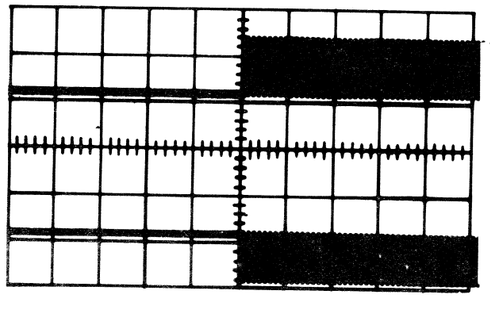
+ RD/WR Op Dld
A2Q2B10 (BH100)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.



–Write Gate
A2Q2G10 (BH140)

–Write Mode
A2P2U12 (BG140)

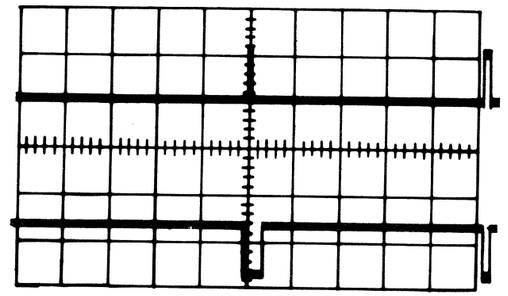


+ Sync Out MST
A2S2U11 (BC170)

–Sync In
A2S2U10 (BC170)

2 ms/div

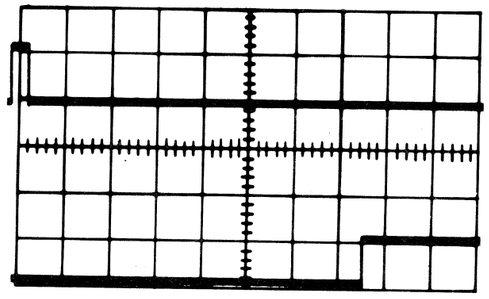
+ End Data
A2P2S03 (BG170)



+ Recycle
A2G2S10 (BF160)

Time as above with delayed sweep at 100 μs/div to expand the pulses.

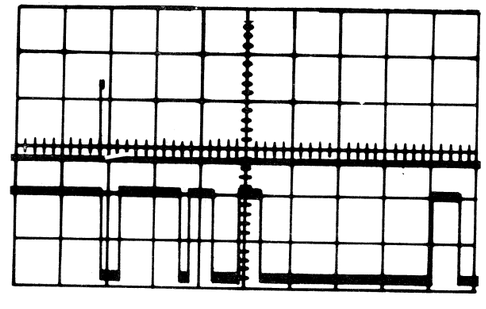
+ End Data
A2P2S03 (BG170)



+ Recycle
A2G2S10 (BF160)

Delayed sweep set at 10 μs/div so that response comes approx. at fall of End Data above

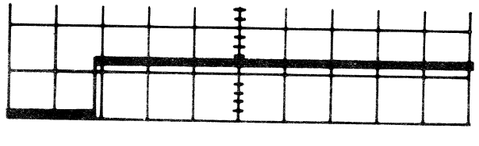
+ Response NPL
A2G2S03 (BF160)
0.2 volts/div X10 probes



+ Normal End NPL
A2K2D11 (BE160)

0.1 volts/div X10 probes
Time as above

–End Data Op
A2P2S05 (BG170)



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ROUTINE AF TEST 7 SCOPING PROCEDURES

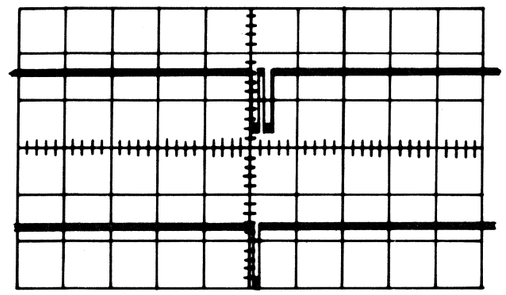
Test 7 duplicates test 6 except that the byte count is increased to cause a Track Overrun. An error is indicated if Track Overrun is not received.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)
2 ms/div

–End Data Op
A2P2S05 (BG170)
0.1 volts/div X10 probes

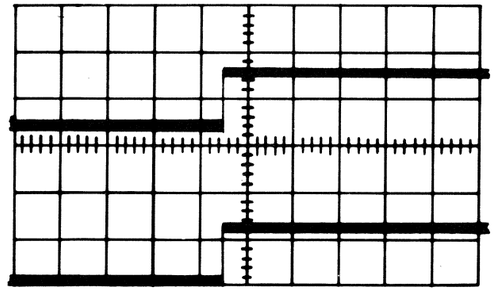
–Trk Ovrn* ECC Data Chk
A2Q2J05 (BH140)
0.1 volts/div X10 probes



Same as above except delayed sweep is used to expand pulses at 2 μs/div.

–End Data OP
A2P2S05 (BG170)
0.1 volts/div X10 probes

–Trk Ovrn* ECC Data Chk
A2Q2J05 (BH140)
0.1 volts/div X10 probes



CG1206	2747124
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ROUTINE AF TEST 8 SCOPING PROCEDURES

Test 8 ensures that on a Format operation, Write Gate and I Write Sense remain active after the data transfer to erase the remainder of the track. Device Bus In Bit 5 during this time is described as I Write Sense. Device Bus In Bit 5 must be on during Write Gate time and off after Write Gate falls.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

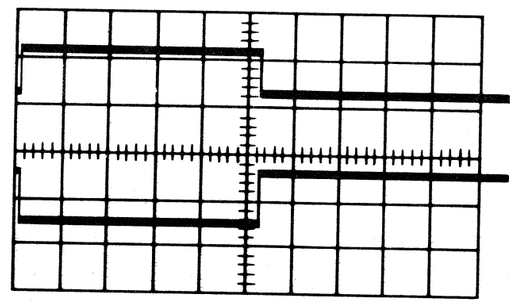
Time: 1 ms/div

Vertical: 0.1 volts/div X10 probes.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

+ Device BI Bit 5 MST
A2F2S10 (BA160)

–Write Gate Suppressed
A2Q2P07 (BH140)



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ROUTINE AF TEST 8
SCOPING ROUTINE
MICFL 1210

ROUTINE AF TEST 9 SCOPING PROCEDURES

Routine AF test 9 attempts to read a record erased in test 8. The result should be a No Sync Byte Found indication.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

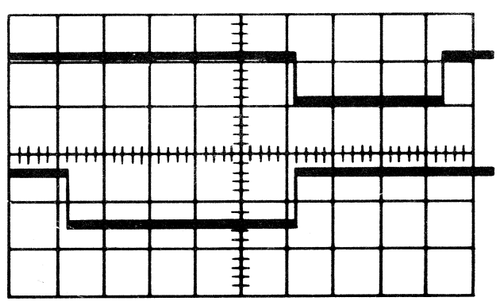
Sync Ext. (–): –RAS TP
A2L2J11(BD100)

Time: 10 μs/div

Vertical: 0.1 volts/div
X10 probes.

–No Sync Found
A2P2M12 (BG140)

–G2
A2Q2D05 (BH110)



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ROUTINE AF TEST 9
SCOPING ROUTINE
MICFL 1212

ROUTINE AF TEST 0A SCOPING PROCEDURES

Routine AF

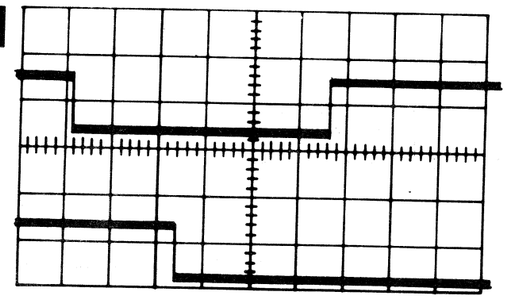
Test OA writes an AM (G3) record. Picture 1 shows the OP decode and Write Gate. Picture 2 shows the Write Data-note AM area and data area. The upper trace shows Sync In pulses for the data. Picture 3 shows the ECC area and the Normal End Pulse.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

10 μs/div

–G3 (Write G3 OP) 0.1 volts/div X10 probes
A2Q2D02 (BH110)

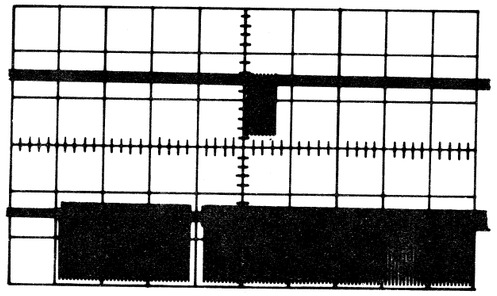
1



–Write Gate
A2Q2G10 (BH140) 0.1 volts/div X10 probes
–Address Mark
A2Q2U06 (BH140)

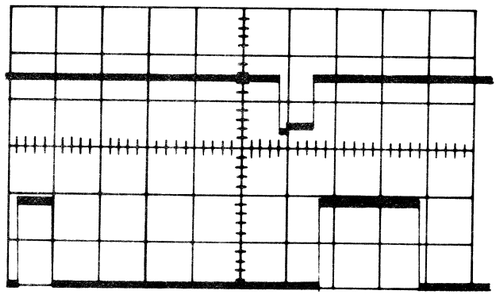
–Sync In 0.1 volts/div X10 probes
A2S2U10 (BC170)

2



–Wr Data TP 0.1 volts/div X10 probes
A2T2B04 (BJ130)

3



–Xfer ECC 0.1 volts/div X10 probes
A2P2G08 (BG170)

+ Normal End NPL 0.2 volts/div X10 probes
A2K2D11 (BE160)

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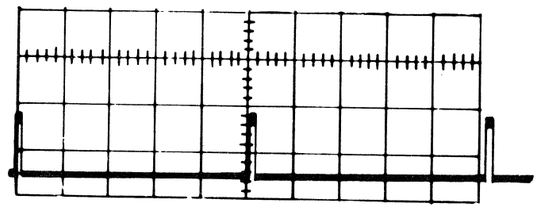
Picture 4 shows the entire area of the test which is slightly more than 1 revolution. Picture 5 is the right pulse from No. 4 expanded with delayed sweep and shows the relation to G3 for read. Picture 6 shows the relationship of G3 to Raw Read Data and the Address Mark.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

4



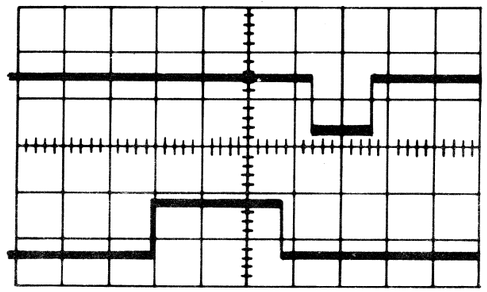
2ms/div

+ G1 0.1 volts/div X10 probes
A2Q2J09 (BH120)

Delayed sweep. Last pulse above is displayed on lower trace below at 50 μs/div

– G3 (Read G3 OP) 0.1 volts/div X10 probes
A2Q2D02 (BH120)

5

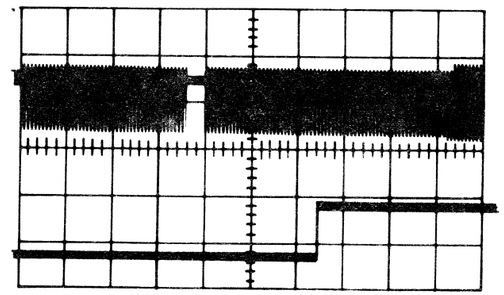


+ G1 0.1 volts/div X probes
A2Q2J09 (BH120)

Delayed sweep speed expanded to 10 μs/div

– Raw Read Data 0.1 volts/div X10 probes
A2T2D04 (BJ130)

6

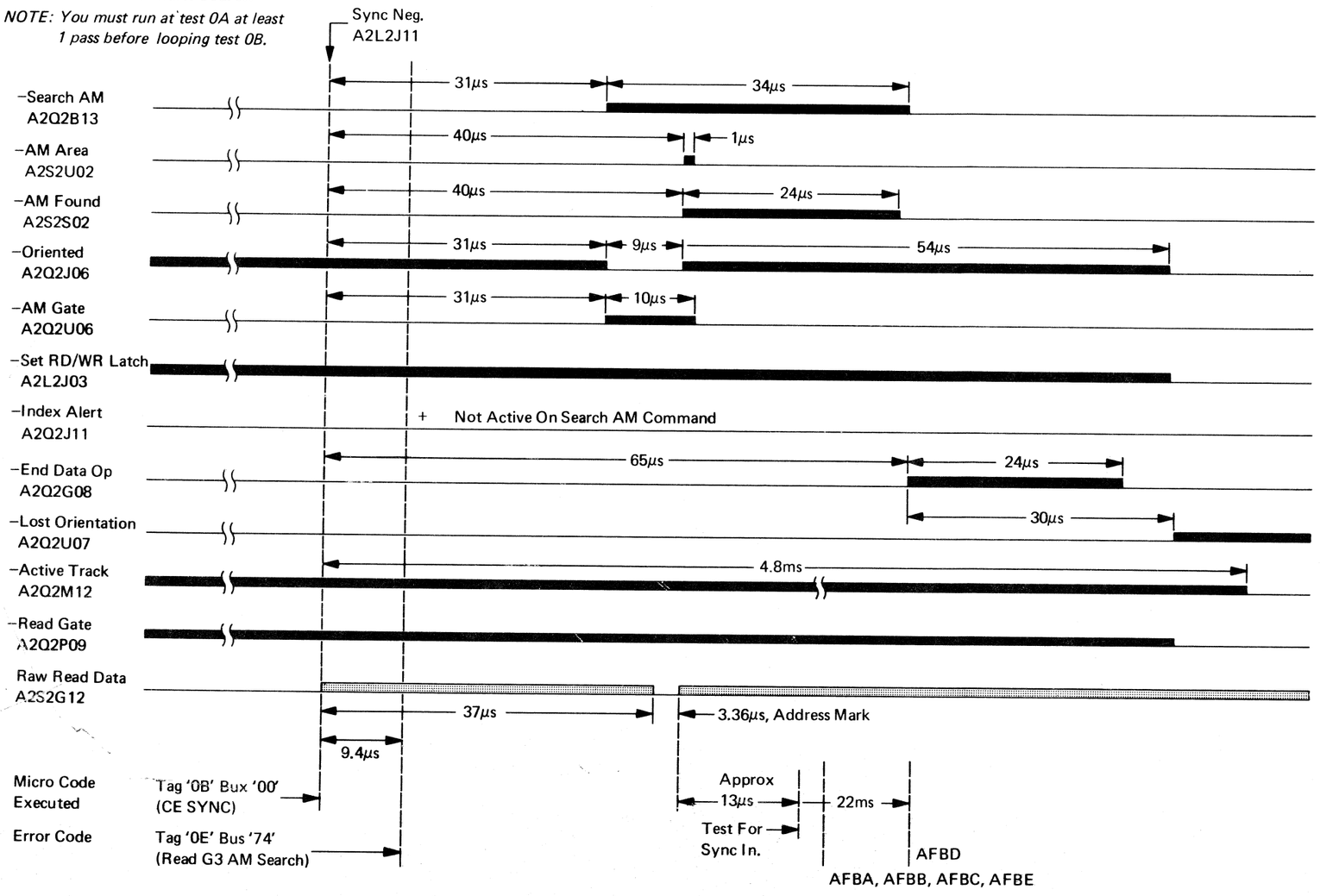


– G3 (as above) .1 volts/div X10 probes
A2Q2D02 (BH110)

ROUTINE AF TEST 0B TIMING CHART

Read G3 Address Mark Search

NOTE: You must run at test 0A at least 1 pass before looping test 0B.



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ROUTINE AF TEST 0B SCOPING PROCEDURES

Routine AF

Test 0B uses the record created in Test 0A to search AM

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

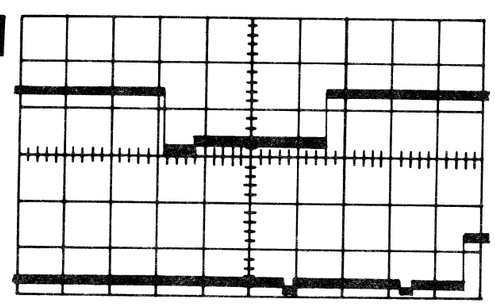
1

–Search AM
A2Q2B13 (BH130)

10 μs/div
0.1 volts/div X10 probes

–Read Gate
A2Q2P09 (BH140)

0.1 volts/div X10 probes



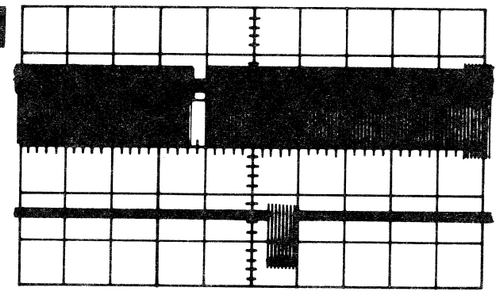
2

–Raw Read Data
A2T2D04 (BJ130)

0.1 volts/div X10 probes

–Sync In
A2S2U10 (BC170)

0.1 volts/div X10 probes



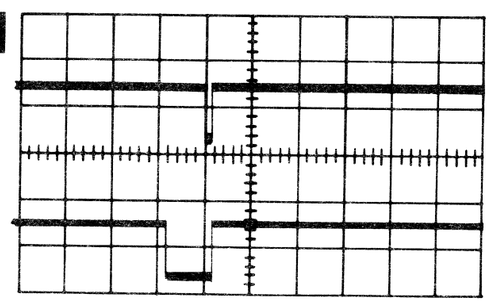
3

–AM Area
A2S2U02 (BC140)

0.1 volts/div X10 probes

–Address Mark Gate
A2Q2U06 (BH140)

0.1 volts/div X10 probes

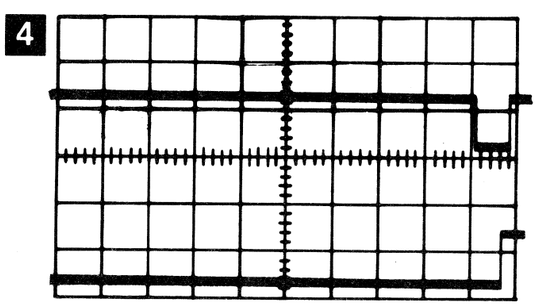


4

–AM Area
A2S2U02 (BC140)

Delayed sweep of
1 μs/div to expand
pulses as in picture 3.

–Address Mark Gate
A2Q2U06 (BH140)



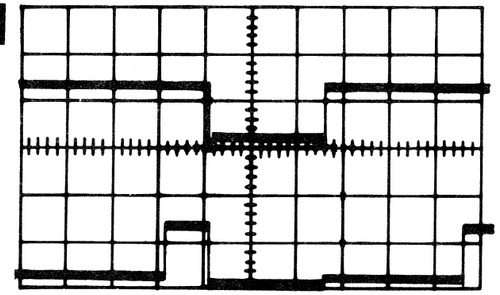
5

–AM Found
A2S2S02 (BC140)

10 μs/div
0.1 volts/div X10 probes

–Oriented
A2Q2J06 (BH130)

0.1 volts/div X10 probes



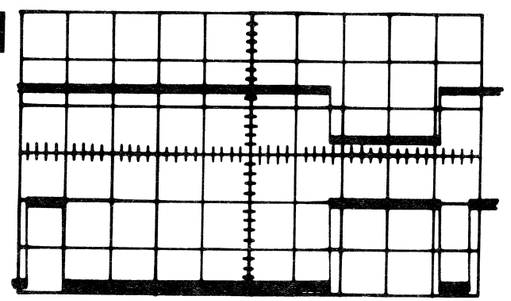
6

–End Data Op
A2P2S05 (BG170)

0.1 volts/div X10 probes

+Normal End NPL
A2K2D11 (BE160)

0.2 volts/div X10 probes



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ROUTINE AF TEST OC SCOPING PROCEDURES

Routine AF Test OC executes a Format Erase operation. Then an AM Search is initiated. No AM Found is the expected result.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

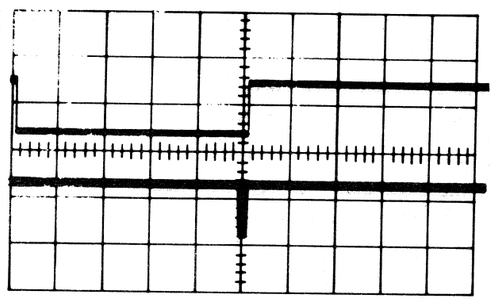
1

–Write Gate
A2Q2G10 (BH140)

2 ms/div
0.1 volts/div X10 probes

Note Write Gate active until Index time

–Index
A2F2G09 (BH140)



2

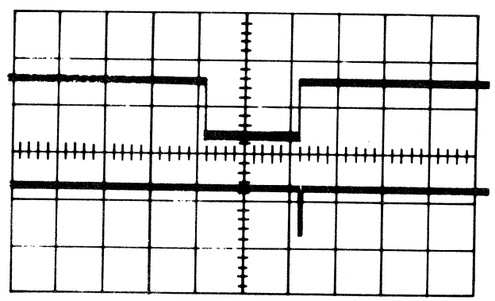
–Search AM
A2Q2B13 (BH130)

5 ms/div
0.1 volts/div X10 probes

Comes up at Start OP on second revolution.

–No AM Found
A2Q2J13 (BH140)

0.1 volts/div X10 probes



Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

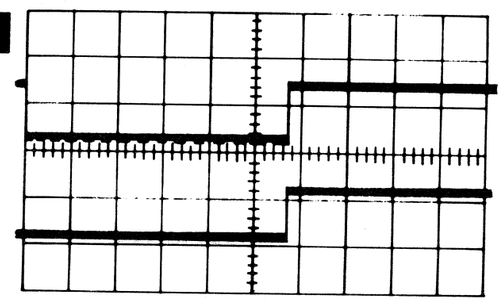
3

–End Data OP
A2P2S05 (BG170)

0.1 volts/div X10 probes

–No AM found
A2Q2J13 (BH140)
Same as picture 2. Delayed sweep of 5 μs/div

0.1 volts/div X10 probes



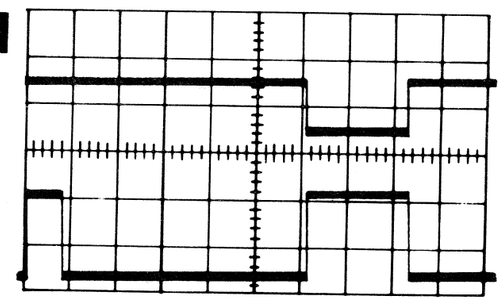
4

–End Data OP
A2P2S05 (BG170)

0.1 volts/div X10 probes

+Check End
A2K2D05 (BE160)

0.1 volts/div X10 probes



CG1217	2747126
Seq. 1 of 2	Part No. ( )

440200	440202	440203				
25 Jun 73	7 Sept 73	2 Nov 73				

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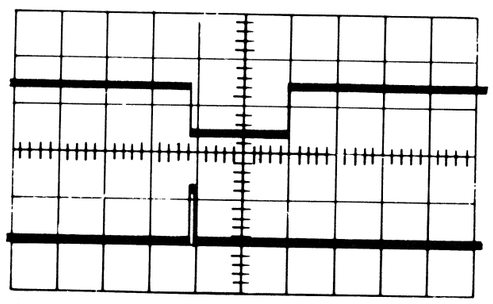
ROUTINE AF TEST OD SCOPING PROCEDURES

Test OD writes a special G1 record. Instead of bring-up Write Mode at approximately 120 microseconds after Index, it comes up at approximately 260 microseconds after Index.

Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

–Write Gate
A2Q2G10 (BH140)
5 ms/div
0.1 volts/div X10 probes

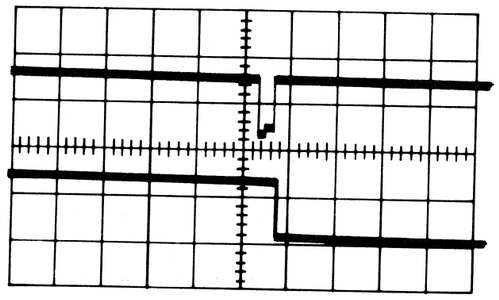
+FMT G1
A2Q2M13 (BH140)
0.1 volts/div X10 probes



Delayed sweep at 50 μs/div
to expand FMT G1 from above.

–Write Mode
A2P2U12 (BG140)
0.1 volts/div X10 probes

+FMT G1
A2Q2M13 (BH140)
0.1 volts/div X10 probes



Note: When scoping, be aware that once an error is detected futher testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

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ROUTINE AF TEST OD
SCOPING ROUTINE
MICFL 1219

ROUTINE AF TEST 0E SCOPING PROCEDURES

This routine writes a normal G1 Gap and Home Address. Since test 0D writes a Special G1. This test may also be used to ensure that a normal G1 Gap is on the CE track (track 1 only).

The accompanying pictures show normal timings for a G1 operation.

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

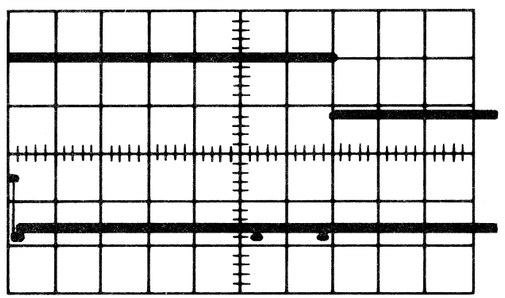
Sync Ext. (–): –RAS TP
A2L2J11 (BD100)

Time: 5 ms/div using
triggered delayed sweep.
Triggered plus external on
+FMT G1 A2Q2M11 (B H140).
Delay time 20 μs/div.
Vertical: 0.1 volts/div X 10 probes.

+ FMT G1
A2Q2M11 (BH140)
Alternate: A2P2P02 (BG140)

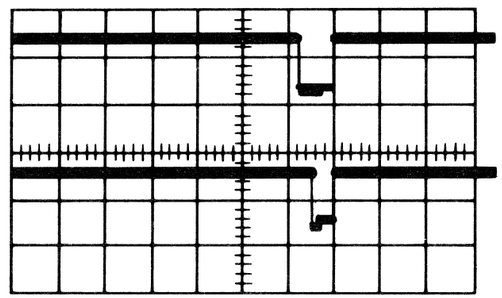
–Write Gate
A2Q2G10 (BH140)

Also:
–Address Mark Gate
A2Q2U06 (BH140)



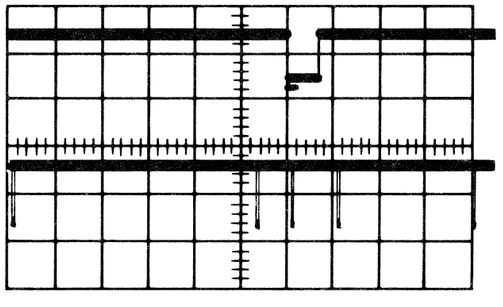
–Run ECC
A2P2S13 (BG170)

–Xfer ECC
A2P2G08 (BG170)



–Write Mode
A2P2U12 (BG140)

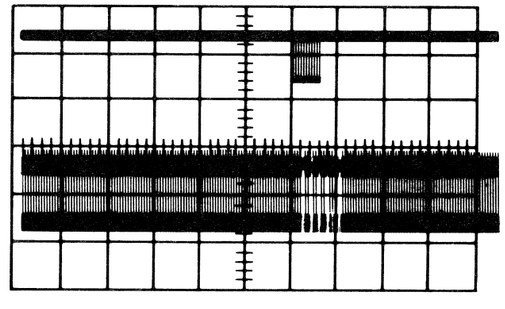
–Reset Ctr
A2P2B07 (BG100)



–Sync In
A2S2U10 (BC170)

Use X10 to display 10 Sync In pulses and to expand the Write Data below.

–Wr Data TP
A2T2B04 (BJ130)



CG1221	2747616	440202	440203					
Seq. 1 of 1	Part No. ( )	7 Sept 73	2 Nov 73					

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ROUTINE B0 – REFORMAT CE TRACKS UTILITY PROGRAM

DESCRIPTION

The purpose of Routine B0 is to provide the CE with a method of reformatting any specified track on the CE cylinder (349).

The routine formats a single track (head number specified by CE parameter 1) and writes a series of records defined by CE parameter 2. Parameter 2 allows the CE to specify that either a Normal or a Defective Flag be written in the Home Address, and that either a Normally Positioned or an Extended Positioned (+ 128 byte) Home Address be written on the track.

If the Defective Flag is specified, the routine writes an HA field (G1), R0 Count field (G2) and an 8-byte R0 Data field (G2). The R0 Count field points to the same track as the alternate.

If the Normal Flag is specified, the routine writes an HA field (G1), R0 Count field (G2), an 8-byte R0 Count field (G2), R1 Count field (G3) and a 256-byte R1 Data field (G2). The 256-byte Data field consists of a repeated 4-byte pattern of '77 77 FF AA'.

After writing the above records, the routine reads back each record and checks for any errors.

Parameters 1 and 2 must be entered by the CE. Default values in these parameters cause an error display.

TABLE OF OPERATIONS

Operation NR.	Operation Type	Tag/Bus Value	Byte CTR Value	Save Data Switch=	Data Pattern Name
1	READ G1	T'0E'B'49'	9	1	
2	FMT G1	T'0F'B'49'	9	—	Logical HA
3	FMT SPCL G1	T'0F'B'C9'	9	—	Logical HA
4	FMT G2	T'0F'B'6D'	13	—	R0 Count
5	FMT G2	T'0F'B'68'	8	—	R0 Data
6	FMT G3	T'0F'B'5D'	13	—	R1 Count
7	FMT G2	T'0F'B'60'	256	—	R1 Data
8	READ G1	T'0E'B'49'	9	0	—
9	READ G2	T'0E'B'6D'	13	0	—
10	READ G2	T'0E'B'68'	8	0	—
11	READ G3	T'0E'B'5D'	13	0	—
12	READ G2	T'0E'B'60'	256	0	—

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedure.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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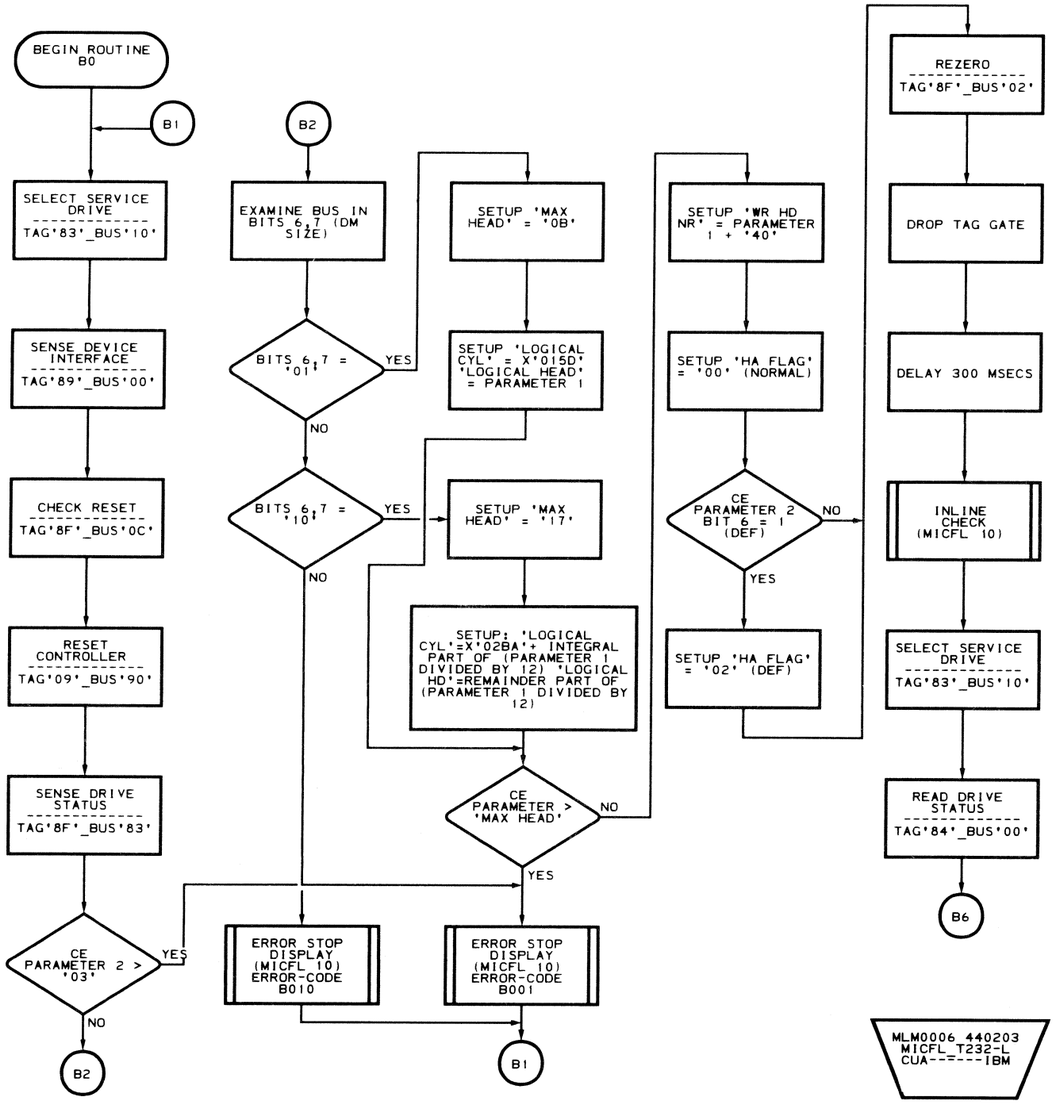

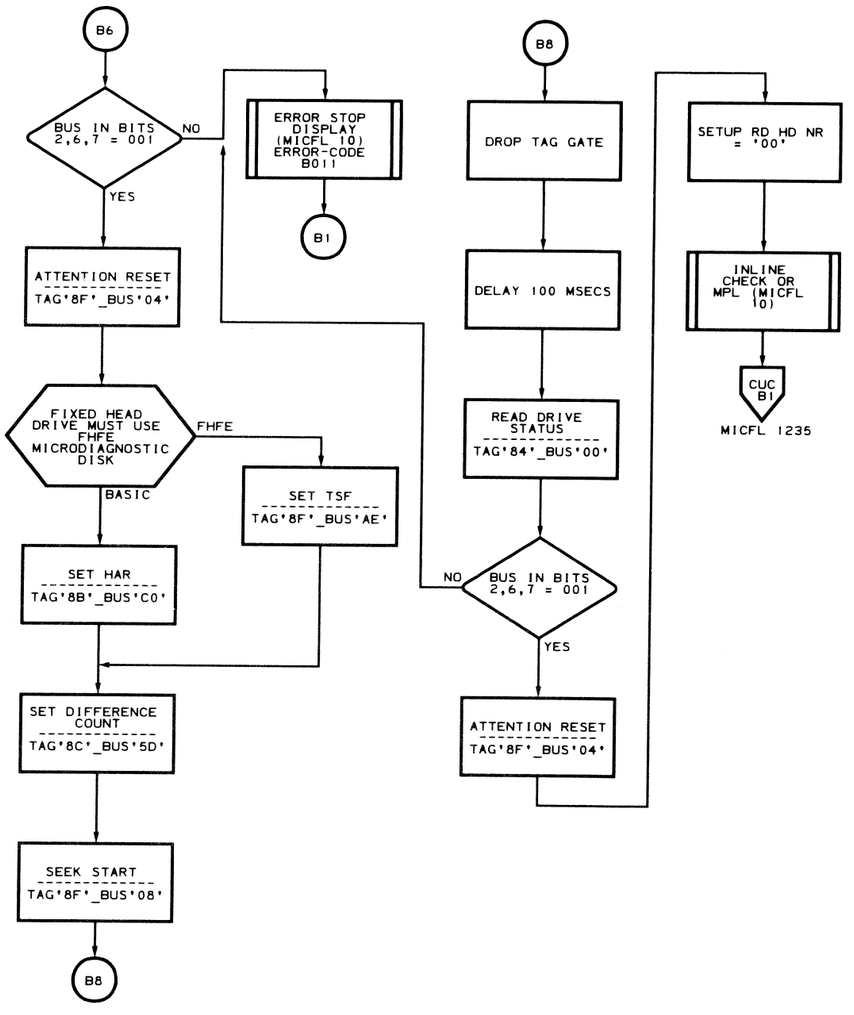

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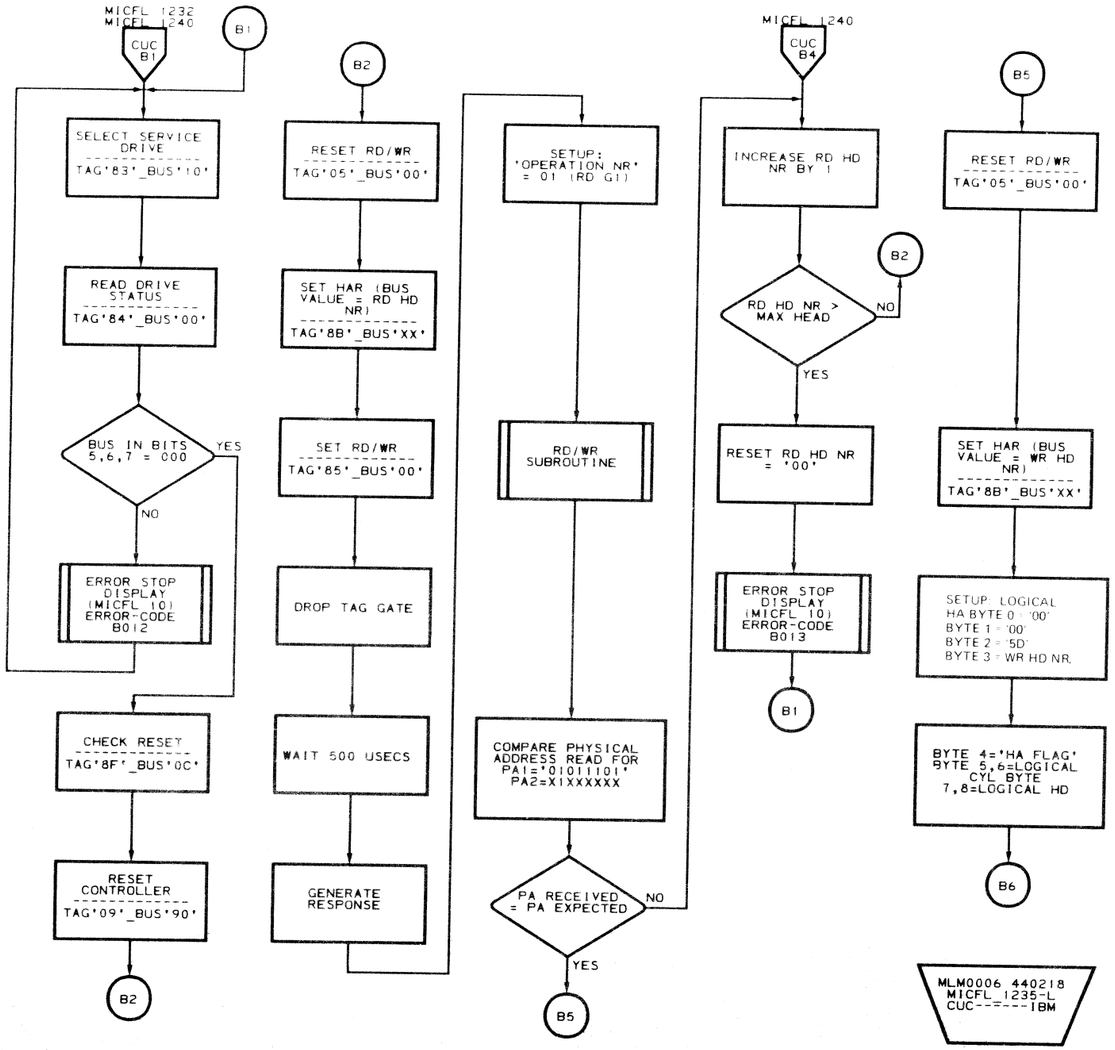
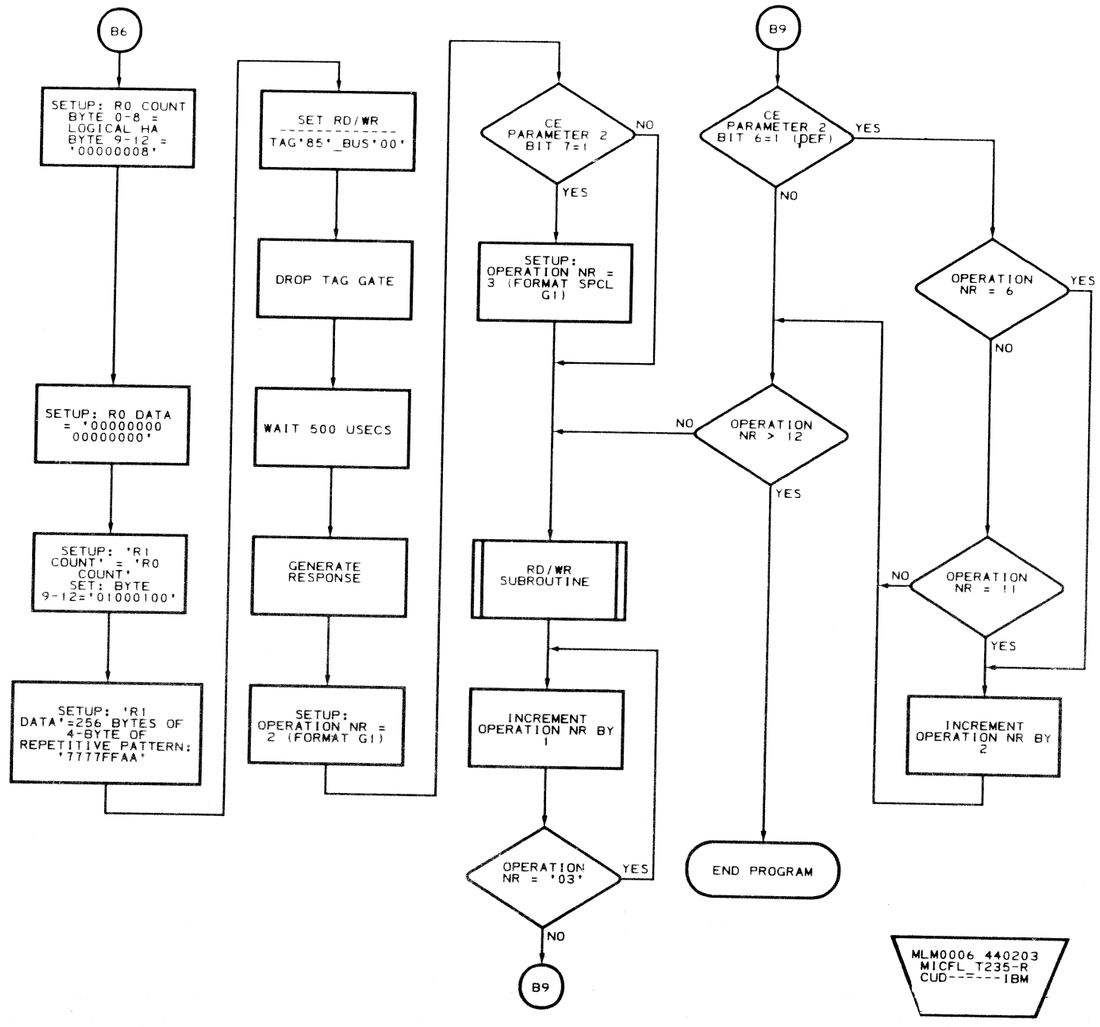
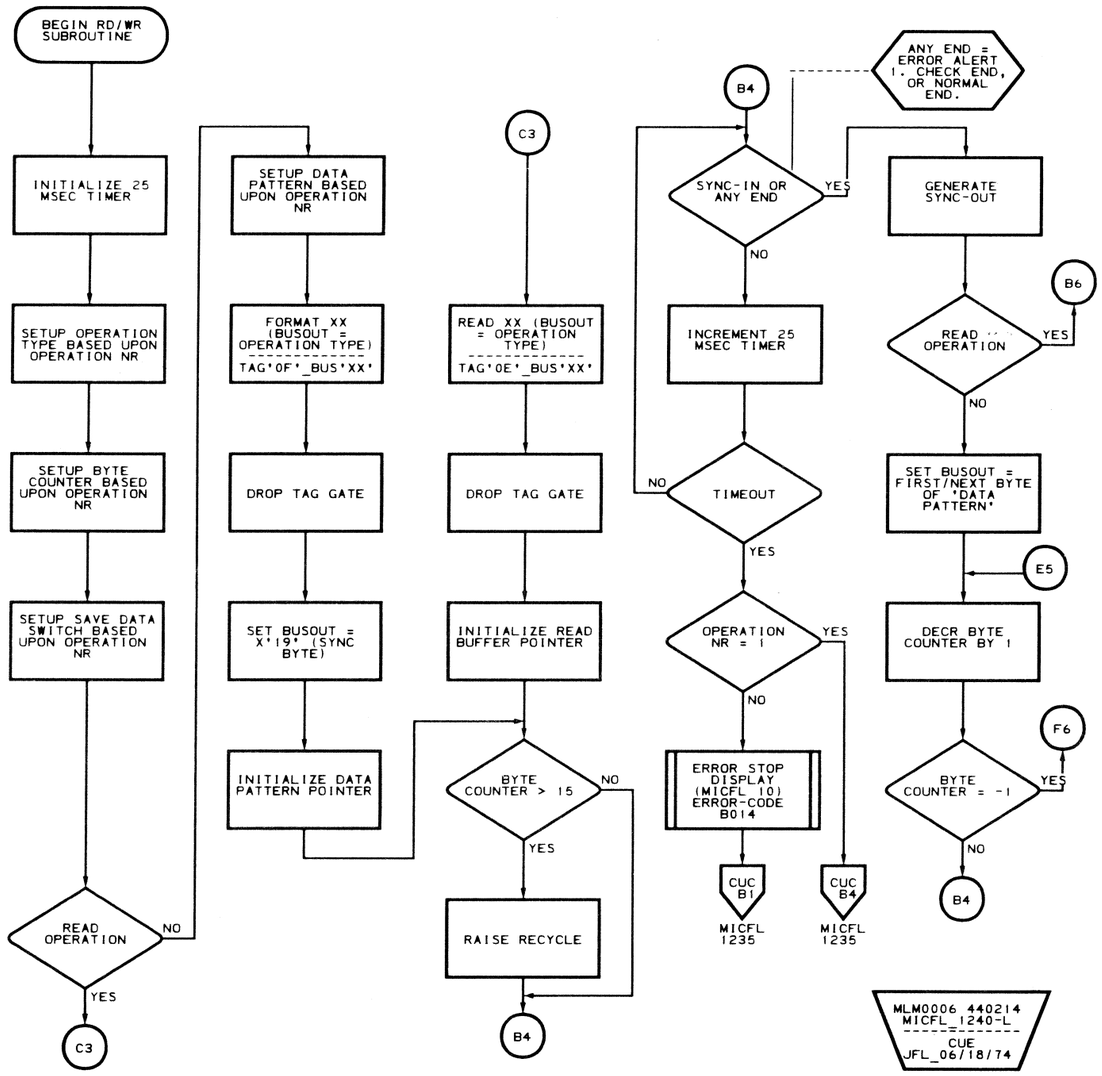
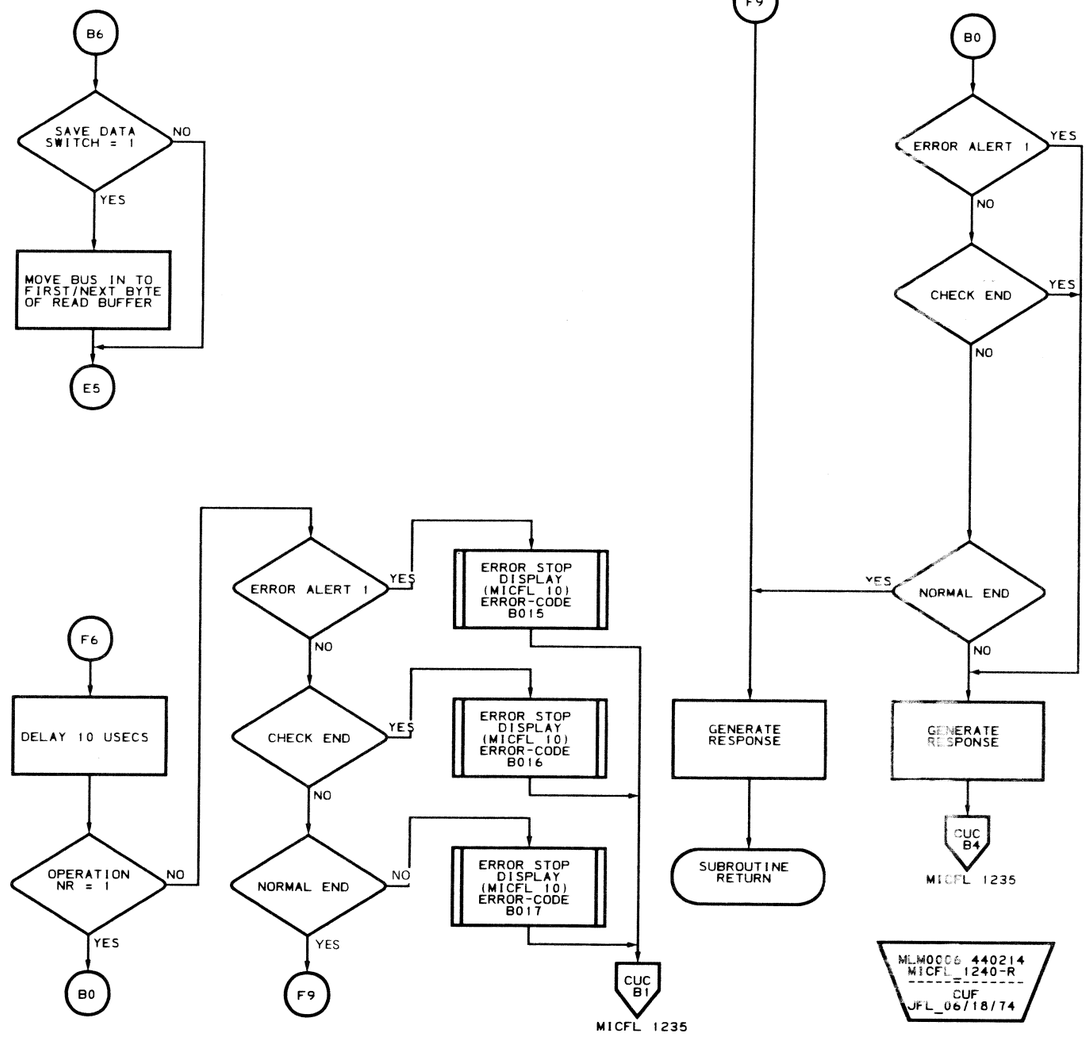
REFORMAT CE TRACKS UTILITY (Routine B0)









CG1232	2747754	440203	440214	440218	440223			
Seq. 2 of 2	Part No.( )	2 Nov 73	17 Jun 74	5 Aug 74	14 Mar 75			

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ROUTINE B1 – READ TEST

DESCRIPTION

Routine B1 reads all records on a track or cylinder and verifies successful operation by checking for no ECC Data Check.

In normal (default) operation, Routine B1 reads all records on the even-numbered tracks of the CE cylinder (349) beginning with Track 0. These tracks are prewritten read test tracks.

Prewritten CE tracks contain the following data:

1. Standard Home Address field (may have skip displacement)
2. Standard R0
3. 256 byte R1 with a 4-byte repetitive pattern of '77 77 FF AA'

Optional parameter entries may be used to select any single cylinder or head for testing. Cylinder selection is not limited to the default CE cylinder, but may be any value cylinder or head on the data module. With the exception of the Home Address and Count fields, the data read is not stored but is examined for ECC Data Check at the end of each record.

The read test bypasses any defective flagged tracks and is capable of reading any valid type of skip displacement on a track including:

Moved HA field
Moved fields: Count, Key, or Data
Split fields: Key or Data

A third parameter may be entered to force the routine into either a HA Only or Full Track Scope-Loop Mode in which all error analysis is suspended.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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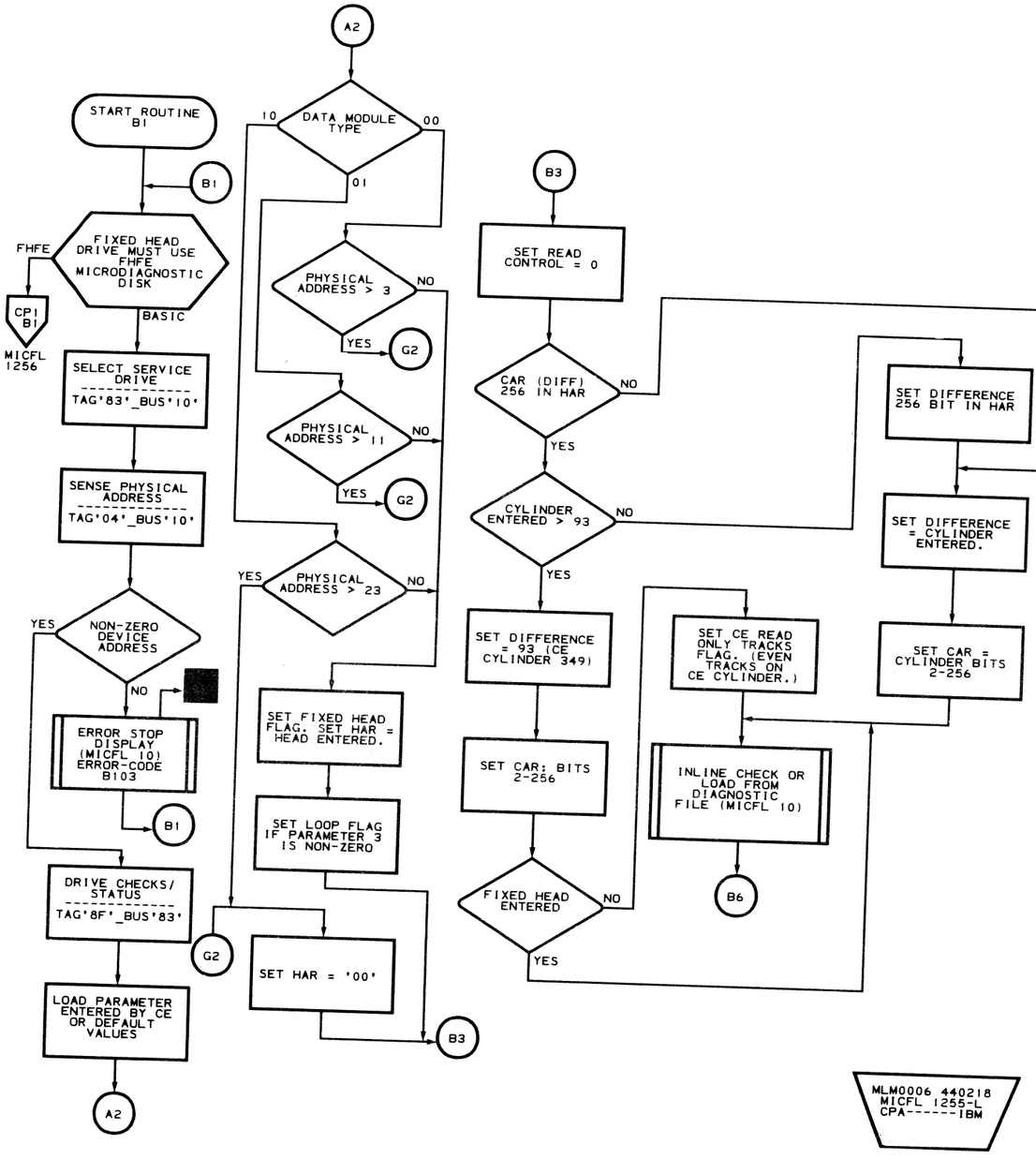
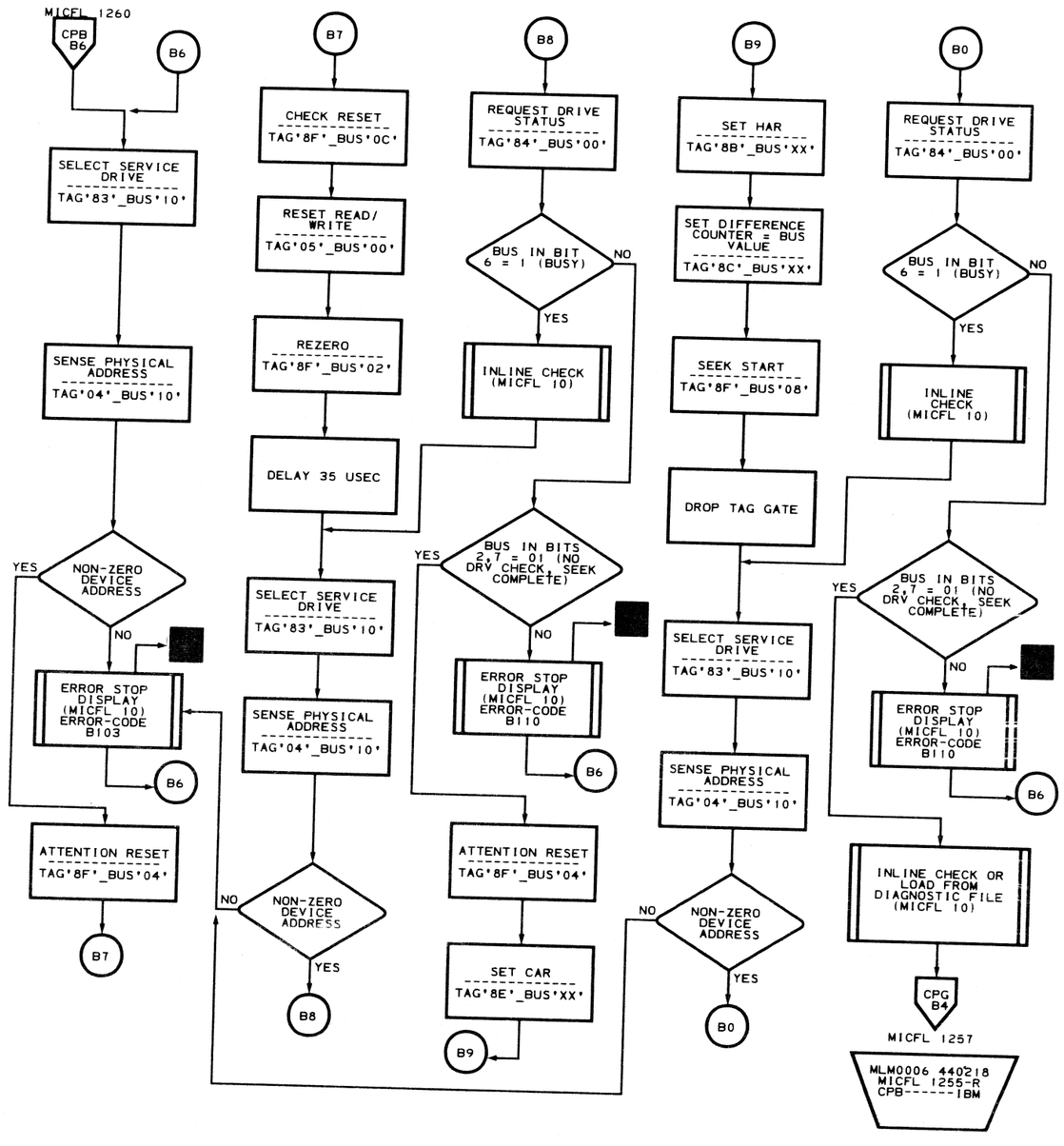
READ TEST (Routine B1)





CG1255 Seq. 1 of 2	2747127 Part No.( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440218 5 Aug 74			

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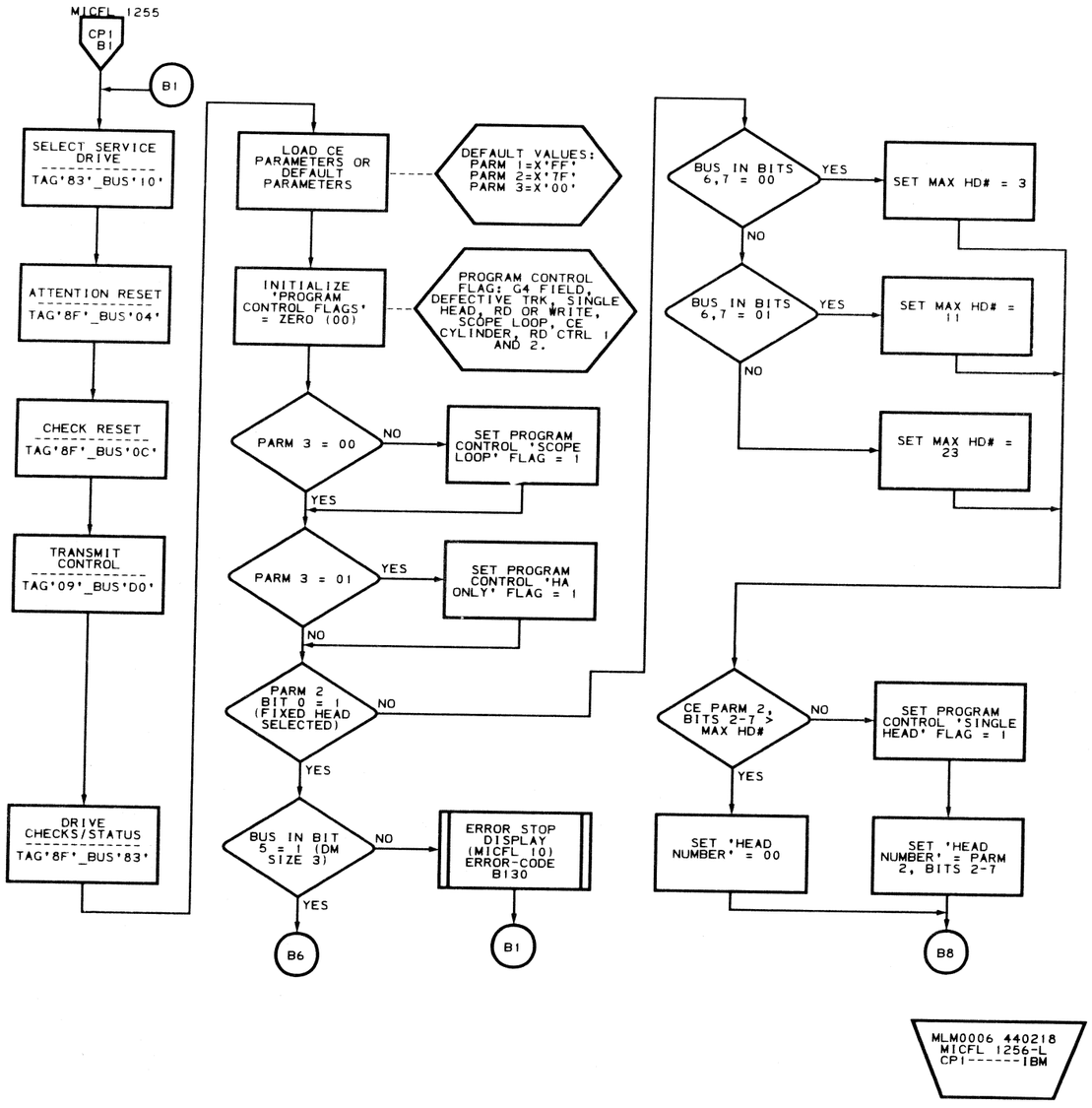

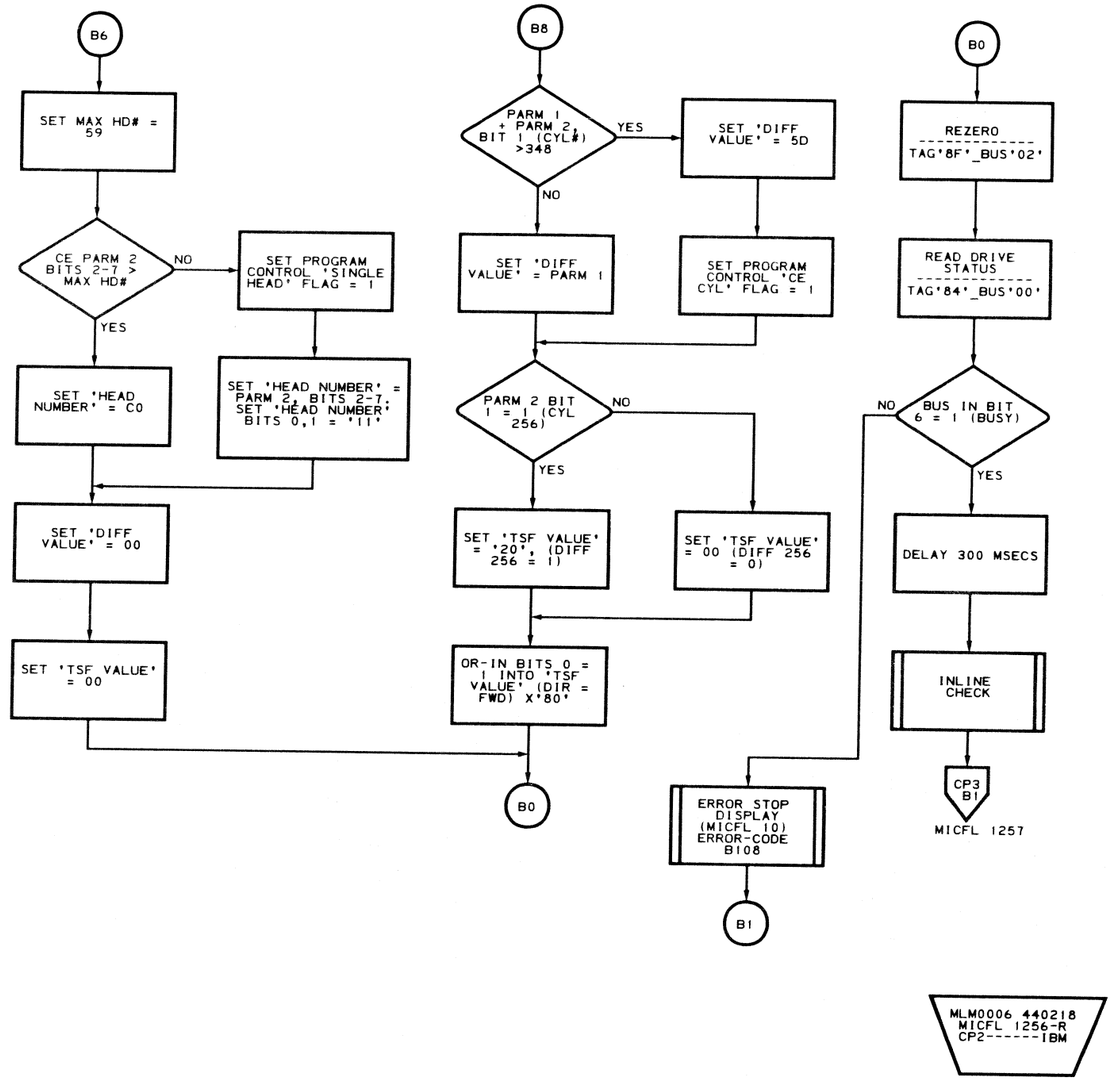

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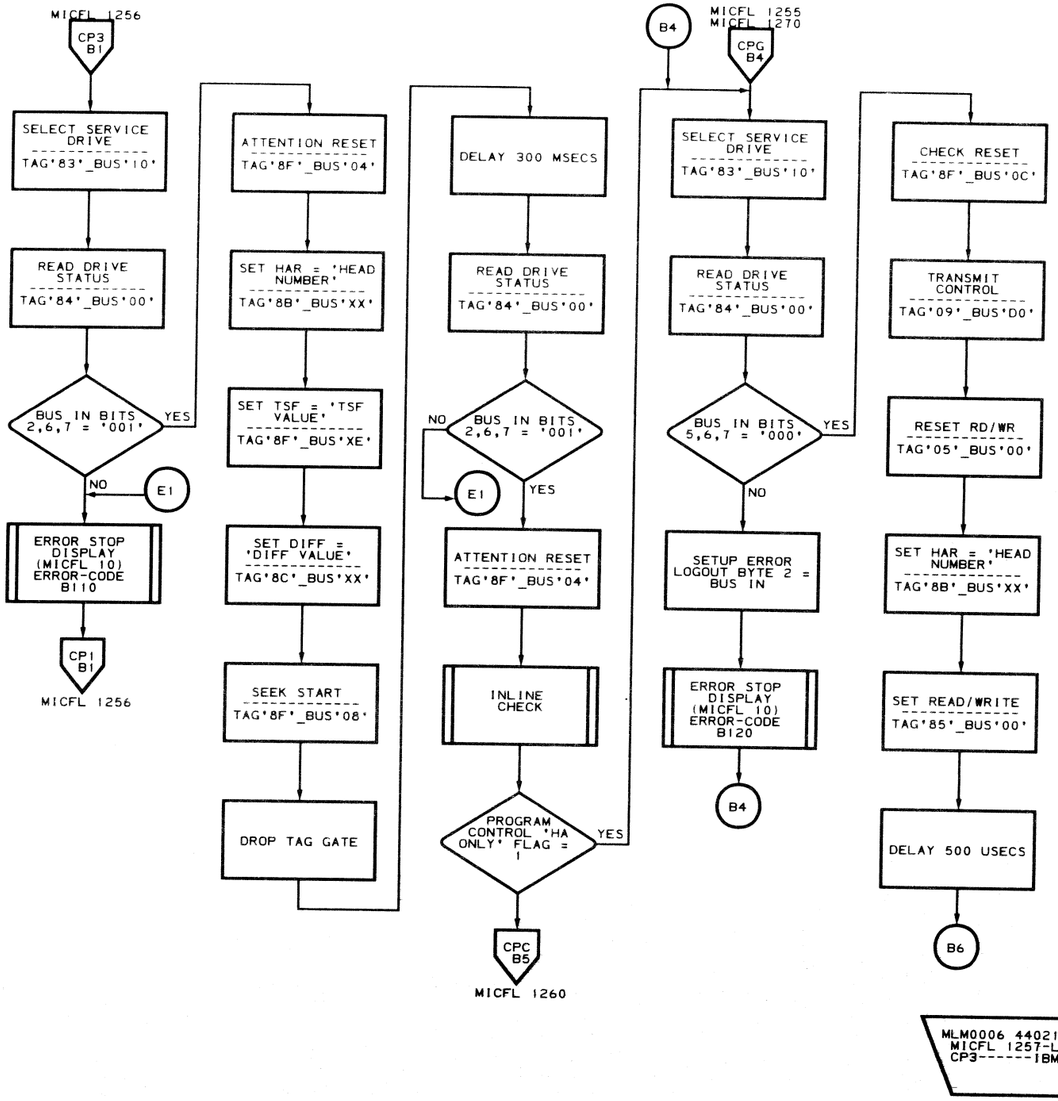
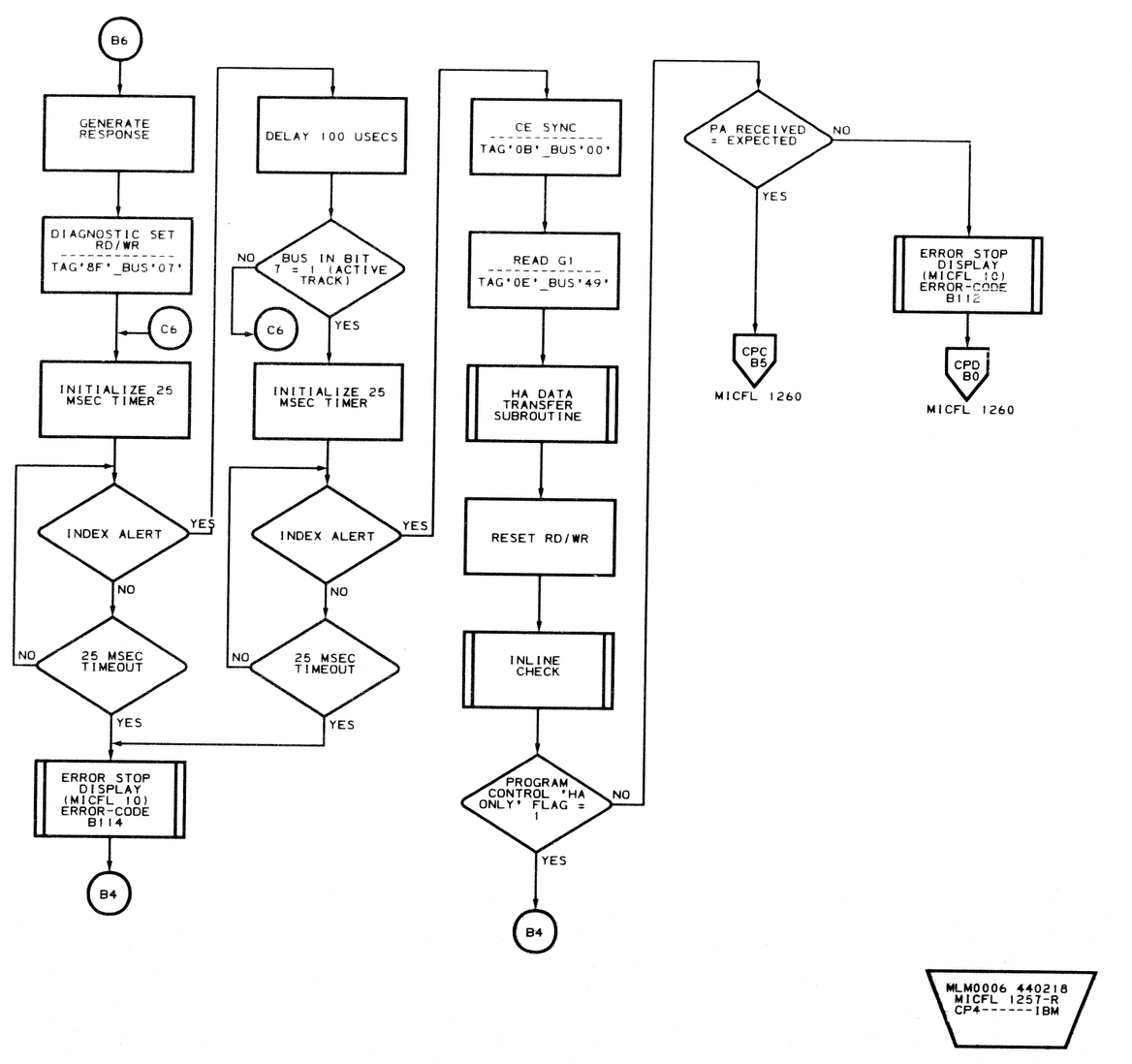
READ TEST (Routine B1)





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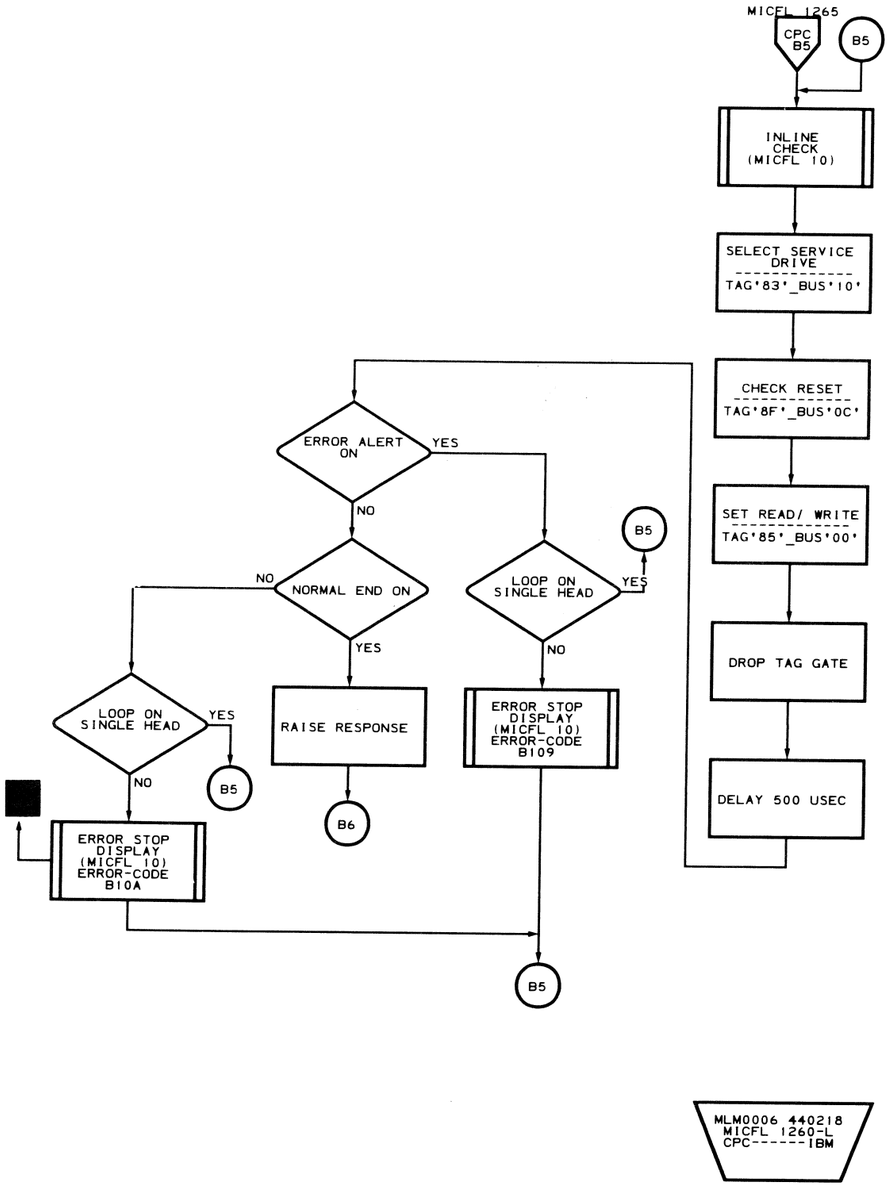

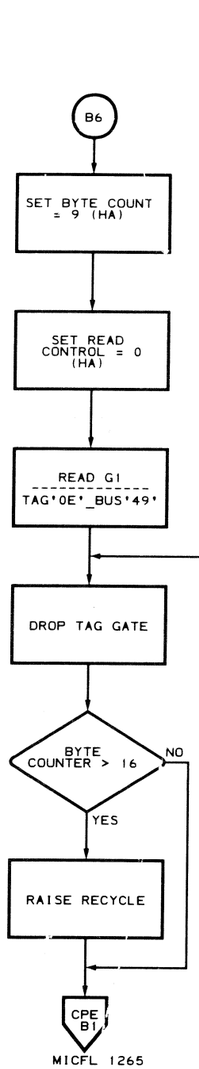

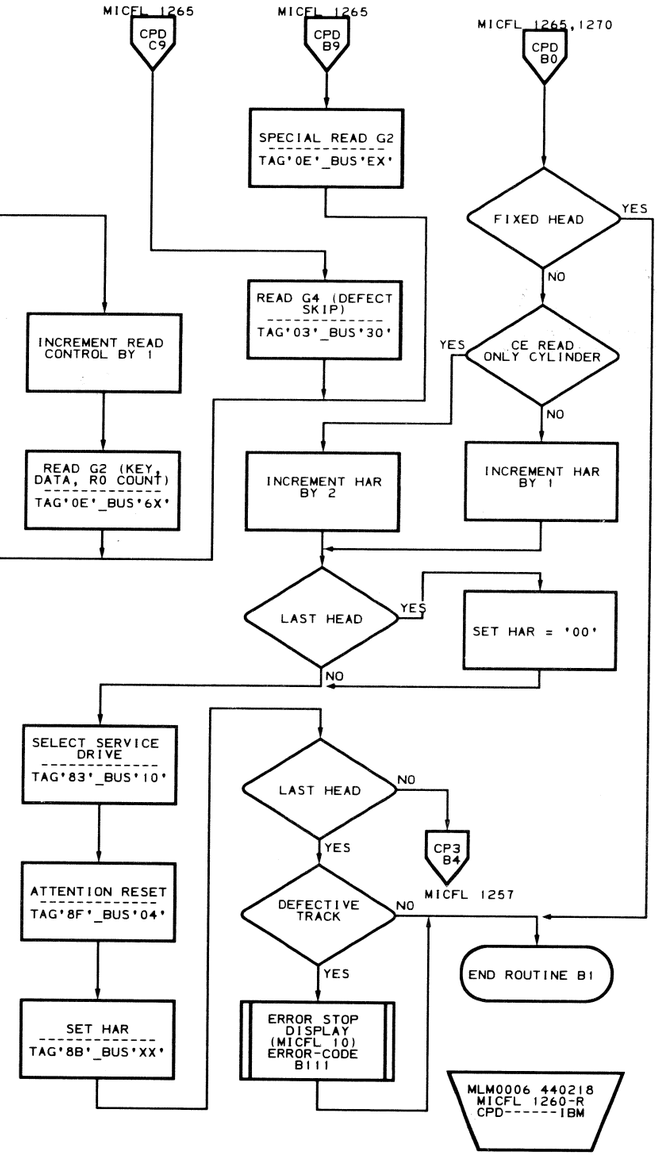

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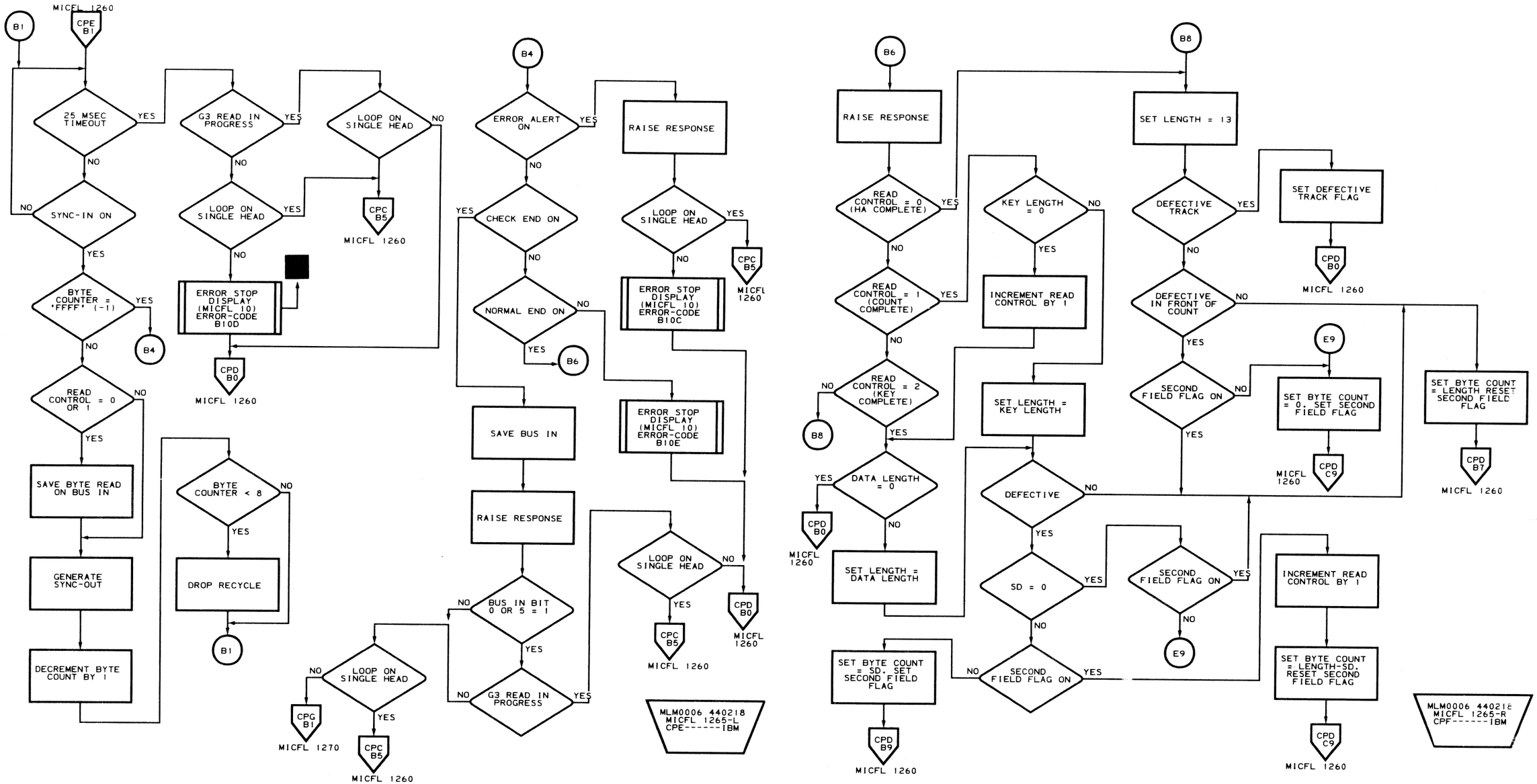
DATA TRANSFER AND ERROR ANALYSIS (Routine B1)



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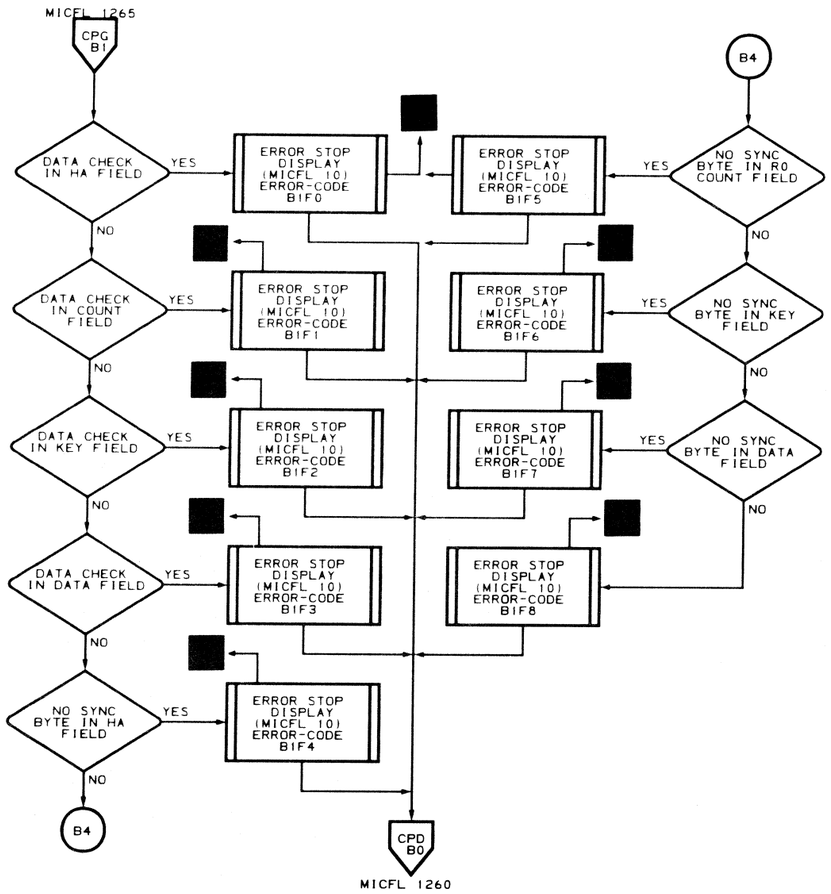

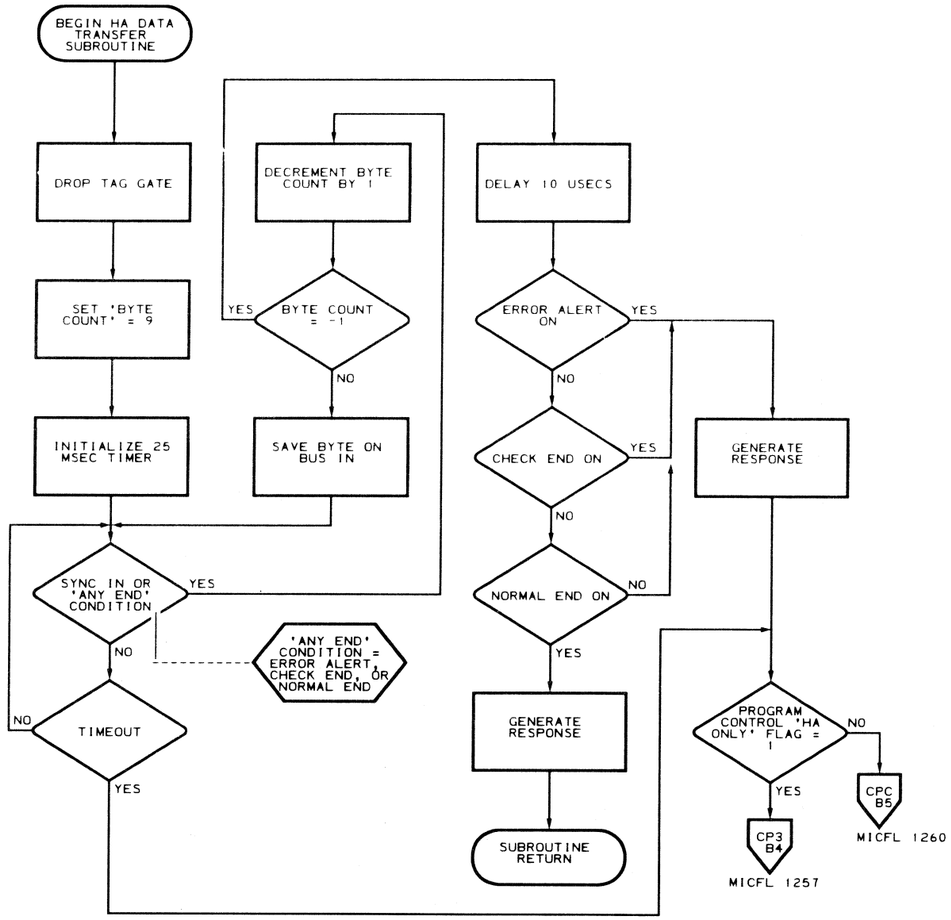

MLM0006 440218
MICFL 1270-L
CPG------IBM

MLM0006 440218
MICFL 1270-R
CPH------IBM

CG1260	2747128	440200	440202	440203	440218			
Seq. 2 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74			

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ROUTINE B2 — WRITE TEST

DESCRIPTION

Routine B2 writes a 256-byte field on the specified track or tracks of the CE cylinder.

In the normal (default) operation, Routine B2 writes R0 of 256 data bytes on each of the write test tracks of the CE cylinder (odd tracks of cylinder 349). The data pattern written is a 4-byte worst-case pattern of '7777FFAA'.

After each track is written, the data is read back. Read validity is determined by ECC checking.

Prior to writing the first R0, the routine reads the Home Address to verify proper access position.

Optional parameter entries may be used to select any single odd head for testing and/or to bypass the Read Back operation.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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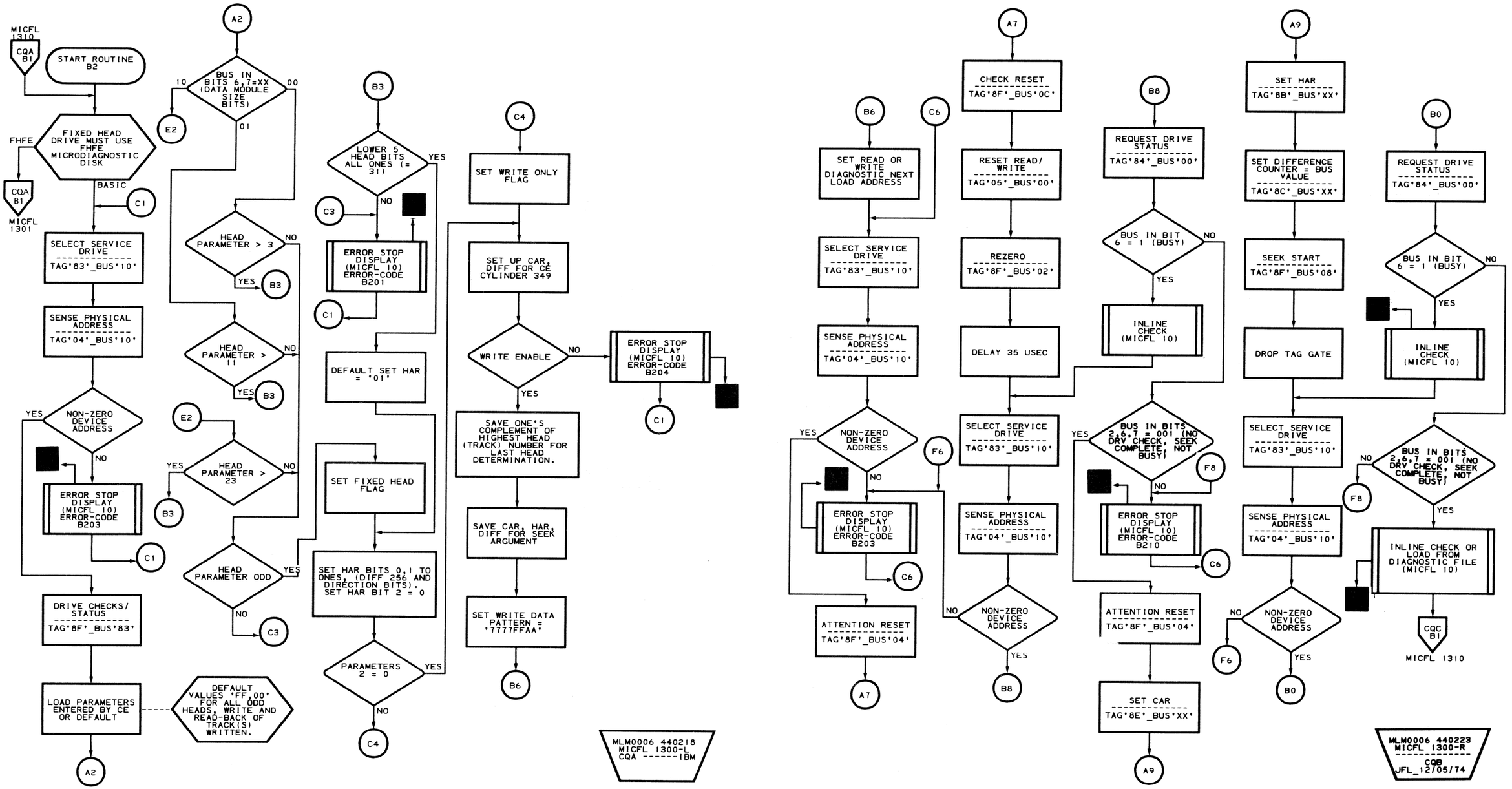
PARAMETER ANALYSIS (Routine B2)



CG1305	2747130
Seq.1 of 2	Part No.( )

440200	440202	440203	440214	440218	440219	440223
25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74	5 Aug 74	26 Sept 74	14 Mar 75

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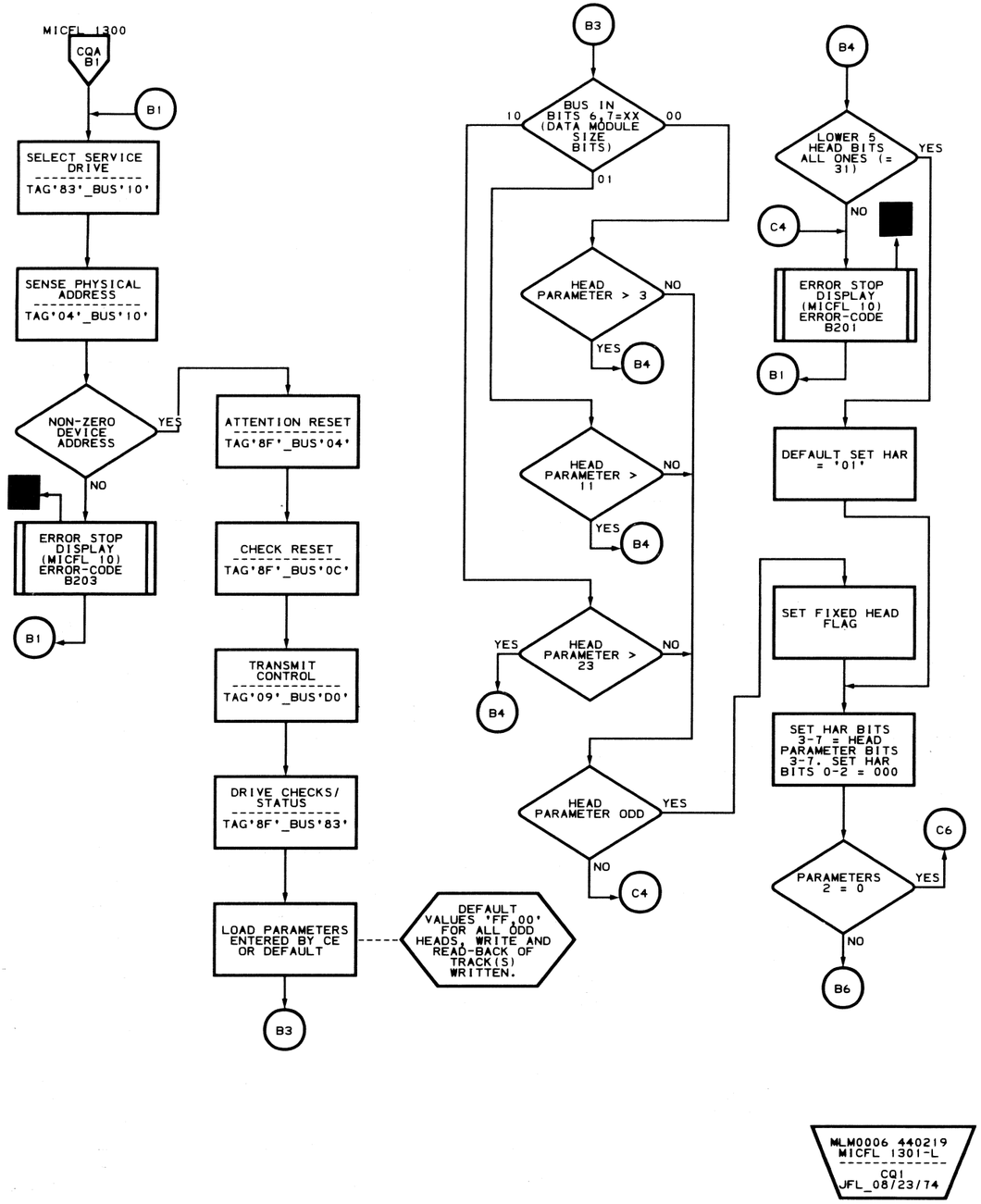
PARAMETER ANALYSIS (Routine B2)



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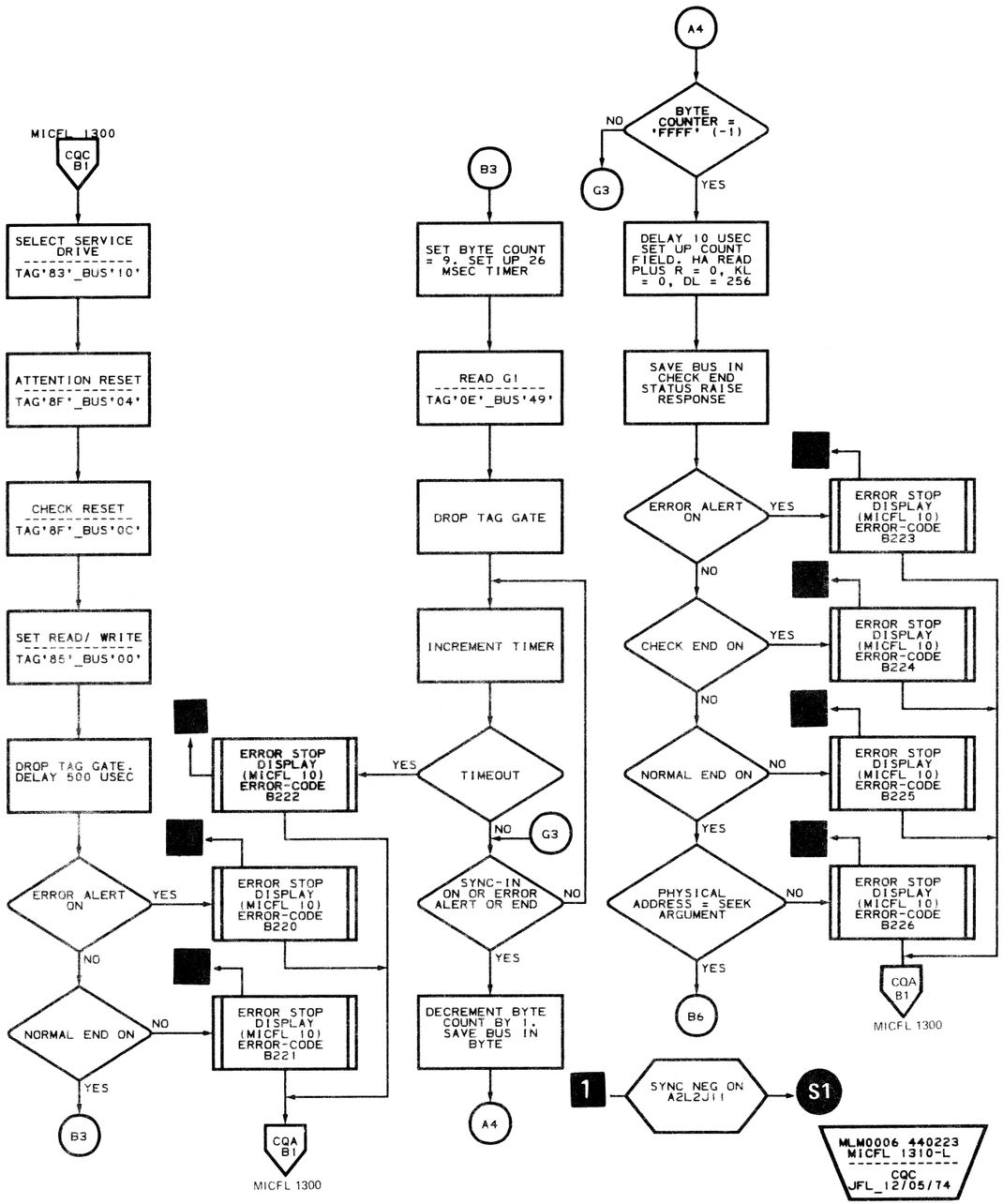
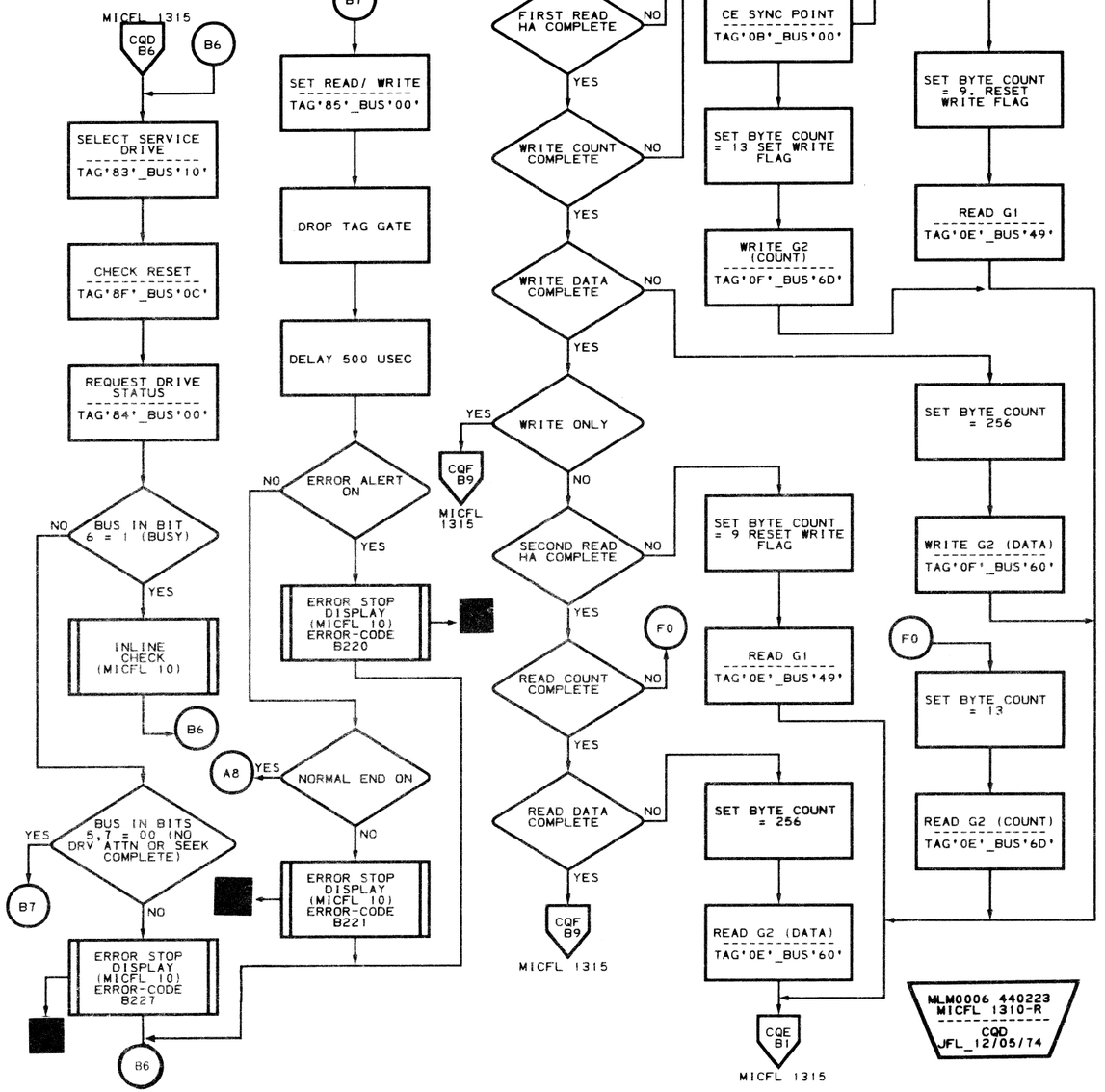
READ HA TO VERIFY PHYSICAL ADDRESS (Routine B2)





CG1307	2747906	440218	440223					
Seq. 1 of 1	Part No.( )	5 Aug 74	14 Mar 75					

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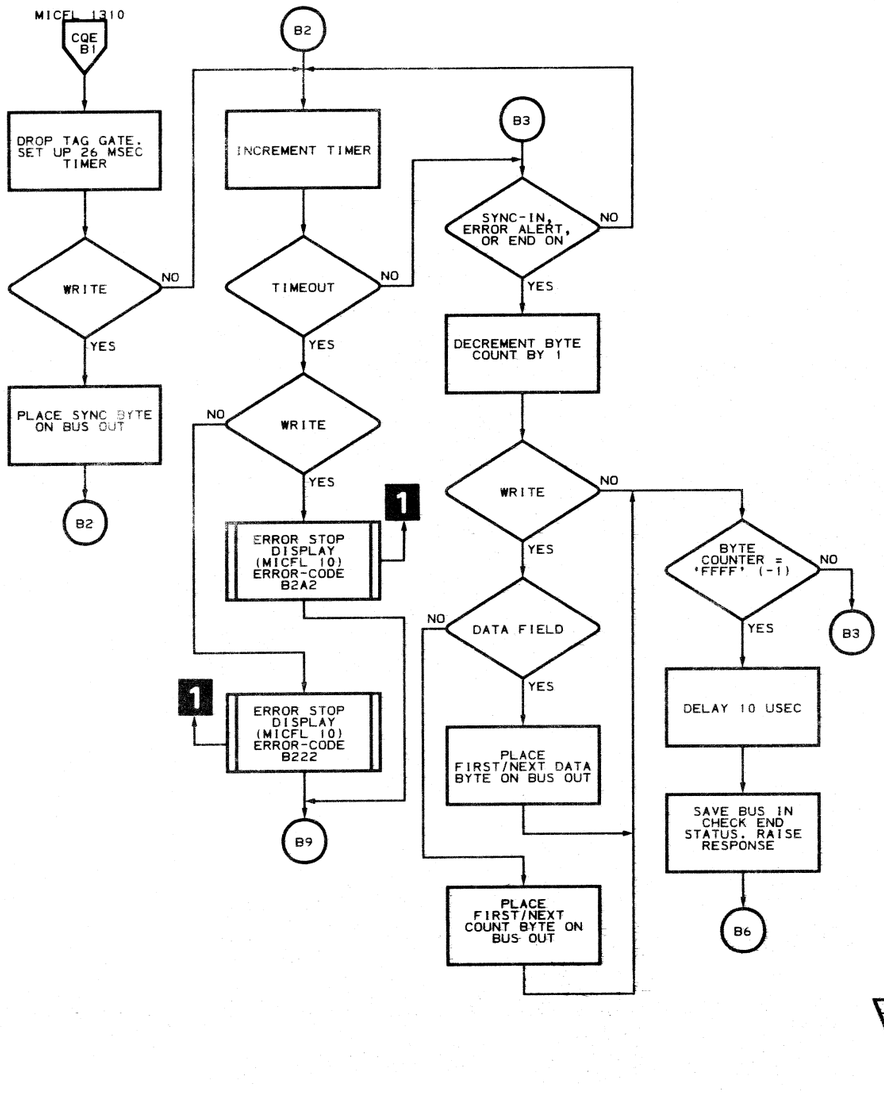
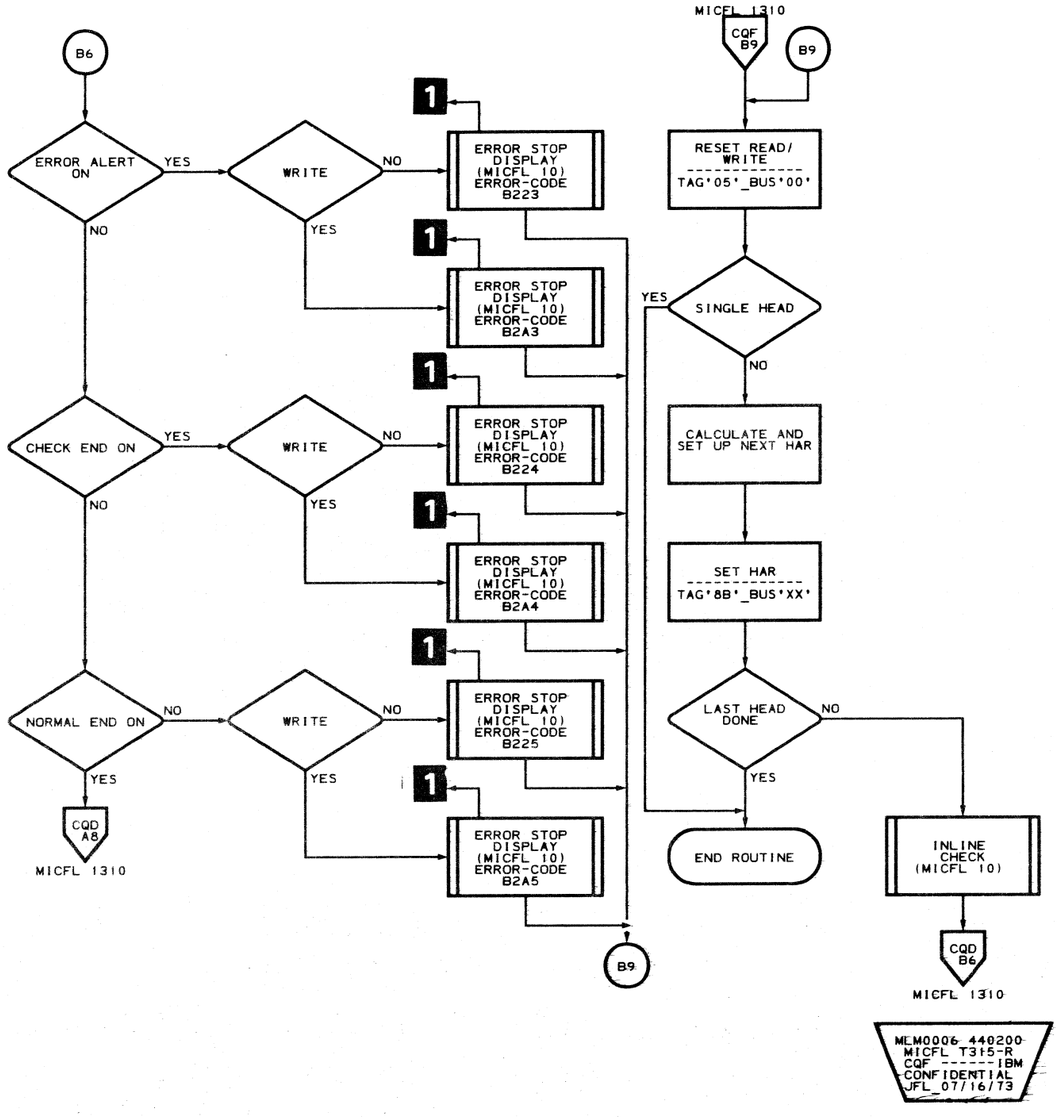
DATA TRANSFER/ERROR ANALYSIS, END OF TRACK (Routine B2)





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ROUTINE B3 – 3340 DEVICE STATUS DISPLAY PROGRAM

DESCRIPTION

The purpose of Routine B3 is to provide additional information regarding the status of a given drive. Its primary function is to supplement the information obtained from running a microdiagnostic that encounters an error. A symptom code and/or 15 bytes of status information are provided. The program is designed to run in two passes as follows:

Pass 1:

Pass 1 generates a symptom code from the failing state of the device or controller. It is important that the device be left in its failing state (no resets performed). The controller may be reset, as the Controller Interface Check byte and the Controller Check byte are stored by the diagnostic control monitor whenever a microdiagnostic detects an error. If pass 1 is unable to generate a symptom code, 'E1FF' is displayed.

Pass 2:

Pass 2 retrieves 12 bytes of information from the drive and 3 bytes of information from the controller. This is displayed in the Data Display lamps one byte at a time and provides the current state of a given drive and controller.

Note 1: Routine B3 does not issue any resets, and therefore can be reloaded and/or restarted as often as desired.

Note 2: If the routine is restarted after Pass 2, only Pass 2 is repeated. It is necessary to reload the routine in order to repeat Pass 1.

Note 3: Pass 2 information is displayed in the following order:

Byte	Meaning	Command Issued
1	Sense Physical Address (CE Drive Physical Address)	Tag '04' Bus '10'
2	Sense HAR	Tag '8F' Bus '05'
3	Sense Difference Counter	Tag '8F' Bus '09'
4	Request Drive Status	Tag '84' Bus '00'
5	Drive Checks/Status	Tag '8F' Bus '83'
6	Data Module Sequence Control	Tag '8F' Bus '43'
7	Load Switch Status	Tag '8F' Bus '23'
8	Read/Write Safety	Fetched from Monitor
9	Access Status	Tag '8F' Bus '13'
10	Controller Checks	Fetched from Monitor
11	Controller Interface Checks	Fetched from Monitor
12	Device Interface Checks	Tag '89' Bus '00'
13	Sense Target Register	Tag '8F' Bus '0D'
14	Cyl Address Register	Tag '8F' Bus '01'
15	Sense Status 0	Fetched from Monitor

Note 4: When the last byte (byte 15) has been displayed, the message displayed is 'CEB3'. CE (in the Control lamps) indicates the end of logout and B3 (in the Data Display lamps) indicates the Routine ID. This is standard message display for all logouts.

PREREQUISITES

Refer to the microdiagnostic reference chart on MICRO 36.

OPERATING PROCEDURE

Refer to detailed run instructions on MICRO 36.

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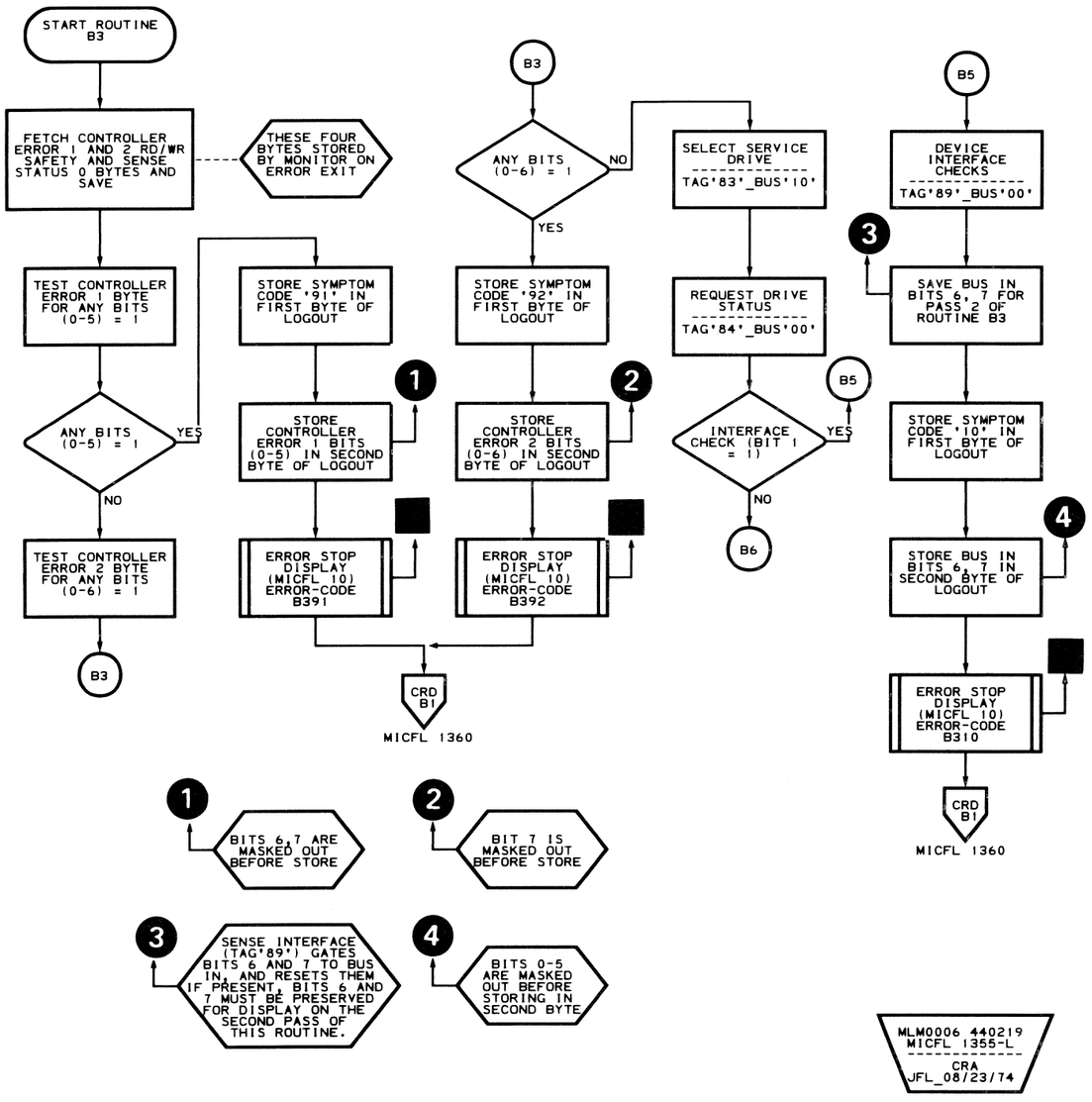
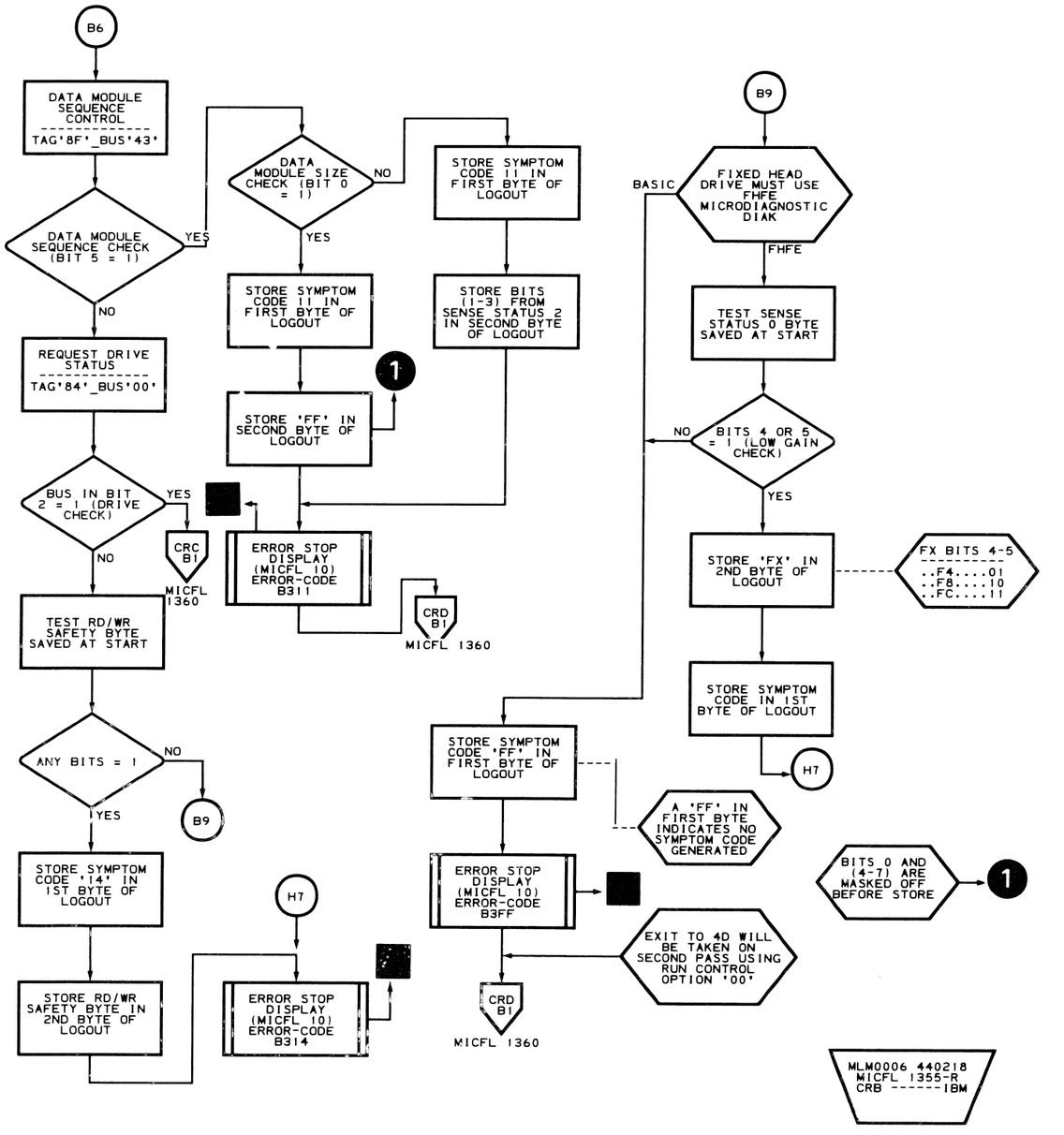
SYMPTOM CODE GENERATOR (Routine B3)





CG1355	2747132	440200	440202	440203	440218	440219	440223	
Seq. 1 of 2	Part No.( )	25 Jun 73	7 Sept 73	2 Nov 73	5 Aug 74	26 Sept 74	14 Mar 75	

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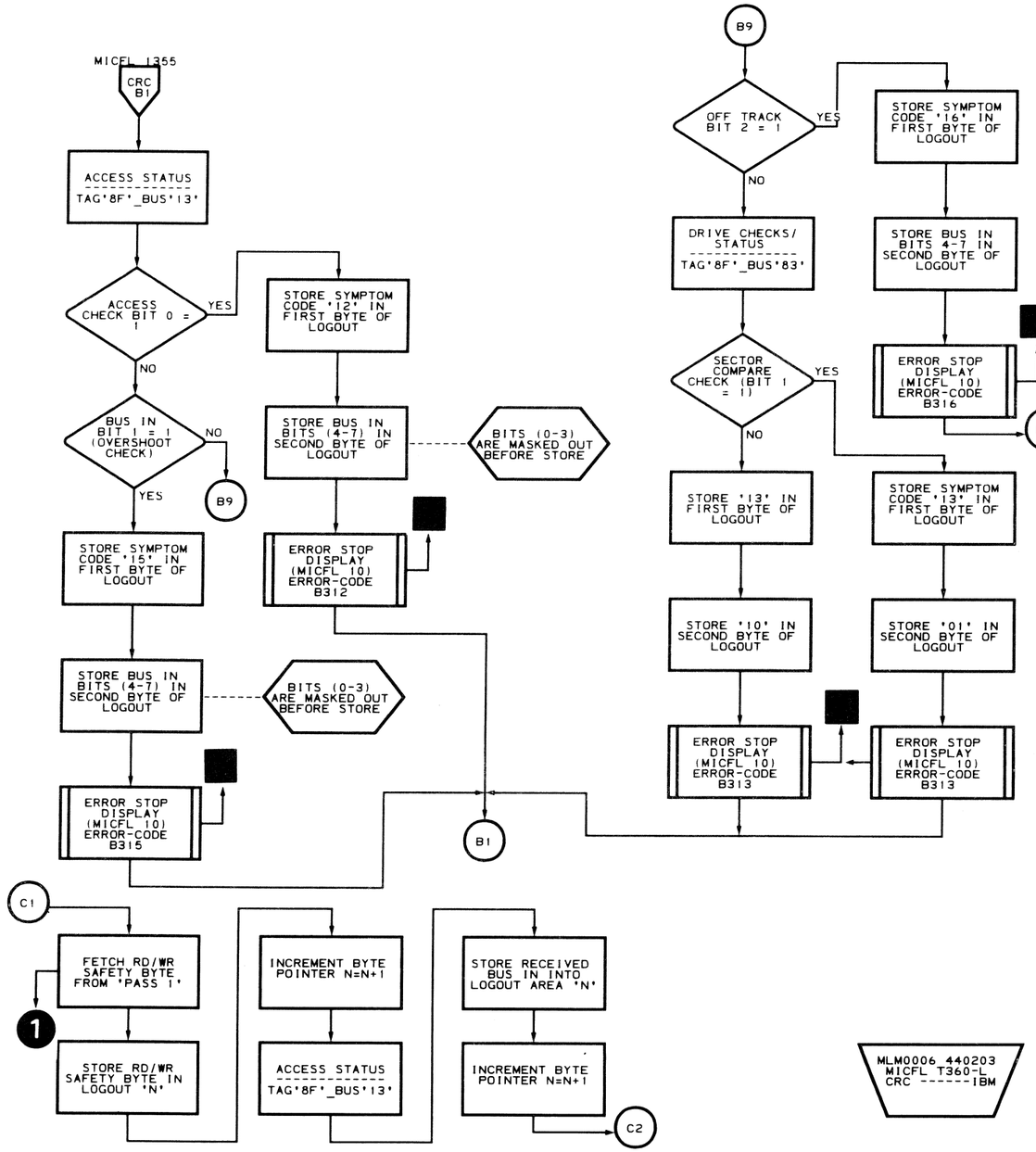
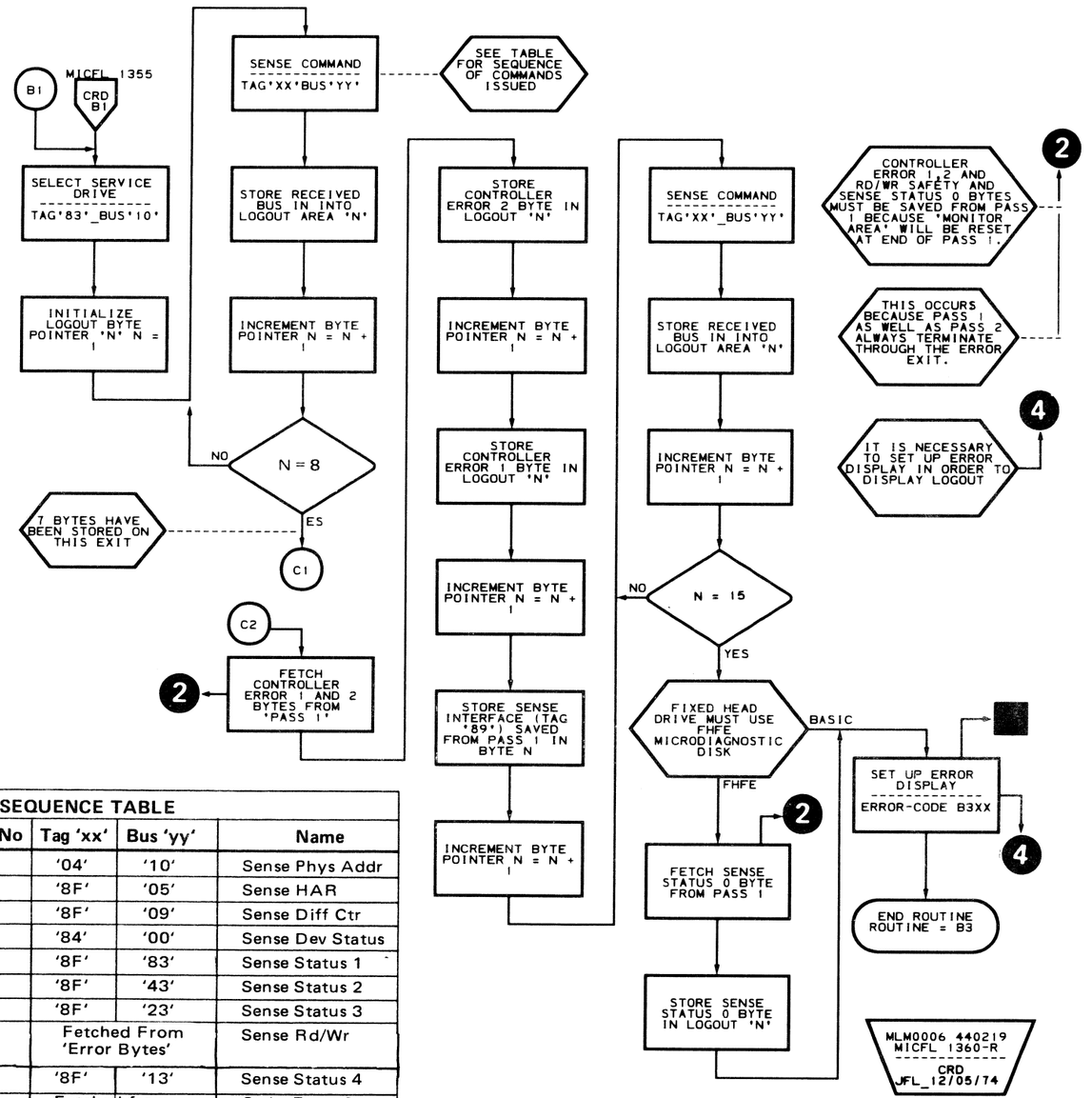
SYMPTOM CODE GENERATOR (Routine B3)





TAG SEQUENCE TABLE			
Byte No	**Tag 'xx'**	**Bus 'yy'**	**Name**
1	'04'	'10'	Sense Phys Addr
2	'8F'	'05'	Sense HAR
3	'8F'	'09'	Sense Diff Ctr
4	'84'	'00'	Sense Dev Status
5	'8F'	'83'	Sense Status 1
6	'8F'	'43'	Sense Status 2
7	'8F'	'23'	Sense Status 3
8	Fetched From 'Error Bytes'		Sense Rd/Wr
9	'8F'	'13'	Sense Status 4
10	Fetched from		Ctrlr, Error 2
11	'Error Bytes'		Ctrlr, Error 1
* 12	'89'	'00'	Sense Interface
13	'8F'	'0D'	Sense Target
14	'8F'	'01'	Sense CAR
** 15	'8F'	'03'	Sense Status 0

* Sense Interface Bus-In saved from Pass 1
** FHFE only

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ROUTINE B4 – TAG CYCLE UTILITY PROGRAM

DESCRIPTION

Routine B4 executes any valid tag bus or delay commands that the CE selects with parameter entry, with the exception of Rezero (Tag '8F' Bus '02') and Seek Start (Tag '8F' Bus '08').

Each delay or tag command consists of two bytes of entry and up to seven commands at one time. These entries are known as the command string. Following the last command, zeros must be entered to complete the parameter field.

Once the desired commands have been entered, execution can be started by the Start/Stop run control option. (Refer to MICRO 10 and 11.)

When the routine begins, the commands are executed in a sequential manner. When '00' appears in the control byte, execution halts and an inline check is performed. After the diagnostic control monitor has returned control, the routine begins command execution with the first command. This procedure provides a continuous loop.

If the command string requires modification after execution has started, the routine must be reloaded. The routine may be halted and restarted at any time by using run control option 00. (Refer to MICRO 10 and 11.)

The following describes the format of command bytes. The first byte is called the control byte. This byte is used to: (1) signal the end of the command string. (2) describe the tag or delay being issued, and (3) control the data to and from the CE panel. The second byte of the command is used for Bus Out or a base delay value depending on the command in the control byte.

Since the tag only uses 5 bits of the first byte (0, 4, 5, 6, and 7), the remaining bits (1, 2, and 3) are used for special control options. The ORing of these two fields forms the control byte.

The tags for the 3340 Drive are described on OPER 100 and 101.

CAUTION
Do not use Seek Start (Tag '8F' Bus '08') or Rezero (Tag '8F' Bus '02'). Data module damage may result and a B413 error stop occurs.

SPECIAL CONTROL OPTIONS

000 Forms a control byte of '0000 0000', which is used for End of String indicator.

001 The routine executes a Tag '0A' Bus '40' (Read Data Entry switches) prior to execution of the tag in bits 0, 4, 5, 6, and 7. The value read from the Data Entry switches is used as a Bus Out value during the execution of the coded tag.

Note: Tag '0A' Bus '40' (Read Data Entry switches) also resets the CE Alert Line that is activated by the Execute switch. If this command is used, the program may require repeated operation of the Execute switch in order to stop execution.

Example: To transmit a Set Head Address Register Tag (1000 1011) with the ability to vary the value, use option code 001. The ORing of Tag '1000 1011' and control 001 forms a control byte of '1001 1011'. Refer to sample command string on this page.

When this control byte is encountered by the program, it splits off and does two tags:
1. Tag '0A' Bus '40' Read Data Entry switches
2. Tag '8B' Bus 'xx' Set Head Address Register
   where xx = Data Entry switches

010 This control option is used in the same manner as option 001 except that the Bus In received from the coded tag is transmitted to the Data Display lamps.

Example: '1010 1111' control option byte (Tag '8F' and control option 010) coded with a Bus Out of '05' creates a Sense Head Address Register Tag. When this control byte is encountered by the program, the control byte issues a Data Display Tag after the coded tag was issued. (Refer to sample command string on this page.)

Tag '8F' Bus '05' Sense Head Address Register
Tag '0D' Bus 'xx' Data Display
where xx = Bus In value from the Sense Head Address Register Tag

011 This option code is used to insert *microsecond* delays in the command string. When this code is used, bits 4, 5, 6, and 7 become the delay multiplier. The base delay value is contained in the second byte of the command. See example for different values of delays. Tag Gate is dropped at beginning of any delay.

100 This option code is used to insert *millisecond* delays in the command string. When this code is used, bits 4, 5, 6, and 7 become the delay multiplier. The base delay value is contained in the second byte of the command. Tag Gate is dropped at beginning of any delay.

101 thru 111 Not used.

Example of Different Delays

	Command Entry Byte 1	Byte 2	Delay Value
a.	30	C8	200 microseconds
b.	32	C8	400 microseconds
c.	40	C8	200 milliseconds
d.	41	C8	200 milliseconds
e.	43	64	300 milliseconds

Example b:

C8 (hex)	=	200 (decimal)
multiplier	=	2
Total	=	400
3 in byte 1	=	microsecond
Therefore, total delay	=	400 microseconds

Example e:

64 (hex)	=	100 (decimal)
multiplier	=	3
Total	=	300
4 in byte 1	=	millisecond
Therefore, total delay	=	300 milliseconds

Note: 0 multiplier is defaulted to 1.

Sample Command String

Parameter Byte	Hex Value	
1	83	Tag to Select Drive
2	00	Bus Out *Note: Bus Out in the case of A select tag is supplied by the program. (Service Drive only)*
3	9B	Tag to set Head Address Register. Option Code 1001 is used so Bus Out is supplied from the Data Entry switches.
4	00	Must be 00 with Option Code 1001.
5	AF	Tag to Sense Head Address Register (HAR). Option Code 1010 is used so received Bus In is transmitted to the Data Display lamps.
6	05	Bus Out for Sense HAR Tag
7	8C	Tag to set Difference Counter
8	FF	Bus Out value
9	8F	Tag to Sense Difference Counter
A	09	Bus Out for Sense Difference Counter
B	42	200 millisecond delay
C	64	
D	00	
E	00	Filler for remaining parameter
F	00	

Note: The run control option '00' must be entered to begin program execution. The desired HAR value must be set in the Data Entry switches as soon as the '8C' message is displayed in the control lamps.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiaognostic reference charts starting on MICRO 20 for parameter entry.

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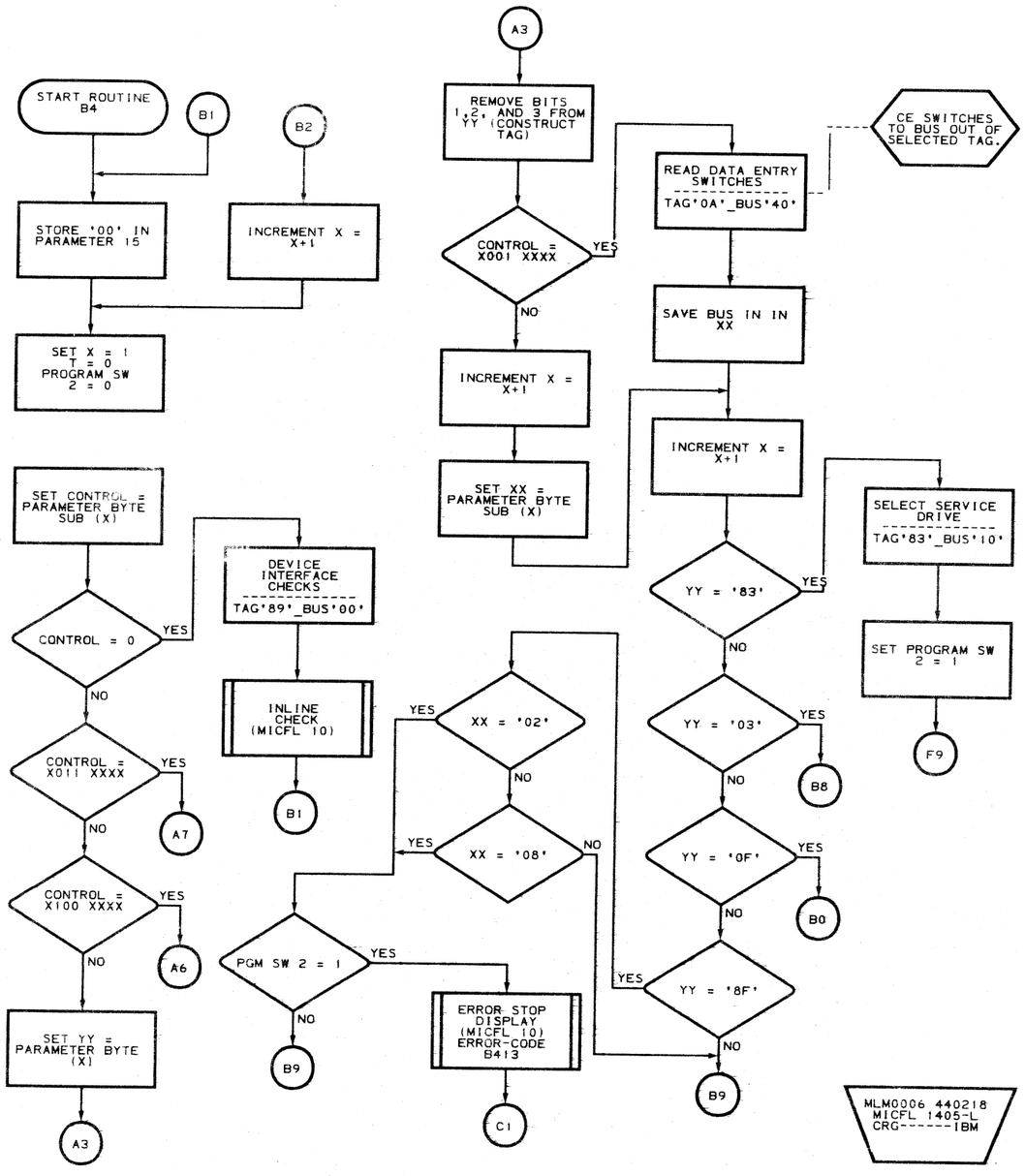
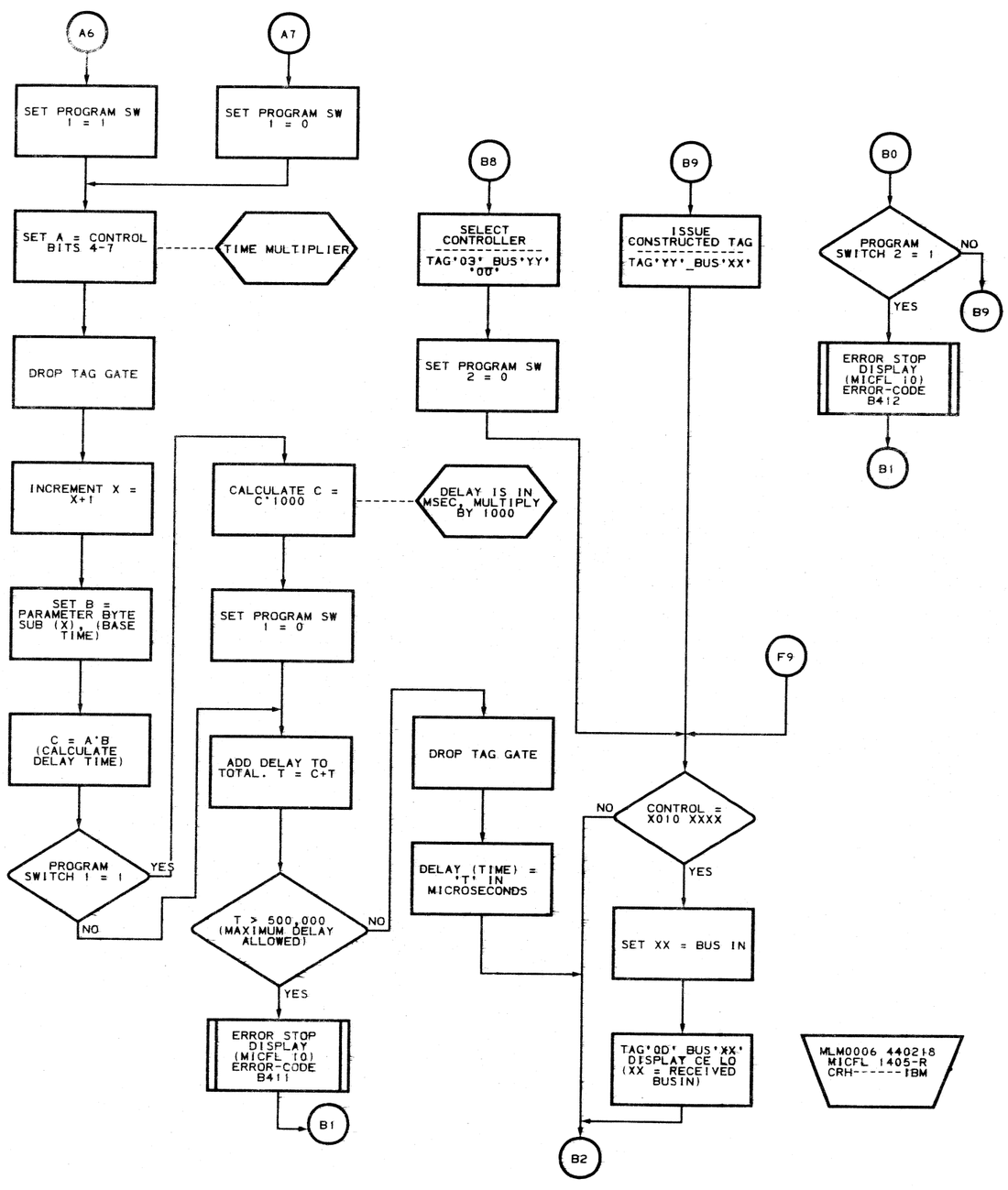
TAG CYCLE UTILITY (Routine B4)





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ROUTINE B7 – 3340 CARRIAGE GO HOME UTILITY PROGRAM

DESCRIPTION

Routine B7 provides a scope loop to aid in the diagnosis of carriage latching problems. There are no error stops other than those tested in the required initial conditions such as CE service drive selected. Refer to MICRO 85 for common error stops.

Note 1: Routine B7 loops indefinitely or until stopped by the '00' run control option.

Note 2: Routine B7 runs with or without a data module present.

PREREQUISITES

Refer to microdiagnostic reference charts starting on MICRO 20.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

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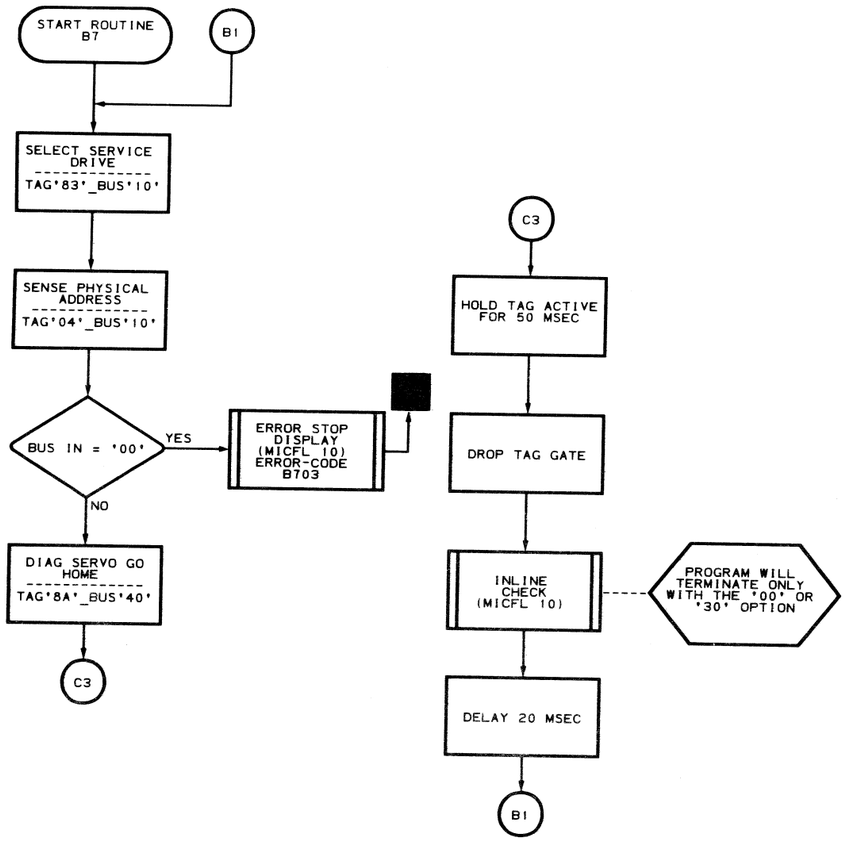
ROUTINE B7



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CG1480	2747135	440200	440202	440203				
Seq. 1 of 1	Part No.( )	25 June 73	7 Sept 73	2 Nov 73				

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3340 – CTL INTERFACE BRINGUP PROGRAM

DESCRIPTION

Prerequisites

- The "CTL Interface Bringup Program" must be run from the storage control. For S/370 Model 135 run instructions, refer to 370/135 Failure Analysis manual page IFA-312. For S/370 Models 115 and 125, refer to System CTM (Central Test Manual) Section 17. For System/7, refer to the 5998 CTM, MAP 1302.
- Storage control must be operational.
- The controller must be capable of a Power-On Reset. (One indicator of a successful Power-On Reset = Parity Check lights on CE Panel are off.)

Purpose of the Tests

Test 1A – Hot Bus In/Control lines test.
Tests for active bits on Bus In and active interface lines.

Test 1B – Missing Bus In test.

Test 2 – Tag Bus/Bus Out test.
Cycles patterns on Bus Out or Tag Bus to find open or faulted lines.

Test 3 – Control lines test.
Tests three basic control lines for operational status:
Select Hold
Tag Gate
Recycle

Test 1A – Bus In/Control Lines Test

This test cycles continually until stopped by manual intervention. The test samples Control Interface Bus In and up to six control lines on the control interface. If any lines are found to be active while the controller is in a reset state, an error occurs and the active lines are displayed. Testing can be accomplished with the controller selected, or not selected, as determined by parameter entry (see the Parameter Table on MICFL 1501). It is recommended that the test first be run without selecting a controller. Under this condition, the unselected bits on Bus In are sampled as well as the following control lines:

Selected Alert 1
Select Active
Sync In
Normal End
Check End
Tag Valid

If the select controller option is chosen, Bus In is sampled while selected and all of the above control lines are tested with the exception of Select Active.

OPERATION:

Perform the General Operating Procedures on MICFL 1501 and return here.

ERROR CODES

Errors are indicated in the 3830-2/ISC Address/Check/Program Display lamps. Ignore the Register/Storage Display lamps.

F1XX = Control line active lamps 8–15 identify the active control line.
Resolve these errors before continuing with test 1B. Note which line is active and take action on CTL-I 101.

Lamp No.	Control Line
8	Selected Alert 1
9	Select Active
10	Sync In
11	Not used
12	Normal End
13	Check End
14	Tag Valid
15	Not used

F2XX = Bus In active lamps 8–15 identify the active bit(s).
Resolve these errors before continuing with test 1B. Note which bit is active and take action on CTL-I 102.

Lamp No.	Bus In Bit
8	0
9	1
10	2
11	3
12	4
13	5
14	6
15	7

To clear error indications, to stop the test, or to change parameters, operate the 3830-2/ISC Execute switch.

Test 1B – Bus In Test

This test provides a procedure to test for missing bits on Bus In. The data register which is nominally reset to all bits on (FF) is forced onto Bus In. Correct operation will cause a display of F2FF where FF is the Bus In value. Any other value would indicate a missing bit(s). For example, a display of F2F7 would mean a missing bit 4.

OPERATION:

Perform the General Operating Procedures on MICFL 1501 and return here.

With the test running:

1. Momentarily ground +Not Index Data Good A2Q2D10 (BH160) to force -Read Mode Ctl Latch on.
2. Jumper one of the following pins to ground (D08) depending on the machine.
   A. Basic Machine
   +Contrlr Poll Op 02 A2G2J12 (BH 110)to force -BI Gated.
   B. String switch (Interface A)
   +CE Connect A A2D2S08 (BM170).
   Note: Disable Interface B (PANEL 10).
   C. String switch (Interface B)
   +CE Connect B A2E2S08 (BN170).
   Note: Disable Interface A (PANEL 10).
3. Observe that the 3830-2/ISC display should equal 'F2FF'.
4. If display does not equal 'F2FF', verify -Read Mode Ctl. Scope A2P2S04 (BG150) for a minus MST level. If not minus, replace A2P2.
5. If 'F2XX' is not displayed, verify setup (Steps 1 and 2).
6. If 'F2XX' where XX ≠ FF insure that cards, flat cables and interface cables are properly seated. The display will continuously indicate the state of Bus In so that it can be determined if a fix is effected (Display = 'F2FF'). If this action is not successful, scope the NPL Bus In lines per CTL-I 105 (CTL-I 115 for SWFE) for a static plus NPL level.
7. Remove the jumper installed in Step 2 above.
8. Reset the Read Mode Ctl latch by either of the following:
   A. Ground to D08 -Read Mode Ctl A2P2S04 (BG150) or
   B. Power off then power on the controller
9. To stop the test, or to change parameters, operate the 3830-2/ISC Execute switch.

Test 2 – Tag Bus/Bus Out Test

This test is designed to cycle any two patterns on Tag Bus or Bus Out. The parameters entered determine whether Tag Bus or Bus Out is to be tested and the pattern to be used (see the Parameter Table on MICFL 1501). The test cycles in the following manner:

- Pattern 1 is placed on either Tag Bus or Bus Out.
- Tag Gate is raised and held active for 6.4 microseconds.
- Tag Gate is dropped and held down for 2 microseconds.
- Pattern 2 is placed on either Tag Bus or Bus Out.
- Tag Gate is again raised and held active for 6.4 microseconds.
- Tag Gate is dropped and held down for 2.6 microseconds before pattern 1 is recycled.

The test cycles indefinitely until stopped by operating the 3830-2/ISC Execute switch once, or Stop, Reset and Start.

Test 2 does not produce any error indications, as it is intended for scoping purposes only.

Perform the General Operating Procedures on MICFL 1501 and return here.

To stop the test, or to change parameters, operate the 3830-2/ISC Execute switch.

Test 3 – Control Lines Test

This test allows the following control lines to cycle for scoping purposes:

Select Hold
Tag GAte
Recycle

This test loops continually until stopped by manual intervention. No errors are displayed. Control line selection is by parameter entry (see the Parameter Table on MICFL 1501).

Perform the General Operating Procedures on MICFL 1501 and return here.

To stop the test, or to change parameters, operate the 3830-2/ISC Execute switch.

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3340 – CTL INTERFACE BRINGUP PROGRAM

GENERAL OPERATING PROCEDURE

Prerequisites

- Vary the 3340 file sybsystem (including the 3830-2/ISC) offline.
- Perform a Power-On Reset to the controller to be tested.

CAUTION
Do not use the Execute switch on the controller. This routine must be executed from the 3830-2/ISC CE Panel only.

Run Procedure

The following steps are performed from the 3830-2/ISC CE Panel:

1. Set Operation Mode switch to CE Normal position.
2. Operate Stop/SI switch once.

CAUTION
Before stopping the 3830-2/ISC, insure that the customer has terminated his operations on the subsystem and that it is varied offline.

3. Operate Reset switch.
4. Insert the 3340 microdiagnostic disk in the 23FD MPL file.
5. Operate the IMPL switch and check that the MPL Power-on light turns on.
6. When the MPL Power-on light goes off, turn the Enter/Display switch to IAR position.

   The Address/Check Program display lamps should indicate '0048' when the Clock Stopped lamp is off. If the 3830-2/ISC is stopped with the Stop/SI switch, the program loops between addresses '0008' and '0040'. This can be verified by repeated operation of the Stop/SI switch. If the display lamps agree with the above values, go to step 7.

   If the display lamps fail to give the above indications, one of the following errors probably occurred:

   a. Wrong disk was inserted in the 23FD MPL file.
   b. There was an IMPL error. Check the Clock Stopped and Check 1 lamps.
   c. There was an active CE Alert line from the 3340 controller. Verify that the Execute Request lamp is off on the 3340 controller CE Panel. If it is on, power-off and then power-on the 3340 controller and return to step 5.

7. If the Clock Stopped lamp is on, operate the 3830-2/ISC CE Panel Start switch.
8. Set the Enter/Display switch to the Program Data Entry/Display position.
9. Enter four parameters by placing each parameter in the Data Entry switches, then operating the Execute switch.

   a. For Test 1A:

   Parameter 1 = 01 Test 1
   2 = 00 Nonselect or
   01 Select
   3 = 00 Nonselect or to select →

Ctlr Addr	Enter
0	00
1	20
2	40
3	60

   4 = 00

   b. For Test 1B:

   Parameter 1 = 01 Test 1
   2 = 00 Nonselect
   3 = 00
   4 = 00

   c. For Test 2:

   Parameter 1 = 02 Test 2
   2 = 00 Tag Bus or
   = 01 Bus Out
   3 = 00-FF Pattern No. 1 to be placed on Tag Bus or Bus Out
   4 = 00-FF Pattern No. 2 to be placed on Tag Bus or Bus Out

   d. For Test 3:

   Parameter 1 = 03 Test 3
   2 = 40 Tag Gate
   = 80 Select Hold
   = C0 Tag Gate and Select Hold
   = F0 Recycle
   3 = XX Enter any number
   4 = XX Enter any number

   Note: If incorrect parameters are entered or control is lost, the program can be reinitialized by operating the Stop/SI, the Reset, and Start switches. This returns the test to the 2-word loop described in step 6.

10. To verify that the test is running correctly:
    a. Turn the Enter/Display switch to IAR.
    b. The Address/Check/Program display should contain '00FC' (program running).
11. Return to the specific test operation on MICFL 1500.

PARAMETER TABLE

Parameter	Test	Parameter Description	Value	Comments
1		Test number used to select Test 1, 2, or 3.	01 = Test 1 02 = Test 2 03 = Test 3	All other values cause unpredictable results.
2	1	Select/not select controller.	00 = Not select 01-FF = Select	Run Test 1 not selected to test for active Select Active line.
	2	Set Tag Bus or Bus Out.	00 = Tag Bus 01 = Bus Out	All other values cause unpredictable results.
	3	Select control line.	40 = Tag Gate 80 = Select Hold C0 = Tag Gate and Select Hold F0 = Recycle	All other values cause unpredictable results.
3	1	Controller address (if parameter 2 is nonzero).	Ctlr Addr 00 = 0 20 = 1 40 = 2 60 = 3	Controller address must be known and proper address entered in order to select.
	2	Pattern No. 1 to be placed on Bus Out or Tag Bus.	00-FF	Any pattern can be cycled on Bus Out. Bits 1, 2, and 3 not used on Tag Bus.
	3	Not used in this test, but must be entered.	00-FF	Enter any number in Test 3.
4	1	Not used in this test, but must be entered.	00-FF	Enter any number in Test 1.
	2	Pattern No. 2 to be placed on Bus Out or Tag Bus.	00-FF	Any pattern can be cycled on Bus Out. This can be the same or different from Pattern 1. Bits 1, 2, and 3 not used on Tag Bus.
	3	Not used in this test, but must be entered.	01-FF	Enter any number in Test 3.

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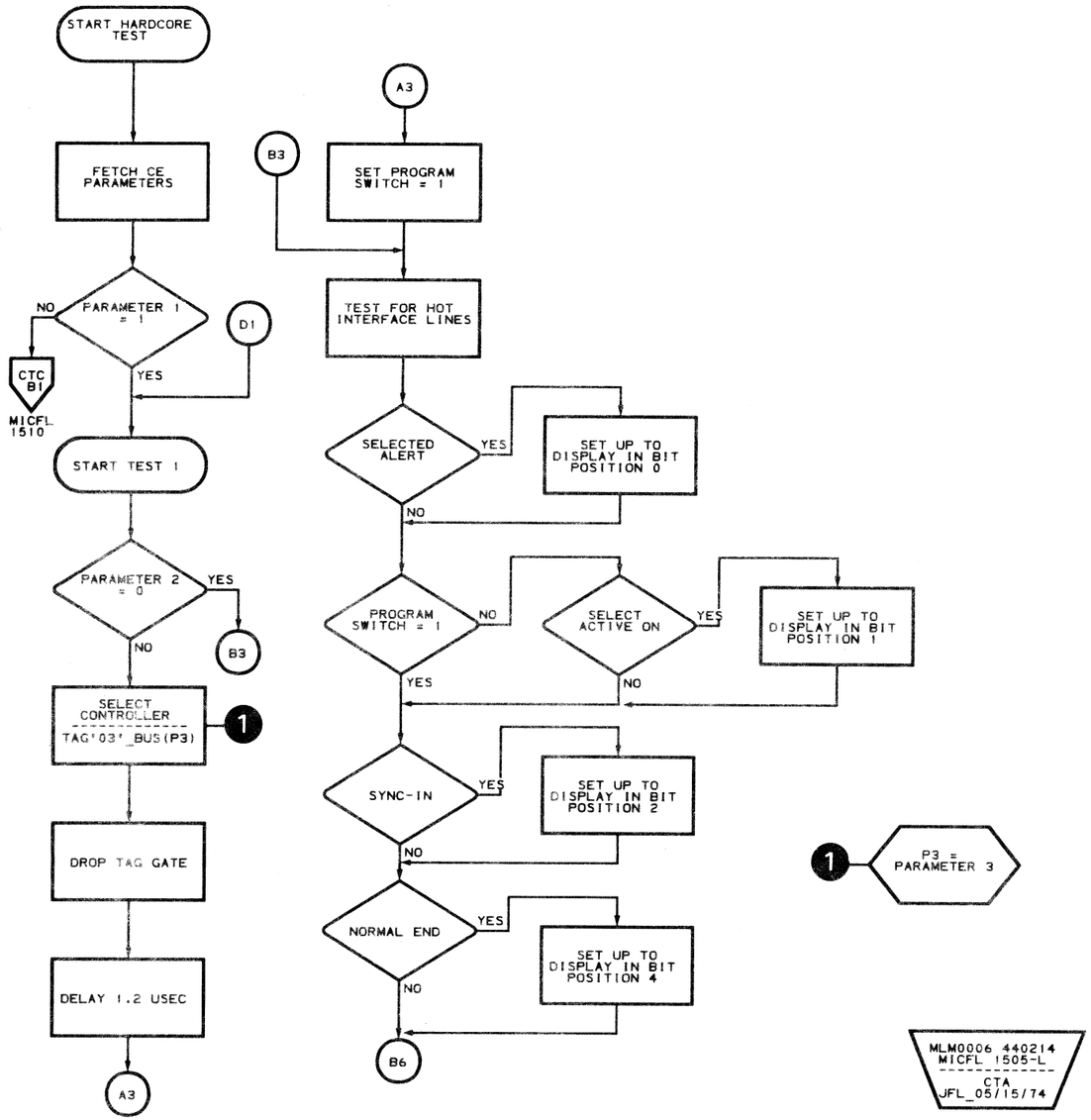

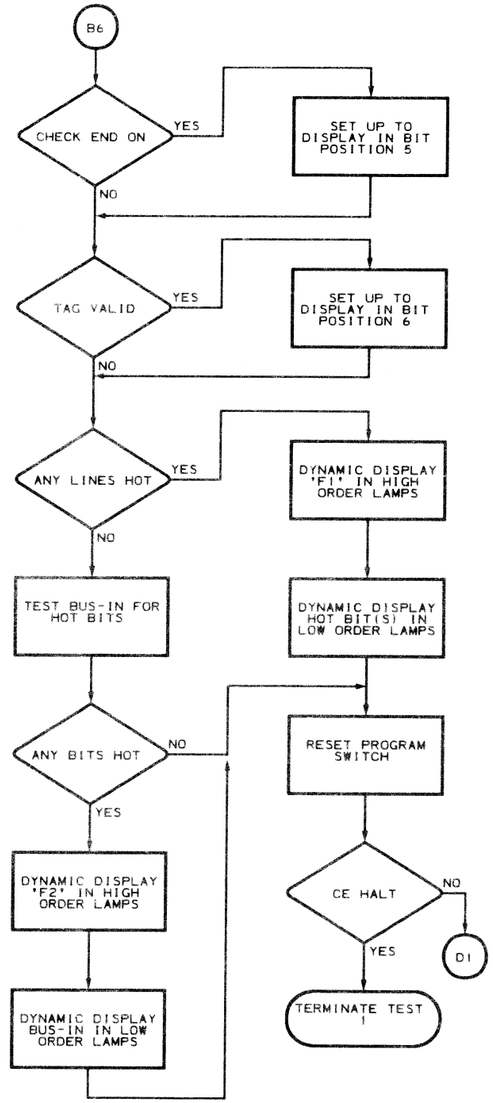

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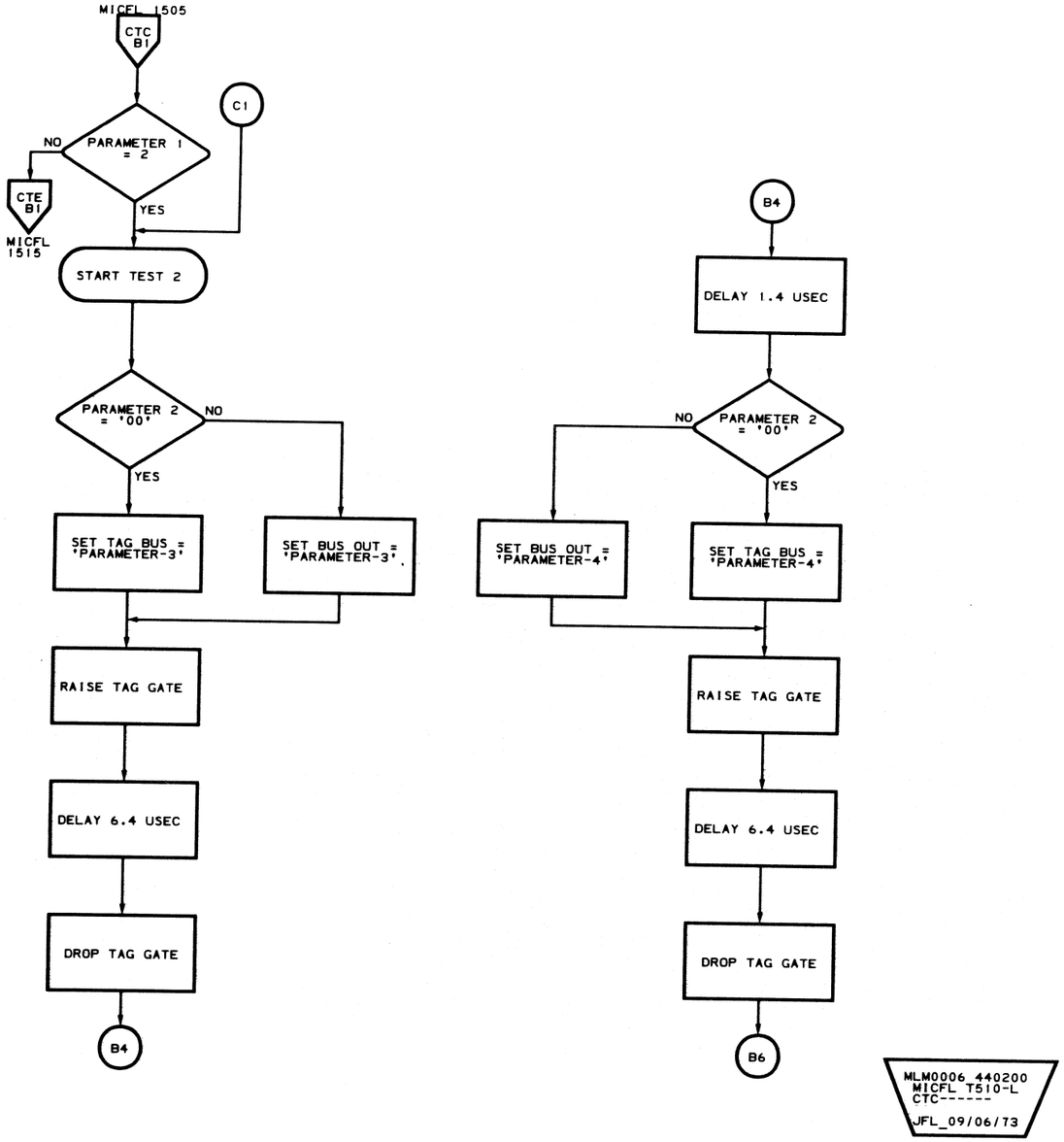

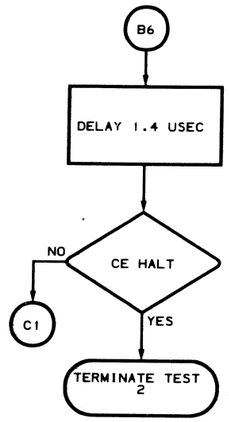

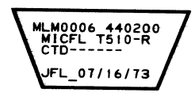

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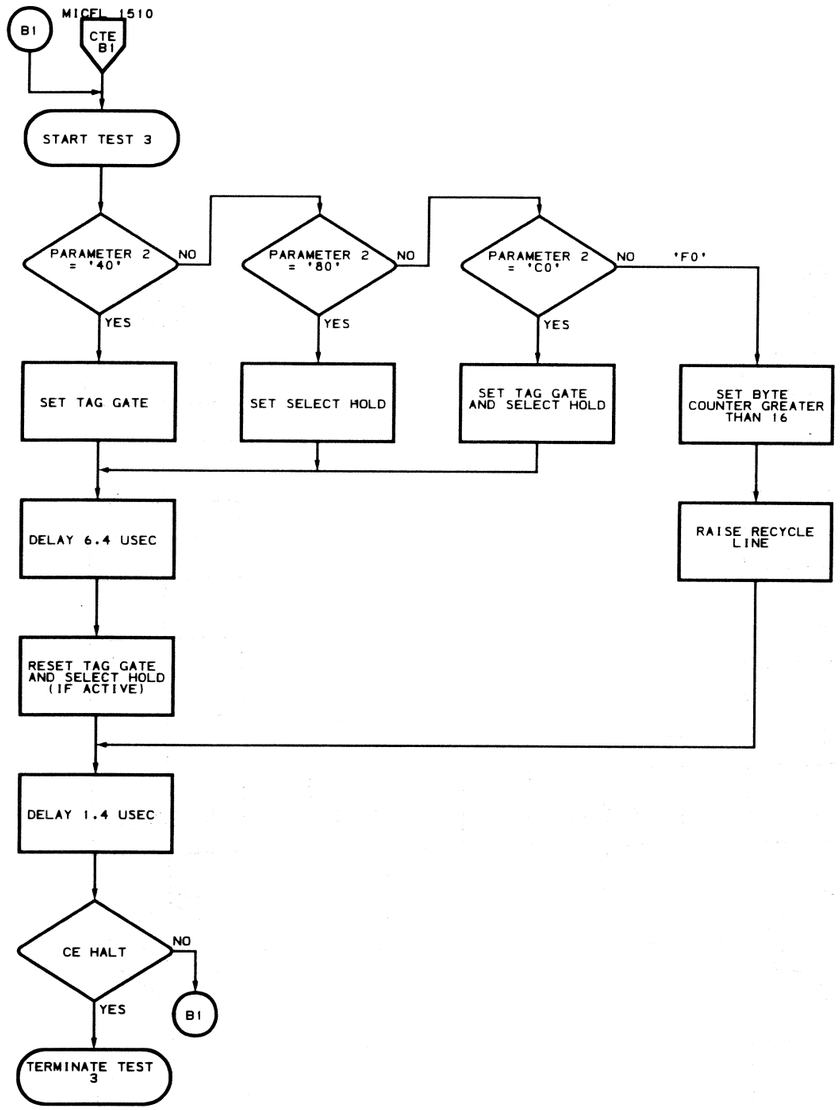

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