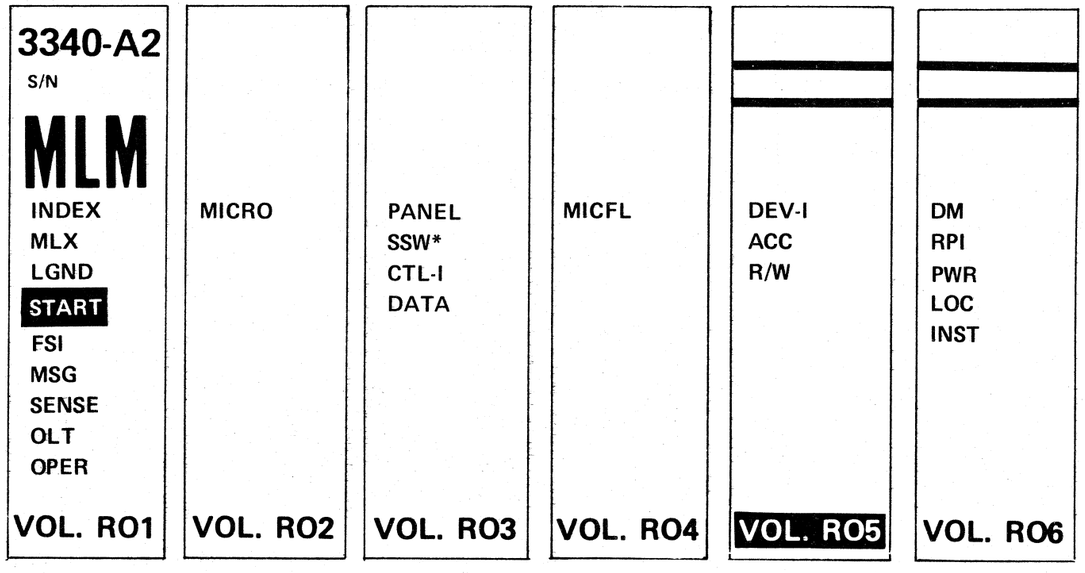
IBM Maintenance Library

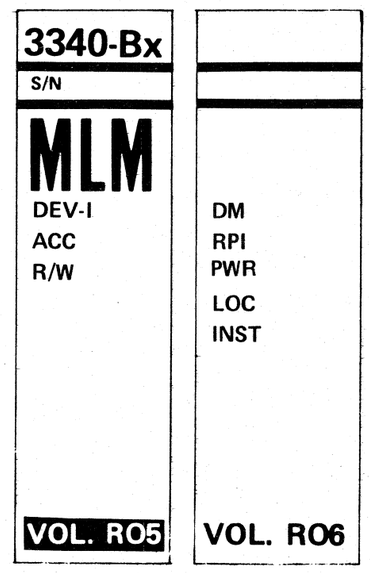
CONTROL MODULE



Volumes RO1, 2, 3, and 4 accompany only Control Modules (A2).

** This section is only with Control Modules that have the string switch feature installed.*

SATELLITE MODULE



Volumes RO5 and RO6 accompany every Control Module (A2) and every Satellite Module (B1 or B2). (One set per serial numbered frame.) To ensure proper documentation level, use the volume that goes with the module you are working on.

3340 Disk Storage

DA0010	2747526	440200	440203	440218				
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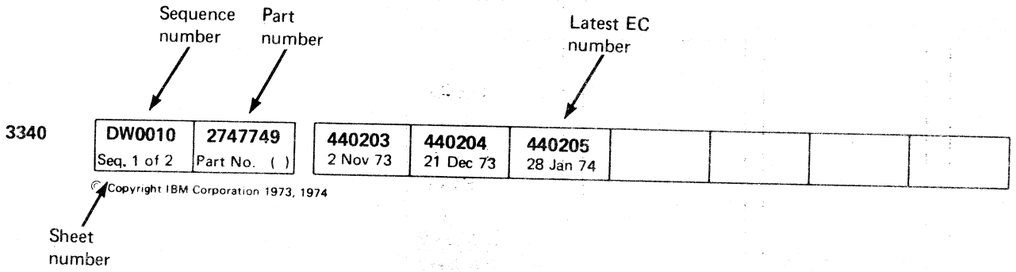
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PREFACE

MAINTENANCE LIBRARY ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3340 Maintenance Library can be ordered from the San Jose plant by using the *Wiring Diagram/Logic Page Request* (Order No. 120-1679). In the columns headed "Logic Page", enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

Example:



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DA0010	2747526	440200	440203	440218				
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SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)



2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).



3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

DEV-I CONTENTS

DEV-I MAPs – – – – – – – – – – – **DEV-I 110–293**

Provides maintenance procedures for analyzing device-interface-related problems.

Device Interface Descriptions – – – – **OPER 93**

Presents a high-level description of the Device Interface.

Interface Operation with Detailed Descriptions – – – – – – – – – – **OPER 95–105**

Presents Tag sequence, interface data and control flow, and detailed Tag and Bus descriptions.

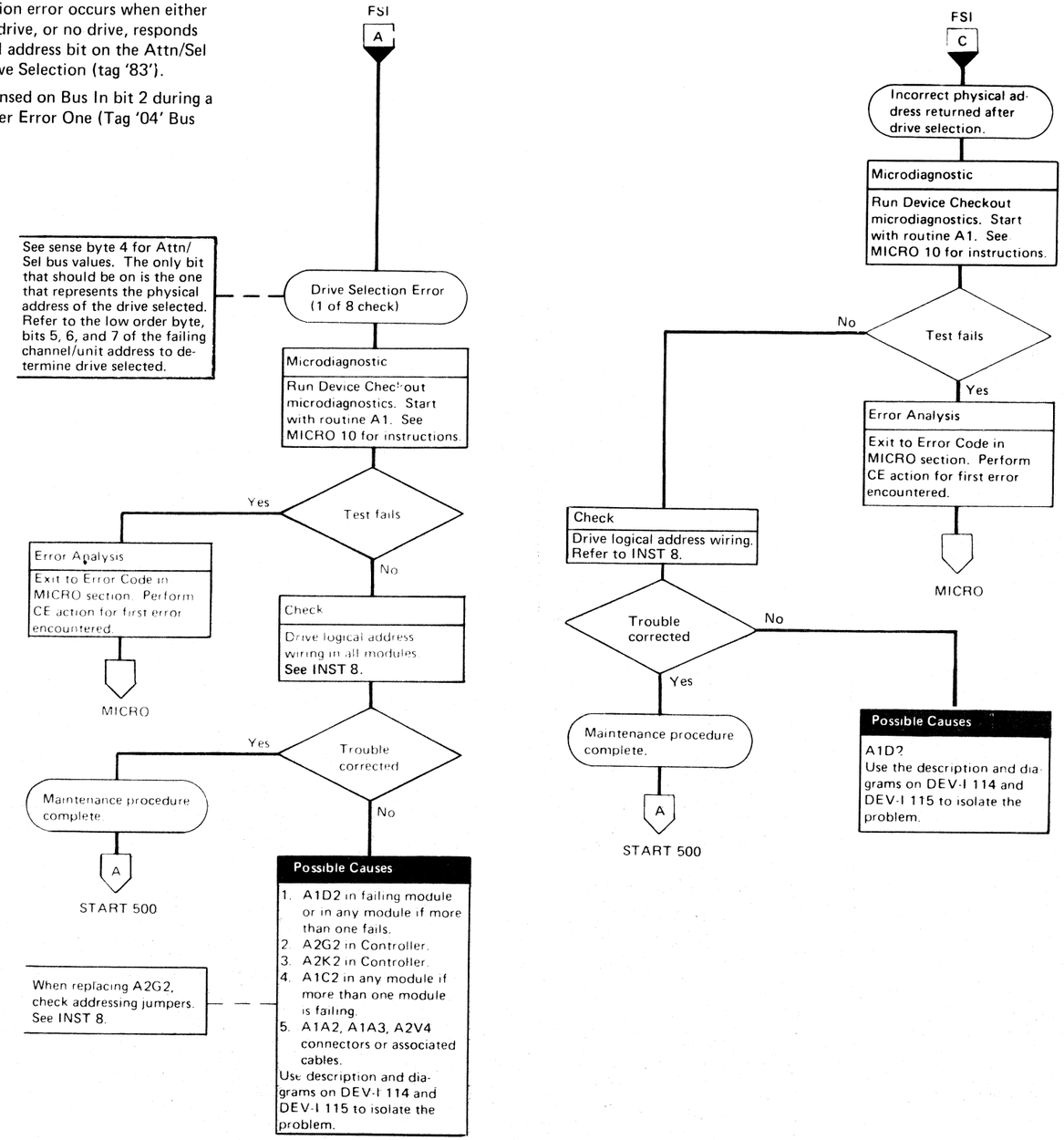
DRIVE SELECTION FAILURE

A Drive Selection error occurs when either more than on drive, or no drive, responds with a physical address bit on the Attn/Sel bus during Drive Selection (tag '83').

This error is sensed on Bus In bit 2 during a Sense Controller Error One (Tag '04' Bus Out '01').

DRIVE PHYSICAL ADDRESS

Drive Selected	Attention Select Bus
0	1000 0000
1	0100 0000
2	0010 0000
3	0001 0000
4	0000 1000
5	0000 0100
6	0000 0010
7	0000 0001

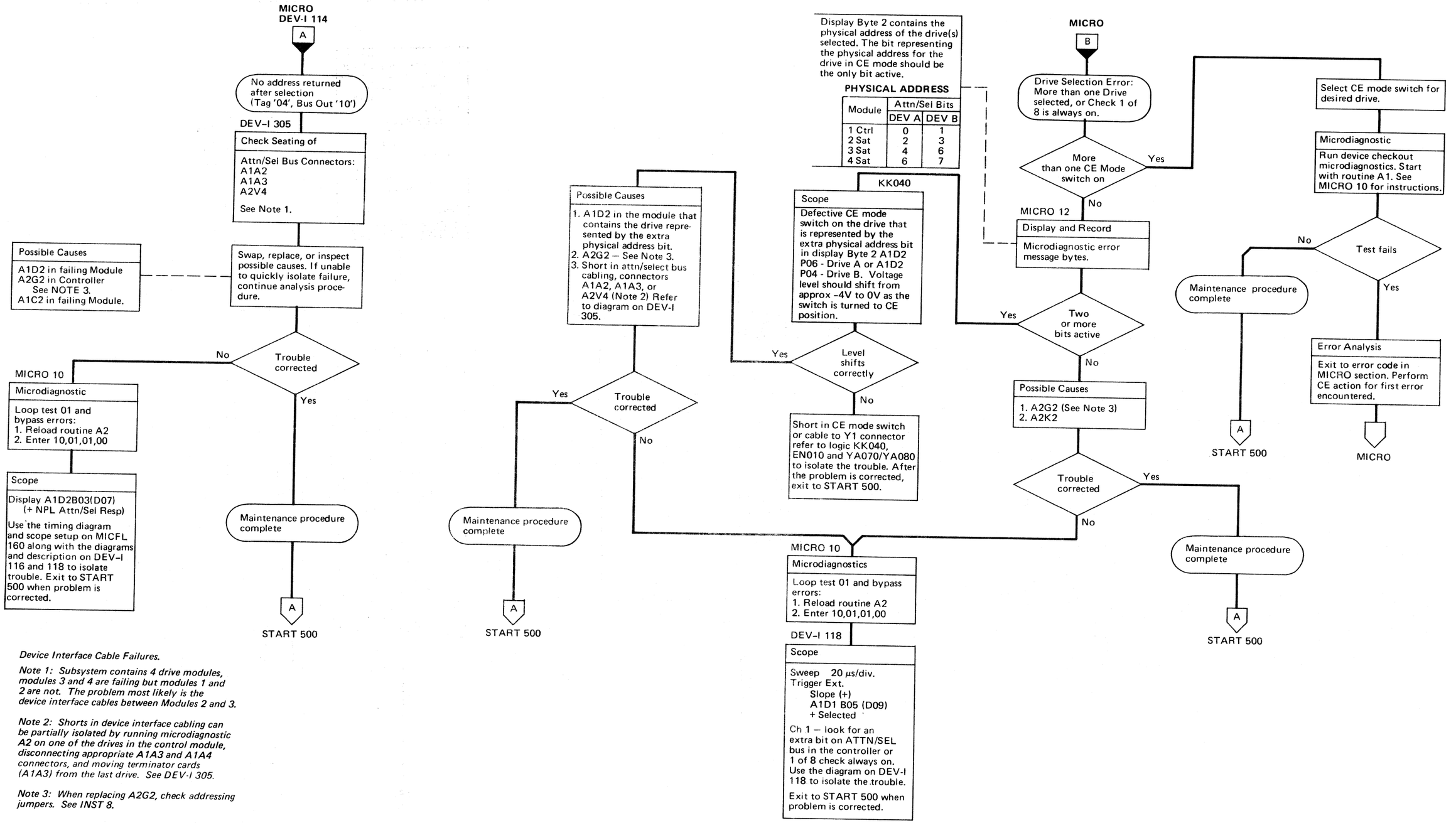


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DRIVE SELECTION FAILURE



Device Interface Cable Failures.

Note 1: Subsystem contains 4 drive modules, modules 3 and 4 are failing but modules 1 and 2 are not. The problem most likely is the device interface cables between Modules 2 and 3.

Note 2: Shorts in device interface cabling can be partially isolated by running microdiagnostic A2 on one of the drives in the control module, disconnecting appropriate A1A3 and A1A4 connectors, and moving terminator cards (A1A3) from the last drive. See DEV-I 305.

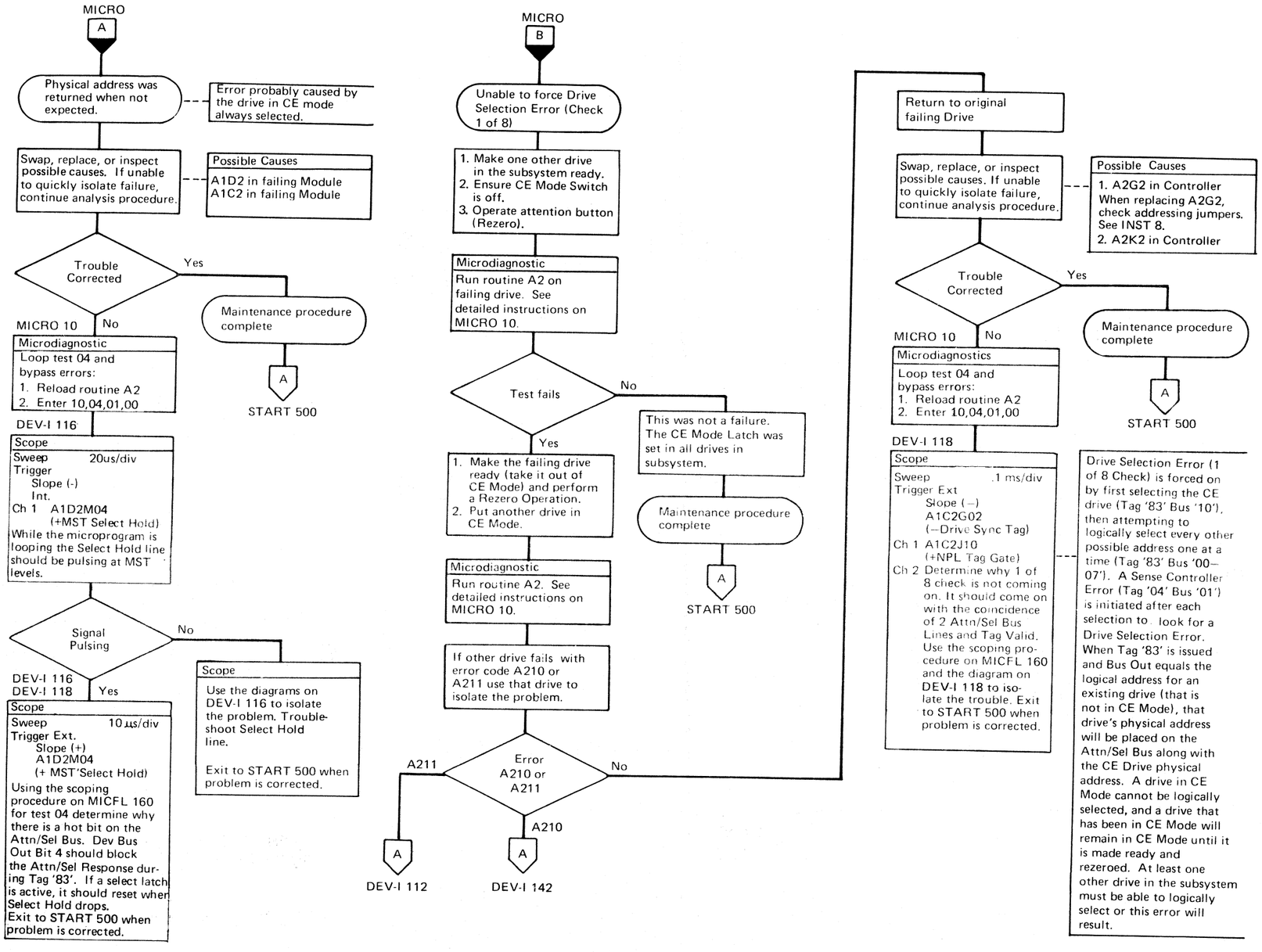
Note 3: When replacing A2G2, check addressing jumpers. See INST 8.

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DRIVE SELECTION FAILURE



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DRIVE SELECTION FAILURE

DRIVE SELECTION

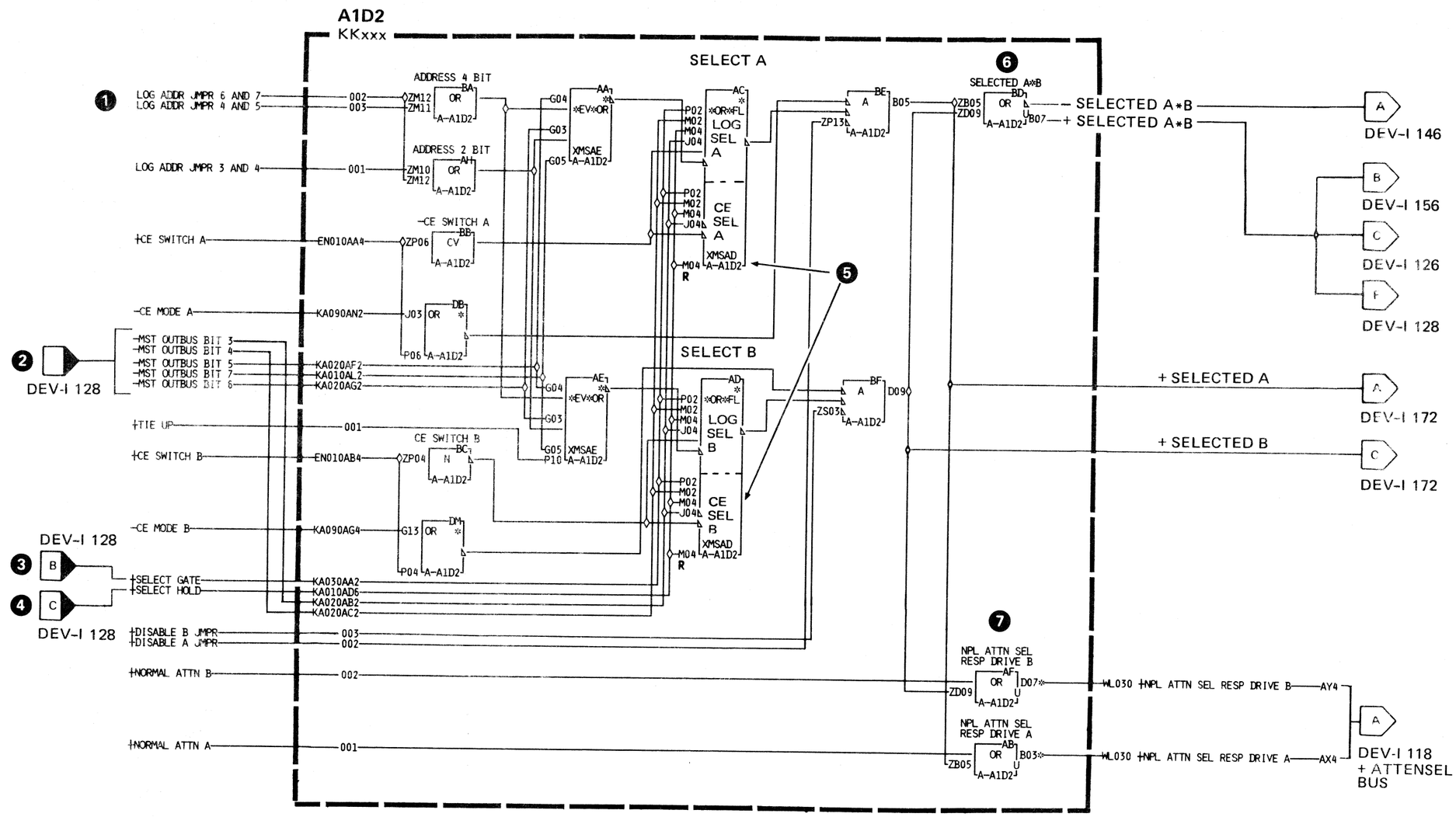
- Storage Control issues Tag '83' to the Controller with the drive's Logical Address on Bus Out bits 5, 6, and 7 (2) (respective values of 4, 2, and 1).

  Refer to OPER 104 for description of Tag '83'.

- The Storage Control brings up 'Select Hold' (4) to the Controller which becomes 'Select Hold' in the Drive.
- Controller Tag '83' becomes Device Tag '0' which decoded becomes 'Select Gates' (3).
- The Logical Address (Bus Out bits 5, 6, and 7) is compared with the Logical Address Jumpers (1) for a Logical Address Match.
- A Logical Address Match and 'Select Gate', set a Select Latch which activates selected A and B. (6)
- An Attention Select Response (7) is generated to allow the Selected Drive to place its unique physical Address Bit on the Attention Select Bus. See DEV-I 118.

CE DRIVE SELECTION – USED BY MICRODIAGNOSTICS TO SELECT A DRIVE IN CE MODE

- CE Drive Selection is the same as Normal Selection except that instead of using Out Bus bits 5, 6, and 7 for a Logical Address Match, the Storage Control brings up Out Bus bit 3 (2) along with the Tag '83'. If a CE mode switch is in the CE position, CE Select (5) is brought up.



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DRIVE SELECTION FAILURE

ATTENTION/SELECT BUS

Drive Selected

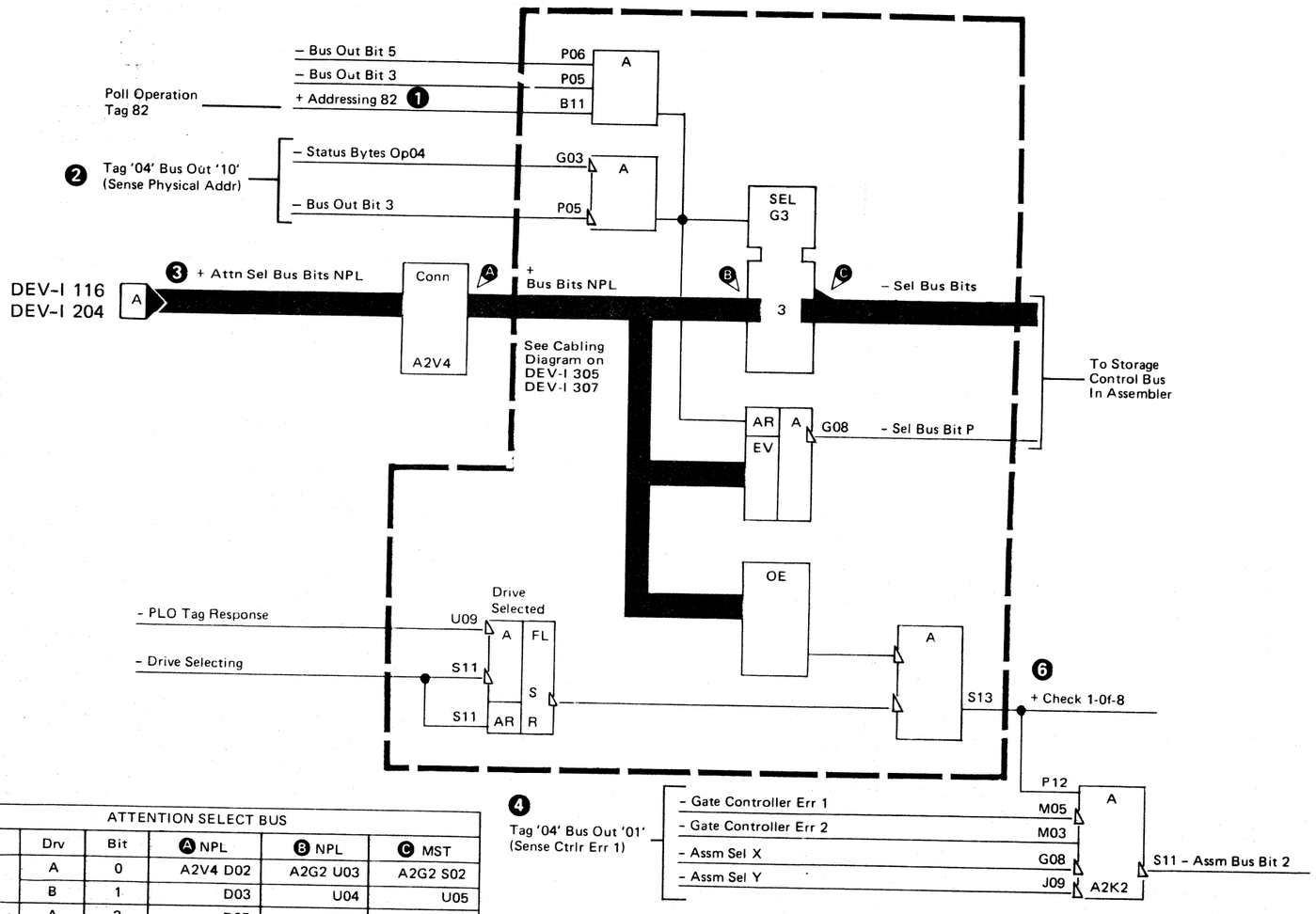
- A drive generates an attention select response when it is selected. Each drive attention select reponse line is wired to a bit on the attention select bus as indicated in the attention select bus chart. ❺
- The Attention Select Bus Lines ❸ are rotated in pairs as they pass through each Drive Module. This eliminates the need for Physical Address Jumpers during installation. See DEV-I 305 and DEV-I 307 for cabling information.
- The microprogram can interrogate the Attention Select Bus with a Sense Physical Address Tag ❷ (Tag '04' Busout '10'). The contents of the Attention Select Bus is placed on the Bus In to the storage control.
- More than one bit or an absence of bits on the Attention Select Bus when a Drive is selected results in a 1-of-8 check. ❻
- The 1-of-8 Check signals an error alert to the storage control. The Microprogram can determine the cause of the error alert by a Sense Controller error 1 Tag ❹ (Tag '04' Bus Out '01'). The 1-of-8 Check activates Bus In Bit 2.

Refer to OPER 102 for description of Tag '04'.

POLLING OPERATION – DRIVE NOT SELECTED.

Polling Operation – Drive Not Selected.

- When Storage Control polls the controller (with Tag '82' and Bus Out bits 0, 1, and 2 equal to the Controller Address the + Addressing 82 line ❶ is brought up), the Attn/Set bus is gated to Bus In and good parity is generated.

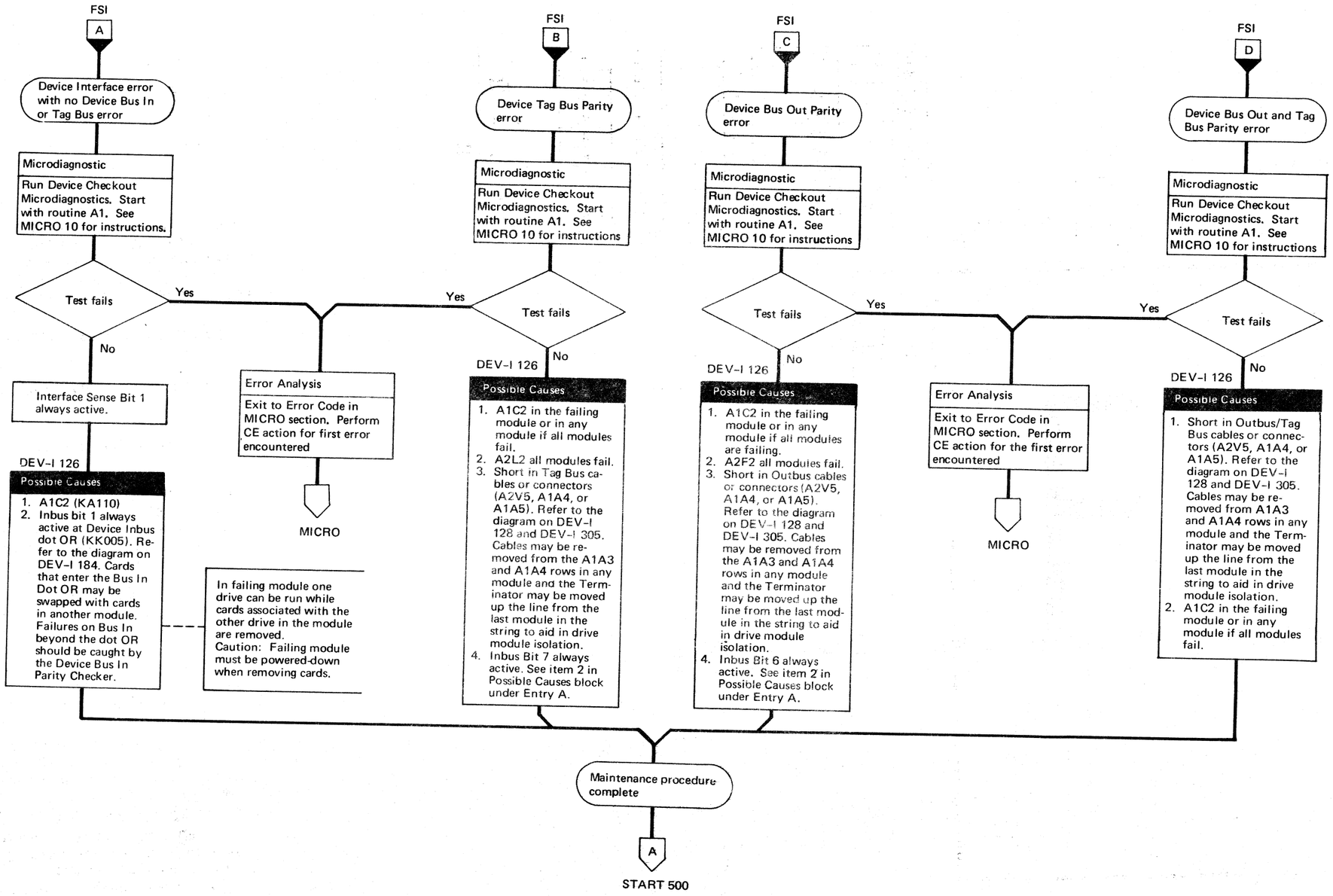


❺

ATTENTION SELECT BUS					
Module	Drv	Bit	Ⓐ NPL	Ⓑ NPL	Ⓒ MST
CTRL	A	0	A2V4 D02	A2G2 U03	A2G2 S02
	B	1	D03	U04	U05
SAT 1	A	2	D05	U06	U02
	B	3	D06	U07	M12
SAT 2	A	4	D07	S08	M13
	B	5	D09	U10	P13
SAT 3	A	6	D10	U11	S09
	B	7	D11	S12	U13

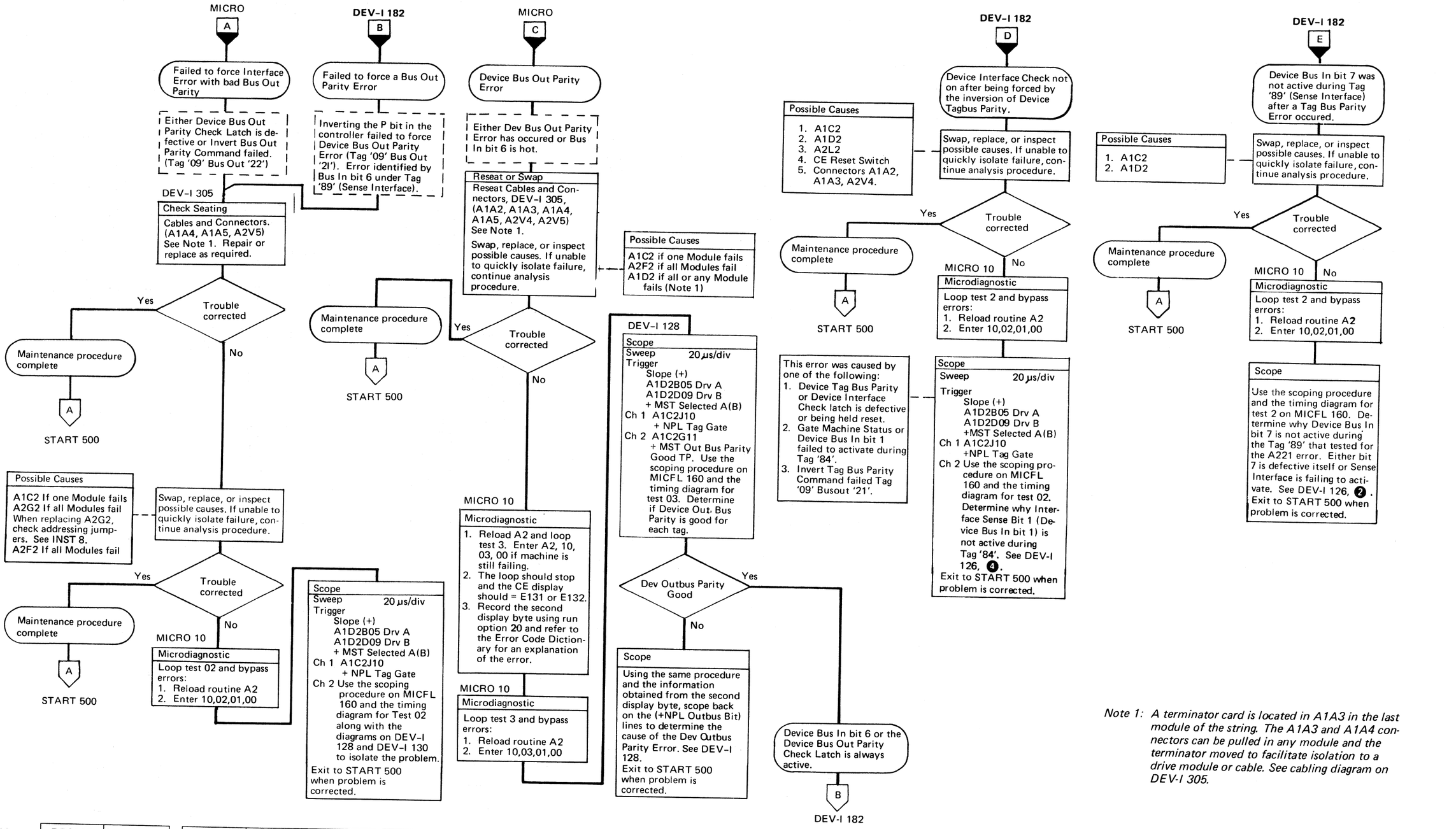
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DEVICE INTERFACE ERRORS



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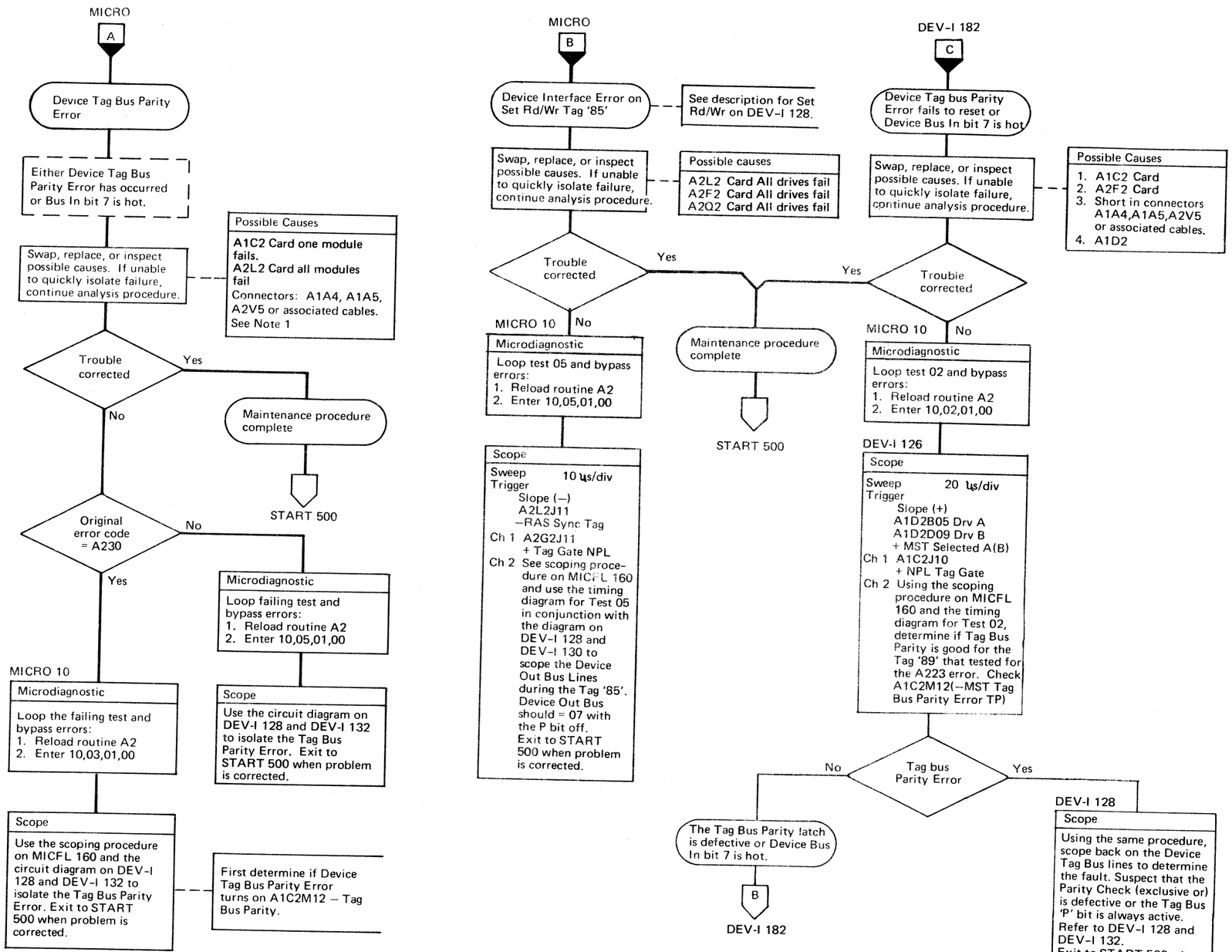
DEVICE INTERFACE ERRORS



Note 1: A terminator card is located in A1A3 in the last module of the string. The A1A3 and A1A4 connectors can be pulled in any module and the terminator moved to facilitate isolation to a drive module or cable. See cabling diagram on DEV-I 305.

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DEVICE INTERFACE ERRORS



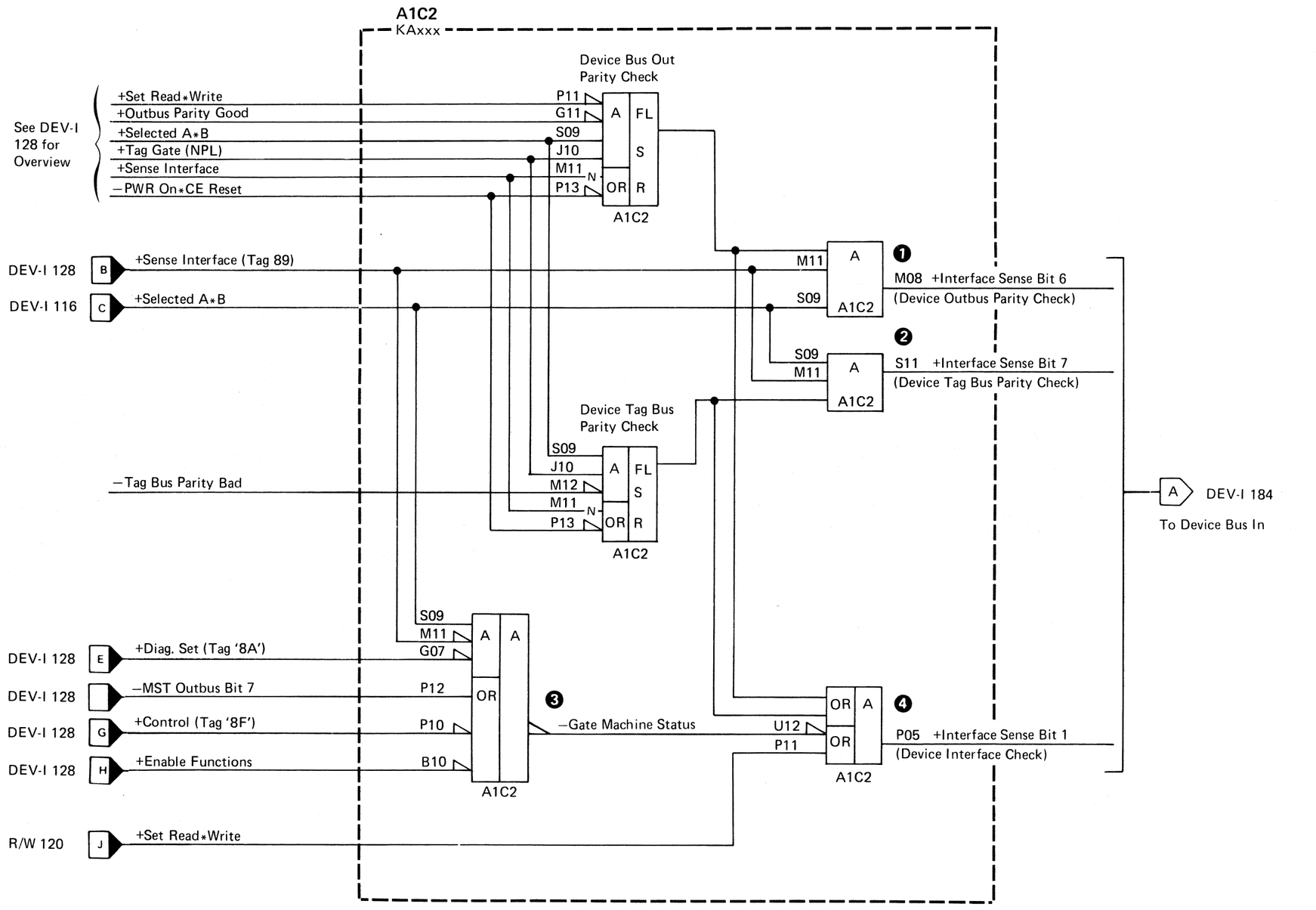
Note 1: A terminator card is located in A1A3 in the last module of the string. The A1A3 and A1A4 connectors can be pulled in any module and the terminator moved to facilitate isolation to a drive module or cable. See cabling diagram on DEV-I 305.

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DEVICE INTERFACE ERRORS

See DEV-I 300 for an overview.

- Gate Machine Status ❸ is active when Enable Functions, Tag '89' and Tag '8A' are not active. Interface Sense Bit 1 (Device Interface Check) ❹ is gated to Device Bus In when Gate Machine Status and either Device Outbus or Device Tag Bus parity check are active.
- Tag '84' (Request Drive Status tag) gates Interface Sense Bit 1 ❹ from Device Bus In to storage control on CTL Bus In Bit 1.
- The Device Interface check is further identified by Sense Interface tag '89'. Tag '89' raises device tag '1' (see chart 3, DEV-I 128) and gates Interface Sense Bit 6 ❶ or Bit 7 ❷ to DEV Bus In and to storage control on CTL Bus In.



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ENABLE FUNCTIONS

See DEV-I 300 for an overview.

Enable functions **2** is a result of no device tag bus or outbus parity errors with device tag gate active. Device tag bus and device out bus parity is generated in the controller.

During a Set Read/Write **1** (tag '85'), device outbus bits 5, 6, and 7 and device tag bus bits 0, 1, and 2 are forced to the active state. The P bits are forced to the inactive state. Device outbus parity is only checked for an instant and then is blocked to allow for read/write control. Device outbus parity checking is suspended until reset read/write (tag '05' is issued.

Refer to OPER 102–106 for tag descriptions.

Note 1: The Bus Out and Tag Bus Parity latches are reset by a (–) shift on the Sense Interface line.

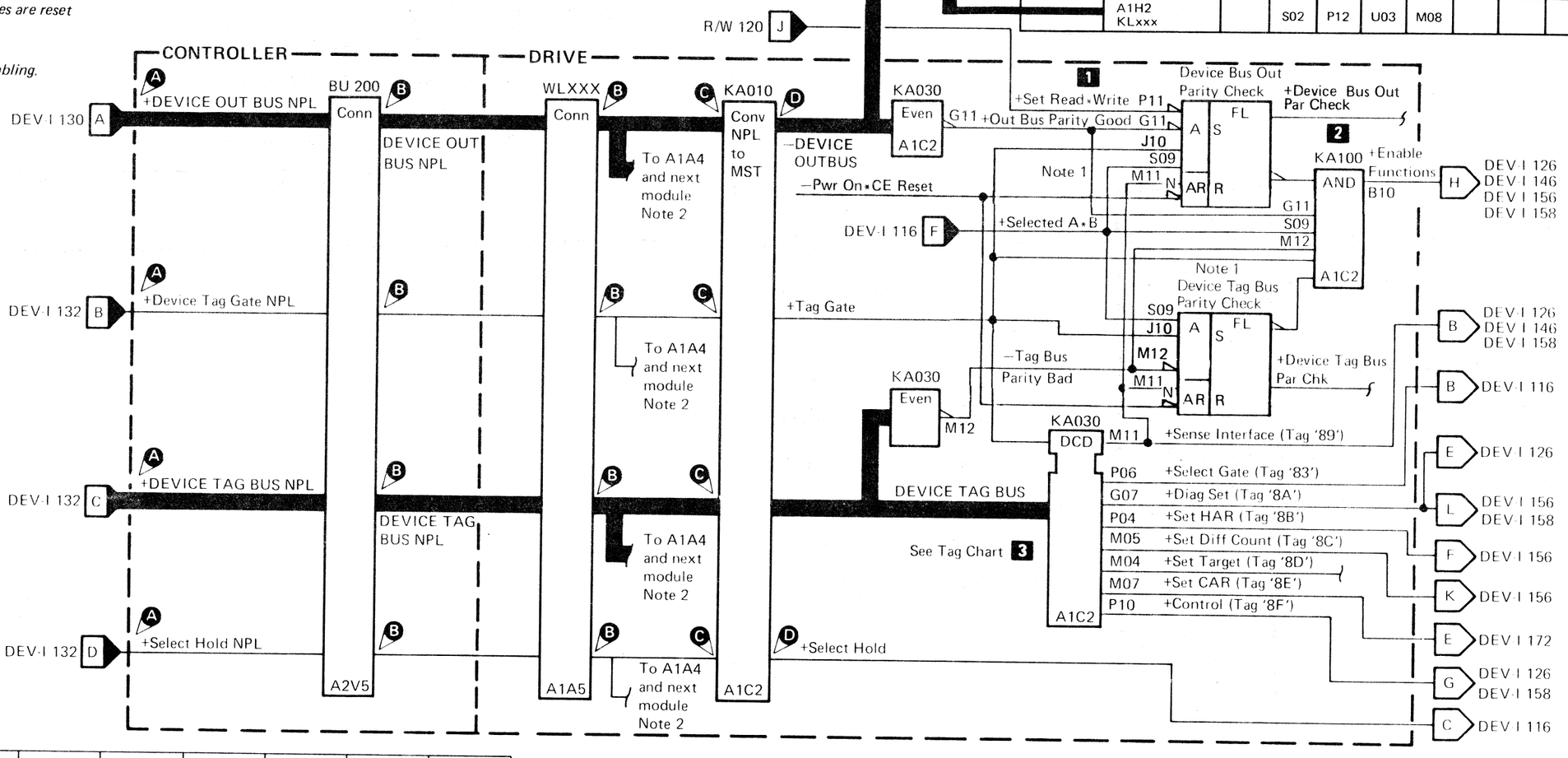
Note 2: See DEV-I 305 for Device Interface cabling.

Line Name	A NPL	B NPL	C NPL	D MST
Device Out Bus Bit 0	A2F2 P10	A2V5/A1A5 B02	A1C2 G09	A1C2 J12
Device Out Bus Bit 1	A2F2 P12	A2V5/A1A5 B04	A1C2 B13	A1C2 J13
Device Out Bus Bit 2	A2F2 U02	A2V5/A1A5 B05	A1C2 J02	A1C2 P03
Device Out Bus Bit 3	A2F2 S03	A2V5/A1A5 B06	A1C2 D13	A1C2 P02
Device Out Bus Bit 4	A2F2 S12	A2V5/A1A5 B08	A1C2 B04	A1C2 G04
Device Out Bus Bit 5	A2F2 U12	A2V5/A1A5 B09	A1C2 B03	A1C2 U04
Device Out Bus Bit 6	A2F2 U05	A2V5/A1A5 B10	A1C2 D03	A1C2 M13
Device Out Bus Bit 7	A2F2 U09	A2V5/A1A5 B12	A1C2 J11	A1C2 P13
Device Out Bus Bit P	A2F2 M07	A2V5/A1A5 B13	A1C2 D04	
Device Tag Gate	A2L2 J02	A2V5/A1A5 D07	A1C2 J10	
Device Tag Bus Bit 0	A2L2 J10	A2V5/A1A5 D02	A1C2 U03	
Device Tag Bus Bit 1	A2L2 P03	A2V5/A1A5 D03	A1C2 S02	
Device Tag Bus Bit 2	A2L2 J12	A2V5/A1A5 D05	A1C2 U02	
Device Tag Bus Bit P	A2L2 J04	A2V5/A1A5 D06	A1C2 S03	
Select Hold	A2L2 M03	A2V5/A1A5 D09	A1C2 G10	A1C2 J09

Device outbus off-page references, card locations and bit identification. (Any card can affect the bits associated with that card on the device outbus).

–Device Outbus Distribution

MLM Reference	Card (Logic)	Bit 0	1	2	3	4	5	6	7
DEV-I 116	A1D2 (KKxxx)				J04	M02	G04	G03	G05
DEV-I 156	A1F2(A1E2) KBxxx (KCxxx)	M04	G13	P05	P10	S02	M10	J13	P06
DEV-I 158 DEV-I 126	A1C2 (KAxxx)					G04	U04	M13	P12
DEV-I 172	A1J4 (KMxxx)	B02	B03	B04	B05	B10	D11	B12	B13
RPI 604 RPI 605	A1G2 (KDxxx)	P02	B03	B05	B04	G12	J13	G13	J06
	A1N2 (KJxxx)	M11	U09						
	A1P2 (KHxxx)	M11	U09						
	A1H2 KLxxx		S02	P12	U03	M08			



3

Tag	Name	Device Tag Bus Bits P	0	1	2
83	Select Gate	1	0	0	0
89	Sense Interface	0	0	0	1
8A	Diag Set	0	0	1	0
8B	Set HAR	1	0	1	1
8C	Set Diff Count	0	1	0	0
8D	Set Target	1	1	0	1
8E	Set CAR	1	1	1	0
8F	Control	0	1	1	1

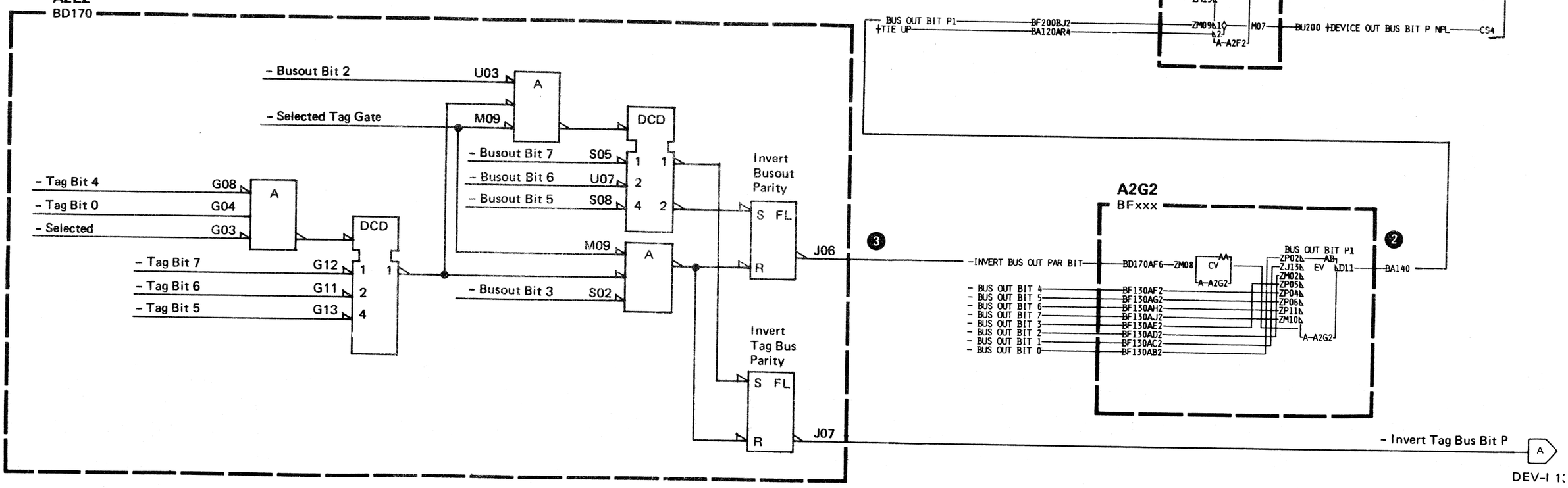
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DEVICE INTERFACE ERRORS

DEVICE OUTBUS

- Device Outbus (1) is developed from Control Interface Busout.
- Device Outbus Parity (2) is generated in the Controller (A2-Board) and checked in each Device (A1-Board).
- By Microprogramming Busout and Device Busout, Parity can be inverted for diagnostic purposes, (3)
  Tag '09' Busout '72' – Invert Busout and Device Busout Parity
  Tag '09' Busout '10' – Reset Invert Busout and Device Busout Parity
- Set Read/Write (4) (Tag '85') switches the Device Outbus to a Read/Write Control Bus. Bits 5, 6, and7 are forced to an active state and the P bit is forced to the inactive state.

Refer to OPER 102–106 for tag descriptions.



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DEVICE INTERFACE ERRORS

DEVICE TAG BUS

Device Tag Bus bits 0, 1, and 2 ❷ (see Figure 1), are developed from Control Interface Tag Bus bits 5, 6, and 7 except for the following conditions:

- Set Read/Write, Tag '85' forces Device Tag Bus bits 0, 1, and 2 and Device Tag Gate to active state and Device Tag Bus bit P to the inactive state.
- Sense Drive Status, Tag '84' is not a Device Tag and does not activate Device Tag Bus or Device Tag Gate.
- Drive Select, Tag '83' (Controller addressed and Tag Bit 0) hold the Device Tag Bus register reset, forcing Device Tag Bus to zero.

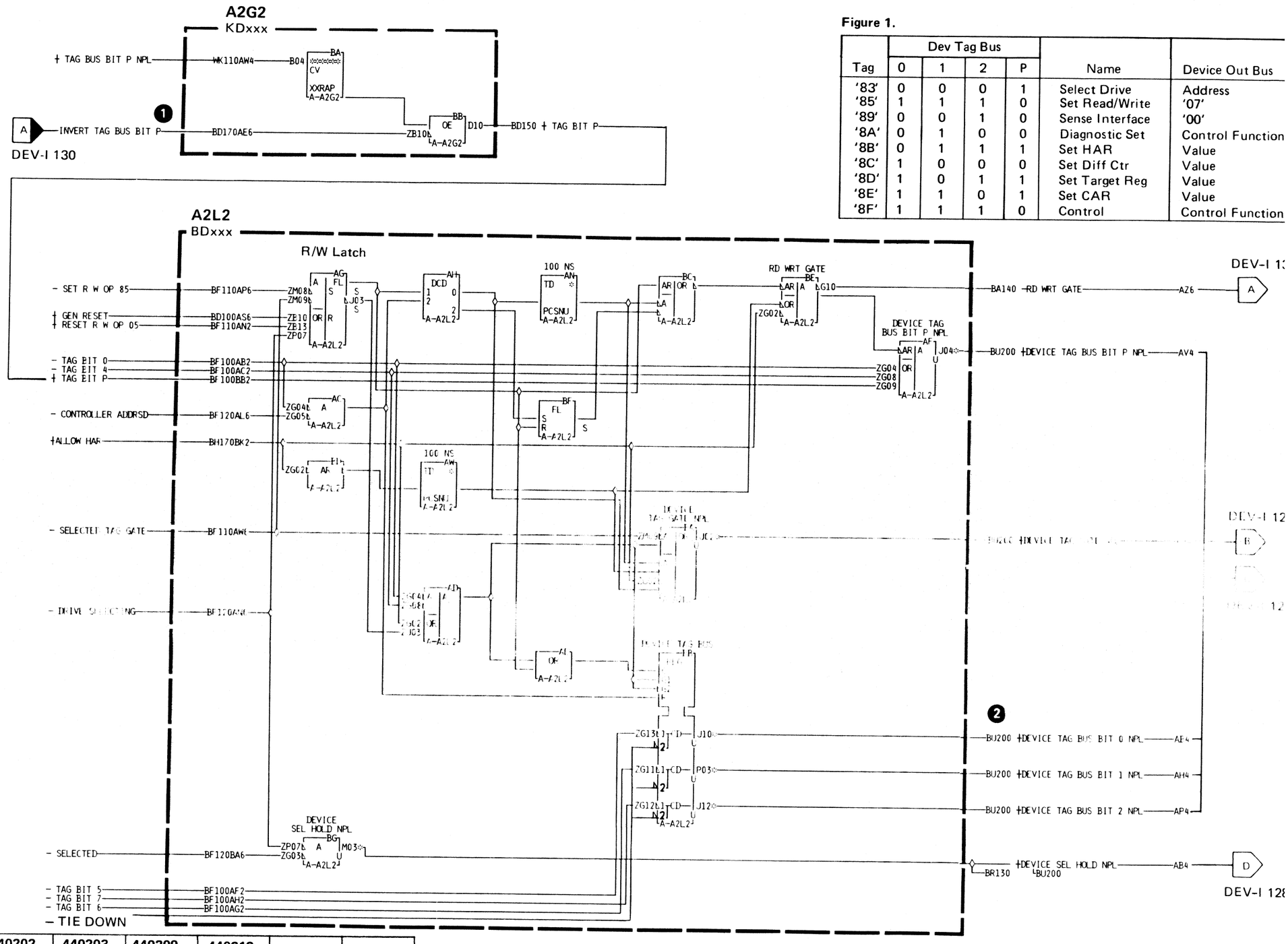
By microprogramming Tag Bus and Device Tag Bus, parity can be inverted for diagnostic purposes ❶. See DEV-I 130:

Tag '09' Bus Out '21' – Invert Tag Bus Parity
Tag '09' Bus Out '10' – Reset Invert Tag Bus Parity

Refer to OPER 102 for description of Tag '09'.

Figure 1.

Tag	Dev Tag Bus 0	1	2	P	Name	Device Out Bus
'83'	0	0	0	1	Select Drive	Address
'85'	1	1	1	0	Set Read/Write	'07'
'89'	0	0	1	0	Sense Interface	'00'
'8A'	0	1	0	0	Diagnostic Set	Control Function
'8B'	0	1	1	1	Set HAR	Value
'8C'	1	0	0	0	Set Diff Ctr	Value
'8D'	1	0	1	1	Set Target Reg	Value
'8E'	1	1	0	1	Set CAR	Value
'8F'	1	1	1	0	Control	Control Function

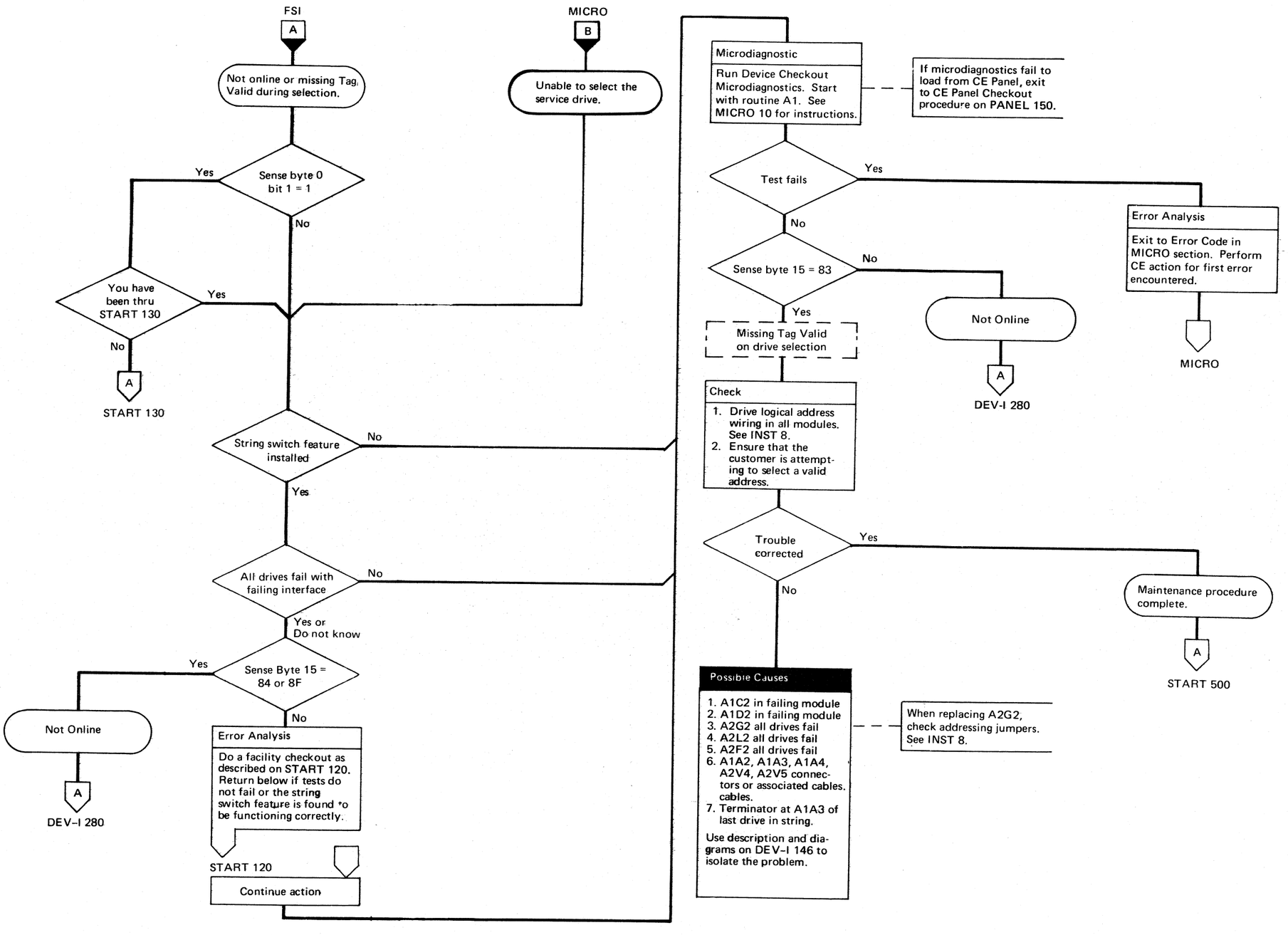


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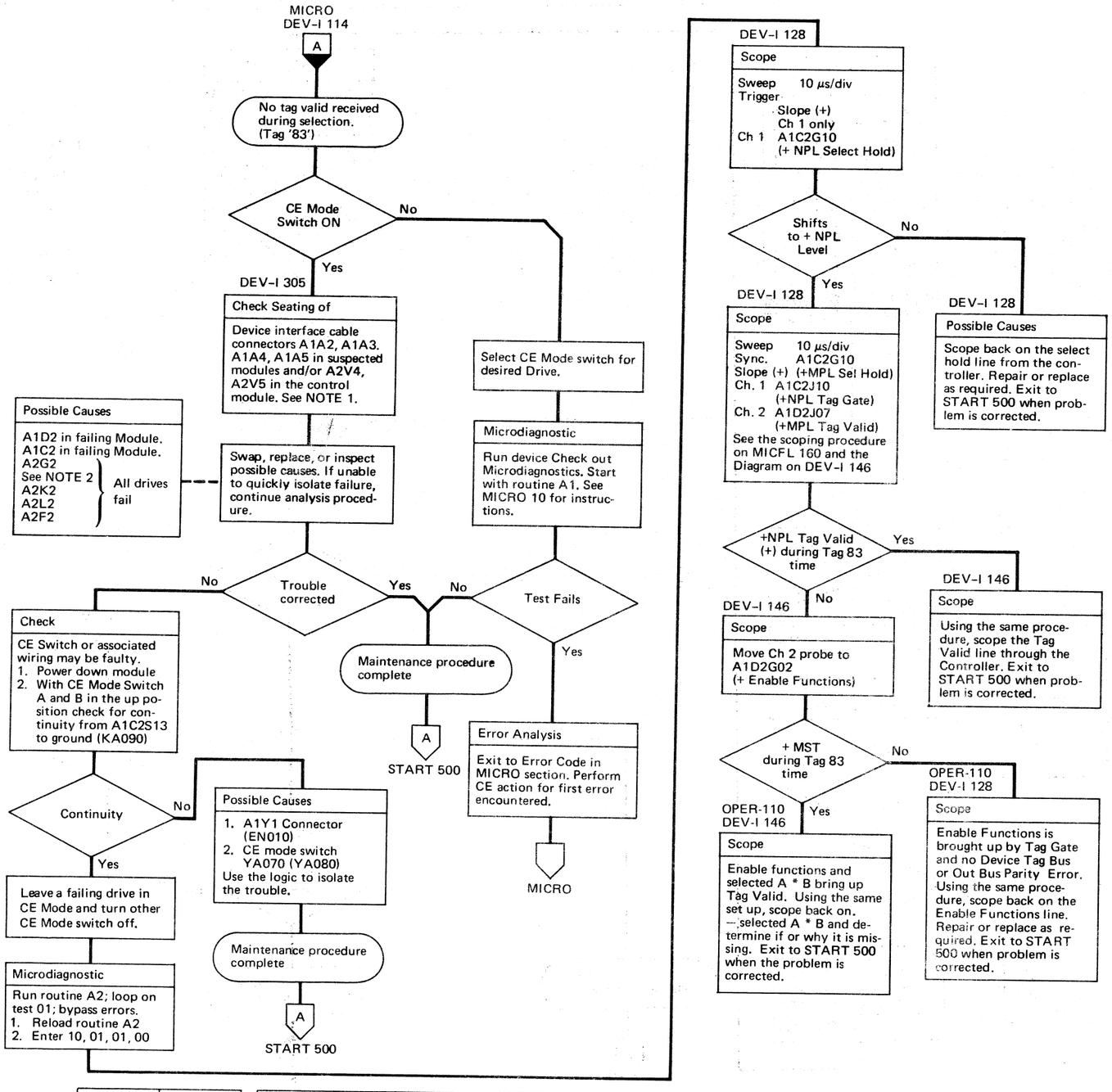
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FILE TAG VALID FAILURE



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FILE TAG VALID FAILURE



Note 1: Example:

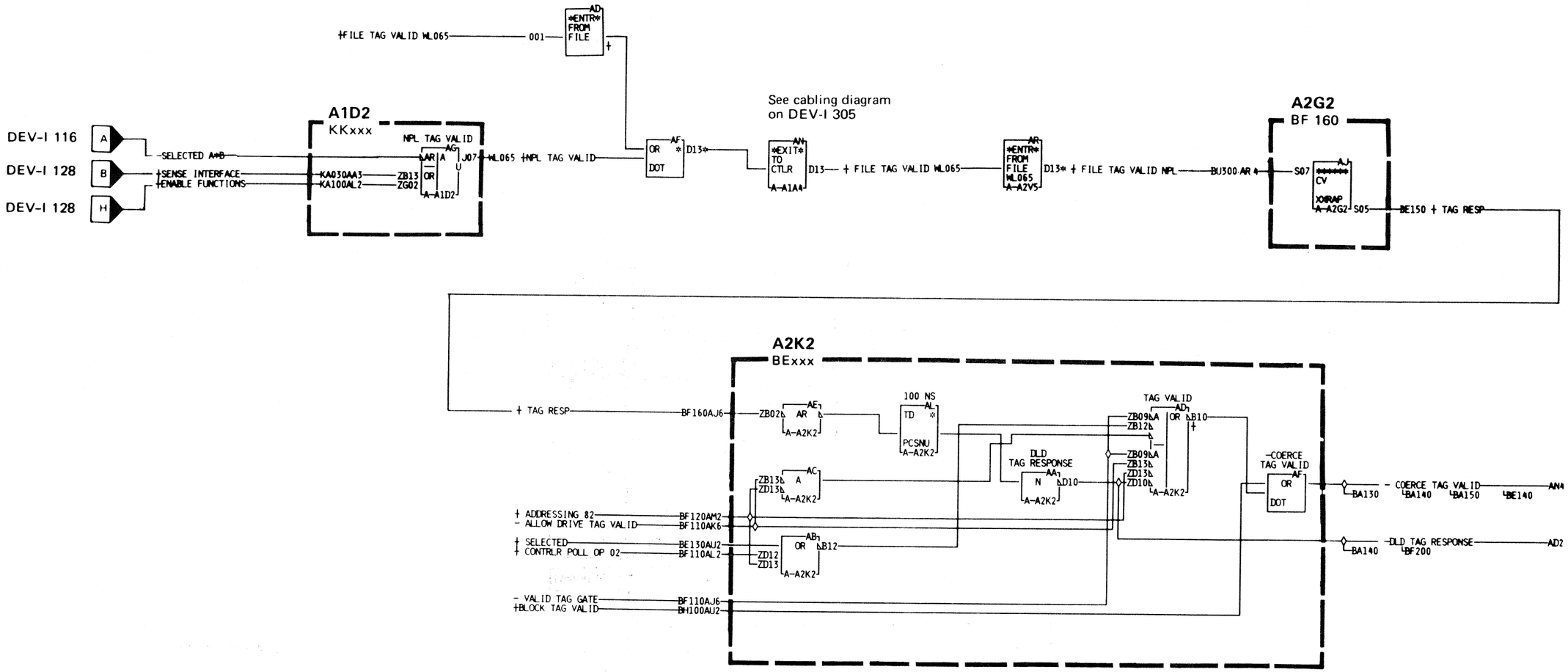
Subsystem contains 4 drive modules; modules 3 and 4 are failing, but modules 1 and 2 are not. The problem most likely is in the device interface cables between modules 2 and 3.

Note 2: When replacing A2G2, check addressing jumpers. See INST 8.

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FILE TAG VALID

- File Tag Valid is sent to the controller over the Device Interface. It becomes Coerce Tag Valid which is sent to the Storage Control over the Control Interface as Tag Valid.
- File Tag Valid results from the controller propagating Tag Gate to the device over the device interface along with good parity on Device Tag Bus and Device Out Bus.



DB0143 Seq. 1 of 2	2747146 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440218 5 Aug 74		

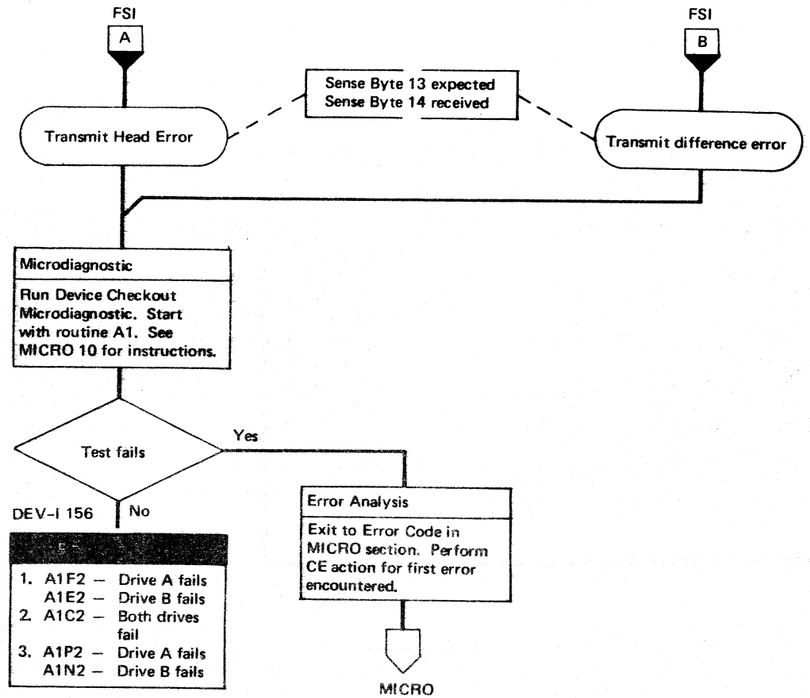
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TRANSMIT HEAD / TRANSMIT DIFFERENCE ERROR

Transmit Head Error – Unexpected results on Bus In during a Sense HAR command (Tag '8F' Bus Out '05').

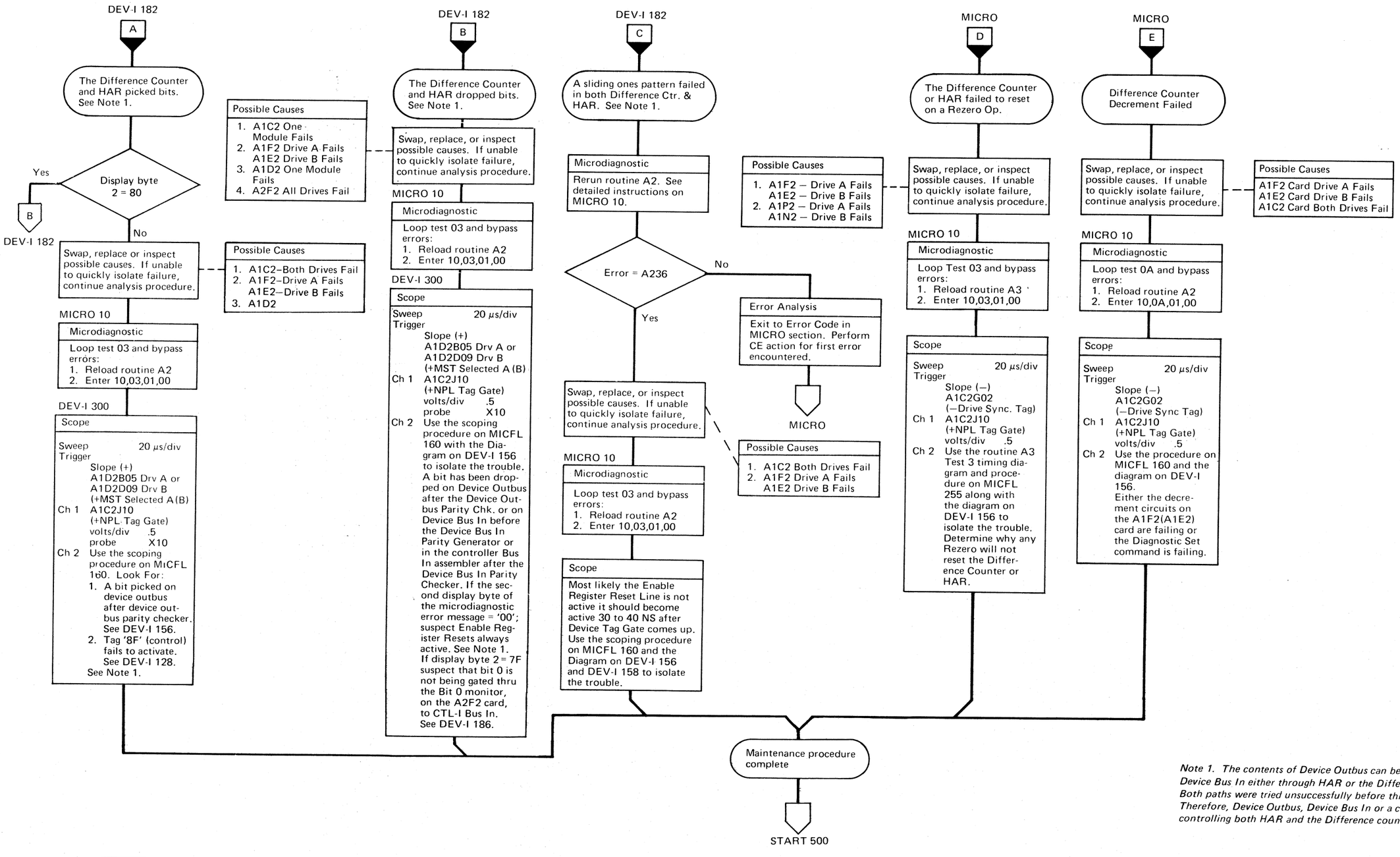
Transmit Difference Error – Unexpected results on Bus In during a Sense Difference Counter command (Tag '8F' Bus Out '09').

Refer to OPER 105 for description of Tag '8F'.



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HAR AND DIFFERENCE COUNTER FAILURES



Note 1. The contents of Device Outbus can be transferred to Device Bus In either through HAR or the Difference counter. Both paths were tried unsuccessfully before this error occurred. Therefore, Device Outbus, Device Bus In or a control line controlling both HAR and the Difference counter failed.

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HAR AND DIFFERENCE COUNTER FAILURES

MICRO A

HAR Picked Bits
HAR was Set to '00'

Swap, replace or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

1. Operate CE Reset.
2. Rerun A2.

Error A282 — Yes / No

Exit to Error Code Dictionary

MICRO

DEV-I 156
If Display Byte 2 = 'FF', most likely set HAR is always active.

MICRO B

HAR Dropped Bits
HAR was Set to 'FF'

Swap, replace or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

DEV-I 156
If Display Byte 2 = '00', most likely set HAR or Sense HAR failed to activate.

MICRO 37

Microdiagnostic

Run microdiagnostic B4 with the following Tag sequence:
1. Tag '83' Bus Out '10' - Select CE Drive
2. Tag '8F' Bus Out '0A' - Drive Sync. Tag
3. Tag '8B' Bus Out 'XX' - Set HAR to value on Bus Out
   XX = Desired failing data pattern.
4. Tag '8F' Bus Out '05' - Sense HAR (HAR value is put on Device Bus In)

Load routine B4.
Enter: 10,83,10,8F,0A, 8B,XX,8F,05,00,00,00, 00,00,00,00,00.
XX = Failing Data Pattern

Scope

Sweep 10 µs/div
Trigger
Slope (–) A1C2G02 (–Drive Sync. Tag)
Ch 1 A1C2J10 (+NPL Tag Gate volts/div 0.5 Probe X10
Ch 2 Use timing diagram 'A' with DEV-I 156. Isolate the problem by scoping HAR control lines and bit lines.
Exit to START 500 when problem is corrected.

START 500

MICRO C

HAR Picked or Dropped Bits With Random Data Pattern

Swap, replace or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

DEV-I 156
Display Byte 2 = Received Bus In Display Byte 3 = Expected Bus In.

MICRO D

Difference Ctr. picked bits. It was set to '00'.

Swap, replace or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

DEV-I 156
If Display Byte 2 = 'FF', most likely Set Difference Ctr is always active.

MICRO E

Difference Ctr dropped bits. It was set to 'FF'.

Swap, replace or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

DEV-I 156
If Display Byte 2 = '00', most likely Set Difference Ctr or Sense Difference Ctr failed to activate.

Microdiagnostic

Run microdiagnostic B4. With the following tag sequence:
1. Tag '83' Bus Out '10' - Select CE Drive
2. Tag '8F' Bus Out '0A' - Drive Sync Tag
3. Tag '8C' Bus Out 'XX' – Set Difference Ctr to value on Bus Out. XX = Desired failing data pattern.
4. Tag '8F' Bus Out '09' - Sense Difference Ctr. (Difference Ctr value is put on Dev Bus In.)

Load routine B4.
Enter: 10,83,10,8F,0A, 8C,XX,8F,09,00,00,00, 00,00,00,00,00.
XX = Failing Data Pattern

Scope

Sweep 10 µs/div
Trigger
Slope (–) A1C2G02 (–Drive Sync. Tag)
Ch 1 A1C2J10 (+NPL Tag Gate) volts/div 0.5 Probe X10
Ch 2 Use Timing Diagram 'B' with DEV-I 156. Isolate the problem by scoping Difference Ctr. Control lines and Bit Lines.
Exit to START 500 when problem is corrected.

START 500

MICRO F

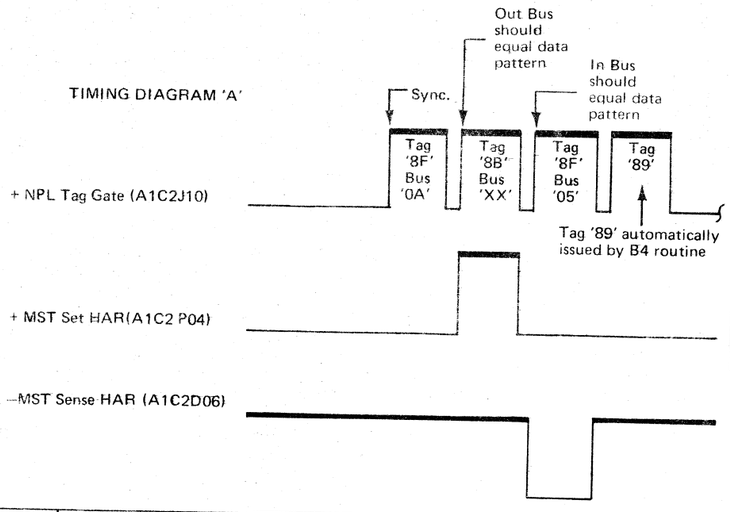
Difference Ctr. picked or dropped bits random data pattern.

Swap, replace or inspect possible causes. If unable to quickly isolate failure continue analysis procedure.

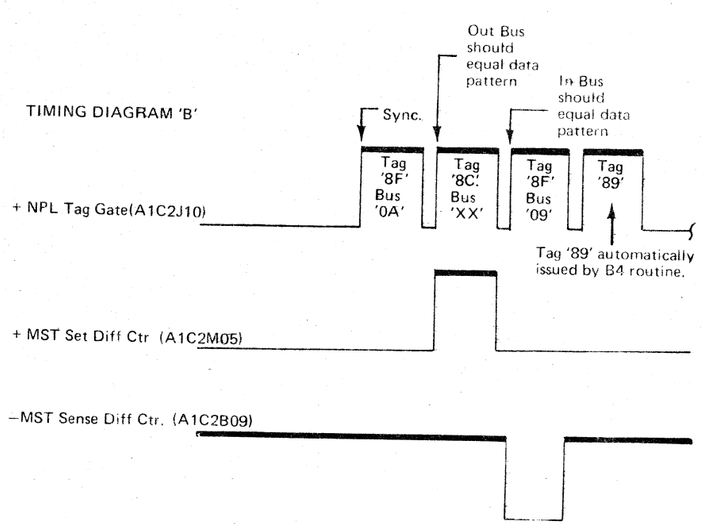
DEV-I 156
Display Byte 2 = Received Bus In Display Byte 3 = Expected Bus In

Possible Causes
1. A1F2 Drive A Fails
   A1E2 Drive B Fails
2. A1C2 Both Drives Fail

TIMING DIAGRAM 'A'



TIMING DIAGRAM 'B'



TRANSMIT HAR AND DIFFERENCE COUNTER

See DEV-I 300 for an overview.

Refer to OPER 105 for descriptions of Tag '8A'–'8F'.

Set HAR (Tag '8B')

- Resets HAR before setting it.
- Set HAR command and Enable Functions load HAR with the value on MST Out bus, bits 0–7.

Reset HAR

- Any Rezero
- Power On or CE Reset.
- Set HAR command and Enable Reg Reset resets HAR.

Decrement HAR (Tag '8A', Bus Out '01')

- HAR bit 1 is the Difference Counter bit 256 and is decremented by the Difference Counter decrement controls.

Sense HAR (Tag '8F', Bus Out '05')

- Sense HAR command gates the value of HAR to Device In Bus.

Set Difference Counter (Tag '8C')

- Resets Difference Counter before setting it.
- Set Diff Count command and Enable Functions set the Difference Counter to the value on the MST Out Bus.

Reset Difference Counter

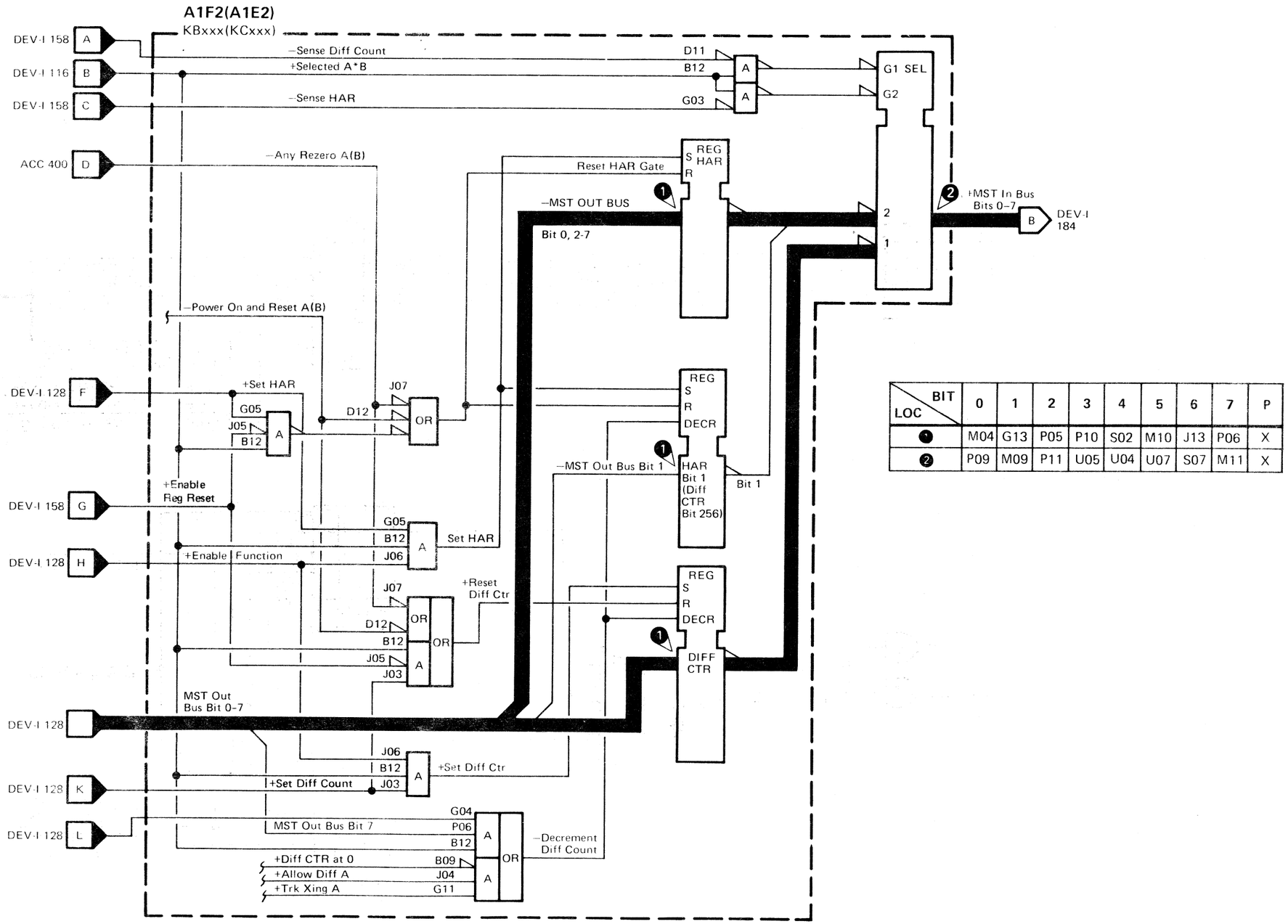
- Any Rezero
- Power On or CE Reset
- Set Diff Count command and Enable Reg Reset resets the Difference Counter.

Decrement Difference Counter (Tag '8A', Bus Out '05')

- During a Seek operation with Allow Diff and each track crossing pulse.
- Diagnostic Set command and MST Bus bit 7 on (Diff count decrements by 1).

Sense Difference Counter (Tag '8F', Bus Out '09')

- Diff Count Sense command gates the Difference counter value to the Device In Bus.



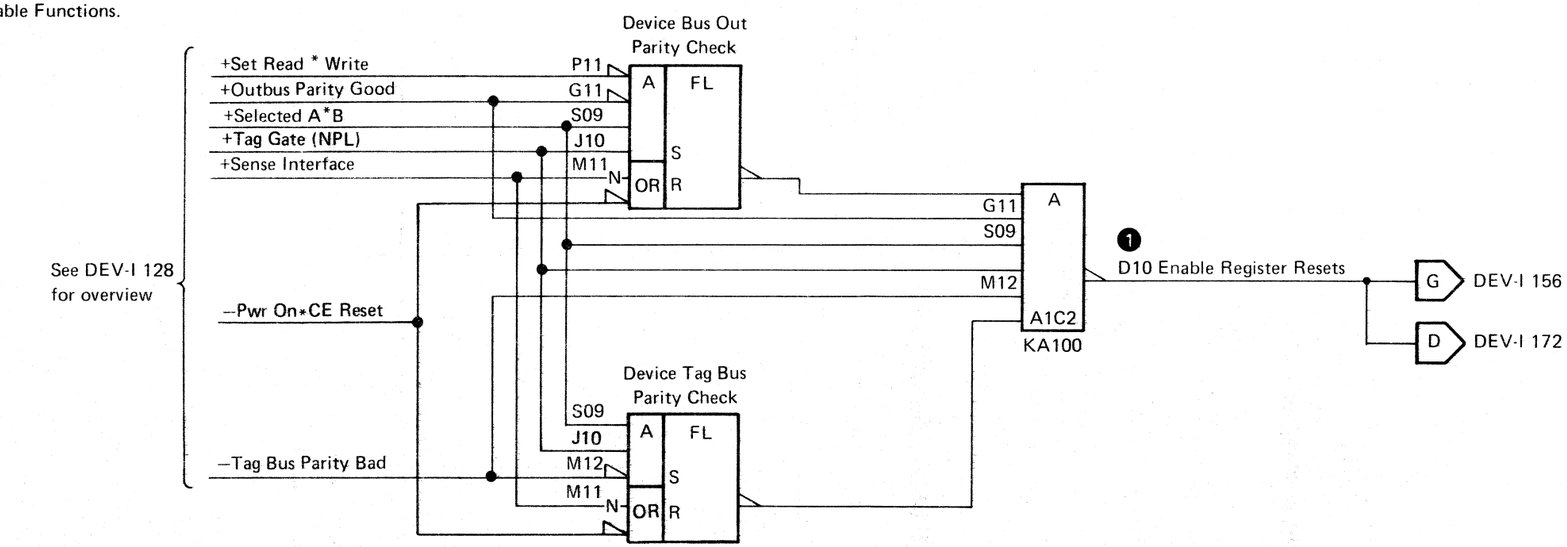
LOC \ BIT	0	1	2	3	4	5	6	7	P
❶	M04	G13	P05	P10	S02	M10	J13	P06	X
❷	P09	M09	P11	U05	U04	U07	S07	M11	X

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ENABLE REGISTER RESETS

Enable Register Resets ❶ is a result of No Device Tag Bus or Device Outbus Parity Errors with Device Tag Gate active. Enable Register reset is developed in the same way as Enable Functions. Refer to DEV-I 128.



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TRANSMIT CAR ERROR

Unexpected results on Bus In during a Sense CAR Tag (Tag '8F', Bus Out '01').

Refer to OPER 105 for description of Tag '8F'.

FSI
A

Sense Byte 13 – Expected
Sense Byte 14 – Received

Transmit CAR error

MICRO 10

Microdiagnostic

Run Device Checkout microdiagnostics. Start with routine A1.

Test fails

Yes

Error Analysis

Exit to Error Code in MICRO section. Perform CE action for first error encountered.

MICRO

No

Possible Causes

1. A1J4
2. A1C2

Use the diagram on DEV-I 172 to isolate the trouble. After the trouble is corrected, exit to START 500.

MICRO
B

CAR picked bits. It was set to '00'

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Possible Causes

1. A1J4
2. A1C2

DEV-I 172

If display byte 2 = FF, most likely Set CAR is always active.

MICRO
C

CAR dropped bits. It was set to 'FF'

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Possible Causes

1. A1J4
2. A1C2

DEV-I 172

If display byte 2 = '00' most likely Set CAR or Sense CAR failed to activate

MICRO
D

CAR picked or dropped bits - random data pattern

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue anlaysis procedure.

Possible Causes

1. A1J4
2. A1C2

DEV-I 172

Display byte 2 = received bus in and Display byte 3 = expected bus in.

MICRO 37

Microdiagnostic

Run microdiagnostic B4 with the following tag sequence.

1. Tag '83' bus out '10' Select CE Drive.
2. Tag '8F' bus out '0A' Drive Sync Tag.
3. Tag '8E' bus out 'XX' Set CAR to value on bus out. XX = desired failing data pattern.
4. Tag '8F' bus out '01' Sense CAR (CAR value is put on bus in)

Load Routine B4, enter:
10, 83, 10, 8F, 0A, 8E, XX, 8F, 01, 00, 00, 00, 00, 00, 00, 00, 00

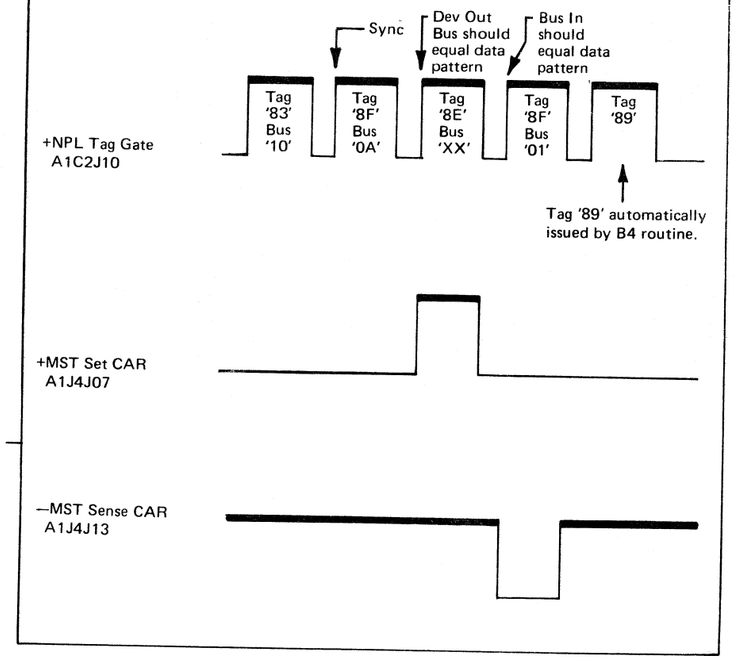
XX = failing data pattern

Scope

Sweep 10 us/div
Trigger
Slope (-)
A1C2G02
–Drive Sync Tag
Ch 1: A1C2J10 (+NPL Tag Gate)
Volts/div 0.5
Probe X10
Ch 2: Use the timing diagram with DEV-I 172. Isolate the problem by scoping CAR control lines and bit lines.

After the trouble is corrected, exit to START 500.

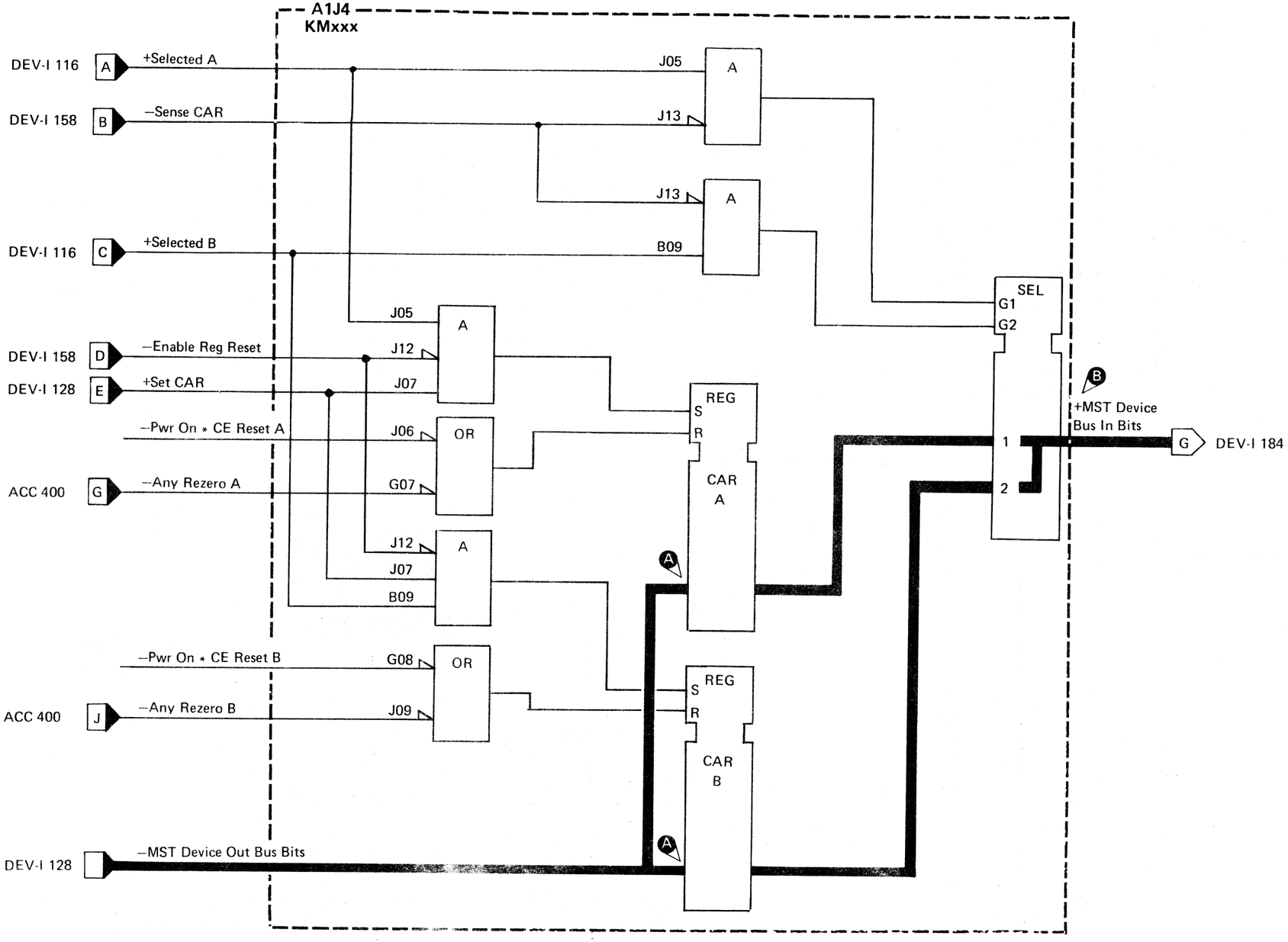
TIMING DIAGRAM



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CYLINDER ADDRESS REGISTER (CAR)

LOC \ BIT	0	1	2	3	4	5	6	7
A	B02	B03	B04	B05	B10	D11	B12	B13
B	G02	G03	G04	G05	G10	G11	G12	G13



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DEVICE BUS IN FAILURE

CTL-I 160 FSI

A

Device Bus In Parity Check

Microdiagnostic

Run Device Checkout Microdiagnostics. Start with routine A1. See MICRO 10 for instructions.

Test fails

No

Possible Causes

A2F2 All drives fail
A2K2 All drives fail
A2G2 All drives fail
A1D2
A1A2 Conn.
A1A3 Conn.
A2V4 Conn.
A1A3 Terminator of last module on string.

Examine history to determine drives involved. Refer to Note 2. Use DEV-I 184, 186 to isolate the trouble.

Yes

Error Analysis

Exit to Error Code in MICRO section. Perform CE action for first error encountered.

MICRO

MICRO

B

Failure to force Device Bus In Parity Check

Possible Causes

A2F2 All drives fail
A2K2 All drives fail

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Microdiagnostic

Loop test 07 and bypass errors:
1. Reload routine A2
2. Enter 10,07,01,00

Scope

Sweep 20 μs/div
Trigger
Slope (–)
A1C1G02
(–Drive Sync Tag)

Ch 1 A1C1J10
(+NPL Tag Gate)
volts/div 0.5
probe X10

Either the Device Bus In Parity Checker or Latch is failing or set diagnostic (Tag '09' Bus Out '20') has failed to invert the Device Bus in 'P' Bit.

Ch 2 Use the scoping procedure on MICFL 160 and the timing diagram for test 07 to determine why Device Bus In parity error is not coming on. Refer to DEV-I 188. Exit to START 500 when problem is corrected.

MICRO

C

Unable to reset Device Bus In Parity Check

Possible Causes

A2F2 All drives fail
A2L2

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Microdiagnostic

Loop test 07 and bypass errors:
1. Reload routine A2
2. Enter 10,07,01,00

Device Bus In Parity latch is reset by + Gen Reset (A2F2M11).

Scope

Use DEV-I 188 to determine why the Device Bus In Parity latch does not reset. Sync on A1C1M11, KA100 (+Sense Interface) (Tag '89'). See note 1.

Repair or replace as required. Exit to START 500 when problem is corrected.

Load routine B4. Enter: 10, 83, 10,8F,0A, 8B, XX, 8F, 05, 00, 00, 00, 00, 00, 00, 00, 00. XX = Failing Data Pattern

MICRO

D

Device Bus In Parity Check. Suspect P bit.

No, or do not know

All drive modules in string fail

No

Yes, do not know, or only module in string.

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Possible Causes

A2F2
A1D2
A2K2
Short in Device Bus In cabling or terminator.
A1C2

Refer to Note 1 and isolate the failure to a drive module. See cabling diagram on DEV-I 305.

MICRO 37

Microdiagnostic

Run routine B4 and enter the following drive tag sequence:
1. Tag '83' Bus Out '10' Select CE Drive
2. Tag '8F' Bus Out '0A' Drive Sync Tag
3. Tag '8B' Bus Out 'XX' Set HAR to Value on Bus Out XX = the desired failing data pattern.
4. Tag '8F' Bus Out '05' Sense HAR (HAR Value is put on Device Bus In)

The Device Bus In Parity Indicator comes on when this tag sequence is executed and a failing data pattern was entered in Step 3.

DEV-I 182

E

Bit(s) dropped

Yes

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Possible Causes

A1D2 In failing module if only one module is failing
A1C2 Device Bus In cabling or terminator (Note 2). See cabling diagram on DEV-I 305.

DEV-I 132
DEV-I 133

Scope

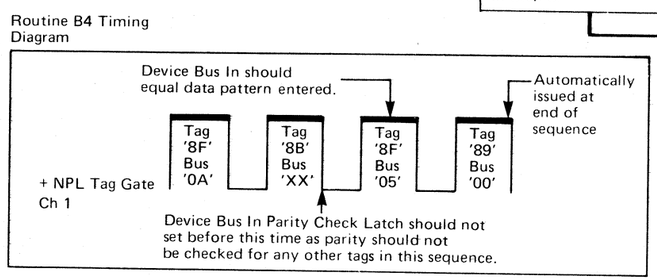
Sweep 20 μs/div
Trigger
Slope (–)
A1C2G02 - Drive Sync Tag

Ch 1 A1C2J10+NPL Tag Gate
volts/div 0.5
probe X10

Ch 2 Use the timing diagram on this page and scope Device Bus In and the Device Bus In Parity Check Latch to determine the reason for the error;

Refer to DEV-I 184 and 186. Exit to START 500 when problem is corrected.

Routine B4 Timing Diagram

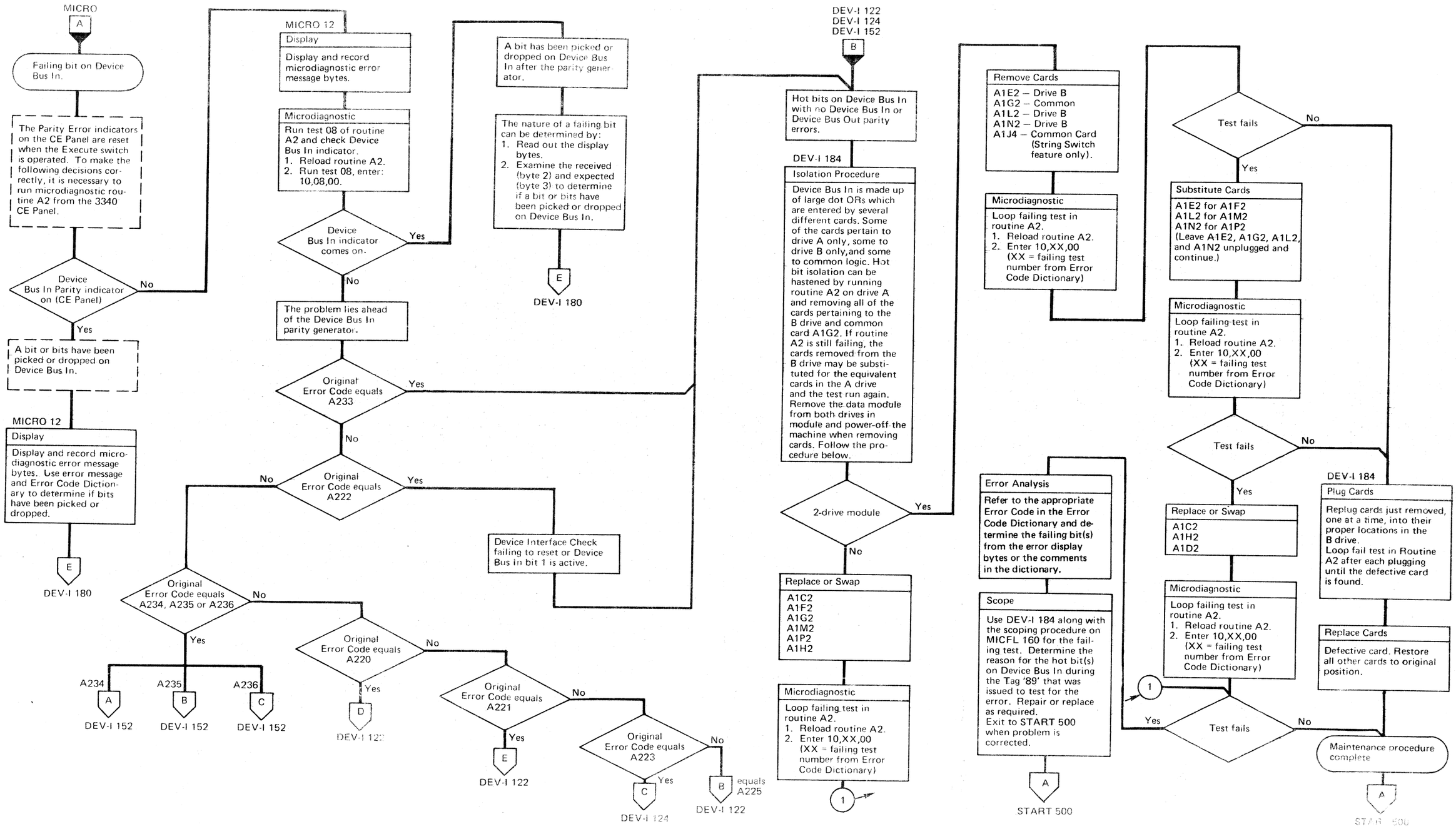


Note 1: The Device Bus In Bit Lines from each drive module are dot ORed together on the device interface. A hot bit on the interface causes all drives to fail; a dropped bit causes one or more modules to fail. To isolate the failure to a module it is necessary to disconnect device interface connectors A1A3, A1A4 in appropriate modules, insert terminator card A1A3 from last module in the string, and then run microdiagnostic A2 on one of the drives in the control module. See cabling diagram on DEV-I 305.

Note 2: An open terminator (A1A3-last module) does not necessarily cause a failure. The terminator card is a double card and should be located in positions A3 and A4 of the last module in the string.

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DEVICE BUS IN FAILURE

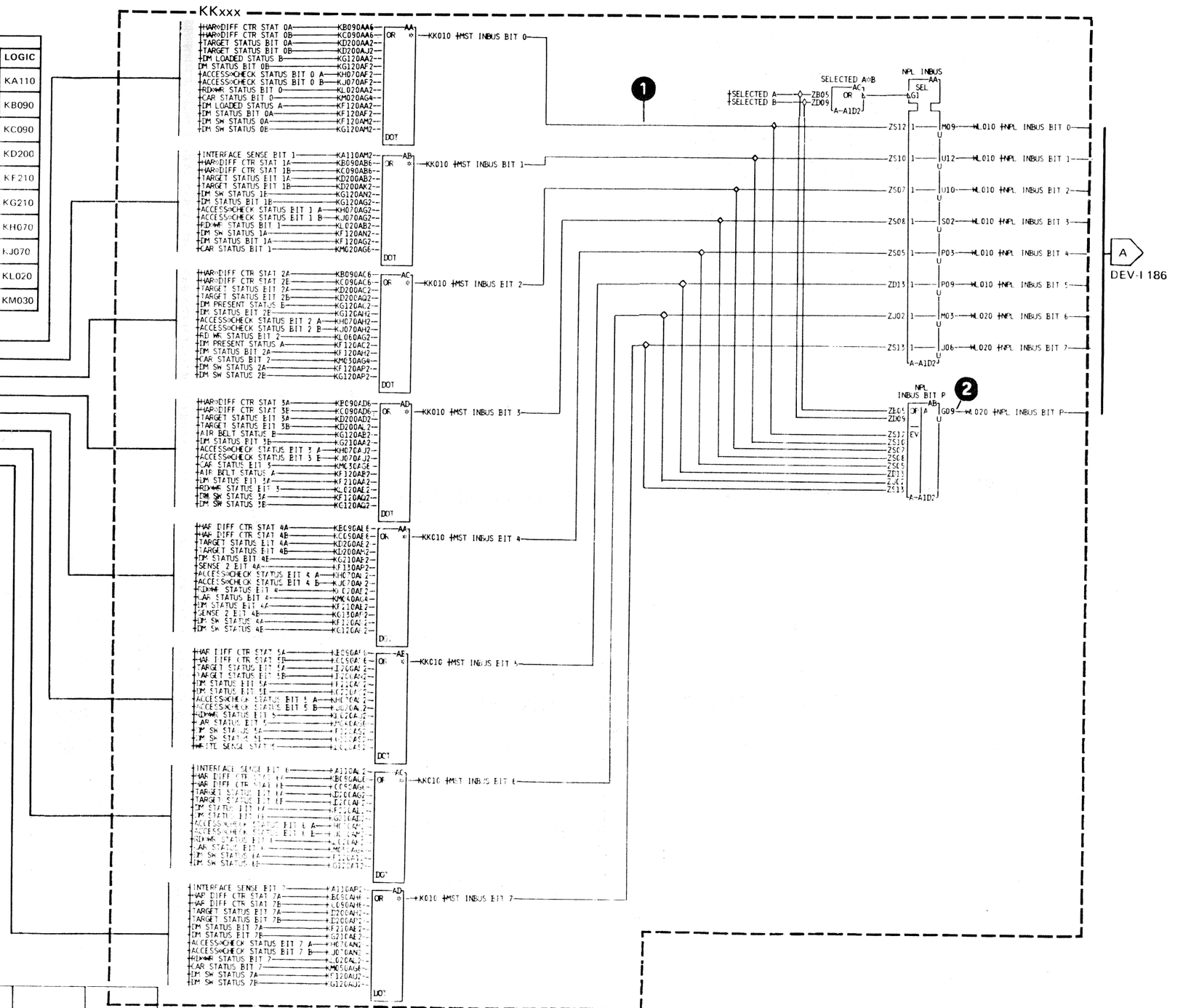


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DEVICE BUS IN ASSEMBLER

See DEV-I 300 for overview.

	LINE NAME	CARD	BITS 7	6	5	4	3	2	1	0	LOGIC
A DEV-I 126	+ INTF SENSE BITS A&B DRIVES	A1C2	S11	M08					P05		KA110
	+ HAR•DIFF CNT STAT BITS A DRIVE	A1F2	M11	S07	U07	U04	U05	P11	M09	P09	KB090
B DEV-I 156	+ HAR•DIFF CNT STAT BITS B DRIVE	A1E2	M11	S07	U07	U04	U05	P11	M09	P09	KC090
	+ TARGET STATUS BITS A&B DRIVES	A1G2	J11	G11	G05	G07	D10	D07	B10	B07	KD200
	+ DM STATUS BITS A DRIVE	A1M2	P12	D09	J03	B12	B04	B02	D02	B05	KF210
	+ DM STATUS BITS B DRIVE	A1L2	P12	D09	J03	B12	B04	B02	D02	B05	KG210
	+ ACCESS•CHECK STAT BITS A DRIVE	A1P2	D02	B04	B05	B02	B07	D10	B10	D07	KH070
	+ ACCESS•CHECK STAT BITS B DRIVE	A1N2	D02	B04	B05	B02	B07	D10	B10	D07	KJ070
	+ RD•WR STATUS BITS A&B DRIVES	A1H2	P07	S07	U07	S11	U06	J07	S13	U13	KL020
G DEV-I 172	+ CAR STATUS BITS A&B DRIVES	A1J4	G13	G12	G11	G10	G05	G04	G03	G02	KM030



Device Bus In parity is generated in each device attachment at the drives on the A1D2 card ❷ and is checked in the controller on the A2F2 card.

A parity error is gated on the A2K2 card to controller Bus In Bit 3 with Controller Error One (Tag '04', Bus Out '01').

Good parity is continually generated for a selected drive but is only checked for the following device tags:

1. Tag '8F' Bus Out '01' (not used)
2. Tag '8F' Bus Out '05' (Sense HAR)
3. Tag '8F' Bus Out '09' (Sense Difference Counter)
4. Tag '8F' Bus Out '0D' (Sense Target)

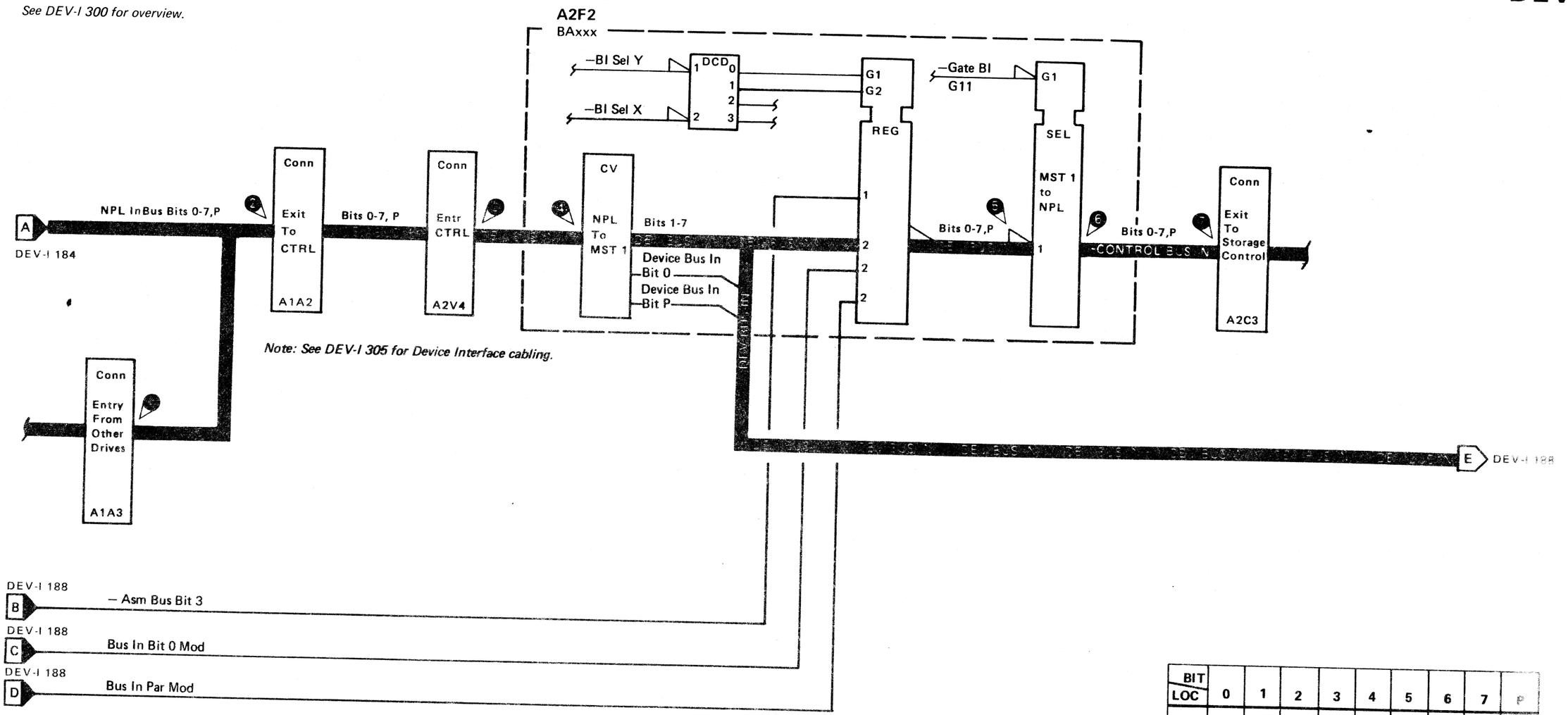
If a bit is picked or dropped in a device attachment ahead of the Device Bus In drivers, Device Bus in Parity Check does not occur. ❶

Device Bus in Parity Check is reset by General Reset (Tag '09' Bus Out '80'), but the indicator latch is not reset until the execute switch is operated.

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DEVICE BUS IN FAILURE

See DEV-I 300 for overview.

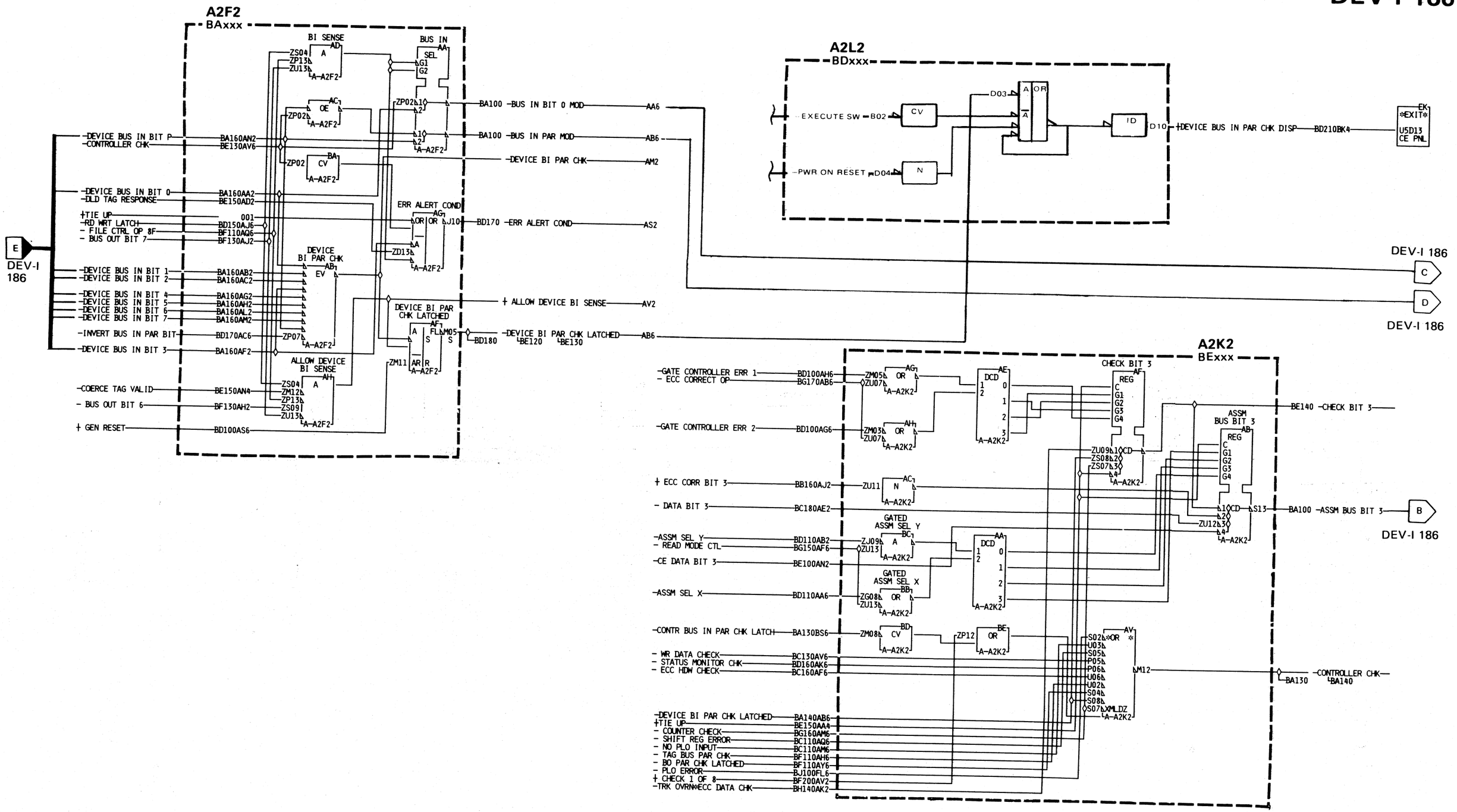


Note: See DEV-I 305 for Device Interface cabling.

BIT / LOC	0	1	2	3	4	5	6	7	P
1	B02	B04	B05	B06	B08	B09	B10	B12	B13
2	B02	B04	B05	B06	B08	B09	B10	B12	B13
3	B02	B04	B05	B06	B08	B09	B10	B12	B13
4	B10	B07	G03	B09	G12	J04	G05	G13	J13
5	P05	M10	M08	S07	P06	U03	P09	U06	U04
6	D06	B03	D10	D09	J02	J07	J11	J03	J12
7	D05	B05	D06	B08	D09	B10	D11	B12	B02

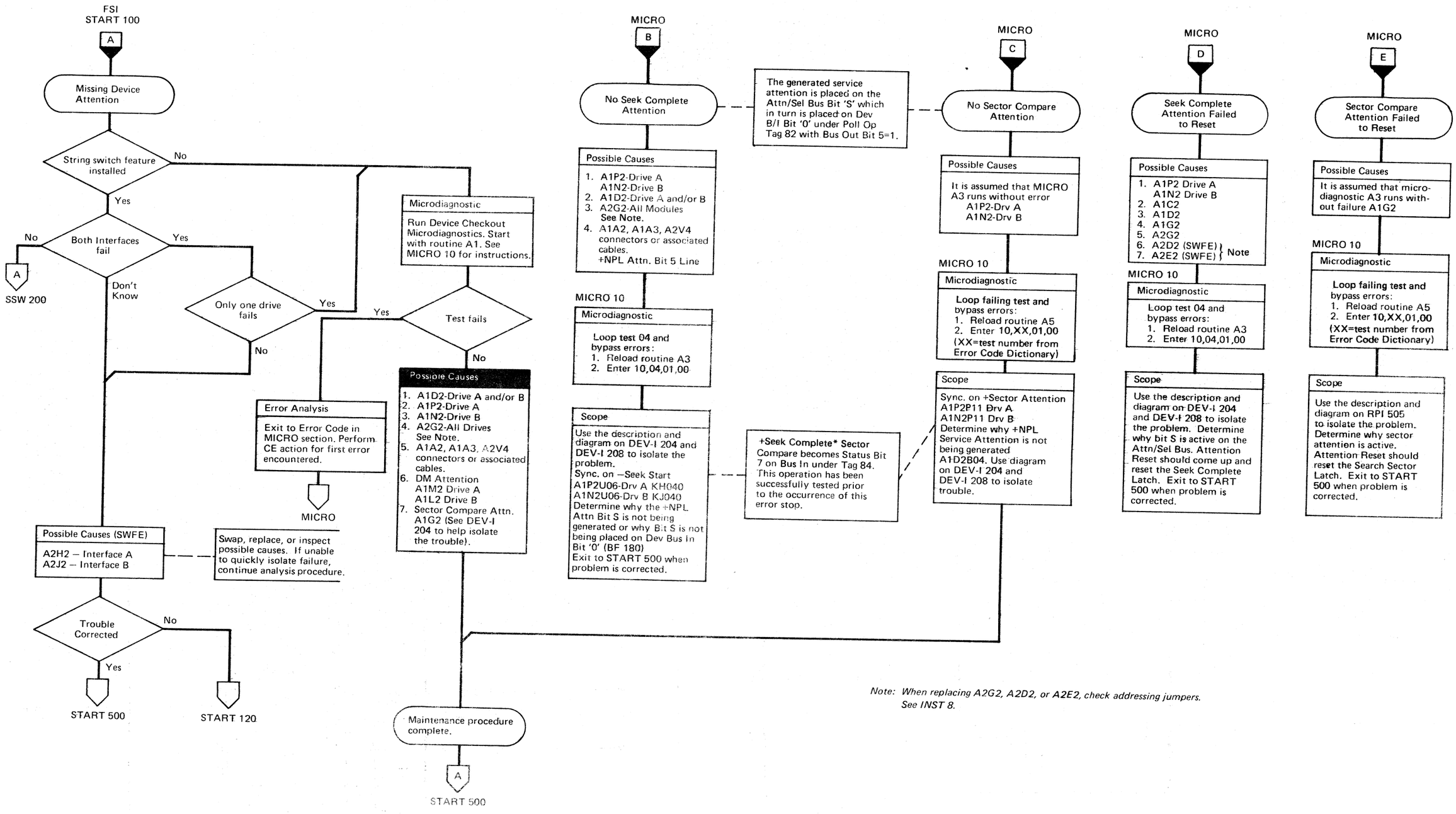
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DEVICE BUS IN FAILURE



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MISSING ATTENTION



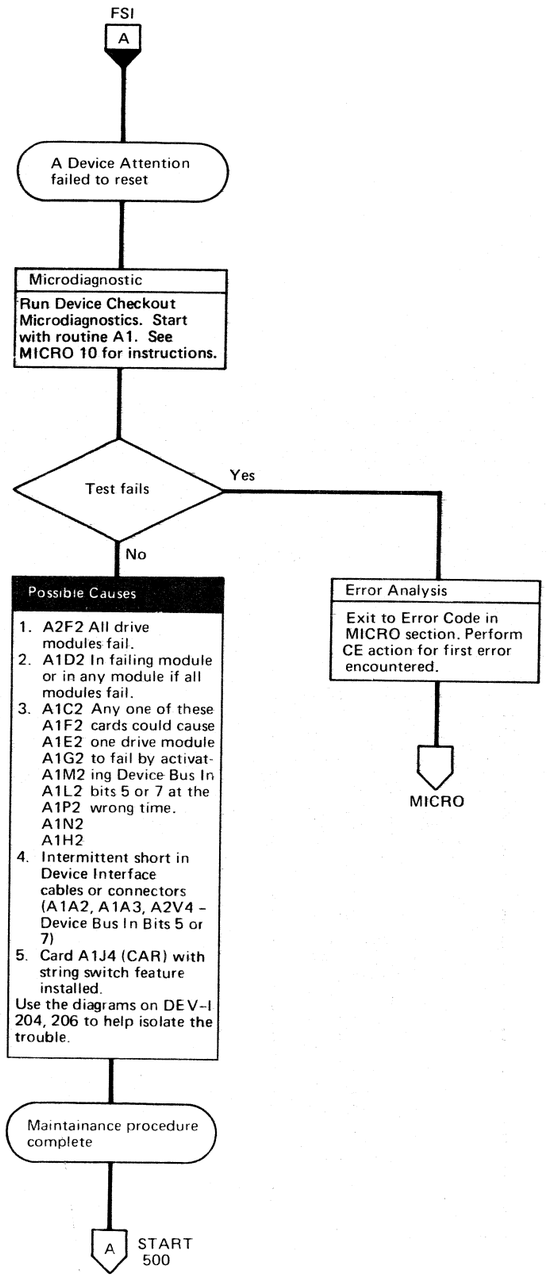
Note: When replacing A2G2, A2D2, or A2E2, check addressing jumpers. See INST 8.

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ATTENTION CHECK

The Attention Check error is caused by Bus In bits 5 or 7 being active during a Request Drive Status operation (Tag '84') after a Device Attention has been serviced and reset by Attention Reset. (Tag '8F' Bus Out '04').

Refer to OPER 104 for description of Tag '84' and OPER 105 for description of Tag '8F'.



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DEVICE ATTENTION

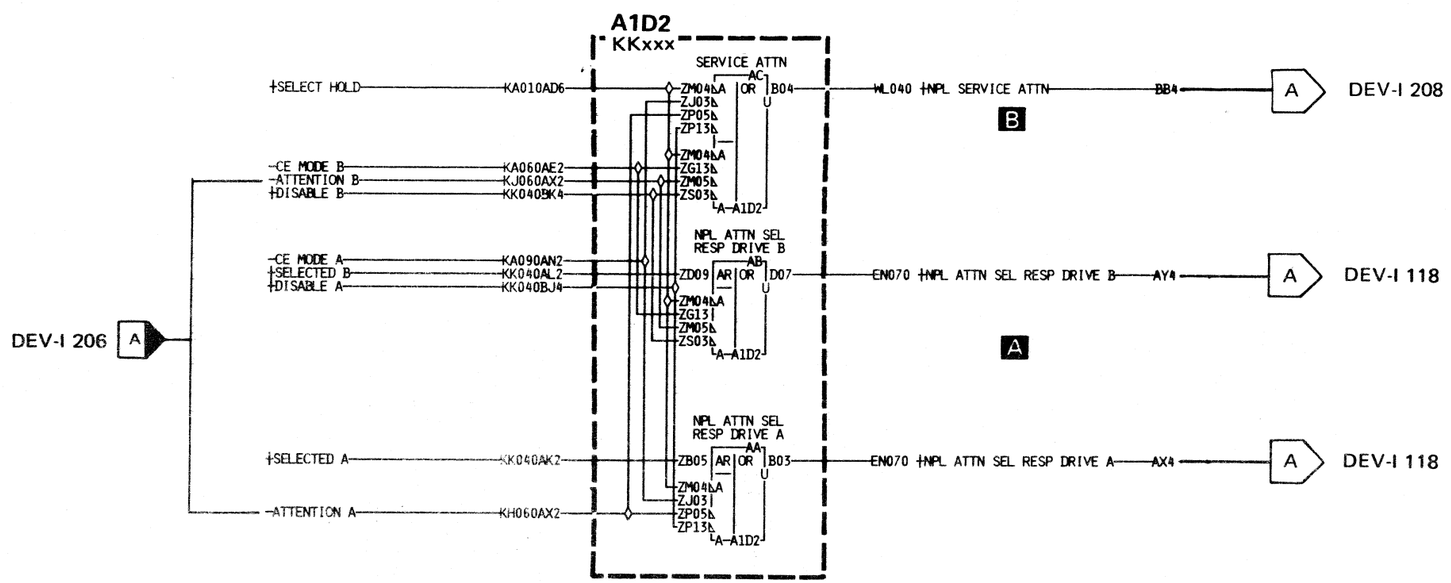
Attention A

1. A drive presents an attention by placing its unique physical address on the Attn/Sel bus.
   a. The +NPL Attn/Sel Response lines from each drive are wired to the Attention/Select bus. The bus is rotated as it passes through each module. This allows each drive to present its own unique physical address bit when it is selected or when it had an Attention to present. See DEV-I 307.
2. When Storage Control polls the Controller (Tag '82' with Bus Out bits 0, 1, and 2 equal to the Controller address), the Attn/Sel bus is gated to Bus In and good parity generated.

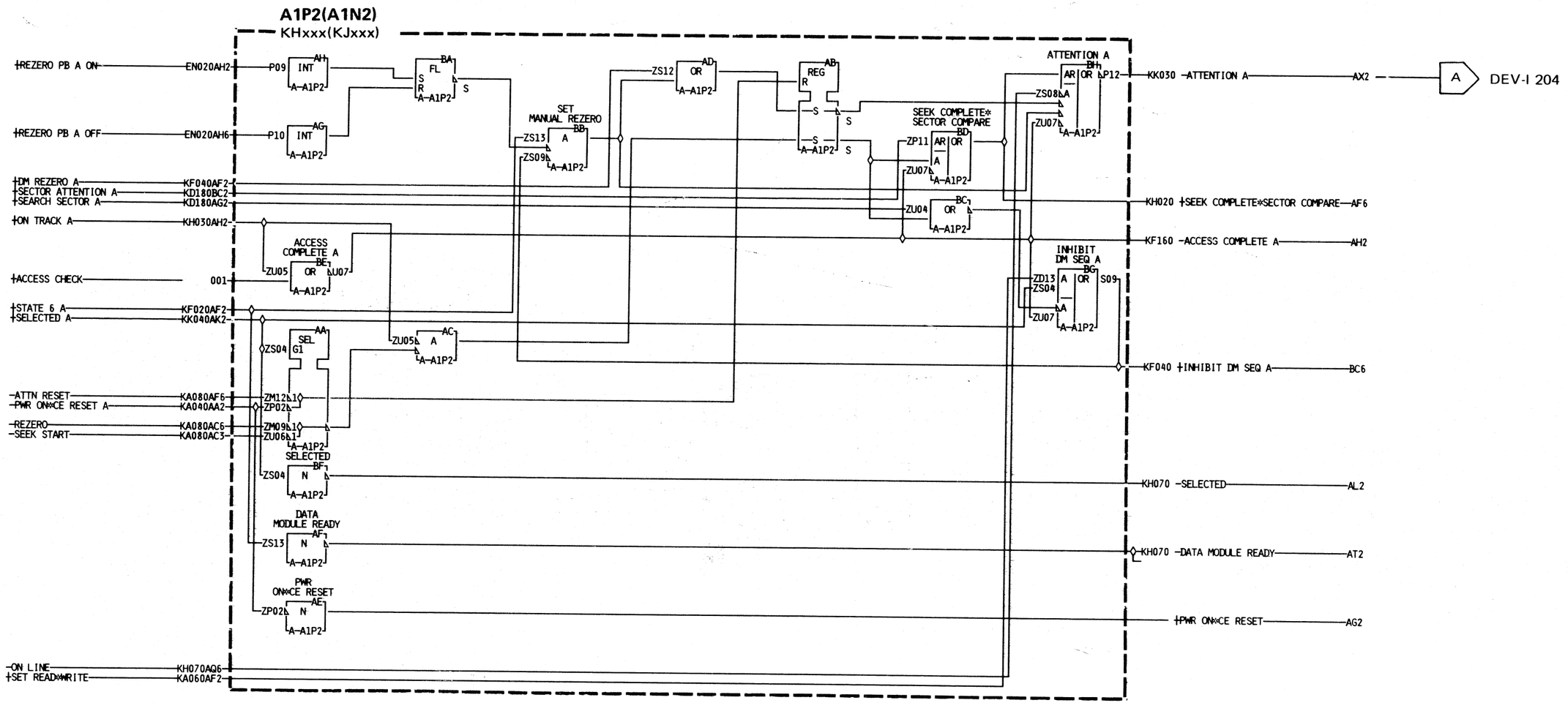
Refer to OPER 104 for description of Tag '82'.

Service Attention B

1. A Service Attention is presented instead of a normal Attention when the drive is in CE Mode. The Service Attention is placed on Attn/Sel bus bit 'S' (DEV-I 208).
2. When Storage Control polls the Controller for a Service Attention (Tag '82' with Bus Out bits 0, 1, and 2 equal to the Controller address and bit 5 on), the Attn/Sel bus bit 'S' is gated to Bus In Bit '0'.



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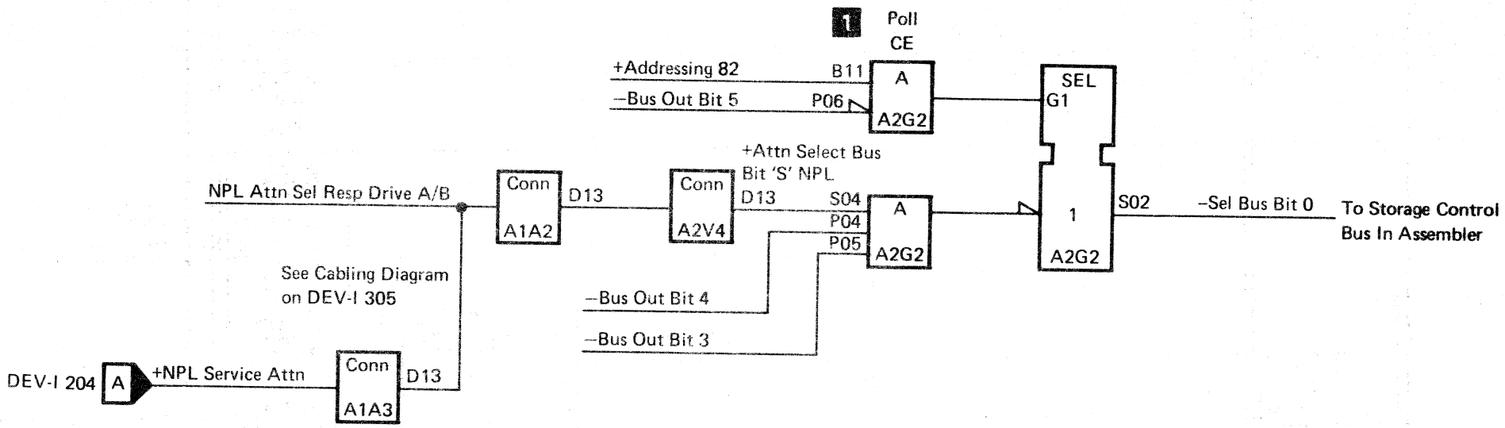


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SERVICE ATTENTION (BITS)

A Poll CE Tag 1 (Tag '82', Bus Out 'X4'), gates a Service Attention (Bit S) from the drive in CE Mode to Select Bus Bit 0. Select Bus Bit 0 is gated to Bus In Bit 0.

Refer to OPER 104 for description of Tag '82'.

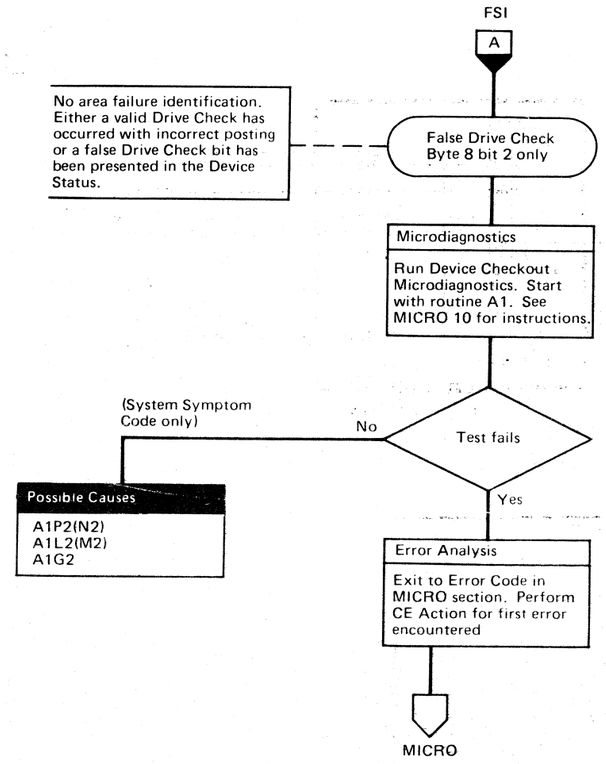


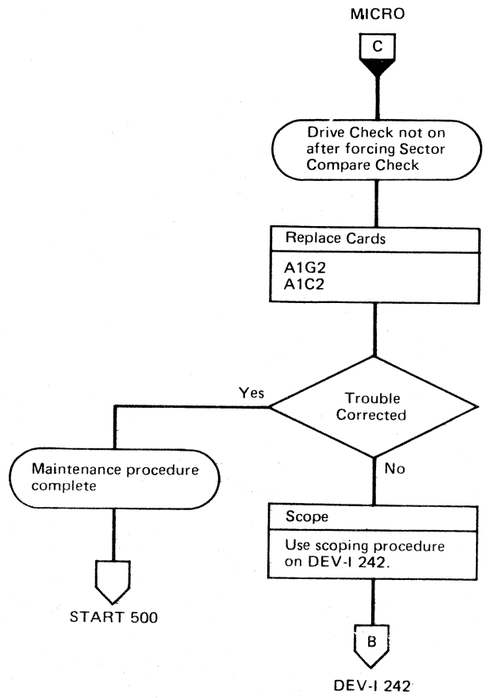
DB0253	2747702
Seq. 2 of 2	Part No. ( )

440203	440209	440218				
2 Nov 73	25 Mar 74	5 Aug 74				

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DRIVE CHECK





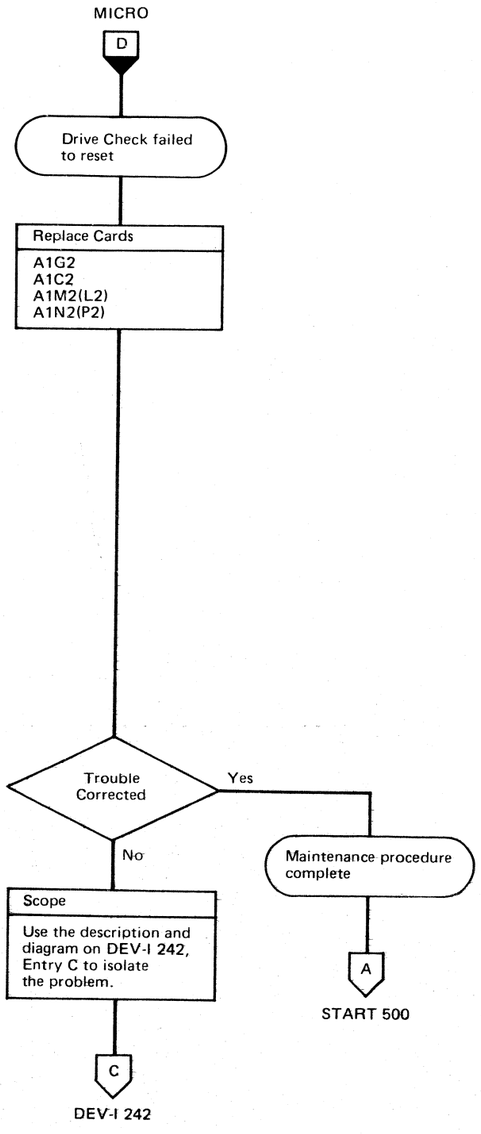
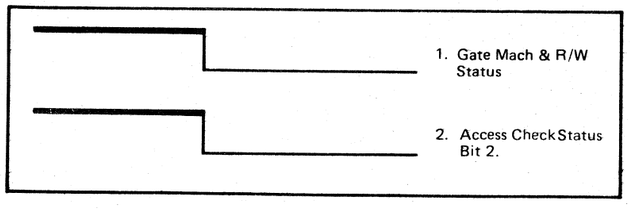
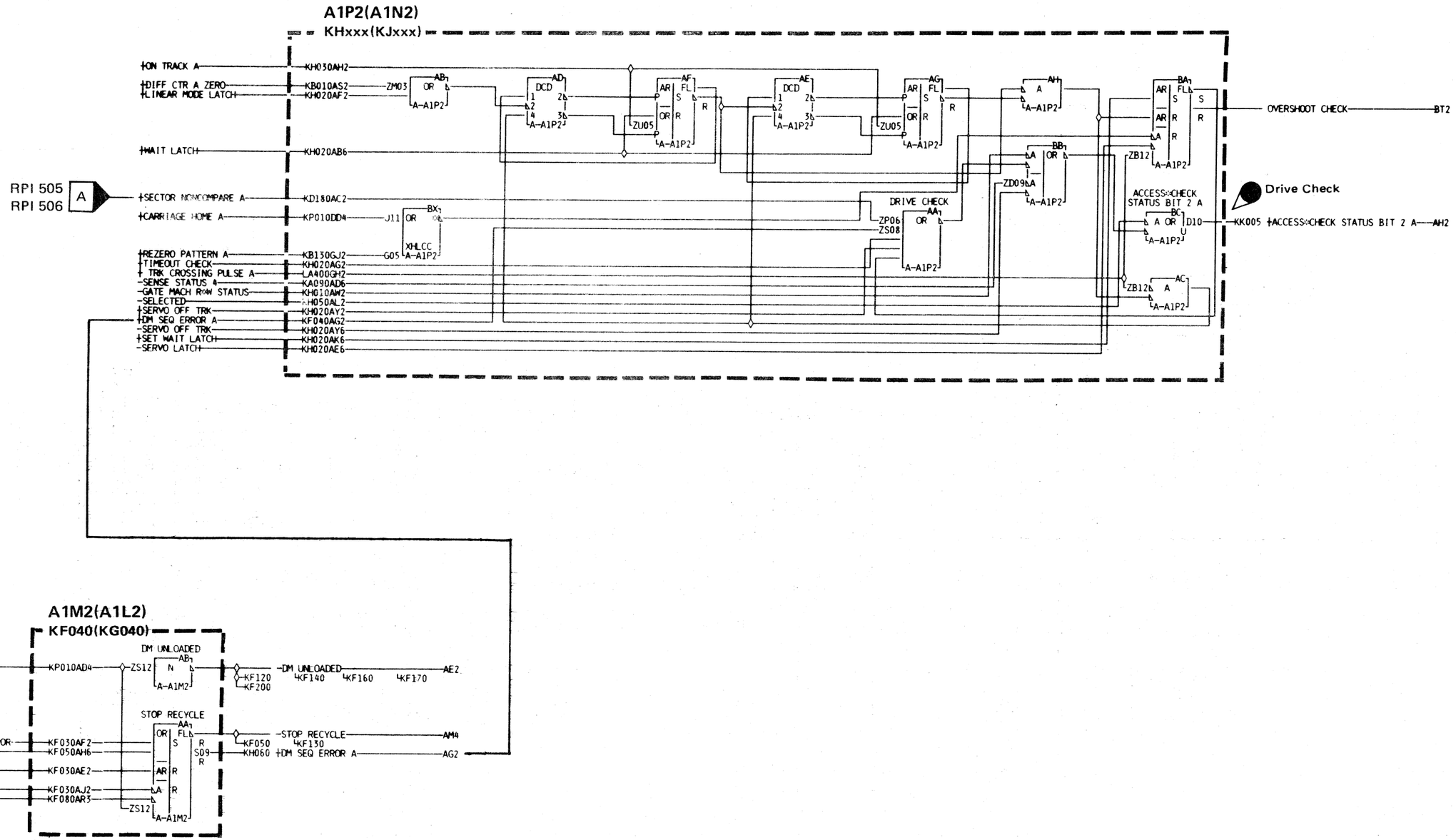


Fig. 1



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DRIVE CHECK

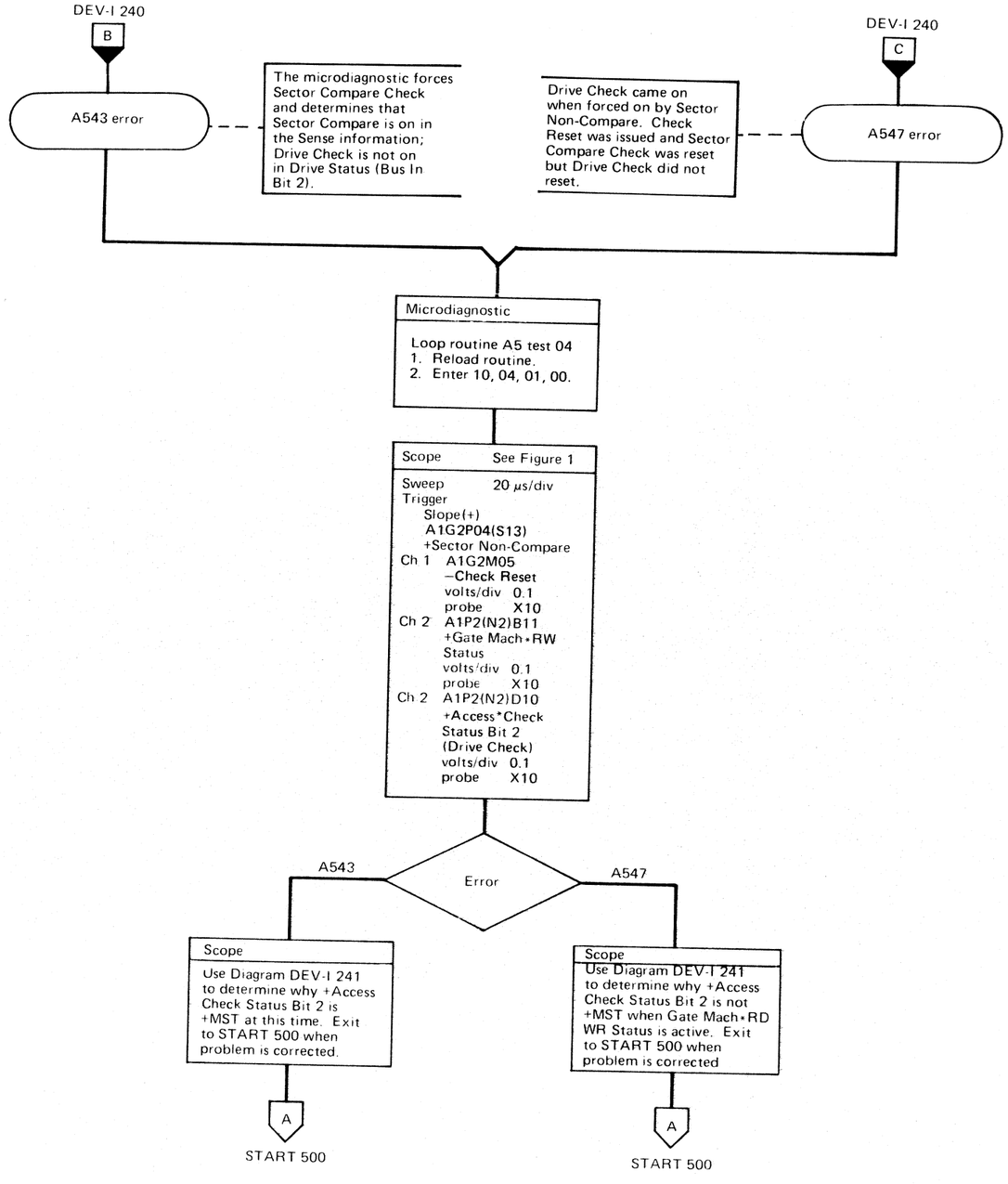
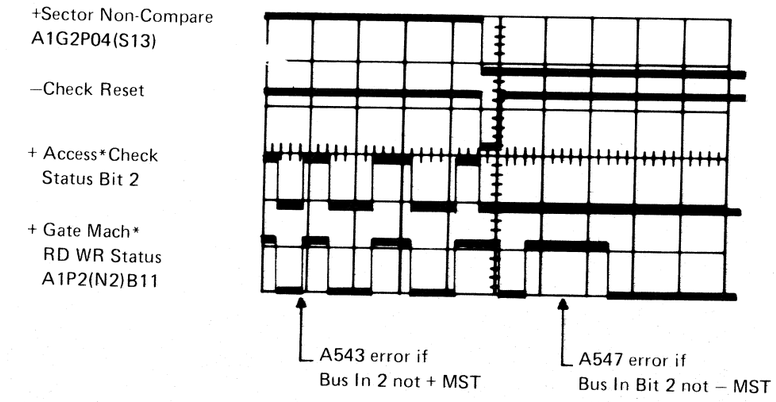
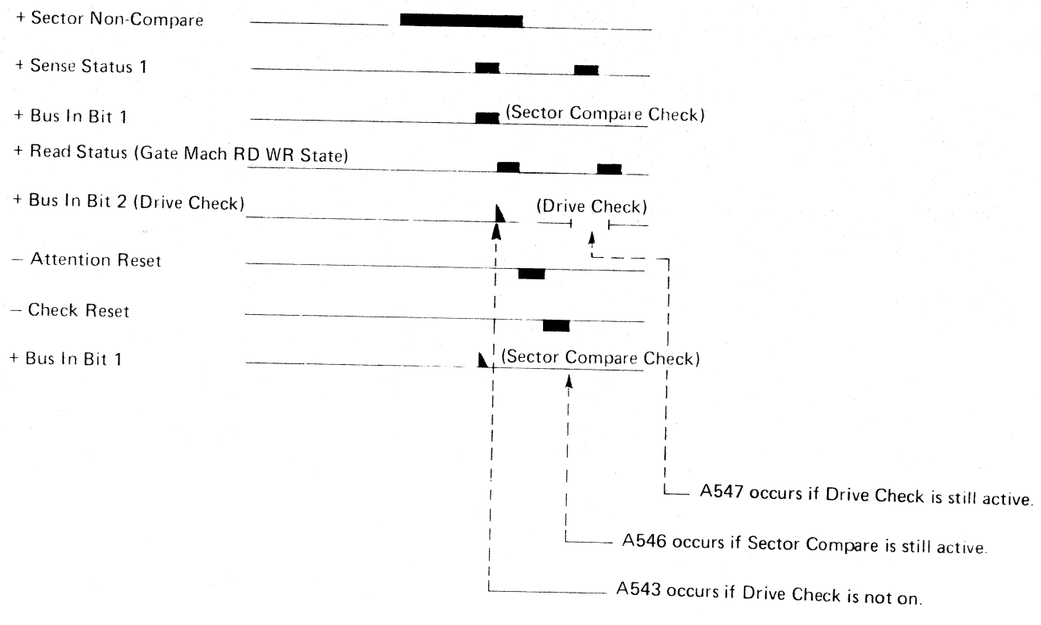


Figure 1



Timing Chart



DB0290 Seq. 1 of 1	2747154 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440214 17 Jun 74	

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INTERVENTION REQUIRED/NOT ONLINE

ONLINE

When the drive is selected, sense byte 8 bit 4 in the drive status indicates the drive is online.

Initial Online is established if during the DM Load operation, DM Ready State 6 is reached and the initial rezero in the load sequence was successful (Access Ready).

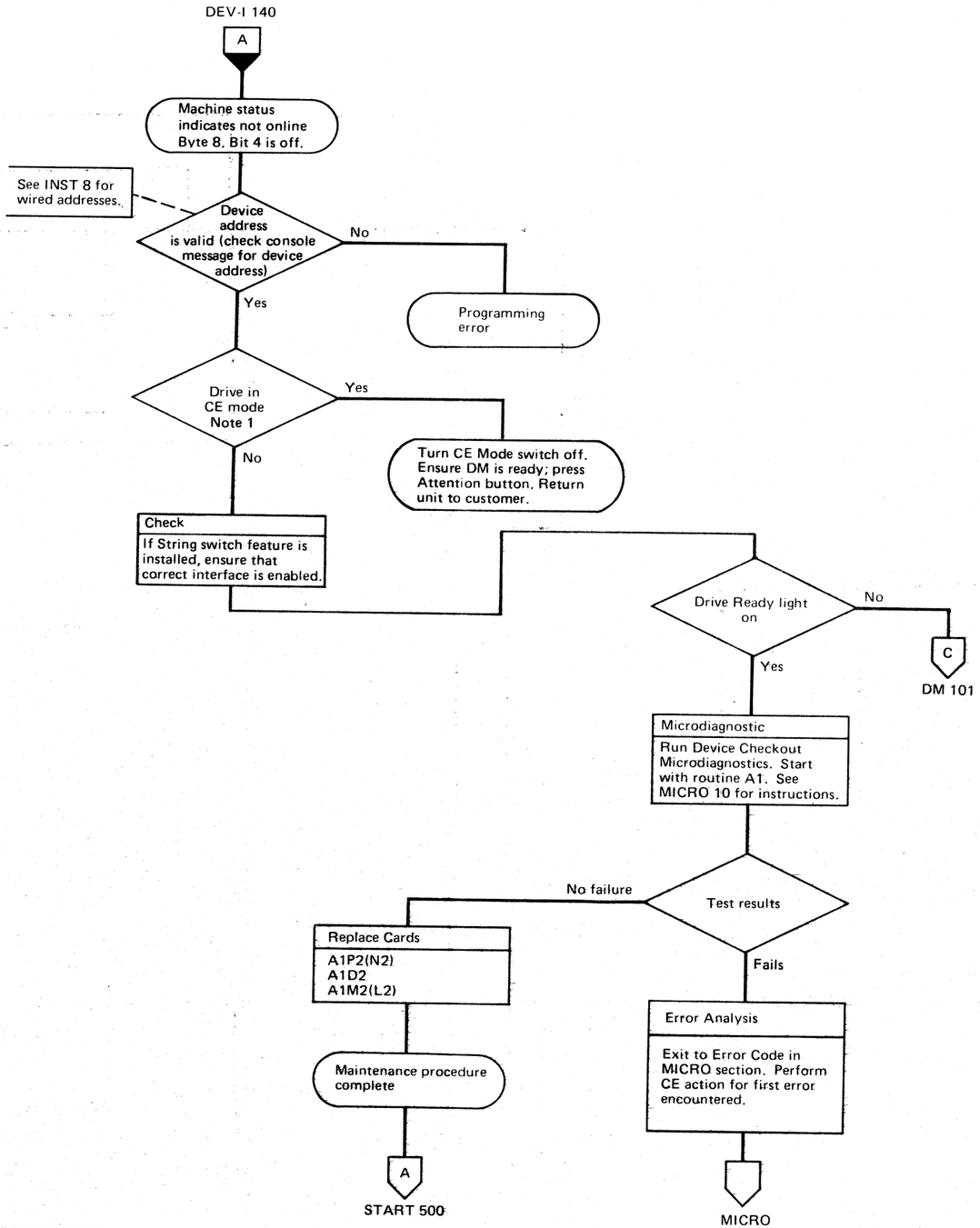
Online status is reset if:

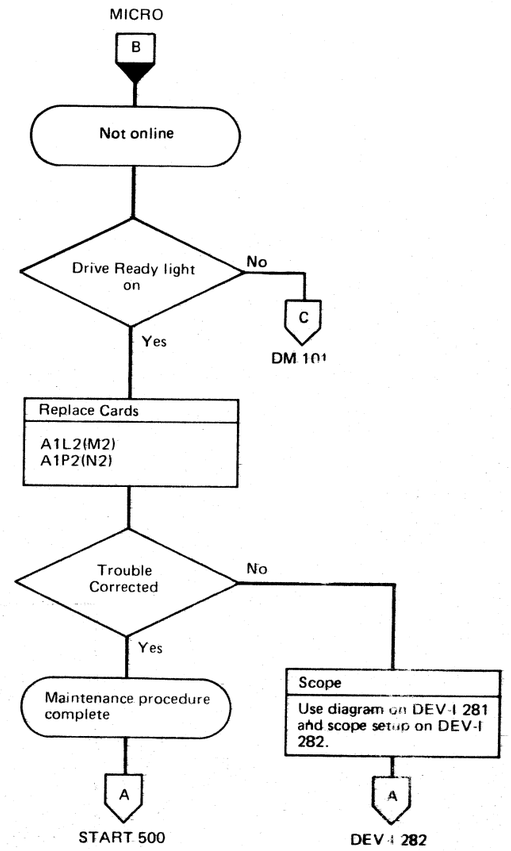
1. The drive Start/Stop switch is turned to Stop.
2. A DM Interlock error occurs after Ready State 6 is reached, which unloads the data module.

A DM Interlock error is caused by:

1. Loss of Air Belt.
2. Loss of Motor-at-Speed.
3. Loss of DM Loaded switch.
4. DM size check.

Note 1: To determine if the CE Mode Latch is on or does not reset, check:
–CE Mode A A1C2S12 (KA090)
–CE Mode B A1C2U11 (KA060)

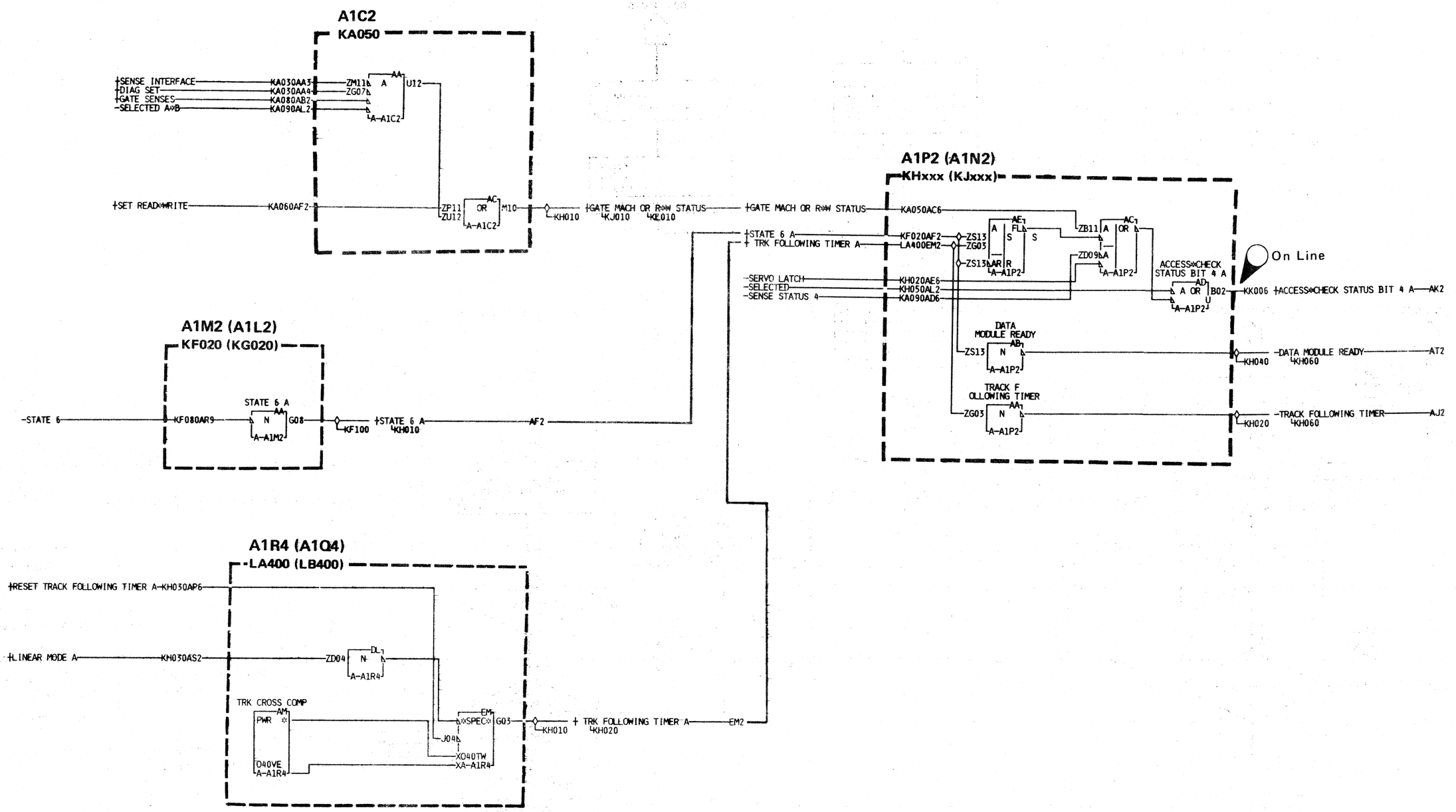




DB0293 Seq. 1 of 2	2747155 Part No. ( )

440200 25 Jun 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440223 14 Mar 75		

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INTERVENTION REQUIRED/NOT ONLINE

DEV-I 280

A

The drive Ready light is on which indicates the Data Module Sequencer is at State 6 and the servo is track following.

MICRO 37

Microdiagnostic

Run routine B4
Enter: 10, 83, 10, 84, 10, 00, 00, 00, 00, 00, 00, 00, 00, 00, 00, 00.

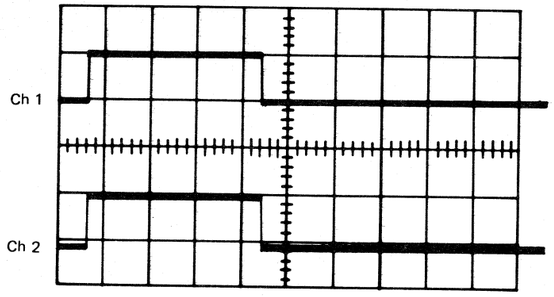
Read Status command activates +Gate Mach or R*W Status.

Scope

Sweep 5 μs/div
Trigger
Slope +
Ck 1 only
Ch 1 A1C2M10
+Gate Mach or R*W Status
volts/div 0.05
probe X10

Ch 2 A1P2(N2)B02
+Access Check Status
Bit 4 (this is Bus In 4 an online bit).
volts/div 0.05
probe X10

If Bit 4 is not +MST, probe A1P2(N2)S13 + State 6 and A1P2(N2)G03 +Trk Following Timer. These levels should be +MST. Use DEV-I 281 to isolate the problem. Exit to START 500 when problem is corrected.



A

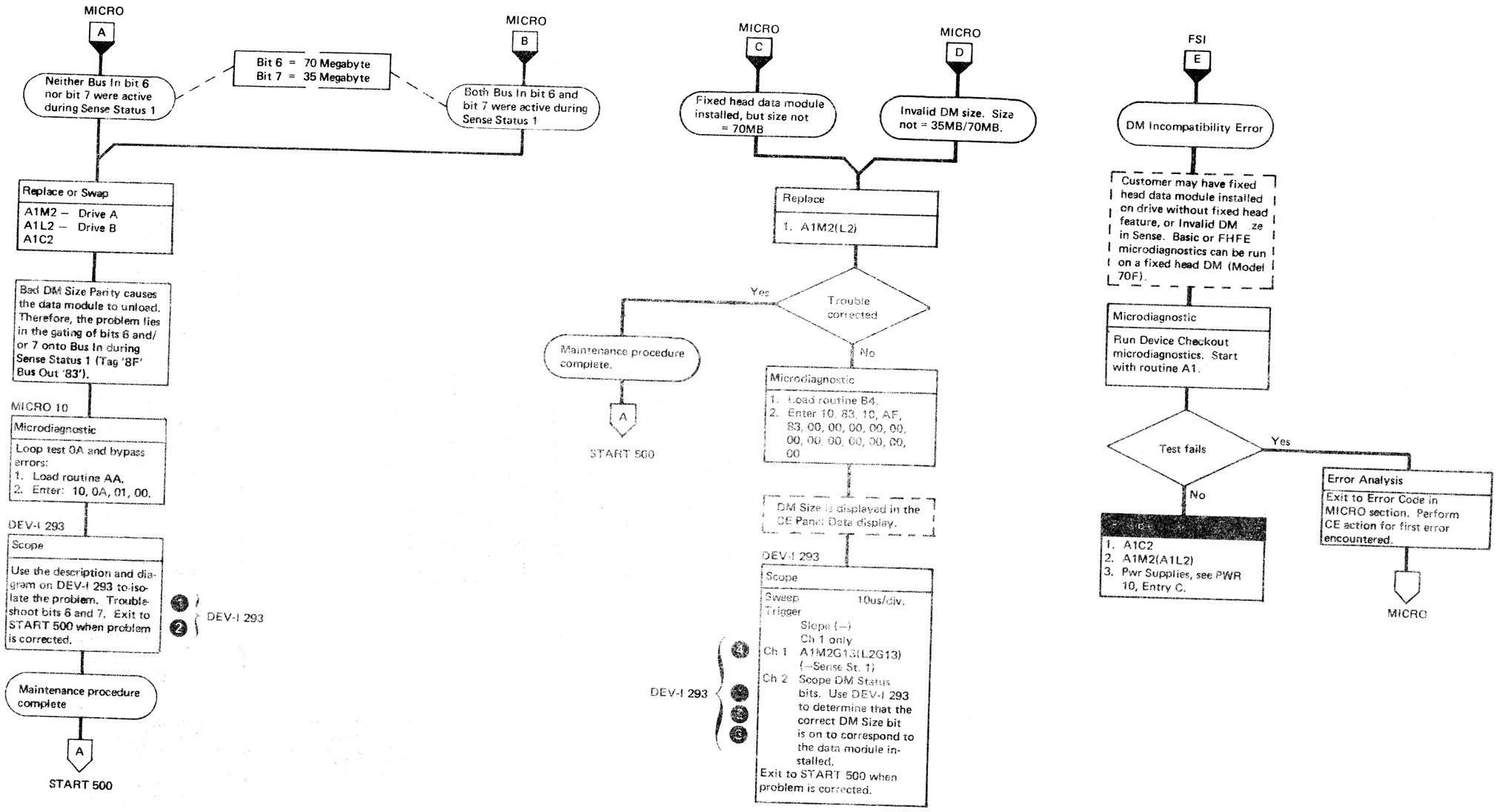
START 500

DB0298 Seq. 1 of 2	2747703 Part No. ( )

440203 2 Nov 73	440209 25 Mar 74	440214 17 Jun 74	440218 5 Aug 74	440223 14 Mar 75		

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DATA MODULE SIZE BIT FAILURE



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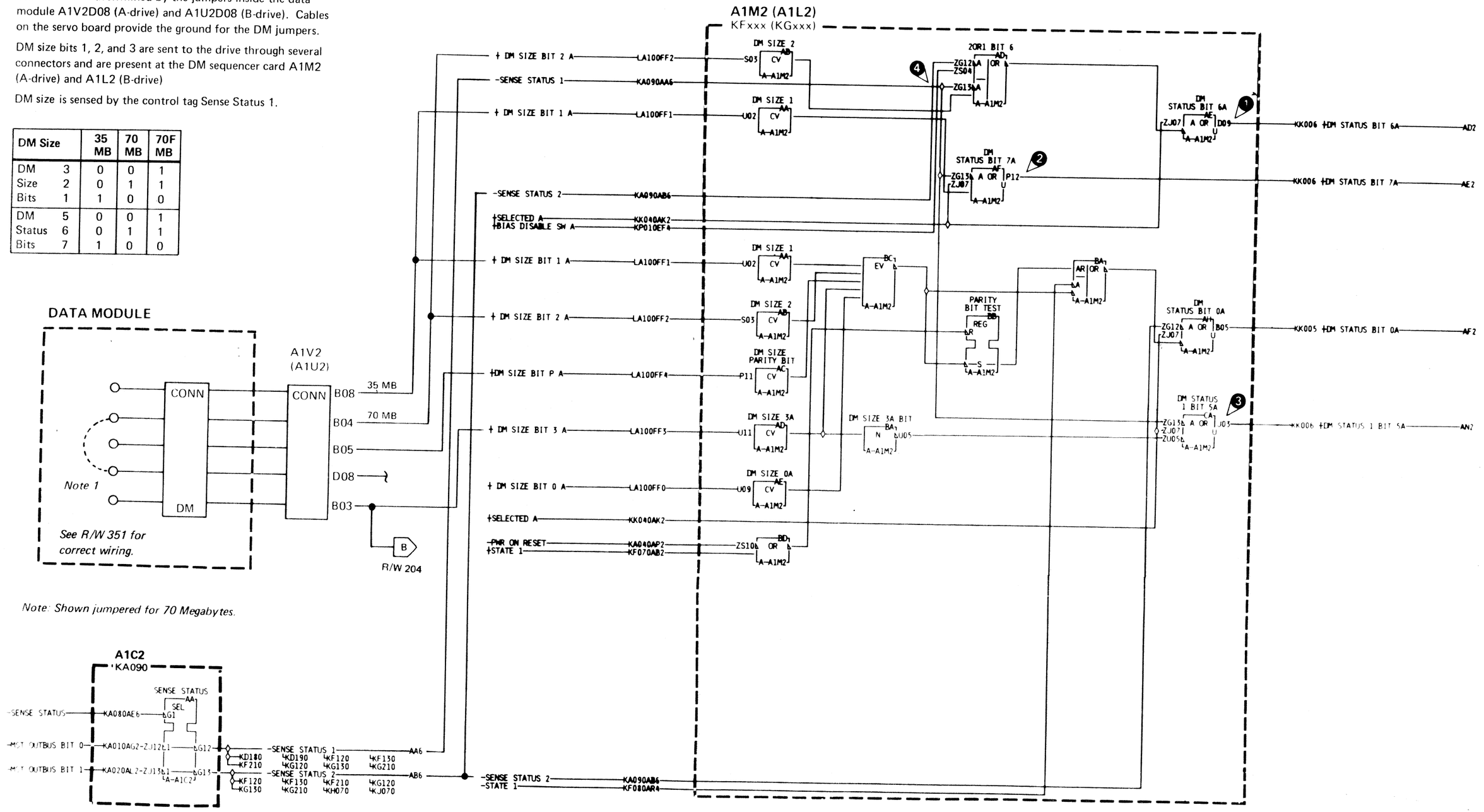
DATA MODULE SIZE

The DM size is determined by the jumpers inside the data module A1V2D08 (A-drive) and A1U2D08 (B-drive). Cables on the servo board provide the ground for the DM jumpers.

DM size bits 1, 2, and 3 are sent to the drive through several connectors and are present at the DM sequencer card A1M2 (A-drive) and A1L2 (B-drive)

DM size is sensed by the control tag Sense Status 1.

DM Size		35 MB	70 MB	70F MB
DM Size Bits	3	0	0	1
	2	0	1	1
	1	1	0	0
DM Status Bits	5	0	0	1
	6	0	1	1
	7	1	0	0



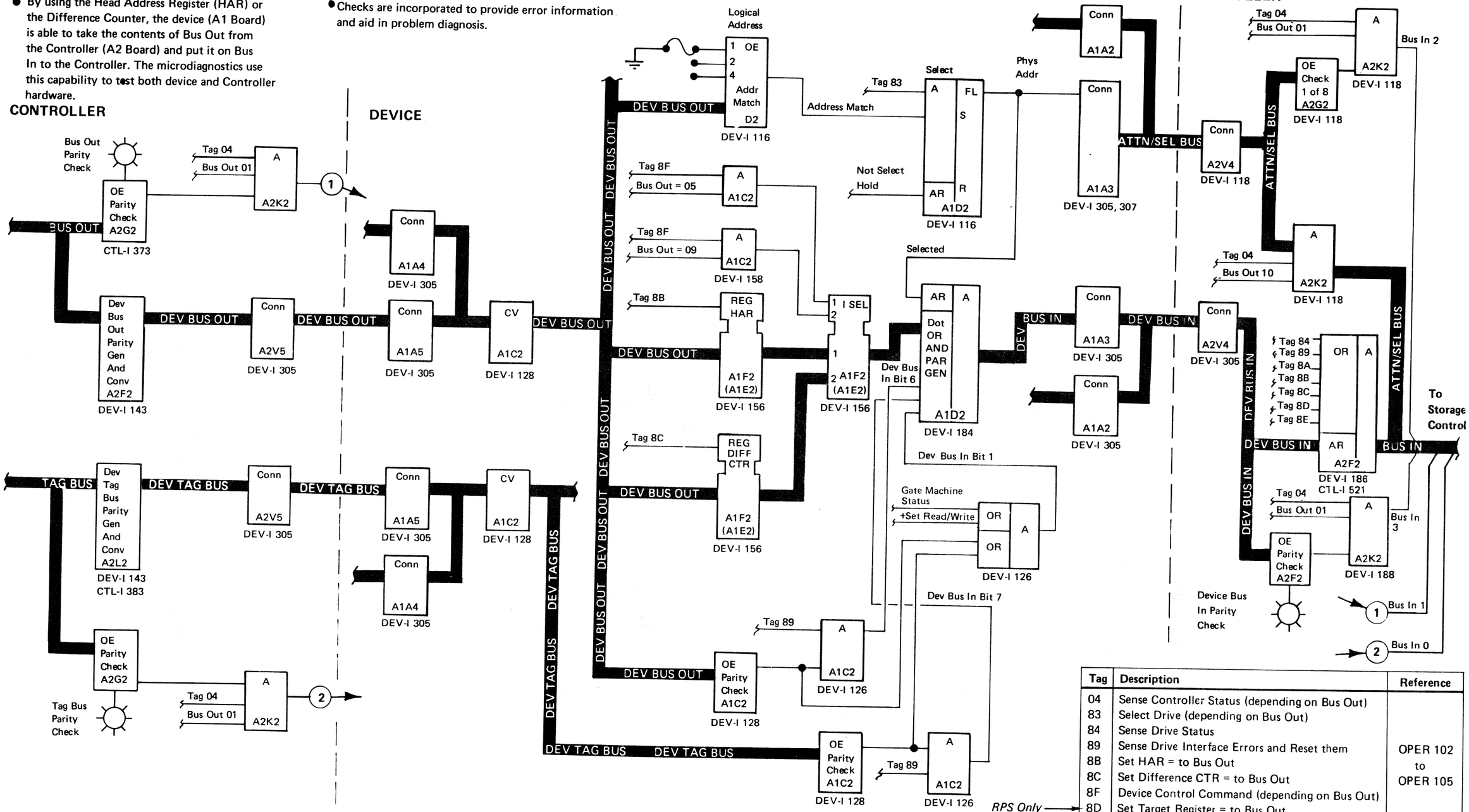
Note: Shown jumpered for 70 Megabytes.

DB0300	2747823	440209	440214	440218				
Seq. 1 of 1	Part No. ( )	25 Mar 74	17 Jun 74	5 Aug 74				

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DEVICE INTERFACE DATA FLOW AND ERROR DETECTION

- By using the Head Address Register (HAR) or the Difference Counter, the device (A1 Board) is able to take the contents of Bus Out from the Controller (A2 Board) and put it on Bus In to the Controller. The microdiagnostics use this capability to test both device and Controller hardware.
- Checks are incorporated to provide error information and aid in problem diagnosis.

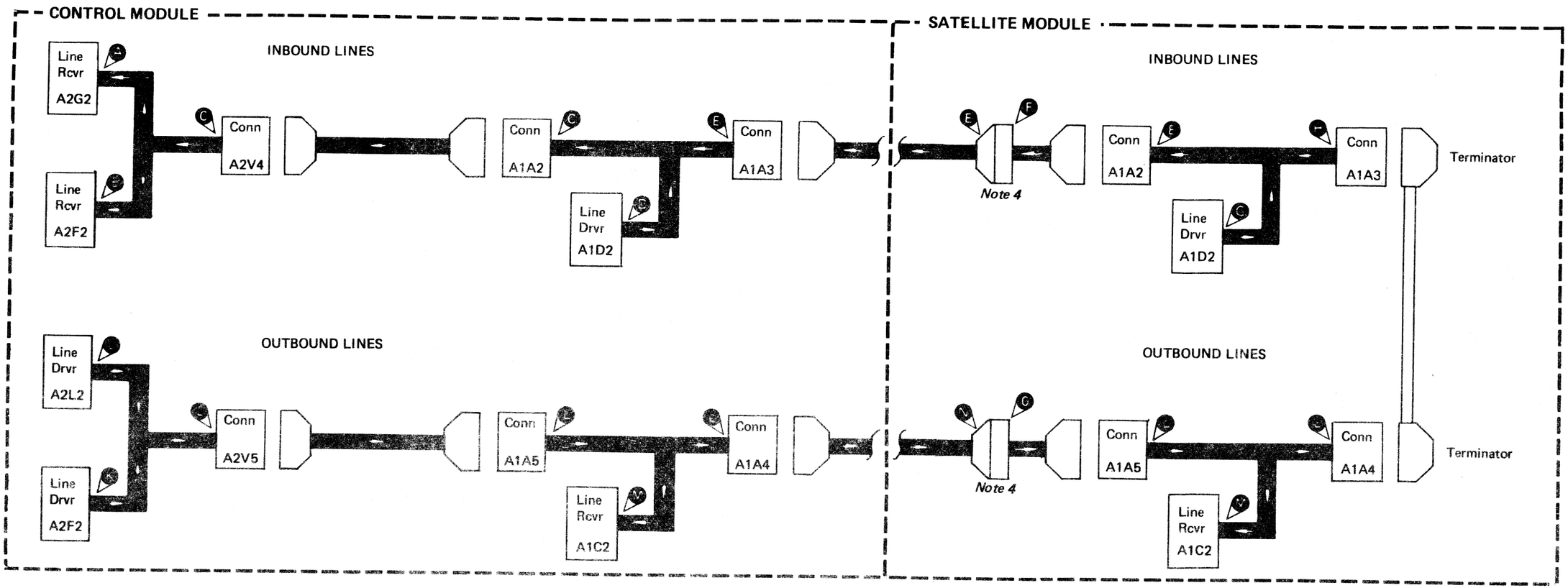


Tag	Description	Reference
04	Sense Controller Status (depending on Bus Out)	OPER 102 to OPER 105
83	Select Drive (depending on Bus Out)	
84	Sense Drive Status	
89	Sense Drive Interface Errors and Reset them	
8B	Set HAR = to Bus Out	
8C	Set Difference CTR = to Bus Out	
8F	Device Control Command (depending on Bus Out)	
8D	Set Target Register = to Bus Out	
8E	Set CYL ADDR Register = to Bus Out.	

RPS Only
String Switch Only

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DEVICE INTERFACE DATA FLOW AND ERROR DETECTION DEV-I 300



Inbound Line Name		A	B	C	D	E	F	G	H
Device Bus In Bit 0		—	B10	B02	M09	B02	D02	M09	B02
Device Bus In Bit 1		—	B07	B04	U12	B04	D04	U12	B04
Device Bus In Bit 2		—	G03	B05	U10	B05	D05	U10	B05
Device Bus In Bit 3		—	B09	B06	S02	B06	D06	S02	B06
Device Bus In Bit 4		—	G12	B08	P03	B08	D08	P03	B08
Device Bus In Bit 5		—	J04	B09	P09	B09	D09	P09	B09
Device Bus In Bit 6		—	G05	B10	M03	B10	D10	M03	B10
Device Bus In Bit 7		—	G13	B12	J06	B12	D12	J06	B12
Device Bus In Bit P		—	J13	B13	G09	B13	D13	G09	B13
Attn Select Bus Bit 4	Note 3	S08	—	D07	—	D05	B05	—	D02
Attn Select Bus Bit 5	Note 3	U10	—	D09	—	D06	B06	—	D03
Attn Select Bus Bit 6	Note 3	U11	—	D10	—	D07	B07	—	D05
Attn Select Bus Bit 7	Note 3	S12	—	D11	—	D08	B09	—	D06
Attn Select Bus Bit 0	Note 3	U03	—	D02	D07	D10	B10	—	D07
Attn Select Bus Bit 1	Note 3	U04	—	D03	B03	D11	B11	—	D09
Attn Select Bus Bit 2	Note 3	U06	—	D05	—	D02	B02	D07	D10
Attn Select Bus Bit 3	Note 3	U07	—	D06	—	D03	B03	B03	D11
Attn Select Bus Bit S		S04	—	D13	—	D13	B13	—	D13

Outbound Line Name		J	K	L	M	N	O
+ Device Out Bus Bit 0		—	P10	B02	G09	B02	D02
+ Device Out Bus Bit 1		—	P12	B04	B13	B04	D04
+ Device Out Bus Bit 2		—	U02	B05	J02	B05	D05
+ Device Out Bus Bit 3		—	S03	B06	D13	B06	D06
+ Device Out Bus Bit 4		—	S12	B08	B04	B08	D08
+ Device Out Bus Bit 5		—	U12	B09	B03	B09	D09
+ Device Out Bus Bit 6		—	U05	B10	D03	B10	D10
+ Device Out Bus Bit 7		—	U09	B12	J11	B12	D12
+ Device Out Bus Bit P		—	M07	B13	D04	B13	D13
+ NPL Tag Bus Bit 0		J10	—	D02	U03	D02	B02
+ NPL Tag Bus Bit 1		P03	—	D03	S02	D03	B03
+ NPL Tag Bus Bit 2		J12	—	D05	U02	D05	B05
+ NPL Tag Bus Bit P		J04	—	D06	S03	D06	B06
+ NPL Tag Gate		J02	—	D07	J10	D07	B07
+ NPL Select Hold		M03	—	D09	G10	D09	B09
— Power On Reset (Note 1)		Note 1		D10		D10	B10
				D11		D11	B11
+ File Tag Valid (Note 2)		Note 2		D13		D13	B13

Note 1: —Power On Reset is an MST line developed on the A1 board (A1C2U05) in the control module and sent to the A2 board (A2L2D04) on the outbound cable.

Note 2: +File Tag Valid is an NPL inbound line developed on the A1 board (A1D2J07) and sent to the A2 board (A2G2J07) on the outbound cable.

Note 3: The Attention Select bus lines are rotated in pairs as they pass through each module. This is done to allow each drive to present its unique physical address to the controller without the use of external address jumpers. See DEV-I 307 for Attention Select bus in bound lines.

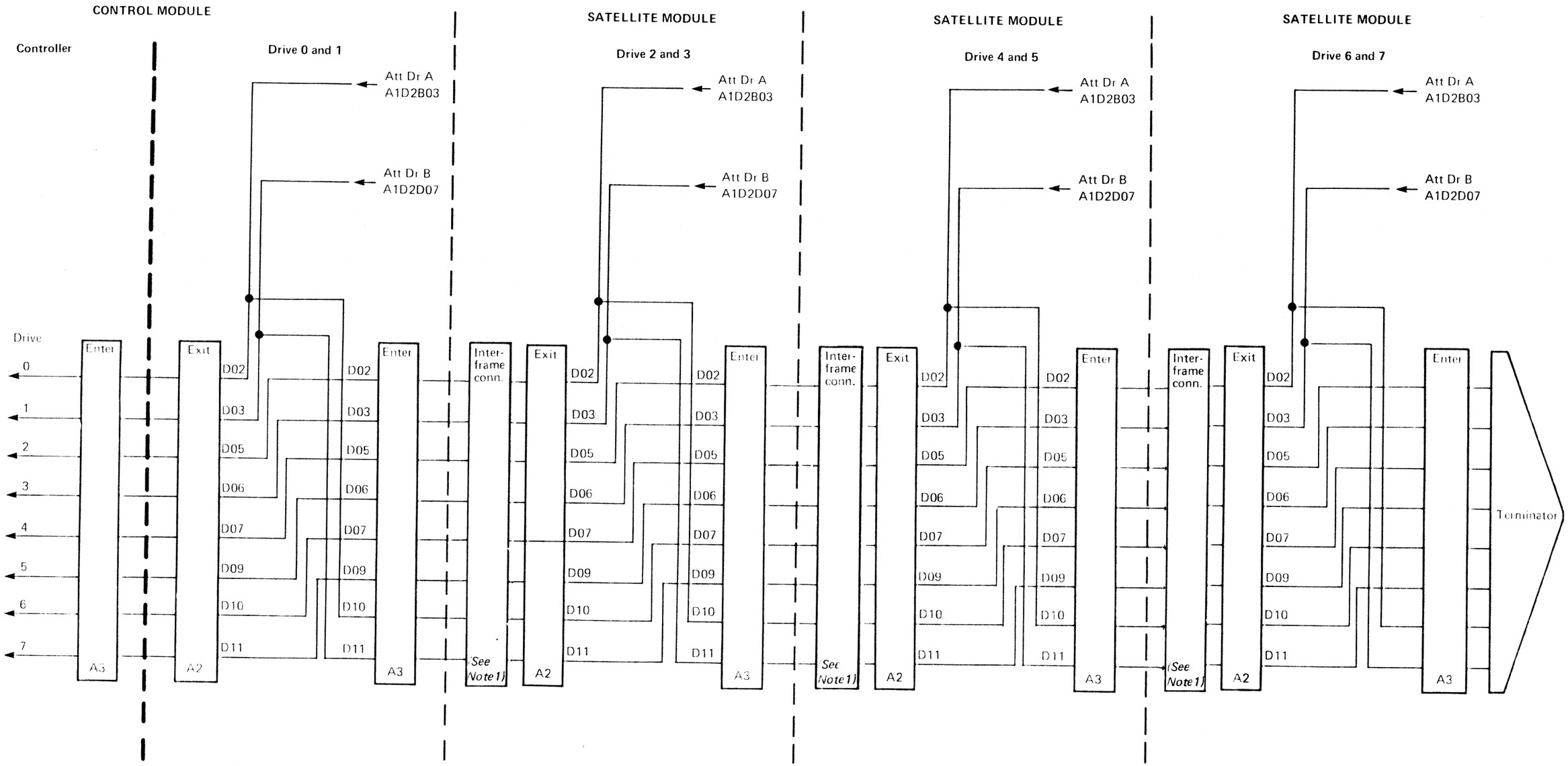
Note 4: Some satellite modules have the interframe cable connector as shown in the drawing. Pin designations E, F, N, and O show pins for this connector. Ignore these columns for machines without the connector.

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ATTENTION SELECT BUS
(DRIVE PHYSICAL ADDRESS WIRING)

The Attention Select bus lines are rotated in pairs as they pass through each module. This is done to allow each drive to present its unique physical address to the controller without the use of external address jumpers.

Note 1: Some satellite modules have an interframe cable connector. Refer to INST 5 for its physical location and DEV-I 305 for pin connections. Machines without the interframe connector are connected by cable directly between A2 of one module and A3 of the adjacent module.



DB0310	2747825	440209	440223					
Seq. 1 of 1	Part No. ( )	25 Mar 74	14 Mar 75					

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ACC CONTENTS

ACC MAPs – – – – – – – – – – – – – ACC 100–910

Provide maintenance procedures for analyzing problems related to the Access mechanism.

Access Operation – – – – – – – – – – – OPER 115, 116

High-level block diagram and description of access control, by card.

Access Control Sequence – – – – – – – OPER 119, 120

Flowchart of access control sequencing from one state to the next.

Track Following – – – – – – – – – – – OPER 123–125

High-level description of the track following function of the access mechanism.

INDEX Detection – – – – – – – – – OPER 126

Summary of the format of the even and odd indexes on the data module and how they are detected.

Rezero – – – – – – – – – – – – – – – – OPER 129–138

Functional diagrams, descriptions, and flowchart of the Rezero operation.

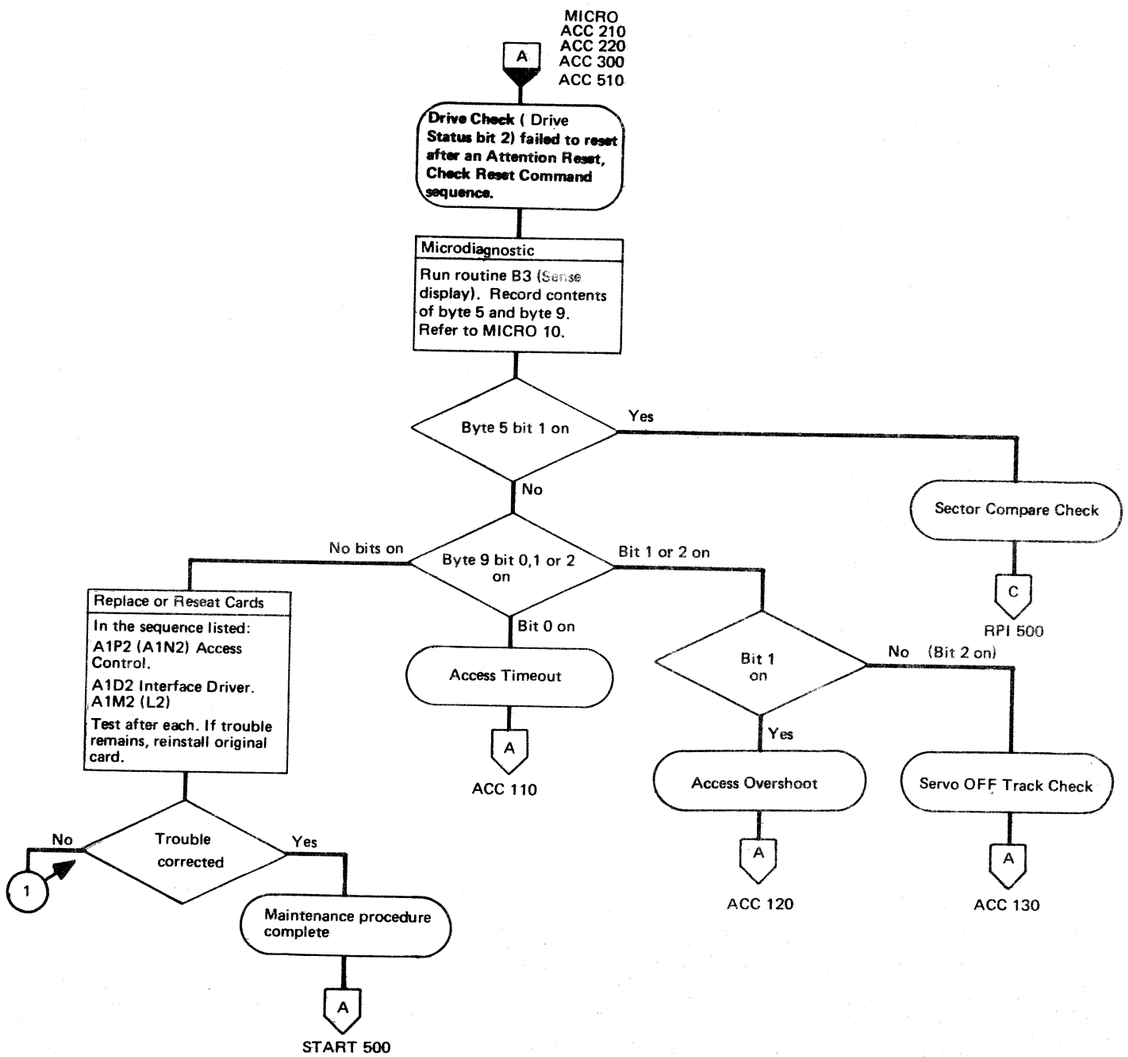
Seek – – – – – – – – – – – – – – – – – OPER 141–148

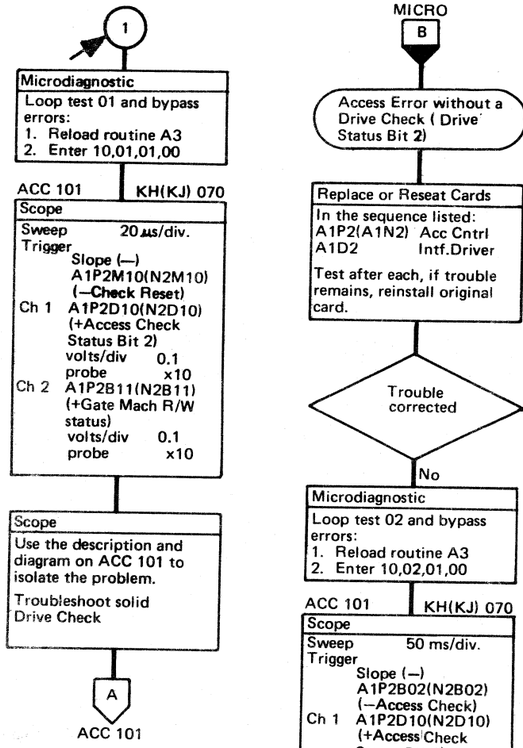
Functional diagrams, descriptions, and flowchart of the Seek operation.

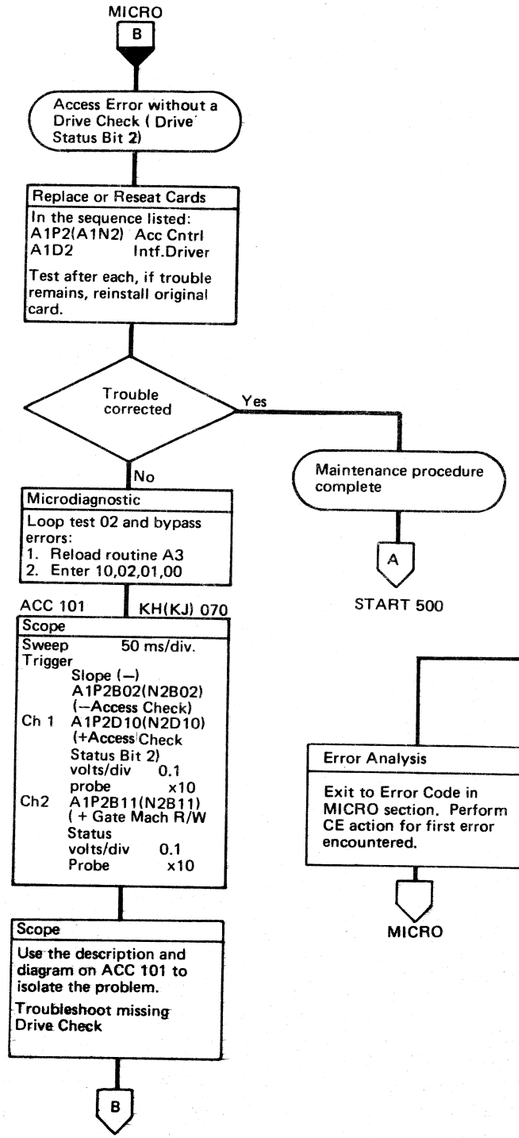
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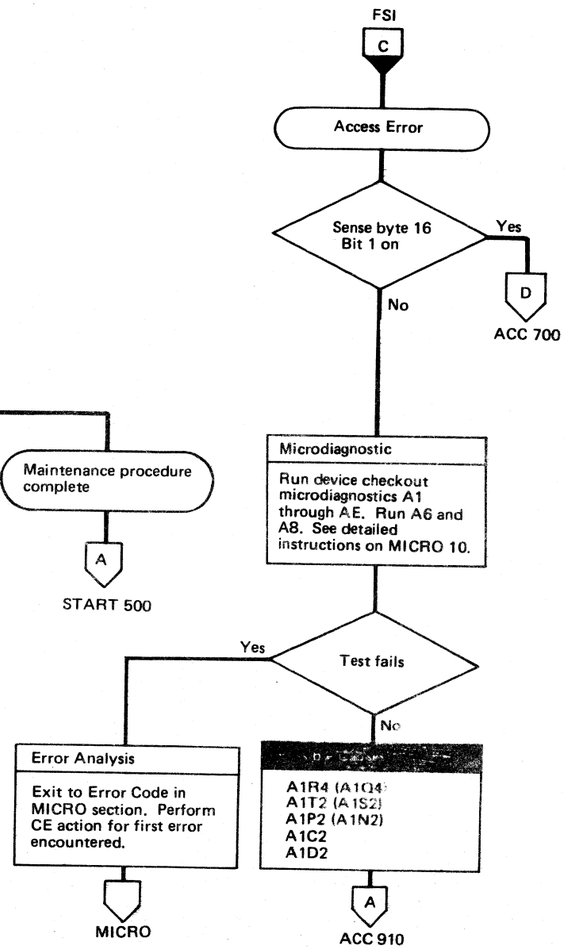
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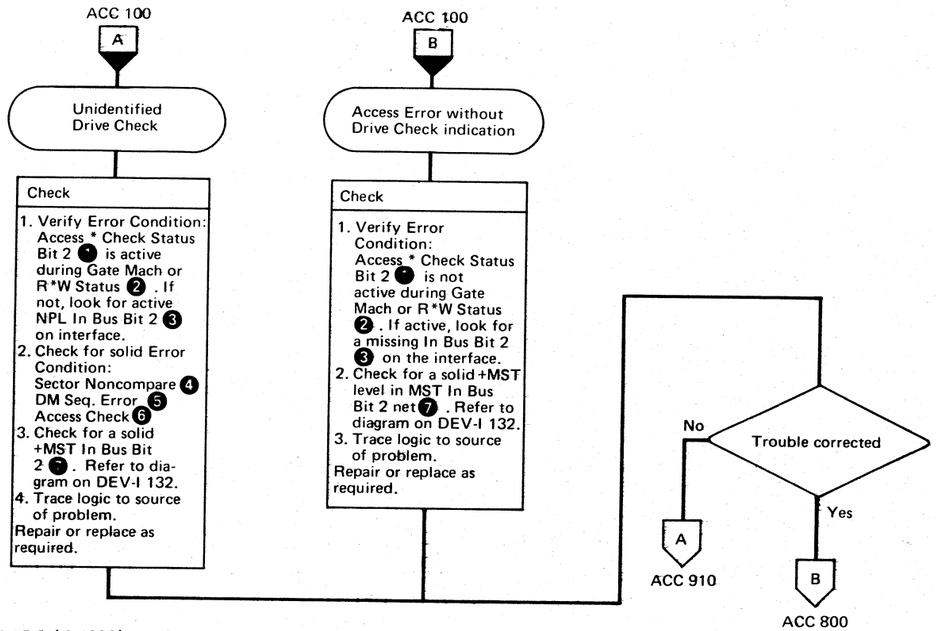


DE0100 Seq. 2 of 2	2747158 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440223 14 Mar 75			

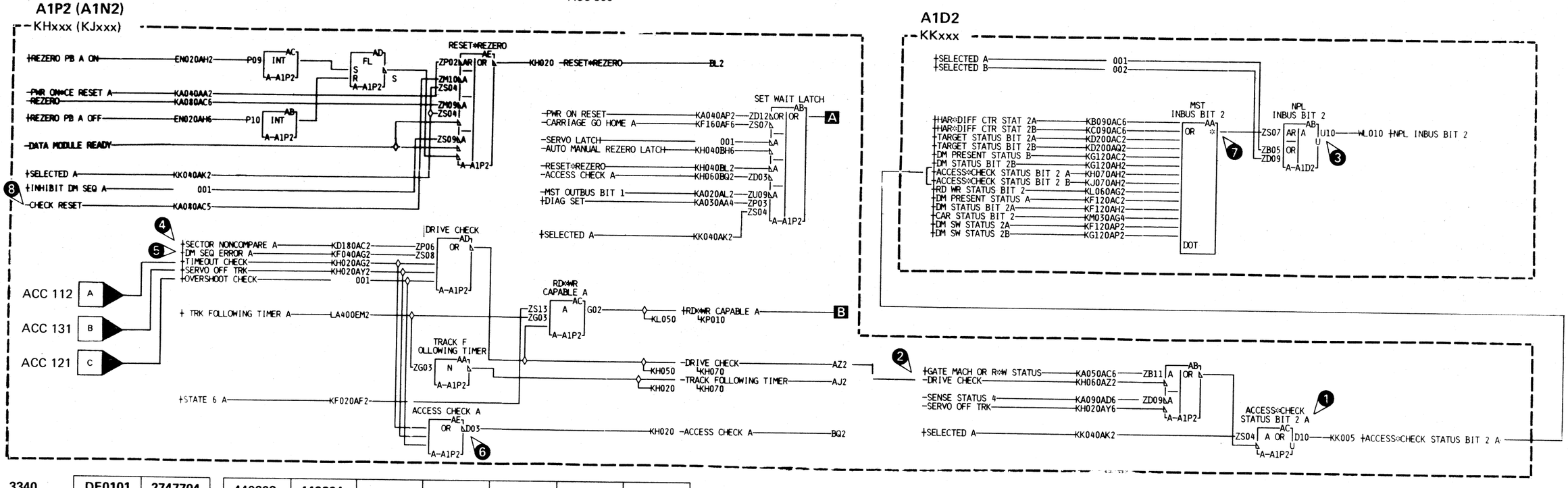
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DRIVE CHECK DIAGRAM



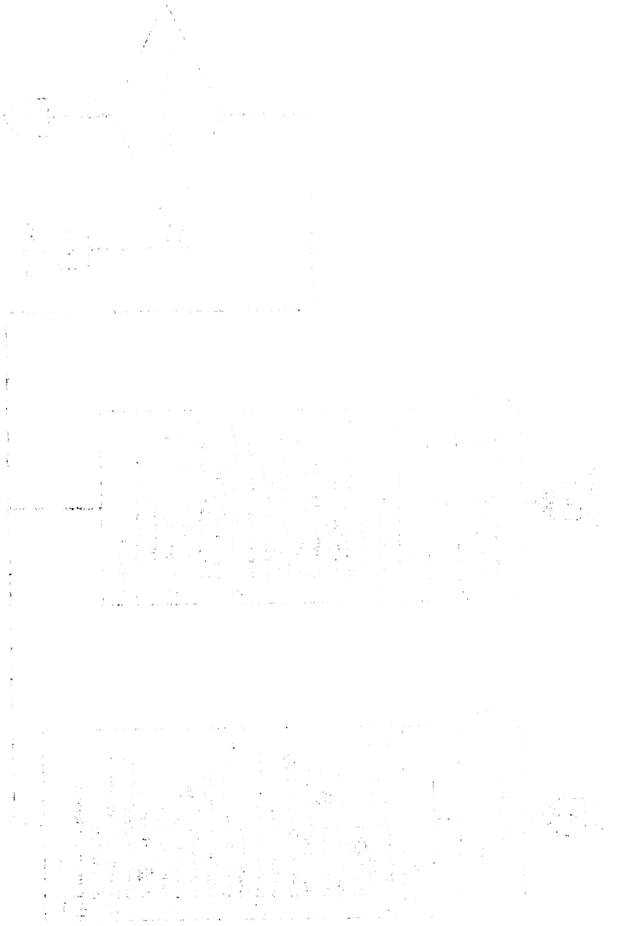
A +Set Wait Latch resets any access check condition. Check Reset ❽ or an Auto or Manual Rezero operation activates +Set Wait Latch.

B –Drive Check controls the condition of + Rd * Wr Capable (and the Ready Lamp) if the DM Sequence is in State 6 (DM Ready).

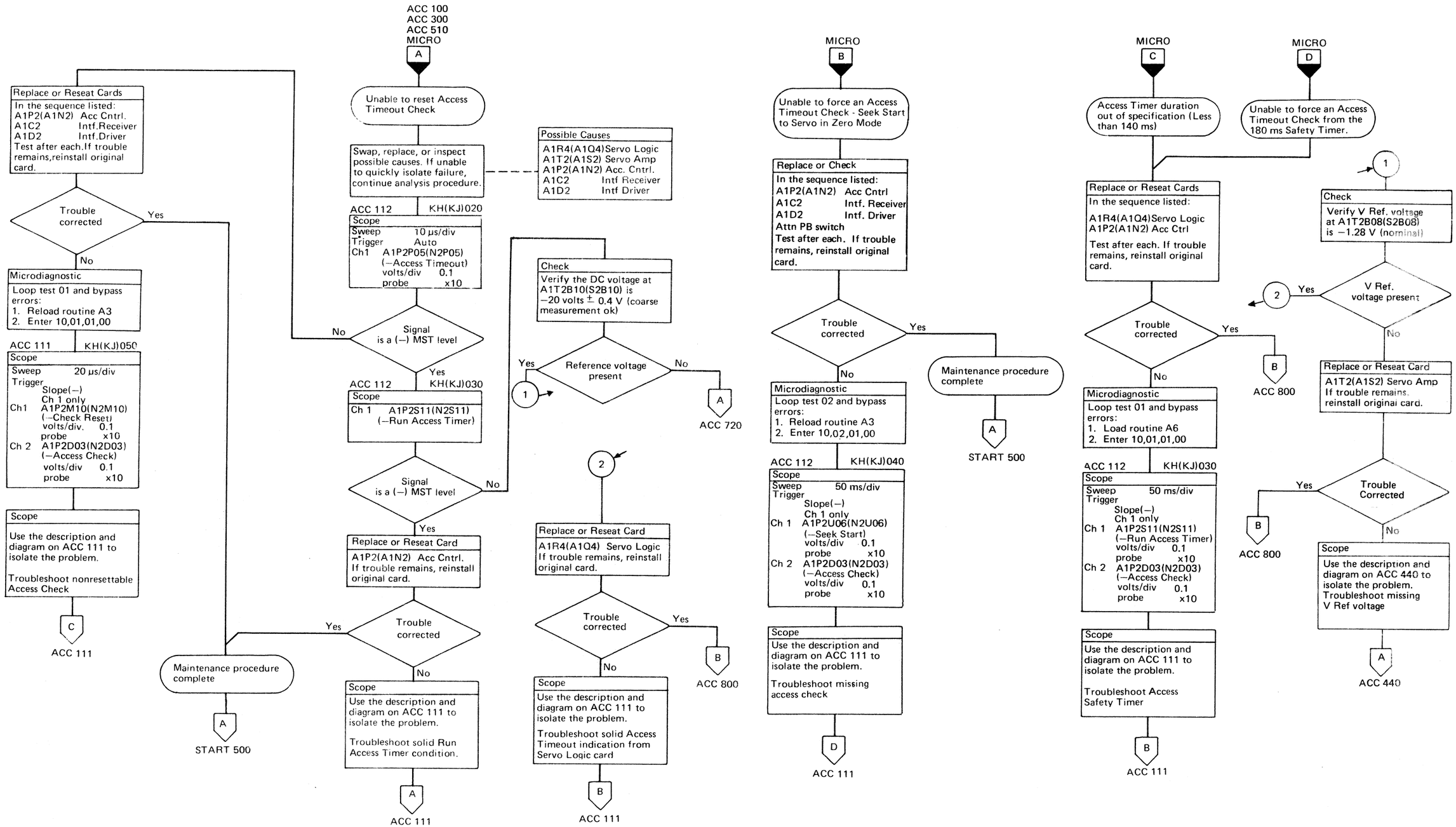


3340	DE0101 Seq. 1 of 1	2747704 Part No. ( )	440203 2 Nov 73	440204 21 Dec 73			

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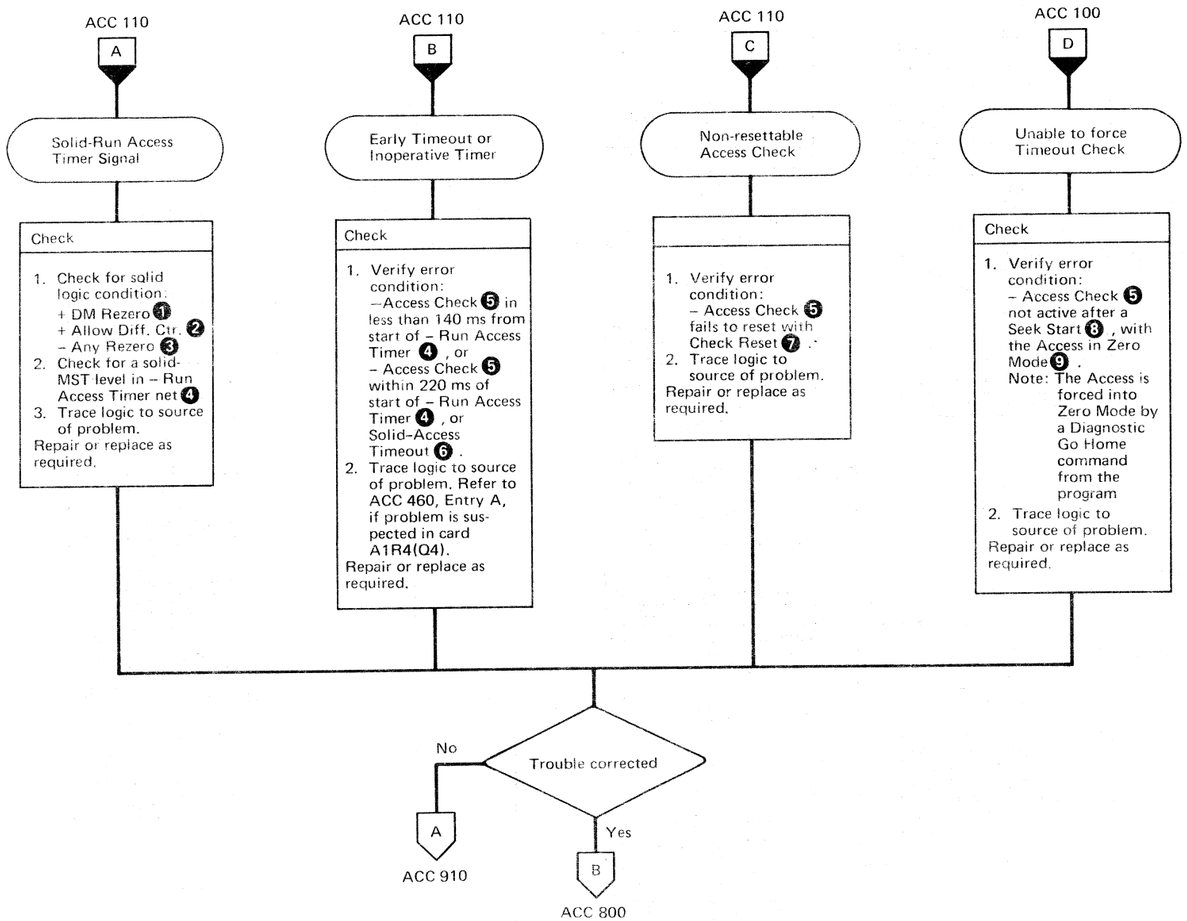


ACCESS CHECK/ACCESS SAFETY TIMER



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ACCESS SAFETY TIMER



A The Access Safety Timer generates a (–) Access Timeout pulse 180 ms ± 20% after the start of – Run Access Timer.

– Run Access Timer is reset with the completion of the Access Operation or detection of any Access Check.

B The Timeout Check latch is set by:

1. An Access Timeout during any Access operation.
2. A Seek Start command that is issued to an Access in Zero Mode.

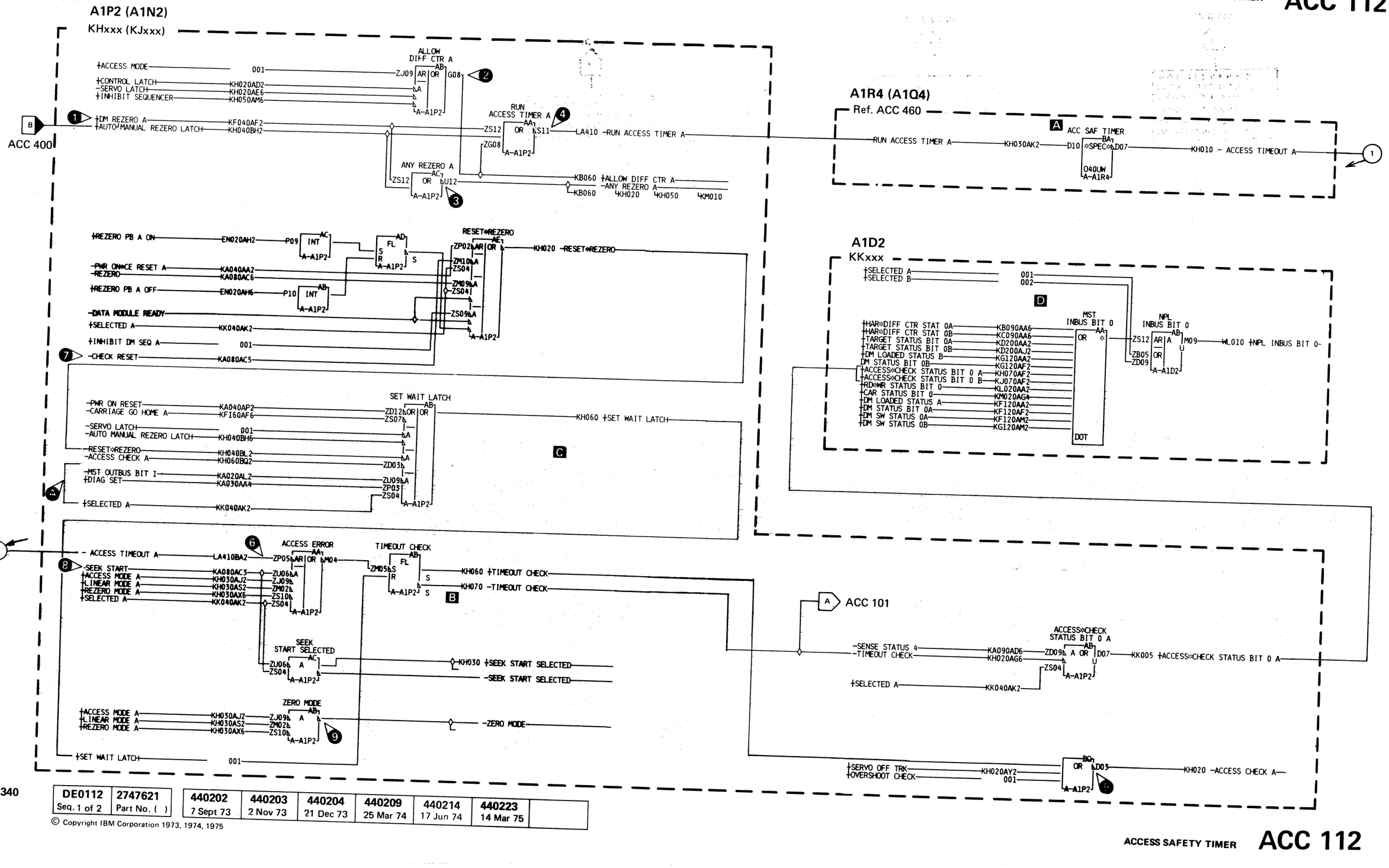
C The Timeout Check latch is reset by any condition that sets the Wait latch, including the manual rezero pushbutton.

D Refer to the diagram on DEV-I 184 for the complete MST In Bus configuration.

DE0110 Seq. 2 of 2	2747159 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440218 5 Aug 74	

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ACCESS SAFETY TIMER



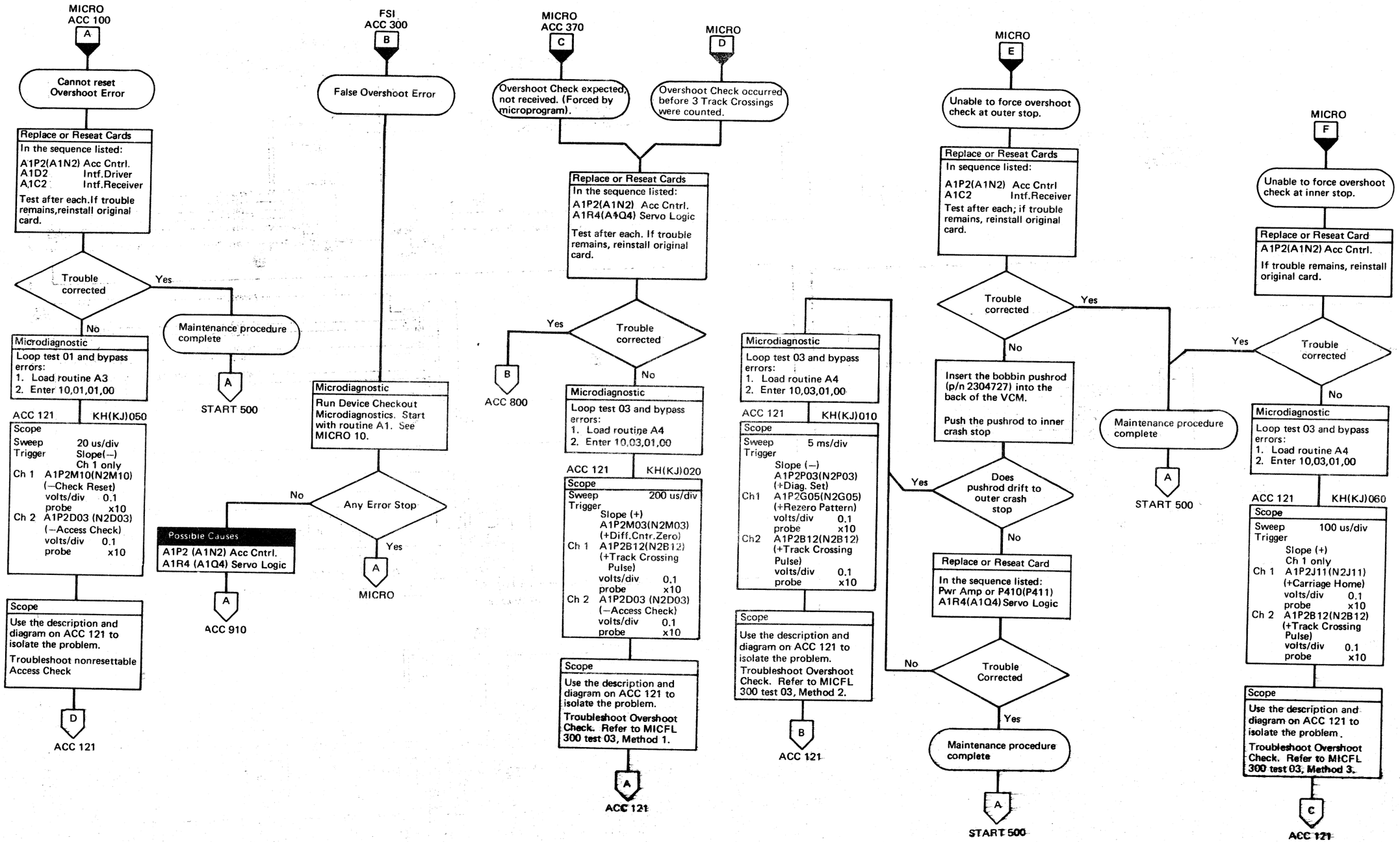
3340

DE0112	2747621
Seq. 1 of 2	Part No. ( )

440202	440203	440204	440209	440214	440223	
7 Sept 73	2 Nov 73	21 Dec 73	25 Mar 74	17 Jun 74	14 Mar 75	

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ACCESS CHECK/OVERSHOOT CHECK



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OVERSHOOT CHECK DIAGRAM

ACC 120 A

Overshoot Track Crossing counter defective

Check

1. Verify error condition:
   The Difference Counter is set to zero ❶ in the middle of a Seek operation. After a count of 3 Track Crossing Pulses ❷, –Access Check ❸ is set by the Overshoot Check latch.
2. Trace logic to source of problem.

Repair or replace as required.

Trouble corrected?

No → A → ACC 910

Yes → B → ACC 800

ACC 120 B

Overshoot check not detected in Pattern Area

Check

1. Verify error condition:
   The Servo is forced into Zero Mode (Ref. ACC 112) by a Diagnostic Servo Reset command ❹. The carriage is free floating and drifts towards the Rezero Pattern area. The Track Crossing Pulse ❷ signal is reset to a solid (+) MST level and detection of Rezero Pattern ❺ sets the Overshoot Check latch and turns on Access Check ❸ (Note A).
2. Trace logic to source of problem.

Repair or replace as required.

ACC 120 C

Overshoot check not detected at Home Position

Check

1. Verify error condition:
   The program issues a series of 1-track Seeks towards the inner stop. Detection of a Track Crossing Pulse ❷ after the Carriage Home position ❻ is indicated sets the Overshoot Check latch and turns on Access Check ❸ (Note B).
2. Trace logic to source of problem.

Repair or replace as required.

ACC 120 D

Non-resettable Overshoot check

Check

1. Verify error condition:
   A Check Reset ❼ command activates the Set Wait latch signal C, which resets the Overshoot Check Latch and turns off –Access Check ❸.
2. Trace logic to source of problem.

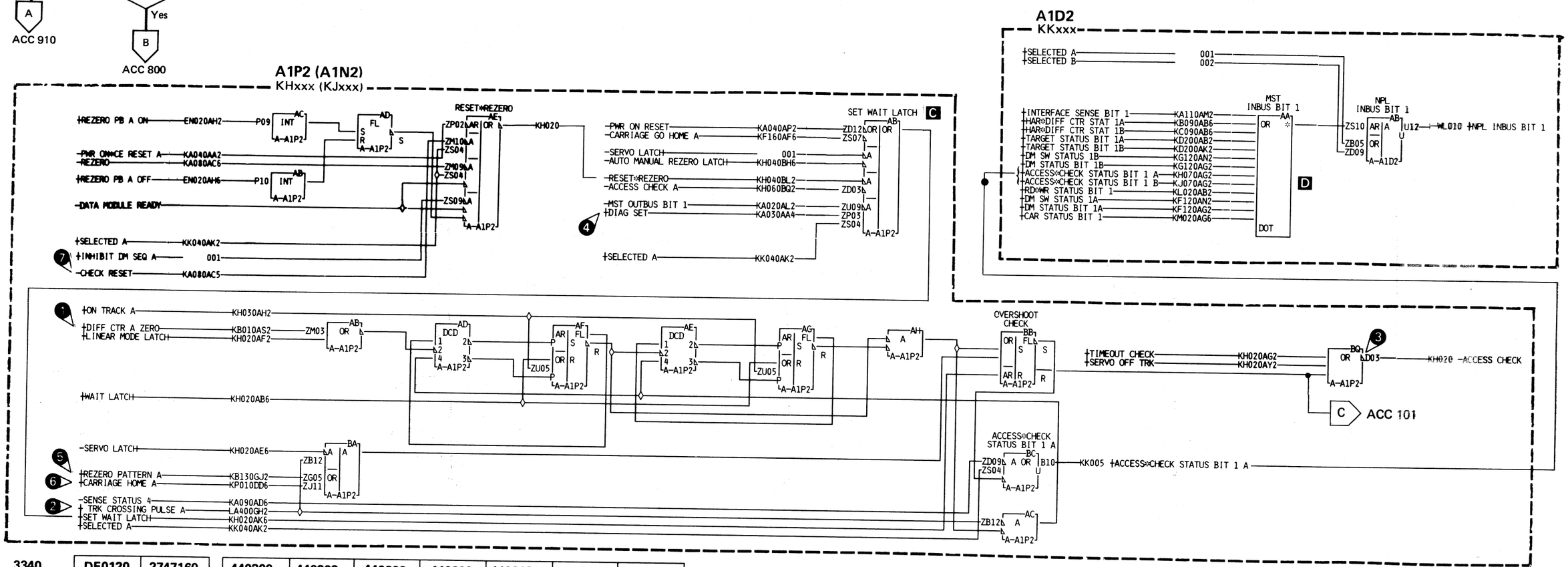
Repair or replace as required.

A This test simulates error detection from a Seek into the outer crash stop or Rezero Pattern area.

B This test simulates error detection from a Seek into the inner crash stop or Home Position.

C The Overshoot Check latch is reset by any condition that sets the Wait latch.

D Refer to the diagram on DEV-1 184 for the complete MST In Bus configuration.



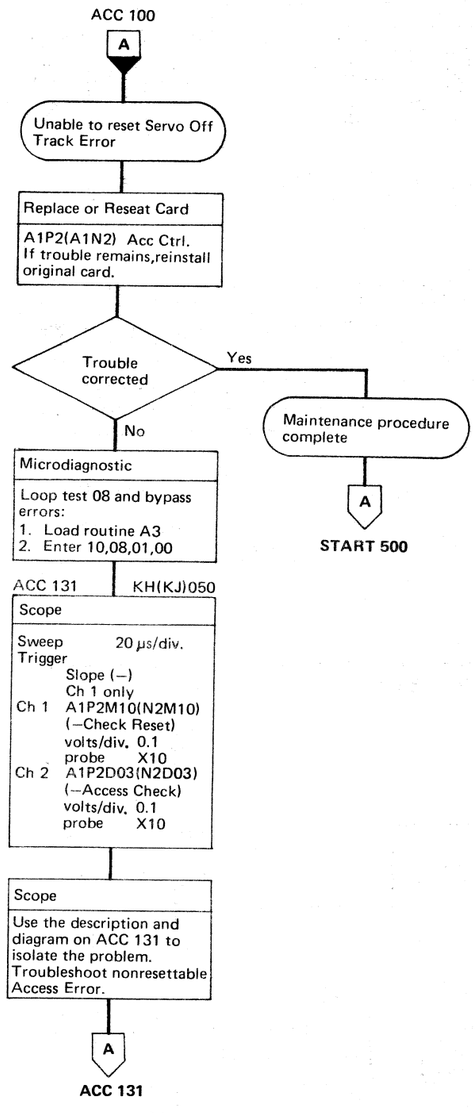
DE0120 Seq. 1 of 2	2747160 Part No. ( )

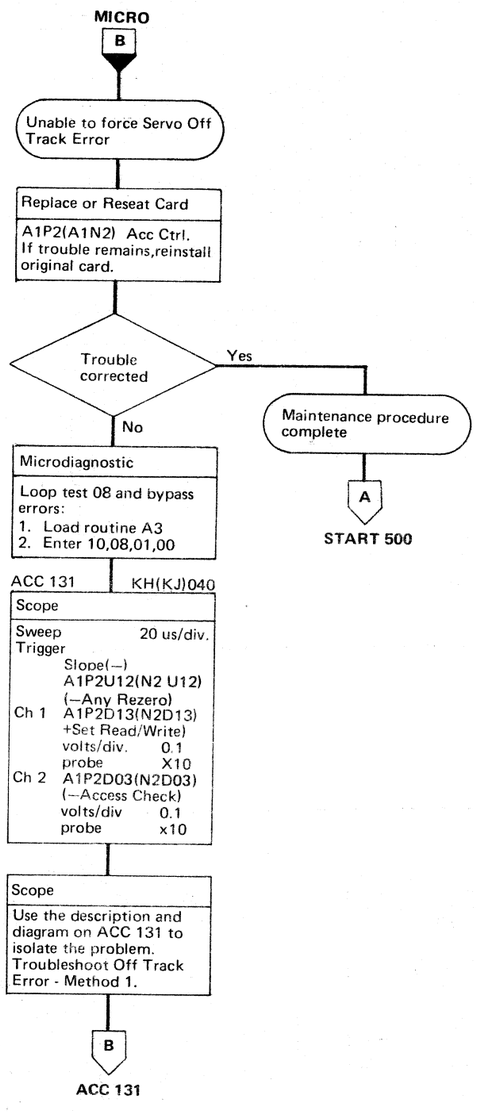
440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440213 13 May 74	440214 17 Jun 74	440223 14 Mar 75

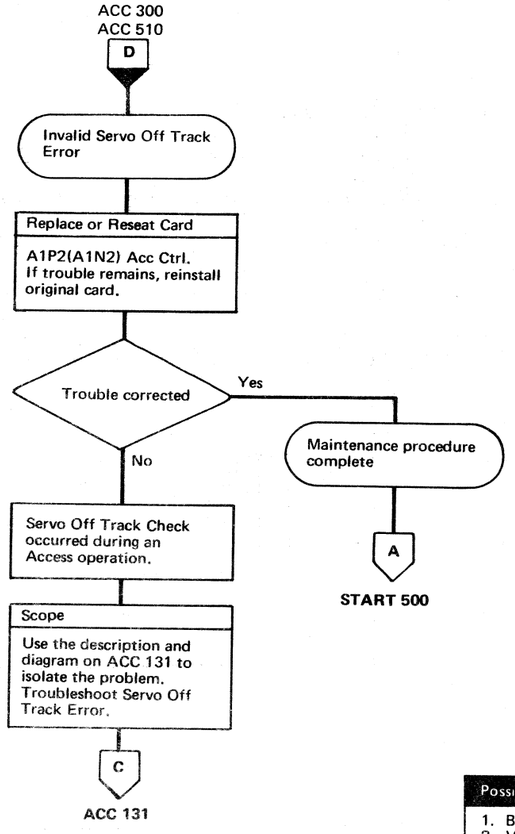
3340

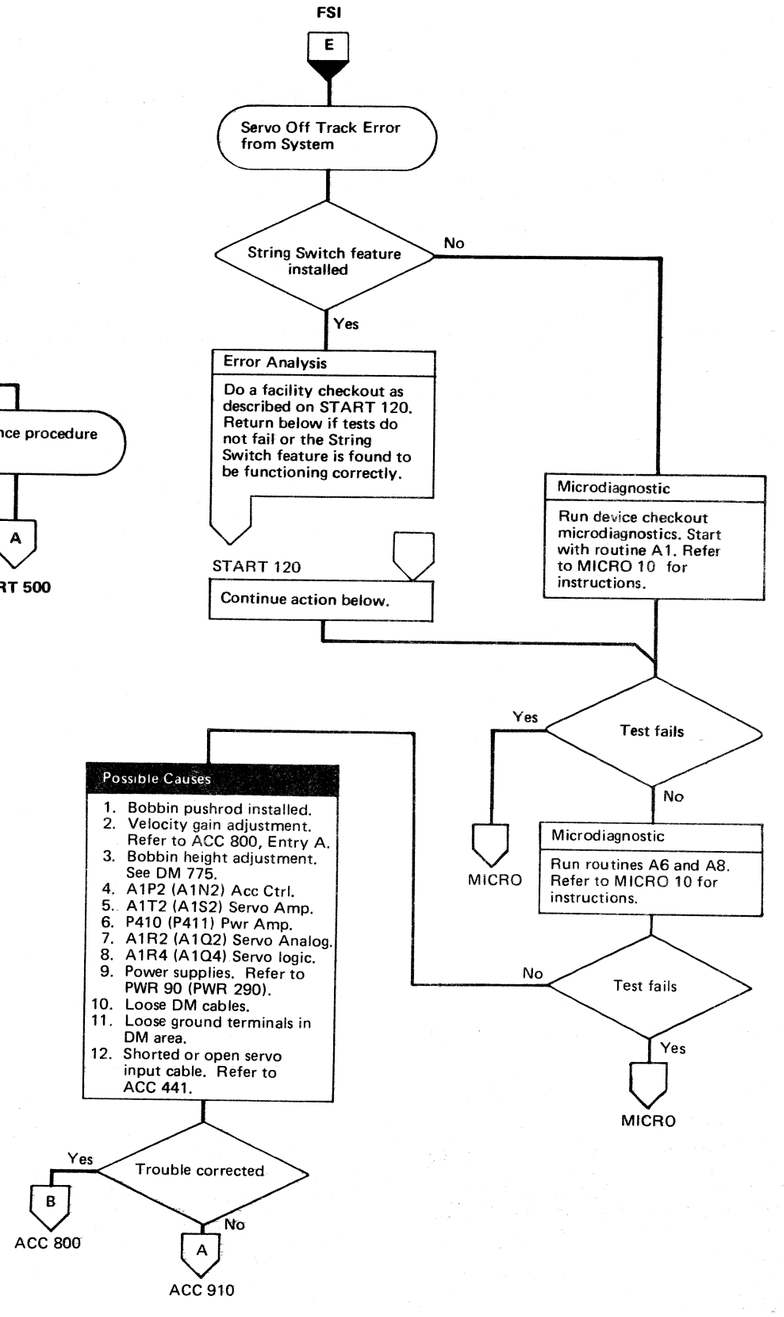
© Copyright IBM Corporation 1973, 1974, 1975

ACCESS CHECK/SERVO OFF TRACK









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SERVO OFF-TRACK

ACC 130 A

Non-resettable servo off-track error

Check

1. Verify Error condition:
   A Check Reset ❶ command activates the Set Wait latch signal **A** which resets the Servo Off Track latch and turns Off-Access Check ❷.
2. Trace logic to source of problem.

Repair or replace as required.

ACC 130 B

Unable to force servo off-track error

Check

1. Verify error condition:
   +Set Read*Write ❸ active during a Rezero operation causes Track Following Timer ❹ to reset and results in an Access Check ❷.
2. Trace logic to source of problem.

Repair or replace as required.

ACC 130 C

Servo off-track error occurred during an Access operation

Microdiagnostic

Loop the failing test and bypass errors.
1. Reload routine.
2. Enter 10,XX,01,00
   (XX = test number).

Check

1. Verify error condition:
   +Set Read*Write ❸ should not be on when +Track Following Timer ❹ is normally off during an Access operation during which time Read/Write operations should not be attempted.
2. Trace logic to source of problem.

Repair or replace as required.

No — Trouble corrected

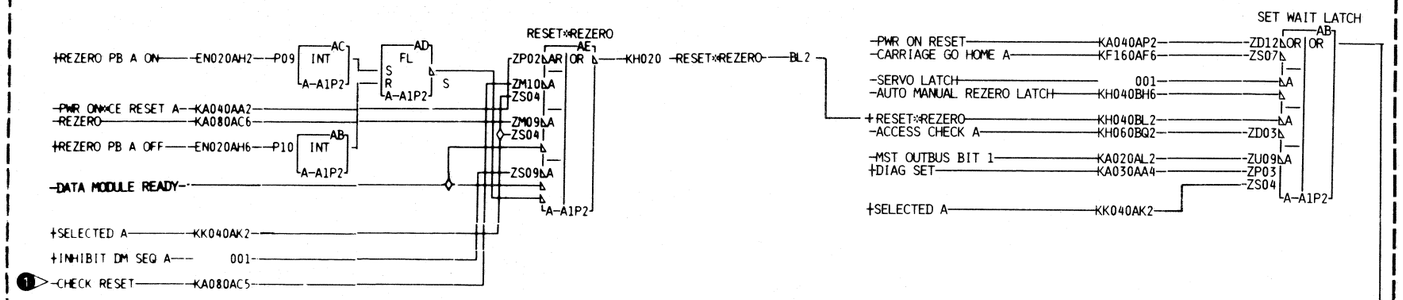
Yes — Maintenance procedure complete

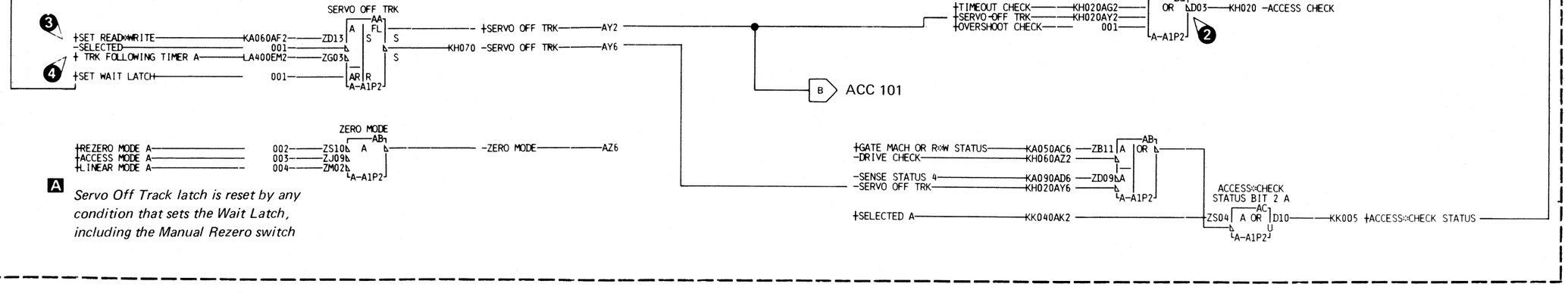
A → ACC 910

A → START 500

A1P2 (A1N2)

KHxxx(KJxxx)

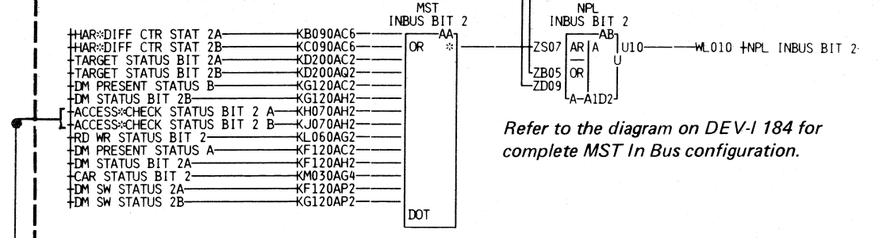




A *Servo Off Track latch is reset by any condition that sets the Wait Latch, including the Manual Rezero switch*

A1D2

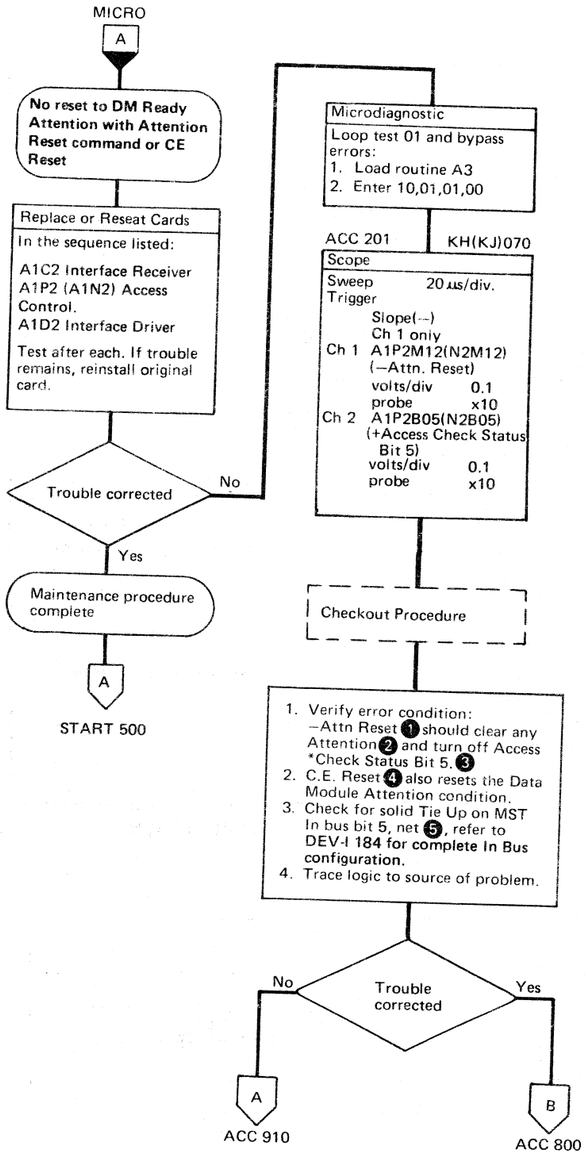
KKxxx



Refer to the diagram on DEV-I 184 for complete MST In Bus configuration.

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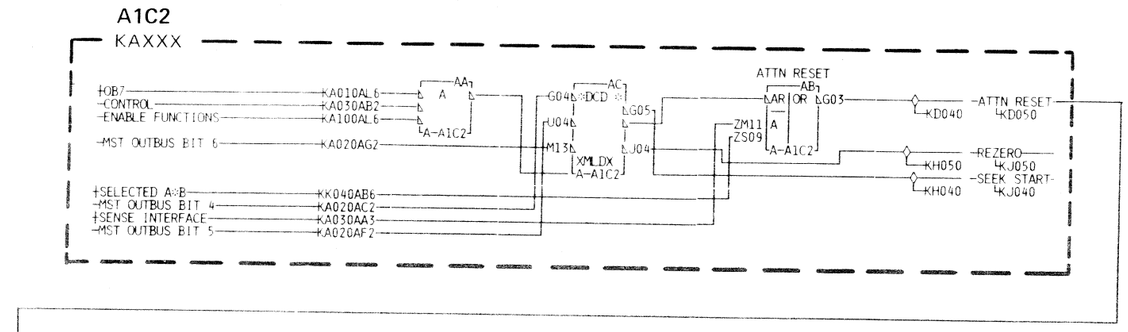
DRIVE STATUS/DATA MODULE READY

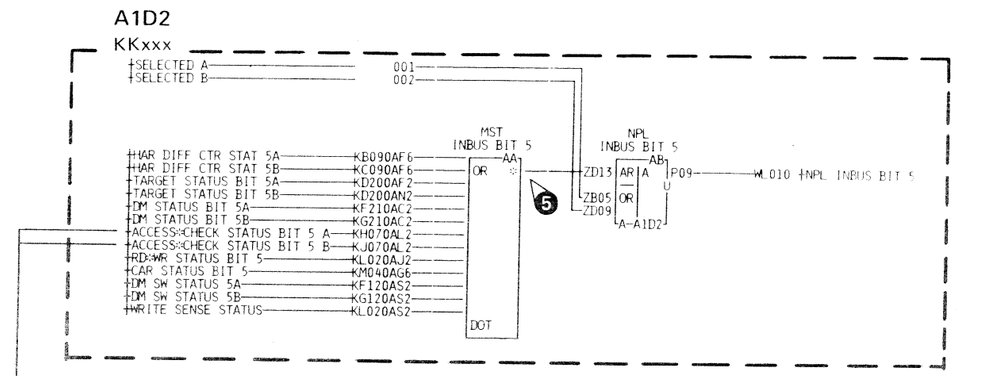


DE0130	2747161	440200	440202	440203	440209	440214		
Seq. 2 of 2	Part No. ( )	25 Jun 73	7 Sept 73	? Nov 73	25 Mar 74	17 Jun 74		

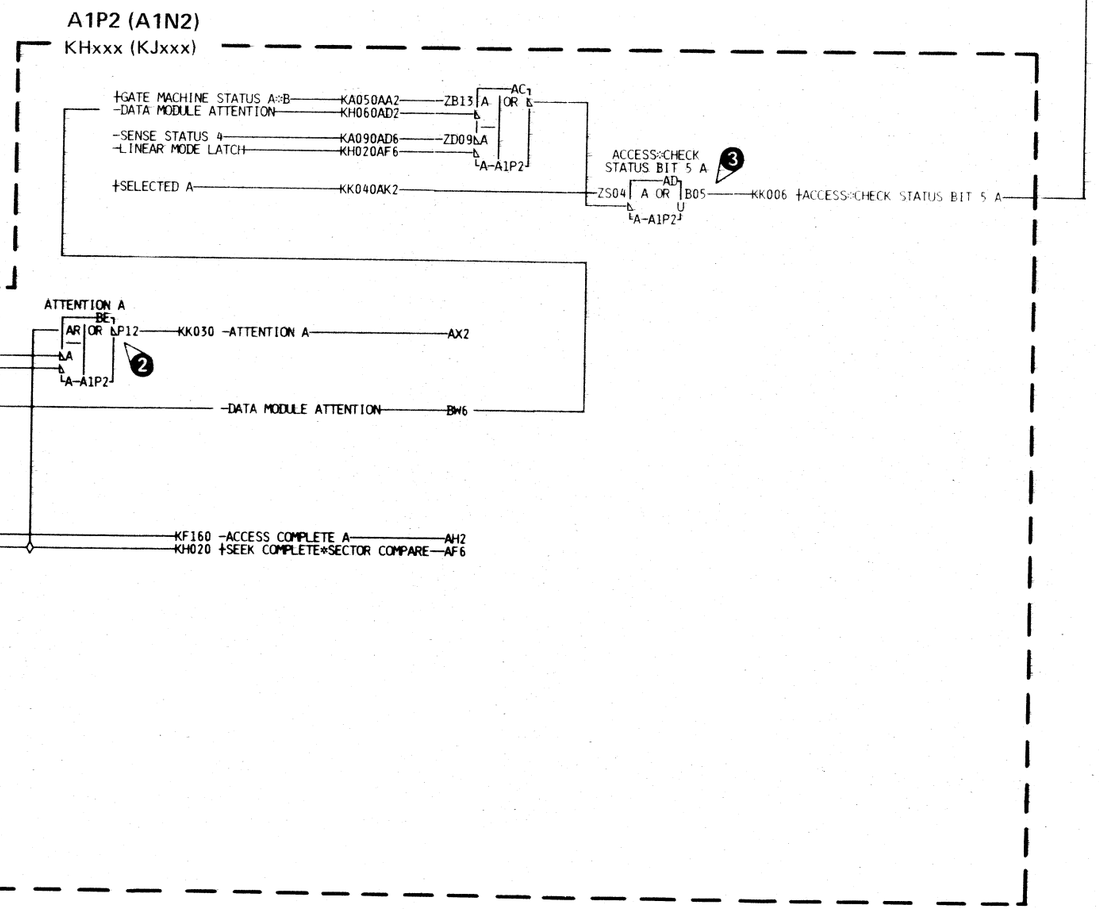
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DATA MODULE READY DIAGRAM



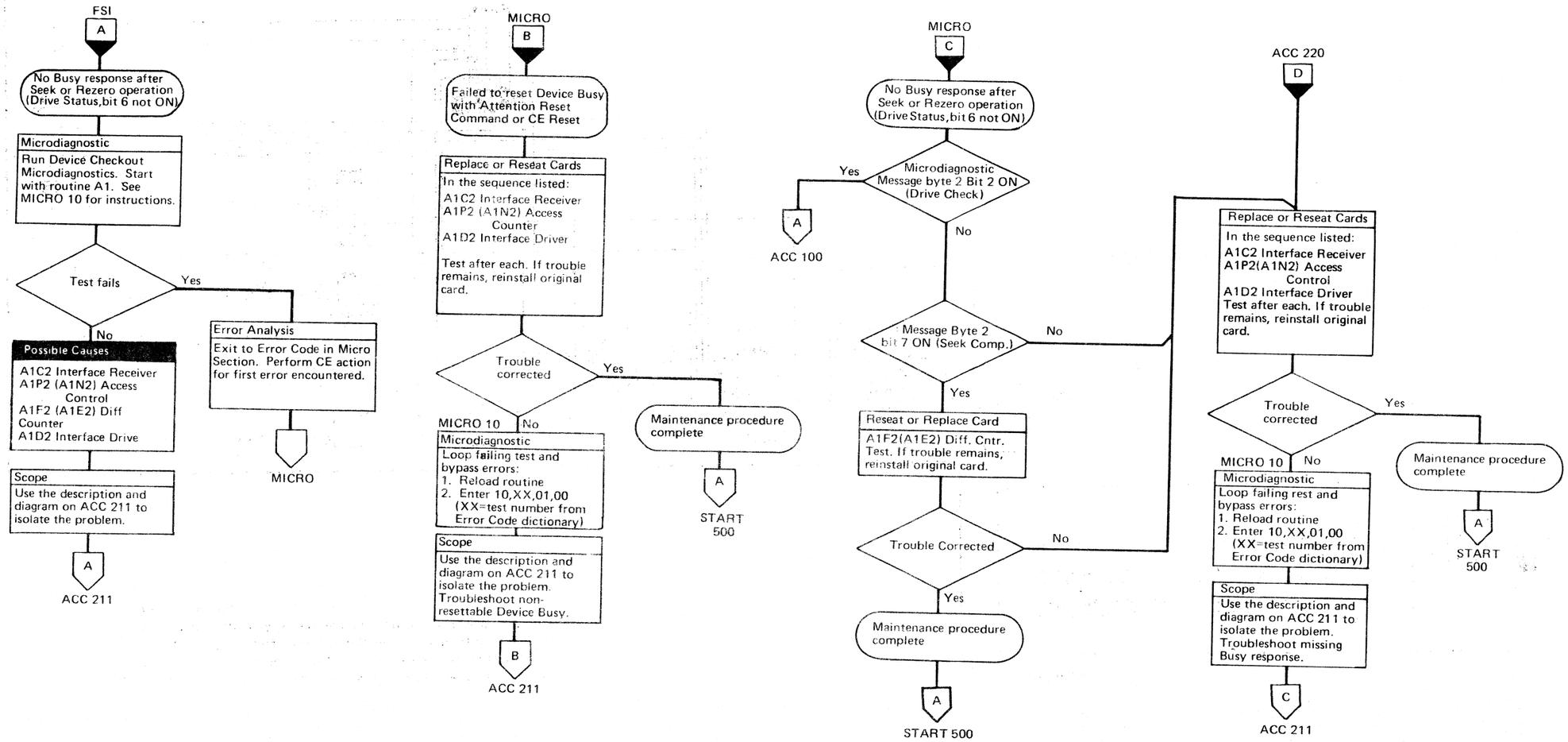


A The Data Module Attention latch is set during a Manual Rezero (Pushbutton) and a Data Module Load Rezero. The output is gated to the In Bus by Access Complete. An Attention is posted except where the DM Rezero ended in an Access Check and the drive is not online.



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DRIVE STATUS/DEVICE BUSY



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DEVICE BUSY DIAGRAM

ACC 210 A

No Busy Response from an access operation

Theory of operation:
The Busy Latch A is set on by a Seek Start 1 or Rezero 2 command and Not On Track 3. (Refer to ACC 400 for Rezero Start logic and ACC 600 for Seek Start logic.) Busy is sensed on the interface until Seek Complete is set by either an On Track or an Access Check. The Busy Latch is reset by an Attention Reset command.

ACC 210 B

Non-resettable Device Busy

Check

1. Verify that +Access * Check Status Bit 6 4 is not active with +Gate Machine Status 5 after an Attention Reset 6.
2. Verify that +Search Sector 7 is off.
3. Check for a solid +MST level in MST In Bus Bit 6 net 8. **Refer to DEV-I 184** for In Bus configuration.
4. Trace logic to source of problem.

Repair or replace as required.

ACC 210 C

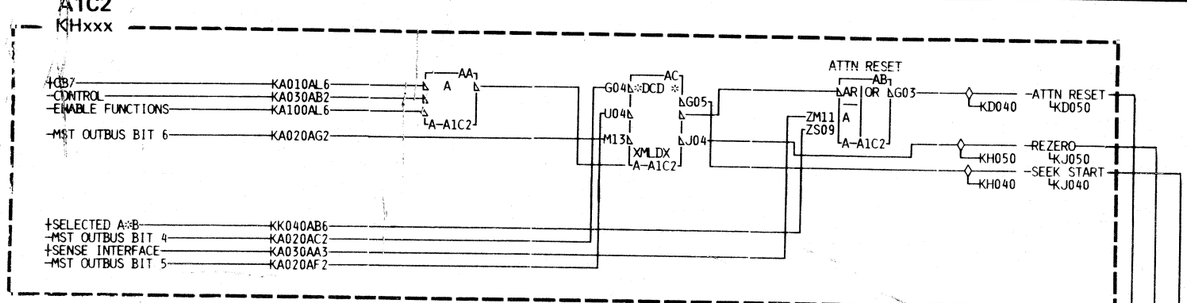
No Busy response from an Access Operation

Check

1. Verify that +Access * Check Status Bit 6 4 is active with +Gate Machine Status 5 after a Rezero 2 or Seek Start 1.
2. Verify that On Track 3 or Access Check (ACC 101) is not active before Gate Machine Status. If On Track is active, refer to ACC 400 for Rezero Start, or ACC 600 for Seek Start logic. If Access Check is active, refer to ACC 101 for Drive Check logic.
3. Trace logic to source of problem.

Repair or replace as required.

Trouble corrected? No → A → ACC 910; Yes → A → START 500

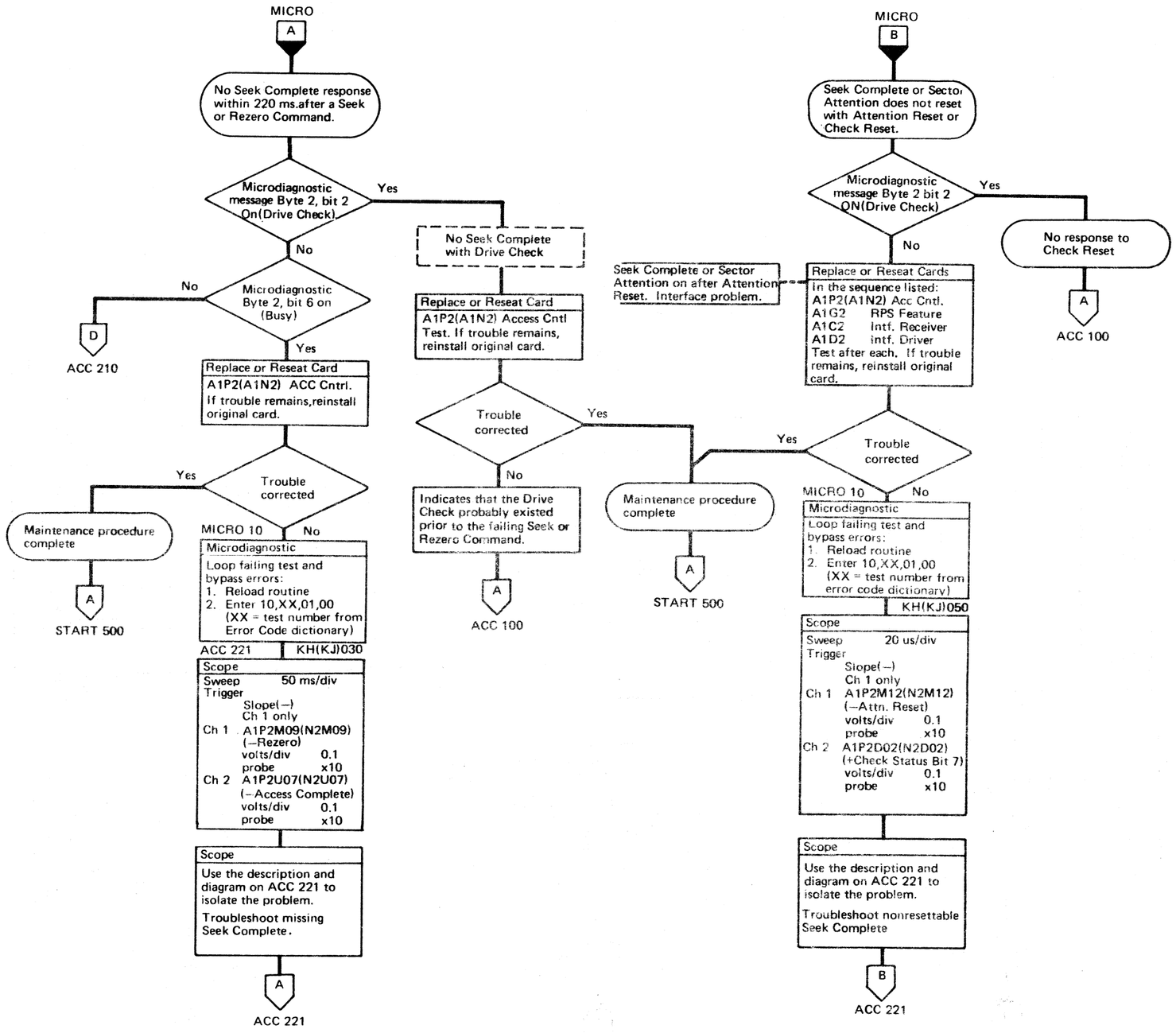


DE0210 Seq. 1 of 2	2747163 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74			

3340

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DRIVE STATUS–SEEK COMPLETE



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DRIVE STATUS -- SEEK COMPLETE DIAGRAM

ACC 220 (A)

No Seek Complete response from a Seek or Rezero command

Check

1. Verify the following:
   --Access Complete ❶ is active within a maximum of 220 ms after any Selected ❷, Rezero ❸, or Seek Start ❹ command.
   If --Access Complete is not active and + On Track ❺ does not become active, refer to ACC 111, Entry B, for checkout of Access Safety timer.
2. +Check Status Bit 7 ❻ and +Gate Machine Status ❼ indicates Seek Complete * Sector Compare to the In Bus.
3. Trace logic to source of problem.

Repair or replace as required.

ACC 220 (B)

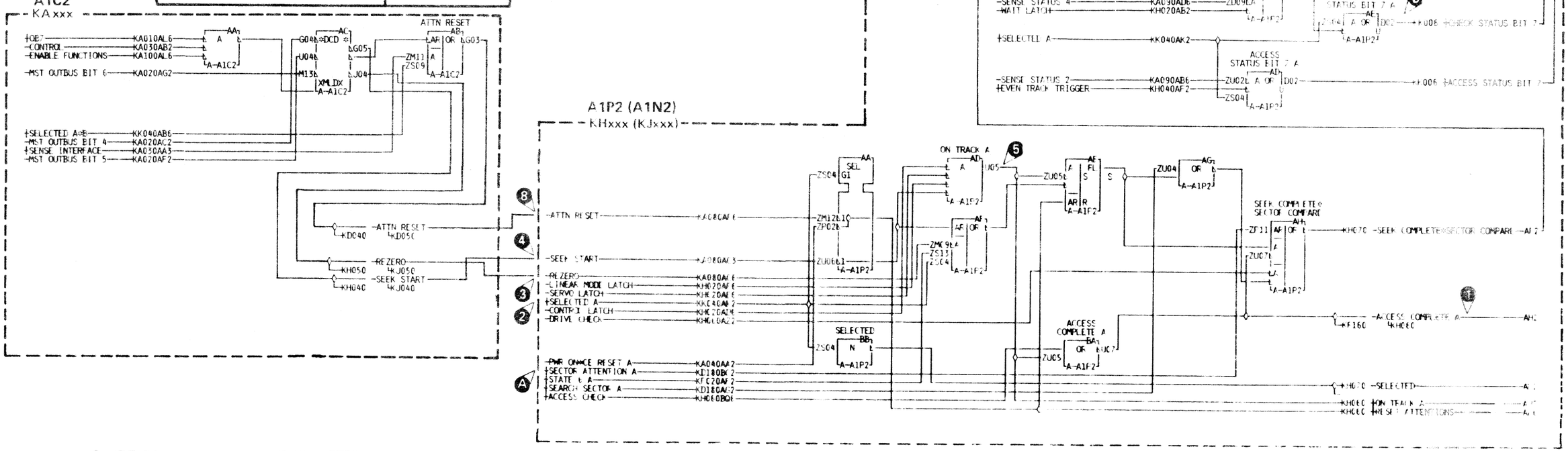
Non-Resettable Seek Complete

Check

1. Verify the following:
   --Attn. Reset ❽ or --Pwr On * CE Reset resets the Busy latch which blocks --Access Complete from being gated to In Bus Bit 7 ❾ as Seek Complete
2. Verify +Sector Attention ❿ is a --MST level.
3. Check for a solid +MST level in MST In Bus Bit 7 net. Refer to DEV-I 184 for the complete In Bus configuration.
4. Trace logic to source of problem.

Repair or replace as required.

Trouble corrected? No → A (ACC 910) / Yes → B (ACC 800)

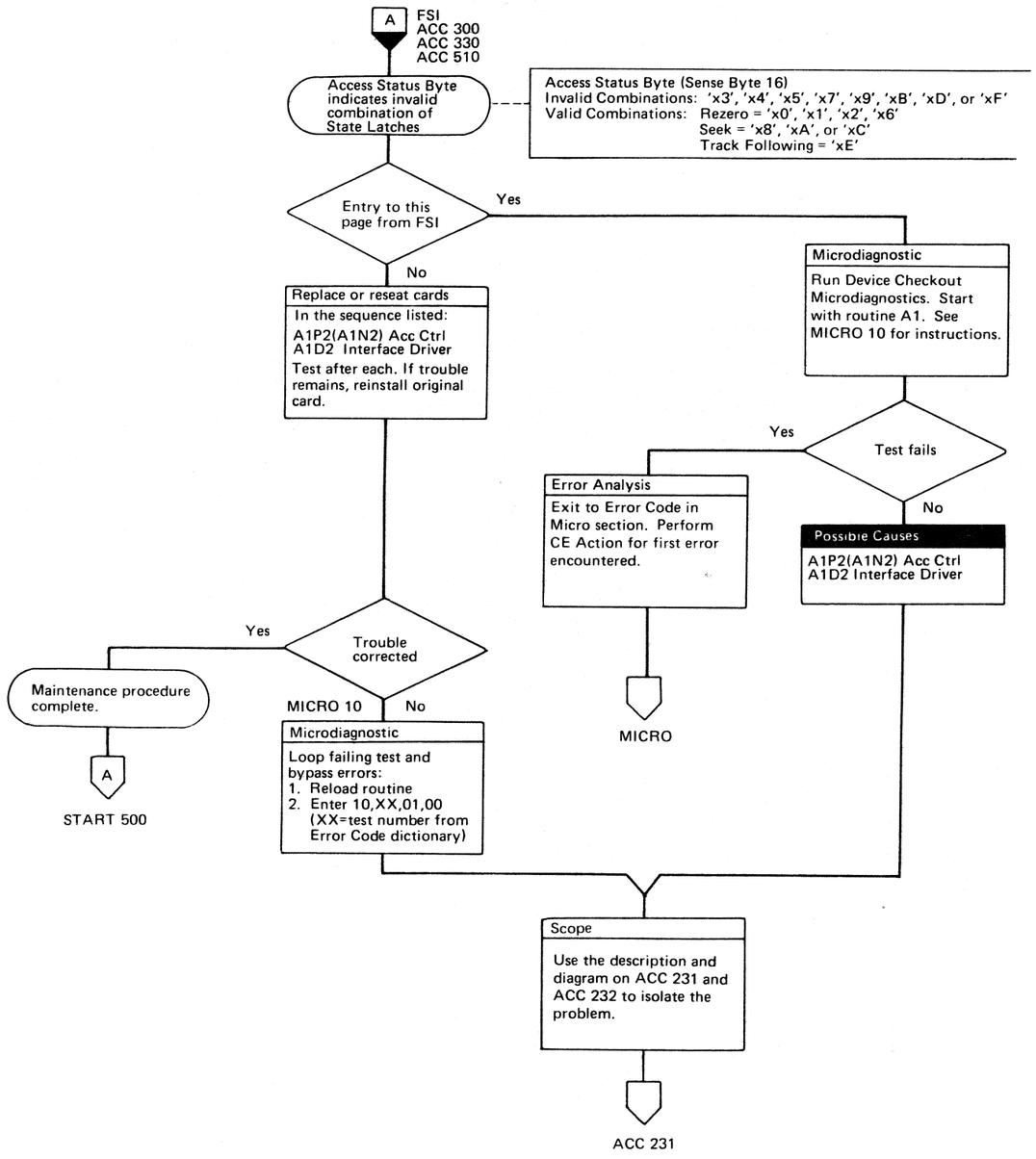


3340	DEC220	2747164	440200	440202	440203	440209
	Sht 1 of 1	Part No. rev	25 Jun 73	7 Sep 73	1 Nov 73	25 Mar 74

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ACCESS STATUS–INVALID STATE

ACCESS STATUS–INVALID STATE

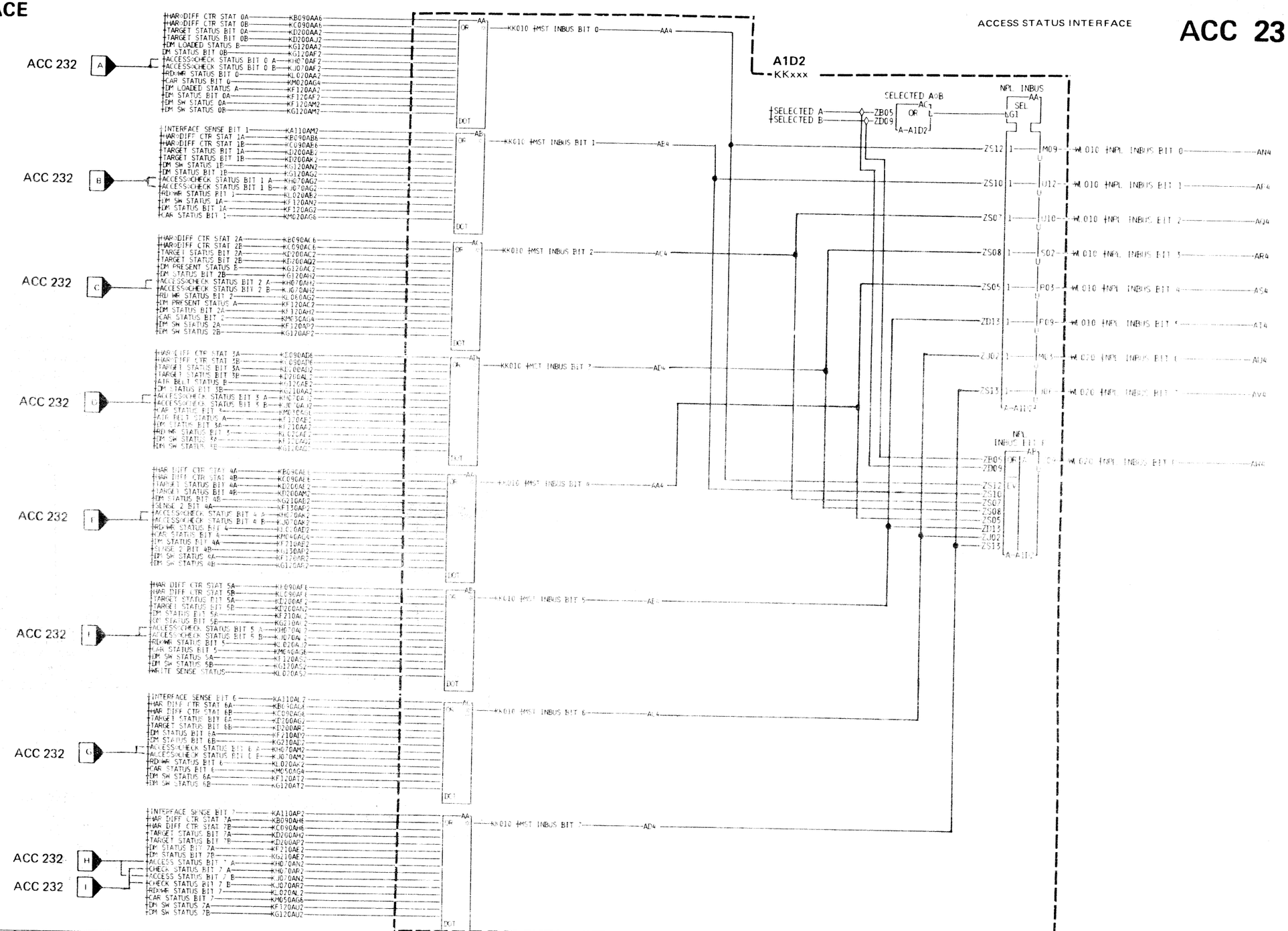


DE0230 Seq. 1 of 2	2747165 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440223 14 Mar 75			

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ACCESS STATUS INTERFACE

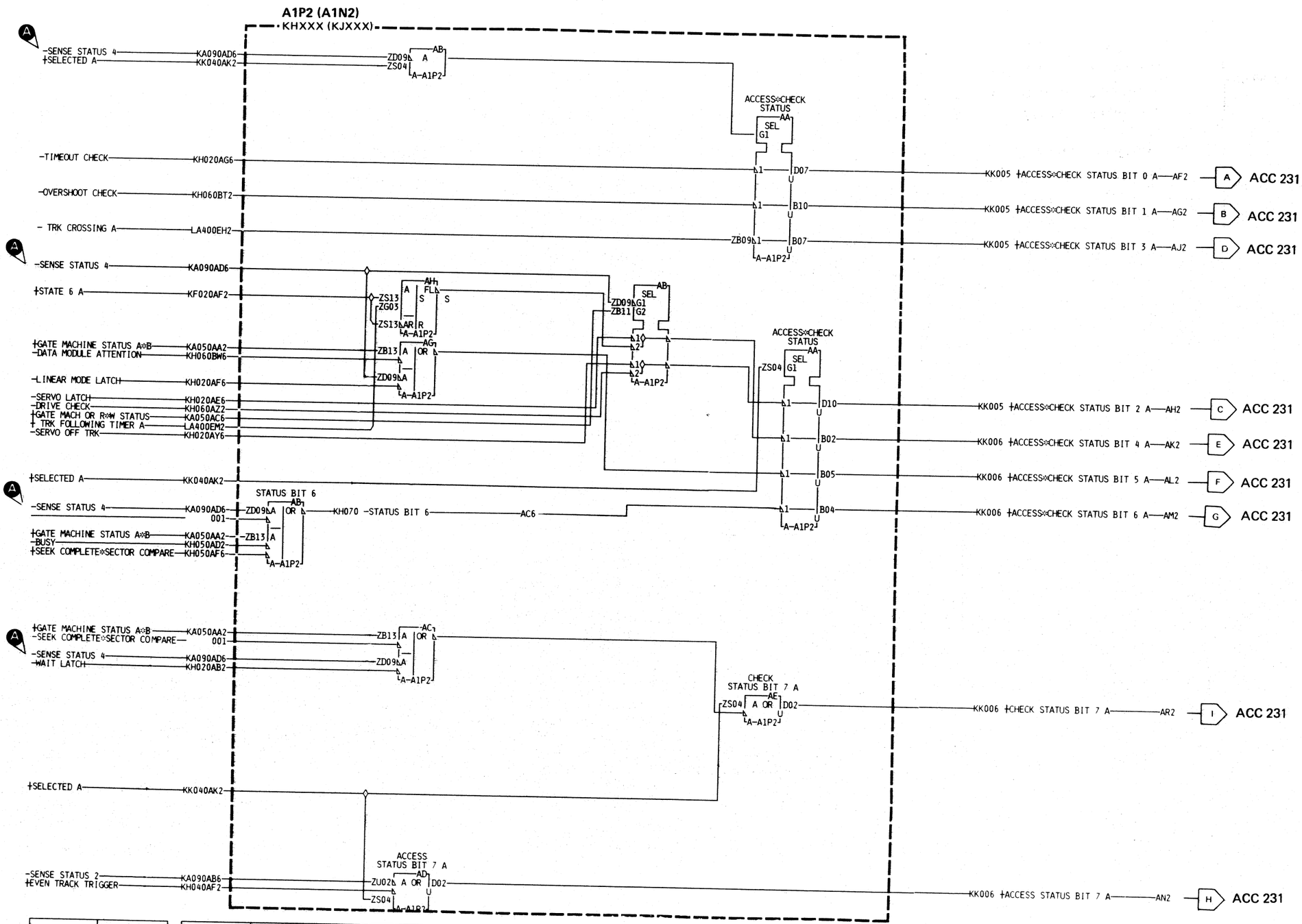


DE0230 Seq 2 of 2	2747165 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440223 15 Mar 75			

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ACCESS STATUS INTERFACE



DE0232 Seq. 1 of 2	2747166 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73				

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ACCESS CONTROL SENSE INTERFACE – CIRCUIT DESCRIPTION

Format 1, Sense Byte 16 contains Access Control Sense information. The information is gated to the interface by –SENSE STATUS 4 (A)

SENSE BYTE 16 – BIT SUMMARY

Bit 0 Access Timeout Check (ACC 111)
An Access operation (Seek or Rezero was not completed within 180 milliseconds.

Bit 1 Access Overshoot Check (ACC 121)
During a Seek or Rezero operation, one of the following events caused a Drive Check:

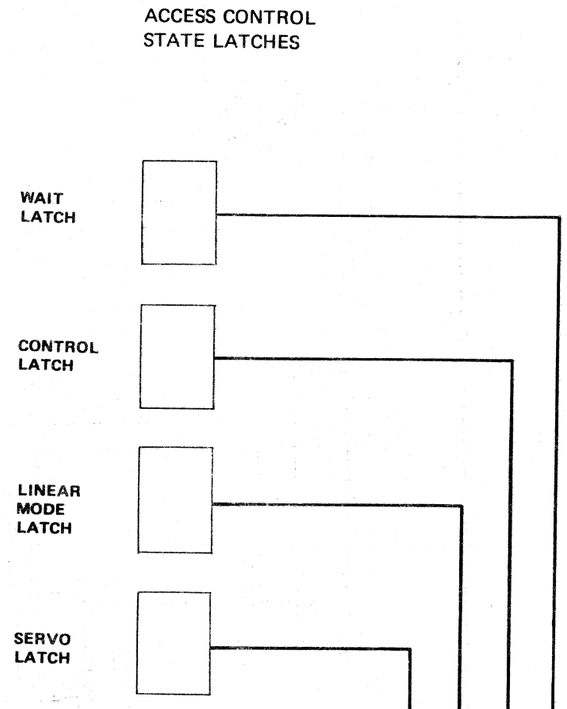
a. Three track crossing pulses were detected after the Difference Counter decremented to zero.
b. Three track crossing pulses were detected after the Access Control advanced to Linear Mode.
c. A Seek operation moved the carriage into inner or outer crash stop.

Bit 2 Servo Off Track Check (ACC 131)
The servo is not 'On Track' and Track Following while "Set Read * Write" is active.

Bit 3 Track Crossing Latch (ACC 460)
Used by microdiagnostics to count track crossings during Seek operations or Rezero operations.

Bit 4 Servo Latch
Bit 5 Linear Mode Latch
Bit 6 Control Latch
Bit 7 Wait Latch

} These bits indicate the "current state" of the Access Control. Depending on which latch(s) is(are) on, the Access Control may be in any one of these states:



0	0	0	0	=	State 1	Wait State	} Reset (ACC 400)
0	0	0	0	=	State 0	Move Out	} Rezero Op. (ACC 400)
0	0	1	0	=	State 2	Move In	
0	1	1	0	=	State 6	Linear Mode	
1	1	1	0	=	State E	On Track	
1	0	1	0	=	State A	Accelerate	} Seek Op. (ACC 600)
1	0	0	0	=	State 8	Decelerate	
1	1	0	0	=	State C	Linear Mode	
1	1	1	0	=	State E	On Track	

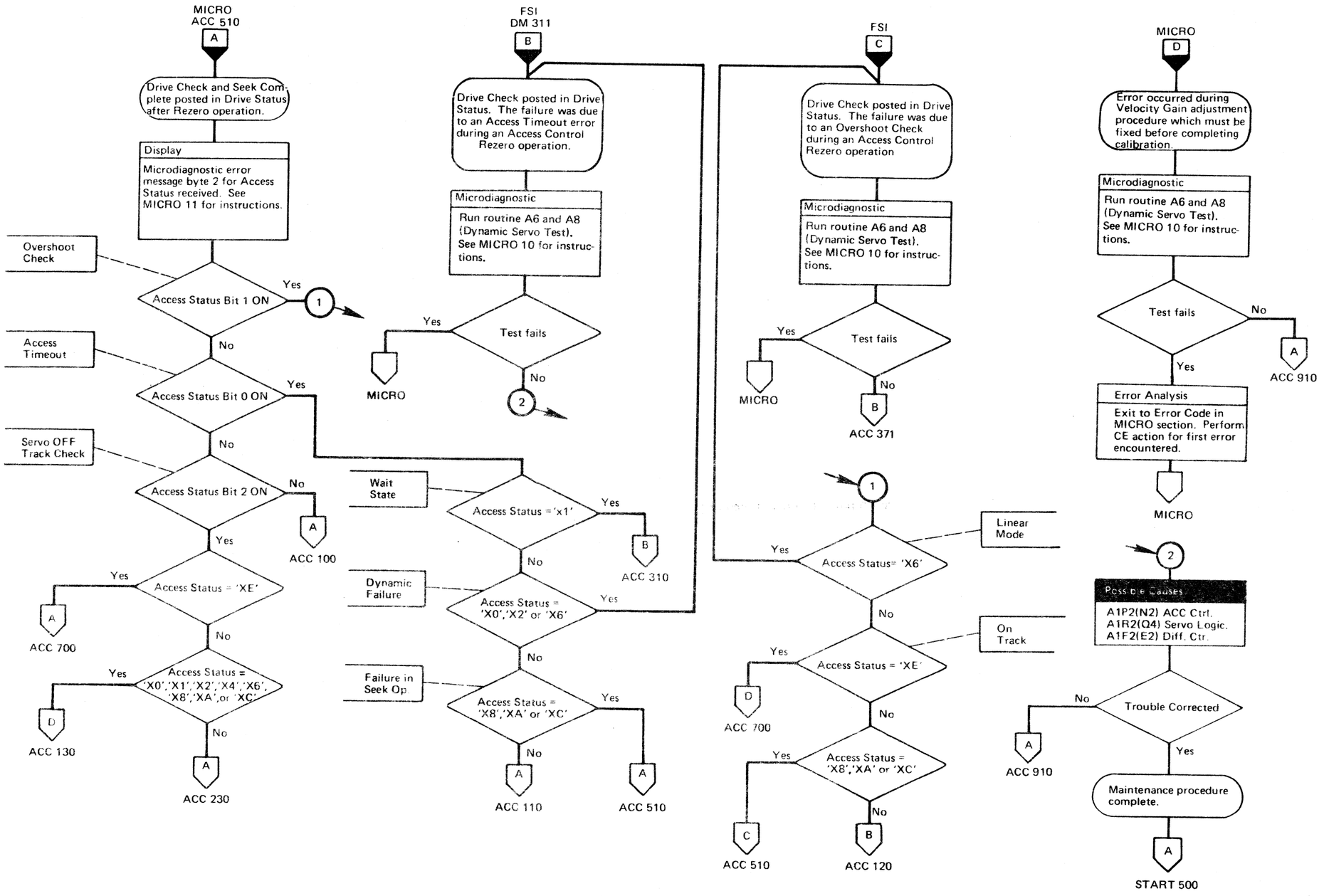
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REZERO–INITIAL ANALYSIS

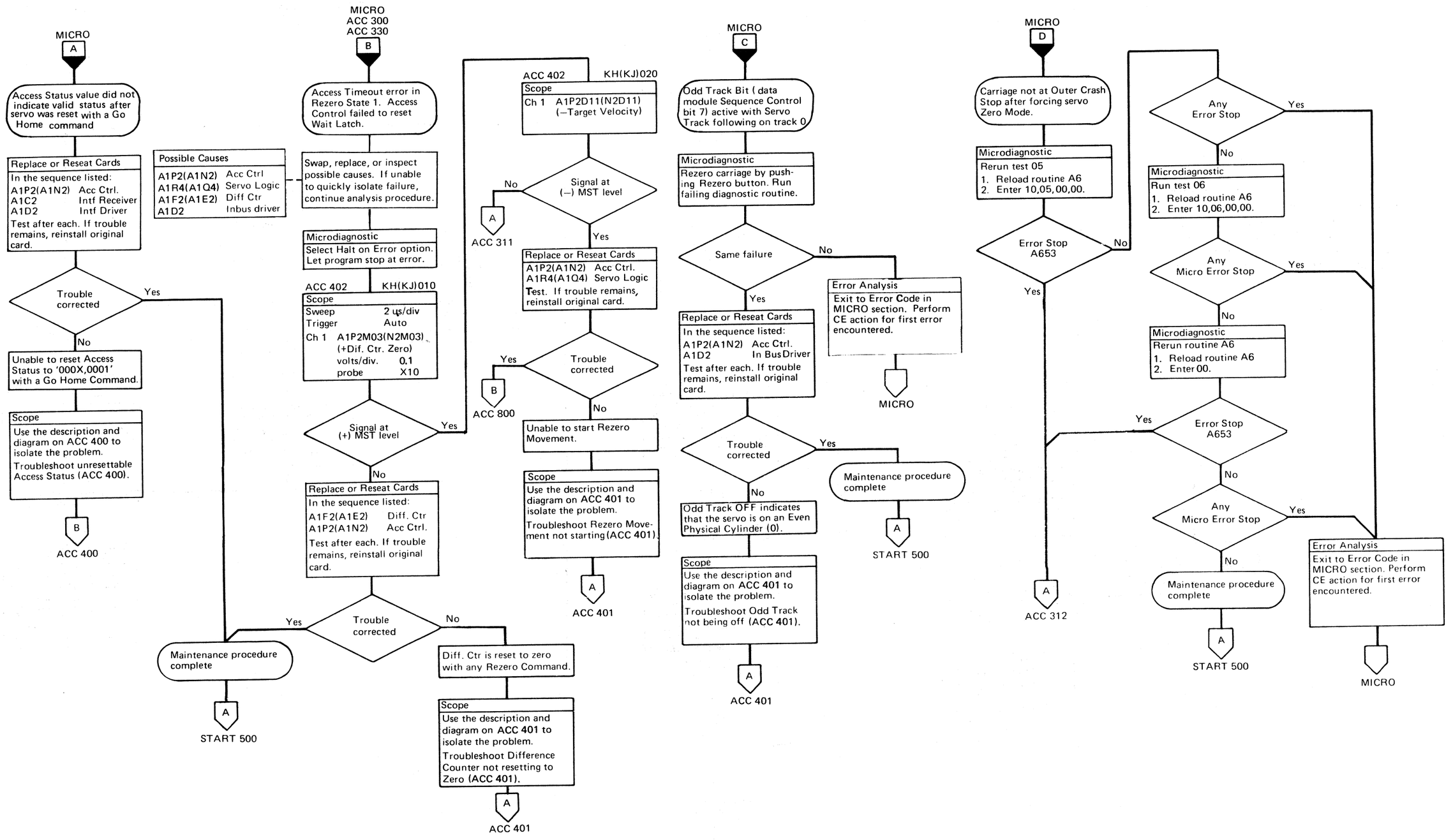


DE0300	2747168
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440205	440214	440223	
25 Jun 73	7 Sept 73	2 Nov 73	28 Jan 74	17 Jan 74	14 Mar 75	

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REZERO–RESET AND INITIAL CONDITIONS

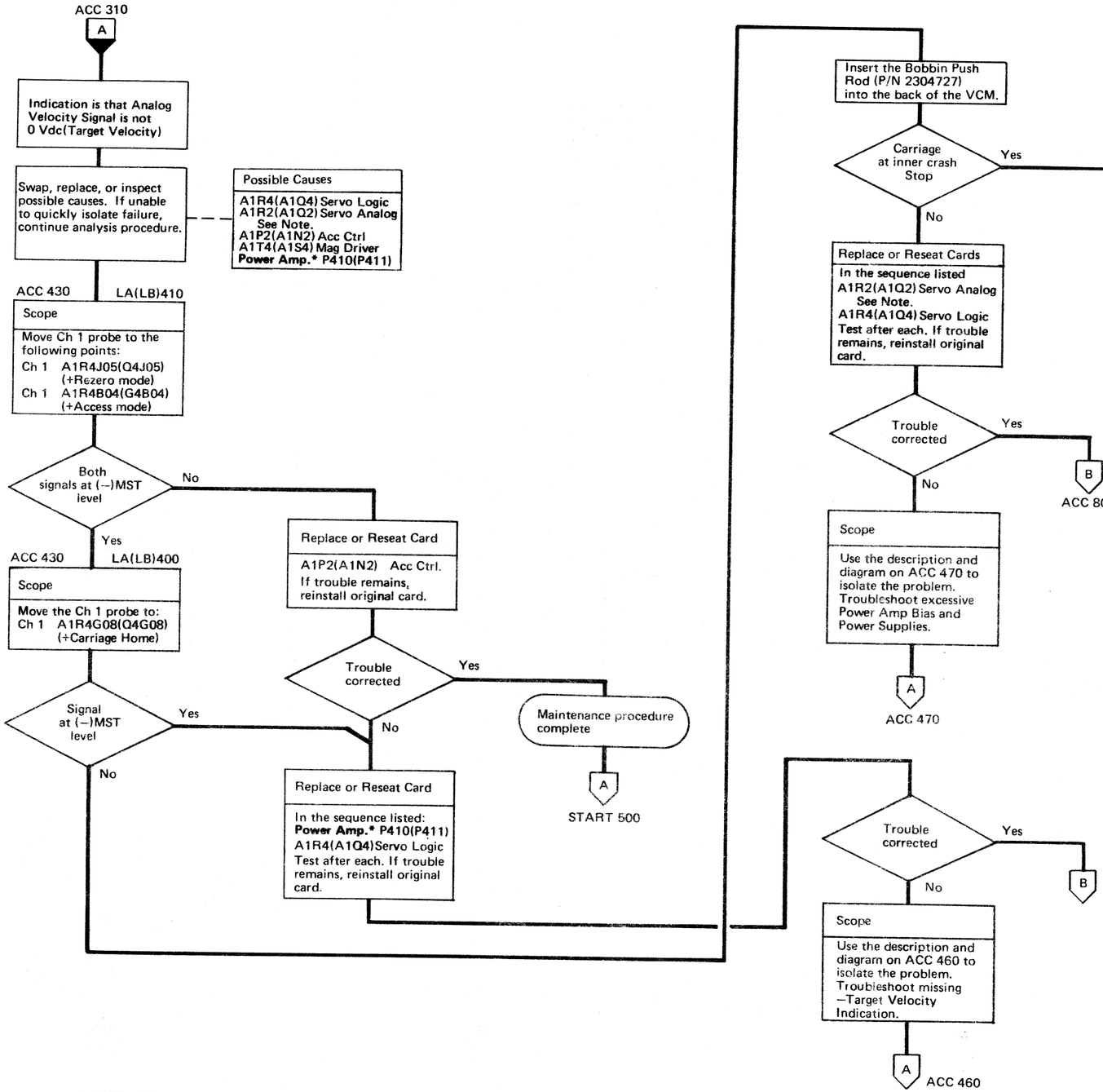


DE0310	2747167
Seq. 1 of 2	Part No. ( )

See	440218	440223				
EC History	5 Aug 74	14 Mar 75				

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REZERO–RESET AND INITIAL CONDITIONS



Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

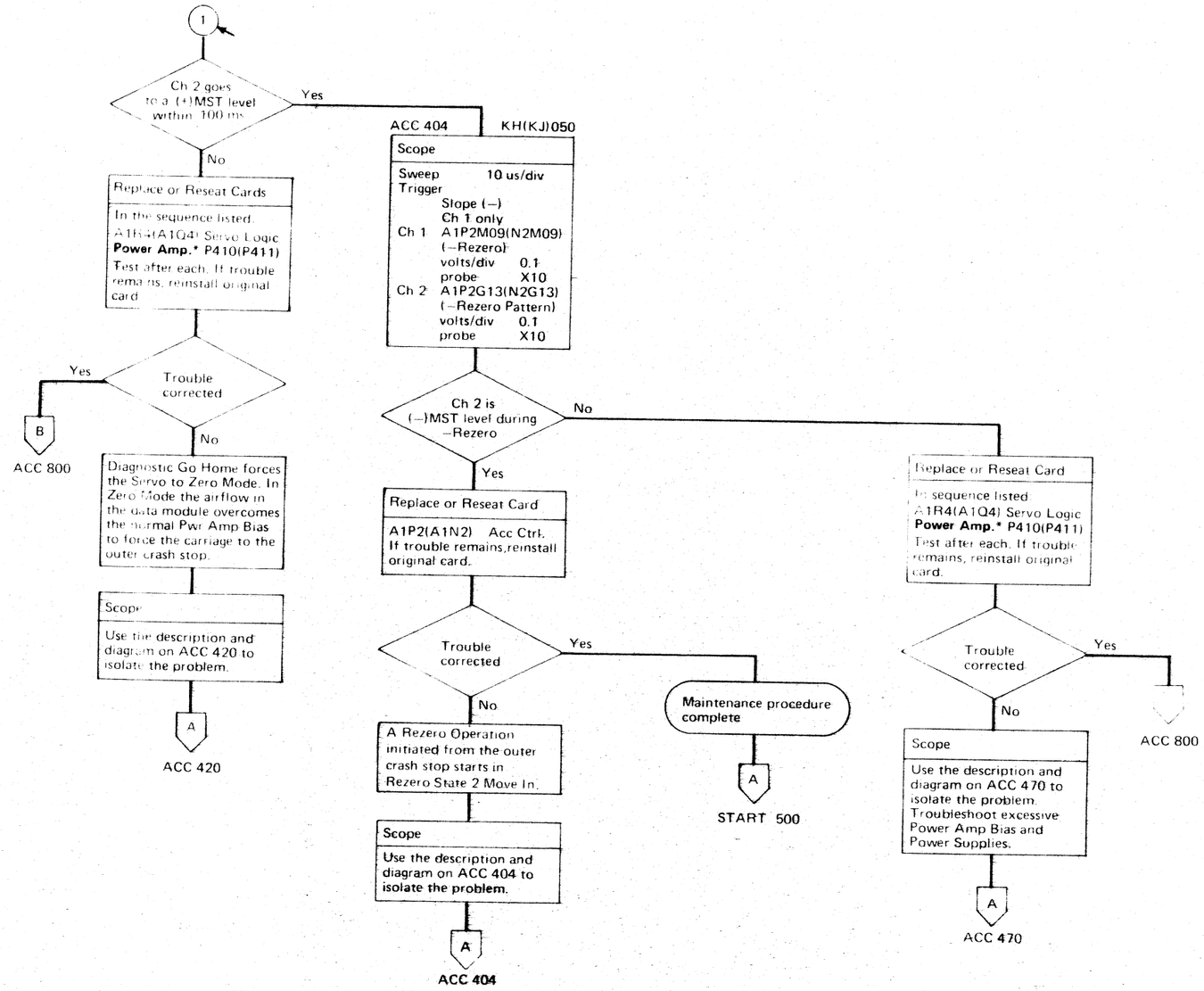
**See LOC 2 for P410(P411).*

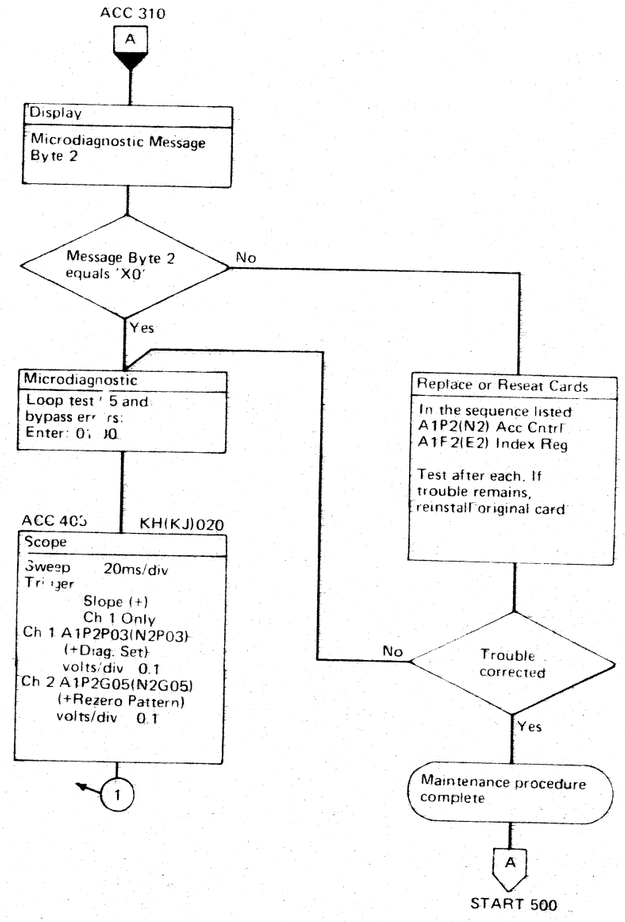
DE0310	2747167
Seq. 2 of 2	Part No. ( )

See	440218	440223				
EC History	5 Aug 74	14 Mar 75				

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REZERO – RESET AND INITIAL CONDITIONS





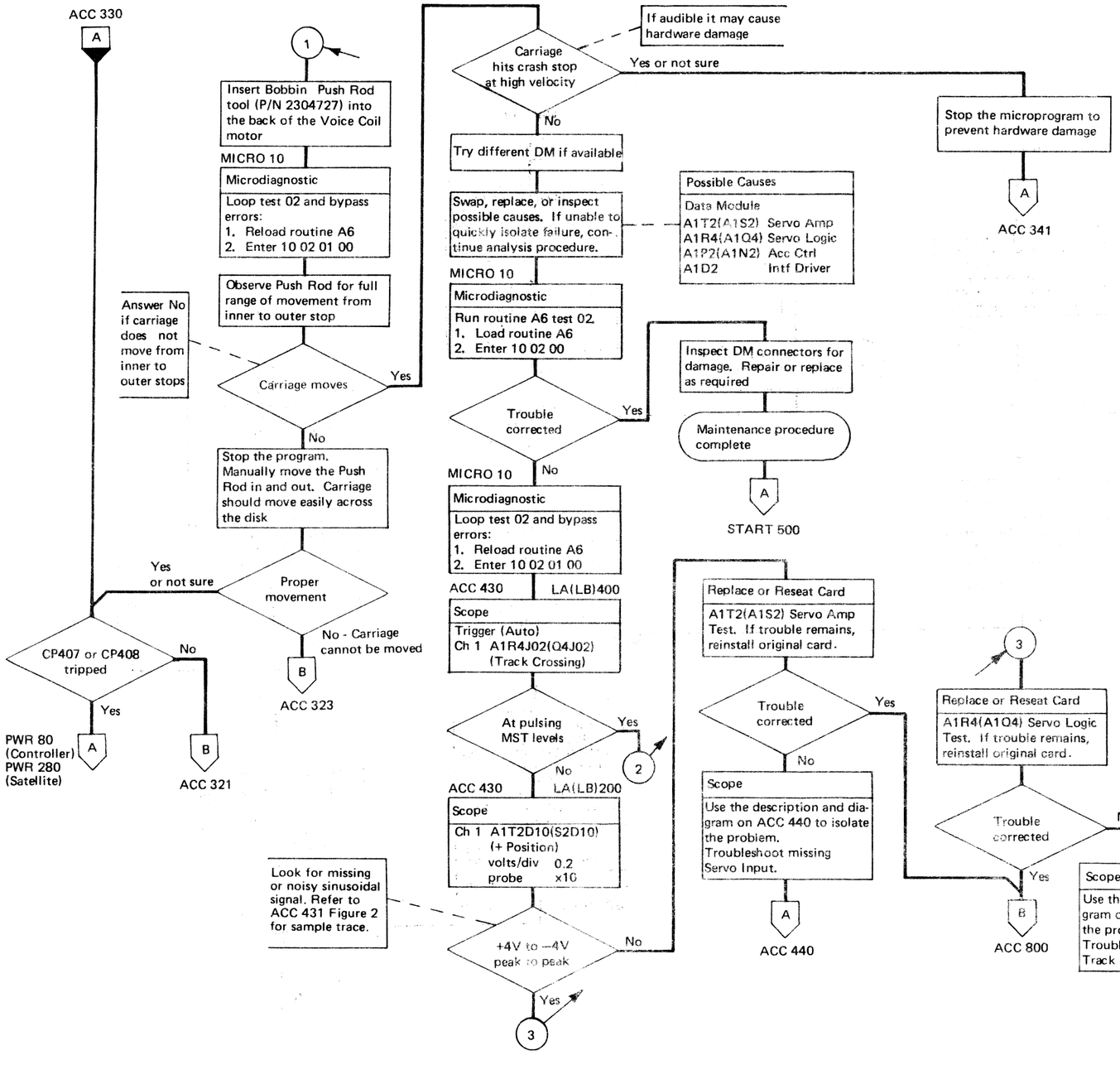
See LOC 2 for P410(P411).

DE0312	2747169
Srq 1 of 2	Part No ( )

440200	440202	440203	440209	440214	440223	
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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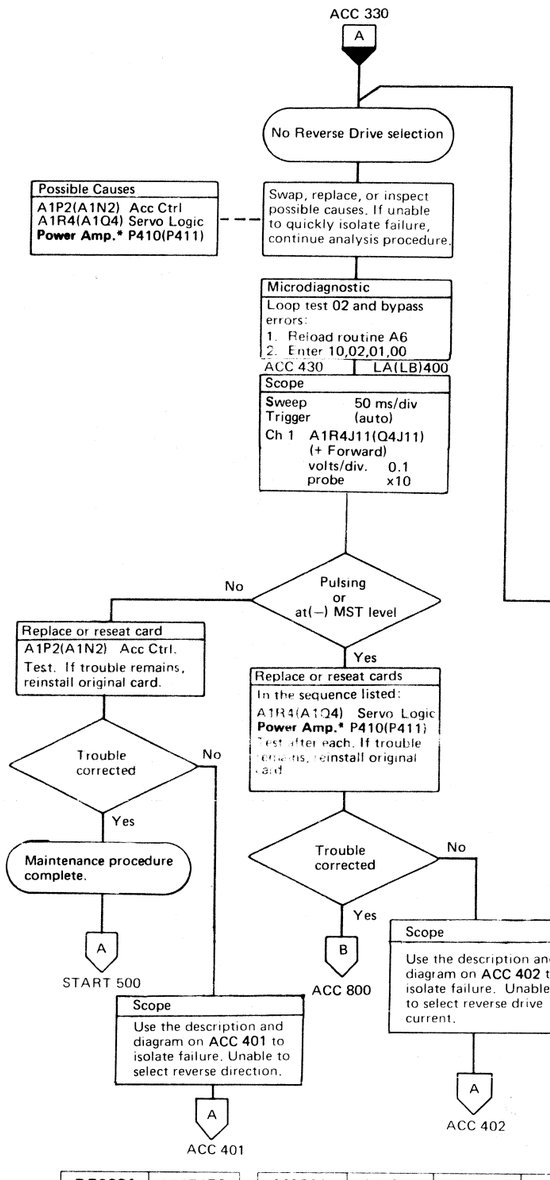
REZERO–CARRIAGE MOVEMENT DETECTION

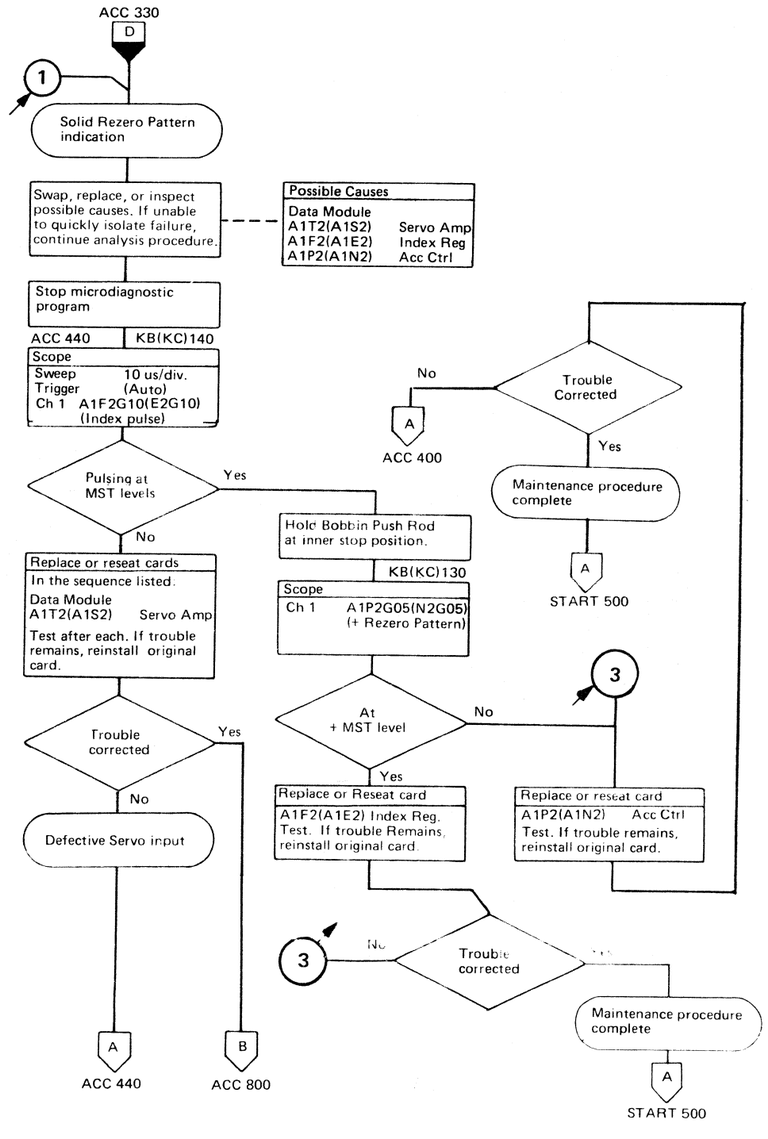


Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

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REZERO–CARRIAGE MOVEMENT DETECTION

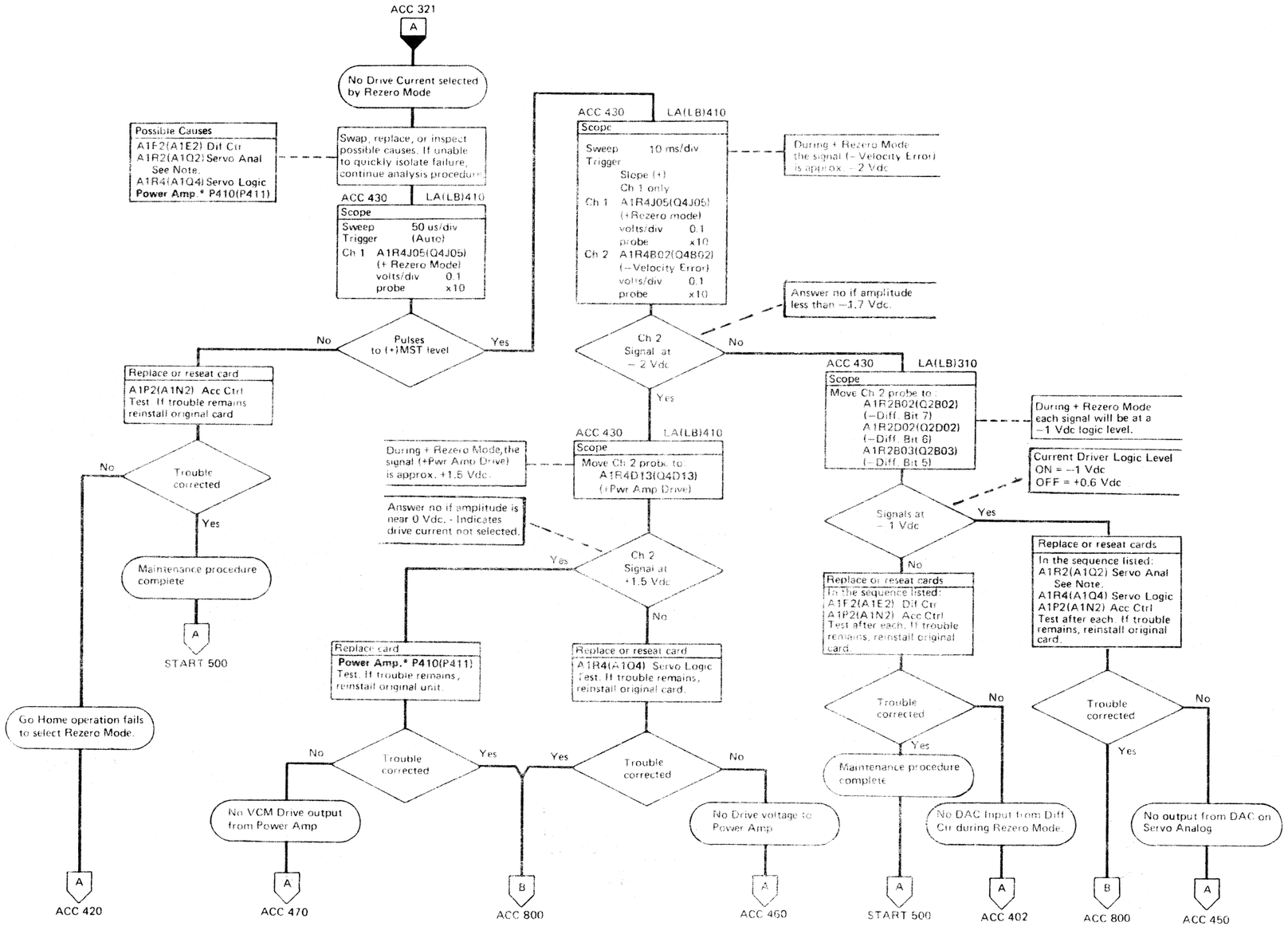




3340	DE0321	2747170	440200	440202	440203	440209	440214	440223	
	Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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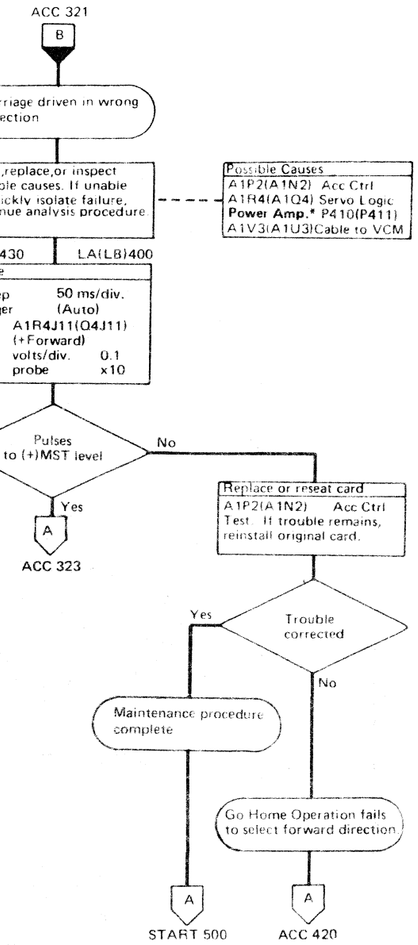
REZERO–CARRIAGE MOVEMENT DETECTION



DE0321	2747170
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440209	440214	440223
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75

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Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

**See LOC 2 for P410(P411).*

REZERO–CARRIAGE MOVEMENT DETECTION

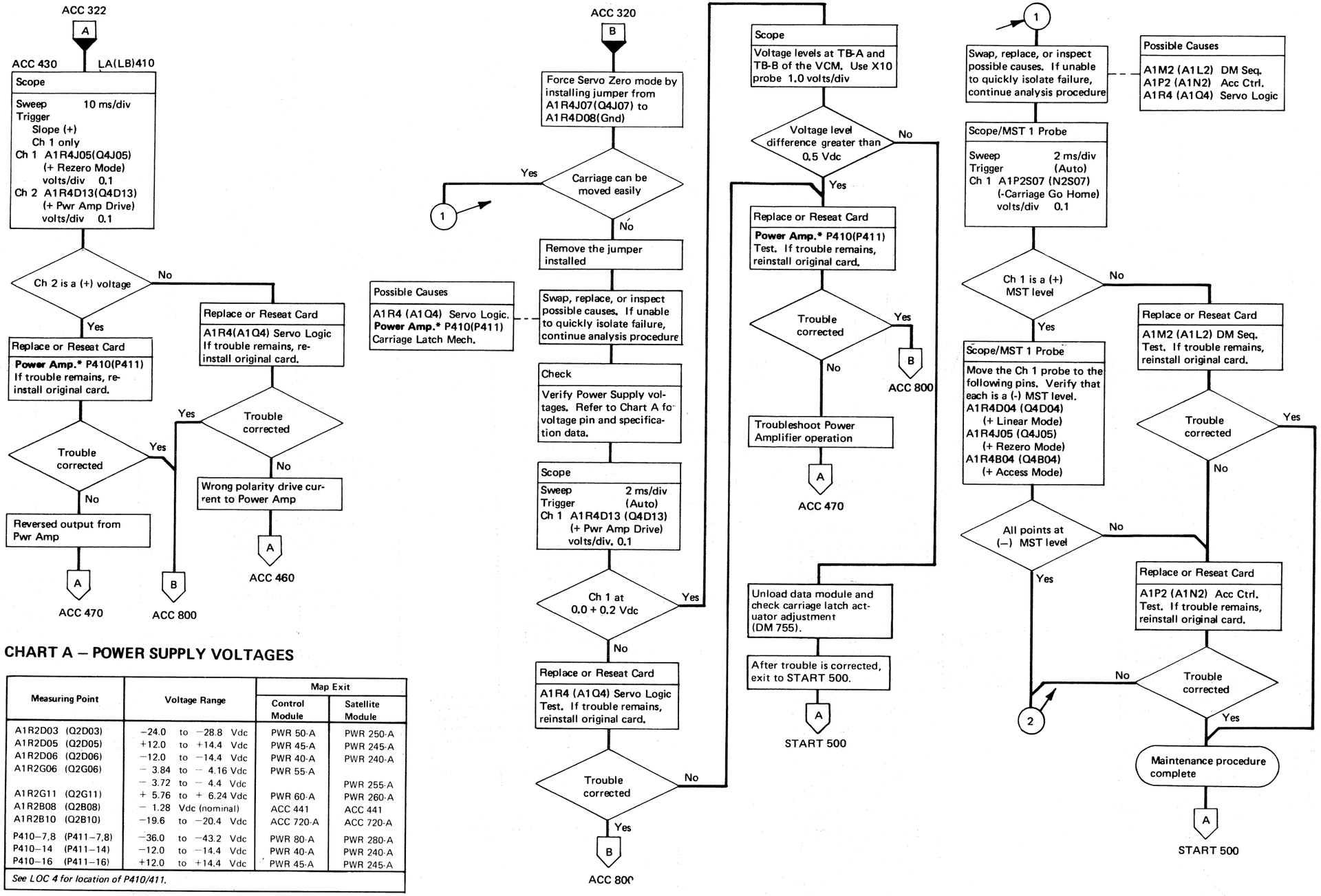


CHART A – POWER SUPPLY VOLTAGES

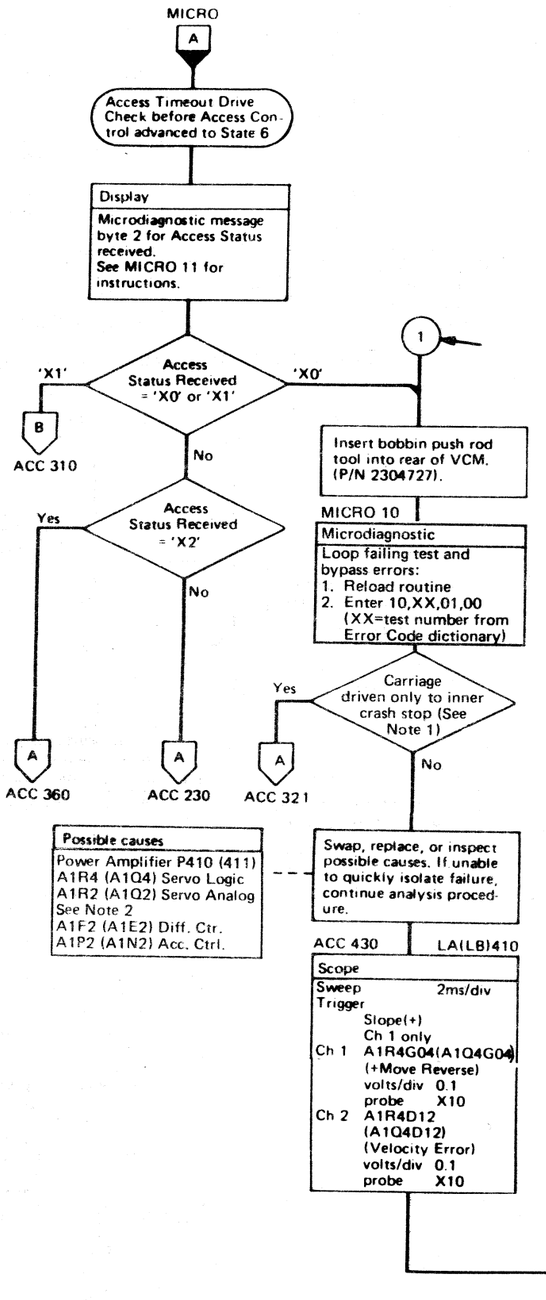
Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R2D06 (Q2D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R2G06 (Q2G06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A
A1R2B08 (Q2B08)	− 1.28 Vdc (nominal)	ACC 441	ACC 441
A1R2B10 (Q2B10)	−19.6 to −20.4 Vdc	ACC 720-A	ACC 720-A
P410–7,8 (P411–7,8)	−36.0 to −43.2 Vdc	PWR 80-A	PWR 280-A
P410–14 (P411–14)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
P410–16 (P411–16)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A

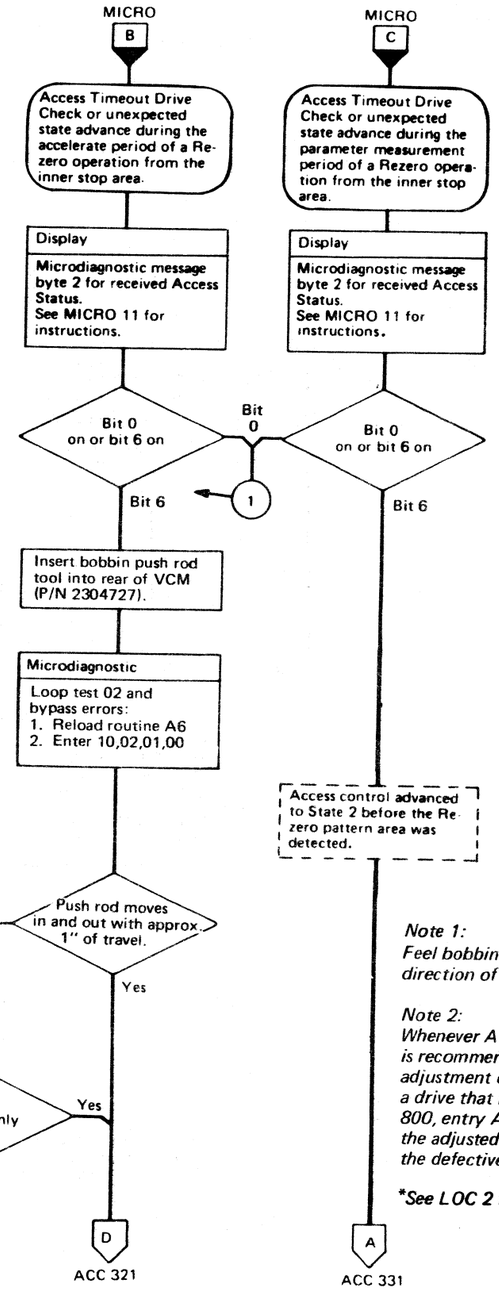
See LOC 4 for location of P410/411.

See LOC 2 for P410(P411).

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REZERO – STATE 0 TIMEOUT ERROR





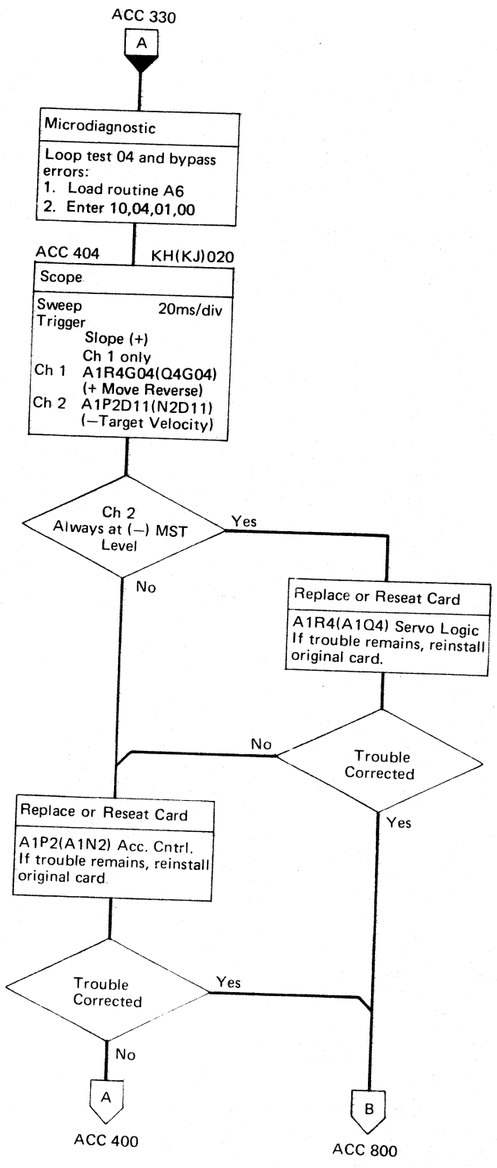
Note 1:
Feel bobbin push rod to determine direction of drive current.

Note 2:
Whenever A1R2 (A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then, the adjusted card may be installed in the defective drive.

See LOC 2 for P410(P411).

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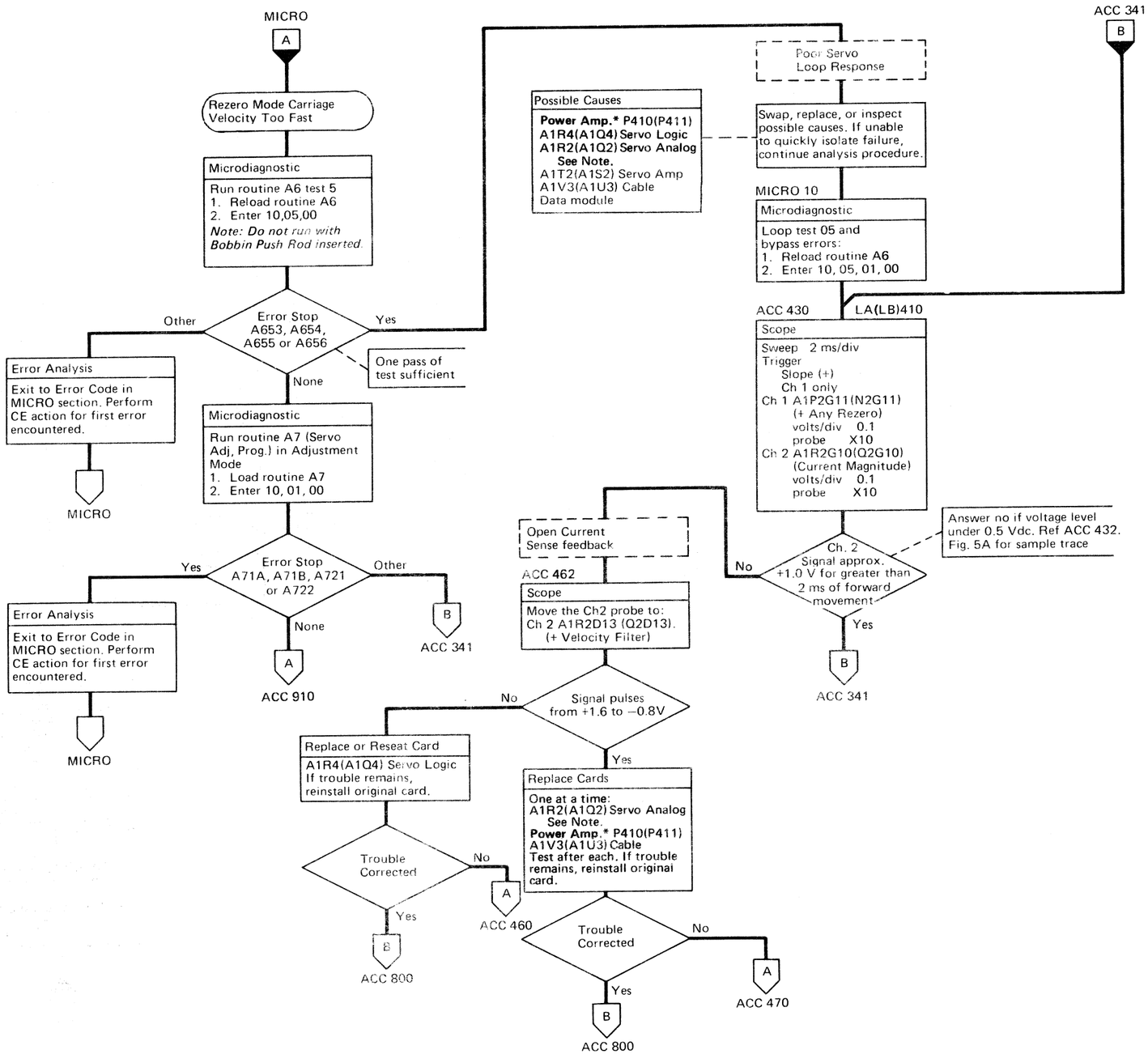
REZERO – STATE 0 TIMEOUT ERROR



DE0330	2747172	440200	440202	440203	440209	440214	440223	
Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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REZERO OPEN SERVO LOOP



Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

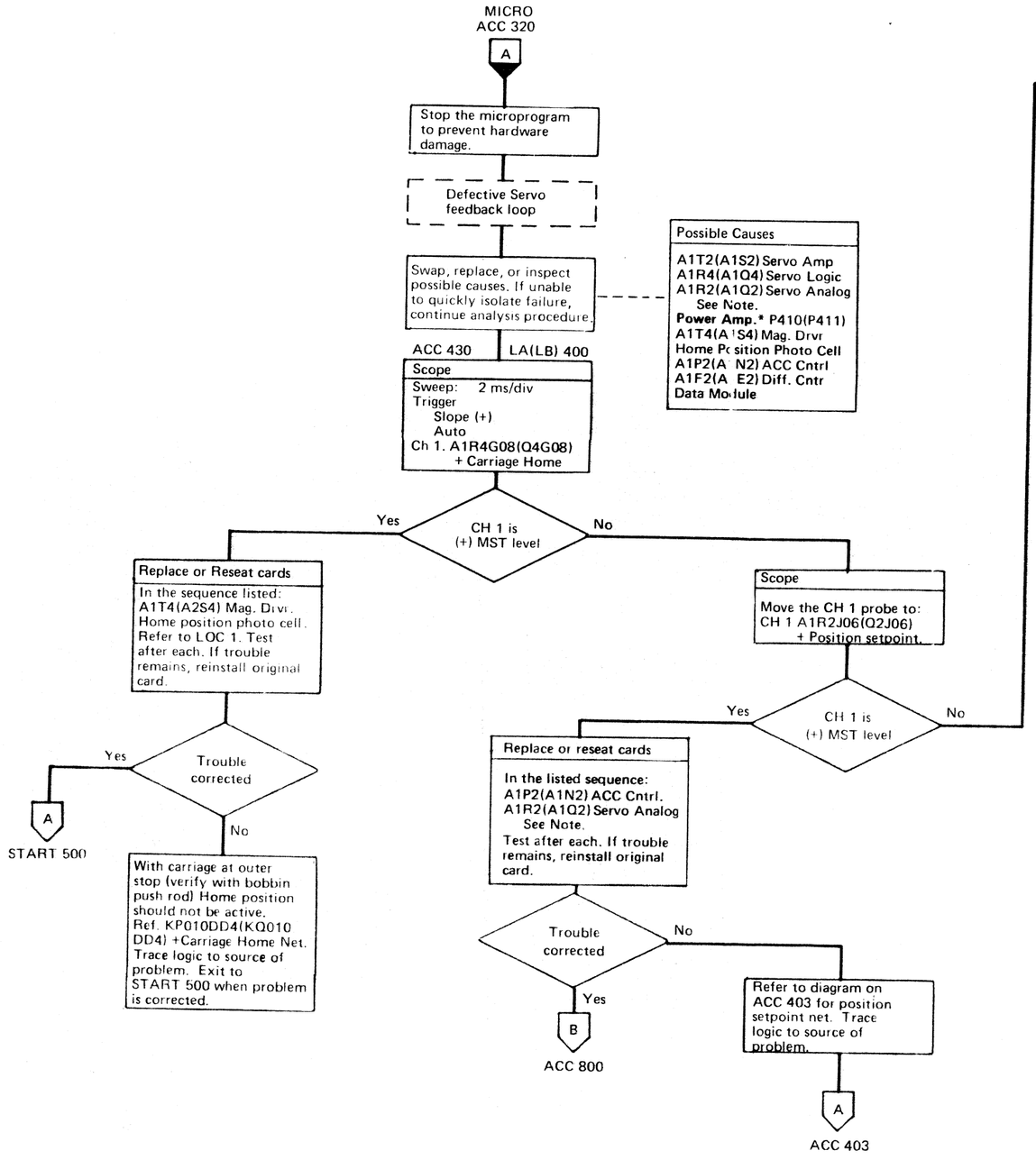
**See LOC 2 for P410(P411).*

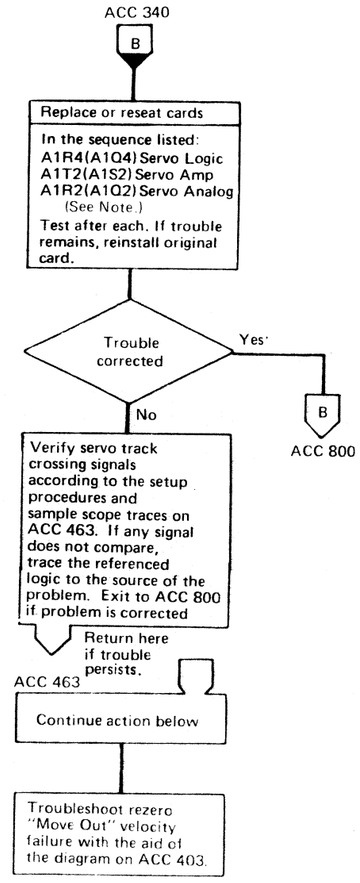
DE0330 Seq. 2 of 2	2747172 Part No. ( )

440200	440202	440203	440209	440214	440223	
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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REZERO OPEN SERVO LOOP





Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

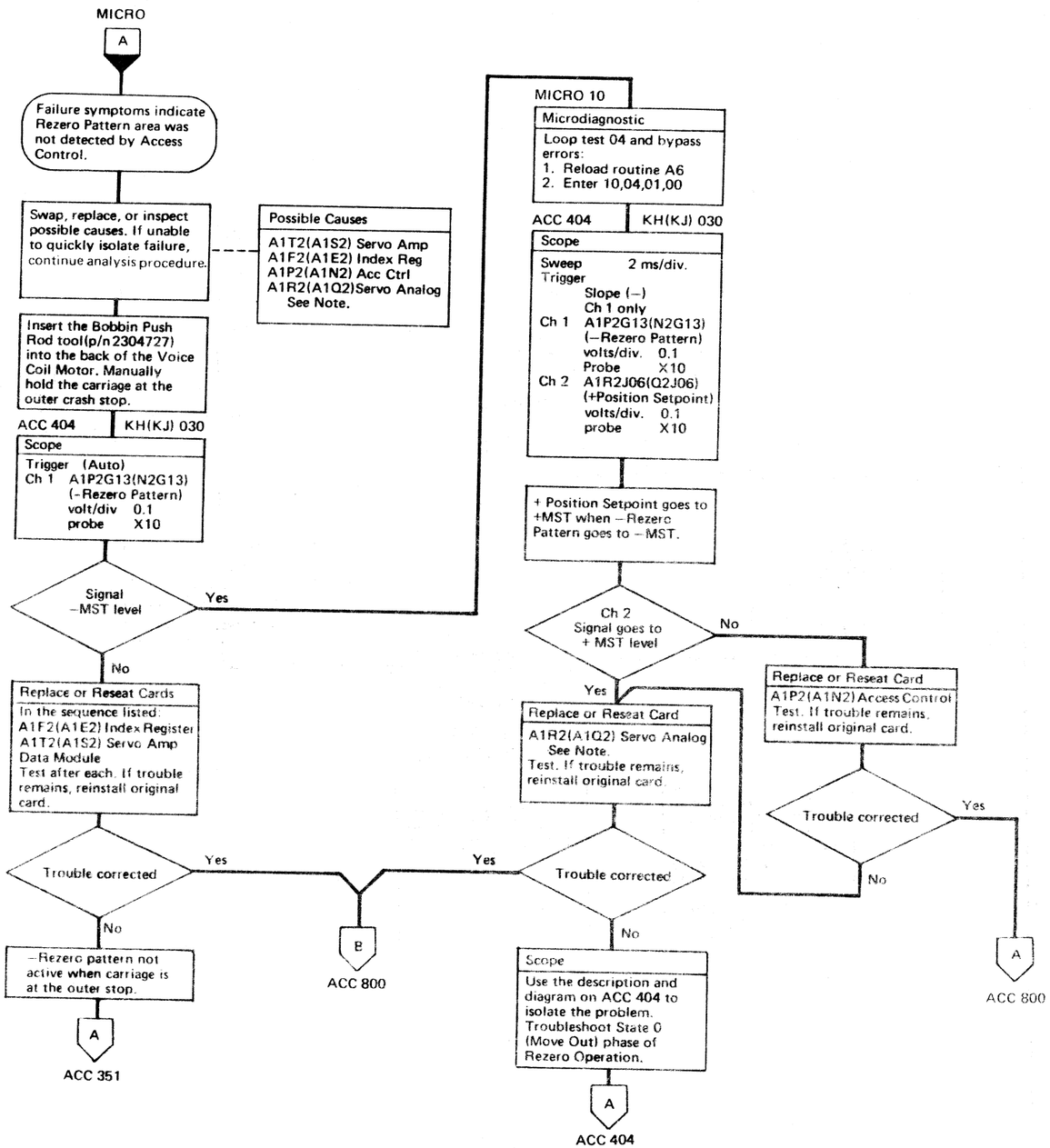
**See LOC 2 for P410(P411).*

DE0340	2747173	440200	440202	440203	440209	440214	440218	440223
Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	5 Aug 74	14 Mar 75

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REZERO – STATE 0 PATTERN DETECTION

REZERO – STATE 0 PATTERN DETECTION



Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

DE0340	2747173
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440209	440214	440218	440223
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	5 Aug 74	14 Mar 75

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REZERO PATTERN DETECTION DIAGRAM

ACC 350

A

Rezero Pattern Area not detected

Error Analysis

Verify Servo Amp. and Data Module operation according to the procedure on ACC 440.

A

ACC 440

Return here if trouble persists

Continue action below

Insert the Bobbin Push Rod into the VCM and manually hold the Carriage at the outer crash stop.

Check

Verify Index Register Operation:

1. —Rezero Pattern flip latch ❶ is set on by a '0 1 0 1 0' Index pattern that is decoded continuously when the Servo head is in the Rezero Pattern Area.
2. —Rezero Pattern flip latch is reset by a '0 0 0 0 1' pattern decoded from the Index register.
3. +Servo Clock ❷ gates the register deocde to set or reset the Rezero Pattern flip latch.
4. +Sector Count Pulse ❸ shifts Index Bit data ❹ through the Index register.
5. Trace logic to source of problem.

Repair or replace as required.

Trouble corrected

No

Yes

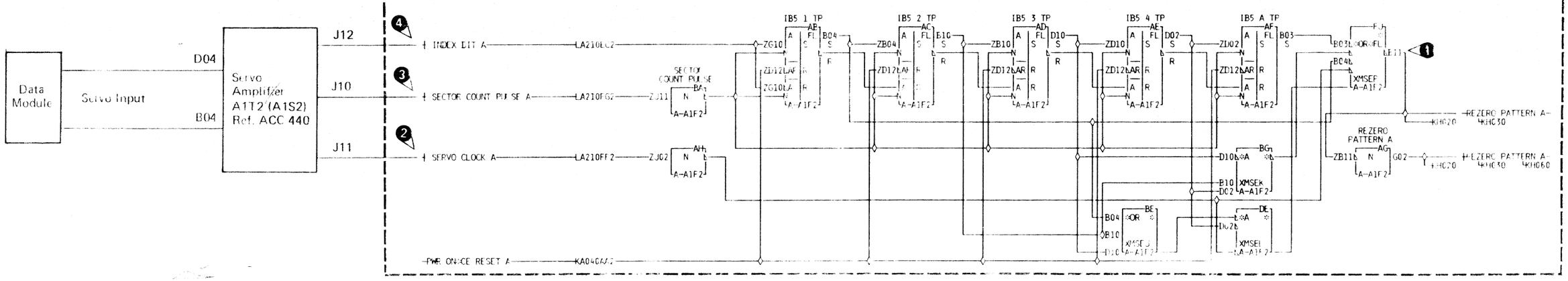
A

ACC 910

B

ACC 800

A1F2 (A1E2)
KBXXX (KCXXX)



REZERO – STATE 2 ACCESS TIMEOUT ERROR

ACC 330
MICRO
A

Access Timeout error during Access Control State 2 (Move In) of a Rezero Operation.

Possible Causes
A1P2(A1N2) Acc Ctrl.
A1R4(A1Q4) Servo Logic
A1T2(A1S2) Servo Amp

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure.

Microdiagnostic
Loop test 05 and bypass errors:
1. Reload routine A6
2. Enter 10,05,01,00

ACC 405 KH(KJ)030
Scope
Sweep 10 us/div
Trigger
Slope (–)
Ch 1 only
Ch 1 A1P2M09(N2M09)
(–Rezero)
volts/div 0.1
probe X10
Ch 2 A1P2J05(N2J05)
+Forward)
volts/div 0.1
probe X10

CH 2 is a (+)MST level
Yes
No

Replace or Reseat Card
A1P2(A1N2) Acc Ctrl.
If trouble remains, reinstall original card.

Trouble corrected
No
Yes
ACC 405
Maintenance procedure complete
START 500

ACC 405 KH(KJ)040
Scope
Ch 2 A1P2J10(N2J10)
(–Even Track)

CH 1 is a (–)MST level
Yes
No

Replace or Reseat Cards
In the sequence listed:
A1P2(A1N2) Acc Ctrl.
A1T2(A1S2) Servo Amp.
Test after each. If trouble remains, reinstall original card.

Trouble corrected
Yes
No
B
ACC 800

–Even Track should be set to a (–)MST level during a Rezero operation.
A
ACC 405

ACC 440 LA(LB)210
Scope
Sweep 1 us/div
Trigger Slope (+)
A1T2J11(S2J11)
(+Servo Clock)
Ch 1 A1T2J02(S2J02)
(+ Gate 1)
volts/div 0.1
probe X10
Ch 2 A1T2J06(S2J06)
(+ Gate 2)
volts/div 0.1
probe X10

+Gate 1 and +Gate 2 should be in the sequence indicated by Figure 1.

Sequence correct
Yes
No

Replace or Reseat Card
A1T2(A1S2) Servo Amp.
If trouble remains,reinstall original card.

Trouble corrected
Yes
No
B
ACC 800

Troubleshoot wrong sequence of Gate 1 and Gate 2.
A
ACC 440

ACC 405 KH(KJ)030
Scope
Sweep 100 us/div
Trigger
Slope (–)
Ch 1 only
Ch 1 A1P2M09(N2M09)
(–Rezero)
volts/div 0.1
probe X10
Ch 2 A1P2J13(N2J13)
(–Pos.Coarse Track)
volts/div 0.1
probe X10

Ch 2 is a (–)MST level pulsing to a (+)MST level
No
Yes

Replace or Reseat Card
A1P2(A1N2) Acc Ctrl.
If trouble remains,reinstall original card.

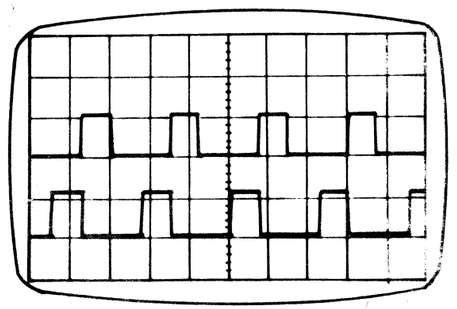
Trouble corrected
Yes
No
A
ACC 400

Maintenance procedure complete
A
START 500

Replace or Reseat Card
A1R4(A1Q4) Servo Logic
If trouble remains,reinstall original card.

Trouble corrected
No
Yes
B
ACC 800

Fig. 1 Gate Timing



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REZERO–STATE 2 CAPTURE VELOCITY

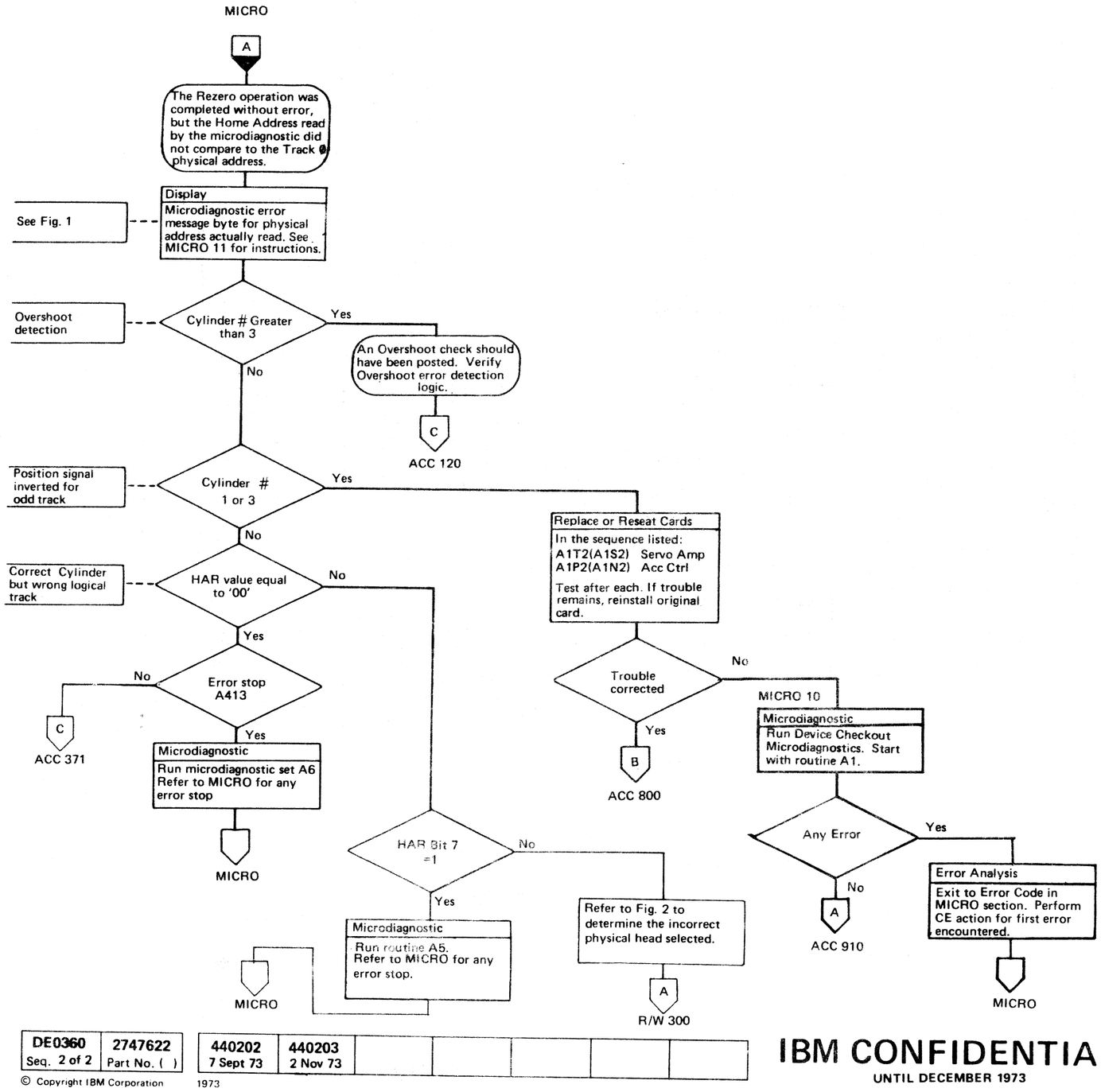


Fig. 1 Physical Address Bytes

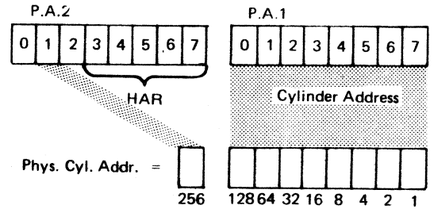


Fig. 2 HAR Conversion Chart

P.A.2: 0 1 2 3 4 5 6 7

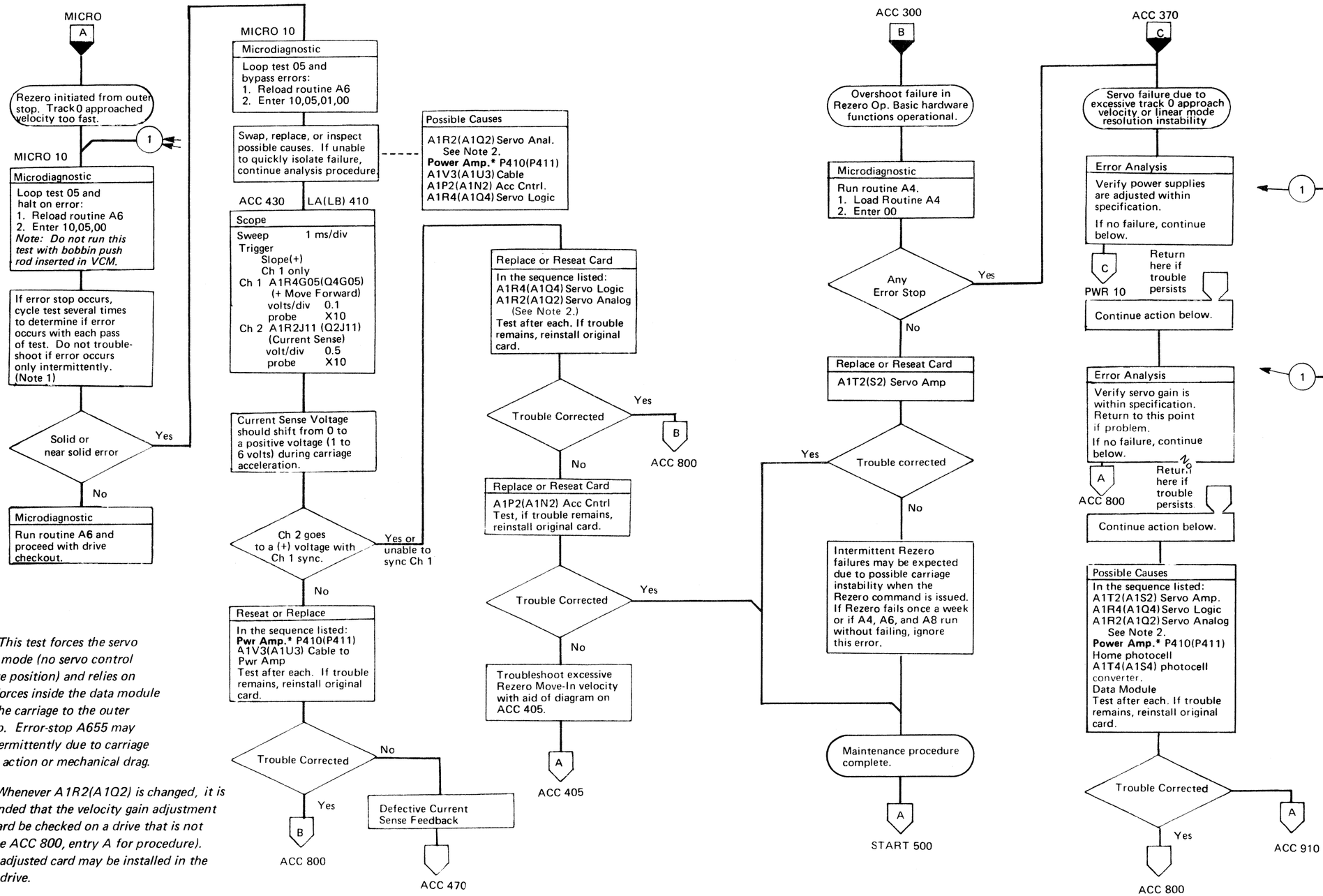
HAR	PHYS HEAD	INDEX
00	0	Even
01	0	Odd
02	1	Even
03	1	Odd
04	2	Even
05	2	Odd
06	3	Even
07	3	Odd
08	4	Even
09	4	Odd
0A	5	Even
0B	5	Odd
0C	6*	Even
0D	6*	Odd
0E	7*	Even
0F	7*	Odd
10	8*	Even
11	8*	Odd
12	9*	Even
13	9*	Odd
14	10*	Even
15	10*	Odd
16	11*	Even
17	11*	Odd

* 70 MB Data Module Only

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REZERO – STATE 2 CAPTURE VELOCITY



Note 1: This test forces the servo into zero mode (no servo control of carriage position) and relies on air-flow forces inside the data module to push the carriage to the outer crash-stop. Error-stop A655 may occur intermittently due to carriage bouncing action or mechanical drag.

Note 2: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

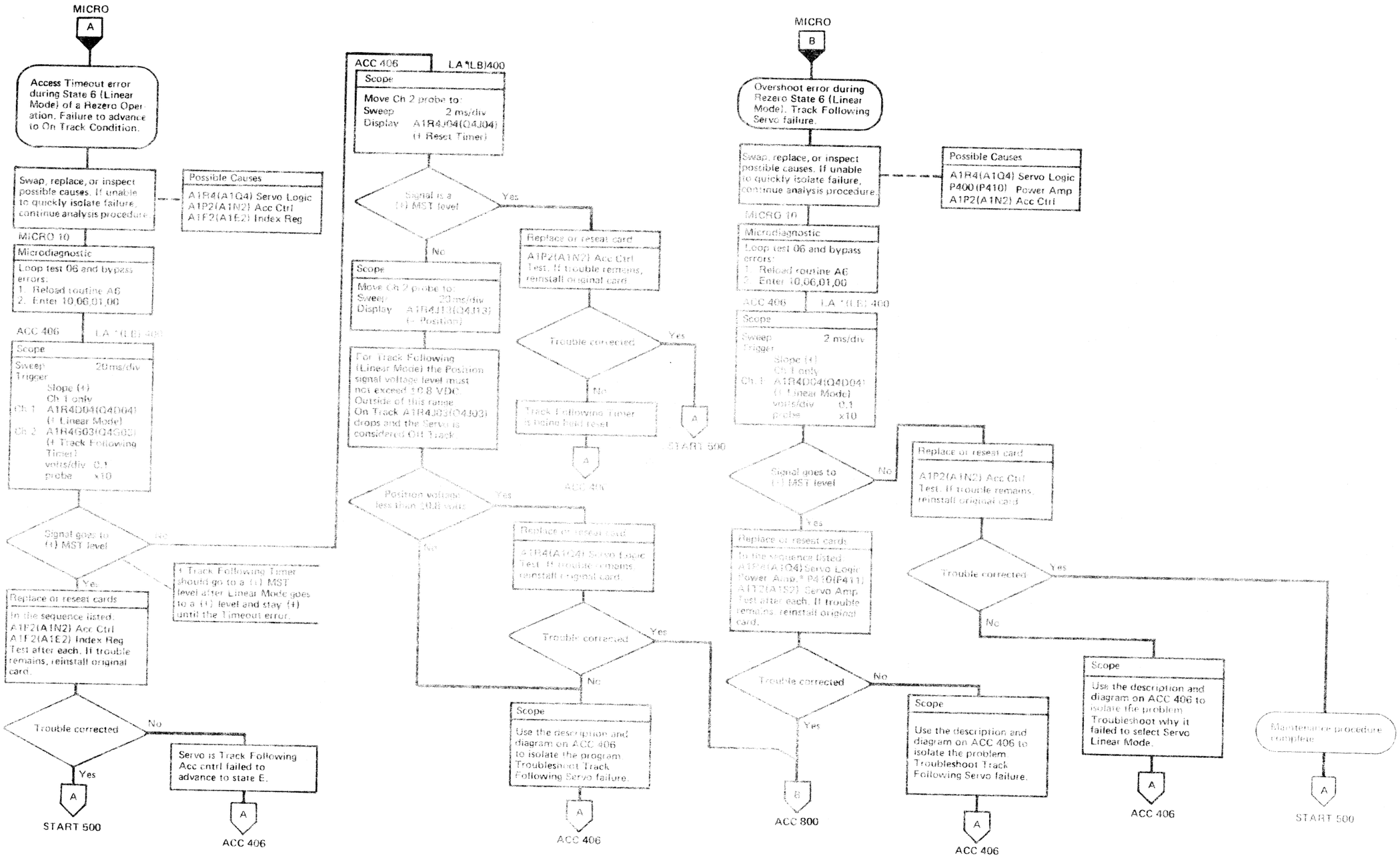
*See LOC 2 for P410(P411).

DE0370	2747175
Seq. 1 of 2	Part No. ( )

440200	440202	440203	440204	440209	440214	440223
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	25 Mar 74	17 Jun 74	14 Mar 75

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REZERO–STATE 6 ACCESS ERROR



*See LOC 2 for P410(P411).

DE0370	2747175
Seq. 2 of 2	Part No. ( )

440200	400200	440203	440204	440209	440214	440223
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	25 Mar 74	17 Jun 74	14 Mar 75

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BOBBIN BIAS

DM 110
DM 170
DM 350
MICRO

A

Data module load or unload failure caused by one of the following:
- No Bobbin Bias current to VCM
- Reversed Bobbin Bias current to VCM
- Open Home Position detector

DM Load or Unload Failure

Unload the data module. Do not force it if it is stuck.

DM unloaded? — Yes

No

Insert the Bobbin Push Rod into the back of VCM (P/N 2304727).

Push the carriage to the Home Position (inner crash stop) and hold.

Carriage can be forced Home? — No

Yes

Operate CE Reset. DM should unload.

DM unloads? — No

Yes

Turn drive ac power off. (See Note.)

Push the carriage to the Home Position and manually unload DM with unload tool (3/16" Allen wrench).

Refer to DM 500 for more detailed information on removal.

Turn drive ac power on.

DO NOT proceed beyond this point if data module has not been removed from drive.

Error Analysis

Verify drive voltages as shown. Refer to PWR 10, Entry C for any voltage problem.

1

Note: For Satellite Module, turn Off CB202 (See LOC 12). Do not unload data module.

POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit: Control Module	Map Exit: Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R2D06 (Q2D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R2G06 (Q2G06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A
A1R2B08 (A2B08)	− 1.28 Vdc (nominal)	ACC 441	ACC 441
A1R2B10 (Q2B10)	−19.6 to −20.4 Vdc	ACC 720-A	ACC 720-A
P410−7,8 (P411−7,8)	−36.0 to −43.2 Vdc	PWR 80-A	PWR 280-A
P410−14 (P411−14)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
P410−16 (P410−16)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
P410−9,10 (P411−9,10)	Ground	YA060 (YB060)	YA060 (YB060)
P410−13 (P411−13)	Ground	YA060 (YB060)	YA060 (YB060)

1

Possible Causes
- A1P2 (A1N2)
- A1T2 (A1S2)
- A1R2 (A1Q2)
- A1R4 (A1Q4)
- A1M2 (A1L2)
- P410 (P411)
- A1F2 (A1E2)
- A1T4 (A1S4)
- Data module
- Home photocell
- VCM

Scope
Voltage levels at TB-A and TB-B of the VCM. Use X10 probe, 1.0 volts/div.

Both at equal voltage level? — Yes → A (ACC 396)

No or Pulsing

TB-A = 0 Vdc and TB-B = −40 Vdc? — No

Yes

VCM coil is open

Turn drive power off. (See Note.)

Remove TB-A and B connections to VCM

Check
Troubleshoot open coil with ohmmeter — check for loose connections to ribbon. Repair or replace as required.

Trouble corrected? — Yes → B (ACC 800)

No → A (ACC 910)

Force Servo Zero Mode by installing jumper from A1R4J07 (Q4J07) to A1R4D08 (Gnd)

TB-A and TB-B at equal voltage level? — No → B (ACC 398)

Yes

Scope
Check the voltage level of the following:
A1R4B04 (Q4B04)
+ Access Mode
A1R4J05 (Q4J05)
+ Rezero Mode
A1R4D04 (Q4D04)
+ Linear Mode
Volts/div = 0.1

All at (−) MST level? — Yes

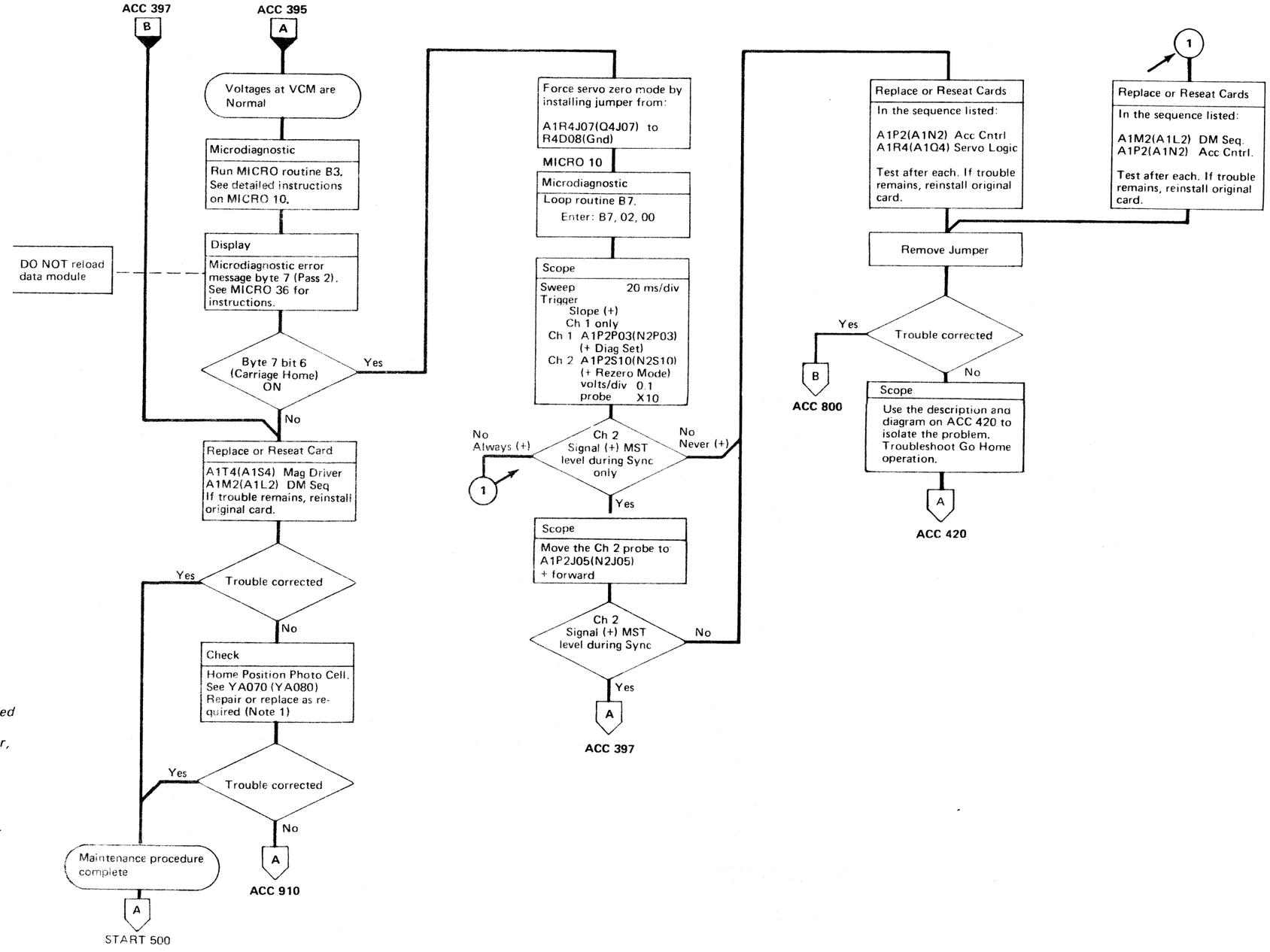
Reseat or Replace Card
A1R4 (A1Q4) Servo Logic
If trouble remains, reinstall original card.

No

Reseat or Replace Card
In sequence listed:
A1P2 (A1N2) Acc Ctrl
A1M2 (A1L2) DM Seq.
Test after each. If trouble remains, reinstall original card.

Remove jumper installed above

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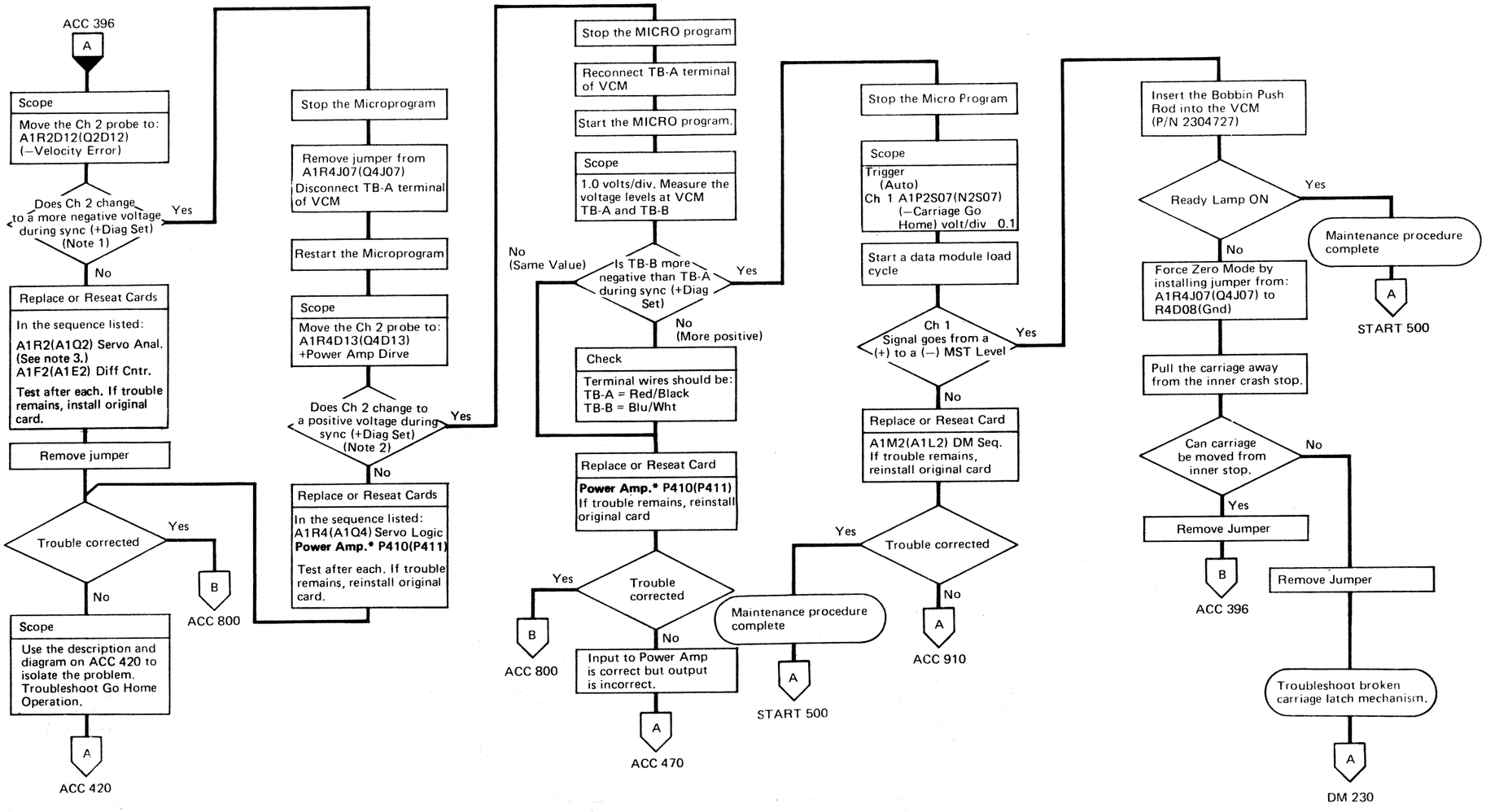
Note 1: Ensure bobbin is at home in the uncoupled position. If not in the uncoupled position, hand-cycle to loaded position, pull bobbin over coupler, then hand unload.

Voltage measurements at the photocell output may not be indicative of a good or bad device because the photocell is strictly a current device. A check can be made at the output of the photocell amplifier, A1T4J06 (A1S4J06), for good MST levels.

DE0395 Seq. 2 of 2	2747177 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440214 17 Jun 74	440223 14 Mar 75

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Note 1: Expect a change from –1.6 volts to –2.0 volts.

Note 2: Expect a change from 0 volts to +1.5 volts.

Note 3: Whenever A1R2 (A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

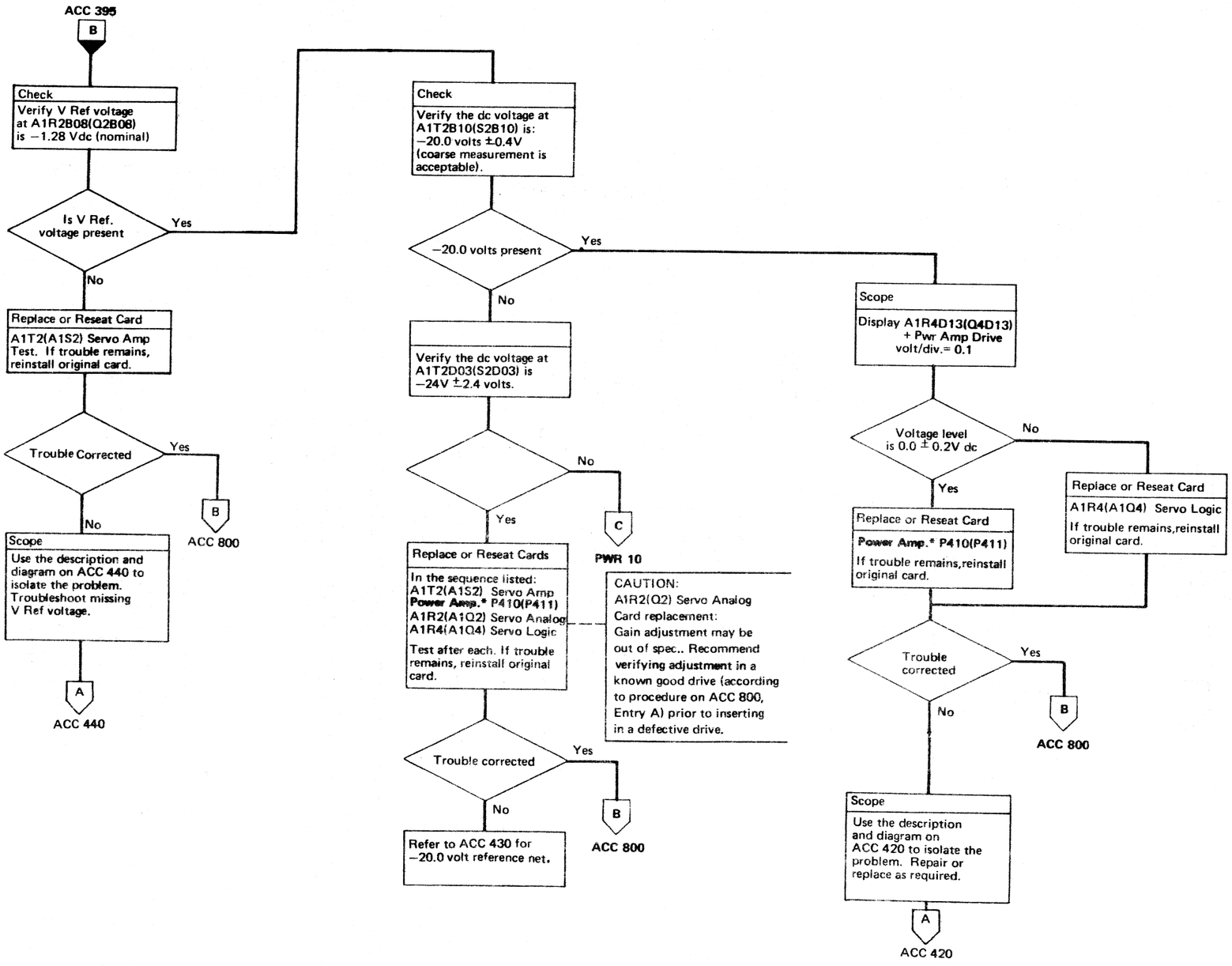
**See LOC 2 for P410(P411).*

DE0397 Seq. 1 of 2	2747178 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440223 14 Mar 75	

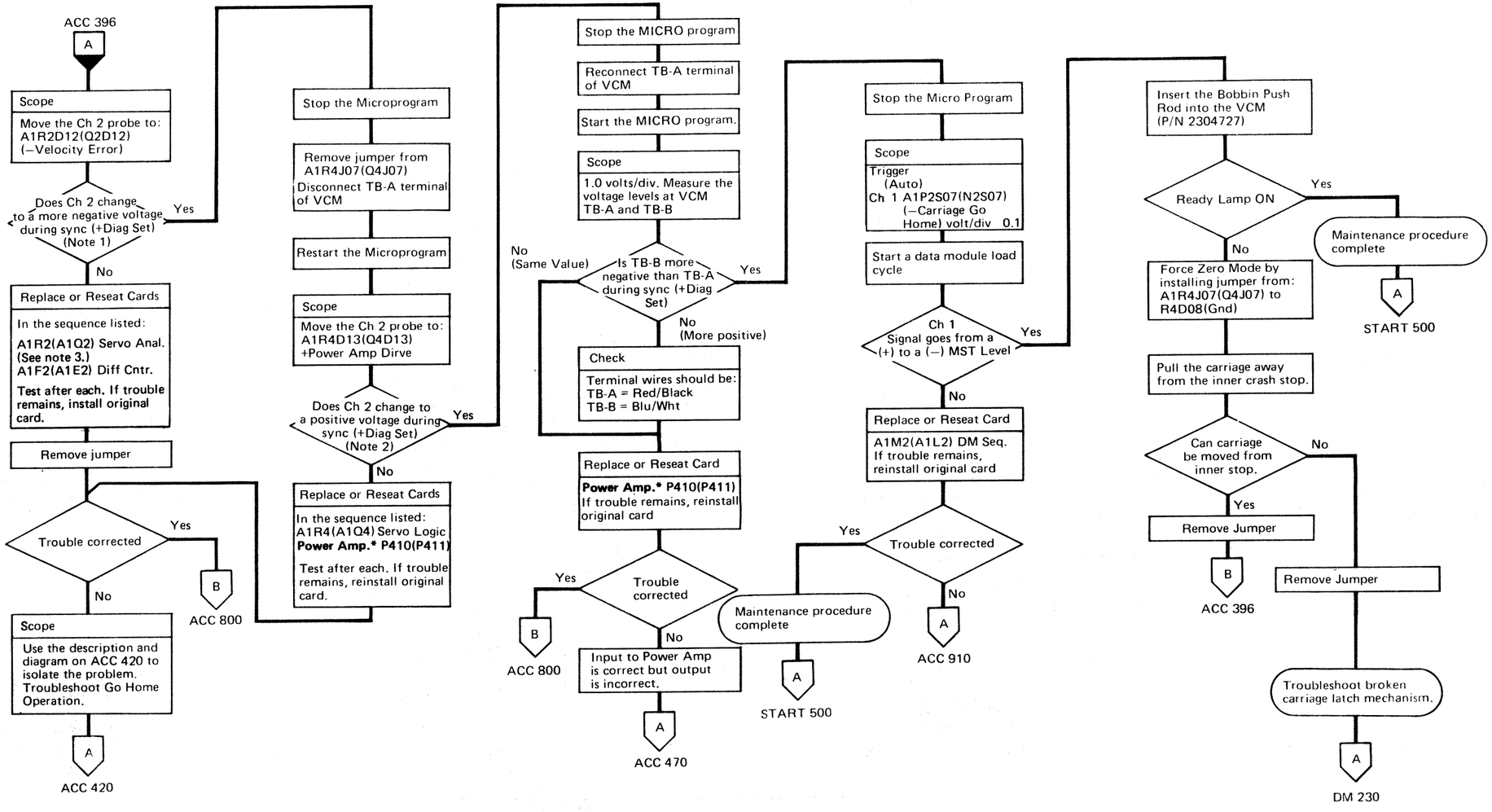
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BOBBIN BIAS



**See LOC 2 for P410(P411).*

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Note 1: Expect a change from –1.6 volts to –2.0 volts.

Note 2: Expect a change from 0 volts to +1.5 volts.

Note 3: Whenever A1R2 (A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

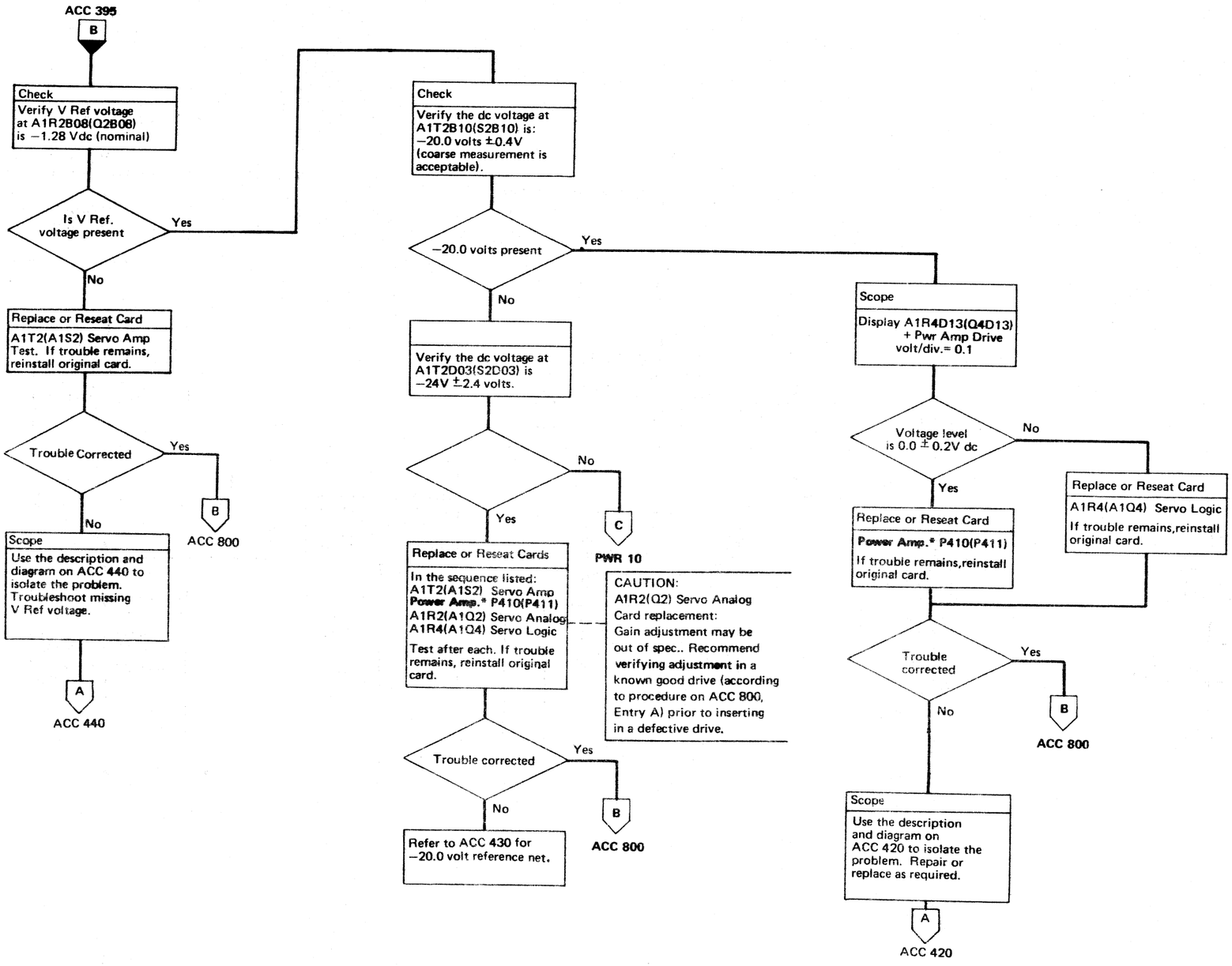
**See LOC 2 for P410(P411).*

DE0397 Seq. 1 of 2	2747178 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440223 14 Mar 75	

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BOBBIN BIAS



**See LOC 2 for P410(P411).*

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REZERO OPERATION DIAGRAM

ACC 321
ACC 331
ACC 360

A

3

Defective Rezero Operation. Check entire Rezero operation.

Verify Supply Voltages

Refer to ACC 420, Chart A, for voltage pin and specification data. Repair or replace as required.

Verify V.Ref Voltage

A1T2B08 (S2B08) is −1.28 Vdc (nominal). Refer to ACC 430. Repair or replace as required.

Verify −20.0 Volt Regulator

A1T2B10 (S2B10) is −20.0 ± 0.4 Vdc. Refer to ACC 430.

Access Control responds to Reset commands and rezero commands by setting the Wait latch. Wait Latch On resets all error conditions, forces Access Status to 000X, 0001 (Note 1), and prepares the Access Control to start a Rezero operation.

Detection of any rezero movement indicates that the Set Wait latch is operational.

Set Wait Latch is operational

No or not sure

Yes

A ACC 401

Verify each Set Wait Latch condition:

1. −Power on Reset ❶. Use Micro B3 to verify Access Status (Message Byte 9) = 000X, 0001.
2. −Carriage Go Home ❷ Unload Data Module and use Micro B3 to verify Access Status (Message Byte 9) = 000X, 0001.
3. Diag Go Home Verify that Micro A6, test 5, does *not* stop with error A650.
4. Check Reset ❹. Verify that Micro A3, test 2, does *not* stop with error A320, A323, or A324.
5. Auto +Manual Rezero ❺. Verify Micro A3, test 3, and the Manual Rezero Pushbutton result in carriage movement or an Access Error (Note 2).

If any Set Wait Latch condition is inoperative, trace logic to source of problem.

Trouble corrected

Yes

No

Maintenance procedure complete

A START 500

A ACC 401

Note 1: Micro B3 Message display byte 9 is drive Access Status.

Note 2: Bit 0, 1, or 2 of Access Status are on.

ACC 310

B

Invalid Access Status after Go Home command

Check Error Condition:

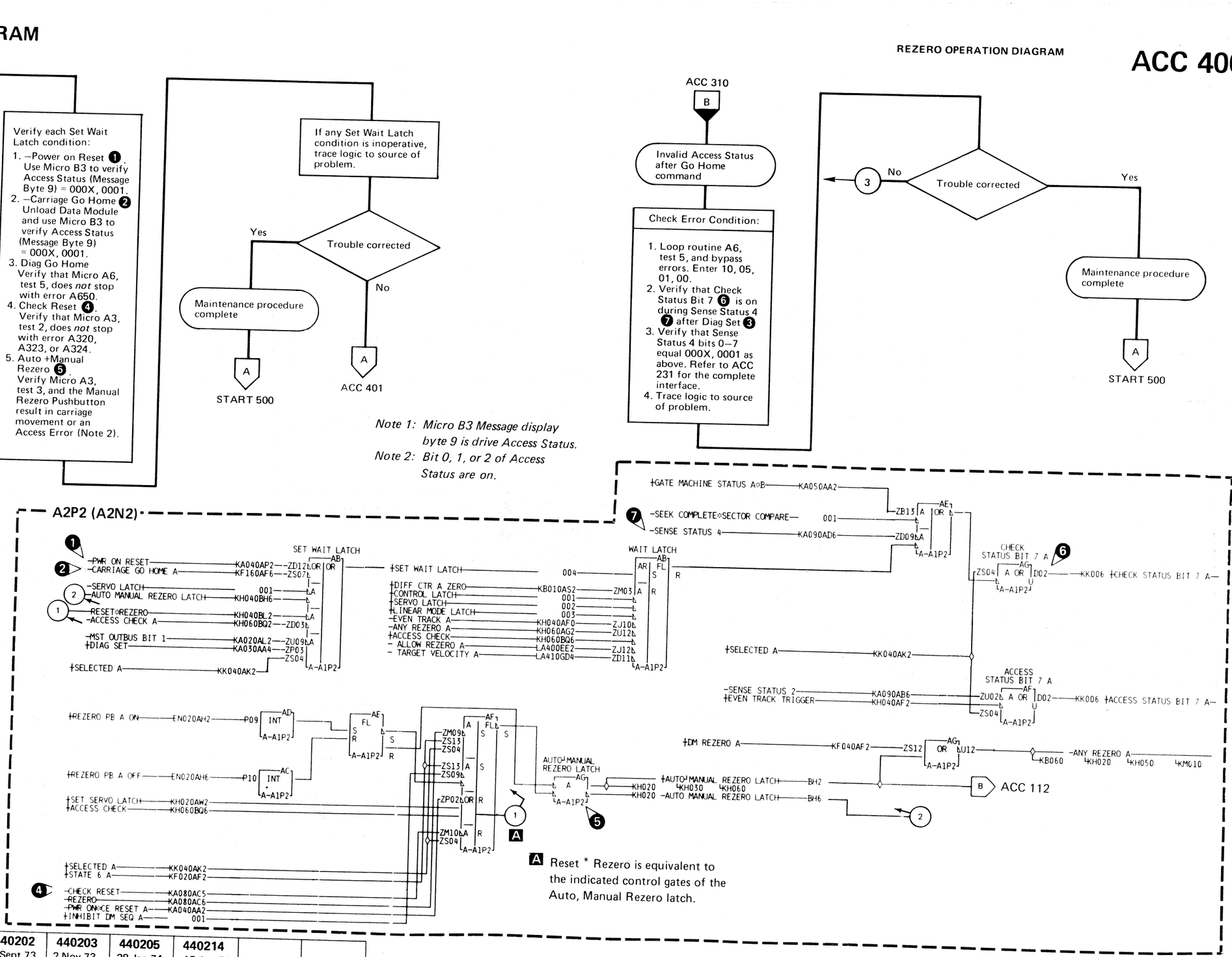
1. Loop routine A6, test 5, and bypass errors. Enter 10, 05, 01, 00.
2. Verify that Check Status Bit 7 ❻ is on during Sense Status 4 ❼ after Diag Set ❸
3. Verify that Sense Status 4 bits 0−7 equal 000X, 0001 as above. Refer to ACC 231 for the complete interface.
4. Trace logic to source of problem.

3 No Trouble corrected Yes

Maintenance procedure complete

A START 500

A2P2 (A2N2)



A Reset * Rezero is equivalent to the indicated control gates of the Auto, Manual Rezero latch.

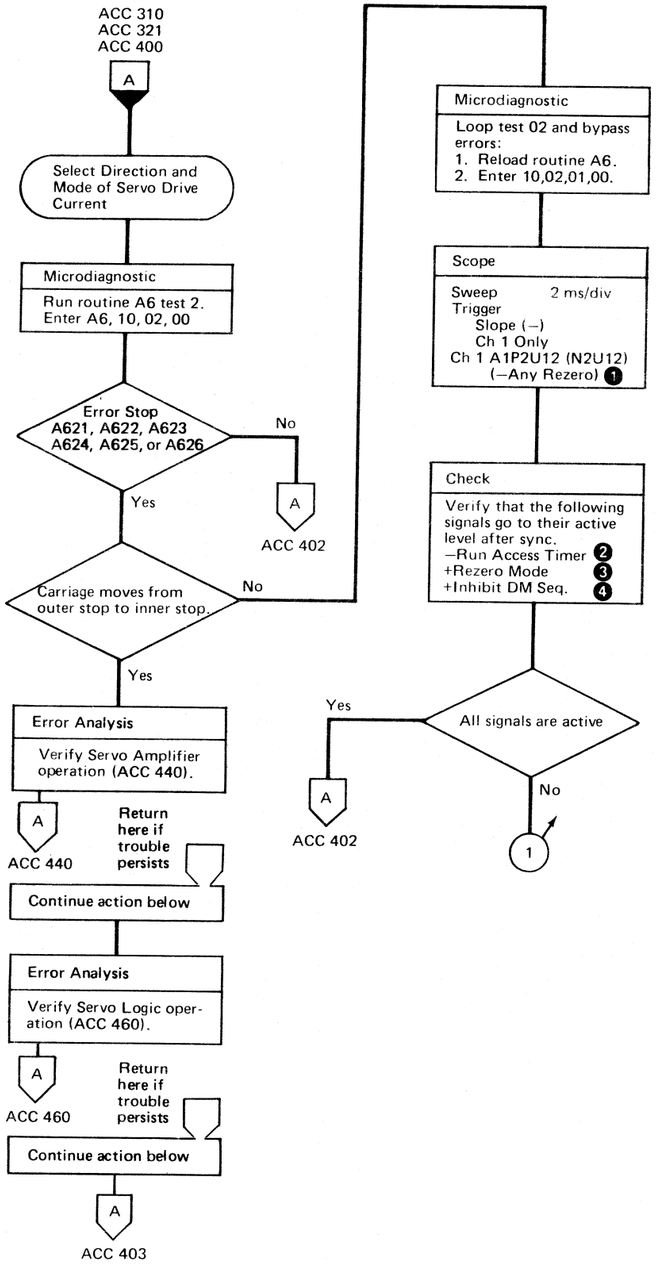
3340

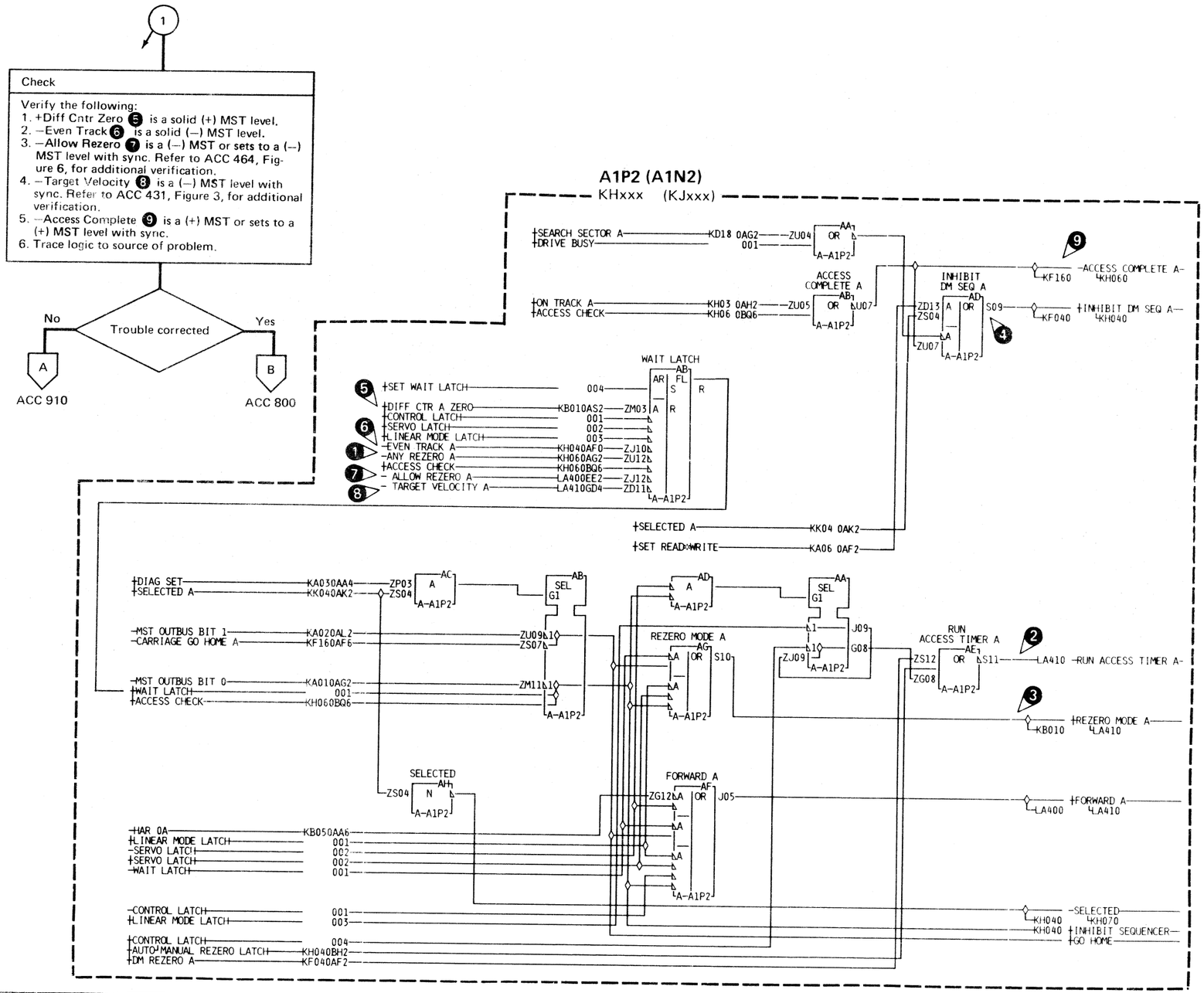
DF0400	2747180
Seq. 1 of 2	Part No. ( )

440200	440202	440203	440205	440214		
25 Jun 73	7 Sept 73	2 Nov 73	28 Jan 74	17 Jun 74		

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REZERO OPERATION DIAGRAM





DF0400	2747180
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REZERO OPERATION DIAGRAM

ACC 321
ACC 322
ACC 401

A

Carriage movement during Rezero Mode.

Visually observe carriage or use Bobbin Push Rod. Check with Rezero Push-button or Micro A6, test 2.

Carriage moves in response to a Rezero command.

Yes → A → ACC 403

No or uncertain of correct direction of movement

Microdiagnostic
Run routine B7.
Enter B7,00.

Carriage is driven into inner stop

No → Carriage not driven to inner stop, very weak drive current, erratic control of carriage movement. → 1

Yes

Microdiagnostic
Run routine A6, test 2.
Enter: A6,10,02,01,00.

Carriage is driven in both forward and reverse direction.

No → 2

Yes → A → ACC 403

1 →

Scope
Sweep: 10 ms/div
Trigger: Slope (+) CH1 only
CH1 A1R4J05 (Q4J05)
+Rezero Mode

Check
Verify the following:
1. +Rezero Mode ❶ is active for 50ms.
2. +Position Setpoint ❷ is solid (–) MST level.
3. +Forward ❸ is (+) MST level during Rezero Mode.
4. –Diff. Bit 5, 6 & 7 ❹ is –1.0 volt CS level.
5. DAC Output TP ❺ is +1.5 to +2.23 Vdc during Rezero Mode.
6. –Velocity Error ❻ is –2 volts during Rezero Mode.
7. +Move Forward ❼ is (+) MST level.
8. +Move Reverse ❽ is (–) MST level.
9. +Linear Mode ❾ is (–) MST level.
10. +Pwr Amp Drive Ⓐ is +1.5 volts during Rezero Mode.
11. VCM TB-B Ⓑ is more negative than TB-A during Rezero Mode.
12. Trace logic to source of problem.

2 →

Scope
Sweep: 2 ms/div
Trigger: Slope (+) CH1 only
CH1 A1P2G11 (N2G11)
+Any Rezero

Check
Verify the following:
1. +Position Setpoint ❷ is solid (–) MST level.
2. +Forward ❸ is (–) MST level.
3. –Diff. Bit 5, 6, & 7 ❹ is –1.0 volt C. S. level.
4. DAC Output TP ❺ is +1.5 to +2.23 Vdc during Rezero Mode.
5. –Velocity Error ❻ changes to a more negative level with synchronization
6. +Move Forward ❼ is (–) MST level.
7. +Move Reverse ❽ is (+) MST level.
8. +Linear Mode ❾ is (–) MST level.
9. Pwr Amp Drive Ⓐ changes to a negative voltage with sync
10. VCM TB-B Ⓑ is more positive than TB-A with sync
11. Trace logic to source of problem.

Trouble corrected

No → A → ACC 910

Yes → B → ACC 800

Access Control
A1P2 (A1N2)
Ref. ACC **400**, ACC 401
KHXXX (KJXXX)

M02 +Linear Mode
J05 +Forward
S10 +Rezero Mode
P13

Difference Counter
A1F2 (A1E2)
KBxxx (KCxxx)

❷ +Position S.P. J06
–Diff. Bit 2 D04
–Diff. Bit 3 B05
–Diff. Bit 4 B04
–Diff. Bit 5 B03
–Diff. Bit 6 D02
–Diff. Bit 7 B02

Servo Analog
A1R2 (A1Q2)
Ref. ACC 450

D12 –Velocity Error
D11 DAC Output TP ❺

❾ D04
❸ J11
❶ J05
B02 ❻

Servo Logic
A1R4 (A1Q4)
Ref. ACC 460

Ⓐ D13 Pwr Amp Drive
❼ G05 +Move Forward
G04 +Move Reverse ❽

Conn. D10 A1V3 (U3)
12

Power Amplifier
P410 (P411)
Ref. ACC 470

Ⓑ TB-B
1
2
3 VCM
4
TB A

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REZERO OPERATION DIAGRAM

ACC 330
ACC 341
ACC 401
ACC 402

A

Servo Controlled Carriage movement during Rezero Mode — Move Reverse

Microdiagnostic
Run routine A6 tests 2 & 3.
1. Enter A6, 10, 02, 00.
2. Enter A6, 10, 03, 00.

Tests run error free? — No

Error Analysis
Check Servo Input and Servo Amplifier card (ACC 440). Trace logic to source of problem.

A → ACC 440 — Return here if trouble persists

Continue action below

Microdiagnostic
Run Routine B7.
Enter B7, 00.

Scope
Sweep: 20 ms/div
Trigger:
Slope (+)
Ch 1 only
Ch 1 A1R4J05 (Q4J05)
+ Rezero Mode

Check
—Diff. Bits 2, 3, & 4 ❶ are +0.6 Vdc CS level. +Position Setpoint ❷ is (—) MST level. DAC Output TP ❸ is +0.7 Vdc during Rezero Mode. +Access Mode ❹ is (—) MST level. Repair or replace as required.

Trouble corrected? — Yes → B → ACC 800 — No

Error Analysis
Check Track Crossing timing. Refer to ACC 463 and 464 for setup and sample scope traces. (Note: Setup A & B only.)

ACC 463 — Return here if trouble persists

Continue action below

Error Analysis
Verify Power Amplifier (ACC 470).

A → ACC 470 — Return here if trouble persists

Continue action below

Error Analysis
Verify Rezero Operation. Refer to ACC 431 and 432 for setup and sample scope traces. (Note: Setup A and B only.)

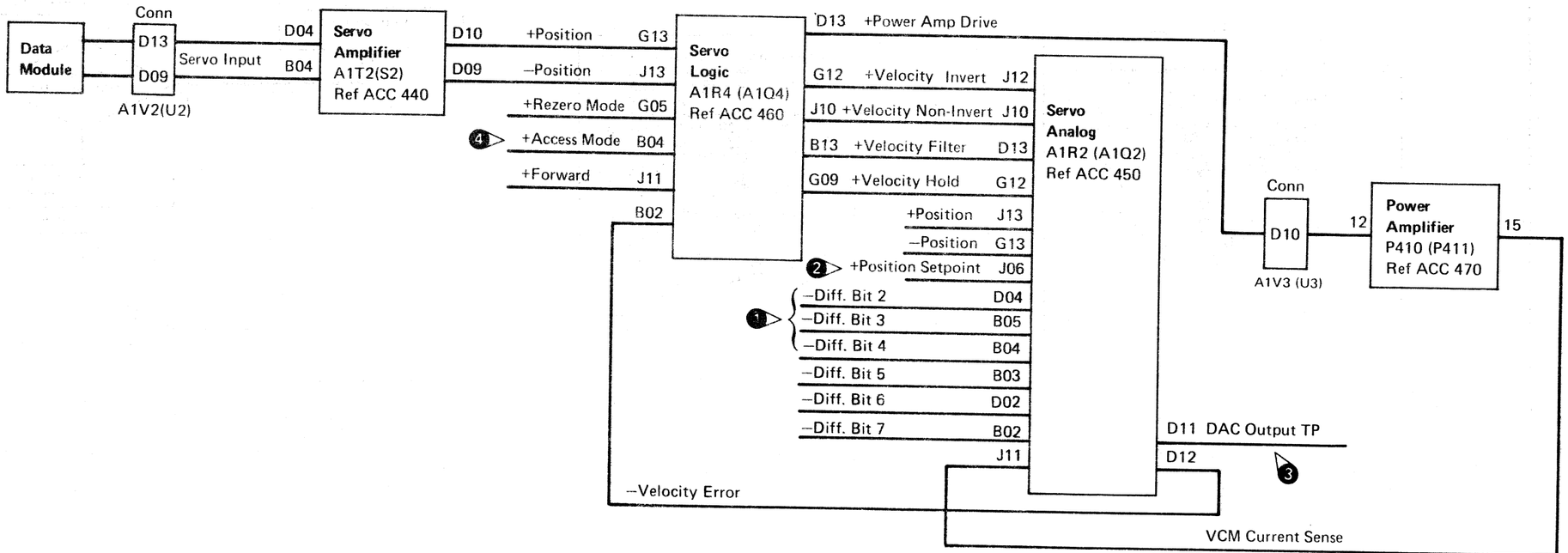
ACC 431 — Return here if trouble persists

Continue action below

A → ACC 404

A → ACC 404

SERVO FEEDBACK CONTROL DIAGRAM



DF0402	2747181	440200	440202	440203	440214			
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REZERO OPERATION DIAGRAM

ACC 312
ACC 350
ACC 403

A

Access Error during Rezero Operation State 0 — Move Reverse

Microdiagnostic

Run Routine A6, test 4.
Enter A6, 10, 04, 00

Test runs error free — No

Yes

A

ACC 405

Scope

Sweep 2 ms/div
Trigger Slope (—)
Ch 1 Only
Ch 1 A1P2G13(N2G13)
(—Rezero Pattern)

Check

Verify the following:
1. —Rezero Pattern ❶ goes to a (—) MST level during Rezero operation.
2. +Position Setpoint ❷ goes to a (+) MST level with —Rezero Pattern.
   Refer to ACC 431, Figure 3, for additional verification.
3. —Target Velocity ❸ goes to a (—) MST level after + Position Setpoint.
   Refer to ACC 431, Figure 3C, for sample timing relationship.
4. The Control latch is set on (Access State 2) with detection of —Target Velocity in the Rezero Pattern Area, which turns off +Position Setpoint. Refer to ACC 431, Figure 3C.
5. Trace logic to source of problem.

Trouble corrected — Yes

No

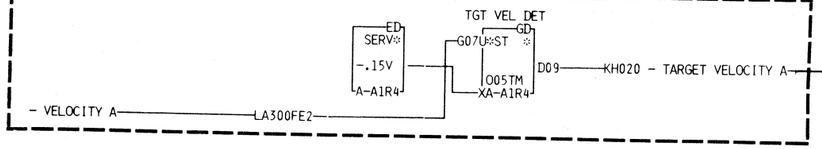
A

ACC 910

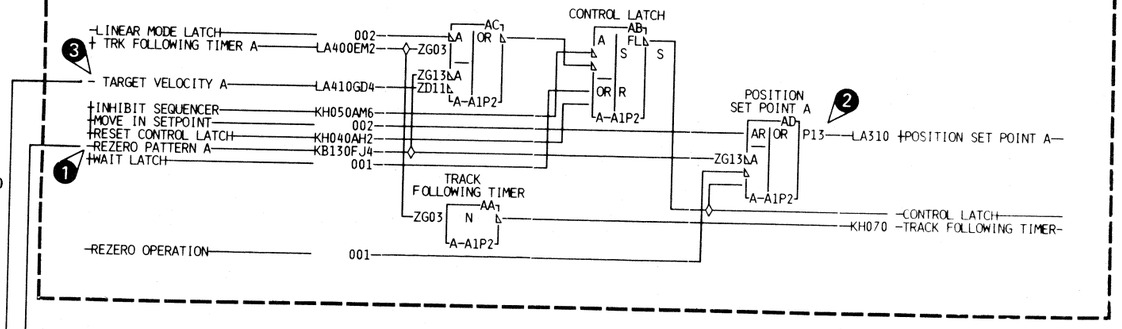
B

ACC 800

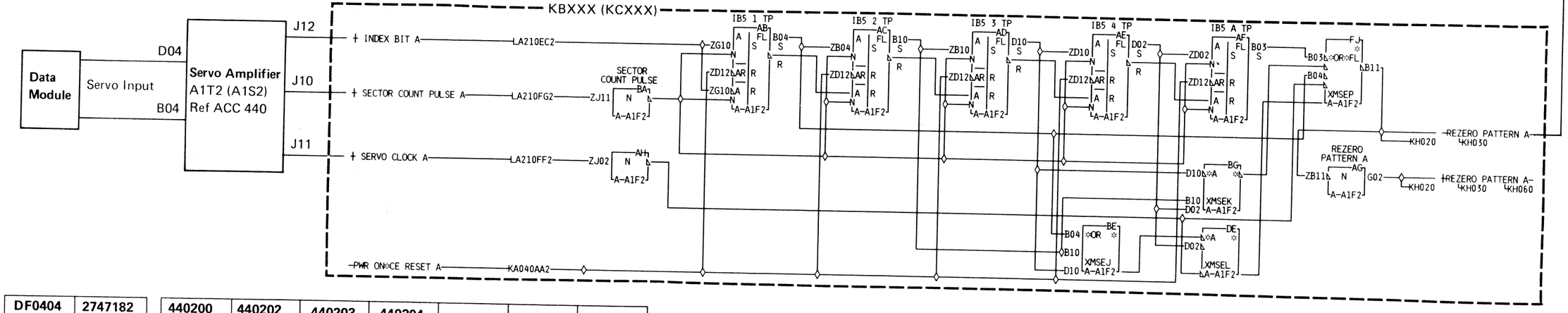
A1R4 (A1Q4)
ACC 460



A1P2 (A1N2)
KHXXX (KJXXX)



A1F2 (A1E2)
KBXXX (KCXXX)



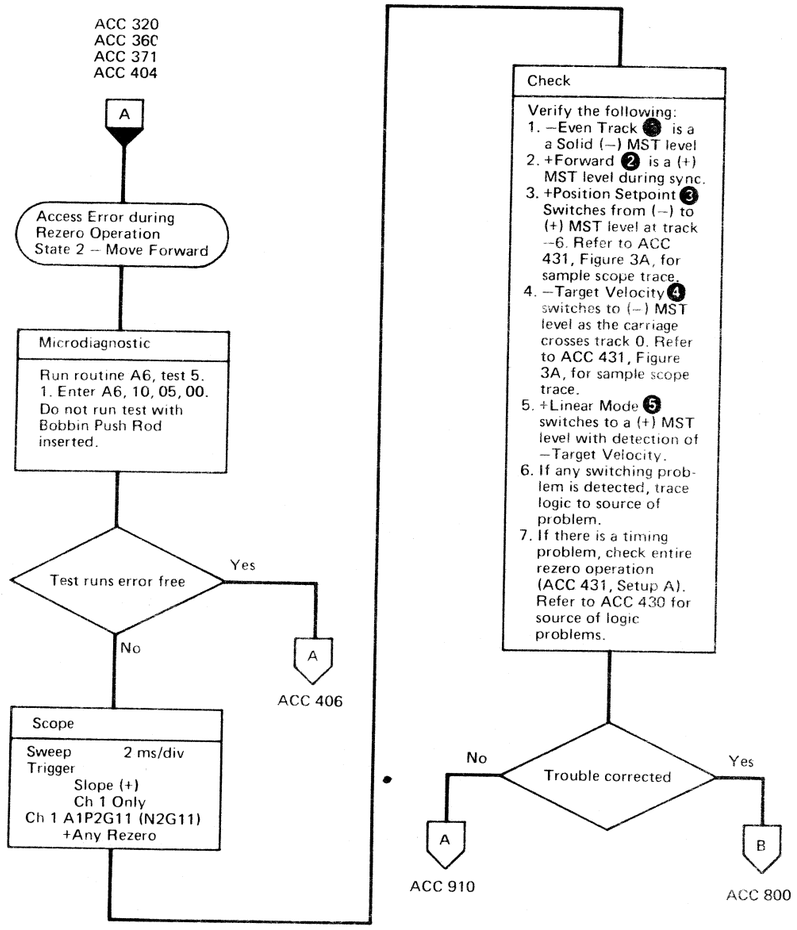
3340

DF0404	2747182
Seq. 1 of 2	Part No. ( )

440200	440202	440203	440204			
25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73			

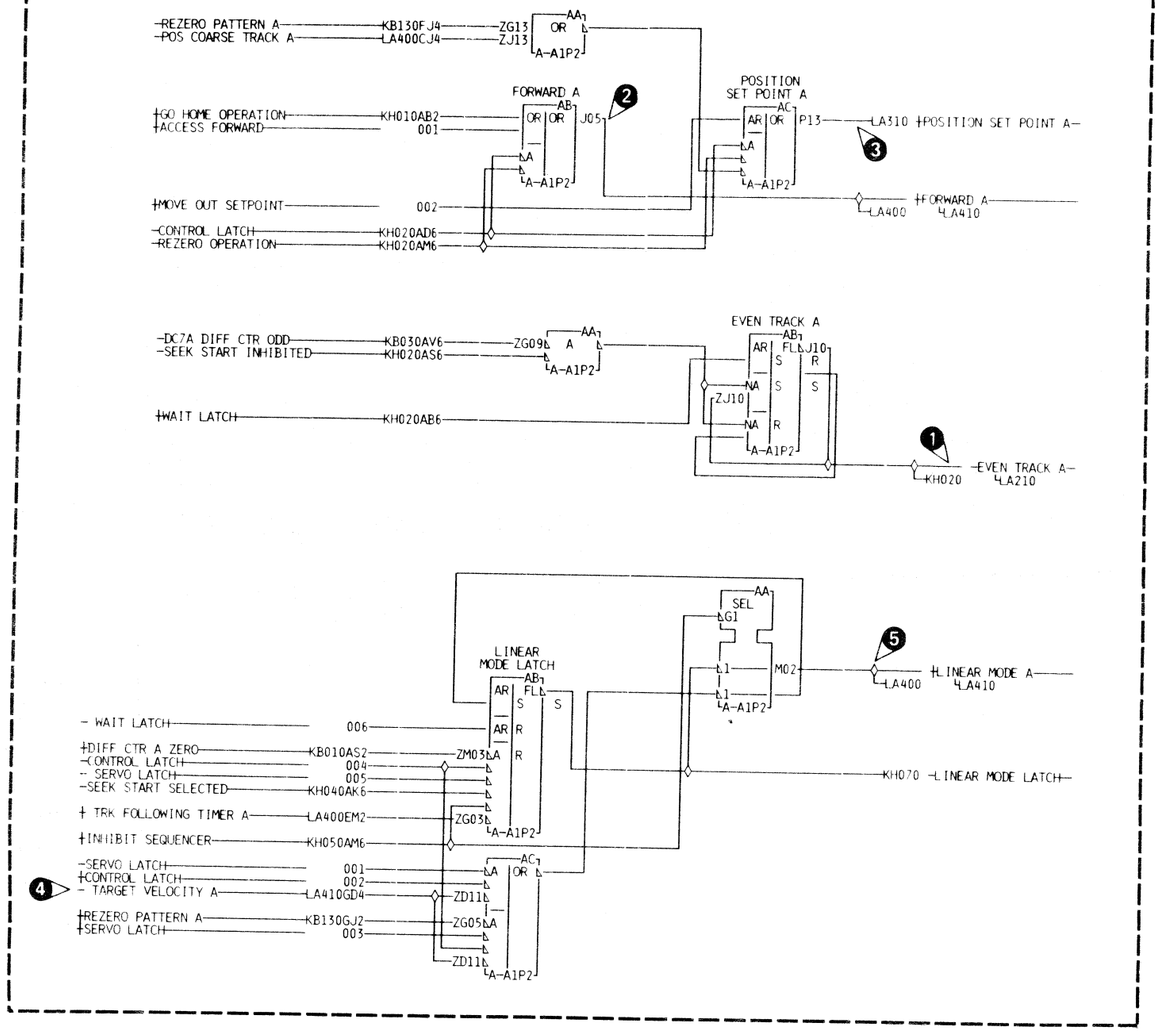
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REZERO OPERATION DIAGRAM



A1P2 (A1N2)

KHXXX (KJXXX)

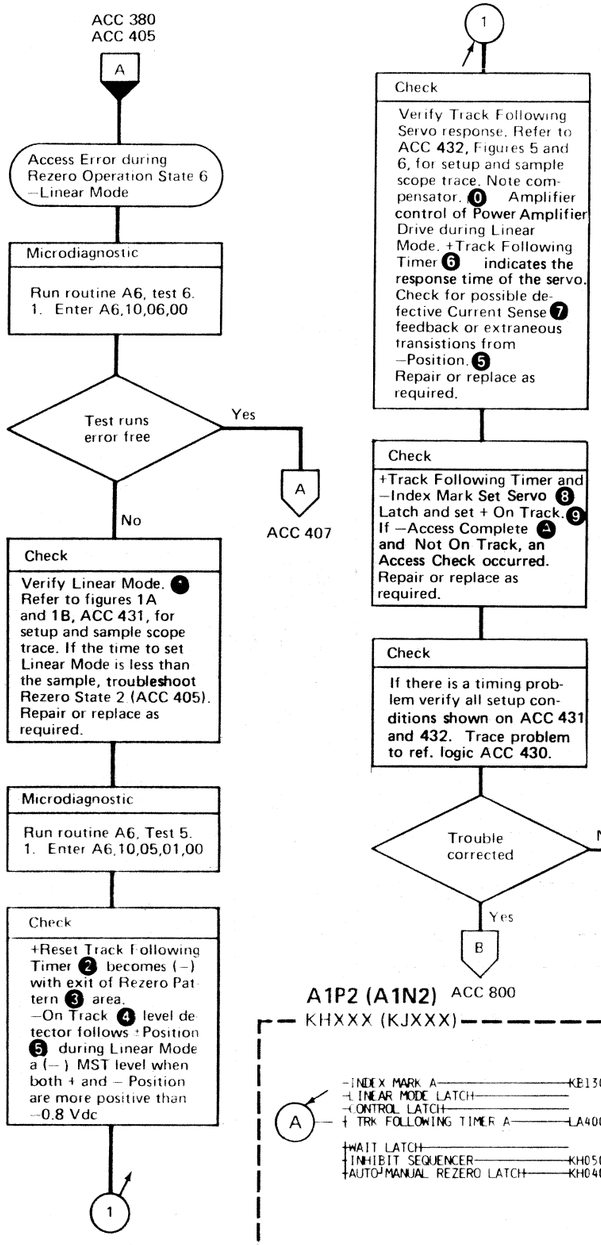


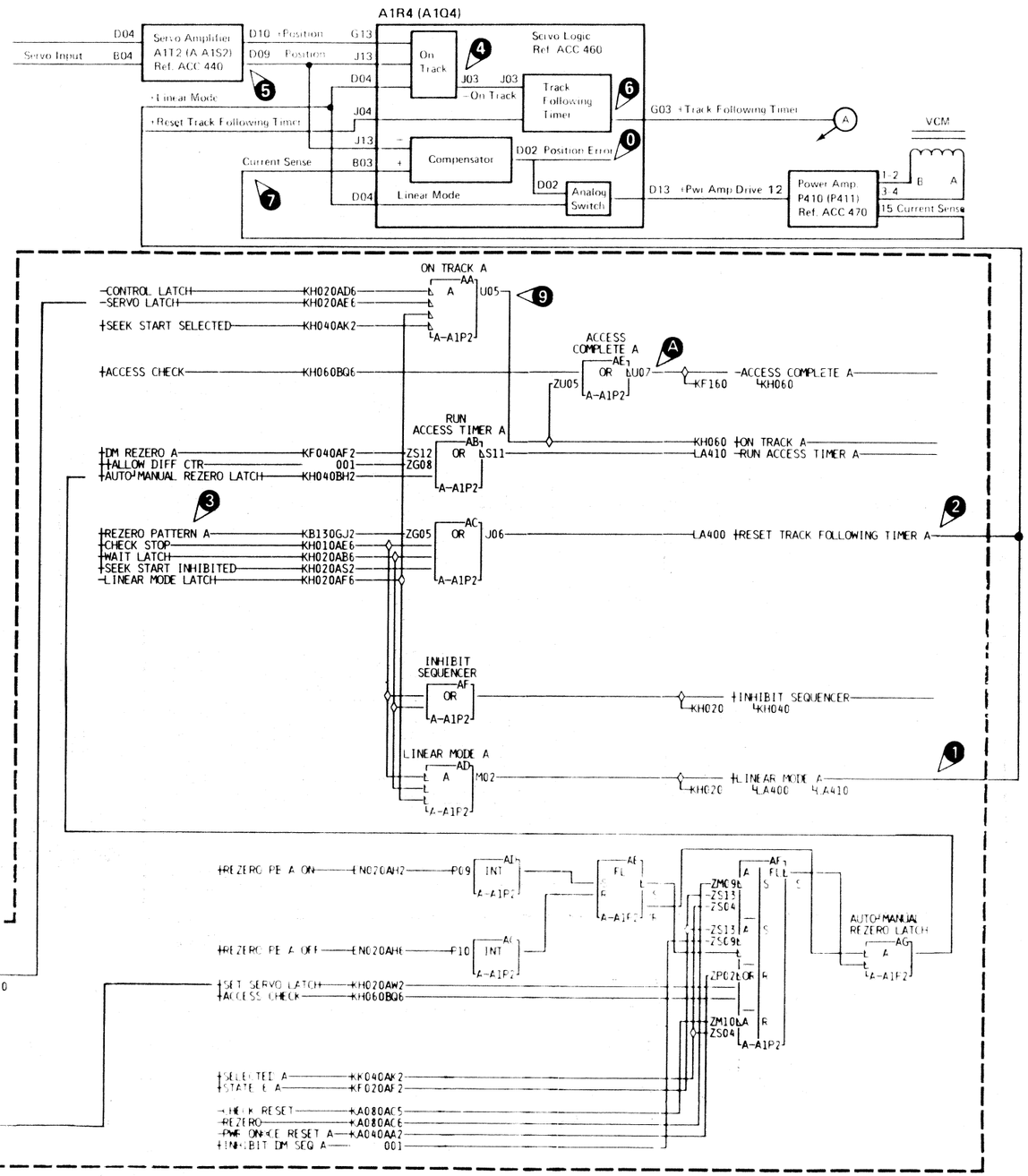
DF0404 Seq. 2 of 2	2747182 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73			

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REZERO OPERATION DIAGRAM

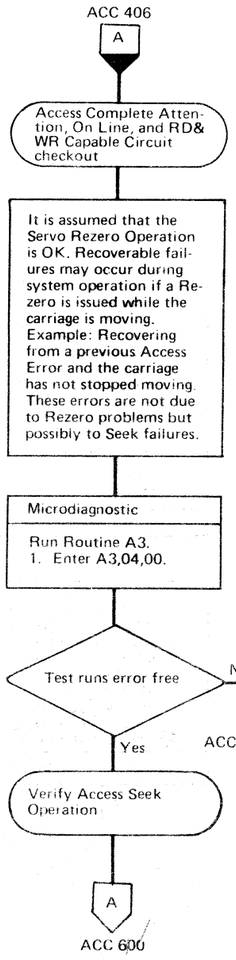


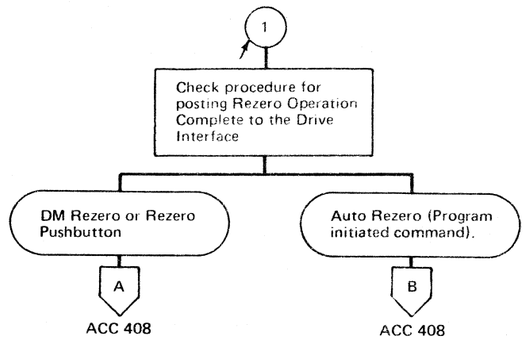


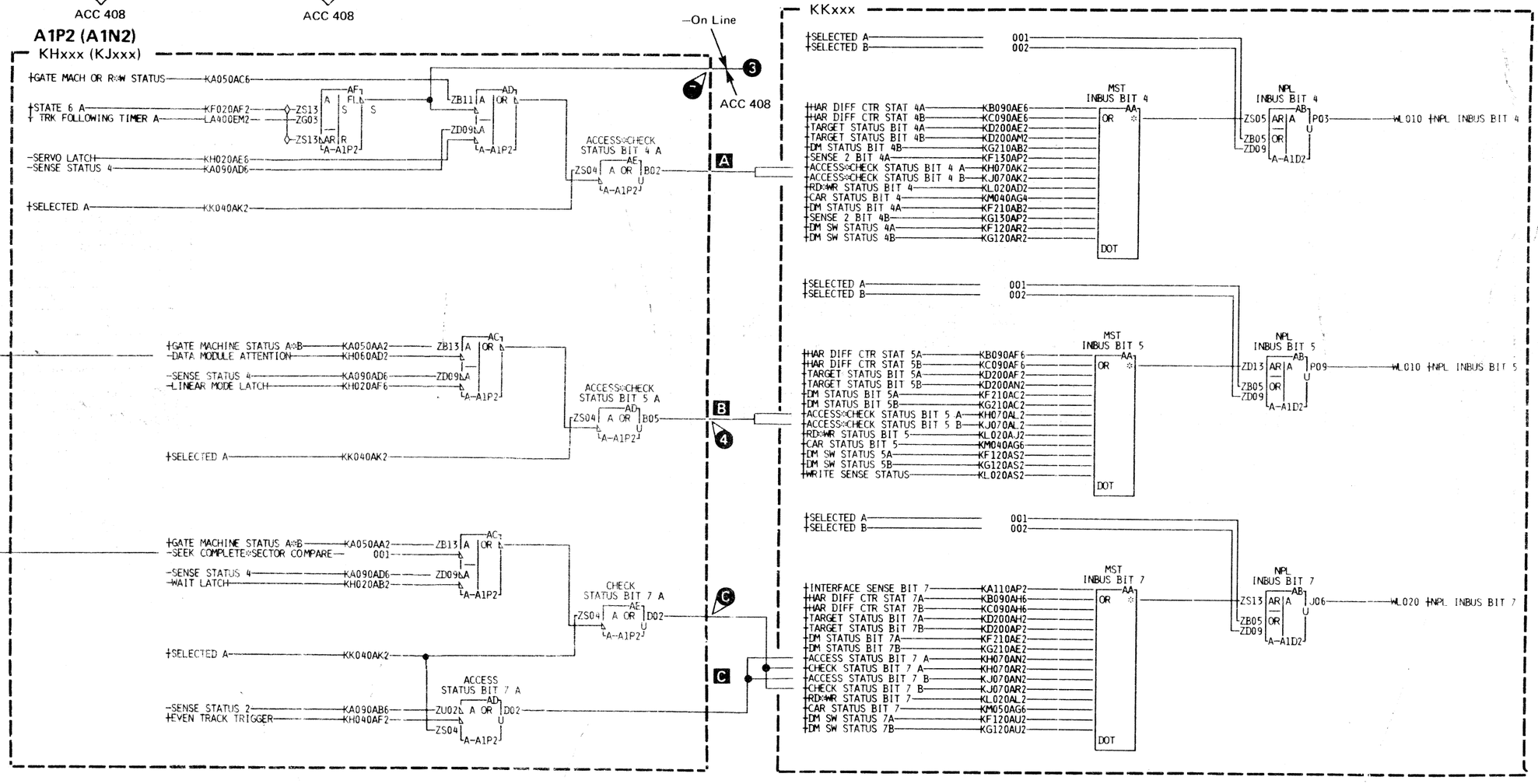
DF0406	2747183	440200	440202	440203	440214			
Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	17 Jun 74			

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REZERO OPERATION DIAGRAM







A Access*Check Status Bit 4

On Line – Sense Data Format 1, Byte 8, or Micro B3, Byte 4.

Servo Latch – Sense Data Format 1, Byte 16, or Micro B3, Byte 9.

B Access*Check Status Bit 5

Data Module Attention – Sense Data Format 1, Byte 8, or Micro B3, Byte 4.

Linear Mode Latch – Sense Data Format 1, Byte 16, or Micro B3, Byte 9.

C Check Status Bit 7

Seek Complete*Sector Compare – Sense Data Format 1, Byte 8, or Micro B3, Byte 4.

Wait Latch – Sense Data Format 1, Byte 16, or Micro B3, Byte 9.

Odd Track – Sense Data Format 1, Byte 10, or Micro B3, Byte 6.

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REZERO OPERATION DIAGRAM

ACC 407 A

Check

Verify the following:
1. +DM Rezero (1) or a Manual Rezero (2) pushbutton enables a Data Module Attention (3). DM Attention is available on the In Bus as Access*Check Status Bit 5 (4) when Access Complete (5) is set on after the Rezero operation.
2. A "Pack Change" Attention (6) is posted to the interface if the drive is in On Line (7) status.
   - The data module load is completed without an error.
   - The Manual Rezero is initiated to an (An unsuccessful Manual Rezero still generates a "Pack Change" Attention.)
3. Rd*Wr Capable (8) is active when the servo is track following and no error conditions are active. The Ready lamp is a direct function of Rd*Wr Capable.
4. Attention Reset (9) or CE Reset (pushbutton) (A) turn off DM Ready and –Attention.
5. Trace logic to source of problem.

ACC 407 B

Microdiagnostic

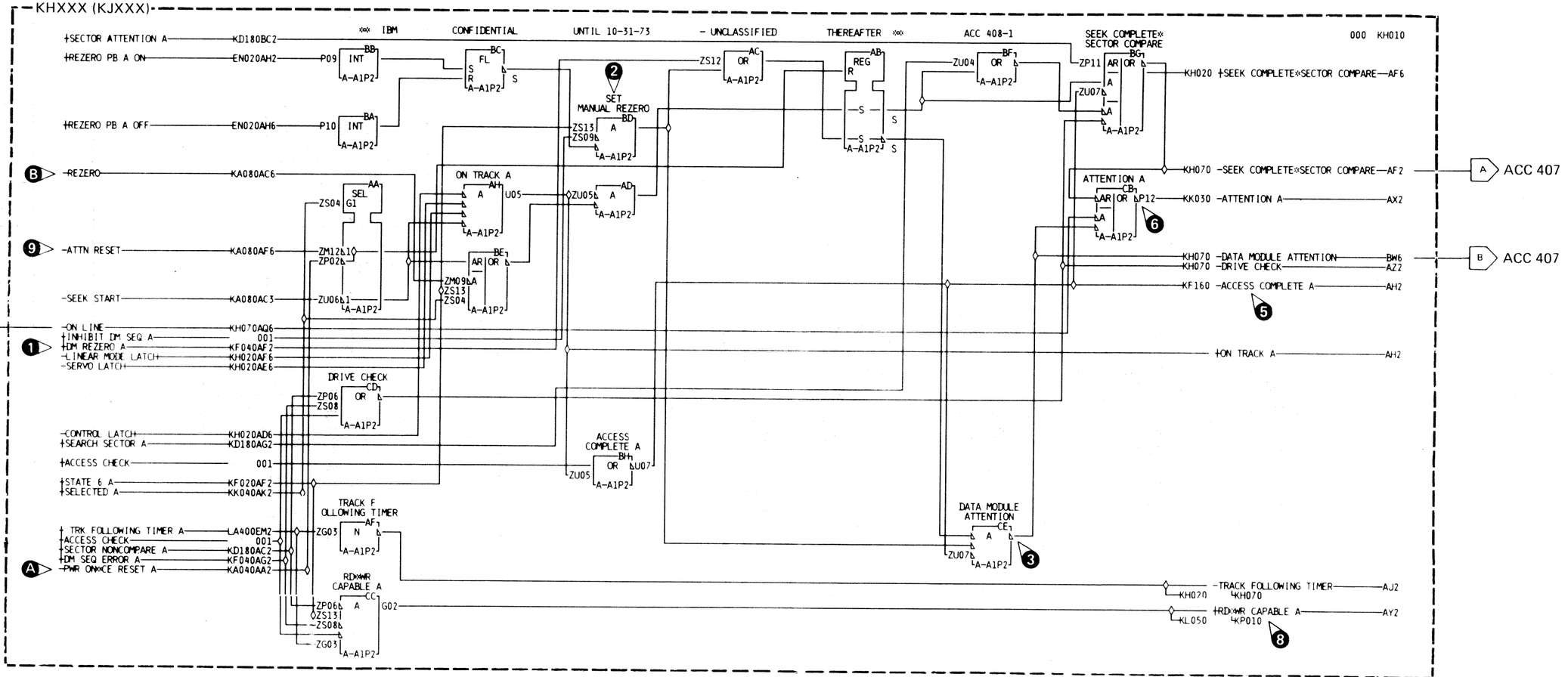
Run routine A3, test 3.
1. Enter A3,10,03,01,00.

Check

Verify the following:
1. –Access Complete (5) after an Auto Rezero (B) gates Seek Complete*Sector Compare to the In bus as Check Status Bit 7 (C).
2. An Attention (6) is also posted to the interface by Seek Complete*Sector Compare.
3. Rd*Wr Capable (8) is active when the Servo is Track Following and no error conditions are active. The Ready lamp is a direct function of Rd*Wr Capable.
4. Attention Reset (9) or CE Reset (pushbutton) (A) turns off the Busy Latch, which degates Seek Complete*Sector Compare and –Attention.
5. Trace logic to source of problem.

Trouble corrected? No → A → ACC 910; Yes → A → START 500

A1P2 (A1N2)
KHXXX (KJXXX)



DF0408	2747653	440202	440203	440205	440223			
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GO HOME OPERATION DIAGRAM

DM 320, DM 330
ACC 312, ACC 322
ACC 323, ACC 396
ACC 397, ACC 398

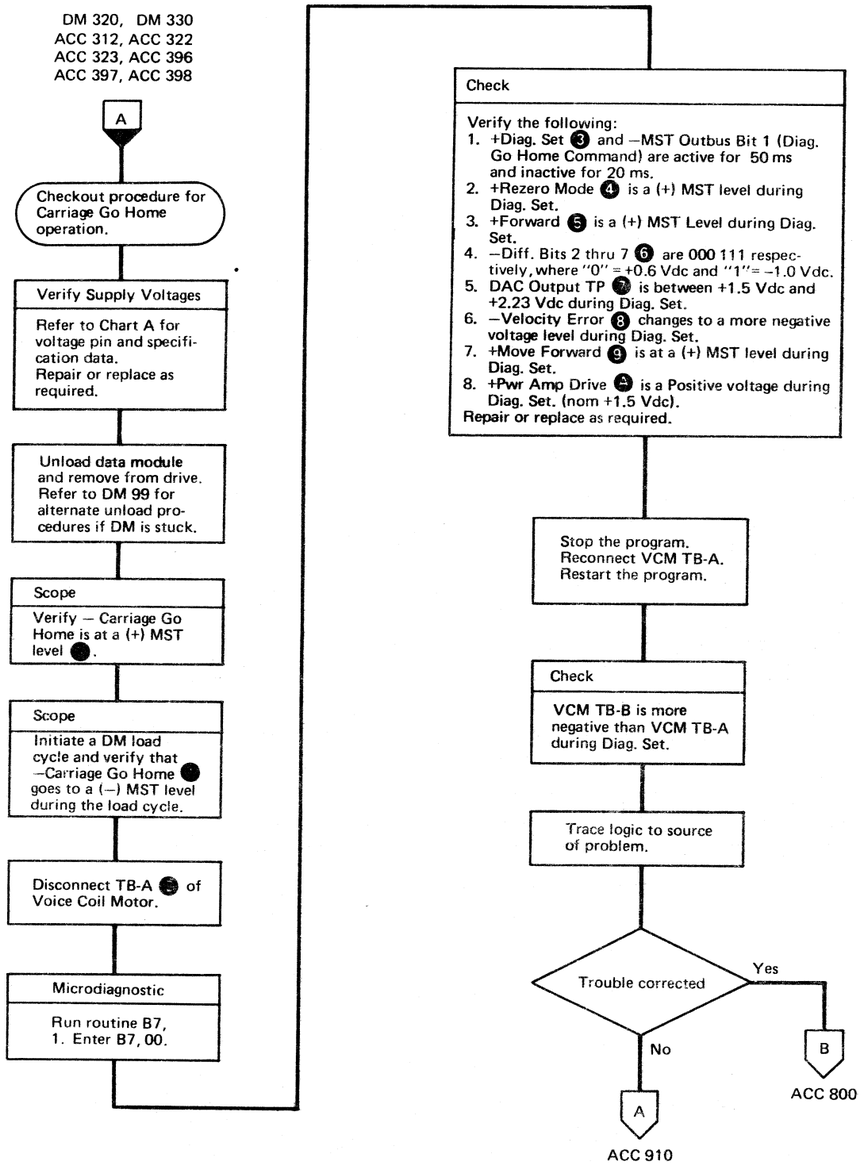


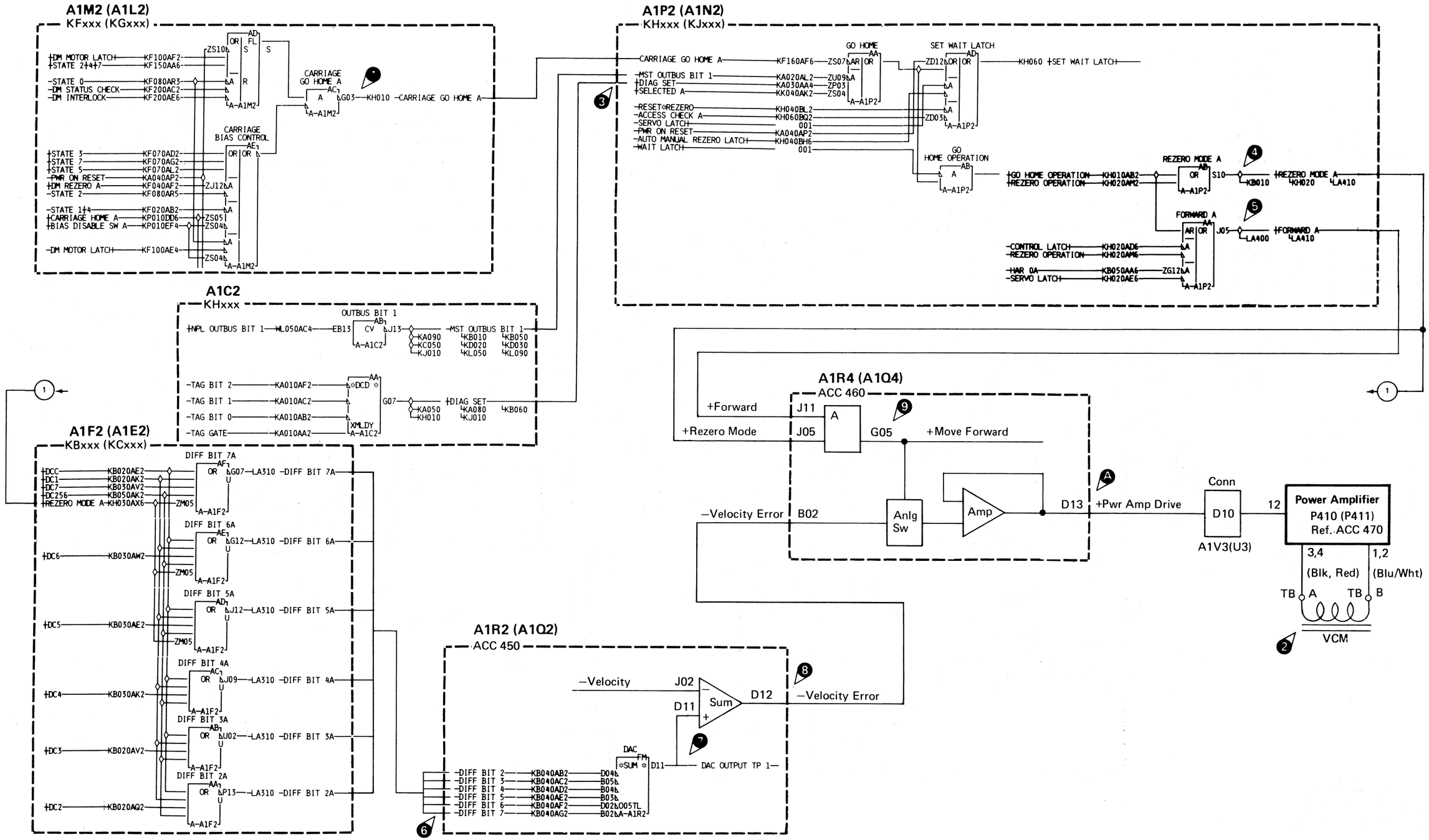
CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1R2D03 (Q2D03)	–24.0 to –28.8 Vdc	PWR 50-A	PWR 250-A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R2D06 (Q2D06)	–12.0 to –14.4 Vdc	PWR 40-A	PWR 240-A
A1R2G06 (Q2G06)	– 3.84 to – 4.16 Vdc	PWR 55-A	
	– 3.72 to – 4.4 Vdc		PWR 255-A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A
A1T2B08 (S2B08)	– 1.28 Vdc (nominal)	ACC 441	ACC 441
A1T2B10 (S2B10)	–19.6 to –20.4 Vdc	ACC 720-A	ACC 720-A
P410–7,8 (P411–7,8)	–36.0 to –43.2 Vdc	PWR 80-A	PWR 280-A
P410–14 (P411–14)	–12.0 to –14.4 Vdc	PWR 40-A	PWR 240-A
P410–16 (P411–16)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A

See LOC 4 for location of P410/411.

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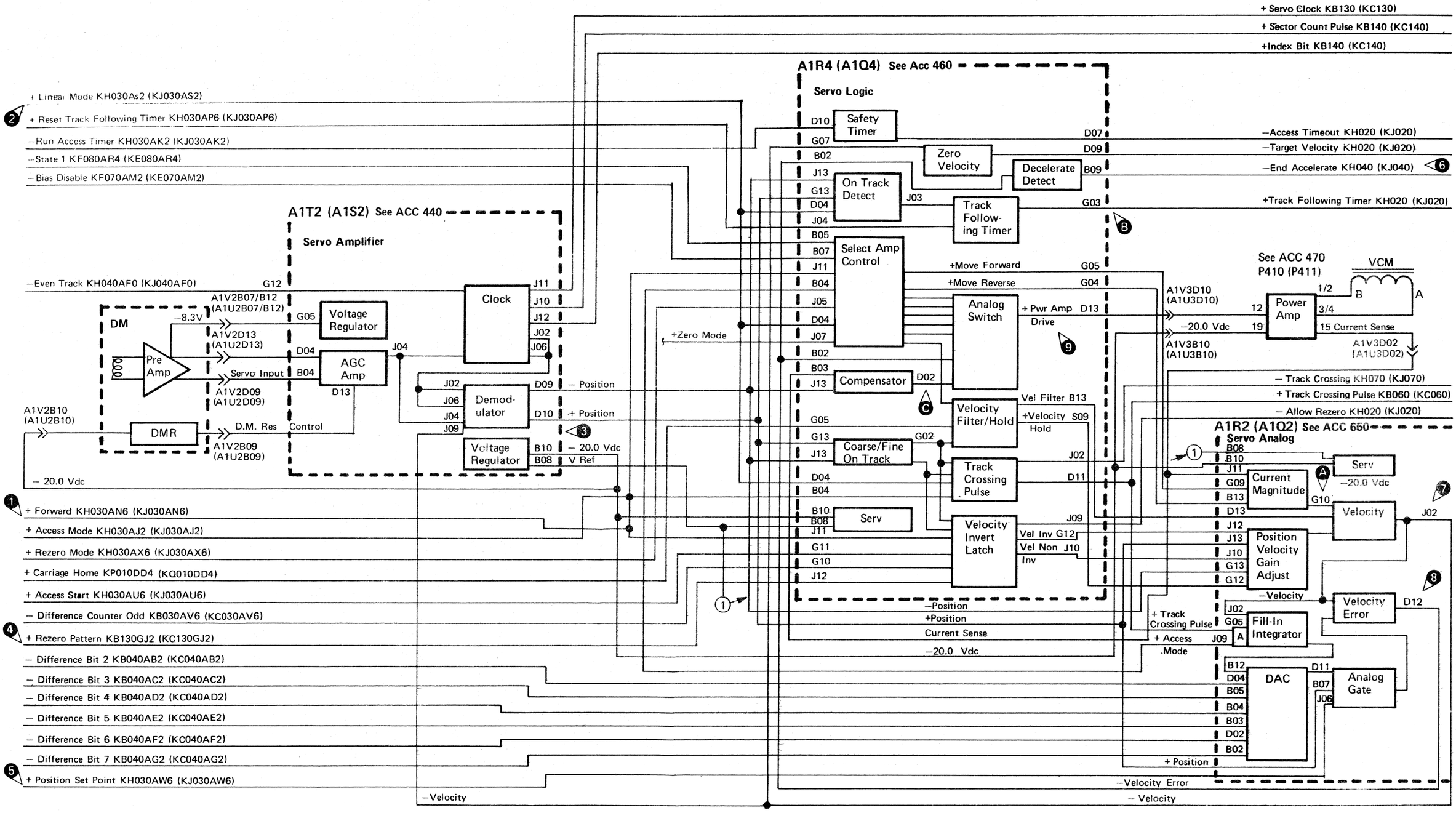
GO HOME OPERATION DIAGRAM



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3340	DF0420 Seq. 2 of 2	2747184 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440212 29 Apr 74		

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REZERO OPERATION TIMING

See ACC 430 for test points

❶ Ch 1 A1R4J11(Q4J11)
+ Forward
volt/div 0.1
probe X10

❷ Ch 2 A1R4D04(Q4D04)
+ Linear Mode
volt/div 0.1
probe X10

❸ Ch 1 A1T2D10(S2D10)
+ Position
volt/div 0.5
probe X10

❹ Ch 2 A1R4J12(Q4J12)
+ Rezero Pattern
volt/div 0.1
probe X10

❺ Ch 1 A1R2J06(Q2J06)
+ Position Setpoint
volt/div 0.1
probe X10

❻ Ch 2 A1R4D09(Q4D09)
– Target Velocity
volt/div 0.1
probe X10

Setup A - Rezero from Outer Stop

Microdiagnostic A6 test 5
1. Load Routine A6
2. Enter 10,05,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11(N2G11) + Any Rezero

Fig 1A

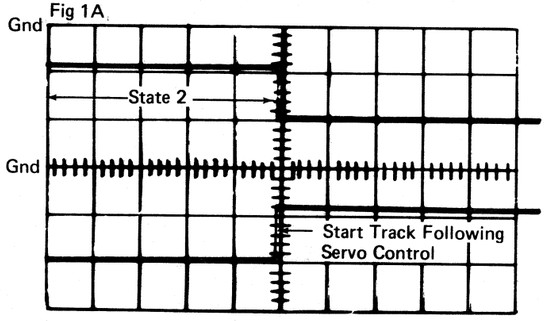


Fig 2A

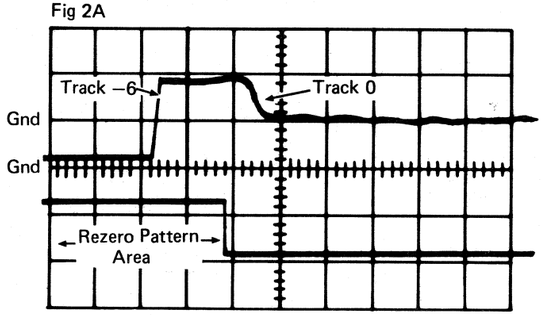
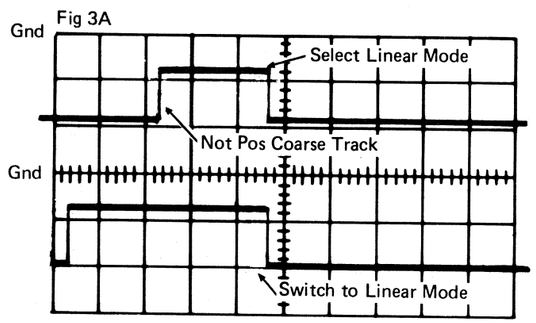


Fig 3A



Setup B - Rezero from Track 0

Microdiagnostic A3 test 3
1. Load routine A3
2. Enter 10, 03, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Fig 1B

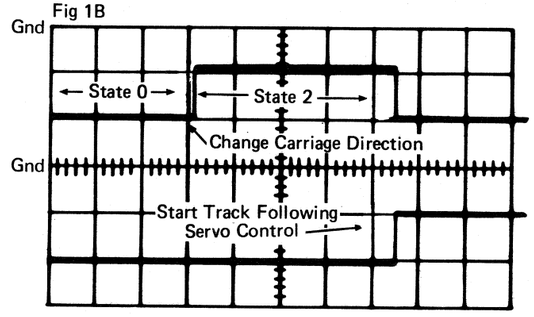


Fig 2B

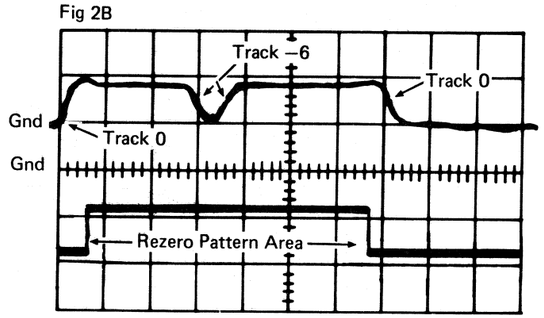
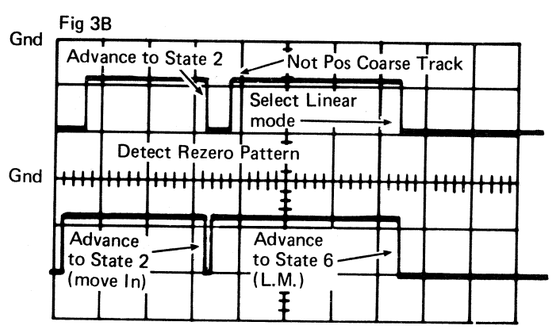


Fig 3B



Setup C - Rezero from Track 12

Microdiagnostic A4 test A
1. Load routine A4
2. Enter 10, 0A, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Fig 1C

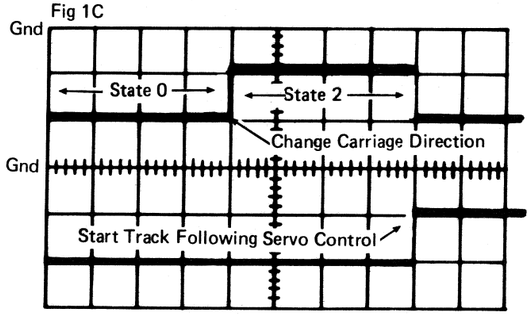


Fig 2C

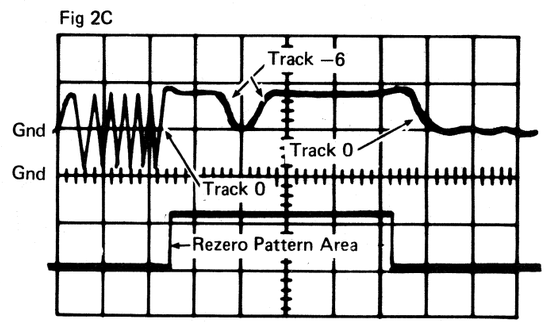
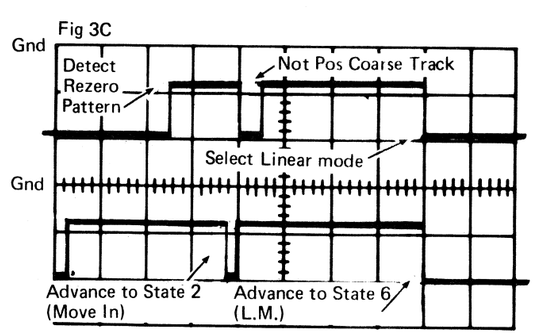


Fig 3C



DF0430 Seq. 1 of 2	2747623 Part No. ( )

440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73				

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REZERO OPERATION TIMING

See ACC 430 for test points

❼ Ch 1 A1R2J02(Q2J02)
– Velocity
volt/div 0.1(Setup B=0.05)
probe X10

❽ Ch 2 A1R2D12(Q2D12)
– Velocity Error
volt/div 0.2
probe X10

❾ Ch 1 A1R4D13(Q4D13)
+ Power Amp Drive
volt/div 0.2
probe X10

Ⓐ Ch 2 A1R2G10(Q2G10)
Current Magnitude
volt/div 0.2
probe X10

Ⓑ Ch 1 A1R4G03(Q4G03)
+ Track Following Timer
volt/div 0.1
probe X10

Ⓒ Ch 2 A1R4D02(Q4D02)
Compensator Amp
volt/div 0.1
probe X10

Setup A – Rezero from Outer Stop

Microdiagnostic A6 test 5
1. Load routine A6
2. Enter 10,05,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Fig 4A

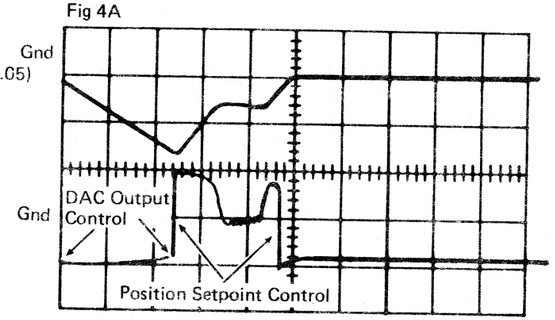


Fig 5A

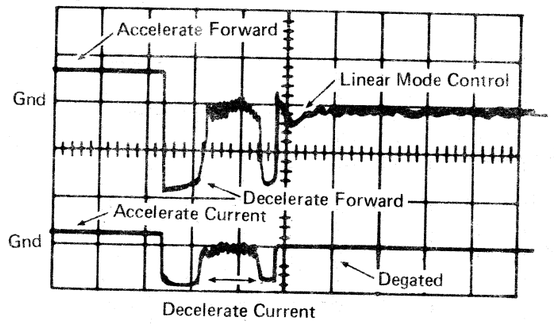
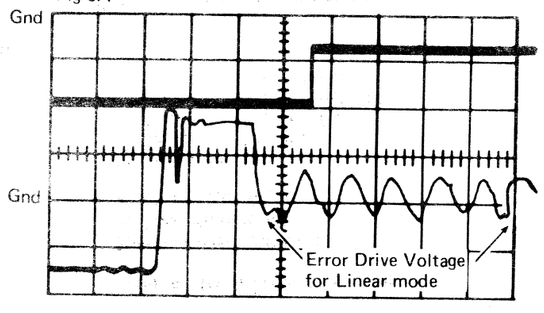


Fig 6A



Setup B – Rezero from Track 0

Microdiagnostic A3 test 3
1. Load routine A3
2. Enter 10,03,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Fig 4B

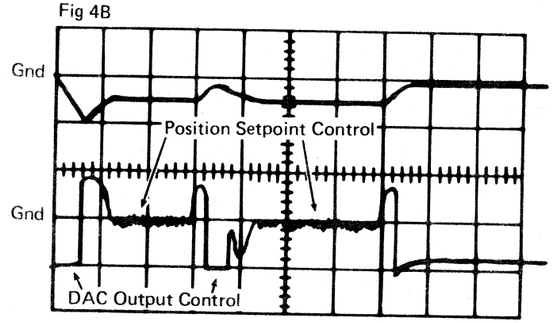


Fig 5B

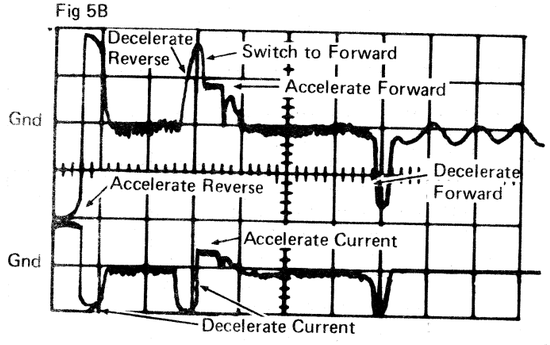
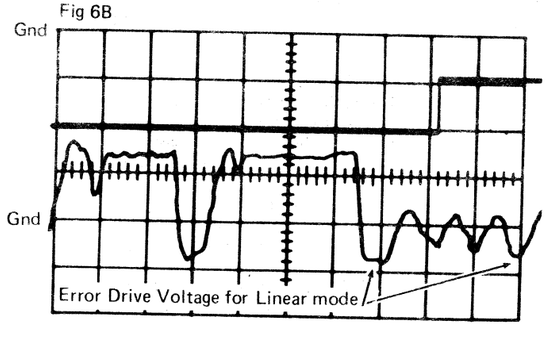


Fig 6B



Setup C – Rezero from Track 12

Microdiagnostic A4 test A
1. Load routine A4
2. Enter 10,0A,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) +Any Rezero

Fig 4C

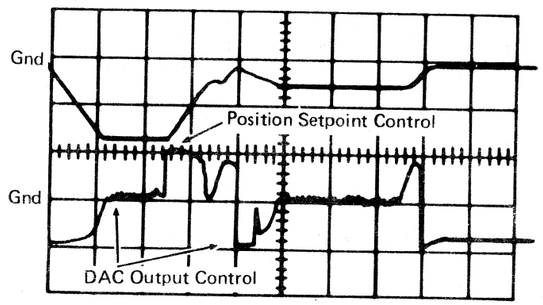


Fig 5C

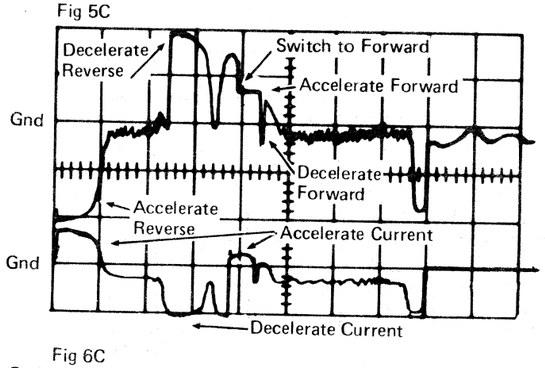
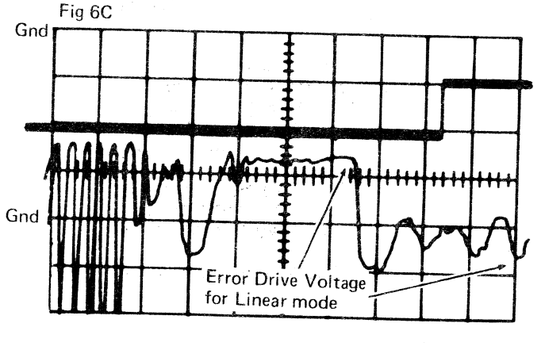


Fig 6C



DF0430	2747623
Seq. 2 of 2	Part No. ( )

440202	440203	440204			
7 Sept 73	2 Nov 73	21 Dec 73			

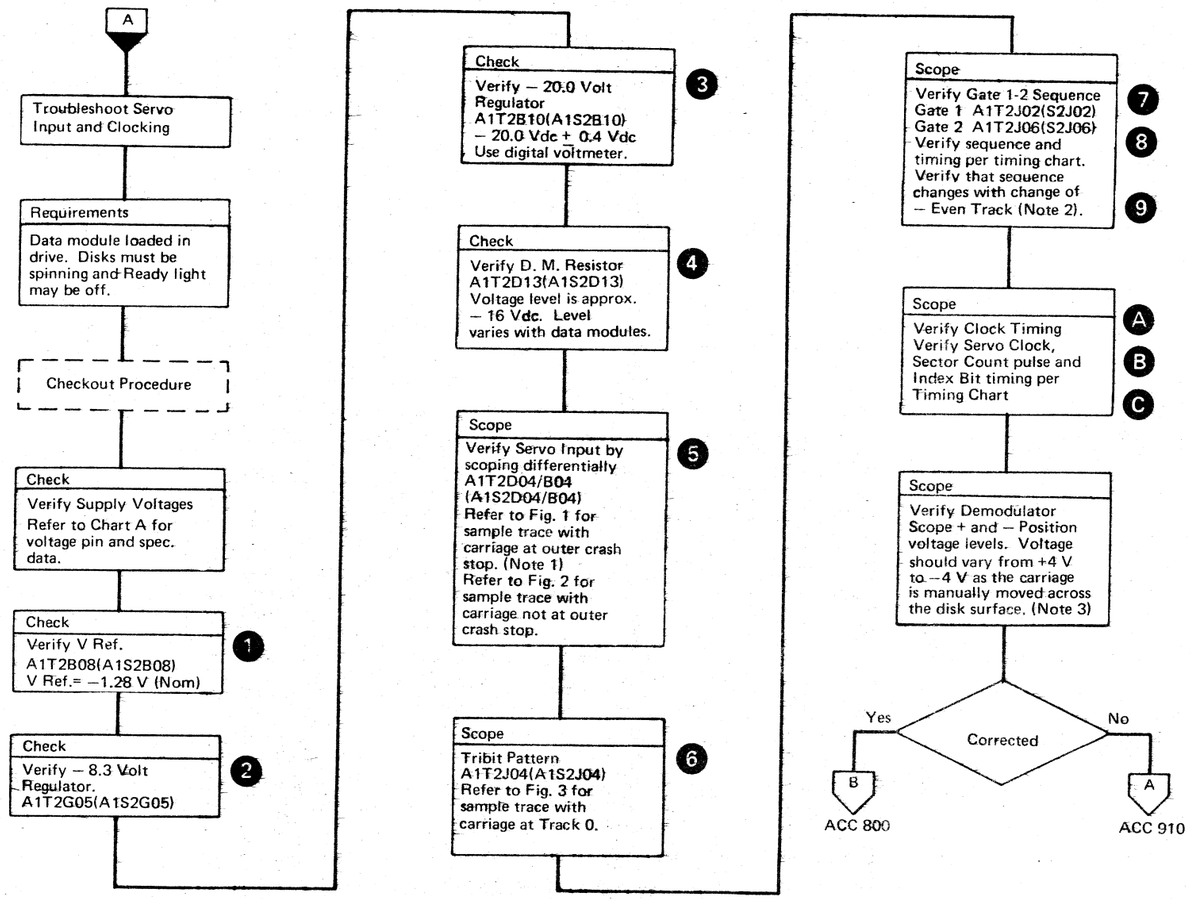
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SERVO AMPLIFIER

ACC 440



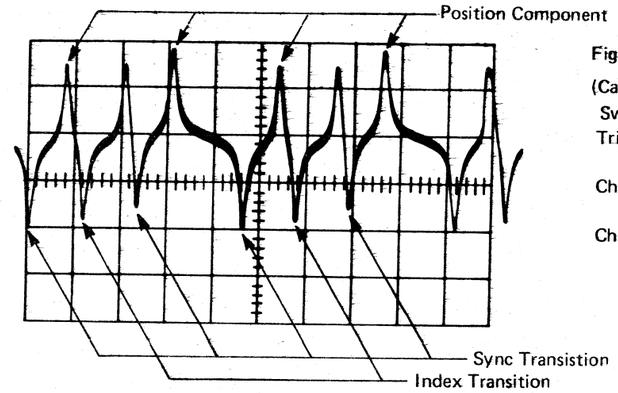


Figure 1 - Servo Input
(Carriage at Outer Stop)
Sweep 1 μs/div.
Trigger/Mode Norm/Add
Slope (−)
Ch 1 A1T2B04 (S2B04)
0.05 volts/div, X1 probe
Ch 2 A1T2D04 (S2D04)
0.05 volts/div, X1 probe
Invert

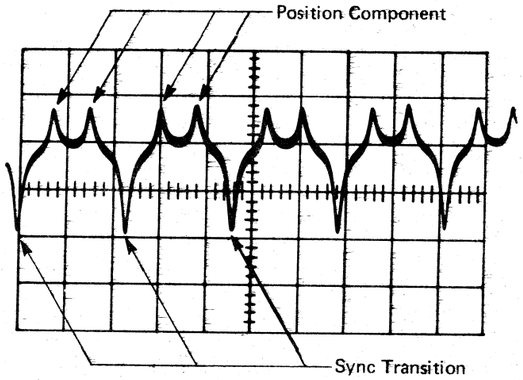


Figure 2 - Servo Input
(Carriage at Track 0)

Scope setup same as for Figure 1.
Sweep 1 μs/div
Trigger/Mode Norm/Add
Slope (−)
Ch 1 A1T2B04(S2B04)
0.05 volts/div, X1 probe
Ch 2 A1T2D04(S2D04)
0.05 volts/div, X1 probe
Invert

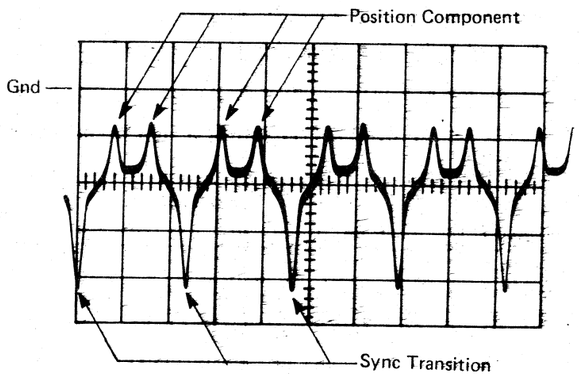


Figure 3 - Tribit Pattern
(Carriage at Track 0)

Sweep 1 μs/div.
Trigger
Slope (−)
Ch 1 Only
Ch 1 A1T2J04(S2J04)
0.2 volts/div, X10 probe

CHART A — POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1T2D03 (S2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1T2D05 (S2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1T2D06 (S2D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1T2B06 (S2B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1T2G11 (S2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A

Note 1: Insert Bobbin Push Rod (P/N 2304727) to move the carriage to the outer crash stop.

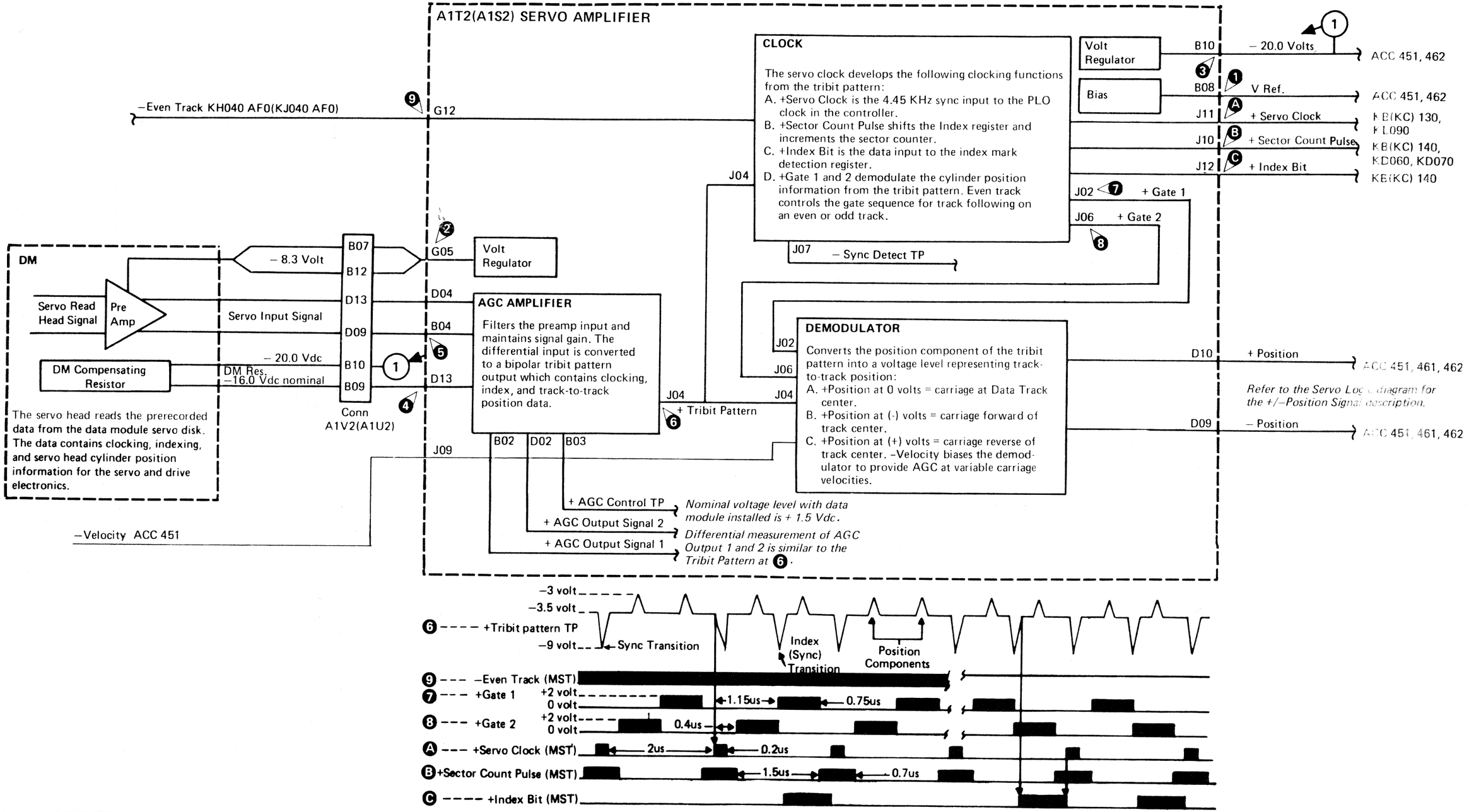
Note 2: Jumper A1T2G12 (S2G12) to Gnd (D08) to force to (+) MST Level.

Note 3: Use Bobbin Push Rod to manually move carriage. Ready lamp must be off.

DF0431 Seq. 2 of 2	2747185 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74			

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DF0441 Seq. 1 of 2	2747186 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440205 28 Jan 74	440214 17 Jun 74	440223 14 Mar 75

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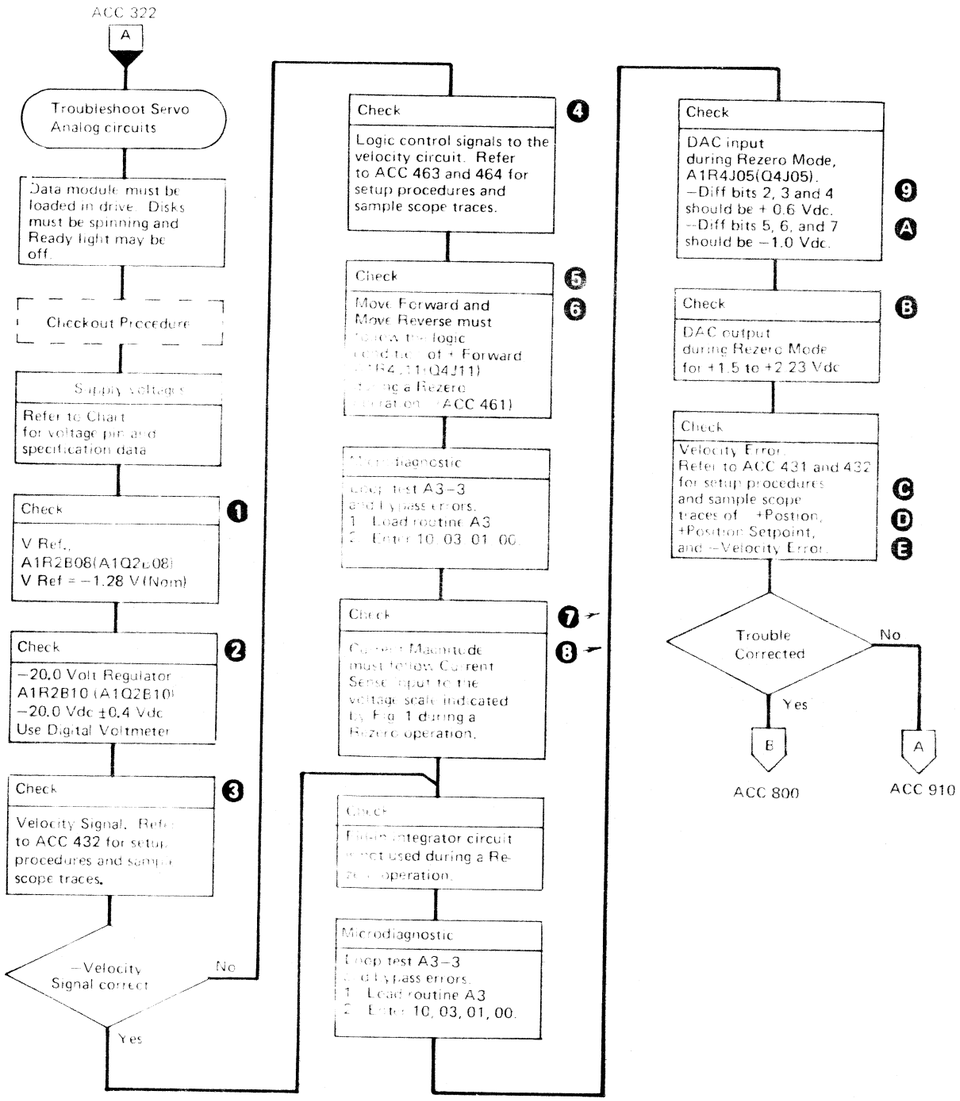
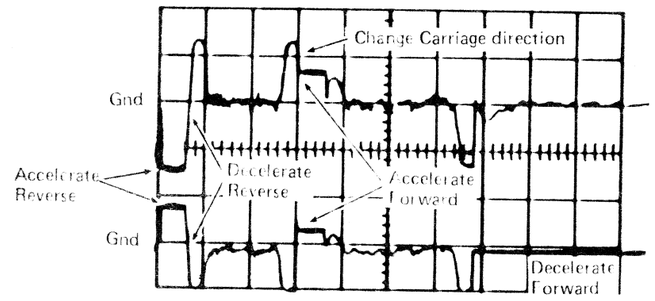


Figure 1. Current Sense/Current Magnitude

Microdiagnostic routine A3 test 3
1. Load routine A3
2. Enter 10, 03, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11 (N2G11)
+ Any rezero

Figure 1



(See ACC 451 for test points)

Ch 1 A1R2J11 (Q2J11)
Current Sense
8 Volts/div 0.5
Probe X10

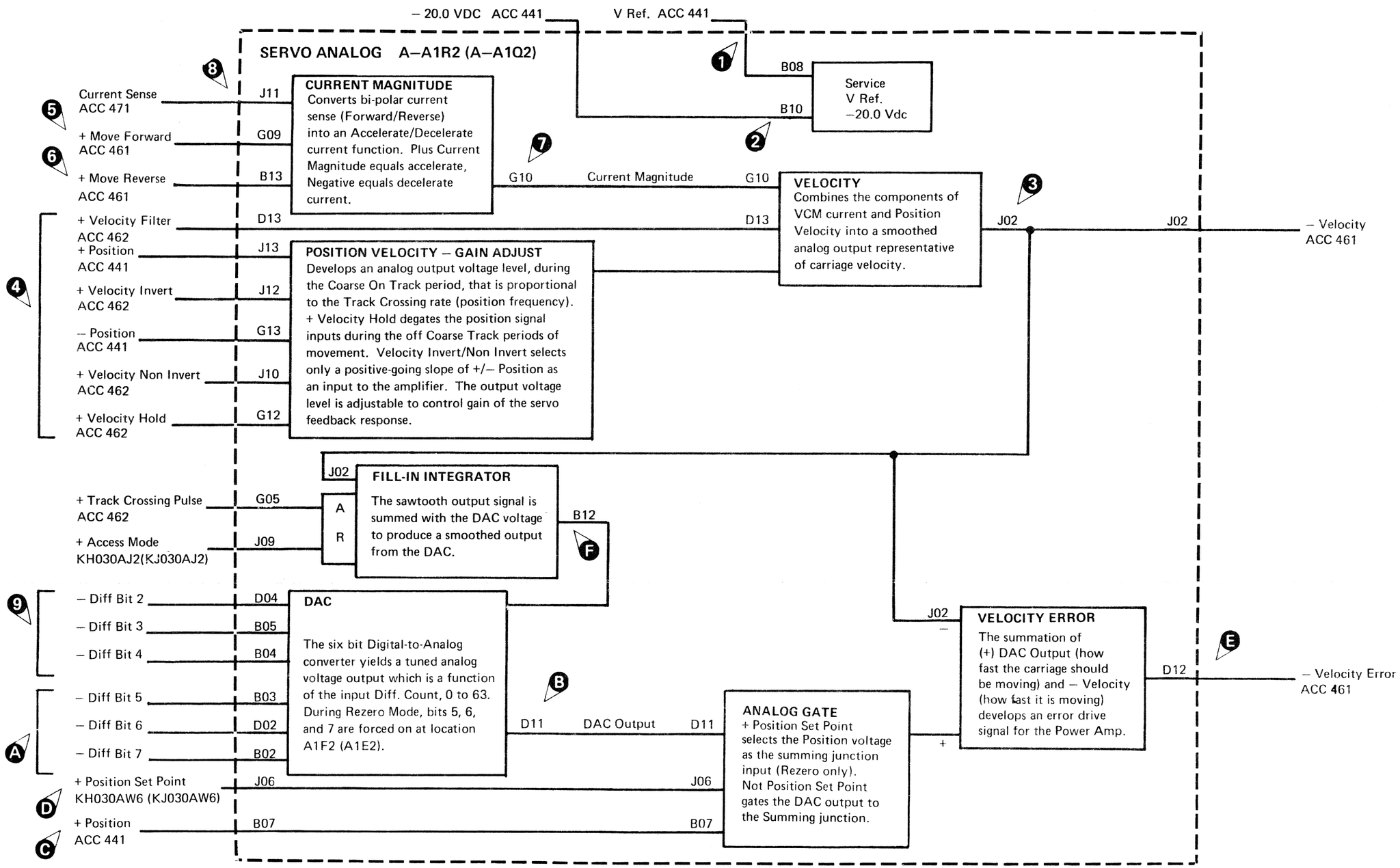
Ch 2 A1R2G10(Q2G10)
Current Magnitude
7 Volts/div 0.2
Probe X10

POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	PWR 50 A	PWR 250 A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	PWR 45 A	PWR 245 A
A1R2D06 (Q2D06)	−12.0 to −14.4 Vdc	PWR 40 A	PWR 240 A
A1R2G06 (Q2G06)	− 3.84 to − 4.16 Vdc	PWR 55 A	
	− 3.72 to − 4.4 Vdc		PWR 255 A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	PWR 60 A	PWR 260 A

DF0441	2747186	440200	440202	440203	440204	440205	440214	440223
Seq. 2 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	28 Jan 74	17 Jun 74	14 Mar 75

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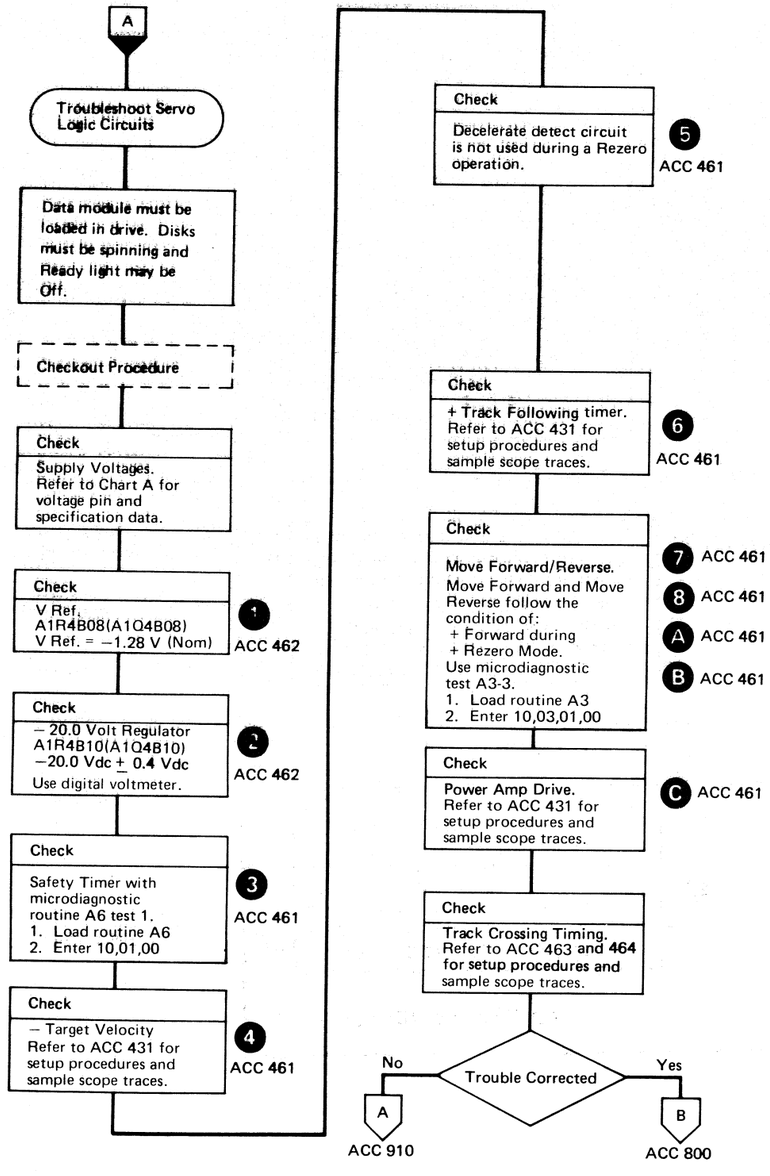


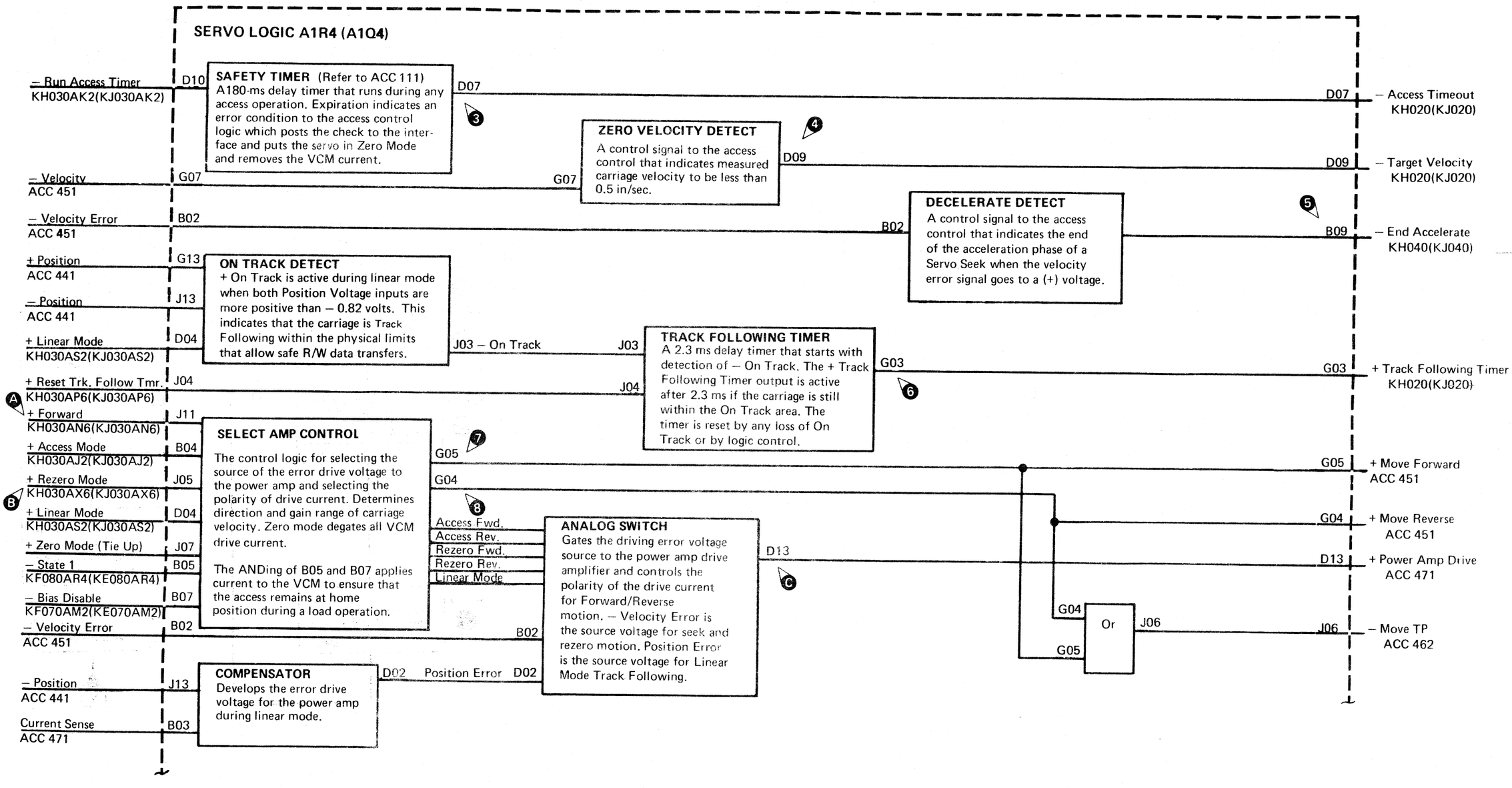
CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1R4D05 (A1Q4D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R4D06 (A1Q4D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R4B06 (A1Q4B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.40 Vdc		PWR 255-A
A1R4B11 (A1Q4B11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A

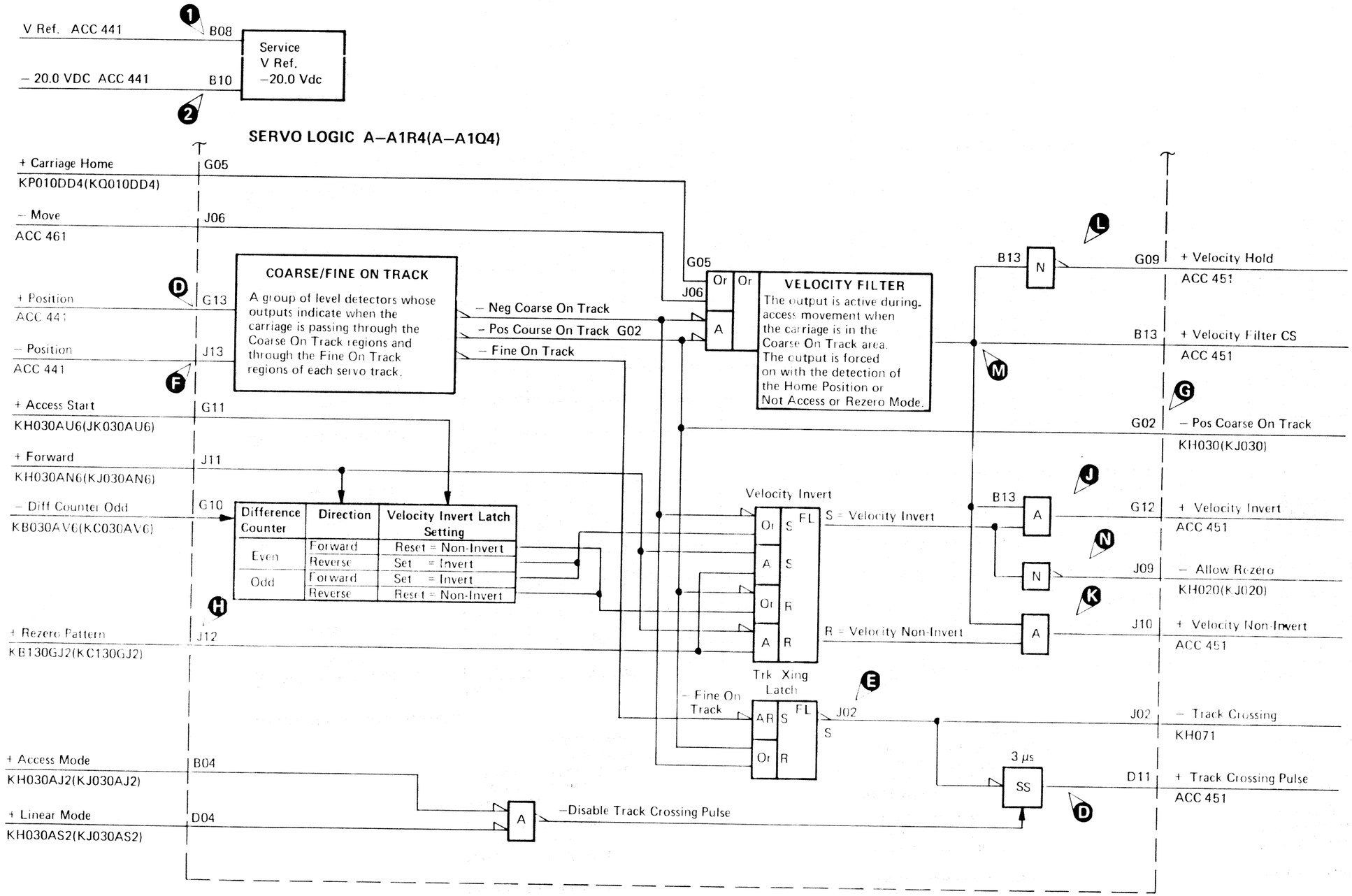
DF0460 Seq. 1 of 2	2747188 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440205 28 Jan 74	440212 29 Apr 74

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UNTIL DECEMBER 1973

TRACK CROSSING TIMING

Setup A - Rezero from Outer Stop

Microdiagnostic A6 test 5
1. Load routine A6
2. Enter 10, 05, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11(N2G11) + Any Rezero

Setup B - Rezero from Track 0

Microdiagnostic A3 test 3
1. Load routine A3
2. Enter 10,03,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope(+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Setup C - Rezero from Track 12

Microdiagnostic A4 test A
1. Load routine A4
2. Enter 10,0A,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

See ACC 461 and 462 for test points

Ⓓ Ch 1 A1R4G13(Q4G13) + Position
volts/div 0.5
probe X10

Ⓔ Ch 2 A1R4J02(Q4J02) – Track Crossing
volts/div 0.1
probe X10

Fig 1A

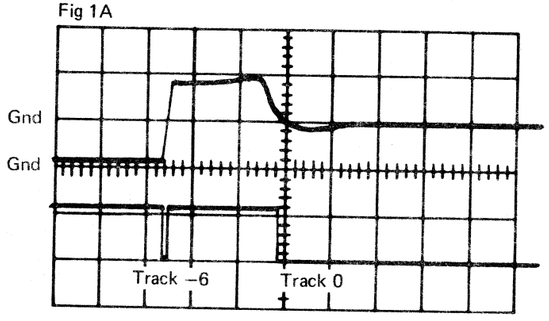


Fig 1B

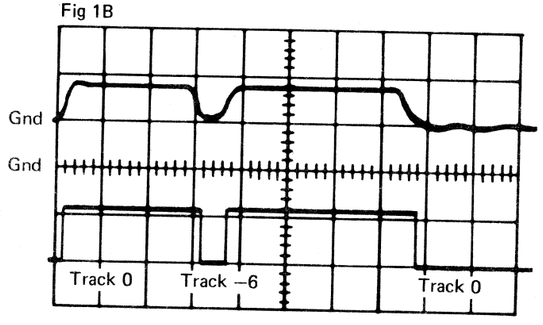
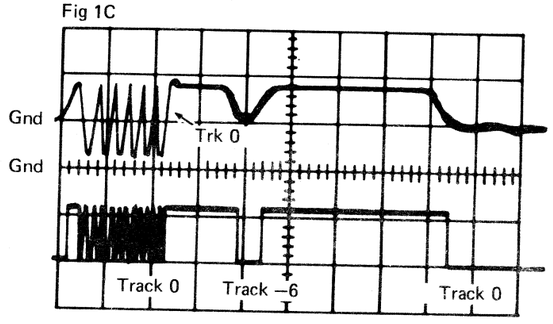


Fig 1C



Ⓕ Ch 1 A1R4J13(Q4J13) – Position
volts/div 0.5
probe X10

Ⓖ Ch 2 A1R4G02(Q4G02) – Pos Coarse On Track
volts/div 0.1
probe X10

Fig 2A

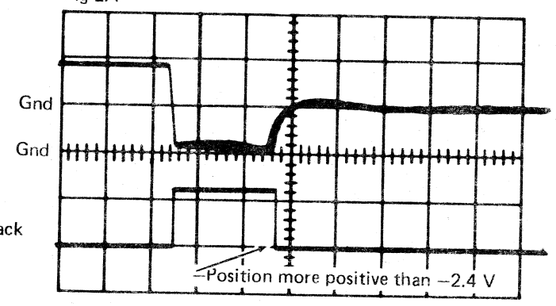


Fig 2B

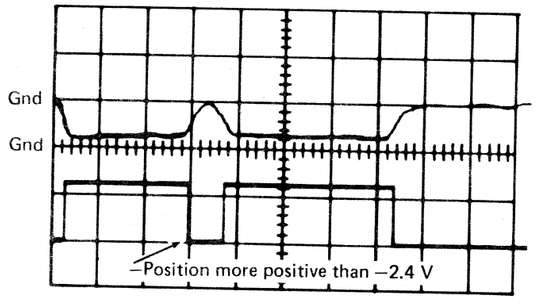
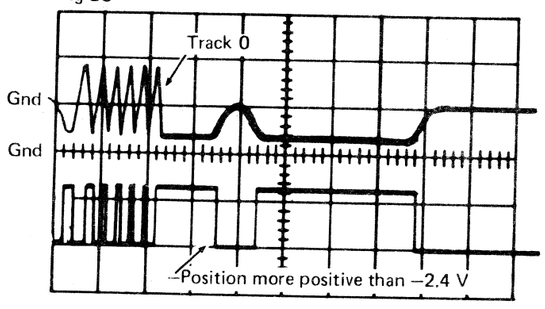


Fig 2C



Ⓗ Ch 1 A1R4J12(Q4J12) + Rezero Pattern
volts/div 0.1
probe X10

Ⓐ Ch 2 A1R4J11(Q4J11) + Forward
volts/div 0.1
probe X10

Fig 3A

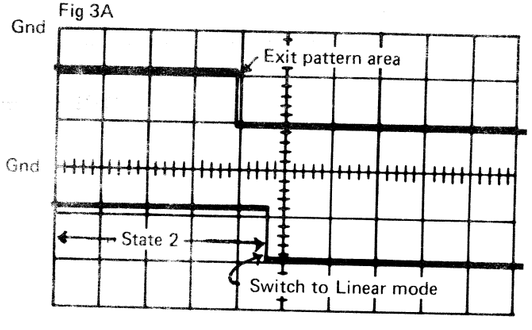


Fig 3B

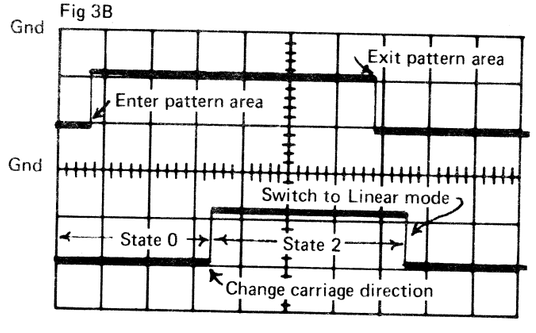
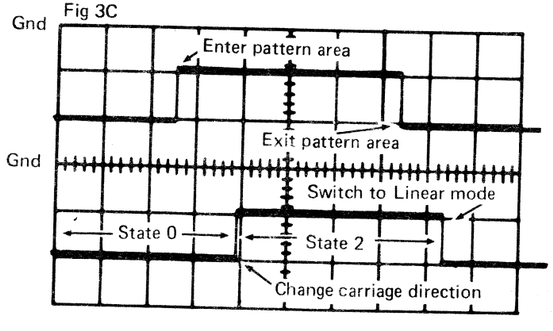


Fig 3C



DF0462 Seq. 2 of 2	2747189 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73			

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TRACK CROSSING TIMING

See ACC 462 for test points

Ⓙ Ch 1 A1R4G12(Q4G12)
+ Velocity Invert
volt/div 0.1
probe X10

Ⓚ Ch 2 A1R4J10(Q4J10)
+ Velocity Non-Invert
volt/div 0.1
probe X10

Ⓛ Ch 1 A1R4G09(Q4G09)
+ Velocity Hold
volt/div 0.1
probe X10

Ⓜ Ch 2 A1R4B13(Q4B13)
+ Velocity Filter CS
volt/div 0.1
probe X10

Ⓝ Ch 1 A1R4J09(Q4J09)
– Allow Rezero
volt/div 0.1
probe X10

Setup A - Rezero from Outer Stop

Microdiagnostic A6 test 5
1. Load routine A6
2. Enter 10, 05, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11(N2G11) + Any Rezero

Figure 4A

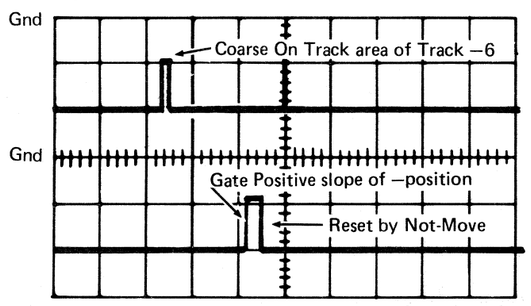


Figure 5A

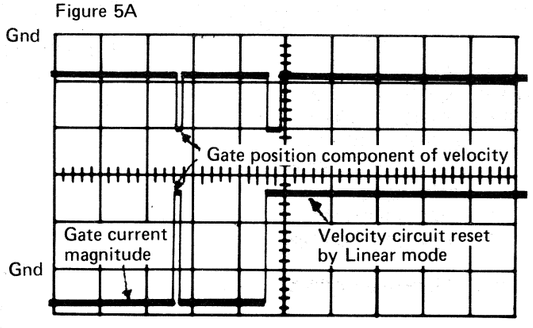
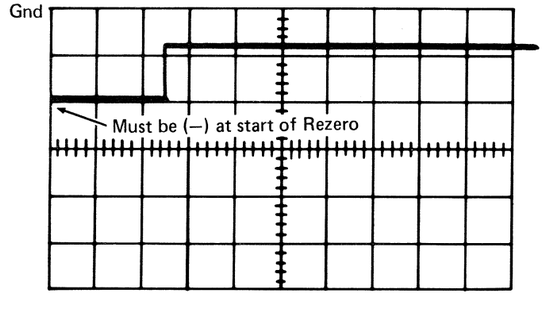


Figure 6A



Setup B - Rezero from Track 0

Microdiagnostic A3 test 3
1. Load routine A3
2. Enter 10, 03, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11(N2G11) + Any Rezero

Figure 4B

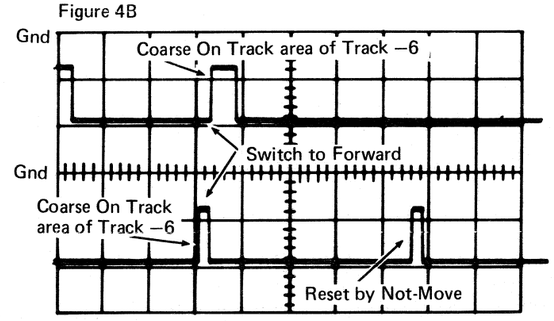


Figure 5B

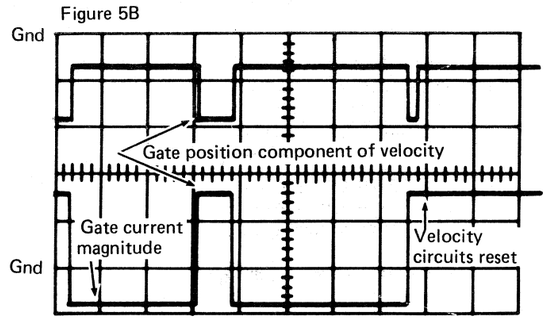
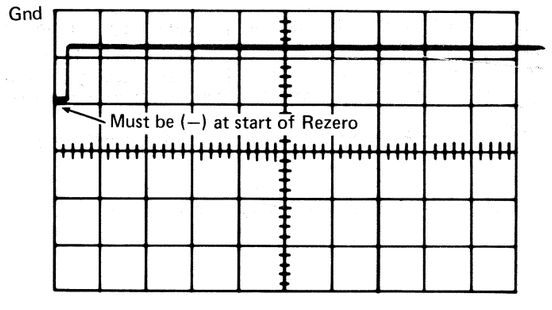


Figure 6B



Setup C - Rezero from Track 12

Microdiagnostic A4 test A
1. Load routine A4
2. Enter 10, 0A, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext
Sync: A1P2G11(N2G11) + Any Rezero

Figure 4C

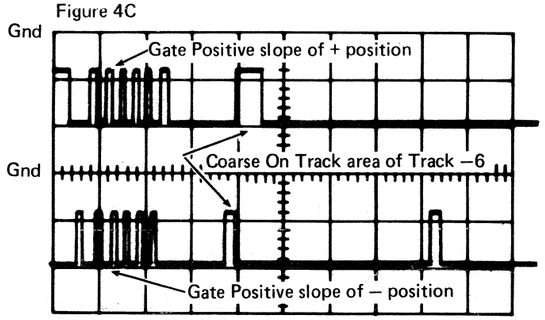


Figure 5C

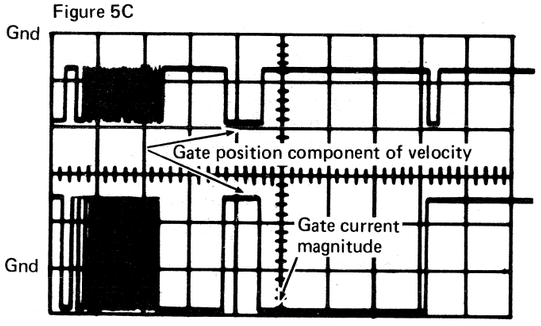
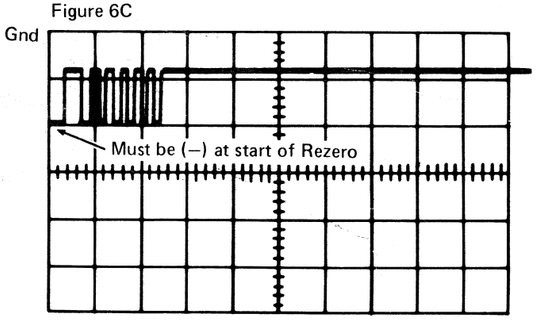
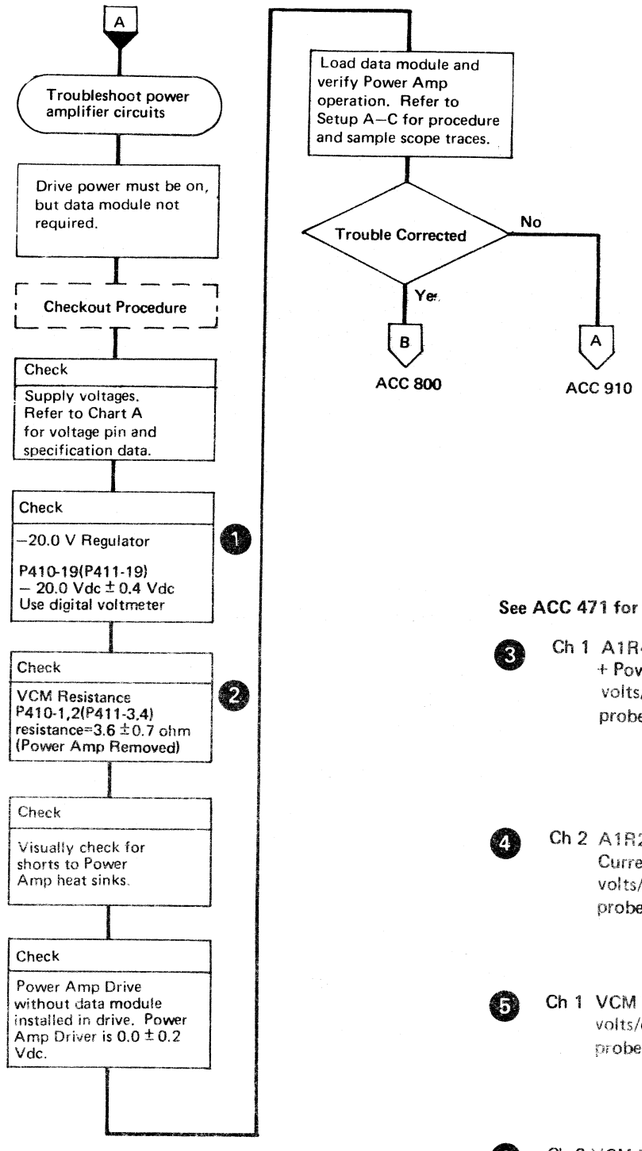


Figure 6C



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See ACC 471 for test points

3 Ch 1 A1R4D13(Q4D13)
+ Power Amp Drive
volts/div 0.5
probe X10

4 Ch 2 A1R2J11(Q2J11)
Current Sense
volts/div 0.5
probe X10

5 Ch 1 VCM TB-A
volts/div 2.0
probe X10

6 Ch 2 VCM TB-B
volts/div 2.0
probe X10
Invert
Mode: Added

CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
P410–7,8 (P411–7,8)	–36.0 to –43.2 Vdc	PWR 80-A	PWR 280-A
P410–14 (P411–14)	–12.0 to –14.4 Vdc	PWR 40-A	PWR 240-A
P410–16 (P411–16)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A

Setup A - Rezero from Outer Stop

Microdiagnostic A6 test 5
1. Load routine A6
2. Enter 10,05,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Setup B - Rezero from Track 0

Microdiagnostic A3 test 3
1. Load routine A3
2. Enter 10, 03, 01, 00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Setup C - Rezero from Track 12

Microdiagnostic A4 test A
1. Load routine A4
2. Enter 10,0A,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2G11(N2G11) + Any Rezero

Fig 1A

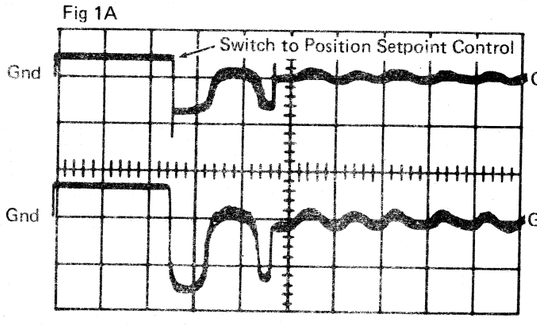


Fig 1B

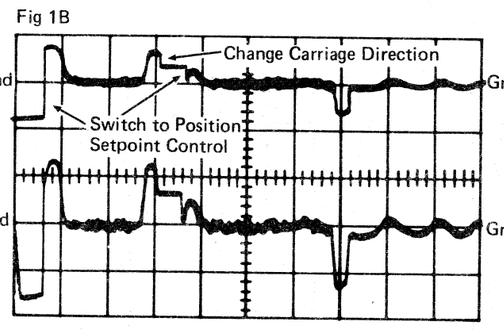


Fig 1C

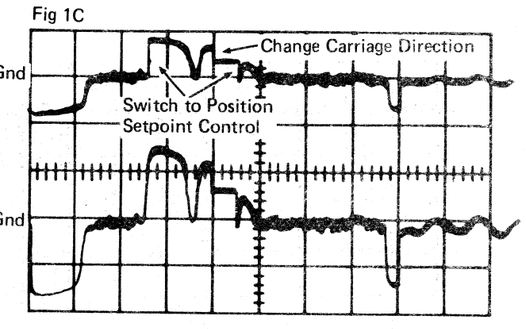


Fig 2A

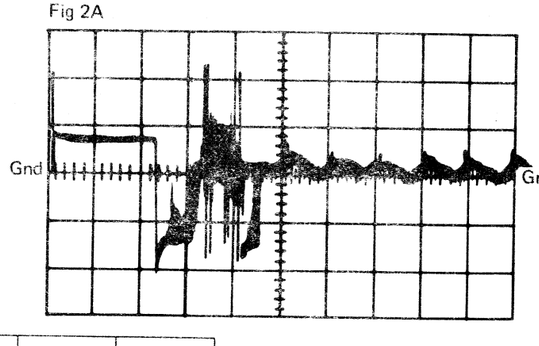


Fig 2B

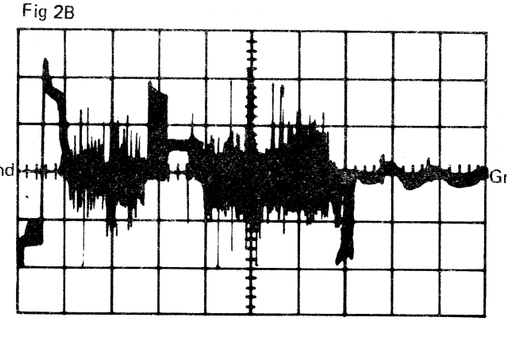
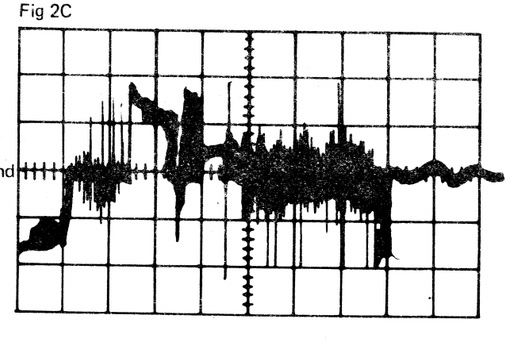
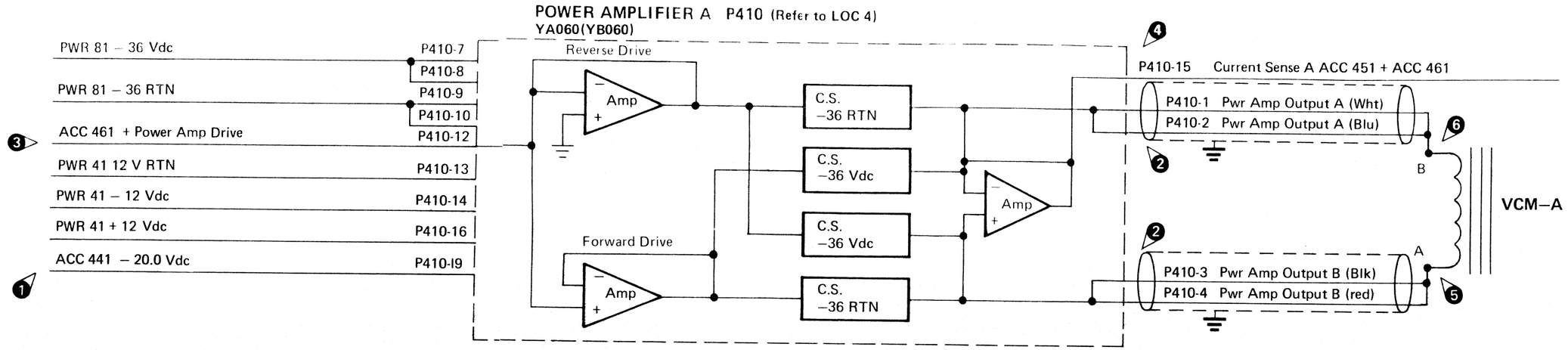
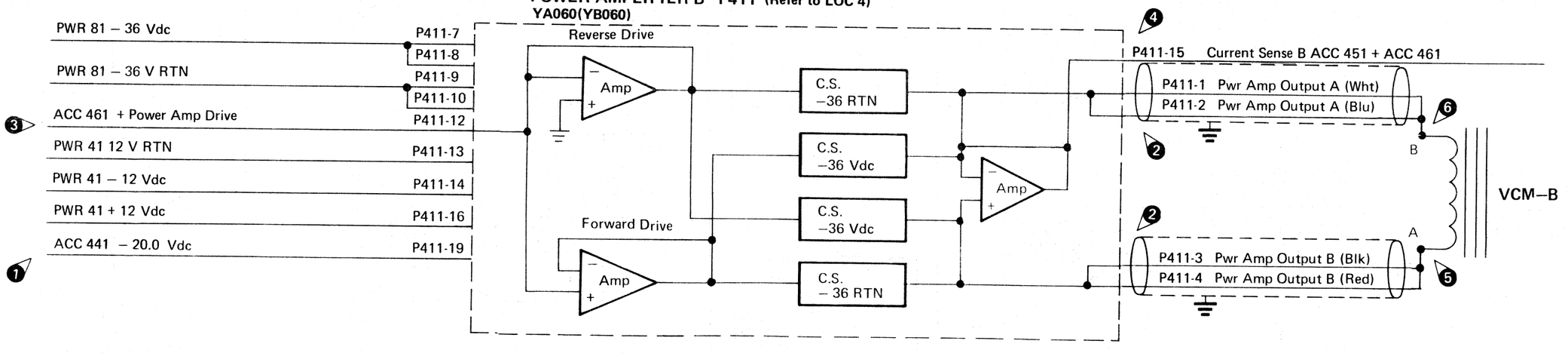


Fig 2C



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DF0470 Seq 1 of 2	2747625 Part No. ( )	440202 25 Jun 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440223 14 Mar 75		

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SEEK – VERIFICATION CHECK

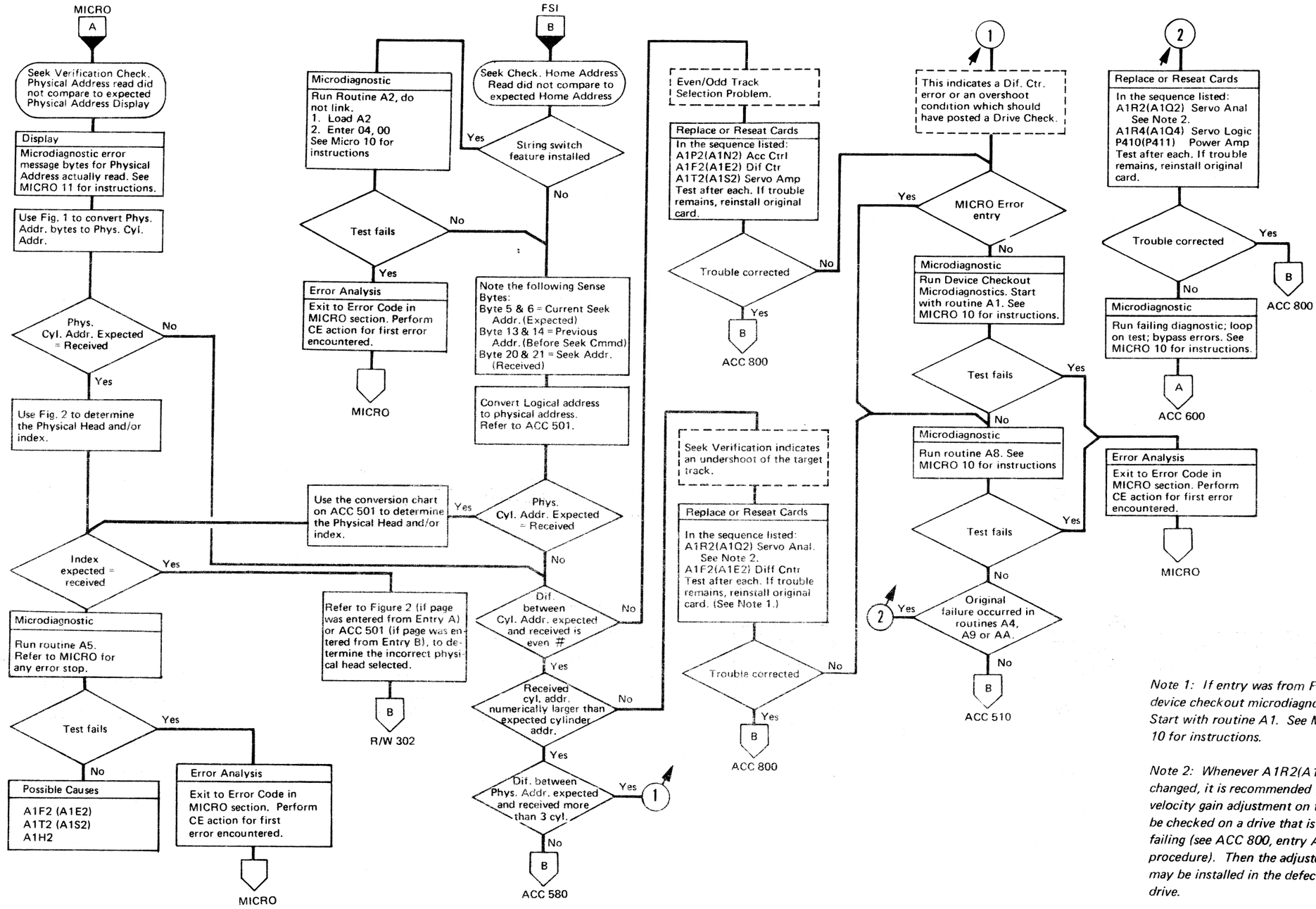


Figure 1. Physical Address Bytes

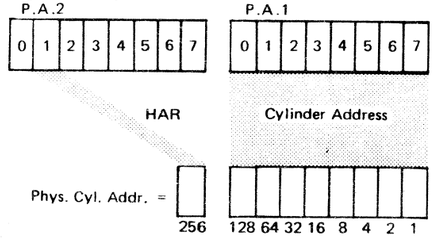
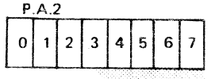


Figure 2. HAR Conversion Chart



HAR	PHYS HEAD	INDEX
00	0	Even
01	0	Odd
02	1	Even
03	1	Odd
04	2	Even
05	2	Odd
06	3	Even
07	3	Odd
08	4	Even
09	4	Odd
0A	5	Even
0B	5	Odd
0C	6*	Even
0D	6*	Odd
0E	7*	Even
0F	7*	Odd
10	8*	Even
11	8*	Odd
12	9*	Even
13	9*	Odd
14	10*	Even
15	10*	Odd
16	11*	Even
17	11*	Odd

* 70 Mb Data Module Only

Note 1: If entry was from FSI, run device checkout microdiagnostics. Start with routine A1. See MICRO 10 for instructions.

Note 2: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

DF0470 Seq. 2 of 2	2747625 Part No. ( )	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440223 14 Mar 75		

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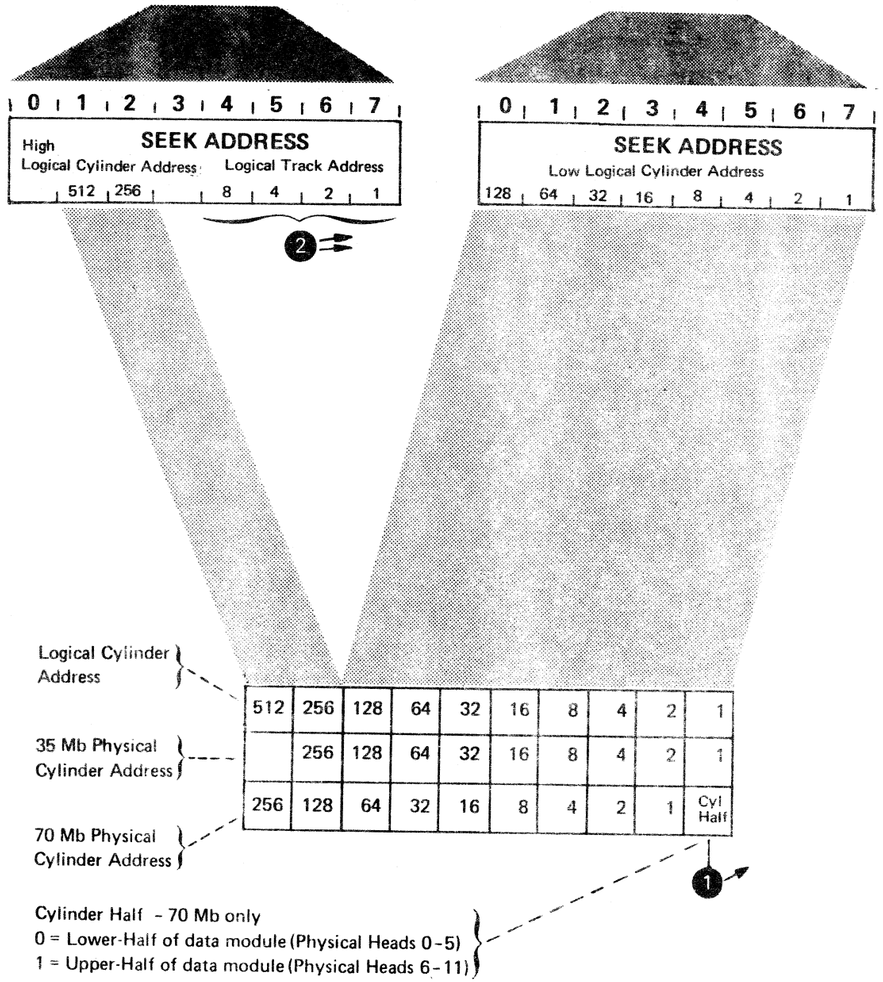
SENSE BYTE – CYLINDER AND HEAD CONVERSION CHARTS

LOGICAL CYLINDER ADDRESS

Sense Byte 6 — **CURRENT SEEK ADDRESS** — Sense Byte 5

Sense Byte 14 — **PREVIOUS SEEK ADDRESS** — Sense Byte 13

Sense Byte 21 — **RECEIVED SEEK ADDRESS** — Sense Byte 20



PHYSICAL HEAD CONVERSION

35 Mb Data Module

LOGICAL TRACK	PHYSICAL HEAD	INDEX
0	0	Even
1	0	Odd
2	1	Even
3	1	Odd
4	2	Even
5	2	Odd
6	3	Even
7	3	Odd
8	4	Even
9	4	Odd
A	5	Even
B	5	Odd

70 Mb Data Module

1. Note the Low Logical Cylinder Byte, bit 7 (1)
2. Note the Logical Track Address (2)
3. Find the Physical Head and Index on the same line as 1 and 2.

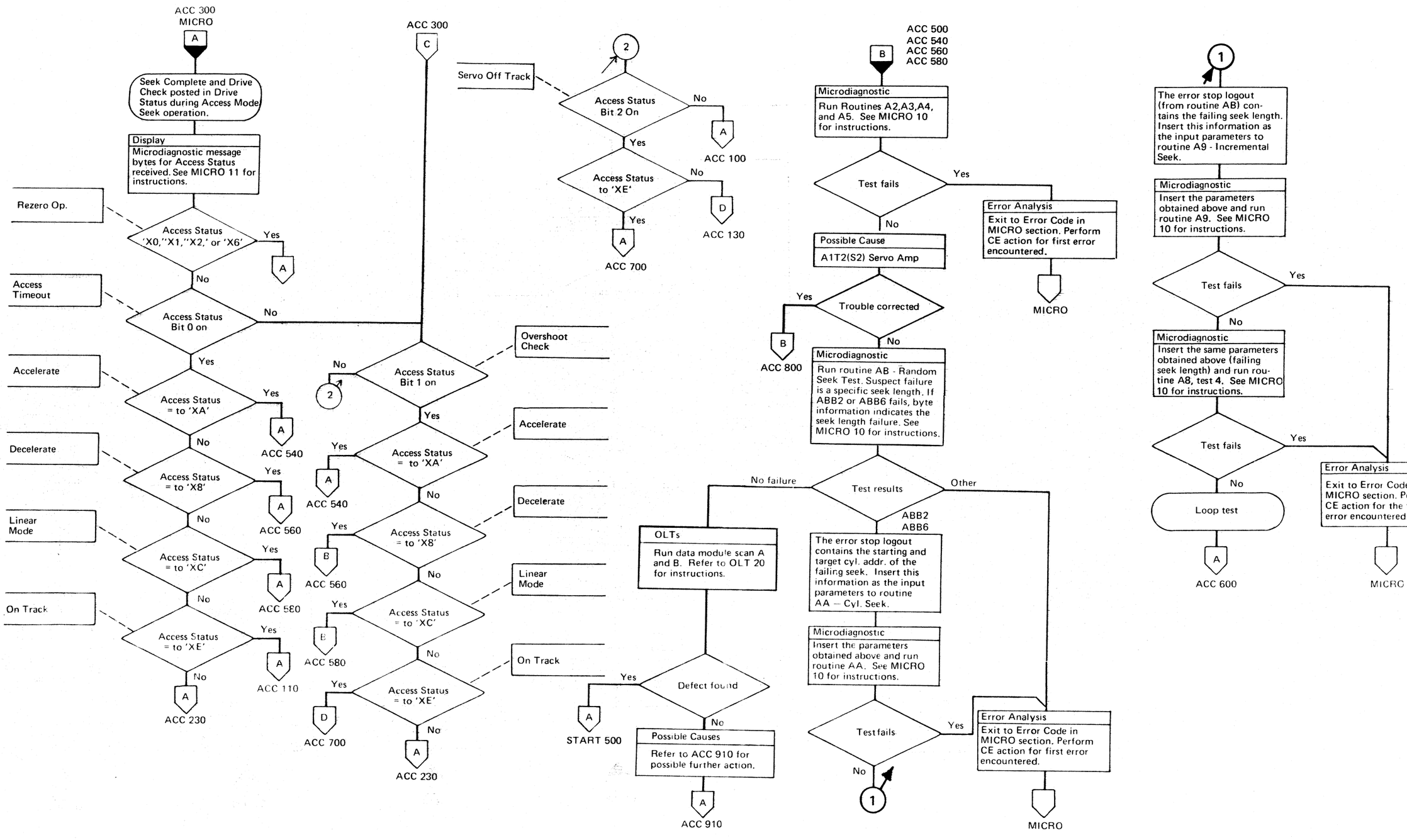
LOGICAL CYL BIT 7	LOGICAL TRACK	PHYSICAL HEAD	INDEX
0	0	0	Even
0	1	0	Odd
0	2	1	Even
0	3	1	Odd
0	4	2	Even
0	5	2	Odd
0	6	3	Even
0	7	3	Odd
0	8	4	Even
0	9	4	Odd
0	A	5	Even
0	B	5	Odd
1	0	6	Even
1	1	6	Odd
1	2	7	Even
1	3	7	Odd
1	4	8	Even
1	5	8	Odd
1	6	9	Even
1	7	9	Odd
1	8	10	Even
1	9	10	Odd
1	A	11	Even
1	B	11	Odd

DM Size Chart

Sense Byte 2 Bit 6 and 7		DM Size
0	0	Parity Error (not used)
0	1	35 Mb
1	0	70 Mb
1	1	Parity Error (not used)

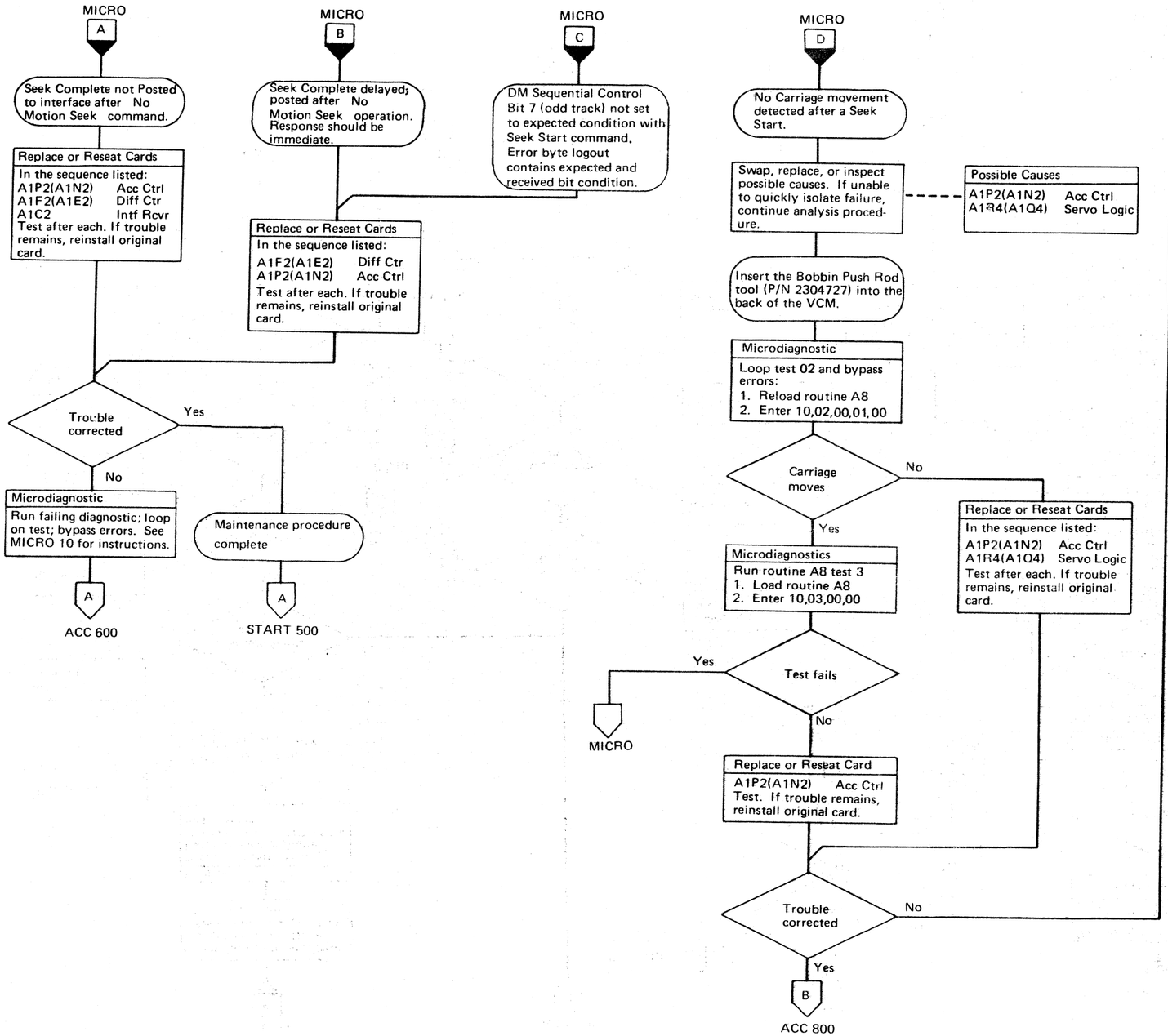
© Copyright IBM Corporation 1973, 1974

SEEK – INITIAL ANALYSIS



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SEEK – START SELECTION AND MOVEMENT



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SEEK – DIFFERENCE COUNTER CONTROL

SEEK – DIFFERENCE COUNTER CONTROL

MICRO A

Difference Counter value received did not compare with the value expected

Possible Causes

Swap, replace, or inspect possible causes. If unable to quickly isolate failure, continue analysis procedure

Possible Causes

A1F2(A1E2) Diff Cntr.
A1R4(A1Q4) Servo Logic
A1P2(A1N2) Access Cntrl

Display

Microdiagnostic message bytes 2, 3 and 4 for the Received, Expected, and Original Diff Cntr values. See MICRO 11 for instructions.

Subtract expected value from original value

Difference Equals 1

No

Yes

Cycle test several times to see if the error stop logout bytes indicate a consistent failing bit pattern.

Failure is consistent with a unique bit combination

No or unknown

Yes

Failure occurred at first track crossing of Seek operation

Replace or Reseat Cards

In the Sequence listed.
A1R4(A1Q4) Servo Logic
A1F2(A1E2) Diff Cntr
A1P2(A1N2) Access Cntrl
Test after each, if trouble remains, reinstall original card.

Replace or Reseat Cards

A1F2(A1E2) Diff Cntr
If trouble remains, reinstall original card.

Replace or Reseat Cards

In the Sequence listed.
A1R4 (A1Q4) Servo Logic
A1F2(A1E2) Diff Cntr.
Test after each. If trouble remains, reinstall original card.

Trouble corrected

Yes

No

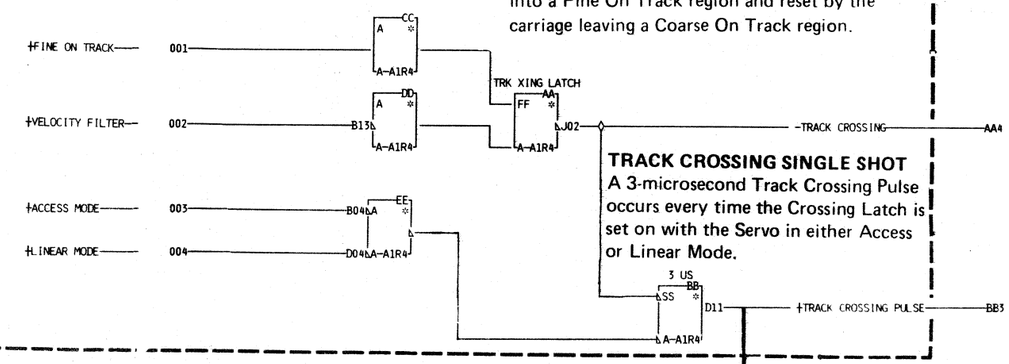
B

ACC 800

Use the description and diagram on this page to isolate problem.

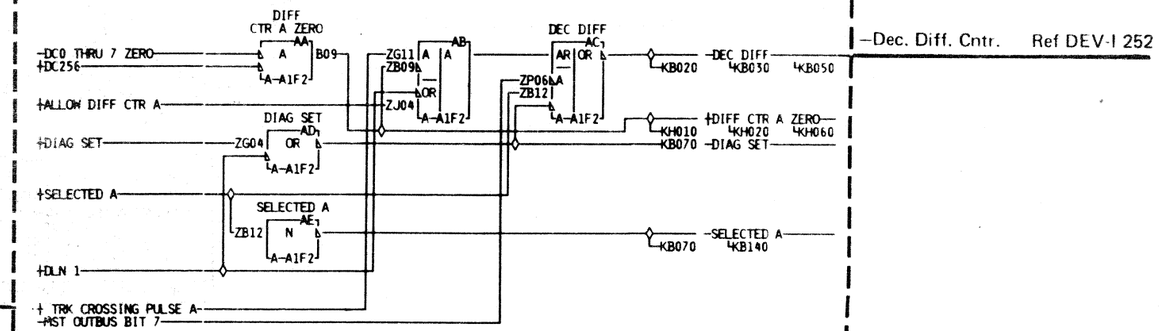
A1R4 (A1Q4)
LA400 (LB400)
Ref ACC 652

TRACK CROSSING LATCH
The Track Crossing Latch line is set on with entry into a Fine On Track region and reset by the carriage leaving a Coarse On Track region.



TRACK CROSSING SINGLE SHOT
A 3-microsecond Track Crossing Pulse occurs every time the Crossing Latch is set on with the Servo in either Access or Linear Mode.

A1F2 (A1E2)
KBxxx (KCxxx)



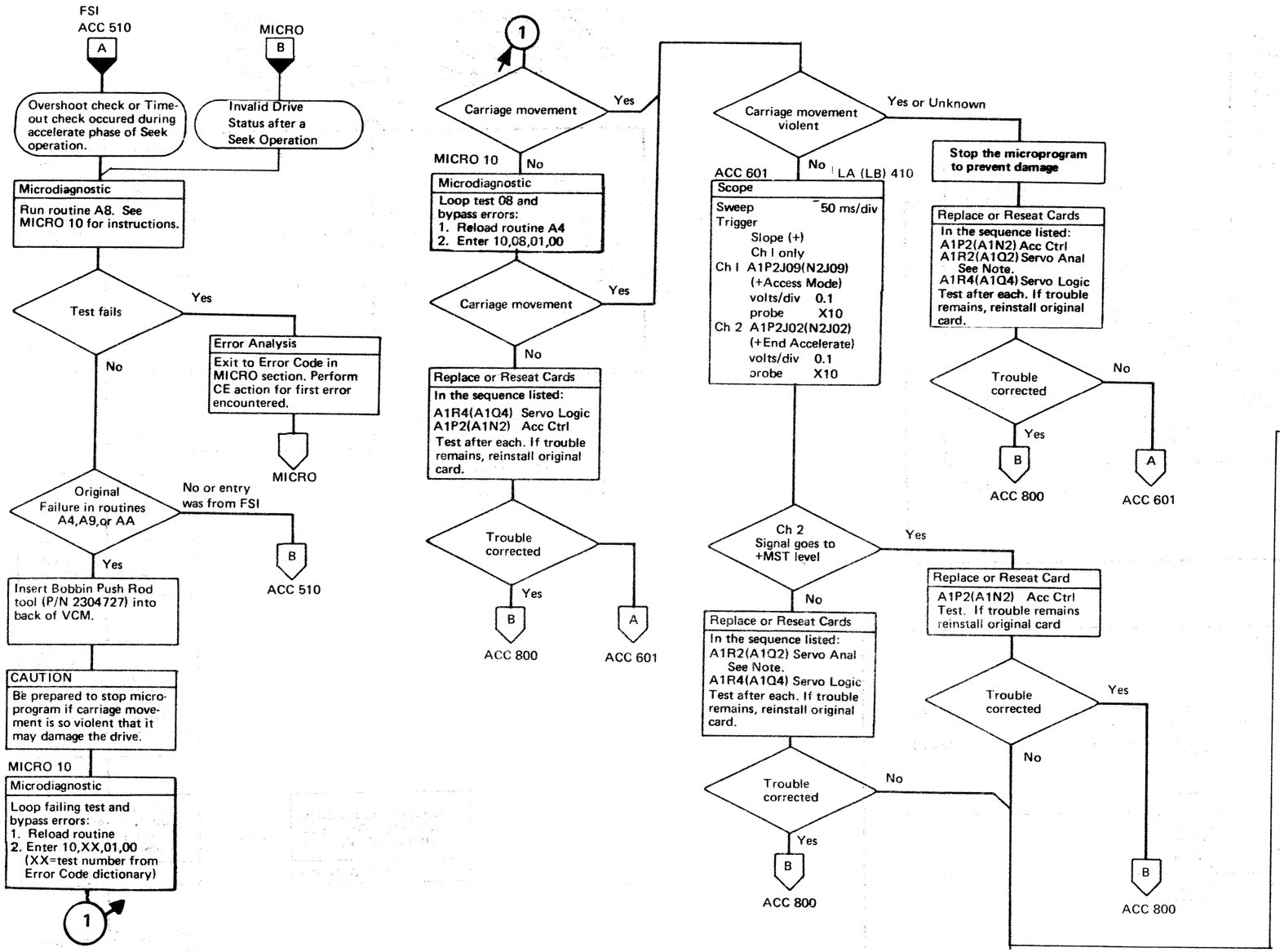
DIFFERENCE COUNTER DECREMENT
Track Crossing pulses are gated into the Difference Counter by +ALLOW DIFFERENCE COUNTER and by a minus (–) level at B09 (Difference Counter not zero).

During a Seek operation, the Difference Counter is decremented by one every time the Servo head crosses over a track.

DF0530	2747192	440200	440202	440203	440209	440214	440223	
Seq. 1 of 2	Part No. ( )	25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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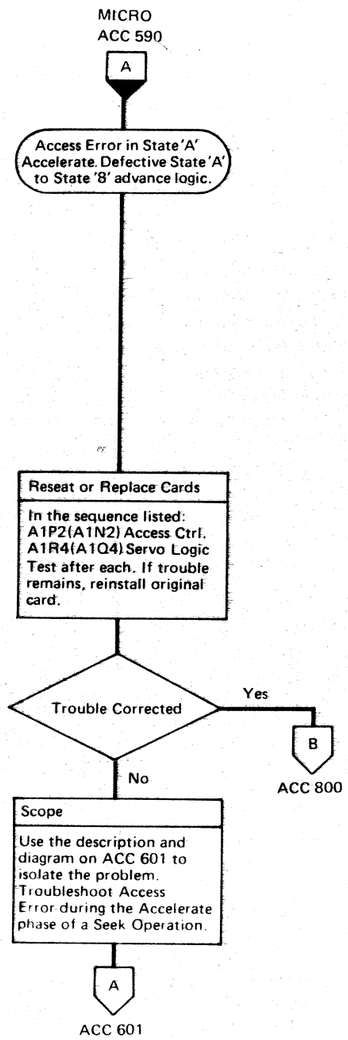
SEEK – STATE A ACCESS ERROR



Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (See ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

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SEEK-STATE A ACCESS ERROR



DF0541	2747193	440200	440202	440203	440204	440209	440214	440223
Seq. 1 of 2	Rel. No. 1.1	25 Jun 73	7 Sept 73	2 Nov 73	21 Dec 73	25 Mar 74	17 Jun 74	14 Mar 75

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SEEK – STATE A ACCELERATE TIME

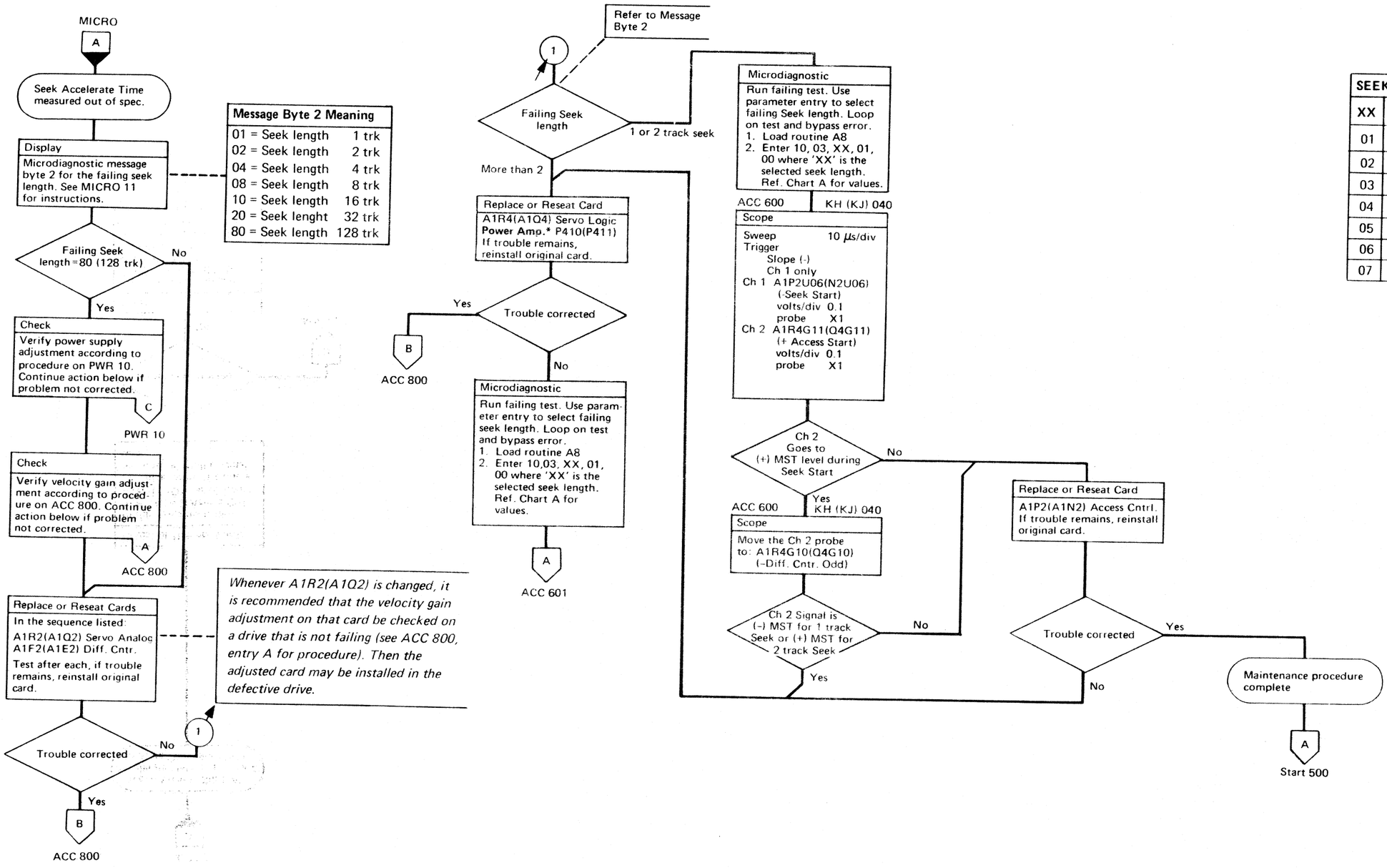


Chart A

SEEK LENGTH PARAMETER ENTRY	
XX	**Seek Length**
01	128 Track
02	32 Track
03	16 Track
04	8 Track
05	4 Track
06	2 Track
07	1 Track

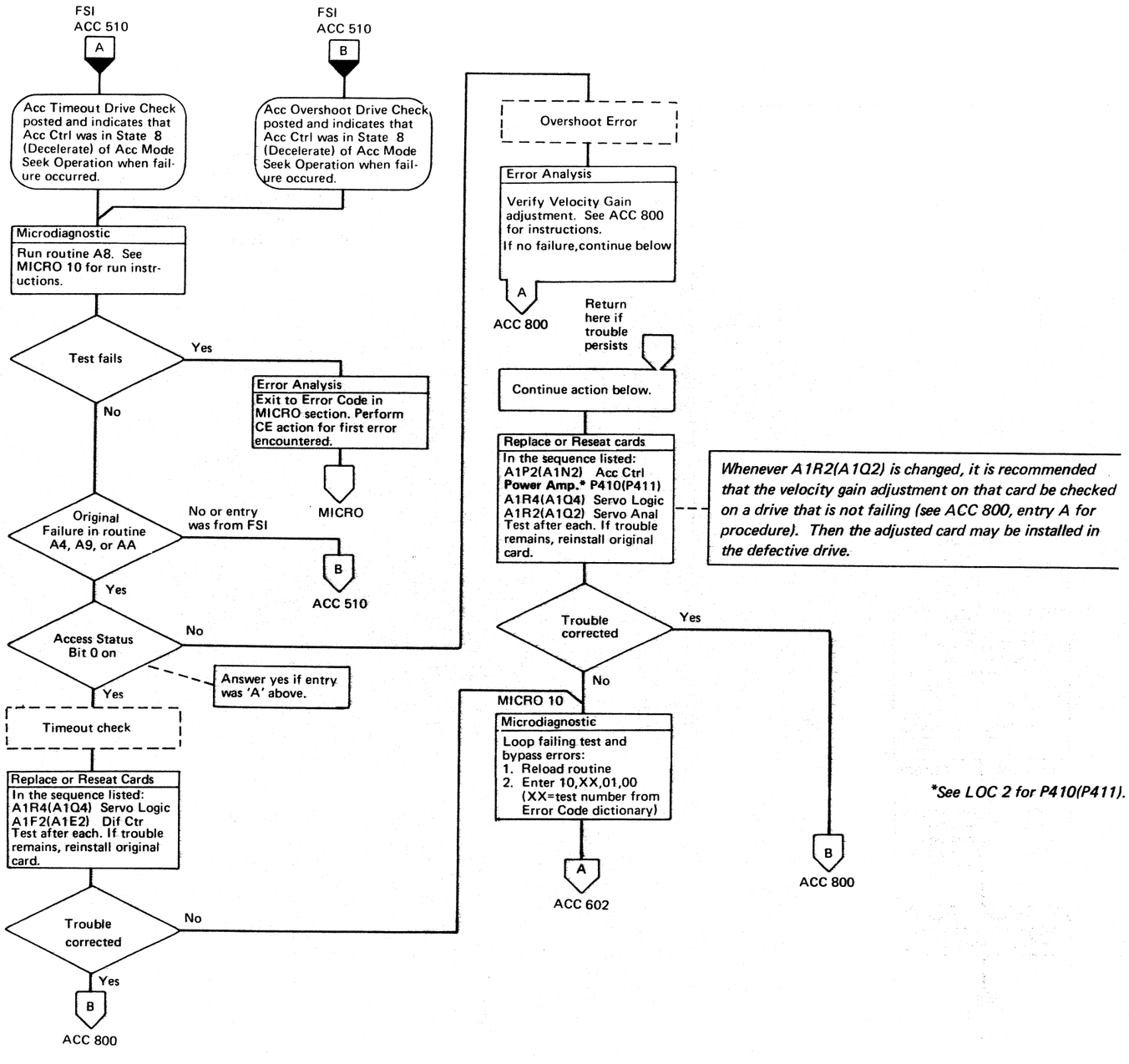
**See LOC 2 for P410(P411).*

DF0541 Seq. 2 of 2	2747193 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440214 17 Jun 74	440223 14 Mar 75

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SEEK – STATE 8 ACCESS ERROR



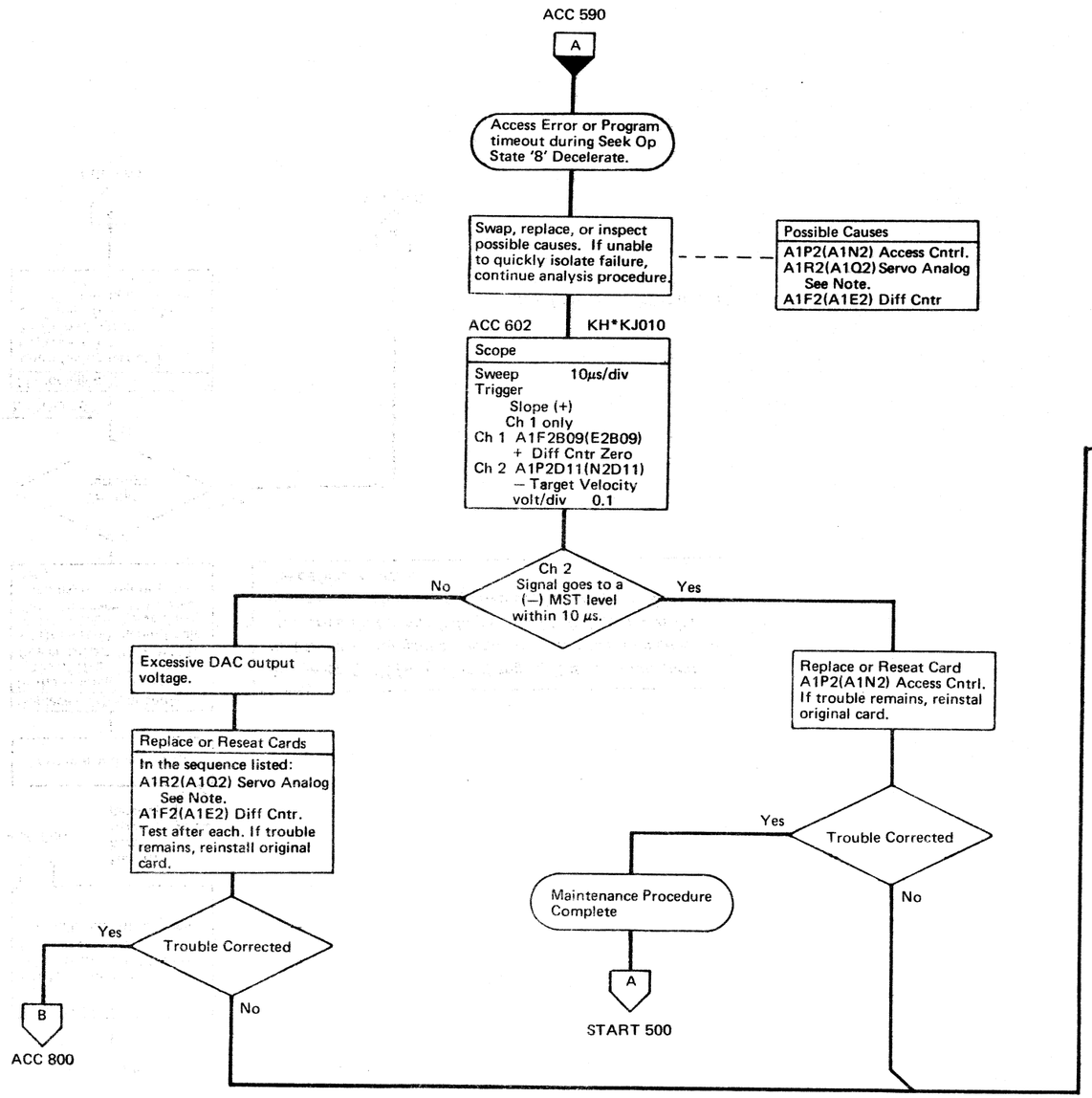
Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

**See LOC 2 for P410(P411).*

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SEEK – STATE 8 ACCESS ERROR

SEEK – STATE 8 ACCESS ERROR



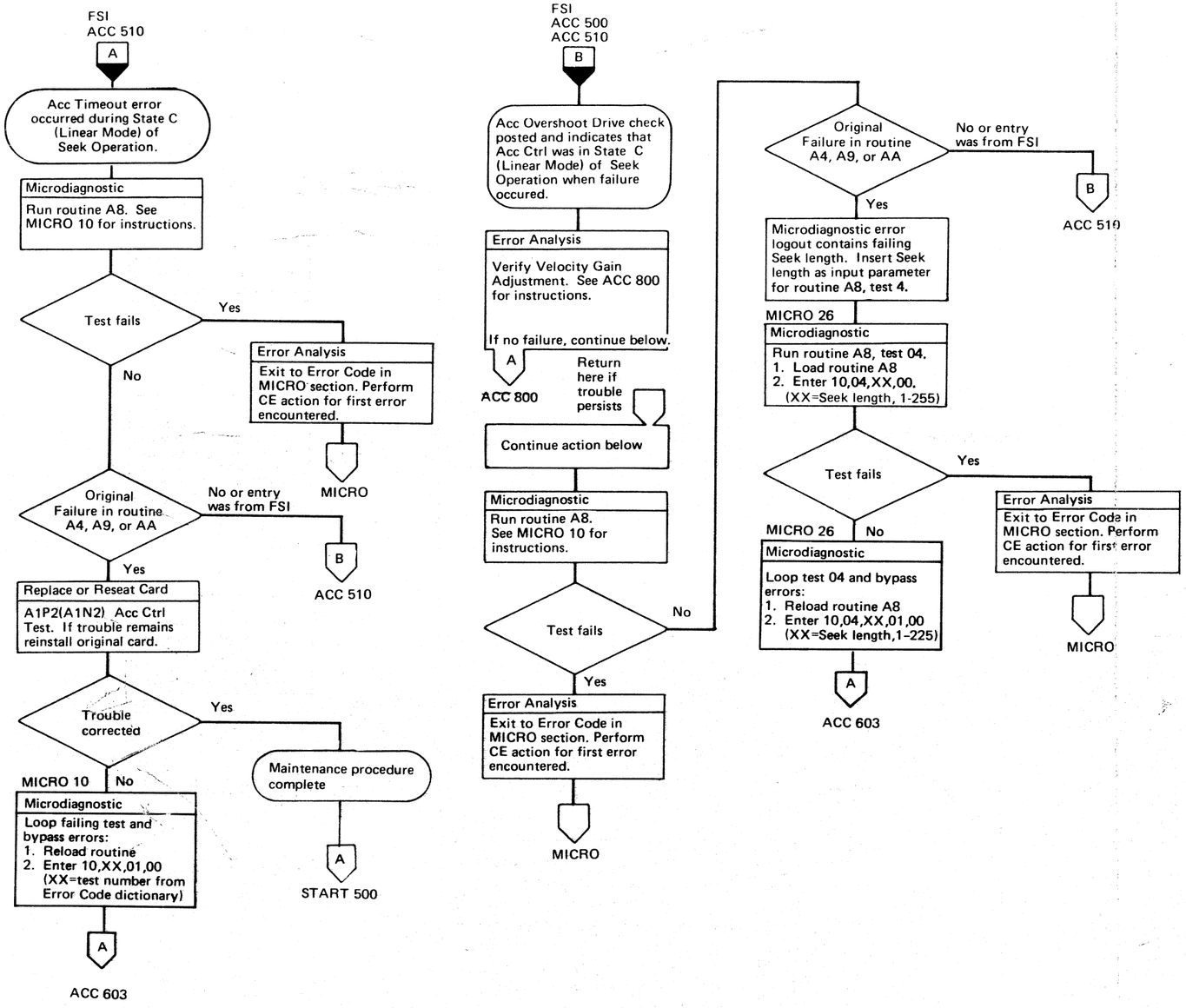
Note: Whenever A1R2(A1Q2) is changed, it is recommended that the velocity gain adjustment on that card be checked on a drive that is not failing (see ACC 800, entry A for procedure). Then the adjusted card may be installed in the defective drive.

DF0560	2747194
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440209	440223		
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	14 Mar 75		

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SEEK – STATE C ACCESS ERROR

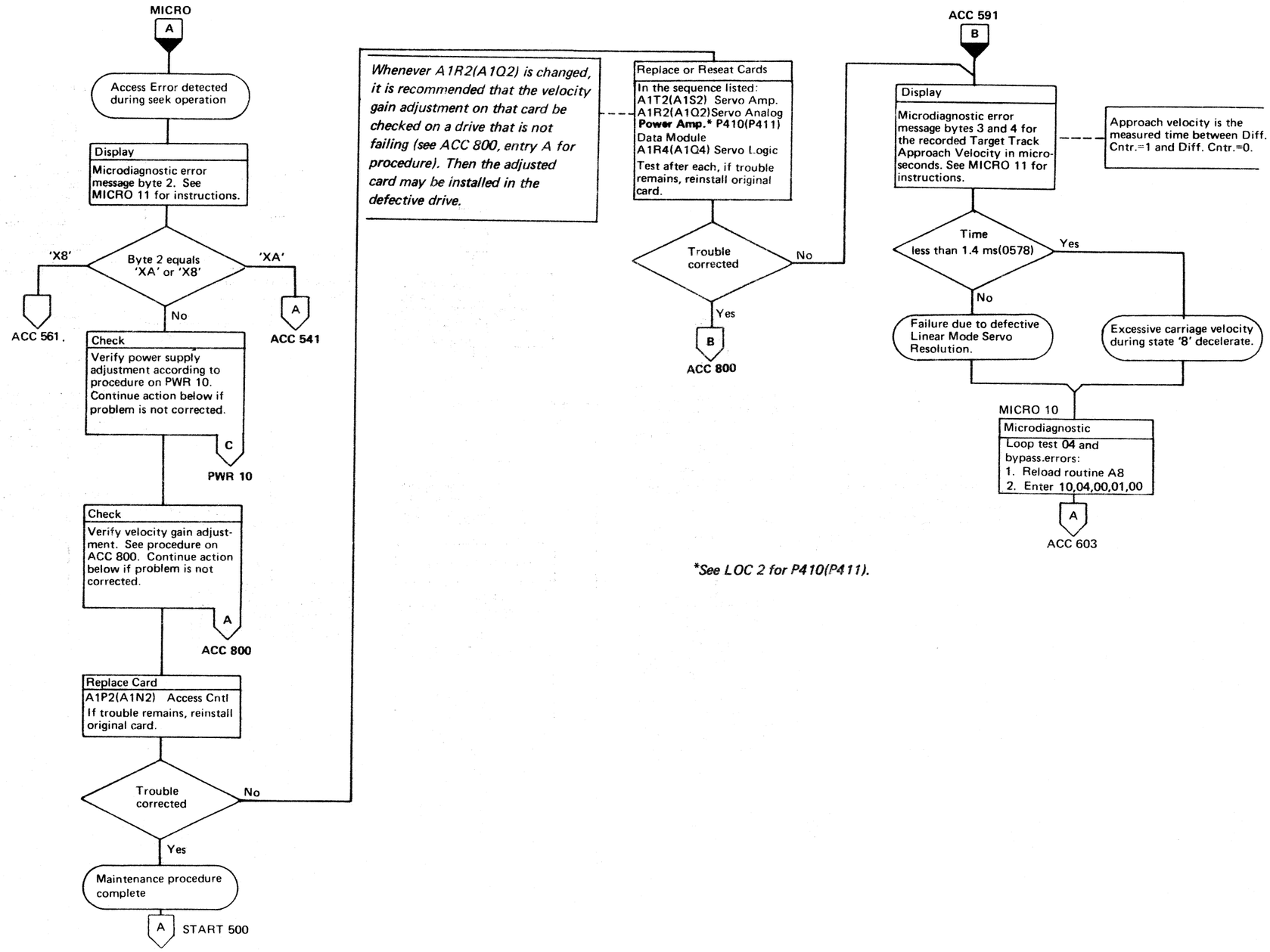


DF0590 Seq. 1 of 2	2747196 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440214 17 Jun 74	440223 14 Mar 75

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SEEK – STATE C CAPTURE VELOCITY



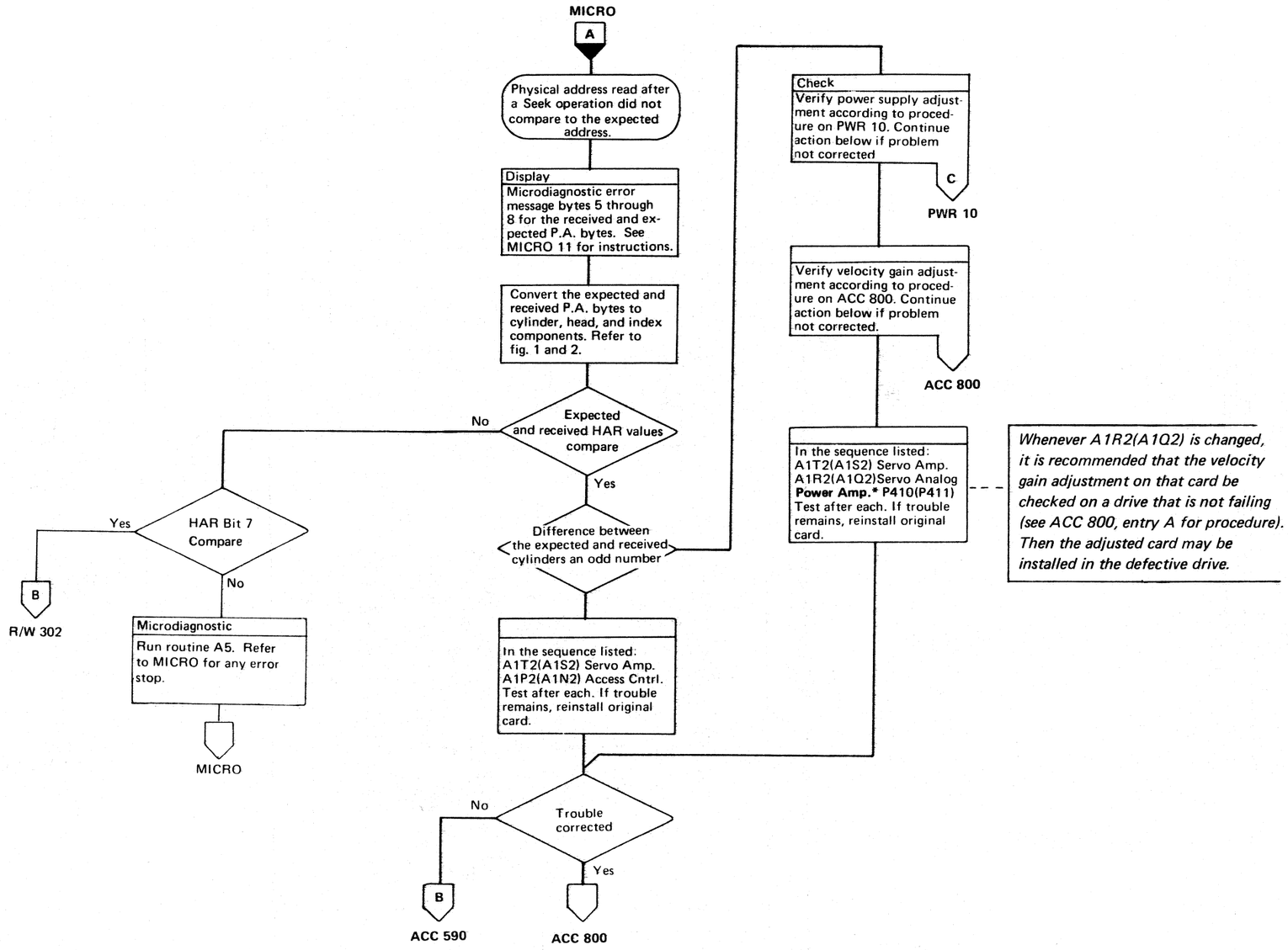
*See LOC 2 for P410(P411).

DF0590	2747196
Seq. 2 of 2	Part No. ( )

440200	440202	440203	440209	440214	440223	
25 Jun 73	7 Sept 73	2 Nov 73	25 Mar 74	17 Jun 74	14 Mar 75	

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SEEK – STATE C CAPTURE VELOCITY



*See LOC 2 for P410(P411).

Figure 1. Physical Address Bytes

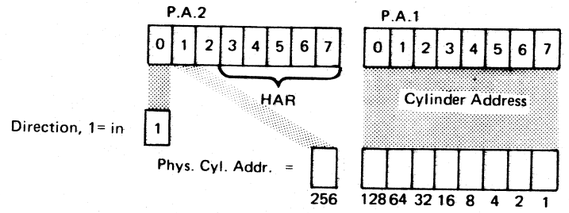
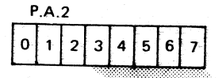


Figure 2. HAR Conversion Chart



HAR	PHYS HEAD	INDEX
00	0	Even
01	0	Odd
02	1	Even
03	1	Odd
04	2	Even
05	2	Odd
06	3	Even
07	3	Odd
08	4	Even
09	4	Odd
0A	5	Even
0B	5	Odd
0C	6*	Even
0D	6*	Odd
0E	7*	Even
0F	7*	Odd
10	8*	Even
11	8*	Odd
12	9*	Even
13	9*	Odd
14	10*	Even
15	10*	Odd
16	11*	Even
17	11*	Odd

*70 Mb Data Module Only

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SEEK OPERATION DIAGRAM

ACC 407
ACC 500
ACC 510
ACC 520

A

Defective Seek

Check entire Seek Operation according to the following procedures.

Verify Supply Voltages

Refer to ACC 420, Chart A for voltage pin and specification data.
Repair or replace as required.

Microdiagnostic

Run routine A8, test 1.
1. Enter A8,10,01,00,00.

Test runs error free — Yes → A → ACC 601

No

MICRO 10

Microdiagnostic

Loop routine A8, test 1.
1. Enter A8,10,01,00,01,00.

Scope

Sweep	0.2 ms/div
Trigger	Slope (–) CH1 Only

CH1 A1P2U06 (N2U06) (–Seek Start) 1

Check

Verify the following:
1. +Diff. Ctr. Zero 2 is a (–) MST level with sync.
2. –DC7 Diff. Ctr Odd 3 is a (–) MST level (Diff. Cntr. set for a 1-track Seek).
3. –Even Track 4 toggles from a (–) to a (+) MST level with sync.
4. +Forward 5 is a (+) MST level with sync.
5. +On Track 6 switches to a (–) MST level with sync.
6. –Access Complete 7 switches to a (+) MST level with sync.
7. +Access Start 8 is a (+) MST pulse the width of –Seek Start.
8. +Reset Track Following Timer 9 is a (+) MST pulse the width of –Seek Start.
9. +Track Following Timer A becomes a (–) MST level with synchronization.
10. +Linear Mode B becomes a (–) MST level before the end of –Seek Start.
11. +Access Mode C becomes a (+) MST level before the end of –Seek Start.
12. +Allow Diff Ctr. D a (+) MST level before the end of –Seek Start.
13. –Run Access Timer E becomes a (–) MST level before the end of –Seek Start.
14. Trace logic to source of problem.

Repair or replace as required.

Trouble corrected — Yes → B → ACC 800

No → A → ACC 910

A1P2 (A1N2)
KHxxx (KJxxx)

–SERVO LATCH — KH020AE6
+INHIBIT SEQUENCER — KH050AM6
+LINEAR MODE LATCH — KH020AF2
+CONTROL LATCH — KH020AD2
+AUTO/MANUAL REZERO LATCH — KH040BH2
+DM REZERO A — KF040AF2
+GO HOME OPERATION — KH010AB2
+HAR 0A — KB050AA6
–SERVO LATCH — KH020AE6
+SELECTED A — KK040AK2
+REZERO START
+DIAG SERVO RESET
+WAIT LATCH
+ACCESS CHECK — KH060BQ6
+REZERO PATTERN A — KB130GJ2
–SEEK START — KA080AC3
+DIFF CTR A ZERO — KB010AS2
–CONTROL LATCH — KH020AD6
–SERVO LATCH — KH020AE6
–LINEAR MODE LATCH — KH020AF6
+SEEK START SELECTED — KH040AK2
+ACCESS CHECK — KH060BQ6
–DC7A DIFF CTR ODD — KB030AV6
–SEEK START INHIBITED — KH020AS6
+WAIT LATCH — KH020AB6

A +Track Following Timer

Servo Logic
A1R4 (A1Q4)
Ref. ACC 460

D10 — +ALLOW DIFF CTR A — KB060
RUN ACCESS TIMER A — +RUN ACCESS TIMER A — LA410
B04 — +ACCESS MODE A — KH020 LA310 LA400
FORWARD A — +FORWARD A — LA400 LA410
G11 — +ACCESS START A — LA400
J04 — +RESET TRACK FOLLOWING TIMER A — LA400
D04
G03 A

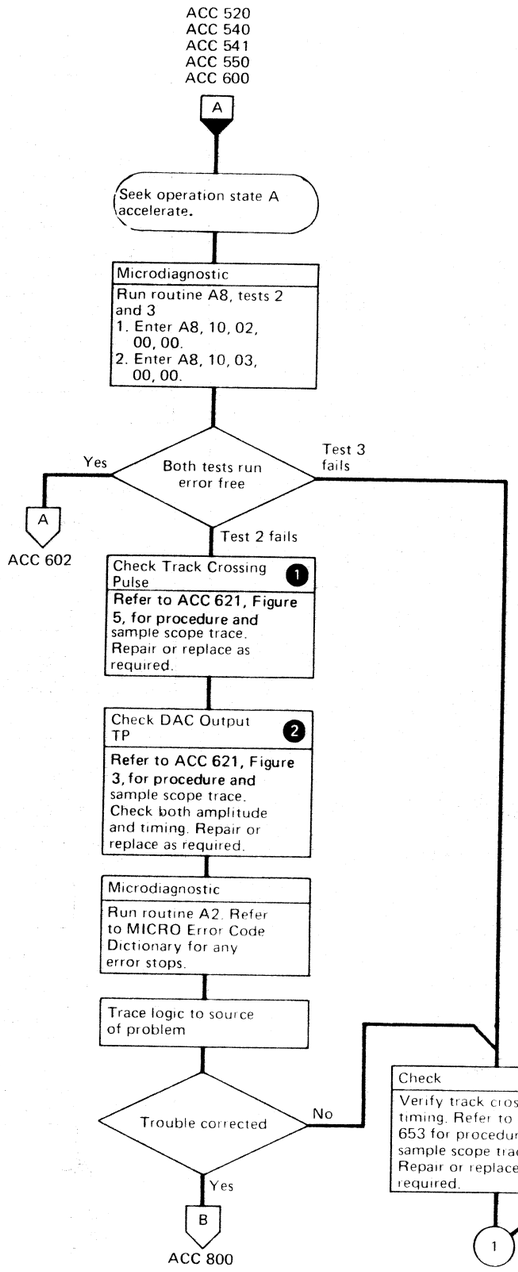
ACCESS START A
ON TRACK A
ACCESS COMPLETE A — –ACCESS COMPLETE A — KH060 KF160
EVEN TRACK A — –EVEN TRACK A — KH020 LA210
INHIBIT SEQUENCER — +INHIBIT SEQUENCER
SEEK START SELECTED — +SEEK START SELECTED / –SEEK START SELECTED
SEEK START INHIBITED — –SEEK START INHIBITED

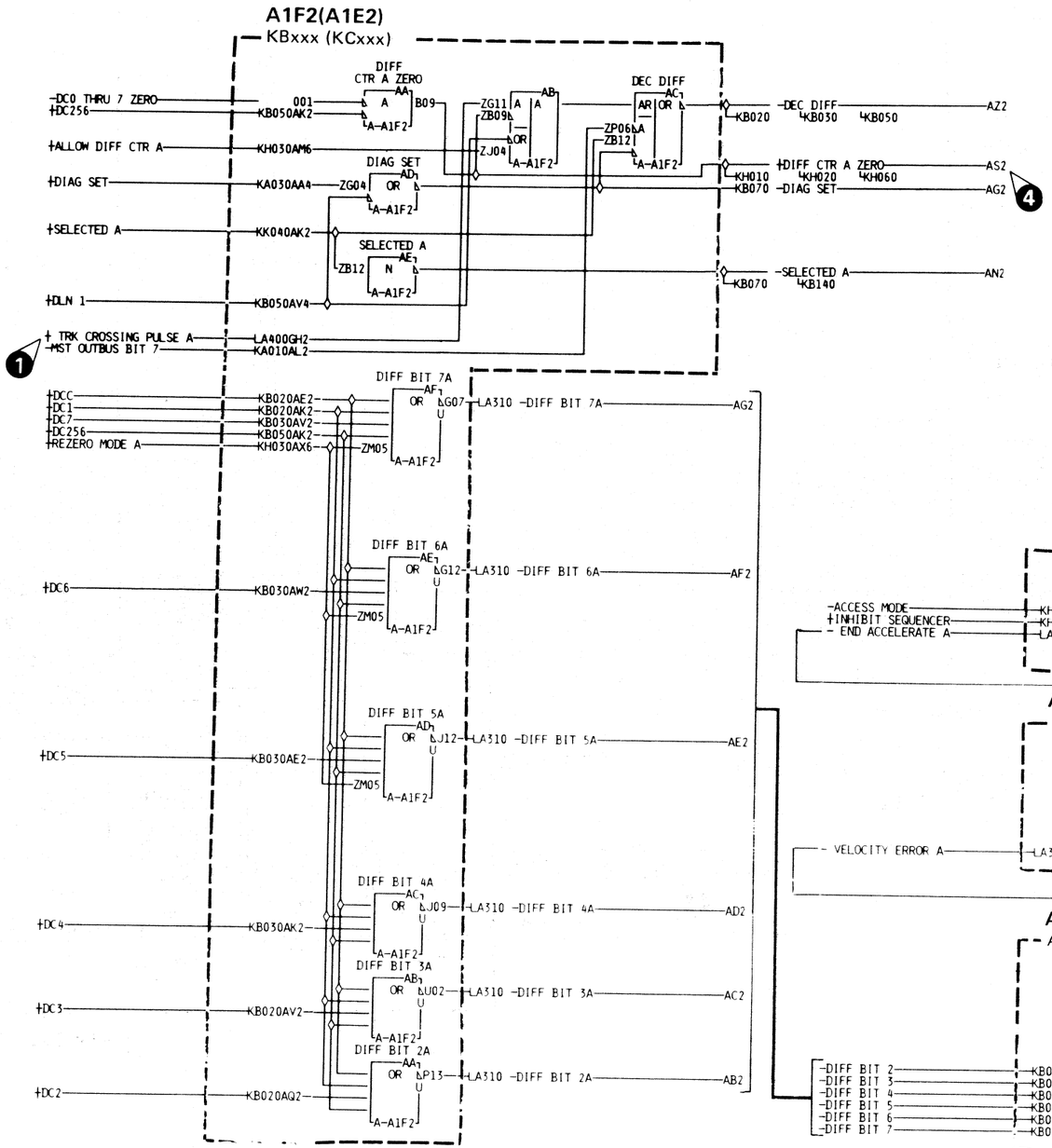
A — Reset Linear Mode Latch — M02 +Linear Mode B

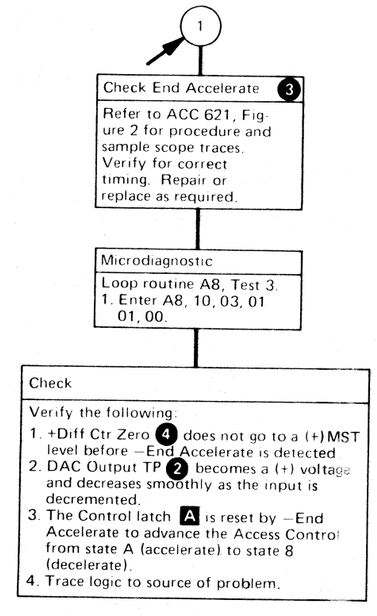
3340	DF0600 Seq. 2 of 2	2747197 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440209 25 Mar 74	440214 17 Jun 74	440223 14 Mar 75

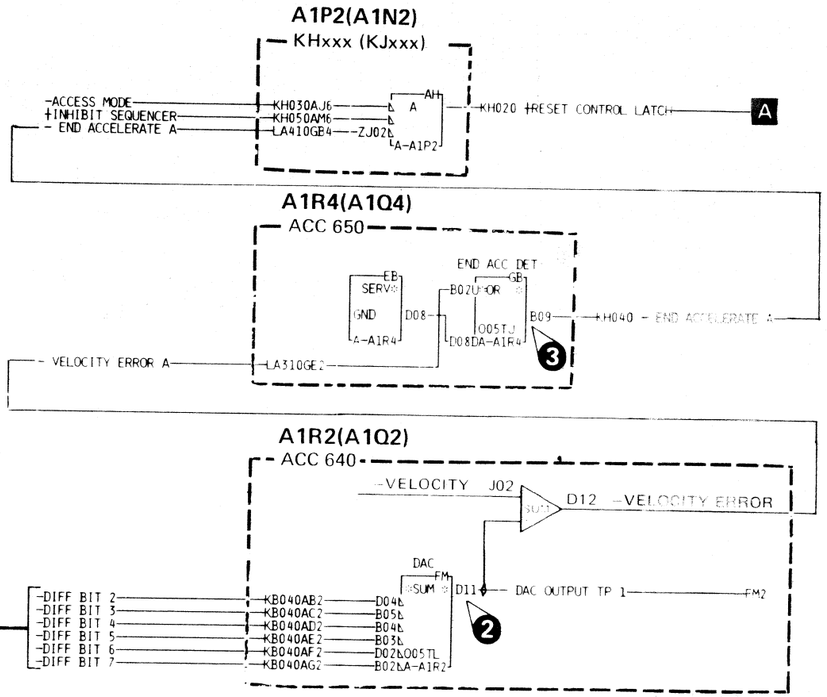
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SEEK OPERATION DIAGRAM









DF0602 Seq. 1 of 2	2747198 Part No. ( )

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SEEK OPERATION DIAGRAM

ACC 560
ACC 561
ACC 601

A

Seek Operation State 8 (Decelerate).

Microdiagnostic

Run routine A8, test 4.
1. Enter A8, 10, 04, 00, 00.

Error stop A843, Message Byte 2 = 'X8'

No → A → ACC 603

Yes

Microdiagnostic

Loop routine A8, test 4.
1. Enter A8, 10, 04, 00, 01, 00.

Scope

Sweep 2ms/div.
Trigger Slope (+)
CH1 only
CH1 A1P2J09 (N2J09)
+Access Mode

Check

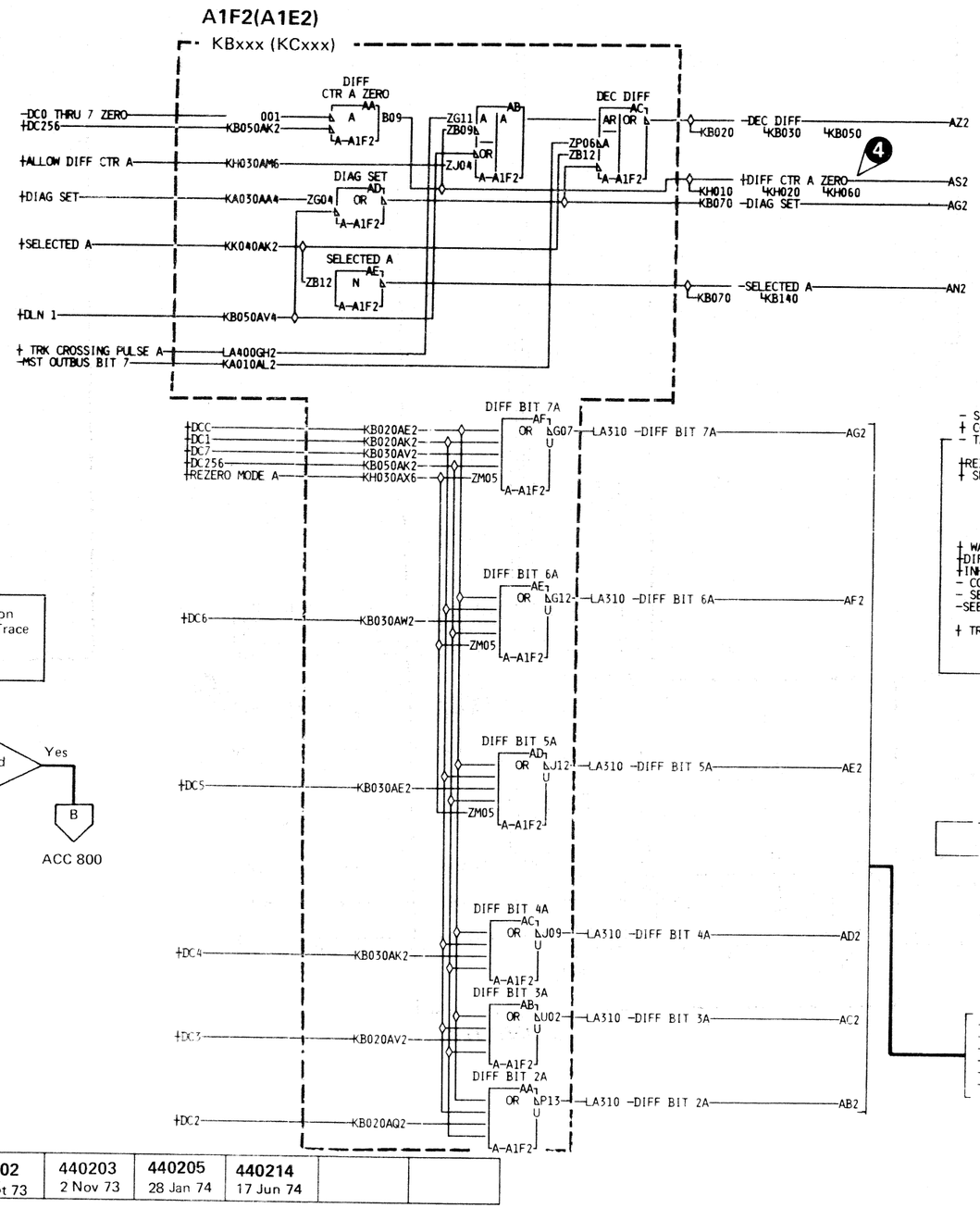
Verify the following:
1. +Linear Mode ❶ becomes a (+) MST level with the detection of −Target Velocity ❷ .
2. Refer to ACC 621, Fig 1D, for sample timing.
3. −Target Velocity ❷ becomes a (−) MST level when −Velocity ❸ is less than 0.15V
4. Refer to ACC 621, Fig 3D, for sample timing.
5. −Diff. Ctr Zero ❹ becomes a (−) MST level at about the same time as target velocity.

Verify Seek Operation timing (ACC 621). Trace any fault to the referenced diagram.

Trouble Corrected

Yes → B → ACC 800

No → A → ACC 910



DF0602	2747198
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SEEK OPERATION DIAGRAM

ACC 580
ACC 590
ACC 602

A

Seek Operation State C (Linear Mode)

Microdiagnostic
Run routine A8, Test 04.
1. Enter A8,10,04,00,00.

Test runs error free — Yes

No

Microdiagnostic
Loop routine A8, Test 04.
1. Enter A8,10,04,00,01,00.

Scope

Sweep	0.5 ms/div
Trigger	Slope (+) CH1 Only

CH1 A-A1P2M02 (N2M02) (+Linear Mode). ❶

Check
Verify the following:
1. +On Track ❷ becomes a (+) MST level with −Access Complete.
2. +Track Following Timer ❸ becomes a (+) MST level before −Access Complete.

Repair or replace as required.

Check
Verify Track Following Servo operation (ACC 701). Return to this point if problem is not found.
Repair or replace as required.

A → ACC 701

A

Check
Verify Seek operation timing (ACC 621). Look for any discrepancy that may cause failure and trace to referenced diagram.

Trouble corrected — Yes → B → ACC 800

No → A → ACC 910

A

Servo Input B04

D04 **Servo Amplifier** A1T2 (A1S2) Ref. ACC 630

D10 +Position
D09 −Position
+Linear Mode D04

A1R4 (A1Q4) ACC 650

G13 → **On Track** → J03 −On Track → **Track Following Timer** → G03 +Track Following Timer → A ❸

J13 +Reset Track Following Timer
J04

Compensator
B03 +Linear Mode D04

D02 Position Error → **Analog Switch** → D13 +Pwr Amp Drive 12 → **Power Amp.** P410 (P411) Ref. ACC 660

1-2 → VCM B A
3-4
15 → Current Sense

A1P2 (A1N2)
KHxxx (KJxxx)

−LINEAR MODE LATCH — KH020AF6 — AS A A-A1P2 M02 ❶ — KH020 +LINEAR MODE A LA400 LA410
+INHIBIT SEQUENCER — KH050AM6
+REZERO PATTERN A — KB130GJ2
+SEEK START INHIBITED — KH020AS2
AP OR A-A1P2 ZG05 J06 — LA400 +RESET TRACK FOLLOWING TIMER A

A

−LINEAR MODE LATCH — 001
+ TRK FOLLOWING TIMER A — LA400EM2 — ZG03
−REZERO PATTERN A — KB130FJ4 — ZG13
−REZERO OPERATION — 002
− TARGET VELOCITY A — LA410GD4 — ZD11
AC OR A-A1P2

+RESET CONTROL LATCH — KH040AH2
+INHIBIT SEQUENCER — KH050AM6
+WAIT LATCH — 003

CONTROL LATCH AB FL A S S OR R A-A1P2

−CONTROL LATCH — KH020AD6
−SERVO LATCH — KH020AE6
−LINEAR MODE LATCH — KH020AF6
+SEEK START SELECTED — KH040AK2
ON TRACK A AA A A-A1P2 U05 ❷

+ACCESS CHECK — KH060BQ6
ACCESS COMPLETE A AB OR A-A1P2 ZU05 U07 — KF160 −ACCESS COMPLETE A KH060
KH060 +ON TRACK A

+SECTOR NONCOMPARE A — KD180AC2
+DM SEQ ERROR A — KF040AG2
+TIMEOUT CHECK — KH020AG2
+SERVO OFF TRK — KH020AY2
+OVERSHOOT CHECK — 001
DRIVE CHECK AD OR A-A1P2 ZP06 ZS08

+ TRK FOLLOWING TIMER A — LA400EM2
RD&WR CAPABLE A AC A A-A1P2 ZS13 ZG03 G02 — KL050 +RD&WR CAPABLE A KP010 — AY2
TRACK F OLLOWING TIMER AA N A-A1P2 ZG03
−DRIVE CHECK KH070 — KH050 — AZ2
−TRACK FOLLOWING TIMER KH070 — KH020 — AJ2

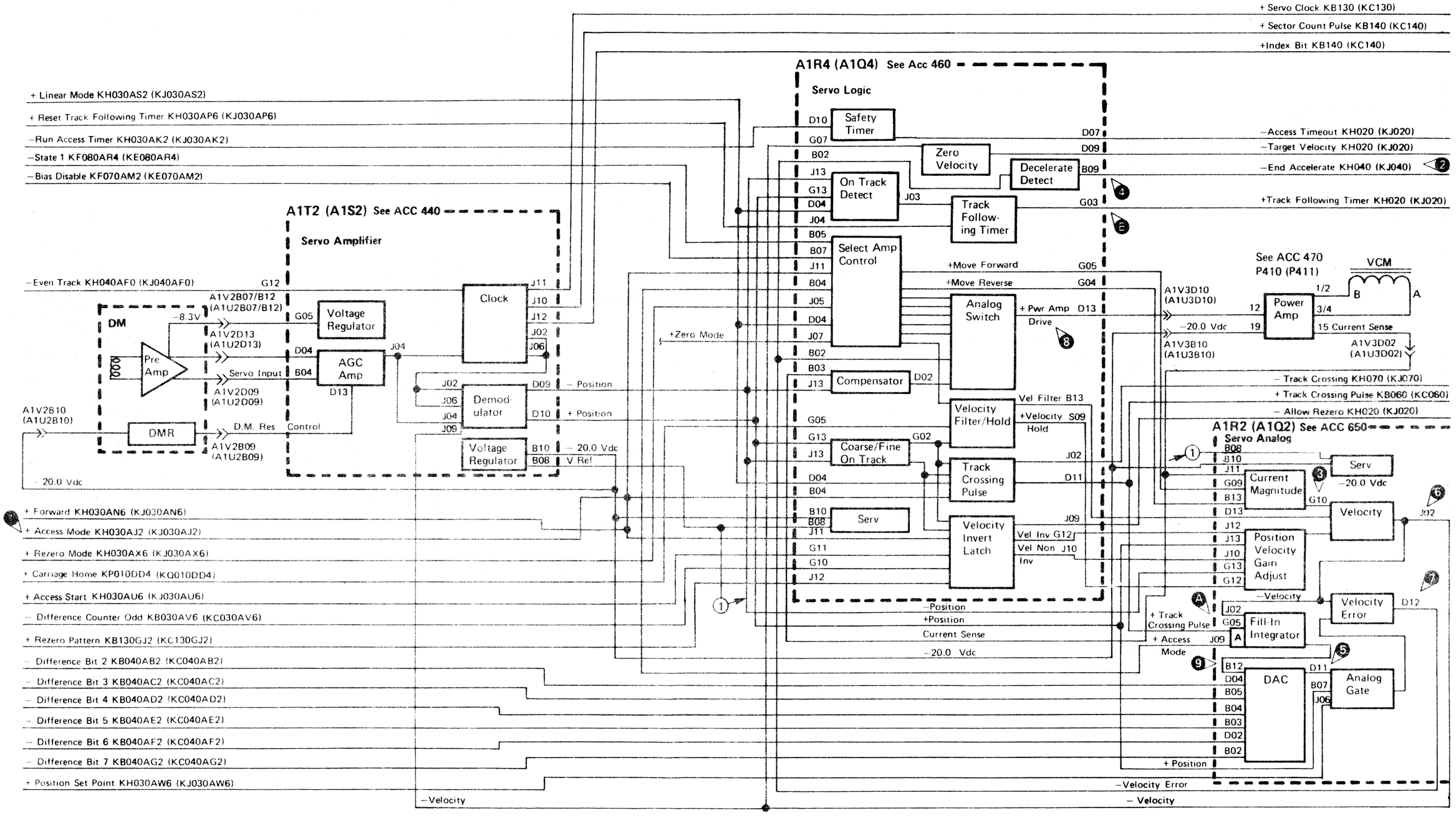
+STATE 6 A — KF020AF2
ACCESS CHECK A AE OR A-A1P2 DD03 — KH020 −ACCESS CHECK A — BQ2

DF0620 Seq. 1 of 2	2747199 Part No. ( )

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SERVO BLOCK DIAGRAM



3340

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SEEK TIMING

See ACC 620 for test points

1 Ch 1 A1R4B04(Q4B04)
+ Access Mode
volts/div 0.1
probe X10

2 Ch 2 A1R4D09(Q4D09)
– Target Velocity
volts/div 0.1
probe X10

3 Ch 1 A1R2G10(Q2G10)
Current Magnitude
volts/div 0.1
probe X10

4 Ch 2 A1R4B09(Q4B09)
– End Accelerate
volts/div 0.1
probe X10

5 Ch 1 A1R2D11(Q2D11)
DAC Output TP 1
volts/div (as shown)
probe X10

6 Ch 2 A1R2J02(Q2J02)
– Velocity
volts/div (as shown)
probe X10

7 Ch 1 A1R2D12(Q2D12)
– Velocity Error
volts/div (as shown)
probe X10

8 Ch 2 A1R4D13(Q4D13)
+ Power Amp Drive
volts/div 0.5
probe X10

9 Ch 1 A1R2B12(Q2B12)
+ Fill-In Integrator
volts/div 0.5
probe X10

A Ch 2 A1R4D11(Q4D11)
+ Track Crossing Pulse
volts/div 0.1
probe X10

Setup A – 1 Track Seek
Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,07,01,00
Scope Setup:
Sweep: 0.2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2J09(N2J09) + Access Mode

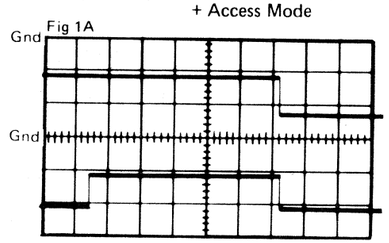
Fig 1A


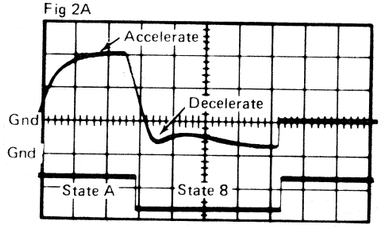
Fig 2A


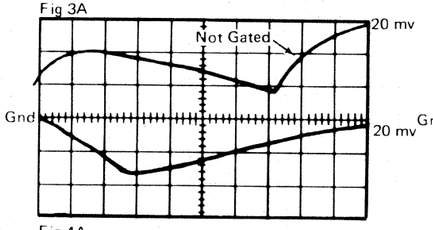
Fig 3A


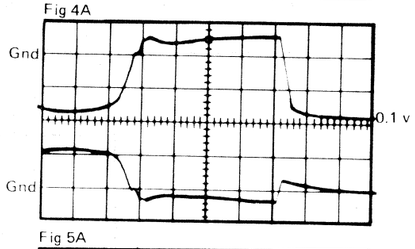
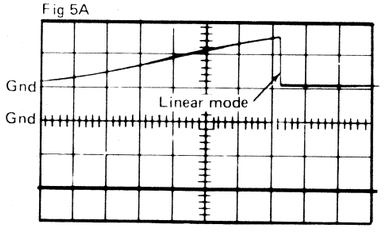
Fig 4A


Fig 5A


Setup B – 2 Track Seek
Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,06,01,00
Scope Setup:
Sweep: 0.5 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2J09(N2J09) + Access Mode

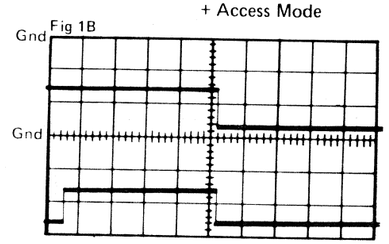
Fig 1B


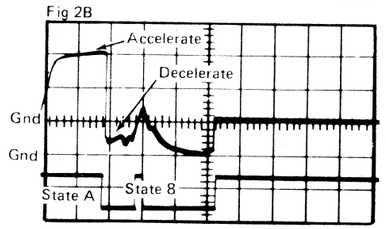
Fig 2B


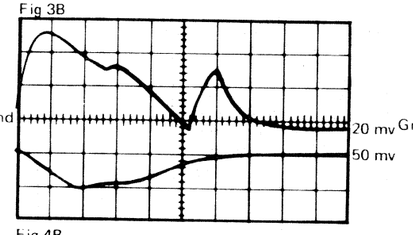
Fig 3B


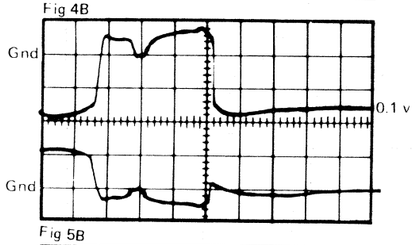
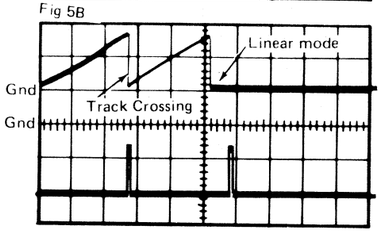
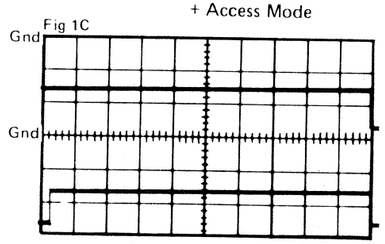
Fig 4B


Fig 5B


Setup C – 32 Track Seek
Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,02,01,00
Scope Setup:
Sweep: 1 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2J09(N2J09) + Access Mode

Fig 1C


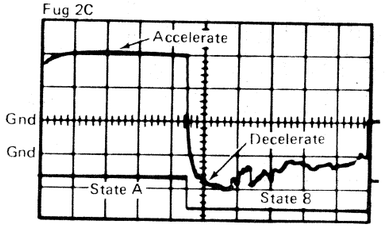
Fug 2C


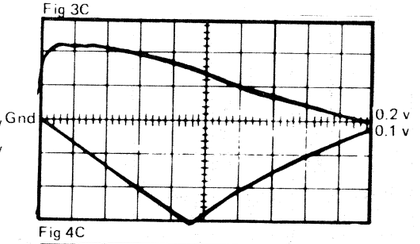
Fig 3C


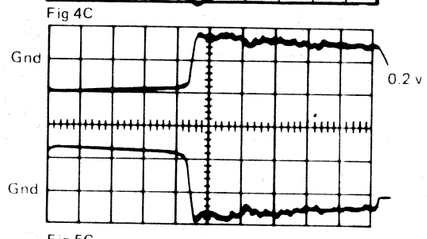
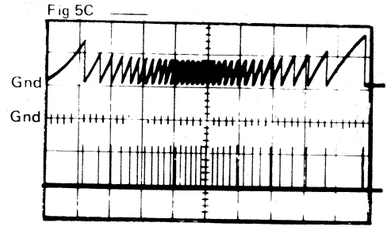
Fig 4C


Fig 5C


Setup D – 128 Track Seek
Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,01,01,00
Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1P2J09(N2J09) + Access Mode

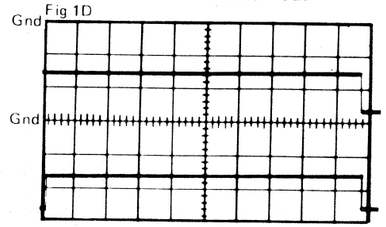
Fig 1D


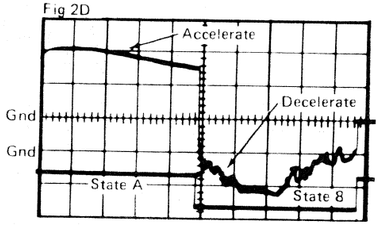
Fig 2D


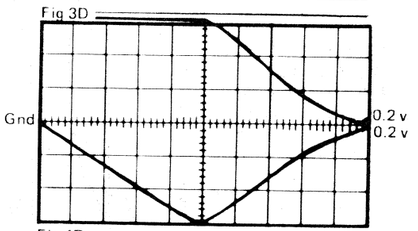
Fig 3D


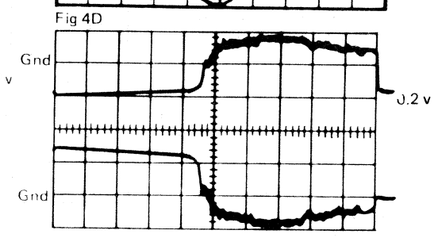
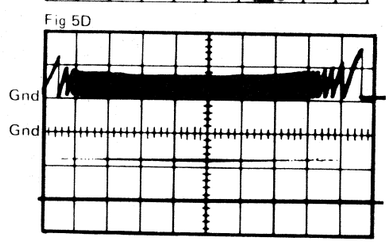
Fig 4D


Fig 5D


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440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440205 28 Jan 74	440223 14 Mar 75	

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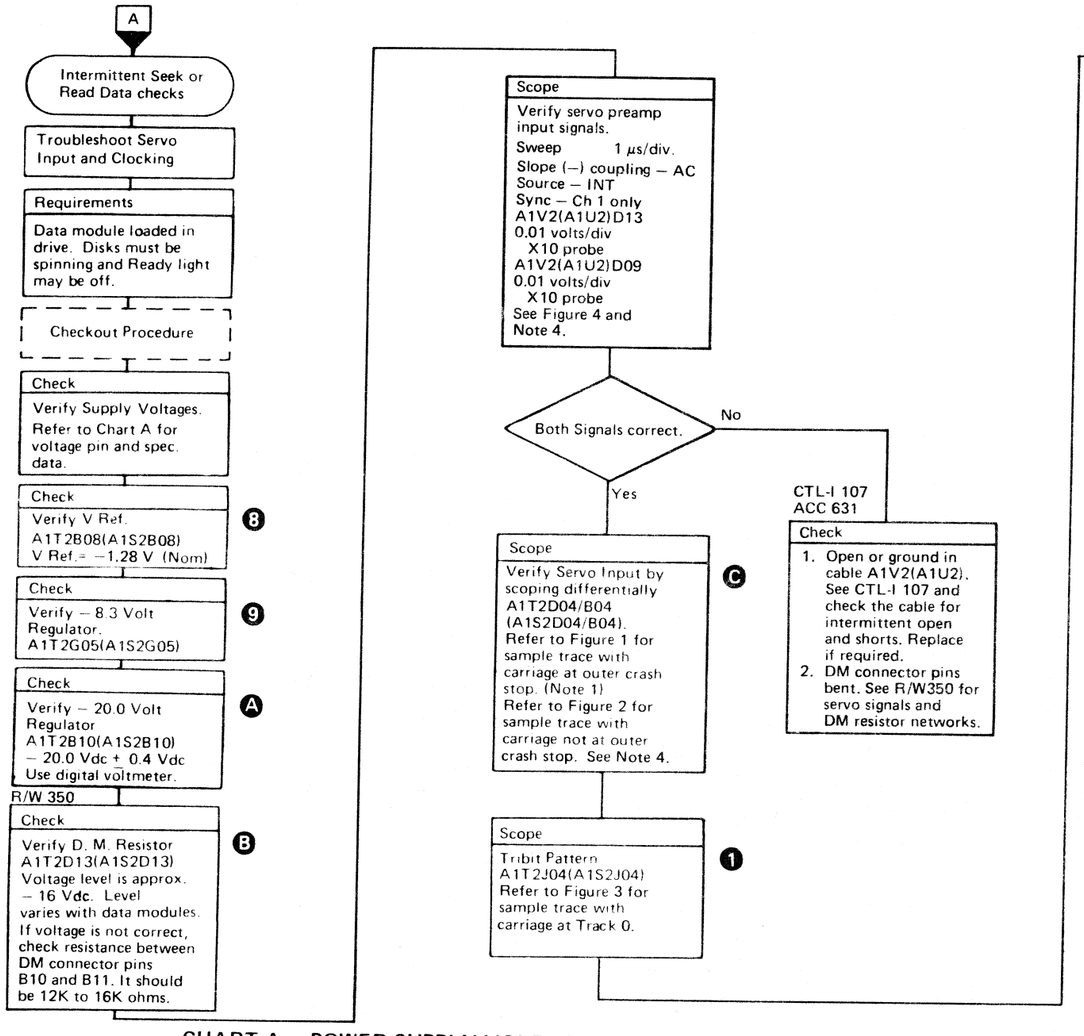


CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1T2D03 (S2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1T2D05 (S2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1T2D06 (S2D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1T2B06 (S2B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1T2G11 (S2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A

Note 1: Insert Bobbin Push Rod (P/N 2304727) to move the carriage to the outer crash stop.

Note 2: Jumper A1T2G12 (S2G12) to Gnd (D08) to force to (+) MST Level.

Note 3: Use Bobbin Push Rod to manually move carriage. Ready lamp must be off.

Note 4: If the servo is not track following, it may be necessary to position the carriage over the servo track until the correct pattern is obtained. Tape the tach rod in position if necessary.

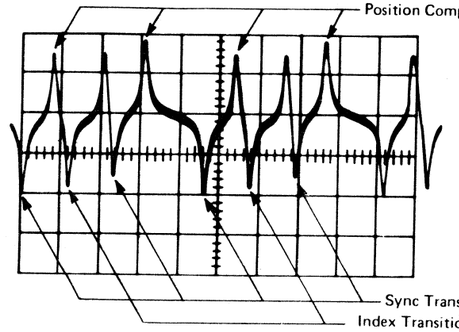


Figure 1 - Servo Input
(Carriage at Outer Stop)
Sweep 1 µs/div.
Trigger/Mode Norm/Add
Slope (−)
Ch 1 A1T2B04 (S2B04)
0.05 volts/div, X1 probe
Ch 2 A1T2D04 (S2D04)
0.05 volts/div, X1 probe
Invert

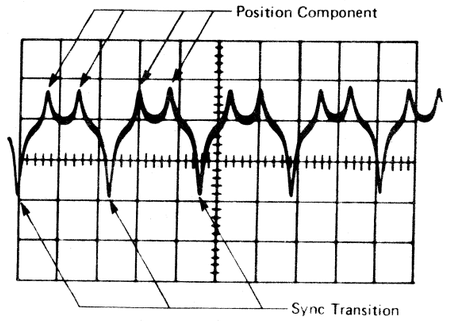


Figure 2 - Servo Input
(Carriage at Track 0)
Scope setup same as for Figure 1.
Sweep 1 µs/div
Trigger/Mode Norm/Add
Slope (−)
Ch 2 A1T2D04(S2D04) - Servo Preamp 1
0.05 volts/div, X1 probe
Ch 1 A1T2B04(S2B04) - Servo Preamp 2
0.05 volts/div, X1 probe
Invert

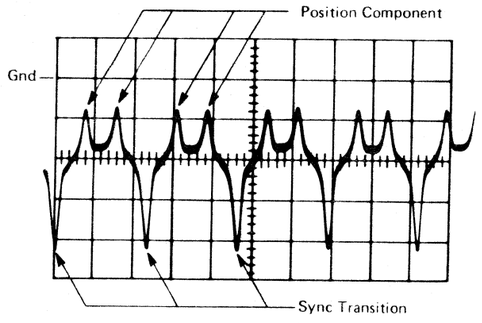


Figure 3 - Tribit Pattern
(Carriage at Track 0)
Sweep 1 µs/div.
Trigger
Slope (−)
Ch 1 Only
Ch 1 A1T2J04(S2J04)
0.2 volts/div, X10 probe

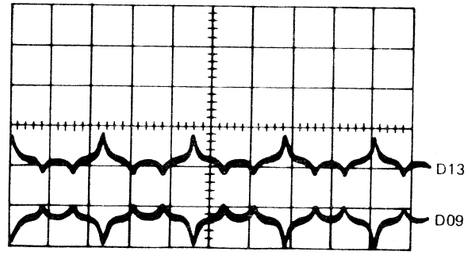
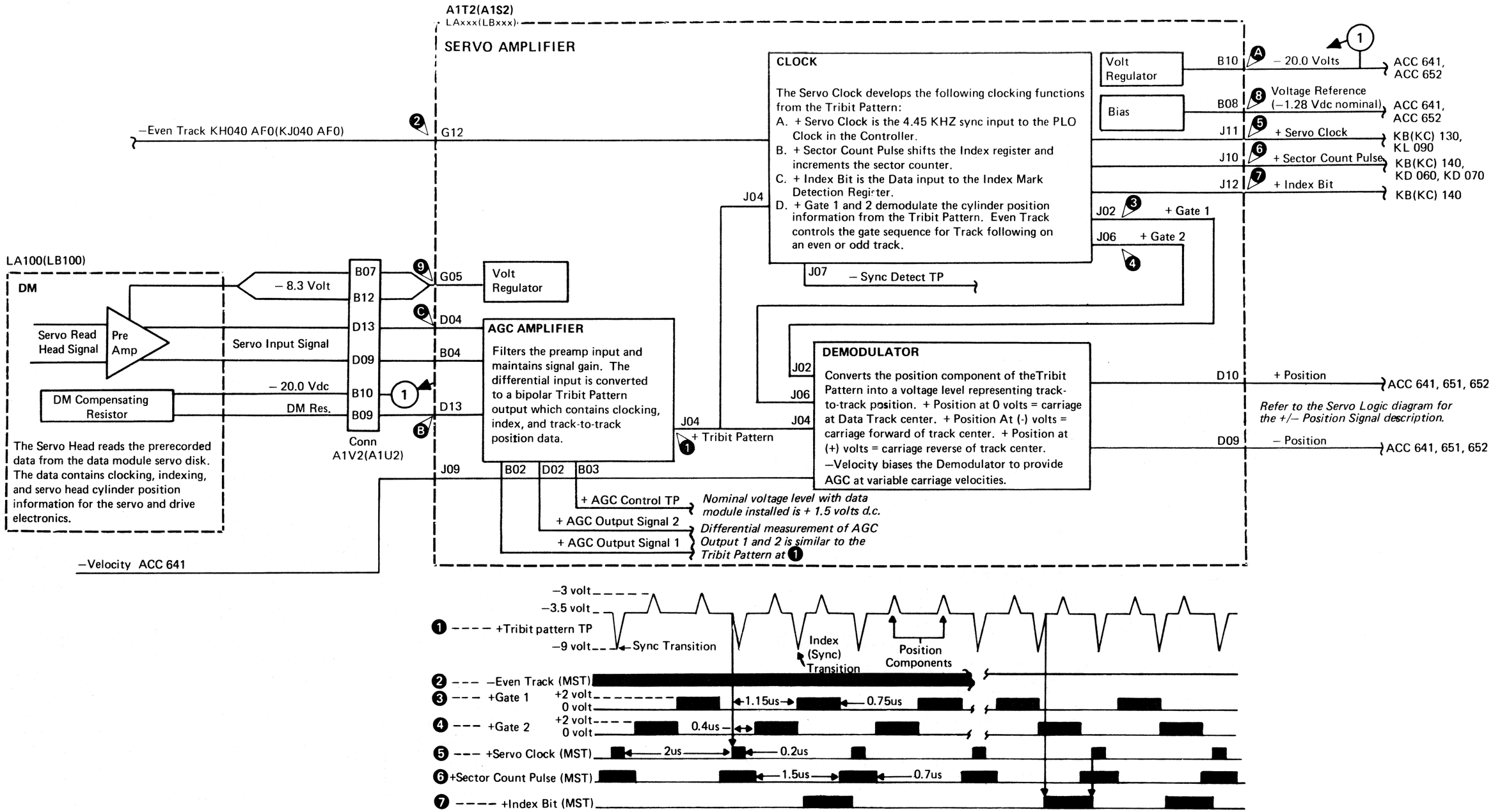
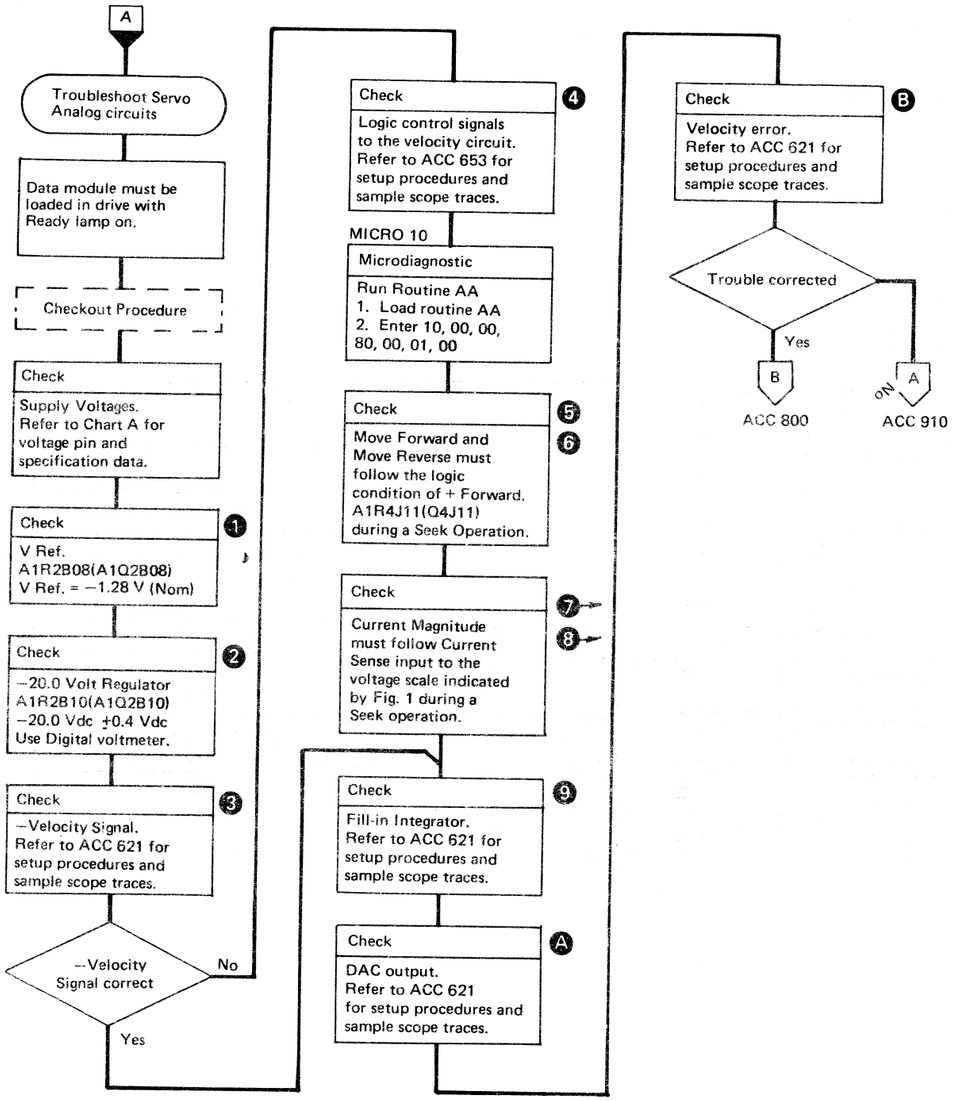


Figure 4 - Servo Preamp Input
Sweep 1 µs/div.
Slope (−)
Sync Int AC Ch1 only
Servo Preamp 1
A1V2(A1U2)D13
Servo Preamp 2
A1V2(A1U2)D09
0.01 volts/div, X10 probe

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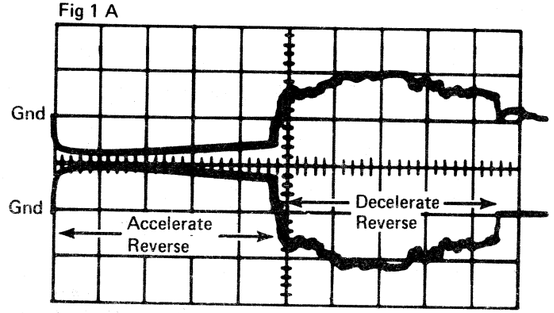
DF0640 Seq. 2 of 2	2747201 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74	440223 14 Mar 75		

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FIGURE 1 – CURRENT SENSE/CURRENT MAGNITUDE

Microdiagnostic routine AA
1. Load routine AA – 128 track seek forward/reverse
2. Enter 10,00,00,80,00,01,00

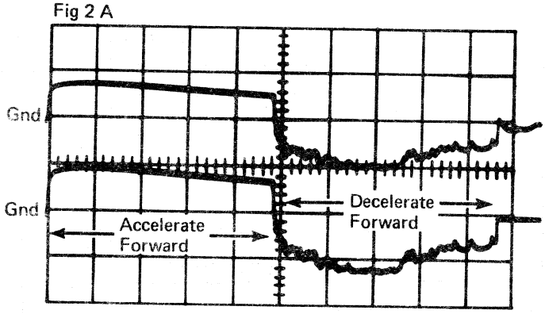
Fig 1 A



See ACC 461 for test points.

Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync:1 A1R4G04(Q4G04) + Move Reverse
Ch 1 A1R2J11(Q2J11)
8 Current Sense volts/div 1.0 probe X10
Ch 2 A1R2G10(Q2G10)
7 Current Magnitude volts/div 0.2 probe X10

Fig 2 A

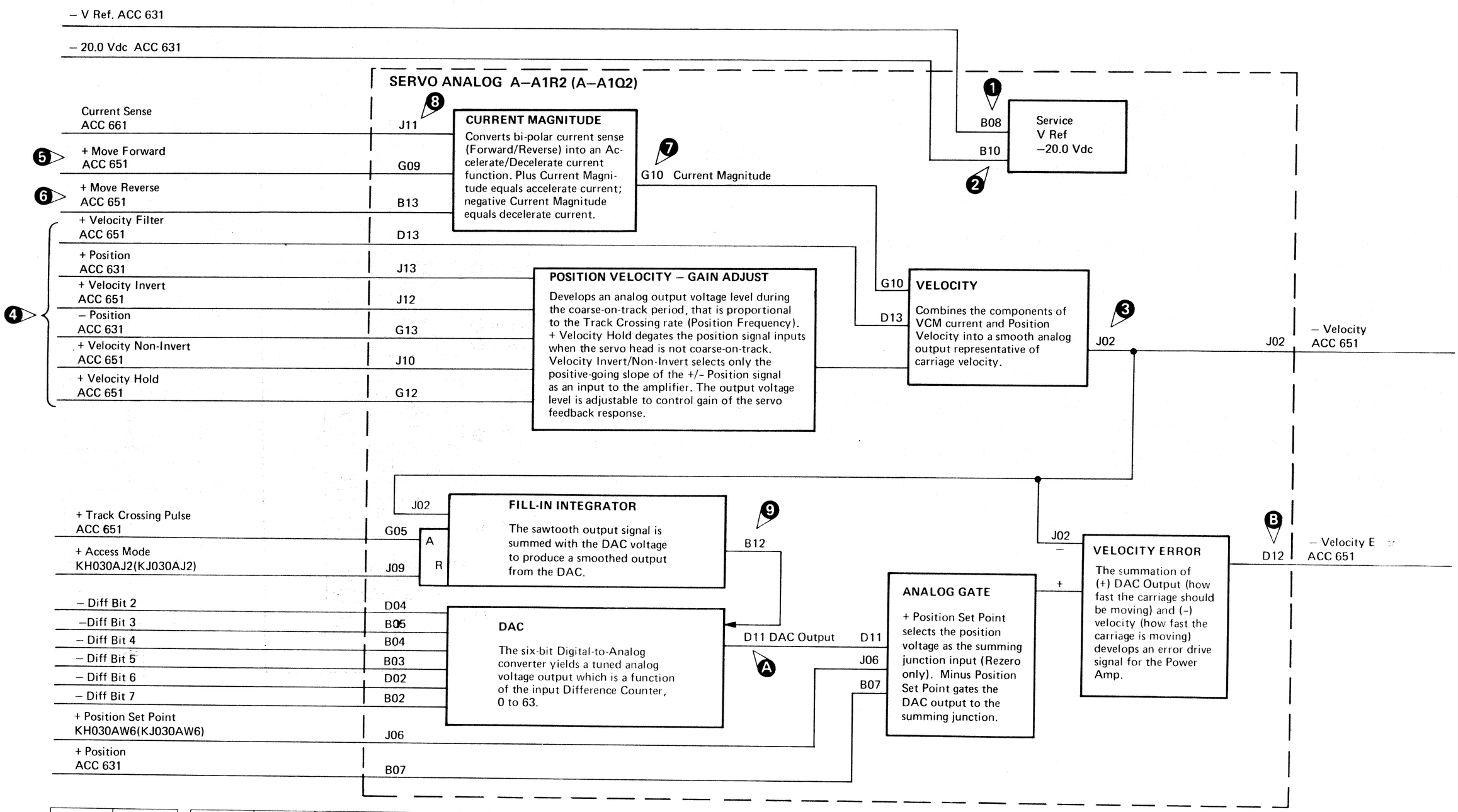


Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4G05(Q4G05) + Move Forward
Ch 1 A1R2J11(Q2J11)
8 Current Sense volts/div 1.0 probe X10
Ch 2 A1R2G10(Q2G10)
7 Current Magnitude volts/div 0.2 probe X10

CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit: Control Module	Map Exit: Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R2D06 (Q2D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R2B06 (Q2B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A

SERVO ANALOG DIAGRAM



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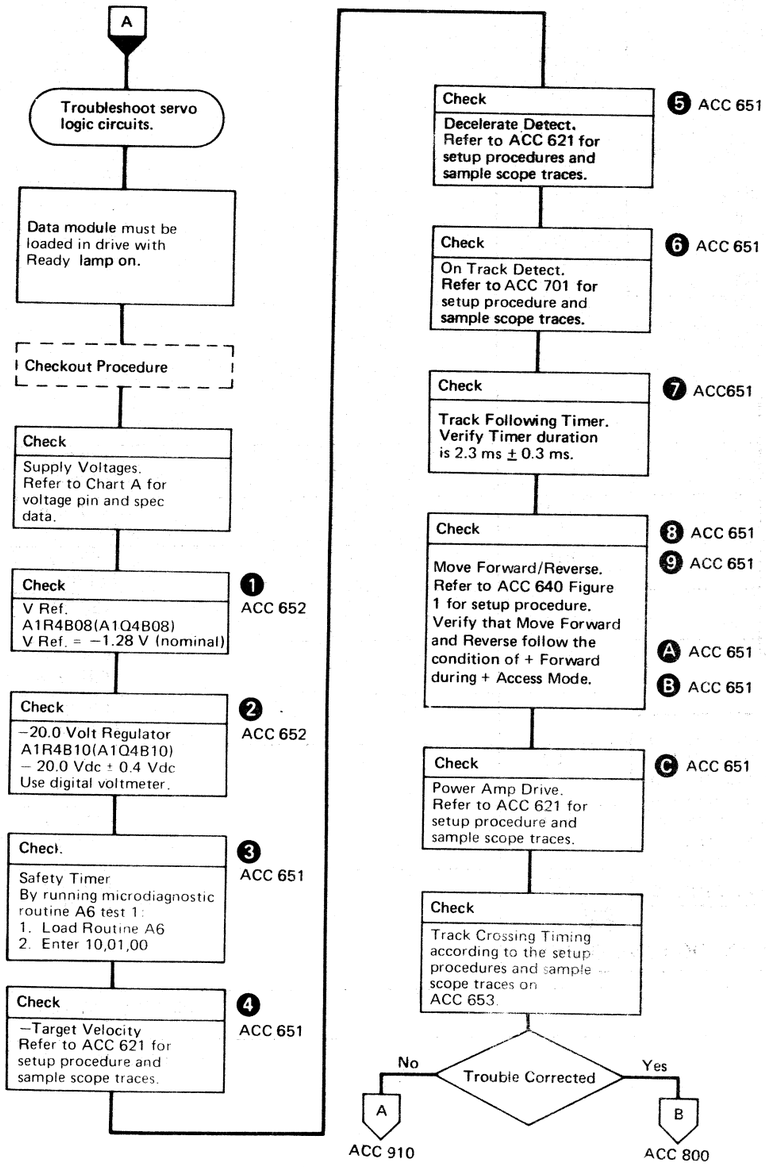


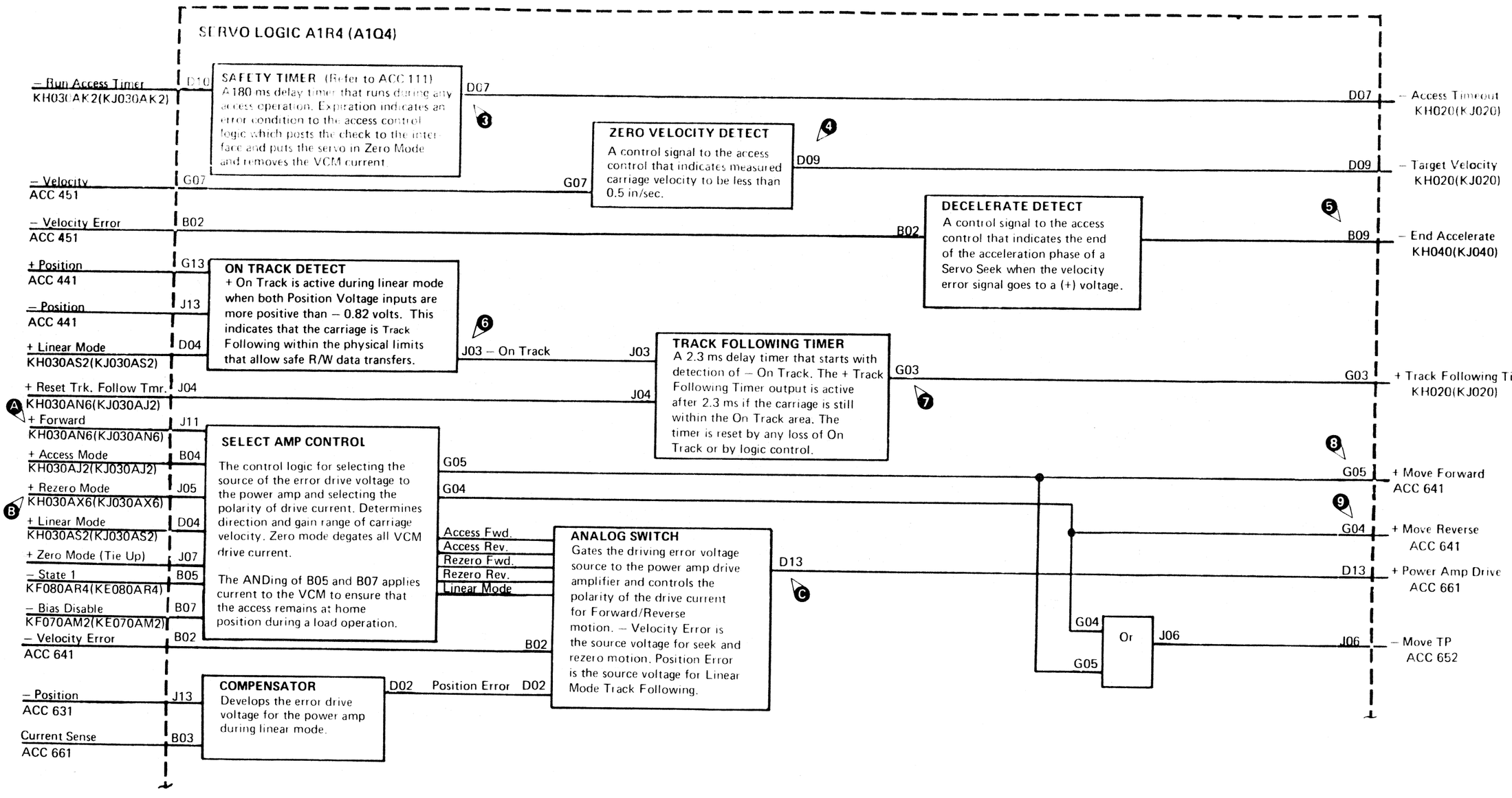
CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
A1R4D05 (A1Q4D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R4D06 (A1Q4D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R4B06 (A1Q4B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1R4B11 (A1Q4B11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A

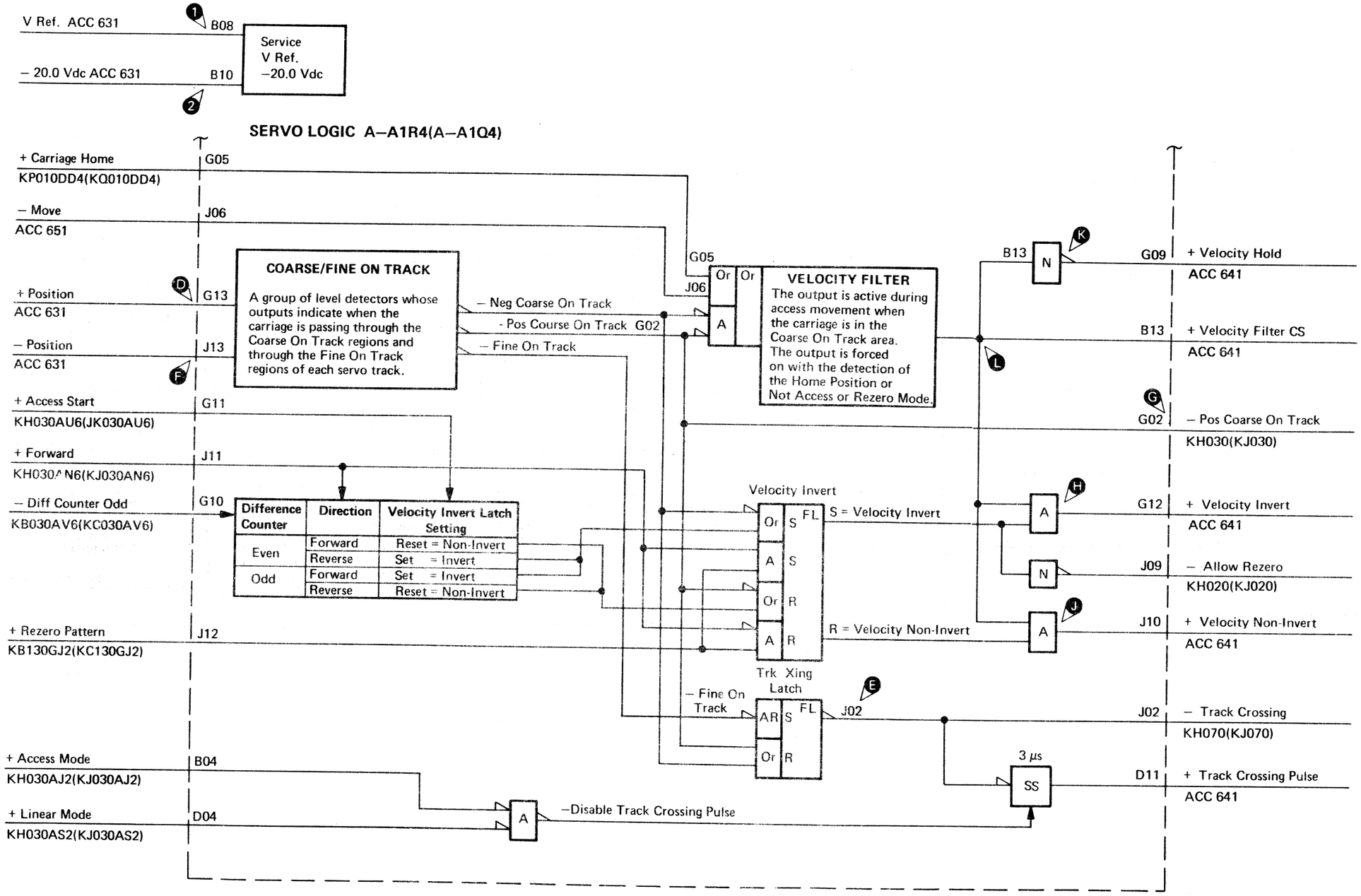
DF0641 Seq. 2 of 2	2747202 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440205 26 Jan 74	

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3340	DF0651 Seq. 2 of 2	2747203 Part No. ( )	440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440212 29 Apr 74	440223 14 Mar 75	

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TRACK CROSSING TIMING–SEEK

Note 1: –Velocity is a function of both current magnitude and position.

Note 2: –Velocity is a function of current magnitude only

See ACC 652 for test points.

D Ch 1 A1R4G13(Q4G13)
+ Position
volt/div 0.5
probe X10

E Ch 2 A1R4J02(Q4J02)
– Track Crossing
volt/div 0.1
probe X10

F Ch 1 A1R4J13(Q4J13)
–Position
volt/div 0.5
probe X10

G Ch 2 A1R4G02(Q4G02)
– Pos Coarse On Track
volt/div 0.1
probe X10

H Ch1 A1R4G12(Q4G12)
+ Velocity Invert
volt/div 0.1
probe X10

J Ch 2 A1R4J10(Q4J10)
+ Velocity Non-Invert
volt/div 0.1
probe X10

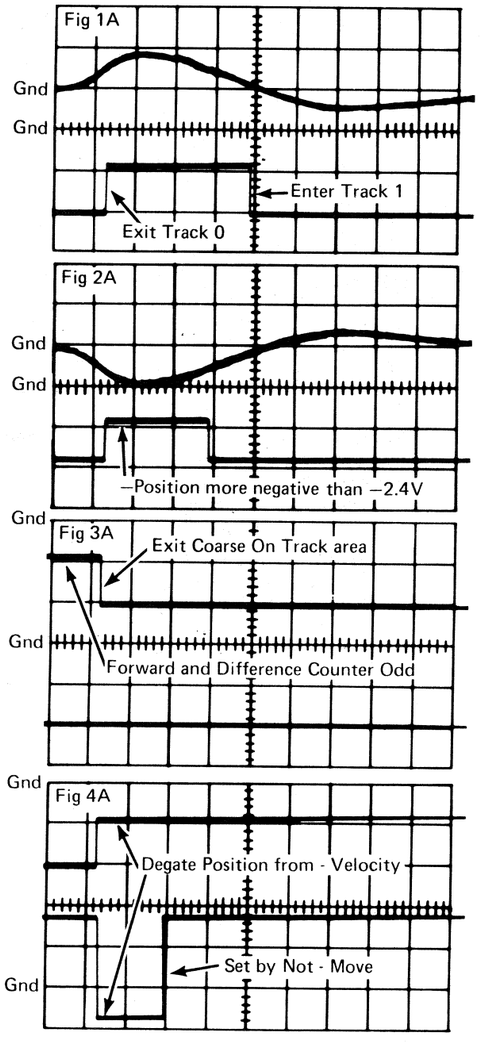
K Ch 1 A1R4G09(Q4G09)
+ Velocity Hold
volt/div 0.1
probe X10

L Ch 2 A1R4B13(Q4B13)
+ Velocity Filter CS
volt/div 0.1
probe X10

Setup A – 1 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,07,01,00

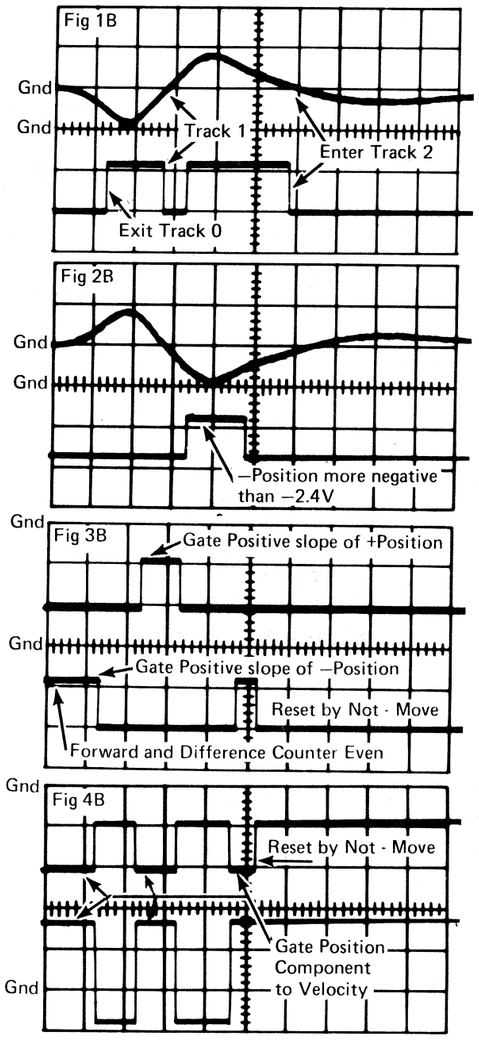
Scope Setup:
Sweep: 0.5 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode



Setup B – 2 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,06,01,00

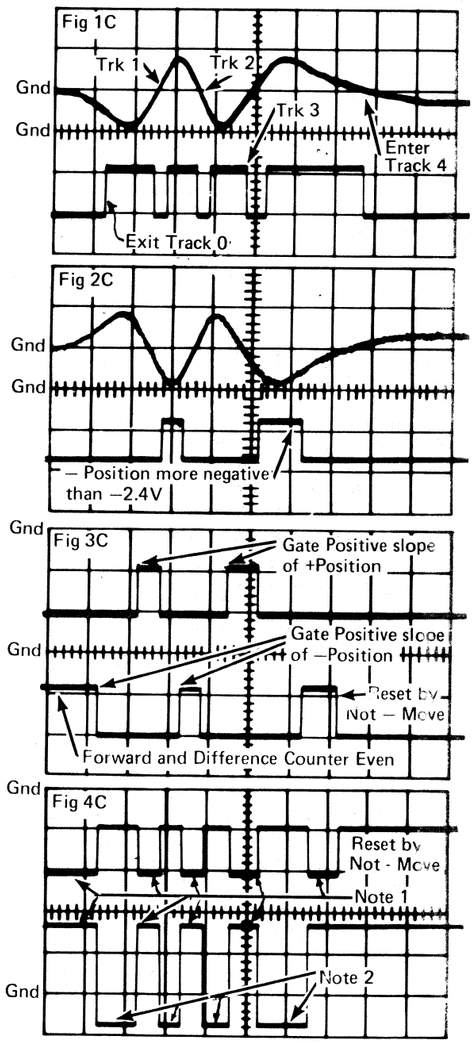
Scope Setup:
Sweep: 0.5 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode



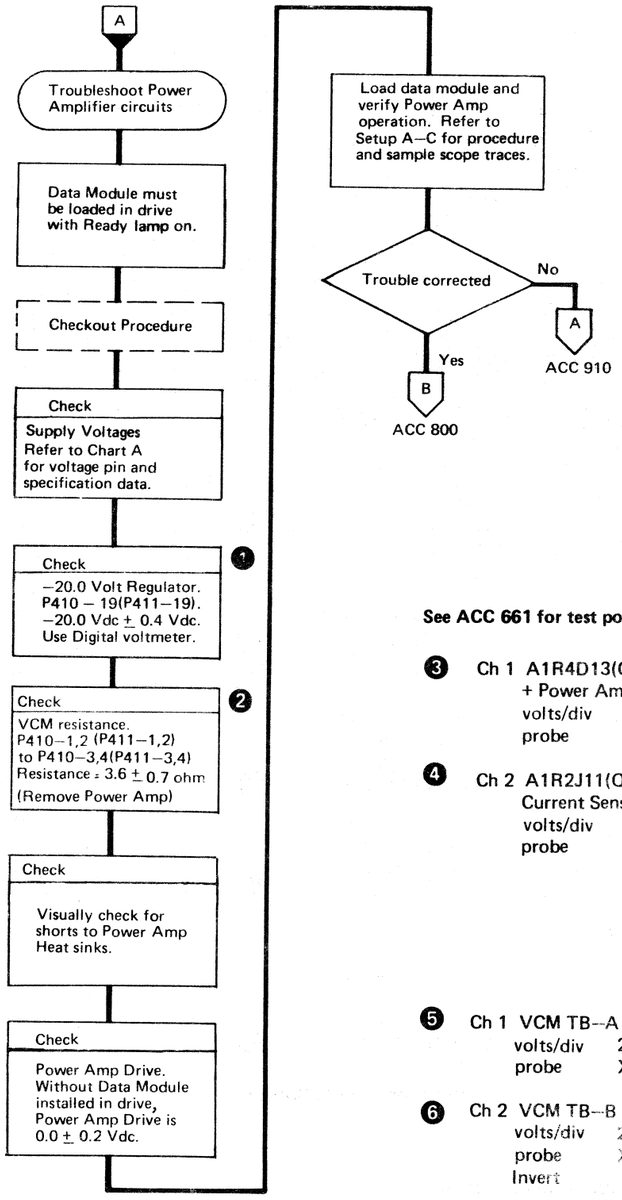
Setup C – 4 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,05,01,00

Scope Setup:
Sweep: 0.5 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode



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See ACC 661 for test points.

❸ Ch 1 A1R4D13(Q4D13)
+ Power Amp Drive
volts/div 0.5
probe X10

❹ Ch 2 A1R2J11(Q2J11)
Current Sense
volts/div 0.5
probe X10

❺ Ch 1 VCM TB−A
volts/div 2.0
probe X10

❻ Ch 2 VCM TB−B
volts/div 2.0
probe X10
Invert

Mode: Added

CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit	
		Control Module	Satellite Module
P410–7,8 (P411–7,8)	−36.0 to −43.2 Vdc	PWR 80-A	PWR 280-A
P410–14 (P411–14)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
P410–16 (P411–16)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A

Setup A - 2 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,06,01,00

Scope Setup:
Sweep: 0.5 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode

Fig 1A

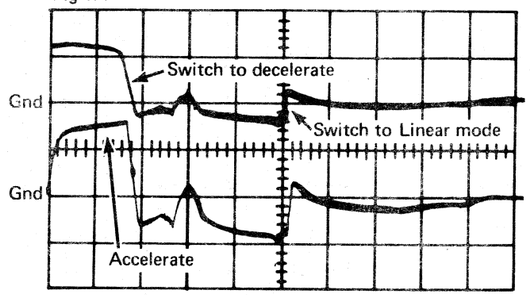
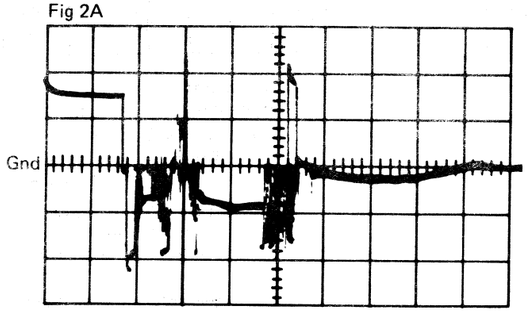


Fig 2A



Setup B - 32 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,02,01,00

Scope Setup:
Sweep: 1 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode

Fig 1B

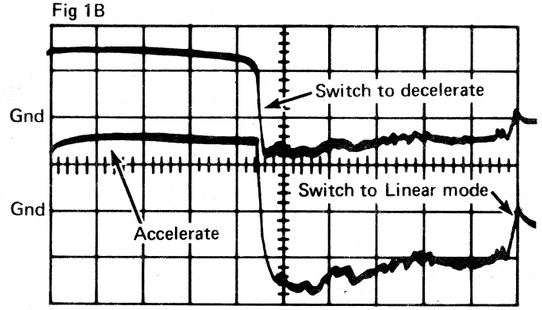
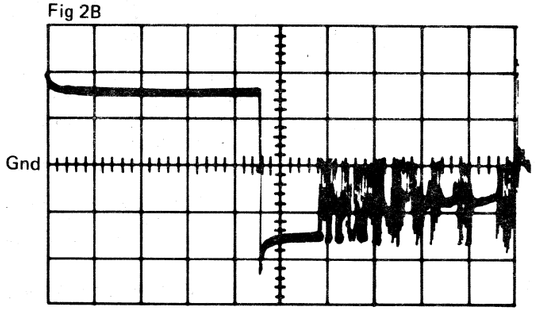


Fig 2B



Setup C - 128 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,01,01,00

Scope Setup:
Sweep: 2 ms/div
Trigger: Slope (+) Ext.
Sync: A1R4B04(Q4B04) + Access Mode

Fig 1C

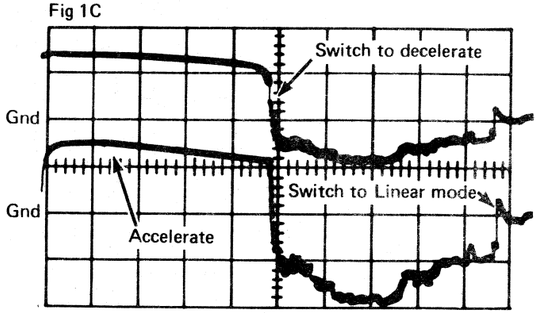
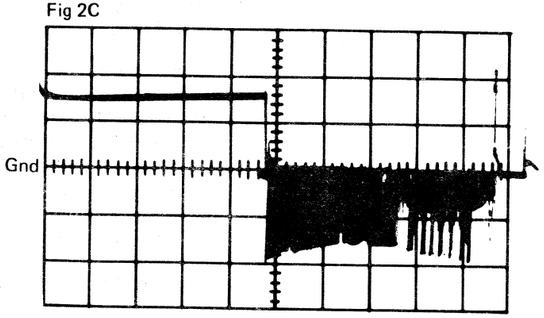


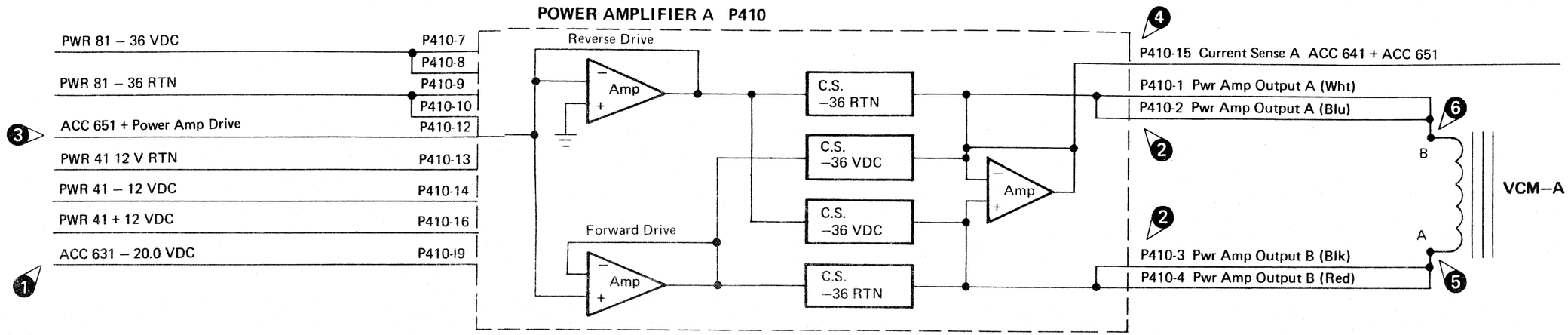
Fig 2C

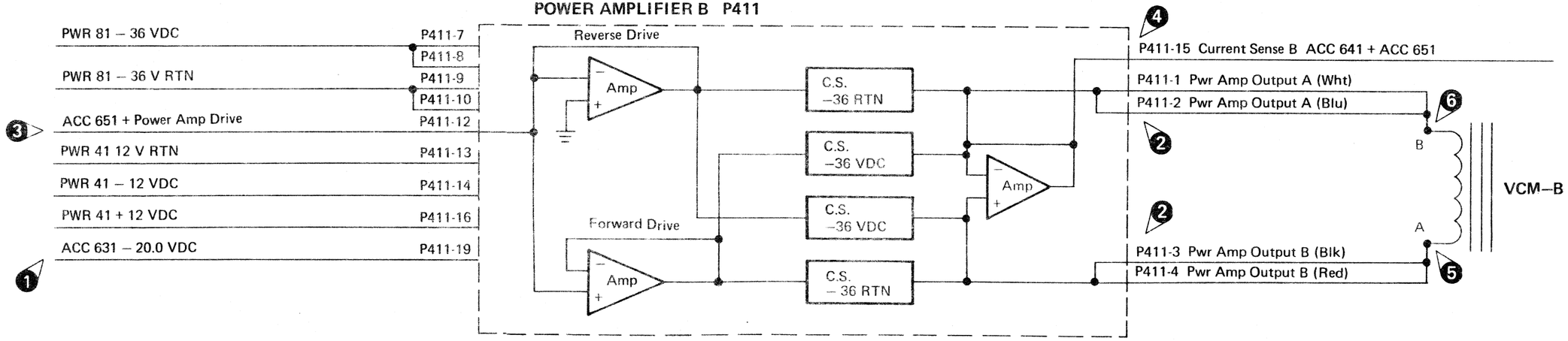


DF0653 Seq. 2 of 2	2747626 Part No. ( )

440202 7 Sept 73	440203 2 Nov 73	440205 28 Jan 74				

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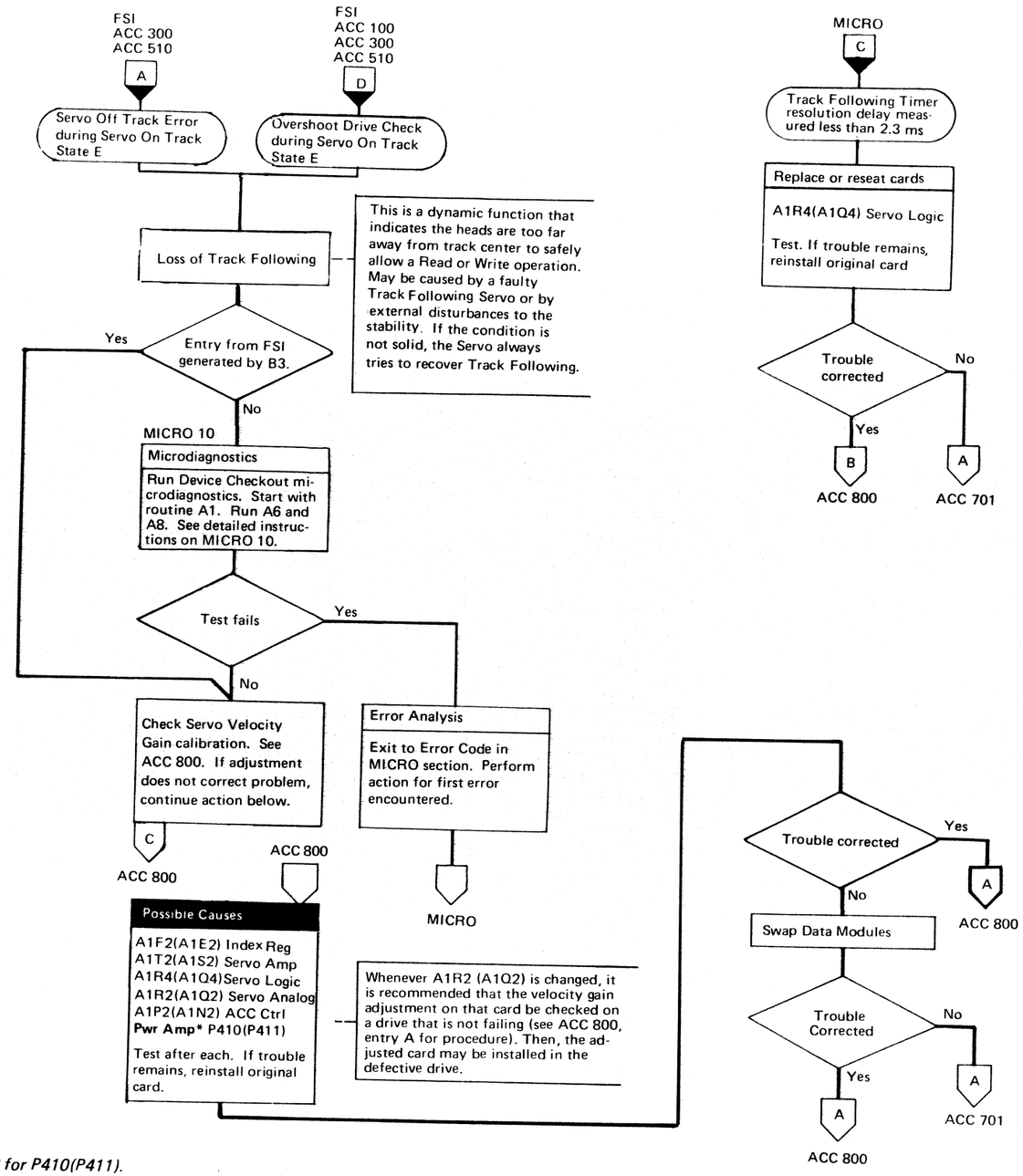
DF0660	2747204
Seq. 1 of 1	Part No. ( )

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440200	440202	440203				
25 Jun 73	7 Sept 73	2 Nov 73				

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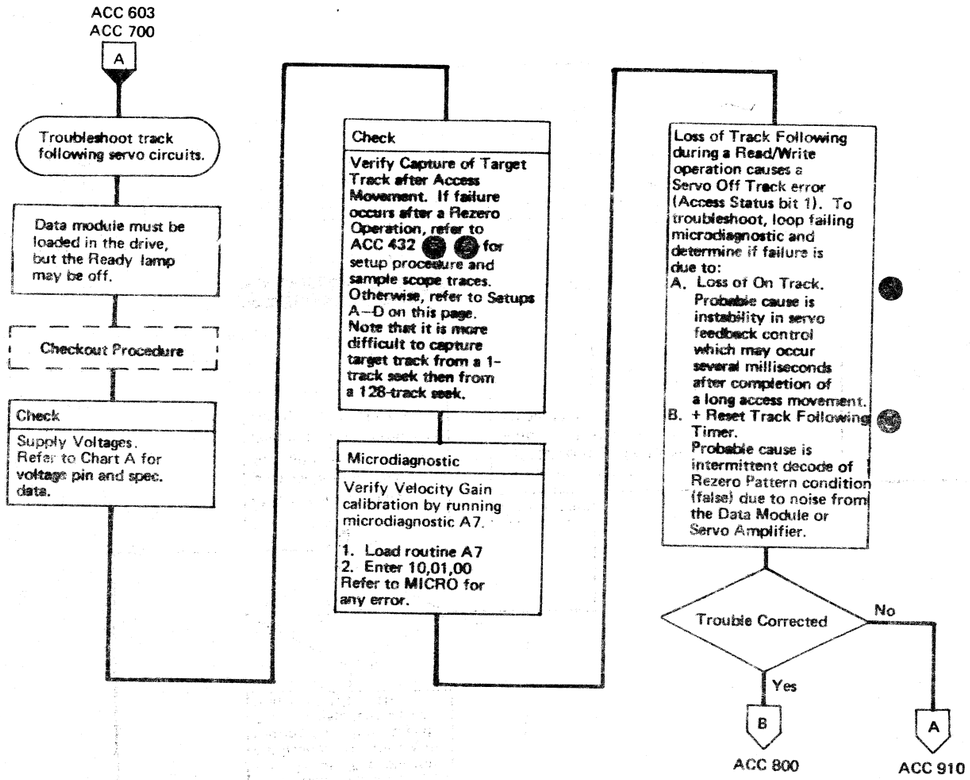
TRACK FOLLOWING SERVO



See LOC 2 for P410(P411).

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TRACK FOLLOWING SERVO



See ACC 702 for test points.

CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Map Exit: Control Module	Map Exit: Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	PWR 50-A	PWR 250-A
A1R4D05 (Q4D05)	+12.0 to +14.4 Vdc	PWR 45-A	PWR 245-A
A1R4D06 (Q4D06)	−12.0 to −14.4 Vdc	PWR 40-A	PWR 240-A
A1R4B06 (Q4B06)	− 3.84 to − 4.16 Vdc	PWR 55-A	
	− 3.72 to − 4.4 Vdc		PWR 255-A
A1R4B11 (Q4B11)	+ 5.76 to + 6.24 Vdc	PWR 60-A	PWR 260-A
A1R4B10 (Q4B10)	−19.6 to −20.4 Vdc	ACC 720-A	ACC 720-A

Scope Setup

Sweep: 0.5 ms/div
Trigger: Slope (–) Ext.
Sync: A1R4B04(Q4B04) (Not) + Access Mode

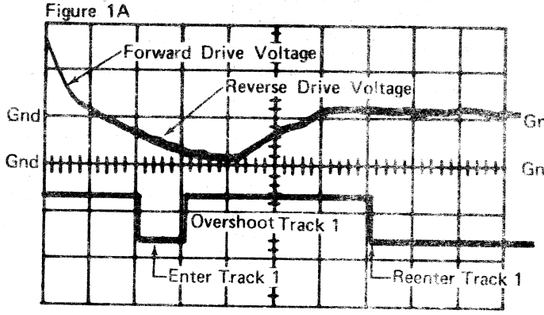
Ch 1 A1R4D02(Q4D02) Compensator
volts/div 0.1
probe X10

Ch 2 A1R4J03 (Q4J03) – On Track
volts/div 0.1
probe X10

Setup A - 1 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,07,01,00

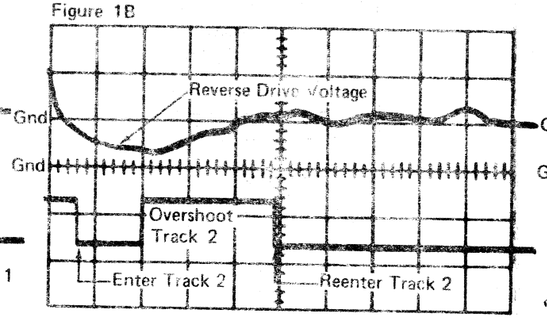
Figure 1A



Setup B - 2 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,06,01,00

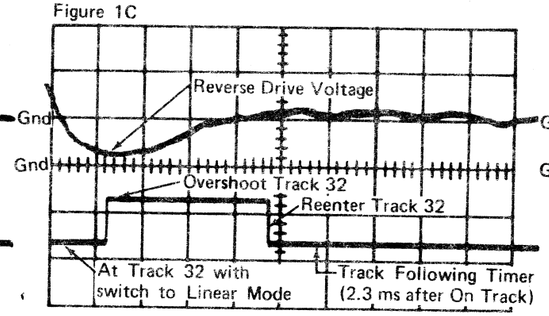
Figure 1B



Setup C - 32 Track Seek

Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,02,01,00

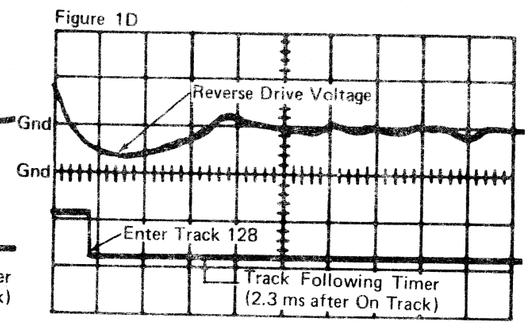
Figure 1C



Setup D - 128 Track Seek

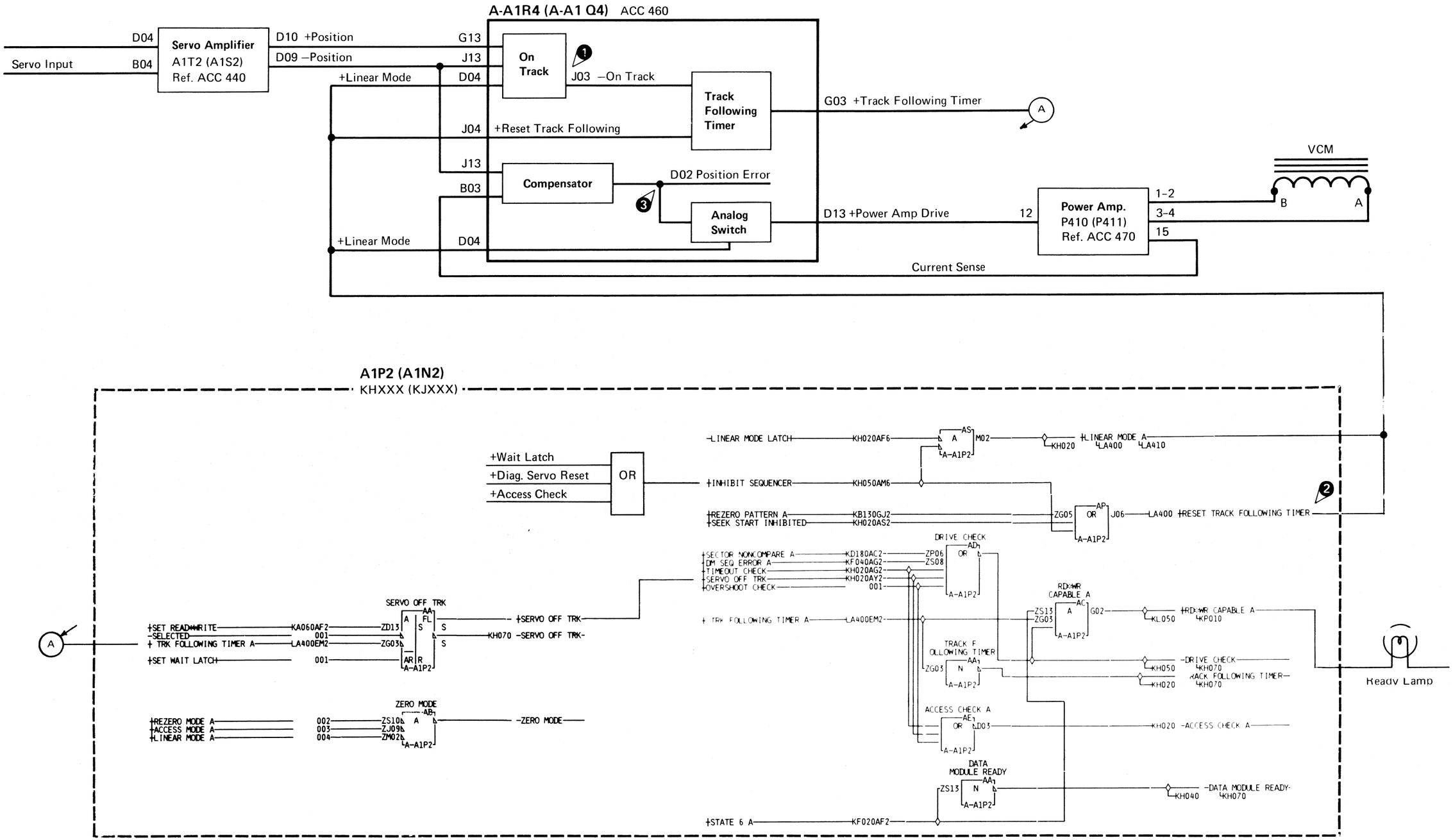
Microdiagnostic A8 test 3
1. Load routine A8
2. Enter 10,03,01,01,00

Figure 1D



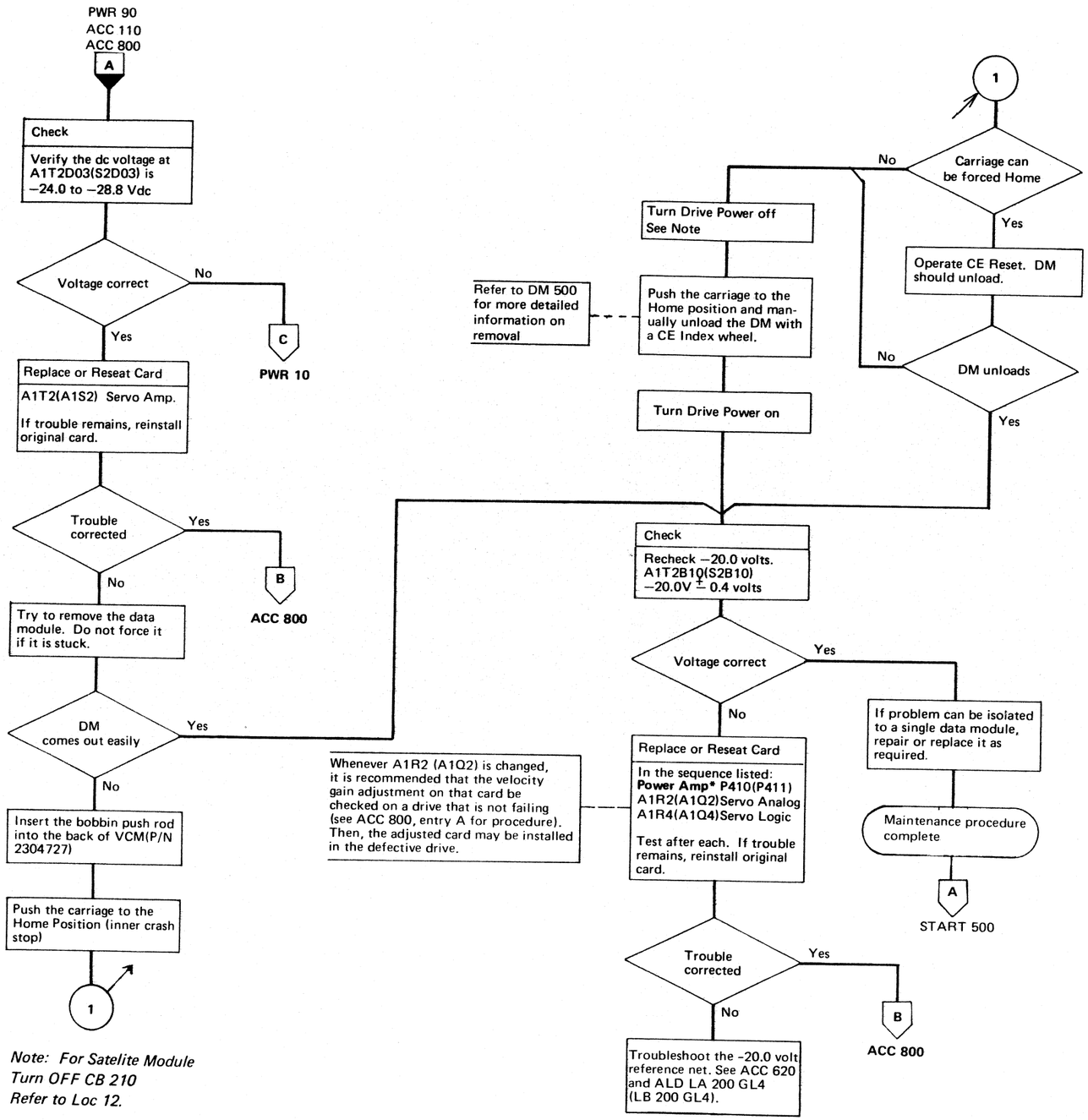
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TRACK FOLLOWING SERVO



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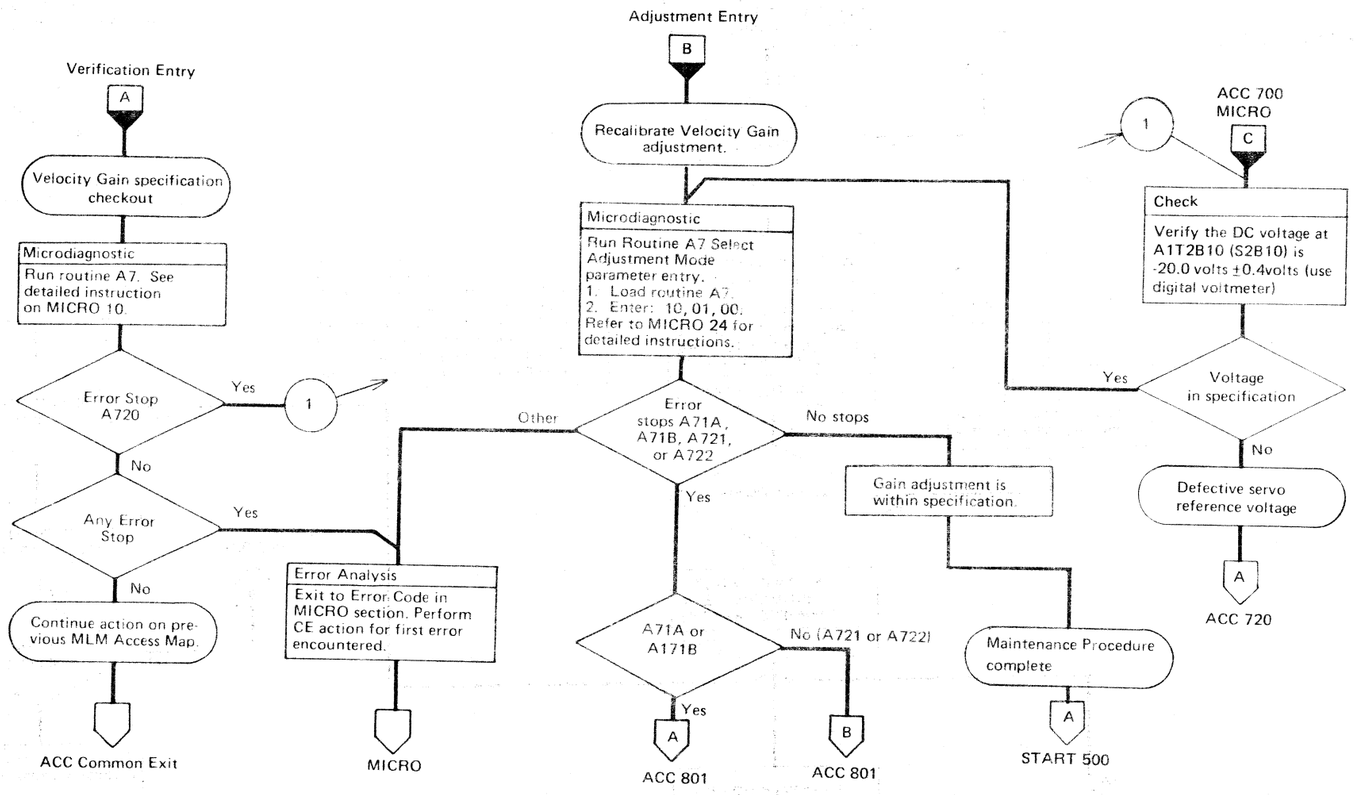
–20.0 VOLT SERVO REFERENCE



*See LOC 2 for P410(P411).

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VELOCITY GAIN CALIBRATION

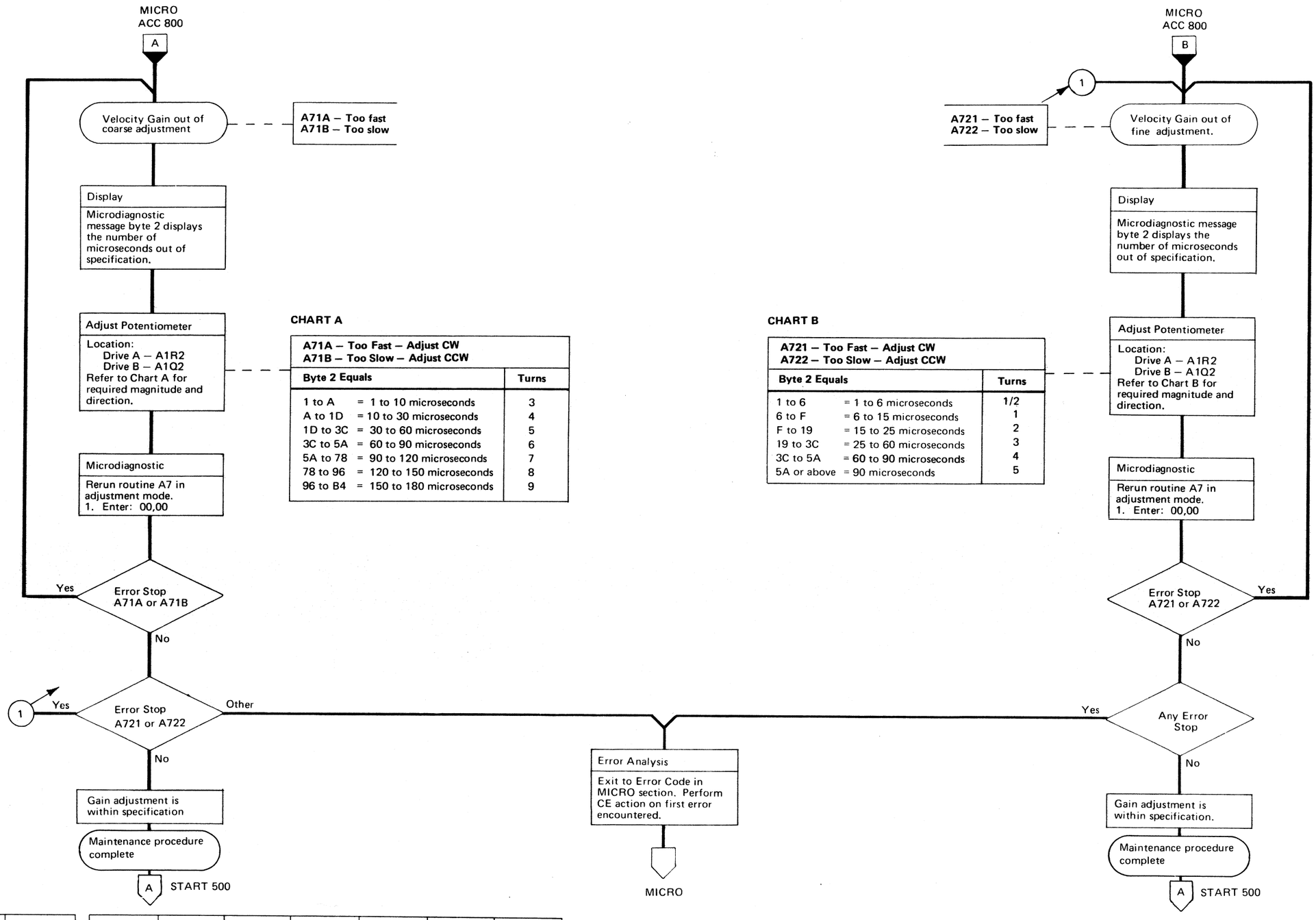


DF0800 Seq. 2 of 2	2747206 Part No. ( )

440200 25 Jun 73	440202 7 Sept 73	440203 2 Nov 73	440204 21 Dec 73	440205 28 Jan 74	440223 14 Mar 75	

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VELOCITY GAIN CALIBRATION

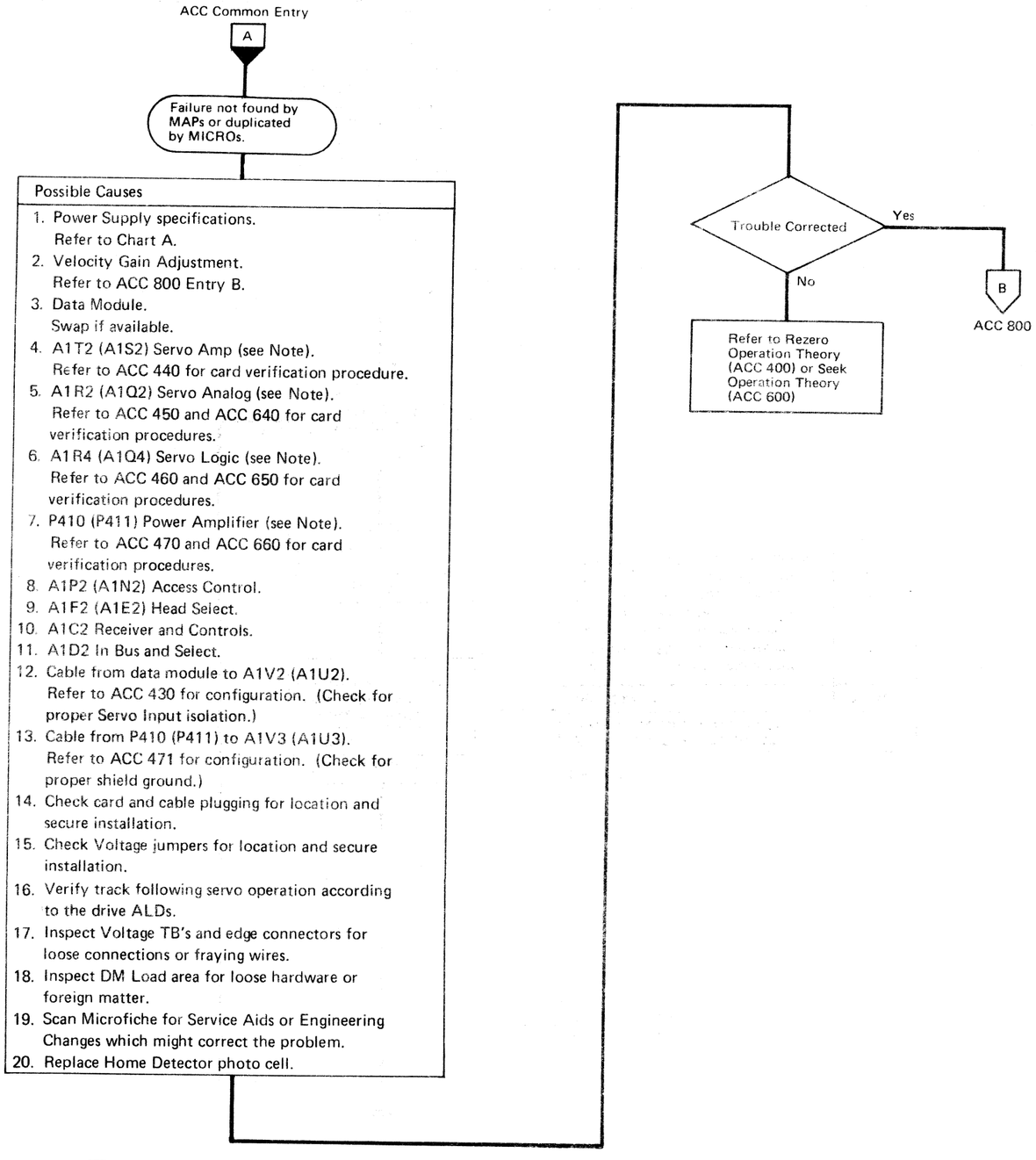


DF0900 Seq. 1 of 2	2747207 Part No. ( )

440200 25 Jun 73	440203 2 Nov 73	440204 21 Dec 73	440205 28 Jan 74	440214 17 Jun 74	440223 14 Mar 75	

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NO TROUBLE FOUND



Note: Card replacement should be followed by Velocity Gain calibration before retesting drive operation. Refer to the procedure on ACC 800 Entry B.

CHART A – POWER SUPPLY VOLTAGES

Measuring Point	Voltage Range	Maximum Ripple	Map Exit	
			Control Module	Satellite Module
A1R2D03 (Q2D03)	−24.0 to −28.8 Vdc	0.08 V p-p	PWR 50-A	PWR 250-A
A1R2D05 (Q2D05)	+12.0 to +14.4 Vdc	0.10 V p-p	PWR 45-A	PWR 245-A
A1R2D06 (Q2D06)	−12.0 to −14.4 Vdc	0.10 V p-p	PWR 40-A	PWR 240-A
A1R2G06 (Q2G06)	− 3.84 to − 4.16 Vdc	0.04 V p-p	PWR 55-A	
	− 3.72 to − 4.4 Vdc	0.16 V p-p		PWR 255-A
A1R2G11 (Q2G11)	+ 5.76 to + 6.24 Vdc	0.08 V p-p	PWR 60-A	PWR 260-A
A1T2B08 (S2B08)	− 1.28 Vdc (nominal)	———	ACC 441	ACC 441
A1T2B10 (S2B10)	−19.6 to −20.4 Vdc	0.07 V p-p	ACC 720-A	ACC 720-A
P410–7,8 (P411–7,8)	−36.0 to −43.2 Vdc	0.14 V p-p	PWR 80-A	PWR 280-A
P410–14 (P411–14)	−12.0 to −14.4 Vdc	0.10 V p-p	PWR 40-A	PWR 240-A
P410–16 (P411–16)	+12.0 to +14.4 Vdc	0.10 V p-p	PWR 45-A	PWR 245-A
P410–9,10 (P411–9,10)	Ground	———	YA060 (YB060)	YA060 (YB060)
P410–13 (P411–13)	Ground	———	YA060 (YB060)	YA060 (YB060)

See LOC 4 for location of P410/411.

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R/W CONTENTS

R/W MAPs – – – – – – – – – – – – **R/W 200–350**

Provides maintenance procedures for analyzing drive-related R/W data problems

Write Operations in Drive – – – – – **R/W 100**

Detailed Read Operation Description – **R/W 315–350**

Provides more detailed Read theory. Tied directly to MAPs.

Read/Write Control – – – – – – – – **OPER 210–218**

Description of Set R/W and Reset R/W with circuit and timing diagrams.

Write Operation Description – – – – **OPER 225–227**

High-level description of a Write operation with data flow and timing diagrams.

Read Operation Description – – – – **OPER 230–232**

High-level description of a Read operation with data flow and timing diagrams.

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WRITE OPERATIONS IN DRIVE

Refer to OPER 225 for an overview of Write operations.

1. To activate the Read/Write controls in the drive, the Set Read/Write Tag is held active in the drive. The appropriate Bus Out bits set the Read or Write controls. These two functions are provided by the controller.

2. When the Write controls in the drive are active, the controller supplies Write Data to the selected drive.

3. During Write operations, all safety conditions are monitored to ensure that all Write controls are functioning correctly. If a Safety Check is detected, Read/Write Safe is deactivated, which suspends all further writing. Read/Write Check (Bus in bit 3) is activated to signal the controller an error has occurred, and the type of Read/Write Check is latched for further sensing.

4. The following controls are necessary to write data (See R/W 101):

   Write Gate **A** must be active to the R/W matrix card.

   Current Source Blocked **B** must be inactive to the R/W matrix card.

   Read Transmit **C** must be inactive at the Read Detector.

   One R/W head **D** must be selected.

   Write Data **E** must be present at the R/W matrix card.

   Read/Write Safe **F** must be active indicating no Read/Write Check conditions.

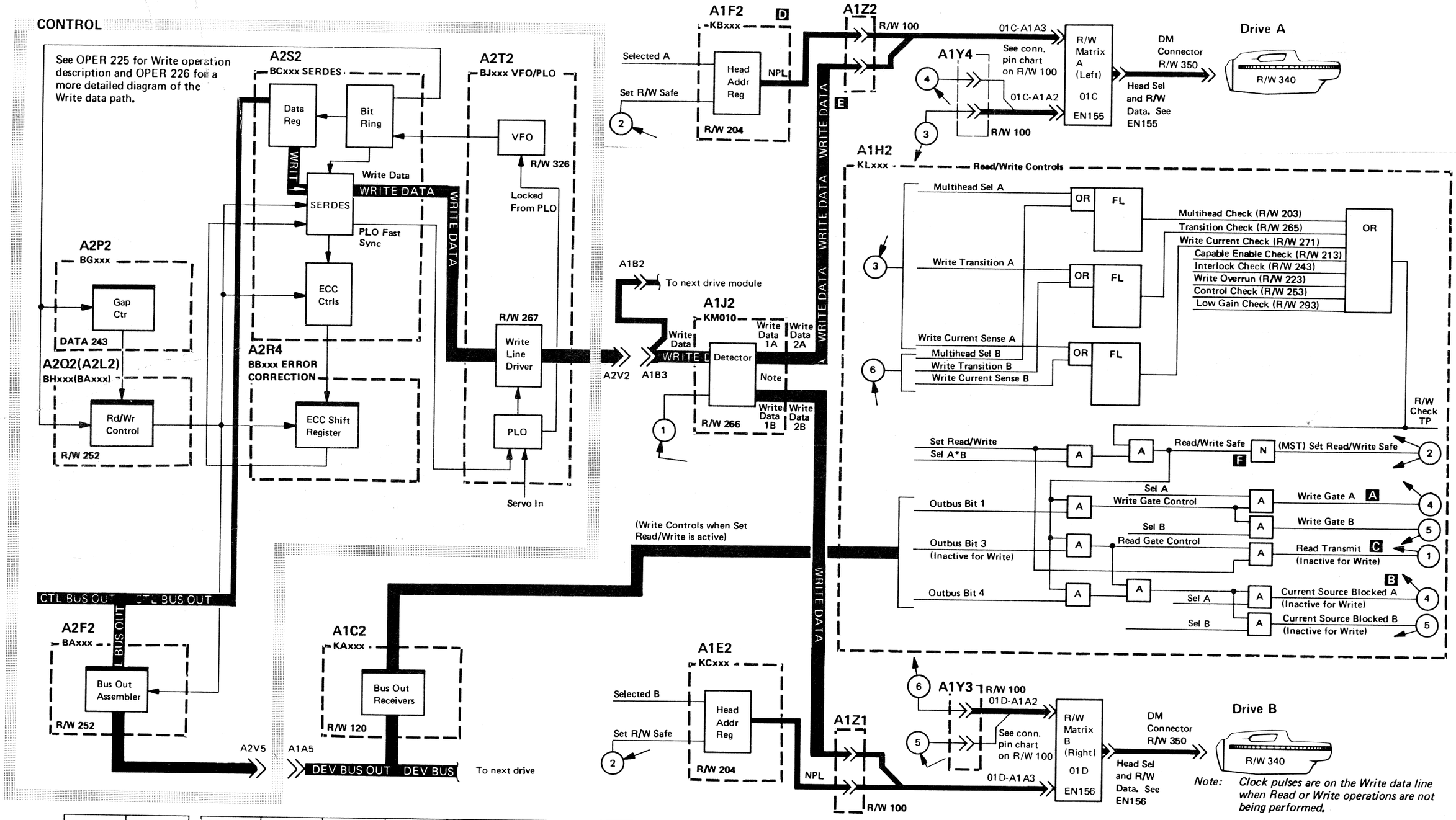
5. Detailed information on Read/Write Checks are on the following pages:

Capable Enable Check	R/W 210–213
Control Check	R/W 250–253
Read/Write Interlock Check	R/W 240–243
Low Gain Check (Optional Feature)	R/W 293
Multihead Check	R/W 200–205
Read/Write Check and Sense	R/W 280–283
Write Current Check	R/W 270–275
Write Overrun Check	R/W 200–223
Write Transition Check	R/W 260–269

R/W Matrix Card Signals

Line Name	Card		A-DRIVE Cable (A1 Board to R/W Matrix)		B-DRIVE Cable (A1 Board to R/W Matrix)		Read/Write Matrix Card Pin	Normal Level	Read/Write Matrix Card Cable 01C(01D)
	A-Drive	B-Drive	Conn. Pin (R/W 303)	Bd.Exit Pin	Conn. Pin (R/W 303)	Bd Exit Pin			
– Head Select 0	A1F2S12	A1E2S12	Z2B13	A1G6A04	Z1B13	A1C6E04	G13	NPL +6 V = Inactive 0 V = Active	A1A3B13
" 1	A1F2S13	A1E2S13	Z2D10	A1F6C02	Z1D10	A1C6B02	J10		A1A3D10
" 2	A1F2U13	A1E2U13	Z2B06	A1E6D04	Z1B06	A1B6C04	G06		A1A3B06
" 3	A1F2U09	A1E2U09	Z2D06	A1E6D02	Z1D06	A1B6C02	J06		A1A3D06
" 4	A1F2S09	A1E2S09	Z2D07	A1E6E02	Z1D07	A1B6D02	J07		A1A3D07
" 5	A1F2S08	A1E2S08	Z2D11	A1F6D02	Z1D11	A1C6C02	J11		A1A3D11
" 6	A1F2U06	A1E2U06	Z2B09	A1F6B04	Z1B09	A1C6A04	G09		A1A3B09
" 7	A1F2S05	A1E2S05	Z2D05	A1E6C02	Z1D05	A1B6B02	J05		A1A3D05
" 8	A1F2U10	A1E2U10	Z2B12	A1F6E04	Z1B12	A1C6D04	G12		A1A3B12
" 9	A1F2U12	A1E2U12	Z2D09	A1F6B02	Z1D09	A1C6A02	J09		A1A3D09
" 10	A1F2S10	A1E2S10	Z2B10	A1F6C04	Z1B10	A1C6B04	G10		A1A3B10
" 11	A1F2U11	A1E2U11	Z2B08	A1F6A04	Z1B08	A1B6E04	G08		A1A3B08
– Write Transitions	A1H2P04	A1H2M04	Z2D02	A1D6E02	Z1D02	A1A6D02	J02	MST	A1A3D02
– Write Current Sense	A1H2P05	A1H2P06	Z2B04	A1E6B04	Z1B04	A1B6A04	G04	MST	A1A3B04
Write Data Output 1	A1J2B04	A1J2D05	Z2D03	A1E6A02	Z1D03	A1A6E02	J03	MST	A1A3D03
Write Data Output 2	A1J2B05	A1J2D07	Z2B02	A1D6E04	Z1B02	A1A6D04	G02	MST	A1A3B02
– Rd Wr Intlk Open			Z2D13	A1G6A02	Z1D13	A1C6E02	J13	–4 V to +MST	A1A3D13
+ Squelch	A1H2J04	A1H2G03	Y4D09	A1N1A11	Y3D09	A1J1C11	D09	0 V to +1.5 V	A1A2D09
– Current Source Blkd	A1H2M05	A1H2M07	Y4B12	A1N1D13	Y3B12	A1K1A13	B12	0 to +6 V	A1A2B12
– Write Gate	A1H2D06	A1H2B12	Y4D11	A1N1C11	Y3D11	A1J1E11	D11	0 to +6 V	A1A2D11
+ Read Gate	A1H2D02	A1H2B05	Y4B05	A1M1B13	Y3B05	A1H1D13	B05	0 to +2.3 V	A1A2B05
– Multiple Head Select	A1H2P09	A1H2M09	Y4D13	A1N1E11	Y3D13	A1K1B11	D13	MST	A1A2D13
– Rd Wr Intlk Open			Y4D03	A1J1E11	Y3D03	A1H2B11	D03	–4 V to +MST	A1A2D03
– Read Signal Output 1	A1J2G02	A1J2G02	Y4B02	A1L1D13	Y3B02	A1H1A13	B02		A1A2B02
– Read Signal Output 2	A1J2J02	A1J2J02	Y4D02	A1L1D11	Y3D02	A1H1A11	D02		A1A2D02
+Low Gain Sense (Optional Feature)	A1H2J13	A1H2M02	Y4B04	A1M1A13	Y3B04	A1H1C13	B04	MST	A1A2B04

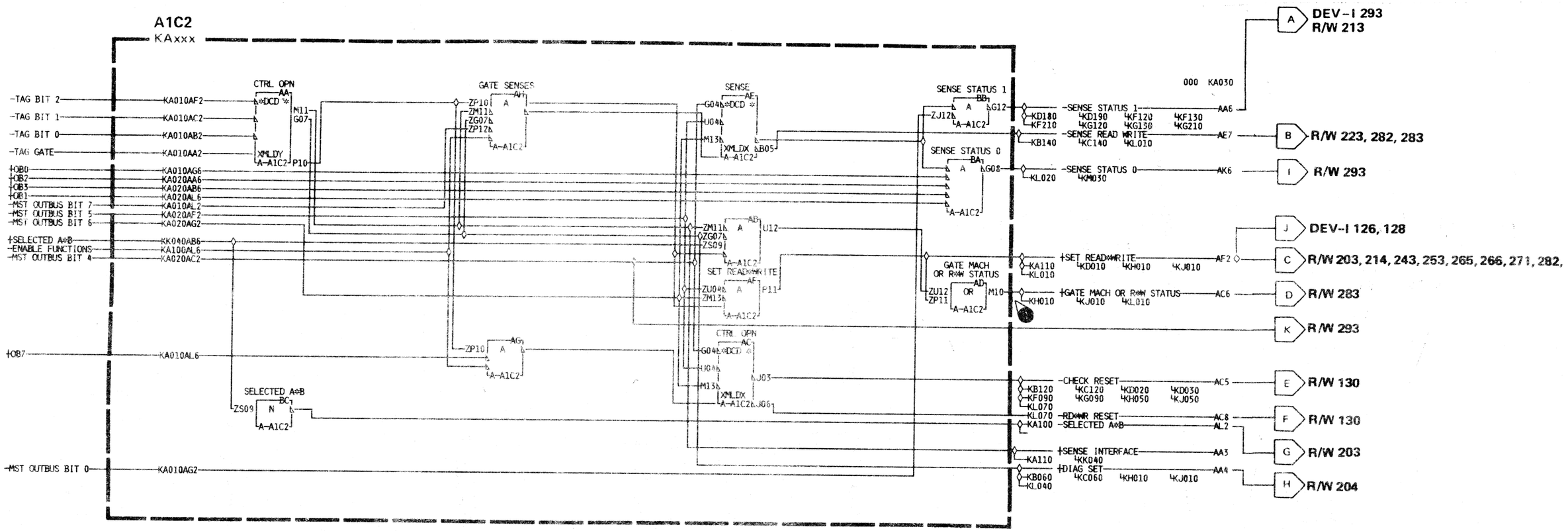
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DG0010 Seq. 1 of 2	2747527 Part No. ( )

440200	440203	440204	440205	440209	440218	440223
25 Jun 73	2 Nov 73	21 Dec 73	28 Jan 74	25 Mar 74	5 Aug 74	14 Mar 75

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DRIVE COMMAND DESCRIPTION FOR READ/WRITE OP

SENSE STATUS 1 – Bit 4 status byte indicates selected drive is Write Enabled (other bits are not meaningful for Read/Write).

SENSE READ/WRITE – Status byte indicates type of Read/Write check. See R/W 280 for bit definition.

SET READ/WRITE – Held active during Read or Write. Subsequent device bus out information determines Read or Write controls. Allows special Read/Write controls on bus in (bus in 6=index, bus in 7=active track).

GATE MACH OR R/W STATUS – Allows bus in bit 3 (Read/Write check) to be available to the interface.

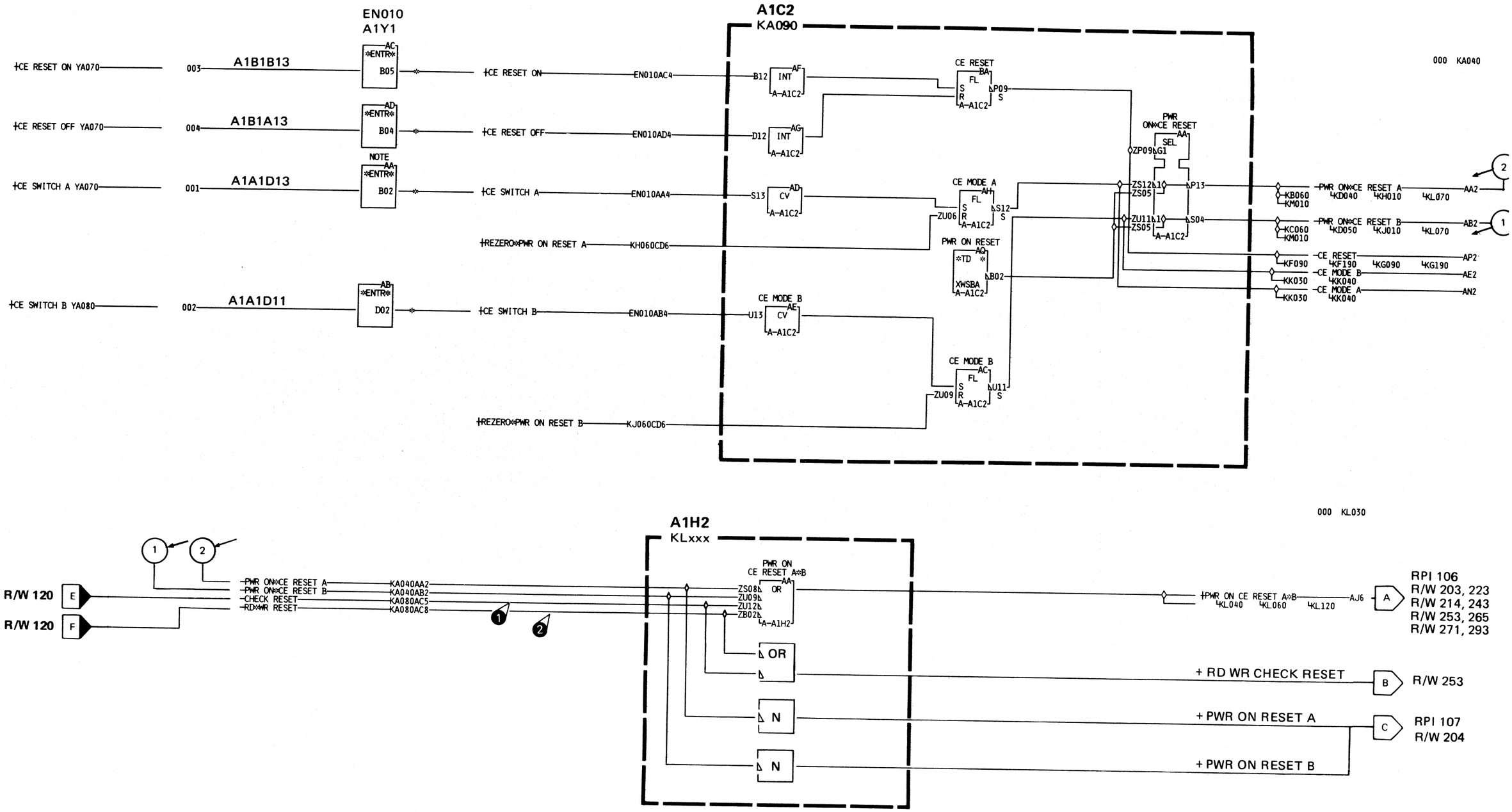
R/W RESET – Resets all Read/Write check latches.

CHECK RESET – Resets all Read/Write check latches.

DIAG SET – Used to force multihead select error.

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COMMON READ/WRITE CHECK LATCH RESET



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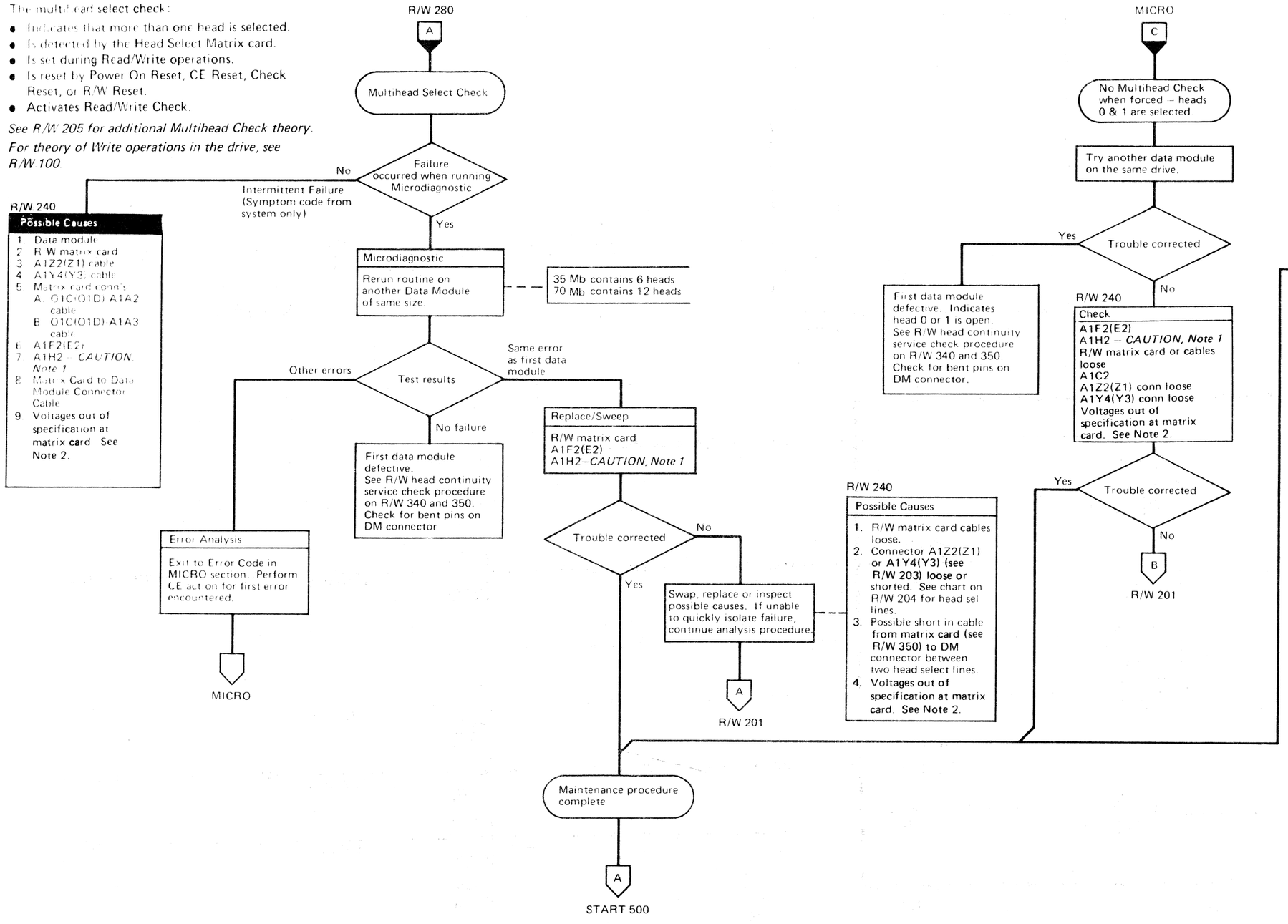
MULTIHEAD CHECK

The multihead select check:

- Indicates that more than one head is selected.
- Is detected by the Head Select Matrix card.
- Is set during Read/Write operations.
- Is reset by Power On Reset, CE Reset, Check Reset, or R/W Reset.
- Activates Read/Write Check.

See R/W 205 for additional Multihead Check theory.

For theory of Write operations in the drive, see R/W 100.



Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: –4 Vdc (–3.84 V to –4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin.

If either of these voltages is not as specified, go to PWR 10, Entry C.

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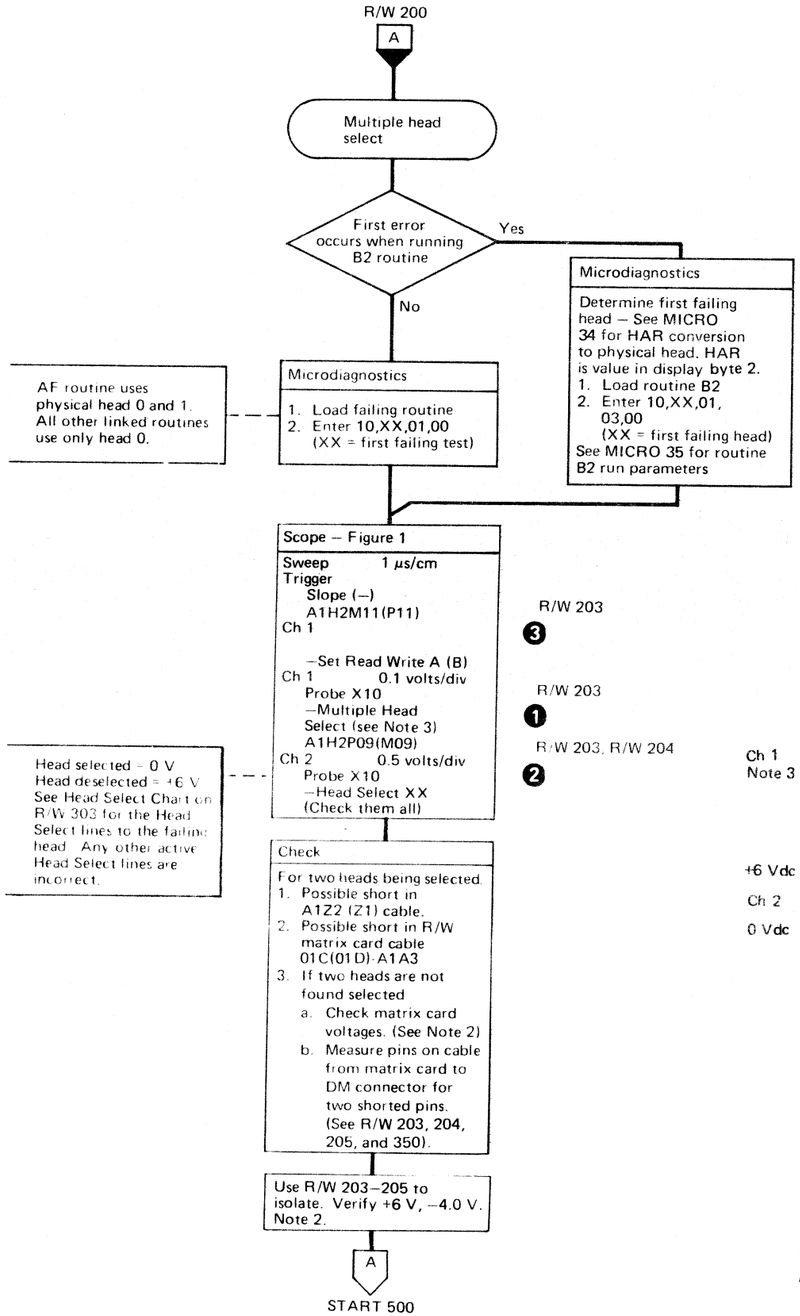
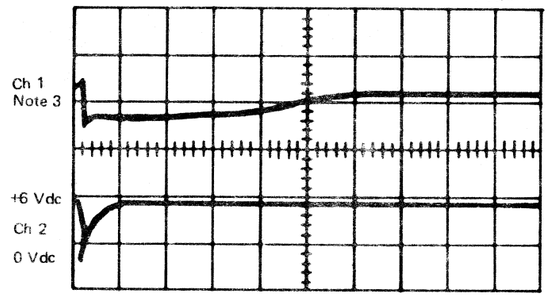


Figure 1

Typical error condition – Note that the Head Select line is only active until multihead check occurs.



Note 1: If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.

Note 2: –4 Vdc (–3.84 V to –4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin.

If either of these voltages is not as specified, go to PWR 10, Entry C

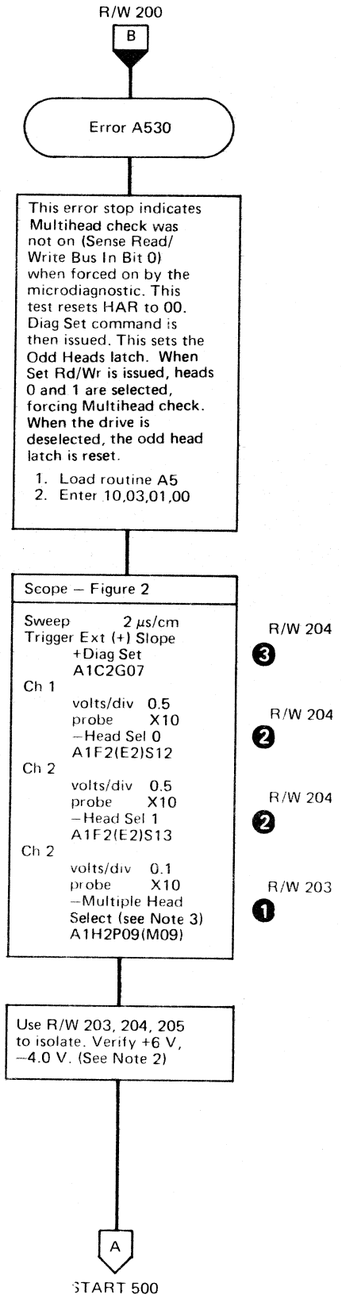
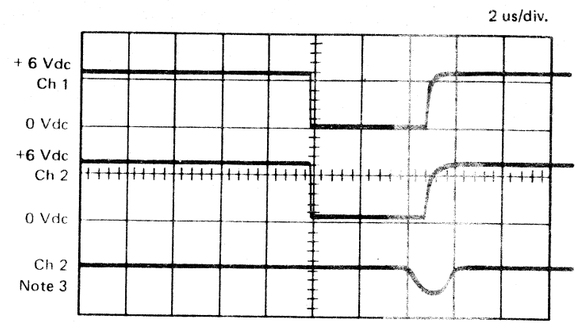


Figure 2. A530 Error (see Timing Chart on R/W 202)



Note 3: –Multiple Head Select signal may not reach a stable –MST level as Multihead Check will degate Head Select lines

DG0020	2747707	440203	440205	440209	440214	440218	440223	
Seq. 1 of 1	Part No. ( )	2 Nov 73	28 Jan 74	25 Mar 74	17 Jun 74	5 Aug 74	14 Mar 75	

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MULTIHEAD CHECK

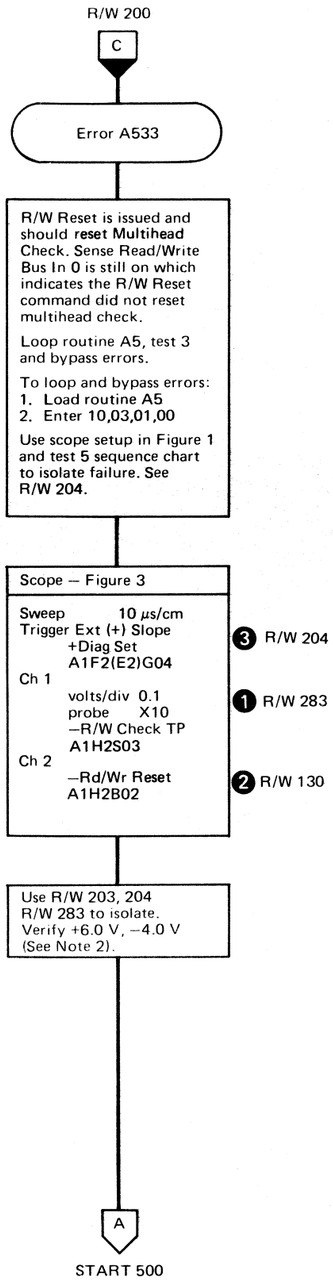
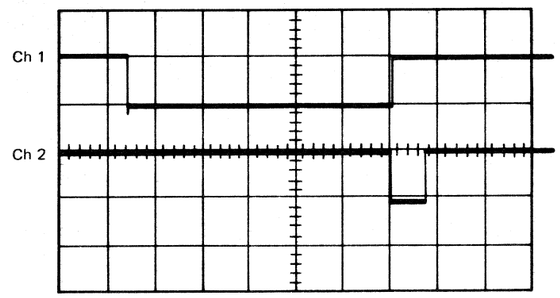


Figure 3

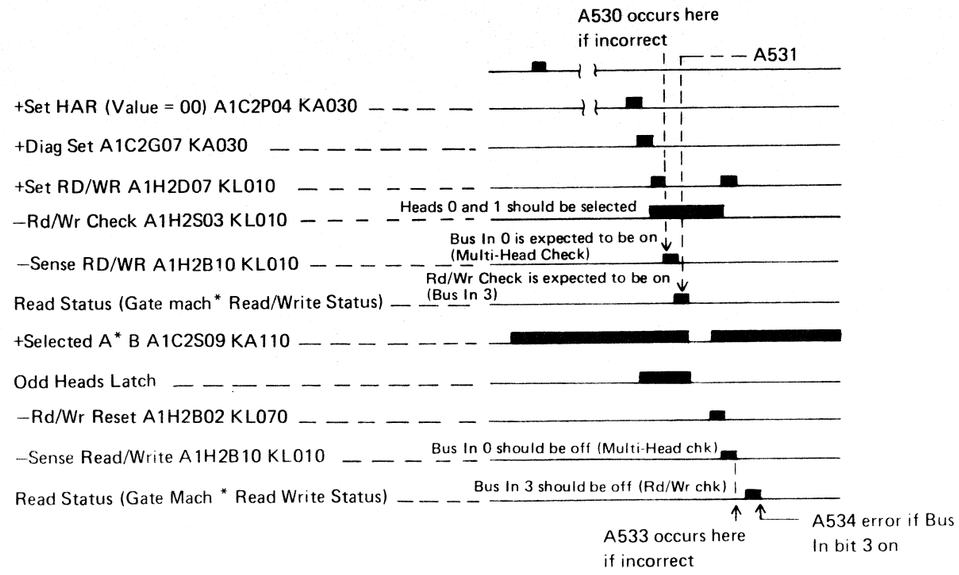


Note 1: If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.

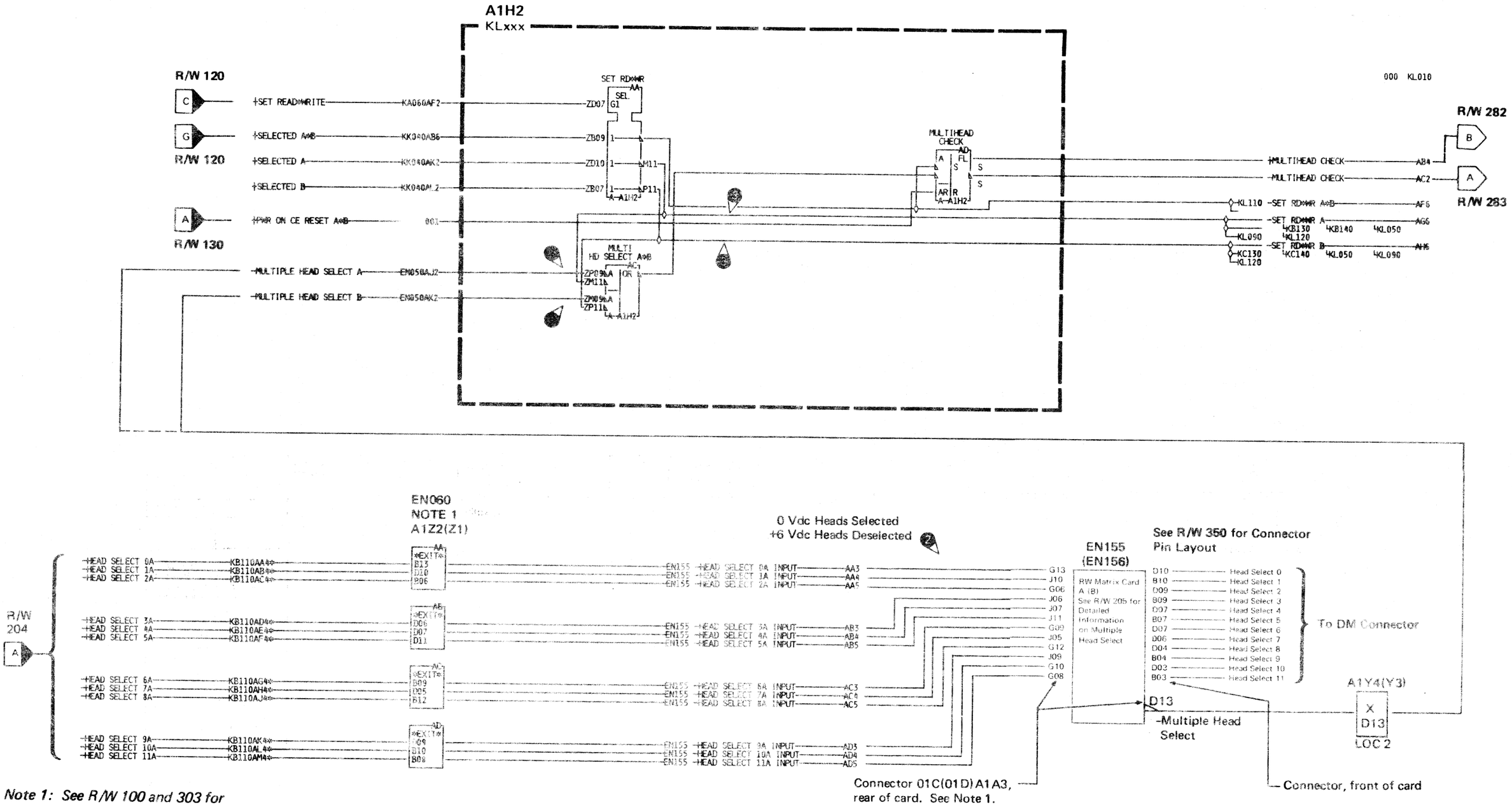
Note 2: –4 Vdc (–3.84 V to –4.16 V) A1H1E13 to Y3B06 (A1M1C13 to Y4B06) to matrix card pin B06.

+ 6 Vdc (+5.76 V to + 6.24 V) A1K1B13 to Y3B13 (A1N1F13 to Y4B13) to matrix card pin B13.

If either of these voltages is not as specified, go to PWR 10 Entry C.



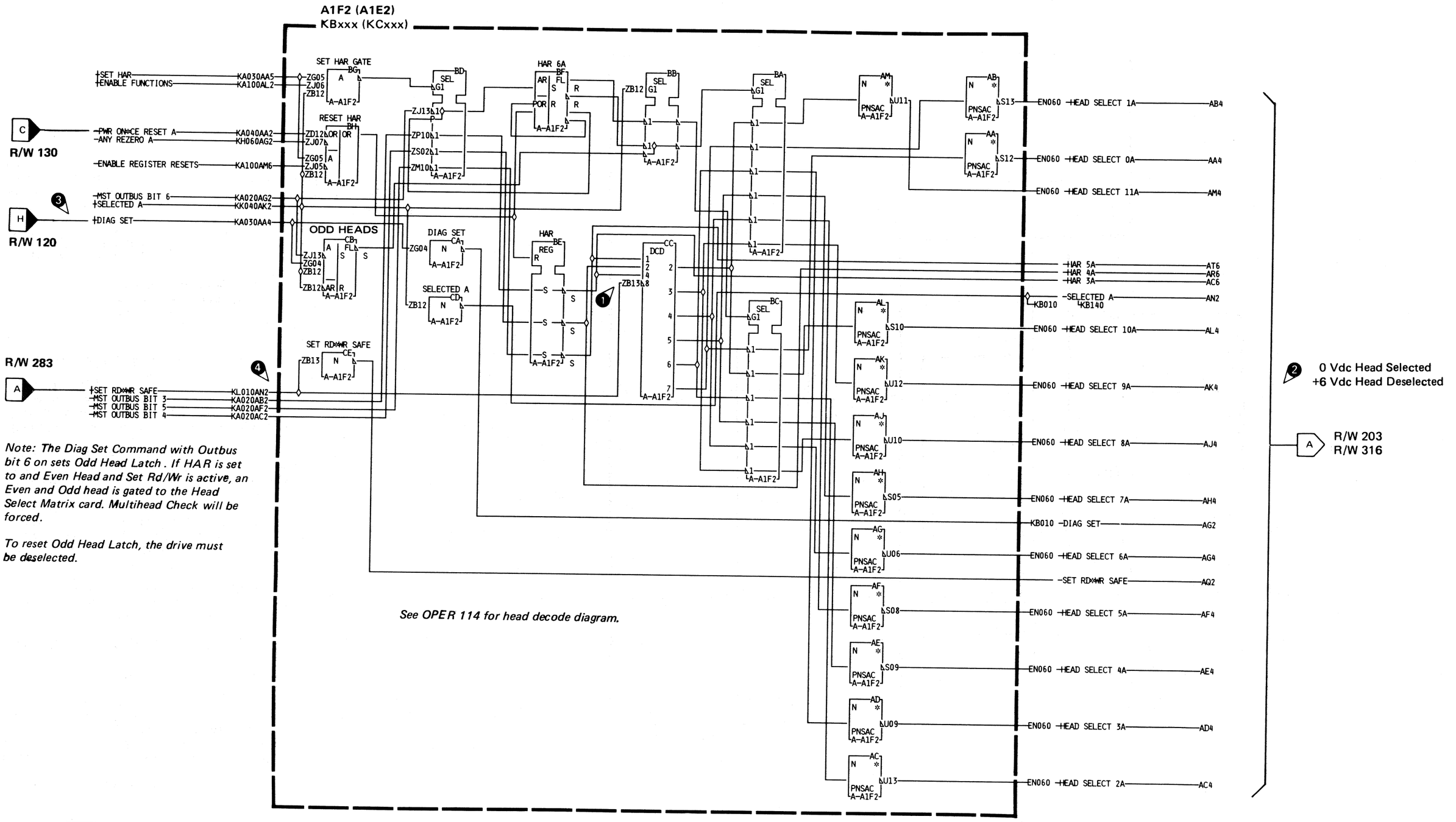
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Note 1: See R/W 100 and 303 for pin chart of head select lines.

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MULTIHEAD CHECK



Note: The Diag Set Command with Outbus bit 6 on sets Odd Head Latch . If HAR is set to and Even Head and Set Rd/Wr is active, an Even and Odd head is gated to the Head Select Matrix card. Multihead Check will be forced.

To reset Odd Head Latch, the drive must be deselected.

See OPER 114 for head decode diagram.

DG0027	2747828
Seq. 1 of 2	Part No.( )

440209	440218	440223			
25 Mar 74	5 Aug 74	14 Mar 75			

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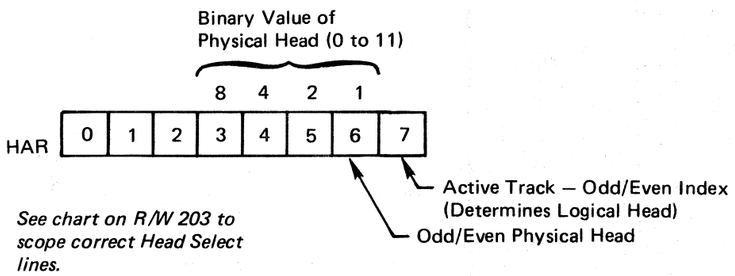
MULTIPLE HEAD SELECT

When set Read/Write is active in the drive, the HAR value is gated to the Head Select lines which activate Head Select transistors. If two or more heads are selected, the input to the level detector shifts and causes the – Multiple Head Select line to change to – MST.

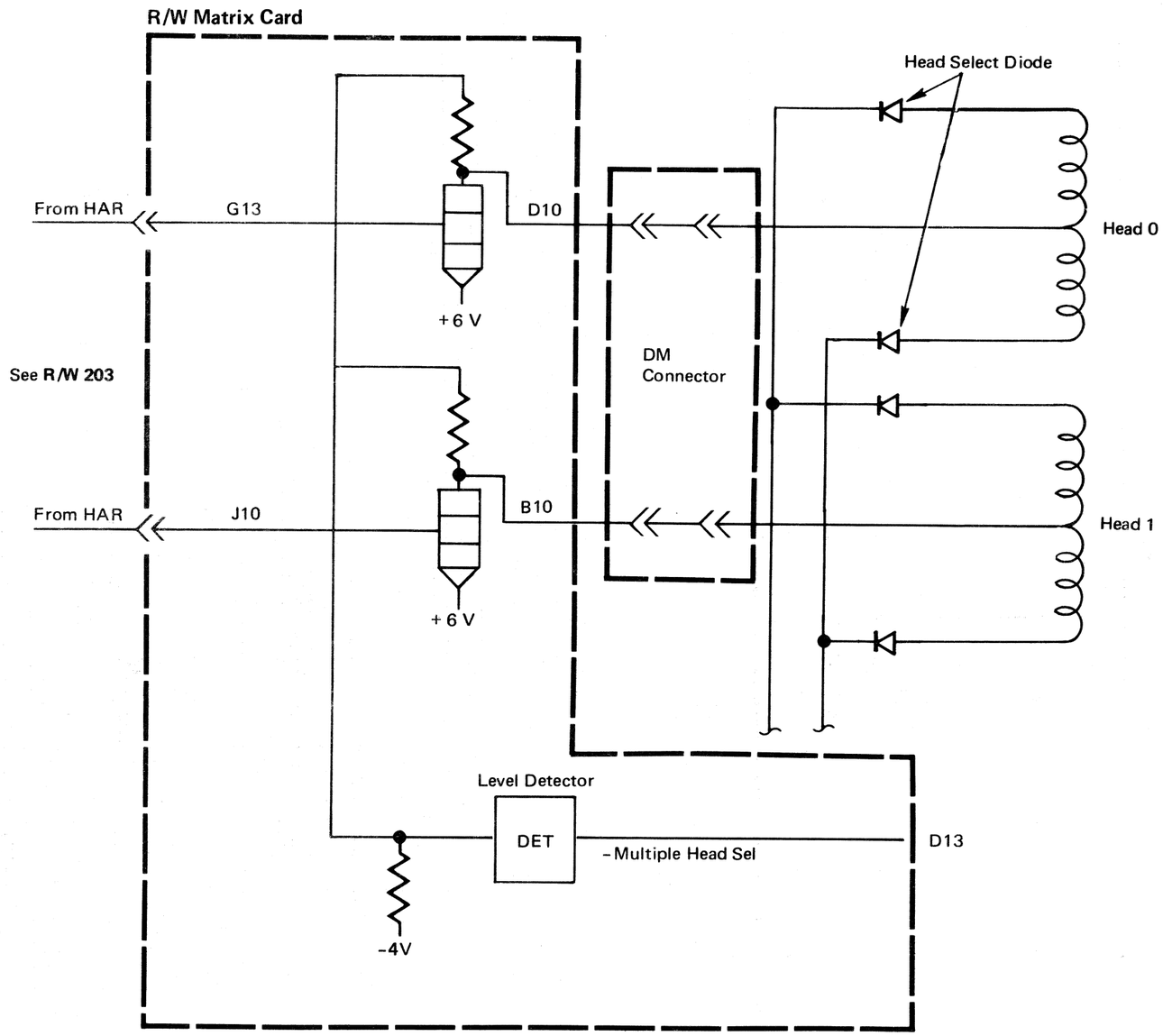
For theory of Write operations in the drive, see R/W 100.

Possible Causes of Multiple Head Checks

- If a Head Select diode in the data module is shorted, the output of the level detector changes to – MST when any other head is selected. The error follows the data module.
- If a short between two Head Select lines occurs in the cable from the A1 board to the R/W matrix card, the level detector output changes to – MST when either of the two heads are selected.
- If two Head Select lines are active from the head address card (A1F2 – A drive, A1E2 – B drive), the level detector changes to – MST.
- If one Head Select line is active all the time, all other heads selected cause the level detector output to change to – MST (Problem in A1F2 – A drive, A1E2 – B drive).
- Faulty check latch on A1H2 card.



See chart on R/W 203 to scope correct Head Select lines.



DG0027	2747828
Seq. 2 of 2	Part No.( )

440209	440218	440223				
25 Mar 74	5 Aug 74	14 Mar 75				

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CAPABLE ENABLE CHECK

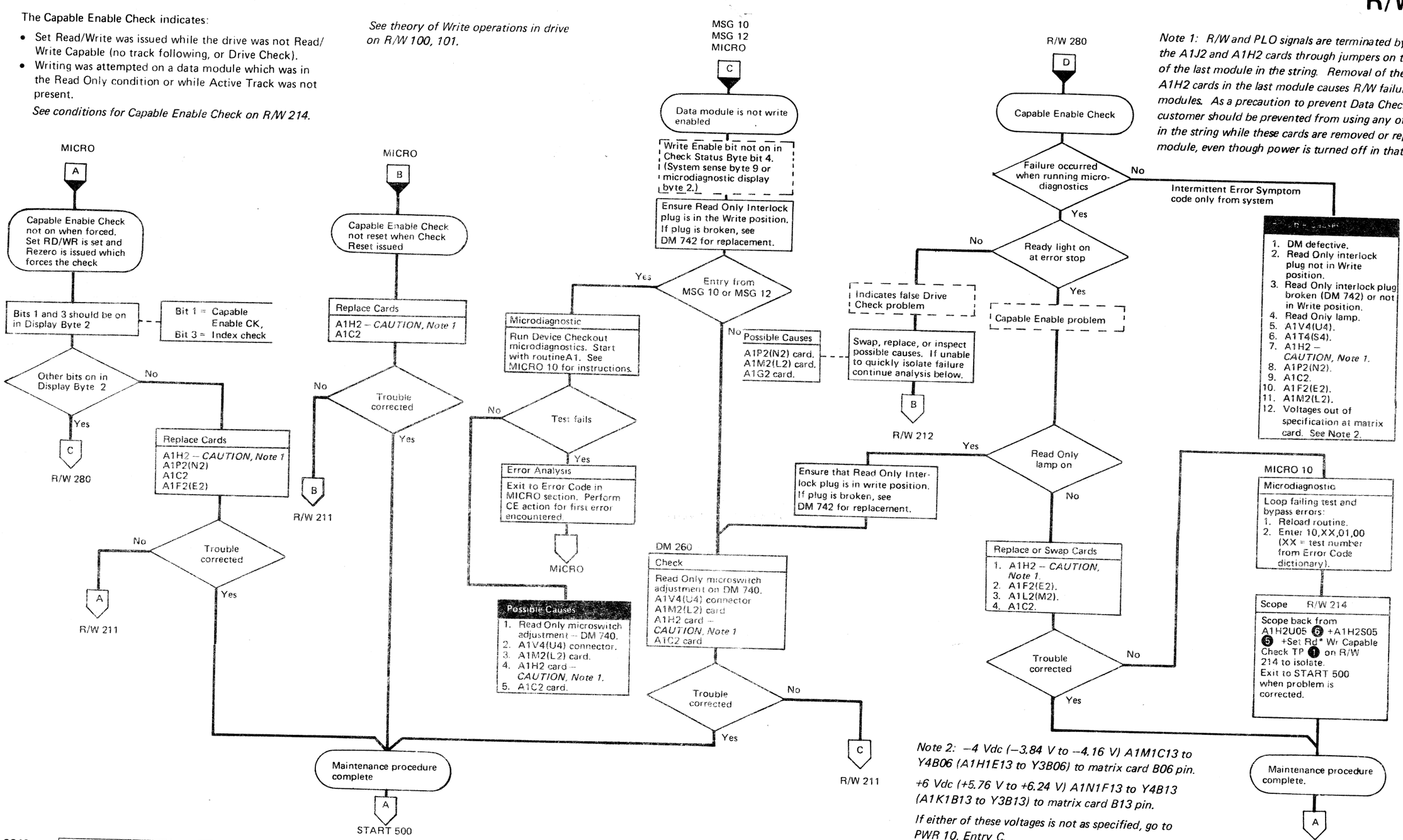
The Capable Enable Check indicates:

- Set Read/Write was issued while the drive was not Read/Write Capable (no track following, or Drive Check).
- Writing was attempted on a data module which was in the Read Only condition or while Active Track was not present.

See conditions for Capable Enable Check on R/W 214.

See theory of Write operations in drive on R/W 100, 101.

Note 1: R/W and PLO signals are terminated by resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removal of the A1J2 or A1H2 cards in the last module causes R/W failures in other modules. As a precaution to prevent Data Checks, the customer should be prevented from using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module.



Note 2: –4 Vdc (–3.84 V to –4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin.

If either of these voltages is not as specified, go to PWR 10, Entry C.

DG0030	2747708
Seq. 2 of 2	Part No. ( )

440203	440205	440209	440218	440223		
2 Nov 73	28 Jan 74	25 Mar 74	5 Aug 74	14 Mar 75		

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CAPABLE ENABLE CHECK

R/W 210 A

A384 Error

Capable Enable Check is forced on in test. A Re-zero command is given. Set Read Write is then issued. Capable Enable Check will then occur because the servo is no longer on track. Sense Read Write Command is issued and Bus In bit 1 is expected to be on. Use scope procedure in Figures 1 and 2. Use R/W 213 and 214 to isolate problem. This is the first test that issues +Set Read Write to the drive.

Microdiagnostic
1. Load routine A3
2. Enter 10, 08, 01, 00

Scope Figure 1
Sweep 10 ms/div
Trigger
Slope (+) Ext
A1H2D10(B02)
+Selected A(B)
Ch 1 A1H2D07
+Set Read Write
Volts/div 0.1
probe X10
Ch 2 A1P2(N2)G02
+Rd/Wr Capable
Volts/div 0.1
probe X10
Use R/W 213 to isolate

R/W 214 ⑦
R/W 213 ④

R/W 210 B

A388

Capable Enable check was not reset after check reset was issued.

Microdiagnostic
1. Load Routine A3
2. Enter 10, 08, 01, 00

R/W 282 ②

Scope Figure 2
Sweep 10 µs/div
Trigger
Slope (–)
Ch 1 Only
Ch 1 A1H2B10
–Sense Read Write
Volts/div 0.1
probe X10
Ch 2 A1H2S13
+Rd/Wr Status Bit 1
(Capable Enable Bit)
Volts/div 0.1
probe X10
Use R/W 213 to isolate

R/W 282 ①

Maintenance procedure complete

A

START 500

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

Figure 1

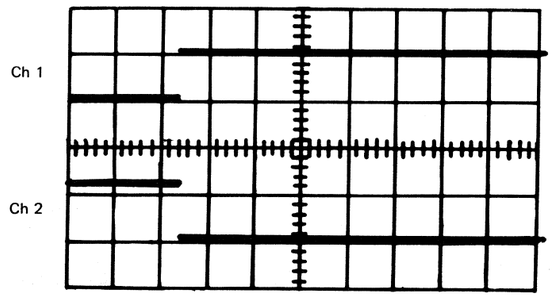
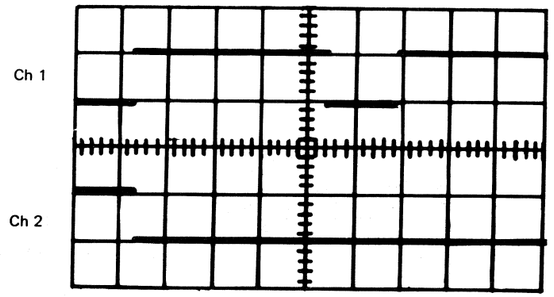
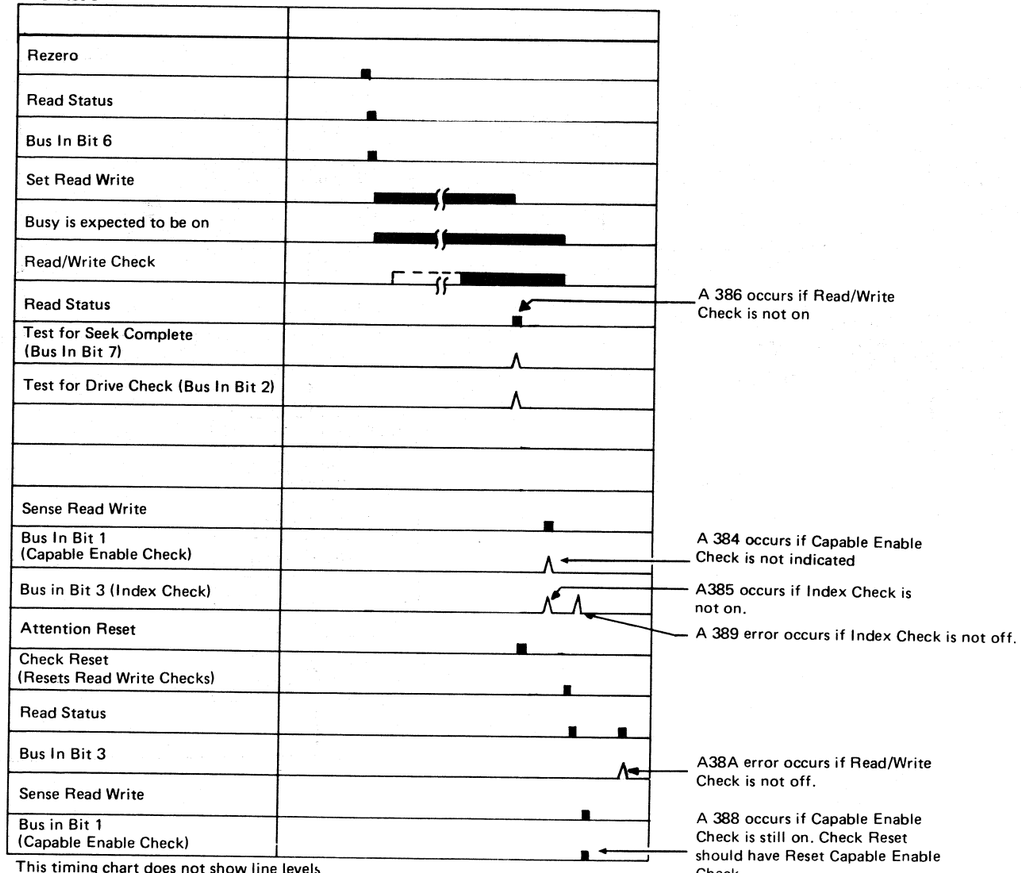


Figure 2



A3 Test 8



This timing chart does not show line levels and is intended for timing purposes only.

R/W 210 C

XX04 Error
No
Yes

Read Only lamp stays on.

Scope
Read Only lamp circuit on R/W 213.

⑩

Write Enable Problem

Microdiagnostic
1. Load routine B4.
2. Enter 10, 83, 10, 8F, 00, 00, 00, 00, 00, 00, 00, 00, 00, 00, 00, 00

Check status byte bit 4 on indicates if the data module is write enabled. It was not on at error stop.

Scope
Sweep 10 µs/div
Trigger
Slope (–)
Ch 1 only
Ch 1
A1M2(L2)G13
–Sense Status 1
Volts/div 0.1
probe X10
Ch 2
A1M2(L2)B12
+Sense 1 bit 4A
(Write Enabled Bit)

R/W 213 ⑧
R/W 213 ⑨

Maintenance procedure complete

A

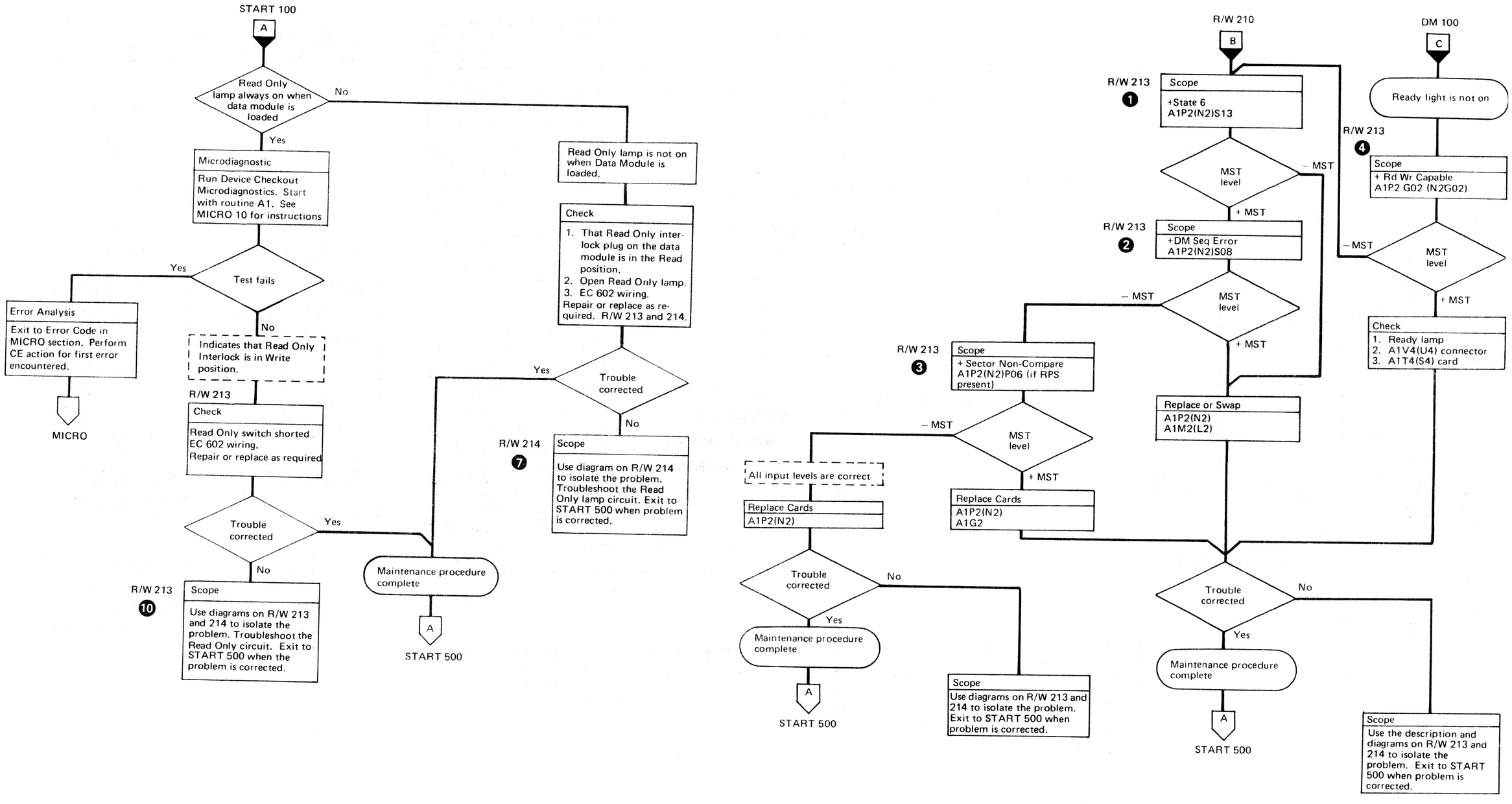
START 500

DG0040	2747709
Seq. 1 of 2	Part No. ( )

440203	440205	440209	440223			
2 Nov 73	28 Jan 74	25 Mar 74	14 Mar 75			

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CAPABLE ENABLE CHECK



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CAPABLE ENABLE CHECK

Actuated by Read Only Interlock plug in data module when plug is in write position.

Read Only Lamp (YA070)

Read Only Switch

EC602-H

EC602-C

+ 24 Vdc

EC602-G

Switch shown in unactuated (read only) position.

READ ONLY SW A YA070

NOTE *ENTR* A1V4 (A1U4) B02

A1M2 (A1L2)
KFxxx (KGxxx)

READ ONLY SW A — M10 CV A-A1M2 — READ ONLY ON AA

READ ONLY A AC AR A-A1M2 — P10 — KL030 — READ ONLY A — H R/W 214

-SENSE STATUS 1
+SELECTED A

ZG13 ZJ07 A OR U B12 — KK006 — +SENSE 1 BIT 4A — (WRITE ENABLE) — AP2

SENSE 1 BIT 4A AB A-A1M2

DM SEQ ERROR A AB

-STOP RECYCLE — N A-A1M2 — S09 — KH060 — +DM SEQ ERROR A

STATE 6 A AA

-STATE 6 — N A-A1M2 — G08 — KF100 — +STATE 6 A KH010

R/W 120 A

A1T4 (A1S4)
KPxxx (KQxxx)

+RD*WR CAPABLE A
SPECIAL GND G05

ZJ10 G05X A-A1T4 — FL AR-MD B08 — READY LAMP A — NOTE *EXIT* A1V5 (A1U5) AP D12 — -READY LAMP A — Ready Lamp (YA070) — EC602-C — + 24 Vdc

A1P2 (A1N2)
KHxxx (KJxxx)

DATA MODULE READY AB

+STATE 6 A — ZS13 — N A-A1P2

TRACK F OLLOWING TIMER AA

+ TRK FOLLOWING TIMER A — ZG03 — N A-A1P2

+DM SEQ ERROR A — S08 — OR XLLDD A-A1P2 AZ

RPI 505 (506) A — +SECTOR NON-COMPARE — P06 — OR

AY A XLLDD KA-A1P2 — G02 — KL050 — +RD*WR CAPABLE A KP010 — G R/W 214

-DATA MODULE READY KH040 KH050 KH070 — AT2

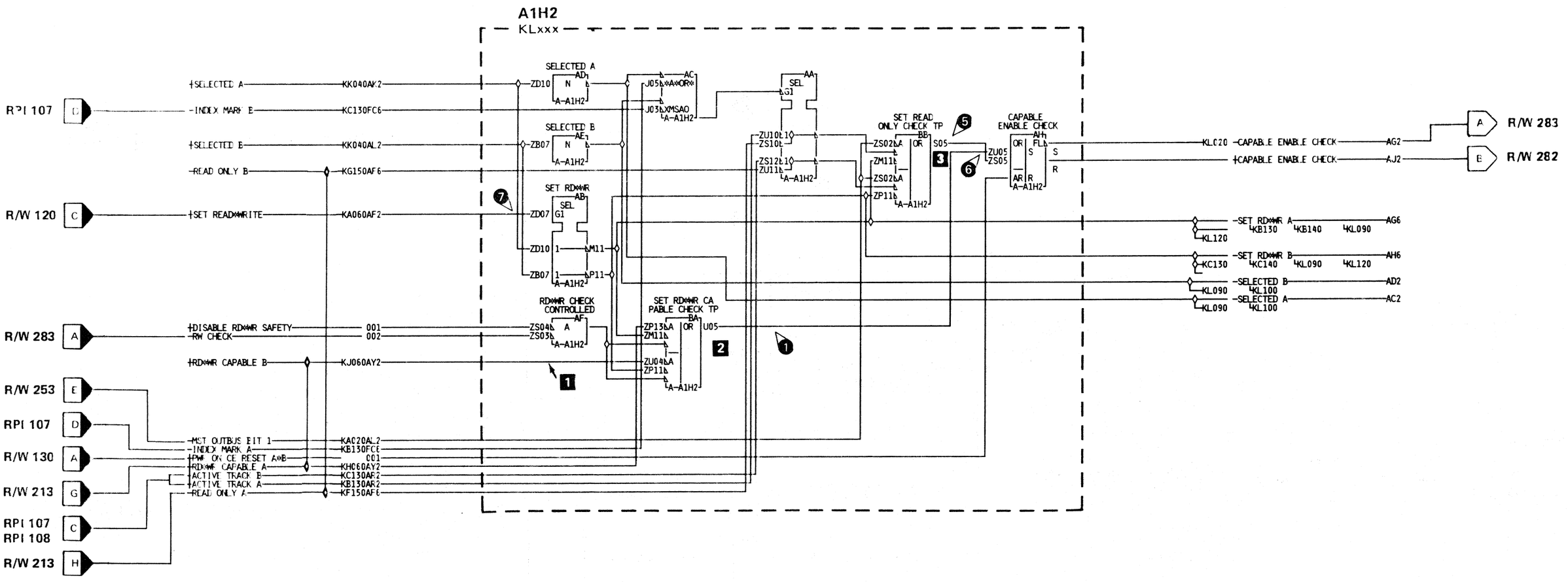
-TRACK FOLLOWING TIMER KH020 KH070 — AJ2

DG0050	2747710
Seq. 1 of 2	Part No.( )

440203	440205	440209	440218	440223	
2 Nov 73	28 Jan 74	25 Mar 74	5 Aug 74	14 Mar 75	

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CAPABLE ENABLE CHECK



Capable Enable Check Conditions

If A1H2S05 **3** ever goes +MST, it indicates that during a Write operation (set read*write active and MST outbus bit 1 active) Active Track was not active. (See RPI 100 for a description of Active Track.)

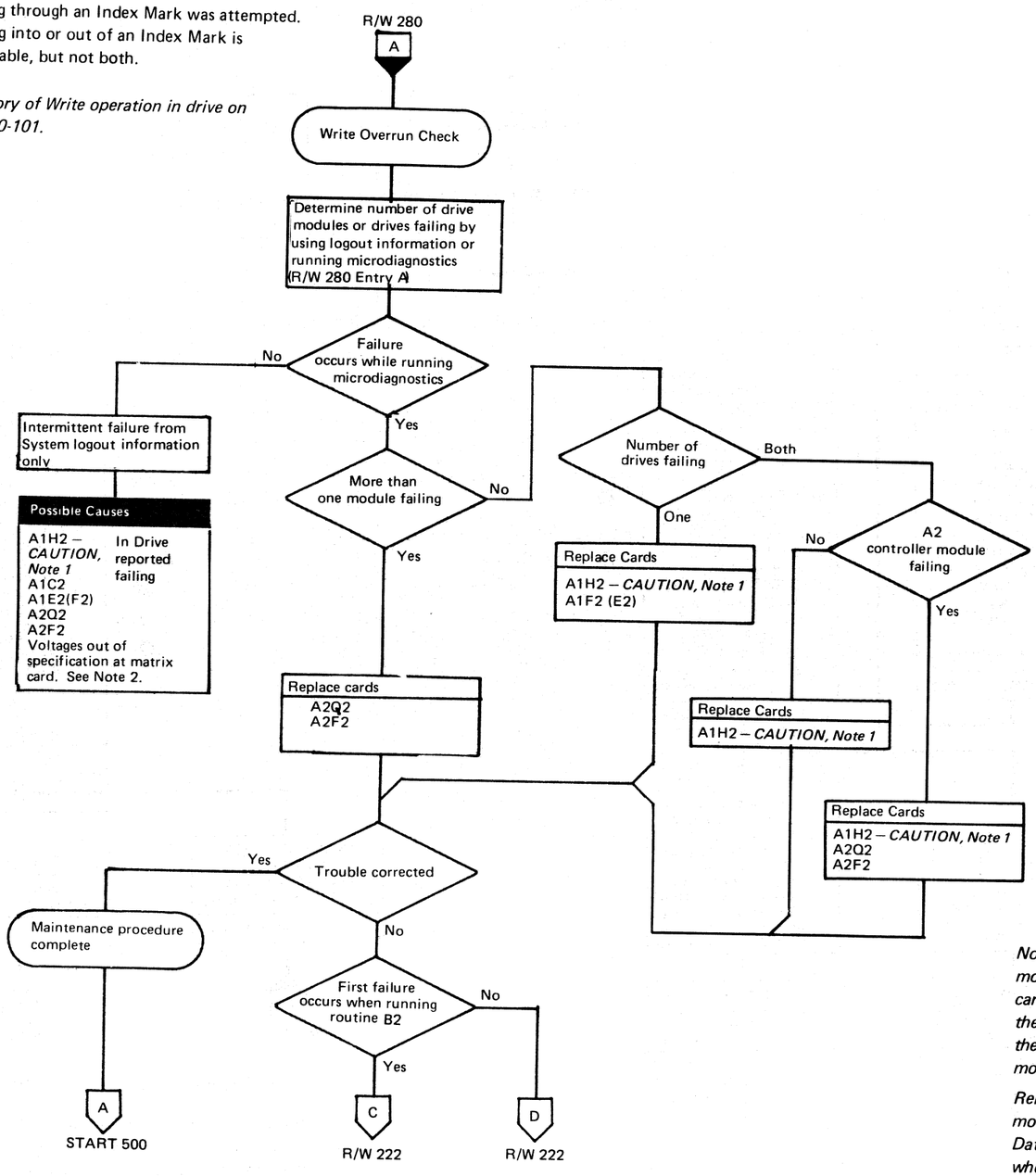
If A1H2U05 **2** goes +MST the indication is that during a read or write operation the drive was not capable. **1**

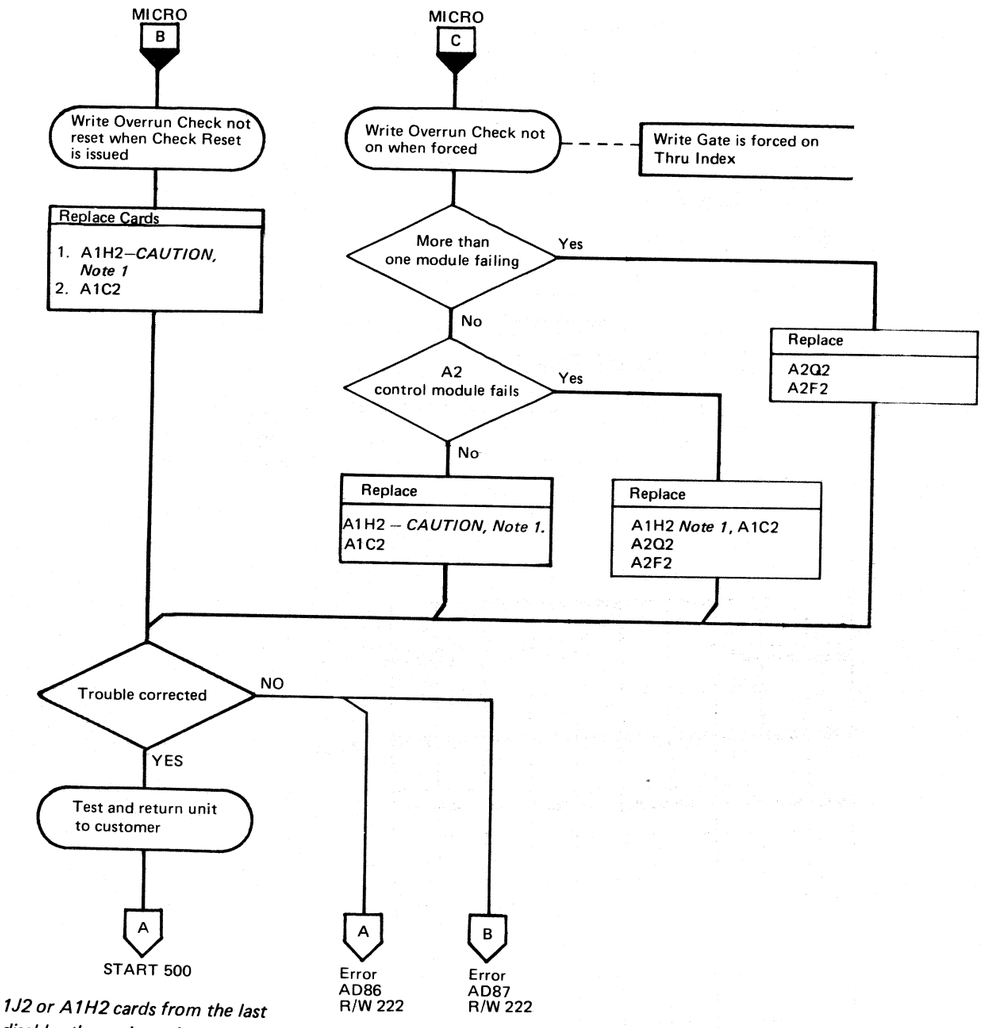
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WRITE OVERRUN CHECK

The Write Overrun Check indicates that writing through an Index Mark was attempted. Writing into or out of an Index Mark is acceptable, but not both.

See theory of Write operation in drive on R/W 100-101.





Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: −4 Vdc (−3.84 V to −4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin. If the fixed head feature is installed, make sure that the 6 V jumper is also plugged to A1K1B13.

If either of these voltages is not as specified, go to PWR 10, Entry C.

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WRITE OVERRUN CHECK

MST Outbus bit 1 controls Write Gate when Set Read/Write is active (both under controller Set Read/Write controls). If Write Gate is active through an Index Mark, Write Overrun is indicated and Read/Write Check is set on. A subsequent Sense Read/Write command indicates Write Overrun Check if Bus In bit 2 is on. Check Reset resets all Read/Write Checks. The timing chart in Figure 1 represents proper operation.

See theory of Write operation in drive on R/W 100-101.

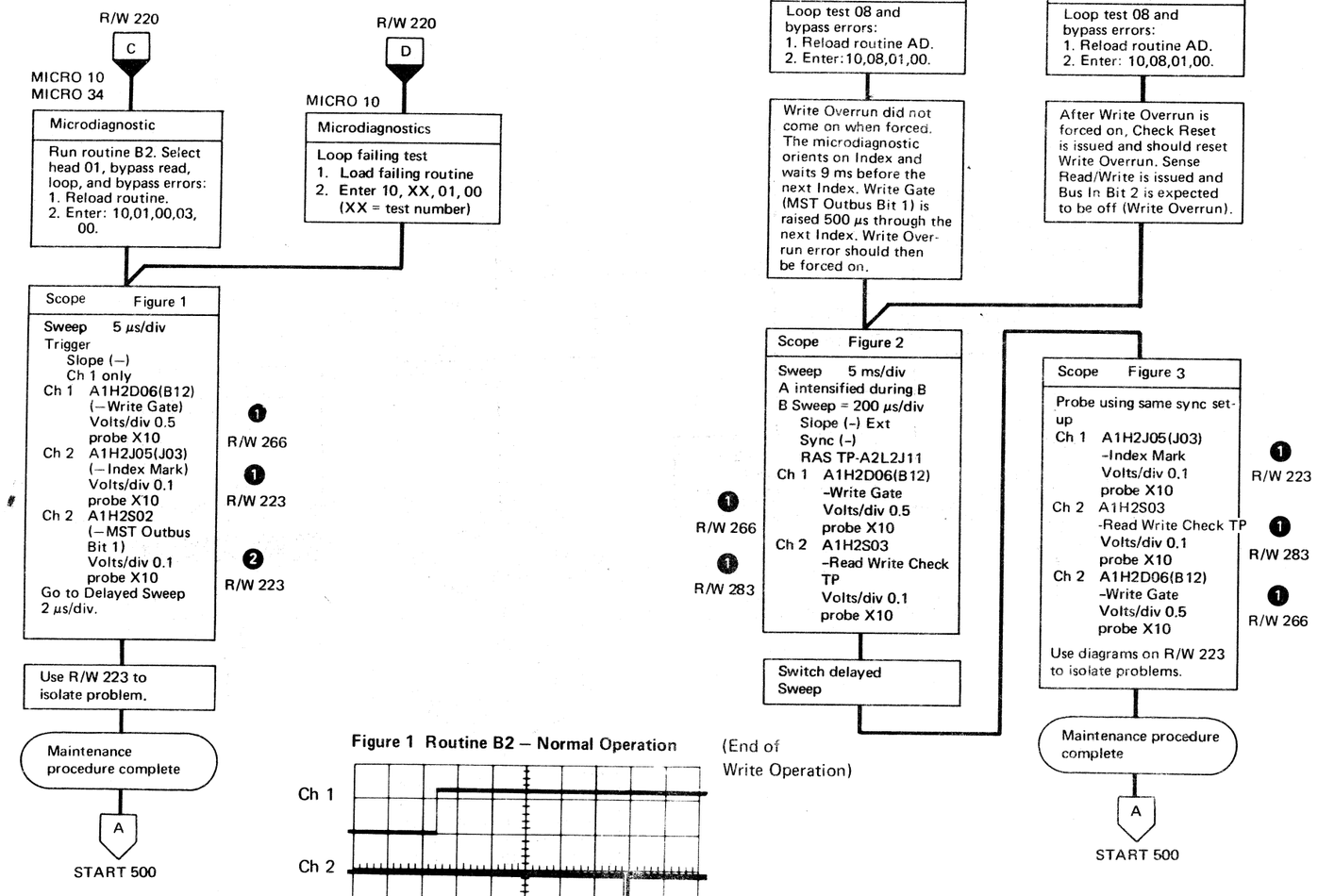
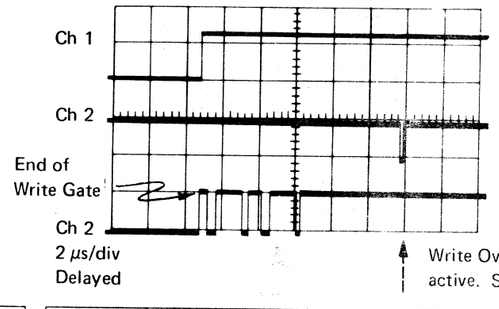


Figure 1 Routine B2 – Normal Operation (End of Write Operation)



Write Overrun occurs if Write Gate is still active. See R/W 223 to isolate the problem.

Figure 2 – Forced Write Overrun 5 ms/div

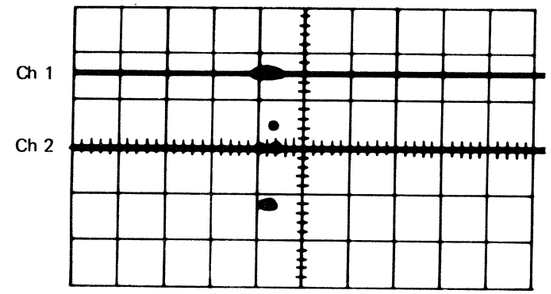
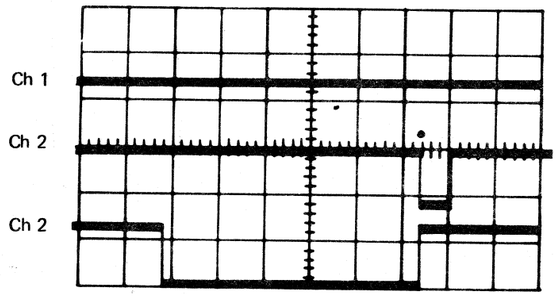
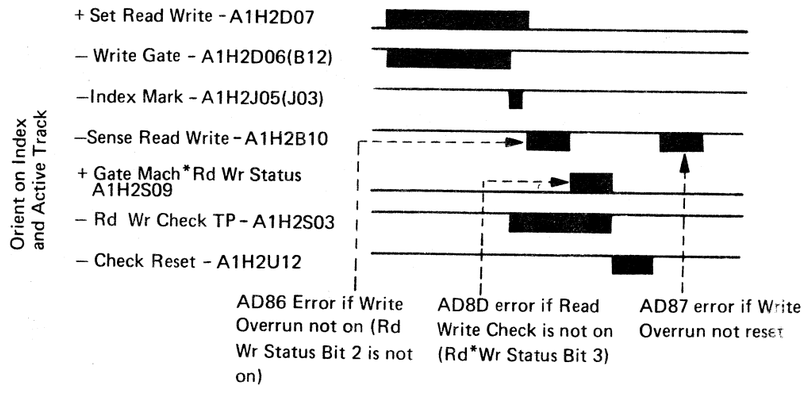


Figure 3 – Delayed Sweep B 200 µs/div

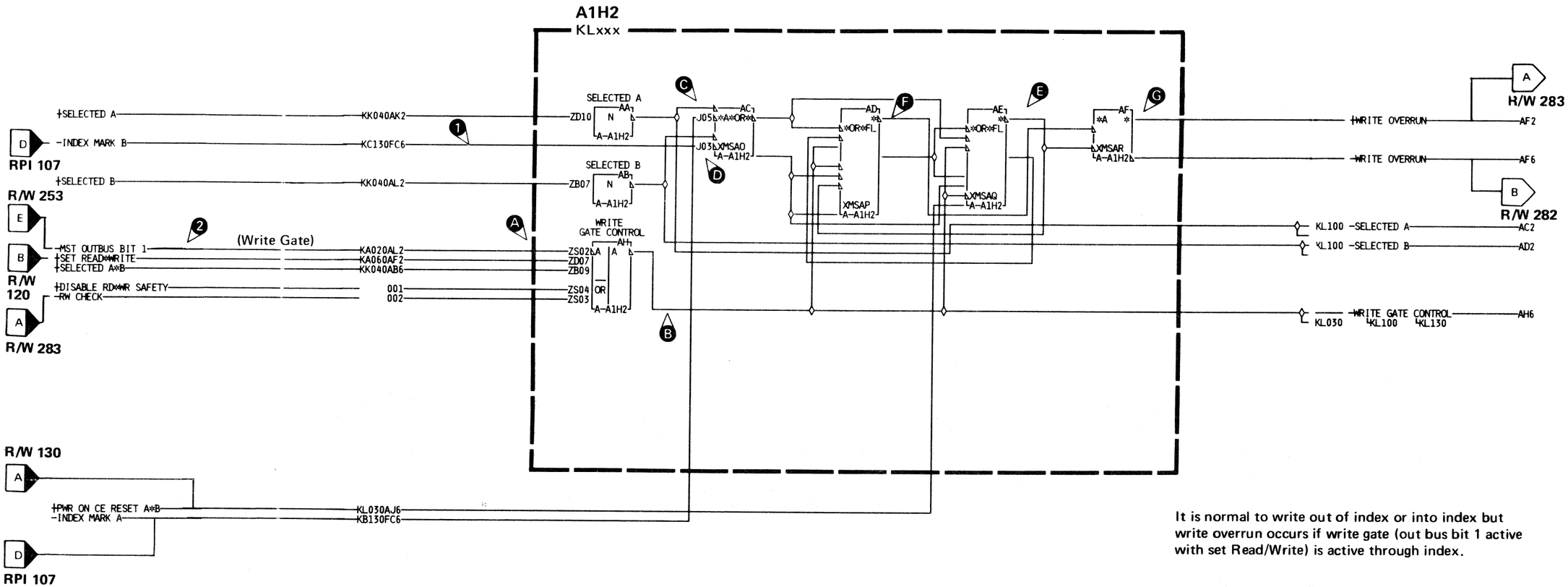


AD86
AD87
AD8D **FORCED WRITE OVERRUN - See Figures 2 and 3**

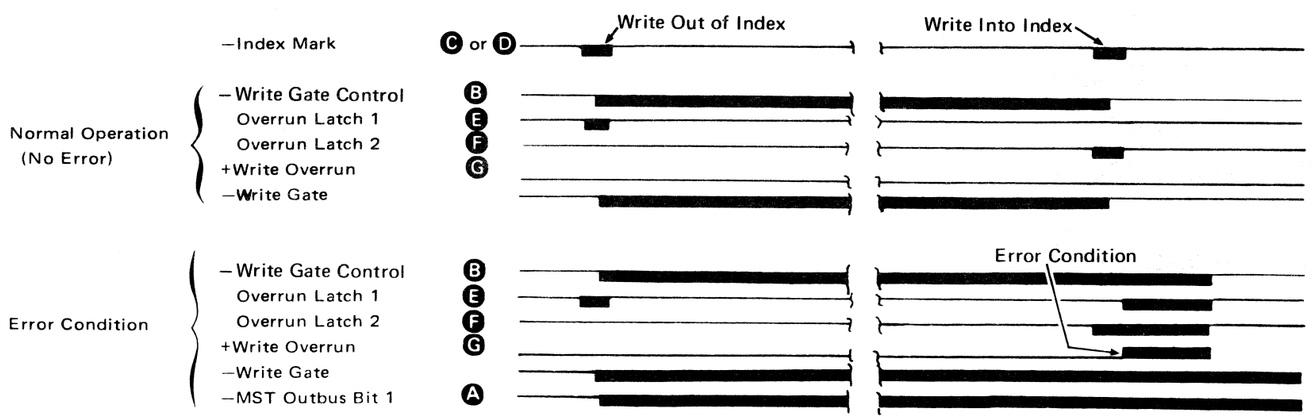


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WRITE OVERRUN CHECK



It is normal to write out of index or into index but write overrun occurs if write gate (out bus bit 1 active with set Read/Write) is active through index.



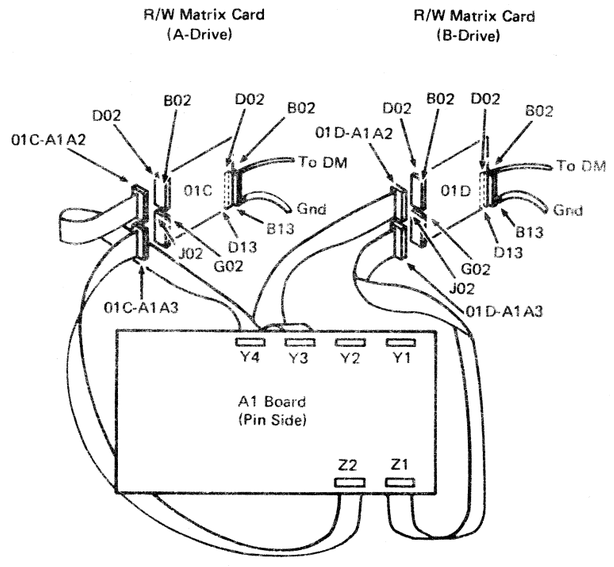
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READ/WRITE INTERLOCK CHECK

The read/write interlock check indicates that read/write cards, cables, or connectors are loose or missing.

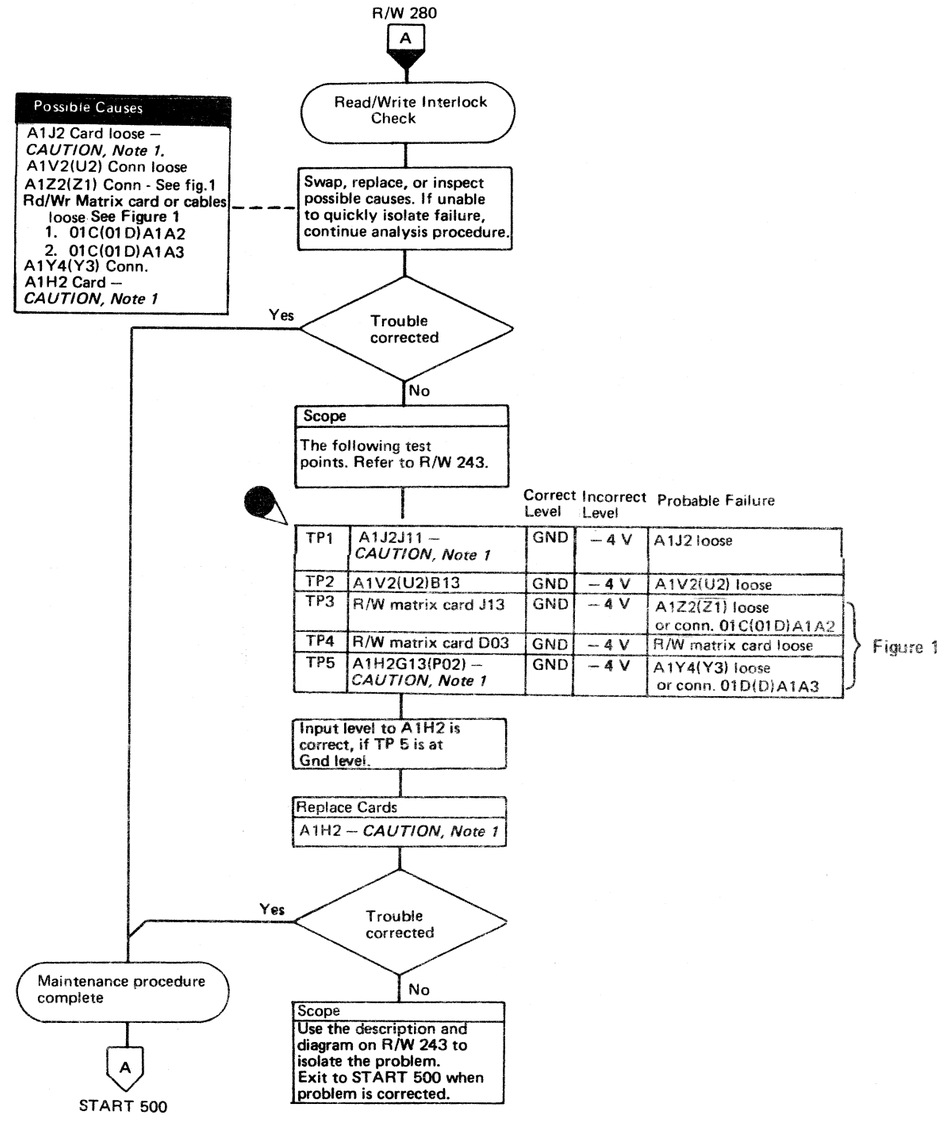
See theory of Write operation in drive on R/W 100-101.

Figure 1



Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

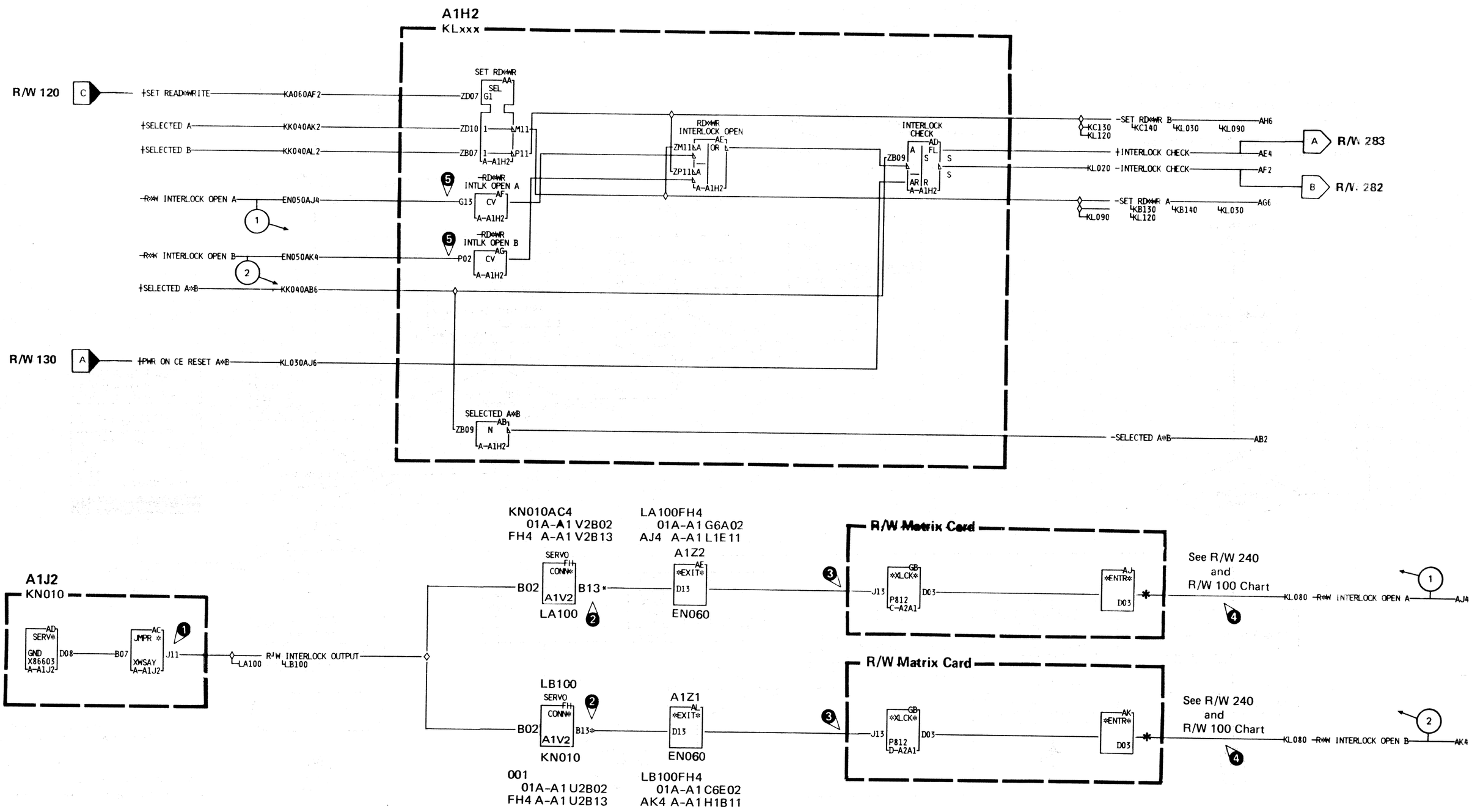
Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.



DG0070 Seq. 2 of 2	2747712 Part No. ( )

440203 2 Nov 72	440205 28 Jan 74	440209 25 Mar 74	440218 5 Aug 74	440223 14 Mar 75		

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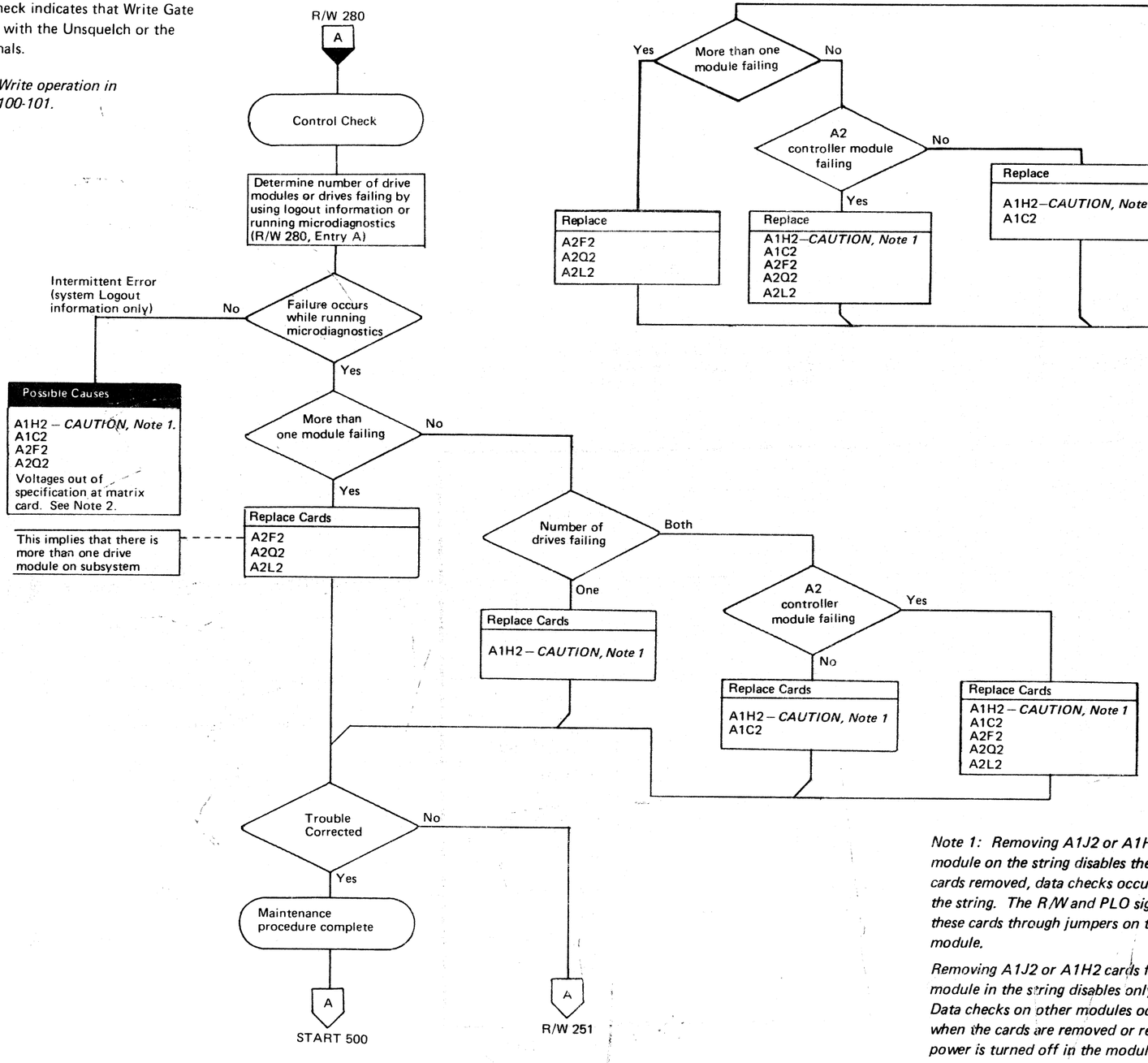


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CONTROL CHECK

The control check indicates that Write Gate signal is active with the Unsquelch or the Read Gate signals.

See theory of Write operation in drive on R/W 100-101.



Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: –4 Vdc (–3.84 V to –4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin.

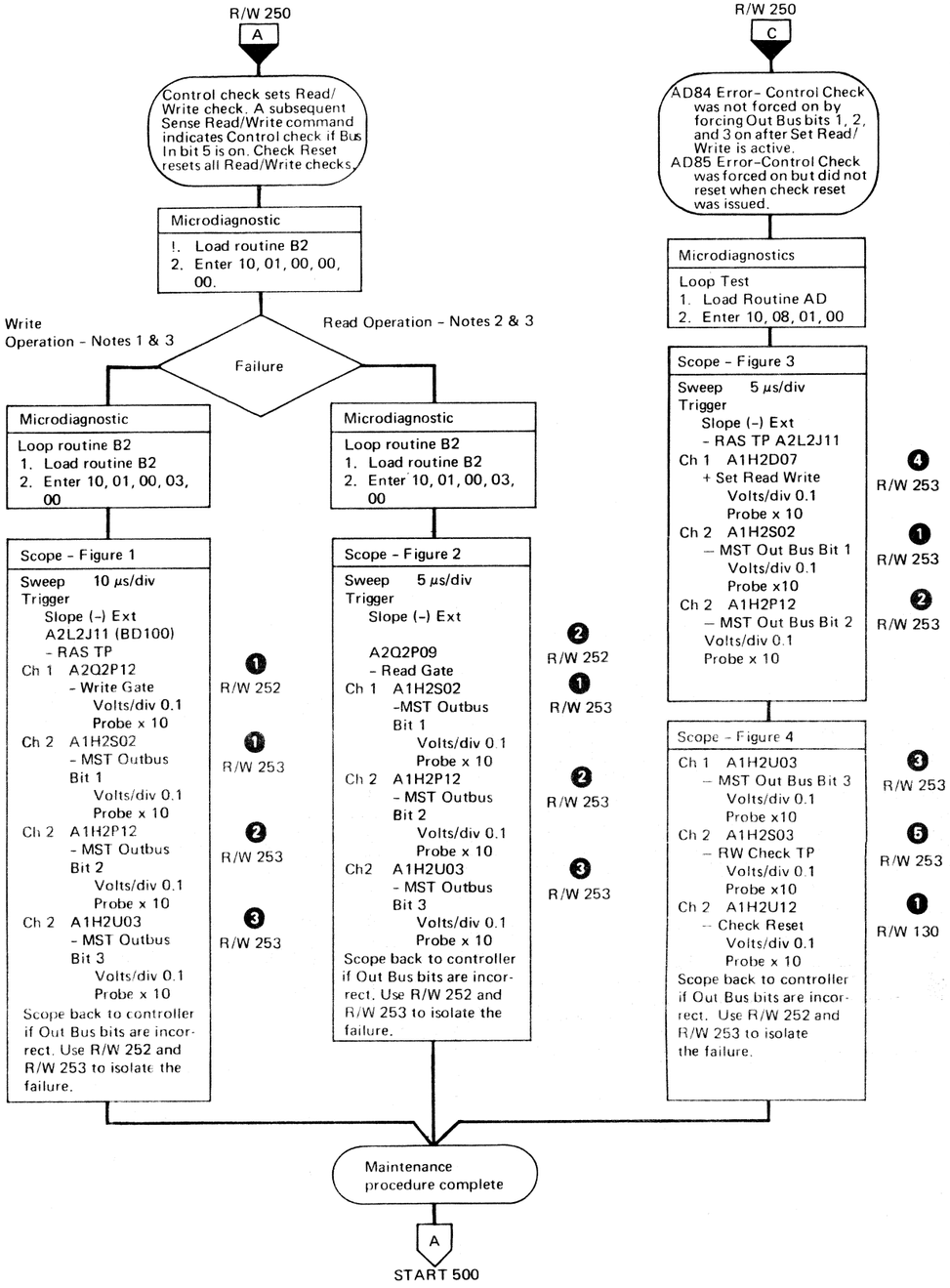
If either of these voltages is not as specified, go to PWR 10, Entry C.

DG0080 Seq. 2 of 2	2747713 Part No. ( )

440203	440205	440209	440218	440223		
2 Nov 73	28 Jan 74	25 Mar 74	5 Aug 74	14 Mar 75		

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CONTROL CHECK



NOTE 1: Write Operation – Control Check occurs if MST Out Bus bits 1 and 3 are on when Set Rd/Wr is active or if Out Bus bits 1 and 2 are active.

NOTE 2: Read Operation – Control Check occurs if MST Out Bus bits 1 and 3 are on when Set Rd/Wr is active.

Figure 1 - Write Operation

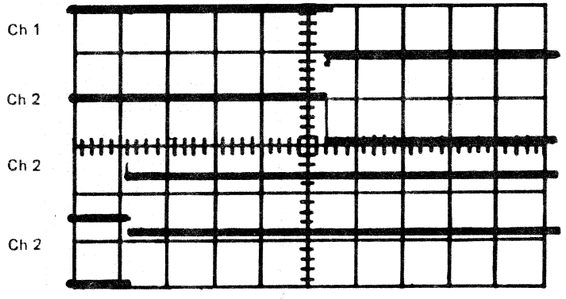
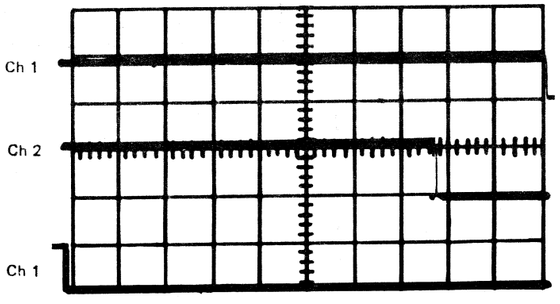


Figure 2 - Read Operation



AD84
AD85
AD8C

Forced Control Check - See Figure 3

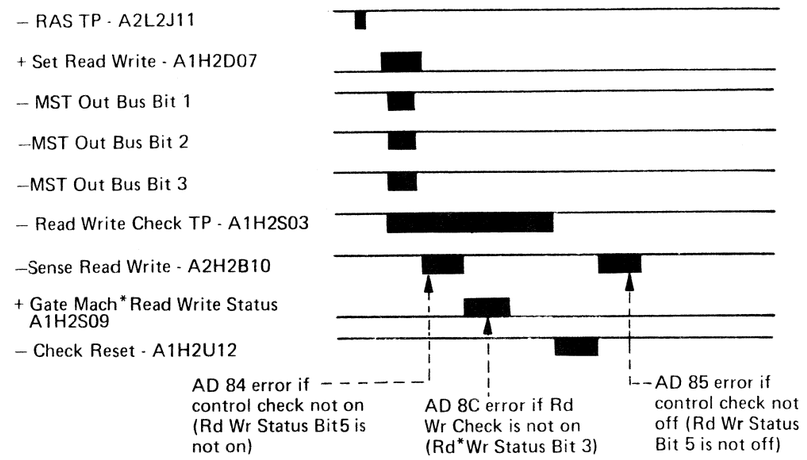


Figure 3 - Force Control Check

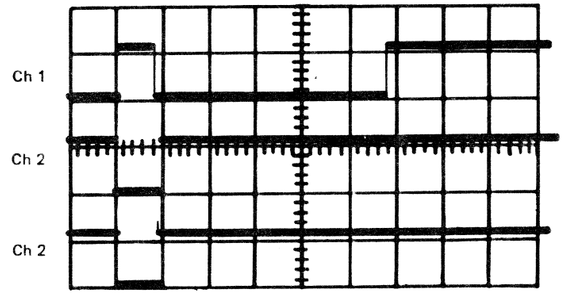
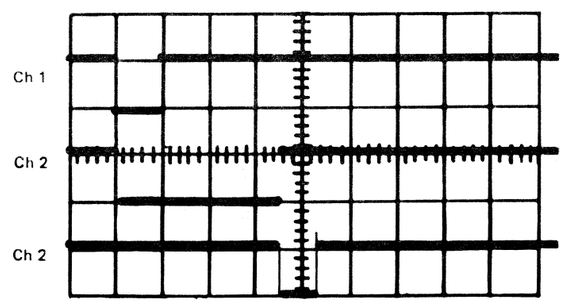
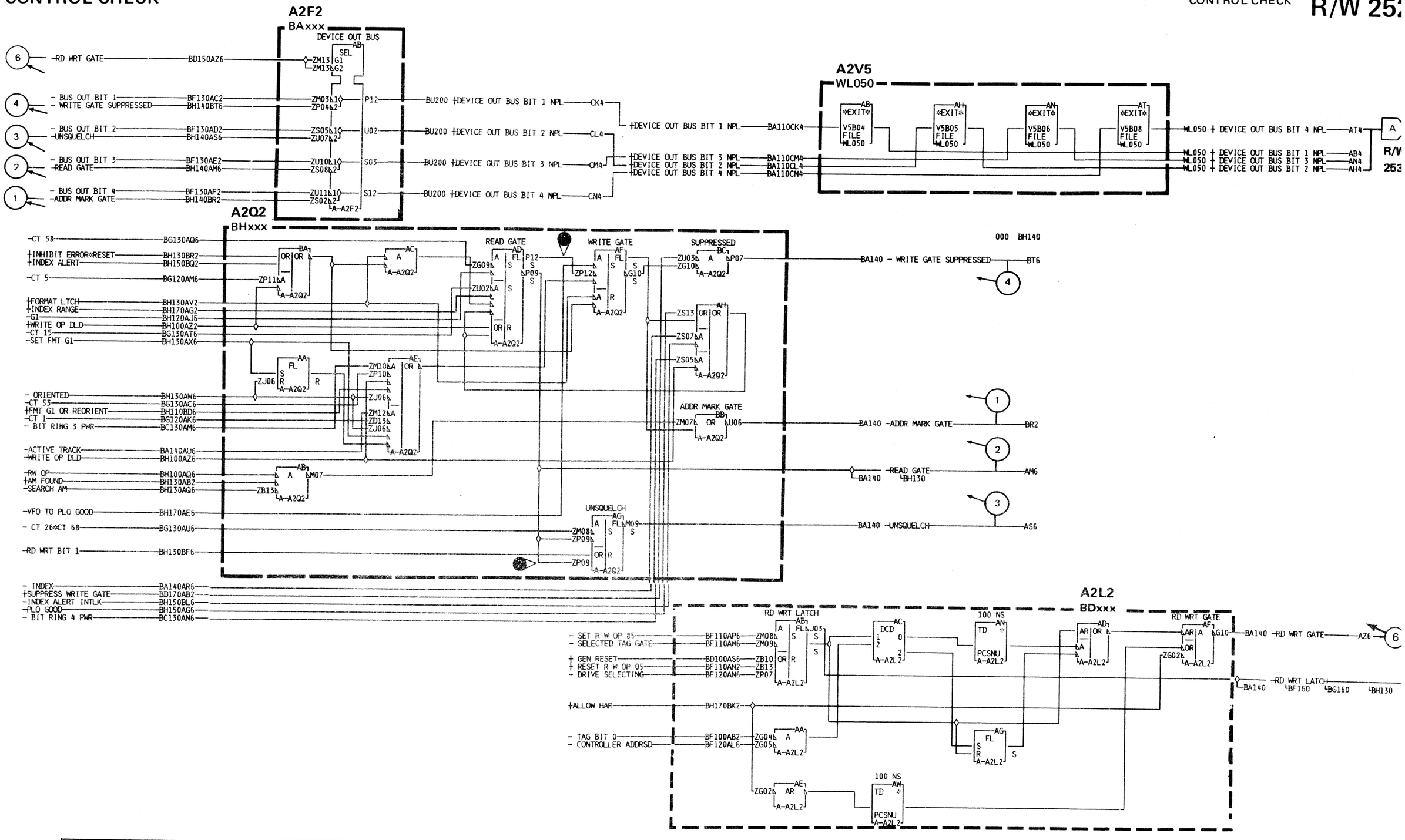


Figure 4 - Forced Control Check-Delayed



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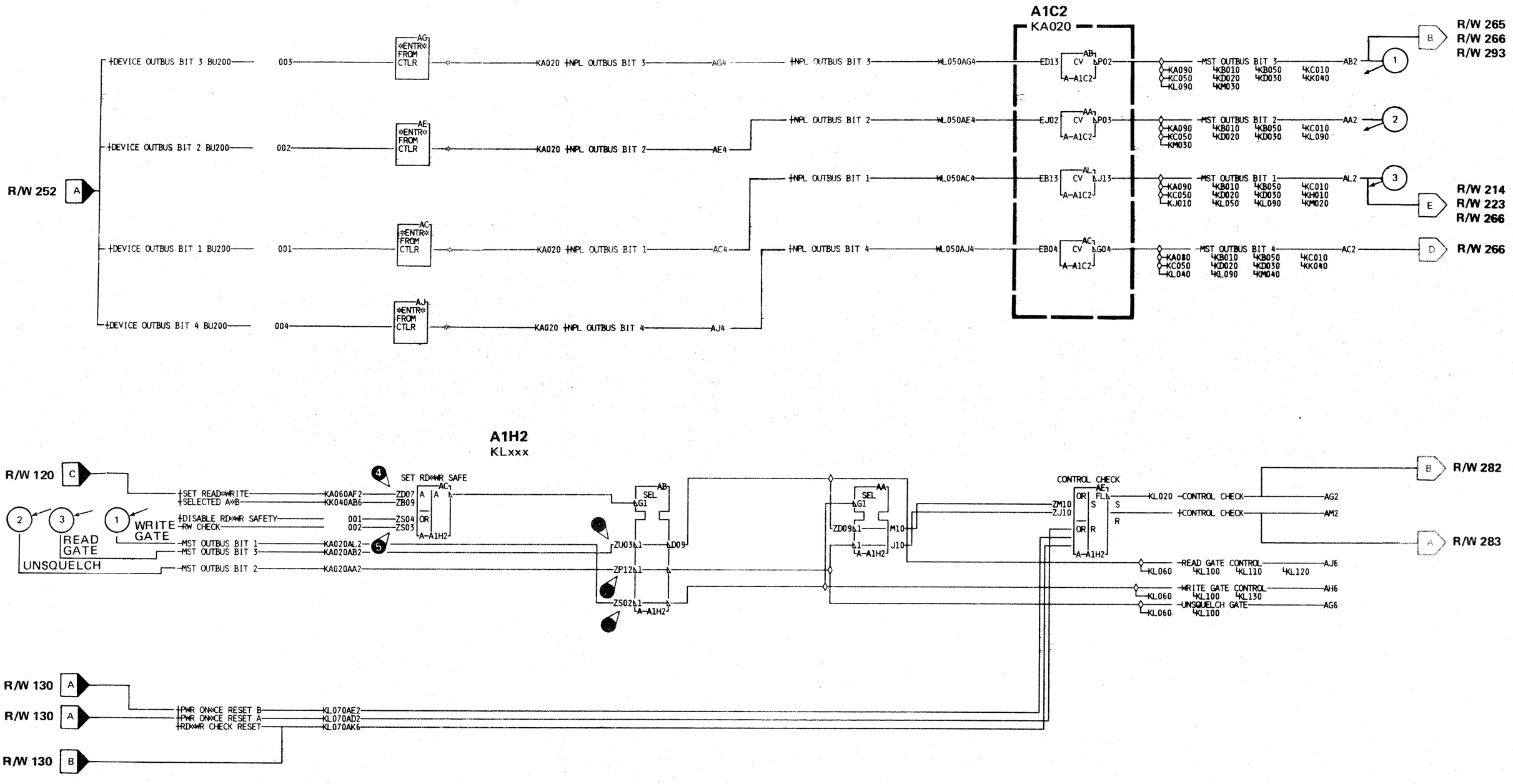
CONTROL CHECK



DG0090	2747714
Seq. 2 of 2	Part No.( )

440203	440205	440209				
2 Nov 73	28 Jan 74	25 Mar 74				

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WRITE TRANSITION CHECK

A Write Transition Check occurs:

- If Write transitions are not detected 4 μs (nominal) after Write Gate is turned on.
- If Write transitions are not present when Write Gate is turned off.
- If Write transitions are detected while reading.

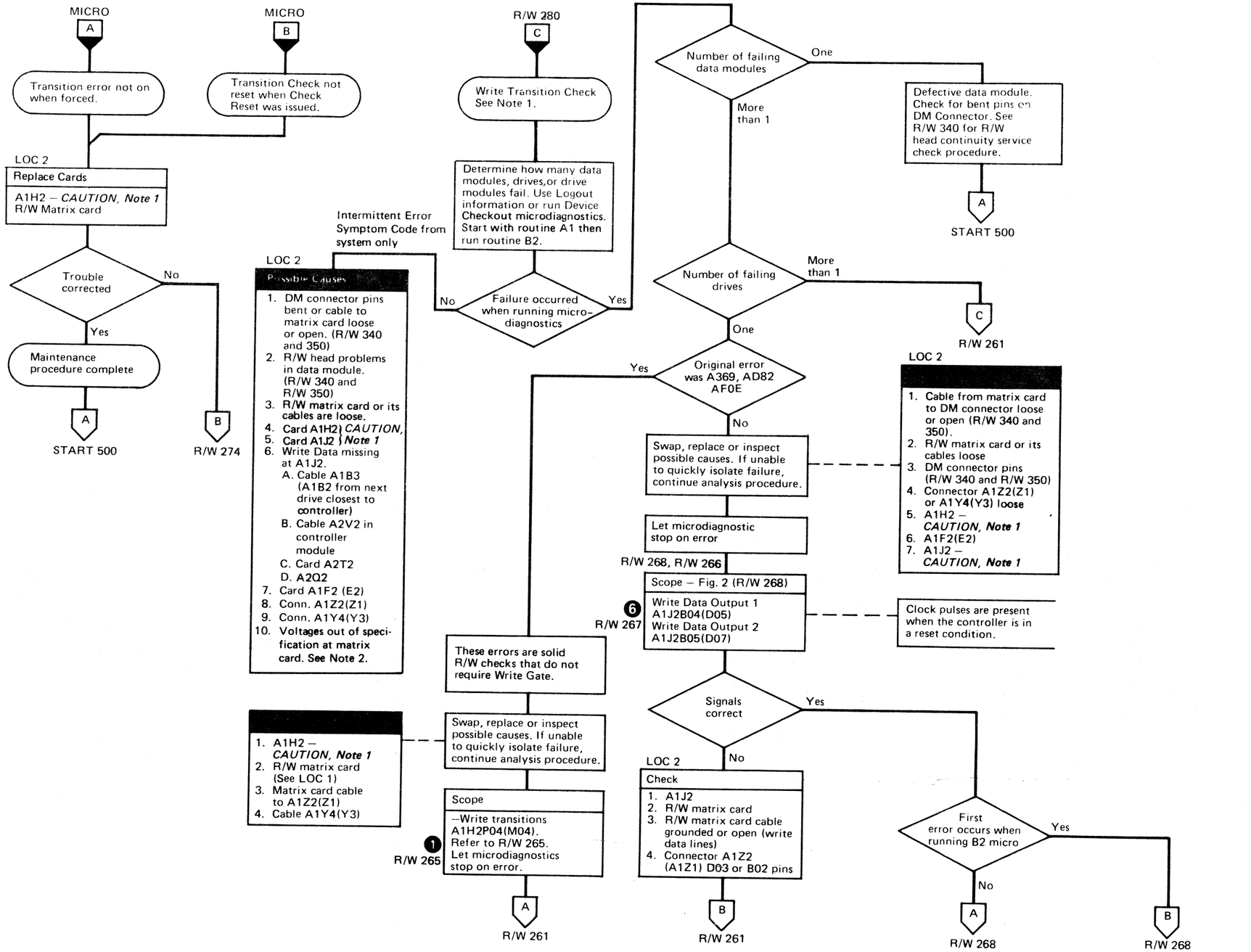
For theory of Write operation in the drive, see R/W 100.

Note 1: R/W and PLO signals are terminated by resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removal of the A1J2 or A1H2 cards in the last module causes R/W failures in other modules. As a precaution to prevent data checks, the customer should be prevented from using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module. See INST 10 for termination instructions.

Note 2: −4 Vdc (−3.84 V to −4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin. If the fixed head feature is installed, make sure that the 6 V jumper is also plugged to A1K1B13.

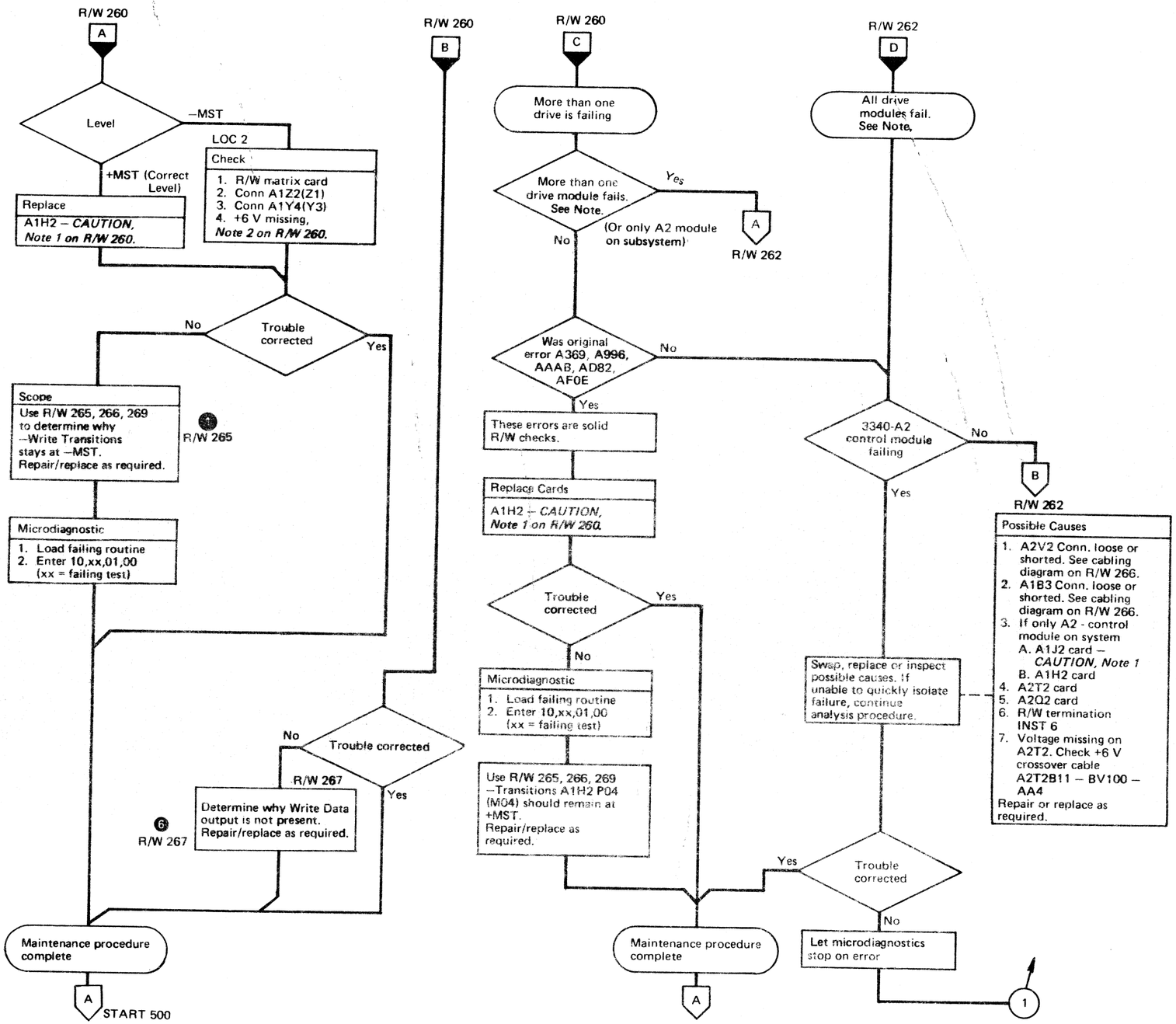
If either of these voltages is not as specified, go to PWR 10, Entry C.

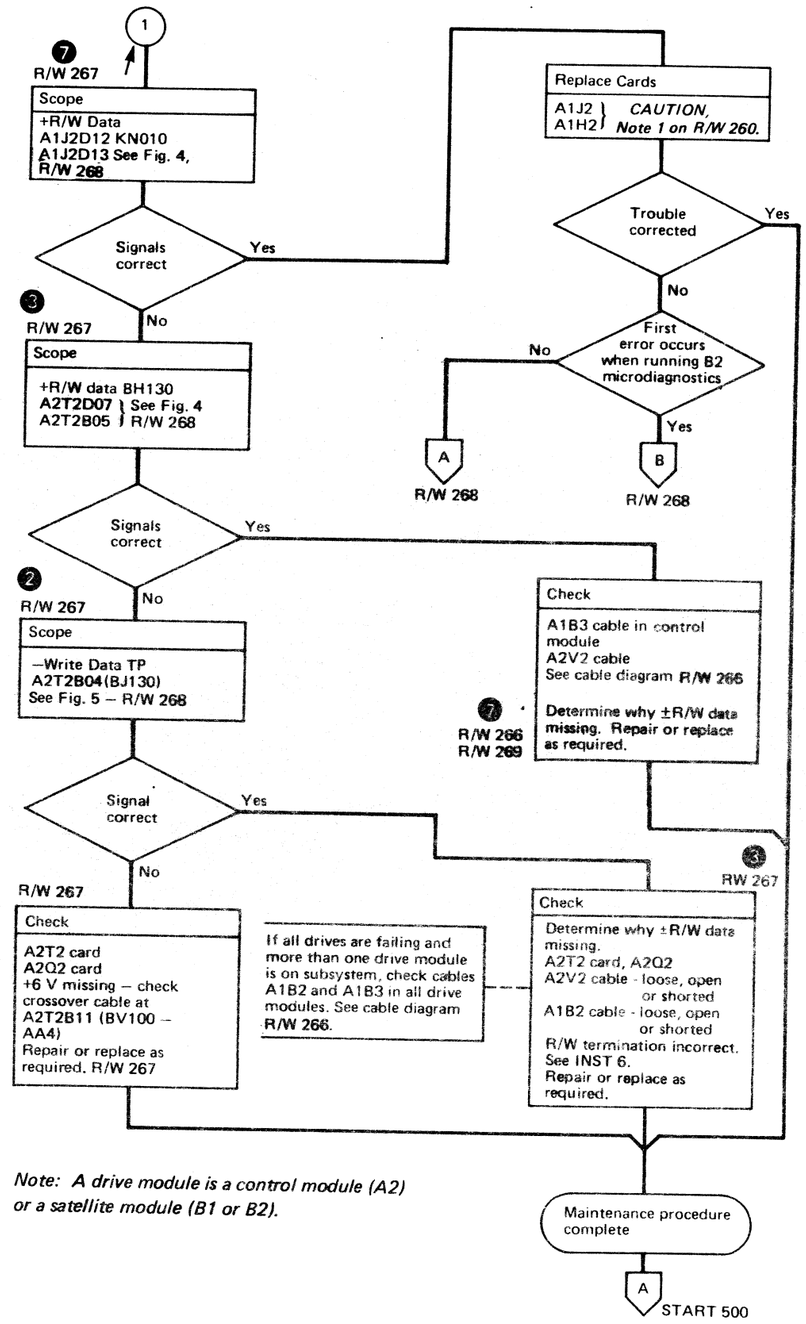


DG0110 Seq. 1 of 2	2747716 Part No. ( )	440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440214 17 Jun 74	440218 5 Aug 74	440223 14 Mar 75	

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WRITE TRANSITION CHECK

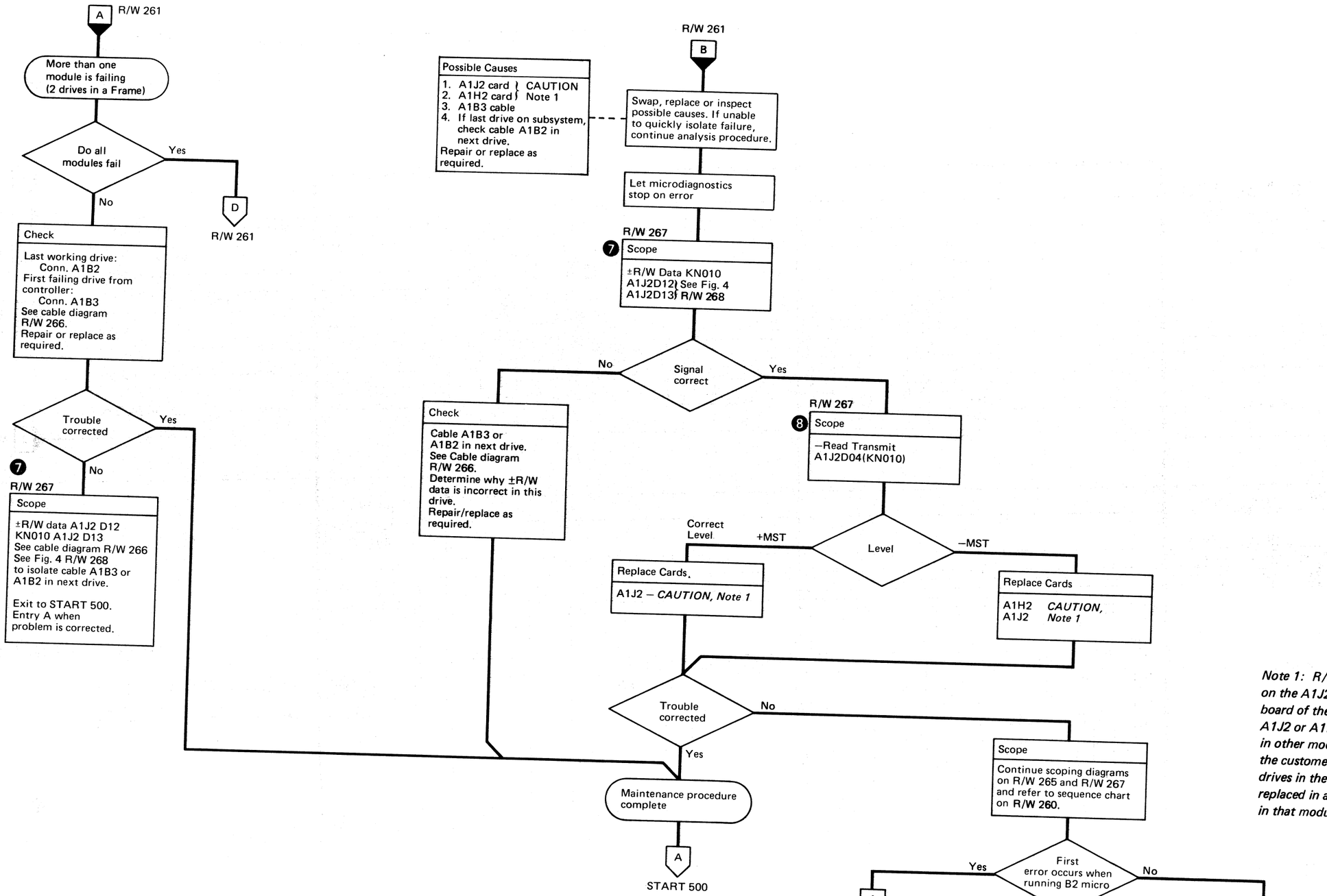




Note: A drive module is a control module (A2) or a satellite module (B1 or B2).

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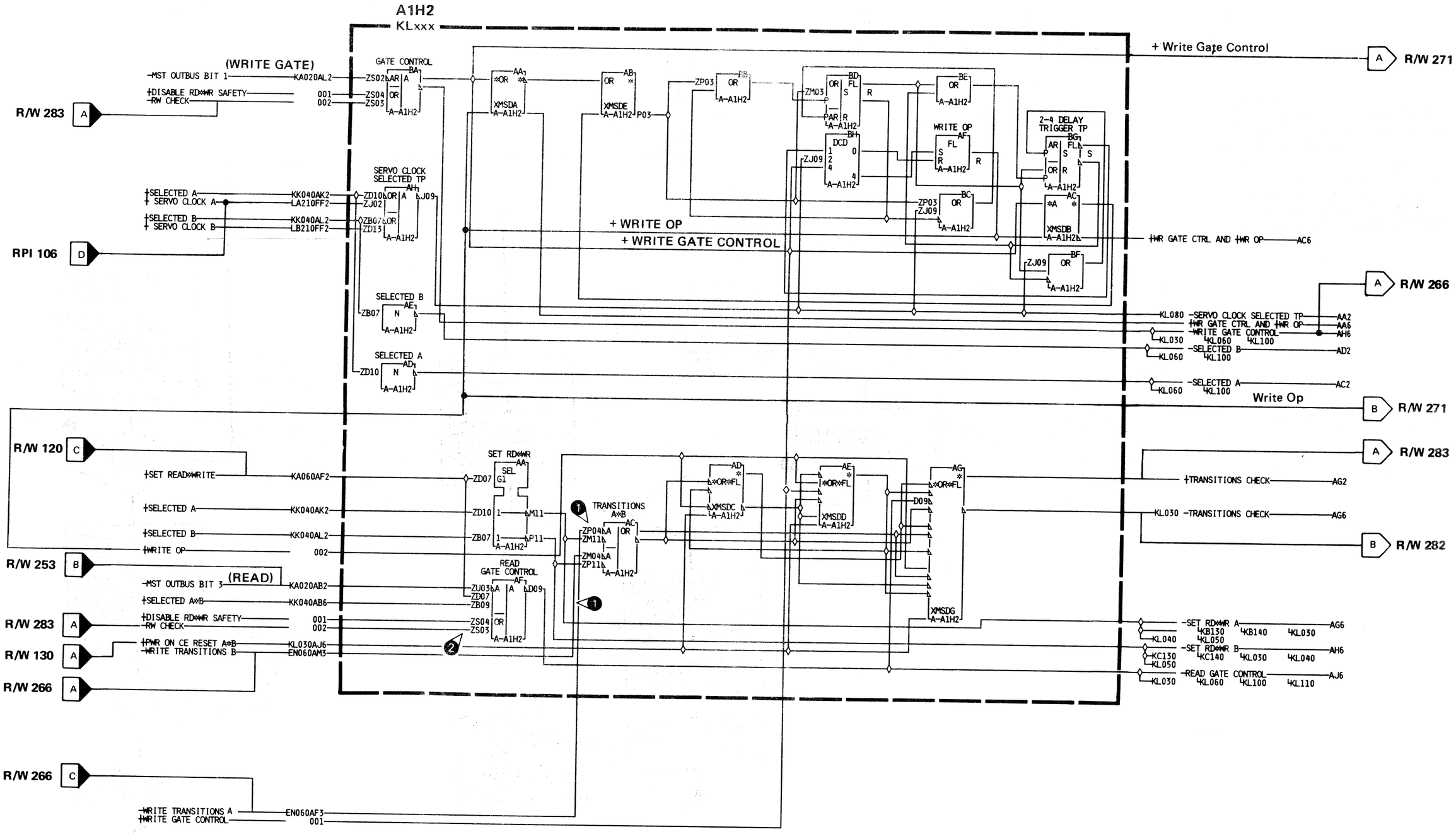
WRITE TRANSITION CHECK



Note 1: R/W and PLO signals are terminated by resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removal of the A1J2 or A1H2 cards in the last module causes R/W failures in other modules. As a precaution to prevent data checks, the customer should be prevented from using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module.

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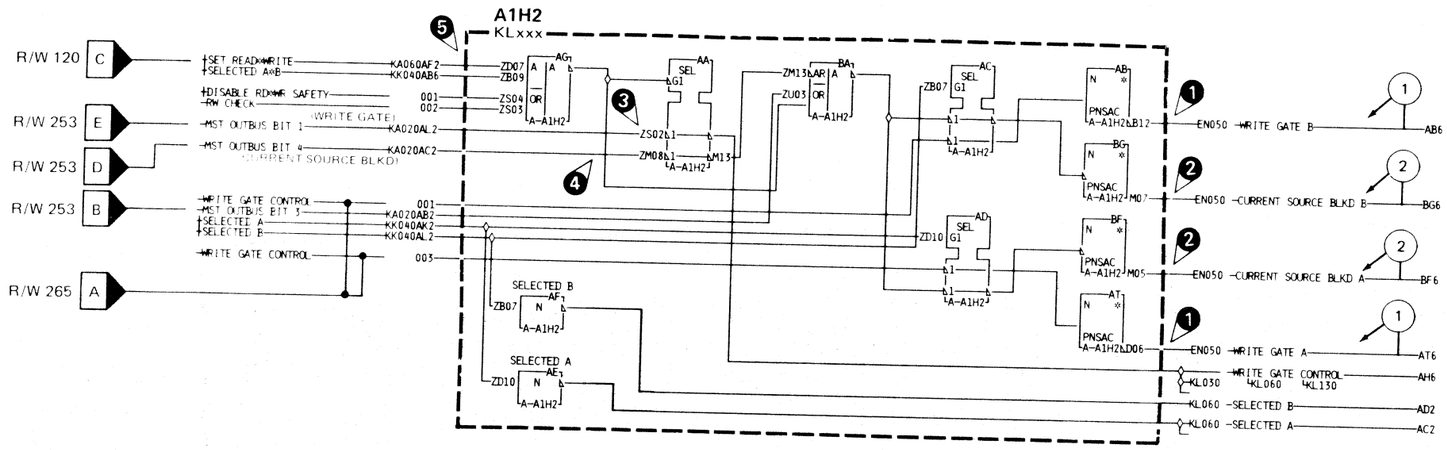
WRITE TRANSITION CHECK

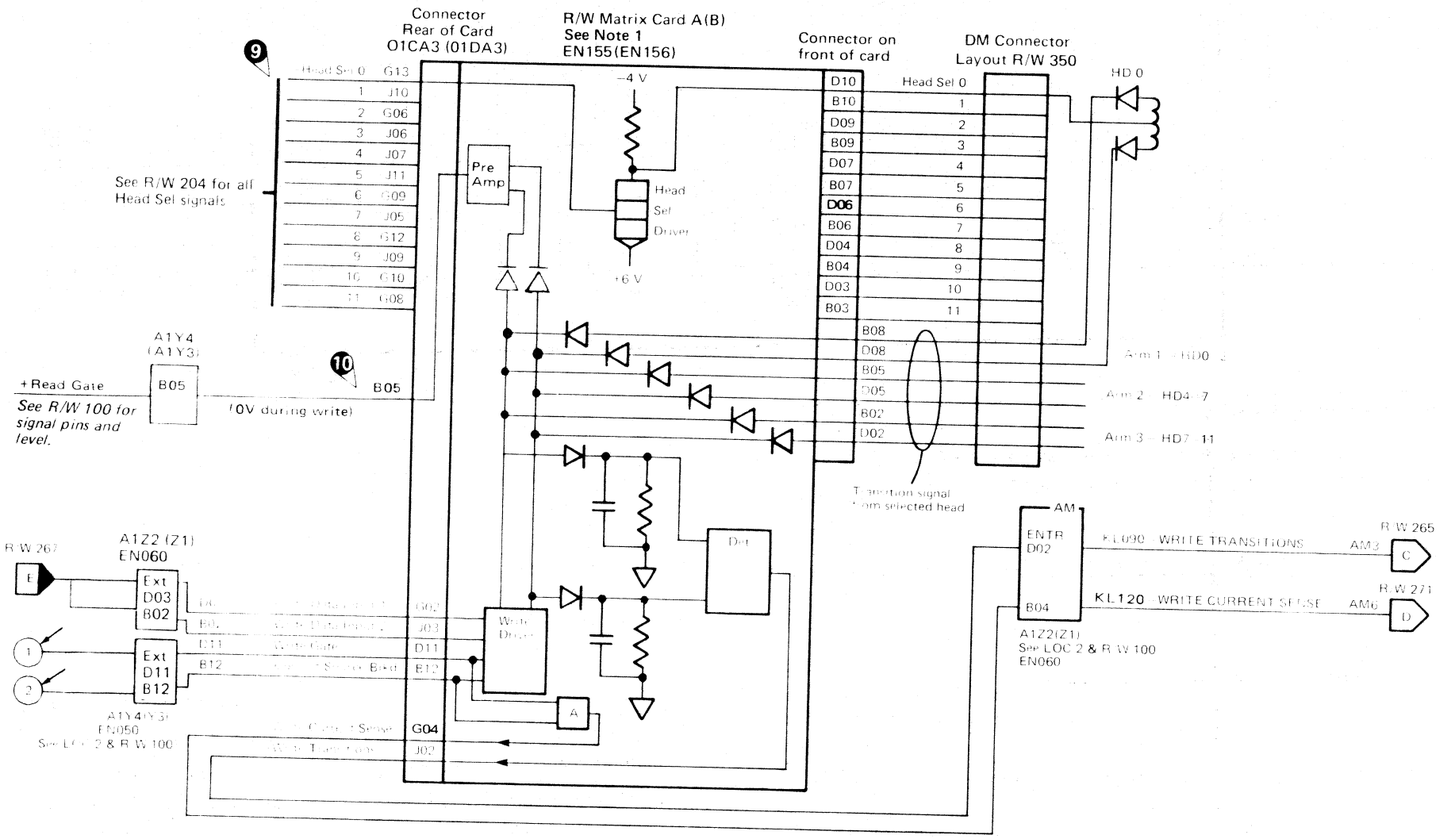


3340	DG0120 Seq. 2 of 2	2747717 Part No.( )	440203 2 Nov 73	440209 25 Mar 74	440223 14 Mar 74			

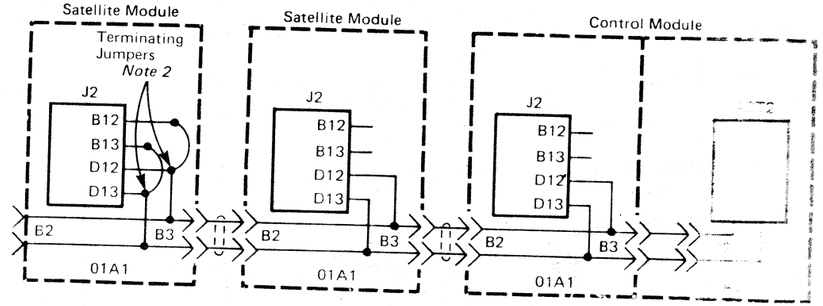
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WRITE TRANSITION CHECK





Write Data Flow



Note 1: See R/W 269 for description of R/W Matrix card. See R/W 100 for chart of signals to and from A1Z2 card.

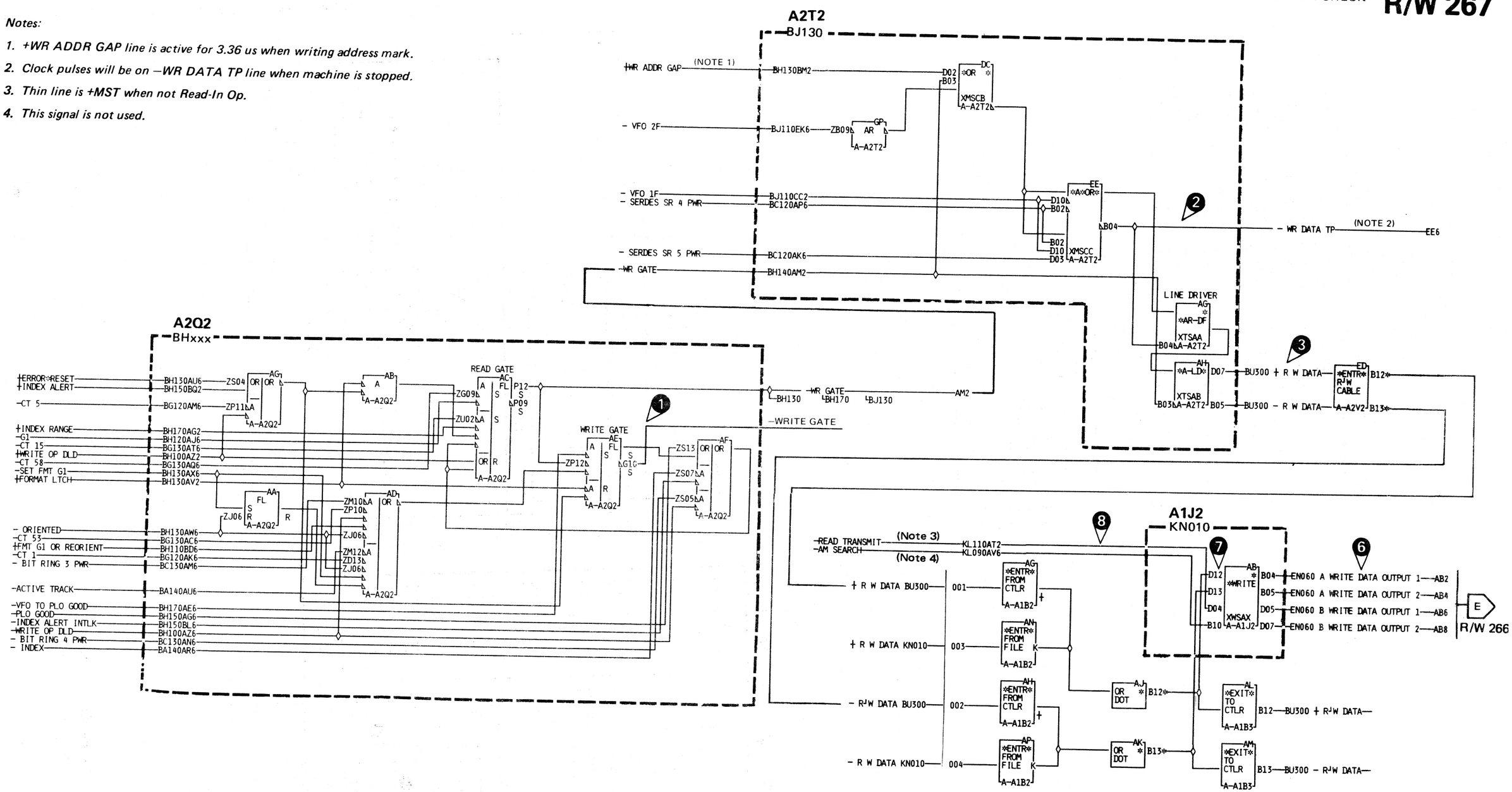
Note 2: R/W and PLO signals are terminated in resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removing the A1J2 or A1H2 cards in the last module causes failures in other modules. As a precaution to data checks, the customer should be prevented using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module. See INST 10 for operating instructions.

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WRITE TRANSITION CHECK

Notes:

1. *+WR ADDR GAP line is active for 3.36 us when writing address mark.*
2. *Clock pulses will be on –WR DATA TP line when machine is stopped.*
3. *Thin line is +MST when not Read-In Op.*
4. *This signal is not used.*



DG0130 Seq. 2 of 2	2747718 Part No.( )

440203 2 Nov 73	440209 25 Mar 74	440223 14 Mar 75				

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WRITE TRANSITION CHECK

Write Transitions are checked at the beginning and end of each Write operation. The checking is delayed from two to four servo clock times after writing begins and is checked after the writing stops. In order for transitions to occur, the following controls are necessary:

1. Write Gate active.
2. Current Source Blocked inactive.
3. Correct Write head operation.
4. Write Data must be present to Rd/Wr Matrix card.
5. Set Read/Write Safe must be active (No Read/Write checks).

If a transition check is detected, the transition latch is turned on, Read/Write Check is set, and Set Read/Write Gate. is turned off. This degates the Head Select lines and the Write Gate.

If transitions are detected during a Read operation, Transition Error and Read/Write Check are posted. A subsequent Sense Read Write command indicates a Transition error on Bus In bit 6.

See R/W 269 for description of Write Transitions.

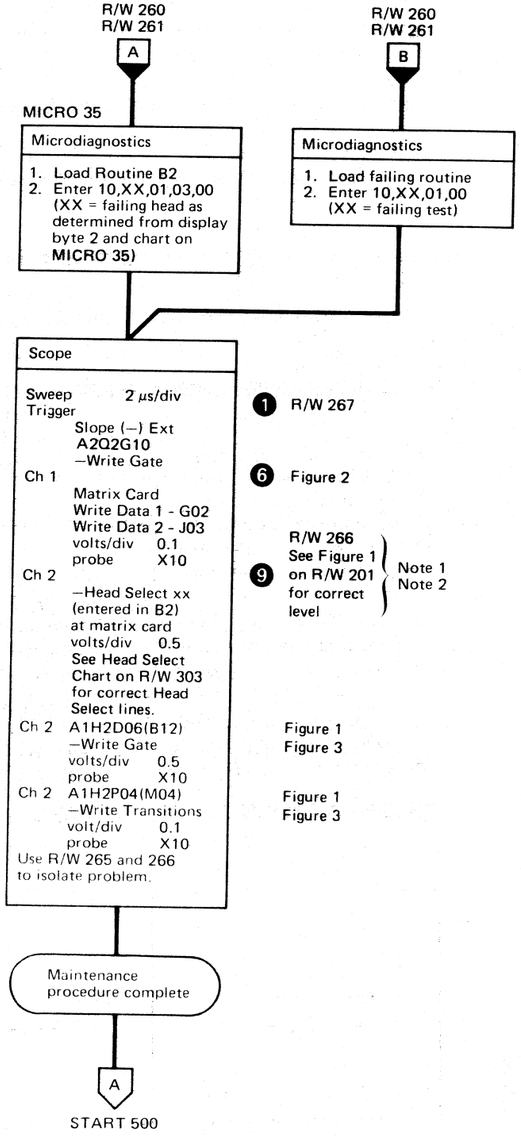
See theory of Write operation in drive on R/W 100-101.

Note 1: Scope Head Selects, R/W 266.
AF1A uses head 1. All other error stops use head 0.
Head selected = 0 V
Head deselected = +6 V

If an error is detected while looping a test, the microprogram terminates the test and starts it over again from the beginning. Any part of the signal appearing after the error is detected and before the test is restarted is not valid.

Note 2: If Head Select is correct to matrix card and matrix card was replaced previously, check for open in cable from matrix card to DM connector pins. See R/W 340. If Head Select is correct, continue scoping.

Note 3: If –Write Transitions does not reach a stable –MST level, check +Read Gate at R/W matrix card pin B05. Ensure level is inactive (0V).



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Figure 1. Start of Write Operation

2 µs/div 0.1 volts/div X10 probe

R/W 266 1 –Write Gate
A1H2D06(B12) (KL010)

R/W 265 1 (Note 3) –Write Transitions
A1H2P04(M04) (KL090)

–Write Current Sense
A1H2P05(P06) (KL120)

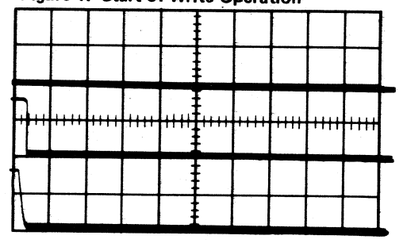


Figure 2. MST Levels

5 µs/div 0.01 volts/div X10 probe

R/W 267 6 Write Data 1
A1J2B04(D05) (KN010)
Matrix Card G02

R/W 267 6 Write Data 2
A1J2B05(D07) (KN010)
Matrix Card J03

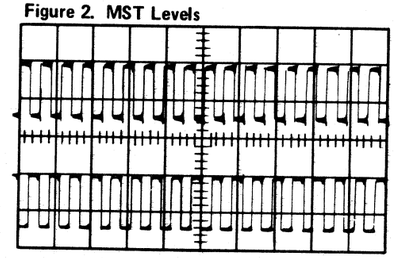


Figure 3. End of Write Operation

2 µs/div 0.1 volts/div X10 probe

R/W 266 1 –Write Gate
A1H2D06(B12) (KL010)

R/W 265 1 (Note 3) –Write Transitions
A1H2P04(M04) (KL090)

–Write Current Sense
A1H2P05(P06) (KL120)

Use delayed sweep

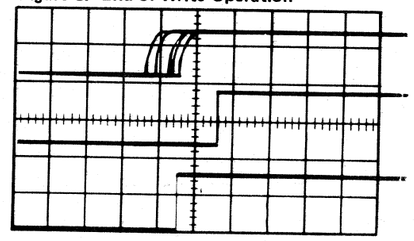


Figure 4. R/W Data

Sync Int (+)

0.5 µs/div 50 mv/div X10 probe

+R/W Data
A2T2D07 A1J2D12

–R/W Data
A2T2B05 A1J2D13

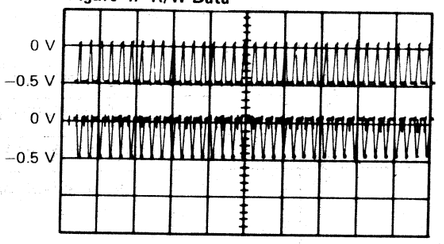
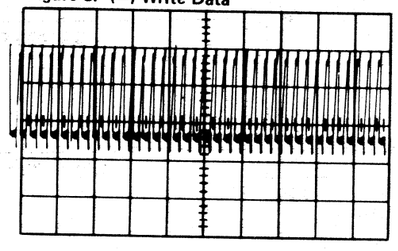


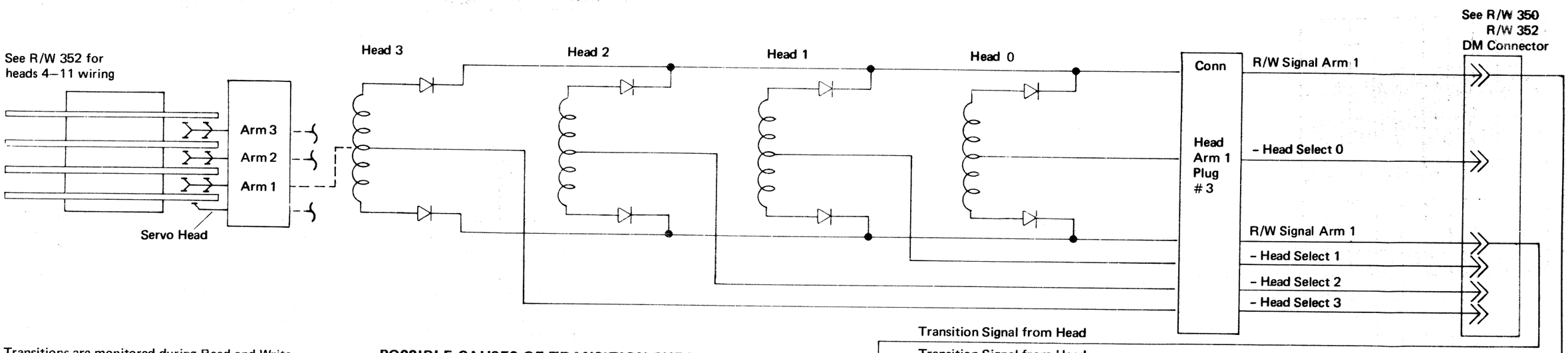
Figure 5. (–) Write Data

0.5 µs/div 0.05 volts/div X10 probe

Write Data Test Point
A2T2B04 (BJ130)



WRITE TRANSITION CHECK



Transitions are monitored during Read and Write operations. Transitions detected when not in a Write operation set the transition check latch; see R/W 265.

During Write operations, transitions are detected on the R/W matrix card. Transitions must be present after writing begins and ends, or a transition check occurs.

The accompanying diagram gives an overview of how transitions are detected in the R/W matrix card. The inputs to the transition detector are from each arm. The diagram above shows Arm 1, which contains physical heads 0, 1, 2, and 3.

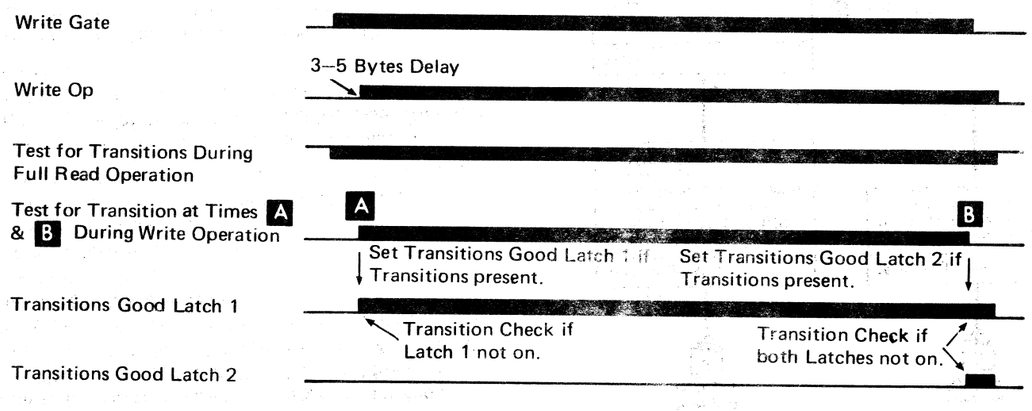
See diagrams on R/W 265, 266, and 267.

POSSIBLE CAUSES OF TRANSITION CHECKS

ONE HEAD FAILS – Follows data module; open head or faulty DM connector. See R/W 340, R/W 350. All data modules fail; failing head not being selected. See R/W 204.

FOUR HEADS AND ONE ARM FAIL – Follows data module-possible open wire at data module connector or head arm plug. All data modules fail; open transition diode in R/W matrix card.

ALL HEADS FAIL –
1. Absence of Write data. See R/W 266 for Write data path.
2. Faulty transition detector on R/W matrix card.
3. Faulty check circuitry on A1H2 card.



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WRITE CURRENT CHECK

A Write Current Check occurs:

- If Write Current is not detected at all times while Write Gate is active.
- If Write Current is detected while Write is not active.

See R/W 275 for detailed information on Write Current sense.

See theory of Write operation in drive on R/W 100-101.

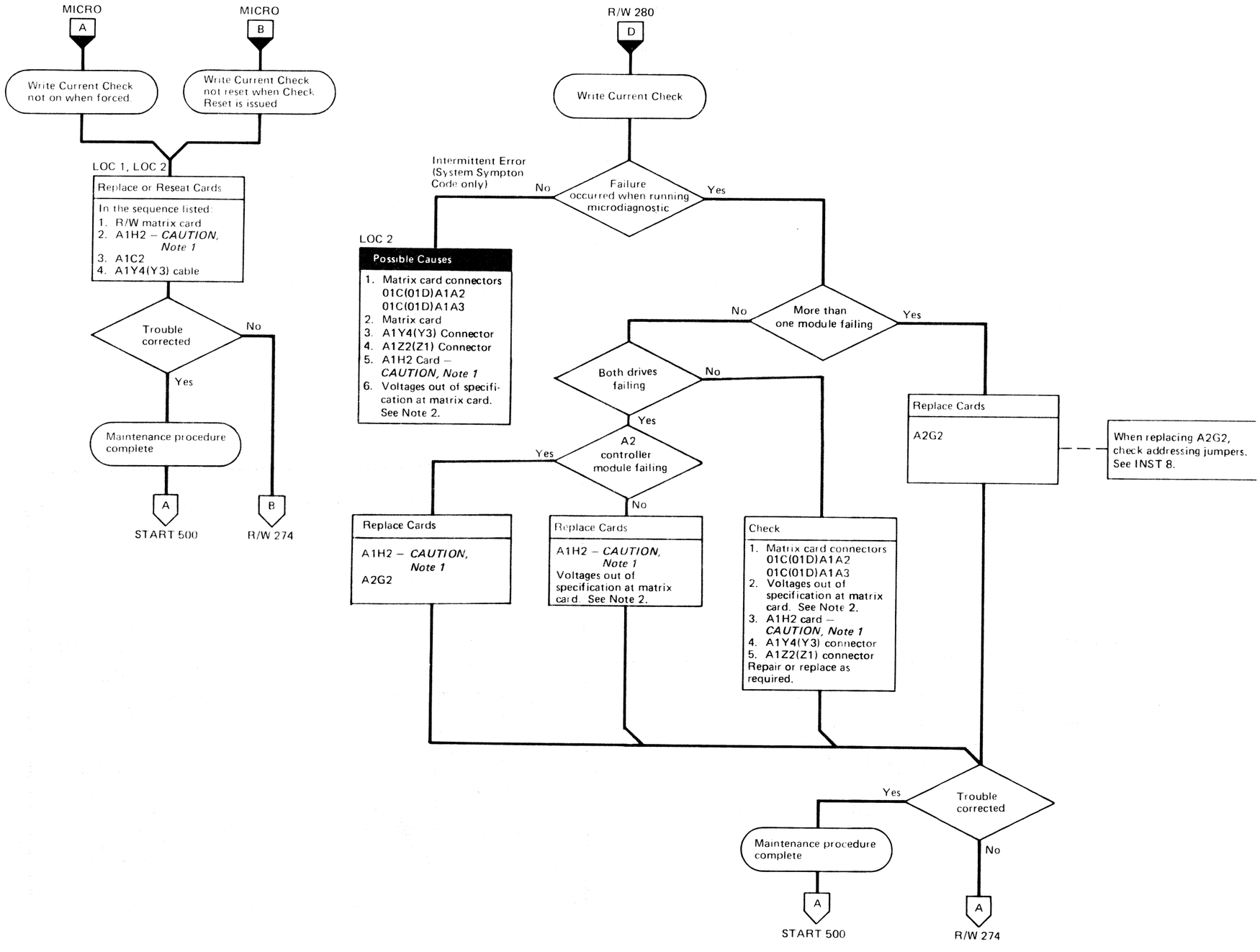
Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: −4 Vdc (−3.84 V to −4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin.

If either of these voltages is not as specified, go to PWR 10, Entry C.

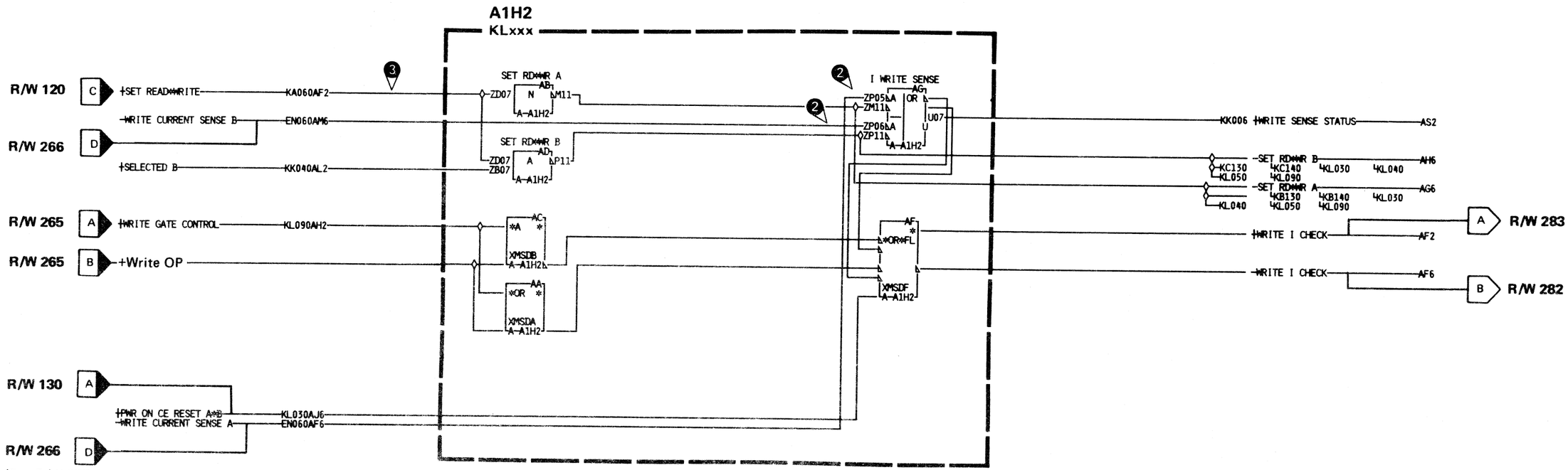


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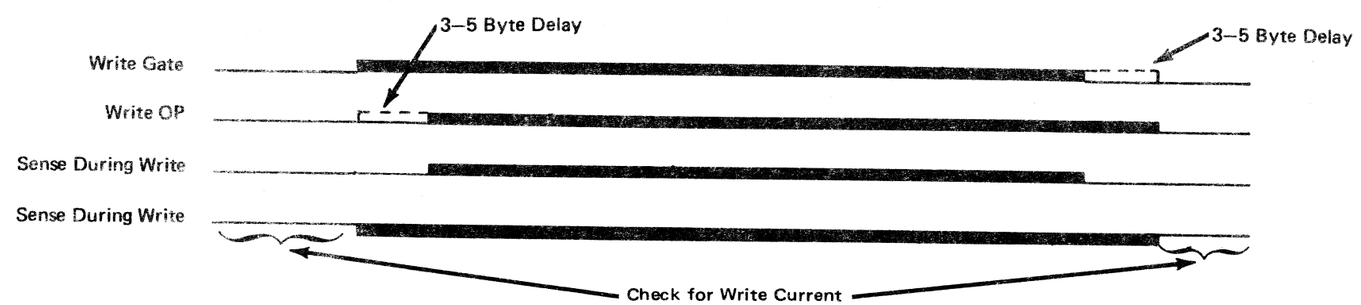
440203 2 Nov 73	440205 28 Jan 74	440209 25 Mar 74	440218 5 Aug 74	440223 14 Mar 75		

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WRITE CURRENT CHECK



(See R/W 275 for detailed information.)



Write Current Check
No Write current during a Write operation, or detection of Write current while not writing.

See R/W 275 for Write Current Sense information.

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WRITE CURRENT CHECK

Refer to R/W 275 for Write Current Sense theory.

R/W 270
A

A369 error
No
Yes

Microdiagnostic
1. Load routine A3
2. Enter 10,06,01,00

Scope – Figure 1
Sweep 0.1 μs/div
Slope (+)
Ch 1 only
Ch 1 A1H2D07
+Set Read Write
volts/div 0.1
probe X10
Ch 2 A1H2P05(P06)
–Write Current Sense
This signal should remain +MST.
Use R/W 271 to isolate. See theory on R/W 275.

R/W 271 ❸
R/W 271 ❷

Failure occurs on B2 Micro
No
Yes

Microdiagnostic
1. Load routine B2
2. Enter 10,01,00, 03, 00

Microdiagnostic
1. Load failing routine
2. Enter 10,XX,01,00 (XX = failing test)

Scope – Figure 2
Sweep 1.0 μs/div
Slope (–) Ext
–Write Gate A(B) A1H2D06(B12)
Ch 1 A1H2M05(M07) –Current Source Blkd
volts/div 0.5
probe X10
Ch 2 A1H2P05(P06) –Write Current Sense
volts/div 0.1
probe X10
These signals should remain at –MST as long as write gate is active.
Use R/W 271 and R/W 266 to isolate. See theory on R/W 275.

R/W 266 ❶
R/W 266 ❷
R/W 271 ❷

Maintenance procedure complete

A
START 500

Figure 1 – A369 Error

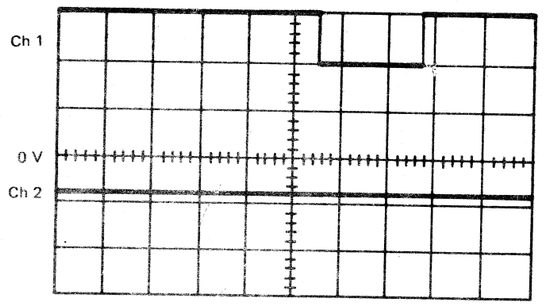
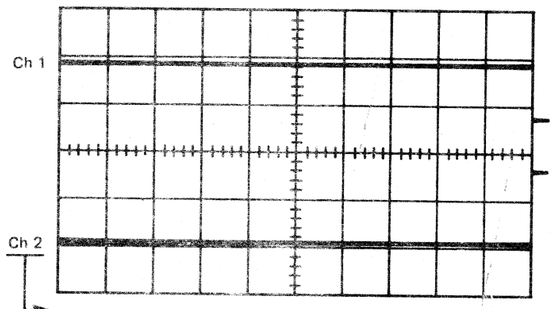


Figure 2 – Shows B2 Routine



In order for Write Current Sense to be active, the following R/W Matrix Card Controls are necessary:

1. Write Gate active.
2. Current Source Blocked inactive.
3. Set Read Write Safe active (no R/W Checks).

Note: When scoping, be aware that once an error is detected further testing is suspended and the error message is generated. Therefore the signals beyond the point of the error are not valid.

R/W 270
B

Microdiagnostic
1. Load routine AD
2. Enter 10,08,01,00

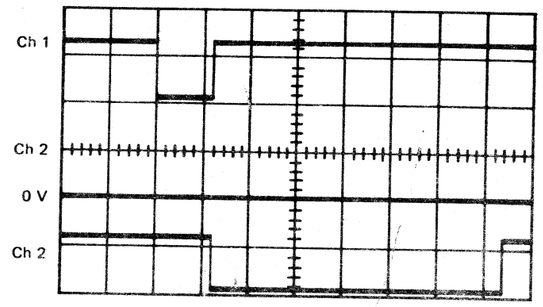
Scope – Figure 3
Sweep 10 μs/div
Slope (–) Ext
–Drive Sync Tag TP A1C2G02
Ch 1 A1H2D06(B12) –Write Gate A (B)
volts/div 0.5 V
probe X10
Ch 2 –Current Source Blocked A1H2M05(M07)
volts/div 0.5 V
probe X10
This signal should remain at 0 V (active).
Ch 2 A1H2S03 –Read Write Check TP
volts/div 0.1 V
probe X10
Use diagram on R/W 271 and description on R/W 275 and 269 to isolate.

R/W 266 ❶
R/W 266 ❷
R/W 283 ❶

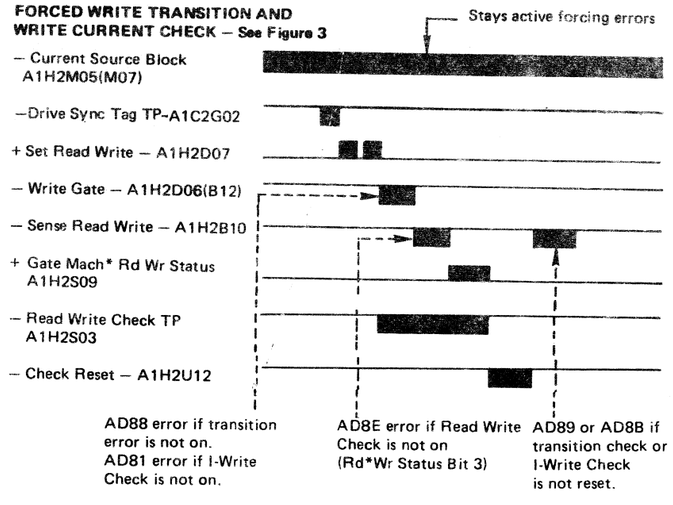
Maintenance procedure complete

A
START 500

Figure 3



FORCED WRITE TRANSITION AND WRITE CURRENT CHECK – See Figure 3



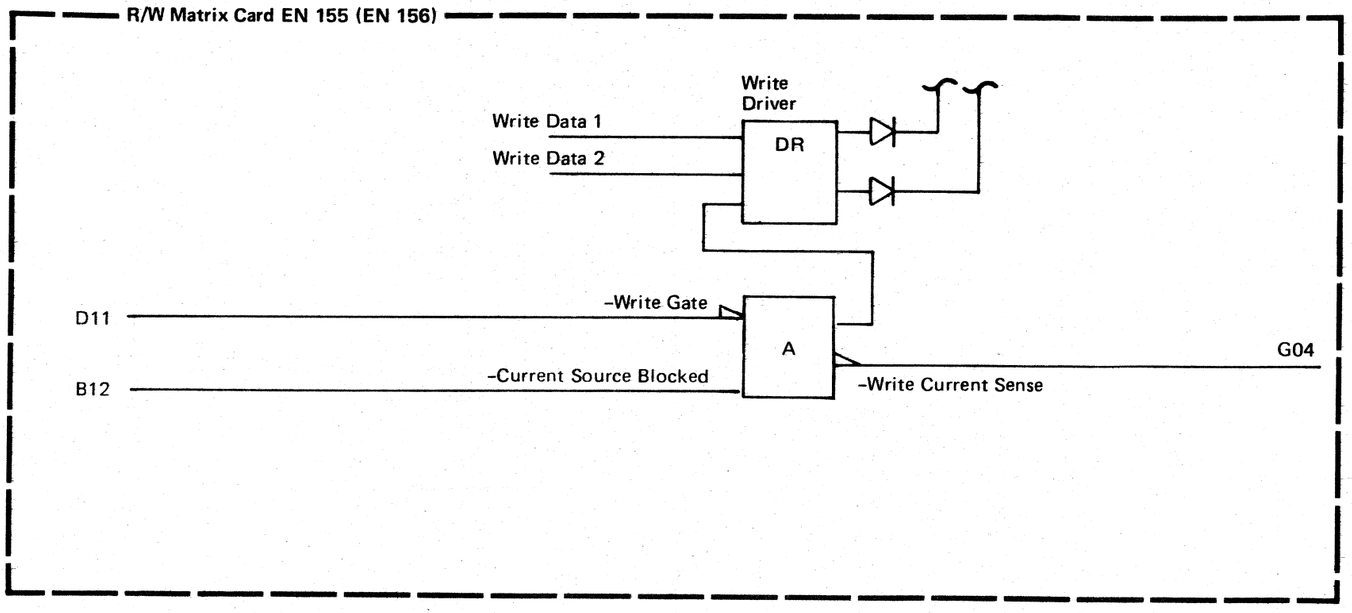
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WRITE CURRENT SENSE

The Write Current line is monitored during the Write operation except for a 3–5 byte delay at the beginning of Write Gate (Address Mark Area on Write Format G3 OP). If –Write Current Sense is not present, Write Current Check is detected. If –Write Current sense is active when set Read/Write in drive is active (not Write OP), Write Current Check is detected.

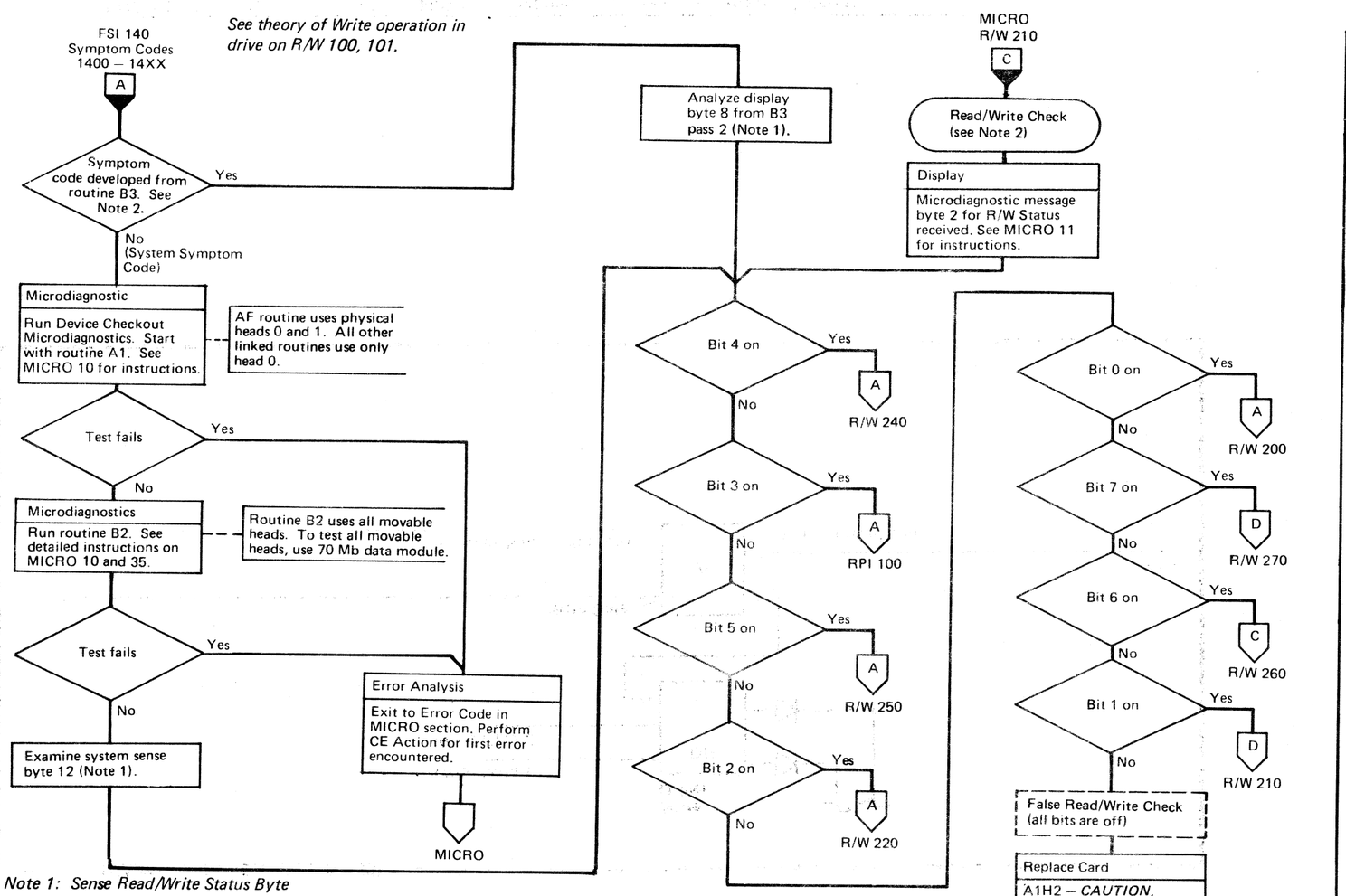
The Write Current Sense line is active if –Write Gate at the R/W matrix card is active and –Current Sense Blocked is inactive (OK to write). See Diagram **R/W 271** for I-Write Check Error Latch.

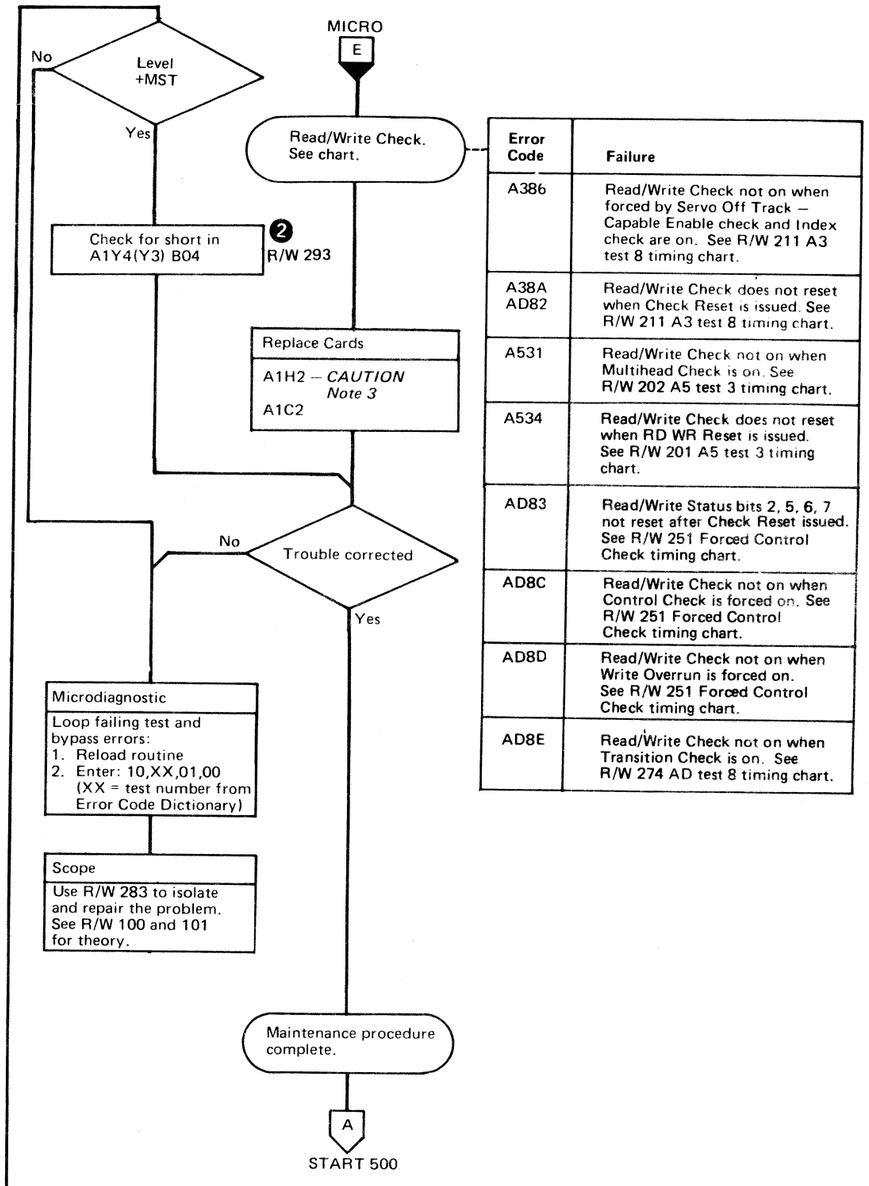
See theory of Write operation in drive on R/W 100,101.



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READ/WRITE CHECK





Error Code	Failure
A386	Read/Write Check not on when forced by Servo Off Track – Capable Enable check and Index check are on. See R/W 211 A3 test 8 timing chart.
A38A AD82	Read/Write Check does not reset when Check Reset is issued. See R/W 211 A3 test 8 timing chart.
A531	Read/Write Check not on when Multihead Check is on. See R/W 202 A5 test 3 timing chart.
A534	Read/Write Check does not reset when RD WR Reset is issued. See R/W 201 A5 test 3 timing chart.
AD83	Read/Write Status bits 2, 5, 6, 7 not reset after Check Reset issued. See R/W 251 Forced Control Check timing chart.
AD8C	Read/Write Check not on when Control Check is forced on. See R/W 251 Forced Control Check timing chart.
AD8D	Read/Write Check not on when Write Overrun is forced on. See R/W 251 Forced Control Check timing chart.
AD8E	Read/Write Check not on when Transition Check is on. See R/W 274 AD test 8 timing chart.

Note 1: Sense Read/Write Status Byte

a. System Sense Byte 12, Format 1.
b. Microdiagnostic routine B3 Sense Byte 8 Record Message Byte 8 of pass 2. See MICRO 36 for run instructions.

	Bit
Multihead Check	0
Capable/Enable Check	1
Write Overrun Check	2
Index Check	3
Interlock Check	4
Control Check	5
Transitions Check	6
Write Current Check	7

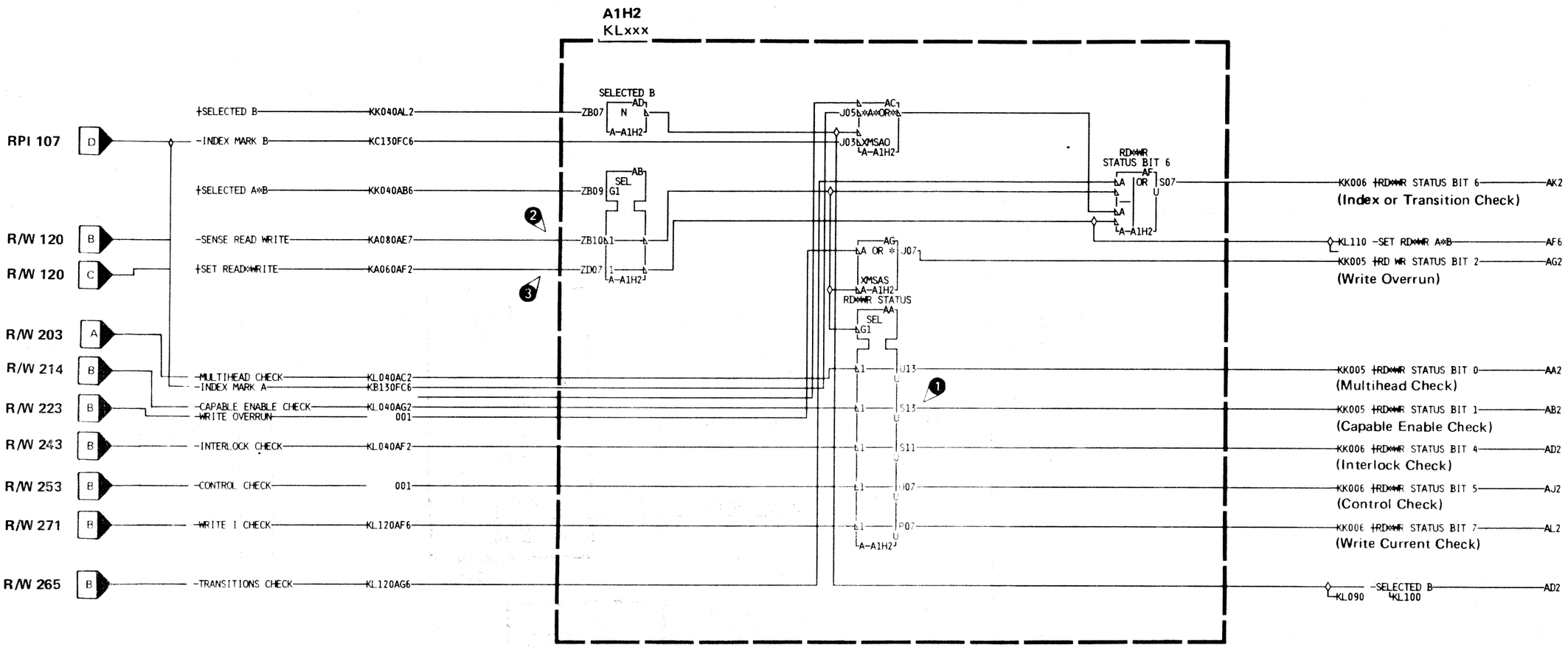
Note 2: It is possible to get multiple Read/Write Check bits set as a result of problems in this area. Troubleshooting the primary errors first avoids confusion. For A384 error, ignore bits 1 and 3 if on.

Note 3: R/W and PLO signals are terminated by resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removal of the A1J2 or A1H2 cards in the last module causes R/W failures in other modules. As a precaution to prevent data checks, the customer should be prevented from using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module.

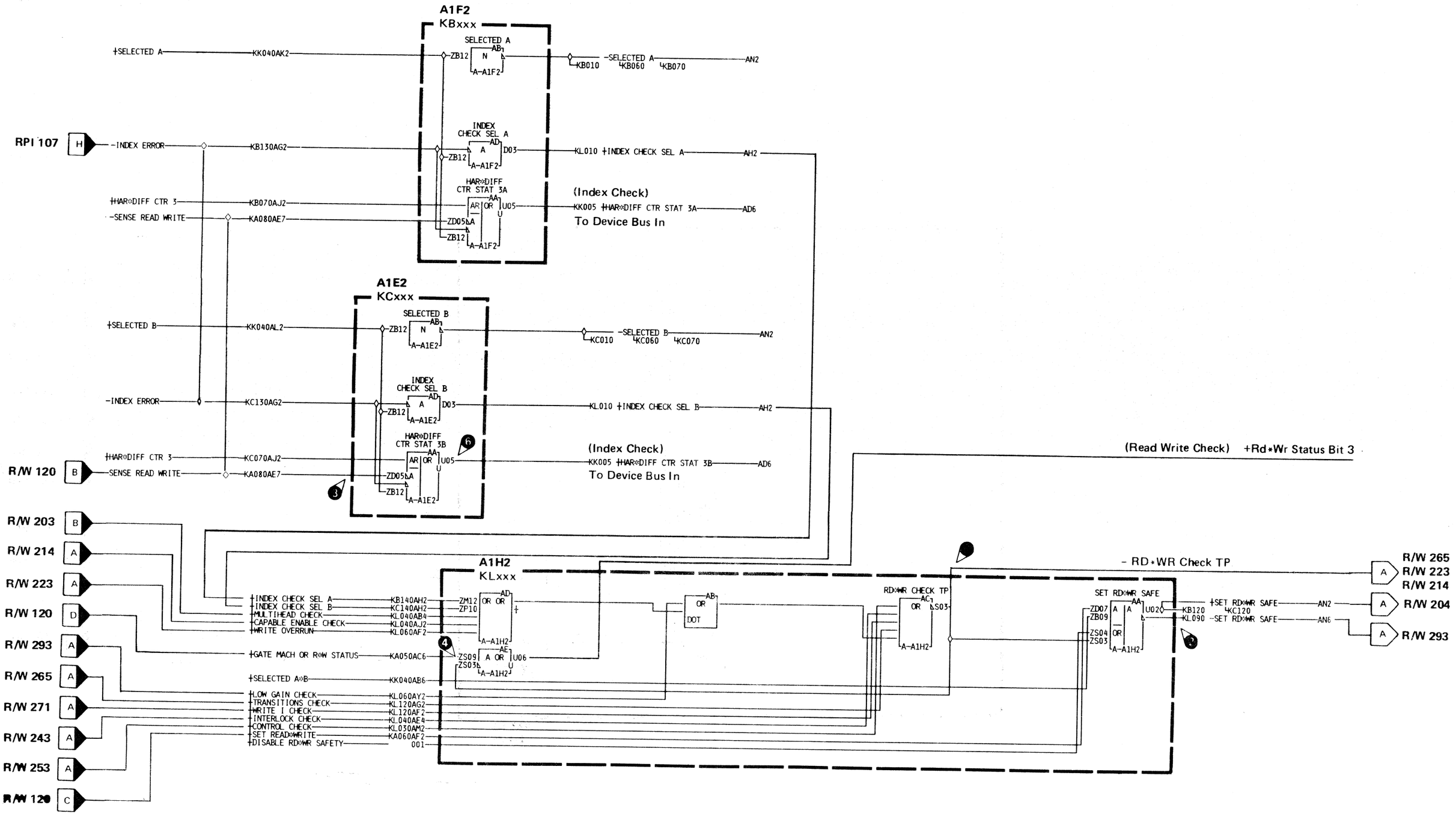
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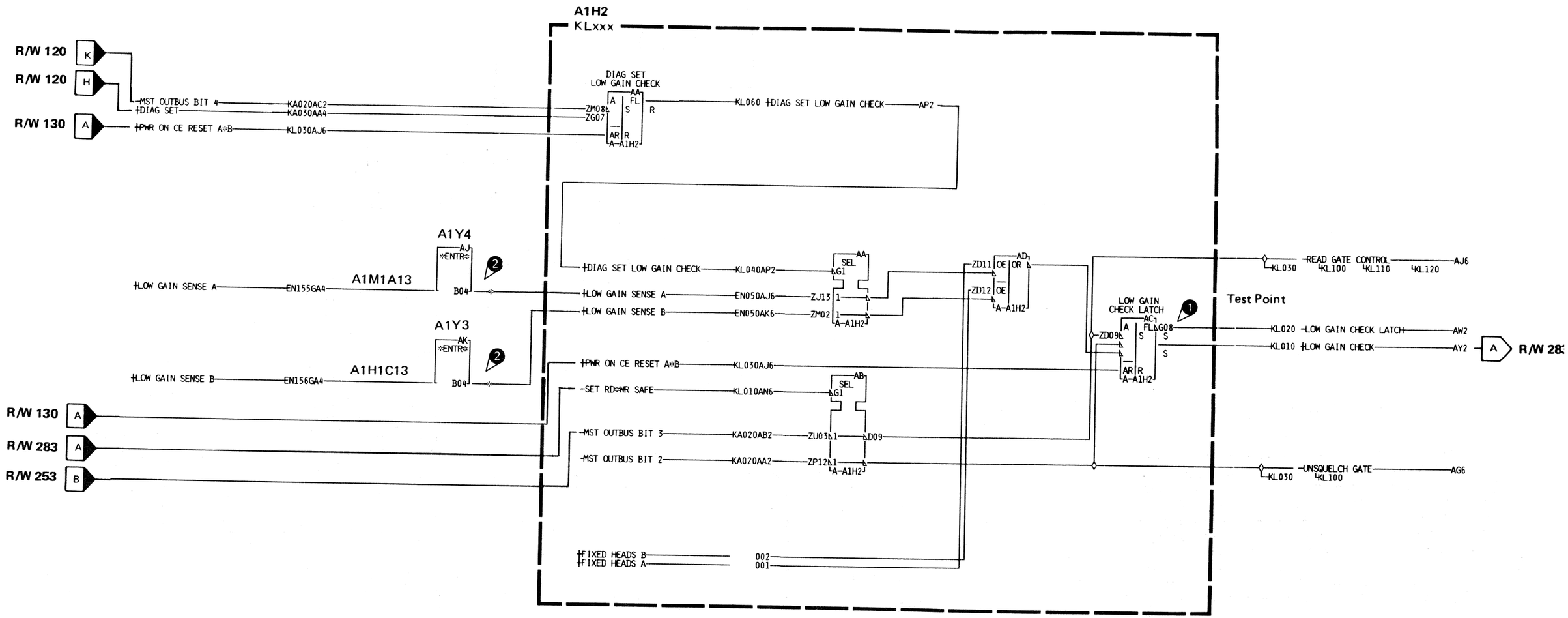


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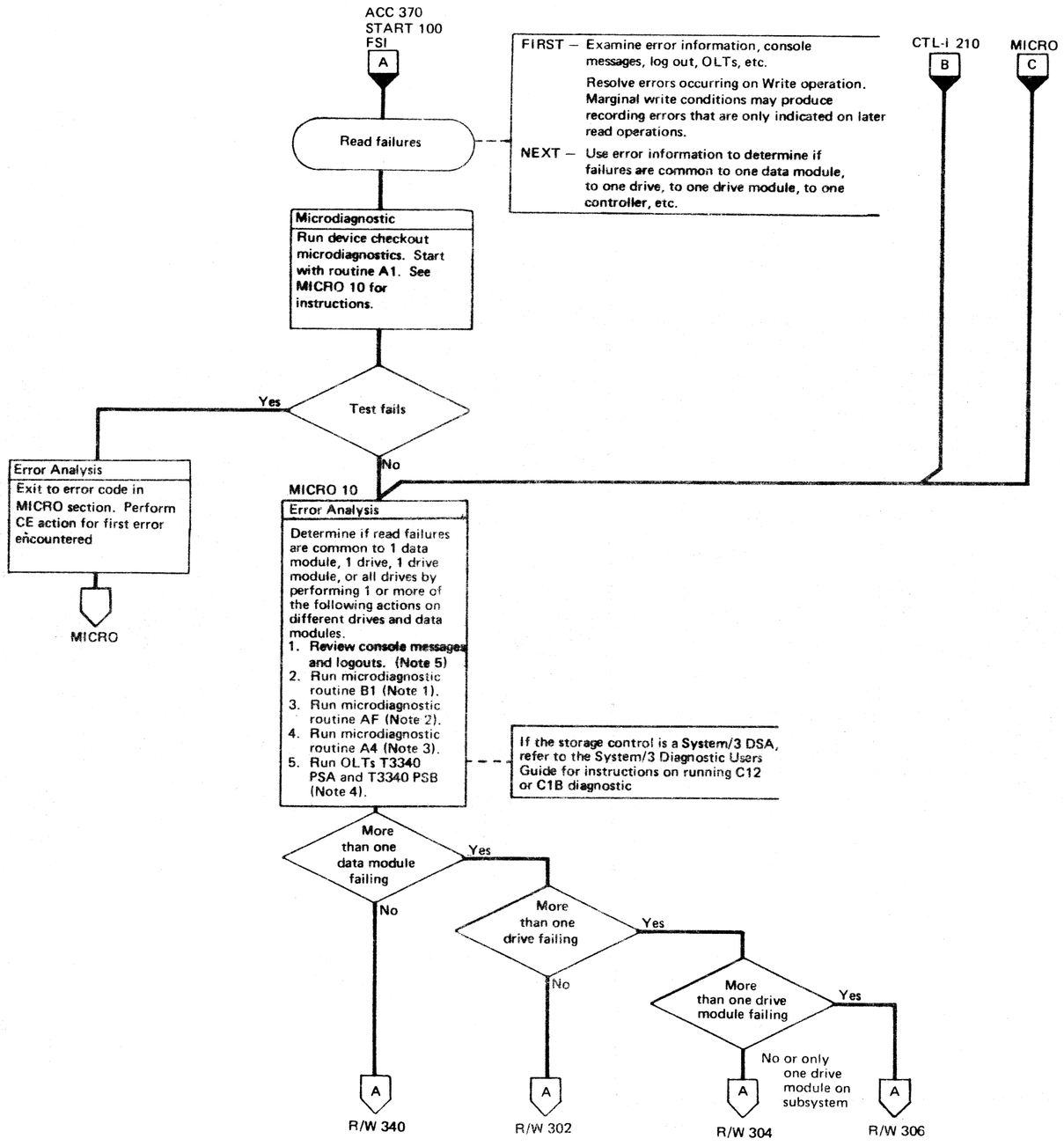
LOW GAIN SENSE



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READ FAILURE UNIT ISOLATION



Note 1:
Routine B1, running in default mode, reads the home address and all records on the even CE cylinders using all physical heads. By entering parameters, any customer cylinder and head may be selected and checked for errors. See MICRO 34. If the Fixed Head feature is installed, with a fixed head data module loaded, and parameters are entered to read the fixed heads, routine B1 reads all records on all even and odd fixed head cylinders (cylinders 001 – 005) and stops on error. See MICRO 34

Note 2:
Routine AF uses physical head 0 to verify the seek to the even CE cylinder. Physical head 1 is then used to perform all Write and Read operations on the odd CE cylinder. See MICRO 32.

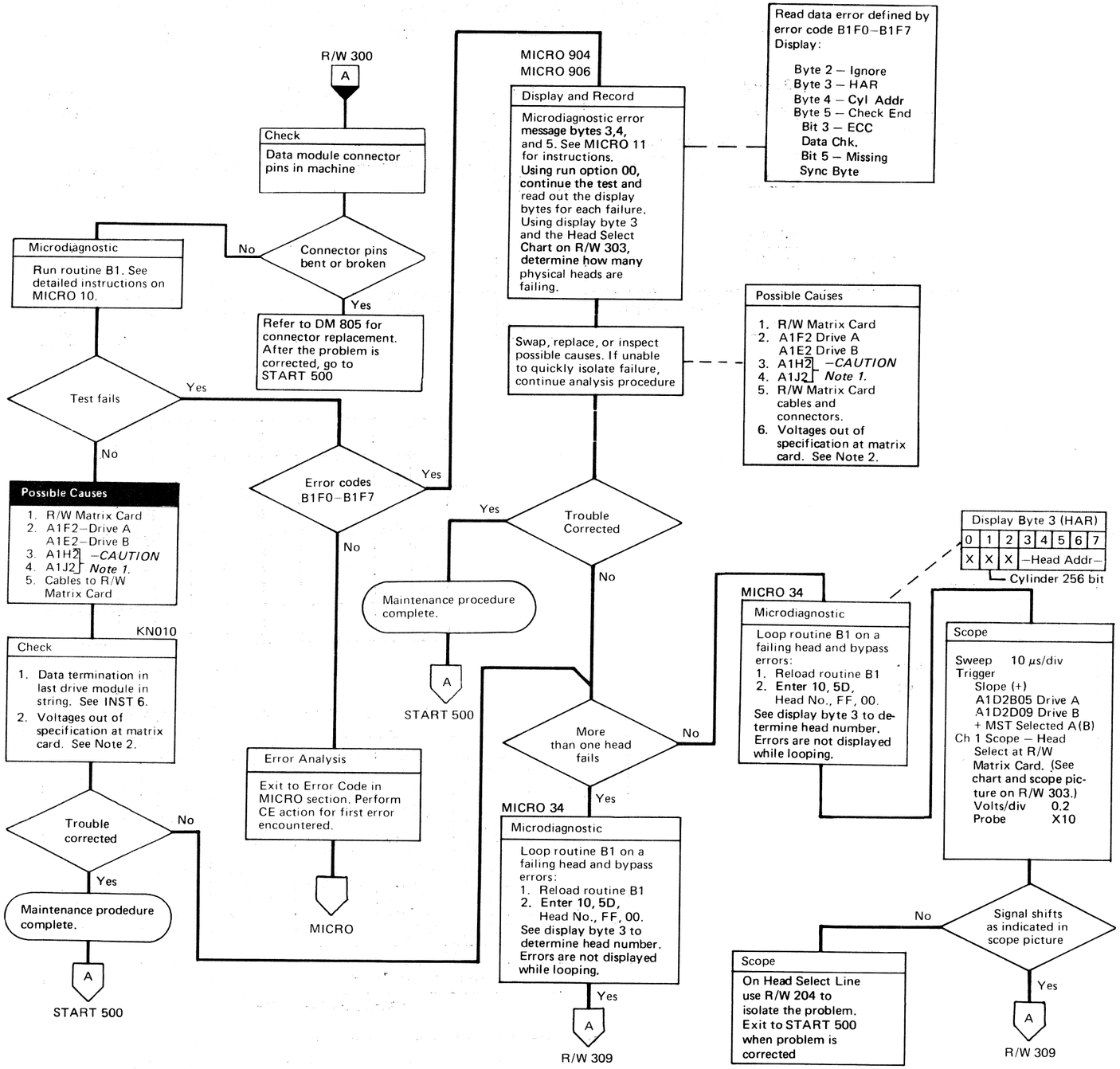
Note 3:
Routine A4 reads all even cylinder home address fields on the data module with physical head 0. See MICRO 22.

Note 4:
OLT T3340 PSA reads all customer home address and R0 fields on the data module. The CCHH bytes of the Home Address are compared to the CCHH bytes of R0 and an error summary is printed upon completion. OLT T3340 PSB reads all customer records and prints an error summary upon completion. See the OLT section of the MLM for information and instructions. If the storage control is a System/3 DSA, refer to the System/3 Diagnostic Users Guide for information and instructions.

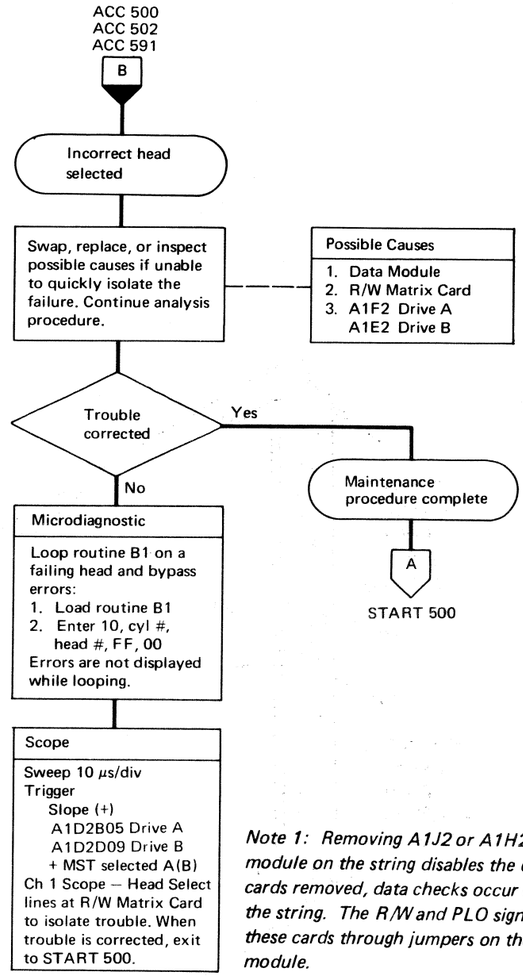
Note 5:
Refer to MSG section and SENSE 100 and 102 for analysis.

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SINGLE DRIVE READ FAILURE ANALYSIS



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Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: –4 Vdc (–3.84 V to –4.16 V) A1H1E13 to Y3B06 (A1M1C13 to Y4B06) to matrix card pin B06.

+6 Vdc (+5.76 V to +6.24 V) A1K1B13 to Y3B13 (A1N1F13 to Y4B13) to matrix card pin B13.

If either of these voltages is not as specified, go to PWR 10, Entry C.

HEAD SELECT SCOPING PROCEDURE

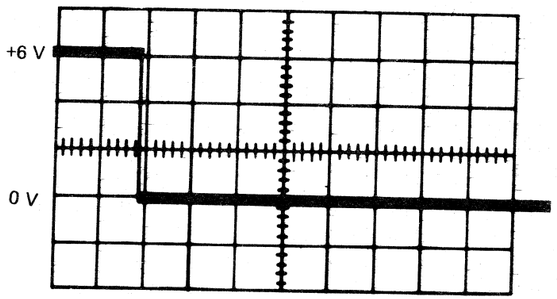
Determine the Head Select line that should be active (0 V) from the HAR value. Bits 3 to 7 of microdiagnostic routine B1, message byte 3 or parameter entry byte 2, mean the same as bits 3 to 7 of HAR. Use the chart and scope picture below to scope Head Select lines.

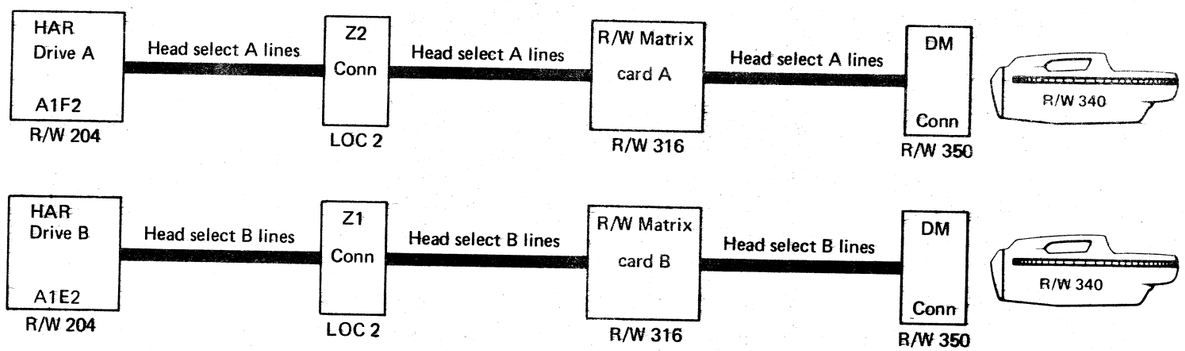
HEAD SELECT CHART

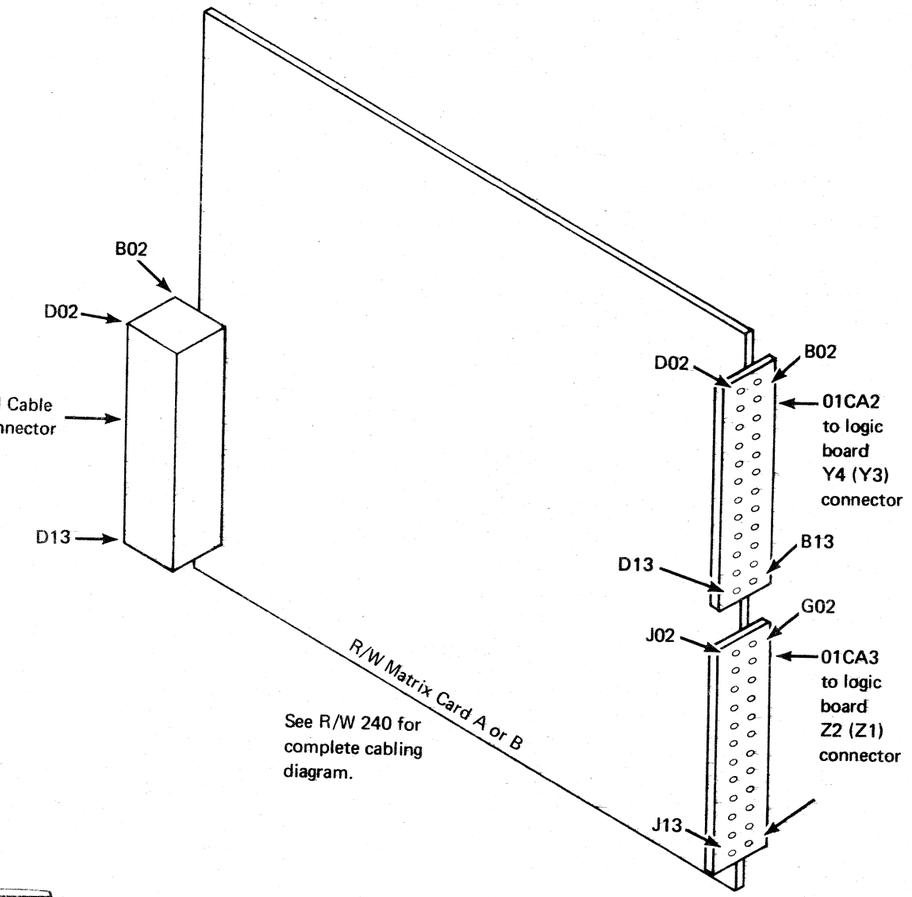
PHYSICAL HEAD		HAR BITS 3–7	HEAD SELECT LINES				
			DRIVE A		DRIVE B		R/W MATRIX
			CARD	CONN Z2	CARD	CONN Z1	CARD
35 Mb and 70 Mb	0	00 or 01	A1F2S12	A1G6A04	A1E2S12	A1C6E04	G13
	1	02 or 03	A1F2S13	A1F6C02	A1E2S13	A1C6B02	J10
	2	04 or 05	A1F2U13	A1E6D04	A1E2U13	A1B6C04	G06
	3	06 or 07	A1F2U09	A1E6D02	A1E2U09	A1B6C02	J06
	4	08 or 09	A1F2S09	A1E6E02	A1E2S09	A1B6D02	J07
	5	0A or 0B	A1F2S08	A1F6D02	A1E2S08	A1C6C02	J11
70 Mb Only	6	0C or 0D	A1F2U06	A1F6B04	A1E2U06	A1C6A04	G09
	7	0E or 0F	A1F2S05	A1E6C02	A1E2S05	A1B6B02	J05
	8	10 or 11	A1F2U10	A1F6E04	A1E2U10	A1C6D04	G12
	9	12 or 13	A1F2U12	A1F6B02	A1E2U12	A1C6A02	J09
	10	14 or 15	A1F2S10	A1F6C04	A1E2S10	A1C6B04	G10
	11	16 or 17	A1F2U11	A1F6A04	A1E2U11	A1B6E04	G08

Sync: A1D2B05 (Drive A) + MST Selected A(B) 10 μs/div
A1D2D09 (Drive B)

Scope: –Head Select 0.2 volts/div



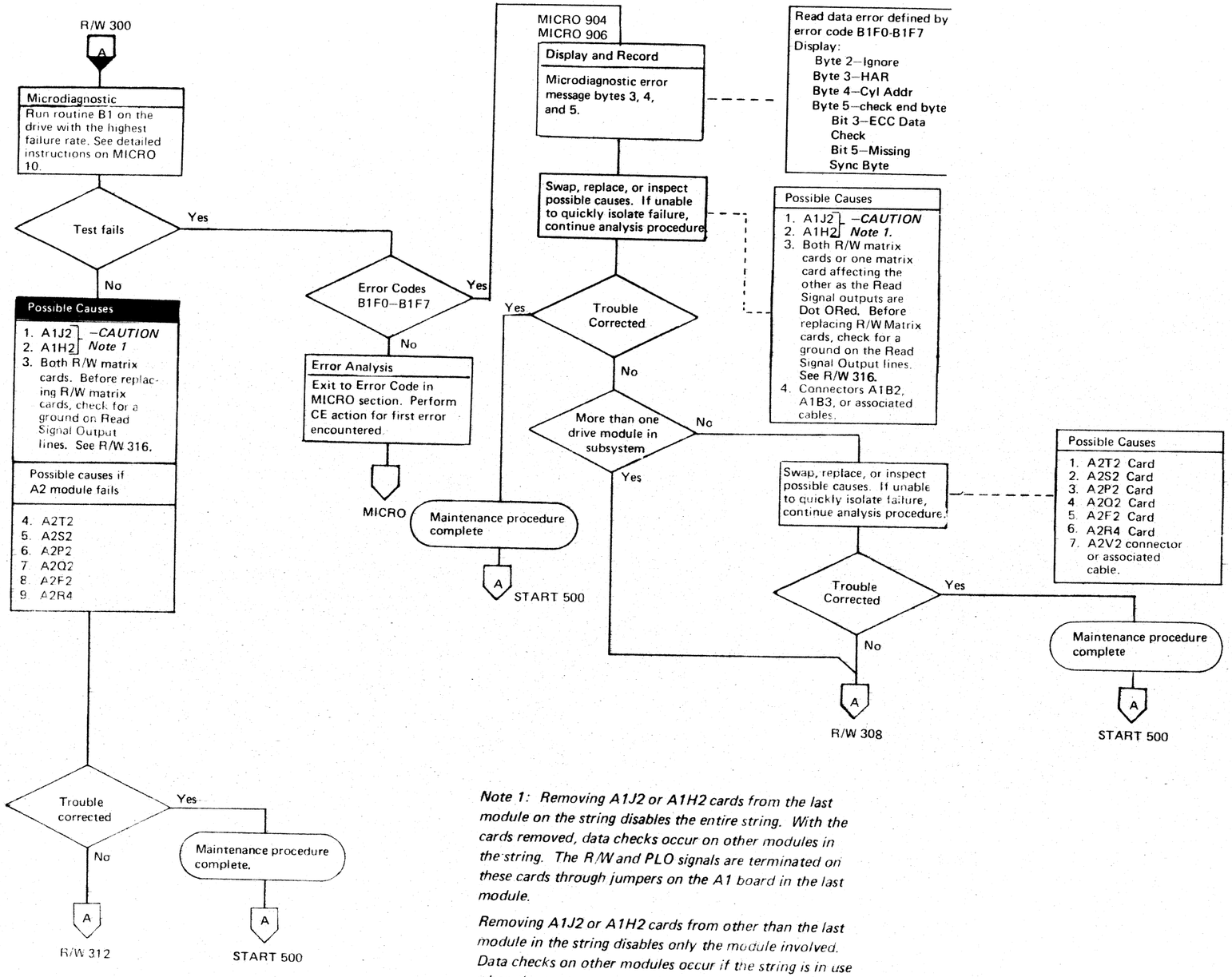




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DRIVE MODULE COMMON READ FAILURE ANALYSIS

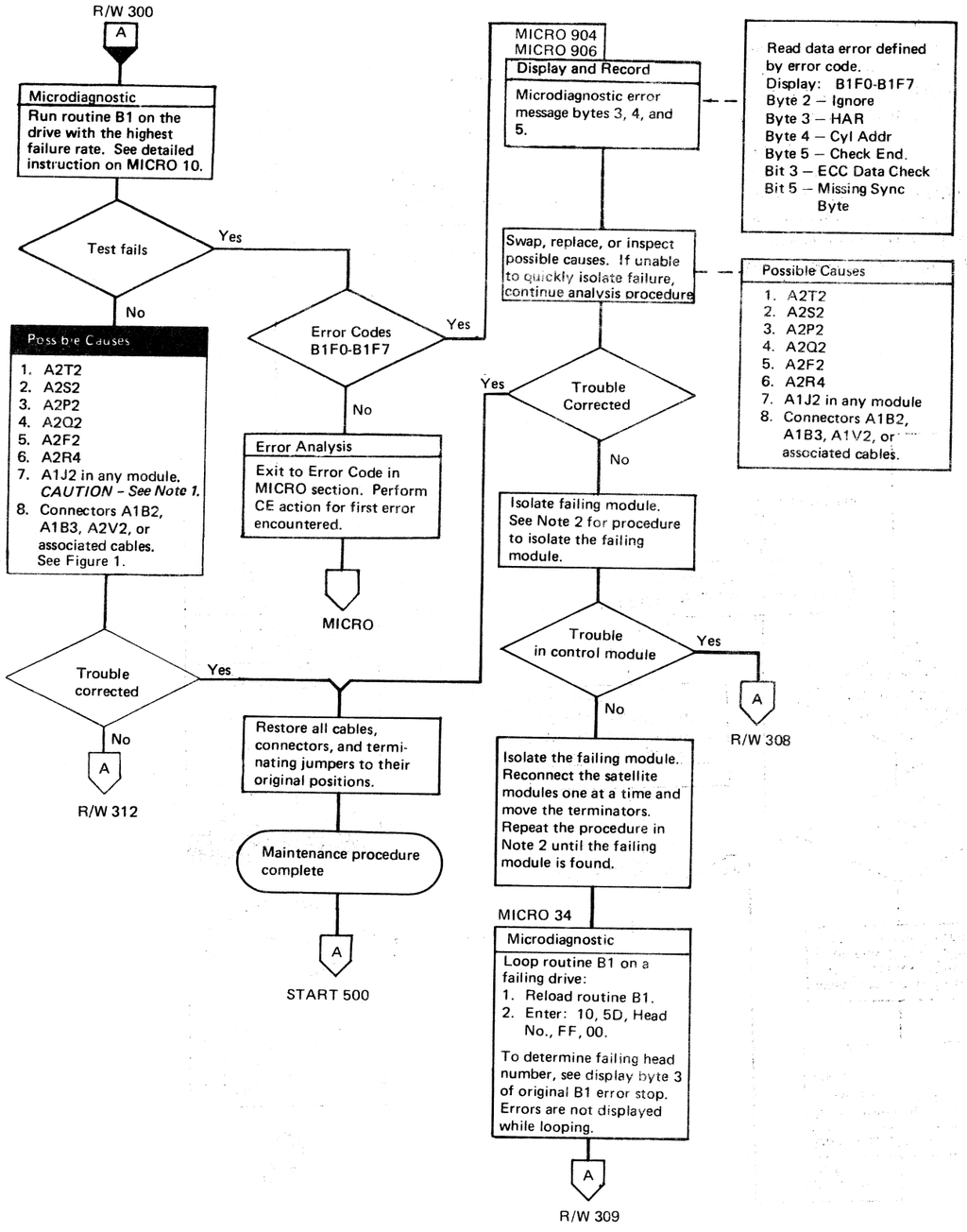


Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

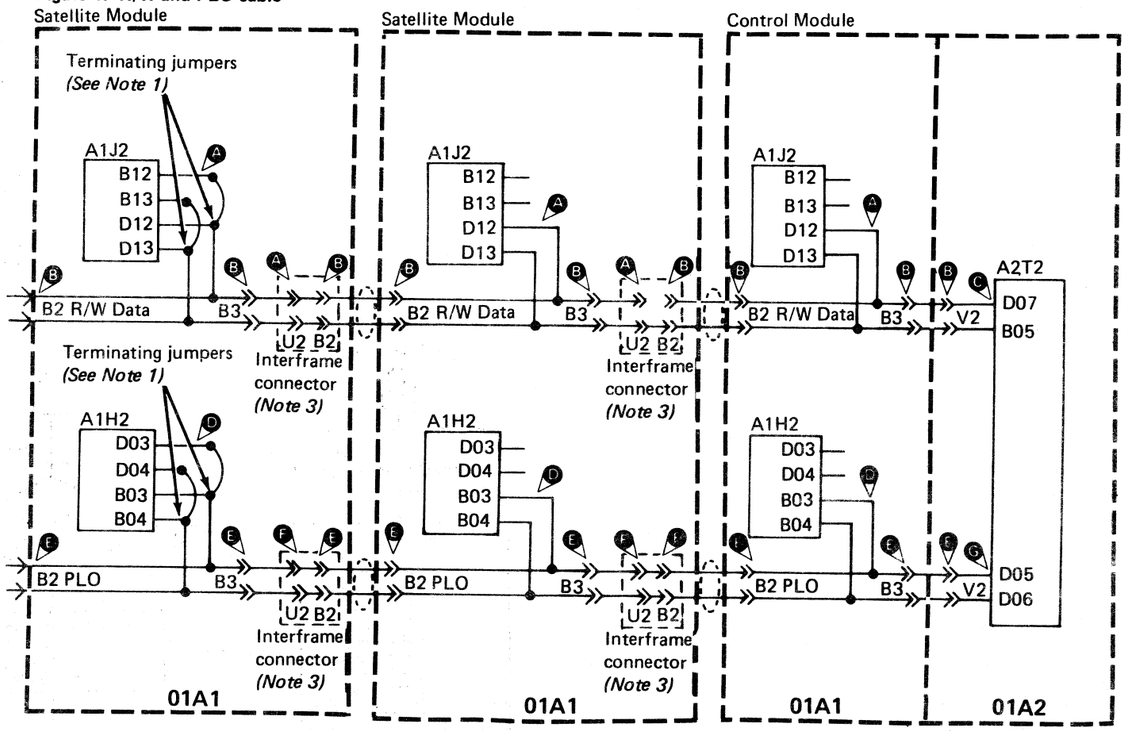
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SUBSYSTEM READ FAILURE ANALYSIS



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Figure 1. R/W and PLO cable



Line Name	A	B	C	D	E	F	G
+R/W Data	D12	B12	D07				
–R/W Data	D13	B13	B05				
–PLO Pulse Dr				B03	D02	B02	D05
–PLO Pulse Dr				B04	D03	B03	D06

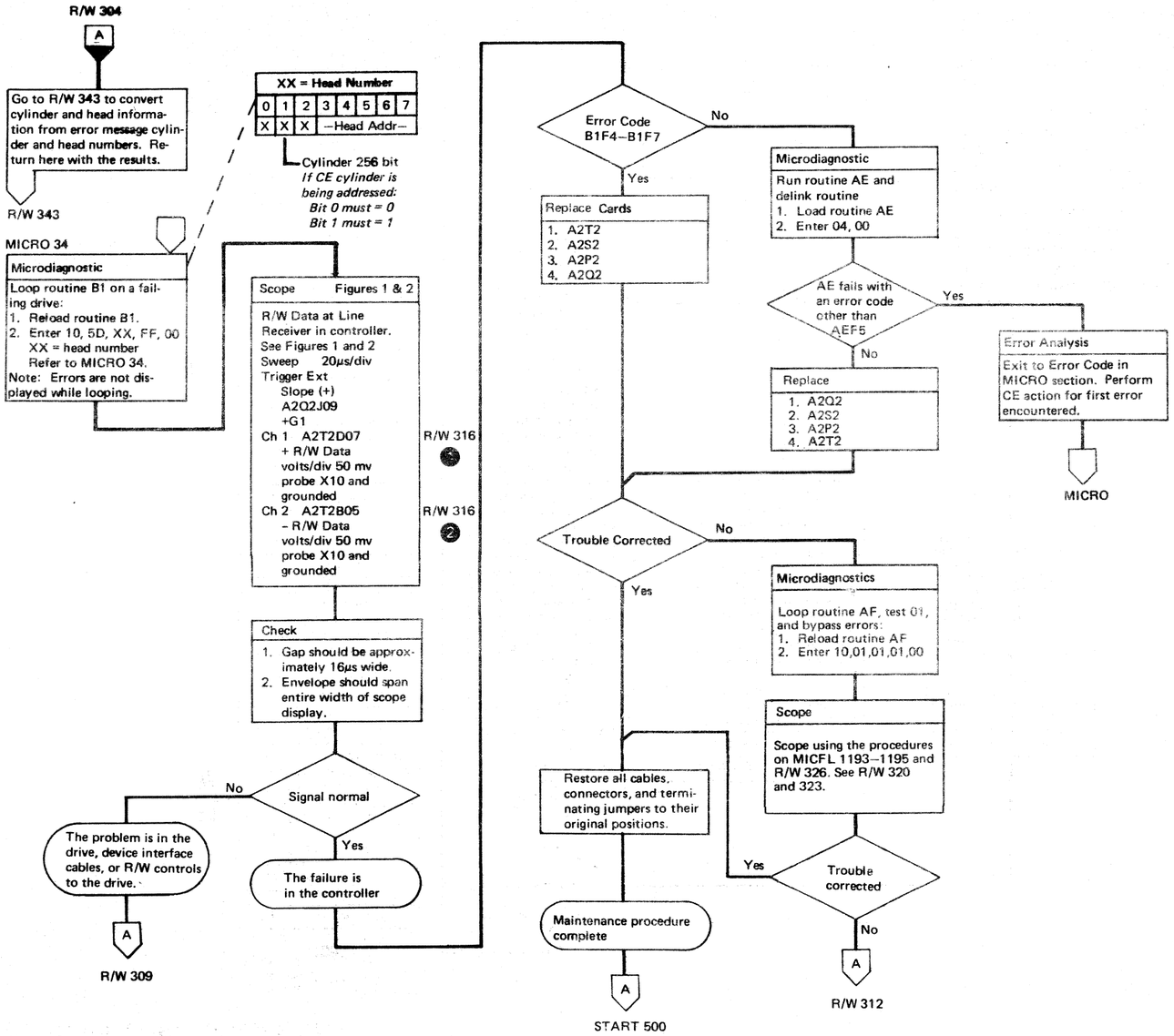
Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired. See INST 4 and ALD page KN010 for terminating jumper information.

Note 2: R/W data from each module (output of A1J2 card) is Dot ORed on the device interface. Isolate the problem to a module by disconnecting appropriate connectors and rerunning routine B1 on a control module drive. Start by powering down the subsystem and disconnecting A1B2 in the control module. Move the R/W and PLO terminators to the control module (Note 1). See Figure 1. Turn on one CE Mode switch in the control module. Turn all other CE Mode swithces off. Power-up the subsystem. Load a data module on the drive in CE Mode and rerun routine B1.

Note 3: The interface connector is not present on all machines.

READ FAILURE ISOLATION



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Figure 1

Ch 1 A2T2D07 + R/W Data
Ch 2 A2T2B05 – R/W Data

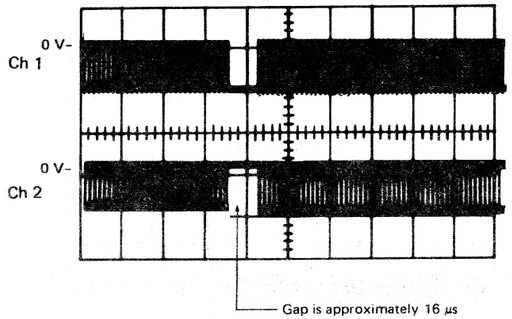
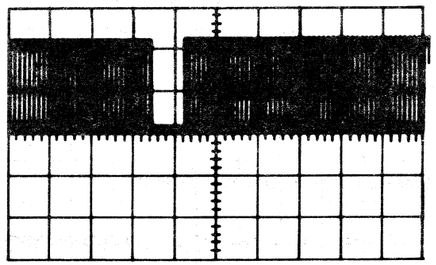


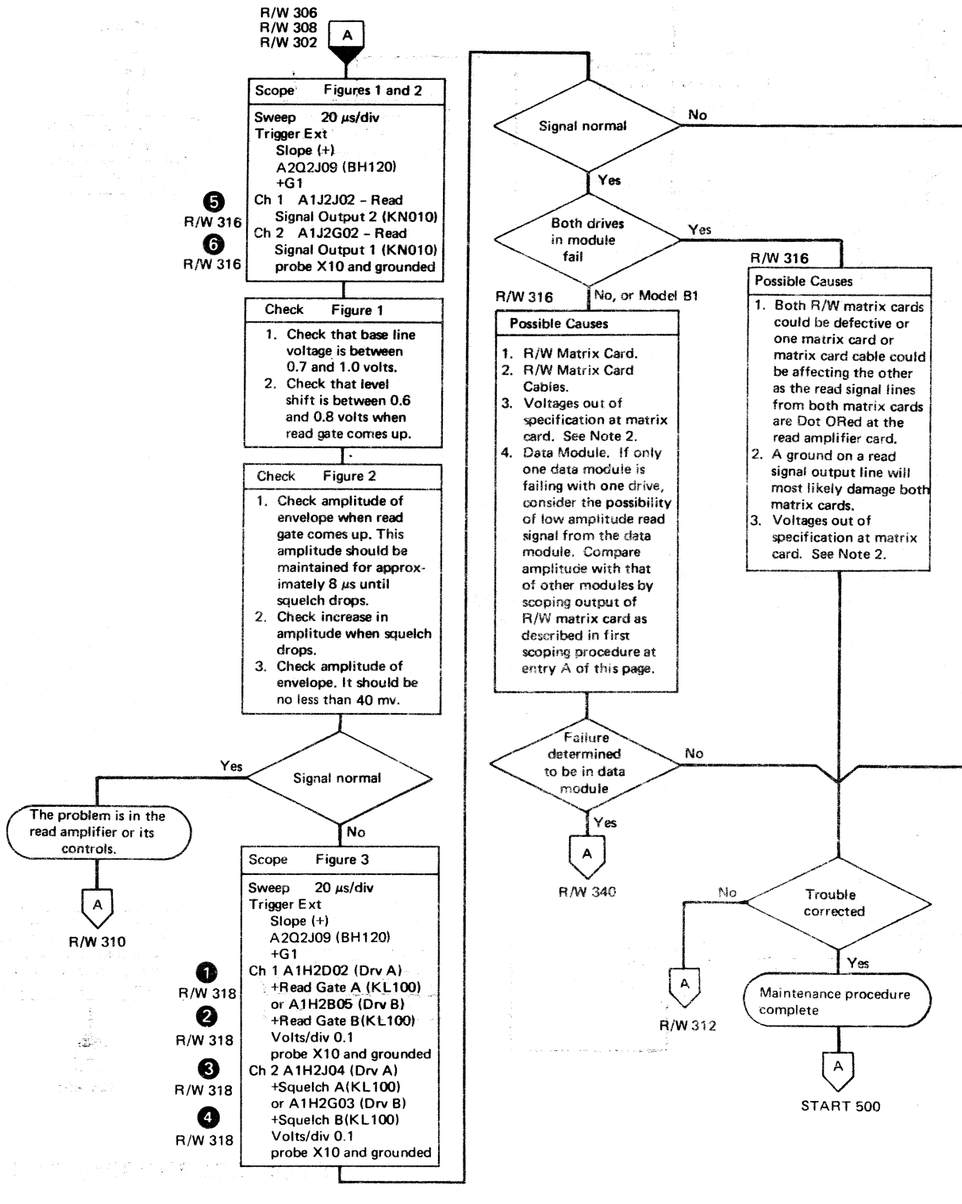
Figure 2

Same as Figure 1 except it is scoped differently (added mode with Ch 2 inverted).

Ch 1 and Ch 2 added



READ FAILURE ISOLATION



Note 1: Removing A1J2 or A1H2 cards from the last module on the string disables the entire string. With the cards removed, data checks occur on other modules in the string. The R/W and PLO signals are terminated on these cards through jumpers on the A1 board in the last module.

Removing A1J2 or A1H2 cards from other than the last module in the string disables only the module involved. Data checks on other modules occur if the string is in use when the cards are removed or replaced even though power is turned off in the module being repaired.

Note 2: −4 Vdc (−3.84 V to −4.16 V) A1M1C13 to Y4B06 (A1H1E13 to Y3B06) to matrix card B06 pin.

+6 Vdc (+5.76 V to +6.24 V) A1N1F13 to Y4B13 (A1K1B13 to Y3B13) to matrix card B13 pin. If the fixed head feature is installed, make sure that the 6 V jumper is also plugged to A1K1B13.

If either of these voltages is not as specified, go to PWR 10, Entry C.

Figure 1 - Read Signal at Output of R/W Matrix Card

Ch 1 A1J2J02 KN010 - Read Signal Output 2
Ch 2 A1J2G02 - Read Signal Output 1
50 mv/div probe X10

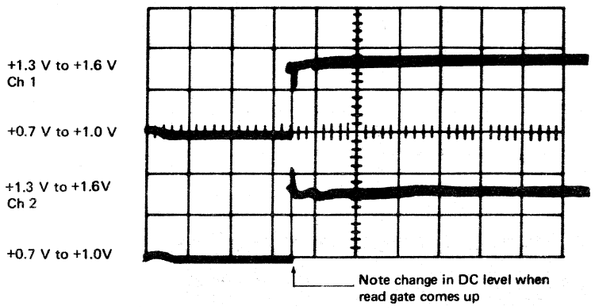


Figure 2 - Read Signal - Scoped Differentially

Same as Figure 1 above except scoped differently (added mode with Ch 2 inverted)
10 mv/div probe X10

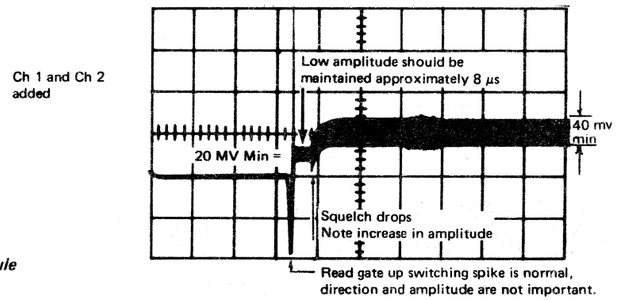
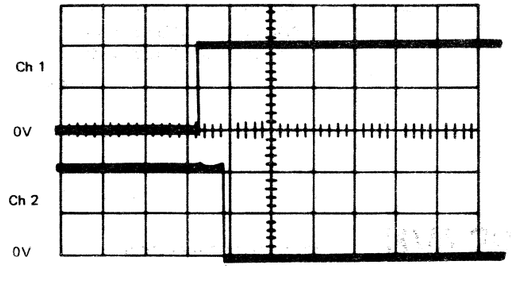


Figure 3 - R/W Matrix Card Control Lines

Ch 1 A1H2D02 (Drv A) or A1H2B05 (Drv B) + Read Gate
Ch 2 A1H2J04 (Drv A) or A1H2G03 (Drv B) + Squelch
0.1 volts/div probe X10



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READ FAILURE ISOLATION

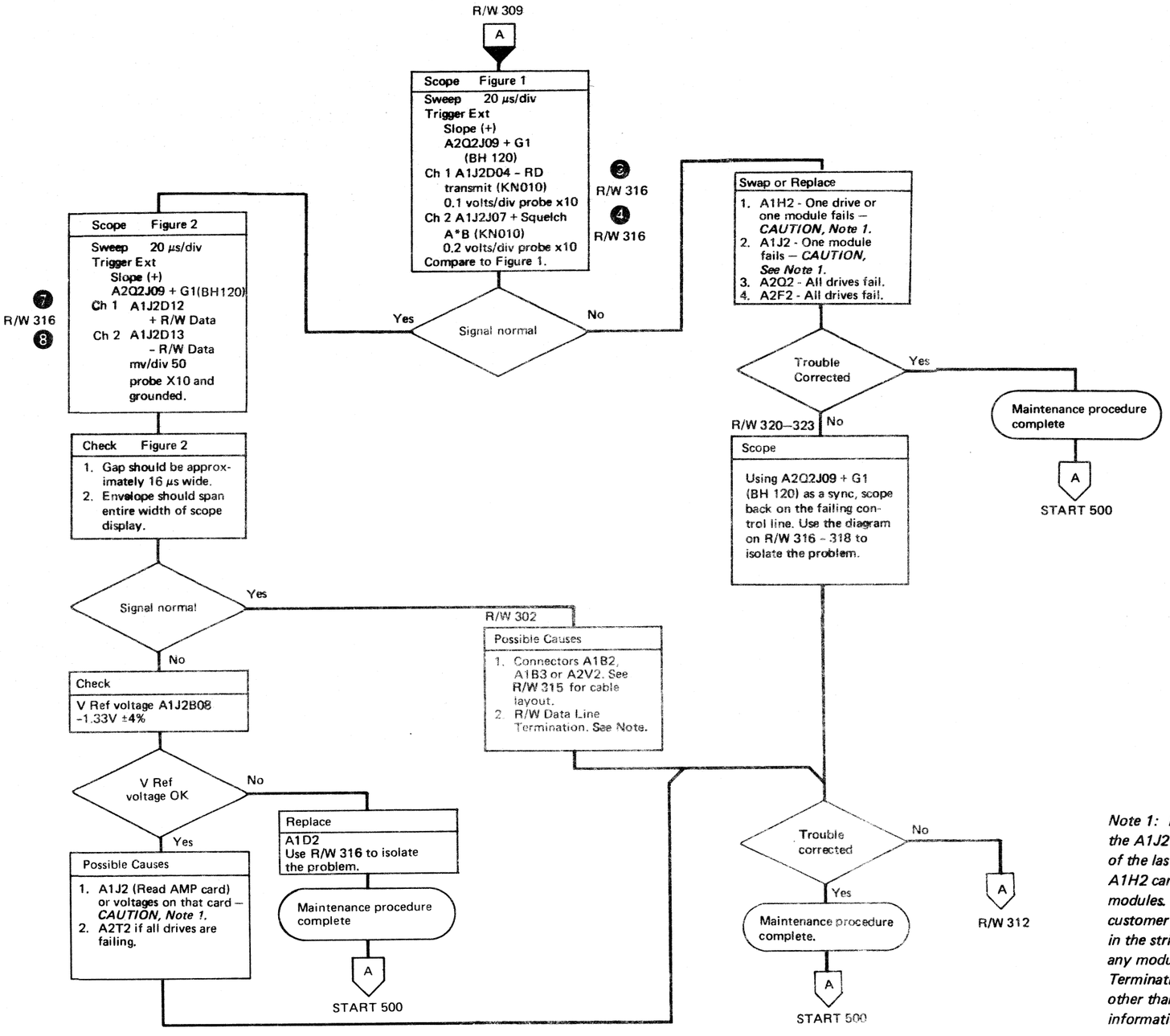


Figure 1 - Read Amplifier Controls

Ch 1 A1J2D04 KN010 — Read Transmit
Ch2 A1J2J07 KN010 + Squelch A*B

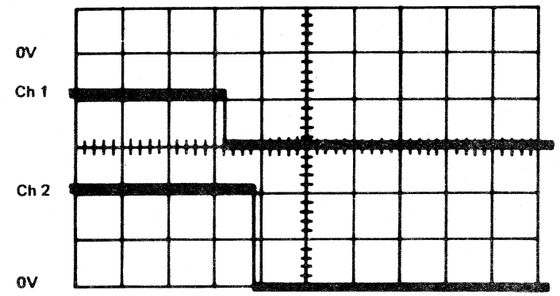
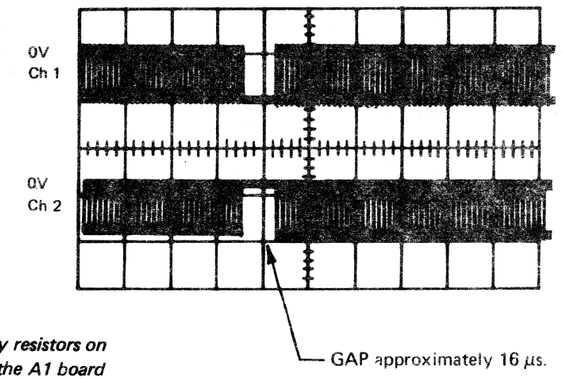


Figure 2 - R/W Data at Output of Read Amplifier

Ch 1 A1J2D12 + R/W Data 50 mv/div probe X10
Ch 2 A1J2D13 - R/W Data 50 mv/div probe X10

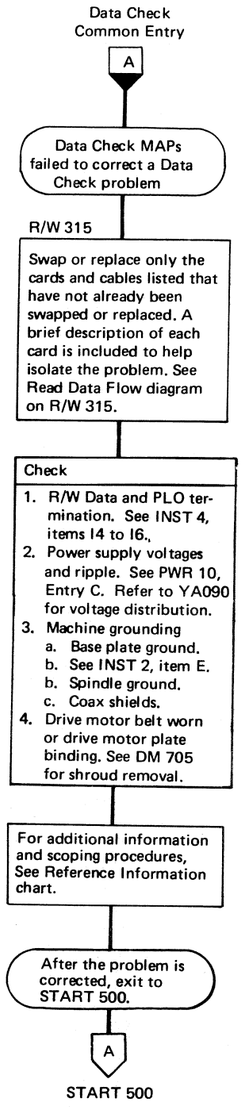


Note 1: R/W and PLO signals are terminated by resistors on the A1J2 and A1H2 cards through jumpers on the A1 board of the last module in the string. Removal of the A1J2 or A1H2 cards in the last module causes R/W failures in other modules. As a precaution to prevent data checks, the customer should be prevented from using any of the drives in the string while these cards are removed or replaced in any module, even though power is turned off in that module. Terminating jumpers should not be installed in any module other than the last module in the string. For jumper information, refer to INST 4 and ALD page KN 010.

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DATA CHECK – NO TROUBLE FOUND



1. R/W Matrix Card: This card contains the head selection matrix and read preamplifiers. The normal failure mode is one drive fails. However, the outputs of the R/W Matrix cards in any one module are Dot ORed together and certain types of failures in one card can cause both drives to fail. See R/W 309, Figures 1 and 2, to scope data output.

2. A1J2: This card contains the read amplifier for both drives in one module. The normal failure mode is one module fails. However, the output of the read amplifier is Dot ORed on the data cable with the output of the read amplifiers in the rest of the modules on the string; certain failures in one read amplifier can cause the others to fail. See R/W 308, Figures 1 and 2, to scope data output.

3. A1H2: This card develops the control lines for the R/W Matrix card and the read amplifier card. The normal failure mode is either one drive or both drives in one module fail.

4. A1F2(E2): These cards contain the Head Address Registers (HARs) for their respective drives and are interchangable. The normal failure mode is one drive fails. These cards are tested with microdiagnostic A2; unless the failure is intermittent, it is unlikely that these cards are at fault.

5. A2T2: This card contains the read line receivers, the VFO, the PLO, and the Bit Ring. The normal failure mode is all drives in the string fail.

6. A2S2: This card contains the SERDES Register, the Data Register, and various ECC controls. The normal failure mode is all drives in the string fail.

7. A2Q2: This card provides read/write controls for the controller and the selected drive. The normal failure mode is all drives in the string fail.

8. A2F2: This card contains the Bus Out Assembler, and transmits read/write controls to the selected drive over Device Bus Out. The normal failure mode is all drives in the string fail.

9. A2P2: This card contains the Gap Counter which provides timing for Read and Write operations. The normal failure mode is all drives in the string fail.

10. A2R2: This card contains the ECC Shift Register. It does not cause a No Sync Found indication. The normal failure mode is all drives in the string fail with ECC Data Checks.

11. A1R4(Q4): These cards contain the servo logic for their respective drives and are interchangeable. Certain failures in this card can cause the servo to drift off track and cause Data Checks. The normal failure mode is one drive fails. Before changing this card, go to ACC 701, Entry A.

12. Cables and Connectors:
    a. R/W Matrix card to data module connector. See R/W 350.
    b. R/W Matrix card to A1Y4(Y3)/A1Z2(Z1). See R/W 204.
    c. Read/Write Data and PLO cable between modules. Connectors: A1B2, A1B3, and A2V2. See Figure 1 on R/W 306.
    d. Servo cable between data module connector and A1V2(U2). An open or intermittent failure in this cable may cause off-track problems or noise that results in Data Checks rather than servo errors. See ACC 440, Entry A, and diagrams on R/W 350 and 352.

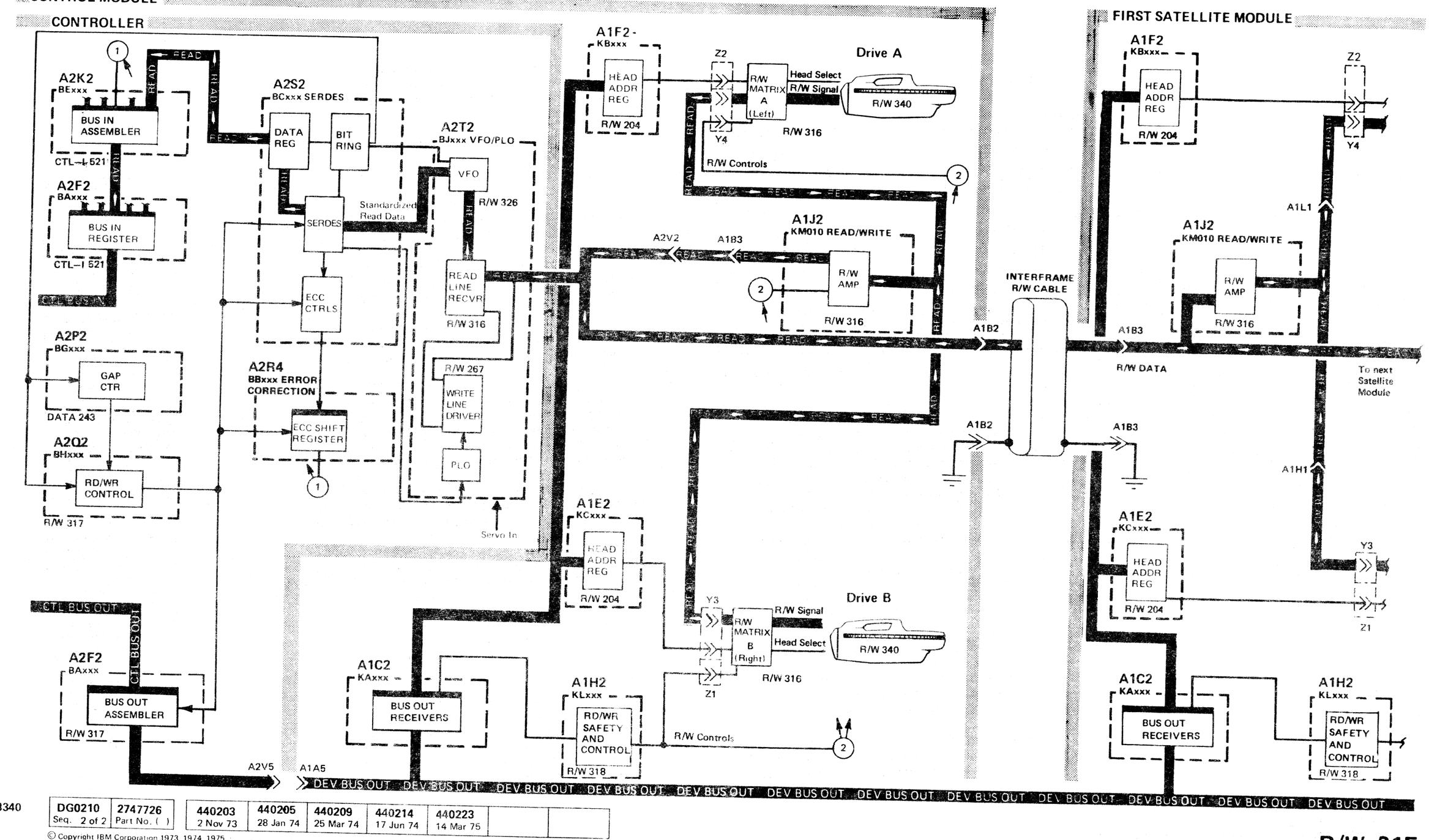
Reference Information

Description	MLM Page
Data Module Scoping Procedure	R/W 347
Data Module Disk Surface Layout	OPER 10–12
Diagrams, Read Operation	R/W 315–318
Physical Address Conversion	R/W 343–346
Read Operation Description	OPER 230–233
Read Home Address	R/W 320–323
Scoping Procedure for Read Operation	MICFL 1193–1195
Set Read/Write Description	OPER 213–217
Track Format	OPER 20–21
VFO Error Signal Analysis	R/W 326

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READ DATA FLOW

See R/W 320–323 and OPER 230–233 for Read Operation Description.



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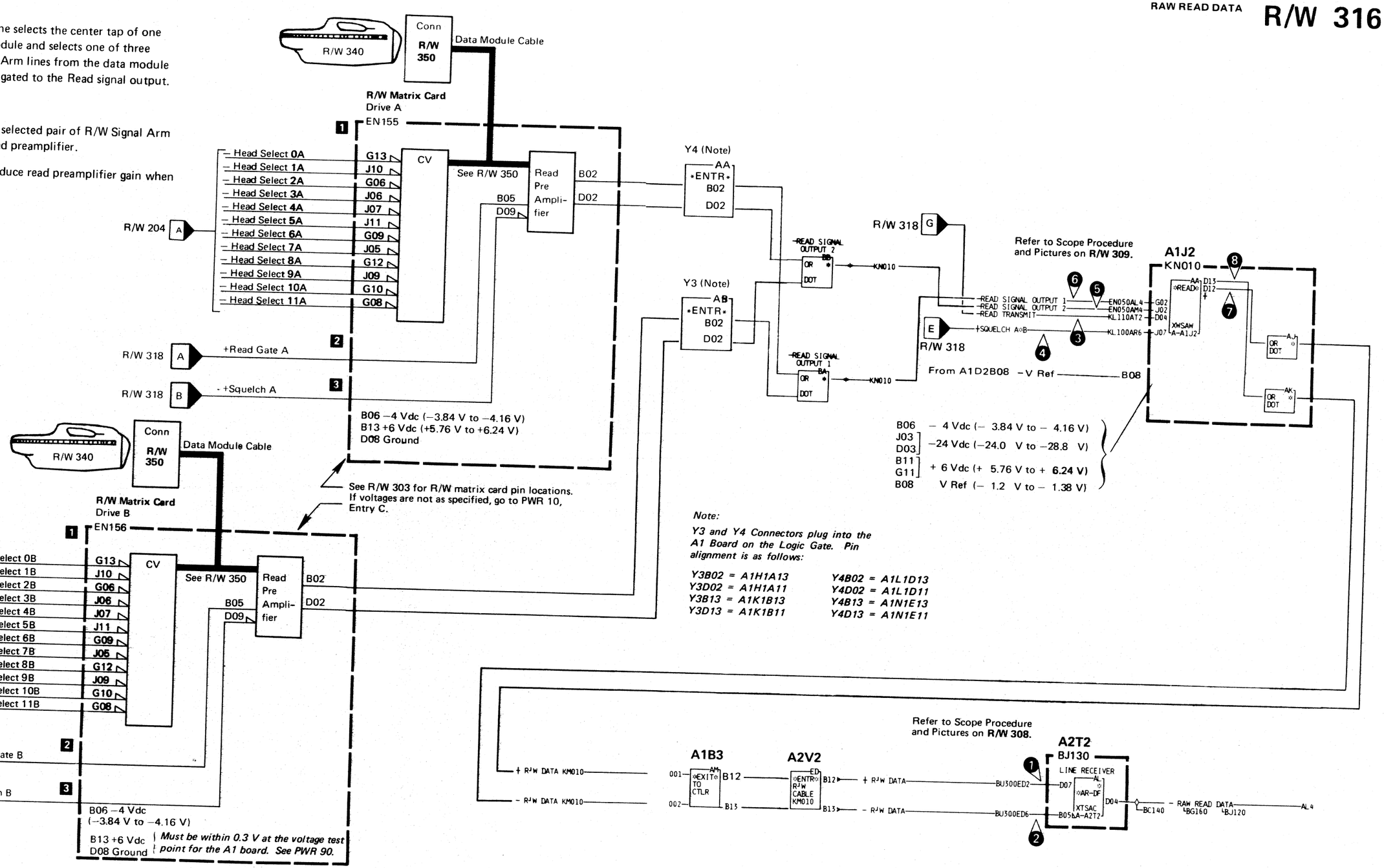
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RAW READ DATA

1 Each Head Select line selects the center tap of one head in the data module and selects one of three pairs of R/W Signal Arm lines from the data module to be amplified and gated to the Read signal output. See R/W 352.

2 Read Gate gates the selected pair of R/W Signal Arm lines through the read preamplifier.

3 Squelch is used to reduce read preamplifier gain when not reading.

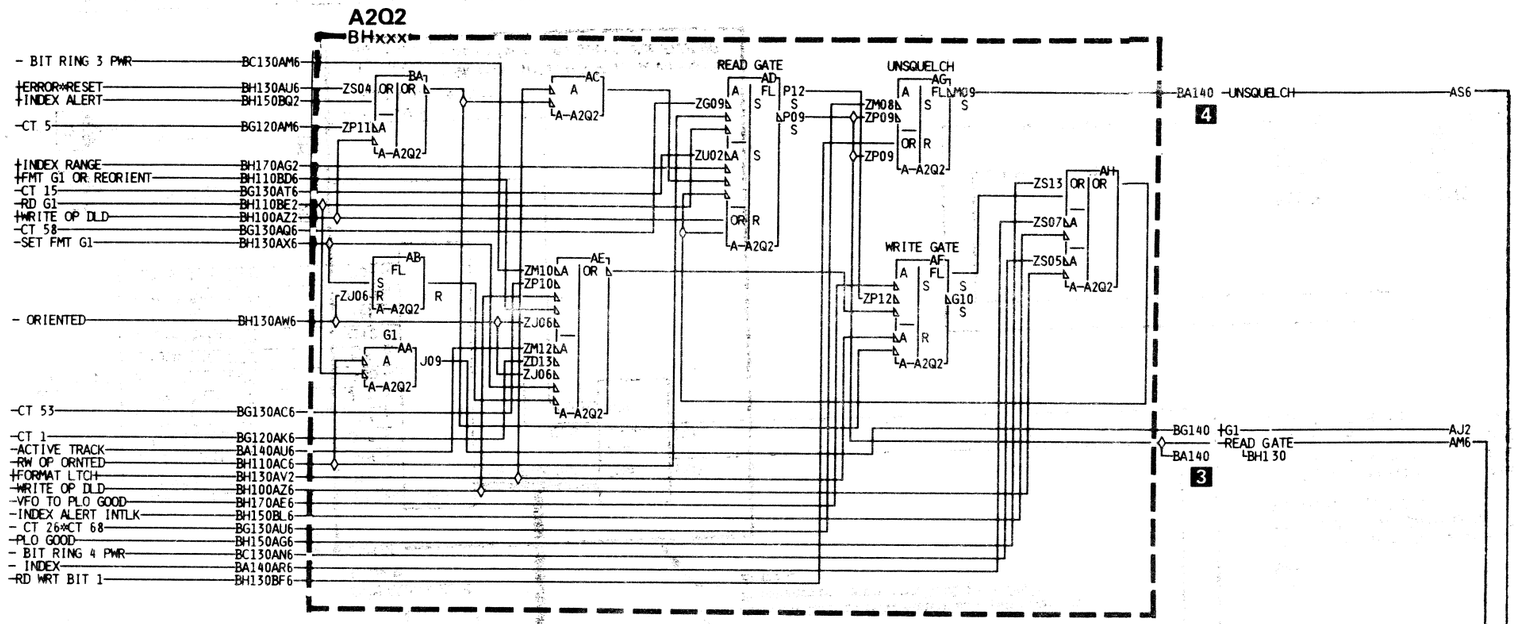


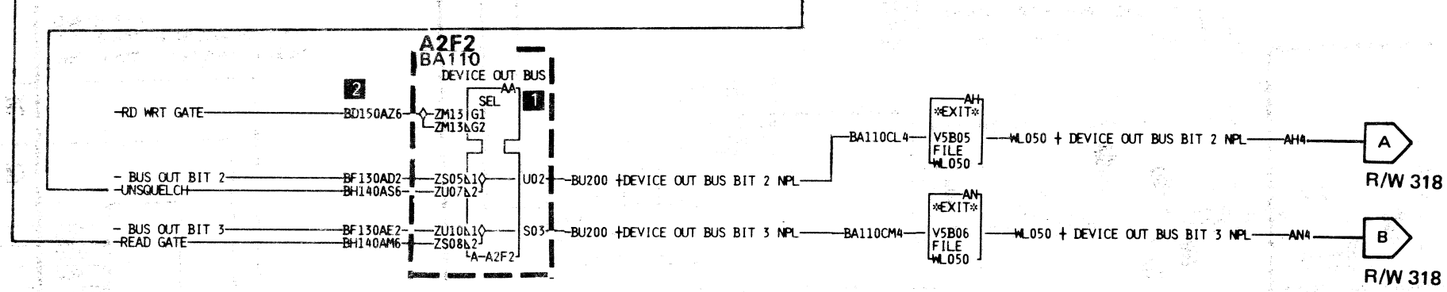
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READ CONTROLS





1 Device Outbus is used to transfer Read/Write controls over the Device Interface during Read and Write operations. Device Outbus parity checking is suspended. Refer to DEV-I 128-130.

2 Read/Write Gate transfers Device Outbus to a Read/Write control bus. Read/Write Gate is the result of a Set Read/Write operation (Tag '85'). After being activated it does not reset until a Reset Read/Write operation is initiated (Tag '05').

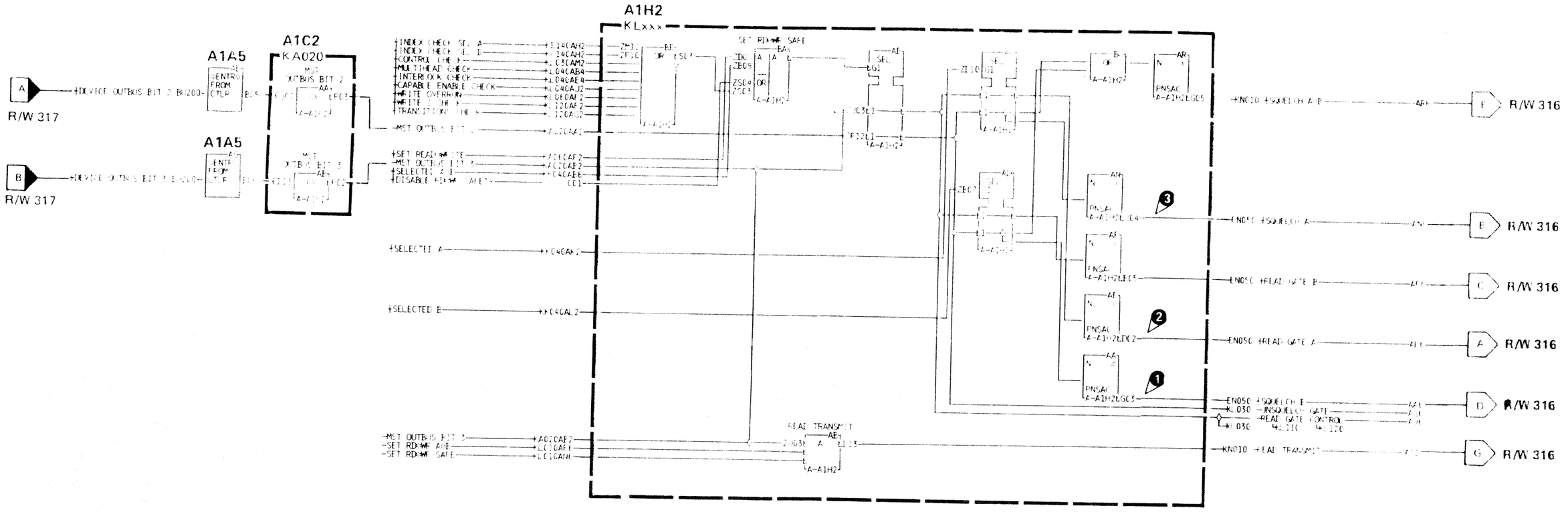
3 Read Gate is used to gate Raw Read Data through the R/W matrix card and the read amplifier to the controller. Refer to R/W 320 and 323 for timings on a Read Home Address operation.

4 Unsquelch is used to drop Squelch to the read amplifier and the R/W matrix card. Squelch is used to reduce the gain of the read amplifier and read preamplifier when not reading. This prevents Read/Write control switching transients from overdriving the amplifiers.

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READ CONTROLS R/W 318



B06, G06, M06, S06	−4Vdc (−3.84V to −4.16V)
B11	+6Vdc (+5.76V to +6.24V)

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440203 2 Nov 73	440204 21 Dec 73	440209 25 Mar 74	440214 17 Jun 74			

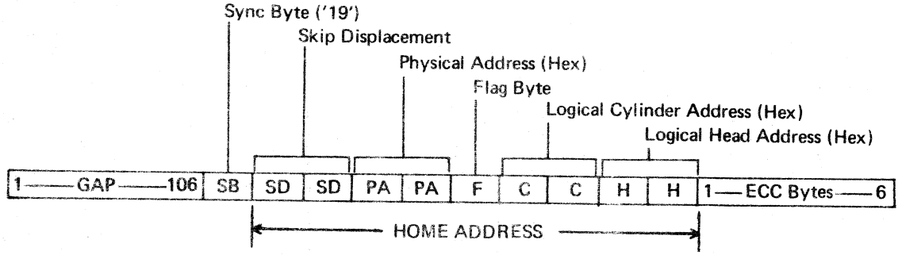
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READ HOME ADDRESS (READ G1 - TAG '0E' BUS '49')

This is a description of a Read G1 operation as it is used in microdiagnostic routine AF, test 01.

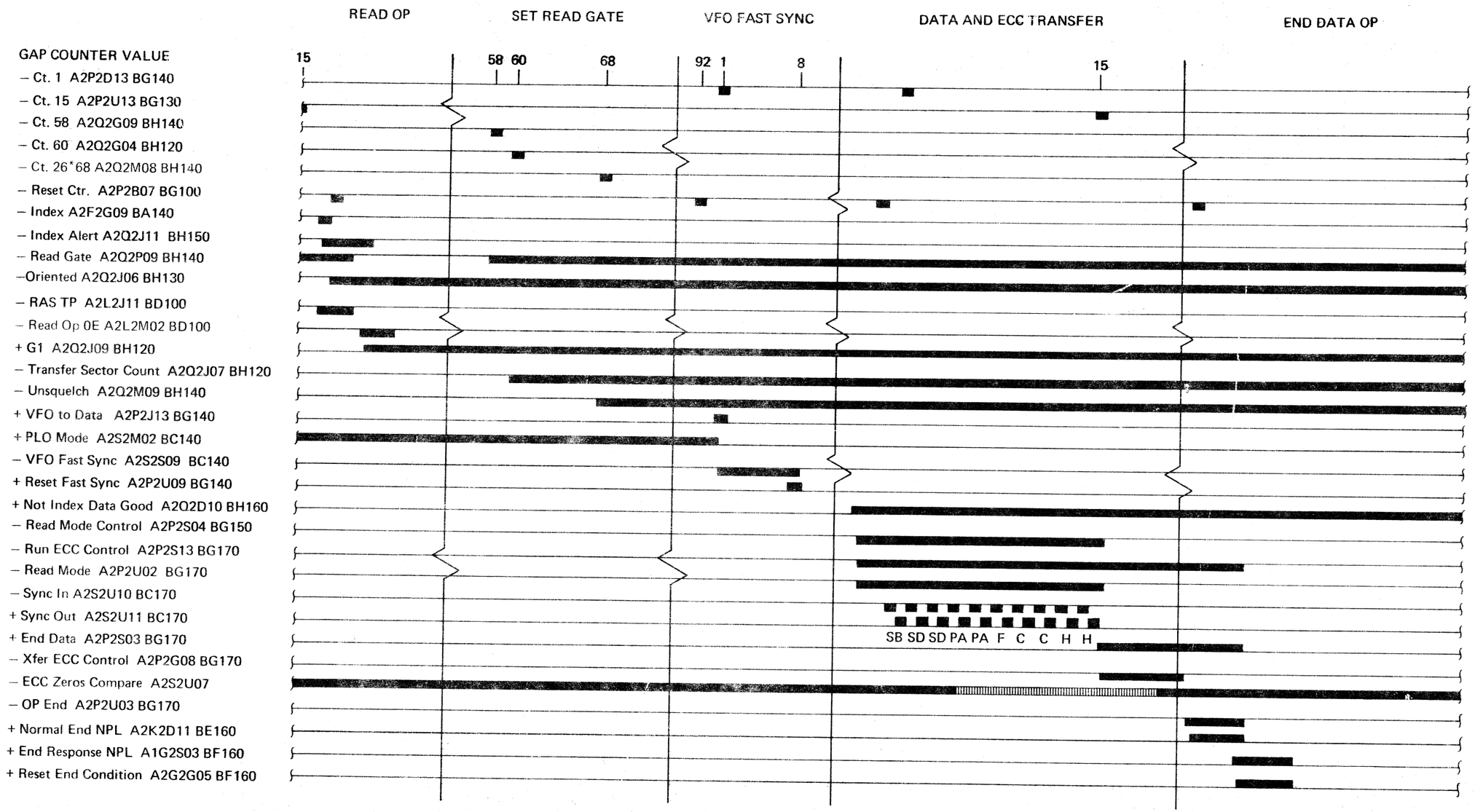
See OPER 230–233 for a general description of a Read operation.

1. Before the Read G1 tag is executed, the CE drive is selected (Tag '83' Bus '10') and a Set Read Write (Tag '85') is issued.
2. As soon as the drive is oriented (Index and Active Track), the Gap Counter is reset and the microdiagnostic issues a Sync Tag (Tag '0B') to aid scoping.
3. The microdiagnostic issues the Read G1 Tag (Tag '0E' Bus '49') . The 9 in Bus Out bits 4 through 7 is the Modulo count (units position of the byte count). This indicates that 9 data bytes are to be transferred.
4. At Count 58 time the controller raises Read Gate to the drive.
5. At Count 68 time the controller raises Unsquelch to the drive.
6. At Count 92 time the Gap Counter is reset to zero.
7. At Count 1 time the VFO is locked to data and put in Fast Sync Mode.
8. At Count 8 time Fast Sync is reset and the hardware starts looking for a sync byte in SERDES (Hex '19').
9. After the sync byte is detected, Data Good is raised. This indicates that the next byte entering SERDES is a data byte. If no sync byte is detected by Count 21 time, the G1 Retry Latch (BG 140) is set to allow for a possible skip defect. At Count 128 time the Gap Counter is reset to zero. VFO is locked to data again and if a sync byte is not detected by Count 21 time, a Check End condition with a No Sync Byte Found indication results.
   See OPER 43 for additional information on the Sync Byte.
10. Read Mode, Run ECC, and Run Modulo are raised and the Gap Counter is again reset to zero.
11. The Gap Counter is set to the inverted Modulo Count, which in this case is 6 (see number 3). The sync byte is placed on Bus In and Sync In is sent to the Storage Control.
12. Sync Out is returned from the Storage Control.
13. Nine more Sync In and Sync Out cycles transfer the Home Address to the Storage Control. The data transfer is ended when the Gap Counter equals 15.
14. End Data and Transfer ECC come up and Read Mode is dropped.
15. The six ECC bytes are transferred to the ECC Shift Register. If ECC Zeros Compare is active after the six ECC bytes are transferred, ECC Data Check is blocked.
16. Op End is raised and Normal End is sent to the Storage Control. If ECC Data Check was not blocked (see number 15), Check End, Command Overrun (Bus In bit 0) and ECC Data Check (Bus In bit 3) are sent to the Storage Control instead.
17. End Response is returned from the Storage Control.
18. Reset End Condition is raised in the Controller.



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READ HA TIMING CHART



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VFO ERROR SIGNAL ANALYSIS

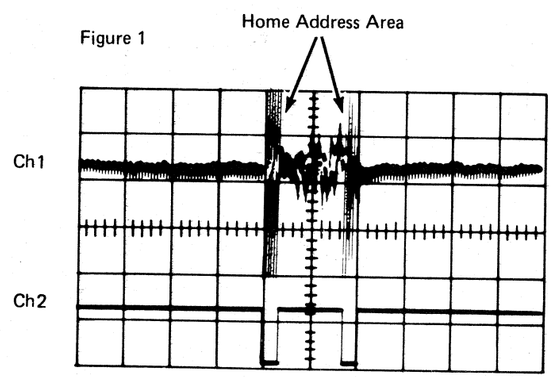
The purpose of scoping the VFO Error Signal is to determine if the VFO is the cause of a Read Data problem in the controller.

The VFO Error Signal should be scoped only after Read Data has been scoped at the receivers in the controller and is determined to be good in accordance with the scope pictures on R/W 308.

Loop routine AF, test 01.
1. Load routine AF
2. Enter: 10,01,01,01,00.

Scope:
Sweep 20 µs/div
Trigger
Slope (+)
Ext.
A2Q2J09(BH120)
(G1)
Ch 2: A2T2G05
(–VFO Fast Sync)
Volts/div 0.1 V
Probe X10 and grounded.

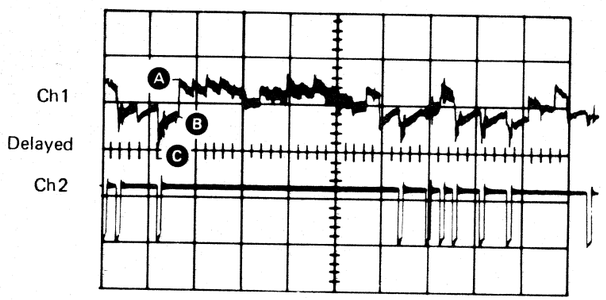
Figure 1



Analysis:
Refer to Figure 1 and notice the two fast sync bursts. The first burst is due to the fast sync that occurs when VFO is locked to data before the Home Address is read. The second burst is due to the fast sync that occurs when VFO control is returned to the PLO after the Home Address is read.

Using delayed sweep, expand the Home Address portion of the trace between the two fast sync bursts (Figure 2). The peak voltage at this time should not exceed ± 1 volt from ground reference. The peak-to-peak voltage of any one transition of the VFO error signal should not exceed 150 mV. An example at a transition is between Ⓐ and Ⓑ but not between Ⓐ and Ⓒ.

Figure 2



–Same as Ch1 above except delayed sweep is used and the Home Address area is expanded.

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DATA MODULE FAILURE

CAUTION
When the data module door is open, cleanliness is extremely important. Do not smoke or allow particles of any kind to enter the data module. The data module disk surfaces are lubricated. Do NOT *clean them.*

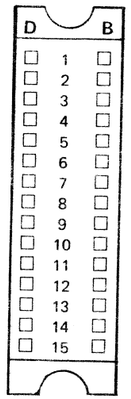
READ/WRITE HEAD CONTINUITY SERVICE CHECK

Use CE meter P/N 452796 or equivalent.

1. Locate failing R/W Head or Arm assembly on plug chart.
2. Take forward, reverse, and ground resistance readings at points indicated on DM connector.
   a. Forward resistance: Connect meter Ω– to a R/W signal line and then connect Ω+ to each head select for that Head Arm. Repeat with the Ω– connected to the second R/W signal. Normal forward resistance is 15 to 50 ohms.
   b. Reverse resistance: Repeat step above with meter leads reversed. Normal reverse resistance is infinity on the RX1 scale.
   c. Normal resistance between DM frame ground and any connector pin, except U10, D11, D12, and B12, is infinity on the RX1000 scale.
3. If an abnormal reading is obtained in Step 2, remove the DM connector mounting screws and pull the connector forward until the plugs on the rear side are accessible.
4. Remove the plug for the failing R/W Head Arm assembly and remake the resistance check through the plug contacts.
5. A normal resistance reading in Step 4 indicates a defective DM connector.

DATA MODULE CONNECTOR PLUG CHART

View as seen looking through data module door.



See R/W 350

R/W Head Arm 3 Plug

Not used on Model 35

R/W Signal Arm 3	1		R/W Signal Arm 3
Head Select 11	2		Head Select 10
Head Select 9	3		Head Select 8

R/W Head Arm 2 Plug

R/W Signal Arm 2	4		R/W Signal Arm 2
Head Select 7	5		Head Select 6
Head Select 5	6		Head Select 4

R/W Head Arm 1 Plug

R/W Signal Arm 1	7		R/W Signal Arm 1
Head Select 3	8		Head Select 2
Head Select 1	9		Head Select 0

Electrical Connector Pin No.

Note: Servo Arm and Interlock plugs are not shown.

R/W 300
R/W 309

A

Problem was isolated to a data module by running OLTs, microdiagnostics, or by analysis of error log data.

Check

Open the data module door and visually inspect the data module for:
1. Bent or broken electrical connector pins.
2. Disk surface damage or metal particles that may indicate head-to-disk interference. Do not attempt to clean disk surfaces.
3. Loose, broken, or worn parts on or near carriage.

CAUTION
When the data module door is open, cleanliness is extremely important. Do not smoke or allow particles of any kind to enter the data module. The data module disk surfaces are lubricated. Do NOT *clean them.*

Defect observed

Item 1

Repair or Replace

Electrical connector. See DM 870 and R/W 350.

Test data module on drive with the failing program, OLT, or microdiagnostic.

Trouble corrected

Yes

No

Items 2 or 3

No

R/W 343

Determine if failures are common to one logical track, one physical head, or one physical head arm by doing one or more of the following and refering to R/W 343:
1. Run OLTs T3340 PSA and T3340 PSB. Note 1.
2. Examine error log data.
3. Run microdiagnostic routine B1. Note 2.

Data Check Problem

No

Yes

Unit is not field repairable. Advise customer and handle according to existing procedures.

Maintenance procedure complete.

A

START 500

A

R/W 347

Single track failure

Yes

Advise customer so that track may be flagged and an alternate assigned.

No

Single physical head or 2 or more heads on same arm fail

No

Yes

Perform continuity service check on failing head or head arm assembly. See connector plug chart on left.

Electrical connector defective

No

Yes

Repair or Replace

Electrical connector. See DM 870 and R/W 350.

Test data module on a drive with the failing program, OLT, or microdiagnostic.

Trouble corrected

No

Yes

Maintenance procedure complete.

A

START 500

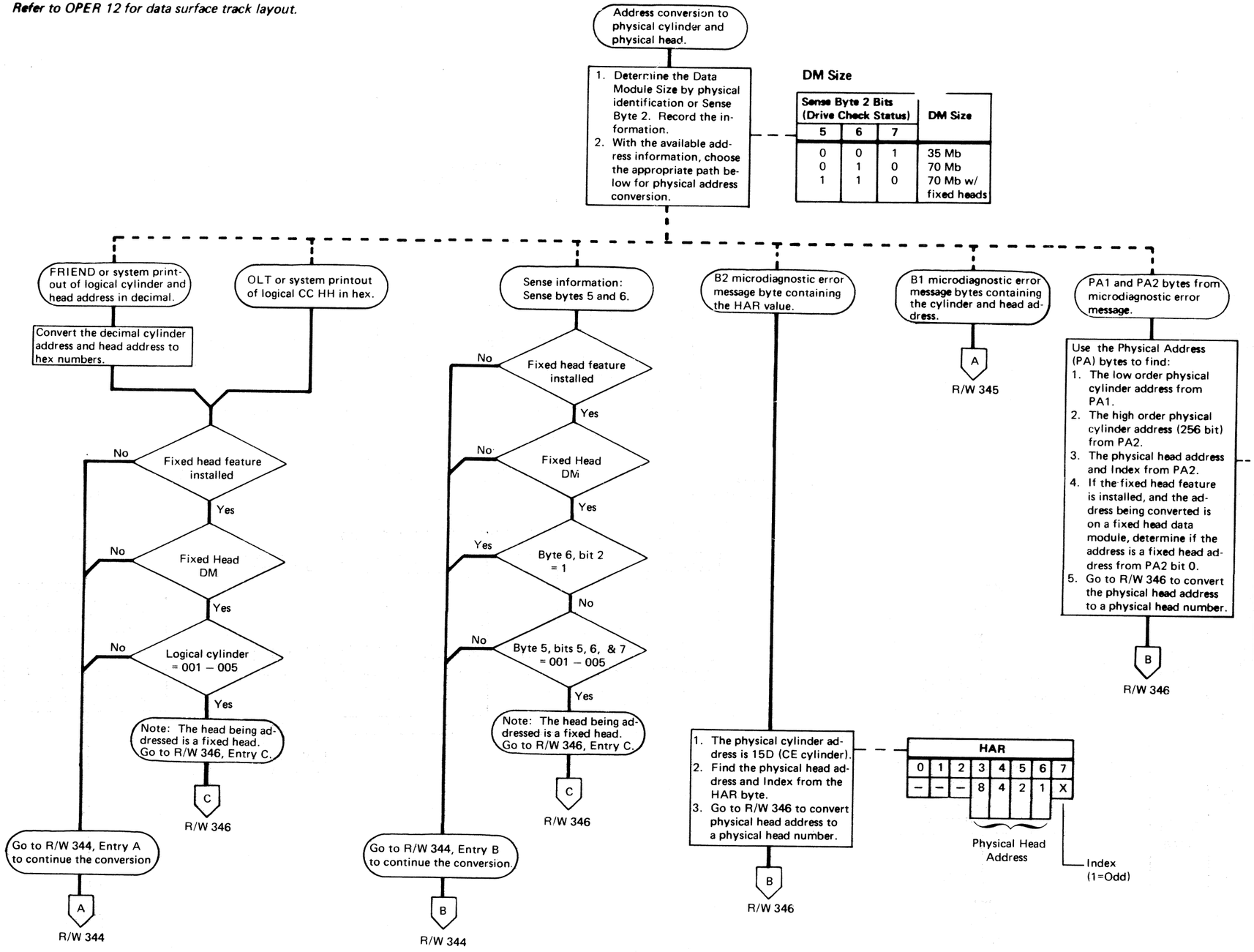
Note 1:
OLT T3340 PSA reads all customer home address and R0 fields on the data module. The CCHH bytes of the Home Address are compared to the CCHH bytes of R0 and an error summary is printed upon completion. OLT T3340 PSB reads all customer records and prints an error summary upon completion. See the OLT section of the MLM for information and instructions. If the host system is a System/3 Model 15, refer to the System/3 Diagnostic Users Guide for OLT information and instructions.

Note 2:
Routine B1, running in default mode, reads the home address and all records on the even CE cylinders using all physical heads. By entering parameters, any customer cylinder and head may be selected and checked for errors. See MICRO 34. (If the problem is unique to one CE track, initialize the track again, using Routine B0.)

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ADDRESS CONVERSION

Refer to OPER 12 for data surface track layout.

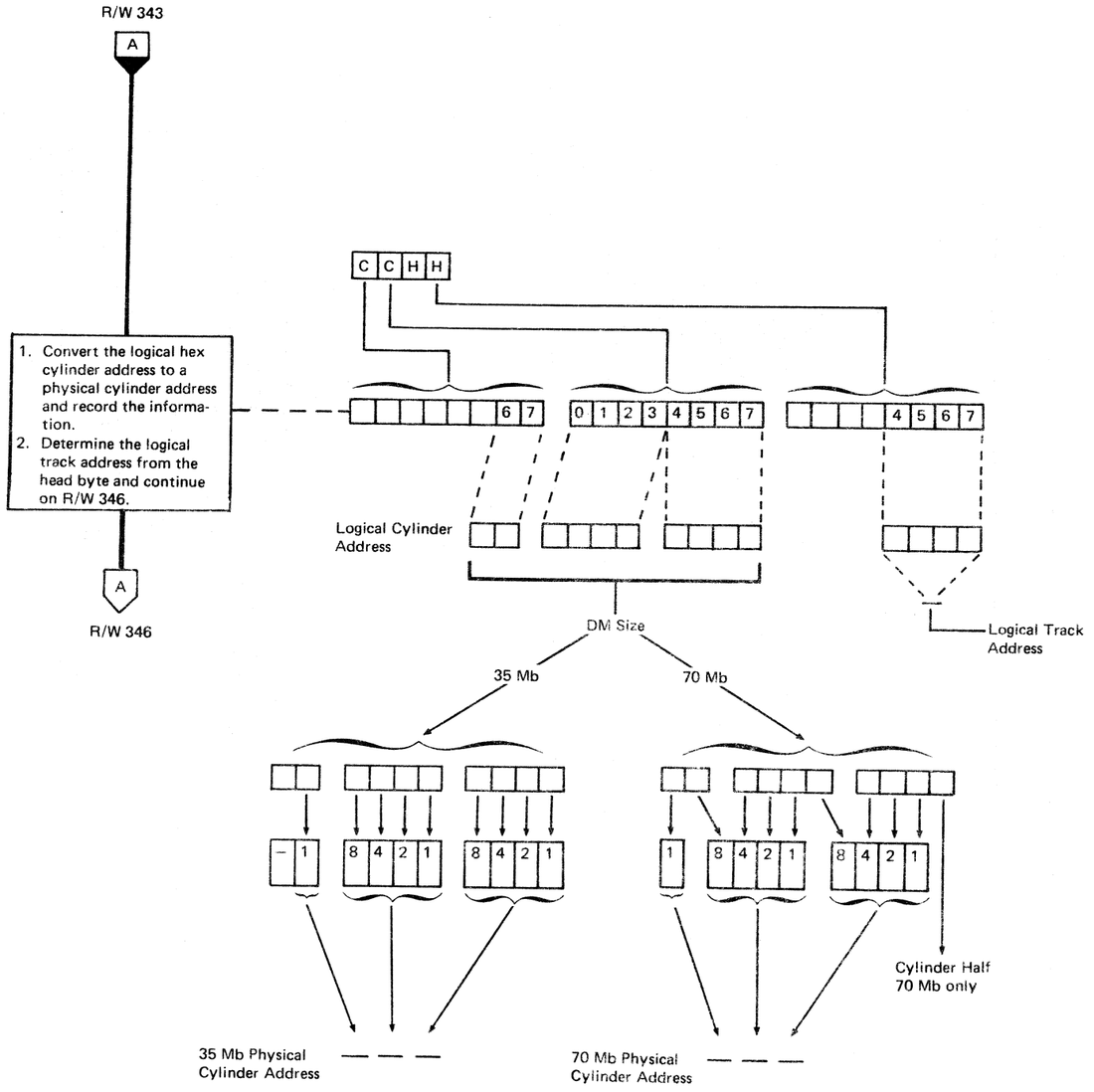


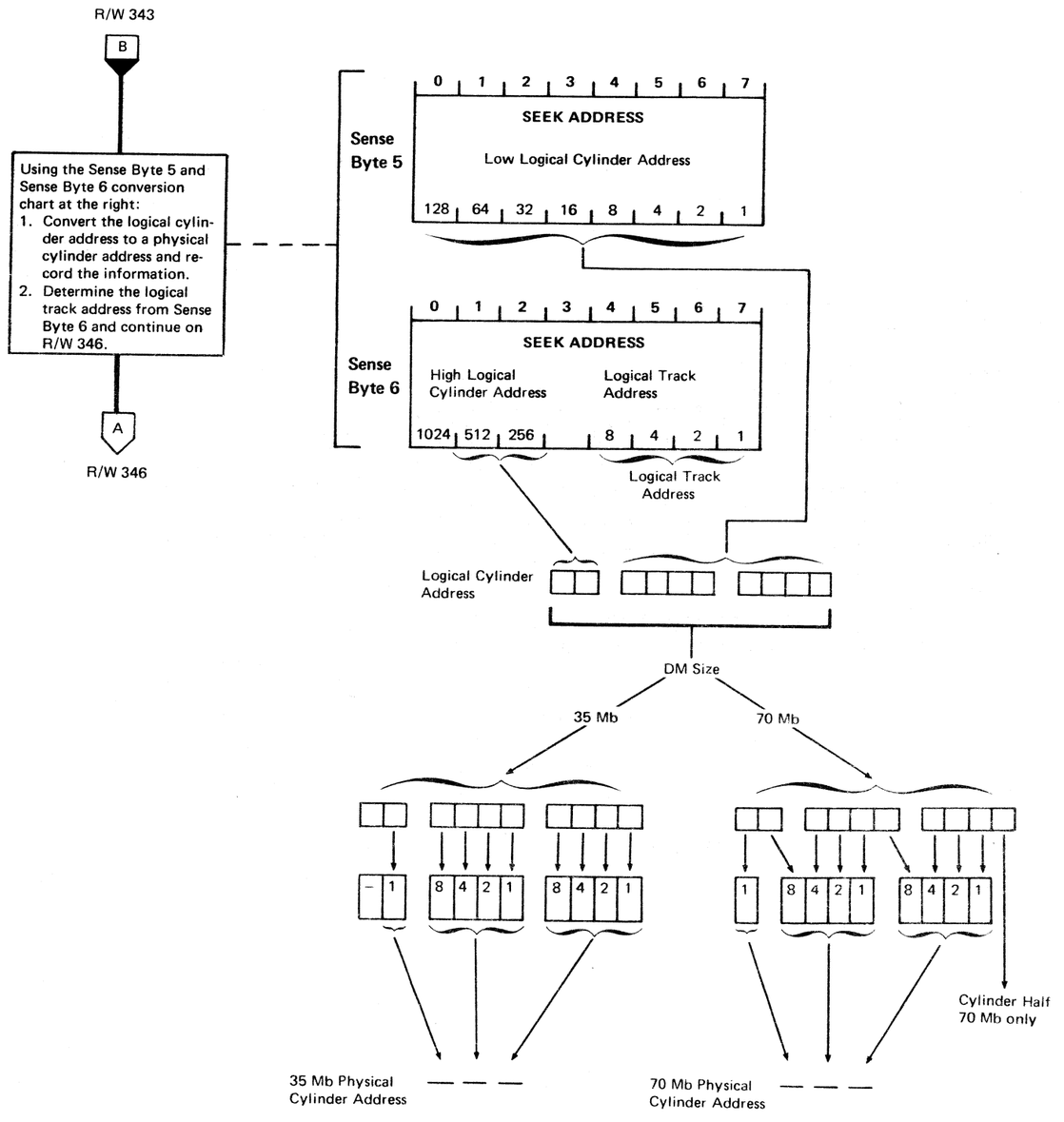
PHYSICAL ADDRESS (PA) BYTES

- Are recorded on the disk in the HA and count fields.
- Are used for seek verification.
- Are not directly retrievable at the system level.
- Are retrieved by the microdiagnostics for display on seek verification errors.

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ADDRESS CONVERSION (Continued)



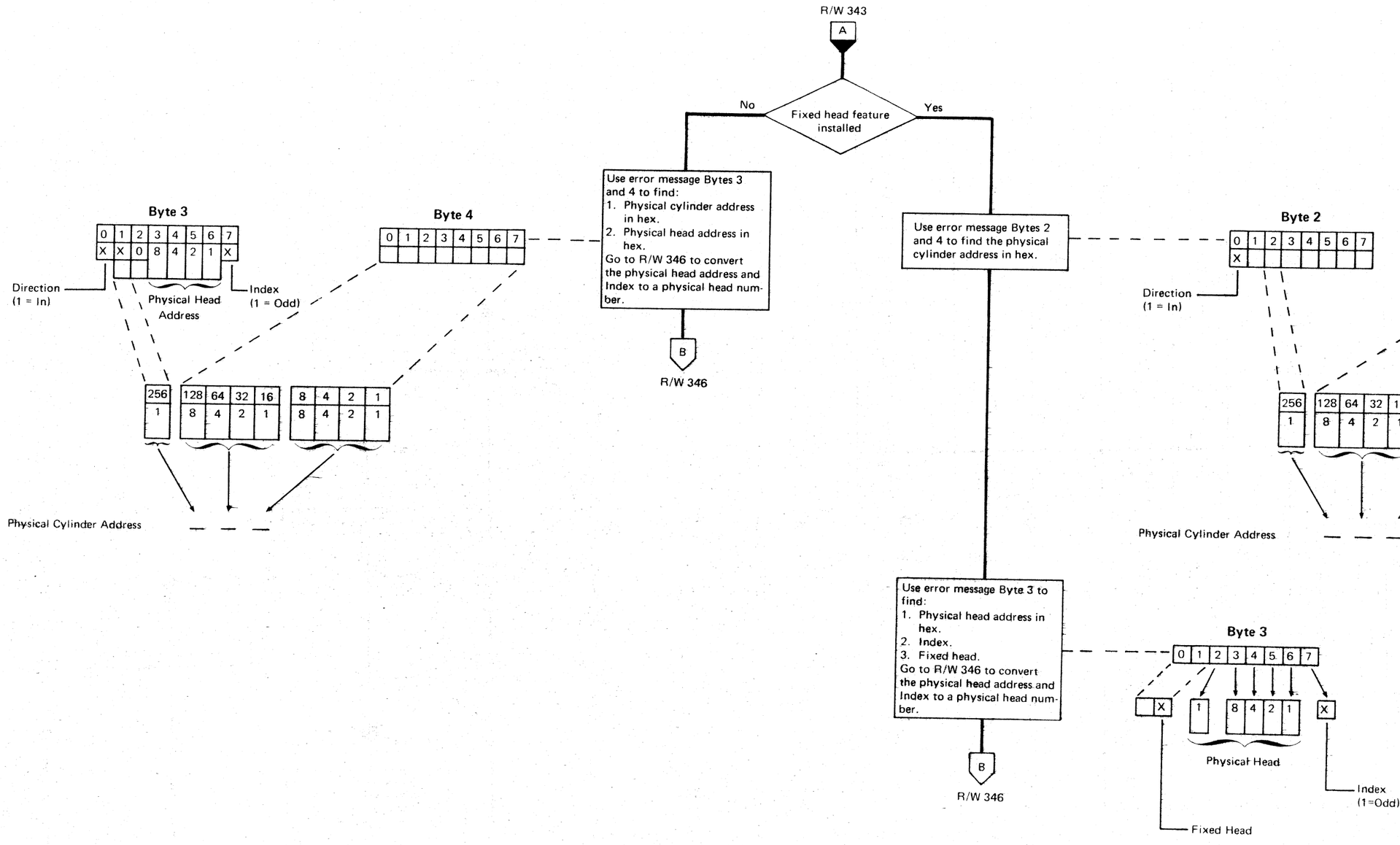


DG0260	2747731
Seq. 2 of 2	Part No. ( )

440203	440204	440209	440214			
2 Nov 73	21 Dec 74	25 Mar 74	17 Jun 74			

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ADDRESS CONVERSION (Continued)



DG0261	2747893	440214						
Seq. 1 of 2	Part No. ( )	17 Jun 74						

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ADDRESS CONVERSION (Continued)

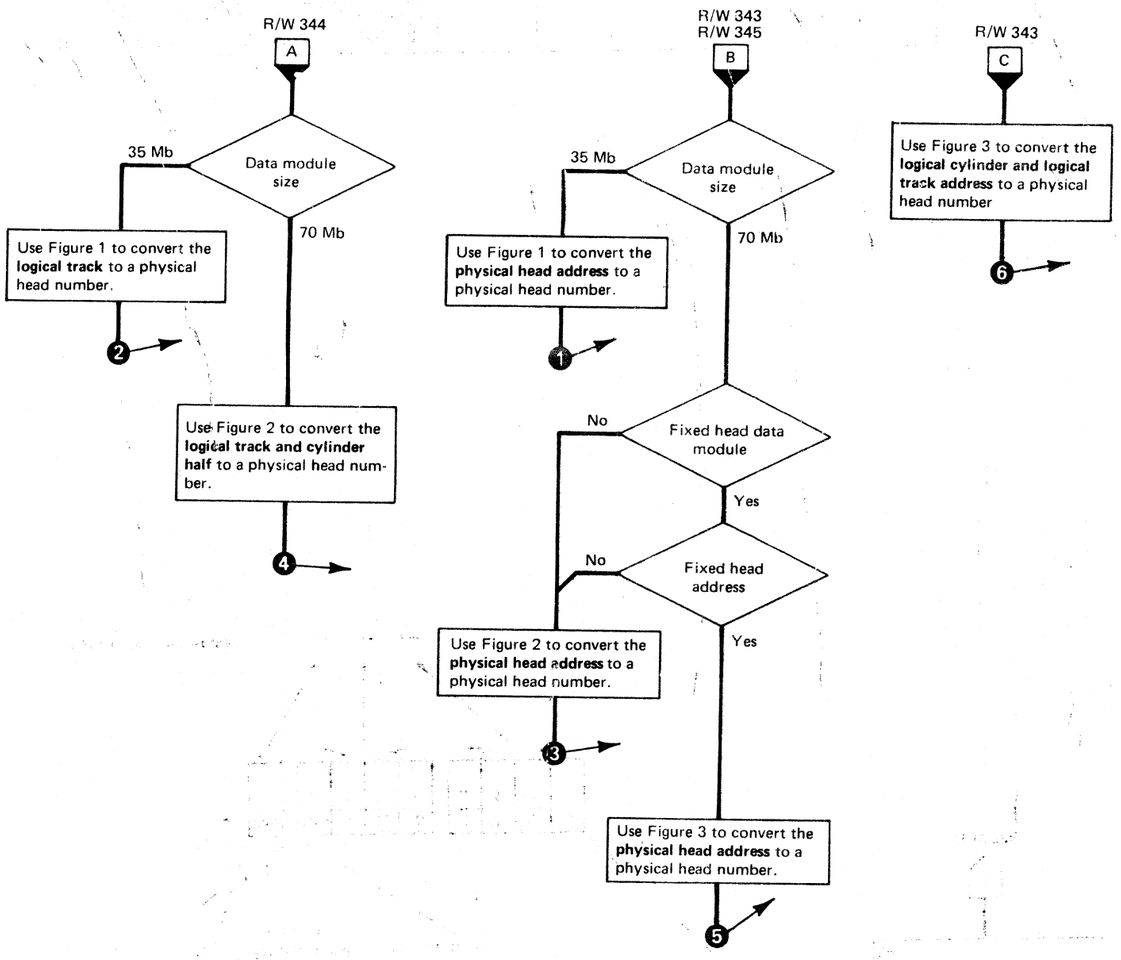


FIGURE 1 – 35 MB

1 Physical Head Addr. (Hex)	2 Logical Track	Physical Head No.	Index
00	00	0	Even
01	01	0	Odd
02	02	1	Even
03	03	1	Odd
04	04	2	Even
05	05	2	Odd
06	06	3	Even
07	07	3	Odd
08	08	4	Even
09	09	4	Odd
0A	0A	5	Even
0B	0B	5	Odd

FIGURE 2 – 70 MB

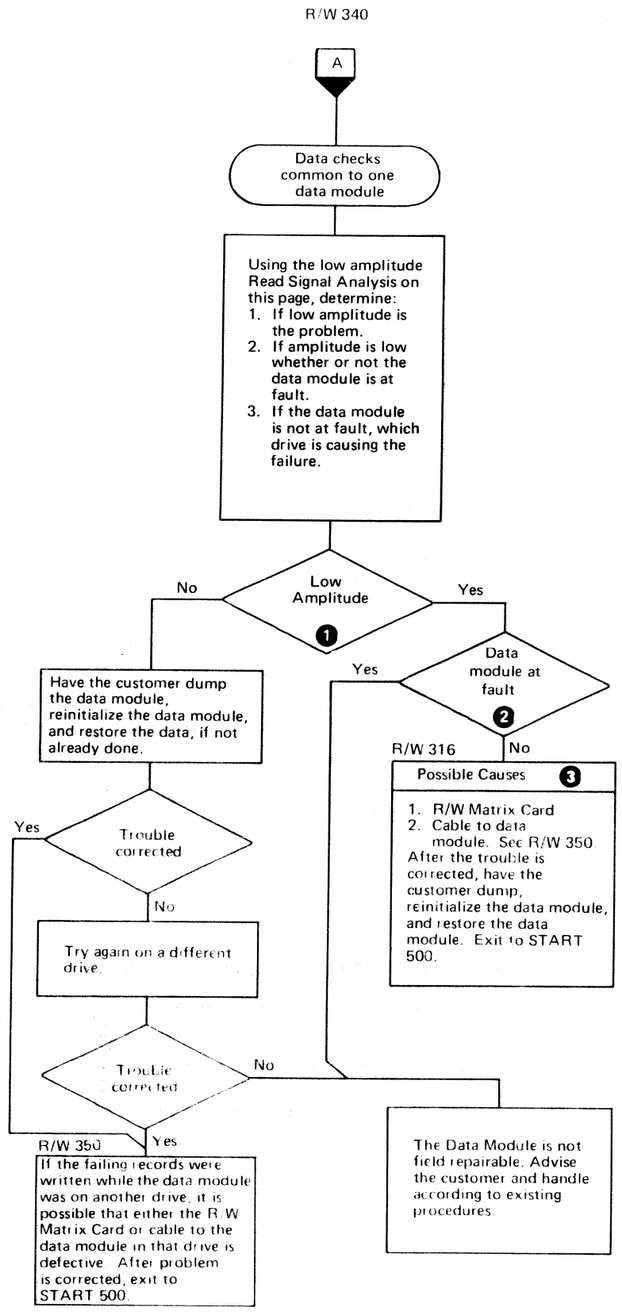
3 Physical Head Addr. (Hex)	Cylinder Half	4 Logical Track	Physical Head No.	Index
00	0	00	0	Even
00	0	01	0	Odd
01	0	02	1	Even
01	0	03	1	Odd
02	0	04	2	Even
02	0	05	2	Odd
03	0	06	3	Even
03	0	07	3	Odd
04	0	08	4	Even
04	0	09	4	Odd
05	0	0A	5	Even
05	0	0B	5	Odd
06	1	00	6	Even
06	1	01	6	Odd
07	1	02	7	Even
07	1	03	7	Odd
08	1	04	8	Even
08	1	05	8	Odd
09	1	06	9	Even
09	1	07	9	Odd
0A	1	08	10	Even
0A	1	09	10	Odd
0B	1	0A	11	Even
0B	1	0B	11	Odd

FIGURE 3 – FIXED HEAD CHART

5 Physical Head Addr. (Hex)	6 Logical Cyl No.	Logical Track	Physical Head No.	Index
00		0	0	Even
00		1	0	Odd
01		2	1	Even
01		3	1	Odd
02		4	2	Even
02	001	5	2	Odd
03		6	3	Even
03		7	3	Odd
04		8	4	Even
04		9	4	Odd
05		A	5	Even
05		B	5	Odd
06		0	6	Even
06		1	6	Odd
07		2	7	Even
07		3	7	Odd
08		4	8	Even
08	002	5	8	Odd
09		6	9	Even
09		7	9	Odd
0A		8	10	Even
0A		9	10	Odd
0B		A	11	Even
0B		B	11	Odd
0C		0	12	Even
0C		1	12	Odd
0D		2	13	Even
0D		3	13	Odd
0E		4	14	Even
0E	003	5	14	Odd
0F		6	15	Even
0F		7	15	Odd
10		8	16	Even
10		9	16	Odd
11		A	17	Even
11		B	17	Odd
12		0	18	Even
12		1	18	Odd
13		2	19	Even
13		3	19	Odd
14		4	20	Even
14	004	5	20	Odd
15		6	21	Even
15		7	21	Odd
16		8	22	Even
16		9	22	Odd
17		A	23	Even
17		B	23	Odd
18		0	24	Even
18		1	24	Odd
19		2	25	Even
19		3	25	Odd
1A		4	26	Even
1A	005	5	26	Odd
1B		6	27	Even
1B		7	27	Odd
1C		8	28	Even
1C		9	28	Odd
1D		A	29	Even
1D		B	29	Odd

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SINGLE DATA MODULE READ FAILURE ANALYSIS



LOW AMPLITUDE READ SIGNAL ANALYSIS

❶ Using the read data envelope scoping prodedure, scope a failing head and cylinder to determine if the amplitude is low. See R/W 343 and R/W 345 to help determine failing head and cylinder. Whether or not the amplitude is low, it must be considered that the failure could have occurred when the record was written. If the amplitude is found to be low, continue analysis.

❷ By using one or more of the following methods, determine if the low amplitude is being caused by the data module.

a. Loop routine B1 several times with different cylinder and head values using the read data envelope scoping procedure on this page each time.

b. Write on the odd CE Tracks using routine B2 with default parameters. Read and scope the odd CE Tracks as appropriate, using the read data envelope scoping procedure. If low amplitude is found, try again on another drive until satisfied that the problem is or is not in the data module.

c. Unload the customer data and reinitialize the data module or use OLT TO 200 (FRIEND) to write on a failing track. Read and scope the appropriate tracks using the read data envelope scoping prodedure. If amplitude is low, try again on another drive until satisfied that the problem is or is not in the data module.

❸ If the data module is not at fault, either the amplitude on the track(s) has deteriorated or it was written at low amplitude. To check the write circuits in a drive, run routine B2 with default parameters on a data module that is known to be good. Use the read data envelope scoping prodedure to scope the odd CE Tracks and check the amplitude.

Note: If the CE Tracks have been destroyed, use micro-diagnostic routine B0 to restore them.

READ DATA ENVELOPE SCOPING PROCEDURE

❶ Loop microdiagnostic B1 on the desired head and cylinder. Refer to MICRO 34.

a. Load B1

b. Enter 10, XX, YY, FF, 00

XX = Low-order physical cylinder address in Hex (00 – 5D)

YY = Head address register value (00 - 57 where bit 1 is the high-order cylinder address bit).

❷ Scope output of R/W Matrix Card at input of read amplifier. Refer to diagram on R/W 316.

Sweep 1 ms/div

Trigger external A2Q2J09, + G1

Slope +

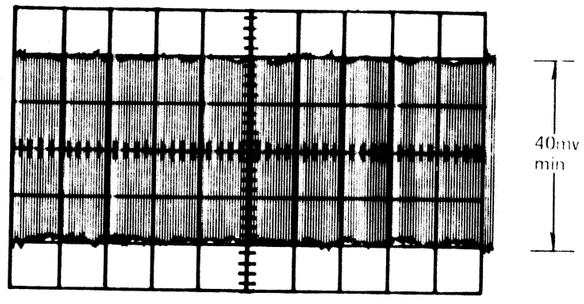
CH1: A1J2J02,read signal
20 mv/div, X1 grounded probe

CH2: A1J2G02, read signal
20 mv/div, X1 grounded probe

Mode added with CH2 inverted.

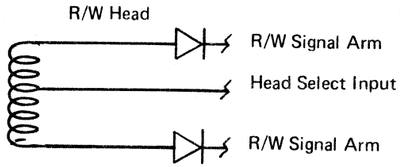
❸ The amplitude of the envelope should not drop below 40mv (See Figure 1).

Figure 1 Read Data Envelope



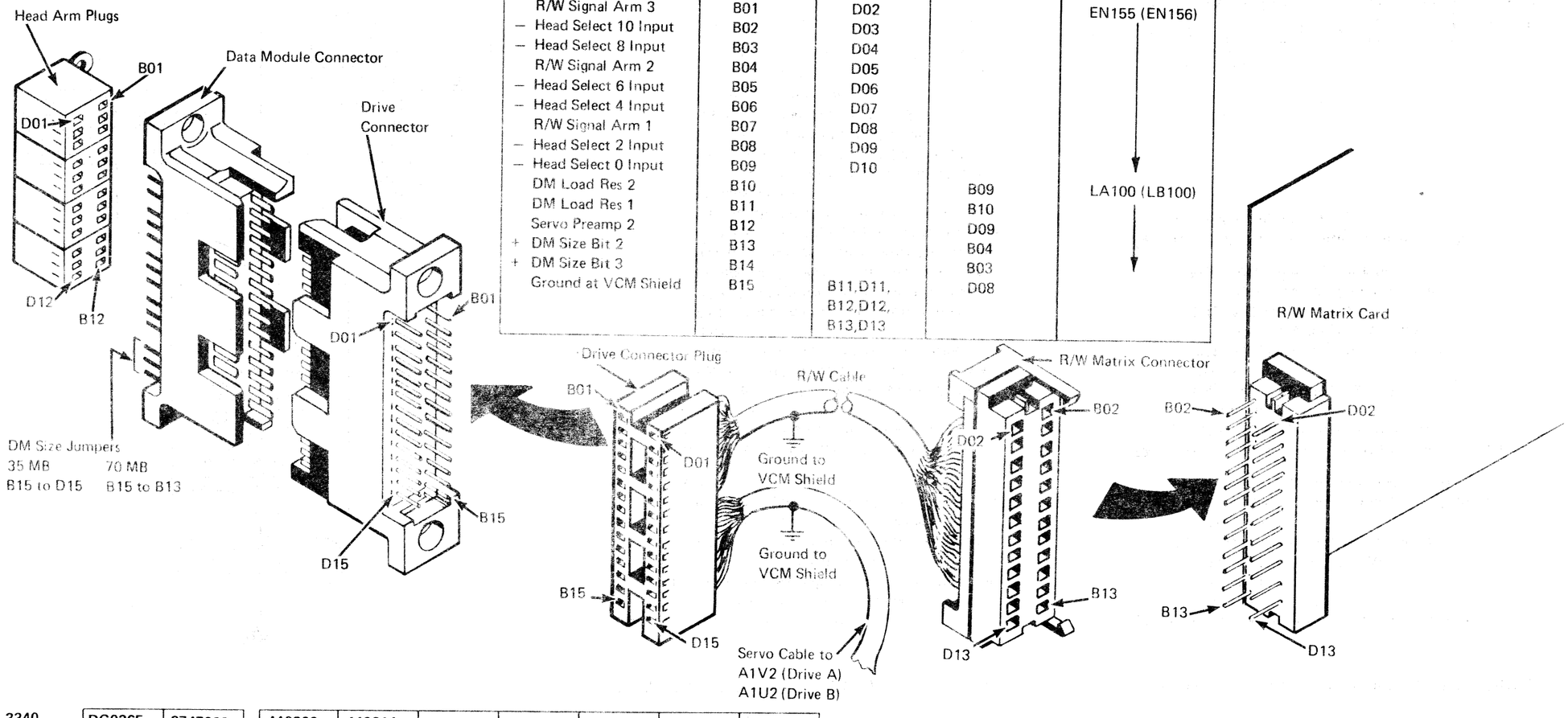
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DATA MODULE SIGNAL DISTRIBUTION



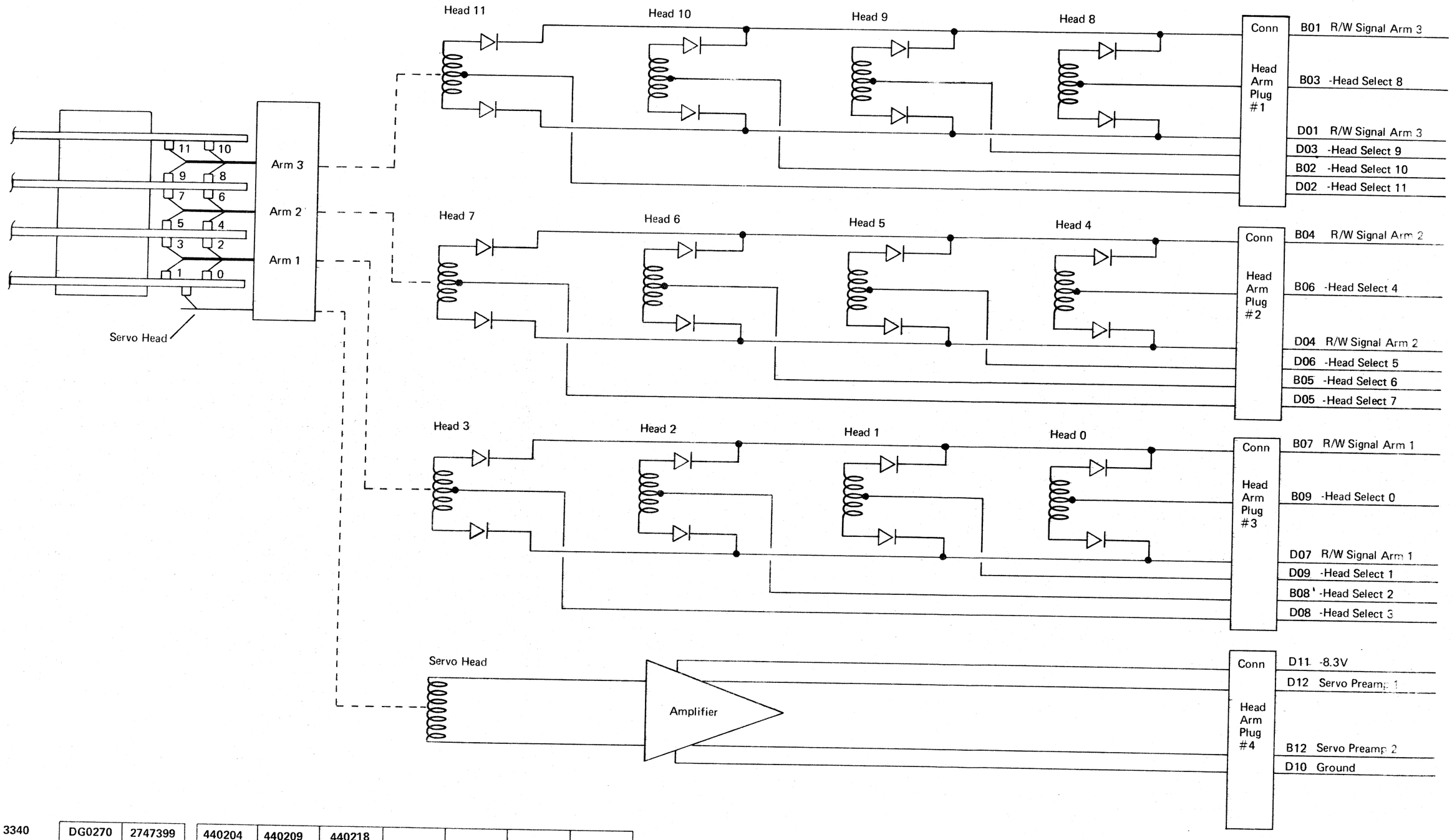
Refer to R/W 352 for complete data module wiring.

	Line Name	Data Module Connector	R/W Matrix Connector	A1V2(A1U2) Connector	Logic Reference
	R/W Signal Arm 3	D01	B02		EN155 (EN156)
–	Head Select 11 Input	D02	B03		
–	Head Select 9 Input	D03	B04		
	R/W Signal Arm 2	D04	B05		
–	Head Select 7 Input	D05	B06		
–	Head Select 5 Input	D06	B07		
	R/W Signal Arm 1	D07	B08		
–	Head Select 3 Input	D08	B09		
–	Head Select 1 Input	D09	B10		
	Ground at VCM Shield	D10			
–	8.3 V	D11		B12	LA100 (LB100)
	Servo Preamp 1	D12		D13	
+	DM Size Bit P	D13		B05	
+	DM Size Bit 0	D14		D03	
+	DM Size Bit 1	D15		B08	
	R/W Signal Arm 3	B01	D02		EN155 (EN156)
–	Head Select 10 Input	B02	D03		
–	Head Select 8 Input	B03	D04		
	R/W Signal Arm 2	B04	D05		
–	Head Select 6 Input	B05	D06		
–	Head Select 4 Input	B06	D07		
	R/W Signal Arm 1	B07	D08		
–	Head Select 2 Input	B08	D09		
–	Head Select 0 Input	B09	D10		
	DM Load Res 2	B10		B09	LA100 (LB100)
	DM Load Res 1	B11		B10	
	Servo Preamp 2	B12		D09	
+	DM Size Bit 2	B13		B04	
+	DM Size Bit 3	B14		B03	
	Ground at VCM Shield	B15	B11,D11, B12,D12, B13,D13	D08	



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DATA MODULE WIRING



DG0270	2747399
Seq. 1 of 1	Part No. ( )

440204	440209	440218				
21 Dec 73	25 Mar 74	5 Aug 74				

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