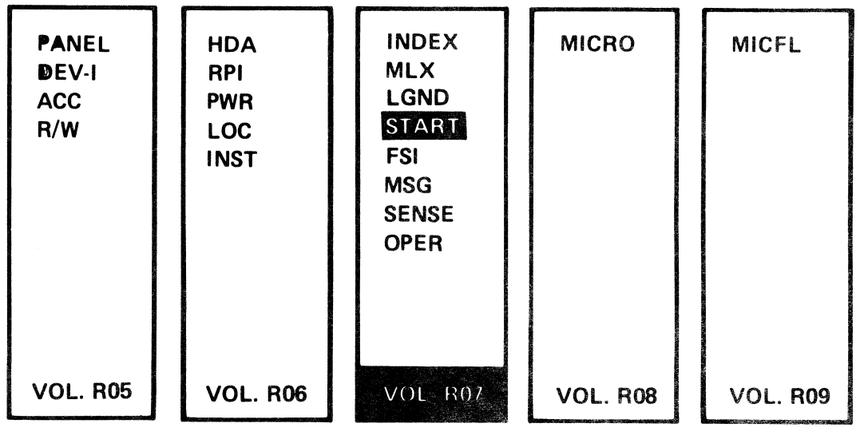
IBM Maintenance Library



Every Satellite Module on the 3340 subsystem (including the 3344) has its own Volumes R05 and R06.

The 3344 MLM also includes Volumes R07, R08, and R09. See the START section in Volume R07 for details.

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Disk Storage Maintenance Information

3344

KA0000 Seq. 1 of 2	2359022 Part No.

441235 28 May 76				

PREFACE

MAINTENANCE LIBRARY MANUAL ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3344 Maintenance Library Manual can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request (Order No. 120-1679). In the columns headed "Logic Page" enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

This manual was prepared by the IBM General Products Division, Technical Publishing, Department G26, San Jose, California 95193.

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SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)

2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

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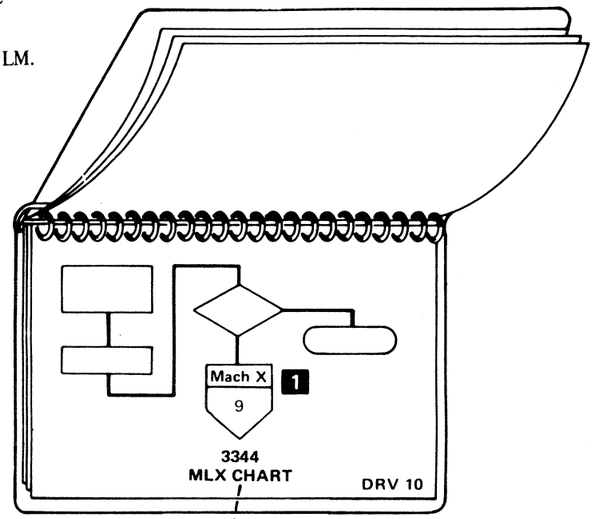
MAINTENANCE LIBRARY CROSS REFERENCE

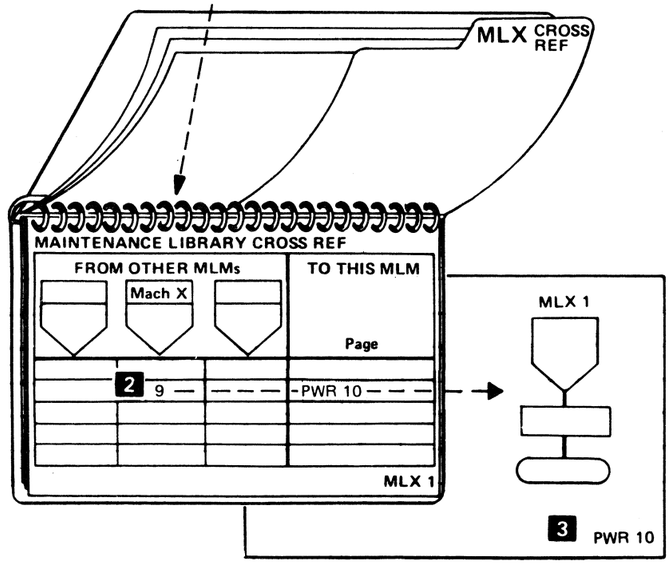
USE THIS PAGE WHEN ENTERING THIS MLM FROM OTHER MAINTENANCE LIBRARY MANUALS.

1. Note exit number on page of MLM you are leaving.
2. Find that exit number in the appropriate column of the chart on this page.
3. Proceed to the referenced page in this MLM.

Machine X Maintenance Library



3344 Maintenance Library



FROM OTHER MLMs: 4331	370/115	370/125	370/135	ISC	3830	TO THIS MLM: Page
			1	3, 5	3, 5	START 100, Entry A
1			6	6	6	START 100, Entry B
				7, 12	7, 12	START 101, Entry C
				8	8	START 101, Entry B
	10	10		14, 20	14, 20	SENSE 100, Entry A
3	11	11				MICRO 10
2	12	12				MICRO 90
	13	13		10	10	OPER 98
	14	14				FSI 100

3344 MLM EXIT LISTING

Note: *Use this page when tracing back from other maintenance library manuals to locate a line that exited from this MLM.*

Exit	Page(s)
1	MICFL 860, MICRO 84
2	SENSE 100, SENSE 106
3	
4	
5	START 101
6	
7	SENSE 103, START 101
8	
9	SENSE 100
10	MICRO 11
11	MICRO 8
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	

Exit 1: To Storage Control for instructions on running 3880 wrap test.

Exit 2: To Storage Control for definition of sense bytes 5 and 6 in Format 6 when attached to a 3880.

Exit 5: To Storage Control for definition of sense byte Formats other than 1, 4, 5 and 6 (Formats for system or attachment detected problems).

Exit 7: To Storage Control for definition of sense bytes 18 through 23 of Format 6 (Not device dependent information).

Exit 9: To Storage Control for definition of sense byte Formats which are not defined by the 3344 (Not Formats 1, 4, 5 or 6).

Exit 10: To Storage Control for Fxxx microdiagnostic error displays (usually reader errors detected in storage control).

Exit 11: To Storage Control for instructions on how to load device microdiagnostics.

LGND CONTENTS

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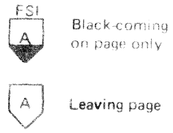
MAINTENANCE ANALYSIS PROCEDURE (MAP) LEGEND

FLOWCHART SYMBOLS

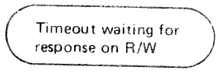


External Page Connector

Connection between diagrams on separate pages. Letter keys are used to identify corresponding points. Below the symbol is the page number of the connecting point.

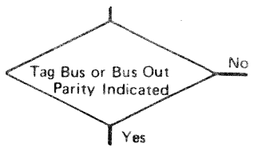
Internal Page Connector

Connection between several parts of the same diagram. Line-of-sight arrows assist in locating other connector(s).



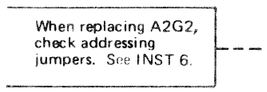
Terminal Block

Beginning or end of flow path.



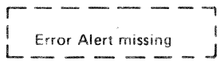
Decision Block

Branch to alternate paths.



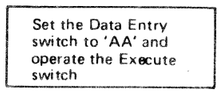
Annotation Block (Supplementary)

Descriptive comment or explanatory note.

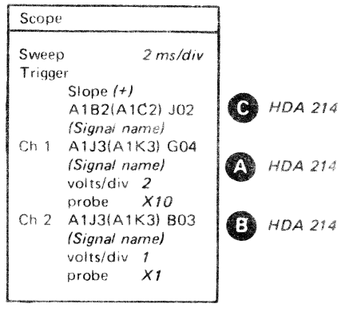


Annotation Block (In Line)

Descriptive comment or explanatory note.

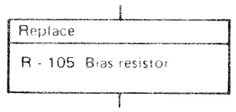


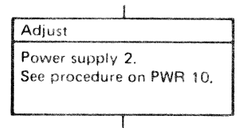
General Purpose Action Block

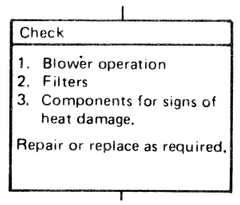


Scope Setup Block

Shows how to set up to scope.
Keys outside the block reference the test points being scoped and the MLM page showing the diagram of those test points.

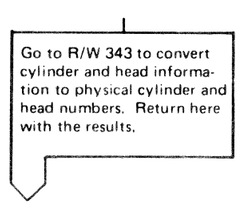


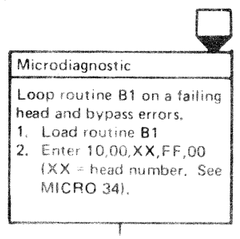




Specific Action Blocks

Denotes special CE actions: Replacing Cards, Checking, Running Microdiagnostics, Adjusting, or Installing.





Return Block

This special block is used as a reminder that, after branching to another page, returning to this flowchart is necessary to complete the analysis.

MAINTENANCE ANALYSIS PROCEDURE (MAP) LEGEND

FLOWCHART EXAMPLE

Controller Address	Message bits Byte 3 0 1 2 3	4 5 6 7	Hex Value
0	0 0 0 -	- 1 1 1	07
1	0 0 1 -	- 1 1 0	26
2	0 1 0 -	- 1 0 1	45
3	0 1 1 -	- 1 0 0	64

The controller address is determined by jumpers on the A2G2 card. See INST 6 for jumper locations.

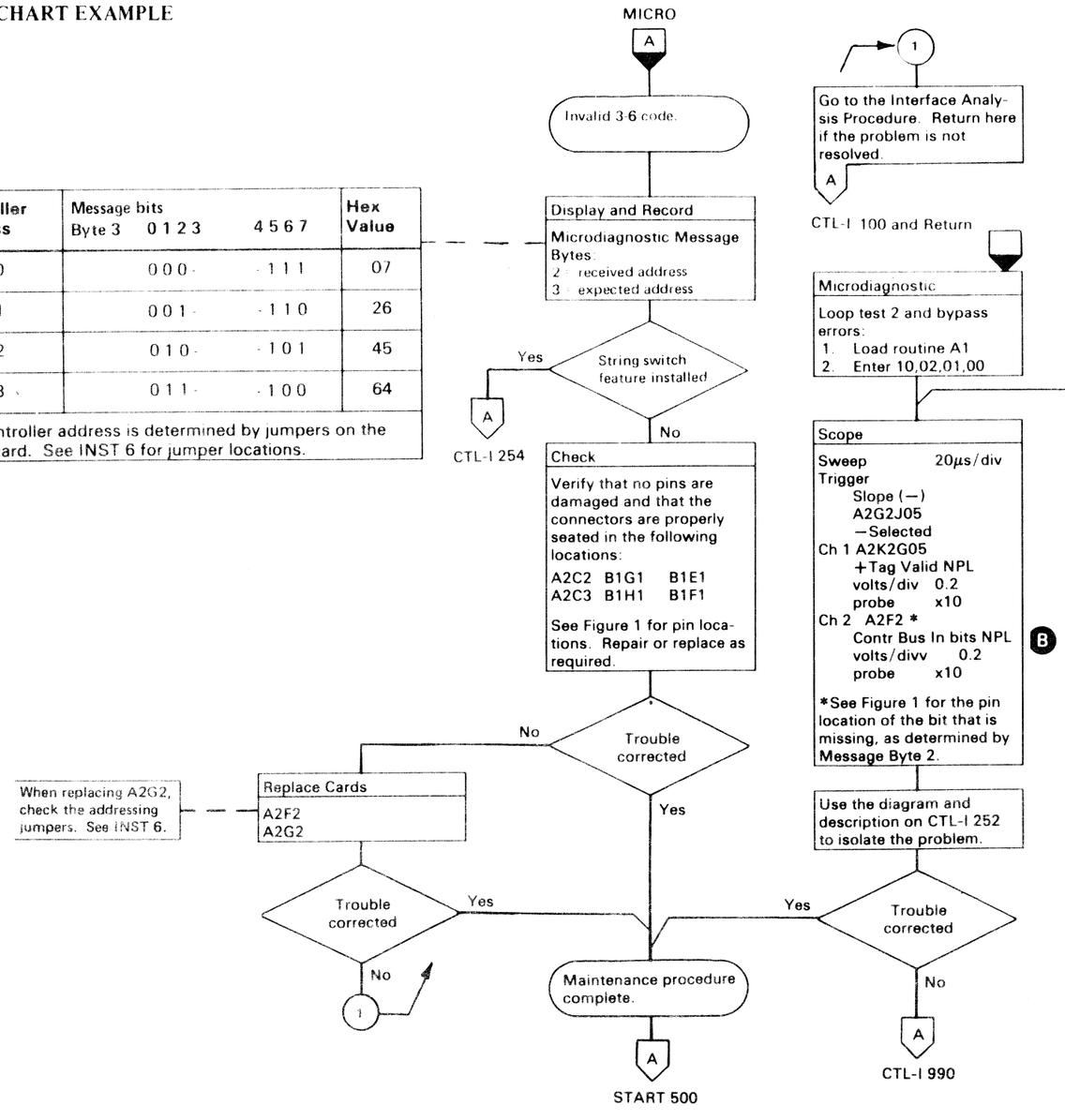


Figure 1. Pin Locations

Line Name	Card A2G2 Pins (A)	Card A2F2 Pins (B)	Conn A2C3 Pins (C)	Conn B1H1 Pins (D)	Conn B1F1 Pins (E)
+Contr Bus In Bit 0	S02	D06	D05	J04	J04
+Contr Bus In Bit 1	U05	B03	B05	G05	G05
+Contr Bus In Bit 2	U02	D10	D06	J06	J06
+Contr Bus In Bit 3	M12	D09	B09	G08	G08
+Contr Bus In Bit 4	M13	J02	D10	J09	J09
+Contr Bus In Bit 5	P13	J07	B10	G10	G10
+Contr Bus In Bit 6	S09	J11	D11	J11	J11
+Contr Bus In Bit 7	U13	J03	B12	G12	G12
+Contr Bus In Bit P	G08	J12	B02	G03	G03

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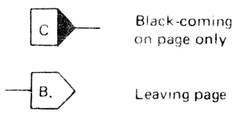
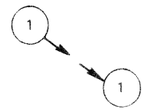
MAINTENANCE ANALYSIS PROCEDURE (MAP) LEGEND

DIAGRAM SYMBOLS



External Page Connectors

Connection between diagrams on separate pages. Letter keys are used to identify corresponding points.



Internal Page Connectors

Connection between several parts of the same diagram. Line-of-sight arrows assist in locating other connector(s).

Test Points

Used on diagrams to indicate key test points or key circuit parts.

CHANNEL INTERFACE (CHL–I)

CONTROL INTERFACE (CTL–I)

DEVICE INTERFACE (DEV–I)

Interface Between Two Functional Units

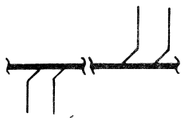
(For examples of their use, see OPER 3.)

DEV BUS IN DEV BUS IN

CTL BUS OUT CTL BUS OUT

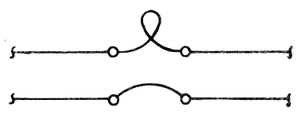
READ ⟷ WRITE ⟷ READ

Channel Buses and Read/Write Bus



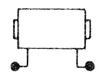
Bus or Cable

(Multiple lines entering and exiting.)



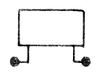
Interboard Connector

(Trilead or jumper.)



Solenoid

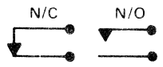
Identified by name, for example, Brake Solenoid.



Relay or Contactor

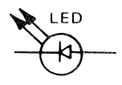
Type indicated by letter code.

P = Pick	H = Hold
PL = Pick Lower	LP = Latch Pick
PU = Pick Upper	LU = Latch Upper



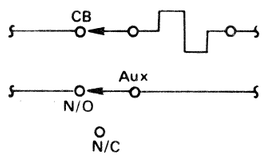
Relay Contacts

Shown in the de-energized position.
N/C = Normally Closed (break).
N/O = Normally Open (make).



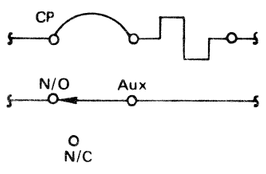
LED (Light Emitting Diode)

Indicator (lamp)



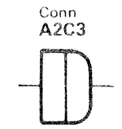
Circuit Breaker (CB) with Aux Points

Electrically or manually tripped, handle generally higher current, and may have auxiliary points (aux). N/O points make contact when associate CB is positioned to conduct current.

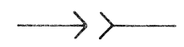


Circuit Protector (CP) with Aux Points

Normally tripped electrically, handle lower current, and may have auxiliary points (aux). N/O points make contact when associate CP is positioned to conduct current.



Connector (multiple line)



Disconnect

MAINTENANCE ANALYSIS PROCEDURE (MAP) LEGEND

DIAGRAM SYMBOLS

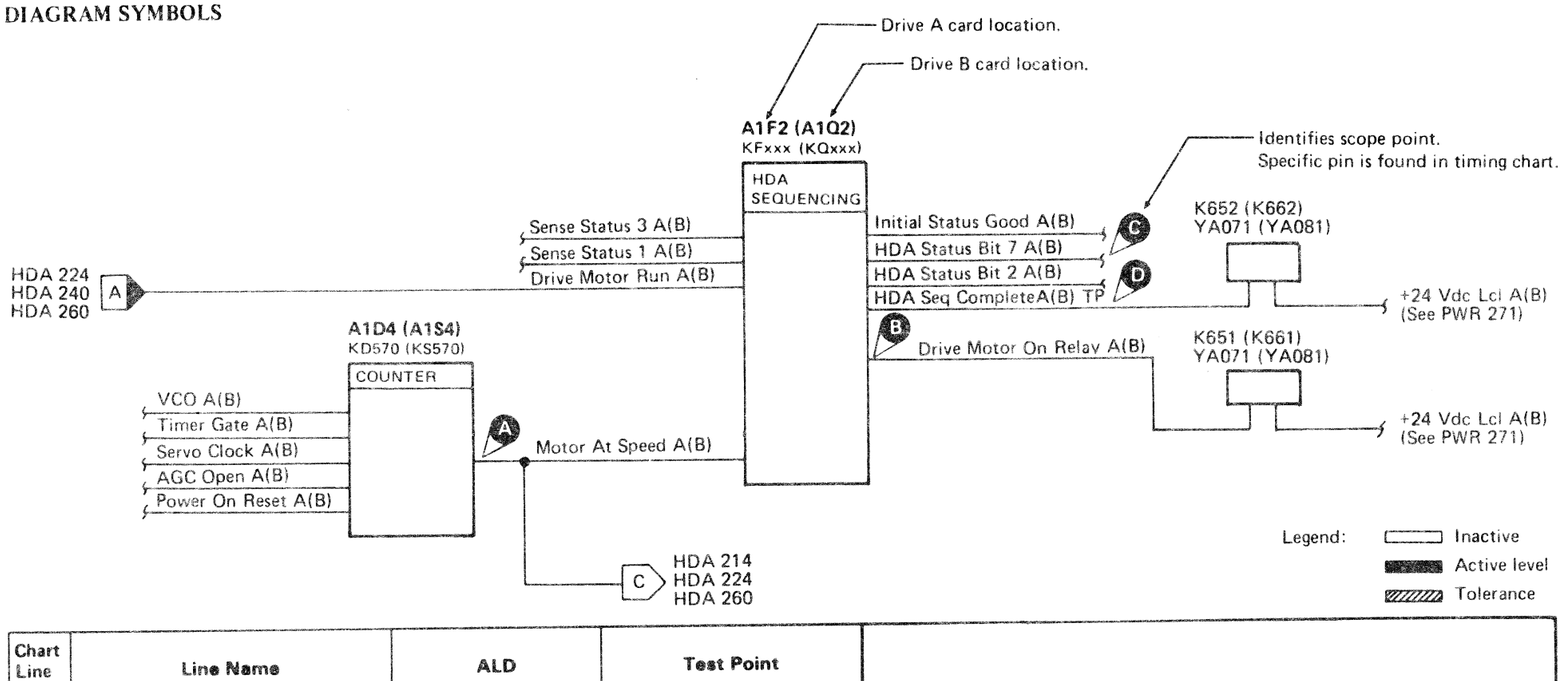
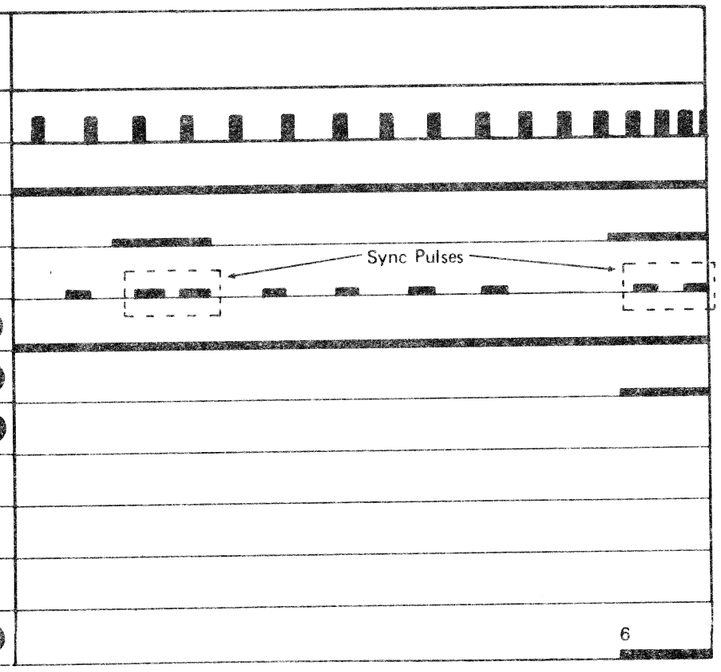


Chart Line No.	Line Name	ALD	Test Point	
1	+VCO A(B)	KD570 (KS570)	A1D4 (A1S4) D13	
2	+AGC Open A(B)	KD570 (KS570)	A1D4 (A1S4) B11	
3	+Timer Gate A(B)	KD570 (KS570)	A1D4 (A1S4) J13	
4	+Servo Clock A(B)	KD570 (KS570)	A1D4 (A1S4) G10	
5	−Drive Motor On Relay A(B)	KF260 (KQ260)	A1F2 (A1Q2) U13	B
6	+Motor At Speed A(B)	KD570 (KS570)	A1D4 (A1S4) D07	A
7	+HDA Status Bit 7 A(B)	KF240 (KQ240)	A1F2 (A1Q2) J11	C
8	−Sense Status 3 (A)B	KF130 (KQ130)	A1F2 (A1Q2) B04	
9	+HDA Status Bit 2 A(B)	KF230 (KQ230)	A1F2 (A1Q2) B02	
10	−Sense Status 1 A(B)	KF130 (KQ130)	A1F2 (A1Q2) D04	
11	−HDA Seq Complete A(B) TP	KF260 (KQ260)	A1F2 (A1Q2) S02	D



Block Diagrams

Show the cards that relate to a specific failure in Drive A. The information in the parentheses applies to Drive B. This diagram also shows the ALD references, line names, and test points for each card.

Sequence Charts

The heavy black lines show the active state for the test point shown.

For example: HDA Seq Complete A(B) TP (chart line no. 11) goes minus when Motor At Speed A(B) is active (chart line no. 6).

AUTOMATED LOGIC DIAGRAMS

STORAGE ELEMENT LINE DEFINITIONS

Inputs to blocks are identified by letters inside the block, adjacent to each input. Examples of line designations are shown above.

AC Coupled FF: The J, T, and K input sources provide an ac triggered flip flop. At least one of the inputs must have a positive transition to cause the FF output to change. However, input sources T and J must both be down simultaneously prior to the positive transition in order to set the FF. Input sources T and K must both be down simultaneously prior to the positive transition in order to Reset the FF. If J and K are both down, then the FF changes states with each positive shift of input source T; input source T may be a clock timing pulse. If J and K are both up, then No transition occurs with positive shift of input source T. If J is down and K is up, a positive shift of T or J sets the FF it is not already set. Conversely, if J is up and K is down, then a positive shift of T or K resets the FF if it is not already reset.

S Set: When set is active, all outputs are at the polarity shown.

R Reset: When reset is active, all outputs are at a polarity opposite to that shown.

C Control: When active, the control input permits the output to change with changes to the data in input line. When inactive, the control line holds the output at whatever polarity it possessed at the moment the control line became active.

CD Controlled Data: When the associated control input is the polarity shown, a CD input at the polarity shown sets the storage element. Likewise, a CD input at its opposite polarity resets the storage element, when a control input is active, If multiple CD inputs to the storage element, any one active CD input can set the storage element.

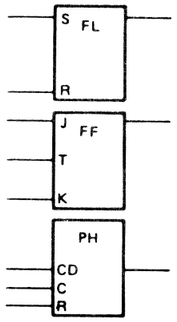
G Gate: Represents the AND function without the use of the AND logic symbol. When multiple gating lines are required, gates are identified by the same numerals used to identify its related gated dependent line. A G1 gate controls an input or output line marked with a 1.

G Gate (input): When at the polarity shown, G Gate allows a dependent inputs of the polarity indicated to affect the storage element. In all other cases, it can be considered inactive.

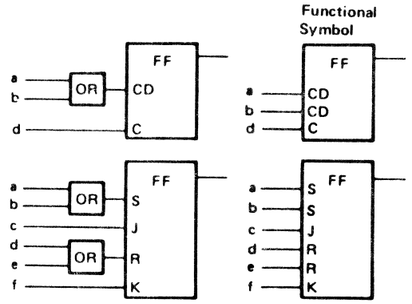
G Gate (output): The dependent output is at the polarity shown when the associated gating line is at its indicated polarity. In all other conditions the output stands opposite to the polarity shown.

STORAGE ELEMENTS

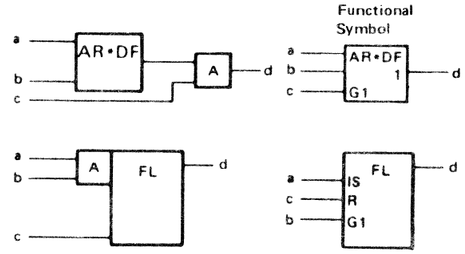
Basic Storage Symbols



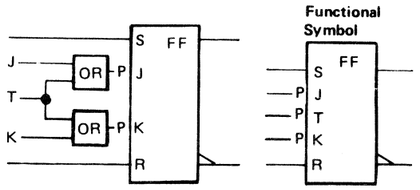
Inherent-OR In The FF



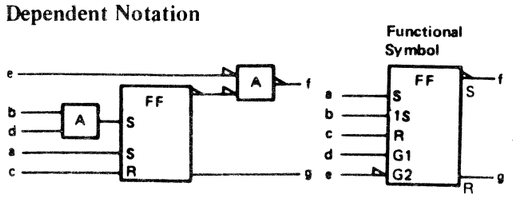
Single Function Application



AC Coupled FF

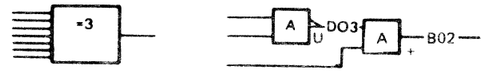


Dependent Notation



Note: If the outputs can be determined for simultaneous set/reset, an S or R below an output indicates the FF condition, either set or reset. Multiple set (or reset) inputs are considered to br ORed.

Special Notations



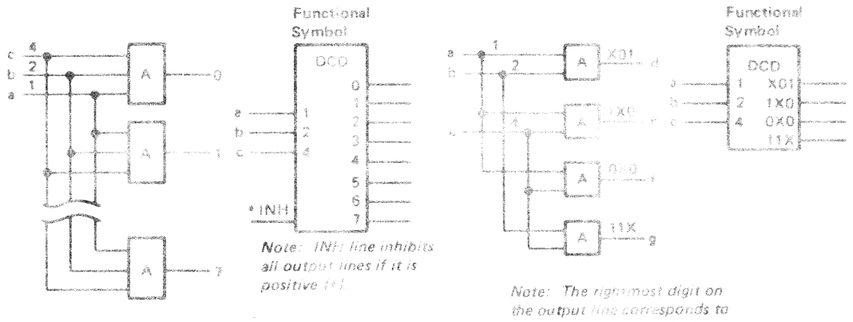
An equal sign (=) followed by a number specifies the number of input lines of the polarity shown required to produce the indicated output.

A plus (+) or minus (▷) under an output line indicates the extreme potential that may be forced by an external source.

A loading character (L or U) under the output line indicates that the external load cannot be isolated from the driving circuit without affecting the output of the driver.

AUTOMATED LOGIC DIAGRAMS

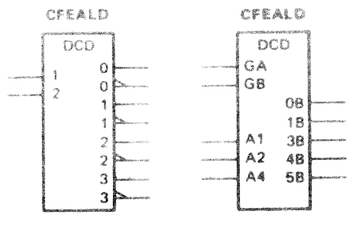
DECODE



The decimal sum of the line values of those inputs that are at their active level equals the value of the active output line. If no input lines are active, the 0 output line is active. If all input lines are active, the 7 output line is active.

Note: The decimal sum value existing at the decoder inputs agrees with the decimal number shown at the output line labels. Only one output can be active at any given time.

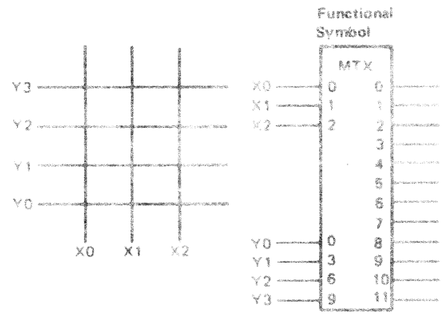
Output Value	Input Line Condition
0	$\bar{a}$ $\bar{b}$ $\bar{c}$
1	$\underline{a}$ $\bar{b}$ $\bar{c}$
2	$\bar{a}$ b $\bar{c}$
3	$\underline{a}$ b $\bar{c}$
4	$\bar{a}$ $\underline{b}$ c
5	$\underline{a}$ $\underline{b}$ c
6	$\bar{a}$ b c
7	a b c



Multiple output lines can be associated with a given output (sum).

A decoder shown with gating lines.

MATRIX



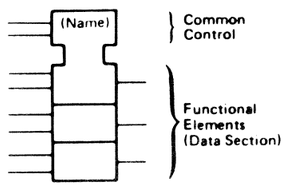
Active Input Lines							Active Output
X0	X1	X2	Y0	Y1	Y2	Y3	
X			X				0
	X		X				1
		X	X				2
X				X			3
	X			X			4
		X		X			5
X					X		6
	X				X		7
		X			X		8
X						X	9
	X					X	10
		X				X	11

Note: The matrix (MTX) is a functional logic block with two or more groups of inputs. The decimal numbered output is active when it equals the decimal sum of one active line from each input group (shown in Chart). If any input group does not have an active input, then there is no active output from the matrix block.

AUTOMATED LOGIC DIAGRAMS

ELEMENTS WITH COMMON INPUTS/OUTPUTS

Element Description

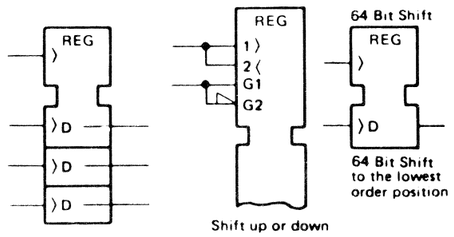


COMMON CONTROL SECTION: Used only for dependancy (gating) and/or common lines for the register. There are no outputs from the common control section.

NAME: May be any of the following- selector (SEL), register (REG), decoder (DCD), matrix (MTX), multiregister (MREG), and delay (DLY).

DATA SECTION: A group of vertically stacked function elements. The number of stacked elements varies with the number of inputs.

Shift Register (REG)



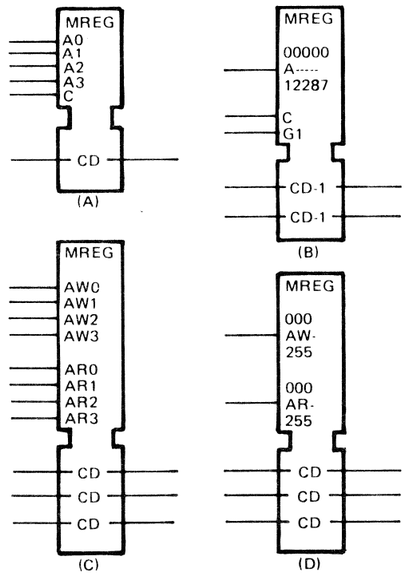
DEFINITION: The control input causes the data in each bit position to shift one position, as indicated by one of the following designations.

Greater than (): When this line becomes active, the data content shifts from the top (upper-most) bit position. Similarly, the contents of each bit position shifts down the symbol.

Less than (): When the line becomes active, the data content shifts from the bottom to the next bit position above and similarly for each bit position in the shift register symbol.

Note: A time difference in shifting is indicated by a trailing edge symbol (¬).

Multiregister (MREG)



DEFINITION: The MREG functional logic block represents groups of associated storage elements in addressable word configuration. The MREG requires address inputs. All functional lines used for storage elements including the dependency notation are applicable.

Addresses are previously decoded and the resultant address line(s) is handled by a single flowline representing all addresses.

Address notation A, AR, or AW must prefix the data. This indicates the data is dependent on an address.

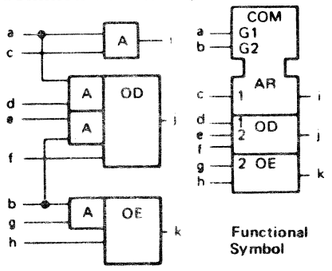
- A = Read Only Storage (ROS) or when the read/write address is identical.
- AW = Write address. AW must be shown as data input dependent (for example, AWCD).
- AR = Read address. AR must be shown as data output dependent.

The numeric address span is specified in the common section.

The G replaces the C to control the data information in the MREG. The C is reserved for the condition that would place a zero in all storage cells not addressed.

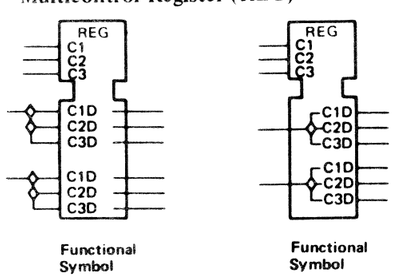
Example	Input Lines Needed	Output Lines Needed
(A)	A(0,1,2,3) C CD	A(0,1,2,3) CD (data)
(B)	A(0-12287) C CD	A(0-12287) G1 (gate) CD (data)
(C)	AW(0,1,2,3) CD	AR(0,1,2,3) CD (data)
(D)	AW(0-255) CD	AR(0-255) CD (data)

Common Function (COM)



DEFINITION: Common Function block may be associated with any group of basic logic elements functionally related by their dependent gating. Each functional element contains the proper letter(s) that makes it an approved logic symbol. The common section may contain the letters COM at the very top line.

Multicontrol Register (REG)



The multiple control inputs are designated by sequential numbers shown entering the common section; for example, C1, C2.

The control data enters the data section of the symbol and is normally diagrammed as multiple outputs.

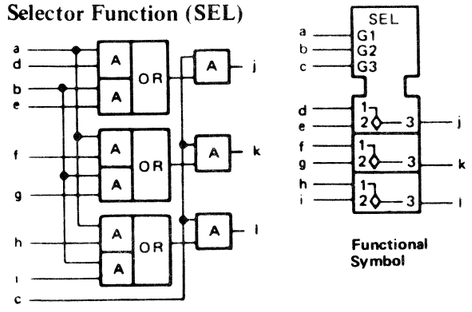
The "C" designator must be a suffix to differentiate it from a gate.

Example:

C1D = Storage Data controlled by C1.

Note: The "◇" symbol represents the OR function connection in the data section.

Selector Function (SEL)



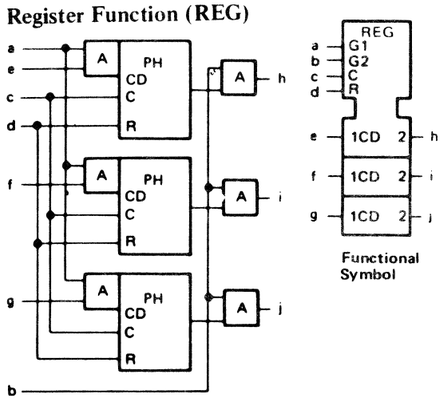
DEFINITION: A selector is a functional logic block that consists of two or more OR blocks having input and/or output signals dependent upon common gates.

Example:

Output line "j" is active when line "c" is active and lines "d" and "a" or lines "e" and "b" are active.

Note: The "◇" symbol represents the OR function connection in the data section.

Register Function (REG)



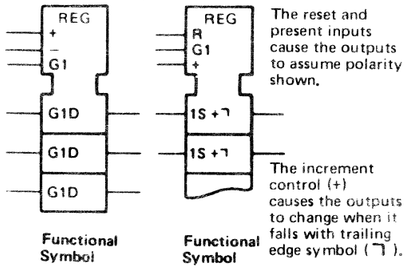
DEFINITION: A register logic block consisting of a group of associated storage elements with common input and/or output gating or other common input lines such as reset.

Note: Descriptive nomenclature such as bit 1, may be placed in each logic element.

Example:

Output "h" is active when input lines "e" and "a" are active and the output gate line "b" is active.

Counter (REG)



DEFINITION: A register to be incremented or decremented under control of input lines drawn to the common section of the symbol with the following notations.

+n: When this line goes to its indicated polarity, the decimal quantity n is added to the binary count contained in the register. The n need not appear when it is a one.

–n: When this line goes to its indicated polarity, the decimal quantity n is subtracted from the binary count contained in the register. The n need not appear when it is a one.

ABBREVIATIONS AND DEFINITIONS

A

A	AND function (logic block)
A2	control module
A2F	Control module with fixed heads installed
A * OR	AND * OR function (logic block)
AC, ac	alternating current
ACC	access
addr	address
ALD	Automated Logic Diagram
AM	Address Mark
amps	amperes
AP-1	Analysis Program
AR	Amplifier (logic block)
asm	assembly
assm	assembler
attn	attention

B

B2	satellite module
B2F	satellite module with fixed heads installed
BCD	binary coded decimal
BI	Bus In
BO	Bus Out
BSCA	bit significant controller address
BSDA	bit significant device address
BS	Bootstrap
BSM	basic storage module
BTU	British Thermal Unit
Bus In	bus entering a functional unit
Bus Out	bus leaving a functional unit
byte	eight bits plus a parity bit

C

C	capacitor
CA	controller address
CAR	Cylinder Address Register
CB	circuit breaker
CC=3	condition code 3
CCB	Correction Code Byte
CCHH	cylinder (2 bytes), head (2 bytes)
ccw	counterclockwise
CCW	Channel Command Word
CDS	Configuration Data Set
CE	Customer Engineer
CFEALD	Condensed Field Engineering Automated Logic Diagram
chan	channel
chaining	sequential linking of instructions or data
CHK-1	Check 1
CHK-2	Check 2
CHL-1	channel interface
clk	clock
cm	centimeters
corr	correction
CP	circuit protector
CPU	Central Processing Unit
CR	diode; rectifier (semiconductor)
CSW	Channel Status Word
CTL-I	control interface
ctlr	controller
CU	control unit
CUA	Channel Unit Address
CV	converter
cw	clockwise
cylinder	a set of tracks on a storage device that can be accessed without repositioning the access mechanism

D

DA	device address
DAC	digital-to-analog converter
DC, dc	direct current
DCB	Detection Code Byte
DCD	decoder (logic block)
decrement	decrease by regular consecutive steps
Delta, △	A three-terminal circuit configuration (usually refers to the primary winding arrangement of a transformer). Also used to indicate a change in some dimension, such as: △t= change in time; △d= change in distance
DEV-I	device interface
Diff	Difference Counter
DIO	Device Input/Output
dld	delayed
D_L	data length
DOS	Disk Operating System
drive	mechanical assembly to control one HDA
Drive A	left drive in a module
Drive B	right drive in a module
drop	de-energize relay

E

EC	edge connector, engineering change
ECB	Event Control Block (OS/VS only)
ECC	Error Correction Code
EL	Error Log
EOF	end of file
EPO	emergency power off
ERP	error recovery program
EREP	Environmental Record Editing and Printing
Error Code	Error Symptom Code generated by a microdiagnostic failure
EXIO	execute input/output
ext	external

F

F	Flag Byte
FEALD	Field Engineering Automated Logic Diagram
FF	Flip-Flop (logic block)
FL	Flip Latch (logic block)
FPM	file protect mode
FRIEND	Fast Running Interpreter Enabling Natural Diagnosis
FRU	field replaceable unit
FSC	Fault Symptom Code
FSI	Fault Symptom Index

G

g	grams
G1	gap between Index point and R0
G2	gap between Count area and Key area
G3	gap between Data area and the Address Mark of the following record
G4	gap after Data area of the last record on a track
glitch	spurious signal
gnd	ground

H

H	henries
HA	Home Address
HAR	Head Address Register
hard error	a malfunction that is detected internally and considered to be of a catastrophic magnitude
HDA	head/disk assembly
head	an electromechanical device that records, reads, or erases a storage medium
hex	hexadecimal
Hz	hertz, cycles per second

I

ID	identifier
IFA	integrated file adapter
IMPL	initial microprogram load
increment	increase by regular consecutive steps
int	internal
IPO	immediate power off
IO	input/output
IPL	initial program load
ISC	integrated storage control
IW	write current

J

J	connection, receptacle
JCL	job control language

K

K	relay (contactor)
K_L	key length

L

L	inductor
LB	laminar bus
LED	light emitting diode
LIM	limiter (logic block)
LOC	location
loop	microdiagnostic test loop
LR	line receiver (logic block)
LT	line terminator (logic block)

M

M	meter
map	maintenance analysis procedure
Mb	megabyte
MICFL	microdiagnsotic flowchart
MICRO	microdiagnostic Error Code Dictionary
MLM	maintenance library manual
MLX	maintenance library cross reference index
module	serial numbered frame containing two drives
modulo	number system to a base other than ten
MPL	microprogram load
ms	millisecond
MSG	message
MST	monolithic system technology
MST-1	voltage level (see divider tabs)
M/T	multiple track
μs	microsecond

N

N	inverter (logic block)
N/C	normally closed point
N/O	normally open point
N OR	inverter -OR (logic block)
NOP	no operation
NPL	voltage level (see divider tabs)
ns	nanosecond

ABBREVIATIONS AND DEFINITIONS

O

OBR	outboard recorder
OE	exclusive OR function
offline	isolated control of a unit from a primary function
OLT	online test
OLTEP	online test executive program
OLTSEP	online test standalone executive program
online	unit is available to a primary function
op	operation
OR	OR function (logic block)
OR * FL	OR flip latch function (logic block)
OS	operating system

P

P	plug (connector)
PA	physical address
par	parity
parameter	constant value for a given purpose
P bit	parity bit
PC	parity check
PG	parity generator
PH	polarity hold (logic block)
pick	energize relay
PLD	power line dip
PLO	phase locked oscillator
P/N	part number
P/P	peak-to-peak
PS	power supply
PSW	Program Status Word
PWR	power

Q

Q	transistor

R

R	resistor
raw data	data as it is read from the storage medium
R0	Record 0
RCVR	receiver (logic block)
Rd	Read
RDCKD	Read Count Key Data
RDHA	Read Home Address
reg	register, regulator
RESV	Reserved
RPS	Rotational Position Sensing
R/W	read/write

S

S	switch
SCR	silicon controlled rectifier
SCRID	SCR indicator driver
SD	skip displacement
SEL	selector (logic block)
SERDES	serializer/deserializer
servo	head positioning system
SERVOUT	Service Out
SFM	Set File Mask
SIO	start input/output
SIP	Seek in progress
SK	Seek
SL	system library
SLT	solid logic technology
soft error	internally recoverable malfunction that is transparent to the user
SOSP	standalone/online support program that is transparent to the user
spindle	contained in the HDA
SS	single shot (logic block)
SWFE	string switch feature
sync bit	generated by the storage control during Read and Write operations
SYSPRINT	a printer (program assignment)

T

T	transformer or terminal
TB	terminal board
TIC	transfer in channel
TP	test point
track (trk)	a location on a storage medium accessable by one R/W head
truncate	to end an operation before completing the function

U

UC	Unit Check
UCW	Unit Command Word
unsuppr	unsuppressible

V

V	voltage amplifier (logic block)
VCM	voice coil motor
VCO	voltage controller oscillator
VFO	variable frequency oscillator

W

WCKD	Write Count Key Data
word	four bytes
Write	Write operation
wraparound	advance according to some sequence with automatic restart provisions
Wye	a three terminal circuit configuration (usually refers to the primary winding arrangement of a transformer)

X

XEQ	execute
XOR	exclusive OR function (logic block)

Z

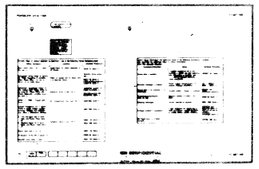
Z	impedance network

START CONTENTS

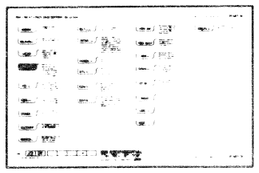
Note: *For 3340 problems (and all problems not related to the 3344), go to the START section in the 3340 MLM.*

3344 MAINTENANCE INFORMATION MANUAL

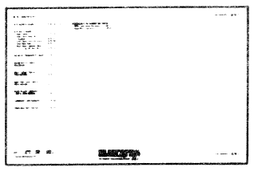
ORGANIZATION OF INFORMATION



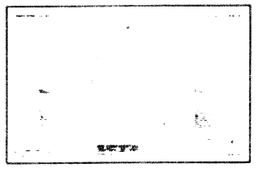
The START section describes the MLM and the 3344 maintenance philosophy. All problem analysis begins on START 100.



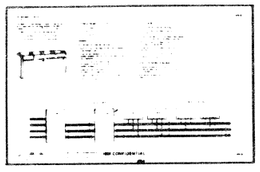
Documentation description on START 20 and 21 defines each section of the manual.
Where practical, documentation is arranged in sections corresponding to natural breakdown of machine elements.



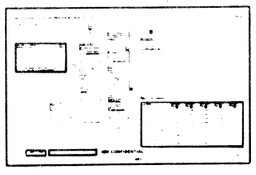
Page 1 of each section shows the contents of that section and where related information can be found in other sections of the manual.



Maintenance analysis procedures in each section are entered after the START section and lead the reader through a detailed analysis of each problem. These procedures consist of flowcharts, block diagrams and timing charts.

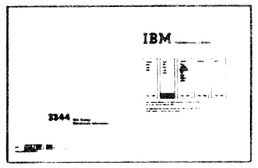


The OPER section describes the functional operation of the 3344. The information is presented logically; each subject is presented in the order in which it occurs in overall machine operation.

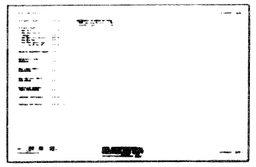


The LGND section defines each symbol used throughout the manual and shows examples of the diagrams used. This section also includes a glossary of special words and abbreviations.

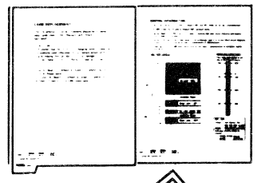
HOW TO FIND INFORMATION



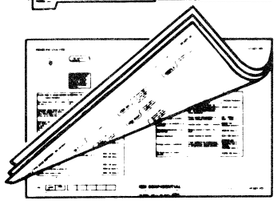
Title page in the front of each volume shows the location of each section by volume.



Page 1 of each section shows the contents of that section and where related information can be found in other sections of the manual.

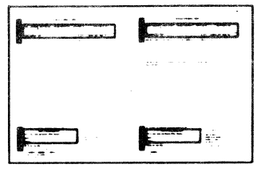


Divider tabs make it easy to locate sections. The tabs also contain useful information about scoping and voltage levels.



Page numbers and titles in "thumbing" position allow rapid scanning.

The alphabetic subject index gives references to specific subjects in the manual.



MLM Feedback forms are located in the front of Volume R01. This is a simple and quick means of sending comments and suggestions directly to the author.

3344 MAINTENANCE INFORMATION MANUAL

HOW TO PERFORM A TASK

To install the machine:

Go to INST 1.

To troubleshoot or repair the machine:

Go to START 100.

To analyze a console message:

Go to MSG 9 for OS/VS.
Go to MSG 13 for DOS/VS.

To run microdiagnostics:

Go to MICRO 8.

To run online tests:

Go to OLT 1 in the 3340 MLM.

To analyze a diagnostic error message:

Go to MICRO 12 for microdiagnostic error messages.
Go to OLT 40 in the 3340 MLM for online test error

To analyze an EREP printout:

Go to MSG 22.

To analyze sense bytes:

Go to SENSE 100.

To power off a drive:

Go to PANEL 10.

To learn how the machine operates:

Go to OPER 1.

To remove and replace mechanical parts:

Go to HDA 700.

To operate the CE Panel:

Go to PANEL 20 in the 3340 MLM.

To run FRIEND:

Go to OLT 26 in the 3340 MLM.

To assign alternate tracks:

Go to OLT 30 in the 3340 MLM.

To review the maintenance philosphy:

Go to START 50.

3344

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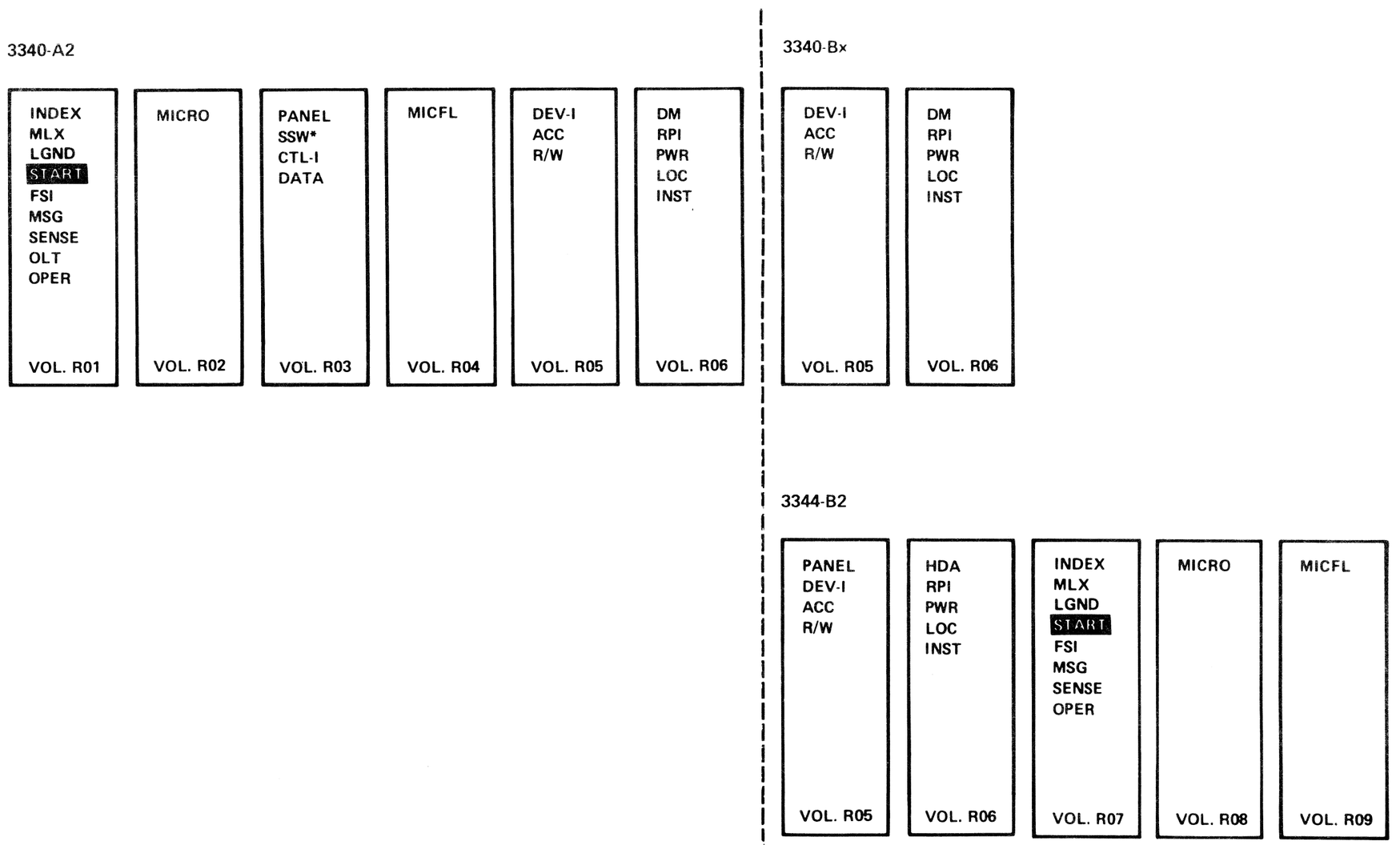
DOCUMENTATION DESCRIPTION

The 3344 MLM was designed to be a part of the 3340 MLM.

The 3340 MLM contains six volumes. The entire set of six volumes is shipped with every 3340-A2 Module. Only two volumes, R05 and R06, are shipped with every 3340-Bx Module. Each serial-numbered 3340 module is shipped with its own MLM volumes to ensure that the correct level of documentation for any machine is matched with hardware at any level.

Because the 3344 module is a B2 Module that attaches to a 3340 subsystem, it also has its own volumes R05 and R06. Because of other differences between the 3340 and the 3344, the 3344 MLM also includes volumes R07, R08, and R09.

See START 21 for descriptions of the individual sections.



DOCUMENTATION DESCRIPTION (By section)

These sections can only be found with each 3340 Control Module (one set per facility). See START 20 in the 3340 MLM.

START — Primary MLM starting point:
The 3340 START section points to the 3344 START section for all 3344 maintenance information. (1)

PANEL CE OPER. — Description, operation, and maintenance of the 3340 CE and Operator panels. The 3344 MLM also contains a PANEL section for the 3344 Operator Panels.

SSW STRING SWITCH FEATURE — Maintenance (MAPs) and theory for the string switch feature and associated circuits.

CTL-I NTERFACE — Maintenance (MAPs) and theory for the control interface and associated circuits. (Tag decodes, addressing, bus assembly circuits, etc.)

DATA CONTROL — Maintenance (MAPs) and theory for the controller circuits involved with data transfer. Includes: Read/Write control, Error Detection and correction, SERDES, and PLO/VFO.

These sections accompany every 3344 (one set per serial numbered frame).

VOLUME R05

PANEL OPER — Description of the 3344 Operator Panel.

DEV-I NTERFACE — Maintenance (MAPs) and theory for device interface and associated circuits. (Tag decodes, selection, bus assembly circuits, etc.)

ACC ESS — Maintenance (MAPs), adjustments, and theory of servo circuits and head positioning mechanics.

R/W DRIVE READ/WRITE — Maintenance (MAPs) and theory for drive read/write circuits.

VOLUME R06

HDA HEAD/DISK ASSEMBLY — Maintenance (MAPs), theory, adjustments, and removals for the head/disk assembly.

RPI ROTATIONAL POSITION INDEX — Maintenance (MAPs) and theory for the Index detection and checking, and the rotational position sensing circuits.

POWER — Maintenance (MAPs), adjustments, and theory for power supplies, distribution, and sequencing.

LOC ATIONS — Shows structural and component locations.

INST ALLATION — Installation instructions.

VOLUME R07

INDEX — Alphabetical subject index of the MLM.

MLX CROSS REFERENCE — Pages for cross-referencing other MLMs (3830-2, ISC, IFAs, etc.).

LGND — Glossary of technical terms. Abbreviations, Legend of the symbols used in the MLM, including FEALD circuit symbology.

(1) **START** — 3344 MLM starting point: Documentation description. How to use the MLM. Maintenance philosophy. Entry point for trouble-shooting and exits to MAPs within functional area MLM sections.

FSI FAULT SYMPTOM — Fault Symptom Code description, generation instructions, and index to tie the Fault Symptom Code to the proper analysis procedures.

MSG SYSTEM MESSAGES — Presents and explains basic console error message format, EREP summaries (OS), OBR error record (OS), and logging mode error record.

SENSE DATA — Summary and detailed description of sense data.

OPER ATIONS — Description of 3344 operations to tie functional units together. Provides high level description of string operation, including some command descriptions allowing the CE to obtain the "big picture" without going to system documentation.

VOLUME R08

MICRO OPER INST — Microdiagnostic operating instructions and brief routine and test descriptions for the 3344 drives only. See the MICRO section in the 3340 MLM for 3340 microdiagnostic operating instructions.

MICRO A0XX — Microdiagnostic Error Code Dictionary. Defines Error Codes and ties codes to analysis procedures for the 3344 drives only. See the MICRO section in the 3340 MLM for 3340 Microdiagnostic Error Code Dictionary.

VOLUME R09

MICFL A0 000 — Microdiagnostic routine descriptions, flowcharts, and scoping procedures for the 3344 drives only. See the MICFL section in the 3340 MLM for the 3340 microdiagnostic flowcharts.

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3344 MAINTENANCE PHILOSOPHY

The 3344 is always attached to a 3340-A2 Controller. Because it is attached to a 3340-A2, all maintenance action begins on START 100 of the 3340 MLM. When maintenance is required on a 3344 drive, the START section of the 3340 MLM points to the START section of this 3344 MLM.

The main objective of the 3344 maintenance philosophy, incorporated in the Maintenance Library Manual (MLM), is to help the CE repair hardware failures quickly. To accomplish this objective, emphasis is placed on "how to fix" rather than "how it works". For each failure, the "how to fix" approach utilizes the CE resources, the failure isolation techniques, and the individual analysis procedures.

RESOURCES

Although the maintenance philosophy is designed for the Product Trained CE, it is recogonized that there are significant differences in skill levels, experience, and natural ability among CEs. Additional maintenance procedures and sections of the MLM are provided to allow each individual CE to continue with the maintenance procedure until he has exhausted his recources, or until existing policies dictate that he request assistance.

TECHNIQUES

The normal card-isolation technique is to replace or swap the specified cards within a particular maintenance procedure until the failing card is located. At the CE's discretion, and/or depending on the customer's requirements, cards may be swapped between drives and/or modules to speed the isolation. In certain areas where it is not practical to rapidly swap or replace components, information is provided to allow isolation of the failing replaceable unit. (These areas include the Power and Head/Disk Assembly.)

Scoping procedures are provided if components are not available for replacement or swapping. Keep in mind that swapping or replacing is the primary card-isolation technique and that scoping is the secondary technique.

PROCEDURES

Maintenance Analysis Procedures (MAPs) are provided to assist the CE in making decisions (based on sense data, microdiagnostic results, customer data, or visual indications) to isolate the failure to the smallest possible area. MAPs are composed of analysis flowcharts, functional diagrams, and descriptions. Analysis flowcharts and functional diagrams reference other material in the MLM and ALDs to provide a more complete path to failure isolation. The descriptions are provided to help the CE understand the failing operation. The MAPs are made up of the following interacting parts:

Start
Flowcharts
- Entry
- Microdiagnostics
- Replace Or Order
- Isolation
- Interaction With Other MAP Parts

Diagrams
Routines
- Microdiagnostics
- Online Tests (OLTs) - (3340 MLM)
- Special Utility Microdiagnostics

Scoping Procedures
Support Material And References
Support Theory

Start

START 100, in this volume, is always the beginning page for all 3344 maintenance activity. START 100 lists symptoms from visual indications, sense data, console messages, or customer information to point to the correct analysis procedure. (For problems not related to the 3344 drive, go to START 100 in the 3340 MLM.)

FSI

When instructed to exit to the FSI section, use the FSI section in the appropriate MLM (3340 or 3344).

Flowcharts

(For a complete coverage of the blocks used in the flowcharts, refer to the LGND section.)

ENTRY

Entry into the flowcharts is made from START, the Microdiagnostic Error Code Dictionary, or another flowchart.

MICRODIAGNOSTICS

The MAP flowcharts show the CE when to run microdiagnostics. If the tests fail, a base or reference point is established (even on intermittent errors). The microdiagnostics are also run to verify repairs.

MICRO 10

Microdiagnostics
Run device checkout microdiagnostics. Start with routine A1.

REPLACE OR ORDER

Replace or Order blocks attempt to call out all possible field replaceable units (FRUs) for a given symptom. The FRUs listed in the Replace or Order blocks are arranged with the most probable unit first, the next most probable unit second, and so on.

Replace or Order
A1H2 A1K2(A1L2) A1F2(A1Q2) If parts are not readily available, order them and continue below.

The Replace or Order blocks appear early in the MAP flowcharts so that:

- They may be used as a shopping list for ordering parts as soon as possible.
- They may be used as a starting point for intermittent failures.

ISOLATION

The MAPs usually list several possible field replaceable units. The CE has the option of three methods to follow when replacing FRUs.

- Replace the first FRU on the list and retest to see if the problem is resolved. If not, reinstall the original FRU, replace the second FRU, and so on until the failing FRU is located.
- Replace half of the FRUs and determine if the failing FRU is among that group. If it is, continue the isolation to the failing FRU. If the failing FRU is not among the first group, reinstall the original FRUs and replace the remaining half. Continue the isolation for that group.
- Replace all the FRUs, return the machine to the customer and defer the isolation procedure until a more opportune time. The CE must use his knowledge of the customer situation, good fiscal management of his territory, and parts availability, to determine the best method for each incident.

INTERACTION WITH OTHER MAP PARTS

The flowchart is the focal point of the Maintenance Analysis Procedure. Since the other MAP components are all integral parts of the procedure, they are tied to the flowcharts in some way, either directly or by reference.

Diagrams

The block diagrams and sequence charts support the flowcharts. They give more detail, such as interconnections between cards, and show specific test points for each function. They include physical location and ALD page references if more specific information is needed. (See LGND 10.) Where necessary, detailed descriptions and scoping information are provided.

Routines

MICRODIAGNOSTICS

Microdiagnostics are the CE's primary tool to help him to duplicate a customer failure and isolate it to a particular functional failure. The microdiagnostic philosophy is provided in the MICFL section. MICRO 1 through MICRO 84 give operating instructions and routine summaries.

ONLINE TESTS (OLTs)

OLTs are secondary tests that allow the CE to test the HDA concurrently with customer programs. (See OLT 1 in the 3340 MLM or the System/3 Diagnostic Users Guide if the storage control is a DSA.)

SPECIAL UTILITY MICRODIAGNOSTICS

Special utility microdiagnostics available to the CE are:

- Dynamic Servo Adjustment
- Reformat CE Tracks Utility
- Tag Cycle Utility
- Device Status Display
- String Switch Test
- Control Interface Bringup Utility

Detailed test descriptions are given in the MICFL section. Operating instructions and routine summaries are presented in MICRO. (See MICRO 1.)

3344 MAINTENANCE PHILOSOPHY

Scoping Procedures

Scoping is used in conjunction with ALDs, diagrams, flowcharts, sense information, and theory of operation. Each MAP handles scoping according to the particular needs of that MAP. Scoping to find a failure is the secondary diagnostic procedure. Swapping or replacing is the primary diagnostic procedure.

MLM page reference	ALD page reference
Scope	
Sweep	2 ms/div
Trigger	
Slope (+)	
A1D2(A1S2)J02	
(Signal name)	
Ch 1 A1E4(A1R4)G04	
(Signal name)	
volts/div	0.1
probe	X10
Ch 2 A1K2(A1L2)B03	
(Signal name)	
volts/div	0.1
probe	X1

Support Material And References

Special references and information, EREP summaries, locations, and sense data are provided in the following MLM sections:

INDEX
MLX
LGND
MSG
SENSE
MICFL
LOC
INST

A summary of the contents of these sections is located on START 20.

Support Theory

A high-level theory of operation is presented in the OPER section of the 3344 MLM to provide a basic overview of 3344 operation.

START 120
MSG 10
MSG 12
MLX

A

A 3344 drive failure is suspected.

Determine the type of unit with the highest failure rate or the one with a known problem and follow the analysis procedure for that device type.

If unable to identify the failing drive choose the 3340 path. If the trouble is not corrected, choose the 3344 path.

The problem is in a 3344 drive

No (3340)

B

START 100
(3340 MLM)

Yes (3344)

#2

Users of this maintenance package must be familiar with the maintenance philosophy of the 3344. If necessary, read the maintenance philosophy on START 55 and then return here.

#3

This table must be read from top to bottom for system priority.
Visually check (or consult operator) to determine if any of the following Failure Symptoms exist:

Failure Symptom	Location	Analysis Procedure
Drive or drives fail to come Ready. (For loss of Ready, see Drive loses Ready Symptom/Condition below.)		**START 140, Entry A**
Access mechanism out of control (noisy or erratic). Suspect operation may result in mechanism damage.		**ACC 600, Entry B**
Ready lamp fails to turn off.		**HDA 110, Entry A**
Spindle motor brake is noisy.		**HDA 110, Entry A**

1

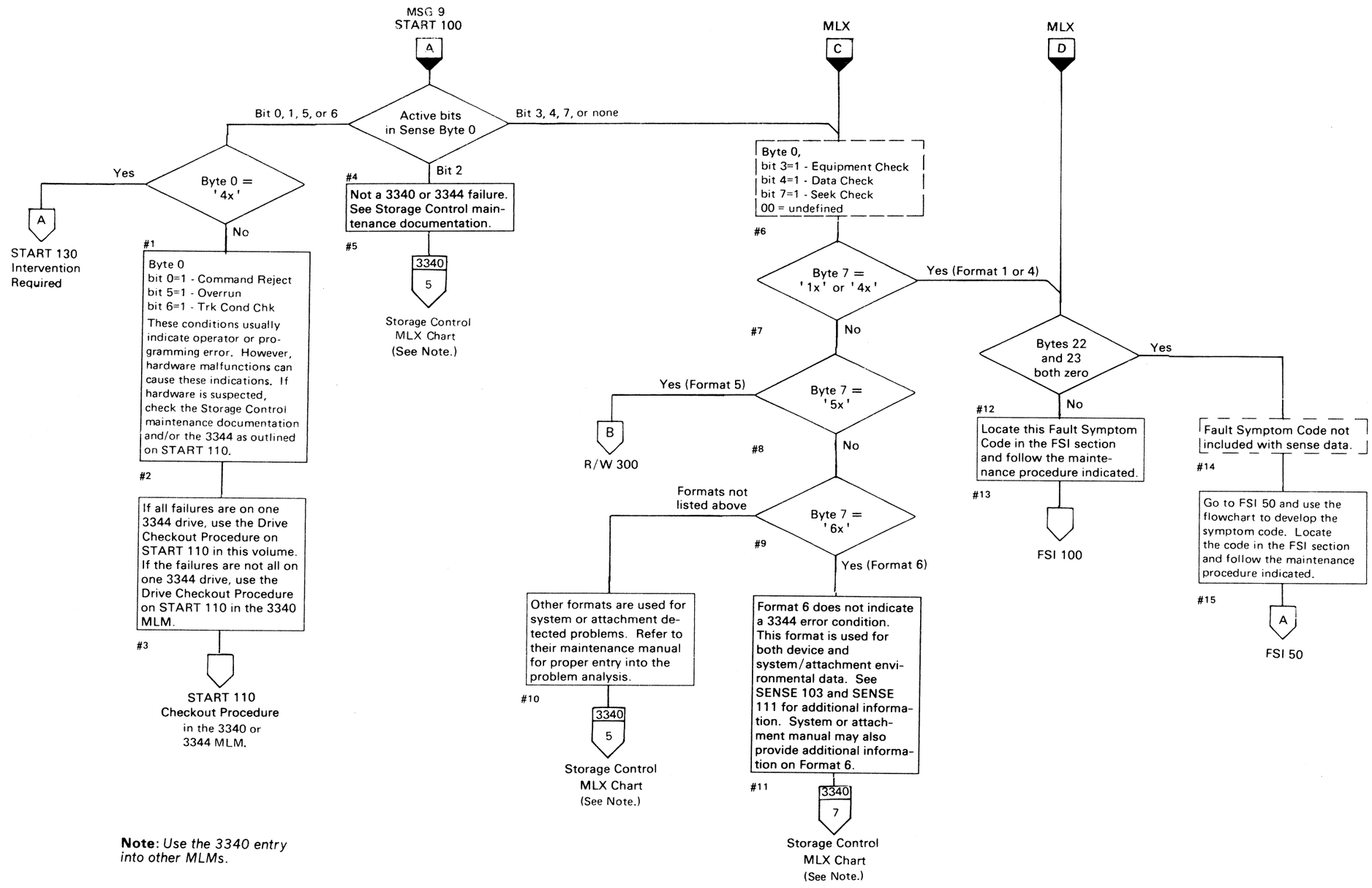
MLX

B

1

Gather failure information and determine which of the following Symptoms/Conditions best describes the suspected failure (or failure information).
More than one path may exist.

Symptom/Condition	Notes	Analysis Procedure
Sense data is available.	If multiple controllers are on one interface or switch unit and confusing error information is received, see CTL-I 290 for Multiple Controller Check procedure.	**START 101, Entry A**
Console message is available.	Review system documentation for console message information.	**OS – MSG 10** **DOS – MSG 12** **SYSTEM/3–MSG 22**
Drive loses Ready.		**ACC 570, Entry C**
Sense data is not available or not meaningful.	Includes system " hangs" or timeouts.	**START 110** (Checkout procedure)
Degraded performance. Error rates are high.	Requires analysis of history. Run EREP.	**MSG 30,** (3340 MLM)
Missing interrupts.	Usually reported by operator.	DEV-I 274, Entry A
Voltage problem is suspected.	If logic problems are unresolved by other procedures, suspect possibility of voltage (power supply) problems.	**PWR 280, Entry B**
CE Panel does not function correctly.		**PANEL 150, Entry A** (3340 MLM)



Note: *Use the 3340 entry into other MLMs.*

DRIVE CHECKOUT PROCEDURE

3344 SINGLE DRIVE CHECKOUT

To check the entire string, go to START 110 in the 3340 MLM.

1. The drive to be tested must be varied offline from the system to run in inline mode (time sharing with an operating system such as OS).
2. Set the CE Mode switch to A or B to select the drive to be tested.
3. Check that the Ready lamp is on. If the lamp is not on and all switches are in their correct position, go to START 100 and analyze the problem.
4. Load the correct 3344 microdiagnostic disk into the storage control reader. See MICRO 8 and 10 for complete details on the use of the 3340 CE Panel for loading and running microdiagnostics. If the storage control is a System/3 DSA, refer to the System/3 Diagnostic Users Guide for instructions on loading and executing program C12 and microdiagnostics.
5. Enter routine number A1 to run the microdiagnostics listed below. These routines are linked together and the complete sequence runs without intervention. If the routine cannot be loaded successfully, go to PANEL 150 in the 3340 MLM to analyze the problem. Refer to the MICFL section for detailed test descriptions.

   A1 Control Interface and Logic tests
   A2 Device Interface and Logic tests
   B8 HDA/Control Logic tests
   A5 Index/Sector tests
   AD Gap Counter tests
   AF Format Read/Write tests
   B9 Dynamic Servo tests
   AE ECC tests

   If errors occur, refer to the Error Code Dictionary (in the MICRO section of the MLM) and follow instructions for the error(s) encountered. After obtaining all information from the first error, it is recommended that the test be restarted to see if the same Error Code occurs a second time. Intermittent errors do not always stop on the best Error Code to provide easy analysis. It is usually best to use the lowest-order Error Code obtainable (that is, the Error Code in the earliest test routine in the sequence).

   Record all information from all Error Codes and look for some common element that might be helpful. For example, if the same bit position in the received information is always incorrect, it might indicate a Bus In problem.

6. To complete the checkout procedure, the following microdiagnostics should be run. These are not linked. Enter routine and any required parameter(s) as defined in the description in the MICRO section of the MLM (start on MICRO 28). Run the routine to completion.

   AB Random Seek tests
   B1 Read tests
   B2 Write tests

ADDITIONAL TESTING

HDA Checkout Procedure From the System

If it is desired to test an HDA, the following online tests are available:

T3340-PSA Pack Scan A (OLT 22 in the 3340 MLM)
T3340-PSB Pack Scan B (OLT 24 in the 3340 MLM)

Refer to OLT 5 in the 3340 MLM for running instructions. If other tests are desired, use FRIEND. See OLT 26 in the 3340 MLM for a summary of FRIEND operation.

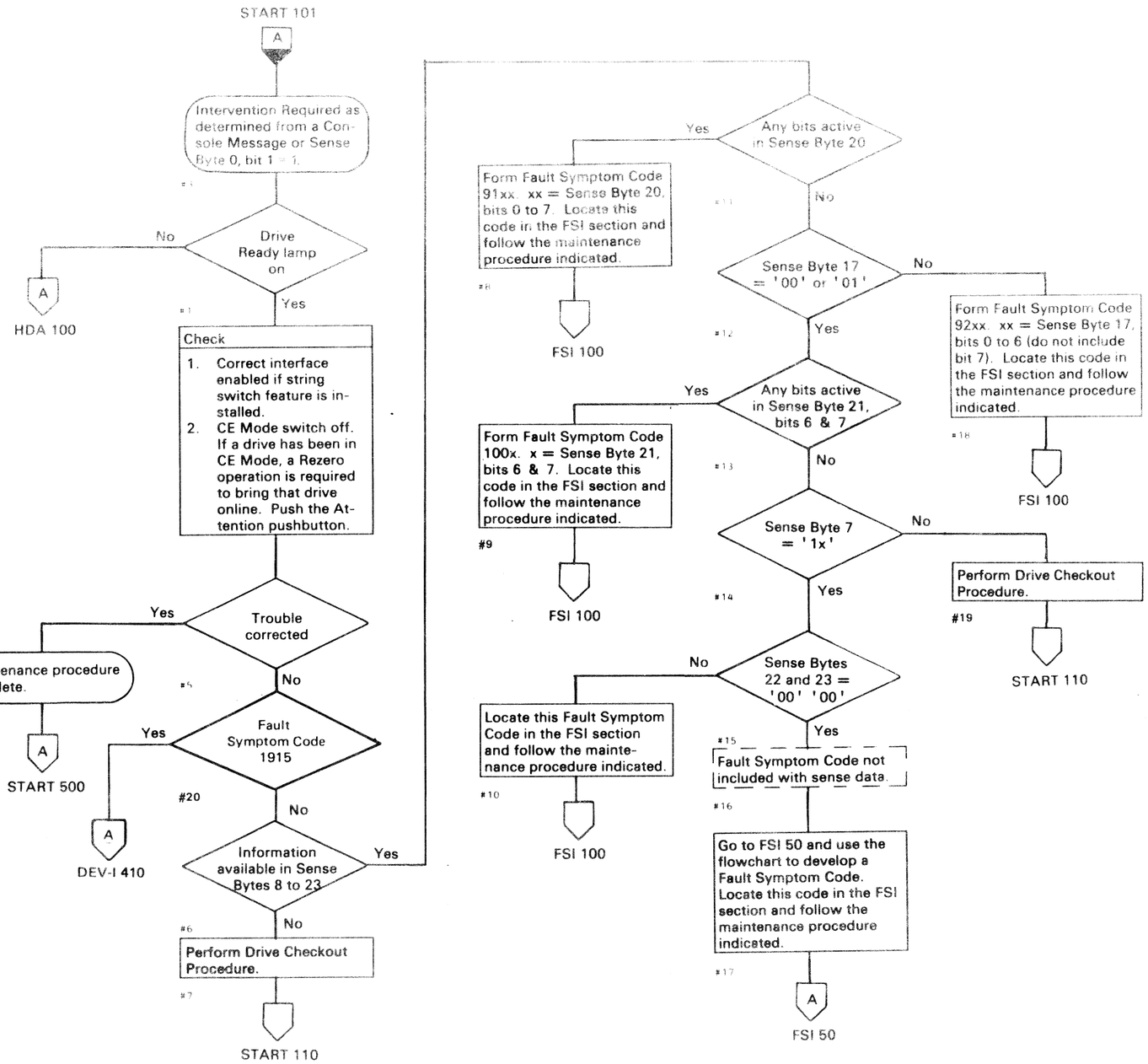
If the storage control is a System/3 DSA, run diagnostic test section C1B (3340 Data Module Scan Program). See the System/3 Diagnostic Users Guide for the loading and running instructions.

INTERVENTION REQUIRED

Intervention Required message is used to indicate to the operator that his intervention is required to make the machine ready for use. It is possible for certain hardware malfunctions to give this indication. This MAP is designed as a guide to the proper area of the MLM when these malfunctions occur.

Intervention Required can be caused by the CE Mode latch being on. To determine if the CE Mode latch is on or does not reset, check:

CE Mode A – A1K2B05 KK180
CE Mode B – A1L2B05 KK180



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DRIVE READY FAILURE ANALYSIS

START 100

A

Drive or drives fail to come Ready.

#1

CP557 (CP568) tripped (see LOC 14)

Yes

#2

No

Reset CP557 (CP568) and proceed. (The CP may not remain reset.)

#3

A

ACC 600

Check

Be sure that all Start/Stop switches are in the Start position.

#4

1. With all Start/Stop switches in the Start position, a failure = no Ready lamp on.
2. All drives in the 3340 string can come Ready even though the Power Sequence Complete relay (K532 in the controller) is not active.

#8

Only one 3344 drive (spindle) fails

No

#5

Yes

Drive DC Power switch set to Both Drives On (See LOC 14)

Yes

#6

No

Set the Drive DC Power switch to the Both Drives On position.

#7

A

PWR 290

Drive now in failing condition

No

D

HDA 100

Yes

D

HDA 110

All 3344 drives in this string fail

Yes

#9

No

No

Only two drives fail

#10

Yes

No

Both drives in the same module

A

HDA 100

#11

Yes

Power Check LED on in failing module

Yes

A

PWR 216

#15

No

The problem is in the drive sequencing circuits. Use PWR 207, PWR 208, and ALD page YB055 to isolate the problem.

Possible causes:

1. Jumper between T501 and T502 in a 3344 module or between T510 and T511 in a 3340 module missing or open.
2. P631, P646, P647, P648, or P514 in failing module.
3. P513 in adjacent 3340 module.
4. Sequence Board A (3344) or associated distribution wiring.

When problem is corrected, exit to START 500.

A

START 500

Any 3340-Bx modules in this string

Yes

#12

No

No

Only one 3344 module in this string

A

PWR 202

#13

Yes

Power Sequence Complete LED on

Yes

#14

No

A

PWR 202

Any Start, Stop, or Air LED on (A or B). (3344 Seq Board B)

No

B

PWR 272

Yes

Check

+ 24 Vdc at TP538 on 3340 Sequence Board B in the controller.

#18

+ 24 Vdc present

No

#19

Yes

A

HDA 100

Normal power on indications are:
AC and DC LEDs on in a 3340-Bx module and Power Sequence Complete LED on with Power Check LED off in a 3344-B2.

Check for abnormal Power Sequence LED conditions. The first module in the string with abnormal LED conditions is the failing module.

Failing condition is indicated in

Neither

3344-B2

B

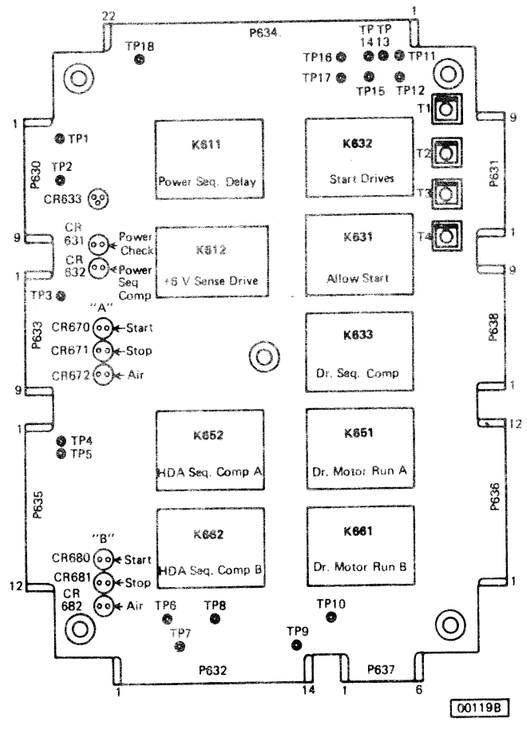
PWR 202

3340-Bx

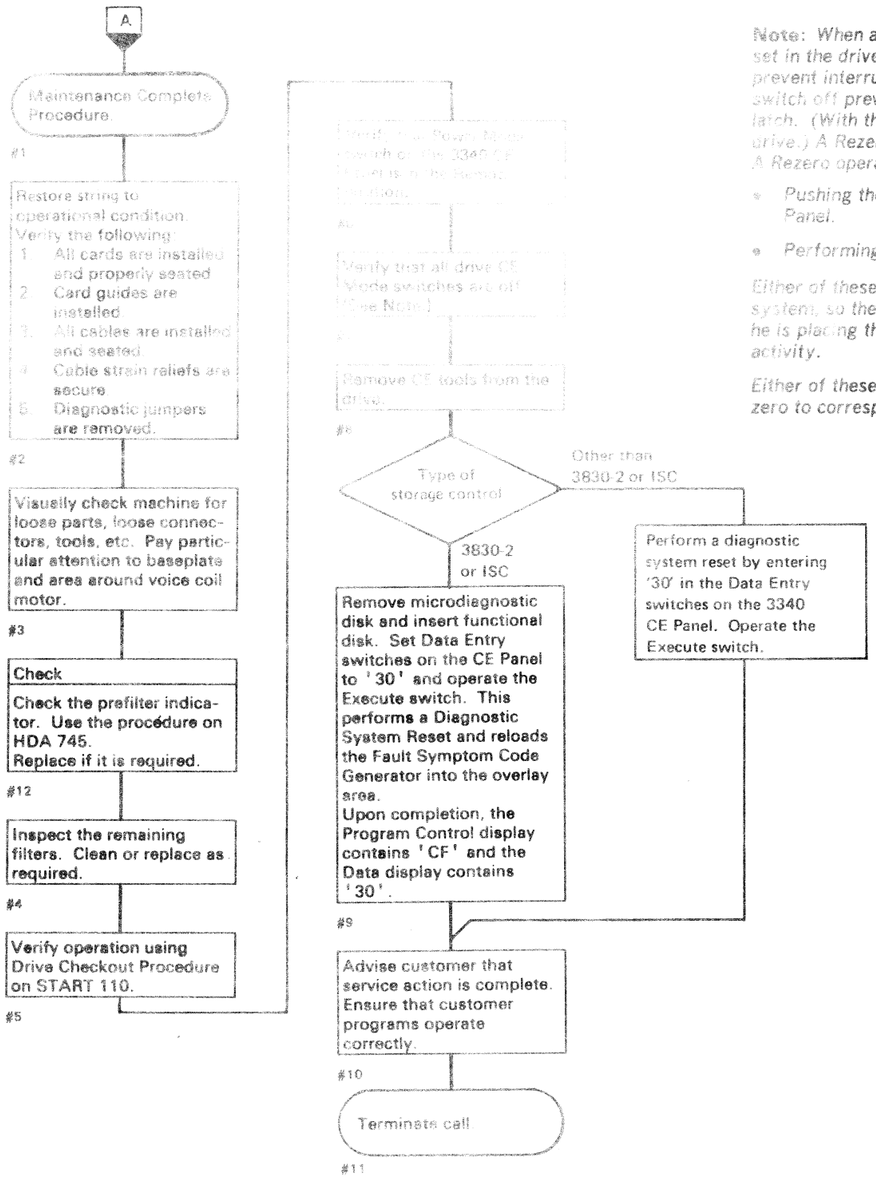
B

PWR 210
(3340 MLM)

3344 Sequence Panel Board B



MAINTENANCE COMPLETE PROCEDURE



Note: *When a 3344 drive is switched to CE Mode, a latch is set in the drive to allow selection with the CE address and to prevent interrupts to the system. Turning the CE Mode switch off prevents CE addressing but does not reset the latch. (With the latch set, the customer cannot address the drive.) A Rezero operation must take place to reset the latch. A Rezero operation can be initiated by:*

- *Pushing the Attention pushbutton on the Operator Panel.*
- *Performing an HDA load cycle.*

Either of these operations generates an interrupt to the system, so they are usually performed by the customer when he is placing the device back online following maintenance activity.

Either of these operations also resets the cylinder address to zero to correspond to the access position.

FSI CONTENTS

FAULT SYMPTOM INDEX USAGE

INTRODUCTION

This page defines the proper use of the Fault Symptom Index (FSI) format and briefly describes how the Fault Symptom Code (FSC) is generated.

The Fault Symptom Codes are listed in sequence within the FSI section. The two high-order numbers of the Fault Symptom Code are the two high-order numbers of the FSI pages. For example, FSC 4944 would be found on an FSI page between 490 and 499.

FSC DETECTION

There are two ways an FSC is received:

- System detection.
- Microdiagnostic background detection.

System Detection

These errors are detected by the system and are posted on the system log (EREP) as an FSC.

Microdiagnostic Background Detection

When running microdiagnostics, it is possible for a hardware failure to occur in an area that has not been previously tested nor is it the main hardware area being tested. This is called a background error and the analysis of the Error Code received gives instructions to run microdiagnostic routine B3. Routine B3 analyzes the status bytes and FSI 60 shows how to develop the FSC.

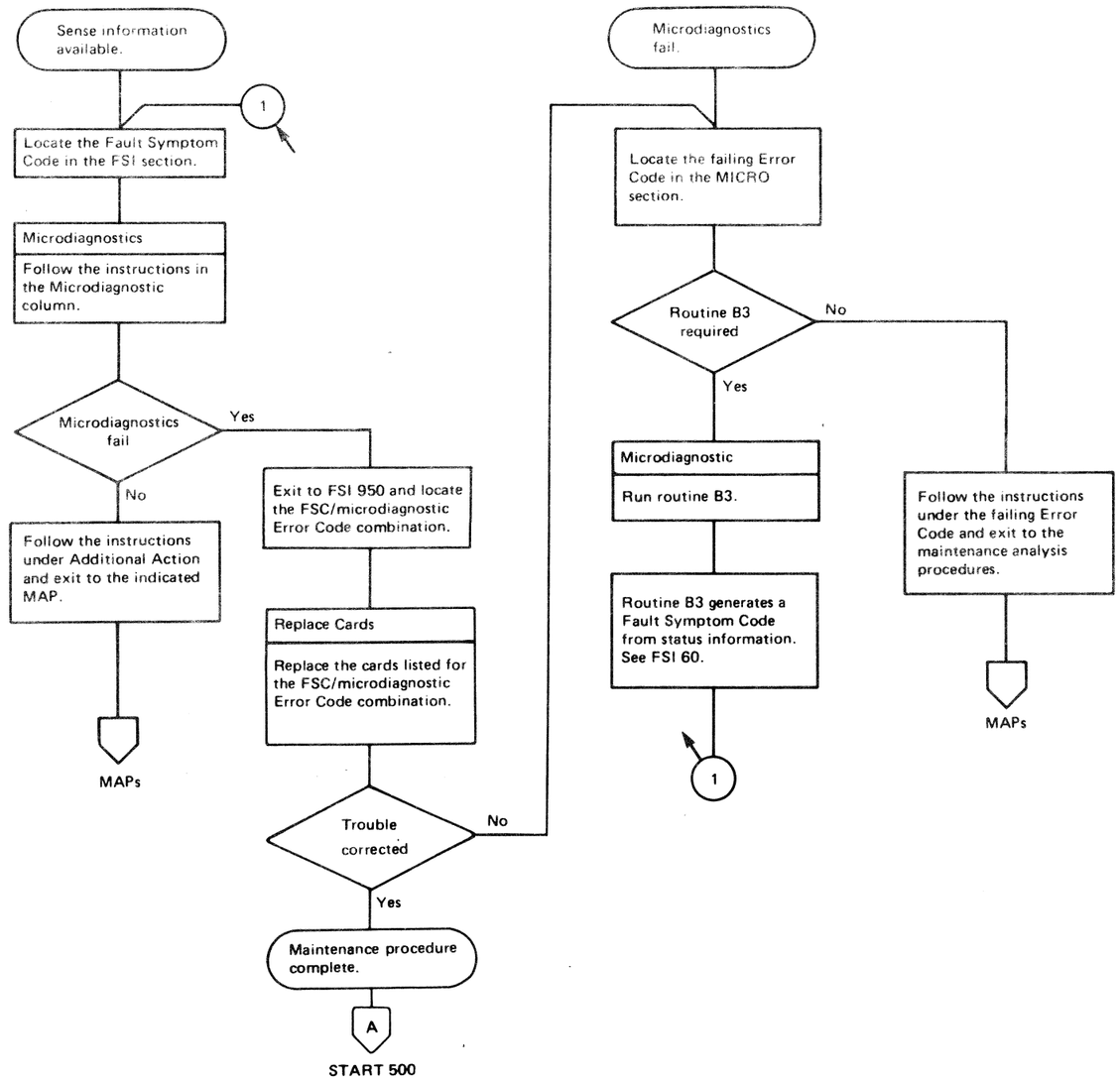
FSI USAGE

The procedure for using the FSI section is to locate the FSC and follow the instructions in each column from left to right.

The flowchart on this page shows the procedure to follow in analyzing both types of FSC.

POSSIBLE CAUSES

The cards listed in the Possible Causes column are in the order of their probability of causing that FSC. The dashed line in the list separates the high probability cards from the low.



FAULT SYMPTOM CODE GENERATION

This chart illustrates how the storage control microprogram develops a Fault Symptom Code from sense information. The 4-character hexidecimal code is presented in Sense Bytes 22 and 23. The chart can be used to manually develop a symptom code if the generator microprogram code is not available in the storage control.

On a 3830-2 and ISC it is necessary to reload the Fault Symptom Code Generator.

To reload the Fault Symptom Code Generator:

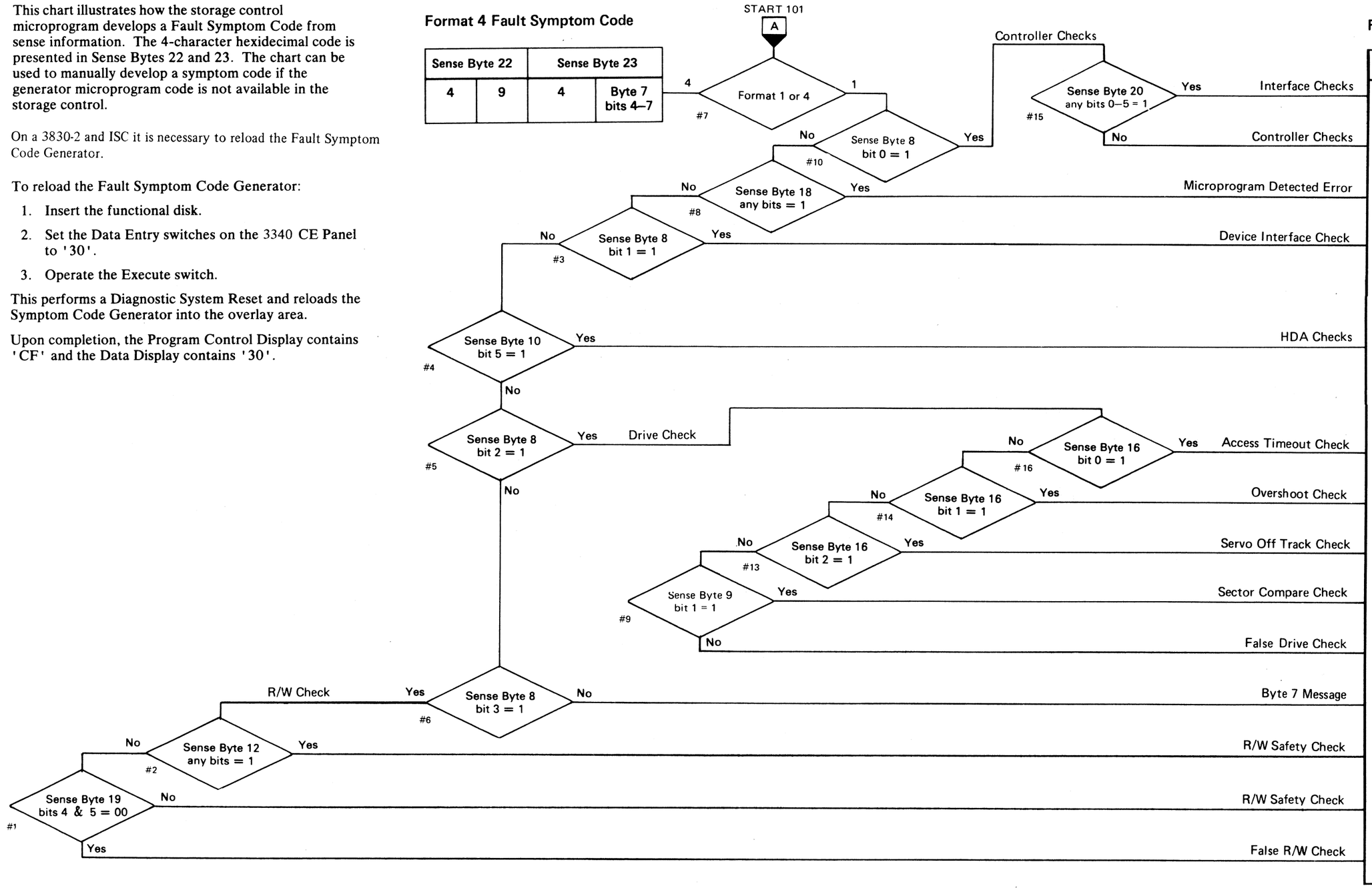
1. Insert the functional disk.
2. Set the Data Entry switches on the 3340 CE Panel to '30'.
3. Operate the Execute switch.

This performs a Diagnostic System Reset and reloads the Symptom Code Generator into the overlay area.

Upon completion, the Program Control Display contains 'CF' and the Data Display contains '30'.

Format 4 Fault Symptom Code

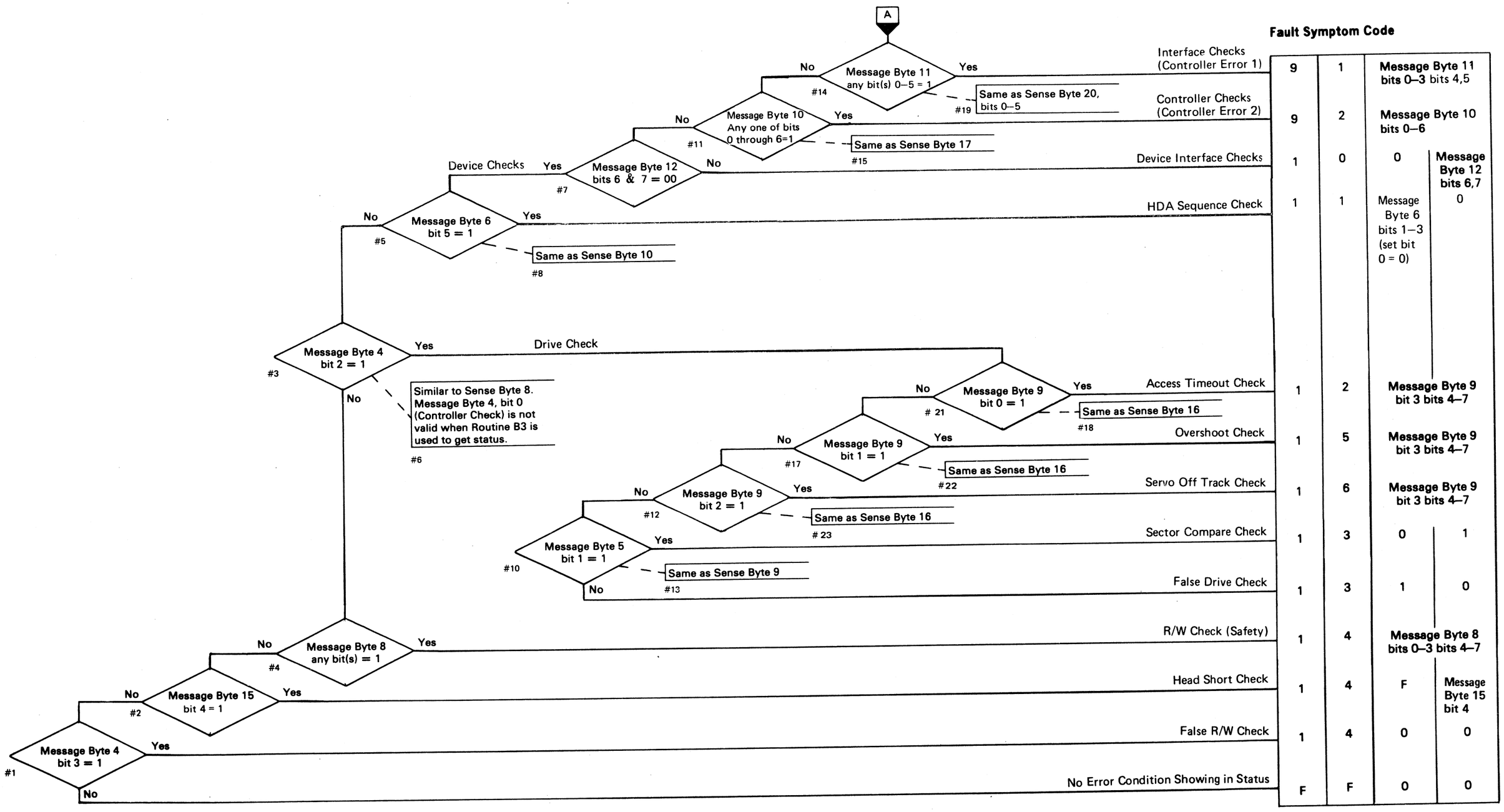
Sense Byte 22		Sense Byte 23	
4	9	4	Byte 7 bits 4–7



Format 1 Fault Symptom Code

Sense Byte 22		Sense Byte 23	
9	1	Byte 20 bits 0–3	Byte 20 bits 4,5
9	2	Byte 17 bits 0–3	Byte 17 bits 4–6
9	0	Byte 18 bits 0–3	Byte 18 bits 4–7
1	0	0	Byte 20 bits 6–7
1	1	Byte 10 bits 1–3	0
1	2	Byte 16 bit 3	Byte 16 bits 4–7
1	5	Byte 16 bit 3	Byte 16 bits 4–7
1	6	Byte 16 bit 3	Byte 16 bits 4–7
1	3	0	1
1	3	1	0
1	9	Byte 7 bits 0–3	Byte 7 bits 4–7
1	4	Byte 12 bits 0–3	Byte 12 bits 4–7
1	4	F	Byte 19 bit 4
1	4	0	0

B3 MICRODIAGNOSTIC SYMPTOM CODE GENERATION (Pass 1)



KL0050 Seq. 2 of 2	2359313 Part No.

441235 28 May 76	441236 30 Sept 76	441239 15 Jun 79	441241 29 Aug 80	

B3 MESSAGE DISPLAY — PASS 2

PROGRAM CONTROL DISPLAY HEX VALUE	MESSAGE B3 BYTE	DATA DISPLAY	0	1	2	3	4	5	6	7	DETAILED DESCRIPTION
E1	1	Physical Drive Identification	A	B	C	D	E	F	G	H	Sense Byte 4 SENSE 106
E2	2	Sense HAR	Fixed Heads (32 to 59)	Fixed Heads (0 to 31)	HAR 32	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1	
E3	3	Sense Difference Counter	128	64	32	16	8	4	2	1	
E4	4	Drive Status	Controller** Check	Device ** Interface Check	Drive ** Check	Read/Write** Check	Online *	HDA Attention	Busy	Seek Complete, Search Sector	Sense Byte 8 SENSE 107
E5	5	Checks/Status (Sense Status 1)		Sector ** Compare Check	Motor at ** Speed Latched	Air Switch ** Latched	Write Enable	HDA Size Bit Fixed Heads Installed	HDA Size Bit	HDA Size Bit	Sense Byte 9 SENSE 107
E6	6	HDA Sequence Control (Sense Status 2)		HDA Sequence* Latch 4	HDA Sequence* Latch 2	HDA Sequence Latch 1	HDA Timer Check Latch	HDA Sequence Check Latch		Odd Track	Sense Byte 10 SENSE 107
E7	7	Loaded Switch Status (Sense Status 3)	Drive Start* Switch	Guardband Pattern	Target Velocity	Track* Crossing		Air* Switch		Motor at * Speed	Sense Byte 11 SENSE 108
E8	8	R/W Safety (Sense R/W)	Multiple ** Head Select Check	Capable/ ** Enable Check	Write ** Overrun	Index ** Check	Delta I** Write Check	Control ** Check	Write ** Transition Check	Write Current ** on Read Check	Sense Byte 12 SENSE 108
E9	9	Access Status (Sense Status 4)	Access ** Timeout Check	Overshoot ** Check	Servo Off ** Track Check	Rezero Mode Latch	Servo * Latch	Linear * Mode Latch	Control * Latch	Wait Latch	Sense Byte 16 SENSE 108
EA	10	Controller Checks (Controller Error 2)	01 = Missing Servo Input** 10 = Phase Error during Write** 11 = Missing data input**		SERDES ** Check	Gap ** Counter Check	Write ** Data Check	Monitor ** Check	ECC ** Check	ECC* Zeros Detected	Sense Byte 17 SENSE 109
EB	11	Control Interface Checks (Controller Error 1)	Control Interface** Tag Bus Parity Check	Control Interface** Bus Out Parity Check	Device ** Selection Check	Device Bus In Parity Check **	Control Interface Bus In Parity Check **	I Write ** Fail			Sense Byte 20 Bits 0–5 SENSE 110
EC	12	Device Interface Checks							Device Bus ** Out Parity Check	Device Tag ** Bus Parity Check	Sense Byte 21 Bits 6 and 7 SENSE 110
ED	13	Target Address Register	Rotational Position Sensing	64	32	16	8	4	2	1	
EE	14	Sense Cylinder Address Register (Switch Feature)	256	128	64	32	16	8	4	2	
EF	15	Status (Sense Status 0)	Direction Bit 1 = IN	Difference 512	Difference 256	Cylinder Address 512	Head Short ** Check			1 (Always On)	Sense Byte 19 Bits 4 and 7 SENSE 109
CE		Routine Number	1	0	1	1	0	0	1	1	MICRO 36

**Indicators that are normally on with no error condition, Ready lamp on, and HDA sequence at State 6.*

*** Error or check condition.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1000	False Device Interface Check	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on A1 Board first. For multiple drive failures, replace cards on A2 Board in the controller first. 2. Check the cable connector seating for cable group 1. See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1K2 (A1L2)*	A2L2	DEV-I 116	C
1001	Device Interface Check – Tag Bus Parity error			A1K2 (A1L2)*	A2L2	DEV-I 140	B
1002	Device Interface Check – Bus Out Parity error			A1K2 (A1L2)*	A2F2 A2G2* A2L2	DEV-I 400	A
1003	Device Interface Check – Tag Bus and Bus Out Parity error		1. Replace cards listed in Possible Causes column in the order shown. For single drive failures, replace cards on A1 Board first. For multiple drive failures, replace cards on A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1K2 (A1L2)*	A2G2* A2L2	DEV-I 112	B

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODES – 11XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
11XX	HDA Sequence Check This indicates either an initial status problem was detected during the sequence from State 0 to State 6 (Ready), or a run status problem was detected while in State 6.	Was this FSC generated by running routine B3? YES Run microdiagnostic routine BA. See MICRO 76 for instructions. Exit to the MICRO section and follow the instructions under the first failing Error Code. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Swap or replace the following relays: K652 (K662) K632 K631 K633 K651 (K661) 2. Replace cards listed in Possible Causes column in the order shown. 3. Exit to MAP Entry.	A1C2 (A1T2)** A1F2 (A1Q2) A1D4 (A1S4)** --- A1K2 (A1L2)* A1E2 (A1R2) A1D2 (A1S2)** A1C4 (A1T4)** A1H2 (A1N2)		HDA 110	B

*When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

**When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1200	Access timeout error during Recalibrate, State 0 – Move Out	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check for intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB – Enter AB, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Power Amp Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check that the VCM terminals A and B are tight. (For details, see LOC 16). 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1D2 (A1S2)** --- A1D4 (A1S4)** A1C2 (A1T2)** A1C4 (A1T4)** A1G2 (A1P2) A1F2 (A1Q2)		ACC 600	A
1201	Access timeout error during Recalibrate, State 1 – Reset			A1E2 (A1R2) --- A1C2 (A1T2)** A1C4 (A1T4)** A1F2 (A1Q2) A1K2 (A1L2)* A1H2 (A1N2)		ACC 600	A
1206	Access timeout error during Rezero, State 6 – Rezero Linear Mode			A1D2 (A1S2)** A1C4 (A1T4)** A1E2 (A1R2) A1D4 (A1S4)** A1C2 (A1T2)** Pwr Amp P532 (P542)** A1G2 (A1P2) A1F2 (A1Q2)		ACC 600	A
1208	Access timeout error during Seek, State 8 – Decelerate			A1E2 (A1R2) --- A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** A1G2 (A1P2) Pwr Amp P532 (P542)**		ACC 630	A
120A	Access timeout error during Seek, State A – Accelerate			A1E2 (A1R2) --- A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** A1G2 (A1P2) Pwr Amp P532 (P542)**		ACC 630	A

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 12XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
120C	Access timeout error during Seek, State C – Seek Linear Mode	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check for intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB – Enter AB, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Power Amp. Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check that the VCM terminals A and B are tight. (For details, see LOC 16.) 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** A1G2 (A1P2) Pwr Amp P532 (P542)**		ACC 630	A
120E	Invalid timeout error posted during Seek, State E – On Track			A1E2 (A1R2) A1C4 (A1T4)** – – – – – – – – – – – A1C2 (A1T2)** A1D2 (A1S2)** A1D4 (A1S4)** A1K2 (A1L2)* A1H2 (A1N2)		ACC 600	A
1210	Access timeout error during Rezero, State 10 – Move Out			A1D4 (A1S4)** A1D2 (A1S2)** A1G2 (A1P2) – – – – – – – – – – – A1E2 (A1R2) A1C2 (A1T2)** Pwr Amp P532 (P542)** A1C4 (A1T4)** A1F2 (A1Q2) A1H2 (A1N2) A1J4 (A1M4)		ACC 600	A
1212	Access timeout error during Rezero, State 12 – Turn Around			A1E2 (A1R2) A1C4 (A1T4)** A1D4 (A1S4)** – – – – – – – – – – – A1C2 (A1T2)** A1D2 (A1S2)** Pwr Amp P532 (P542)** A1G2 (A1P2) A1F2 (A1Q2) A1H2 (A1N2) A1J4 (A1M4)		ACC 600	A

**When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 12XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1216	Access timeout error during Rezero, State 16 – Move In	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.*	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Power Amp. Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check that the VCM terminals A and B are tight. (For details, see LOC 16.) 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1C4 (A1T4)** A1D4 (A1S4)** A1E2 (A1R2) – – – – – – – – – – A1C2 (A1T2)** A1D2 (A1S2)** Pwr Amp P532 (P542)** A1G2 (A1P2) A1F2 (A1Q2) A1H2 (A1N2) A1J4 (A1M4)		ACC 600	A
12XX	Access timeout error during an invalid control state	Microdiagnostic fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check tor intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB – Enter AB, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.		A1E2 (A1R2) A1K2 (A1L2)* A1F2 (A1Q2) A1G2 (A1P2) A1H2 (A1N2) A1J4 (A1M4)		ACC 600	A

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

**When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 13XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1301	Sector Compare This indicates that a Sector Compare was not received within two Index Marks (one complete revolution of the disk).	Was this FSC generated by running routine B3? YES Exit to RPI 300, Entry A. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations and R/W 370 for cable diagrams. 2. Replace cards listed in the Possible Causes column in the order shown. 3. Exit to MAP Entry.	A1J4 (A1M4) A1E2 (A1R2) A1D4 (A1S4)** A1K2 (A1L2)* A1G2 (A1P2) A1C2 (A1T2)**		RPI 306	A
1310	False Drive Check This indicates that a Drive Check occurred without a Sector Compare or Access Check.		1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on A1 Board first. For multiple drive failures, replace cards on A2 Board in the controller first. 2. Exit to MAP Entry.	A1J4 (A1M4) A1E2 (A1R2) A1D4 (A1S4)** A1K2 (A1L2)* A1G2 (A1P2) A1C2 (A1T2)**	A2L2 A2G2*	RPI 308	A

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

**When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1400	False Read/Write Check. Sense Bytes 12 and 19 (B3 Message Bytes 8 and 15)	Was this FSC generated by running routine B3? YES Exit to R/W 100, Entry A. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Run microdiagnostic routine B2. Routine B2 fails? YES Exit to Error Code Dictionary in MICRO section and follow the instructions under the first failing Error Code. NO Exit to MAP Entry.		A1D4 (A1S4)** A1H2 (A1N2) --- A1G2 (A1P2)		R/W 100	B
1401	Write Current on Read			A1H2 (A1N2) A1G2 (A1P2) --- A1J2 (A1M2)			
1402	Write Transition Check			A1J2 (A1M2) A1H2 (A1N2) A1G2 (A1P2)	A2T2 A2Q2 A2P2 --- A2S2		
1404	Control Check			A1H2 (A1N2)	A2F2 A2Q2 A2L2		
1408	Delta I Write Check			A1H2 (A1N2) A1J2 (A1M2) --- A1G2 (A1P2)	A2Q2		
1410	Index Check			A1D4 (A1S4)** --- A1H2 (A1N2) A1J2 (A1M2) A1G2 (A1P2) A1K2 (A1L2)* A1J4 (A1M4)			

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

**When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 14XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1420	Write Overrun	Was this FSC generated by running routine B3? YES Exit to R/W 100, Entry A. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Run microdiagnostic routine B2. Routine B2 fails? YES Exit to Error Code Dictionary in MICRO section and follow the instructions under the first failing Error Code. NO Exit to MAP Entry.		A1H2 (A1N2)	A2P2	R/W 100	B
				A1D4 (A1S4)** A1J2 (A1M2) A1J4 (A1M4)	A2Q2 A2F2		
1440	Capable/Enable Check			A1H2 (A1N2) A1E2 (A1R2)			
				A1F2 (A1Q2) A1D4 (A1S4)** A1G2 (A1P2)			
1480	Multiple Chip Select			A1G2 (A1P2) A1H2 (A1N2)			
				A1D4 (A1S4)** A1G2 (A1P2)			
14F8	Head Short Check			A1H2 (A1N2) A1G2 (A1P2)			
14XX	Multiple Read/Write Checks			A1H2 (A1N2) A1D4 (A1S4)** A1K2 (A1L2)* A1G2 (A1P2) A1E2 (A1R2)			

**When replacing A1K2, A1L2, A2G2, A2D2 or A2E2, check the addressing jumpers. See INST 6.*

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 15XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1500	Overshoot Check during Rezero	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 15, Entry A in the 3340 MLM.* Microdiagnostics fail ? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check for intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB – Enter AB, 06, 00 Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Power Amp Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check the HDA carriage for binding. (For details, see HDA 712.) 5. Check that the VCM terminals A and B are tight. (For details, see LOC 16.) 6. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 7. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 8. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** Pwr Amp P532 (P542)** A1G2 (A1P2) A1F2 (A1Q2) A1H2 (A1N2)		ACC 600	A
1506	Recalibrate – Track 0 Overshoot Check						
1508	Overshoot Check during Seek, State 8 – Decelerate			A1D2 (A1S2)** A1G2 (A1P2) A1E2 (A1R2)			
150A	Overshoot Check during Seek, State A – Accelerate			A1C2 (A1T2)** A1C4 (A1T4)** A1D4 (A1S4)** A1K2 (A1L2)* Pwr Amp P532 (P542)**			
				A1C4 (A1T4)** A1E2 (A1R2) A1G2 (A1P2) A1K2 (A1L2)*			
				A1C2 (A1T2)** A1D2 (A1S2)** A1D4 (A1S4)** Pwr Amp P532 (P542)**		ACC 630	A
150C	Overshoot Check during Seek, State C – Linear Mode			A1E2 (A1R2) A1G2 (A1P2) A1D2 (A1S2)**			
				A1C2 (A1T2)** A1C4 (A1T4)** A1D4 (A1S4)** A1K2 (A1L2)* Pwr Amp P532 (P542)**			

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 15XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
150E	Overshoot Check – Lost servo track following	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check for intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB– Enter AB, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Power Amp Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check the Voice Coil using the procedure on HDA 708. 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** A1G2 (A1P2) Pwr Amp P532 (P542)**		ACC 630	A
1510	Overshoot Check during Rezero						
1512	Overshoot Check during Rezero					ACC 600	A
1516	Overshoot Check during Rezero						
15XX	Overshoot Check during an invalid state						

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 16XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
160E	Servo Off Track error during On Track state	Was this FSC generated by running routine B3? YES Exit to ACC 301, Entry B. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop the following microdiagnostic routines individually to check for intermittent failures: Routine B8 – Enter B8, 06, 00. Routine B9 – Enter B9, 06, 00. Routine AB – Enter AB, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out Group 3 – Servo Power Amp Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For detials, see INST 3.) 4. Check the Voice Coil using the procedure on HDA 708. 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)** Pwr Amp P532 (P542)**		ACC 630	A
16XX	Servo Off Track error during an invalid control state or Set Read*Write active during access motion			A1E2 (A1R2) A1K2 (A1L2)* A1H2 (A1N2) A1F2 (A1Q2) A1G2 (A1P2) A1C4 (A1T4)** A1J4 (A1M4)	A2L2 A2G2*	ACC 630	A

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODES – 19XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1910	Error Alert	Follow instructions in the Additional Action column.	1. If there are other device types attached to the storage control, verify that this 3340 is the failing unit. This may be done by checking the channel/unit address on the console or by checking the EREP log information sheet. See the MSG section. 2. Verify that the correct functional microprogram has been loaded. 3. Exit to MAP Entry.		A2D2* | A2E2* | SWFE A2G2* A2L2 --- A2F2 A2Q2	CTL-I 402 (3340)	A
1911	Transmit Target error	Was this FSC generated by running routine B3? YES Exit to RPI 200, Entry C. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES	1. Replace cards listed in the Possible Causes column in the order shown. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1J4 (A1M4) --- A1K2 (A1L2)* A1H2 (A1N2) A1E2 (A1R2) A1G2 (A1P2)		RPI 220	A
1912	Microprogram detected error (detailed information is in Sense Byte 18)		1. Form Fault Symptom Code 900X, where X equals bits 4 to 7 of Sense Byte 18. 2. Exit to FSI 900 and locate 900X.				
1913	Transmit Difference High error	1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for cable group 0. See FSI 940 for cable group locations and DEV-I 100 for a cable diagram. 3. Exit to MAP Entry.	A1G2 (A1P2) A1K2 (A1L2)* --- A1H2 (A1N2) A1E2 (A1R2) A1C2 (A1T2)**	A2F2 A2G2* A2L2	DEV-I 180	C

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

**When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1914	Sync Out timing error	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for cable Group 9. See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.		A2S2 A2G2* A2P2 --- A2Q2 A2K2 A2M2 (SWFE)	DATA 110 (3340)	B
1915	Unexpected File status at initial selection		Exit to MAP Entry.	A1K2 (A1L2)* A1E2 (A1R2) A1D4 (A1S4)** A1G2 (A1P2) A1H2 (A1N2) A1F2 (A1Q2) A1C2 (A1T2)** --- A1D2 (A1S2)**	A2L2 A2F2 A2G2* --- A2K2 A2D2* A2E2* A2H2 } SWFE A2J2 A2M2	START 130	A
1916	Transmit CAR error	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on A1 Board first. For multiple drive failures, replace cards on A2 Board in the controller first. 2. Exit to MAP Entry.	A1G2 (A1P2) A1K2 (A1L2)*		DEV-I 194	D
1917	Transmit HAR error			A1G2 (A1P2) A1K2 (A1L2)* --- A1H2 (A1N2)		DEV-I 230	D
1918	Transmit Difference Counter error			A1G2 (A1P2) A1K2 (A1L2)* --- A1H2 (A1N2)		DEV-I 240	D

**When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*

***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
1919	Unexpected file status during Read IPL		Exit to START 110 and perform the Subsystem Checkout Procedure.				
191A	Seek Verification Check	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Run the following microdiagnostics: Routine B1 – Enter B1, 00. Routine AB– Enter AB, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 3 – Servo Pwr Amp. Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations and LOC 16 for the location on the machine. 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check that the VCM terminals A and B are tight. (For details, see LOC 16.) 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Verify that the Servo Gain adjustment is correct. (For details, see ACC 800, Entry A.) 7. Replace cards listed in the Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1C4 (A1T4)** A1D2 (A1S2)** A1E2 (A1R2) A1G2 (A1P2) --- A1C2 (A1T2)** A1D4 (A1S4)** Pwr Amp P532 (P542)** A1K2 (A1L2)* A1H2 (A1N2) A1J2 (A1M2)	A2L2 A2Q2 A2F2	**ACC 630**	**A**

**When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*
***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
191B	Sector Compare Check if Byte 9, bit 1 is on (B3 Message Byte 5, bit 1) Access Timeout if Byte 16, bit 0 is on (B3 Message Byte 9, bit 1) Access Overshoot if Byte 16, bit 1 is on (B3 Message Byte 9, bit 0)	Was this FSC generated by running routine B3? YES Follow instructions in the Additional Action column. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	Go to FSC 1301 on FSI 130. Go to FSC 12YY starting on FSI 120. *YY* = Sense Byte 16 or B3 Message Byte 9, bit 3 to 7. Go to FSC 15YY starting on FSI 150. *YY* = Sense Byte 16 or B3 Message Byte 9, bits 3 to 7.				
191C	No interrupt from drive (missing Device Attention)	Run Link Series Starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check for a missing or unstable –12 V at A1C4 (A1T4) D06. See PWR 290, Entry B for voltage tolerances and procedures. 3. Exit to MAP Entry.	A1C4 (A1T4)** A1E2 (A1R2) ***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*		DEV-I 274	A

FAULT SYMPTOM CODES – 19XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
191E	Invalid 3344 HDA configuration bit combination.	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150. Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out Group 8 – Control Interface Bus In See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.	A1K2 (A1L2)* A1G2 (A1P2) A1F2 (A1Q2) A1H2 (A1N2) A1D2 (3340)	A2G2* A2F2 A2K2	DEV-I 430	

*Whenever replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
4940	ECC Data Check – HA field	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Exit to MAP Entry.	Exit to MAP Entry.	A1J2 (A1M2) A1H2 (A1N2) A1G2 (A1P2)	A2P2 A2S2 A2Q2 --- A2R4 A2K2 A2T2		
4941	ECC Data Check – Count field				A2T2 A2S2		
4942	ECC Data Check – Key field			A1J2 (A1M2) A1H2 (A1N2) A1G2 (A1P2)	A2P2 A2Q2 A2R4 A2K2		
4943	ECC Data Check – Data field					R/W 300	D
4944	No Sync Byte Found – HA field			A1G2 (A1P2) A1H2 (A1N2) --- A1J2 (A1M2) A1J4 (A1M4)	A2S2 A2P2 A2T2 A2Q2 --- A2K2		
4945	No Sync Byte Found – Count field						

FAULT SYMPTOM CODES – 49XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
4946	No Sync Byte Found – Key field	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Exit to MAP Entry.	Exit to MAP Entry.	A1G2 (A1P2) A1H2 (A1N2) --- A1J2 (A1M2) A1J4 (A1M4)	A2S2 A2P2 A2T2 A2Q2 --- A2K2	R/W 300	A
4947	No Sync Byte Found – Data field						

FAULT SYMPTOM CODES – 90XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9001	Tag Valid missing on Read/Write operation	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Exit to MAP Entry.	A1K2 (A1L2)* A1E2 (A1R2)	A2Q2 --- A2T2 A2K2	CTL-I 250 (3340)	A
9002	Normal or Check End missing following Read/Write or ECC operation	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions.	1. Replace cards listed in the Possible Causes column in the order shown. 2. Check the cable connector seating for the following cable groups: Group 7 – Control Interface Tag In Group 8 – Control Interface Bus In Group A – Control Interface Tag See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.		A2Q2 A2P2 --- A2S2 A2L2 A2T2 A2G2* A2M2 (SWFE) A2K2 A2F2	CTL-I 260 (3340)	A
9003	No response from controller on a Control operation	**Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail ? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for cable group 1. See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1K2 (A1L2)*	A2F2 A2Q2 --- A2D2* } SWFE A2E2* } A2H2 } A2J2 A2L2 A2G2* A2S2 A2P2	DEV-I 400	

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9004	Timeout waiting for Index	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drives failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 7 – Control Interface Tag In Group 8 – Control Interface Bus In See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.	A1H2 (A1N2) A1D4 (A1S4)** A1K2 (A1L2)*	A2Q2 A2F2 A2P2 --- A2S2 A2L2 A2K2	RPI 160	D
9005	ECC Hardware Check		1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 1 – Device Bus Out Group C – CE Panel Data See FSI 940 for cable group locations and DEV-I 100 for a cable diagram. 3. Exit to MAP Entry.		A2Q2 A2K2 --- A2L2 A2P2	DATA 214 (3340)	A
9006	Multiple controllers selected	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 7 – Control Interface Tag In Group 8 – Control Interface Bus In Group 9 – Control Interface Bus Out See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.		A2F2 A2G2* A2D2* (SWFE) A2E2* (SWFE) --- A2L2 A2M2 (SWFE) A2K2 **When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.* ***When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.*	CTL-I 300 (3340)	A

FAULT SYMPTOM CODES – 90XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9007	Preselection Check	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check voltages at the following locations for proper tolerances: A2K2 B11 for +6 V A2L2 B11 for +6 V A2K2 B06 for –4 V See PWR 290, Entry B for procedure. 3. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 7 – Control Interface Tag In Group 8 – Control Interface Bus In See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 4. Exit to MAP Entry.		A2K2 A2G2* A2M2 (SWFE) A2P2 A2Q2 --- A2L2 A2N2 A2S2 A2F2	CTL-I 320 (3340)	A
9008	Repetitive Command Overruns on G1 operations.	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	During orientation it appears that two drives have the same address. 1. Check the addressing jumpers at A1K2 (A1L2) on all drives to verify that none are the same. See INST 16. 2. Verify that the system configuration is not allowing two drives to be selected with the same address. 3. Replace cards listed in the Possible Causes column in the order shown. 4. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 8 – Control Interface Bus In See FSI 940 for cable group locations and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 5. Exit to MAP Entry.		A2Q2 A2K2 --- A2P2 A2L2 A2F2 A2M2 (SWFE)	DATA 90 (3340)	A

* *When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9009	Busy missing after Seek Start is issued	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Loop microdiagnostic routine B8 to check for intermittent failures: Enter B8, 06, 00. Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 3 – Servo Power Amp Group 5 – HDA Servo Group 6 – HDA Head Select See FSI 940 for cable group locations and R/W 370 for cable diagrams 2. Check the –36 volt CP at: CP557 Drive A CP568 Drive B (For details, see LOC 14.) 3. Verify that the bobbin pushrod is removed from the voice coil motor (VCM). (For details, see INST 3.) 4. Check that the VCM terminals A and B are tight. (For details, see LOC 16.) 5. Check that the belt-in-place spring is installed. (For details, see HDA 760.) 6. Replace cards listed in Possible Causes column in the order shown or exit to the MAP Entry for further isolation.	A1E2 (A1R2) A1K2 (A1L2)* A1H2 (A1N2) A1J4 (A1M4) A1G2 (A1P2) A1C2 (A1T2)** A1C4 (A1T4)** A1D2 (A1S2)** A1D4 (A1S4)**	A2F2	ACC 630	A
900A	Physical Address Check – incorrect physical address returned after a drive selection	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Exit to MAP Entry.	A1K2 (A1L2)* *When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6. **When replacing A1C2 (A1T2), A1C4 (A1T4), A1D2 (A1S2), A1D4 (A1S4) or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.	A2G2* A2H2 A2J2 A2D2* A2E2* SWFE	DEV-I 112	B

FAULT SYMPTOM CODES – 90XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
900E	Device Interface failure	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for cable group 0. See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1K2 (A1L2)* A1H2 (A1N2) A1E2 (A1R2) --- A1F2 (A1Q2)	A2F2 --- A2L2	DEV-I 170	B
900F	Attention Check – Device Attention failed to reset	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out Group 8 – Control Interface Bus In See FSI 940 for cable group locations and DEV-I 100 and CTL-I 105 and 113 in the 3340 MLM for cable diagrams. 3. Exit to MAP Entry.	A1K2 (A1L2)* A1H2 (A1N2) A1J4 (A1M4) A1E2 (A1R2) --- A1F2 (A1Q2) A1G2 (A1P2)	A2F2 A2G2* --- A2L2 A2D2* } SWFE A2E2* } SWFE A2H2 } SWFE A2J2 } SWFE	DEV-I 420	A

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9104	I Write Fails	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Exit to MAP Entry.	A1H2 (A1N2)	A2Q2 A2P2 --- A2F2 A2K2	DATA 124 (3340)	A
9108	Control Bus In Parity Check		1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 1 – Device Bus Out Group 8 – Control Interface Bus In See FSI 940 for cable group locations. 3. Exit to MAP Entry.	A1K2 (A1L2)*	A2K2 A2F2 A2S2 --- A2G2* A2P2 A2L2	CTL-I 390 (3340)	A
9110	Device Bus In Parity Check		1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for the following cable groups: Group 0 – Device Bus In Group 1 – Device Bus Out See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1H2 (A1N2) A1K2 (A1L2)*	A2F2 A2K2 --- A2G2*	DEV-I 235	B
9118	Device Bus In Parity Check and Control Bus In Parity Check			A1K2 (A1L2)* A1G2 (A1P2)	A2K2 A2F2	DEV-I 235	C
9120	One of eight (1-of-8) Drives Selected Check The number of drives selected is less than or greater than one.			A1K2 (A1L2)*	A2G2* A2L2 --- A2K2 A2F2	DEV-I 112	B

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODES – 91XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9140	Control Interface Bus Parity Check	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. Note: *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace the cards listed in the Possible Causes column in the order shown 2. Check the cable connector seating for cable group 9. See FSI 940 for cable group locations. 3. Exit to MAP Entry.		A2D2* } SWFE A2E2* } A2G2* A2K2 A2F2	CTL-I 370 (3340)	C
9180	Control Interface Tag Bus Parity Check		1. Replace cards listed in the Possible Causes column in the order shown. 2. Check the cable connector seating for the following cable groups: Group A – Control Interface Tag Out Group C – CE Panel Data See FSI 940 for cable group locations. 3. Exit to MAP Entry.		A2D2* } SWFE A2E2* } A2G2* A2H2 } SWFE A2J2 } A2K2 A2L2 A2F2	CTL-I 380 (3340)	C
91FF	Control Interface Bus In Assembly failure	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. Note: *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Exit to MAP Entry.		A2P2 A2Q2 --- A2K2 A2F2 A2L2	CTL-I 445 (3340)	A
91XX	Some failures cause multiple Fault Symptom Codes		Exit to FSI 914, Entry A.				

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

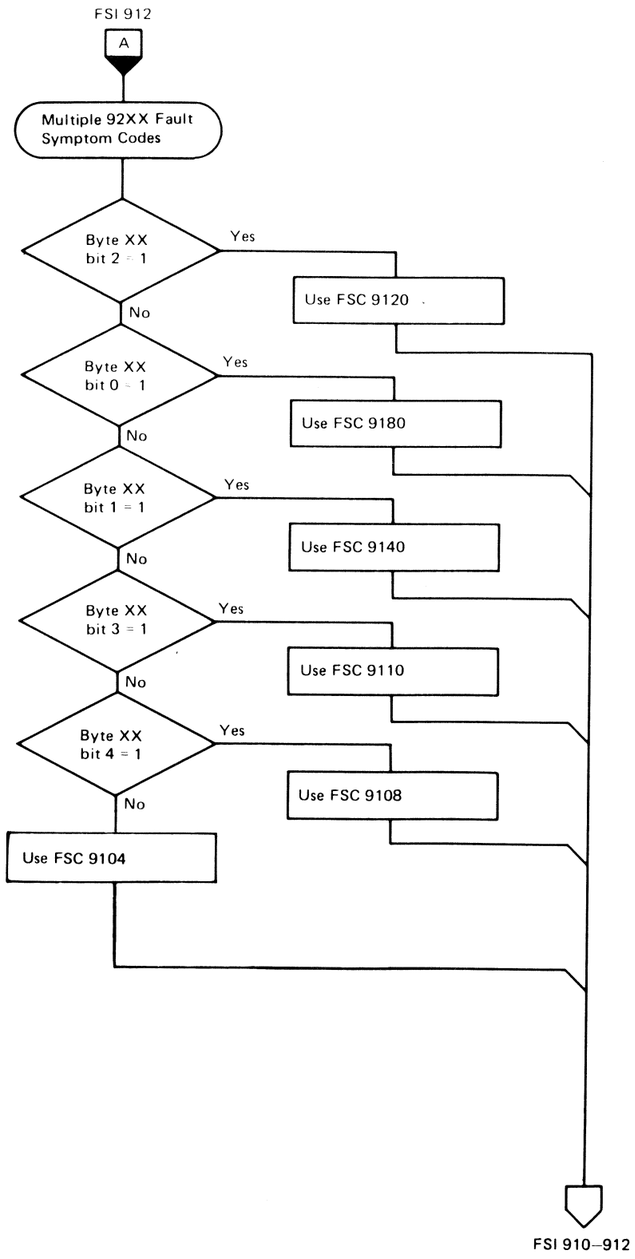
MULTIPLE FAULT SYMPTOM CODES

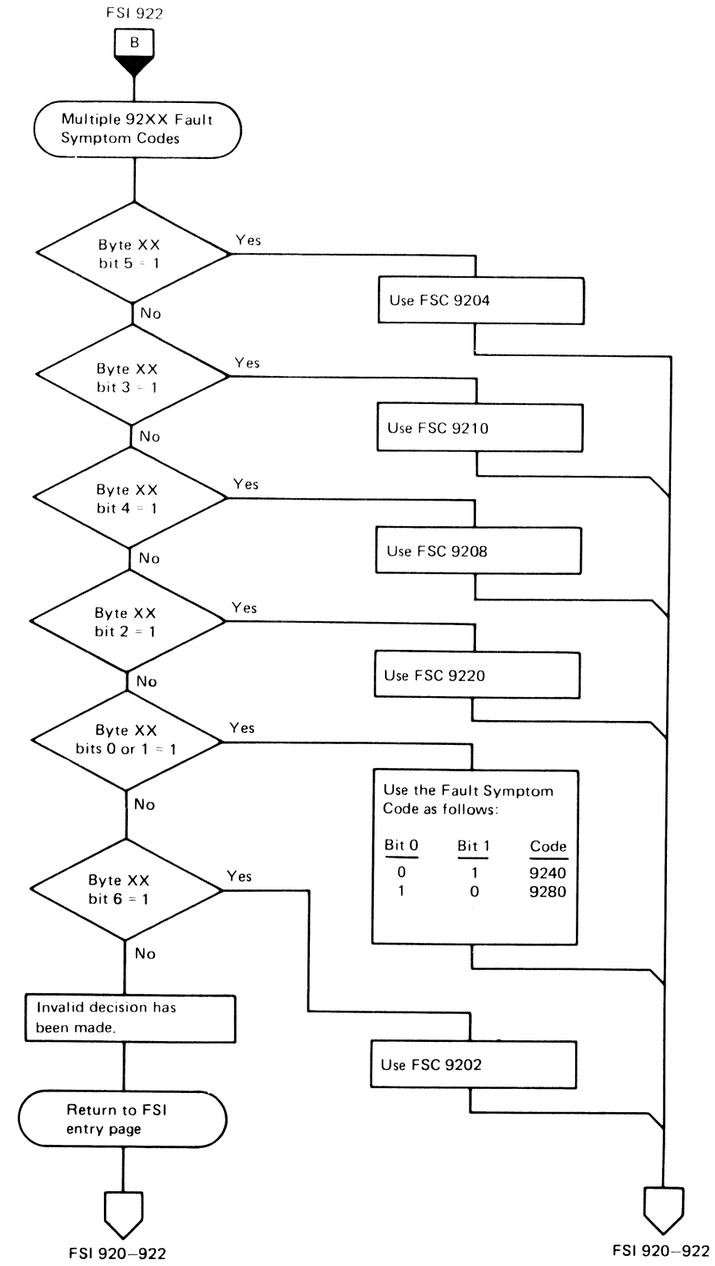
Some malfunctions cause multiple error indications (two or more Fault Symptom Codes at the same time). To properly analyze these malfunctions, a priority of the most meaningful Fault Symptom Code must be established. The flowchart on this page is designed to identify the most meaningful error indicator bit.for combinations of 91XX or 92XX Fault Symptom Codes, where XX is the byte with the multiple error bits on.

Follow the decision blocks at the right and form a new Fault Symptom Code which allows troubleshooting one error at a time.

If the trouble is not corrected, return to the decision block where the Yes exit was taken (on the initial entry decision), and continue by taking the No exit path this time.

It is suggested that a list of the Fault Symptom Codes used during the analysis be kept. This list enables the retracing of the error condition paths that are followed.





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FAULT SYMPTOM CODES – 92XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9200	False Controller error	Is the string switch feature installed on this 3340? YES Exit to CTL-I 110, Entry A in the 3340 MLM. NO Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. 2. Exit to MAP Entry.		A2K2 A2F2 --- A2L2 A2G2* A2D2* A2E2* A2P2 A2Q2	CTL-I 400 (3340)	B
9201	ECC Zero Compare. This indicates the normal completion of a Read or Write operation. *No action required.*		No action required.				
9202	ECC Hardware Check	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Replace cards listed in the Possible Causes column in the order shown. 2. Check cable group 2. See FSI 940 for cable group instructions. 3. Exit to MAP Entry.		A2S2 A2R4 A2P2 --- A2Q2 A2K2 A2T2	DATA 200 (3340)	A
9204	Monitor Check			A1J2 (A1M2)	A2P2 A2L2 A2S2 --- A2K2 A2Q2	DATA 220 (3340)	B
9208	Write Data Check				A2S2 --- A2G2* A2P2 A2K2	DATA 230 (3340)	A
9210	Gap Counter Check				A2P2 A2S2 --- A2G2* A2K2	DATA 240 (3340)	B

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

FAULT SYMPTOM CODES – 92XX

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
9220	Shift Register error	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	1. Verify that the –4 V distribution plugs are properly seated at A2S2 B06 and G06. 2. Replace cards listed in the Possible Causes column in the order shown. 3. Exit to MAP Entry.		A2S2 A2T2 --- A2K2 A2P2 A2F2	DATA 250 (3340)	A
9240	Missing PLO input.		1. Replace cards listed in the Possible Causes column in the order shown. For single drive failures, replace cards on the A1 Board first. For multiple drive failures, replace cards on the A2 Board in the controller first. 2. Check the cable connector seating for cable group 2. See FSI 940 for cable group locations and DEV-I 100 for cable diagram. 3. Exit to MAP Entry.	A1H2 (A1N2)	A2T2 A2Q2 --- A2P2	DATA 260 (3340)	A
9280	PLO Check		1. Replace cards listed in the Possible Causes column in the order shown. 2. Exit to MAP Entry.		A2Q2 A2T2 --- A2S2 A2F2 A2K2	DATA 270 (3340)	A
92XX	Some failures cause multiple Fault Symptom Codes		Exit to FSI 914, Entry B				

FAULT SYMPTOM CODE	ERROR DESCRIPTION	MICRODIAGNOSTICS	ADDITIONAL ACTION	POSSIBLE CAUSES (Listed in order of probability)		MAP	
				A1 Board (Drive)	A2 Board (Controller)	Section	Entry
93XX	Invalid Fault Symptom Code	Run Link Series starting with routine A1. See MICRO 10 for detailed instructions. **Note:** *If the microdiagnostics fail to load, exit to PANEL 150, Entry A in the 3340 MLM.* Microdiagnostics fail? YES 1. Display and record the Error Message Bytes. See MICRO 12 for detailed instructions. 2. Exit to FSI 950. NO Follow the instructions in the Additional Action column.	Replace cards listed in the Possible Causes column.		A2G2*		

When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.

CABLE CHART

This Cable chart shows the specified cables and connectors in the 3344 and associated 3340 A2 Board cables and connectors. When directed to check cables, check every connector in the group.

The chart is valid for the 3340 A2 Board and 3344 A1 Board. It is not valid for the 3340 A1 Board.

See CTL-I 107 for cable checking hints.

Figure 1. Cable Chart for 3340 A2 Board and 3344 A1 Board

Cable Group No.	Cable Group Name		Cable Connector Locations					Reference Diagrams
0	Device Bus In		01A-A2V4*	01E-A1A2	01E-A1V2	01A-A1V2	01A-A1A2	DEV-I 100
1	Device Bus Out		01A-A2V5*	01E-A1A3	01E-A1V3	01A-A1V3	01A-A1A3	
2	Device R/W Data/PLO		01A-A2V2*	01E-A1B2	01E-A1U2	01A-A1U3	01A-A1B3	R/W 326
3	Servo Power Amp.	Drive A Drive B		01A-A1A4 01A-A1V4	P532 P542			LOC 14
4	HDA Sequence Control	Drive A Drive B		01A-A1A5 01A-A1V5	P635 P636			LOC 14
5	HDA Servo	Drive A Drive B		01A-A1B2 01A-A1U2	01C-A1A3 01D-A1A3			LOC 16
6	HDA Head Select	Drive A Drive B		01A-A1Y3 01A-A1Y4	01C-A1A2 01D-A1A2			R/W 370
7	Control Interface Tag In	Basic SWFE A SWFE B	01A-A2C2 01A-A2A2 01A-A2B2	01B-A1G2 01B-A1G2 01B-A1C2	01B-A1E2 01B-A1E2 01B-A1A2			CTL-I 105 and 113 (3340 MLM)
8	Control Interface Bus In	Basic SWFE A SWFE B	01A-A2C3 01A-A2A3 01A-A2B3	01B-A1H2 01B-A1H2 01B-A1D2	01B-A1F2 01B-A1F2 01B-A1B2			CTL-I 105 and 113 (3340 MLM)
9	Control Interface Bus Out	Basic SWFE A SWFE B	01A-A2C4 01A-A2A4 01A-A2B4	01B-A1H1 01B-A1H1 01B-A1D1	01B-A1F1 01B-A1F1 01B-A1B1			CTL-I 105 and 113 (3340 MLM)
A	Control Interface Tag Out	Basic SWFE A SWFE B	01A-A2C5 01A-A2A5 01A-A2B5	01B-A1G1 01B-A1G1 01B-A1C1	01B-A1E1 01B-A1E1 01B-A1A1			CTL-I 105 and 113 (3340 MLM)
B	CE Panel Switch	Basic	01A-A2U4					
C	CE Panel Data		01A-A2U5					
D	SWFE Panel Switch	SWFE	01A-A2V3					

*3340 AI Board Connectors are shown on 3340 MLM DEV–I 305.

3340 A2 Board

FSC/ERROR CODE MATRIX

DESCRIPTION

The chart that starts on FSI 952 contains combinations of Fault Symptom Codes and microdiagnostic Error Codes. The flowchart on this page shows how to use that chart.

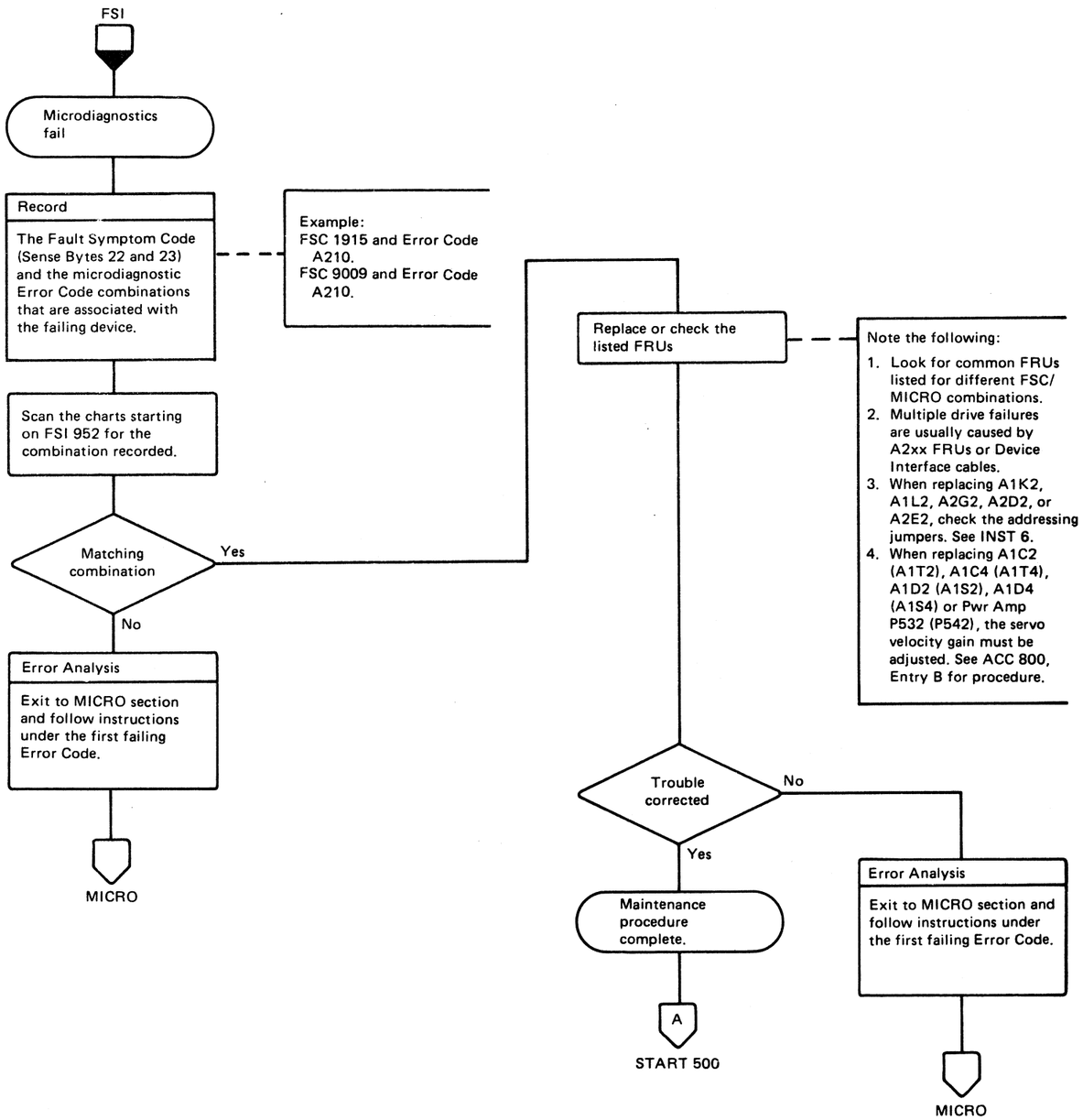
LEGEND

Cbl Grp X – This refers to one of the specific cable groups shown on FSI 940.

HANG – No FSC available but the CPU is in a hang condition.

NOLD – Microdiagnostics cannot be loaded.

TOUT – Functional microcode timed-out.



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FSC/ERROR CODE MATRIX

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
HANG	A120	A2G2	A2F2		
HANG	A14D	A2L2	A2K2		
HANG	A152	A2K2	A2Q2	A2P2	
HANG	A157	A2Q2			
HANG	A158	A2L2	CBL GRP 1		
HANG	A212	CBL GRP 0	A2G2		
HANG	A240	A2G2	A2F2	CBL GRP 0	
HANG	A258	A2K2	A2G2		
HANG	A52A	A2F2	A2K2		
HANG	AF26	A2P2	A2K2	CBL GRP 7	
HANG	NOLD	A2F2	CBL GRP 8	A2G2	CBL GRP A
TOUT	A158	CBL GRP 0	CBL GRP 1	A1K2(L2)	A1H2(N2)
TOUT	A222	A1J4(M4)	A1G2(P2)		
TOUT	A235	A1K2(L2)	A1E2(R2)		
TOUT	A236	A1K2(L2)	A1G2(P2)		
TOUT	A526	A1G2(P2)			
TOUT	A527	A1G2(P2)			
TOUT	A542	A1J4(M4)			
TOUT	A553	A1E2(R2)	A1J4(M4)		
TOUT	B811	A1K2(L2)	A1E2(R2)		
TOUT	B845	A1E2(R2)			
TOUT	B861	A1K2(L2)	A1E2(R2)		
TOUT	B881	A1E2(R2)			
0000	A125	A2K2			
0000	A130	A2G2	CBL GRP A		
0000	A132	A2F2			
0000	A14D	A2P2	A2G2		
0000	A153	A2F2	CBL GRP 8		
0000	A157	A2F2	CBL GRP 8		
0000	A210	CBL GRP 1	A2G2		
0000	A215	A2K2	A2G2		
0000	A216	CBL GRP 1	A2F2		
0000	A224	CBL GRP 1	A2L2		
0000	A240	A2G2	A2F2		
0000	AD04	A1F2(Q2)	CBL GRP 4	CBL GRP 0	
0000	AD15	A2Q2			
0000	AD18	A2G2	A2P2	A2S2	CBL GRP 9
0000	AD1A	A2S2			
0000	AD48	A2G2	CBL GRP A	A2P2	
0000	AEF9	A2P2	A2S2		
0000	AF1A	A2S2	A2P2		
0000	AF1B	A2S2			
0000	AF26	A2K2			
0000	AF9B	A2T2			
0000	B8D4	CBL GRP A	A2G2		
0000	NOLD	A2G2	CBL GRP 9	CBL GRP A	A2F2
1000	A215	CBL GRP 1	A1K2(L2)		
1001	A223	CBL GRP 1	A1K2(L2)		
1001	A224	CBL GRP 1	A1K2(L2)		
1001	A230	CBL GRP 1	A1K2(L2)		

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
1002	A216	A2F2	CBL GRP 1	A1K2(L2)	
1002	A227	CBL GRP 1	A2F2	A1K2(L2)	
1002	A232	A2F2	CBL GRP 1	A1K2(L2)	
1160	A234	A1K2(L2)			
11FF	A234	A1K2(L2)			
1200	A292	A1G2(P2)			
1200	B832	A1D4(S4)			
1200	B837	A1C4(T4)			
1200	B839	A1E2(R2)			
1201	B811	A1F2(Q2)	A1E2(R2)	A1C4(T4)	
1202	B827	A1C4(T4)	A1E2(R2)		
1202	B841	A1D4(S4)			
1206	B844	A1E2(R2)			
120A	B873	A1E2(R2)	A1D4(S4)		
120A	B874	A1E2(R2)			
120A	B8A5	A1E2(R2)	A1C4(T4)		
1310	A135	A2L2	A2G2		
1310	A542	A1D4(S4)			
1310	A553	A1J4(M4)			
1310	A563	A1J4(M4)			
1310	NOLD	A2G2	A2L2		
1400	B8D9	A1H2(N2)	A1D4(S4)		
1401	A294	A1G2(P2)			
1401	AD15	A1G2(P2)	CBL GRP 5		
1401	B8DB	A1G2(P2)	A1J2(M2)	A1H2(N2)	
1402	AD15	A1J2(M2)	A2T2	CBL GRP 6	A1H2(N2)
1402	AF1D	A2P2	A2Q2		
1403	AF9B	A2Q2	A2F2		
1404	AD15	A1H2(N2)			
1404	B8DB	A1H2(N2)			
1408	AD9D	A1H2(N2)			
1408	B20C	A1H2(N2)	A1J2(M2)		
1408	B8DB	A1H2(N2)	A1G2(P2)		
1410	B8DB	A1D4(S4)			
1410	B8F4	A1D4(S4)			
1440	AD15	A1H2(N2)			
1440	AD88	A1H2(N2)	A1G2(P2)		
1440	B8DB	A1H2(N2)			
1440	B8F4	A1H2(N2)			

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
1480	B8D3	A2P2	A2Q2		
1480	B8DB	A1G2(P2)	CBL GRP 6	A1H2(N2)	
14F8	AD15	A1G2(P2)	CBL GRP 5		
14F8	B8DA	A1H2(N2)	A1G2(P2)		
1500	B827	A1C4(T4)			
1500	B828	A1D2(S2)			
1501	A234	A1K2(L2)			
1501	B811	A1E2(R2)			
1506	B827	A1E2(R2)	A1D4(S4)		
1506	B837	A1D2(S2)			
1506	B844	A1E2(R2)	A1D2(S2)		
1508	B832	A1D2(S2)			
1508	B838	A1D2(S2)			
1508	B888	A1D2(S2)			
1508	B892	A1G2(P2)			
1508	B893	A1G2(P2)	A1D2(S2)		
1508	B8A9	A1G2(P2)	A1D2(S2)		
1508	B8AB	A1D2(S2)	A1G2(P2)		
1508	B931	A1D2(S2)	A1G2(P2)		
150A	B874	A1C4(T4)			
150A	B875	A1E2(R2)			
150A	B893	A1G2(P2)	A1D2(S2)		
150C	B8AD	A1D2(S2)	A1G2(P2)		
1600	A240	A1K2(L2)	CBL GRP 0		
1600	B862	A1E2(R2)	A1K2(L2)		
1601	B811	A1E2(R2)			
1601	B829	A1E2(R2)			
1910	A127	A2L2	A2Q2	A2F2	
1910	A136	A2F2	A2G2		
1910	A1A1	A2G2	CBL GRP 9		
1910	NOLD	A2G2	CBL GRP 9	CBL GRP A	A2F2
1911	A220	A1H2(N2)			
1911	A235	A1K2(L2)			
1911	A514	A1J4(M4)	A1K2(L2)		
1911	A515	A1J4(M4)			
1911	B834	A1E2(R2)			
1913	A234	A1G2(P2)			
1913	A235	A1G2(P2)	A2G2	A1H2(N2)	A1K2(L2)
1913	A275	A1G2(P2)			

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
1914	A152	A2K2			
1914	A210	A2G2			
1914	AD17	A2G2	CBL GRP A		
1914	AD18	A2K2	CBL GRP 8	A2P2	
1914	AD48	A2P2	A2S2		
1914	AF1A	A2S2	A2P2		
1914	B8D3	A2P2			
1915	A132	CBL GRP 1	A2F2		
1915	A140	A2K2	A2G2		
1915	A141	A2L2	A2G2		
1915	A150	A2F2	CBL GRP 8		
1915	A157	A2G2			
1915	A1A1	A2G2			
1915	A210	CBL GRP 1	A2L2	A1K2(L2)	A2F2
1915	A211	A1K2(L2)			
1915	A215	CBL GRP 1	A1K2(L2)		
1915	A216	CBL GRP 1	A1K2(L2)	A2F2	
1915	A217	CBL GRP 1	A1K2(L2)		
1915	A220	A1H2(N2)	A1K2(L2)		
1915	A227	A2F2	CBL GRP 1	A1K2(L2)	
1915	A232	CBL GRP 1	A1K2(L2)		
1915	A234	A1K2(L2)			
1915	A235	A1H2(N2)	A1C4(T4)	CBL GRP 0	A1K2(L2)
1915	B810	A1F2(Q2)	A1D4(S4)		
1915	B820	A1E2(R2)			
1915	B822	A1E2(R2)			
1915	B827	A1K2(L2)			
1915	B828	A1C4(T4)	A1E2(R2)		
1915	B831	A1D2(S2)	A1C4(T4)	A1E2(R2)	A1C2(T2)
1915	B832	A1D4(S4)	A1D2(S2)	A1K2(L2)	
1915	B837	A1D2(S2)	A1E2(R2)	A1C4(T4)	A1G2(P2)
1915	B838	A1D4(S4)	A1C2(T2)	A1C4(T4)	CBL GRP 3
1915	B839	A1D4(S4)	A1D2(S2)	A1C4(T4)	A1E2(R2)
1915	B840	A1D4(S4)			
1915	B841	A1C4(T4)	A1E2(R2)	A1D4(S4)	
1915	B842	A1C4(T4)	A1D4(S4)	A1E2(R2)	A1D2(S2)
1915	B844	A1E2(R2)	A1C4(T4)	A1C2(T2)	A1D2(S2)
1915	NOLD	A2G2	A2L2	A2F2	
1916	A210	A1K2(L2)			
1916	A234	A1G2(P2)			
1916	A235	A1G2(P2)	A1K2(L2)	A1H2(N2)	A1E2(R2)
1916	A2B2	A1K2(L2)	A1G2(P2)		
1916	A2B3	A1K2(L2)	A1G2(P2)		
1917	A150	A2F2			
1917	A235	A1G2(P2)	A1H2(N2)		
1917	A272	A1G2(P2)			
1917	A273	A1K2(L2)			
1917	A282	A1K2(L2)	A1G2(P2)		
1917	B8F4	A2G2	A2L2		
1917	NOLD	A2G2	CBL GRP A		

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Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
1918	A235	A1G2(P2)	A1H2(N2)	A1K2(L2)	
1918	A292	A1G2(P2)	A1K2(L2)		
1918	A293	A1G2(P2)	A1K2(L2)		
1918	A294	A1K2(L2)			
191A	A152	A2F2			
191A	A223	A1G2(P2)			
191A	A527	A1G2(P2)			
191A	AD15	A2Q2			
191A	AD37	A2Q2			
191A	AF12	CBL GRP 5	A1G2(P2)		
191A	AF18	CBL GRP 5			
191A	AF53	A2Q2	A2L2		
191A	B827	A1E2(R2)	A1C4(T4)		
191A	B840	A1D4(S4)			
191A	B873	A1E2(R2)	A1C4(T4)	A1G2(P2)	
191A	B874	A1C4(T4)	A1D2(S2)	A1E2(R2)	
191A	B886	A1D2(S2)	A1G2(P2)		
191A	B8AA	A1G2(P2)	A1D2(S2)		
191A	B8AB	A1E2(R2)			
191A	B913	A1G2(P2)			
191A	B925	A1D2(S2)	A1G2(P2)		
191E	A221	CBL GRP 0	A1H2(N2)	A2F2	
191E	A225	A1H2(N2)			
191E	A234	A1G2(P2)	A1K2(L2)		
191E	A235	A1G2(P2)	A1K2(L2)		
191E	A272	A1F2(Q2)	A1K2(L2)		
191E	A274	A1G2(P2)			
191E	A276	A1K2(L2)			
4940	A152	A2Q2	A2K2		
4940	AD78	A2P2			
4940	AF1B	A2R4	A2Q2	A2P2	A2S2
4944	A157	A2Q2			
4944	A216	CBL GRP 1	A2F2		
4944	A234	A1K2(L2)	A1G2(P2)		
4944	A530	A1G2(P2)	CBL GRP 5	A1H2(N2)	
4944	AD0E	A2P2			
4944	AD15	A2T2	A2S2	A2P2	A1J2(M2)
4944	AD18	A2S2			
4944	AD1A	A2S2	A2T2	A2Q2	A2P2
4944	AD78	A2S2			
4944	AD84	A1H2(N2)			
4944	AF1B	A2S2	A2Q2	A2P2	A2T2
4944	B1FD	A1G2(P2)	CBL GRP 6	A1J2(M2)	
4944	B1FF	A1H2(N2)			
4944	B8D2	A2P2			
4944	NOLD	A2Q2	A2P2		
4945	AF1B	A2S2	A2T2		
9001	A140	A2Q2			
9001	AD15	A2T2			

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
9002	A131	A2Q2			
9002	A13C	A2L2	A2K2	A2G2	
9002	A140	A2Q2			
9002	A141	CBL GRP 7	A2K2		
9002	A14C	A2L2			
9002	A14D	A2P2			
9002	A152	A2K2			
9002	A157	A2Q2	A2G2		
9002	A255	A2L2	A2G2		
9002	A526	A1G2(P2)			
9002	AD15	A2Q2			
9002	AD17	A2P2			
9002	AD57	A2Q2	A2P2		
9002	AD67	A2P2	A2Q2		
9002	AD68	A2Q2			
9002	AF1D	A2Q2	A2P2		
9002	B8D3	A2P2	A2Q2	A2G2	A2L2
9002	B8D6	A2Q2	A2P2		
9002	B8D8	A2Q2	A2P2		
9002	B8F5	A1D4(S4)			
9002	NOLD	A2L2	CBL GRP 1	A2G2	
9003	A14D	A2Q2			
9003	A152	A2S2	A2Q2		
9003	A210	CBL GRP 1	A1K2(L2)		
9003	A232	A2F2	CBL GRP 1	A1K2(L2)	
9003	A250	A2L2			
9003	A254	A2F2	A2Q2	A2L2	
9003	AD28	A2P2	A2Q2		
9003	NOLD	A2L2	A2G2		
9004	A123	A2P2	A2Q2		
9004	A124	A2Q2	A2S2	A2P2	
9004	A152	A2Q2	A2K2		
9004	A157	A2L2			
9004	A223	A1K2(L2)			
9004	A521	A1H2(N2)	A1D4(S4)		
9004	A52A	A2F2			
9004	AD15	A2Q2	A2P2	A2F2	A2S2
9004	AD25	A2K2	CBL GRP 7		
9004	B832	A1H2(N2)			
9004	B8D2	A2G2	CBL GRP 9		
9004	B8F5	A2Q2	A2L2	A1D4(S4)	
9005	AE20	A2K2	A2Q2		
9005	AF26	A2Q2			
9006	A120	A2F2	A2G2	CBL GRP 8	
9006	A131	A2G2			
9006	A140	A2K2	CBL GRP 7		
9006	A240	A2G2	A2F2		
9006	NOLD	A2F2	A2G2	A2L2	CBL GRP 8

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Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
9007	A111	A2K2	CBL GRP 7		
9007	A112	CBL GRP 7	A2K2		
9007	A113	A2K2	CBL GRP 7		
9007	A114	CBL GRP 7	A2K2		
9007	A115	A2L2	CBL GRP 7		
9007	A116	CBL GRP 7	A2K2		
9007	A117	A2K2	CBL GRP 8		
9007	A122	A2K2			
9007	A123	A2P2	A2K2		
9007	A126	A2Q2	A2S2	A2K2	
9007	A127	A2L2			
9007	A135	A2L2	A2G2	A2F2	
9007	A158	CBL GRP 0	A1H2(N2)		
9007	A222	A1K2(L2)	A1F2(Q2)		
9007	A233	A1K2(L2)	A1E2(R2)		
9007	B2FC	A1G2(P2)			
9007	B824	A1K2(L2)			
9007	NOLD	A2G2	CBL GRP A		
9008	A131	A2L2	A2K2		
9008	A152	A2Q2	A2K2		
9008	AD15	A2Q2			
9008	AD67	A2P2			
9008	AF15	A2Q2	A2K2		
9008	AF1D	A2Q2			
9008	NOLD	A2K2			
9009	A120	A2F2	CBL GRP 8		
9009	A210	CBL GRP 1	A2L2		
9009	A216	A2G2	A2L2	A2F2	
9009	A217	CBL GRP 1	A2L2		
9009	A223	A2L2	CBL GRP 1		
9009	A227	A2G2	A2F2		
9009	A230	CBL GRP 1	A2L2		
9009	A542	A1J4(M4)			
9009	A556	A1E2(R2)			
9009	B820	A1E2(R2)			
9009	B821	A1E2(R2)	A1K2(L2)		
9009	B827	A1E2(R2)	A1K2(L2)		
9009	NOLD	A2G2	A2L2	CBL GRP 9	
900A	NOLD	A2F2	CBL GRP 8		
900B	NOLD	A2L2	A2G2		
900F	A223	A1K2(L2)	A1H2(N2)	A1G2(P2)	A1F2(Q2)
900F	A227	A1K2(L2)	A1E2(R2)		
900F	A235	A1F2(Q2)	A1E2(R2)		
900F	B813	A1J4(M4)	A1E2(R2)	A1K2(L2)	
900F	B814	A1E2(R2)	A1K2(L2)	A1J4(M4)	
900F	NOLD	A2F2	CBL GRP 8	A2Q2	A2P2

Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
9104	A157	A2Q2			
9104	AD15	A1H2(N2)	A2Q2	A2F2	
9104	AD38	A2Q2	A2P2		
9104	AF1A	A2P2			
9104	AF6A	A2F2	A2P2		
9104	AF9A	A2Q2			
9108	A125	A2S2	A2P2		
9108	A127	A2K2	A2F2		
9108	A132	A2F2	A2K2		
9108	A140	A2Q2			
9108	A14D	A2K2	A2F2		
9108	A153	A2F2			
9108	A157	A2K2	A2S2	A2F2	
9108	A233	A2F2			
9108	A240	A2G2	A2F2		
9108	A254	A2S2			
9108	AD0F	A2F2	A2G2		
9108	AD15	A2S2			
9108	AD1A	A2S2			
9108	AD78	A2S2			
9108	AE10	A2F2	A2K2		
9108	AF1A	A2K2	A2P2	A2F2	
9108	B8D7	A2F2	A2K2		
9108	NOLD	A2F2	A2K2	A2S2	CBL GRP 9
910C	NOLD	A2K2	A2F2		
9110	A127	A2K2			
9110	A158	CBL GRP 0	A2F2	A1H2(N2)	
9110	A220	A1H2(N2)	A2F2	CBL GRP 0	
9110	A225	CBL GRP 0	A2F2	A1H2(N2)	
9110	A234	CBL GRP 0	A2F2	A1H2(N2)	
9110	A235	CBL GRP 0	A1H2(N2)	A2F2	
9110	A281	CBL GRP 0	A2F2	A1H2(N2)	A2K2
9118	A136	A2L2	A2F2		
9118	A233	A2F2			
9118	A235	A1K2(L2)			
9118	A281	A2G2	A2K2	A1K2(L2)	CBL GRP 1
9118	NOLD	A2K2	A2F2		
9120	A127	A2K2	A2G2		
9120	A158	A2G2			
9120	A210	CBL GRP 0	A1K2(L2)		
9120	A211	CBL GRP 0	A2G2		
9120	A212	A1K2(L2)	CBL GRP 1	A2L2	CBL GRP 0
9120	A216	A2L2			
9128	NOLD	A2F2	A2K2		
9130	A210	A1K2(L2)			
9140	A127	A2K2	A2G2		
9140	AD15	A2Q2			

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Fault Symptom Code	Micro Error Code	FRU 1	FRU 2	FRU 3	FRU 4
9148	NOLD	A2K2	A2F2		
9180	A127	A2G2			
9180	NOLD	A2G2	CBL GRP A		
9188	NOLD	A2K2	A2F2		
9200	A127	A2K2	A2F2		
9200	A13C	A2P2	A2L2	A2K2	
9200	NOLD	CBL GRP A	A2G2		
9202	A127	A2S2	A2P2	A2K2	
9202	A150	A2K2	A2F2		
9202	AD17	A2P2			
9202	AD1A	A2S2	A2P2		
9202	AD57	A2Q2	A2P2		
9202	AD78	A2S2	A2R4	A2Q2	
9202	AF1A	A2S2	A2R4	A2P2	
9202	AF9A	A2Q2	A2P2		
9204	A127	A2P2	A2S2	A2L2	A2Q2
9204	A14D	A2Q2			
9204	AFBA	A2P2	A2T2	A2Q2	
9204	AFCA	A2P2			
9204	B8D6	A2S2	A2P2		
9206	AF1A	A2T2	A2S2	A2Q2	A2P2
9208	A127	A2S2	A2K2		
9208	AD1A	A2P2			
9208	A157	A2P2	A2S2		
920A	AD1A	A2S2	A2G2		
920A	AD78	A2S2	A2P2	A2G2	
9210	A127	A2P2	A2S2	A2K2	
9210	AD1A	A2P2			
9210	AD38	A2Q2	A2P2		
9210	AD48	A2P2			
9210	AF16	A2P2			
9210	AF1B	A2S2			
9210	AFBB	A2S2			
9210	B8D6	A2P2	A2Q2		
9212	AD18	A2P2	A2G2		
9212	AD48	A2P2			
9212	AF16	A2S2	A2P2		
9212	AF6A	A2G2	A2P2		
9214	A127	A2S2	A2P2	A2T2	
9220	A127	A2S2	A2K2		
9220	AD1A	A2S2			
9220	AD48	A2Q2			
9220	AF1A	A2S2			
9220	AF1B	A2P2			
9220	AF6A	A2S2	A2P2		
9222	AD15	A2S2			
9222	AD1A	A2S2			
9222	AD78	A2S2			
9222	AF6A	A2P2			
9240	A127	A2T2	A2S2	A2Q2	A2K2
9240	A14D	A2T2	A2L2		
9240	B8D3	A2Q2			
9240	B8D6	A1H2(N2)	A1D4(S4)	CBL GRP 2	A2T2
9244	A127	A2Q2			
9280	A127	A2T2	A2Q2	A2K2	
9280	A14D	A2T2			
9280	A233	A2T2			
9305	NOLD	A2L2			

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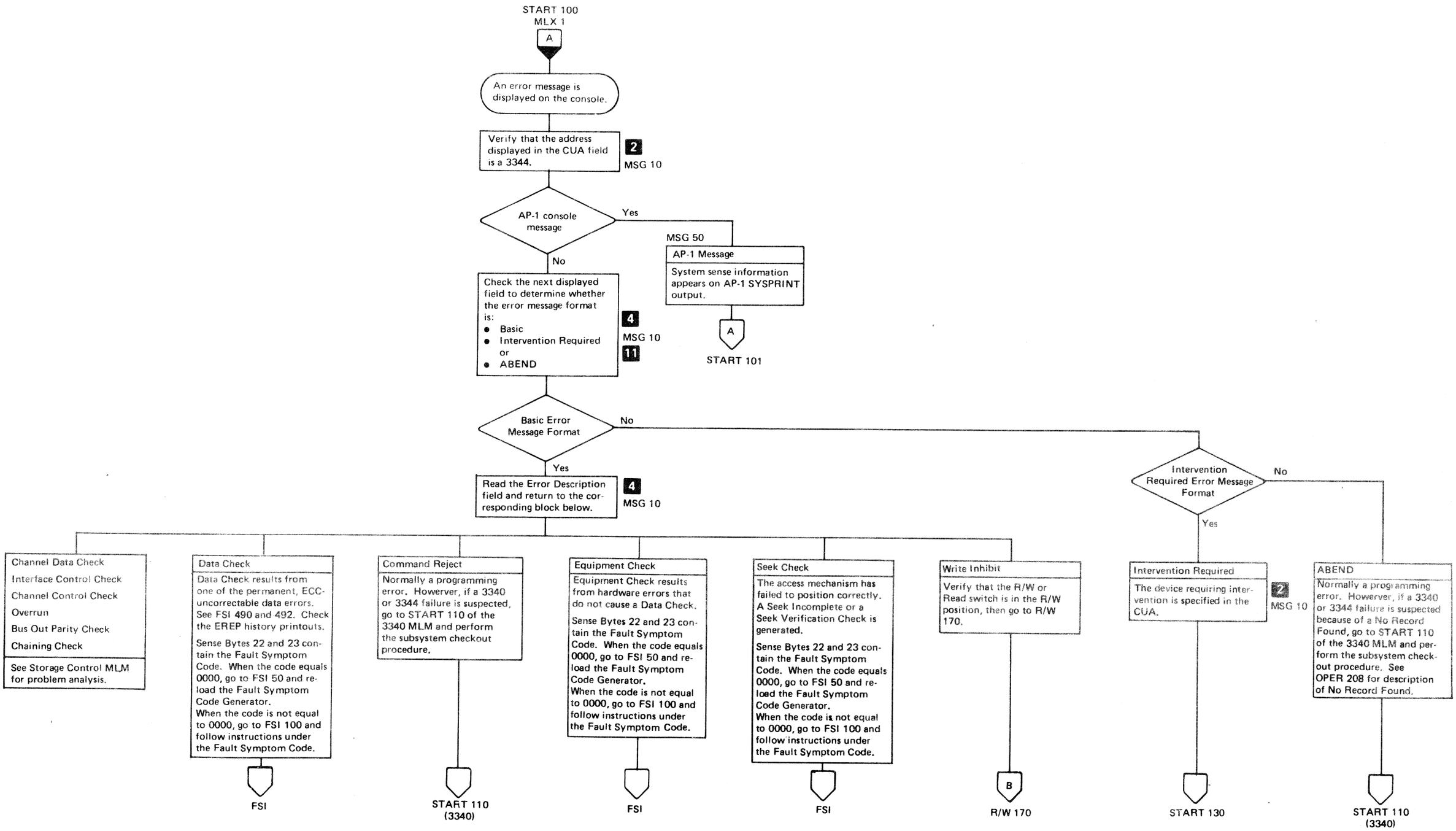
OS/VS CONSOLE ERROR MESSAGE ANALYSIS



OS/VS CONSOLE ERROR MESSAGE ANALYSIS

BASIC ERROR MESSAGE FORMAT

I E A 0 0 0 I	CUA(3)	,	Error Description(3)	,	CMD(2)	,	CSW Stat(4)	,	Sense Data(0 to 24)	,	Seek Address(6)	,	Volume ID(6)	,	Job ID(8)
1	2	3	4		5		6		7		8		9		10

The basic error message format contains the following fields:

1 Message Identifier

The message identifier identifies the type of error message. The content of each message identifier is unique to an operating system.

2 Channel/Unit Address (CUA)

The three characters in the channel/unit address contain the system logical device address.

3 End-of-Field Comma

The end of each field (except the last) is marked by a comma. More than one comma in sequence indicates that one or more fields have been omitted.

4 Error Description

The three characters in the error description contain one of the following:

Error Description	Condition	No. of Lines*	Sense Data	Seek Address
CDC	Channel Data Check	1	N/A	Yes
ICC	Interface Control Check	1	N/A	Yes
CCC	Channel Control Check	1	N/A	Yes
OVR	Overrun	2	0–8 Δ (Line 2)	Yes
BOC	Bus Out Parity Check	2	0–7 Δ (Line 2)	Yes
CHC	Chaining Check	1	N/A	Yes
DCK	Data Check	2	0–23 Δ (Line 2)	N/A
CMD	Command Reject	2	0–8 Δ (Line 2)	Yes
EQC	Equipment Check	2	0–23 Δ (Line 2)	N/A
SKC	Seek Check	2	0–23 Δ (Line 2)	Yes
WRI	Write Inhibit	2	0–8 Δ (Line 2)	Yes

* A basic error message is displayed on one or two lines.
Δ The message identifier and the CUA are displayed with the sense data and the seek address on line 2.

5 Command Code (CMD)

The two characters in the command code contain the command code of the failing CCW.

6 Unit/Channel Status Word (CSW Stat)

The first two characters in the unit/channel status word contain the unit status. The last two characters contain the channel status.

7 Sense Data

The sense data contains 0 to 24 bytes of sense information. When the sense data contains more than 6 bytes, it is displayed on line 2 of a two-line display. Sense data is displayed in hexadecimal pairs.

8 Seek Address (BBCCHH)

The six bytes in the seek address contain the logical address of the track where an error occurs. If an error occurs when trying to obtain the seek address, the six bytes in the seek address contain the last successful seek address. See R/W 400 to convert the logical address to a physical address.

9 Volume ID (Volume Label)

The six characters in the volume identifier contain the customer identification for the logical HDA volume.

10 Job ID

The eight characters in the job identifier contain the name of the job.

INTERVENTION REQUIRED ERROR MESSAGE FORMATS

The intervention required error message formats contain an Intervention Required field 11 not found in the basic error message format.

Device Intervention Required

I E A 0 0 0 A	CUA(3)	,	INT REQ	,	CMD(2)	,	CSW Stat(4)	,	Sense Data(6)	,	Volume ID(6)	,	Job ID(8)
	2		11										

Controller Not Available

I E A 0 0 0 A	CUA(3)	,	INT REQ	,	CC=3/No Paths Available	,	,	,	Job ID (8)
	2		11						

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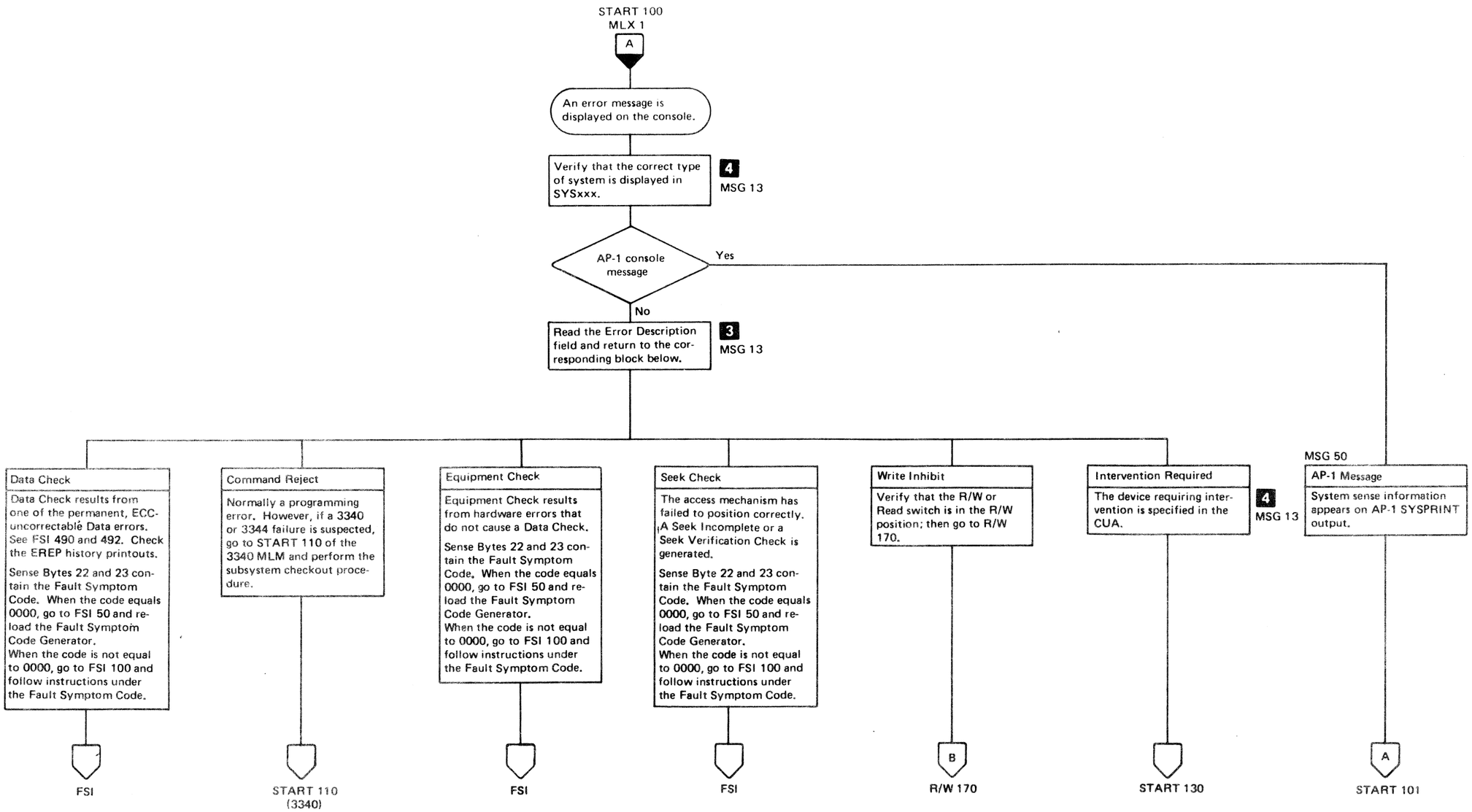
DOS/VS CONSOLE ERROR MESSAGE ANALYSIS MSG 12

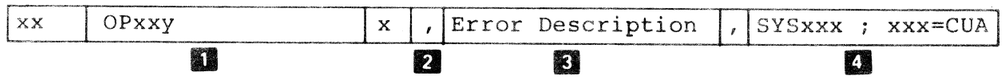


DOS/VS CONSOLE ERROR MESSAGE ANALYSIS

DOS/VS ERROR MESSAGE FORMAT

The DOS/VS error message is displayed on three lines. When the error description 3 contains Intr Reqd (intervention required), only line 1 of the DOS/VS error message is displayed.

Line 1



Line 1 of the DOS/VS error message contains the following fields.

1 Message Identifier

The message identifier contains the following subfields:

- xx, the partition modifier, indicates the partition from which the message was issued.
- OPxxy, the error message code. The xx indicates the type of error. The y indicates the type of operator action required.
- x, the operator response, indicates how the operator should reply to y, the type of operator action required.

2 End-of-Field Comma

The end of each field (except the last) is marked by a comma.

3 Error Description

The error description contains one of the following statements:

Data Check

Cmd Reject

Equip Check

Seek Check

Write Inhibit

Intr Reqd

Only line 1 of the DOS/VS error message is displayed when the error description contains Intr Reqd (intervention required).

4 System Assignment and Channel/Unit Address (CUA)

SYSxxx, the system assignment, contains the type of system (for example, S/360 or S/370) to which the device is connected.

xxx, the channel/unit address, contains the address of the device where the error occurred.

Line 2

Line 2 of the DOS/VS error message contains the following fields:

5 Command Code and Channel Status Word (CCSW)

The first byte, the command code, contains the command of the failing CCW.

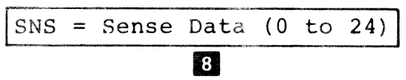
The remaining eight bytes, the channel status word, contain information about the end of the previous CCW.

6 Address of the User Command Control Block (CCB)

7 Seek Address

The six bytes in the seek address contain the logical address of the track where an error occurred. If an error occurs when trying to obtain the seek address, the six bytes in the seek address contain the last successful seek address.

Line 3



Line 3 of the DOS/VS error message contain sense data.

8 Sense Data

The sense data contains 0 through 24 bytes of sense information. When sense data contains less than 24 bytes, the remaining bytes are displayed as zeros. When all Sense Bytes are zero, only the first byte of zeros is displayed.

ERROR CONDITION TABLE

The error condition table is a supplementary aid for the CE in interpreting 3344/3340 error messages.

The error condition table lists the following:

- Sense Byte 0, 1, or 2
- An active sense bit in the Sense Byte. Storage control sets the sense bit.
- The error condition indicated by the Sense Byte/Active Sense Bit combination.
- A description of the error condition.
- An indication of whether the error condition is logged or not.

ERROR CONDITION TABLE

Sense Byte	Active Sense Bit	Error Condition	Description	Logged
0	0	Command Reject	Programming error.	No
0 1	0 6	Command Reject Write Inhibit	The selected drive received a Write command while the R/W or Read switch was in the Read (Write inhibit position).	No
0	1	Intervention Required	The drive is offline in Not Ready or in CE Mode.	No
0 10	1 4 & 5	Intervention Required Drive Power-off	The Power-Off switch on the module is activated or a sequence error occurred.	Yes
0	2	Bus Out Parity	Bus Out Parity error.	Yes
0	3	Equipment Check	This indicates a hardware error.	Yes
0 1	3 0	Equipment Check Permanent	This indicates an uncorrectable hardware error.	Yes
0 1	4 0	Data Check Permanent	This indicates an uncorrectable data error. Storage control issued the maximum number of retries.	Yes
0 1	4 7	Data Check Operation Incomplete	This indicates a correctable data error in the second or in a subsequent overflow segment, excluding the data area of the overflow segment.	No

ERROR CONDITION TABLE (Continued)

Sense Byte	Active Sense Bit	Error Condition	Description	Logged
0 1 2	4 7 1	Data Check Operation Incomplete Correctable	This indicates a correctable data error in the data area of any but the last overflow segment.	Yes
0 2	4 1	Data Check Correctable	This indicates a correctable data error in any data area.	Yes
0	5	Overrun	This indicates a data overrun in the second or in a subsequent overflow segment, or a data overrun during a Format Write command.	Yes
0 1	5 0	Overrun Permanent	Storage control issued the maximum number of retries for a service overrun condition.	Yes
1	1	Invalid Track Format	The capacity of a track has been exceeded.	No
1	2	End of Cylinder	A cylinder boundary has been detected during a multitrack operation.	No
1 1	2 7	End of Cylinder Operation Incomplete	A cylinder boundary has been detected during an overflow operation.	No
1	4	No Record Found	This indicates a programming error. The searched data does not exist on the track being searched.	No
1	5	File Protected	File Mask has been violated during a Seek command or during a Read/Search multitrack operation.	No
1 1	5 7	File Protected Operation Incomplete	File Mask has been violated during a Read overflow or a Write overflow operation.	No
1	7	Operation Incomplete	After initiation of data transfer during an overflow operation, one of the following has occurred: • A defective or an alternate track has been detected. • A seek error has been detected in the second or in a subsequent overflow segment.	No
2	3	Environmental Data Present	Drive error or drive usage statistical data is present.	Yes

EREP (Environmental Record Editing and Printing)

EREP is a program in the operating system (OS/VS) or in the disk operating system (DOS/VS) under which the 3344 is running. EREP edits and prints performance data collected by the Error Recovery Programs (ERPs).

There are two types of performance data collected by the Error Recovery Programs:

Statistical Data

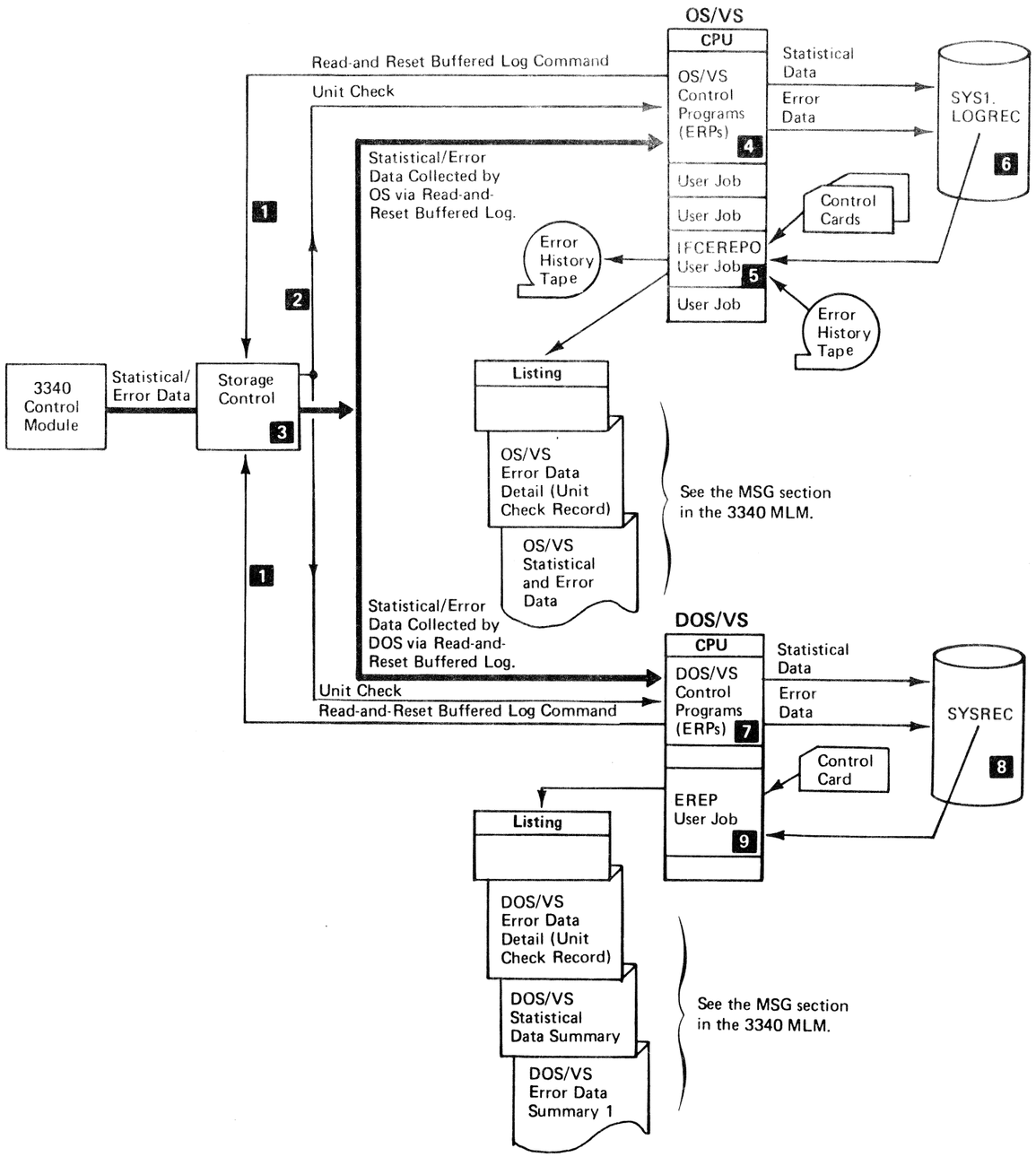
Error Data

HOW TO RUN EREP

Most installations have an established procedure for processing performance data. This procedure should not only include JCL statements for the execution of the EREP program, but should also define the operating practices necessary to periodically print accumulated error records via EREP. Examples of the JCL required to execute EREP are described in the following:

- *System/370 Diagnostic Reference Summary,* Order No. SY25-0512.
- *OS/VS2 System Programming Library: SYS1.LOGREC Error Recording,* Order No. GC28-0677.
- *OS/VS1 SYS1.LOGREC Error Recording,* Order No. GC28-0668.
- *DOS/VS Serviceability Aids and Debugging Procedures,* Order No. GC33-5380.
- *IBM Virtual Machine Facility/370: OLTSEP and Error Recording Guide,* Order No. GC20-1809.

Go to the MSG section of the 3340 MLM for examples of EREP output.



EREP (ENVIRONMENTAL RECORD EDITING AND PRINTING)

STATISTICAL DATA COLLECTION

The statistical data contains the following:

Sense Bytes 0 through 7 (see SENSE 100).

Sense Bytes 8 through 23 (see SENSE 103).

Statistical data is collected as a result of one of the following:

- The operator issued a Halt EOD (End-of-Day) command for OS/VS or an ROD (Record on Demand) command for DOS/VS.
- The EREP program is executed.
- A drive error counter in storage control exceeded 512 correctable Data Checks, 64 Data Retry Checks, or 8 Seek errors.
- A drive usage counter in storage control exceeded $2^{31}-1$ bytes read or $2^{15}-1$ access motions.

Halt EOD or ROD Statistical Data Logging

Halt EOD command, ROD command, or the EREP program cause statistical data to be logged as follows:

1. When the operator issues a Halt EOD or an ROD command, the operating system (OS/VS or DOS/VS) initiates the Read-and-Reset Buffered Log **1** sense command.
2. Read-and-Reset Buffered Log reads the statistical data (Sense Bytes) in the buffered log in storage control **3**.
3. The Sense Bytes are logged in the SYS1.LOGREC (OS/VS) **6** or in the SYSREC (DOS/VS) **8** along with the following:

   Date and time the Sense Bytes were collected.

   Type of device from which the Sense Bytes originated.

   Channel/Unit address of the device from which the Sense Bytes originated.

   Physical Controller/Drive address from which the Sense Bytes originated.

   Volume ID (customer label).
4. Read-and-Reset Buffered Log **1** resets the Sense Bytes in the buffered log in storage control **3**.

Drive Error or Drive Usage Statistical Data Logging

Drive error or drive usage statistical data is logged as follows:

1. When a drive error or drive usage counter in storage control **3** exceeds a certain value, the next Start I/O command to the drive is not executed. Instead, storage control sends a Unit Check **2** to the operating system (OS/VS or DOS/VS).
2. Format 6 Sense Bytes are sent to the Error Recovery Procedures (ERPs) in the OS/VS or DOS/VS control programs **4** or **7** for analysis.
3. The Sense command resets the Sense Bytes in the buffered log in storage control **3**.
4. The ERPs determine that the Sense Bytes contain drive error or drive usage statistical data (see SENSE 100, Byte 2, bit 3 and Byte 7 for Format 6).
5. The operating system re-issues the Start I/O command.
6. The drive error or drive usage statistical data is logged in the SYS1.LOGREC (OS/VS) **6** or in the SYSREC (DOS/VS) **8** along with the following:

   Date and time the Sense Bytes were collected.

   Type of device from which the Sense Bytes originated.

   Channel/Unit address of the device from which the Sense Bytes originated.

   Physical Drive address from which the Sense Bytes originated.

   Volume ID (customer label).

FORCED LOGGING MODE

Forced logging mode is used to collect additional drive error data concerning highly intermittent Seek Checks or highly intermittent Data Checks.

Forced logging mode is initiated by placing the 3830 CE Mode switch in the FORCED LOGGING position.

In forced logging mode, the value in the drive error counter in storage control is disregarded.

ERROR DATA COLLECTION

The error data contains the following:

Sense Bytes 0 through 7 (see SENSE 100).

Sense Bytes 8 through 23 (see SENSE 103).

Error data is collected as a result of one of the following:

- Equipment Check
- Permanent Uncorrectable Data Check
- Correctable Data Check
- Bus Out Parity Check
- Overrun

Error Data Logging

Error data is logged as follows:

1. When the operating system (OS/VS or DOS/VS) detects an I/O interrupt caused by a Unit Check **2**, the error data (Sense Bytes) is sent to the Error Recovery Procedures (ERPs) in the OS/VS or DOS/VS control programs **4** or **7**.
2. The Sense Bytes are recorded in the SYS1.LOGREC (OS/VS) **6** or the SYSREC (DOS/VS) **8** along with the following:

   Data and time the Sense Bytes were collected.

   Type of device from which the Sense Bytes originated.

   Program ID (job name).

   Channel/Unit address of the device from which the Sense Bytes originated.

   Physical Drive address from which the Sense Bytes originated.

   Volume ID (customer label).

   Failing CCW.

   CSW.

   Last Seek Address.

STATISTICAL AND ERROR DATA RETRIEVAL, EDITING, AND PRINTING

Statistical data and error data are retrieved, edited, and printed from SYS1.LOGREC **6** by IFCEREPO (OS/VS) **5** or from SYSREC **8** by EREP (DOS/VS) **9**.

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

AP-1 is an online utility program designed to be run by the customer to verify correct drive operation and ensure that data is readable from the entire volume.

AP-1 is run when the customer suspects single drive failures. AP-1 output (error messages and Head Error tables) should be available when the CE arrives.

The AP-1 program executes two basic testing steps:

1. Drive Test issues Seek, Read, and Write commands to the logical device under test.
2. Data Verification Test (optional) reads the disk surface of the entire logical volume to detect data reading errors.

Output of AP-1 detected errors are printed in the form of console and diagnostic messages. These messages are available following AP-1 execution on suspected single drive failures.

See OS/VS and DOS/VS Analysis Program-1 (AP-1) Users Guide (GC26-3855) for operational information.

DESCRIPTION

Drive Test

The Drive testing sequence is as follows:

1. Seek and read with each physical movable head on physical cylinder 14.
2. Seek and read with all fixed heads.

Note: *Errors that occur during Steps 1 or 2 cause AP-1 to terminate without testing on the CE tracks.*

3. Seek to the CE cylinder and read with all heads.
4. Write on the CE cylinder with all heads.
5. Read on the CE cylinder with all heads.
6. Read multitrack.
7. Test Skip Defect ability.
8. Reformat CE tracks with standard CE data.

Data Verification Test (Optional)

The Data Verification testing sequence is as follows.

FOR OS:

1. Read data on entire cylinder.
2. Read R0s on entire cylinder.
3. Repeat Steps 1 and 2 for each cylinder.

FOR DOS:
Read R0 and all data on each cylinder.

When AP-1 detects an error, a message is printed at the operator console, and a detailed diagnostic message, including the test that failed and a physical head matrix, is printed on the system printer.

DIAGNOSTIC MESSAGES

The AP-1 program prints diagnostic messages on the system printer, not on the operator console. The message contains the failing test name and is followed by information appropriate to the error:

1. The Channel Command Word (CCW) at the failure.
2. The Channel Status Word (CSW) at the failure.
3. The Sense Bytes.
4. The Event Control Block (ECB) completion code if an OS/VS system.

MSG 60 shows the diagnostic messages in alphabetical order, the corresponding channel program that was executing at the time and the meaning of each message. For a description of the channel programs, see MSG 75.

Console Messages

Messages to the operator are printed at the operator console during the AP-1 program. For a description of the console messages, see MSG 125.

Drive Test Messages

During the Drive test, diagnostic messages are issued on SYSPRINT for each error detected during execution of a channel program (see MSG 60).

Event Control Block (ECB) Code

The ECB is a return code from the control program (OS/VS only). It is possible for an error code to be returned without a valid CSW or sense information. If AP-1 detects an error and the status (CSW) or sense information does not appear to be valid, AP-1 should be rerun. Have a system programmer investigate the ECB Code returned in this message (see the Diagnostic Message Issued columns in the tables on MSG 60).

Event Control Block (ECB) Code Definitions

Hex Digit	Description
80	W – Waiting for completion of an event.
40	C – The event has completed.
	One of the following completion codes will appear at the completion of a channel program:
7F	Channel program has terminated without error. (CSW contents useful.)
41	Channel program has terminated with permanent error. (CSW contents useful.)
42	Channel program has terminated because a direct access extent address has been violated. (CSW contents do not apply.)
43	I/O ABEND condition occurred while loading the error recovery routine. (CSW contents do not apply.)
44	Channel program has been intercepted because of a permanent error associated with device end for previous request. You may reissue the intercepted request. (CSW contents do not apply.)
48	Request element for channel program has been made available after it has been purged. (CSW contents do not apply.)
4B	One of the following errors occurred during tape error recovery processing: • The CSW command address in the IOB was zeros. • An unexpected load point was encountered. (CSW contents do not apply in either case.)
4F	Error recovery routines have been entered because of a direct access error but are unable to read Home Addresses or Record 0. (CSW contents do not apply.)
50	Channel program terminated with error. Input block was a DOS-embedded checkpoint record. (CSW contents do not apply.)

Movable and Fixed Head Error Table

In addition to the diagnostic messages, if errors associated with the Read/Write circuitry occurred during the Drive test, AP-1 produces two tables to summarize the errors; a Movable Head Error table and a Fixed Head Error table. These tables are printed on SYSPRINT after the Drive test is completed. MSG 65 shows the format of the Movable Head Error table. The physical heads or tracks are listed in the first column on the left. A 1 is placed in the column corresponding to the type of error detected for a specific head. See MSG 65 for the format of the Fixed Head Error table.

Data Verification Test Messages

During the Data Verification test, diagnostic messages are issued on SYSPRINT if an error is detected. See MSG 70 for a list of messages that may be issued.

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

DRIVE TEST MESSAGES

Use the error information presented here and in the Physical Head Error tables on MSG 65 to aid in analyzing drive failures. See the Channel Command Word (CCW) chain that was used, starting on MSG 75.

Use the Channel Command Word chain and the address (track) to re-create the failure. The Physical Head Error tables provide information supplementing the console and the Environmental Record Editing and Printing (EREP) output.

Diagnostic Message Issued	Channel Program Name	Meaning
AMDET DATA COMPARE ERROR**	AMDET	An error is detected when the wrong record is read.
AMDET TEST*	AMDET	An error is detected when AP-1 attempts to detect an Address Mark and fails.
CLEANUP TEST*	CLEANUP	An error is detected when AP-1 has completed its test and an error occurs during the cleanup of track 1 on the CE cylinder.
FTWRT TEST*	FTWRT	An error is detected when AP-1 attempts to write a full track of data on the CE cylinder and fails.
RDMT DATA COMPARE ERROR*	RDMT	An error is detected when a drive error caused the wrong record to be read.
RDMT TEST*	RDMT	An error is detected when AP-1 attempts to read records on the CE cylinder using the multitrack command and fails.
RECAL TEST*	RECAL	An error is detected when AP-1 attempts to recalibrate the access arm to cylinder 0, head 0 and fails.
RHA HA INCORRECT**	RHA	An error is detected when AP-1 reads a Home Address other than the one expected.
RHA TEST*	RHA	An error is detected when AP-1 attempts to read the CE cylinder Home Address and fails.
RHAFT TEST*	RHAFH	An error is detected when AP-1 attempts to read all the Home Addresses under the fixed heads and fails.
RHAMH TEST*	RHAMH	An error is detected when AP-1 attempts to read Home Addresses under all the movable heads and fails.
RPS TEST*	RPS	An error is detected when AP-1 attempts to read sector or to set sector and fails.
RR01 DATA COMPARE ERROR**	RR01	An error is detected when the record read does not compare equally with the same record previously written.
RR01 TEST*	RR01	An error is detected when AP-1 attempts to read Records 0 and 1 on the CE cylinder and fails.
SD TEST*	SD	An error is detected when AP-1 attempts to write a record with nonzero SD (skip displacement) bytes and rereads it.
SKINCR TEST*	SKINCR	An error is detected when AP-1 attempts to move the access arm and fails.
SKMAX TEST*	SKMAX	An error is detected when AP-1 attempts to move the access arm from cylinder 0 to the maximum cylinder address and fails.
SKRAN TEST*	SKRAN	An error is detected when AP-1 attempts to move the access arm randomly from one cylinder address to another and fails.
SK192 TEST*	SK192	An error is detected when AP-1 attempts to move the access arm from cylinder 0 to physical cylinder 192 and fails.
SNS TEST*	SNS	An error is detected when AP-1 attempts to obtain sense information and fails.
WRT TEST*	WRT	An error is detected when AP-1 attempts to write Records 0 and 1 on the CE cylinder and fails.
WRT WRITE INHIBIT SWITCH ON	WRT	An error is detected when AP-1 attempts to write a record and fails because the R/W or Read switch is in the Read position, or the Read/Write position is defective.
WRTPAD READ WRONG RECORD**	WRTPAD	An error is detected when AP-1 attempts to write a record using the Write Count, Key, and Data command, and read it back. The record read back (which should have been overwritten with zeros) was not as expected.
WRTPAD TEST*	WRTPAD	An error is detected when AP-1 attempts to write a record using the Write Count, Key, and Data command and fails.

*The diagnostic message is followed by:

Failing CCW = hhhh hhhh hhhh hhhh. Failing CCW = is followed by 8 bytes of the failing CCW in hexadecimal digits.

CSW = hh hhhh hhhh hhhh. CSW = is followed by 7 bytes of the CSW in hexadecimal digits.

SNS = hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh. SNS = is followed by 24 bytes of the sense information displayed in hexadecimal digits. For a detailed explanation of sense information, see SENSE 100.

ECB = hh. For a description of the ECB, see MSG 55/

**The diagnostic message is followed by:

EXP = hhhh hhhh hhhh hhhh. EXP = is the expected results and REC = is the received results. EXP = and REC = are followed by 8 bytes of data as follows.

Test Name	Data Expected
AMDET	R2 count
RDMT	R0 count or R1 count
RHA	Home Address CCHH
RR01	R0 count, R1 count, or first 8 bytes of R1 data
WRTPAD	R1 count

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

PHYSICAL HEAD ERROR TABLES

Movable Head Error Table

Head Number	Data Check	Seek Verification Check	Write Check	Data Check CE Cylinder	Data Compare Error
1 00	2	3	4	5	6
01					
02					
03					
04					
05					
06					
07					
08					
09					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					
26					
27					
28					
29					

1 Physical movable head address.

2 A 1 in this column indicates that a Data Check occurred while reading the Home Address on cylinder 4 with the specified movable head. Errors logged in this column cause the test to terminate before performing Write tests on the CE cylinder.

3 A 1 is this column indicates that a Seek Verification Check occurred while reading the Home Address on cylinder 4 with the specified movable head. Errors logged in this column cause the test to terminated before performing Write tests on the CE cylinder.

4 A 1 in this column indicates that a Write Check occurred while writing on the CE cylinder with the specified movable head.

5 A 1 in this column indicates that a Data Check occurred while reading the data previously written on the CE cylinder on the specified movable head.

6 A 1 in this column indicates that data successfully written and read on the CE cylinder did not compare with the pattern written on the specified movable head.

Fixed Head Error Table

Head Number	Data Check	Seek Verification Check	Head Number	Data Check	Seek Verification Check
1 00	2	3	1 30	2	3
01			31		
02			32		
03			33		
04			34		
05			35		
06			36		
07			37		
08			38		
09			39		
10			40		
11			41		
12			42		
13			43		
14			44		
15			45		
16			46		
17			47		
18			48		
19			49		
20			50		
21			51		
22			52		
23			53		
24			54		
25			55		
26			56		
27			57		
28			58		
29			59		

1 Physical fixed head address.

2 A 1 in this column indicates that an uncorrectable Data Check occurred while reading the Home Address on the specified fixed head.

3 A 1 in this column indicates that a Seek Verification Check occurred while reading the Home Address on the specified fixed head.

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

DATA VERIFICATION TEST MESSAGES

Error messages from the Data Verification portion of the AP-1 test are the result of Errors detected may or may not be duplicates of errors that were detected during normal use of the volume. This information should be used to supplement other available Data Check information.

Diagnostic Message Issued	Meaning
DATAVER DATA CHECK CCHH - *hhhh hhhh*[1,2]	A Data Check was detected during the Data Verification test. The Probable cause is a media problem but a drive error may have occurred. The condition that caused the drive error is intermittent or marginal and was not detected during the Drive test. Go to R/W 300, Entry D.
DATAVER DATA CHECKS EXCEEDED THRESHOLD	The number of tracks with Data Checks for the device has exceeded the number of alternate tracks on the volume.
DATAVER DATA FORMAT UNACCEPTABLE ON CYL *hhhh hhhh*[1,2]	Data on the cylinder is written in a format other than the IBM standard format, or an intermittent drive error occurred during the Data Verification test, or the volume under test was accessed by another program and the other program erased an EOD record after it has been read by the Data Verification test and before it has been reread by the test.
DATAVER TEST[2]	A drive error was detected during the Data Verification test.

[1]The logical volume cylinder and head is represented by *hhhh hhhh*. This value is in hexadecimal.

[2]The diagnostic message is followed by: FAILING CCW = *hhhh hhhh hhhh hhhh* CSW = *hh hhhh hhhh hhhh* ECB = *hh* SNS =*hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh* where FAILING CCW = is followed by 8 bytes of the failing CCW in hexadecimal digits, CSW = is followed by 7 bytes of the CSW in hexadecimal digits. ECB = is followed by 2 hexadecimal digits representing the ECB code returned (see MSG 55), and SNS = is followed by 24 bytes of the sense information received in hexadecimal digits.

CHANNEL PROGRAMS FOR AP-1 TESTS

Data Verification Test

Channel Program Name	Channel Program Description Number
READBLD1	1
READBLD2	2
READBLD3	3

Drive Tests In Order Of Execution

Channel Program Name	Channel Program Description Number
RECAL	4
SNS	5
RECAL	4
RHAMH	6
RHAFH	7
RPS	8
SK192	9
SKINCR	10
SKMAX	11
SKRAN	12
RHA	13
WRT	14
RR01	15
RDMT	16
FTWRT	17
AMDET	18
WRTPAD	19
SD	20
CLEANUP	21

Channel Program Descriptions

1. Channel Program for Data Verification Test – READBLD1

   This channel program reads all Count, Key, and Data fields of all records on the volume. The Seek Address is modified to read each succeeding cylinder until all the Count, Key and Data areas on the logical volume have been read. The data is read from the beginning to the end of the cylinder or to an end-of-data record.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine READBLD1.

CCW No.	Command Code Hex	Command Code Description	Address	Flags Hex	Flags Description	Count	Comments	
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0	
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only	
3	08	TIC	CCW4	40	CC		Transfer control to channel program	
4	1A	Read Home Address	buffer	40	CC	5	Position on Home Address	Use CCWs 4 through 9 if DOS/VS
5	16	Read R0	buffer +8	80	CD	8	Read Count for Record 0	
6	16	Read R0	000	70	SLI, SKIP, CC	65535	Read data of Record 0 (no data transferred)	
7	5E	Read Multiple Count, Key, Data	000	70	SKI, SKIP, CC	65535	Read all records on track	
8	9A	Read Home Address Multitrack	buffer	40	CC	5	Position on Home Address of next track	
9	08	TIC	CCW5	00			Repeat to end-of-cylinder or EOD	
4	1A	Read Home Address	000	50	CC, SKIP	5	Position on Home Address	Use CCWs 4 through 7 if OS/VS
5	92	Read Count, Multitrack	buffer	40	CC	8	Count for restart on EOD	
6	0E	Read Key	000	70	CC, SKIP, SLI	65535		
7	08	TIC	CCW2	00		0	Repeat to end-of-cylinder or EOD	

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

2. Channel Program for Data Verification Test – READBLD2

   This CCW chain is used to determine the disk address of the end-of-data record encountered by READBLD1 CCW chain. This CCW chain is also used for reading alternate tracks. The File Mask is set to No Seeks so this CCW chain will stop at the end of the track.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine READBLD2.

CCW No.	Command Code Hex	Command Code Description	Address	Flags Hex	Flags Description	Count	Comments	
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0	
2	1F	Set File Mask	X'58'	40	CC	1	Set File Mask to Read Only, No Seeks	
3	08	TIC	CCW4	40	CC		Transfer control to channel program	
4	1A	Read Home Address	buffer	40	CC	5	Position on Home Address	
5	16	Read R0	buffer +8	80	CD	8	Read Count for Record 0	
6	16	Read R0	000	70	SLI, SKIP, CC	65535	Read data of Record 0 (no data transferred)	Use CCWs 4 through 9 if DOS/VS
7	92	Read Count, Multitrack	buffer +8	40	CC	8	Count for restart on EOD	
8	0E	Read Key, Data	000	70	SLI, SKIP, CC	65535	No data is transferred	
9	08	TIC	CCW7	00				
	31	Search ID Equal	AP1SEEK +2	40	CC	5	Search on EOD record	
4								
5	08	TIC	CCW1	00				
6	92	Read Count, Multitrack	buffer	40	CC	8	Count for restart on EOD	Use CCWs 4 through 8 if OS/VS
7	0E	Read Key and Data	000	70	CC, SKIP, SLI	65535		
8	08	TIC	CCW3	00			Repeat to EOD or end-of-cylinder	

3. Channel Program for Data Verification Test – READBLD3

   This CCW chain is used to restart the READBLD1, READBLD2, or READBLD3 CCW chain when it is broken by an end-of-data record or correctable Data Check. The File Mask is set to No Seeks so this CCW chain will stop at the end of the track.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine READBLD3.

CCW No.	Command Code Hex	Command Code Description	Address	Flags Hex	Flags Description	Count	Comments	
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0	
2	1F	Set File Mask	X'58'	40	CC	1	Set File Mask to Read Only, No Seeks	
3	08	TIC	CCW4	40	CC		Transfer control to channel program	
4	31	Search ID Equal	buffer +8	40	CC	5	Search on EOD record or correctable Data Check	
5	08	TIC	CCW4	00			Repeat search if ID not equal	
6	92	Read Count, Multitrack	buffer +8	40	CC	8	Count for restart on EOD	Use CCWs 4 through 8 if DOS/VS
7	0E	Read Key and Data	000	70	CC, SKIP, SLI	65535	No data is transferred	
8	08	TIC	CCW6	00			Repeat to EOD or end-of-cylinder	
	16	Read R0	buffer	80	CD	8	Read the Count for Record 0	
4								
5	16	Read R0	000	70	SLI, CC, SKIP	65535	Read data of Record 0 (no data is transferred)	
6	23	Set Sector	buffer +8	40	CC	1	Set sector to 127 for the 3350 and 3330 Compatibility Modes, set sector to 063 for 3344.	Use CCWs 4 through 9 if OS/VS
7	96	Read R0 Multitrack	buffer	80	CD	8	Read Count of Record 0	
8	16	Read R0	000	70	SLI, CC, SKIP	65535	Read data of record 0 (no data is transferred)	
9	08	TIC	CCW3	00				

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4. Channel Program for Drive Test – RECAL

   This test issues the Recalibrate command which causes the the access arm to move to cylinder 0 on the logical volume.

   CCWs 1, 2, and 3 are built to IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by the RECAL routine.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	13	Recalibrate	000	60	SLI,CC	1	
5	03	No Operation	000	00		1	To get ending status

5. Channel Program for Drive Test – SNS

   The CCW chain obtains 24 bytes of sense information from the storage control. The sense information is used to determine the drive features.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by the SNS routine.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	04	Sense I/O	buffer	00		24	

6. Channel Program for Drive Test – RHAMH

   This CCW reads the Home Addresses under all the movable heads. The Seek Address is dynamically altered by AP-1 to cover physical tracks 00 through 29. The logical tracks read are: for the 3330-1 Compatibility Mode, cylinder 0 tracks 0-18 and cylinder 4 tracks 0-9; for the 3344, cylinder 0 track 0, cylinder 0 odd-numbered tracks, and cylinders 11-14 odd-numbered tracks.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by the RHAMH routine.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	1A	Read Home Address	000	10	SKIP	5	

7. Channel Program for Drive Test – RHAFH

   This CCW chain reads all fixed head Home Addresses. The Seek Address is dynamically altered by AP-1 to cover all 60 physical fixed heads. The logical tracks read are: for the 3330-1 Compatibility Mode, cylinders 1-3 tracks 0-18; for the 3344, cylinders 1-10 even numbered tracks. This test is performed only for the 3344 devices that have fixed heads installed. This test is always performed for the 3350.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by the RHAMH routine.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 1
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	1A	Read Home Address	000	10	SKIP	5	

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8. Channel Program for Drive Test – RPS

   This CCW chain issues a Read Sector and a Set Sector command.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine RPS.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	22	Read Sector	buffer	40	CC	1	Read random sector
5	03	No Operation	000	40	CC	1	Disorient drive
6	23	Set Sector	buffer	40	CC	1	Set to sector read
7	03	No Operation	000	00		1	Bring in channel end and device end

9. Channel Program for Drive Test – SK192

   This CCW chain seeks to physical cylinder 192 and causes heavy power dissipation. This test is not run on the 3344 because the 3344 cannot seek across 192 physical cylinders.

   CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine SK192.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	buffer	40	CC	6	Seek to physical cylinder 192
5	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
6	23	Set Sector	buffer	40	CC	1	Set sector 0
7-102							The set of CCWs 4, 5, and 6 are repeated 32 times before CCW 103 is performed
103	03	No Operation	000	00		1	To get device end

10. Channel Program for Drive Test – SKINCR

    This CCW chain tests the incremental seek capability. A pair of CCW commands (Seek and Read Home Address) is performed 50 times with the cylinder address being incremented each time.

    CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine SKINCR.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	buffer	40	CC	6	Seek to logical cylinder 11
5	1A	Read Home Address	000	50	SKIP,CC	5	Verify Seek
6-106							Repeat the set of CCWs 4 and 5 48 times incrementing the physical cylinder by 1 and the CCW address by 8 each time
107	07	Seek	buffer +392	40	CC	6	Seek to cylinder *n**
108	1A	Read Home Address	000	10	SKIP	5	Verify Seek

*Seek to logical cylinder 256 for the 3344, and logical cylinder 84 for the 3330-1 Compatibility Mode.

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11. Channel Program for Drive Test – SKMAX

This CCW chain tests the maximum seek capability. A pair of CCW commands (Seek and Read Home Address) is performed 50 times from cylinder 0 to the maximum cylinder address.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine SKMAX.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	buffer	40	CC	6	Seek to high cylinder of logical volume
5	1A	Read Home Address	000	50	SKIP, CC	5	Verify Seek
6	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
7	1A	Read Home Address	000	50	SKIP, CC	5	Verify Seek
8-103							Repeat the set of CCWs 4-7 24 times. The command chaining bit is turned off in the last CCW executed.

12. Channel Program for Drive Test – SKRAN

This CCW chain tests the random seek capability. The test is run 50 times, each time a new cylinder address is derived from table RANTBL.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine SKRAN.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder 0
2	1F	Set File Mask	X'40'	40	CC	1	Set File Mask to Read Only
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	1A	Read Home Address	000	10	SKIP	5	

13. Channel Program for Drive Test – RHA

This CCW chain reads the Home Addresses on the CE cylinder. This CCW chain is repeated for the following tracks: for the 3330-1 Compatibility Mode, tracks 00-18 and 20-29; for the 3344, logical CE cylinders 0-4 even numbered tracks and logical CE cylinder 0 odd numbered tracks.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine RHA.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder *
2	1F	Set File Mask	X'44'	40	CC	1	Set File Mask to Read Only on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder on physical volume
5	1A	Read Home Address	buffer	00		5	Read Home Address to compare

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

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14. Channel Program for Drive Test – WRT

This CCW chain writes R0 and R1 on the CE cylinder. This CCW chain is repeated for the following tracks: for the 3330-1 Compatibility Mode, tracks 00-18 and 20-29, for the 3344, logical CE cylinders 0-4 even numbered tracks and logical CE cylinder 0 odd numbered tracks.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine WRT.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'C4'	40	CC	1	Set File Mask to allow writing on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder on physical volume
5	39	Search Home Address Equal	AP1CESK +2	40	CC	4	Validate if on correct track
6	08	TIC	CCW5	00			Repeat search is Home Address Not Found
7	15	Write Record 0	Buffer	40	CC	16	Write R0
8	ID	Write Count, Key, and Data	buffer +16	00		264	Write R1

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

15. Channel Program for Drive Test – RR01

This CCW chain reads R0 and R1 on the CE cylinder. This CCW chain is repeated for the following tracks: for the3330-1 Compatibility Mode, tracks 00-18 and 20-29; for the 3344, logical CE cylinders 0-4 even numbered tracks and logical CE cylinder 0 odd numbered tracks.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine RR01.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'44'	40	CC	1	Set File Mask to Read Only on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder on physical volume
5	1A	Read Home Address	000	50	CC, SKIP	5	Verify Seek
6	16	Read R0	000	50	CC, SKIP	16	Read Record 0 for a Count compare
7	1E	Read Count, Key, and Data	000	50	CC, SKIP	264	
8-46							Repeat the set of CCWs 5-7 13 times
47	1A	Read Home Address	000	50	CC, SKIP	5	Position to Home Address
48	16	Read R0	buffer	40	CC	16	Read Record 0 for a Count compare
49	1E	Read Count, Key, and Data	buffer +8	00		264	Read for the Count and first 8 bytes of data are compared

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

16. Channel Program for Drive Test – RDMT

This CCW chain performs a multitrack read on the device.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine RDMT.

CCW No.	Command Code Hex	Command Code Description	Address	Flags Hex	Flags Description	Count	Comments
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'44'	40	CC	1	Set File Mask to Read Only on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 0 on physical volume
5	16	Read R0	buffer	40	CC	16	Read Record 0 for a Count compare
6	92	Read Count, Multitrack	buffer +8	40	CC	8	Read Record 1 for a Count compare
7-17							Repeat CCW3 11 times incrementing the buffer address by 8 each time
18	03	No Operation	000	40	CC	1	Force drive to lose orientation
19	12	Read Count	buffer +104	00		8	Read record 1 Count on track 11 again

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

17. Channel Program for Drive Test – FTWRT

This CCW chain tests the full track Read/Write capability.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine FTWRT.

CCW No.	Command Code Hex	Command Code Description	Address	Flags Hex	Flags Description	Count	Comments
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder**
2	1F	Set File Mask	X'04'	40	CC	1	Set File Mask to write on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 1 on physical volume
5	31	Search ID Equal	AP1CESK +2	40	CC	5	Search for ID equal on R0
6	08	TIC	CCW5	00			Repeat search if ID not equal
7	ID	Write Count, Key, and Data	buffer	80	CD	8	Write R1 Count
8	ID	Write Count, Key, and Data	000	40	CC	*n**	Write a full track of data
9	1E	Read Count, Key, and Data	000	10	SKIP	*n*+8*	Read R1 Count full track of data back back (no data is transferred)

*For the 3330-1 Compatibility Mode, *n*=13030; for the 3344, *n*=8368.

**If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

18. Channel Program for Drive Test – AMDET

This CCW chain detects the presence of an address amrk.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine AMDET.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'04'	40	CC	1	Set File Mask to write on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 1 on physical volume
5	31	Search ID Equal	AP1CESK +2	40	CC	5	Search for ID equal on Record 0
6	08	TIC	CCW5	00			Repeat search if ID is not equal
7	ID	Write Count, Key, and Data	buffer	80	CD	8	Write Record 1 Count
8	ID	Write Count, Key, and Data	000	40	CC	1024	Write Record 1 Data
9	ID	Write Count, Key, and Data	buffer +8	80	CD	8	Write Record 2 Count
10	ID	Write Count, Key, and Data	000	40	CC	1024	Write Record 2 Data
11	31	Search ID Equal	buffer	40	CC	5	Search for ID equal on Record 1
12	08	TIC	CCW11	00			Repeat search if ID is not equal
13	03	No Operation	000	40	CC	1	Force drive to lose orientation
14	12	Read Count	buffer +16	00		8	Read Record 2 Count

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

19. Channel Program for Drive Test – WRTPAD

This CCW chain test the Write Padding capability.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine WRTPAD.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'04'	40	CC	1	Set File Mask to write on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 1 on physical volume
5	31	Search ID Equal	AP1CESK +2	40	CC	5	Search for ID equal on Record 0
6	08	TIC	CCW5	00			Repeat search if ID is not equal
7	ID	Write Count, Key, and Data	buffer	40	CC	264	Write Record 1 Count
8	ID	Write Count, Key, and Data	buffer +8	40	CC	8	Write Record 2 Count
9	31	Search ID Equal	AP1CESK +2	40	CC	5	Search for ID equal on Record 0
10	08	TIC	CCW9	00			Repeat Search if ID is not equal
11	ID	Write Count, Key, and Data	buffer	40	CC	264	Write new Record 1
12	1A	Read Home Address	000	50	CC, SKIP	5	Reposition head
13	12	Read Count	000	50	CC, SKIP	8	Read Record 1 Count
14	12	Read Count	buffer +24	00		8	Read Record 1 Count again

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

20. Channel Program for Drive Test – SD

This CCW chain performs the Skip Displacement test.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine SD.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to CE cylinder
2	1F	Set File Mask	X'04'	40	CC	1	Set File Mask to write on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 1
5	39	Search Home Address equal	AP1CESK +2	40	CC	4	Verify Seek
6	08	TIC	CCW5	00			Repeat search if Home Address not equal
7	19	Write Home Address	buffer +x*	40	CC	11−x*	Write Home Address with zeros in SD (Skip Displacement) bytes of Home Address
8	15	Write R0	Buffer +11	40	CC	y*	Write R0 where Data is a dummy R1 record with SD information to be tested
9	1A	Read Home Address	0	50	SKIP, CC	5	Read Home Address to position head
10	0F	Space Count	Buffer +11+y*	40	CC	3	Space across R0 count and indicate R0 Data length = 8
11	1E	Read Count, Key, and Data	0	10	SKIP	264	Read dummy R1 (written as R0 Data)

*x+0 for 3330-1 Compatibility Mode; 4 for 3344.
y=847 for 3330-1 Compatibility Mode; 513 for 3344.

21. Channel Program for CLEANUP

This CCW chain restores track 1 of the CE cylinder.

CCWs 1, 2, and 3 are built by IOS (part of the operating system). CCW3 transfers control to the first CCW (CCW4) of the channel program built by routine CLEANUP.

CCW No.	Command Code		Address	Flags		Count	Comments
	Hex	Description		Hex	Description		
1	07	Seek	AP1SEEK	40	CC	6	Seek to cylinder*
2	1F	Set File Mask	X'C1'	40	CC	1	Set File Mask to allow writing on CE cylinder
3	08	TIC	CCW4	40	CC		Transfers control to channel program
4	07	Seek	AP1CESK	40	CC	6	Seek to CE cylinder, track 1 on physical volume
5	39	Search Home Address equal	AP1CESK	40	CC	4	Verify Seek
6	08	TIC	CCW5	00			Repeat search if Home Address not equal
7	15	Write R0	buffer	40	CC	16	Write Record 0
8	1D	Write Count, Key, and Data	buffer +16	00		264	Write Record 1

*If fixed heads are installed, seek to cylinder 1; if fixed heads are not installed, seek to cylinder 695 for the 3344 and cylinder 403 for the 3330-1 Compatibility Mode.

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

CONSOLE MESSAGES

See OS/VS and DOS/VS Analysis Program-1 (AP-1) Users Guide (GC26-3855) for all other console messages not described.

Message Number		Description
OS/VS	DOS/VS	
IAP001A	8701A	xxx DO YOU WANT TO RUN DATA VERIFICATION TEST, YES OR NO Cause: This message asks the operator if the Data Verification test should be run. System Action: The system waits for the operator to reply by typing Yes of No on the system console. Operator Response: A Yes reply causes AP-1 to run the Data Verification test. A No reply ends the AP-1 test.
IAP003I	8703I	xxx SUSPECTED DRIVE PROBLEM (xxx The controller address of failing drive.) Cause: During the Drive tests, AP-1 detected hardware problems. See SYSPRINT output for details of the error. A Data Check occurring during the RHAMH test results in this message. If a Data Check occured, analyze the sense information and error tables in the SYSPRINT output, then: 1. Use the Checkout Procedure on START 110. 2. If the checkout is ok, attempt to restore the Home Address(es) on the volume. See INTDK (initialize disk) on OLT 30. If no Data Check occurred during the RHAMH test, go to MSG 9, Entry A.
IAP004I	8704I	xxx DATA FORMAT UNACCEPTABLE, TESTING TERMINATED Cause: One of the following: • The Count field in a record specifies an incorrect track or an incorrect record number. The volume was probably not written according to IBM standards. AP-1 cannot be run on this volume. • In an OS/VS system, the Error Recovery Procedure (ERP) was unable to recover from the error and either went into a loop or returned with inconsistent error information. • A program writing on the volume under test erased an end-of-data record read by AP-1, which AP-1 expects to read again. For further information, see the console output and AP-1 SYSPRINT or SYSLST printer output, then: 1. Use the Checkout Procedure on START 110. 2. Run OLT T3340PSA to determine the extent of the damage. 3. If Steps 1 and 2 show no failures or errors, the volume should be restored from a backup volume.

OS/VS AND DOS/VS ANALYSIS PROGRAM-1 (AP-1)

Message Number		Description
OS/VS	DOS/VS	
IAP005I	8705I	xxx ERROR READING DATA xxx = The controller address of the failing drive. Cause: AP-1 detected Data Checks while reading. This message is followed by a message on the printer that identifies the track and cylinder number on which each Data Check occurred. The cause of the problem could be a damaged disk surface or an intermittent Read/Write circuitry failure. For further information, see the console output and AP-1 SYSPRINT or SYSLST printer output, then: 1. Use the Checkout Procedure on START 110. 2. If the checkout is ok, use the SYSPRINT output and go to MSG 9, Entry A. 3. If no failure can be found, have the user perform one of the following, depending on the customer procedures. • Restore the entire volume from a backup volume. • Rebuild the track that has the error (see OLT 30). • Assign an alternate track and then restore the track (see OLT 30). • Rebuild the data volume.
IAP006I	8706I	xxx ALL DATA READ WITHOUT ERRORS Cause: The volume was successfully read during the Data Verification test. Every record on the volume was read (without data transfer) by AP-1, and no errors were detected. If data problems persist, further analysis is needed. Use any available data to locate the symptom in the Symptom/Condition column in the table on START 100 that most closely matches the machine status.
IAP008I	8708I	xxx WRITE TESTS BYPASSED Cause: The CE cylinder is incorrectly formatted. AP-1 does not issue Write commands during the Drive tests. Home Addresses must be rewritten on the CE tracks that are in error (use microdiagnostic routine B2).

Message Number		Description
OS/VS	DOS/VS	
IAP009I	8709I	xxx I/O TIMEOUT, TESTING TERMINATED Cause: AP-1 attempted to access the drive, and received no response during a period of 1 to 2 minutes. To AP-1, the drive appears to be unavailable for basic testing. When the timeout occurred during the Data Verification tests, this message is followed by message IAP004I/8704I DATA FORMAT UNACCEPTABLE. When the timeout occurred during the Drive tests, this message is followed by message IAP003I/8703I SUSPECTED DRIVE PROBLEMS. Verify that the drive has power on and the Power On and Ready lamps are on, and that a path is available from the central processing unit (CPU) to the drive. Then rerun AP-1. For further information, see the console output and the AP-1 SYSPRINT or SYSLST printer output. If the problem persists, use the Checkout Procedure on START 110.
IAP010I	8710I	xxx NO DRIVE PROBLEMS FOUND Cause: The AP-1 program successfully completed executing the basic Drive tests and did not detect any problems. System Action: Processing continues with the Data Verification test if specified by the operator. If a problem is still suspected, use the Checkout Procedure on START 110.
IAP017I	8717I	xxx DEVICE NOT READY, TESTING TERMINATED Cause: The device to be tested is not Ready. Operator Response: Make the device Ready, and when the Ready lamp is on, rerun the AP-1 program. If the error persists, use the Checkout Procedure on START 110.

SENSE CONTENTS

SENSE DATA SUMMARY

MLX A

	Bit 0	1	2	3	4	5	6	7
Byte 0	Command Reject	Intervention Required	Channel Bus Out Parity	Equipment Check	Data Check	Overrun	Track Condition Check	Seek Check
1 (See Note)	Permanent Error (Set by ERPs)	Invalid Track Format	End of Cylinder	Not Used	No Record Found	File Protected (not used with System/3 DSA)	Write Inhibited	Operation Incomplete
2 (See Note)	RPS	Correctable	Not Used	Environmental Data Present	Compatibility Mode	HDA Size 3 Bit (Fixed Heads Installed)	HDA Size 2 Bit	HDA Size 1 Bit
3 (See Note)	RESTART COMMAND (Provided only when Byte 1 bit 7, Operation Incomplete, is active)							
4	Controller Addr Bit 2	Controller Addr Bit 1	CONTROLLER DEVICE ADDRESS 0	0	0	Device Addr Bit 4	Device Addr Bit 2	Device Addr Bit 1
5	LOW-ORDER LOGICAL CYLINDER ADDRESS 128	64	32	16	8	4	2	1
6	HIGH-ORDER LOGICAL CYLINDER ADDRESS (1024)	512	256	(2048)	AND Log. Trk 8	LOGICAL TRACK Log. Trk 4	Log. Trk 2	Log. Trk 1
7	FORMAT (bits 0 to 3 hex)				MESSAGE CODE (bits 4 to 7 hex)			

If the storage control is a System/3 DSA, see the System/3 3340/3344 TMD manual for definition of Sense Bytes 3 and 4.

If the storage control is a 3880 these bytes have a unique meaning for Format 6.

3344 2 — 3880 MLX CHART

MESSAGE CODE FOR BYTE 7 (Bits 4-7 Hex)

B

Format 1 – SENSE 101
Format 4,5 – SENSE 102
Format 6 – SENSE 103

Note: *See Storage Control MLM for sense data and/or message for Formats 0, 2, and 3. If the storage control is a System/3 DSA, see the System/3 3340/3344 TMD manual for Formats 0, 2, and 3.*

3340 9 — Storage Control MLX CHART*

*Use the 3340 entry into other MLMs.

MESSAGES, determined by format and message code (Byte 7)

	Format 1	Format 4	Format 5
0	Not Used	HA Area – Data Check	Not Used
1	Transmit Target Error	Count Area – Data Check	Not Used
2	Microprogram Detected Error (Byte 18)	Key Area – Data Check	Not Used
3	Transmit Difference High Error	Data Area – Uncorrectable Data Check	Data Area – Correctable Data Check
4	Sync Out Timing Error	HA Area – No Sync Byte Found	
5	Unexpected Drive Status at Initial Selection	Count Area – No Sync Byte Found	
6	Transmit CAR Error	Key Field – No Sync Byte Found	
7	Transmit Head Error	Data Area – No Sync Byte Found	
8	Transmit Difference Error		Not Used
9	Drive Status not as expected during Read IPL		
A	Seek Verification Check on physical address		
B	Seek Incomplete or Sector Compare Check		
C	No Interrupt from drive	Not Used	
D	Not Used		
E	Invalid 3344 HDA Configuration Bit Combination		
F	Not Used		

SENSE 100 **FORMAT 1 – DRIVE EQUIPMENT CHECKS**

B

	Byte	Bit 0	1	2	3	4	5	6	7
Drive Status	8	Controller Check	Device Interface Check	Drive Check	Read/Write Check	Online	HDA Attention	Busy	Seek Complete or Search Sector
Check Status	9	Not Used	Sector Compare Check	Motor At Speed Latched	Air Switch Latched	Write Enable	HDA Size 4 Bit (Fixed Head)	HDA Size 2 Bit (Always On)	HDA Size Bit 1 (Always On)
HDA Seq. Control	10		HDA Sequence Latch 4	HDA Sequence Latch 2	HDA Sequence Latch 1	HDA Timer Check Latch	HDA Sequence Check Latch	Not Used	Odd Physical Track
Load Sw Status	11	Drive Start Switch	Guardband Pattern	Target Velocity	Track Crossing	Not Used	Air Switch	Not Used	Motor At Speed
R/W Safety	12	Multiple Chip Select Check	Capable/ Enable Check	Write Overrun	Index Check	Delta I Write Check	Control Check	Write Transition Check	Write Current during Read Check
	13	CONTROL INTERFACE BUS OUT (For Message Code 2 (Byte 7), see Sense Byte 18)				EXPECTED DRIVE STATUS/DATA (When Message Code (byte 7) is 1, 3, 5, 6, 7, 8, and 9)			
	14	CONTROL INTERFACE BUS IN (At the time an error was detected)							
	15	CONTROL INTERFACE TAG BUS (At the time an error was detected)							
Access Status	16	Access Timeout Check	Overshoot Check	Servo Off Track Check	Rezero Mode Latch	Servo Latch	Linear Mode Latch	Control Latch	Wait Latch
Controller Checks	17	PLO Check	No PLO Input Check	SERDES Check	Gap Counter Check	Write Data Check	Monitor Check	ECC Check	ECC Zeros Detected
Micro Detected Errors	18	← Not Used →				CODED ERROR CONDITION (Bits 4-7 Hex)			
Status	19	Set R/W on	← Not Used →			Head Short Check	← Not Used →		1 (Always On)
Interface Checks	20	Control Interface Tag Bus Parity Check	Control Interface Bus Out Parity Check	Drive Selection Check	Device Bus In Parity Check	Control Interface Bus In Parity Check	I Write Fail	Device Bus Out Parity Check	Device Tag Parity Check
	21	PHYSICAL DRIVE IDENTIFICATION							
		A	B	C	D	E	F	G	H
	22	FAULT SYMPTOM CODE							
	23	FAULT SYMPTOM CODE							

Or

5	6	7
I Write Sense	Index Mark	Active Track

If Set R/W is active (Byte 19, bit 0 on), bits above are used.

Or

Previous Address
If Byte 0, bit 7 = 1.
(From)

Or

Present Address
If Byte 0, bit 7 = 1.
(Actual)

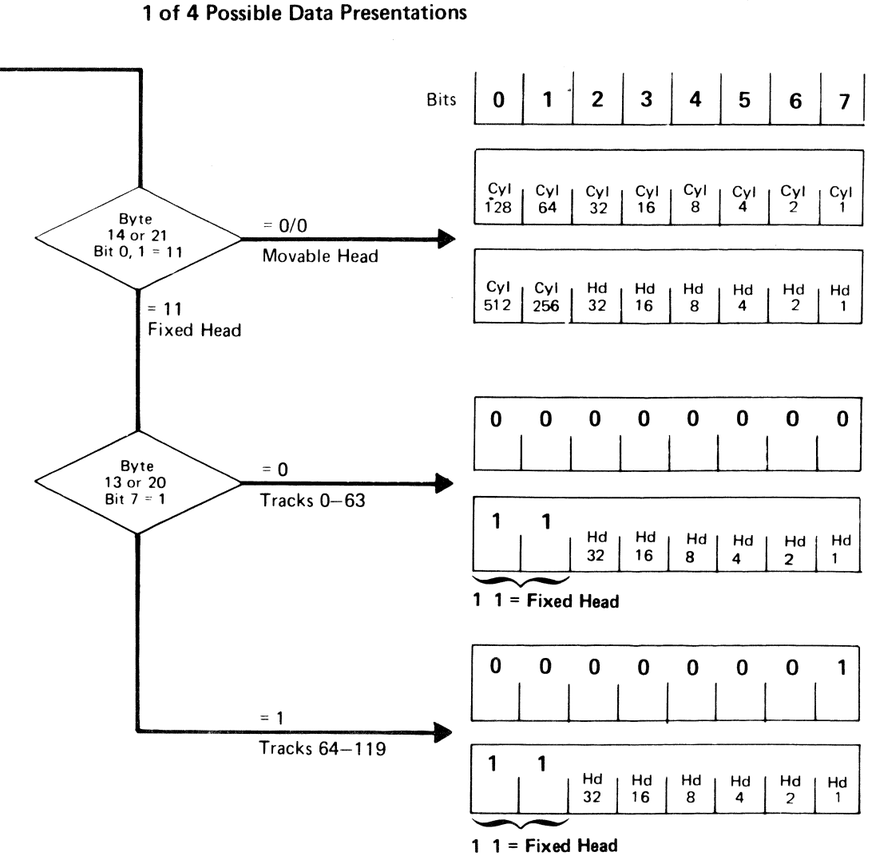
1 Micro

1 Microprogram Error Messages, determined by Sense Byte 18, bits 4–7

0	Not Used
1	No Tag Valid on R/W operation †
2	No Normal or Check End on R/W or ECC operation
3	No Response from controller or Control operation †
4	Timed-out waiting for Index or Active Track (40 ms)
5	ECC Hardware Check †
6	Multiple or no controllers selected †
7	Preselection Check/Short Busy time expired
8	Repetitive Command Overruns on G1 operations.
9	Busy missing after Seek Start is issued
A	Physical Drive Address Check
B–E	Not Used
F	Unresettable Interrupt

†*Sense Bytes 13, 14 and 16 are valid for Microprogram Error Messages.*

1 of 4 Possible Data Presentations



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SENSE 100 **FORMAT 4 – DATA CHECKS NOT PROVIDING DISPLACEMENT INFORMATION**

B

Byte	Bit 0	1	2	3	4	5	6	7
8	CYLINDER ADDRESS							
9	CYLINDER ADDRESS							
10	HEAD ADDRESS							
11	HEAD ADDRESS							
12	RECORD NUMBER							
13	SECTOR NUMBER							
14								
15								
16								
17	NOT USED							
18								
19								
20								
21								
22	FAULT SYMPTOM CODE							
23	FAULT SYMPTOM CODE							

Count Identification

SENSE 100 **FORMAT 5 – DATA CHECKS PROVIDING DISPLACEMENT INFORMATION**

B

Byte	Bit 0	1	2	3	4	5	6	7
8	CYLINDER ADDRESS							
9	CYLINDER ADDRESS							
10	HEAD ADDRESS							
11	HEAD ADDRESS							
12	RECORD NUMBER							
13	SECTOR NUMBER							
14	NOT USED							
15	RESTART DISPLACEMENT							
16	RESTART DISPLACEMENT							
17	RESTART DISPLACEMENT							
18	ERROR DISPLACEMENT							
19	ERROR DISPLACEMENT							
20	ERROR PATTERN							
21	ERROR PATTERN							
22	ERROR PATTERN							
23	NOT USED							

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SENSE 100 B

FORMAT 6 – USAGE AND OVERRUN ERROR STATISTICS

Byte	Bit 0	1	2	3	4	5	6	7
8	NUMBER OF BYTES READ OR SEARCHED (Key and Data Areas Only)							
9	NUMBER OF BYTES READ OR SEARCHED (Key and Data Areas Only)							
10	NUMBER OF BYTES READ OR SEARCHED (Key and Data Areas Only)							
11	NUMBER OF BYTES READ OR SEARCHED (Key and Data Areas Only)							
12								
13	NOT USED							
14								
15								
16	NUMBER OF ACCESS MOTIONS							
17	NUMBER OF ACCESS MOTIONS							
18	Channel select for Bytes 20-23 ← NOT USED →							
19	← NOT USED →							
20	COMMAND OVERRUNS	CHANNEL A if Byte 18, bit 0 is 0 CHANNEL C if Byte 18, bit 0 is 1						
21	DATA OVERRUNS	CHANNEL A if Byte 18, bit 0 is 0 CHANNEL C if Byte 18, bit 0 is 1						
22	COMMAND OVERRUNS	CHANNEL B if Byte 18, bit 0 is 0 CHANNEL D if Byte 18, bit 0 is 1						
23	DATA OVERRUNS	CHANNEL B if Byte 18, bit 0 is 0 CHANNEL D if Byte 18, bit 0 is 1						

If storage control is a System/3 DSA, this area is not used (Byte 18 to 23).

Not device-dependent information. See Storage Control MLM.

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Storage Control MLX CHART*

* Use the 3340 entry into other MLMs.

SENSE DATA DESCRIPTION

Sense Byte 0

Sense Bytes 0 through 2 are generated when a Unit Check is presented. These bytes describe the error condition and identify specific action for subsystem error recovery.

BIT 0 — COMMAND REJECT

Sense Byte 7 identifies the error condition in more specific terms. Any one of the following conditions cause this bit to be generated:

Invalid command code or a command associated with an uninstalled feature has been issued.

Invalid command sequence.

Invalid or incomplete argument has been transferred by a control command.

Track formatted without a Home Address.

Write portion of the File Mask is violated.

A Write command was issued to a drive that had its Read Only switch on. Byte 1, bit 6 (Write Inhibited) is also set.

BIT 1 — INTERVENTION REQUIRED

Bit 1 indicates that the addressed device is:

Not physically attached to the system.

Not online.

A diagnostic Write or Load Channel Command Word (CCW) is issued while an inline microdiagnostic is resident in the storage control.

BIT 2 — CHANNEL BUS OUT PARITY

The storage control has detected bad parity in data transferred from the channel. A parity error detected during command transfer is a Bus Out Check and not a Command Reject.

BIT 3 — EQUIPMENT CHECK

An unusual hardware condition originated in the channel, storage control, controller, or drive. (The conditions of this bit are defined in Sense Bytes 7 through 23.)

BIT 4 — DATA CHECK

If Byte 2, bit 1 is also on, a correctable data error has been detected in information received from the drive. (Correction information is provided in Sense Bytes 15 through 21.)

An uncorrectable data error has been detected in information received from the drive. (This is further defined in Sense Byte 7.)

BIT 5 — OVERRUN

Bit 5 is set whenever:

A channel response to a data transfer request was not received in time by the storage control.

A command from the channel was received too late to be properly executed.

All Data Overrun conditions, other than those that occur in a second or subsequent segment of an Overflow Record, or those that occur during a Format Write, are retried by the storage control.

Detection of an overrun causes an immediate stop of data transfer. When writing, the remaining portion of the record area is padded out with zeros.

BIT 6 — TRACK CONDITION CHECK

Bit 6 is set whenever:

Any single track command other than Search HA, Read HA, or Read RO is executed on a defective track.

Any multitrack command or overflow operation other than Search HA, Read HA, or Read RO switches to a defective track.

Any multitrack command, including Search HA, Read HA, or Read RO, or an Overflow Record operation that attempts to switch from an alternate or defective track is detected by the storage control to be alternate or defective. The storage control detects if a track is alternate or defective only if some single-track Read or Search operation has been executed on the track in the current CCW chain, and no control command other than No-Op has been executed since the single-track Read or Search command.

BIT 7 — SEEK CHECK

The drive has been unable to successfully complete a Seek operation due to an equipment failure that prevented the access mechanism from positioning correctly. This condition is detected by the drive that presents a Seek Incomplete indication or by the storage control when it detects an incorrect physical address when reading Home Address or Count areas.

Bit 7 is also posted when Capable/Enable Check (Format 1, Byte 12, bit 1) is on indicating the access mechanism is not track following properly.

Sense Byte 1

BIT 0 — PERMANENT ERROR

Bit 0 is set by ERPs when the specified number of retry actions is exhausted.

BIT 1 — INVALID TRACK FORMAT

An attempt was made to write data exceeding track capacity. Bit 1 is also posted during a Read or Search operation when the Index Point is detected in the gap after a Count or Key field. This indicates a programming error or an expected programming condition has been detected.

BIT 2 — END OF CYLINDER

One of the following conditions has occurred:

With a System/3 DSA, End of Cylinder occurs during an attempted head switch from cylinder 209 head 19 to cylinder 210 head 0.

A Read Multitrack or Search Multitrack operation has attempted to continue beyond the addressable cylinder boundry.

An overflow operation has attempted to continue beyond the addressable cylinder boundary. Operation Incomplete (Byte 1, bit 7) is also included.

End of Cylinder indicates a programming error or an expected programming condition has been detected.

BIT 3 — NOT USED

BIT 4 — NO RECORD FOUND

One of the following conditions has occurred:

The Index Point at the beginning of the selected logical track has been detected twice in the same command chain without an intervening Read operation in the Home Address area or in a Data area.

The Index Point at the beginning of the selected logical track has been detected twice in the same command chain without an intervening Write, Sense, or Control command.

The storage control always verifies that the access mechanism is positioned properly before posting this bit. This bit indicates a programming error or an expected programming condition has occurred.

BIT 5 — FILE PROTECTED

If the storage contol is a System/3 DSA, the message does not apply.

One of the following conditions has occurred:

A Seek command has violated the File Mask. Includes Seek to a CE track when mask bit 5=0.

A Read Multitrack or Search Multitrack operation has violated the File Mask.

An overflow operation has violated the seek portion of the File Mask. Operation Incomplete (Byte 1, bit 7) is also set.

File Protected indicates a programming error or an expected programming condition has been detected.

BIT 6 — WRITE INHIBITED

A Write command was received for a drive that had its R/W or Read switch in the Read position. Command Reject is also set.

SENSE DATA DESCRIPTION

BIT 7 — OPERATION INCOMPLETE

One of the following conditions has occurred during the processing of an Overflow Record operation:

A defective or alternate track condition is detected after initiation of data transfer. Track Condition Check (Byte 0, bit 6) is also set. If storage control is a System/3 DSA, only this item applies.

Overflow to a file-protected boundary. File Protected (Byte 1, bit 5) is also set.

Overflow past the cylinder boundary. End of Cylinder (Byte 1, bit 2) is also set.

A correctable Data Check was detected in the Data field other than the last segment. Data Check (Byte 0, bit 4) and Correctable (Byte 2, bit 1) are also set.

Sense Byte 3 provides the Restart command and Bytes 8 through 13 provide restart information.

Sense Byte 2

BIT 0 — RPS

Bit 0 indicates that Rotation Position Sensing (RPS) is installed in the selected drive.

BIT 1 — CORRECTABLE

Bit 1 indicates that the Data field Data Check posted by Byte 0, bit 4 is correctable. Sense Bytes 15 through 22 identify the error pattern, error pattern displacement, and restart displacement.

BIT 2 — NOT USED

BIT 3 — ENVIRONMENTAL DATA PRESENT

Bit 3 indicates that Sense Bytes 8 through 23 have usage counter statistics under Format 6. Usage statistics include the number of bytes read/searched, number of overruns by channel, and number of access motion seeks.

BIT 4 — COMPATIBILITY MODE

Bit 4 indicates that the drive is a 3344.

BIT 5 — HDA SIZE

Bit 5 indicates that the 3344 is a fixed head model (B2F).

BITS 6 AND 7 — HDA SIZE

Bit 6 is On and bit 7 Off for 3344 drives.
For System/3 DSA, bits 6 and 7 are On for 3344 drives.

Sense Byte 3

BITS 0 THRU 7 — RESTART COMMAND

Sense Byte 3 is provided when Operation Incomplete (Byte 1, bit 7) is set. This byte identifies the operation in progress when the interrupt occurred. The system recovery program uses this command, along with Channel Status Word (CSW) information, to construct a new Channel Command Word (CCW). The new CCW is issued to the storage control, after correcting the unusual conditions, to continue the operation following the point of interruption.

When Operation Incomplete is set, the Restart command is set to '06' to indicate a Read operation was in progress, or '05' to indicate a Write operation. Sense Byte 3 is zero when Operation Incomplete is not set.

If the storage control is a System/3 DSA, see the System/3 3340/3344 TMD manual for the definition of Sense Byte 3.

Sense Byte 4

Sense Byte 4 contains the coded physical Controller/Device address of the device on which a selection was successful or attempted.

If the storage control is a System/3 DSA, see the System/3 3340/3344 TMD manual for the definition of Sense Byte 4.

Sense Byte 5, Except 3880, Format 6 see

BITS 0 THRU 7 — LOGICAL CYLINDER LOW

Sense Byte 5 identifies the low-order eight bits of the cylinder address of the most current seek argument.

Sense Byte 6, Except 3880, Format 6 see

Sense Byte 6 identifies the logical track address and cylinder of the most current seek argument.

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BIT 0 — LOGICAL CYLINDER HIGH

High-order bit (1024) of cylinder address in Sense Byte 5.

BIT 1 – LOGICAL CYLINDER HIGH

High-order bit (512) of cylinder address in Sense Byte 5.

BIT 2 – LOGICAL CYLINDER HIGH

High-order bit (256) of cylinder address in Sense Byte 5.

BIT 3 – LOGICAL CYLINDER HIGH

High-order bit (2048) of cylinder address in Sense Byte 5.

BITS 4 THRU 7 – LOGICAL TRACK

Bits 4 thru 7 identify the logical track of the last seek (excluding retry seeks). The head address is updated during multitrack and overflow operations.

If an alternate track condition is detected and Operation Incomplete is posted during an overflow operation, Byte 6 is set to the head address of the defective track plus 1. This information is used by the ERPs to construct the seek argument to continue the operation.

Sense Byte 7

BITS 0 THRU 3 — FORMAT

Bits 0 through 3 of Sense Byte 7 identify the specific format of the remaining Sense Bytes (8 through 23). For other than System/3 DSA, see Storage Control MLM for sense data for Formats 0, 2, and 3.

BITS 4 THRU 7 — MESSAGE CODE

Bits 4 through 7 of Sense Byte 7 provide an encoded message that describes the specific nature of the error condition. See SENSE 109 for description of messages.

FORMAT 1 — DRIVE EQUIPMENT CHECKS

Format 1 is generated under the following conditions:

Detection of Drive, Device Interface, or Controller Equipment Checks. Byte 0, bit 3 (Equipment Check) is set.

No online indication in file status (Byte 8, bit 4). Byte 0, bit 1 (intervention Required) is set.

Detection of seek errors. Byte 0, bit 7 (Seek Check) is set.

SENSE DATA DESCRIPTION

Sense Byte 8 — Drive Status

BIT 0 — CONTROLLER CHECK

One of the following conditions has occurred:

No PLO Input. (See Format 1, Byte 17, bit 1.) Three successive PLO pulses were missing.

Bus Out Parity Check.

Device Bus In Parity Check.

Shift Register Error.

Write Data Check.

ECC Hardware Check

Tag Bus Parity Check

1 of 8 Check (Drive Select Check)

Gap Counter Check

PLO Check. (See Format 1, Byte 17, bit 0.)

Monitor Check. (See Format 1 Byte 17, bit 5.)

BIT 1 — DEVICE INTERFACE CHECK

A Device Tag Bus or Device Bus Out Parity error has been detected. Details can be determined using the Sense Interface Tag.

BIT 2 — DRIVE CHECK

One or more of the following conditions has occurred in the drive:

HDA Sequence Check.

Access Error.

Sector Non-Compare Check.

The conditions causing Drive Check are reset by Check Reset and CE Reset.

BIT 3 — READ/WRITE CHECK

Read/Write safety circuits have detected a condition that could endanger data integrity. These conditions are:

Multiple chips selected.

Write current while reading.

High Write Current active while writing on an odd-numbered movable head.

High Write Current not active while writing on an even-numbered movable head or fixed head.

No transitions while writing data.

Overrun while writing.

Set Read/Write while not Read/Write enabled (not track following).

Write Gate on while not write enabled.

Write Gate on while Active Track is off.

Read Gate and Write Gate on together.

Index Check.

Shorted head.

BIT 4 — ONLINE

The drive Start/Stop switch is in the Start position, the drive is Ready (State 6), and the initial Rezero was successful. Online is active until the drive leaves Ready (State 6).

BIT 5 — HDA ATTENTION

If Byte 19, bit 0 = 0:
An HDA is in the Ready condition following a Sequence Start signal, the drive Start/Stop switch is in the Start position, or the Attention switch has been operated. The Read/Write heads are positioned over track 0 with the Difference Counter, HAR, and CAR reset when this signal is present.

If Byte 19, bit 0 = 1:
The drive in Read/Write mode has sensed that Write Current is present at the Read/Write head.

BIT 6 — BUSY

If Byte 19, bit 0 = 0:
The drive is performing a Rezero, Seek, or Search Sector operation. Busy is turned off by Seek Complete or Search Sector. If no Attention Reset is given for a Search Sector operation, Busy is present after Sector Compare is inactive. Bit 6 in combination with bit 7 indicates the following:

Bits 6 and 7 off – Seek or Search Sector is not active.

Bit 6 off and bit 7 on – Seek or Sector Compare Complete generates an interrupt.

Bit 6 on and bit 7 off – Busy, Seek in progress.

Bits 6 and 7 on – Busy, Search Sector in progress.

If Byte 19, bit 0 = 1:
The drive in Read/Write mode has detected an Index Mark.

BIT 7 — SEEK COMPLETE OR SEARCH SECTOR

If Byte 19, bit 0 = 0:

For information on bit 7 in combination with bit 6, see Bit 6 – Busy.

A Seek or Rezero operation initiated by the controlling system has been completed or a Search Sector operation is in progress. It is a result of one of the following conditions:

Seek Complete – This is the normal end of a Seek or Rezero operation initiated by the controlling system; the specified track has been reached and Drive Check is off.

Seek Incomplete – This is the abnormal end of a Seek or Rezero operation and is indicated by Drive Check (Byte 8, bit 2) appearing with Seek/Sector Complete. The access mechanism is in an undefined state.

If Byte 19, bit 0 = 1:

The drive in Read/Write mode has sensed that Active Track is present. Active Track is present if Head Address Register bit 7 is off during the even half track or that Head Address Register bit 7 is on during the odd half track.

Sense Byte 9 — Checks/Status

BIT 0 — NOT USED

BIT 1 — SECTOR COMPARE CHECK

Bit 1 indicates that two Index Marks have been detected without an intervening Sector Compare while performing a Search Sector operation.

BIT 2 — MOTOR AT SPEED SWITCH LATCHED

Bit 2 indicates that the switch failed while the drive was in a Ready state.

BIT 3 — AIR SWITCH LATCHED

Bit 3 indicates that the switch failed while the drive was in a Ready state.

BIT 4 — WRITE ENABLE

Bit 4 indicates that the R/W or Read switch on the Operator Panel is in the R/W position.

BITS 5, 6, AND 7 — FIXED HEADS INSTALLED AND HDA SIZE BITS

Bit 5 Fixed Heads	HDA Size Bits		Description
	Bit 6	Bit 7	
0	1	1	Head/Disk Assembly (HDA) installed
1	1	1	Head/Disk Assembly (HDA) with fixed heads installed.

Sense Byte 10 — HDA Sequence Control

BIT 0 – NOT USED

BITS 1 THRU 3 – HDA SEQUENCE LATCHES 4, 2, AND 1

The condition of these latches indicates the state of the HDA sequence.

SENSE DATA DESCRIPTION

BIT 4 – HDA TIMER CHECK LATCH

Indicates that more than 10 seconds has elapsed between HDA Sequence Control States during a start sequence.

BIT 5 – HDA SEQUENCE CHECK LATCH

The condition of this bit (on/off) along with bits 1 through 3 indicates the sequencing state of the HDA. See HDA Sequence description, HDA 500 through 506, for further details.

BIT 6 — NOT USED

BIT 7 — ODD PHYSICAL TRACK

If bit 7 is on, the current physical cylinder address is odd. If bit 7 is off, the current physical cylinder address is even. This bit also represents the low-order bit of the cylinder address.

Sense Byte 11 — Loaded Switch Status

BIT 0 — DRIVE START SWITCH

BIT 5 — AIR SWITCH

BIT 7 — MOTOR AT SPEED SWITCH

Bits 0, 5, and 7 indicate the condition of the interlock switches for all states of the HDA sequence. The condition of each switch is latch-stored for readout if an interlock fails during Read, or if an HDA Sequence Check occurs.

BIT 1 — GUARDBAND PATTERN

BIT 2 — TARGET VELOCITY

BIT 3 — TRACK CROSSING

Bits 1, 2, and 3 are status conditions of the servo system used for diagnostic purposes.

Sense Byte 12 — Read/Write Safety

BIT 0 — MULTIPLE HEAD SELECT CHECK

More than one head has been selected in the selected drive.

BIT 1 — CAPABLE/ENABLE CHECK

One of the following conditions has occurred:

Set Read/Write was present while the drive was not read/write capable (track following).

Writing was attempted on a drive in the read only condition.

Writing was attempted while Active Track was not present.

BIT 2 — WRITE OVERRUN

Writing through an Index Mark has been attempted. It is permissible to write into or out of an Index Mark, but not both.

BIT 3 — INDEX CHECK

An invalid Index Mark was detected while Set Read/Write was present.

BIT 4 — DELTA I WRITE CHECK

Delta I Write current is incorrect for physical head selected.

BIT 5 — CONTROL CHECK

The Write Gate signal and the Read Gate signal are active at the same time.

BIT 6 — WRITE TRANSITION CHECK

Write transitions were not detected 4 microseconds (nominally) after Write Gate was turned on.

BIT 7 — WRITE CURRENT DURING READ CHECK

Write current was detected while reading.

Sense Byte 13 — Control Interface Bus Out

Sense Byte 13 identifies the contents of Control Interface Bus Out at the time the error is detected for message code C and for message code 2 when Byte 13 equals '01', '03', '05', or '06'. It also identified the expected drive status/data for message codes 1, 3, 5, 6, 7, 8, and 9. If Seek Check (Byte 0 bit 7) and message codes A or B occur, this byte contains the seek argument (low order physical cylinder) issued prior to the current argument (Byte 5).

Sense Byte 14 — Control Interface Bus In

Sense Byte 14 identifies the contents of Control Interface Bus In at the time the error is detected. If Seek Check (Byte 0, bit 7) and message code A or B occur, this byte contains the seek argument (high order/physical cylinder/physical track) issued prior to the current argument (Byte 6).

Sense Byte 15 — Control Interface Tag Bus

Sense Byte 15 identifies the contents of the Control Interface Tag Bus at the time the error is detected.

Sense Byte 16 — Access Status

BIT 0 — ACCESS TIMEOUT CHECK

An access operation (Seek or Rezero) was not completed within 200 milliseconds and has therefore been terminated, or Seek Start was issued to the drive while the servo was not track following.

Access Timeout Check causes a Drive Check.

BIT 1 — OVERSHOOT CHECK

During a Seek or Rezero operation, one of the following events caused a Drive Check:

Three track crossings were detected after the Difference Counter decremented to zero.

Three track crossings were detected after the access control advanced to Linear Mode.

A Seek operation moved the carriage out of the data tracks area.

BIT 2 — SERVO OFFTRACK CHECK

The servo has moved offtrack during a Read or Write operation. A Rezero operation is required to reset this bit.

SENSE DATA DESCRIPTION

BIT 3 — REZERO MODE LATCH

BIT 4 — SERVO LATCH

BIT 5 — LINEAR MODE LATCH

BIT 6 — CONTROL LATCH

BIT 7 — WAIT LATCH

Bits 3 through 7 indicate the current state of the access control. Depending on which latch is on, the access control may be in any one of nine states.

Sense Byte 17 — Controller Checks

BIT 0 — PLO CHECK

One of the following errors has occurred:

Two successive PLO pulses were out of phase with the VFO Oscillator on a Write operation.

Three successive PLO pulses were missing on a Write operation.

A phase error was detected in the PLO.

BIT 1 — NO PLO INPUT CHECK

Three successive PLO pulses were missing on a Write operation. This also causes a PLO check.

BIT 2 — SERDES CHECK

SERDES Shift Register Parity did not match its predicted parity.

BIT 3 — GAP COUNTER CHECK

Incorrect parity was detected in the Gap Counter.

BIT 4 — WRITE DATA CHECK

A parity error was detected as data was transferred to the controller or through SERDES.

BIT 5 — MONITOR CHECK

An error has occurred in the bit ring and associated hardware for a period of three servo pulses.

BIT 6 — ECC CHECK

One of the following errors occurred:

An odd number of ECC Shift Register bits at B time.

Missing C pulse to the Shift Register.

Missing B pulse to the Shift Register.

BIT 7 — ECC ZEROS DETECTED

Bit 7 is used to validate the control function during the ECC Control operation.

Sense Byte 18 — Microprogram Detected Errors

BITS 0 THRU 3 — NOT USED

BITS 4 THRU 7

Bits 4 through 7 indicate the error condition in hex code. The error conditions are as follows:

HEX 1: Tag Valid missing on Read/Write operation. Indicates Tag Valid was not received from the controller in response to the issuance of a Read/Write operation. Bytes 13 through 15 are valid.

HEX 2: No Normal or Check End on a Read/Write or ECC operation. Indicates that neither Normal End nor Check End was received from the controller at the end of a Read, Write, or ECC operation. Bytes 13 through 15 are zero.

HEX 3: No response from Controller on Control operation. Indicates that neither Tag Valid, Normal End, nor Check End was received from the controller in response to the issuance of an operation other than a Read/Write operation. Bytes 13 through 15 are valid.

HEX 4: Timeout waiting for Index or Active Track (40 ms time-out). Indicates that Index was not received from the controller, that it failed to drop, or that Active Track failed to occur. Bytes 13 through 15 are zero.

HEX 5: ECC Hardware Check. Indicates one of the following:

Ending status was presented, but no ECC Zeros detected.

Both ECC pattern bytes are equal to zero.

Bus In bit 4 under Check End on without Bus In bit 3 indicates an ECC Data Check.

Sync In was not received after the ECC Control tag was issued to the controller.

Bytes 13 through 15 are valid.

HEX 6: Multiple or no controllers selected. Indicates that a controller or drive selection command was issued and it was found that more than one controller was selected, or no controllers were selected. Bytes 13 through 15 are valid.

HEX 7: Preselection Check indicates one of the following lines was active prior to selection:

Selected Alert 1 (Error Alert)

Select Active

Index Alert

Sync In

Normal End

Check End

Tag Valid

Bytes 13 through 15 are zero.

Short Busy Timer Expired, on machines with the string switch feature, indicates a Busy response (Index Alert) was received for successive select tags for more than 1 millisecond.

HEX 8: Repetitive Command Overruns on G1 operations. Indicates that an unexpected Check End was detected during a Read G1 operation on 2 successive attempts before the Home Address data transfer was initiated. It is also possible to get this error when 2 devices with the same address are connected to a common storage control or ISC.

HEX 9: Busy missing after Seek Start is issued. Indicates that the drive failed to go Busy when Seek Start was issued for a non-zero cylinder difference seek. Bytes 13 through 15 are zero.

HEX A: Physical Address Check. Indicates that the physical address returned (1 of 8 code) after drive selection was incorrect. Bytes 13 through 15 are zero.

HEX B Thru E: Not Used

HEX F: Unresettable Interrupt

An attempt to reset Drive Attention was unsuccessful and the device was masked to inhibit further system interrupts. Bytes 13 through 15 are zero.

Sense Byte 19 — Status

BIT 0 — SET READ/WRITE

Bit 0 indicates that storage control has issued a Set Read/Write (Tag '85').

BITS 1 THRU 3 — NOT USED

BIT 4 — HEAD SHORT CHECK

Bit 4 indicates that a short has been detected in a Read/Write head.

BIT 5 AND 6 — NOT USED

Must be zero.

BIT 7 – ALWAYS ON

Bit 7 is always a 1 bit. It indicates to the system that the machine is capable of having fixed-head HDAs (whether it is a model B2 or B2F).

SENSE DATA DESCRIPTION

Sense Byte 20 — Interface Checks

If Seek Check (Byte 0, bit 7) and Message A (Seek Verification Check on Physical Address) occur, this byte contains the low order physical cylinder of the track selected.

BIT 0 — CONTROL INTERFACE TAG BUS PARITY CHECK

A parity error was detected on the Control Interface Tag Bus while Tag Gate was active.

BIT 1 — CONTROL INTERFACE BUS OUT PARITY CHECK

A parity error was detected on the Control Interface Bus Out while Tag Gate was active.

BIT 2 — DRIVE SELECTION CHECK

Bit 2 indicates that more than one drive has been selected.

BIT 3 — DEVICE BUS IN PARITY CHECK

A parity error was detected on Device Bus In.

BIT 4 — CONTROL INTERFACE BUS IN PARITY CHECK

The controller detected bad parity on the control Interface Bus In.

BIT 5 — I WRITE FAIL

The controller failed to detect I Write Sense from the device within approximately 9 microseconds after the rise of Write Gate.

BIT 6 — DEVICE BUS OUT PARITY CHECK

A parity error has been detected on the Device Bus Out.

BIT 7 — DEVICE TAG BUS PARITY CHECK

A parity error has been detected on the Device Tag Bus.

Sense Byte 21 — Seek Check or Physical Drive ID

If Seek Check (Byte 0, bit 7) and Message A (Seek Verification on Physical Address) occur, this byte contains the high-order physical cylinder/physical track of the track selected.

If not Seek Check, Sense Byte 21 identifies the physical drive that was selected when Unit Check was generated. The format of Byte 21 is as follows:

Bit Number	Physical Address
Bit 0	Drive A
Bit 1	Drive B
Bit 2	Drive C
Bit 3	Drive D
Bit 4	Drive E
Bit 5	Drive F
Bit 6	Drive G
Bit 7	Drive H

Sense Bytes 22 and 23 — Fault Symptom Code

Sense Bytes 22 and 23 contain a hex code that provides entry to the Fault Symptom Index (FSI). The FSI lists possible failures and references MAPs. The Fault Symptom Code is a number generated from sense data by the storage control. The storage control places the code in Sense Bytes 22 and 23 in sense data Formats 1 and 4. FSI 50 shows how a Fault Symptom Code is generated by analyzing sense information.

FORMAT 1 — MESSAGES

Message 0 — Not Used

Message 1 — Transmit Target Error

Message 1 is generated after a Read Back check of the drive Target Register detects that the Target Register was improperly loaded during a Set Sector operation.

Message 2 — Microprogram Detected Errors

Message 2 is generated by the microprogram as defined in Sense Byte 18.

Message 3 — Transmit Difference High Error

Message 3 is generated when a read back check of Sense Status 0 detects that the direction bit and Difference Counter value of 512 and 256 were improperly loaded on a Set Difference High command. If the string switch feature is installed, cylinder address 512 is also wrong.

Message 4 — Sync Out Timing Error

Message 4 is generated when the controller posts Data Overrun (bit 1 on Bus In when Check End is posted during a Read or Write operation).

Message 5 — Unexpected Drive Status at Initial Selection

Message 5 is generated whenever the subsystem receives status that is not expected from the drive during initial selection.

Message 6 — Transmit Cylinder Address Error

Message 6 is generated after a read back check of the drive Cylinder Address Register (CAR) detects that CAR was improperly loaded during a Seek operation. CAR is installed only in machines with the string switch feature.

Message 7 — Transmit Head Error

Message 7 is generated after a read back check of the drive Head Address Register (HAR) detects that HAR was improperly loaded on a Seek operation.

Message 8 — Transmit Difference Error

Message 8 is generated after a read back check of the Difference Register detected that the register was improperly loaded during a Seek operation.

Message 9 — Drive Status Not as Expected During Read IPL

If the storage control is a System/3–DSA, message is not used.

Message 9 is generated whenever the storage control does not receive expected file status during the execution of a Read IPL command. The drive status checked after the internal recalibrate should be Online and Seek Complete.

Message A — Seek Verification Check on Physical Address

Message A is generated whenever the storage control detects a difference between the current seek address and the physical address read from the Home Address and Count areas. See Sense Bytes 20 and 21 for physical address.

Message B — Seek Incomplete or Sector Compare Check

SEEK INCOMPLETE

Seek Incomplete is generated when the drive has been unable to successfully complete a Seek operation. An equipment failure occurred which prevented the access mechanism from positioning correctly. Seek Check (Byte 0, bit 7) is set.

SECTOR COMPARE CHECK

If the storage control is a System/3–DSA, this description does not apply.

Sector Compare Check is generated if the drive failed to detect a Sector Compare between two Index Marks. Equipment Check (Byte 0, bit 3) is set.

SENSE DATA DESCRIPTION

Message C — No Interrupt from Drive

Message C is generated whenever the storage control does not receive an interrupt from the drive within a specified time. This condition can only occur on an internal recalibrate associated with a Read IPL command.

Message E–Invalid 3344 HDA Configuration Bit Combination

Message E is generated by the storage control if an invalid 3344 HDA configuration bit combination is found. Valid bit combinations are as follows:

Sense Byte 19, bit 7 = 1
Sense Byte 2, bits 5, 6, and 7 = 111 or 011.

FORMAT 4 — DATA CHECKS NOT PROVIDING DISPLACEMENT INFORMATION

Format 4 is generated under the following conditions:

a. Detection of ECC uncorrectable errors in the Data field.

b. Detection of ECC data errors in the Count area, Key area, or Home Address area. The message code in Byte 7 identifies the area that exhibits the error.

Sense Bytes 8 Thru 12 — Count ID

Sense Bytes 8 through 12 contain the record ID (CCHHR) as obtained from the Count area of the record in which the error occurs.

Sense Byte 12, the record number (R), is set to zero if the error occurred in Home Address. This byte is unreliable after a space count.

The contents of these bytes are unreliable if the message code in Byte 7 is either 0 or 4 (error occurred in HA), or 1 or 5 (error occurred in Count area).

Sense Byte 13 — Sector Number

Sense Byte 13 contains the sector number of the record that was in error.

Sense Bytes 14 Thru 21 — Not Used

Set to zero.

Sense Bytes 22 and 23 — Fault Symptom Code

The Fault Symptom Code provides entry to the Fault Symptom Index (FSI). The FSI lists possible failures and references MAPs. The Fault Symptom Code is a number generated from sense information by the storage control. The storage control places the code in Sense Bytes 22 and 23 in Sense Data Formats 1 and 4.

FORMAT 4 — MESSAGES

Message 0 — HA Area-Data Check

Message 0 is generated when a data error, as detected by the ECC hardware, occurs in the Home Address area.

Message 1 — Count Area-Data Check

Message 1 is generated when a data error, as detected by the ECC hardware, occurs in the Count area.

Message 2 — Key Area-Data Check

Message 2 is generated when a data error, as detected by the ECC hardware, occurs in the Key area.

Message 3 — Data Area-Uncorrectable Data Check

Message 3 is generated if an error occurs in the Data area that cannot be corrected by the ECC hardware.

Message 4 — HA Area-No Sync Byte Found

Message 4 is generated if data synchronization on the Home Address area was unsuccessful.

Message 5 — Count Area-No Sync Byte Found

Message 5 is generated if data synchronization on the Count area was unsuccessful.

Message 6 — Key Area-No Sync Byte Found

Message 6 is generated if data synchronization on the Key area was unsuccessful.

Message 7 — Data Area-No Sync Byte Found

Message 7 is generated if data synchronization on the Data area was unsuccessful.

Messages 8 Thru F — Not Used

FORMAT 5 — DATA CHECKS PROVIDING DISPLACEMENT INFORMATION

Format 5 is generated if the data error in the Data area is correctable. Data Check (Byte 0, bit 4) and Correctable (Byte 2, bit 1) are posted.

Sense Bytes 8 Thru 12 — Count ID

Sense Bytes 8 through 12 contain the record ID (CCHHR) as obtained from the Count area of the record in which the error occurred.

Sense Byte 12, the record number (R), is set to zero if the error occurred in the Home Address. This byte is unreliable after a space count.

The contents of these bytes are unreliable if the message code in Byte 7 is either 0 or 4 (error occurred in HA), or 1 or 5 (error occurred in Count area).

Sense Byte 13 — Sector Number

Sense Byte 13 contains the sector number of the record that was in error.

Sense Byte 14 — Not Used

Set to zero.

SENSE DATA DESCRIPTION

Sense Bytes 15 Thru 17 — Restart Displacement

Sense Bytes 15 through 17 identify the number of bytes processed by the storage control between the initiation of data transfer and the end of the Data field in error. The restart displacement includes the first byte transferred but excludes all immediate Home Addresses, Count, and Key areas that may have been clocked. Truncation within the operation does not affect the value of this parameter.

Sense Bytes 18 and 19 — Error Displacement

Sense Bytes 18 and 19 specify the location of the first byte in error within the Data field in relation to the end of that field.

Sense Bytes 20 Thru 22 — Error Pattern

Sense Bytes 20 through 22 identify the bits of a correctable Data Check that are in error. A logical 1 represents an incorrect bit. Byte 22 is always zero.

Sense Byte 23 — Not Used

Set to zero.

FORMAT 5 — MESSAGES

Messages 0 Thru 2 — Not Used

Set to zero.

Message 3 — Data Area-Correctable Data Check

Message 3 is generated if the correctable error occurred in the data area.

Messages 4 Thru F — Not Used

FORMAT 6 — USAGE AND OVERRUN ERROR STATISTICS

Format 6 is generated if the usage statistics or overrun errors require off-loading due to a counter overflow condition or if a Read and Reset Buffered Log command is issued.

Sense Bytes 8 Thru 11 — Bytes Read/Searched

Sense Bytes 8 through 11 provide an accumulated count of the number of bytes processed by the subsystem in Read or Search operations. Only Key and Data area counts are accumulated.

Sense Bytes 12 Thru 15 — Not Used

Set to zero.

Sense Bytes 16 and 17 — Access Motions

Sense Bytes 16 and 17 provide a count of the number of access motions processed by the subsystem.

Sense Byte 18 — Channel Select

BIT 0 — CHANNEL SELECT

Bit 0 indicates to which pair (A and B or C and D) of interfaces the information in Sense Bytes 20 through 23 applies. If bit 0 equals 0, the information applies to interfaces A and B. If bit 0 equals 1, the information applies to interfaces C and D.

BITS 1 THRU 7 — NOT USED

Sense Byte 19 — Not Used

Sense Byte 20 — Command Overrun A(C)

Sense Byte 20 indicates the number of channel A(C) Command Overruns detected by the storage control.

Sense Byte 21 — Data Overrun A(C)

Sense Byte 21 indicates the number of channel A(C) Data Overruns detected by the storage control.

Sense Byte 22 — Command Overrun B(D)

Sense Byte 22 indicates the number of channel B(D) Command Overruns detected by the storage control.

Sense Byte 23 — Data Overrun B(D)

Sense Byte 23 indicates the number of channel B(D) Data Overruns detected by the storage control.

OPER CONTENTS

OPER CONTENTS **OPER 1**

INTRODUCTION

The IBM 3344 Disk Storage is a direct access storage device that attaches to a 3340 subsystem.

The IBM 3340 subsystem must consist of a 3340 Control Module (A2) and any of the following combinations of satellite modules:

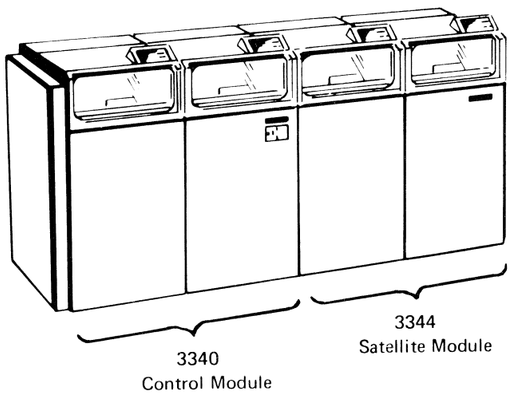
Up to three 3344 B2 or B2F (with fixed heads) modules.

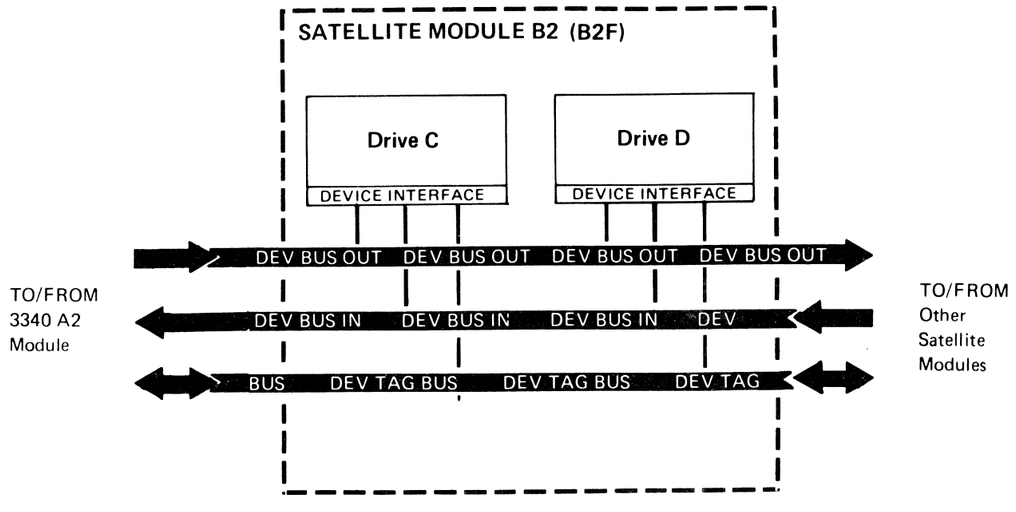
One 3340 B2 or B1 module and up to two 3344 B2 or B2F modules.

Up to two 3340 Bx*modules and one 3344 B2 or B2F module.

Up to three 3340 Bx*modules.

* Bx = Possible combinations of 3340 (B1 and B2) satellite modules





3344 CHARACTERISTICS

The IBM 3344 has these general characteristics:

- The storage medium is a Head/Disk Assembly (HDA)
- The HDA contains four logical 3340 volumes.
- Two 3344 models are available, B2 and B2F (fixed head).
- Rotation Position Sensing is a standard feature.
- Each drive can be serviced independently.

HEAD/DISK ASSEMBLY (HDA)

The Head/Disk Assembly (HDA) is similar to the 3340 Data Module (DM) in the following areas:

- The carriage, heads, and disks are enclosed in a sealed unit.
- The carriage and heads (access mechanism) are attached to and are moved by the Voice Coil Motor (VCM).

The Head/Disk Assembly (HDA) differs from the 3340 Data Module (DM) in the following areas:

- The HDA is not removable by the customer as the DM is.
- The HDA is larger than the DM.

See OPER 30 for a detailed HDA description.

LOGICAL 3340 VOLUMES

The Head/Disk Assembly is four times larger than the Data Module and has:

- Four times as may R/W data recording disk surfaces.
- Four times as many R/W heads.
- Four times as much data capacity.

Because the HDA is four times larger than the 3340 DM, the 3344 appears as four 3340s to the system. The HDA is divided into four logical volumes. Each of these logical volumes has a unique logical address as if each volume were one 3340 device.

See OPER 30 for a detailed HDA description.

3344 MODELS B2 and B2F

Two 3344 models are available:

B2 = 3344 containing two HDAs *without* fixed heads.

B2F = 3344 containing two HDAs *with* fixed heads.

See OPER 250 for a detailed description of fixed heads.

ROTATIONAL POSITION SENSING (RPS)

The 3344 differs from the 3340 in that Rotational Position Sensing is a standard feature on every 3344. It is an optional feature on the 3340.

See OPER 205 for a detailed description of RPS.

INDEPENDENT DRIVE MAINTENANCE

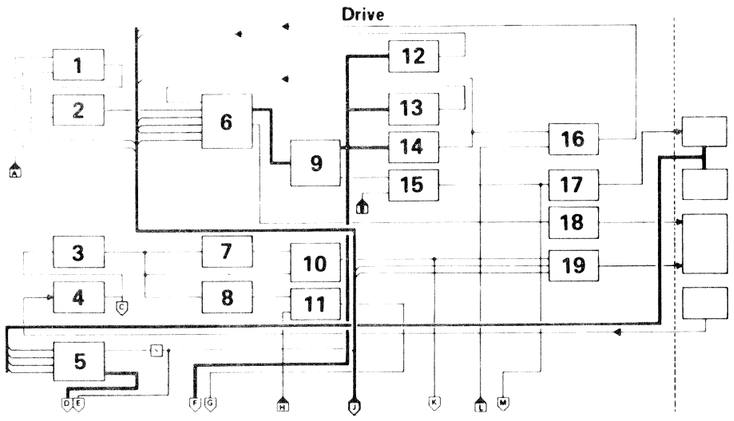
In each 3344 module, each drive has separate Read/Write electronics, power supplies, and sequencing controls to allow it to be serviced independently.

FUNCTIONAL UNITS

DRIVE

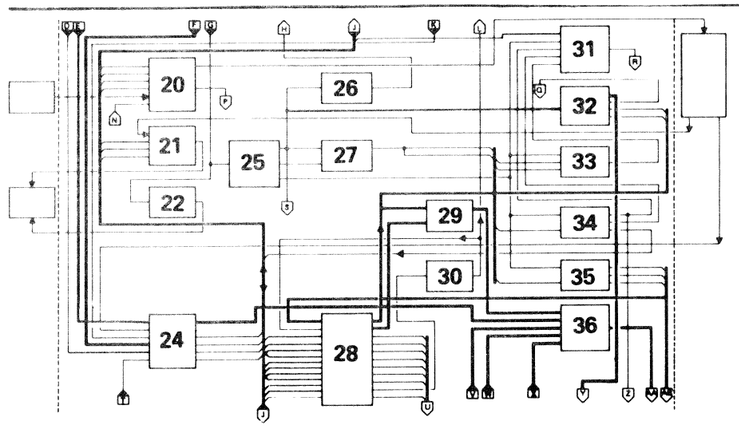
The following pages describe the functional units in the drive. The diagram on this page gives an overall view of the drive functional logic diagram. As indicated on the overall view, the diagram is contained on five pages: OPER 12, 15, 18, 21, and 24. Each of these pages is followed by pages explaining each functional unit as follows:

- The input, or inputs, to the functional unit and their source.
- The function of the functional unit.
- The output, or outputs, from the functional unit and their destination.



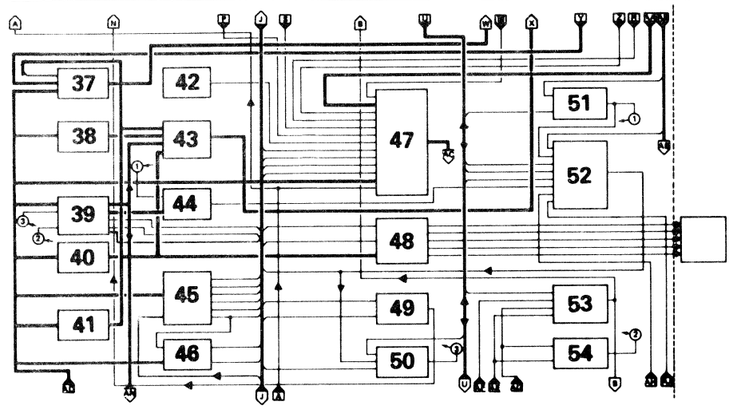
OPER 12

1. Inhibit HDA Sequence Generator (Card A1F2)
2. Stop Sequence Status Generator (Card A1F2)
3. Servo Clock Detector (Card A1C2)
4. Raw Servo Signal Amplifier (Card A1C2)
5. Drive Switches +24 V to MST Convertor (Card A1F2)
6. Bit Latches 1,2,4 (Card A1F2)
7. Access Control Timer Gate Generator (Card A1C2)
8. Incrementer (Card A1D4)
9. State Generator (Card A1F2)
10. Motor-at-Correct-Speed Detector (Card A1D4)
11. Voltage-Controlled Oscillator (Card A1C2)
12. Sequence Rezero Generator (Card A1F2)
13; 15 Second Delay Timer (Card A1F2)
14. Carriage Go Home Generator (Card A1E2)
15. Ready Lamp Driver (Card A1F2)
16. Go Home Complete Generator (Card A1E2)
17. Ready Lamp Driver (Card A1F2)
18. Drive Motor Run Relay Control (Card A1F2)
19. HDA Sequence Complete Relay Control (Card A1F2)



OPER 15

20. Write Data Gate (Card A1J2)
21. Read Data Detector (Card A1J2)
22. Read Servo Gate (Card A1H2)
23. (Not Used)
24. HDA Status Bits Generator (Card A1F2)
25. Servo Byte Counter (Card A1D4)
26. Decrementer (Card A1D4)
27. Index Shift Register (Card A1D4)
28. Access Control (Card A1E2)
29. Access Check Status Gate (Card A1E2)
30. Access Timeout Generator (Card A1C4)
31. Index Check (Card A1D4)
32. Sector Counter (Card A1J4)
33. Index Mark Generator (Card A1D4)
34. Valid Index Generator (Card A1D4)
35. Guardband Pattern Generator (Card A1D4)
36. MST Inbus Generator (Card A1H2)

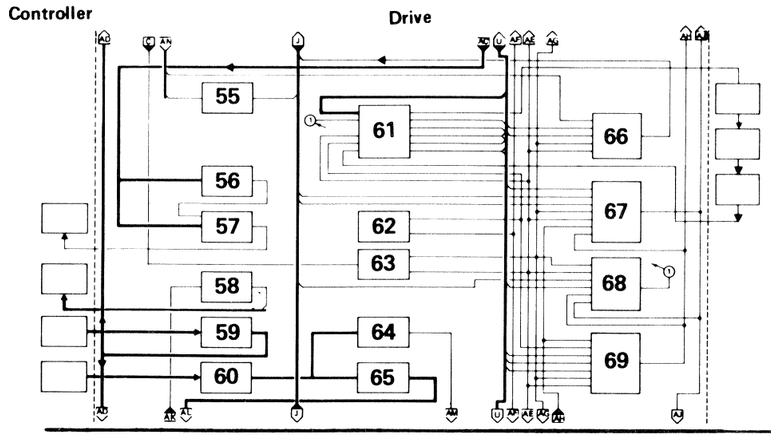


OPER 18

37. Target Register (Card A1J4)
38. Cylinder Address Register (Card A1G2)
39. Difference Counter and Control (Card A1G2)
40. Head Address Register (Card A1G2)
41. Sense Operations Decode (Card A1G2)
42. Head Short Detector (Card A1G2)
43. HAR or CAR or Difference Counter Output Gate (Card A1G2)
44. Digital-to-Analog Convertor (Card A1D2)
45. Read Write Control (Card A1H2)
46. Write Gate Control (Card A1H2)
47. Inbus Generator (Card A1H2)
48. Movable/Fixed Heads Decoder (Card A1G2)
49. Select Write Current Generator (Card A1G2)
50. Allow Difference Counter Generator (Card A1E2)
51. Position Enable Generator (Card A1C4)
52. End of Acceleration Detector (Card A1C4)
53. Track Following Timer (Card A1C4)
54. Track Crossing Detector (Card A1D2)

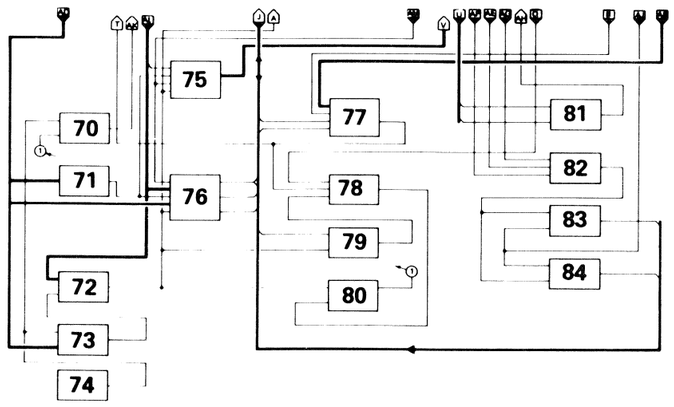
FUNCTIONAL UNITS

DRIVE



OPER 21

55. Even Track Detector (Card A1E2)
56. Inbus Parity Check (Card A1H2)
57. Inbus MST to NPL Convertor (Card A1H2)
58. Attn/Sel Bit MST to NPL Convertor (Card A1K2)
59. Dev Bus Out NPL to MST Convertor (Card A1K2)
60. Dev Tag Bus NPL to MST Convertor (Card A1K2)
61. Access Control Amplifier (Card A1C4)
62. +/−Error Demodulator and Amplifier (Card A1C2)
63. Dev Tag Bus Parity (Card A1K2)
64. Tag Decoder (Card A1K2)
65. Allow Rezero Generator (Card A1D2)
66. Allow Rezero Generator (Card A1D2)
67. Velocity Detector (Card A1D2)
68. Gated Position Derivative Generator (Card A1D2)
69. Access Current Magnitude Detector (Card A1D2)

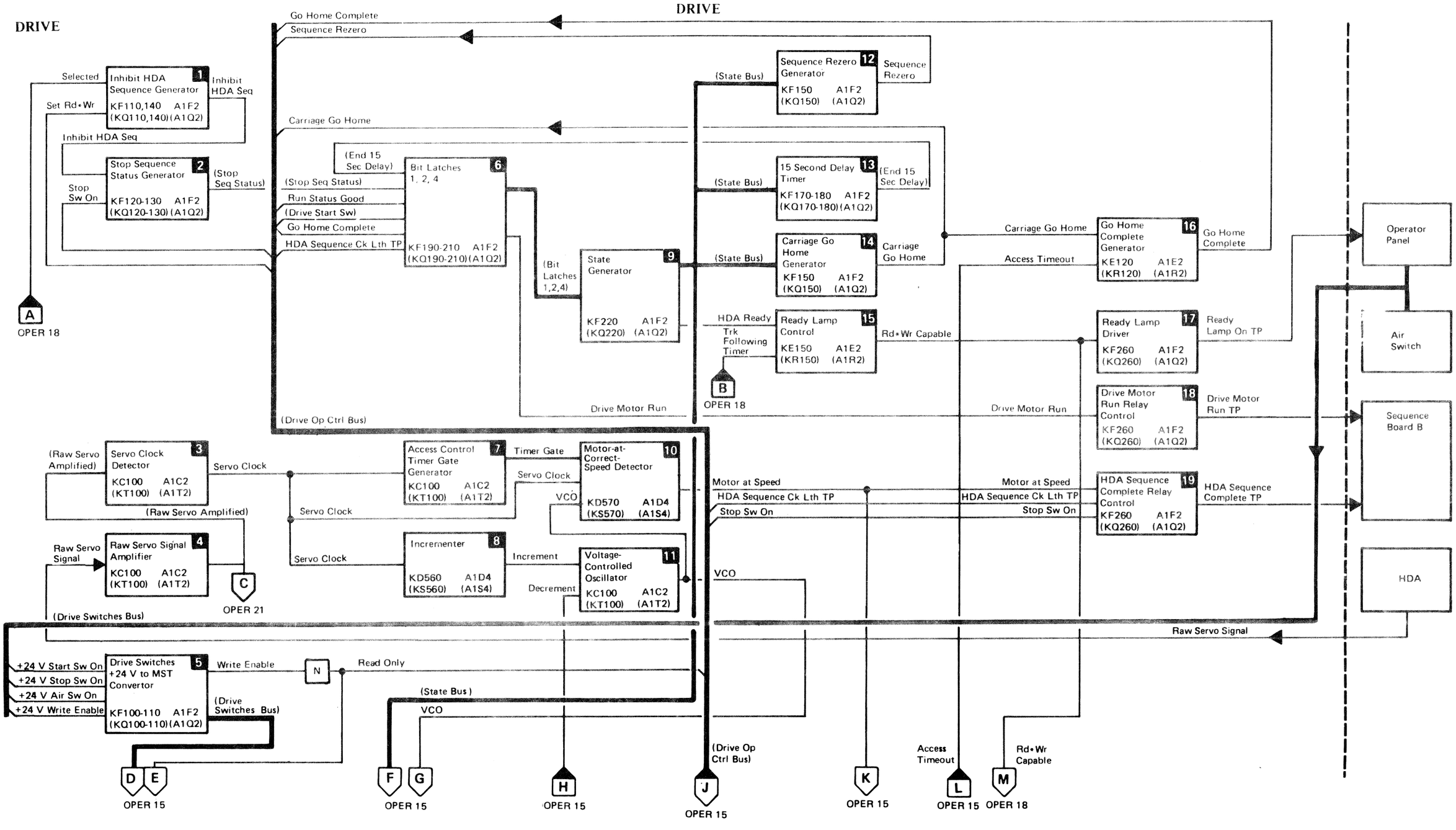


OPER 24

70. Attention/Select Bit Generator (Card A1K2)
71. Dev Bus Out Parity (Card A1K2)
72. Drive Selected Generator (Card A1K2)
73. Drive Address Compare (Card A1K2)
74. Drive Logical Address Jumpers (Card A1K2)
75. Interface Status Bits Generator (Card A1K2)
76. Drive Operation Control (Card A1K2)
77. Access Complete Generator (Card A1E2)
78. Attention Generator (Card A1E2)
79. Access Busy Generator (Card A1E2)
80. Normal Attention Generator (Card A1K2)
81. Velocity Enable Generator (Card A1C4)
82. On Track Detector (Card A1C4)
83. Velocity Intensity Detector (Card A1C4)
84. End of Deceleration Detector (Card A1C4)

DRIVE

DRIVE



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FUNCTIONAL UNITS

DRIVE

1 Inhibit HDA Sequence Generator (Card A1F2)

The Inhibit HDA Sequence Generator functions as follows:

- Receives

  Selected from the Drive Selected Generator (card A1K2).

  Set Rd*Wr via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).

- Generates the Inhibit HDA Seq signal.
- Sends Inhibit HDA Seq to the Stop Sequence Status Generator (card A1F2).

2 Stop Sequence Status Generator (Card A1F2)

The Stop Sequence Status Generator functions as follows:

- Receives

  Inhibit HDA Seq from the Inhibit Sequence Generator (card A1F2).

  Stop Sw On via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).

- Generates the Stop Seq Status signal.
- Sends Stop Seq Status to the Bit Latches 1, 2, 4 (card A1F2).

3 Servo Clock Detector (Card A1C2)

The Servo Clock Detector functions as follows:

- Receives Raw Servo Amplified from the Raw Servo Signal Amplifier (card A1C2).
- Detects the Servo Clock from Raw Servo Amplified.
- Sends Servo Clock to the following:

  Access Control Timer Gate Generator (card A1C2)

  Motor-at-Correct-Speed Detector (card A1D4)

  Incrementer (card A1D4)

4 Raw Servo Signal Amplifier (Card A1C2)

The Raw Servo Signal Amplifier functions as follows:

- Receives Raw Servo Signal from the HDA.
- Amplifies Raw Servo Signal and generates Raw Servo Amplified.
- Sends Raw Servo Amplified to the following:

  Servo Clock Detector (card A1C2)

  +/− Error Demodulator and Amplifier (card A1C2)

5 Drive Switches +24 V to MST Convertor (Card A1F2)

The Drive Switches +24 V to MST Convertor functions as follows:

- Receives drive switch signals via the Drive Switches Bus from the operator panel and the air switch.
- Converts drive switch +24 V voltage levels to MST voltage levels.
- Sends drive switch MST voltage levels via Read Only and the Drive Switches Bus to the HDA Status Bits Generator (card A1F2).
- Also sends Read Only via the Drive Op Ctrl Bus to the Inbus Generator (card A1H2).

6 Bit Latches 1, 2, 4 (Card A1F2)

The Bit Latches 1, 2, 4 block functions as follows:

- Receives

  End 15 Sec Delay from the 15 Second Delay Timer (card A1F2)

  Stop Seq Status from the Stop Sequence Status Generator (card A1F2)

- Also receives the following via the Drive Op Ctrl Bus:

  Run Status Good from the HDA Status Bits Generator (card A1F2).

  Drive Start Sw from the HDA Status Bits Generator (card A1F2).

  Go Home Complete from the Go Home Complete Generator (card A1E2).

  HDA Sequence Ck Lth TP from the HDA Status Bits Generator (card A1E2).

- Generates Bit Latches 1, 2, 4 and sends them to the State Generator (card A1F2).
- Generates Drive Motor Run and sends it to the Drive Motor Run Relay Control (card A1F2).

7 Access Control Timer Gate Generator (Card A1C2)

The Access Control Timer Gate Generator functions as follows:

- Receives Servo Clock from the Servo Clock Detector (card A1C2).
- Generates Timer Gate.
- Sends Timer Gate to the Motor-at-Correct-Speed Detector (card A1D4).

8 Incrementer (Card A1D4)

The Incrementer functions as follows:

- Receives Servo Clock from the Servo Clock Detector (card A1C2).
- Generates Increment.
- Sends Increment to the Voltage Controlled Oscillator (card A1C2).

9 State Generator (Card A1F2)

The State Generator functions as follows:

- Receives Bit Latches 1, 2, 4 from the Bit Latches 1, 2, 4 (card A1F2).
- Generates the State Bus and sends it to the following:

  Sequence Rezero Generator (card A1F2)

  15 Second Delay Timer (card A1F2)

  Carriage Go Home Generator (card A1F2)

  HDA Status Bits Generator (card A1F2)

- Generates HDA Ready and sends it to the Ready Lamp Control (card A1E2).

10 Motor-at-Correct-Speed Detector (Card A1D4)

The Motor-at-Correct-Speed Detector functions as follows:

- Receives

  Timer Gate from the Access Control Timer Gate Generator (card A1C2)

  Servo Clock from the Servo Clock Detector (card A1C2)

  VCO from the Voltage-Controlled Oscillator (card A1C2)

- Generates Motor at Speed.
- Sends Motor at Speed to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  HDA Status Bits Generator (card A1F2)

11 Voltage-Controlled Oscillator (Card A1C2)

The Voltage-Controlled Oscillator functions as follows:

- Receives

  Increment from the Incrementer (card A1D4)

  Decrement from the Decrementer (card A1D4)

- Generates the VCO signal.
- Sends VCO to the following:

  Servo Byte Counter (card A1D4)

  Read Servo Gate (card A1H2)

  Motor-at-Correct-Speed Detector (card A1D4)

12 Sequence Rezero Generator (Card A1F2)

The Sequence Rezero Generator functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates Sequence Rezero.
- Sends Sequence Rezero via the Drive Op Ctrl Bus to the Access Control (card A1E2).

13 15 Second Delay Timer (Card A1F2)

The 15 Second Delay Timer functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates End 15 Sec Delay.
- Sends End 15 Sec Delay to the Bit Latches 1, 2, 4 (card A1F2).

FUNCTIONAL UNITS

DRIVE

14 Carriage Go Home Generator (Card A1F2)

The Carriage Go Home Generator functions as follows:

- Receives the State Bus from the State Generator (card A1F2).
- Generates Carriage Go Home.
- Sends Carriage Go Home to the following:

  Go Home Complete Generator (card A1E2)

  Access Control (card A1E2) via the Drive Op Ctrl Bus.

15 Ready Lamp Control (Card A1E2)

The Ready Lamp Control functions as follows:

- Receives

  HDA Ready from the State Generator (card A1F2).

  Trk Following Timer from the Track Following Timer (card A1C4)

- Generates Rd*Wr Capable.
- Sends Rd*Wr Capable to the following:

  Ready Lamp Driver (card A1F2)

  Inbus Generator (card A1H2)

16 Go Home Complete Generator (Card A1E2)

The Go Home Complete Generator functions as follows:

- Receives

  Carriage Go Home from the Carriage Go Home Generator (card A1F2).

  Access Timeout from the Access Timeout Generator (card A1C4).

- Generates Go Home Complete.
- Sends Go Home Complete via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).

17 Ready Lamp Driver (Card A1F2)

The Ready Lamp Driver functions as follows:

- Receives Rd*Wr Capable from the Ready Lamp Control (card A1E2).
- Generates and amplifies Ready Lamp On TP.
- Sends Ready Lamp On TP to the Ready Lamp on the Operator Panel.

18 Drive Motor Run Relay Control (Card A1F2)

The Drive Motor Run Relay Control functions as follows:

- Receives Drive Motor Run from the Bit Latches 1, 2, 4 (card A1F2).
- Generates and amplifies Drive Motor Run TP.
- Sends Drive Motor Run TP to the Drive Motor Run Relay on the Sequence Board B.

19 HDA Sequence Complete Relay Control (Card A1F2)

The HDA Sequence Complete Relay Control functions as follows:

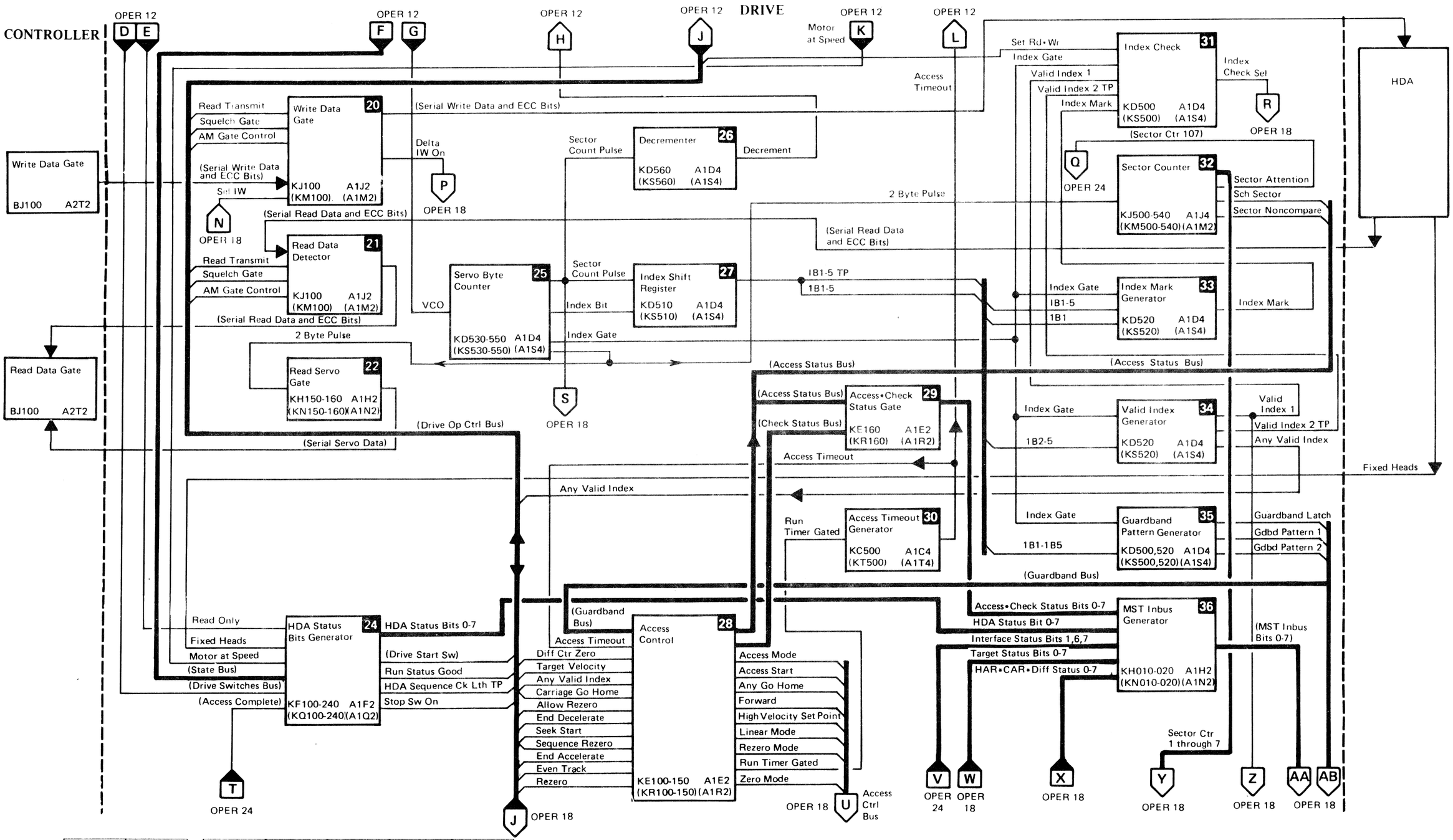
- Receives

  Motor at Speed from the Motor-at-Correct-Speed Detector (card A1D4).

  HDA Sequence Chk Lth TP via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).

  Stop Sw On via the Drive Op Ctrl Bus from the HDA Status Bits Generator (card A1F2).

- Generates and amplifies HDA Sequence Complete TP.
- Sends HDA Sequence Complete TP to the HDA Sequence Complete Relay on the Sequence Board B.



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FUNCTIONAL UNITS

DRIVE

20 Write Data Gate (Card A1J2)

The Write Data Gate functions as follows:

- Receives the following via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2):

  Read Transmit

  Squelch Gate

  AM Gate Control

- Also receives:

  Serial Write Data and ECC Bits from the Write Data Gate (card A2T2) in the controller.

  Sel IW from the Select Write Current Generator (card A1G2).

- Gates Serial Write Data and ECC Bits to the HDA.
- Generates Delta IW On and sends it to the Inbus Generator (card A1H2).

21 Read Data Detector (Card A1J2)

The Read Data Detector functions as follows:

- Receives

  Serial Read Data and ECC Bits from the HDA.

  Read Transmit via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  Squelch Gate via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  AM Gate Control via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

- Detects the Serial Read Data and ECC Bits from the HDA.
- Sends Serial Read Data and ECC Bits to the Read Data Gate (card A2T2) in the controller.

22 Read Servo Gate (Card A1H2)

The Read Servo Gate functions as follows:

- Receives the 2 Byte Pulse (a function of VCO) from the Servo Byte Counter (card A1D2).
- Sends VCO as Serial Servo Data to the Read Data Gate (card A2T2) in the controller.

24 HDA Status Bits Generator (Card A1F2)

The HDA Status Bits Generator functions as follows:

- Receives

  Fixed Heads from the HDA.

  Motor at Speed from the Motor-at-Correct-Speed Detector (card A1D4).

  State Bus from the State Generator (card A1F2)

  Drive Switches Bus from the Drive Switches +24 V to MST Convertor (card A1F2).

  Access Complete from the Access Complete Generator (card A1E2)

- Generates HDA Status Bits 0 through 7 and sends them to the MST Inbus Generator (card A1H2).
- Generates Drive Start Sw and sends it via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).
- Generates Run Status Good and sends it via the Drive Op Ctrl Bus to the Bit Latches 1, 2, 4 (card A1F2).
- Generates HDA Sequence Ck Lth TP and sends it via the Drive Op Ctrl Bus to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  Bit Latches 1, 2, 4 (card A1F2)

- Generates Stop Sw On and sends it via the Drive Op Ctrl Bus to the following:

  HDA Sequence Complete Relay Control (card A1F2)

  Stop Sequence Status Generator (card A1F2)

25 Servo Byte Counter (Card A1D4)

The Servo Byte Counter functions as follows:

- Receives the VCO signal from the Voltage-Controlled Oscillator (card A1C2).
- Generates Sector Count Pulse each time a certain number of VCO pulses are counted.
- Sends Sector Count Pulse to the following:

  Decrementer (card A1D4)

  Index Shift Register (card A1D4)

  Inbus Generator (card A1H2)

- Generates Index Bit and sends it to the Index Shift Register (card A1D4).
- Generates Index Gate and sends it to the following:

  Index Check (card A1D4)
  Index Mark Generator (card A1D4)

  Valid Index Generator (card A1D4)

  Guardband Pattern Generator (card A1D4)

- Generates the 2 Byte Pulse from VCO and sends it to the Read Servo Gate (card A1F2) and the Sector Counter (card A1J4).

26 Decrementer (Card A1D4)

The Decrementer functions as follows:

- Receives Sector Count Pulse from the Servo Byte Counter (card A1D4).
- Generates Decrement.
- Sends Decrement to the Voltage-Controlled Oscillator (card A1C2).

27 Index Shift Register (Card A1D4)

The Index Shift Register functions as follows:

- Receives

  Sector Count Pulse from the Servo Byte Counter (card A1D4).

  Index Bit from the Servo Byte Counter (card A1D4).

- Generates IB1 through 5 TP and also 1B1 through 5.
- Sends IB1 through 5 TP and also 1B1 through 5 via the Index Shift Bus to the following:

  Index Mark Generator (card A1D4)

  Valid Index Generator (card A1D4)

  Guardband Pattern Generator (card A1D4)

28 Access Control (Card A1E2)

The Access Control functions as follows:

- Receives

  The Guardband Bus from the Guardband Pattern Generator (Card A1C4).

  The Access Timeout signal from the Access Timeout Generator (card A1C4).

- Also receives the following control signals via the Drive Op Ctrl Bus:

  Diff Ctr Zero from the Difference Counter and Control (card A1G2).

  Target Velocity from the Velocity Intensity Generator (card A1C4).

  Any Valid Index from the Valid Index Generator (card A1D4).

  Carriage Go Home from the Carriage Go Home Generator (card A1F2).

  Allow Rezero from the Allow Rezero Generator (card A1D2).

  End Decelerate from the End of Deceleration Detector (card A1C4).

  Seek Start from the Drive Operation Control (card A1K2).

  Sequence Rezero from the State Generator (card A1F2).

  End Accelerate from the End of Acceleration Detector (card A1C4).

  Even Track from the Even Track Detector (card A1E2).

  Rezero from the Drive Operation Control (card A1K2).

FUNCTIONAL UNITS

DRIVE

- Generates Access Mode and sends it via the Access Ctrl Bus to the following:
  - End of Acceleration Detector (card A1C4)
  - Allow Difference Counter Generator (card A1E2)
  - Access Control Amplifier (card A1C4)
  - Velocity Detector (card A1D2)
- Generates Access Start and sends it via the Access Ctrl Bus to the Allow Rezero Generator (card A1D2).
- Generates Any Go Home and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Velocity Enable Generator (card A1C4)
- Generates the Forward signal and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Allow Rezero Generator (card A1D2)
- Generates High Velocity Set Point and sends it via the Access Ctrl Bus to the End of Acceleration Detector (card A1C4).
- Generates Linear Mode and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Track Following Timer (card A1C4)
- Generates Rezero Mode and sends it via the Access Ctrl Bus to the Access Control Amplifier (card A1C4).
- Generates Run Timer Gated and sends it to the Access Timeout Generator (card A1C4).
- Generates Zero Mode and sends it via the Access Ctrl Bus to the following:
  - Access Control Amplifier (card A1C4)
  - Velocity Enable Generator (card A1C4)

29 Access Check Status Gate (Card A1E2)

The Access*Check Status Gate functions as follows:

- Receives Access Status Bus from the following:
  - Access Control (card A1E2)
  - Sector Counter (card A1J4)
- Receives Check Status Bus from the Access Control (card A1E2)
- Gates the Access*Check Status Bits 0 through 7 to the MST Inbus Generator (card A1H2).

30 Access Timeout Generator (Card A1C4)

The Access Timeout Generator functions as follows:

- Receives Run Timer Gated from the Access Control (card A1E2).
- Generates Access Timeout.
- Sends Access Timeout to the following:
  - Access Control (card A1E2)
  - Go Home Complete Generator (card A1F2)

31 Index Check (Card A1D4)

The Index Check functions as follows:

- Receives
  - Set Rd*Wr via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).
  - Index Gate from the Servo Byte Counter (card A1D4).
  - Valid Index 1 from the Valid Index Generator (card A1D4).
  - Valid Index 2 TP from the Valid Index Generator (card A1D4).
  - Index Mark from the Index Mark Generator (card A1D4).
- Generates Index Check Sel.
- Sends Index Check Sel to the Inbus Generator (card A1H2).

32 Sector Counter (Card A1J4)

The Sector Counter functions as follows:

- Receives 2 Byte Pulse from the Servo Byte Counter (card A1D4).
- Counts sector count pulses (2 Byte Pulses) and generates Sector Ctr 1 through 7.
- Sends Sector Ctr 1 through 7 to the Target Register (card A1J4).

The Sector Counter also:

- Generates Sector Attention and sends it to the Attention Generator (card A1E4).
- Generates Sch Sector and sends it via the Access Status Bus to the Access*Check Status Gate (card A1E2).
- Generates Sector Noncompare and sends it via the Access Status Bus to the Access*Check Status Gate (card A1E2).

33 Index Mark Generator (Card A1D4)

The Index Mark Generator functions as follows:

- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - IB1 through 5 from the Index Shift Register (card A1D4).
  - 1B1 from the Index Shift Register (card A1D4).
- Generates Index Mark when the Index Shift Register (card A1D4) is full.
- Sends Index Mark to the Index Check (card A1D4).

34 Valid Index Generator (Card A1D4)

The Valid Index Generator functions as follows:

- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - 1B2 through 5 from the Index Shift Register (card A1D4).
- Generates Valid Index 1 and sends it to the Index Check (card A1D4).
- Generates Valid Index 2 TP and sends it to the Index Check (card A1D4).
- Generates Any Index Valid and sends it via the Drive Op Ctrl Bus to the following:
  - Allow Difference Counter Generator (card A1E2)
  - Access Complete Generator (card A1E2)

35 Guardband Pattern Generator (Card A1D4)

The Guardband Pattern Generator functions as follows:

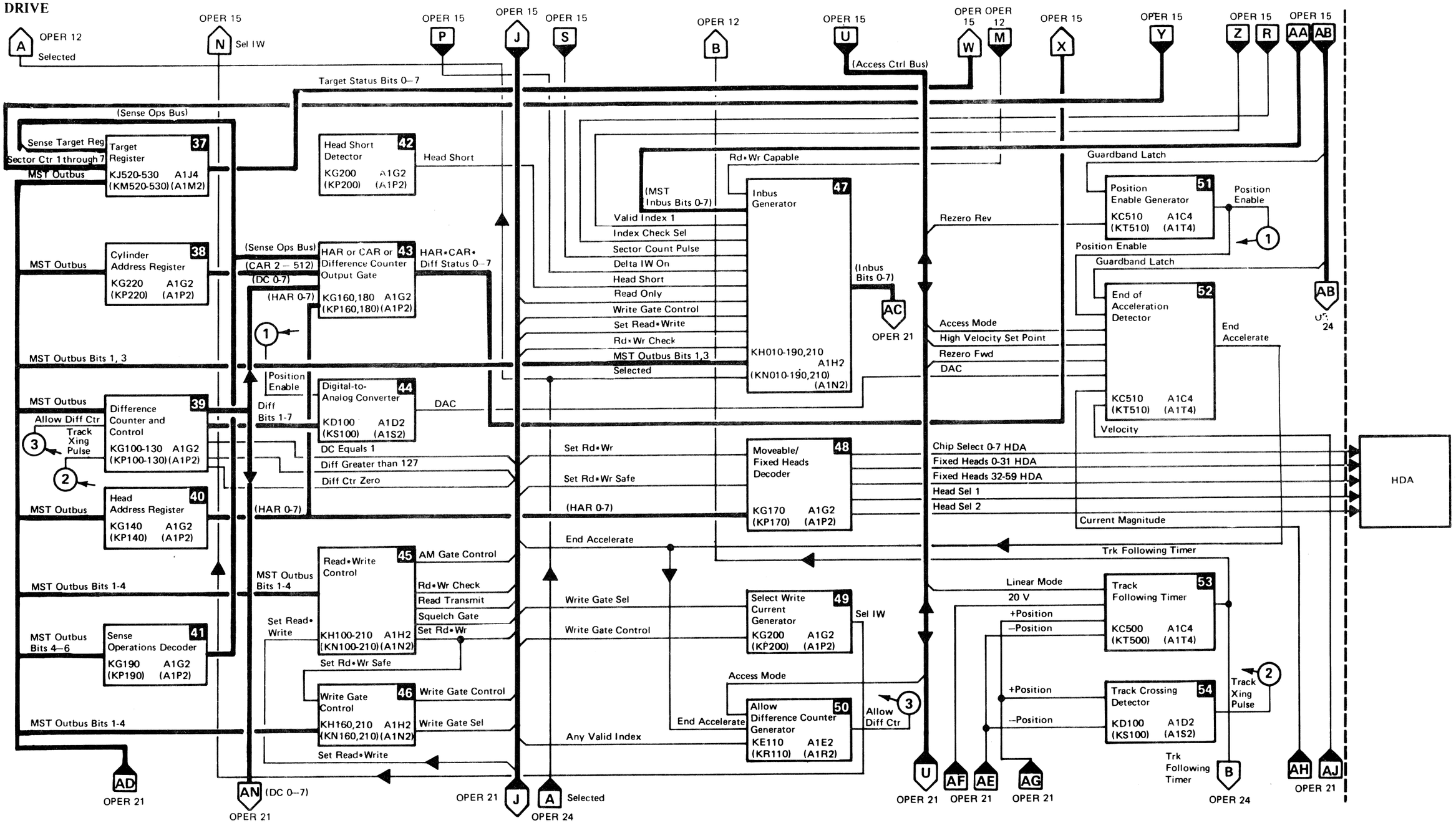
- Receives
  - Index Gate from the Servo Byte Counter (card A1D4).
  - 1B1 through 5 from the Index Shift Register (card A1D4).
- Generates
  - Guardband Latch
  - Guardband Pattern 1
  - Guardband Pattern 2
- Sends the generated signals via the Guardband Bus to the following:
  - Access Control (card A1E2)
  - Position Enable Generator (card A1C4)
  - End of Acceleration Detector (card A1C4)
  - Access Complete Generator (card A1E2)

36 MST Inbus Generator (Card A1H2)

The MST Inbus Generator functions as follows:

- Receives
  - Access*Check Status Bits 0 through 7 from the Access*Check Status Gate (card A1E2).
  - HDA Status Bits 0 through 7 from the HDA Status Bits Generator (card A1F2).
  - Interface Status Bits 1, 6, 7 from the Interface Status Bits Generator (card A1K2).
  - Target Status Bits 0 through 7 from the Target Register (card A1J4).
  - HAR*CAR*Diff Status 0 through 7 from the HAR or CAR or Difference Counter Output Gate (card A1G2).
- Sends the HDA Status Bits, the Access*Check Status Bits, the Interface Status Bits, the Target Status Bits, or the HAR*CAR*Diff Status via the MST Inbus Bits 0 through 7 to the Inbus Generator (card A1H2)

DRIVE



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FUNCTIONAL UNITS

DRIVE

37 Target Register (Card A1J4)

The Target Register functions as follows:

- Receives

  Sense Target Reg via the Sense Ops Bus from the Sense Operations Decoder (card A1G2).

  Sector Ctr 1 through 7 from the Sector Counter (card A1J4).

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

- Generates Target Status Bits 0 through 7.
- Sends the Target Status Bits 0 through 7 to the MST Inbus Generator (card A1H2).

38 Cylinder Address Register (Card A1G2)

The Cylinder Address Register functions as follows:

- Receives the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Generates CAR 2 through 512.
- Sends CAR 2 through 512 to the HAR or CAR or Difference Counter Output Gate (card A1G2).

39 Difference Counter and Control (Card A1G2)

The Difference Counter and Control functions as follows:

- Receives

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Allow Diff Ctr from the Allow Difference Counter Generator (card A1E2).

  Track Xing Pulse from the Track Crossing Detector (card A1D2).

- Generates DC 0 through 7 and sends them to the HAR or CAR or Difference Counter Output Gate (card A1G2).
- Also sends DC 7 via DC 0 through 7 to the following:

  Even Track Detector (card A1E2)

  Allow Rezero Generator (card A1D2)

- Generates Diff Bits 1 through 7 and sends them to the Digital-to-Analog Convertor (card A1D2).
- Generates DC equals 1 and sends it via the Drive Op Ctrl Bus to the following:

  Velocity Detector (card A1D2)

  Gated Positive Derivative Generator (card A1D2)

- Generates Diff Greater than 127 and sends it via the Drive Op Ctrl Bus to the Velocity Detector (card A1D2).
- Generates Diff Ctr Zero and sends it via the Drive Op Ctrl Bus to the Access Control (card A1E2).

40 Head Address Register (Card A1G2)

The Head Address Register (HAR) functions as follows:

- Receives the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Generates HAR 0 through 7.
- Sends HAR 0 through 7 to the following:

  HAR or CAR or Difference Counter Output Gate (card A1G2).

  Movable/Fixed Heads Decoder (card A1G2).

41 Sense Operations Decoder (Card A1G2)

The Sense Operations Decoder functions as follows:

- Receives MST Outbus Bits 4 through 6 from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Decodes MST Outbus Bits 4 through 6 into Sense Ops Bus.
- Sends Sense Ops Bus to the following:

  HAR or CAR or Difference Counter Output Gate (card A1G2)

  Target Register (card A1J4)

42 Head Short Detector (Card A1G2)

The Head Short Detector functions as follows:

- Generates the signal Head Short when more than one head is detected On during a Write operation.
- Sends Head Short to the Inbus Generator (card A1H2).

43 HAR or CAR or Difference Counter Output Gate (Card A1G2)

The HAR or CAR or Difference Counter Output Gate functions as follows:

- Receives

  Sense Ops Bus from the Sense Operations Decoder (card A1G2).

  CAR 2 through 512 from the Cylinder Address Register (CAR) (card A1G2).

  DC 0 through 7 from the Difference Counter and Control (card A1G2).

  HAR 0 through 7 from the Head Address Register (HAR) (card A1G2).

- Gates CAR 2 through 512, DC 0 through 7, or HAR 0 through 7 to the MST Inbus Generator (card A1H2).

44 Digital-to-Analog Convertor (Card A1D2)

The Digital-to-Analog Convertor functions as follows:

- Receives

  Position Enable from the Position Enable Generator (card A1C4).

  Diff Bits 1 through 7 from the Difference Counter and Control (card A1G2).

- Converts the Diff Bits 1 through 7 digital inputs into the DAC analog output.
- Sends DAC to the End of Acceleration Detector (card A1C4).

45 Read*Write Control (Card A1H2)

The Read*Write Control functions as follows:

- Receives

  MST Outbus Bits 1 through 4 from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Set Read*Write via the Drive Op Ctrl Bus from the Drive Operation Control (card A1K2).

- Generates AM Gate Control and sends it via the Drive Op Ctrl Bus to the Read Data Detector (card A1J2).
- Generates Rd*Wr Check and sends it via the Drive Op Ctrl Bus to the Inbus Generator (card A1H2).
- Generates Read Transmit and sends it via the Drive Op Ctrl Bus to the following:

  Read Data Detector (card A1J2)

  Write Data Gate (card A1J2)

- Generates Squelch Gate and sends it via the Drive Op Ctrl Bus to the following:

  Read Data Detector (card A1J2)

  Write Data Gate (card A1J2)

- Generates Set Rd*Wr and sends it via the Drive Op Ctrl Bus to the following:

  Movable/Fixed Heads Decoder (card A1G2)

  Index Check (card A1D4)

  Inhibit HDA Sequence Generator (card A1F2)

- Generates Set Rd*Wr Safe and sends it to the Write Gate Control (card A1H2) and via the Drive Op Ctrl Bus to the Movable/Fixed Heads Decoder (card A1G2).

46 Write Gate Control (Card A1H2)

The Write Gate Control functions as follows:

- Receives

  Set Rd*Wr Safe from the Read/Write Control (card A1H2).

  MST Outbus Bits 1 through 4 from the Dev Bus Out NPL to the MST Convertor (card A1K2).

- Generates Write Gate Control and sends it via the Drive Op Ctrl Bus to the following:

  Select Write Current Generator (card A1G2)

  Inbus Generator (card A1H2)

- Generates Write Gate Sel and sends it via the Drive Op Ctrl Bus to the Select Write Current Generator (card A1G2).

FUNCTIONAL UNITS

DRIVE

47 Inbus Generator (Card A1H2)

The Inbus Generator functions as follows:

- Receives

  Rd*Wr Capable from the Ready Lamp Control (card A1E2).

  MST Inbus Bits 0 through 7 from the MST Inbus Generator (card A1H2).

  Valid Index 1 from the Valid Index Generator (card A1D4).

  Index Check Sel from the Index Check (card A1D4).

  Sector Count Pulse from the Servo Byte Counter (card A1D4).

  Delta IW On from the Write Data Gate (card A1J2).

  Head Short from the Head Short Detector (card A1G2).

  Read Only via the Drive Op Ctrl Bus from the Drive Switches +24 V to MST Convertor (card A1F2).

  Write Gate Control via the Drive Op Ctrl Bus from the Write Gate Control (card A1H2).

  Set Read*Write via the Drive Op Ctrl Bus from the Drive Operations Control (card A1K2).

  Rd*Wr Check via the Drive Op Ctrl Bus from the Read/Write Control (card A1H2).

  MST Outbus Bits 1, 3 via the MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  The signal, Selected, from the Drive Selected Generator (card A1K2).

- Generates Inbus Bits 0 through 7.
- Sends Inbus Bits 0 through 7 to the following:

  Inbus Parity Check (card A1H2)

  Inbus MST to NPL Convertor (card A1H2)

48 Movable/Fixed Heads Decoder (Card A1G2)

The Movable/Fixed Heads Decoder functions as follows:

- Receives

  Set Rd*Wr via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).

  Set Rd*Wr via the Drive Op Ctrl Bus from the Read*Write Control (card A1H2).

  HAR 0 through 7 from the Head Address Register (HAR) (card A1G2).

- Generates the following and sends them to the HDA:

  Chip Select 0 through 7 HDA

  Fixed Heads 0 through 31 HDA

  Fixed Heads 32 through 59 HDA

  Head Sel 1

  Head Sel 2

49 Select Write Current Generator (Card A1G2)

The Select Write Current Generator functions as follows:

- Receives the following via the Drive Op Ctrl Bus from the Write Gate Control (card A1H2)

  Write Gate Sel

  Write Gate Control

- Generates Sel IW.
- Sends Sel IW to the Write Data Gate (card A1J2).

50 Allow Difference Counter Generator (Card A1E2)

The Allow Difference Counter Generator functions as follows:

- Receives

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  End Accelerate from the End of Acceleration Detector (card A1C4).

  Any Valid Index via the Drive Op Ctrl Bus from the Valid Index Generator (card A1D4).

- Generates the Allow Diff Ctr signal.
- Sends Allow Diff Ctr to the Difference Counter and Control (card A1G2).

51 Position Enable Generator (Card A1C4)

The Position Enable Generator functions as follows:

- Receives

  Guardband Latch via the Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Rezero Rev via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

- Generates Position Enable.
- Sends Position Enable to the following:

  End of Acceleration Detector (card A1C4)

  Digital-to-Analog Convertor (DAC) (card A1D2)

52 End of Acceleration Detector (Card A1C4)

The End of Acceleration Detector functions as follows:

- Receives

  Guardband Latch via the Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Position Enable from the Position Enable Generator (card A1C4).

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  High Velocity Set Point via the Access Ctrl Bus from the Access Control (card A1E2).

  Rezero Fwd via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  DAC from the Digital-to-Analog Convertor (card A1D2).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

  The Velocity signal from the Velocity Detector (card A1D2).

- Detects the end of acceleration of the carriage and generates End Accelerate.
- Sends End Accelerate to the Allow Difference Counter Generator (card A1E2) and also via the Drive Op Ctrl Bus to the Access Control (card A1C2).

53 Track Following Timer (Card A1C4)

The Track Following Timer functions as follows:

- Receives

  Linear Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  20 V from the Reference Voltage Generator (card A1C2).

  + Position and also – Position from the +/– Error Demodulator and Amplifier (card A1C2).

- Generates the Track Following Timer signal.
- Sends Track Following Timer to the following:

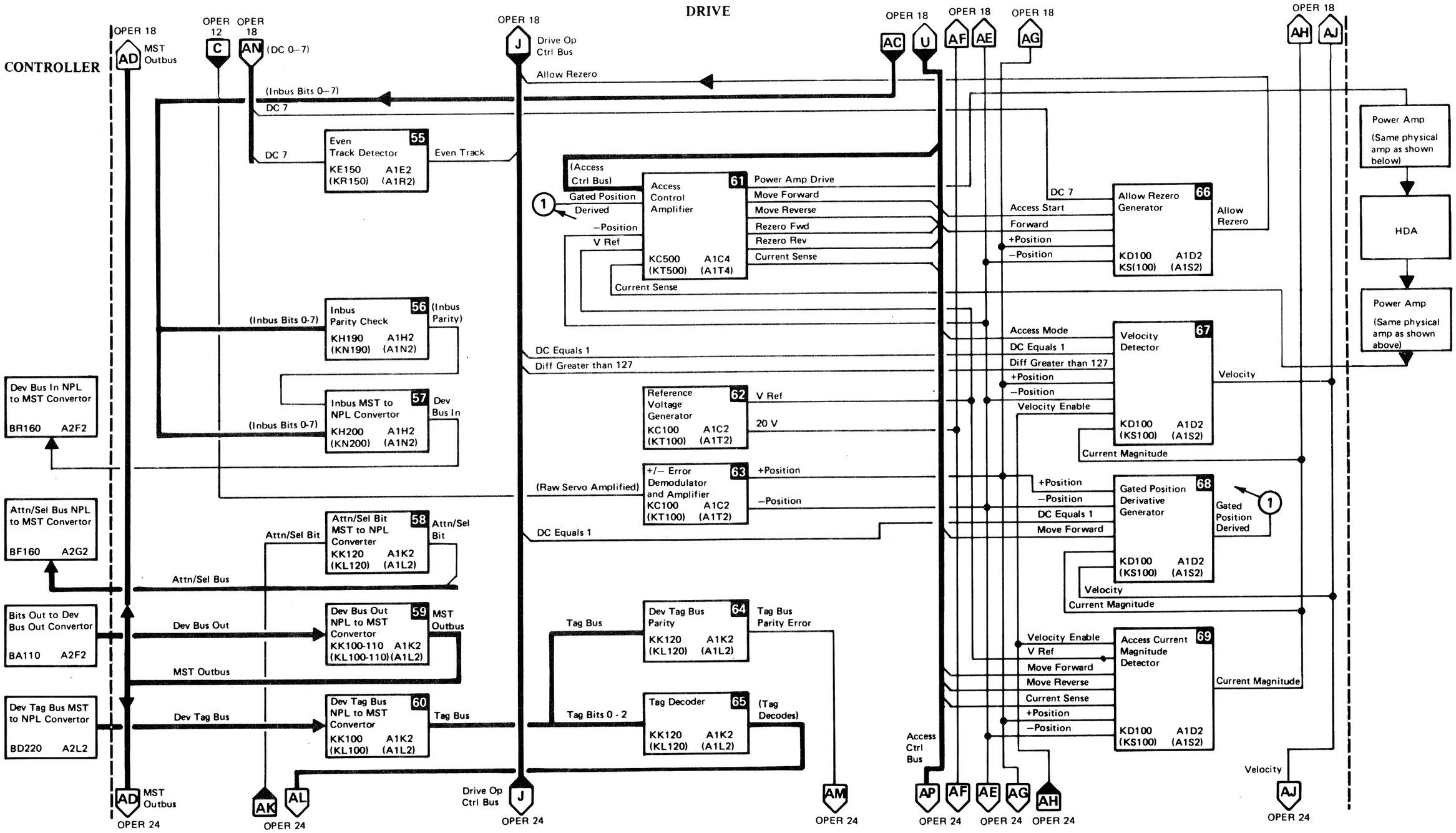
  Ready Lamp Control (card A1E2)

  Access Complete Generator (card A1E2).

54 Track Crossing Detector (Card A1D2)

The Track Crossing Detector functions as follows:

- Receives + Position and also – Position from the +/– Error Demodulator and Amplifier (card A1C2).
- Generates Track Xing Pulse.
- Sends Track Xing Pulse to the Difference Counter and Control (card A1G2).



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FUNCTIONAL UNITS

DRIVE

55 Even Track Detector (Card A1E2)

The Even Track Detector functions as follows:

- Receives DC 7 via DC 0 through 7 from the Difference Counter and Control (card A1G2).
- Generates Even Track.
- Sends Even Track via the Drive Op Ctrl Bus to the Access Control (card A1E2).

56 Inbus Parity Check (Card A1H2)

The Inbus Parity Check functions as follows:

- Receives Inbus Bits 0 through 7 from the Inbus Generator (card A1H2).
- Generates the Inbus Parity signal when an even number of Inbus bits are active.
- Sends Inbus Parity to the Inbus MST to NPL Convertor (card A1H2).

57 Inbus MST to NPL Convertor (Card A1H2)

The Inbus MST to NPL Convertor functions as follows:

- Receives

  Inbus Parity from the Inbus Parity Check (card A1H2).

  Inbus Bits 0 through 7 from the Inbus Generator (card A1H2).

- Converts the Inbus MST voltage levels to Dev Bus In NPL voltage levels.
- Sends Dev Bus In to the Dev Bus In NPL to MST Convertor (card A2F2) in the controller.

58 Attn/Sel Bit MST to NPL Convertor (Card A1K2)

The Attn/Sel Bit MST to NPL Convertor functions as follows:

- Receives the Attn/Sel Bit from the Attention/Select Bit Generator (card A1K2).
- Converts the Attn/Sel Bit MST voltage level to an NPL voltage level.
- Sends the Attn/Sel Bit NPL voltage level via the Attn/Sel Bus to the Attn/Sel Bus NPL to MST Convertor (card A2G2) in the controller.

59 Dev Bus Out NPL to MST Convertor (Card A1K2)

The Dev Bus Out NPL to MST Convertor functions as follows:

- Receives Dev Bus Out from the Bits Out to Dev Bus Out Convertor (card A2F2) in the controller.
- Converts Dev Bus Out NPL voltage levels to MST Outbus MST voltage levels.
- Sends MST Outbus to the following:

  Write Gate Control (card A1H2)

  Sense Operations Decode (card A1G2)

  Read*Write Control (card A1H2)

  Head Address Register (card A1G2)

  Difference Counter and Control (card A1G2)

  Inbus Generator (card A1H2)

  Cylinder Address Register (card A1G2)

  Target Register (card A1J4)

  Dev Bus Out Parity (card A1K2)

  Drive Operation Control (card A1K2)

  Drive Address Compare (card A1K2)

60 Dev Tag Bus NPL to MST Convertor (Card A1K2)

The Dev Tag Bus NPL to MST Convertor functions as follows:

- Receives Dev Tag Bus from the Dev Tag Bus MST to NPL Convertor (card A2L2) in the controller.
- Converts Dev Tag Bus NPL voltage levels to Tag Bus MST voltage levels.
- Sends Tag Bus to the following:

  Dev Tag Bus Parity (card A1K2)

  Tag Decode (card A1K2)

61 Access Control Amplifier (Card A1C4)

The Access Control Amplifier functions as follows:

- Receives

  Access Ctrl Bus from the Access Control (card A1E2).

  Gated Position Derived from the Gated Position Derivative Generator (card A1D2).

  −Position from the +/− Error Demodulator and Amplifier (card A1C2).

  V Ref from the Reference Voltage Generator (card A1C2).

  Current Sense from the HDA via the Power Amp and sends Current Sense via the Access Ctrl Bus to the Access Current Magnitude Detector (card A1D2).

- Generates Power Amp Drive and sends it to the HDA via the Power Amp.
- Generates the signals Move Forward and Move Reverse and sends them via the Access Ctrl Bus to the Access Current Magnitude Detector (card A1D2).
- Generates Rezero Fwd and sends it via the Access Ctrl Bus to the End of Acceleration Detector (card A1C4).
- Generates Rezero Rev and sends it via the Access Ctrl Bus to the Position Enable Generator (card A1C4).

62 Reference Voltage Generator (Card A1C2)

The Reference Voltage Generator functions as follows:

- Generates the reference voltages V Ref and 20 V.
- Sends V Ref to the following:

  Access Control Amplifier (card A1C4)

  Access Current Magnitude Detector (card A1D2).

- Sends 20 V to the following:

  Track Following Timer (card A1C4)

  On Track Detector (card A1C4)

63 +/− Error Demodulator and Amplifier (Card A1C2)

The +/− Error Demodulator and Amplifier functions as follows:

- Receives the Raw Servo Amplified signal from the Raw Servo Signal Amplifier (card A1C2).
- Demodulates the Raw Signal Amplified signal and obtains the signal + Position and the signal −Position.
- Amplifies + Position and − Position and sends them to the following:

  Track Following Timer (card A1C4)

  Track Crossing Detector (card A1D2)

  Allow Rezero Generator (card A1D2)

  Velocity Detector (card A1D2)

  Gated Position Derivative Generator (card A1D2)

  Access Current Magnitude Detector (card A1D2)

  On Track Detector (card A1C4)

- Sends −Position to the Access Control Amplifier (card A1C4).

64 Dev Tag Bus Parity (Card A1K2)

The Dev Tag Bus Parity functions as follows:

- Receives Tag Bus from the Dev Tag Bus NPL to MST Convertor (card A1K2).
- Checks the parity of the Tag Bus.
- Generates Tag Bus Parity Error when Tag Bus parity is odd.
- Sends Tag Bus Parity Error to the following:

  Interface Status Bits Generator (card A1K2)

  Drive Operations Control (card A1K2)

65 Tag Decoder (Card A1K2)

The Tag Decoder functions as follows:

- Receives Tag Bits 0 through 2 via the Tag Bus from the Dev Tag Bus NPL to MST Convertor (card A1K2).
- Decodes Tag Bus into the Tag Decodes.
- Sends the Tag Decodes to the following:

  Interface Status Bits Generator (card A1K2)

  Drive Operations Control (card A1K2)

  Drive Selected Generator (card A1K2)

FUNCTIONAL UNITS

DRIVE

66 Allow Rezero Generator (Card A1D2)

The Allow Rezero Generator functions as follows:

- Receives

  DC 7 via DC 0 through 7 from the Difference Counter and Control (card A1G2).

  Access Start via the Access Ctrl Bus from the Access Control (card A1E2).

  Forward via the Access Ctrl Bus from the Access Control (card A1E2).

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

- Generates Allow Rezero.
- Sends Allow Rezero via the Drive Op Ctrl Bus to the Access Control (card A1E2).

67 Velocity Detector (Card A1D2)

The Velocity Detector functions as follows:

- Receives

  Access Mode via the Access Ctrl Bus from the Access Control (card A1E2).

  DC Equals 1 and also Diff Greater than 127 via the Drive Op Ctrl Bus from the Difference Counter and Control (card A1G2).

  + Position and also − Position from the +/− Error Demodulator and Control (card A1C2).

  Velocity Enable from the Velocity Enable Generator (card A1C4).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

- Generates the Velocity signal.
- Sends Velocity to the following:

  End of Acceleration Detector (card A1C4)

  Gated Position Derivative Generator (card A1D2)

  Velocity Intensity Detector (card A1C4)

  End of Deceleration Detector (card A1C4)

68 Gated Position Derivative Generator (Card A1D2)

The Gated Position Derivative Generator functions as follows:

- Receives

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

  DC equals 1 via the Drive Op Ctrl Bus from the Difference Counter and Control (card A1G2).

  Move Forward via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  Current Magnitude from the Access Current Magnitude Detector (card A1D2).

  The Velocity signal from the Velocity Detector (card A1D2).

- Generates Gated Position Derived.
- Sends Gated Position Derived to the Access Control Amplifier (card A1C4).

69 Access Current Magnitude Detector (Card A1D2)

The Access Current Magnitude Detector functions as follows:

- Receives

  Velocity Enable from the Velocity Enable Generator (card A1C4).

  V Ref from the Reference Voltage Generator (card A1C2).

  Move Forward and also Move Reverse via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  Current Sense via the Access Ctrl Bus from the Access Control Amplifier (card A1C4).

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

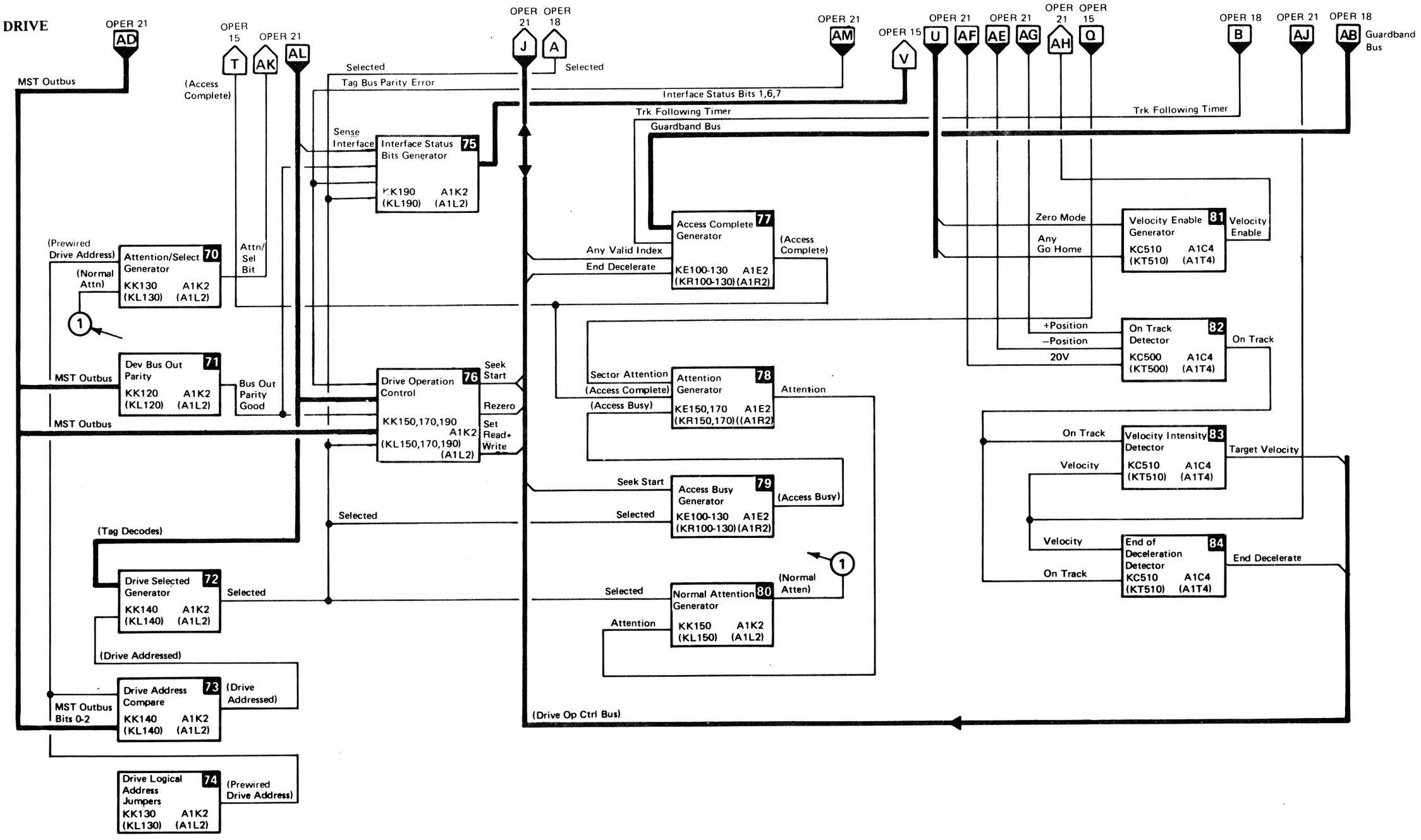
- Generates Current Magnitude
- Sends Current Magnitude to the following:

  Gated Position Derivative Generator (card A1D4)

  Velocity Detector (card A1D2)

  End of Acceleration Detector (card A1C4)

DRIVE



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FUNCTIONAL UNITS

DRIVE

70 Attention/Select Bit Generator (Card A1K2)

The Attention/Select Bit Generator functions as follows:

- Receives

  Prewired Drive Address from the Drive Logical Address Jumpers (card A1K2)

  Normal Attn from the Normal Attention Generator (card A1K2).

- Generates Attn/Sel Bit.
- Sends Attn/Sel Bit to the Attn/Sel Bit MST to NPL Convertor (card A1K2).

71 Dev Bus Out Parity (Card A1K2)

The Dev Bus Out Parity functions as follows:

- Receives MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).
- Checks the parity of the MST Outbus.
- Generates Bus Out Parity Good when parity is odd.
- Sends Bus Out Parity Good to the following:

  Drive Operations Control (card A1K2)

  Interface Status Bits Generator (card A1K2)

72 Drive Selected Generator (Card A1K2)

The Drive Selected Generator functions as follows:

- Receives

  Tag Decodes from the Tag Decoder (card A1K2)

  Drive Addressed from the Drive Address Compare (card A1K2).

- Generates Selected.
- Sends Selected to the following:

  Normal Attention Generator (card A1K2)

  Access Busy Generator (card A1E2)

  Drive Operation Control (card A1K2)

  Interface Status Bits Generator (card A1K2)

  Inbus Generator (card A1H2)

  Inhibit HDA Sequence Generator (card A1F2)

73 Drive Address Compare (Card A1K2)

The Drive Address Compare functions as follows:

- Receives

  Prewired Drive Address from the Drive Logical Address Jumpers (card A1K2)

  MST Outbus Bits 0 through 2.

- Generates Drive Addressed when the address contained in the MST Outbus bits 0 through 2 equals the prewired drive address.
- Sends Drive Addressed to the Drive Selected Generator (card A1K2).

74 Drive Logical Address Jumpers (Card A1K2)

The Drive Logical Address Jumpers block functions as follows:

- Generates Prewired Drive Address.
- Sends Prewired Drive Address to the following:

  Drive Address Compare (card A1K2)

  Attention/Select Generator (card A1K2)

75 Interface Status Bits Generator (Card A1K2)

The Interface Status Bits Generator functions as follows:

- Receives

  Sense Interface via the Tag Decodes Bus from the Tag Decoder (card A1K2).

  Bus Out Parity Good from the Dev Bus Out Parity (card A1K2).

  Tag Bus Parity Error from the Dev Tag Bus Parity (card A1K2).

  Selected from the Drive Selected Generator (card A1K2).

- Generates Interface Status Bits 1, 6, 7.
- Sends Interface Status Bits 1, 6, 7 to the MST Inbus Generator (card A1H2).

76 Drive Operation Control (Card A1K2)

The Drive Operation Control functions as follows:

- Receives

  Tag Bus Parity Error from the Dev Tag Bus Parity (card A1K2).

  Tag Decodes from the Tag Decoder (card A1K2).

  Bus Out Parity Good from the Dev Bus Out Parity (card A1K2).

  MST Outbus from the Dev Bus Out NPL to MST Convertor (card A1K2).

  Selected from the Drive Selected Generated (card A1K2).

- Generates Seek Start and sends it via the Drive Op Ctrl Bus to the following:

  Access Busy Generator (card A1E2)

  Access Control (card A1E2)

- Generates Rezero and sends it via the Drive Op Ctrl Bus to the Access Control (card A1E2).
- Generates Set Read*Write and sends it via the Drive Op Ctrl Bus to the following:

  Read*Write Control (card A1H2)

  Inbus Generator (card A1H2)

77 Access Complete Generator (Card A1E2)

The Access Complete Generator functions as follows:

- Receives

  Guardband Bus from the Guardband Pattern Generator (card A1D4).

  Trk Following Timer from the Track Following Timer (card A1C4).

  Any Valid Index via the Drive Op Ctrl Bus from the Valid Index Generator (card A1D4).

  End Decelerate via the Drive Op Ctrl Bus from the End of Deceleration Detector (card A1C4).

- Generates Access Complete.
- Sends Access Complete to the following:

  Attention Generator (card A1E2)

  HDA Status Bits Generator (card A1F2)

78 Attention Generator (Card A1E2)

The Attention Generator functions as follows:

- Receives

  Sector Attention from the Sector Counter (card A1J4).

  Access Complete from the Access Complete Generator (card A1E2).

  Access Busy from the Access Busy Generator (card A1E2).

- Generates the Attention signal.
- Sends Attention to the Normal Attention Generator (card A1K2).

79 Access Busy Generator (Card A1E2)

The Access Busy Generator functions as follows:

- Receives

  Seek Start via the Drive Op Ctrl Bus from the Drive Operation Control (card A1K2).

  The signal, Selected, from the Drive Selected Generator (card A1K2).

- Generates Access Busy.
- Sends Access Busy to the Attention Generator (card A1E2).

80 Normal Attention Generator (Card A1K2)

The Normal Attention Generator functions as follows:

- Receives

  Selected from the Drive Selected Generator (card A1K2).

  Attention from the Attention Generator (card A1E2).

- Generates Normal Attn.
- Sends Normal Attn to the Attention/Select Bit Generator (card A1K2).

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FUNCTIONAL UNITS

DRIVE

83 Velocity Enable Generator (Card A1C4)

The Velocity Enable Generator functions as follows:

- Receives Zero Mode and also Any Go Home via the Access Ctrl Bus from the Access Control (card A1E2).
- Generates Velocity Enable.
- Sends Velocity Enable to the following:

  Access Current Magnitude Detector (card A1D2)

  Velocity Detector (card A1D2)

82 On Track Detector (Card A1C4)

The On Track Detector functions as follows:

- Receives

  + Position and also − Position from the +/− Error Demodulator and Amplifier (card A1C2).

  20 V from the Reference Voltage Generator (card A1C2).

- Detects that the carriage is on track and then generates the On Track signal.
- Sends On Track to the following:

  Velocity Intensity Generator (card A1C4)

  End of Deceleration Detector (card A1C4)

85 Velocity Intensity Detector (Card A1C4)

The Velocity Intensity Detector functions as follows:

- Receives

  On Track from the On Track Detector (card A1C4).

  The Velocity signal from the Velocity Detector (card A1D2).

- Detects the velocity of the carriage and generates the Target Velocity signal.
- Sends the Target Velocity signal via the Drive Op Ctrl Bus to the Access Control (card A1E2).

84 End of Deceleration Detector (Card A1C4)

The End of Deceleration Detector functions as follows:

- Receives

  The Velocity signal from the Velocity Detector (card A1D2).

  On Track from the On Track Detector (card A1C4).

- Detects the end of deceleration of the carriage and then generates End Decelerate.
- Sends End Decelerate to the Access Control (card A1E2).

HEAD/DISK ASSEMBLY (HDA) — PHYSICAL DESCRIPTION

This page describes only the physical characteristics of the Head/Disk Assembly (HDA). See OPER 31 for the logical description. (The logical description shows the physical location of the logical cylinders and logical heads on the HDA.)

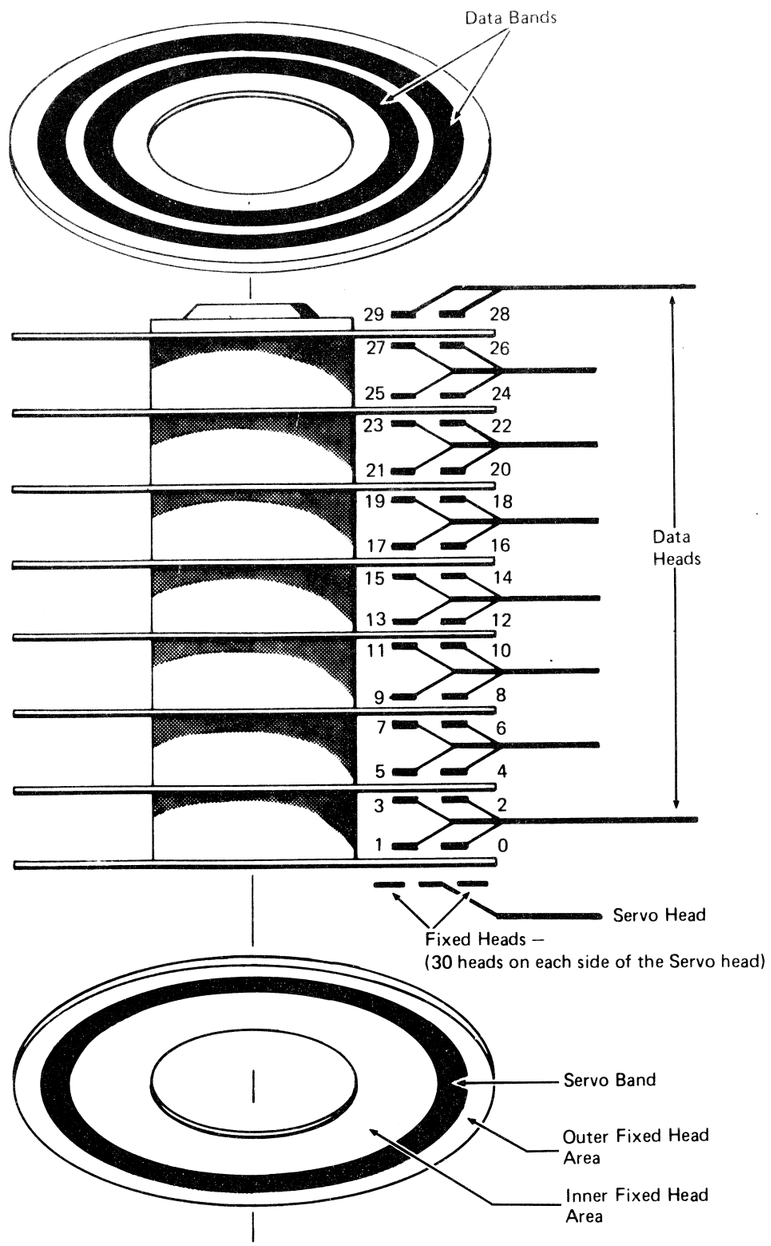
INTRODUCTION

The Head/Disk Assembly (HDA) contains 16 recording surfaces (8 disks). Of these 16 surfaces, the upper 15 are data surfaces; the under side of the bottom disk is the servo surface.

The HDA also contains a movable carriage that attaches outside the HDA to a voice coil motor. The carriage holds 30 movable Read/Write heads and one servo head.

The 30 movable Read/Write heads are located on the 15 data surfaces, two heads for each surface. The servo head is located on the servo surface.

If the 3344 is a Model B2F (with fixed heads), there are 60 additional Read/Write heads on the servo surface. These heads are not attached to the carriage, but are fixed in place outside of the moving range of the servo head with 30 heads on either side of the servo head.



DATA SURFACE

Each data surface contains two data bands. The data bands are divided into tracks numbered from 0 to 560, counting from the outside track to the inside track.

Each data band has its own movable Read/Write head that can read or write information on any of the tracks.

Home addresses are prerecorded on all data tracks for track identification, seek verification, and skip displacement information.

SERVO SURFACE

The servo surface has one servo head and one band of servo data tracks. The servo tracks are prerecorded for seeking, track following, data clocking, Index point signal generation, and rotational position signal generation. If the 3344 is a Model B2F (with fixed heads), the servo surface is also used for reading or writing data by the fixed heads. The fixed-head tracks occupy the areas on both sides of the servo band.

HEAD POSITIONING

The data heads and the servo head are fixed in position on the carriage. The servo head does all of the track seeking and track following; when the servo head is on track, every data head is on track.

Note: *More details of Servo (Access) operation are described on OPER 116 through 142.*

HEAD/DISK ASSEMBLY (HDA) — LOGICAL DESCRIPTION

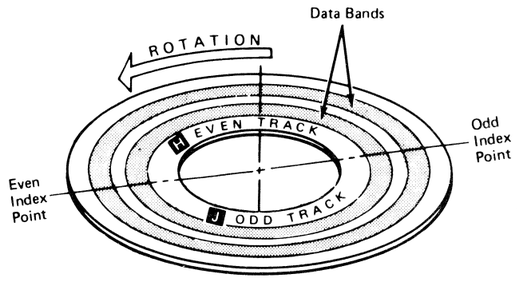
This page describes the logical characteristics of the 3344 HDA. By understanding this page, it is possible to determine the location of any cylinder and/or head address on the HDA.

INDEX POINTS

The 3344 HDA, like the 3340 Data Module, has two Index points on every data surface: the Even Index point and the Odd Index point. See Figure 1.

Each Read/Write head records two logical tracks on a single revolution of the disk: an Even track after sensing the Even Index point and an Odd track after sensing the Odd Index point.

Figure 1.



LOGICAL CYLINDER LOCATIONS

Refer to figure 2.

The HDA is divided into five logical cylinder groups, 0 to 4.

- Logical cylinder group 0 occupies the bottom three data surfaces of the HDA.
- Logical cylinder group 1 occupies the next three data surfaces.
- Each of the other logical cylinder groups also occupy three data surfaces, as shown in Figure 2.

Since there are five logical cylinder groups, it follows that there are five (5) logical cylinders located at each Access position.

Refer to Figure 3 on OPER 32 for the Logical Cylinder/Volume relationship.

When the Read/Write heads are at Access position 0:

- The R/W heads over the disks in logical cylinder group 0 are at logical cylinder address 0.
- The R/W heads over the disks in logical cylinder group 1 are at logical cylinder address 1.
- The R/W heads over the disks in logical cylinder groups 2,3, and 4 are at logical cylinder addresses 2, 3, and 4, respectively.

When the Read/Write heads are at Access position 1:

- The R/W heads over the disks in logical cylinder group 0 are at logical cylinder address 5.
- The R/W heads over the disks in logical cylinder group 1 are at logical cylinder address 6.
- The R/W heads over the disks in logical cylinder groups 2, 3, and 4 are at logical cylinder addresses 7, 8, and 9, respectively.

To find the physical location of any cylinder address, divide the logical cylinder address by 5.

Quotient = Physical cylinder number (track)*
Remainder = Logical cylinder group

Example:

$$5\overline{)117}\quad \begin{array}{l} 23 \leftarrow \text{Quotient: Physical cylinder number (track)} \\ \text{Logical cylinder address} \rightarrow \\ 10 \\ \hline 17 \\ 15 \\ \hline 2 \leftarrow \text{Remainder: Logical cylinder group} \end{array}$$

*Refer to Logical Device Address on OPER 32. This applies to logical 3340 device A.

For Device: B add 140
C add 280
D add 420

LOGICAL HEAD LOCATIONS

Refer to Figure 2.

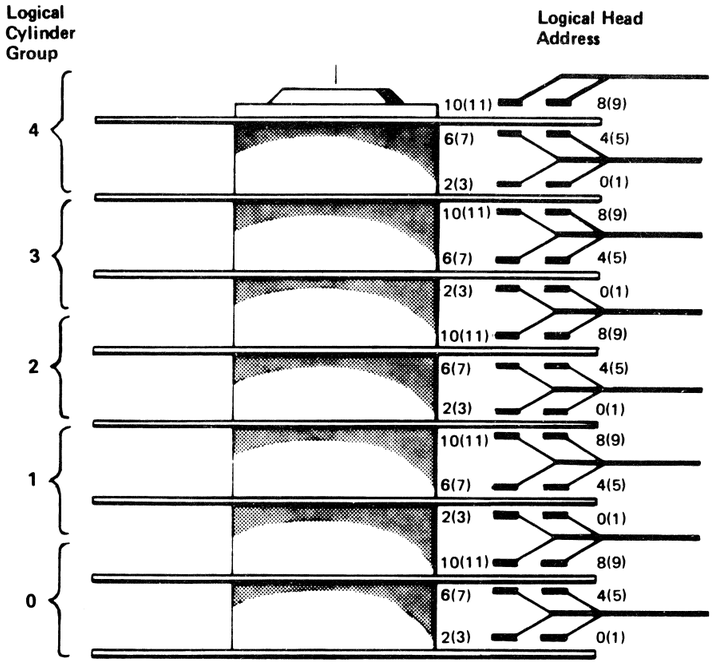
Within each logical cylinder group, there are 11 logical Read/Write head addresses. The logical head numbers for each R/W head address are shown in Figure 2.

Each head has two numbers next to it, – an even number and an odd number, such as 6(7).

The even number, 6 in this example, is the logical address of the R/W head when it is over an Even track (as discussed in an earlier paragraph under Index Points). The odd number (7), is the logical address of the R/W head when it is over an odd track.

The Logical Description of the HDA is continued on OPER 32.

Figure 2.

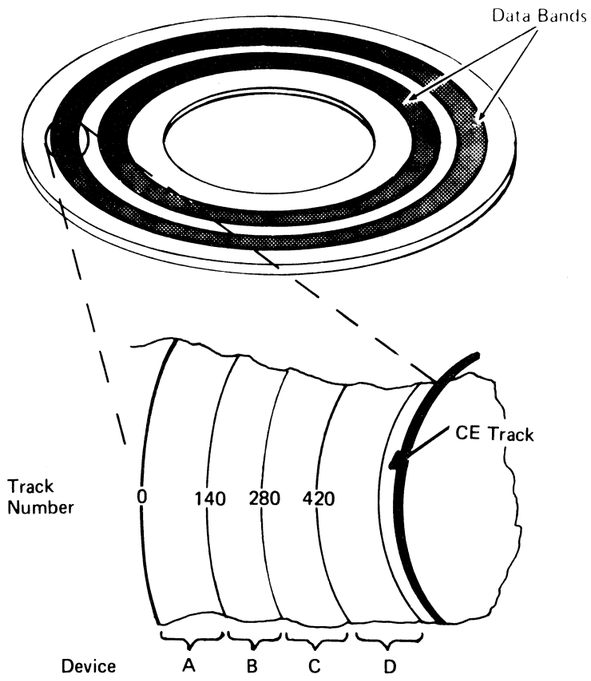


HEAD/DISK ASSEMBLY (HDA) — LOGICAL DESCRIPTION

LOGICAL 3340 VOLUMES

The 3344 HDA is divided into four logical volumes. Each logical volume has a unique logical address, as if each volume were one 3340 volume (or one data module).

Each data band on each data surface of the HDA is divided into four equal parts to make up logical devices A, B, C, and D.



Device A begins at track 0
Device B begins at track 140
Device C begins at track 280
Device D begins at track 420

SUMMARY

Figure 3 shows the logical cylinder addresses and how they relate to the logical volume.

Each logical volume contains:

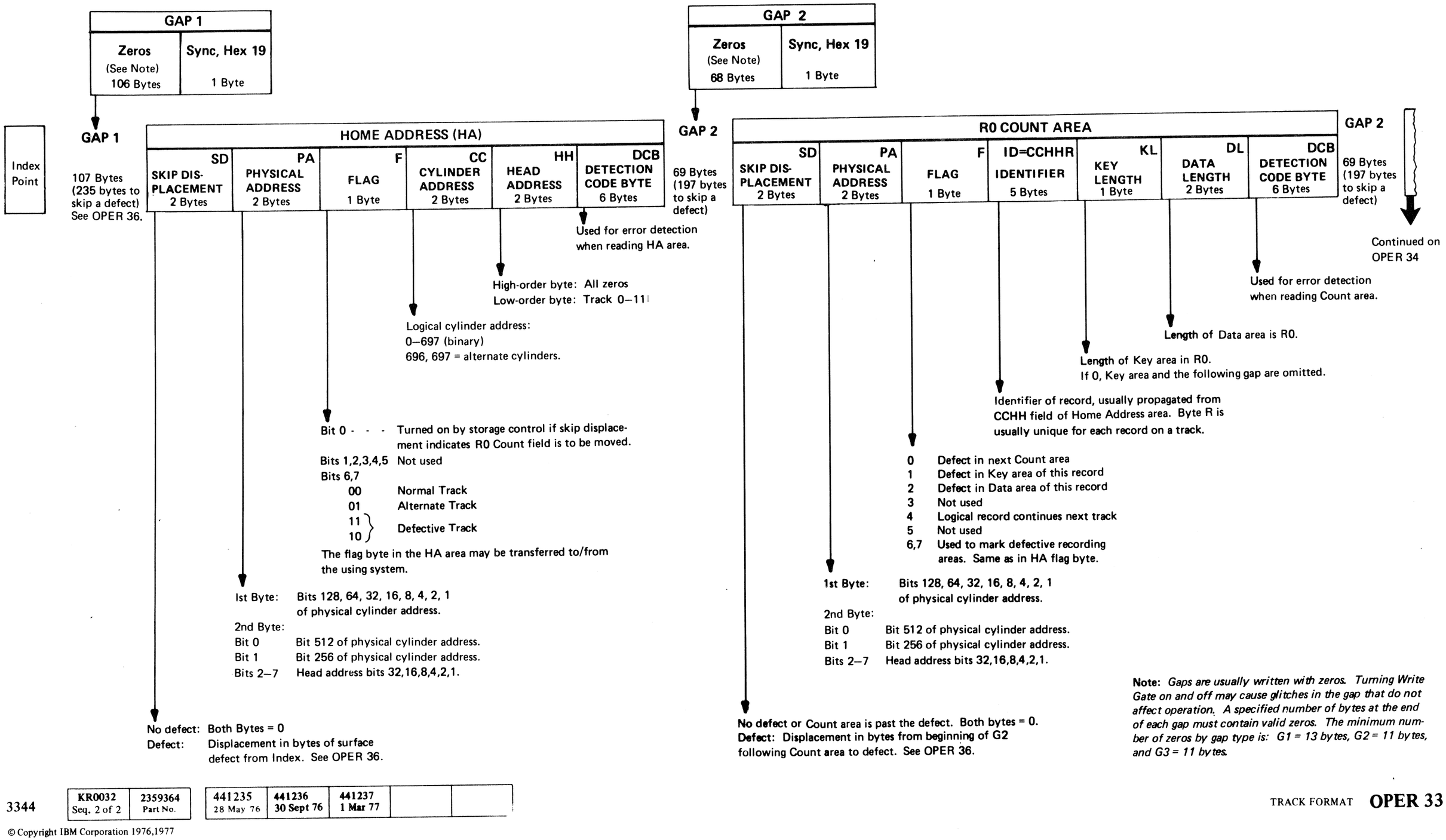
695 Data cylinders
2 Alternate cylinders (696 and 697)

The CE cylinder is located at Access position 560.

For System/3 logical volumes, see the System/3 3340/3344 TMD manual for the logical addresses for each logical volume.

Figure 3. Logical Cylinder/Volume (Device)

Logical Cylinder Group	Device A							Device B							Device C							Device D							CE Cylinder
4	4	9	14		689	694		4	9	14			694		4					694		4	9			694		2804
3	3	8	13		688	693		3	8	13			693		3					693		3	8			693		2803
2	2	7	12		687	692	697	2	7	12			692	697	2	7				692	697	2	7			692	697	2802
1	1	6	11		686	691	696	1	6	11			691	696	1	6				691	696	1	6			691	696	2801
0	0	5	10		685	690	695	0	5	10			690	695	0	5				690	695	0	5			690	695	2800
Access Position →	0	1	2		137	138	139	140	141	142			278	279	280	281				418	419	420	421			558	559	560



Note: *Gaps are usually written with zeros. Turning Write Gate on and off may cause glitches in the gap that do not affect operation. A specified number of bytes at the end of each gap must contain valid zeros. The minimum number of zeros by gap type is: G1 = 13 bytes, G2 = 11 bytes, and G3 = 11 bytes.*

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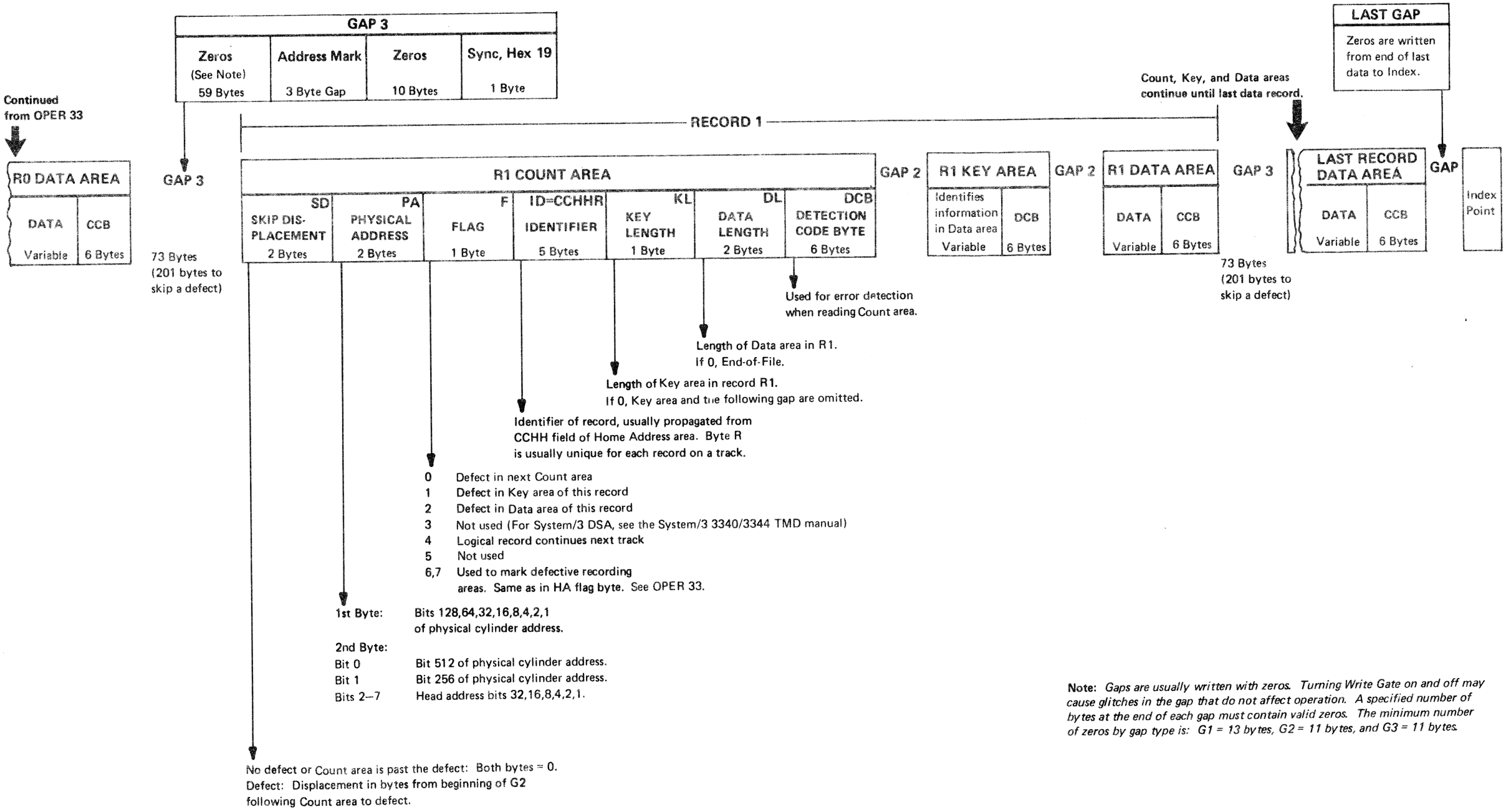
TRACK FORMAT



Note: *Gaps are usually written with zeros. Turning Write Gate on and off may cause glitches in the gap that do not affect operation. A specified number of bytes at the end of each gap must contain valid zeros. The minimum number of zeros by gap type is: G1 = 13 bytes, G2 = 11 bytes, and G3 = 11 bytes.*

SURFACE DEFECT SKIPPING

INTRODUCTION

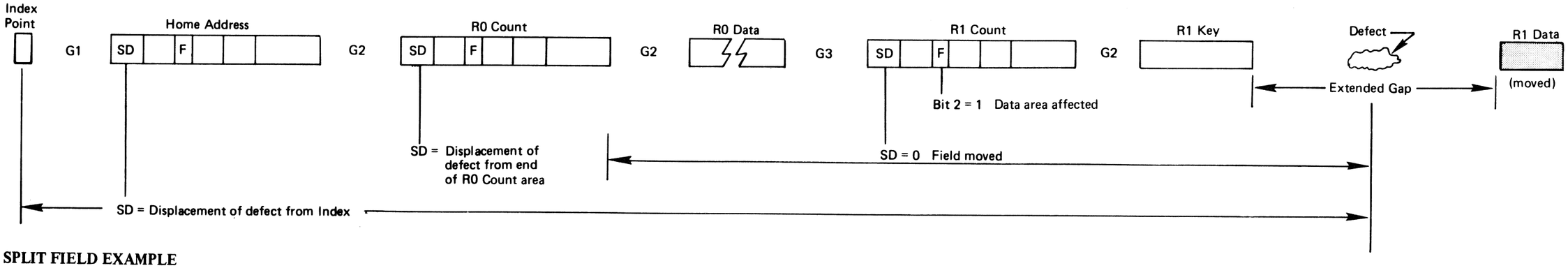
When writing a track containing a defect, a special gap (128 bytes) is written over the defective area so no data can ever be recorded there.

If a defect is too large or if there is more than one defect on a track, the track is flagged as defective and an alternate assigned.

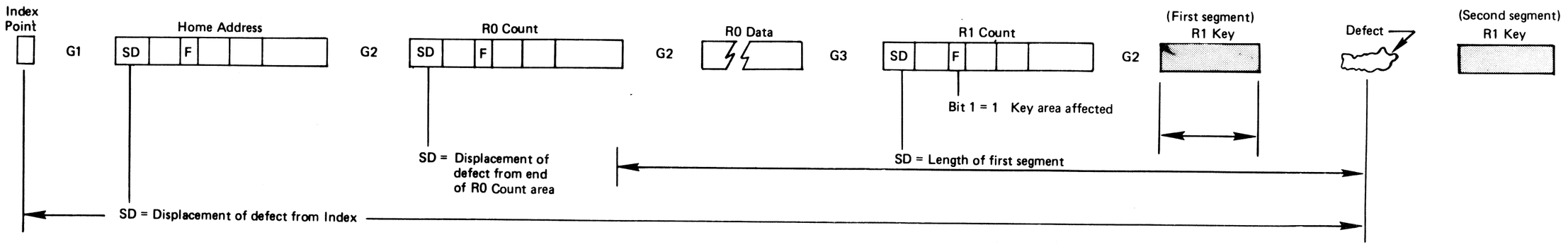
When formatting the tracks and a defect is detected, it is skipped by either:

- Moving a field and extending the preceding gap when the defect fails near or within the gap.
- Splitting the field into two parts positioned on each side of the special gap that was written over the defective area.

EXTENDED GAP EXAMPLE



SPLIT FIELD EXAMPLE



Before an HDA is shipped, a thorough surface analysis-initialization is performed. Home Address and a standard R0 (8-byte data length) are written. If a surface defect is found, its displacement from the Index Point is written in the HA area (SD = distance in bytes from Index Point to center of defect).

When the storage control becomes oriented on a Count area or Home Address during a Write operation, it stores the SD and Flag bytes and, therefore, knows the location of any defect. When the Count area SD and Flag bytes are written during a WRCKD, the key length and data length have not been transferred from the system. The SD and Flag bytes for the Count area are then computed under the assumption that no defect exists. When the gap following the Count area is being written, the key and data length, transferred from the system, and the SD bytes are analyzed to see if the record extends to a track defect. If not, the assumption made while writing the Count area was correct and the SD value for the next Count area is computed.

If the record does extend to a defect, the Count area is not valid and must be rewritten with correct SD and Flag bytes. The necessary reorientation is accomplished by counting over almost a full track worth of bytes, padding to Index and clocking the remainder until a full revolution is completed. While this is happening, the record is being scanned and analyzed to determine whether it must be split or moved. Also, the system, after initially transferring the Count area, is ready to begin transferring the Key (data) area. The Count area is now rewritten from storage control with newly computed SD and Flag bytes. The remainder of the record is then written, splitting or moving fields as appropriate.

Reading a record that has a surface defect is automatically controlled by microcode and no time is lost by seeking alternate tracks or from rotational delay.

HOW TO DETERMINE SKIP DISPLACEMENT

In normal operation, the Skip Displacement field in the Home Address is transparent to the user at the channel level. However, the HA SD field can be determined by executing the following CCW chain via the channel:

Read Home Address

Sense I/O

If there is no outstanding Device End or Unit Check following the execution of this chain, the contents of the HA SD field appear in Sense Bytes 22 and 23.

CONTROL INTERFACE

This page identifies and defines each part of the control interface. (The basic timing sequence of the interface is given on OPER 95. The Tag and Bus information for each Tag decode is summarized in chart form on OPER 98 through 101 and fully described on OPER 102 through 106.)

- The control interface is the common connection between storage control and all attached controllers.
- The controllers are attached in parallel to one set of signal lines, allowing simultaneous addressing or polling by the storage control.
- A controller is connected to the interface until all information is transferred and the storage control signals it to disconnect.
- Only one controller is logically connected to the storage control at a time.
- Signals from different controllers are ORed together to be transmitted to the storage control on common lines.

CONTROL TAG BUS OUT

Tag Bus Out Bits

Tag Bus Out bits 0, 4 through 7, and P send an instruction (control information) to the controller when Tag Gate is active. The instruction identifies the operation to be performed.

All Tag Bus data must be valid at least 100 ns before Tag Gate becomes active, and must remain valid at least 150 ns after Tag Gate becomes inactive.

Tag Gate

Tag Gate indicates the presence of an instruction on Tag Bus. Tag Gate remains active until acknowledged by the controller with Tag Valid.

An operation must be decoded in the controller within 100 ns after Tag Gate becomes active.

Select Hold

Select Hold becomes active during any Select Tag. Select Hold remains active to maintain selection of a drive until the end signal of the last operation to be performed on the drive is received and acknowledged.

Sync Out

Sync Out checks the data count during controller data transfers and orientation clocking.

Sync Out is not dc-interlocked with any inbound line, but it must have a minimum pulse width of 60 ns.

Recycle

Recycle forces the Gap counter (in Modulo-16 mode) to continue counting data bytes by causing the Gap counter to count to 15, step to 0, and count to 15 and continue in this manner until all bytes of data have been transferred. Recycle becomes inactive during transmission of the last 16 bytes of data to end the data transfer sequence at count 15.

Response

Response acknowledges either a Normal End or Check End condition. Response is not dc-interlocked with any line, but it must have a minimum pulse width of 60 ns.

CONTROL BUS OUT

Control Bus Out transfers control or address information to the controller as a tag modifier when Tag Gate is active. Bus Out must be valid at least 100 ns before Tag Gate becomes active, and must remain valid at least 150 ns after Tag Gate becomes inactive.

Control Bus Out transfers data to the controller for the drive when Sync Out is active. All Bus Out data must be valid at least 100 ns before Sync Out becomes active, and must remain valid for at least 100 ns after Sync Out becomes inactive.

CONTROL TAG BUS IN

Sync In

Sync In validates and times Bus In during data transfers from the controller to storage control. Sync In becomes active after Bus In is valid.

Bus In remains valid until after Sync In becomes inactive. During data transfers from the storage control to controller, Sync In provides timing for the data being transferred.

Select Active

Select Active becomes active as a result of the selection sequence. It remains active to indicate proper selection as long as Select Hold is active and selection of the drive is correctly maintained by the controller.

Tag Valid

Tag Valid indicates that the controller or drive has validated and accepted a tag instruction sent from the storage control. When required, Tag Valid indicates to storage control that Bus In information is valid.

Normal End

Normal End indicates that the normal ending of an operation occurred with the xepcted results. Normal End is active with or before Tag Valid for Immediate operations. For Read, Write, Set Read/Write, and ECC Control operations (Extended operations), Tag Gate becomes active and the operation is complete before Normal End becomes active.

Normal End becomes active at the successful completion of the operation. Information on Bus In is valid at the start of Normal End.

When Normal End is generated with Tag Gate, it remains active until Tag Gate falls; otherwise it remains active until Response becomes active.

Check End

Check End indicates that an abnormal ending condition exists. The abnormal condition is presented on Bus In with proper parity during the time Check End is active.

For Read or Write operations, Check End is active and Bus In maintains proper parity until the storage control acknowledges the receipt of the status information by activating the Response line.

Check End is not activated on an Immediate operation.

Alert Lines

Selected Alert lines indicate that certain special events have occurred in the selected drive or controller. They are active only if Select Active is present.

Unselected Alert indicates that the execution of an appropriate polling sequence is required.

SELECTED ALERT LINE (Alert 1): Indicates an unusual condition (Equipment Check) in the selected controller or drive.

SELECTED ALERT LINE 2 (Index Alert): Indicates the detection of Index or an ECC correctable pattern.

UNSELECTED ALERT LINE 1 (CE Alert Execute): Indicates that a CE Panel Execute switch was operated, and that the Data Entry switches were read by the storage control.

If more than one controller is on the interface, the storage control must poll to determine which controller activated the Alert.

CONTROL BUS IN

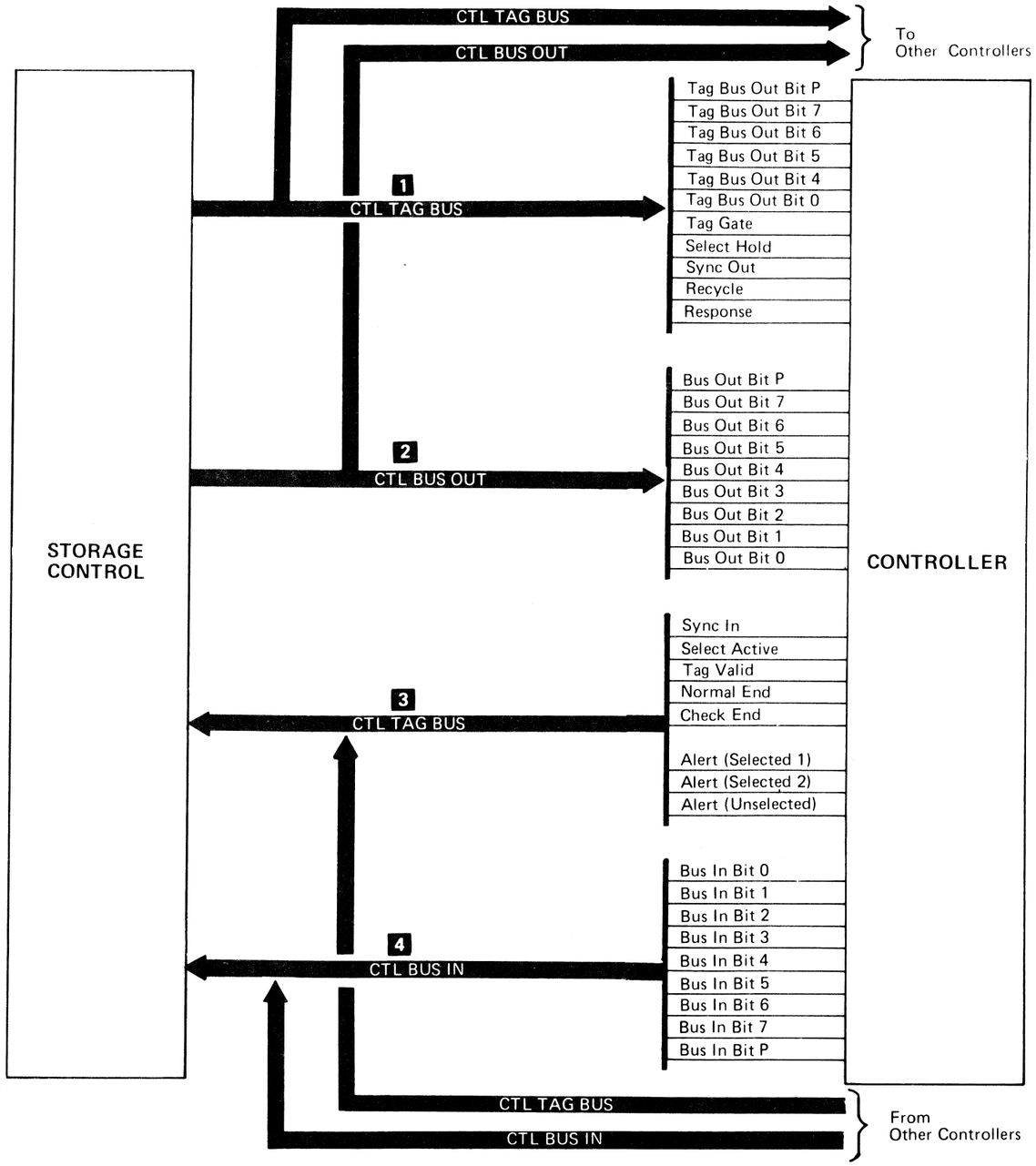
Control Bus In transmits data from the drive to storage control when Sync In is active. Certain commands cause status, error, or information originating in the drive to be transmitted on Bus In while Tag Valid is active.

If an abnormal condition occurs during a Read, Write, or ECC Control operation (Extended operations), Check End is active and the error information relating to the abnormal condition is presented on Bus In.

During read data transfers, Bus In is active at least 125 ns before Sync In and remains active for at least 125 ns after Sync In becomes inactive.

During information transfers, Bus In is active with or before the end tag and is valid until the tag ends.

CONTROL INTERFACE



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DEVICE INTERFACE

This page defines the device interface. (The Tag and Bus information for each Device Tag decode is summarized in chart form on OPER 100 and 101. The Tag decodes are fully described on OPER 104 through 106).

- The device interface is the common connection between all drives and the controller.
- The interface can accommodate up to eight drives.
- All signals from the controller are received by all drives.
- Like signals from different drives are ORed together on a common line to the controller.
- Read/Write data and PLO reference pulses are carried on two balanced, bi-directional cables.

DEVICE BUS OUT

Device Bus Out transfers operational information from the controller to the drive. The meaning of the information is determined by the Tag Bus.

Parity is checked at the drive for all functions except Read/Write.

DEVICE TAG BUS

Device Tag Bus Bits 0, 1, 2, and Parity

The following Device Tag Bus lines are coded to define the data presented on Bus Out:

Code	Tag
000	Select
001	Sense Interface
010	Diagnostic Set
011	Set HAR
100	Set Difference (count)
101	Set Target
110	Set Cylinder (address)
111	Control

Tag Gate

The Tag Gate signal is sent to the drives to gate the Tag Bus and Bus Out. It is raised after the data appears on the bus and an appropriate delay has elapsed (see OPER 95).

Select Hold

Select Hold is used to maintain selection. It must be raised before or during Tag Gate and stay up as long as communication is necessary with the selected drive.

READ/WRITE DATA

The Read/Write data cable carries Read or Write data from the controller to the selected drive when writing, and from the selected drive to the controller when reading.

PLO PULSES

PLO reference pulses, necessary for write data clocking, are transmitted from the selected drive to the controller via the PLO cable when Select Hold is up.

DEVICE BUS IN

Device Bus In carries status and sense information from the selected drive to the controller. As soon as a drive is selected, machine status is placed on Device Bus In. Status stays on the bus until one of the following occurs:

- Select Hold falls.
- A Sense or a Read/Write function control tag is raised.
- A Diagnostic Set or a Sense Interface tag is raised.

ATTENTION/SELECT RESPONSE BUS

This bus transmits the unique 1-bit physical drive address to the controller when the drive has an Attention signal to present or when that drive is selected.

Attention is generated by:

- HDA Attention.
- Seek Complete.
- Sector Compare.
- Search Sector.

If a drive is in CE Mode, Attention appears on Bus Bit S (service drive position).

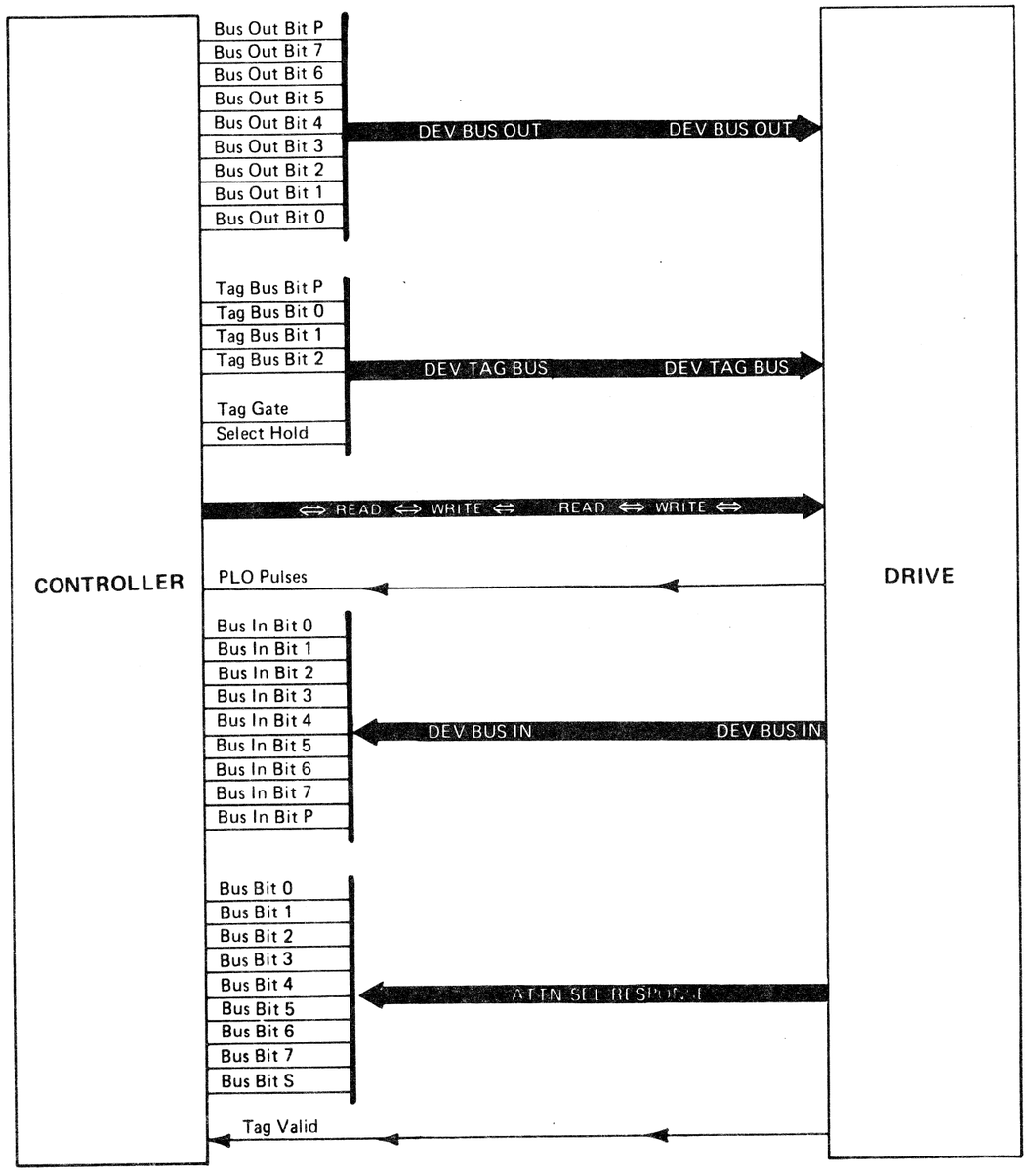
The Select Response signal represents the physical address of the drive that has been selected. Only one bit should appear on the bus when a drive is selected:

Bus Bit	Unique Physical Drive Address
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
S	Service Drive

TAG VALID

Tag Valid is sent from the selected drive to indicate that Device Bus Out and Tag Bus were received with correct parity. Device Tag Valid forces Tag Valid and Normal End in the controller.

DEVICE INTERFACE



CONTROL/DEVICE INTERFACE TIMING

There are three types of interface operation:

- Immediate Operation
- Extended Operation
- Select Operation

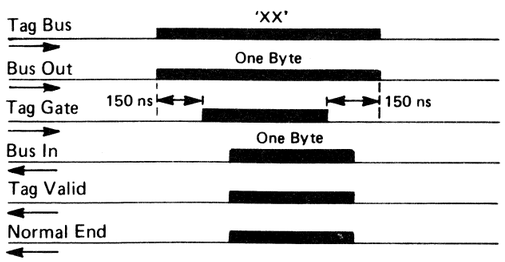
IMMEDIATE OPERATION

An Immediate operation transfers a single control instruction to the controller over the Control Interface and a single byte of information to or from the controller.

The appropriate tag is placed on the Ctl Tag Bus. At the same time, a single byte of data, either an instruction modifier or a byte of information, may be placed on the Ctl Bus Out. Tag Gate is raised after allowing for the 150 ns de-skewing.

The controller responds with Tag Valid, forcing Normal End. Data sent by the controller is placed on Ctl Bus In along with Normal End. The storage control must provide for any de-skewing for the interface. When Normal End is returned, data on Bus In is the expected response from the controller. Tag Gate drops when Tag Valid and Normal End are recognized by the storage control. The controller resets Tag Valid and Normal End when Tag Gate becomes inactive. The storage control cannot activate Tag Gate again until Tag Valid becomes inactive.

Check End is not presented on Immediate operations.



EXTENDED OPERATION

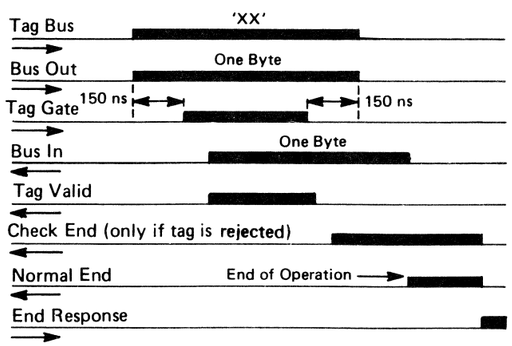
An Extended operation starts a sequence of events in the controller that requires extended time or many transfers across the Control Interface and Device Interface. The Extended operations are Read, Write, Set Read/Write, and ECC Control. The appropriate tag is placed on the Ctl Tag Bus. Simultaneously, a single byte of data or modifier information is placed on Ctl Bus Out. Tag Gate starts after the 150 ns de-skewing interval.

The controller responds with Tag Valid, indicating acceptance of the tag, causing the storage control to reset Tag Gate.

If the operation cannot be performed because of an abnormal condition, such as Command Overrun, Check End is indicated after Tag Gate becomes inactive. Ctl Bus In indicates the check condition.

If the operation can be performed, Normal End is activated at the completion of the operation.

Normal End or Check End remains active until End Response is returned to the controller to acknowledge either end condition.



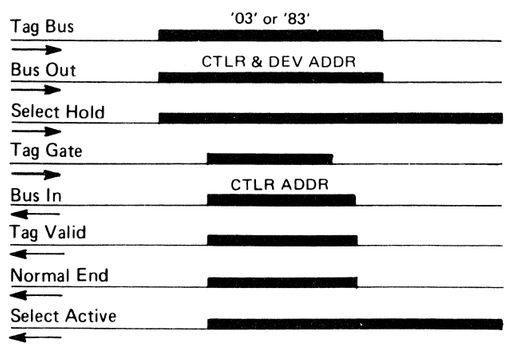
SELECT OPERATION

A Select Operation connects the storage control to a specified controller or drive.

The appropriate select tag is placed on the Ctl Tag Bus. Modifiers and address information are placed on the Ctl Bus Out. Assuming that the tag and bus information is correct, Select Hold and Tag Gate become active.

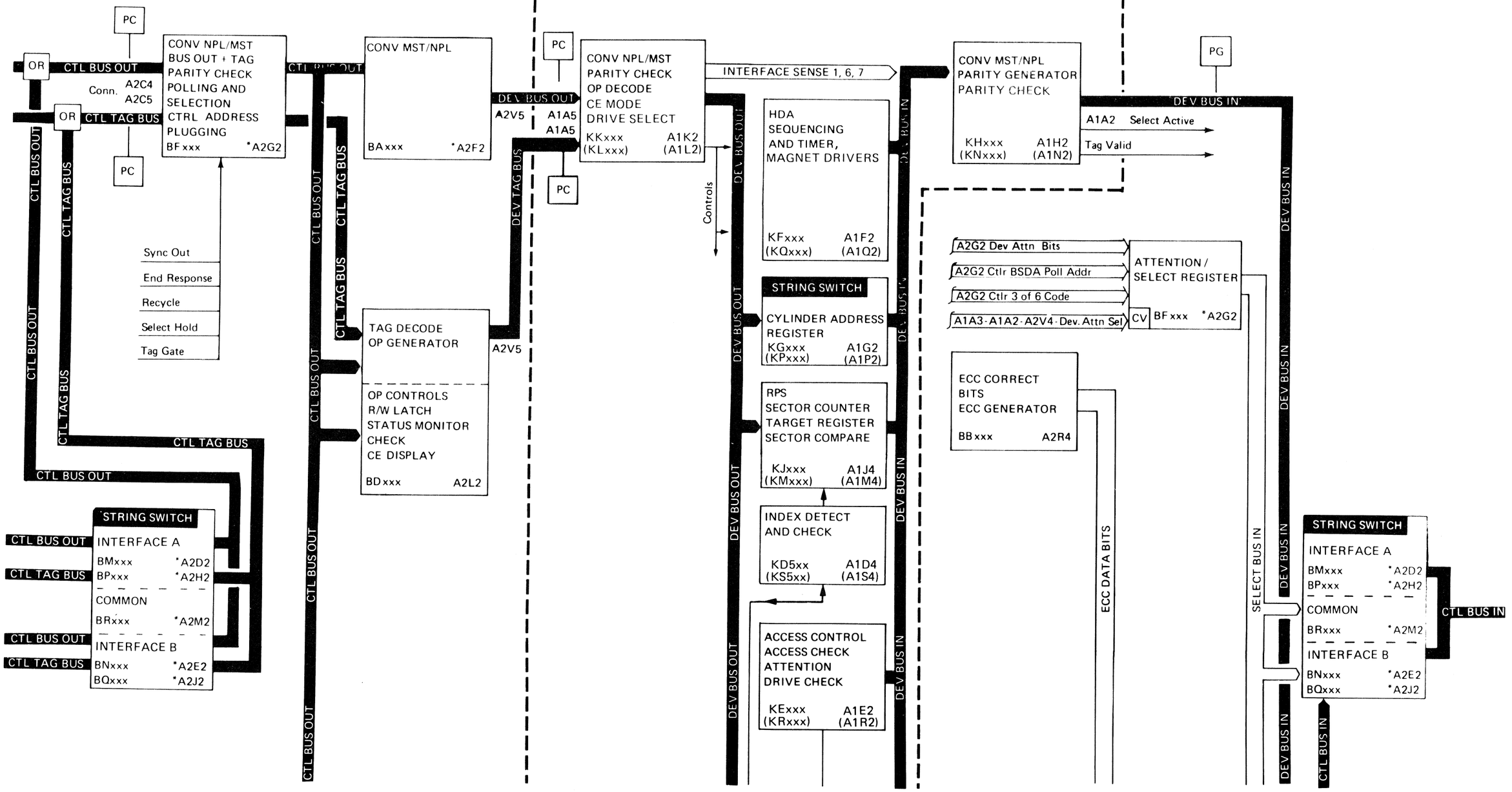
When selection has been completed, the controller responds with Tag Valid, Select Active and Normal End. When these tags are acknowledged by the storage control, Tag Gate becomes inactive. While Tag Valid is present, Ctl Bus In returns the address of the selected controller. The address contains coding that allows the storage control to check for double selection.

Select Hold maintains selection and must remain active until all operations are complete on the selected controller or drive. Select Active remains active until Select Hold falls. If a selection error occurs within the controller or drive, no response is generated.

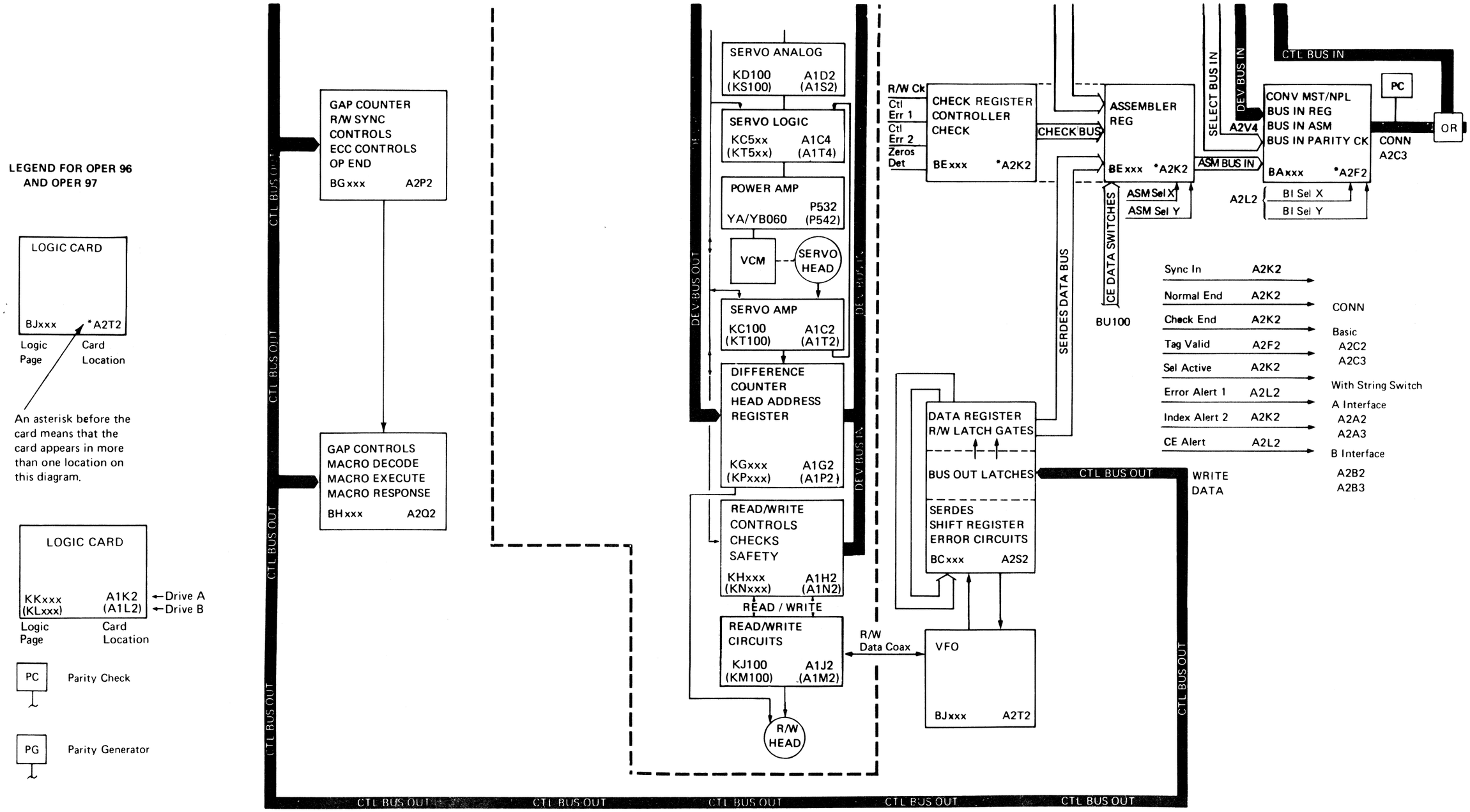


CONTROLLER OUT — DRIVE — CONTROLLER IN

Note: *See Legend on OPER 97.*

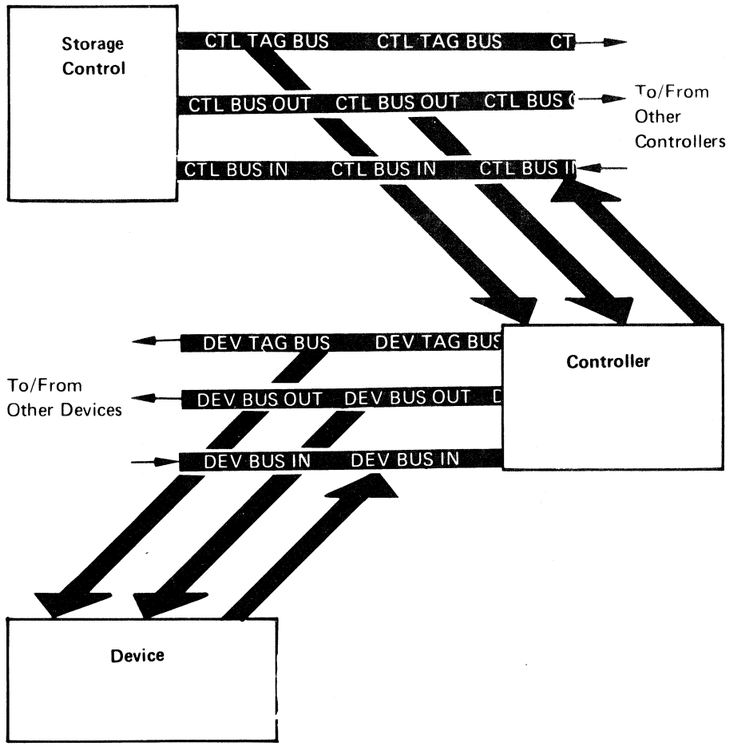


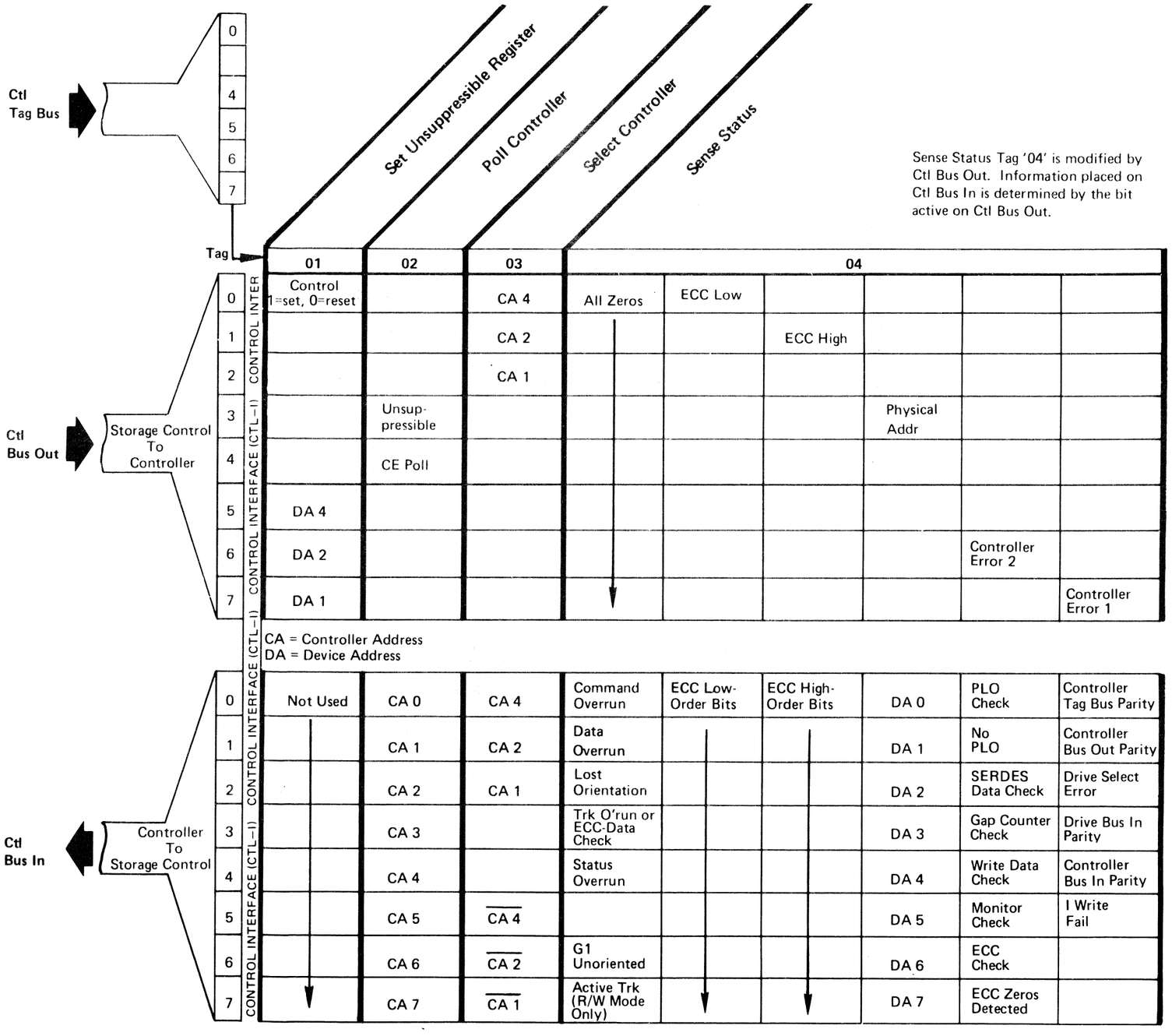
INTERFACE DATA AND CONTROL FLOW OPER 97



CONTROL AND DEVICE INTERFACE SUMMARY

Tag Bus Decode	0	1	2	3	4	5	6	7	Operations performed by:
01–0F	0	–	–	–	X	X	X	X	Controller only
82–85	1	–	–	–	0	X	X	X	Controller and drive
89–8F	1	–	–	–	1	X	X	X	Drive only





	01	02	03	04					
0	Control 1=set, 0=reset		CA 4	All Zeros	ECC Low				
1			CA 2			ECC High			
2			CA 1						
3		Unsup-pressible					Physical Addr		
4		CE Poll							
5	DA 4								
6	DA 2							Controller Error 2	
7	DA 1								Controller Error 1

	Not Used	CA 0	CA 4	Command Overrun	ECC Low-Order Bits	ECC High-Order Bits	DA 0	PLO Check	Controller Tag Bus Parity
0									
1		CA 1	CA 2	Data Overrun			DA 1	No PLO	Controller Bus Out Parity
2		CA 2	CA 1	Lost Orientation			DA 2	SERDES Data Check	Drive Select Error
3		CA 3		Trk O'run or ECC-Data Check			DA 3	Gap Counter Check	Drive Bus In Parity
4		CA 4		Status Overrun			DA 4	Write Data Check	Controller Bus In Parity
5		CA 5	$\overline{\text{CA 4}}$				DA 5	Monitor Check	I Write Fail
6		CA 6	$\overline{\text{CA 2}}$	G1 Unoriented			DA 6	ECC Check	
7		CA 7	$\overline{\text{CA 1}}$	Active Trk (R/W Mode Only)			DA 7	ECC Zeros Detected	

CONTROL AND DEVICE INTERFACE SUMMARY

Ctl Tag Bus → Tag: 0, 4, 5, 6, 7

Ctl Bus Out → CONTROL INTERFACE (CTL–I):

	05 Reset Read/Write	06 Switch Control 1 (SWFE Feature)	07 Switch Control 2 (SWFE Feature)	08 ECC Control	09 Transmit Control	0A Read Control (Information gated on Bus In controlled by bit active on Bus Out)	0B SYNC (RAS TP)	0C Display CE High	0D Display CE Low	0E Read OP	0F Write OP
0	0	See OPER 102	See OPER 102		Controller Reset	Device Type	Not Used	Lamp 0	Lamp 0	Modifier Bits	Modifier Bits
1	0					Data Entry Switches		1	1		
2	0				Set Diagnostic			2	2		
3	0				Reset Diagnostic			3	3		
4	0			Count 8				4	4	Count 8	Count 8
5	0			4	Diagnostic Bit 4			5	5	4	4
6	0			2	2			6	6	2	2
7	0			1	1			7	7	1	1

Type of Read Op defined by bits 0–3:
0001 Clock G3
0010 Clock G2
0011 Read G4
0100 Read G1
0101 Read G3
0110 Read G2
0111 Read G3 AM Search
1110 Special Read G2

Type of Write OP defined by bits 0–3:
0010 Write G2
0011 Format Reorient
0100 Format G1
0101 Format G3
0110 Format G2
0111 Format/Erase
1011 Write G4
1100 Special Format G1
1110 Special Format G2

Diagnostic Bit Decodes:
000 = Invert Dev Bus In and Ctl Bus In P bit
001 = Invert Tag Bus P bit
010 = Invert Bus Out P bit
011 = Suppress Write Gate

Ctl Bus In ← CONTROL INTERFACE (CTL–I):

	05	06	07	08	09	0A		0B	0C	0D	0E	0F
0	Not Used	See OPER 102	See OPER 102		0		CE Switch 0	Not Used	Undefined	Undefined	Tag Valid	Tag Valid
1					1		1					
2					2		2				Lost Orientation	Lost Orientation
3					3		3					
4					4		4				Status Overrun	Status Overrun
5					5	3340	5					
6					6		6				Read G1 Unoriented	
7				ECC Zeros Detected	7		7				Active Track	Active Track

	Normal End	Check End
Tag Valid	0	Command Overrun
	0	Sync Out Timing Error
Lost Orientation	0	
	0	ECC Data Check
Status Overrun	0	No AM* Found
	0	No Sync Byte Found
Read G1 Unoriented	0	Data Found
Active Track	0	

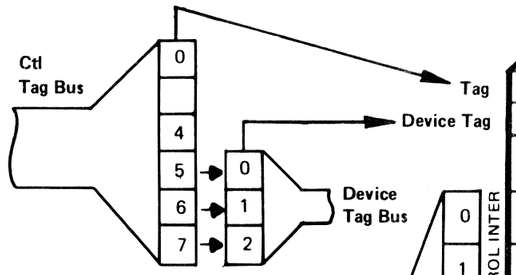
Tag Valid	Normal End	Check End
	0	Command Overrun
	0	Sync Out Timing Error
Lost Orientation	0	
	0	Track Overrun
Status Overrun	0	
	0	
	0	
Active Track	0	

*Redundant ECC Data Check (see OPER 103).

CONTROL AND DEVICE INTERFACE SUMMARY

The three bits of Dev Tag Bus are forced to 000 for Select Device operation (Tag '83') and to 111 for Set Rd/Wr (Tag '85').

For Tags '89' through '8F', Ctl Tag Bus bits 5, 6, and 7 are shifted to Device Tag Bus bits 0, 1, and 2 without change.



CONTROL AND DEVICE INTERFACE TAG SUMMARY

For Drive Only operations '8A' through '8F', Ctl Bus Out is routed through the controller to the device without change. Dev Bus Out and Dev Bus In only are shown.

Control Tag '8F' is modified by Dev Bus Out. Information placed on Dev Bus In is determined by bits active on Dev Bus Out.

Device Bus Out

DEVICE INTERFACE (DEV I)	8A Diagnostic Set	8B Set HAR	8C Set Difference	8D Set Target	8E Set Cylinder	8F Control																	
	2	3	4	5	6	7																	
0	Servo Reset	Fixed Heads 32–59	Difference Counter 128	Target Register	Cylinder Address Register 256							Direction 1 = In						1	0	0	0		Transfer Sector Count
1	Go Home	Fixed Heads 0–31	64	64	128							Difference Counter 512						0	1	0	0		Write Gate
2		Head Address Register 32	32	32	64							Difference Counter 256						0	0	1	0		Unsquelch
3		16	16	16	32							Cylinder Address Hi 512						0	0	0	1		Read Gate
4		8	8	8	16	Seek Start 1	Attention Reset 0	Check Reset 1	Rezero 0	Drive Sync 1	Read/Write Check Reset 0	Set Difference Hi 1	Sense CAR 0	Sense Difference Counter 1	Sense HAR 0	Sense Target 1	Sense Status 0	Sense Status 1 (Drive Checks) 0	Sense Status 2 0	Sense Status 3 0	Sense Status 4 (Access Status) 0	Sense Read/Write 1	Address Mark Gate
5		4	4	4	8	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1
6	Force Multichip Check	2	2	2	4	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1
7	Decrement Difference Counter	1	1	1	2	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Device Bus In

DEVICE INTERFACE (DEV-I)																							
0	Undefined	Machine Status*	Machine Status*	Machine Status*	Machine Status*	Machine Status*	Machine Status*	Machine Status*	Machine Status*	Not Used	Machine Status*	Machine Status*	Cylinder Address Register 256	Difference Counter 128	Fixed Heads 32–59	RPS Installed	Direction 1 = In	Size		Drive Start Switch On	Access Timeout Check	Multi-chip Check	
1													128	64	Fixed Heads 0–31	64	Difference Counter 512	Sector Compare Check	HDA Sequence Latch 4	Guard-band Pattern	Overshoot	Capable/ Enable Check	
2													64	32	Head Address Register 32	32	Difference Counter 256	Motor at Speed Latched	HDA Sequence Latch 2	Target Velocity	Servo Off-Track	Write Overrun	Drive Check
3													32	16	16	16	Cylinder Address 512	Air Switch Latched	HDA Sequence Latch 1	Track Crossing	Rezero Mode	Index Check	R/W Check
4													16	8	8	8	Head Short Check	Write Enable	HDA Sequence Check Latch		Servo Latch	Delta I Write Check	On Line
5													8	4	4	4		Size Bit 4	Inhibit HDA Recycle	Air Switch	Linear Mode Latch	Control Check	I Write Sense
6													4	2	2	2		Size Bit 2			Control Latch	Transition Check	Index Mark
7													2	1	1	1	1 (Always On)	Size Bit1	Odd Physical Track	Motor at Speed	Wait Latch	Write I Check	Active Track

Head Address Register: 16, 8, 4, 2, 1

Target Register: 32, 16, 8, 4, 2, 1

** Machine Status bits are same as Dev Bus In under Tag '84', R/W On or R/W Off.*

CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

SET UNSUPPRESSIBLE REGISTER — '01'

Tag '01' sets the unsuppressible register in the controller to mask certain drive addresses and block them from activating Bus In during polling. This allows some interrupt priority decisions to be made at the controller level. This tag is of the immediate class.

Bus Out bits 5, 6, and 7 contain the drive address. The appropriate latch is set when bit 0 is active and it is reset when bit 0 is inactive.

The unsuppressible register is reset during power on.

POLL CONTROLLER — '02'

Tag '02' allows all controllers to be polled for service requests. Bus Out defines the type of service request the poll is addressing. If Bus Out bits 3 and 4 are zero, a drive interrupt from any drive causes the controller to respond with the controller bit significant address on Bus In.

If Bus Out bit 3 is active, the controller responds to only those drive interrupts that have their drive addresses set in the unsuppressible register. For example, if a drive with address 3 has an interrupt, but bit 3 of the unsuppressible register is inactive, then the controller does not respond on Bus In.

If Bus Out bit 4 is active, the controller responds on Bus In with its bit significant address only if it has a CE maintenance panel request.

Tag Valid and Normal End are initiated by all controllers. This tag is of the immediate class.

SELECT CONTROLLER — '03'

Tag '03' is used when CE Panel communication is desired.

Bus Out bits 0 through 2 contain the controller address. If the address on Bus Out matches that assigned to the controller, Bus In responds with the controller address in bits 0 through 2, and its inverse in bits 5 through 7. Tag Valid, Select Active, and Normal End are activated. Bus In is checked to ensure that only one controller is selected.

If the address on Bus Out is not recognized or if either Bus Out or Tag Bus have incorrect parity, no inbound lines are activated. Parity on Bus In is guaranteed if Normal End is present.

If a device control command is issued when only the controller has been selected, no Tag Valid or end responses are present. This tag is of the immediate class.

SENSE STATUS — '04'

The Sense Status tag (Error Bytes tag) reads the drive physical address, error correction pattern, and controller detected errors. Bus Out defines the byte present on Bus In as follows:

0000 0000 Orientation Status Byte

All zeros on Bus Out bring up Tag Valid to check the status bytes at the beginning of a Read/Write operation.

1000 0000 Gate ECC Low Byte

Bit 0 gates the ECC low-order correction byte into Bus In.

0100 0000 Gate ECC High Byte

Bit 1 gates the ECC high-order correction byte onto Bus In.

0001 0000 Gate Physical Address

Bit 3 gates the bit significant physical address of the drive onto Bus In.

0000 0010 Gate Controller Error 2

Bit 6 gates Error Byte 2 onto Bus In. Except for ECC Zeros Detected (Bus In bit 7), Error Byte 2 contains errors or conditions that were reported as a Controller Check in the status byte. These errors or conditions are shown on OPER 98.

0000 0001 Gate Controller Error 1

Bit 7 gates Error Byte 1 onto Bus In. Error Byte 1 contains errors or conditions reported as a Controller Check in the status byte. These errors or conditions are shown on OPER 98.

RESET READ/WRITE — '05'

Tag '05' resets the Read/Write state established by Set Read/Write. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

SWITCH CONTROL 1 — '06' (STRING SWITCH ONLY)

Tag '06' sets and resets the Assignment, Device End, and Pack Change registers in the drive; it also reads the switch status.

Bus Out

1100 xaaa	Assign Drive to interface
0100 xaaa	Unassign Drive from interface
1010 xaaa	Set Device End latch
0010 xaaa	Reset Device End latch
1001 xaaa	Set Pack Change latch for opposite interface.
0001 xaaa	Reset Pack Change latch for this interface.

Note: *aaa = binary drive address*

Bus In

1001 0xxx	Device End Interrupt is active for this interface.
0101 0xxx	Pack Change Interrupt is active for this interface.
0011 0xxx	Addressed drive is assigned to this interface.
0001 0xxx	Connection is made through a switchable controller.
0001 1xxx	Addressed drive is assigned to the opposite interface.

If the string switch feature is not installed, no Bus In bits are active.

Parity is never generated.

SWITCH CONTROL 2 — '07' (STRING SWITCH ONLY)

Long Connection is required when extended operations are to be performed (see OPER 95). Tag '07' with Bus Out modifiers sets and resets Long Connection.

The Reset Disable Interlock command activates the disabled portion of the Enable/Disable manual switch.

Bus Out

11x0 xxxx	Set Long Connection
01x0 xxxx	Unlock Switch operation (Reset Long Connection latch)
00x1 xxxx	Reset Disable Interlock

ECC CONTROL — '08'

Tag '08' is used when a Data Check has been detected to determine correctability of the data. This is done while Set Read/Write is still active.

This tag is of the extended class.

TRANSMIT CONTROL — '09'

Tag '09' initiates an operation as defined by the contents of Bus Out. This tag is of the immediate class.

Bus Out bits, when active, perform the following functions:

Bit 0 — Controller Reset

Bit 0 resets all the control latches and the check indicator latches.

Bit 2 — Set Diagnostic

Bit 2 sets the diagnostic modes as defined by the Diagnostic Decode.

Bit 3 — Reset Diagnostic

Bit 3 resets any diagnostic mode that is left set in the controller. These modes are also reset by Power On Reset and Controller Reset.

Bits 5 through 7 — Diagnostic Decodes

Refer to Control and Device Interface Summary Chart (OPER 99) for decodes.

CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

READ CONTROL — '0A'

Tag '0A' reads control bytes from the controller. The contents of Bus Out define the byte presented on Bus In. Bus Out must have only one bit active. This tag is of the immediate class.

Bus Out

10xx xxxx Gate Device Type
Gates the device type bits to Bus In if the selected device is online. Bus In bits 4 defines the 3340 (3344).

01xx xxxx Gate CE Switches
Gate contents of CE data switches onto Bus In.

SYNC — '0B'

Tag '0B' provides a scope sync. Activates Test point A2L2J11 (logic page BD100) during a Tag Gate operation.

DISPLAY CE HI — '0C'

Tag '0C' sets the eight high-order positions of the controller CE Panel lights. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

DISPLAY CE LO — '0D'

Tag '0D' sets the eight low-order positions of the controller CE Panel lights. Bus In is not defined and parity cannot be guaranteed. This tag is of the immediate class.

READ OP — '0E'

Tag '0E' issues Read or Clock Data commands to the controller. Tag '0E' is an extended operation (see OPER 95).

When Tag '0E' is issued, the variable frequency oscillator (VFO) must be locked in and Set Read/Write must be active in the drive. Except for the gap codes involving HA and AM Search, all read codes can only be issued after field orientation has been previously established. The controller responds with Check End indicating Command Overrun if this is violated.

Ctl Bus Out

Ctl Bus Out defines the type of Read or Clock Data command and a count. Bits 4 through 7 contain the modulo-16 count of the number of bytes of the next data field to be transferred by the controller. Bits 0 through 3 contain the type of Read and the prefield gap preceding it. The Read and Clock Data commands are as follows:

0001 xxxx CLOCK G3
0010 xxxx CLOCK G2

Clock G3 and Clock G2 commands allow Key and Data fields to be clocked without locking to data and searching for the sync byte. The controller executes these codes by keeping the VFO locked to servo and simulating a Write G3 or G2 operation with the Write Gate off. Sync In occurs then as if the field were being written. The data on Bus In is valid and therefore parity is not generated.

0011 xxxx READ G4

Read G4 is used for defect skipping. It is used to extend a gap by 128 bytes following the Special Read G2 code or to read an area that has been moved because of a defect.

0100 xxxx READ G1

Read G1 allows orientation on Home Address. This code is executed in two ways. If the gap counter is counting from Index and has not reached byte 63, the execution proceeds immediately. If the counter is past byte 63 or if the counter is not running, the execution is delayed until Index occurs. This code never overruns the command. If no sync byte is located before the normal position of HA on the track, a second attempt to read a sync byte is made 128 bytes later. No Sync Found and Check End occur if the second attempt fails.

0101 xxxx READ G3
0110 xxxx READ G2

Both codes (Read G3 and Read G2) involve locking VFO to data sequence at the proper point in the gap, searching for sync bytes, and if successful, transferring the data read and processing the ECC bytes. The difference between Read G2 and Read G3 is that the Read G3 sets the gap counter to process a G3 prefield gap whereas the Read G2 implies a G2 prefield gap. Also, the Transfer Sector Counter line is only activated during execution of the Read G3 code.

0111 xxxx READ G3 AM SEARCH

Read G3 AM Search initiates an address mark search sequence. Once an Address Mark is found, the execution is the same as a Read G3 code. Field orientation is established when Address Mark (AM) is found. Transfer Sector Count line to the drive is activated when an AM is found.

1110 xxxx SPECIAL READ G2

Special Read G2 is the same as Read G2 except that it denotes there is an inter-record gap following and that there is no ECC at the end of the field.

Ctl Bus In

Ctl Bus In is valid for each Sync In as denoted for data transfer after each gap definition. In addition, Bus In is valid for Tag Valid, Normal End, and Check End.

TAG VALID

Information is gated onto Bus In for Command Overrun control.

Bit 0: Not Used

Bit 1: Not Used

Bit 2 Lost Orientation: Indicates that orientation is not established when the Read or Write operation is issued.

Bit 3: Not Used

Bit 4 Status Overrun: Indicates that Tag Gate is active too late for the operation to continue successfully. It usually means that the channel has not responded to Status In on a chained Read or Write operation.

Bit 5: Not Used

Bit 6 G1 Unoriented: Indicates that a Read G1 operation has been issued when the controller is not oriented, that is, not in a G1 gap area.

Bit 7 Active Track: Indicates that the Active Track signal is present (from the selected drive).

NORMAL END

Normal End is raised after the last ECC byte or last byte of a skipped record has been transferred and no error condition has been detected. Bus In is all zeros with correct parity.

CHECK END

Check End is raised if an unusual condition occurs. Bus In is never zero when Check End is active. The conditions causing Check End are as follows:

Bit 0 Command Overrun: Bus In bit 0 is set if the Read operation is not received at the controller before the gap counter reaches byte count 71. The Read G1 and Read G3 AM Search codes are exceptions since they do not have an overrun point. The Check End lines rise after Tag Gate falls at the controller. Since the gap counter stops running when Command Overrun occurs, record orientation is lost. Bit 0 is reset by Response.

Bit 1 Sync Out Timing Error: Bus In bit 1 is set if there is a late or extra response to a Sync Out. Data transfer stops when this condition is detected. Bit 1 is reset by Response.

Bit 3 ECC Data Check: Bus In bit 3 is set if (after processing the ECC bytes) the ECC hardware indicates a data check. This bit is not reset until the next Read or Write operation.

Bit 4 No AM Found/ECC Data Check: Bus In bit 4 is set as an end condition of the Read G3 AM Search code if an AM is not found. It is also set as a redundant ECC Data Check with bit 3. Bit 4 is reset by Response.

Bit 5 No Sync Found: Bus In bit 5 is set if the controller does not find a sync byte. This does not apply to Clock G3 and Clock G2 codes. Bit 5 is reset by Response.

Bit 6 Data Found: Bus In bit 6 is set if at least a single bit was found from the start of a sync byte search. This bit is only gated to Bus In if bit 5 (No Sync Found) is on. Bit 6 is reset by Response.

ERROR ALERT CONDITIONS

Error Alert Condition is activated whenever an error condition is detected that is not covered by Check End. The Error Alert (Selected Alert 1) line may become active at any time and may accompany Tag Valid, Normal End, or Check End. Except for drive selection errors, any condition that sets Error Alert is latched for examination under the Status and Error bytes.

CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

WRITE OP — '0F'

Tag '0F' issues Write commands to the controller. This tag is an extended operation (see OPER 95).

When this tag is issued, The VFO is locked in as a result of the Set Read/Write tag. If the VFO is not locked in, Error Alert reports a VFO error.

Except for the Format G1 code, all other write codes may only be issued after a field orientation on the active portion of the track has been previously established. If this requirement is not satisfied, the controller responds with Check End, and Command Overrun is noted on Bus In. The Format Write operations cause Write Gate to be set at a predetermined point on the track. From this point Write Gate remains active until Index is detected. If subsequent format operations are not activated, zeros are padded throughout the rest of the track. Write Gate is also dropped with Reset Read/Write or the fall of Select Hold. When a format command has been executed, all subsequent Write commands are executed as format commands. When required, the controller writes the following: the address marker, sync byte, data transferred from storage control, ECC bytes, and gaps. Data transfer is initiated with a Sync In when the controller starts to write the sync byte. The ECC bytes are written immediately following the end of data transfer. ECC hardware sequence is handled by the controller. The normal updating Write command causes Write Gate to be set at a predetermined point in the gap and to be reset at the end of the field after the ECC bytes have been written.

Bus Out

Bits 0 through 3 contain the type of Write command (modifiers) to be performed and the prefield gap associated with it. Bits 4 through 7 contain the modulo-16 residual count of the number of bytes of the next field to be transferred to the controller. This count is loaded into the controller data transfer counter. Following is a summary of the Write modifiers.

0010 xxxx WRITE G2

Bit 2 writes a G2 prefield gap. Write Gate is turned off at the end of the data field.

0011 xxxx FORMAT REORIENT

The Format Reorient tag reorients the R/W head on the track when a count field is reached that contains a defect skip within its control. The count field must be rewritten once this is determined. The command is issued in the gap following the count field. Sync In is presented and padding is continued to Index. Sync In continues to the reorientation point. The count used to reorient ahead of the R0 count field is 19,785 bytes and 19,782 bytes when ahead of other fields. This places the orientation just after the last byte before the ECC bytes of the data field and prior to the desired count field. Normal End is presented in the normal manner.

0100 xxxx FORMAT G1

This code causes the controller to search for Index and Active Track. G1 is formatted and Home Address is written according to the data transfer. The Transfer Counter line to the drive is activated at byte 63 in the gap.

0101 xxxx FORMAT G3

The Format G3 tag writes a G3 prefield gap and writes the address mark. The Transfer Counter line to the drive is activated at byte 63 in the gap.

0110 xxxx FORMAT G2

This code is the same as the Write G2 code. It is used to write a G2 prefield gap. Write Gate is turned off at the end of the data field.

0111 xxxx FORMAT ERASE

This code causes zeros to be written to Index and turns off the Write Gate. Clocking continues until Recycle drops and the modulo-16 count has decremented to zero or Index is detected. Track overrun is presented during this command when Index is detected.

1011 xxxx WRITE G4

This code is used to extend a gap before the gap definition is presented or used during an inter-record gap to define the modulo-16 remainder for the second half of the data field.

1100 xxxx SPECIAL FORMAT G1

This code causes a search for Index and Active Track. When found, 128 bytes of zeros are written. After this, the controller continues writing the Format G1.

1110 xxxx SPECIAL WRITE G2

This code allows a following gap without ECC bytes at the end of the data field. Write Gate is turned off after the last byte of data.

Bus In

Bus In is valid when Tag Valid, Normal End, or Check End is active.

TAG VALID

Bits 0 and 1: Not Used

Bit 2 Lost Orientation: Indicates that orientation is not established at the time the Read or Write operation is issued.

Bit 3: Not Used

Bit 4 Status Overrun: Indicates that Tag Gate is active too late for the operation to continue successfully. It usually means that the channel has not responded to Status In on a chained Read or Write operation.

Bit 5: Not Used

Bit 6: Not Used

Bit 7 Active Track: Indicates that the Active Track signal is present (from the selected drive).

NORMAL END

Normal End is raised if the Check End condition does not exist after the last byte of the ECC field is written. Bus In is set to zero.

CHECK END

Bus In is never zero when Check End is raised. Check End is raised if one of the following unusual conditions occur:

Bit 0 Command Overrun: Bus In bit 0 is set if the command is not received at the controller before the gap counter reaches byte count 63 (for operations requiring maintained operation).

Bit 1 Sync Out Timing Error: Bus In bit 1 is set if Sync Out arrives too late to service a byte of data. If Write Gate is active, it is turned off.

Bit 3 Track Overrun: Bus In bit 3 is set if the index point is detected while a field is being written. The field includes the prerecord gap through the end of the ECC bytes. Write Gate is dropped and Check End is raised when Index is detected, except when Format G1 is being processed.

ERROR ALERT

Error Alert is raised whenever an error condition is detected that is not covered by Check End. The alert line may rise at any time.

POLL DEVICE — '82'

Tag '82' allows the drives of the addressed controller to be polled for service requests and can only be issued when no drive is selected on the control interface. Bus Out bits 0 through 2 contain the address of the desired controller. The controller responds with Tag Valid and Normal End if there is no Bus Out or Tag Bus parity error. If Bus Out bit 3 and 5 are zero, the presence of a drive interrupt from any drive causes the bit significant address of that drive to be activated on Bus In.

If Bus Out bit 3 is active, the drive address for which an interrupt exists is only seen on Bus In if the corresponding address in the controller unsuppressible register is set. For example, if a drive with address 7 has an interrupt, Bus In bit 7 is only activated if bit 7 of the unsuppressible register is set.

Bit 5 on Bus Out polls requests from only the drive in the service mode. Bus In bit 0 indicates a request is present. Bus Out bit 3 (unsuppressible) is not defined when polling the service drive and should not be used.

Parity on Bus In is not guaranteed for Poll Device. This tag is of the immediate class.

SELECT DEVICE — '83'

Tag '83' is used to select both a controller and a drive. Bus Out contains the address of the controller and the logical drive address. The controller generates the selection sequence to the drive. Bus Out to the controller is gated on Bus Out to the drive for the logical drive address contained in bits 5 through 7. The controller responds to this tag with Tag Valid, Select Active, and Normal End if the address on Bus Out matches that assigned to the controller and if Tag Valid is received from the device. Tag Valid is returned from the device to the controller if a drive is selected and there are no device Tag Bus or Bus Out parity checks. Bus In contains the controller address and its inverse if selection is successful. When Bus Out bit 4 = 1, drive selection is blocked. Bus Out bit 3 = 1 causes drive in CE Mode to be selected while ignoring bits 5 through 7. If the address on Bus Out is not recognized, or if either Bus Out or Tag Bus have incorrect parity, no inbound lines are activated. This tag is of the immediate class.

CONTROL AND DEVICE INTERFACE TAG DESCRIPTION

READ STATUS — '84'

Tag '84' causes the controller to transmit the drive status onto Bus In bits 1 through 7. The tag does not affect the drive. The Controller Check bit is transmitted on Bus In bit 0. The drive status has some differences when Set Read/Write is active. Refer to Control and Device Interface Summary chart (OPER 100) for a summary of the status bits with Set Read/Write active and inactive. This tag is of the immediate class.

Correct parity on Bus In is not guaranteed because of the asynchronous state of the information presented.

SET READ/WRITE — '85'

Tag '85' sets the Read/Write control in the controller and synchronizes the VFO with Servo Pulses from the activated drive. The Read/Write control to the device is established as follows:

1. Device Tag Bus bits 0, 1, and 2 are forced to all 1s.
2. Device Bus Out bits 5, 6, and 7 are forced to all 1s.
3. Device Bus Out bits 0 through 4 are conditioned so the various Read and Write controls may be transmitted to the device.
4. Device Tag Gate is forced on.
5. The Device Bus Out parity checker is blocked after Set Read/Write is decoded in the device.
6. Upon detection of Index, the Read/Write controls are blocked for approximately 63 microseconds. This allows the microprogram to set the head address register to a new value during multitrack Read or Search operations.

It is expected that after this tag is issued, Read operation (Tag '0E') or Write operation (Tag '0F') will be issued.

The Read/Write controls are reset by:

1. Reset Read/Write operation (Tag '05').
2. Controller Reset (Tag '09', Bus '80').
3. Dropping Select Hold.

Tag '85' is of the extended class and Normal End usually signals that the Read/Write logic is ready. Check End is not possible.

Bus In is not defined and parity cannot be guaranteed.

SENSE INTERFACE — '89'

Tag '89' determines the cause of a Device Interface check. Bus In bits 6 and 7 indicate:

Bit 6 — Device Bus Out Parity Check.
Bit 7 — Device Tag Bus Parity Check.

This tag forces Tag Valid even though the Device Interface checks are present. The Device Bus Out and Device Tag Bus Parity Check latches are reset when Tag Gate drops.

This tag is of the immediate class. Bus Out is not used.

DIAGNOSTIC SET — '8A'

Tag '8A' is used in conjunction with Device Bus Out to set the selected drive into predefined hardware states to aid troubleshooting.

Device Bus Out

10xx xx00 SERVO RESET

Servo Reset forces the Servo into Zero mode and inhibits access movement or track following control while the tag is active.

01xx xx00 GO HOME

Go Home causes the access mechanism to go to the home position, fully retracted into the Head/Disk Assembly (HDA).

00xx xx10 FORCE MULTICHIP CHECK

The Force Multichip Check command sets the Odd Head latch in the drive. A subsequent Set Read/Write command forces Multichip Check if HAR bit 6 is off.

00xx xx01 DECREMENT DIFFERENCE COUNTER

Decrement Difference Counter causes the difference count to be decreased by one each time Diagnostic Set Tag is applied with Device Bus Out bit 7 active.

SET HAR — '8B'

Tag '8B' is used to transfer the Head Address.

Bits 0 and 1 — Fixed Heads

Bit 0 is on when any one of the 30 fixed heads from 32 to 59 is addressed. Bit 1 is on when any one of the fixed heads from 0 to 31 is addressed.

Bits 2–6 — Head Address

SET DIFFERENCE — '8C'

Tag '8C' loads the difference counter of the selected drive. The difference counter is loaded with the difference between the current cylinder address and the desired cylinder address as calculated by the controlling system. The 256 bit and the 512 bit of the difference counter are loaded with Control Tag '8F' Bus 'xE'. The difference value, including the 256 and 512 bits, must be set at least 8 microseconds before a Seek Start is issued.

SET TARGET — '8D'

Tag '8D' transfers a sector number to the target register of the selected drive for rotational position sensing. The drive immediately begins to perform a Search Sector operation to compare the target register with the sector counter to find a match.

SET CYLINDER — '8E'

Tag '8E' loads the Cylinder Address Register (CAR). CAR is not functionally connected to the access mechanism; it serves only as a storage register to contain current position information of the access mechanism to be used with the string switch feature of the controller. CAR is reset by a Rezero operation to indicate that the heads are positioned over track 0.

CONTROL — '8F'

Tag '8F' transfers control information to the selected drive. Under this tag, the Device Bus Out is divided into two groups of four bits each. Device Bus Out bits 4 through 7 are coded to perform 14 different functions. Bits 0 through 2 are interpreted to further control certain of these functions. Refer to Control and Device Interface Summary chart on OPER 101. The functions are:

Seek Start
Attention Reset
Check Reset
Rezero
Drive Sync
Read/Write Check Reset
Set Difference High
Sense CAR
Sense Difference Counter
Sense HAR
Sense Target Register
Sense Status
Sense Read/Write
Diagnostic Set Read/Write

xxxx 1000 Seek Start

Seek Start causes the drive to move the Read/Write heads as specified by the information contained in the Difference Counter and Head Address Register. The Difference Counter and the Head Address Register must previously have been set. If the difference count is zero, no physical accessing occurs, and the completion of the zero track Seek is signaled immediately. Completion of the action initiated by Seek Start is signaled by Attention. At the termination of a Seek, the Seek Complete status bit in the machine status is on. An Access failure is indicated by the Drive Check bit being active with Attention.

xxxx 0100 Attention Reset

Bit 5 resets the attention signals in the selected drive. To prevent masking of attention signals, Attention Reset should be performed to reset attentions already present prior to the initiation of an operation resulting in an attention. Attention Reset also cancels pending Seek Rezero or Search Sector Attentions.

xxxx 1100 Check Reset

This code resets check conditions in the selected drive including Read/Write checks.

xxxx 0010 Rezero

Bit 6 causes the drive to place the heads over track 0 with HAR and difference counter reset to zero, which is the same condition as that after a head/disk assembly has completed a load sequence. Rezero is a low-speed operation used to recover to a known track position after a seek error has occurred. Check Reset must be issued prior to a Rezero operation if an Access check is present in the drive. The response of the drive to the controller after completion of this control function is similar to Seek Start.

xxxx 1010 Drive Sync

Drive Sync causes A1C2G02 to shift to a minus level (MST–1). The microdiagnostics use this to provide oscilloscope sync pulses.

CONTROL AND DEVICE INTERFACE DESCRIPTION

xxxx 0110 Read/Write Check Reset

Read/Write Check Reset causes these common Read/Write Checks to be reset:

- Multichip Check
- Capable/Enable Check
- Write Overrun
- Index Check
- Delta I Write Check
- Control Check
- Transition Check
- Write Current Check

yyyy 1110 Set Difference High

Set Difference High is used to load yyyy (yyyy=Bus Out bits 0–3):

Bit 0 – Direction (1=in)
Bit 1 – Difference count 512
Bit 2 – Difference count 256 (Bits 2 and 3 are extensions of the difference counter. See Tag '8C'.)
Bit 3 – CAR bit 512. (This is an extension of cylinder address register. See Tag '8E'.)

xxxx 0001 Sense CAR

Sense CAR causes the contents of the cylinder address register to be presented on the Device Bus In.

xxxx 1001 Sense Difference Counter

Sense Difference Counter causes the contents of the difference counter to be presented on the Device Bus In.

xxxx 0101 Sense HAR

Sense HAR causes the contents of the head register to be presented on Device Bus In.

xxxx 1101 Sense Target Register

Sense Target Register causes the contents of the target register to be presented on the Device Bus In.

xxxx 0011 Sense Status

Sense Status causes one of five drive status bytes to be placed on Device Bus In as determined by bits 0 through 3 of Device Bus Out. For a summary of each of the status bytes, refer to the Control and Device Interface Summary Chart on OPER 101.

xxxx 1011 Sense Read/Write

Sense Read/Write presents Read/Write check conditions on the Device Bus In. Refer to OPER 101 for Bus In bit significance.

xxxx x111 Diagnostic Set Read/Write

Diagnostic Set Read/Write causes bits 0 through 4 of the Device Bus Out to control Read/Write functions in the device. While the Set Read/Write Control function is present, parity checking of Device Bus Out by the drive is disabled and Read/Write status of the drive is presented on Device Bus In. Refer to the Control and Device Interface Summary Chart on OPER 101 for the drive status on Device Bus In.

During a normal Set Read/Write, (see Set Read/Write Tag '85' on OPER 105), the controller hardware controls the action of the bits on Device Bus Out. During a Diagnostic Set Read/Write (Tag '8F', Bus xxxx x111) the diagnostic microprogram must control the bits on Device Bus Out.

The control functions under Device Bus Out are as follows:

Bit 0 Transfer Sector Count: The contents of the sector counter are transferred to the target register for later readout.

Bit 1 Write Gate: When active, (along with bit 4) Address Mark Control causes writing to be performed on the head/disk assembly. Read/Write Checks prevent writing.

Bit 2 Unsquelch: During Read operations, bit 2 causes squelch to be removed from the read amplifier to allow read data operations.

Bit 3 Read Gate: Causes the read amplifier, read detector, and data line drivers to be set to Read mode. Read/Write checks prevent Read operations.

Bit 4 Address Mark Control: In Read mode, the read detector is set to detect Address Marks. In Write mode, it must be used with Write Gate to allow writing on the head/disk assembly.

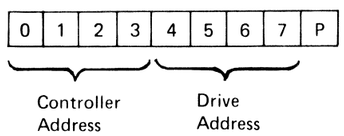
Bits 5 through 7: Must be ones.

SELECT OPERATION

This page describes the diagram on OPER 111.

UNIT SELECTION

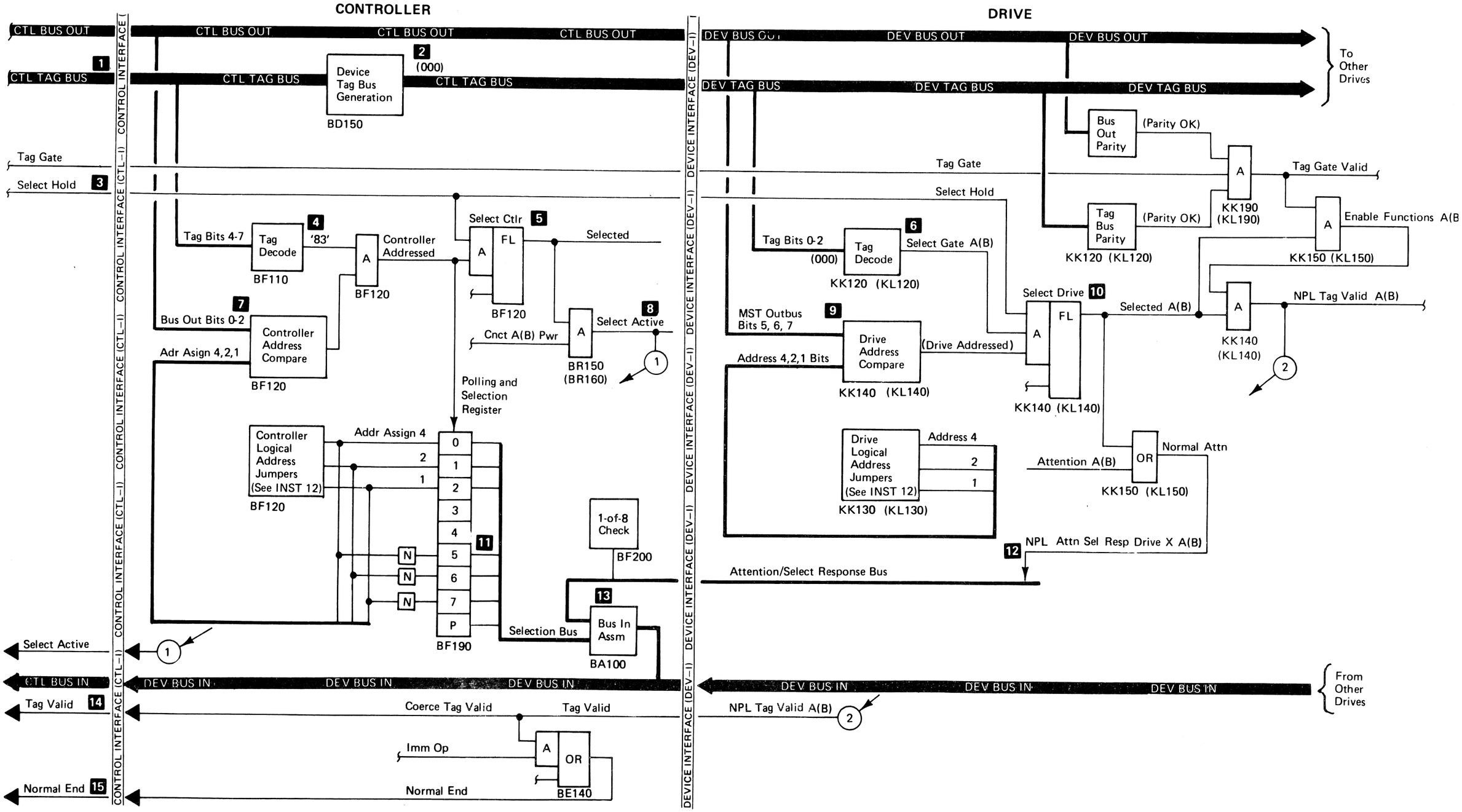
The unit address consists of an 8-bit byte plus parity. Bits 0 through 3 contain the address of a controller. Bits 4 through 7 contain the address of a drive.



To select a drive:

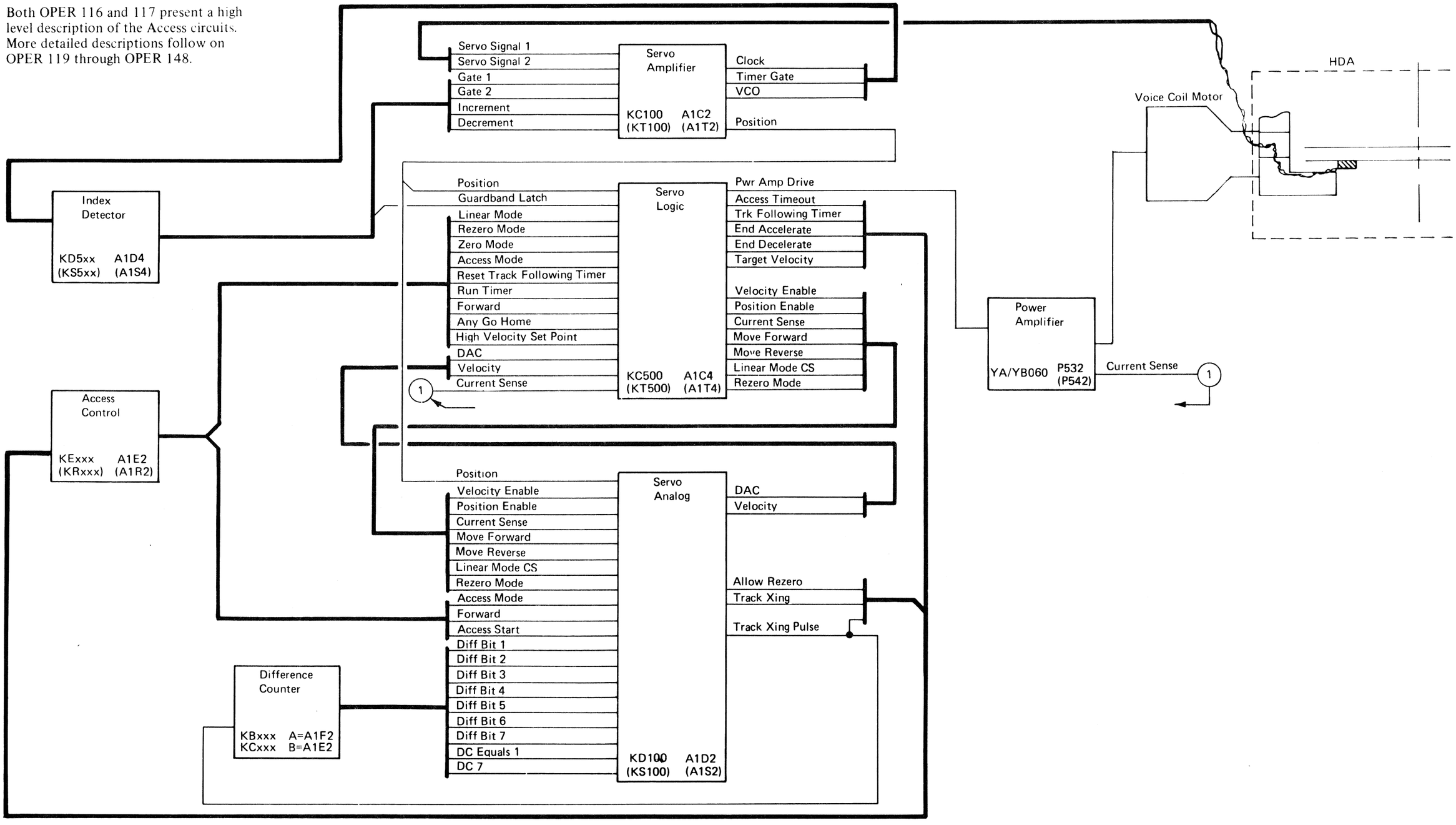
1. Storage control places Tag '83' on Ctl Tag Bus **1**. Tag '83' indicates that an address is on Ctl Bus Out **1**.
2. Each controller decodes Tag '83' **4**.
3. Storage control places a unit address (a controller address and a drive address) on Ctl Bus Out **1**. (Ctl Bus Out bit 3 is zero.)
4. Storage control activates Tag Gate and then Select Hold **3**.
5. Each controller compares its prewired 3-bit address and Bus Out bits 0 through 2 **7**.
6. Comparison is successful in the controller when Controller Addressed becomes active. This sets the Select Ctlr latch **5** and causes Select Active **8** to be sent from the selected controller to storage control.
7. The selected controller places its prewired 3-bit address on Selection Bus bits 0 through 2 and the inverted prewired 3-bit address on Selection Bus bits 5 through 7, (3-of-6 code) **11**. Selection Bus bits 0 through 2 and 5 through 7 are placed on Ctl Bus In by the Bus In Assm **13**.
8. The selected controller generates Dev Tag Bus Tag (000) from Ctl Tag Bus Tag '83' **2**.
9. Each drive attached to the selected controller generates Select Gate **6** from Tag bits 0 through 2 (000).
10. Each drive compares its prewired 3-bit address and MST Outbus Bits 5 through 7 **9**.
11. Comparison will be successful in one drive where Drive Addressed becomes active. This sets the Select Drive latch and activates Selected A (B) **10**.
12. Selected activates NPL Attn Sel Resp Drive X A (B) which activates the drive address bit on the Attention/Select Response Bus **12**. (Bit 0 = drive 0, bit 1 = drive 1, etc.) Selected also gates Tag Gate Valid to the controller.
13. A Sense Physical Address tag (Ctl Tag Bus '04' and Ctl Bus Out '10') gates the Attention/Select Response Bus through the Bus In Assm onto Ctl Bus In **13**.
14. The controller sends Tag Valid **14** and Normal End **15** to storage control.

SELECT OPERATION



ACCESS OPERATION – BLOCK DIAGRAM BY CARD

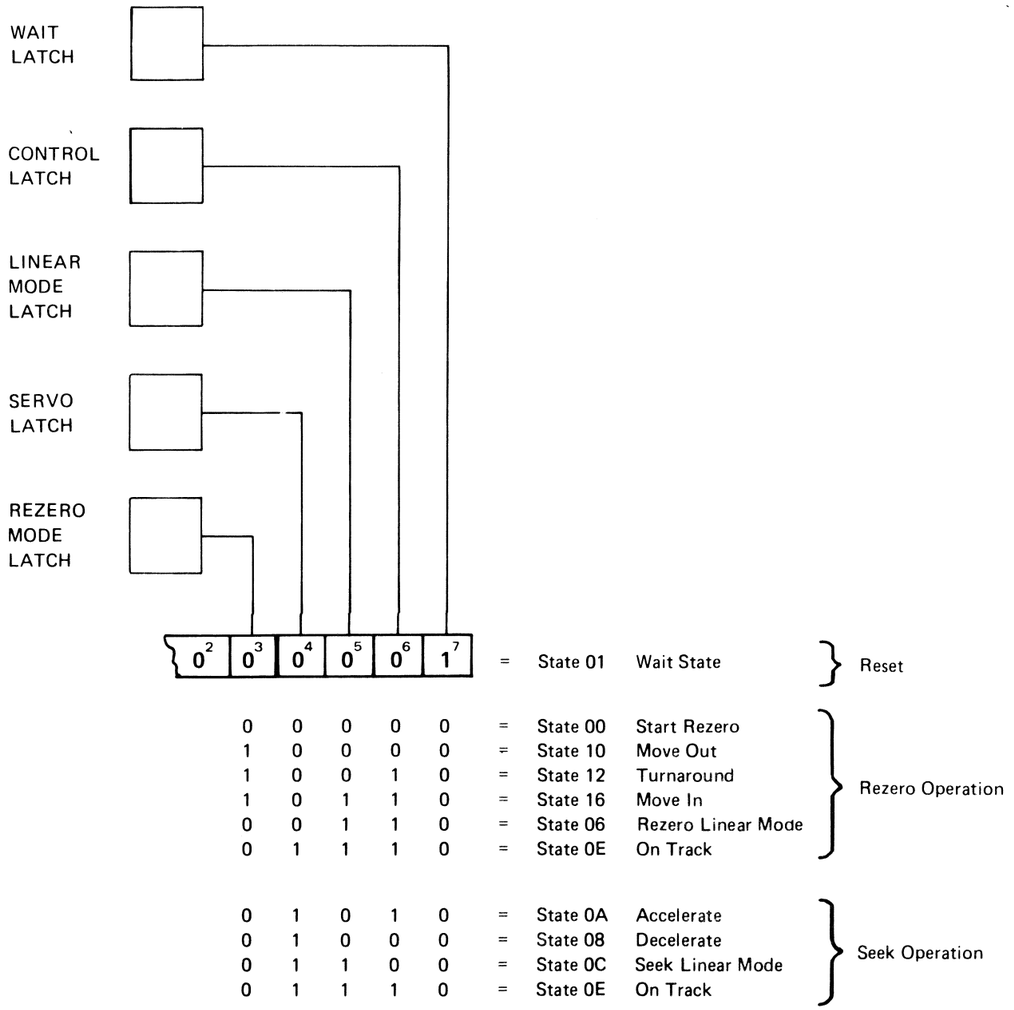
Both OPER 116 and 117 present a high level description of the Access circuits. More detailed descriptions follow on OPER 119 through OPER 148.



ACCESS OPERATION — BLOCK DIAGRAM DESCRIPTION

ACCESS CONTROL

Access control provides control signals for the servo logic to start operations and give direction and speed for access movement. Five latches monitor the correct state of the access operation.



INDEX DETECTOR

The Index detector identifies Index patterns for Index sensing and identifies the sectors for Rotational Position Sensing (RPS).

DIFFERENCE COUNTER

During Seek operations, the difference counter counts track crossings as the heads move from the start track to the target track.

SERVO AMPLIFIER

The servo amplifier maintains an even signal from the servo head to develop the Position signal. It provides input and timing for the Voltage Controlled Oscillator (VCO), the sector counter, and the Index register.

SERVO LOGIC

The Servo Logic circuits drive the power amplifier, monitor access operations, and act as an interface between access control and servo analog.

SERVO ANALOG

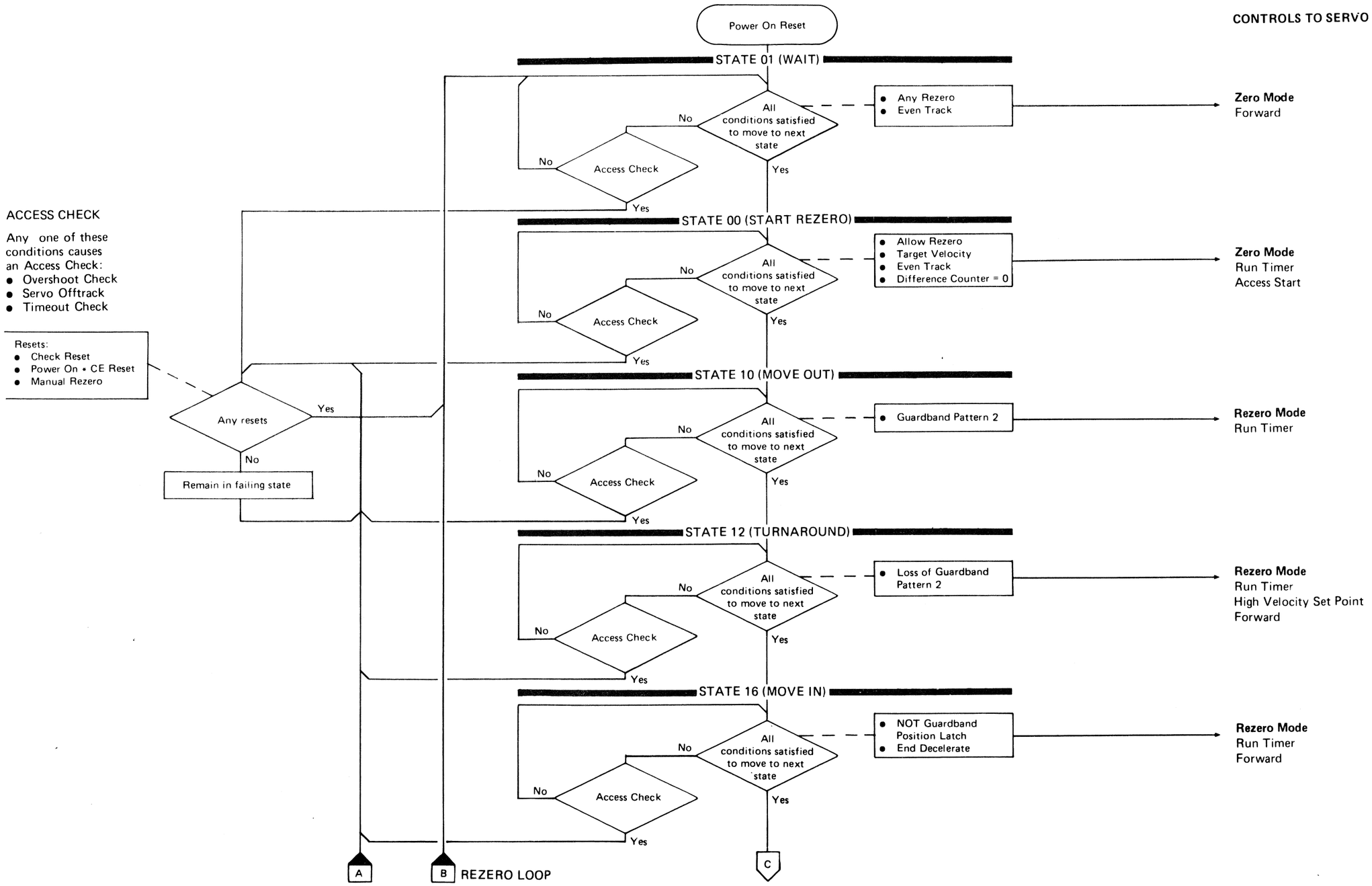
The Servo Analog converts the Position signal, the difference counter, and the track crossing inputs into the Velocity output signal. Velocity represents the carriage speed.

POWER AMPLIFIER

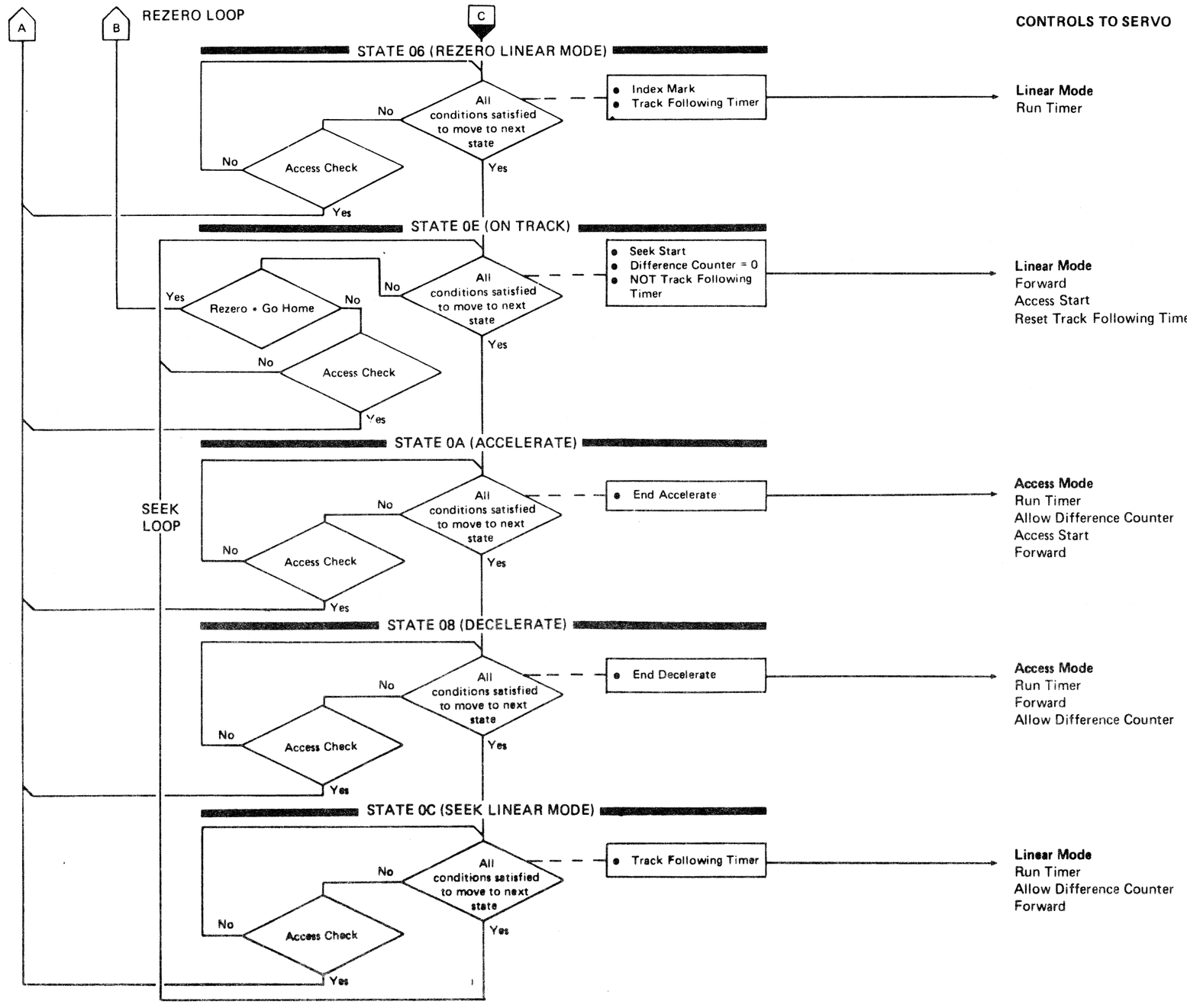
The power amplifier amplifies forward-or reverse-drive current to move the voice coil.

VOICE COIL MOTOR

The voice coil motor is connected to the carriage within the head/disk assembly (HDA). When the voice coil motor moves, the carriage and the heads also move.



ACCESS CONTROL SEQUENCE



TRACK FOLLOWING

All data heads in the head/disk assembly (HDA) are tied directly through the carriage to the servo head. When the servo head is on a particular track, every head is on the same numbered track within its own data band.

At the completion of a Seek or Rezero operation, the servo head locks on the correct track and continues to follow that track until a new Seek or Rezero operation is initiated.

TRACK FOLLOWING LOOP

1. The servo head **1** reads the servo signal.
2. The servo amplifier **2** develops the composite servo signal.

   Steps 1 and 2 are described in more detail on OPER 124 and OPER 125.
3. The demodulator **3** produces a voltage level (Position signal) proportional to the servo head position over the center of the servo track.
4. The compensator **4** uses the Position signal to generate the Position Error signal. This error signal is proportional to the distance that the servo head is off the track center.
5. During track following time, access control provides Linear Mode, which gates Position Error through the select amplifier **5** to generate Power Amp Drive to the power amplifier.
6. The power amplifier **6** provides the current to the voice coil motor to move the servo head back on track.

ACCESS CHECK

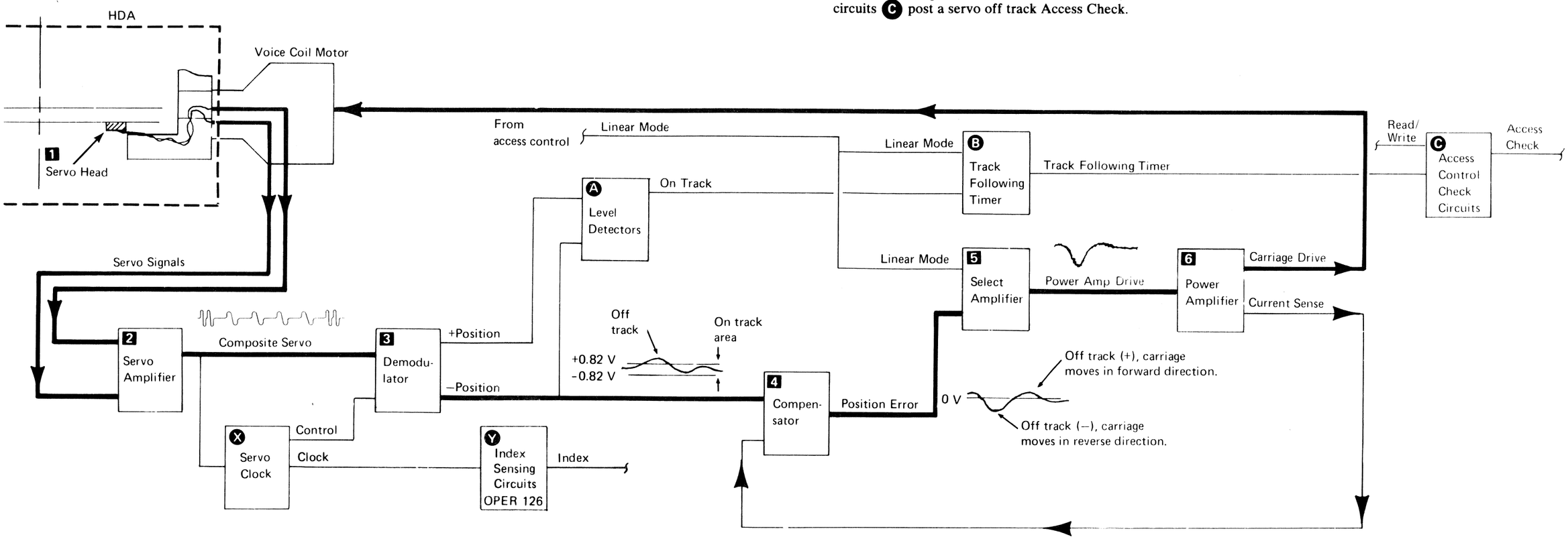
1. The Position signal is checked by voltage level detectors **A** to determine when the servo head is within the proper *on track* area.
2. During Linear Mode, the track following timer **B** sends a signal to access control if the heads remain on track.
3. If the Track Following Timer signal is lost during a Read or Write operation, the access control check circuits **C** post a servo off track Access Check.

SERVO CLOCK

The servo clock **X** develops clock pulses to synchronize Read/Write operations to the disk and access control lines.

INDEX SENSING

Using the clock bits from the servo clock, the Index sensing circuitry **Y** determines when the servo head passes over an Index Mark. (See OPER 126 for a more detailed description of Index detection.)

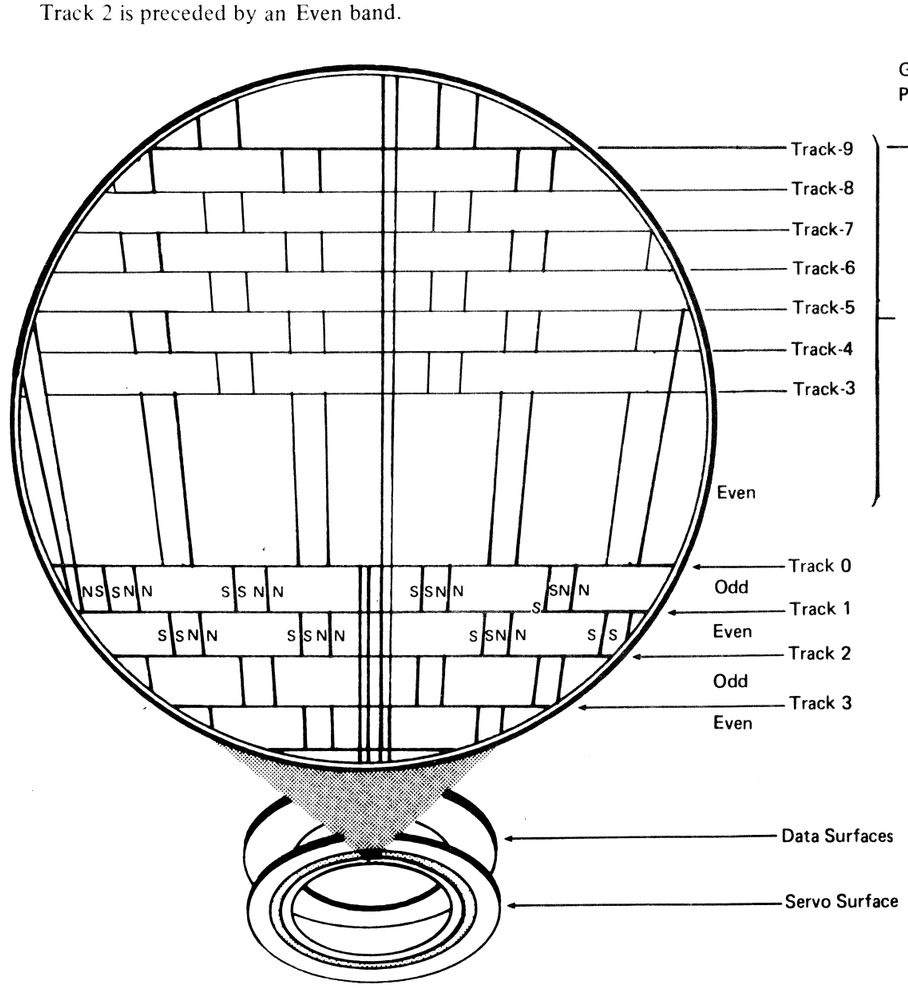


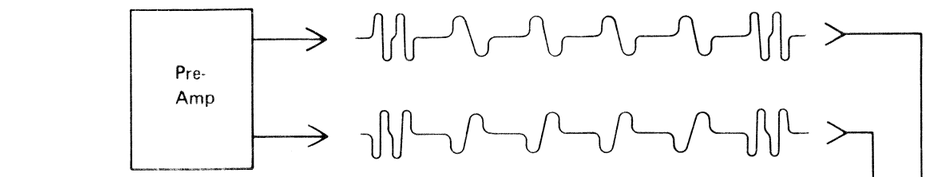
TRACK FOLLOWING

In order for the servo head to be able to track follow, the servo surface of the HDA has the following format:

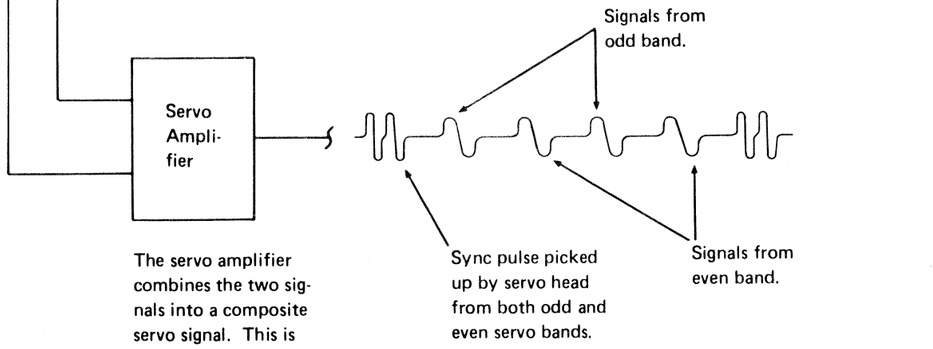
- 561 tracks between special prerecorded bands.
- Bands are either Odd or Even and arranged alternately; one even, one odd.
- Bands are recorded like bar magnets, end-to-end, with north and south poles.
- Odd-numbered tracks are preceded by odd bands; even-numbered tracks by even bands, so that:

  Track 1 is preceded by an Odd band.
  Track 2 is preceded by an Even band.





As the disk rotates, the servo head senses the magnetic changes. The resultant differential signal passes through the preamplifier in the HDA on the way to the servo amplifier.



The servo amplifier combines the two signals into a composite servo signal. This is the basic pattern used by the servo circuits for track following. (Continued on OPER 125.)

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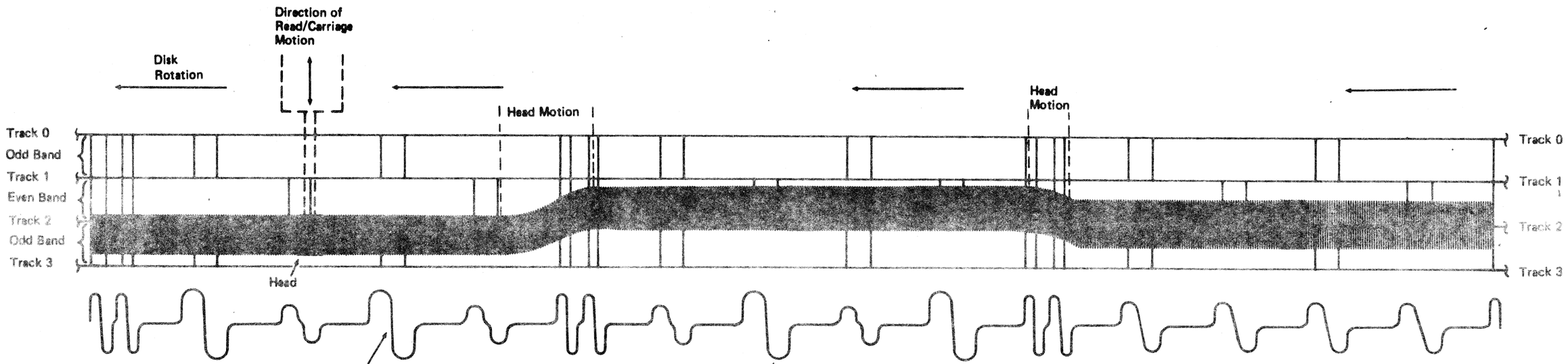
TRACK FOLLOWING

When the servo head is exactly between an "odd" and an "even" band, it is *On Track*. In this example, the head is attempting to follow track 2. As the disk rotates under the head, the carriage tries to keep the head on the track center.



If the servo head drifts off the track center toward the spindle (toward track 3), the composite servo signal becomes unbalanced.

The level of this part of the signal is higher because more current is induced from the odd servo band than from the even band.

If the head drifts off track in the other direction (toward the outer edge of the disk), the signal becomes unbalanced again,

and this part of the signal becomes higher than the other one.

When the servo system recognizes an off-track condition, it moves the carriage in the proper direction to balance the composite servo signal to keep the head on track.

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INDEX DETECTION

It is necessary for Read or Write operations to begin at the correct location on a track. A reference point is needed to indicate the start of the track. The reference point is Index.

The sync characters of the composite servo signal are used for encoding the Index. The method of encoding a single Index bit is to omit the first half of the sync character.

The Index detection circuits recognize an Index bit by this absence of the first half of the sync character and decode it as a one bit.

Figure 1 shows a normal composite servo signal. Figure 2 shows a composite signal with Index coded sync characters.

An Index signal is finally indicated when the correct sequence of ones is decoded. The correct sequence for valid Index 1 is 1-1-0-1-0 and 1-0-1-1-0 for valid Index 2.

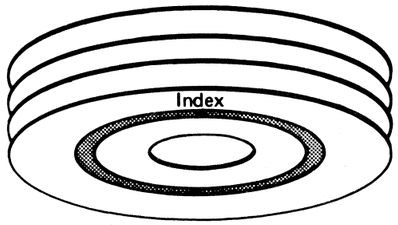


Figure 1. Normal Composite Servo Signal

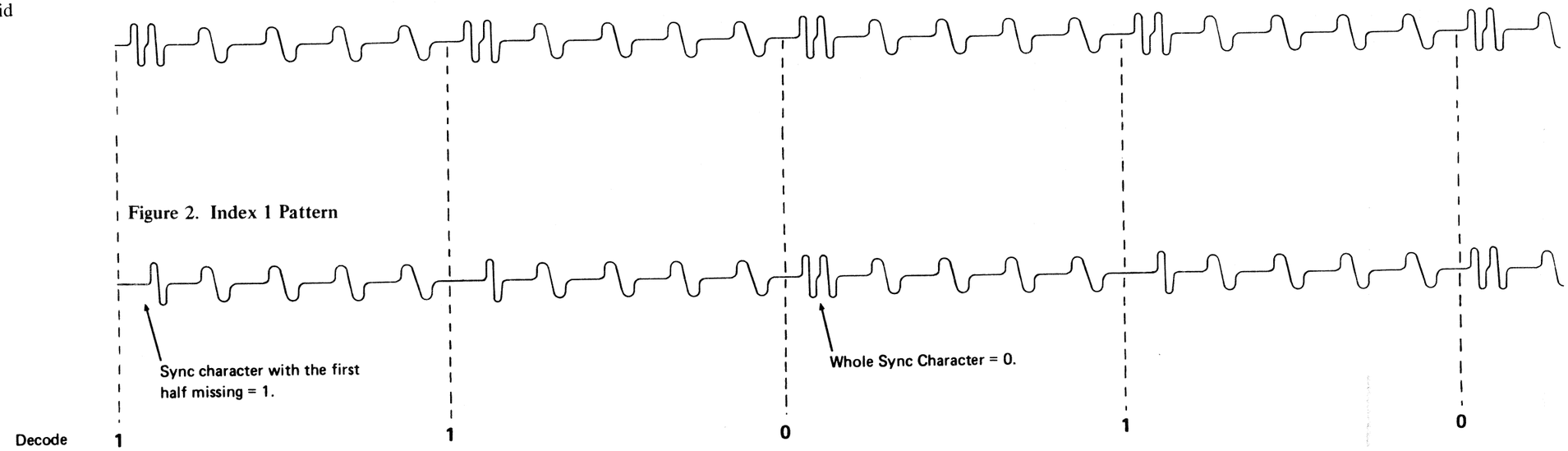
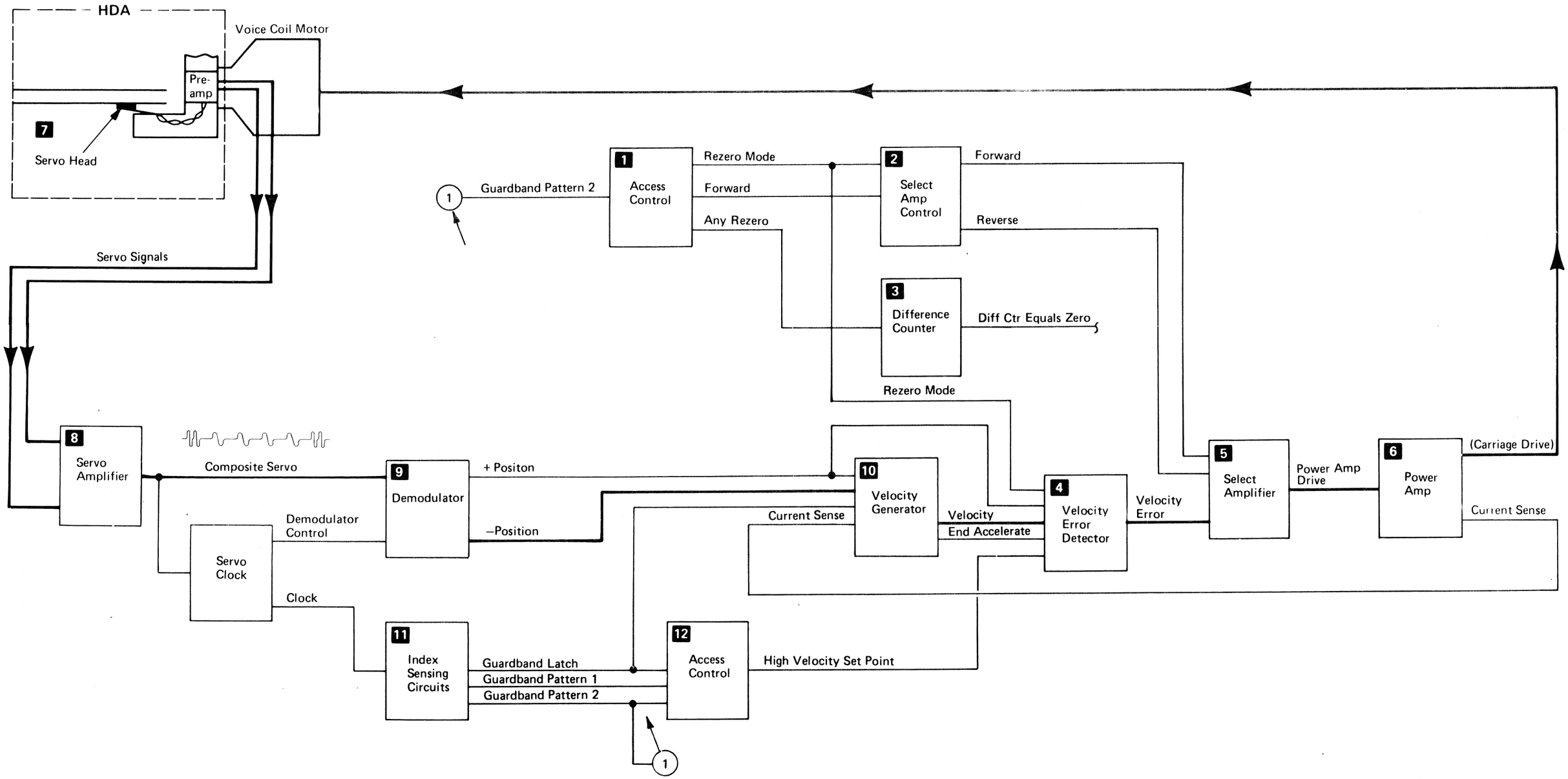


Figure 2. Index 1 Pattern

REZERO -- FUNCTIONAL BLOCK DIAGRAM

See OPER 130 for a description of this diagram



REZERO — BLOCK DIAGRAM DESCRIPTION

The Rezero operation is neccessary to establish (or re-establish) a reference point for access control. Rezero causes the carriage to:

1. Move out from the center of the disk, past track 0.
2. Turn around.
3. Move slowly in the direction of the spindle.
4. Stop and track follow on track 0.

Use the timing diagram on this page with the block diagram on OPER 129.

A Rezero operation begins as a result of one of the following conditions: an HDA Rezero during HDA sequencing, a Recalibrate command under program control, or by a manual Rezero (pushing the Rezero pushbutton on the Operator Panel). For any of these conditions, access control 1 sends Rezero Mode to the select amp control 2 and Any Rezero to the difference counter 3.

The Forward signal from access control to the select amp control 2 indicates the direction the carriage moves at the start of the operation:

- Forward = toward the spindle,
- Reverse = toward the outside edge of the disk.

With Rezero Mode and not Forward as input signals, the select amp control sends Reverse to the select amplifier 5.

Any Rezero from access control resets the difference counter 3. Because the difference counter is reset, and Rezero Mode is active to the velocity detector 4, the maximum velocity of a Rezero operation is 15 inches per second.

With the Velocity Error and Reverse as input signals, the select amplifier 5 provides Power Amp Drive for the power amplifier 6 to start the carriage moving outward from the center of the disk toward track 0.

The servo head 7 reads the servo signal and sends it through the pre-amp and servo amplifier 8 to the demodulator 9.

The output of the demodulator (the Position signal) reflects track crossings used by the velocity generator 10 to calculate the velocity of carriage movement.

When the servo head is in the guardband pattern area, the Index sensing circuits 11 decode Guardband Pattern 1 and send the Guardband Latch signal to the velocity generator 10. (See OPER 131 for a detailed description of guardband pattern detection.)

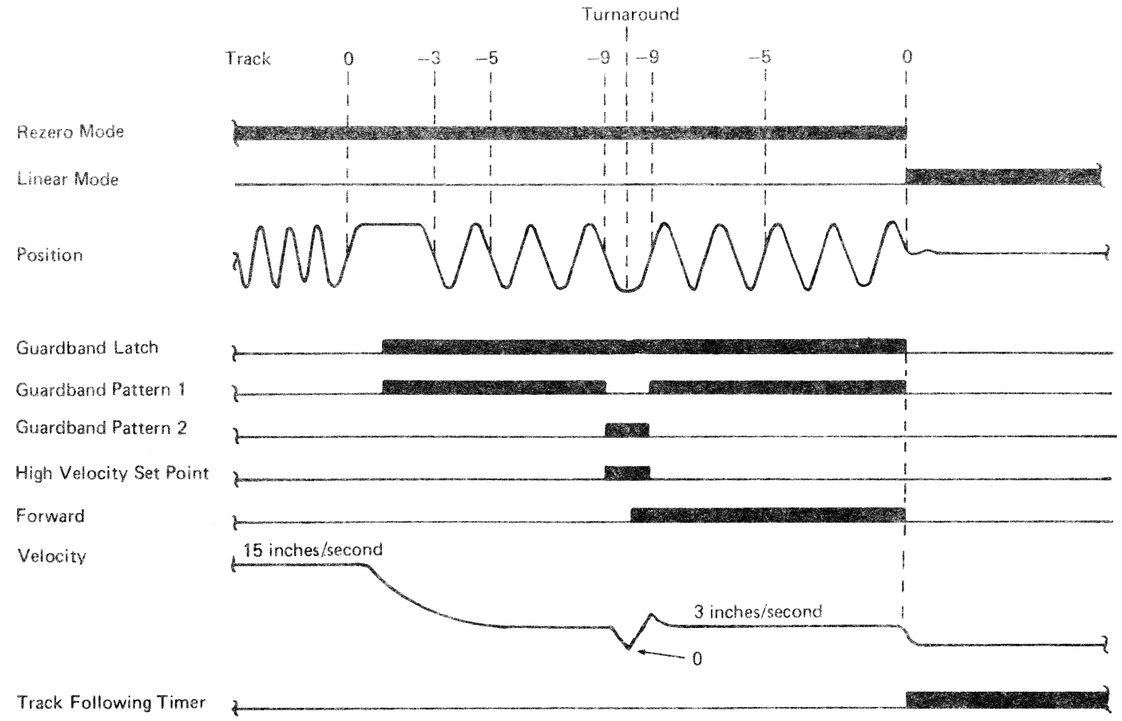
When the velocity generator receives the Guardband Latch signal, it sends End Accelerate to the velocity error detector 4.

End Accelerate controls the carriage speed by gating + Position to the velocity error detector. Carriage velocity decreases to 3 inches per second because of the decrease in voltage (from Position) into the velocity error detector.

The carriage continues at 3 inches per second until it reaches Guardband Pattern 2 near track −9. At Guardband Pattern 2 time, access control 12 sends High Velocity Set Point to the velocity error detector to stop the carriage.

Guardband Pattern 2 also feeds access control 1 and activates the Forward signal for Turn around.

The carriage moves forward toward track 0 at 3 inches per second. When the carriage nears track 0, the Guardband Latch becomes inactive. Rezero Mode and Forward become inactive at access control 1, and the carriage slows down to a stop and begins track following on track 0 in Linear Mode.



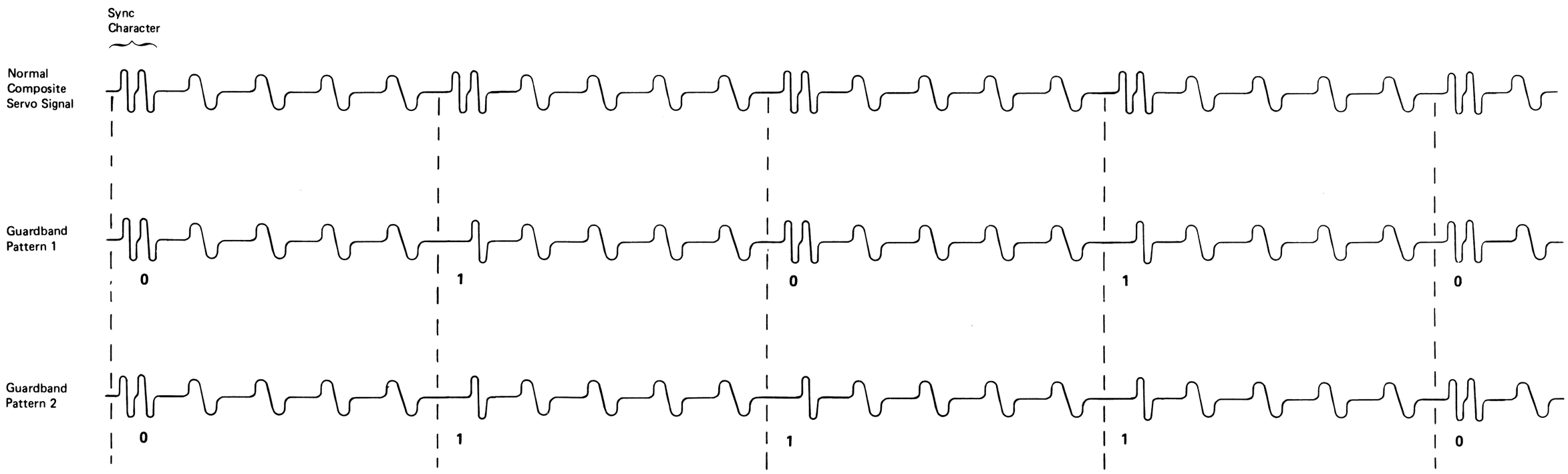
GUARDBAND PATTERN DETECTION

The guardband area is detected by the Index detection circuits in the same way that Index is detected. The Index detection circuits look at each sync character of the composite servo signal for Index bits. As mentioned on OPER 126, the Index detection circuits recognize an Index bit by the absence of the first half of a sync character. This absence is decoded as one bit. The correct sequence of one and zero bits is decoded as follows:

For Guardband Pattern 1 — 0-1-0-1-0

For Guardband Pattern 2 — 0-1-1-1-0

The Index detection circuit decoders are shown on ALD page KD520 (KS520).



SEEK OPERATION DESCRIPTION

The three most important steps of a Seek operation (OPER 108) are Select (Tag '83'), Set HAR (Tag '8B'), and Set Difference (Tag '8C').

SELECT

The controller and the drive must both be selected (Tag '83').

A 6-byte Seek address must be transferred from the channel to the storage control.

Tag Gate and Tag Bus must be latched to the drive.

SET HAR

Ctl Tag '8B' sets the Head Address Register (HAR). Tag bits 6 and 7 are routed through the controller to the device and shifted to Dev Tag Bus bits 1 and 2 (OPER 140 (A)).

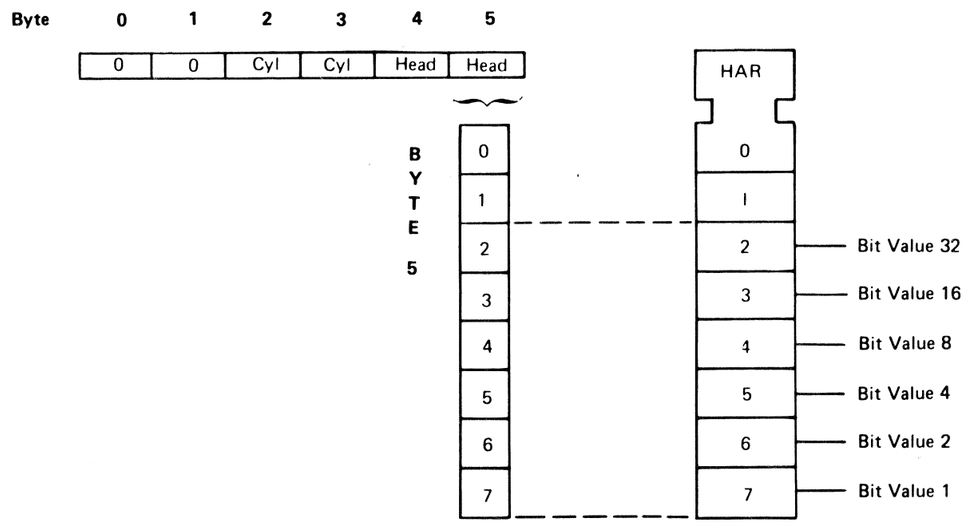
Bytes 2 and 3 of the Seek address specify the logical cylinder address and bits 3 through 7 of byte 5 specify the logical head address. (See Figure 1.) The head address is placed on Bus Out and is routed through the controller and shifted to Dev Bus Out to set the Head Address Register (OPER 140 (C)).

SET DIFFERENCE

Ctl Tag '8C' sets the Difference Counter (OPER 140 (B)). The Difference Counter is loaded with the difference between the current cylinder address and the desired cylinder address as calculated by the storage control.

The storage control sends a Seek Start (OPER 140 (D)) to the drive access control to start carriage movement (see OPER 141 and 142 for access operation during the seek).

Figure 1. Seek Address



Tag '8B'
Tag '8C'
DEV TAG BUS
Tag Gate
Bit 5
Bit 6
Bit 7
Bit 0
Bit 1
Bit 2
DCD
Set Diff Count
Set HAR
Control
A
B
1
Difference Counter
REG
0
1
2
3
4
5
6
7
SERVO
Velocity
Velocity Error
OUTBUS BUS
Three-bit Binary Decoder

Input	4	2	1	Output
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

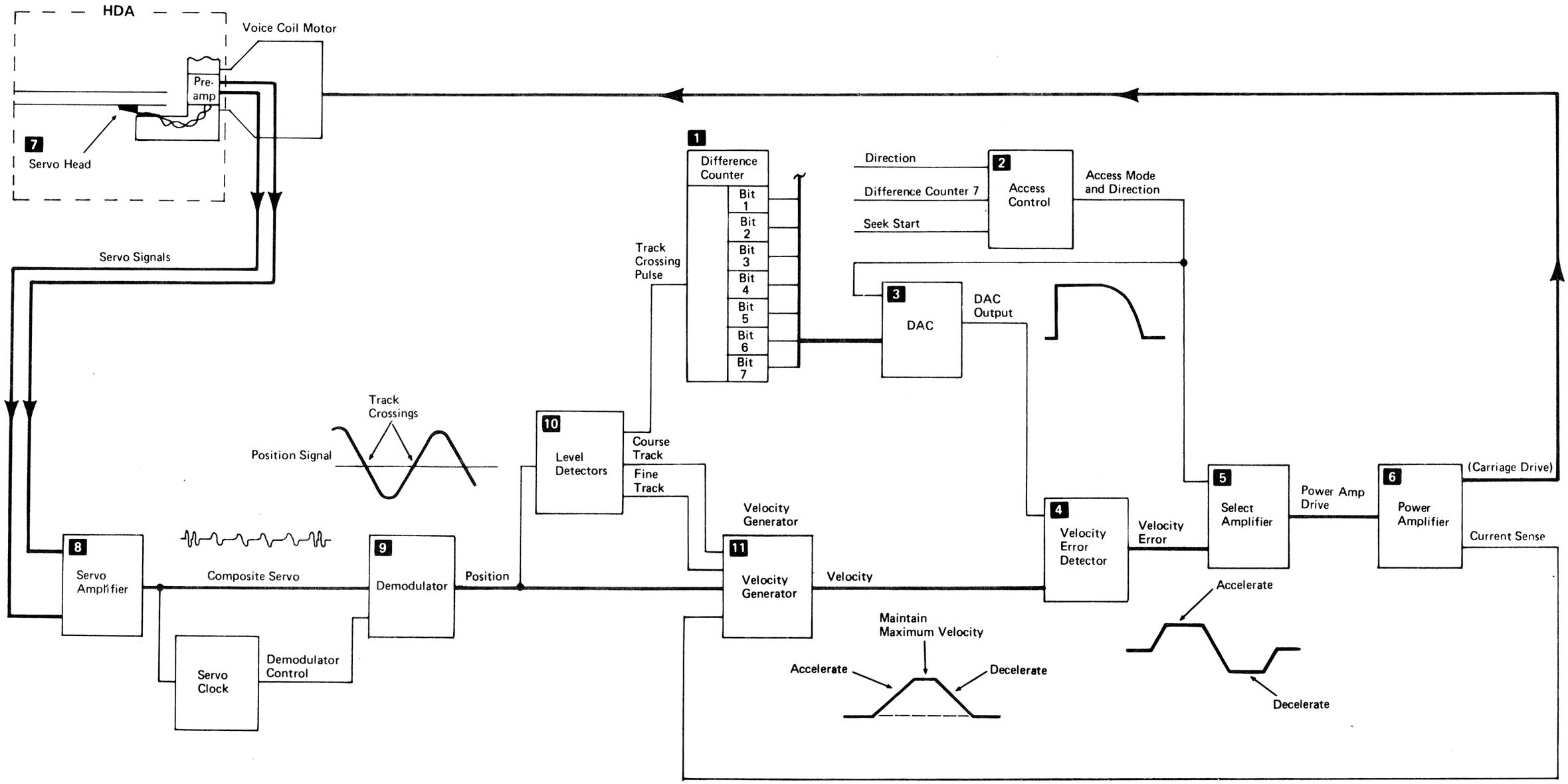
Two-bit Binary Decoder

Input	2	1	Output
	0	0	0
	0	1	1
	1	0	2
	1	1	3

HDA
Movable Head Chip Select
DCD
G
4
2
1
0
1
2
3
4
5
6
7
OR
N
Not FH (Movable Head)
Chip Select 0
Chip Select 1
Chip Select 2
Chip Select 3
Chip Select 4
Chip Select 5
Chip Select 6
Chip Select 7
To other Movable Head Select Modules (1 to each)
Fixed Heads 0–31 Chip Select (Model B2F)
DCD
Chip Select 8
Chip Select 9
Chip Select 10
Chip Select 11
Chip Select 12
Chip Select 13
Chip Select 14
Chip Select 15
To Fixed Head Select Modules 0–31 (1 to each)
Fixed Heads 32–59 Chip Select (Model B2F)
DCD
Chip Select 16
Chip Select 17
Chip Select 18
Chip Select 19
Chip Select 20
Chip Select 21
Chip Select 22
To Fixed Head Select Modules 32–59 (1 to each)
Head Select Modules
DCD
Head Select 0
Head Select 1
Head Select 2
Head Select 3
DCD
Head Select 4
Head Select 5
Head Select 6
Head Select 7
To Every Head Select Module
HAR
REG
0
1
2
3
4
5
6
7
FH Gate 2
FH Gate 1
Head Sel 2
Head Sel 1
C
1
DCD
Outbus Bit 4
Seek Start
D
HAR 7
Valid Odd Index
A
Active Track
OR
N
Valid Even Index
A

SEEK – FUNCTIONAL BLOCK DIAGRAM

See OPER 142 for a description of this diagram.

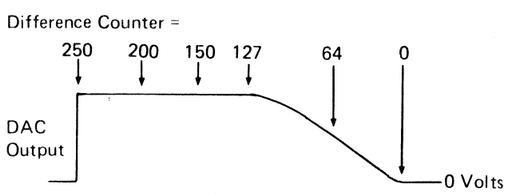


SEEK – DESCRIPTION OF BLOCK DIAGRAM

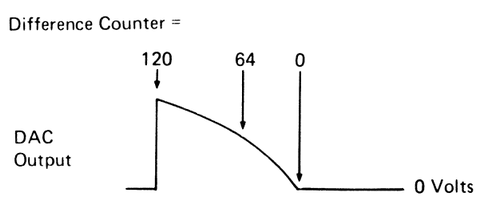
A Seek command causes the carriage to move from one physical track to another by first loading the difference between the current carriage address and the new carriage address into the difference counter. It then places the new head address and direction of the Seek (forward or reverse) in the Head Address Register (HAR). The carriage is moved the correct number of tracks to the new location and track follows on the new track.

The operation begins after the difference counter **1** is loaded and access control **2** sends Access Mode and the direction of the Seek to the servo circuits. This allows the Digital-to-Analog Converter (DAC) **3** to set the speed of the carriage.

If the difference counter has a value of 127 or above, the DAC output voltage is at its maximum point. During the Seek, as the difference counter decreases, the DAC output remains at maximum until the count reaches 127. At that time, the DAC output voltage begins to decrease proportionately to the value in the difference counter. As a result, if the difference counter is 250 at the start of a Seek, the DAC Output signal curve is as shown below:



If the Seek starts with a difference count of less than 127 (for example, 120), the curve is more like the following:



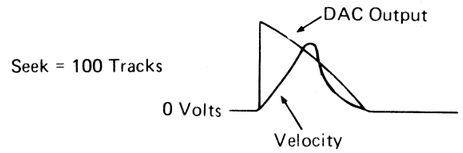
The output of the velocity error detector **4**, Velocity Error, is the sum of DAC Output and Velocity. Velocity Error feeds the select amplifier **5**, which feeds a voltage signal to the power amplifier **6** to drive the carriage toward the target track.

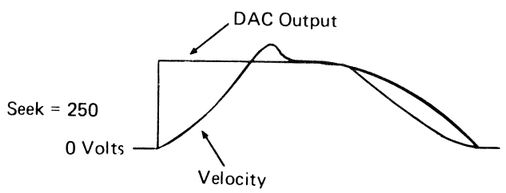
As the servo head **7** moves across the tracks, the servo signal is fed through the servo amplifier **8** to the demodulator **9** where the resulting output Position signal reflects the frequency of the track crossings.

The level detectors **10** use the Position signal to develop the Coarse Track and Fine Track signals, and from them, the Track Crossing Pulse. (See Figure 1 for the relationship of these signals to each other.)

The velocity generator **11** also uses the Position signal to determine the speed of the carriage and sends the Velocity signal to the velocity error detector.

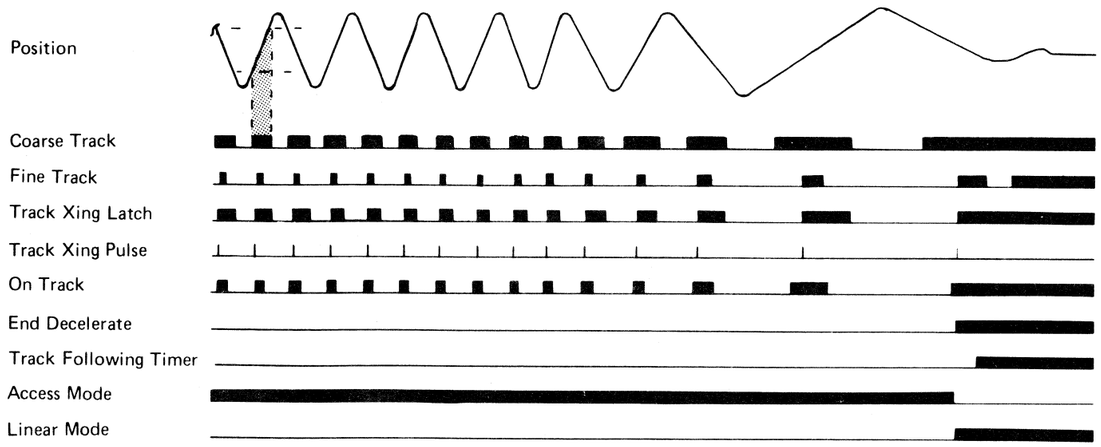
The velocity error detector takes DAC output and the Velocity signal, adds them algebraically, and produces Velocity Error. DAC output represents an ideal carriage velocity; Velocity is the actual velocity of the carriage. The figures below show the Velocity signal superimposed on the DAC output signal to show their relationship for two seeks of different length.





When the Velocity signal becomes greater than the DAC output, reverse current is applied to the Voice Coil Motor (VCM) to slow down the carriage. As the difference counter decreases, the carriage continues to slow down until the target track is reached. At that point, the carriage stops, access control goes to Linear Mode, and the servo system begins track following on the new track.

Figure 1.



SEARCH ID EQUAL

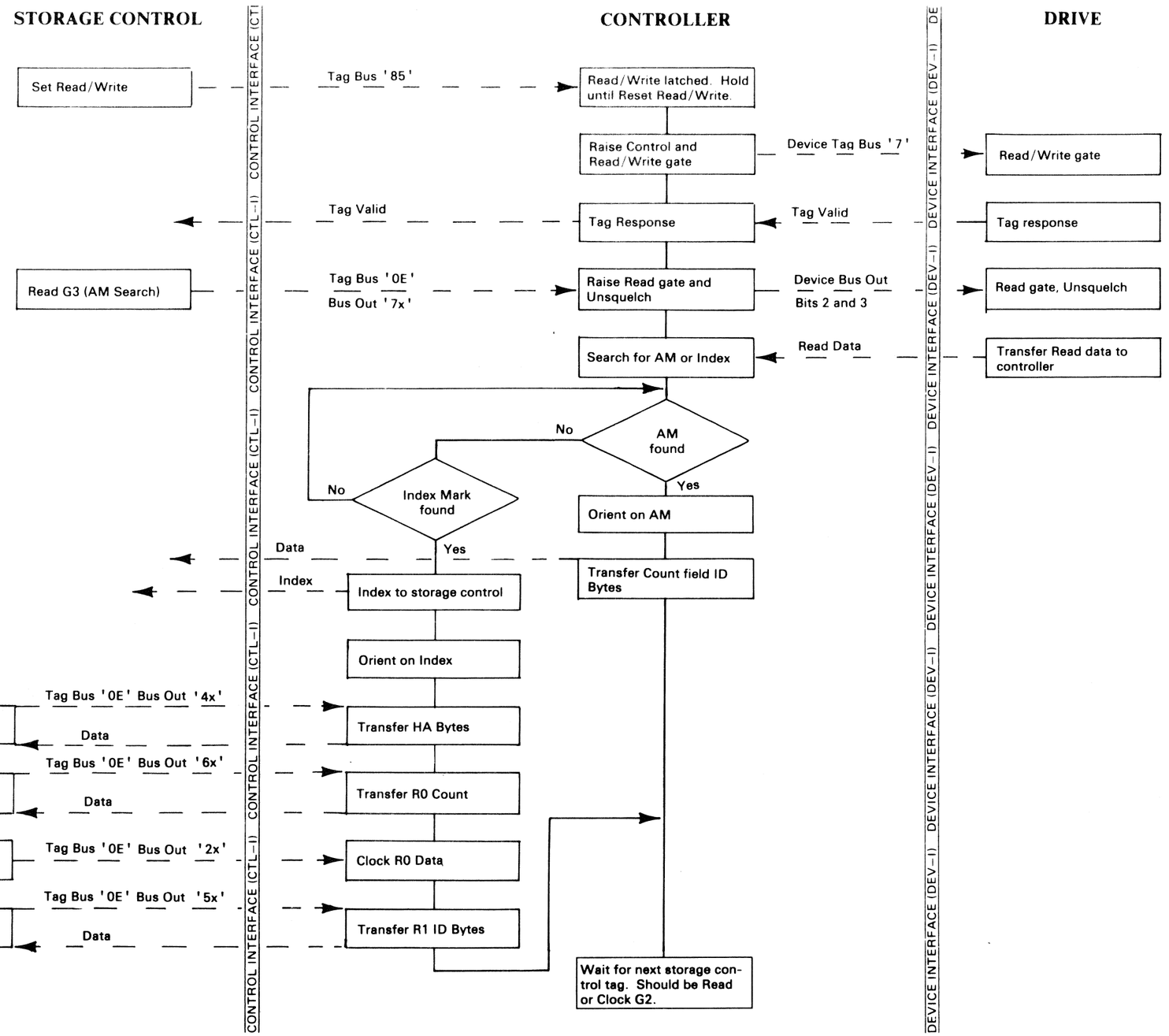
Storage control compares data from the system with data read from the HDA (the ID bytes for Search HA or Search ID; Key field bytes for Search Key).

Only one record is operated on for each Search command.

When the search is unsuccessful, the channel must reissue the Channel Command Word (CCW). This is done by the use of a Transfer In Channel (TIC) back to the Search command.

When the search is successful, the Status Modifier bit in the Channel Status Word (CSW) is set On. This causes the channel to skip the next CCW (TIC) in the chain.

When Index is sensed during an AM search, this sequence of operations is performed to maintain orientation and read the R1 Count field. If the second active Index is sensed before the search is successful, No Record Found is set. (See OPER 208.)



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ROTATIONAL POSITION SENSING

Rotational Position Sensing (RPS) reduces the channel time consumed by disk rotation during Search operations. The channel time consumed is reduced by the drive releasing the channel to perform other operations until just before the record is reached. The drive reconnects to the channel when the Target Register and the Sector Counter are equal (compare equal).

The Sector Counter counts from 0 (at Index) to 127. The Sector Counter runs continuously while the drive is track following. Sector Count pulses are derived from the servo clock. The Sector Clock Counter (see OPER 204) accepts 39 sector count pulses before advancing the Sector Counter one count. After the Sector Counter reaches 127, the Valid Index 1 pulse resets the Sector Counter for the next revolution.

The Target Register performs two functions:

1. It is loaded at the beginning of all Read, Write, and Search CCWs by a Set Sector command. The sector number is fetched from main storage.
2. It holds the starting sector location of the record to be read or written. It temporarily stores the beginning sector count transferred from the Sector Counter.

After the Target Register is loaded during a Search operation, its value can be moved over the channel to main storage by a Read Sector command. The storage location of the sector number is determined by the individual customer program.

An example of an RPS application (Figure 1), is Read Verification (read-back check). The sequence of channel commands or functions is:

1. Seek
2. Search ID
3. TIC*-8
4. Write Data
5. Read Sector
6. Set Sector
7. Disconnect (Function)
8. Search ID
9. TIC*-8
10. Read Data

Seek

Moves the carriage to the desired track and selects the head.

Search ID

Finds the record to be written and transfers the sector number from the Sector Counter to the Target Register at 2

TIC*-8

Loops until the desired ID is located.

Write Data

Transfers data from main storage to the disk record at 3

Read Sector

Moves the sector number from the Target Register at 4 to main storage.

Set Sector

- Moves the sector number from main storage to the Target Register at 5 . The Target Register has the correct sector number but comparison is required three sectors earlier to ensure channel reconnection.
- The number three is subtracted from the sector number in the storage control before it is loaded into the Target Register.

Disconnect

The Disconnect function releases the channel at 6 to perform other operations.

Search ID

Search ID is a short search from 1 to 2.

TIC*-8

Loops until ID is located.

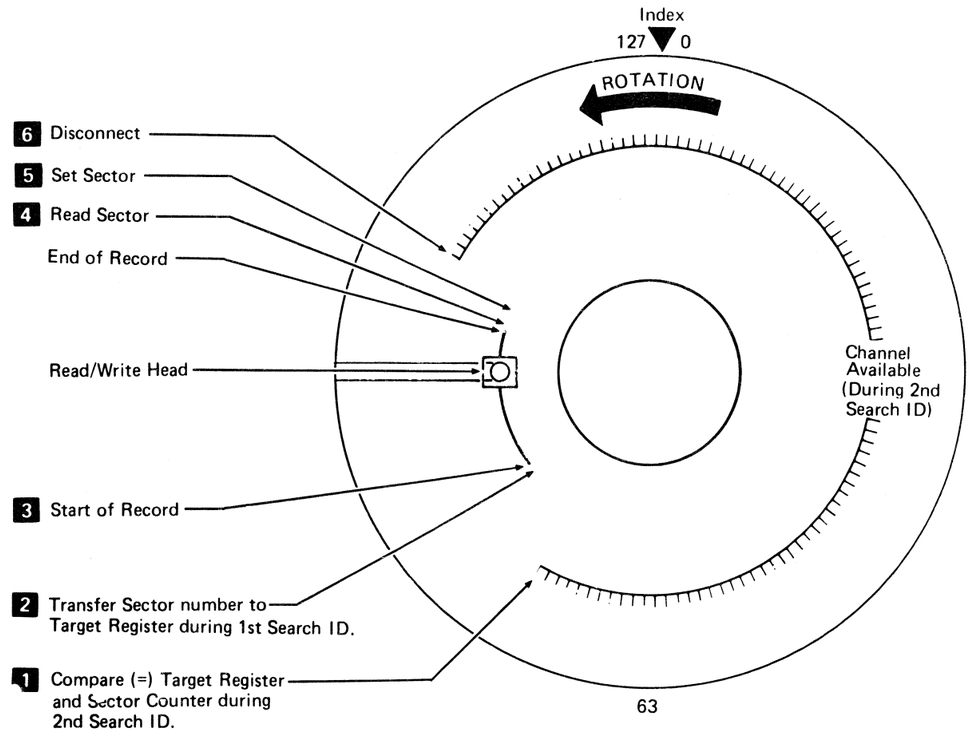
Read Data

The data written earlier at 3 is now read into main storage for comparison with the original data.

If all records were of fixed length, the sector number could be calculated for each record to be written. With RPS, the search before writing could release the channel and reconnect when the Target Register and Sector Counter are compared.

OPER 204 and 205 contain more details on Rotational Position Sensing.

Figure 1. Read Verification with RPS



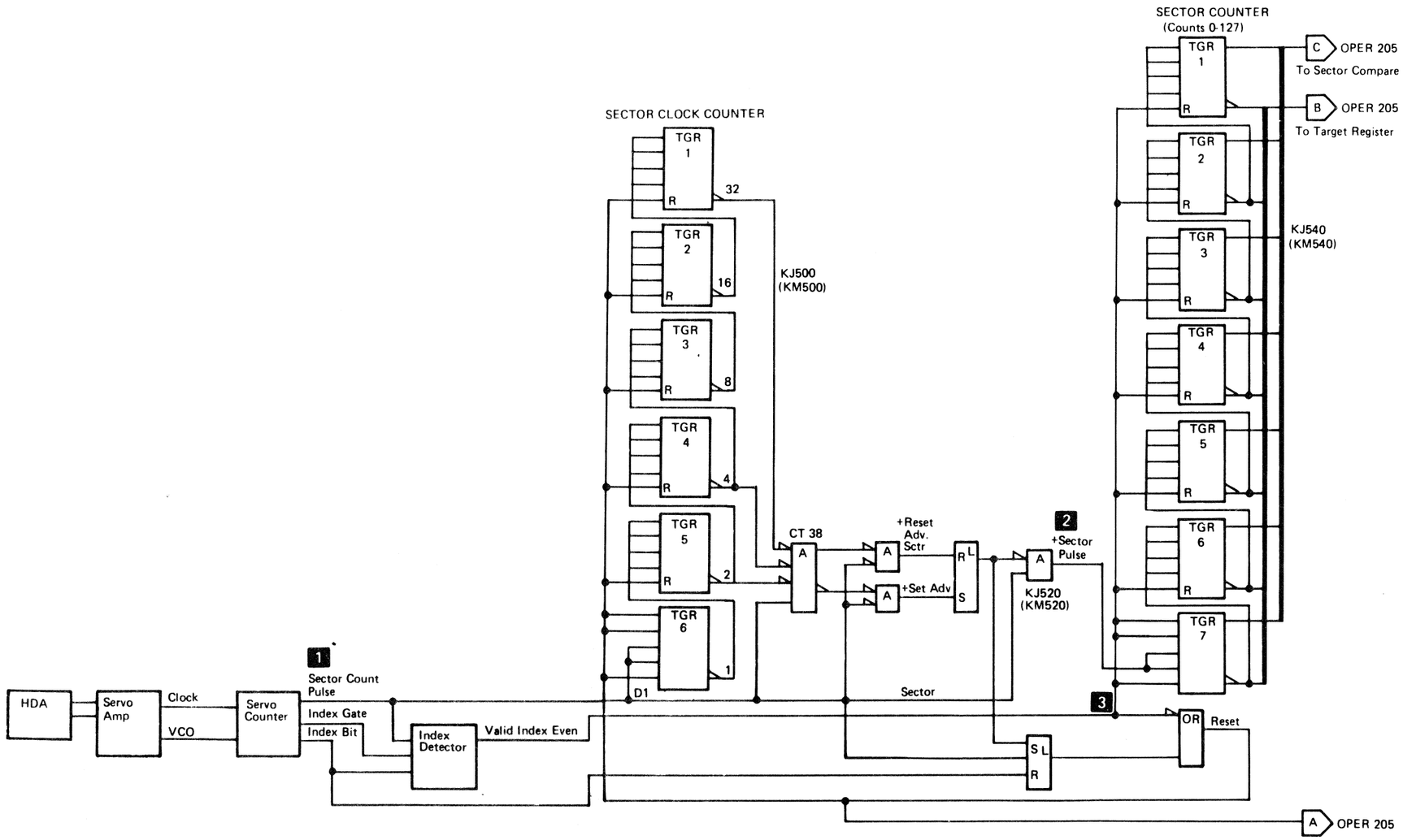
RPS – SEARCH SECTOR OPERATION

Functional characteristics of the Search Sector operation are:

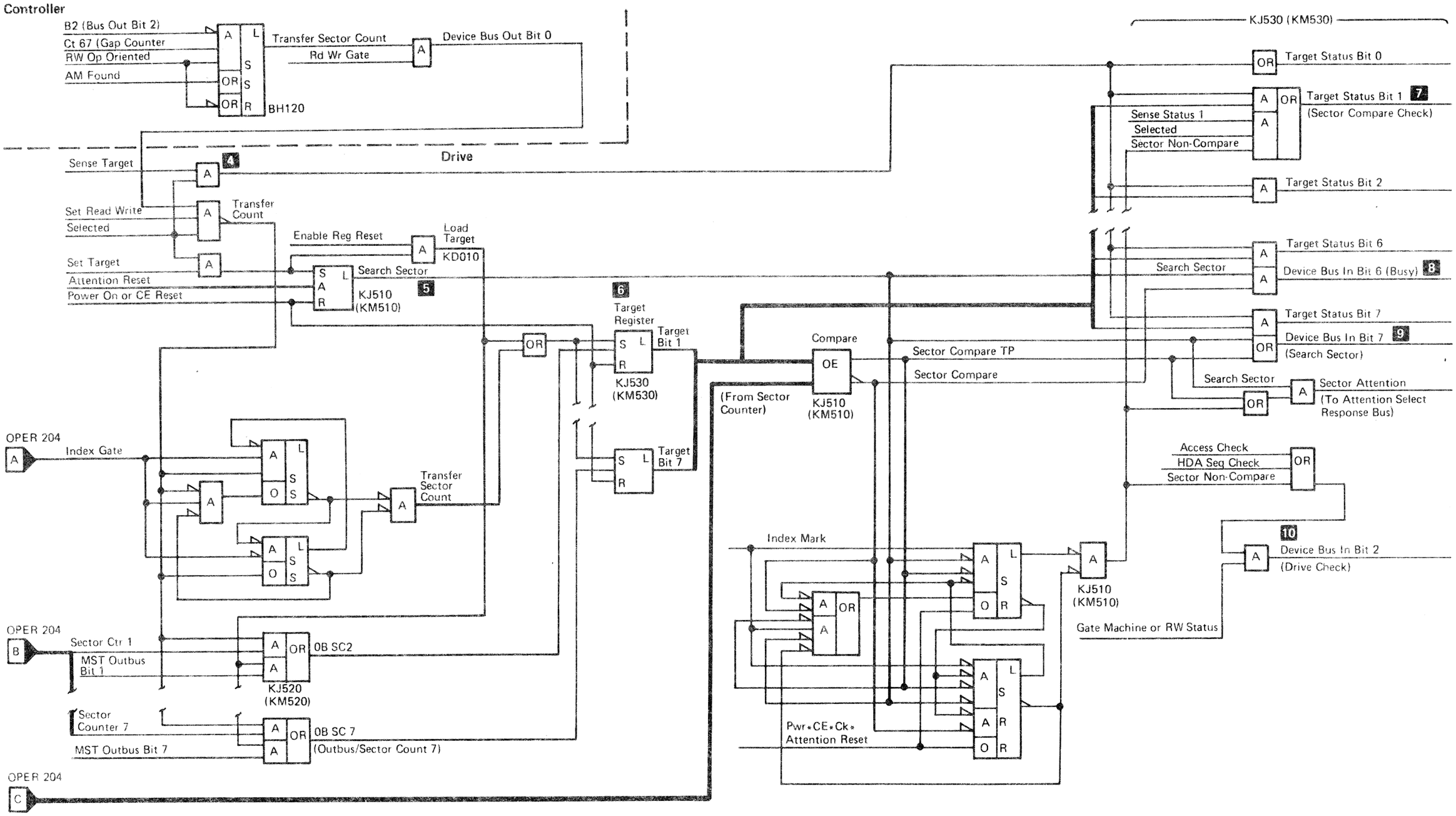
- One sector count pulse for each servo byte **1** .
- 4992 sector count pulses for a full track.
- 128 sectors for each track (0 to 127).
- 39 sector count pulses for each sector (38 clock counter pulses plus next sector count pulse) **2** .
- Sector duration is 124 to 136 microseconds.
- Sector Counter resets at Valid Even Index while the drive is track following **3** .

OPERATION

- The value in the Target Register is set with a Set Target Command which also starts a Search Sector Operation (OPER 205 **6** and **9**).
- When the sector count is equal to the value in the Target Register, a Sector Compare occurs for 124 to 136 microseconds. Attention is also active for that sector time.
- Device Bus In bit 7 **9** is active during the Search Sector operation.
- A Sector Compare occurs each revolution until Attention Reset resets Search Sector (OPER 205 **5**).
- Device Bus In bit 6 (Busy) is active during the Search Sector operation except during the sector in which the compare is equal (OPER 205 **8**).
- Sector Compare Check occurs if a Sector Compare does not take place in two revolutions. Drive Check is set (OPER 205 **7** and **10**).
- The controller issues Transfer Sector Count to the drive before all G1 and G3 Read and Write tags at count 67 time and on Search commands when an Address Mark is found.
- A Sense Target command then sends the value of the sector count to Device Bus In (OPER 205 **4**).



RPS – SEARCH SECTOR OPERATION



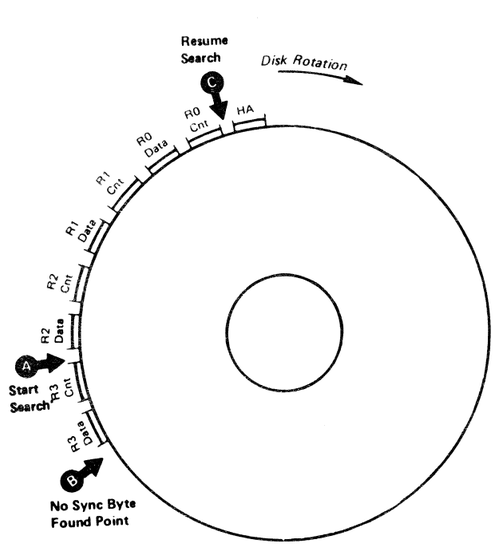
NO RECORD FOUND

A No Record Found condition exists when Index has been passed twice in the same non-multitrack search and TIC loop. When the No Record Found condition is detected, the storage control posts a unit check with No Record Found indicated in Sense Byte 1 bit 4.

To illustrate the No Record Found operation, assume the track is formatted as shown below and the following command chain has been issued:

Seek
Search ID Equal Record 5
TIC-8 (Transfer In Channel To The Previous CCW)
Read Count, Key, Data

When a non-multitrack search and TIC are successive commands in a command chain, the loop continues until either the search is successful or until Index has been passed twice.



If the Search is started at A, the operation becomes oriented on the Address Mark in the gap prior to the record 3 Count area. The record 3 Count area (record 3) is read and compared against the search argument (record 5) and a non-compare results. The TIC-8 causes the Search command to be reissued.

There are no fields after record 3; therefore, no sync byte is found at B. Because no sync byte is found, the storage control suspends the search at B until Index is encountered.

After Index is passed, the storage control reads and clocks the Home Address area and saves certain information. This operation is transparent to the command chain.

The Search command, which was suspended at B, is resumed at C beginning with Record 0 Count area. As before, a non-compare results and a TIC-8 occurs.

The Search command is reissued for record 1, record 2, and record 3 with non-compare results. Then, the Search command is issued for the last time. As before, the search is suspended at B, because no sync byte is found.

When the Index is encountered again, the storage control signals a unit check, which breaks the command chain to terminate the operation.

Sense information is formatted with Byte 1 bit 4 set to 1 to indicate No Record Found.

The Index counter is reset whenever a Read Data, Read Home Address, or any Write Sense or Control command is issued after a successful search. This allows each separate search loop to search past Index twice before posting No Record Found.

SET AND RESET READ/WRITE—TAGS '85' AND '05'

This page describes the diagram on OPER 211.

SET READ/WRITE – Tag '85'

Set Read/Write – Tag '85' is an extended operation. (See OPER 95 for an explanation of an extended operation.) Tag '85' conditions the controller and the drive for data transfer operations (Read or Write operations) in the following way. Set Read/Write:

- Sets the Read/Write latch 1
- Activates G2 (gate 2) on the Device Tag Reg 2 causing tag bits 0, 1, and 2 to be sent to the device (drive).
- Activates Device Tag Gate 3 .
- Activates Rd/Wr Gate 4 which activates G2 (gate 2) of the Bus Out Selector 6 . This deconditions the normal bus out bits (from storage control) and allows the Device Bus Out to carry read/write control information to the drive (from controller hardware). Device Outbus bits 5, 6, and 7 are held active by the Rd Wrt Gate. The other Outbus bits are manipulated by controller hardware 5 to control the data transfer. The device checks the condition of Bus Out ('07') after the Set Read/Write Op is issued, prior to the data transfer.
- Places the device in Control mode 7 .
- Activates Set Rd*Wr 8 in the device. This is a result of Control mode and MST Outbus bits 5, 6, and 7 being active. The Set Rd*Wr line:
  1. Blocks normal device Bus Out Parity Error detection.
  2. Gates machine read/write status to Device Bus In 9 . (See OPER 100 for Device Bus In under Tag '85'.)
  3. Activates Set Rd*Wr Safe if no R/W Check conditions exist 10 .
  4. Provides a path for the Read/Write control lines to the Read Detector card of the selected drive 12 and 13 .
  5. Causes a Read/Write head to be selected in accordance with the value in HAR 15 . (HAR was set during the Seek, Tag '8B', that preceded this tag. See OPER 139 and 140.)
  6. Allows monitoring the Read/Write control lines for proper sequence 11 .
  7. Establishes a data path between the controller and the selected drive 14 .
- Enables the following functions of the data transfer control hardware 5 :
  1. Index processing.
  2. Gap counter control.
  3. Function Pulse generation.
  4. Synchronization of VFO with the controller and Servo pulses on the servo track of the HDA.
  5. Orientation (must be established between microprogram and disk rotational position for most operations).
- Signals the microprogram (with Normal End) that the controller and the device are conditioned to receive a data transfer tag. A data transfer tag is either '0E' for a Read operation or '0F' for a Write operation.

RESET READ/WRITE – Tag '05'

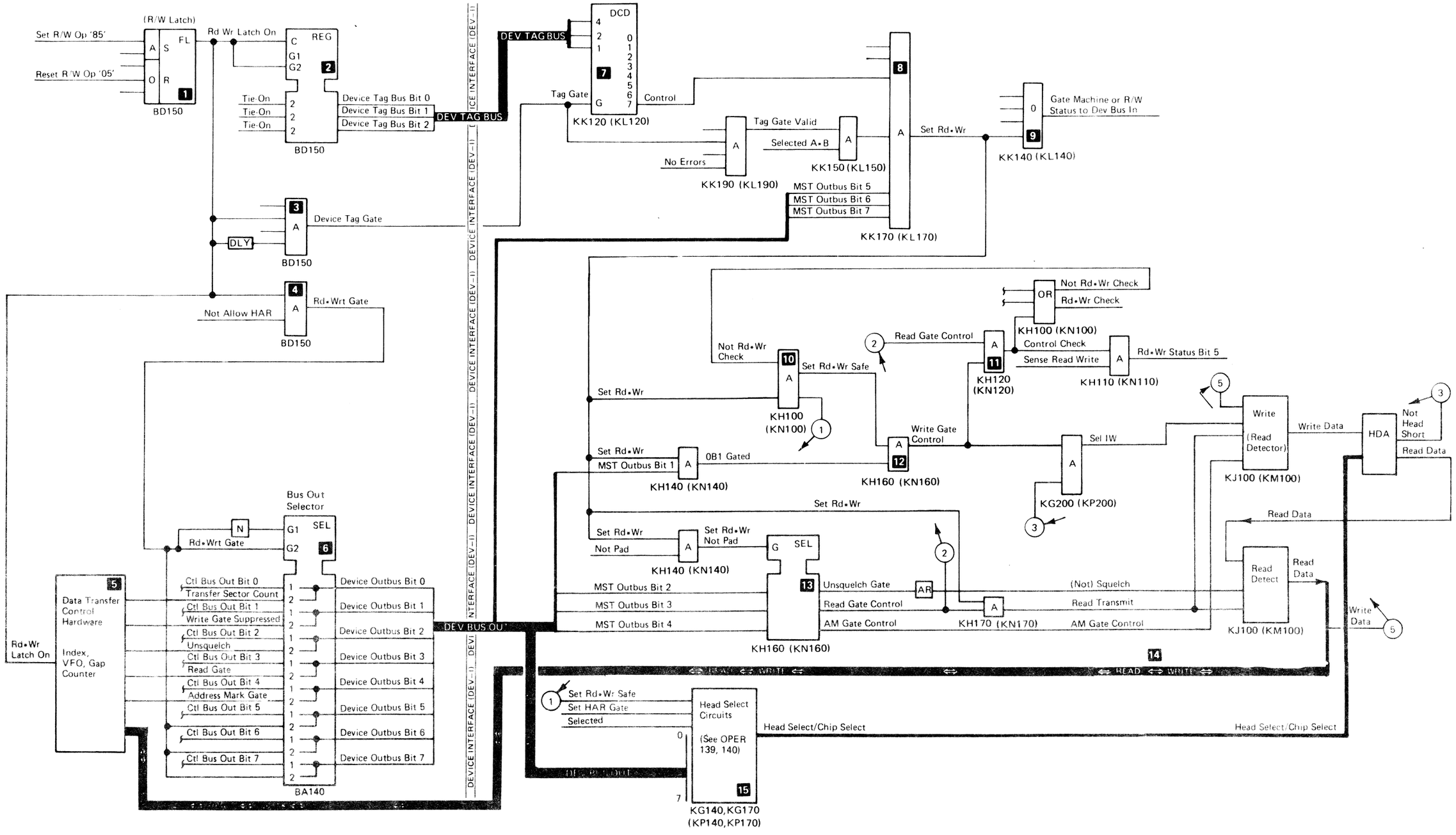
Reset Read/Write – Tag '05' is an immediate operation (see OPER 95 for an explanation of an immediate operation). Tag '05' resets the controller and device hardware that was set by Tag '85' after Read or Write Tags (Tags '0E' and '0F') have been completed.

To have a complete data transfer operation, the sequence of tags should be:

1. Set Read/Write – Tag '85'
2. Data Transfer
   Tag '0E' for Read
   Tag '0F' for Write
3. Reset Read/Write – Tag '05'

Reset Read/Write – Tag '05':

- Resets the Read/Write Latch 1 .
- Deactivates Device Tag Gate 3 , which removes the device from control mode, disabling the device Read/Write hardware.
- Restores data transfer control hardware functions 5 to non-data transfer condition:
  1. Allows bit ring 0 time pulse to reset the gap counter and control the function pulse.
  2. Disables Index processing.
  3. Disables VFO synchronization.
  4. Disables Orientation.
- Returns control of Device Bus Out to the storage control 6 .
- Resets conditions set up during a Read (Tag '0E') or Write (Tag '0F') operation.
- Signals the microprogram with Normal End.



WRITE — TAG '0F'

When the Write command is sent by the CPU to storage control, storage control (the microprogram) issues the appropriate chain of tags to the controller to carry out the Write command.

Note: *So that the R/W head can start from a known reference point on the track, the first tag operation in the chain is the one that establishes orientation: Format G1, Special Format G1, Read G1, or Read G3 AM Search.*

TYPES OF WRITE OPERATIONS

See OPER 99 and OPER 104 – Tag '0F', Bus Out bits 0 to 3 for the type of Write operation on Bus Out.

See OPER 33 and OPER 34 – for track format and gap-to-data-area relationships.

Write G2 (Bus Out = '2x')

Write G2 functions as follows:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the Key area, Data area, or Record 0 (R0) Count area.
- Turns off Write Gate at the end of the written area (after the ECC bytes have been written).

Format Reorient (Bus Out = '3x')

Format Reorient is initiated when a Count area indicates a skipped defect within its control.

Format Reorient functions as follows:

- Begins its operation in the gap immediately following the Count area.
- Reorients to the last byte before the ECC bytes of the preceding Data area.
- Turns off the Write Gate at Index time. (Write Gate is under the control of the Format latch at this time. The Format latch was set by the Format G3 operation that preceded the Format Reorient operation.)

Format G1 (Bus Out = '4x')

Format G1 functions as follows:

- Sets up the Write operation.
- **Orients** on Index and Active Track.
- Writes a Gap 1.
- Writes the sync byte ('19') at the end of Gap 1.
- Writes the Home Address (HA).
- Causes padding after the last Write operation in the tag chain until Index is detected.

Format G3 (Bus Out = '5x')

Format G3 functions as follows:

- Sets up the Write operation during Gap 3 time.
- Writes the AM (Address Mark) in the gap.
- Writes the sync byte ('19') at the end of Gap 3.
- Writes the Count area.
- Keeps Write Gate on at the end of the Count area until Index is detected.

Format G2 (Bus Out = '6x')

Format G2 functions as follows:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the Key area, Data area, or the Record 0 (R0) Count area.
- Causes padding after the last Write operation in the tag chain until Index is detected.

Format/Erase (Bus Out = '7x')

Format/Erase functions as follows:

- Writes zeros to Index

Write G4 (Bus Out = 'Bx')

Write G4 is used to skip a track defect during a Write operation in one of two ways:

1. Extends a normal gap (G1, G2, or G3) by adding a Gap 4 **before** the normal gap. (Gap 4 = 128 bytes, see OPER 33.)
2. Splits an area that contains a defect:
   - Sets up the Write operation during Gap 4 time.
   - Writes the second segment of a Key area or Data area.

Special Format G1 (Bus Out = 'Cx')

Special Format G1 functions as follows:

- Sets up the Write operation.
- **Orients** on Index and Active Track.
- Writes 128 bytes of zeros, followed by the normal Gap 1 to skip a defect.
- Writes the sync byte ('19') at the end of Gap 1.
- Writes the Home Address (HA).
- Causes padding after the last Write operation in the tag chain until Index is detected.

Special Write G2 (Bus Out = 'Ex')

Special Write G2:

- Sets up the Write operation during Gap 2 time.
- Writes the sync byte ('19') at the end of Gap 2.
- Writes the first segment of a Key area or Data area.
- Inhibits writing ECC bytes following the first segment.
- Is followed by a Write G4 to write the final segment and the ECC bytes.

DESCRIPTION OF A WRITE OPERATION

See the diagram on OPER 226.

Prerequisites

The microprogram prerequisites for a Write operation are as follows:

- The Controller and the drive must both be selected (Tag '83').
- Set Read/Write (Tag '85') must be latched.
- Tag Gate and Tag Bus must be latched to the drive.
- VFO must be locked in.
- Orientation must be established.

Sequence of Operation

1. Write command '0F' is placed on the Ctl Tag Bus **1**.

   Ctl Bus Out contains a modifier that specifies the type of Write command and the pre-field gap **2**.

Bus Out Bit Modifier	0	1	2	3	Command
	0	0	1	0	Write G2
	0	0	1	1	Format Reorient
	0	1	0	0	Format G1
	0	1	0	1	Format G3
	0	1	1	0	Format G2
	0	1	1	1	Format/Erase
	1	0	1	1	Write G4
	1	1	0	0	Special Format G1
	1	1	1	0	Special Write G2

2. Write Gate is set **7**.
3. Write Mode is set **3**.
4. Write Mode enables generation of Sync In **4**, which indicates that the controller is ready to accept the first byte of data on Bus Out (Sync Byte '19').
5. Sync Out and the first byte of write data are transferred **5**.
6. Data on Bus Out is sent to the Data Register **6** and serialized by SERDES **9** for recording on the disk surface. The controller is now in the data transfer mode.
7. The controller continues to transfer data until End Data is detected. The path between the ECC shift register **8** and the SERDES shift register **9** is enabled. Six bytes of ECC are transferred from the ECC shift register, through the SERDES shift register, and recorded at the end of the Data field.
8. After End Data is detected, the controller resets the Write Op latch and activates Normal End to the user if there are no check conditions. The user answers with End Response.

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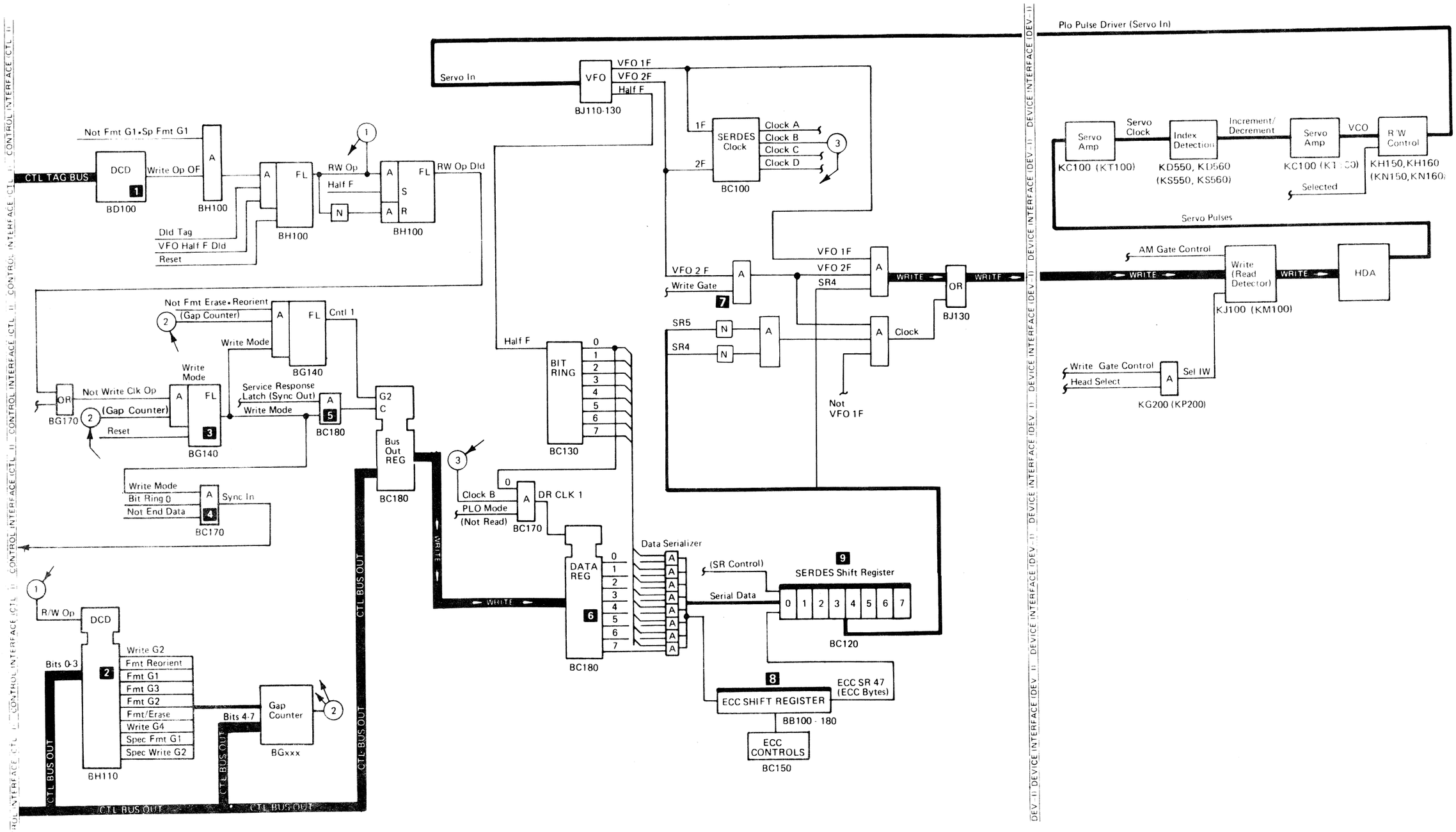
WRITE—TAG '0F'



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When a Read command is sent by the CPU to storage control, storage control (the microprogram) issues the appropriate tags to the controller to carry out the Read operation. For example, the appropriate chain of tags for a Read Data command ('06') might be:

1. Read G3,Tag '0E', Bus '5x'
2. Clock G2,Tag '0E', Bus '2x'
3. Read G2,Tag '0E', Bus '6x'

Note that the tag chain must always begin with either a Read G1 or a Read G3 AM Search for track orientation, so the read head can start reading from a known reference point.

TYPES OF READ OPERATIONS

These operations are defined by bits 0 through 3 of Bus Out during Tag '0E'. See OPER 99 and OPER 103.

See also: Track Format on OPER 33 and 34 for gap-to-read area relationships.

Clock G3 (Bus Out = '1x')

Clock G3 functions as follows:

- Sets up the operation during Gap 3.
- Clocks over the Count area that follows the gap, while maintaining track orientation.

Clock G2 (Bus Out = '2x')

Clock G2 functions as follows:

- Sets up the operation during Gap 2.
- Clocks over the Key or Data area that follows the gap, while maintaining track orientation.

Read G4 (Bus Out = '3x')

Read G4 functions in one of two ways.

1. For reading a moved field:
   - Clocks over the 128-byte gap for a skipped defect.
   - Is followed by a normal Read G2 to read the next area on the track.
2. For reading the second part of a split area after a Special Read G2:
   - Sets up the operation during Gap 4.
   - Reads the second part of the Key or Data area that has been split for defect skipping.

Read G1 (Bus Out = '4x')

Read G1 functions as follows:

- **Orients** on Index and Active Track.
- Sets up the Read operation during Gap 1.
- Reads the Home Address area.

Read G3 (Bus Out = '5x')

Read G3 functions as follows:

- Sets up the Read operation during Gap 3.
- Reads the Count area (except R0 Count area).

Read G2 (Bus Out = '6x')

Read G2 functions as follows:

- Sets up the Read operation during Gap 2.
- Reads the Key area, Data area, or the R0 Count area.

Read G3 AM Search (Bus Out = '7x')

Read G3 AM Search functions as follows:

- Sets up the Read operation.
- **Orients** on the Address Mark (AM) in Gap 3. **(Note:** If Index is detected before the Address Mark, No AM Found is posted and the microprogram orients on Index and issues a Read G1.)
- Reads the Count area that follows the Gap (except R0 Count area).

Special Read G2 (Bus Out = 'Ex')

Special Read G2 functions as follows:

- Sets up the Read operation
- Reads the first part of the Key or Data area that has been split for defect skipping.
- Saves the ECC shift register contents at the end of the data transfer.

DESCRIPTION OF A READ OPERATION (Read G1)

See the diagram on OPER 231 and the timing chart on OPER 232.

Sequence of Operation

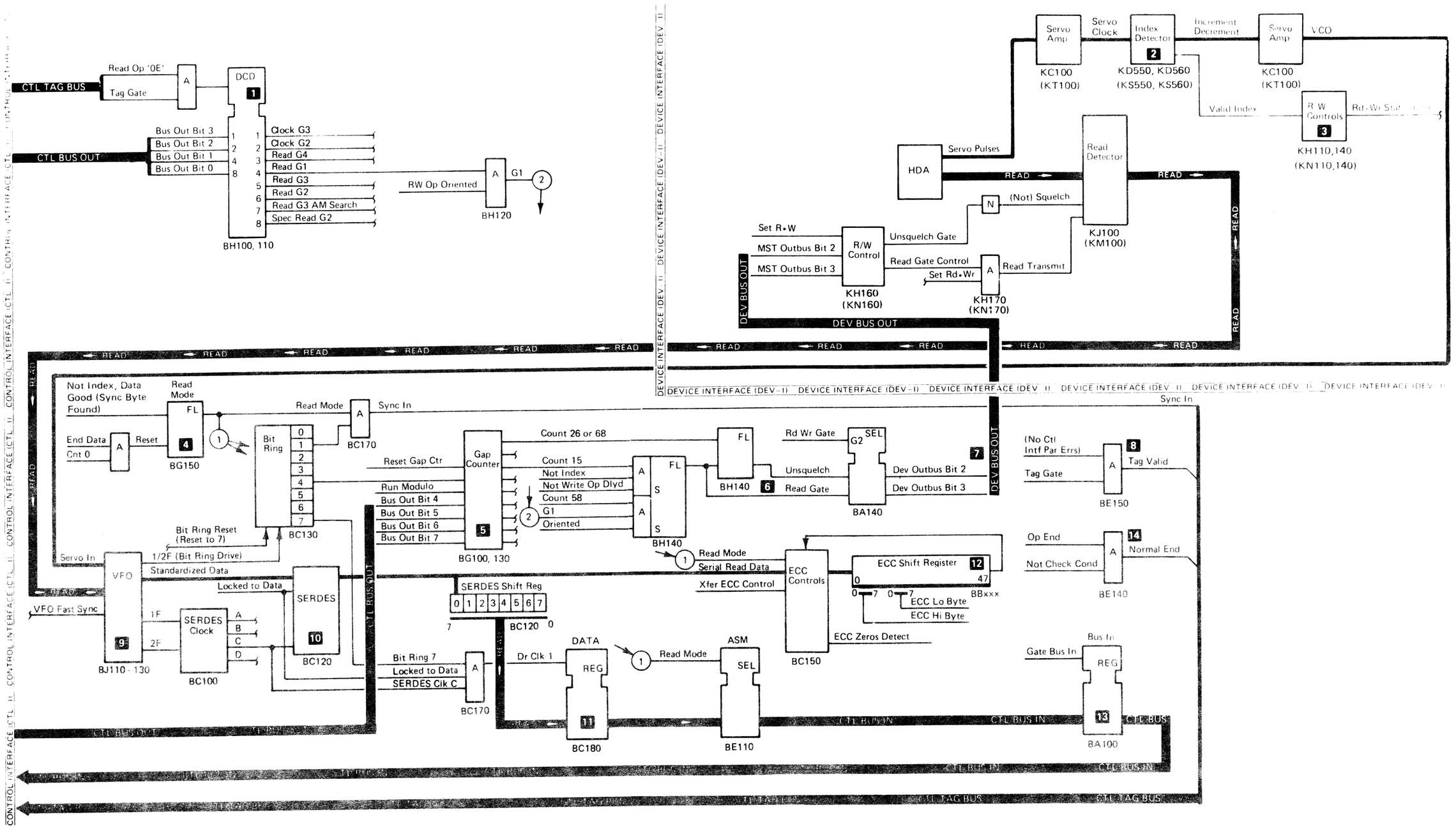
1. Read Op Tag '0E' is placed on Ctl Tag Bus. Ctl Bus Out contains a modifier in bits 0 through 3 that specifies the Read G1 operation (0100) 1. Ctl Bus Out bits 4 through 7 contain the modulo count (units digit of the hex byte count) and are latched for future use by the gap counter 5. For a Read G1, the modulo count is always 9.
2. Tag Valid 8 is returned to the storage control if there are no control interface errors.
3. At Index time, orientation is established 2 and the gap counter is reset. The gap counter starts counting and at count-58 time, Read Gate is raised to the drive 6. At count-68 time, Unsquelch is raised to the drive 6. Device Bus Out bits 2 and 3 are used to transfer these controls to the selected drive 7. These controls are necessary to amplify and transfer read data from the selected drive to the controller 3.
4. Count 92 resets the gap counter.
5. Count 1 time locks VFO to data and activates VFO Fast Sync 9.
6. Count 8 resets VFO Fast Sync and gates Standardized Data to SERDES 10.
7. When a sync byte is detected in SERDES, Data Good causes Read Mode to become active 4. The gap counter is set to the 15s complement of the modulo count. For a Read G1, the complemented modulo count is 6.

   Bit ring 7 transfers the sync byte from SERDES to the data register 11.

   During the next complete bit ring cycle the first data byte is assembled in SERDES. At bit ring 1 time of that cycle, Sync In is sent to the storage control and the sync byte is placed on Ctl Bus In 13.
8. At the next bit ring 4 time, the gap counter is stepped to 7.
9. Bit ring 7 transfers the first data byte to the data register. Bit ring 1 of the next bit ring cycle activates Sync In to the storage control with the data byte on Ctl Bus In. Bit ring 4 increments the gap counter to 8. The next data byte is being assembled in SERDES and is ready to be transferred to the data register at bit ring 7 time.
10. **Data transfer continues until the gap counter reaches 15. Read mode is reset and prevents any further data transfer** 4.

    Count 15 also activates Transfer ECC Control to allow the next byte (first ECC byte) to be gated to the ECC Shift Register 12.
11. The six ECC bytes are transferred to the ECC shift register. If ECC Zeros Compare is active after the six ECC bytes are transferred, ECC Data Check is blocked.
12. Op End is activated and Normal End is sent to the storage control provided no errors have occurred 14.
13. End Response is returned from the storage control and Reset End condition is activated in the controller.

READ — TAG '0E'



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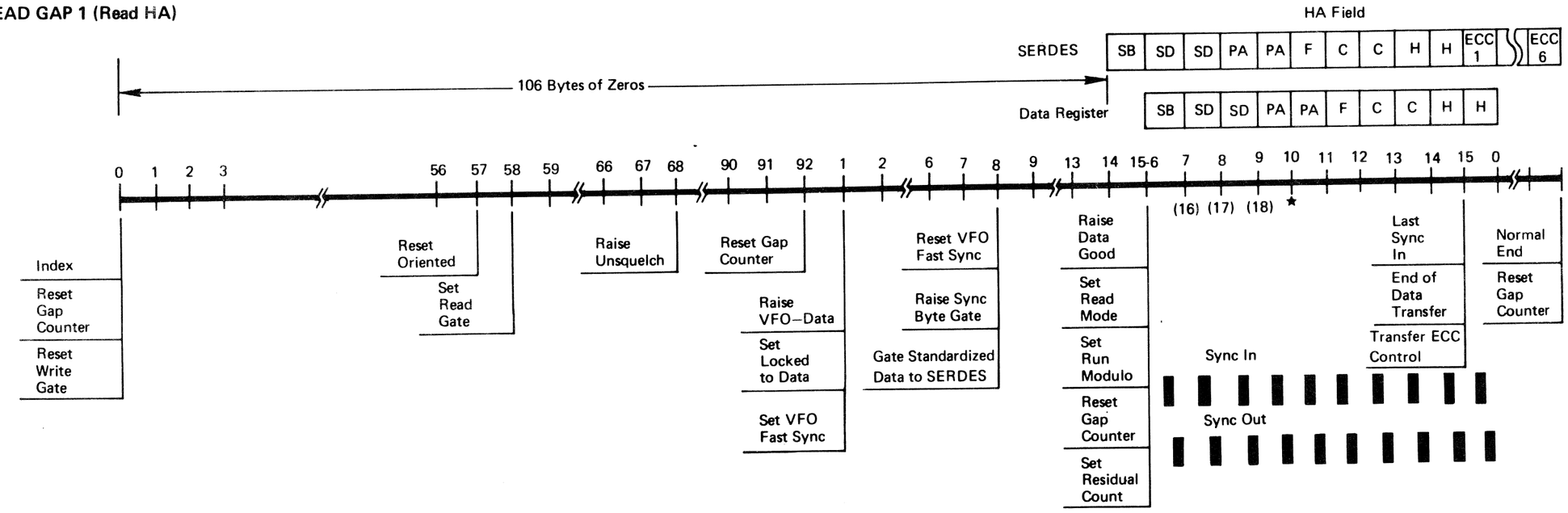
READ G1/G2 TIMING REFERENCE

READ GAP 1 (Read HA)



Legend

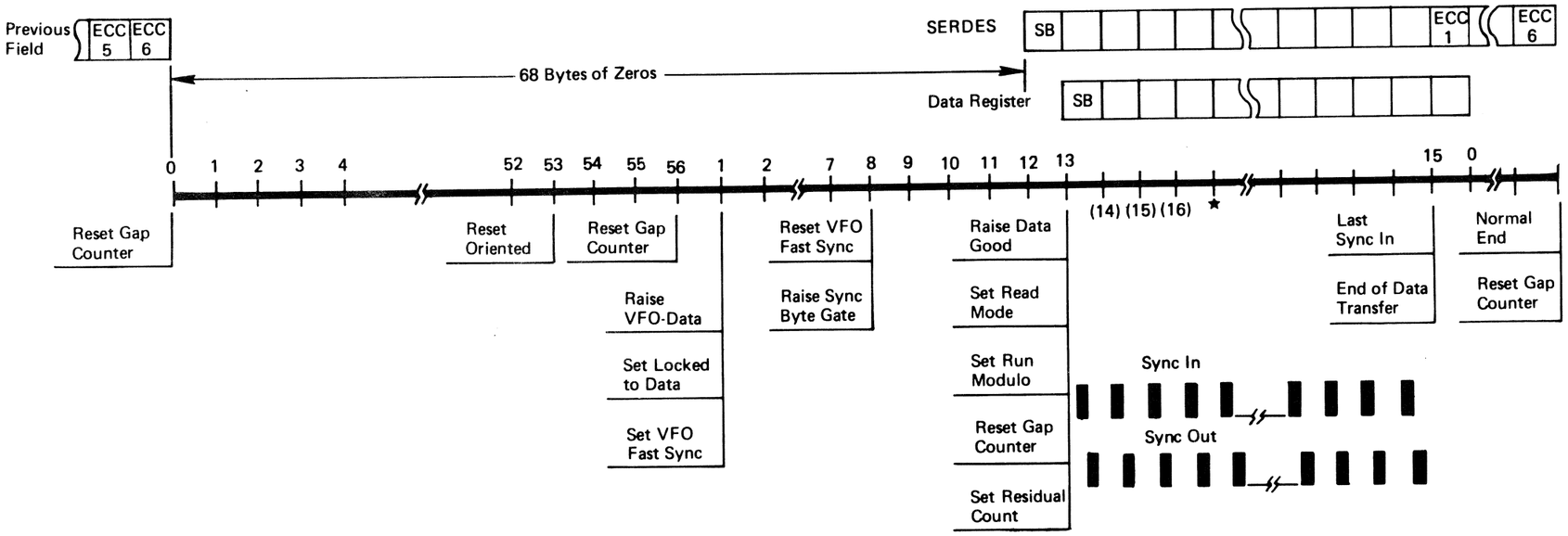
SB = Sync Byte
SD = Skip Displacement
PA = Physical Address
F = Flag
C = Cylinder
H = Head
ECC = Error Correction Code

★ The sync byte (SB) is recognized during the period from count 8 to count 21. When the sync byte is detected in SERDES, the gap counter is reset to the compliment of the Modulo-16 count (Bus Out bits 4 to 7 of Tag '0E'). The sync byte detection activates Data Good.

If the count reaches 21 while performing a Read G1, a defect skip is assumed and at count 128 the Gap Counter is again reset to zero and a new attempt is made to detect the sync byte.

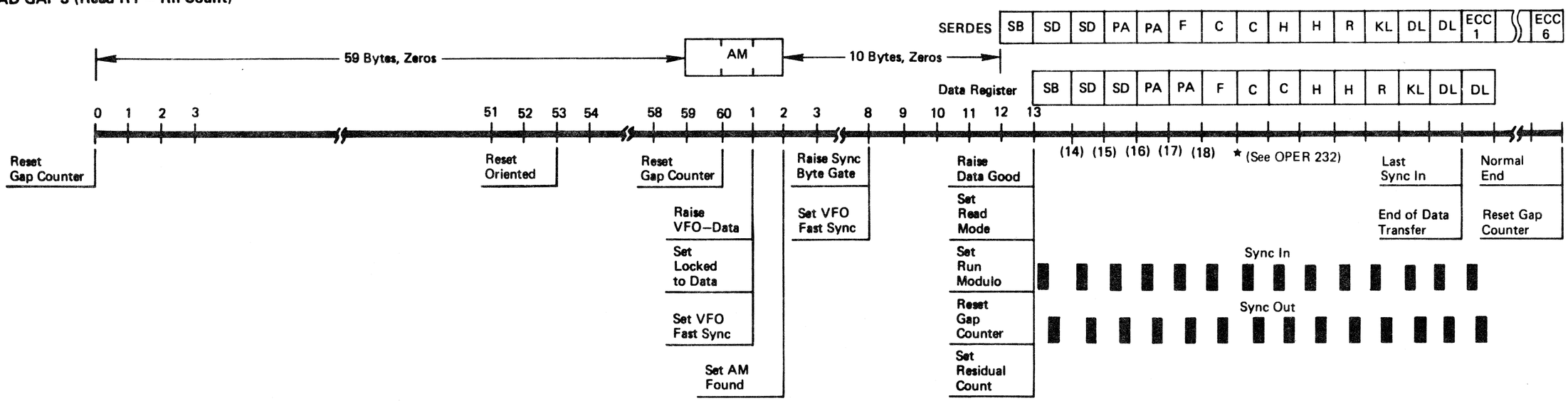
If the count reaches 21 while performing a Read G2 or Read G3, a Check End results and No Sync Byte Found is returned to storage control.

READ GAP 2 (Read Key, Data, R0 Count)

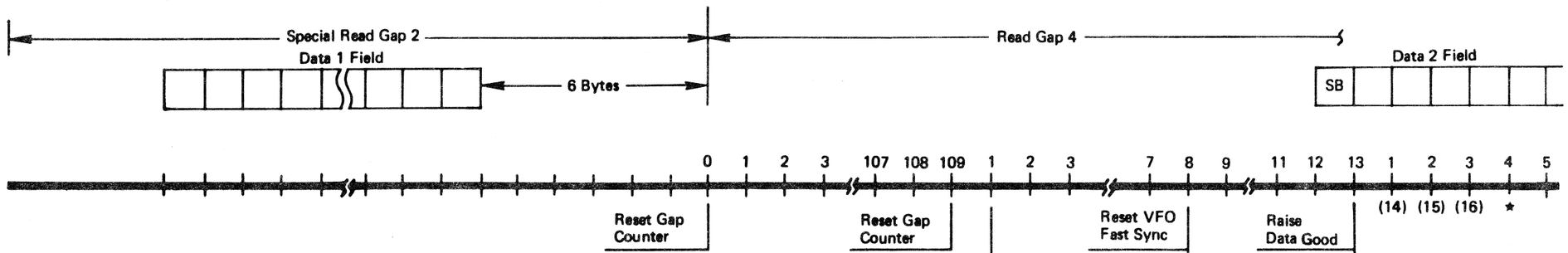


READ G3/G4 TIMING REFERENCE

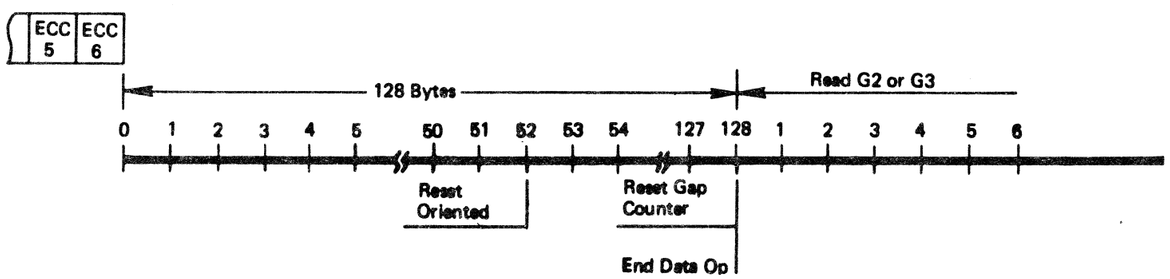
READ GAP 3 (Read R1 – Rn Count)



READ GAP 4 (Split Field)



READ GAP 4 (Moved Field)



FIXED HEADS – MODEL B2F

There are two 3344 models available:

B2: Satellite module without fixed heads.
B2F: Satellite module with fixed heads.

The Model B2F has 60 additional Read/Write heads in the HDA. The heads are fixed in position, one to a data track, on the Servo surface. (See the HDA description on OPER 30.)

Cylinders 1 and 2 are located on the fixed head tracks *instead of* on the movable head tracks. Cylinder 1 is under the first 30 fixed heads; cylinder 2 is under the second 30 fixed heads.

Reference pages:
Physical location on the HDA OPER 30.
Head Select logic OPER 140