

**GA26-1659-4**

File Nos. 8100-05, 4300-05

**Systems**

**IBM 8809 Magnetic  
Tape Unit  
Description**



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### **Fifth Edition (July 1983)**

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## Preface

This book is a reference for the IBM 8809 Magnetic Tape Unit. It includes information about the available models, tape reel requirements, tape loading and formatting, modes of operation, performance timings, and tape handling and storing. This book also includes information describing the status and sense bytes and error recovery procedures for the 8809 Magnetic Tape Unit attached to an IBM 4331 Processor or an IBM 8100 Information System. The information in this book will interest the users of the device including system programmers, who are writing programs for magnetic tape, and system engineers, who are planning installations using magnetic tape.

## Major Divisions of This Publication

This book consists of the following chapters:

- “Introduction” describes the design of the tape unit, the models available and their features, the format of information that is written on tape, and the performance of the tape unit in each of its two operating modes. This chapter also describes how to handle and store tape and tape reels to prevent damage to the information on the tape. The operator panel indicators and pushbuttons, and the procedures to apply or remove power to the tape unit are also described.
- “The 8809 Magnetic Tape Unit with an IBM 4331 Processor” describes the set of internal commands available from the processing unit to transmit instructions to the tape unit, the status bytes and sense bytes that the tape unit transmits to the processor, and the error recovery procedures.
- “The 8809 Magnetic Tape Unit in an IBM 8100 Information System” describes the programmable elements of the 8809 adapter, its programmed operations, the programmed control of the 8809 tape unit, the 8809 tape unit’s sense and status data, and includes programmed error recovery procedures for the 8809 tape unit.

## Related Publications

Although there are no prerequisite publications for an understanding of the information in this book, it is assumed that the reader has a basic knowledge of magnetic tape subsystems.

- *Tape Requirements for IBM One-Half Inch Tape Units at: 556, 800, 1600, and 6250 BPI*, GA32-0006-5 or later version

For IBM 4331 Processor attachment:

- *IBM 4331 Functional Characteristics and Processor Complex Configurator*, GA33-1526
- *IBM 4300 Processors Principles of Operation*, GA22-7070
- *IBM 4300 Processors Summary and Input/Output and Data Communications Equipment Configurator*, GA33-1523
- *IBM 4300 Processors Installation Manual—Physical Planning*, GA24-3667
- *IBM Input/Output Device Summary*, GA32-0039
- *IBM Input/Output Equipment Installation Manual—Physical Planning for System/360, System/370, and 4300 Processors*, GC22-7064

For IBM 8100 Information System attachment:

- *Introduction to the IBM 8100 Information System*, GA27-2875
- *IBM 8100 Information System Principles of Operation*, GA23-0031
- *IBM 8130 Processor Description*, GA27-3196
- *IBM 8140 Processor Description*, GA27-2880
- *IBM 8100 Information System: 8101 Storage and Input/Output Unit Description*, GA27-2882
- *IBM 8100 Information System Site Planning and Preparation Guide for IBM 8130, IBM 8140, IBM 8101*, GC27-2884
- *IBM 8100 Information System Configurator*, GA27-2876



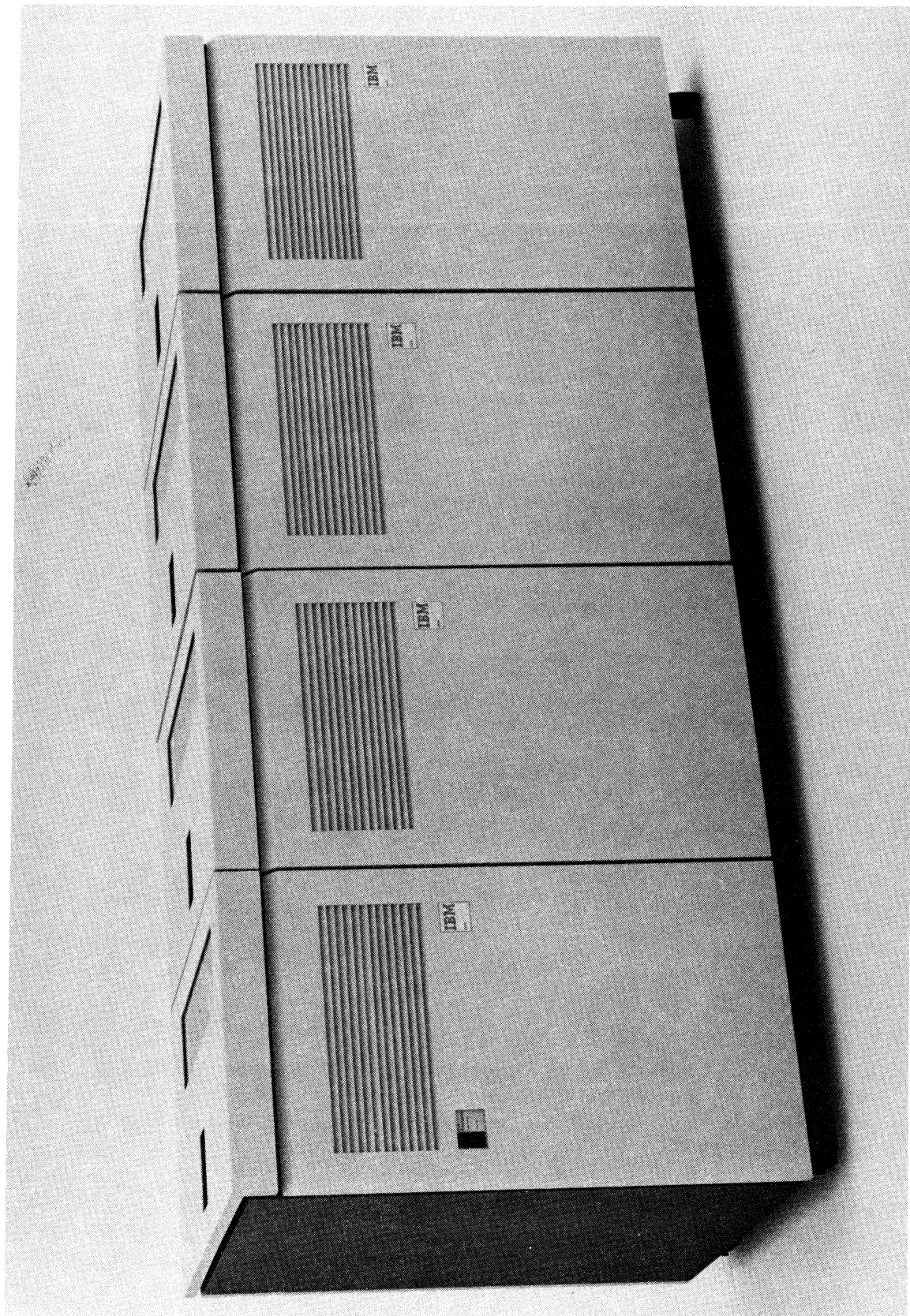
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IBM 8809 Magnetic Tape Units in a Series of Four Units

## Introduction

The IBM 8809 Magnetic Tape Unit introduces a new and simplified design. The tape unit moves tape directly reel-to-reel, without a capstan or vacuum columns; tape tension and velocity are controlled electronically.

The 8809 Magnetic Tape Unit is designed for use with either an IBM 4331 Processor or an IBM 8100 Information System. The 8809 attaches to a 4331 Processor with a Magnetic Tape Unit Adapter as shown in Figure 5. The 8809 attaches to an 8100 Information System in two ways. See Figure 10 for typical tape unit configurations for an IBM 8100 Information System.

The 8809 operates at two speeds: start and stop mode (low speed) and streaming mode (high speed). The start and stop mode operates at a speed of 0.318 meter per second (12.5 inches per second) for applications such as processing and journaling data base and data communication information. This mode provides a data rate of 20,000 bytes per second. The streaming mode operates at a speed of 2.54 meters per second (100 inches per second) to move data to and from direct access storage devices at high speed. This mode provides a data rate of 160,000 bytes per second, and is especially useful to back up data stored on nonremovable disks. The operating modes are set by command under program control from the processor.

## Models Available

The 8809 Magnetic Tape Unit is available in four models: 1A, 1B, 2, and 3. A Model 1A can be attached to either an IBM 4331 Processor or an IBM 8100 Information System. A Model 1B can be attached to only an IBM 8100 Information System. Models 2 and 3 connect to an IBM 4331 Processor or an IBM 8100 Information System through a Model 1A or 1B.

**Model 1A** is the first 8809 in a series of tape units. On the IBM 4331 Processor, the Model 1A attaches by means of the Magnetic Tape Unit Adapter feature. On the IBM 8100 Information System, the Model 1A attaches to an 8101 Storage and I/O Unit, Model A10, A11, A13, A20, A23, or A25 by means of the Magnetic Tape Attachment feature. A Diskette Drive and Magnetic Tape Attachment feature is also required on an IBM 8101 Model A10 and a Model A20. Model 1A contains power for itself and for the second 8809 unit in a series of 8809 units.

**Model 1B** is the first 8809 in a string of tape units that attaches directly to an IBM 8130 or 8140 processor. This model contains power for itself and for the second 8809 unit in a series of 8809 units. An IBM 8100 System Multi-Drive feature is required on the Model 1B if more than one 8809 is attached to an IBM 8130 or 8140 Processor.

**Model 2** is the second, fourth, and sixth 8809 in a string of tape units attached to an IBM 4331 Processor. It is the second and fourth 8809 unit in a string of tape units attached to an IBM 8100 Information System. It does not contain power. It connects to a Model 1A, 1B, or 3 and receives its power from the tape unit to which it is connected.

**Model 3** is the third and fifth 8809 in a string of tape units attached to an IBM 4331 Processor. It is the third 8809 unit in a string of tape units attached to an IBM 8100 Information System. It contains power for itself and supplies power to a fourth and sixth tape unit, which are Model 2 tape units.

## IBM 8100 System Multi-Drive Feature

The IBM 8100 System Multi-Drive feature for the 8809 Model 1B allows up to three IBM 8809 tape units to be physically attached in series to an IBM 8809 Model 1B tape unit.

## Tape Requirements

The 8809 tape unit uses one-half inch magnetic tape, IBM Multisystem tape or its equivalent. See *Tape Requirements for IBM One-Half Inch Tape Units at: 556, 800, 1600, and 6250 BPI* for magnetic tape requirements and recommendations. Reel diameters of 6.25, 7.0, 8.5, and 10.5 inches are accepted; however, IBM 10.5-inch reels with large or padded hubs for 365.8 meters (1200 feet) of tape are not suitable for use on the 8809 tape unit.

Tape reels used on the 8809 tape unit must satisfy the polar moment-of-inertia levels shown in Figure 1. These levels are typical of the tape reels usually encountered.

Empty Tape Reel			
Reel Diameter		Polar Moment of Inertia	
6.25 and 7 in.		0.000480 ± 40% kg m <sup>2</sup>	
8.50 in.		0.00114 ± 17% kg m <sup>2</sup>	
10.50 in.		0.00250 ± 8% kg m <sup>2</sup>	
Full Tape Reel			
Reel Diameter	Tape Length	Polar Moment of Inertia	E-Value*
6.25 in.	91.4–183 m (300–600 ft)	0.000859 ± 0.000213 kg m <sup>2</sup>	0.5 cm (0.2 in.)
7.00 in.	91.4–183 m (300–600 ft)	0.001356 ± 0.000231 kg m <sup>2</sup>	0.6 cm (0.2 in.)
8.50 in.	365.8 m (1200 ft)	0.00336 ± 0.00027 kg m <sup>2</sup>	1.0 cm (0.4 in.)
10.50 in.	731.5 m (2400 ft)	0.00867 ± 0.00042 kg m <sup>2</sup>	1.1 cm (0.4 in.)
*E-value is defined as the radial distance that the reel flanges extend beyond the outermost layer of tape. The polar moment-of-inertia given above is invalid if the tape reel does not have the indicated E-value.			

Figure 1. Polar Moment-of-Inertia Levels

## Operating Environment

The 8809 tape unit operates over a wider environmental range than other IBM tape units. Its extended environmental range permits a wider range of acceptable temperature and humidity conditions.

### 8809 Operating Environment:

Temperature: 15.6–37.8° C (60–100° F)

Relative Humidity: 8–80%

Maximum Wet Bulb: 25.6° C (78° F)

When a tape is written on an IBM tape unit in a normal environment, there can be a degradation of performance if the tape is processed on a tape unit in an extended environment.

### **Normal Operating Environment for other IBM tape units:**

Temperature: 16–32° C (60–90° F)

Relative Humidity: 20–80%

Maximum Wet Bulb: 22° C (72° F)

For further information on tape environmental requirements refer to *Tape Requirements for IBM One-Half Inch Tape Units*.

## **Tape Loading**

The simplified, reel-to-reel tape path of the 8809 is easily accessible to the operator for threading.

When the top cover of the 8809 is open, the operator has access to the tape path. The file reel (mountable) is mounted on the tape unit and latched by the operator. The tape is then manually threaded, and the leader is securely attached to the machine reel (permanently mounted).

**Caution: When threading the tape, the operator must ensure that the tape is properly threaded in the tape guides to prevent damage to the tape.**

A normal load occurs when the tape is mounted with the beginning-of-tape (BOT) mark positioned toward the file reel side of the BOT/EOT sensor. When the cover is closed and the Load Rewind pushbutton pressed, the tape unit loads the tape to the beginning-of-tape mark and the ready light comes on.

A loose wrap load is used to remove loose wraps from a tape. Position the BOT mark toward the machine reel side of the BOT/EOT sensor and press the Load Rewind pushbutton. The 8809 moves the tape forward and searches for the BOT mark. When the mark is not sensed in approximately five seconds, the 8809 moves the tape forward to about the mid-point of a 10.5-inch reel and stops. The tape is then rewound to the normal load point position.

If, during tape loading, the BOT mark is accidentally positioned toward the machine reel side of the BOT/EOT sensor when there are no loose wraps on the tape, the 8809 still does a loose wrap load procedure when Load Rewind is pressed. No harm should occur to the tape in this event.

## **Tape Format**

To provide interchangeability with existing tape products, magnetic tape is recorded in a nine-track, phase encoded (PE) format at a density of 1600 bytes per inch (BPI). This format is compatible with the specification published in American National Standard Institute (ANSI), *Recorded Magnetic Tape for Information Interchange (1600 BPI, PE)*, form X3.39.1973 and approved by the U.S.A. National Bureau of Standards.

A beginning-of-tape (BOT) mark indicates the beginning of the recording area (the load point). An end-of-tape (EOT) mark indicates the end of the recording area. The 8809 tape unit senses the presence of the marks. When tape motion is set to the forward direction, the tape moves toward the EOT, and when set to the backward direction, the tape moves toward the BOT.

**Note:** *When the tape unit is operating in streaming mode (high speed), the BOT mark is positioned approximately 33 cm (13 inches) beyond the BOT/EOT sensor (toward the file reel) upon completion of a Rewind command or a load rewind operation. In start/stop mode (low speed), the BOT mark is positioned at the BOT/EOT sensor when BOT is indicated.*

Beginning adjacent to the BOT mark, a format identification burst is recorded to indicate the 1600 BPI phase-encoded density. The identification burst consists of writing the P track at 1600 flux changes per inch (FCI) and erasing all the other tracks for approximately 120 millimeters (4.7 inches) of tape. There is a 12.7 millimeters (0.5 inch) minimum gap between the identification burst and the first data block. The identification burst is read checked; if it is not written correctly, an error is indicated.

Information on tape is arranged in blocks. A tape block consists of one or more bytes, which are logical units of data. Each data block is preceded by a recorded preamble of 41 characters, 40 characters of which contain 0 bits in all tracks followed by a single character containing 1 bits in all tracks. Each data block is followed by a recorded postamble of 41 characters, the first character of which contains 1 bits in all tracks followed by 40 characters containing 0 bits in all tracks.

Data blocks are separated on tape by an interblock gap (IBG). The 8809 tape unit can operate with either a 30.5 millimeters (1.2 inch) IBG or a 15.2 millimeters (0.6 inch) IBG. Setting the size of the IBG is under program control.

A tape mark separates files. A 1600-BPI tape mark is written as 128 flux reversals (3200 FCI) in all tracks<sup>1</sup> except 1, 3, and 4, which are erased. The tape mark is recognized by the 8809 as the presence of recording in tracks 2, 6, and 7, and the absence of recording in tracks 1, 3, and 4.

## Reading and Writing

During read operations, the 8809 tape unit generates the correct parity for each byte before sending it to the system. Single-track error correction takes place during data transmission as in other IBM tape products in 1600 BPI. During write operations, the parity of each byte is checked when it is received from the system and again after it is written (readback check). For a write operation, a write-enable ring must be placed in the tape reel to enable the 8809 to erase the tape and write new data.

## Modes of Operation

The 8809 tape unit operates in either start and stop mode at 0.318 meter per second (12.5 inches per second) or in streaming mode at 2.54 meters per second (100 inches per second). When power is turned on, the 8809 tape unit is set at low speed (start and stop mode), and thereafter speed is changed by a command under program control.

In the start and stop mode, the 8809 tape unit operates in the same way as do existing tape products, that is, it stops within the interblock gap (IBG) and accelerates when a command is received. Early receipt of a command by the 8809 tape unit results in continuous tape motion across the IBG at 0.318 meter per second (12.5 inches per second).

In the streaming mode, tape motion continues without loss of time due to starting and stopping if the next command is received during the command reinstruct time. The 8809 tape unit maintains the 2.54 meters per second (100 inches per second) velocity through the interblock gap, anticipating the next command. If a command is received within the interblock gap, there is no loss of time due to starting and stopping. If commands arrive after

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<sup>1</sup> Track numbers begin from the edge of the tape nearest to the beginning-of-tape mark and are identified in order 5, 7, 3, P, 2, 1, 0, 6, 4.



command reinstruct time or are discontinued, there is a command overrun. The 8809 automatically recovers from a command overrun to execute a command received during the recovery cycle or to await the next command.

If a command overrun condition is expected or known to be programmed, high-speed streaming mode should not be used. For instance, formatting and archiving jobs or a large amount of system I/O traffic can cause a long command reinstruct time or interval between operations. More efficient operation of the tape unit can be achieved by operating in the start and stop mode.

Figure 2 describes streaming mode recovery cycle following a command overrun.

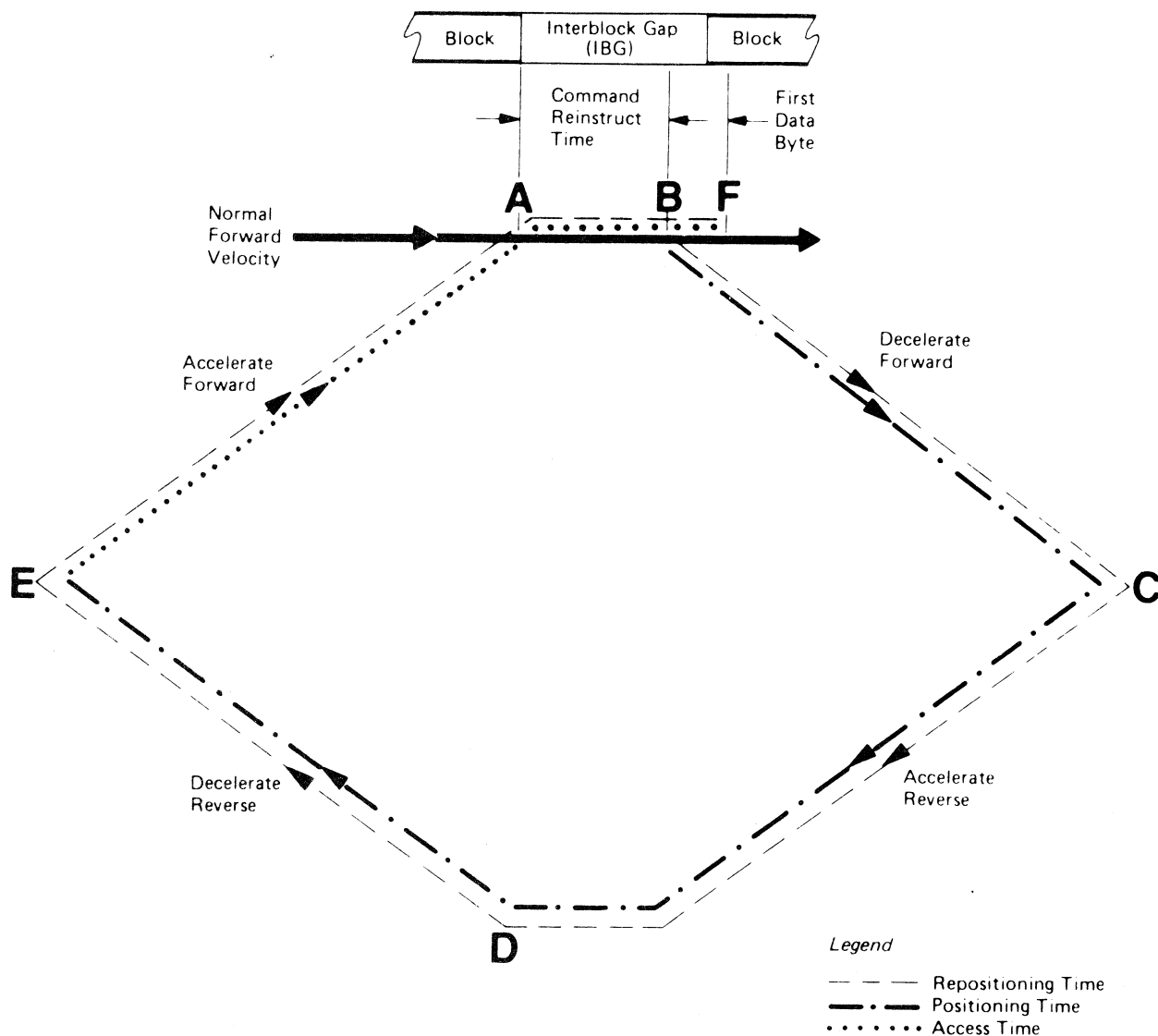
The tape unit recovery cycle is governed by the period during which a command is received.

If a command is received during command reinstruct time, tape motion continues at normal velocity. If commands are discontinued or arrive after the end of the command reinstruct time, there is a command overrun and the tape unit automatically goes through a recovery cycle.

If a command is received between the end of the command reinstruct time and the stopped state, tape motion continues moving toward the stopped state and then accelerates to attain normal velocity, and the command is executed.

If a command is not received before the tape unit reaches the stopped state, tape motion remains stopped and the tape unit waits for the next command.

If a command is received while the tape reel is in the stopped state, tape motion accelerates to attain normal velocity, and the command is executed.



#### Notes:

1. **Command Reconstruct Time (A to B):** Tape motion continues at the normal velocity if a command is received between A and B. If commands are discontinued or arrive after the end of the reconstruct time (B), there is a command overrun, and the 8809 tape unit automatically goes through a recovery cycle.
2. **Repositioning Time (B to C to D to E to A to F):** If a command overrun occurs and a command is received between the end of the reconstruct time (B) and the stopped state (E), the 8809 tape unit proceeds to point E and then accelerates forward from E to attain normal velocity and execute the command.
3. **Positioning Time (B to C to D to E):** If a command overrun occurs and a command has not been received by the time the 8809 tape unit reaches the stopped state (E), the 8809 remains stopped and awaits the next command.
4. **Access Time (E to A to F):** When a command is received while the 8809 tape unit is in the stopped state, the 8809 accelerates forward from E to attain normal velocity and executes the command. (Access time is the time between the stopped state and the transfer of the first byte of data. This definition applies whether the 8809 is operating in start and stop or streaming mode.)

Figure 2. Streaming Mode Recovery Cycle Following a Command Overrun

## Performance Timings

Figure 3 summarizes the performance times for the tape unit in both operating modes, where applicable. Command reinstruct, positioning, and repositioning operations are performed only in streaming mode. The times for transfer of the first byte of data vary significantly in streaming mode depending on whether the command is received while the tape unit is in streaming mode or after a command overrun.

Operation		Start and Stop Mode	Streaming Mode
<b>Load Time:</b>	The time from pressing the Load Rewind pushbutton on the operator panel until the tape is stopped at the BOT with tension established.		
	<ul style="list-style-type: none"> <li>With the BOT mark on the file reel side of the BOT/EOT sensor (normal load)</li> </ul>	10 seconds	10 seconds
	<ul style="list-style-type: none"> <li>With the BOT mark on the machine reel side of the BOT/EOT sensor (loose wrap load)</li> </ul>	3 minutes	3 minutes
<b>Rewind Time:</b>	The maximum time to rewind 730 meters (2400 feet) of tape on a 10.5-inch reel.	2.6 minutes	2.6 minutes
<b>Tape Speed:</b>	Nominal	0.3175 meter per second (12.5 inches per second)	2.54 meters per second (100 inches per second)
<b>Data Rate:</b>	Instantaneous	20,000 bytes per second	160,000 bytes per second
<b>Access Time:</b>	The time from the stopped state to the transfer of the first byte of data to or from the tape. Nominal access times are for a read followed by a read and for a write followed by a write.		
	<ul style="list-style-type: none"> <li>Read, nominal: <ul style="list-style-type: none"> <li>With an IBG of 15.2 millimeters (0.6 inch)</li> </ul> </li> </ul>	44 milliseconds	335 milliseconds
	<ul style="list-style-type: none"> <li>With an IBG of 30.5 millimeters (1.2 inches)</li> </ul>	92 milliseconds	341 milliseconds
	<ul style="list-style-type: none"> <li>Write, nominal: <ul style="list-style-type: none"> <li>With an IBG of 15.2 millimeters (0.6 inch)</li> </ul> </li> </ul>	40 milliseconds	335 milliseconds
	<ul style="list-style-type: none"> <li>With an IBG of 30.5 millimeters (1.2 inches)</li> </ul>	88 milliseconds	341 milliseconds
<b>IBG Time</b>	The time for the interblock gap to traverse the read/write head.		
	<ul style="list-style-type: none"> <li>With an IBG of 15.2 millimeters (0.6 inch)</li> </ul>	48 milliseconds	6 milliseconds
	<ul style="list-style-type: none"> <li>With IBG of 30.5 millimeters (1.2 inches)</li> </ul>	96 milliseconds	12 milliseconds
<b>Command Reinstruct Time:</b>	The time from completion of a command execution to the latest point in the IBG at which the 8809 tape unit can accept another command and does not execute a recovery cycle.		
	<i>Note: These elapsed times include the time that the system or processor requires for completion handling and command initiation.</i>		
	<ul style="list-style-type: none"> <li>With an IBG of 15.2 millimeters (0.6 inch): <ul style="list-style-type: none"> <li>Between Write Block commands</li> </ul> </li> </ul>		4.5 milliseconds
	<ul style="list-style-type: none"> <li>Between Write Tape Mark or Space Block commands</li> </ul>		4.2 milliseconds
	<ul style="list-style-type: none"> <li>Between Read Block commands</li> </ul>		6.0 milliseconds
	<ul style="list-style-type: none"> <li>With an IBG of 30.5 millimeters (1.2 inches): <ul style="list-style-type: none"> <li>Between Write Block or Read Block commands</li> </ul> </li> </ul>		10.5 milliseconds
	<ul style="list-style-type: none"> <li>Between Write Tape Mark or Space Block commands</li> </ul>		8.7 milliseconds
<b>Repositioning Time:</b>	The time for access to the first byte of data from a command received immediately after the command reinstruct time.		
	Nominal		1165 milliseconds
	Worst case		1405 milliseconds
<b>Positioning Time:</b>	The time to recover from a command overrun and return to the stopped state to await the next operation.		
	Nominal		870 milliseconds
	Worst case		1035 milliseconds

Figure 3. Performance Timings

## ***Tape Handling***

You should establish procedures to protect magnetic tape from contamination, which causes degraded tape unit performance. Some general rules are:

- Never leave a tape reel exposed outside its container or leave a container open. Tape can be damaged, and dust that accumulates on the tape or in the container can contaminate the tape. A tape reel that is not in use on a tape unit should always be stored in its container.
- Do not erase a paper tape reel identification label because eraser crumbs can contaminate the tape or the container. Always use new labels when changing reel identification. Use a label with an adhesive backing that does not leave a residue and that can be applied and removed easily.
- Never allow a loose end of tape to trail on the floor; dirt picked up on the tape can reach the tape unit threading path and be passed on to other sections of the tape.
- Do not permit smoking in areas where tape is in use. Ashes contaminate tape; hot ashes can permanently damage the tape surface.
- Do not touch the tape edges through the reel openings or press on the reel flanges. Such pressure can compress the tape and damage its edges.
- Be very careful when removing the write-enable ring. Always unload the tape from the machine reel onto the file reel before removing the write-enable ring; never remove the ring while tape is loaded in the tape path.

## ***Tape Storing***

To prevent tape contamination and damage during storage, follow these procedures:

- Before a tape is stored in its container, secure the loose end with a tape-end retainer to prevent the tape from unwinding.
- Always store tape reels in an upright position. Never store tape reels flat, singly or in stacks; the tape could be compressed, or the tape reel could become warped.
- Store tape reels in a cabinet or shelf elevated from the floor and away from sources of paper and card dust. Paper dust and dirt could be transferred from the outside of the container to the tape during load and unload operations.

## Operator Panel

An operator panel on the 8809 tape unit consists of indicators and pushbuttons as shown in Figure 4 and described in the following text.

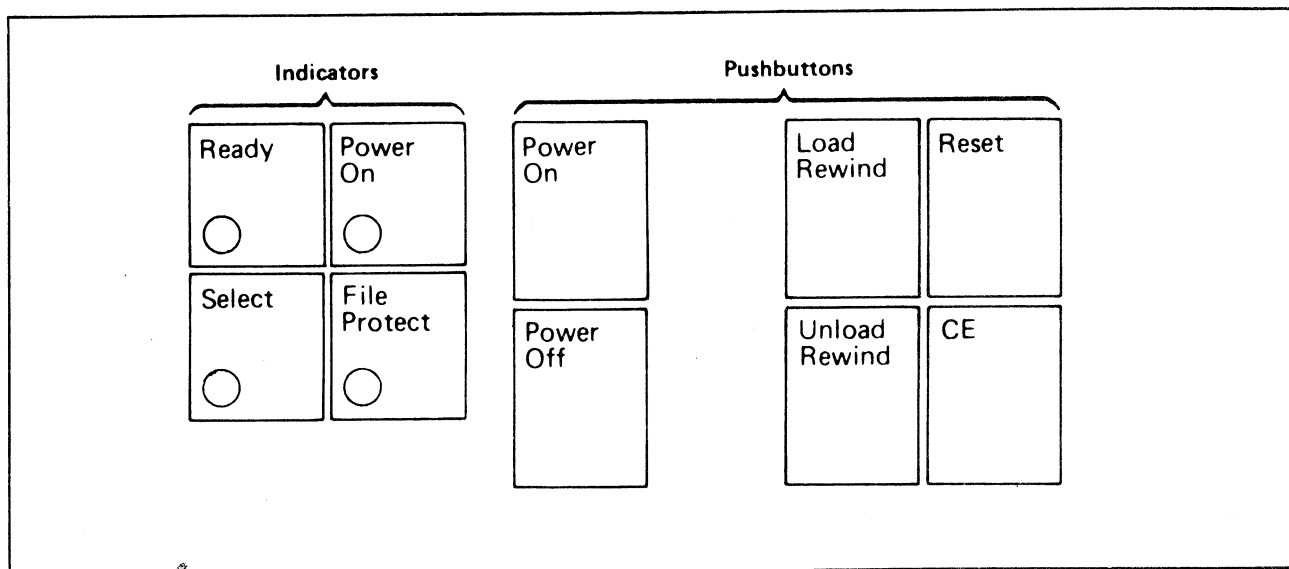


Figure 4. Operator Panel of the IBM 8809 Magnetic Tape Unit

### Indicators

**Ready** indicates that the tape unit is in a ready state.

**Power On** indicates that power is applied to the tape unit.

**Select** indicates that the tape unit is selected.

**File Protect** indicates that no write-enable ring is sensed in the tape reel.

### Pushbuttons

**Power On (Models 1A, 1B, and 3 only)** causes power to be applied to a tape unit or to a pair of tape units (Model 1A, 1B, or 3 and a Model 2). The Unit Emergency switch, located on the front panel of the tape unit, must be in the Power Enable position to enable the Power On pushbutton to apply power.

**Load Rewind** causes the tape unit to establish tension and rewinds the tape to the beginning-of-tape mark.

**Reset** causes the tape unit to go to a not-ready state.

**Power Off** causes power to be removed from a pair of tape units that share a power supply; for instance, a Model 1A or 1B and a Model 2 or a Model 3 and a Model 2. This pushbutton is on all 8809 models.

**Unload Rewind** causes the tape unit to rewind the tape completely onto the file reel so the reel can be removed from the tape unit.

**CE** is used by the service representative during offline servicing. There is no effect if this pushbutton is pressed inadvertently during normal operation.

## ***Power On/Power Off Procedures***

You cannot power on or power off the tape unit from the processor. The power can be controlled at the tape unit only. If power is removed from an 8809 tape unit when it is operating, unpredictable results occur.

### **Power On Procedure**

Press the Power On pushbutton at the Model 1A, 1B, or 3 tape unit. The Model 2 tape unit does not have a Power On pushbutton because it does not have a power supply. It receives power from a Model 1A, 1B, or 3 tape unit. Be sure the Unit Emergency switch is in the Power Enable position.

### **Power Off Procedure**

All the tape units in the series must have completed all operations and have no pending interrupts.

Press the Power Off pushbutton at the operator panel of the tape unit.

**Caution:** Pressing the Power Off pushbutton on one tape unit causes power to go off for a pair of tape units that share a power supply; for instance a Model 1A or 1B and a Model 2, or a Model 3 and a Model 2. When the Unit Emergency switch is in the Power Off position, power is removed for all tape units in a series.

# The 8809 Magnetic Tape Unit with an IBM 4331 Processor

This chapter describes the programming support, models, and features for an 8809 tape unit attached to an IBM 4331 Processor. This chapter also includes tape unit commands, status and sense data, retry counters, and error recovery procedures.

## Programming Support

When attached to an IBM 4331 Processor, the 8809 tape unit is supported by two operating systems, Disk Operating System/Virtual Storage Extended (DOS/VSE) and Virtual Machine/Basic System Extensions, Release 2 (VM/BSE). Utility programs are available for streaming mode support. Satisfactory performance while in streaming mode may require dedicated processor operation and use of a long interblock gap instead of the normal interblock gap.

## Models and Attachment

Up to six 8809 tape units can be attached in a series to an IBM 4331 Processor. The processor requires an IBM Magnetic Tape Unit Adapter feature for attachment of an 8809. See Figure 5 for typical configurations of 8809 tape units with an IBM 4331 Processor.

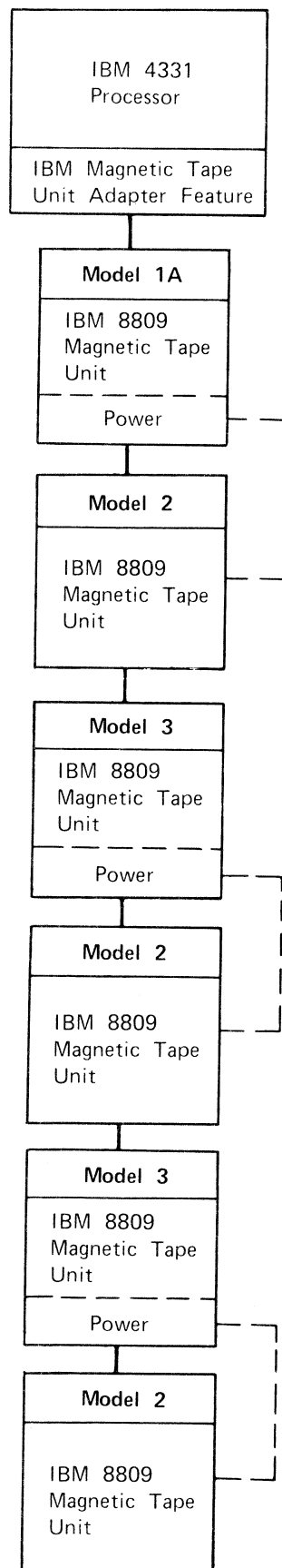
**Model 1A** is the first unit in a series of 8809 tape units. It attaches to an IBM 4331 Processor and contains power for itself and a Model 2.

**Model 2** is the second, fourth, or sixth unit in a series. It connects to a Model 1A or a Model 3 and derives its power from either unit.

**Model 3** is the third or fifth unit in a series. It connects to a Model 2 and contains power for itself and another Model 2.

## *8809 Address Assignments*

Every 8809 tape unit has a unique address consisting of a channel address, a tape control address, and a tape unit address. The 8809 tape unit addresses are within the range X'0' through X'7' and are assigned during installation.



**Figure 5. Typical Configuration for an IBM 8809 Attached to an IBM 4331 Processor**



## Command Set for an 8809 Tape Unit Attached to an IBM 4331 Processor

A Start I/O instruction from the IBM 4331 Processor initiates a tape operation. The processor also sends one of the following commands to designate the operation the tape unit is to execute. Figure 6 is a list of the command codes.

Commands	Command Byte								Hex
	0	1	2	3	4	5	6	7	
Write	0	0	0	0	0	0	0	1	01
Read	0	0	0	0	0	0	1	0	02
Forward Space Block	0	0	1	1	0	1	1	1	37
Backspace Block	0	0	1	0	0	1	1	1	27
Erase Gap	0	0	0	1	0	1	1	1	17
Write Tape Mark	0	0	0	1	1	1	1	1	1F
Data Security Erase	1	0	0	1	0	1	1	1	97
Rewind	0	0	0	0	0	1	1	1	07
Rewind Unload	0	0	0	0	1	1	1	1	0F
Forward Space File	0	0	1	1	1	1	1	1	3F
Backspace File	0	0	1	0	1	1	1	1	2F
Set High Speed	1	1	1	0	0	0	1	1	E3
Set Low Speed	1	0	0	0	0	0	1	1	83
Set Long Gap	0	0	0	1	0	0	1	1	13
Set Normal Gap	0	0	1	0	0	0	1	1	23
Set High Speed and Long Gap	1	0	0	1	0	0	1	1	93
Set High Speed and Normal Gap	0	0	1	1	0	0	1	1	33
Set Low Speed and Long Gap	0	1	0	1	0	0	1	1	53
Set Low Speed and Normal Gap	0	1	1	0	0	0	1	1	63
Loop Write-to-Read	1	0	0	0	1	0	1	1	8B
Control No Op	0	0	0	0	0	0	1	1	03
Mode Set	1	1	0	0	0	0	1	1	C3
Sense	0	0	0	0	0	1	0	0	04
Sense I/O	1	1	1	0	0	1	0	0	E4
Read and Reset Buffered Log	1	0	1	0	0	1	0	0	A4

Figure 6. Command Byte Codes for an IBM 8809 Attached to an IBM 4331 Processor

**Write** measures a gap and writes a block of data in the forward direction. If this command is received when the tape is at the beginning-of-tape mark, the 1600 BPI format identification burst is written prior to the data block. Before writing the data, the 8809 tape unit creates the proper length gap and writes the preamble. After the data, the 8809 writes the postamble and completes the readback check.

**Read** reads the next block in the forward direction.

**Forward Space Block** spaces over the next block in the forward direction.

**Backspace Block** spaces over the next block in the backward direction.

**Erase Gap** erases a gap of 100 millimeters (3.9 inches) in the forward direction. This command is used to increase the gap preceding a block in order to position the head beyond a point on the tape containing a defect.

**Write Tape Mark** erases a gap of 90 millimeters (3.6 inches) and then writes a tape mark in the forward direction. If this command is issued when the tape is at the beginning-of-tape mark, the 1600-BPI format identification burst is written prior to the gap and the tape mark.

**Data Security Erase** erases the tape in the forward direction from the point where the command is issued to a point approximately one meter beyond the EOT mark.

**Rewind** rewinds the tape to the beginning-of-tape mark.

**Rewind Unload** rewinds the tape to the beginning-of-tape mark, releases tension, and unloads the tape leader from the machine reel.

**Forward Space File** searches for the next tape mark in the forward direction. If no tape mark is sensed, the search continues until tape is unwound from the file reel, causing an error condition to interrupt the 4331 processor.

**Backspace File** searches for the next tape mark in the backward direction. If no tape mark is sensed, the search continues until the BOT mark is reached, causing an error condition to interrupt the 4331 processor.

**Set High Speed** sets tape velocity to 2.54 meters per second (100 inches per second) streaming mode.

**Set Low Speed** sets tape velocity to 0.318 meter per second (12.5 inches per second) start and stop mode.

**Set Long Gap** sets the 8809 tape unit to generate an IBG of 30.5 millimeters (1.2 inches), independent of speed setting.

**Set Normal Gap** sets the 8809 tape unit to generate an IBG of 15.2 millimeters (0.6 inch), independent of speed setting.

**Set High Speed and Long Gap** sets tape velocity to 2.54 meters per second (100 inches per second) streaming mode, and sets the 8809 tape unit to generate an IBG of 30.5 millimeters (1.2 inches).

**Set High Speed and Normal Gap** sets tape velocity to 2.54 meters per second (100 inches per second) streaming mode, and sets the 8809 tape unit to generate an IBG of 15.2 millimeters (0.6 inch).

**Set Low Speed and Long Gap** sets tape velocity to 0.318 meter per second (12.5 inches per second) start and stop mode, and sets the 8809 tape unit to generate an IBG of 30.5 millimeters (1.2 inches).

**Set Low Speed and Normal Gap** sets tape velocity to 0.318 meter per second (12.5 inches per second) start and stop mode, and sets the 8809 tape unit to generate an IBG of 15.2 millimeters (0.6 inch).

**Loop Write-to-Read** logically connects the write path and the read path to help isolate data path failures. No tape motion is initiated.

**Control No Op** stores status information in main storage. There is no action at the tape unit.

**Mode Set** is treated as a No Operation command. There is no action at the tape unit.

**Sense** stores up to 24 bytes of sense information in main storage.

**Sense I/O** provides seven bytes of device identification information as follows:

Byte	Contents
0	X'FF'
1	Processor type number
2	Processor type number
3	Processor model number
4	Device type number
5	Device type number
6	Device model number

**Read and Reset Buffered Log** stores up to 32 bytes of statistical information in main storage. This information is stored as format 6 sense bytes. All usage and error counters are reset to zero.

## Status Information and Sense Data

The unit status byte and channel status byte each contain eight bits of status information about the selected tape unit. The halfword of status information is retained by the channel until it is incorporated in the channel status word (CSW) or until another operation is accepted. Status information is updated at the beginning of each tape operation, except Test I/O, to indicate initial status. It is also updated during a tape operation to provide status information when an I/O operation ends. This information is set in the status bytes of the CSW by an I/O interruption or, under some circumstances, by a Start I/O, Test I/O, or Halt I/O instruction. Bits 32 through 39 of the CSW, which indicate tape unit status, and bits 40 through 47 of the CSW, which indicate channel status, are described in this section.

- Only one channel end indication and device end indication are generated for each I/O operation.
- Channel end and device end indication are not generated when programming errors or equipment malfunctions are detected during initiation of an operation prior to the tape unit returning its status.
- When command chaining takes place, only the channel end indication and device end indication of the last operation are available to the program.
- The channel may or may not present channel end indication to the operating system even though channel end indication was present when a tape unit caused premature termination of a chain of commands or during the initiation of a chained command.
- If an unusual condition is detected during initiation of a chained command, the chain is terminated without the device end indication.

## ***Unit Status Byte***

As a result of an instruction such as Test I/O or Start I/O, or when a command is completed, the unit status byte is automatically available in bits 32 through 39 of the channel status word (CSW). The channel status byte is also available in bits 40 through 47 of the CSW. Figure 7 summarizes the status information.

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
32	Attention	This bit is not used in normal operation. However, when an error is detected while the tape unit is idle, the error sets this bit and the unit check bit.
33	Status Modifier	Not Used.
34	Control Unit End	Not Used.
35	Busy	Set when the addressed tape unit is executing a previously started operation or when secondary status (device end indication) is pending because a start I/O was issued. A pending device end indication causes only the addressed tape unit to be busy; the other tape units attached to the Magnetic Tape Unit Adapter are available.
36	Channel End	Set when a command is initiated or when an operation has been completed. Channel end and device end bits are set at the same time.
37	Device End	Set alone only when the tape unit is changed from not ready to ready state (operator pressed the Load Rewind pushbutton at the operator panel on the tape unit). This bit is set with the channel end bit when a command is initiated or when an operation has been completed.
38	Unit Check	<p>Set when an error or unusual situation occurs during an operation or the start of an operation. A Sense command can be issued to determine why this bit is set. A contingent connection with the addressed tape unit is maintained to save the sense information related to the unit check until the next Start I/O instruction is issued with a command other than No Op. Preferably, a Sense command is issued. This bit is set when any of the following occur:</p> <ul style="list-style-type: none"><li>• Bit 32 of the CSW (attention) is set.</li><li>• Any bit in sense byte 0 is set.</li><li>• Bit 0 of sense byte 1 (noise) is set.</li><li>• A Backspace Block or Backspace File operation is initiated into or at the beginning-of-tape mark.</li><li>• Bit 6 of sense byte 1 (file protected) is set during a write operation.</li><li>• Bit 7 of sense byte 1 (not capable) is set.</li></ul> <p>See sense byte 3 for the error recovery procedure characters that are valid for each unit check condition.</p>

Bit	Designation	Interpretation
39	Unit Exception	Set when a specific command cannot be completed for a logical reason: for example, when a Write command causes the tape to run until the end-of-tape mark is reached, or when a Forward Space Block or Backspace Block command encounters a tape mark.

### ***Channel Status Byte***

Bit	Designation	Interpretation
40	Programmed Controlled Interrupt	Set when an interruption was requested because the channel command word (CCW) to which the status applies has the program-controlled interruption (PCI) flag set. The I/O operation continues processing.
41	Incorrect Length	Set for a read operation when the tape has reached the next interblock gap before the count in the CCW has been reduced to zero, or if there is more data available after the CCW count has reached zero. Set for a write operation when the tape runs off the reel. The incorrect length bit also can be set when data transfer operations are stopped by halt I/O or halt device. The incorrect length bit can be suppressed by the program by the SLI flag in the CCW. This bit is not used for Rewind, Rewind Unload, Erase Gap, Write Tape Mark, Data Security Erase, Forward Space Block, Forward Space File, Backspace Block, and Backspace File commands.
42	Program Check	Set when any of the following errors is detected: <ul style="list-style-type: none"> <li>• Invalid CCW address specification</li> <li>• Invalid CCW address</li> <li>• Invalid command code (detected by channel)</li> <li>• Invalid count</li> <li>• Invalid data address</li> <li>• Invalid key</li> <li>• Invalid channel address word format</li> <li>• Invalid sequence</li> </ul> <p><b>Note:</b> <i>The channel checks only the four low-order bits of the command code for the standard patterns for read, write, control, and sense. Although the pattern may be valid for the channel, it may not be valid for the tape unit.</i></p>
43	Protection Check	Set when the key in the channel address word does not match the key in storage for the location referenced by the command or when an attempt is made to access a channel command word or data from a page that is disconnected.
44	Channel Data Check	Not Used.
45	Channel Control Check	Set when a machine malfunction is detected that affects the channel controls. For example, a hardware check is found in the control line and is signaled to the processor.
46	Interface Control Check	Not Used.
47	Chaining Check	Not Used.

## Sense Data

Sense data provides detailed information about the selected tape unit and about the last operation performed. Information transferred by the sense command is more detailed than that supplied by the status bytes, and may be used to determine why a unit check bit is set. Figure 7 summarizes the sense information. An asterisk identifies a bit that does not cause the unit check bit to be set.

Unit Status and Channel Status Bytes								
Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Unit Status	Attention	Status Modifier (Not Used)	Control Unit End (Not Used)	Busy	Channel End	Device End	Unit Check	Unit Exception
Channel Status	Program Controlled Interrupt	Incorrect Length	Program Check	Protection Check	Channel Data Check	Channel Control Check	Interface Control Check (Not Used)	Chaining Check (Not Used)
Sense Bytes								
0	Command Reject	Intervention Required	Not Used	Equipment Check	Data Check	Overrun	Not Used	Not Used
1	Noise	Tape Unit Status A*	Tape Unit Status B*	Not Used	Load Point	Write Status*	File Protected	Not Capable
2	Track in Error pointers.							
3	Two ERP hexadecimal characters that define error recovery procedures performed by the program.							
4	Not Used	Not Used	Tape Indicate*	Permanent Error	Host Detected Error	Loop Write-to-Read Error	Not Used	Not Used
5	Not Used	Not Used	Not Used	PEID Burst Check	Not Used	Not Used	Not Used	Not Used
6	This byte contains all zeros.							
7	Format Code				Data Security Erase	Not Used	Not Used	Not Used
Format 1: Sense Bytes								
8	Ready	Busy	Write Enable	Beginning of Tape	End of Tape	Operation Complete	Low Speed	Positioning
9	Check End Sense	Bus Out Parity Check	Tag Bus Parity Check	Formatter Failure	Control Lines Sequence Check	Command Register Parity Check	Drive Control Parity Check	Formatter Read Failure
10	Data Overrun	Data Check	Not Used	Beginning of Tape	End of Tape	Tape Mark Detected	Not Capable	Not Used
11	Write Bus Parity Check	Bus Out Register Parity Check	Gap Control Check	Sync Out Check	Drive Response Check	Not Capable Space File	Track In Error P	Write Enable Error
12	Write Bus Parity Check	Read Bus Parity Check	Gap Control Check	Sync Out Check	Not Used	Not Used	Track In Error P	Write Enable Error
13	Track in Error 0	Track in Error 1	Track in Error 2	Track in Error 3	Track in Error 4	Track in Error 5	Track in Error 6	Track in Error 7

Figure 7 (Part 1 of 2). Status and Sense Byte Summary, IBM 8809 Attached to an IBM 4331 Processor

Format 1: Sense Bytes								
Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
14	= 0 Nonwrite-type Command	No Track Pointer	Multitrack Error	End Data Check	Start Read Check	Crease	Not Used	Skew Error
	= 1 Write Command	PEID Check				Read Back Failure	Envelope Check	Write Tape Mark Error
15	This byte contains all zeros.							
16	Transport State					Sequence Error	Sense Bus Parity Check	Not Used
17	Start Velocity Check	End Velocity Check	PEID Velocity Check	Clock Parity Error	Servo State		Sense Bus Parity Check	Not Used
18	Load Check	Tension Check	Cover/Reel Latch Interrupt	Tension Status	Not Ready Due to Reset	Long Gap Mode	Sense Bus Parity Check	Not Used
19	Present Transport State					Cover/Reel Latch Status	Sense Bus Parity Check	Not Used
20	Servo Logic Failure	Servo Analog Failure	Write Current Failure	Erase Current Failure	Present Servo State		Sense Bus Parity Check	Not Used
21	Idler Tachometer Failure	Machine Tachometer Failure	File Tachometer Failure	Idler Tachometer Rotation Check	Not Used	Not Used	Sense Bus Parity Check	Not Used
22	BOT/EOT LED Failure	Tape Present LED Failure	Reel Size LED Failure	Drive Control Failure	Not Used	Not Used	Sense Bus Parity Check	Not Used
23	File Amplifier Saturation	Machine Amplifier Saturation	Write Status	Power Amplifier Cable Unseated	Not Used	Not Used	Sense Bus Parity Check	Not Used
24	This byte contains zeros.							
25	This byte contains zeros.							
26	Device Address							
	Address 4	Address 2	Address 1	Not Used	Not Used	Not Address 4	Not Address 2	Not Address 1
27	This byte contains zeros.							
28	Contains contents of control line-tag bus at time of error.							
29	Contains contents of control line-bus out at time of error.							
30	Contains the high-order fault symptom code.							
31	Contains the low-order fault symptom code.							
Format 6: Sense Bytes								
Sense bytes 0, 1, 2, 4, 5, and 6 are set to zeros; sense byte 3 contains the fixed ERP number X'01'; and sense byte 7 contains the format X'60'. Sense bytes 8 through 31 contain the counters.								

**Figure 7 (Part 2 of 2). Status and Sense Byte Summary, IBM 8809 Attached to an IBM 4331 Processor**

## ***Sense Byte 0***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Command Reject	<p>Set when:</p> <ul style="list-style-type: none"><li>• The tape unit receives an unassigned command.</li><li>• A Write, Write Tape Mark, Erase Gap, Data Security Erase, or Loop Write-to-Read command is issued to a file-protected tape.</li><li>• A command is received in the wrong sequence; that is, when a Data Security Erase command is not command-chained from a preceding Erase Gap command, or when a Read command or Forward Space command follows a Write command without an intervening backward command.</li></ul>
1	Intervention Required	<p>Set when the addressed tape unit is not ready, when it is being tested inline, or when it is nonexistent.</p>
2	Not Used	<p>This bit contains a zero.</p>
3	Equipment Check	<p>Set when:</p> <ul style="list-style-type: none"><li>• Internal hardware malfunctions are detected, such as failure of the light-emitting diodes that detect the beginning or end of tape.</li><li>• Velocity errors occur, when a tape mark cannot be written error-free, when tape tension is incorrect, or other tape unit problems are encountered.</li></ul>
4	Data Check	<p>Set when:</p> <ul style="list-style-type: none"><li>• Uncorrectable parity errors are detected.</li><li>• Two or more tracks have low amplitude or a phase error.</li><li>• Excessive skew is detected.</li><li>• One track is in error during a write operation.</li><li>• Two tracks are in error during a read operation.</li></ul>
5	Overrun	<p>Set when storage fails to send or accept data during a data transfer operation. An attempt to chain data within a record causes overrun, and transfer of data terminates.</p>
6	Not Used	<p>This bit contains a zero.</p>
7	Not Used	<p>This bit contains a zero.</p>



## ***Sense Byte 1***

An asterisk identifies a bit that does not cause the unit check bit to be set.

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>															
0	Noise	Set when the data check bit (sense byte 0 bit 4) is set during a read operation.															
1	Tape Unit Status A*	Set when the tape unit is selected and ready.															
2	Tape Unit Status B*	Set when the tape unit is not ready or is busy executing the commands or functions as given in sense byte 8 bit 1. Together, bits 1 and 2 provide the following indications: <table><tr><th>Status A</th><th>Status B</th><th>Status Indication</th></tr><tr><td>0</td><td>0</td><td>Tape unit is nonexistent.</td></tr><tr><td>0</td><td>1</td><td>Tape unit is not ready.</td></tr><tr><td>1</td><td>0</td><td>Tape unit is ready and not busy.</td></tr><tr><td>1</td><td>1</td><td>Tape unit is ready and busy.</td></tr></table>	Status A	Status B	Status Indication	0	0	Tape unit is nonexistent.	0	1	Tape unit is not ready.	1	0	Tape unit is ready and not busy.	1	1	Tape unit is ready and busy.
Status A	Status B	Status Indication															
0	0	Tape unit is nonexistent.															
0	1	Tape unit is not ready.															
1	0	Tape unit is ready and not busy.															
1	1	Tape unit is ready and busy.															
3	Not Used	This bit contains a zero.															
4	Load Point	Set when the selected tape unit is loaded, ready, and is at the beginning-of-tape (BOT) mark.															
5	Write Status*	Set when the selected tape unit has completed a write command. When this bit is not set, the tape unit is in read status.															
6	File Protected	Set if the tape reel on the selected tape unit does not have a write-enable ring installed and the tape unit is ready.															
7	Not Capable	Set when the tape unit cannot read the tape because the 1600-BPI identification burst is not on the tape. This may be due to a new or erased tape, or the tape is not written in phase-encoded mode. This bit always sets the unit check bit.															

## ***Sense Byte 2***

Each bit in the byte represents one track. One or more failing tracks are indicated for diagnostic and recovery purposes. The presence of any one of the bits in this byte sets the data check and unit check bits.

## ***Sense Byte 3***

This byte contains two error recovery procedure (ERP) hexadecimal characters that define the recovery actions to be performed by the operating system program.

ERP Number (Hex)	Action Performed
01	Post statistical record and reissue operation command.
02	Enter the error record and reissue operation command.
03	Provide Equipment Check message, enter the error record, and terminate.
04	Provide Equipment Check and warning messages, enter the error record, and terminate.
05	Provide Intervention Required message, enter the error record, and terminate.
06	Provide Intervention Required message and terminate.
07	Provide Write Data Check message, enter the error record, and terminate.
08	Provide Write Data Check and Hardware Failure messages, and terminate.
09	Provide Read Data Check message, enter the error record, and terminate.
0A	Provide Not Capable message, enter the error record, and terminate.
0B	Provide File Protected message and terminate.
0C	Provide Command Rejected message and terminate.
0D	Provide Backspaced Into Load Point message and terminate.
0E	Provide Data Security Erase Failure message, enter the error record, unit error record log, and terminate.
0F	Provide PEID Check message, enter the error record, and terminate.
10	Provide Overrun message and terminate.

**Figure 8. Recovery Actions Defined by Sense Byte 3**

### ***Sense Byte 4***

An asterisk identifies a bit that does not cause the unit check bit to be set.

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Not Used	This bit contains a zero.
1	Not Used	This bit contains a zero.
2	Tape Indicate*	Set whenever the end-of-tape (EOT) mark is sensed during a forward tape operation. If this bit is set during a Write, Write Tape Mark, or Erase Gap operation, the unit exception bit (CSW bit 39) is also set.
3	Permanent Error	Set when an error is detected and all automatic retry attempts have failed.
4	Host Detected Error	Set when a requirement of the processor has not been met.
5	Loop Write-to-Read Error	Set when an error is detected during a Loop Write-to-Read operation.
6	Not Used	This bit contains a zero.
7	Not Used	This bit contains a zero.

### ***Sense Byte 5***

Bit 3 is the only bit used in Sense Byte 5. Bit 3 (PEID burst check) is set if the PE identification burst written during a Write, Write Tape Mark, or Erase Gap command is detected as faulty.

### ***Sense Byte 6***

This byte contains zeros.

### ***Sense Byte 7***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0-3	Format Code	The format code defines the contents of sense bytes 8 through 31. One of two formats is defined: format 1 (X'10') is set if the sense bytes contain sense data; and format 6 (X'60') is set if the sense bytes contain statistical data.
4	Data Security Erase	Set when the Data Security Erase operation detected signals in the erased area or failed to complete for some other reason.
5	Not Used	This bit contains a zero.
6	Not Used	This bit contains a zero.
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 8***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Ready	Set when the tape unit is loaded and tape tension is established.
1	Busy	Set during execution of the following operations:  Data Security Erase Rewind Rewind Unload Set Low Speed Set High Speed Forward Space File Backspace File  Busy is also set while the tape unit is executing the operator panel functions of Load Rewind or Unload Rewind.
2	Write Enable	Set when the tape reel is not file protected (a write-enable ring is installed).
3	Beginning of Tape	Set when the tape is positioned at the beginning-of-tape mark.
4	End of Tape	Set when the end-of-tape mark is sensed and the tape is moving in the forward direction. It is reset when the end-of-tape mark is sensed and the tape is moving in the backward direction.
5	Operation Complete	Set at the completion of those commands and functions given in sense byte 8 bit 1 that cause the busy bit to be set.
6	Low Speed	Set when the 8809 is set to operate at a speed of 0.318 meter per second (12.5 inches per second).
7	Positioning	Set during the positioning time shown in Figure 2.

### ***Format 1: Sense Byte 9***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Check End Sense	Set when any of sense byte 10 bits 0, 1, 5, and 6 are set.
1	Bus Out Parity Check	Set when even parity is detected on command or data transfer from the 4331 processor. This condition also sets sense byte 0 bit 3 (equipment check).
2	Tag Bus Parity Check	Set when even parity is detected on a command transfer from the 4331 processor. This condition also sets sense byte 0 bit 3 (equipment check).
3	Formatter Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
4	Control Lines Sequence Check	Set when improper sequencing occurs on control lines from the 4331 processor. This condition also sets sense byte 0 bit 3 (equipment check).
5	Command Register Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
6	Drive Control Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Formatter Read Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).

### ***Format 1: Sense Byte 10***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Data Overrun	Set when a data transfer to or from the IBM 4331 processor has not occurred within the time specified for the 8809.
1	Data Check	Set when one or more of the conditions occur as defined in sense byte 14.
2	Not Used	This bit contains a zero.
3	Beginning of Tape	Set when the beginning-of-tape mark is sensed. Sense byte 8 bit 3 is also set.
4	End of Tape	Set when the end-of-tape mark is sensed. Sense byte 8 bit 4 is also set.
5	Tape Mark Detected	Set when a tape mark is detected during a Read, Forward Space Block, or Backspace Block command.
6	Not Capable	Set when: <ul style="list-style-type: none"><li>• A PEID burst is not detected while reading or spacing the tape forward from the beginning-of-tape mark.</li><li>• A PEID burst is not correctly recorded while writing from the beginning-of-tape mark.</li></ul>
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 11***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Write Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Bus Out Register Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Gap Control Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
3	Sync Out Check	Set when the control lines used for data transfer do not operate correctly. This condition also sets sense byte 0 bit 3 (equipment check).
4	Drive Response Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
5	Not Capable Space File	Set when 1600-BPI identification burst is not detected while executing a Space File command from the BOT mark. This condition also sets sense byte 10 bit 6 and sense byte 9 bit 0.
6	Track In Error P	Set when the error correction pointer for track P is on at the end of the last operation for which a Data Check occurred.
7	Write Enable Error	Set when a write operation is attempted and the tape is mounted without a write-enable ring.

### ***Format 1: Sense Byte 12***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Write Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Read Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Gap Control Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
3	Sync Out Check	Set when the control lines used for data transfer do not operate correctly. This condition also sets sense byte 0 bit 3 (equipment check).
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Track In Error P	Set when the error correction pointer for track P is on at the end of the last operation on which Data Check occurred.
7	Write Enable Error	Set when a write is attempted and the tape is mounted without a write-enable ring.

### ***Format 1: Sense Byte 13***

These bits indicate the track(s) for which error correction pointers are on at the end of the last operation on which Data Check occurred.

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Track in Error 0	
1	Track in Error 1	
2	Track in Error 2	
3	Track in Error 3	
4	Track in Error 4	
5	Track in Error 5	
6	Track in Error 6	
7	Track in Error 7	

### ***Format 1: Sense Byte 14***

The definition of sense byte 14 depends on the operation in progress at the time the sense bytes are set. Bit 0 indicates this operation and the meaning that is given to the remaining bits.

#### **Nonwrite-type Commands**

For all commands other than Write Block, Erase Gap, or Write Tape Mark, sense byte 14 has the following meaning:

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Nonwrite-type Command	This bit contains a 0 for a nonwrite command.
1	No Track Pointer	Set when a parity error is detected with no accompanying track pointer. This condition also sets sense byte 0 bit 4 (data check).
2	Multitrack Error	Set when a multiple track error (more than one pointer) is detected. The data is not correctable. This condition also sets sense byte 0 bit 4 (data check).
3	End Data Check	Set when an interblock gap IBG is detected earlier or later than expected. This condition also sets sense byte 0 bit 4 (data check).
4	Start Read Check	Set when a partially recorded data block is detected. This condition also sets sense byte 0 bit 4 (data check).
5	Crease	Set when a temporary loss of data is detected in all tracks of a data block. This condition also sets sense byte 0 bit 4 (data check).
6	Not Used	This bit contains a zero.
7	Skew Error	Set when the skew buffer exceeds its capacity. This condition also sets sense byte 0 bit 4 (data check).

## Write Commands

During a Write Block, Erase Gap, or Write Tape Mark, sense byte 14 has the following meaning:

Bit	Designation	Interpretation
0	Write Command	This bit contains a 1 for a write command.
1	PEID Check (with Data Check)	Set when a PEID burst is not correctly recorded while writing from the beginning-of-tape mark. This condition also sets sense byte 0 bit 4 (data check).
2	Multitrack Error	Same as for nonwrite commands except it applies to readback check. This condition also sets sense byte 0 bit 4 (data check).
3	End Data Check	Same as for nonwrite commands except it applies to readback check. This condition also sets sense byte 0 bit 4 (data check).
4	Start Read Check	Same as for nonwrite commands except it applies to readback check. This condition also sets sense byte 0 bit 4 (data check).
5	Read Back Failure	This bit and sense byte 0 bit 3 (equipment check) are set when readback data does not occur when expected during a Write Block or Write Tape Mark command. This bit and sense byte 0 bit 4 (data check) are set when a temporary loss of data is detected in all tracks of a data block.
6	Envelope Check	Set when a data error is detected during readback check. This condition also sets sense byte 0 bit 4 (data check).
7	Write Tape Mark Error	Set when the tape mark is not written correctly during a Write Tape Mark command. This condition also sets sense byte 0 bit 4 (data check).

### ***Format 1: Sense Byte 15***

This byte contains all zeros.

### ***Format 1: Sense Byte 16***

Sense Byte 16 shows the encoded state of the 8809 when an 8809 sequence error (byte 16 bit 5) occurs. Bits 0 through 4 contain the transport state sequences and bit 5 indicates a sequence error.

Bit	Designation	Interpretation
0-4	Transport State	Used for machine failure diagnosis.
5	Sequence Error	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.



### ***Format 1: Sense Byte 17***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Start Velocity Check	Set when a velocity problem occurs before a write data transfer. This bit indicates that the 8809 did not move the tape. The previous command can be reissued without repositioning the tape. This condition also sets sense byte 0 bit 3 (equipment check).
1	End Velocity Check	Set when a velocity problem occurs during a write data transfer. The tape must be repositioned before rewriting data. This condition also sets sense byte 0 bit 3 (equipment check).
2	PEID Velocity Check	Set when a velocity problem occurs while attempting to write a 1600-BPI phase-encoded identification burst. This condition also sets sense byte 0 bit 3 (equipment check).
3	Clock Parity Error	Set when an internal parity error is detected in the clock generation module. This condition also sets sense byte 0 bit 3 (equipment check).
4, 5	Servo State	Used for machine failure diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 18***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Load Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Tension Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Cover/Reel Latch Interrupt	Set when the cover is opened after tape is loaded and tape tension is established. The ready condition is reset and sense byte 0 bit 3 (equipment check) is reset.
3	Tension Status	Set when the tape is correctly loaded in the tape path.
4	Not Ready Due to Reset	Set when a command is received and the 8809 is not ready. It is also set when the Reset pushbutton is pressed and the tape is not at the beginning-of-tape mark. This condition also sets sense byte 0 bit 1 (intervention required).
5	Long Gap Mode	Set when the 8809 is in long gap mode.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 19***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0–4	Present Transport State	Used for machine diagnosis.
5	Cover/Reel Latch Status	Used for machine diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 20***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Servo Logic Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Servo Analog Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Write Current Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check). This machine failure can cause data to be destroyed.
3	Erase Current Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check). This machine failure can cause data to be destroyed.
4, 5	Present Servo State	Used for machine diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 21***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Idler Tachometer Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Machine Tachometer Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	File Tachometer Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
3	Idler Tachometer Rotation Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 22***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	BOT/EOT LED Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Tape Present LED Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Reel Size LED Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
3	Drive Control Failure	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Byte 23***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	File Amplifier Saturation	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
1	Machine Amplifier Saturation	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
2	Write Status	Set when the tape unit executed a Write, Write Tape Mark, Erase Gap, or Data Security Erase command.
3	Power Amplifier Cable Unseated	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure. This condition also sets sense byte 0 bit 3 (equipment check).
7	Not Used	This bit contains a zero.

### ***Format 1: Sense Bytes 24 and 25***

Sense bytes 24 and 25 contain all zeros.

### ***Format 1: Sense Byte 26***

Bits 0 through 2 contain the tape unit address. Bits 3 and 4 are not used and contain zeros. Bits 5 through 7 are normally zero. When an addressing error is detected, bits 5 through 7 contain the complement of bits 0 through 2.

Bit	Designation	Interpretation
0	Address 4	
1	Address 2	
2	Address 1	
3	Not Used	This bit contains a zero.
4	Not Used	This bit contains a zero.
5	Not Address 4	
6	Not Address 2	
7	Not Address 1	

### ***Format 1: Sense Byte 27***

Sense byte 27 contains all zeros.

### ***Format 1: Sense Byte 28***

Sense byte 28 contains the last command sent to the 8809 over the control lines before a failure.

### ***Format 1: Sense Byte 29***

Sense byte 29 contains the last command sent to the 8809 over the control lines before a failure.

### ***Format 1: Sense Byte 30***

Sense byte 30 contains the high-order fault symptom code for reference into maintenance procedures.

### ***Format 1: Sense Byte 31***

Sense byte 31 contains the low-order fault symptom code for reference into maintenance procedures.

### ***Format 6: Sense Bytes***

In format 6, sense bytes 0, 1, 2, 4, 5, and 6 are set to zero; sense byte 3 contains the fixed ERP number X'01'; and sense byte 7 contains the format code X'60'. Sense bytes 8 through 31 contain the counters described in "Error, Usage, Overrun, and Retry Counters," which follows.

## Error, Usage, Overrun, and Retry Counters

Each tape unit owns a specific control block in a reserved area of IBM 4331 processor storage. Each control block contains statistical information including error, usage, overrun, and retry counters.

The Magnetic Tape Unit Adapter feature functional and error handling microcode updates the counters. When one of the counters overflows, the counter overflow flag is present for the respective tape unit. The next Start I/O instruction that addresses the tape unit having the active overflow flag causes a unit check to be set in the initial status.

The unit check condition causes the operating system to issue a sense command to the addressed tape unit. The format 6 sense bytes are displayed or printed and the counters are set to zeros. A Read and Reset Buffered Log command also causes the format 6 sense bytes to be displayed or printed and the counters to be set to zeros.

The format 6 sense bytes are assigned as follows:

Counter	Sense Byte	Counter Name
Error	8	Multitrack Errors
	9	End Data Checks
	10	Start Read Checks
	11	Readback Failures
	12	Envelope Checks
	13	No Pointer Errors
	14	Crease Errors
	15	Skew Errors
	16	Track 4 Errors
	17	Track 5 Errors
	18	Track P Errors
	19	Velocity Checks
	20	Temporary Read Errors*
	21	Temporary Write Errors*
Usage	22 and 23	Read Operations
	24 and 25	Write Operations
Overrun	27	Data Overruns
Retry	28 and 29	Erase Gap (write retry)**
	30 and 31	Read Retry
* The counters also count permanent errors. **The erase gap counter reflects both usage and write retries because erase gap is a standard operation during a write retry.		

### *Updating the Counters*

The error counters are updated by one each time an error occurs during command execution. Only the appropriate counter for each tape unit is updated. Error counters are not updated during retry attempts.

The usage counters are updated for every operation except retry attempts.

The retry counters are updated for retry attempts.

## 8809 Error Recovery Procedures

Recovery from errors is handled by an automatic retry procedure and software support for operator messages.

Automatic retry is a programmed procedure that causes a failing command to be retried (with required repositioning of the tape) without requiring an I/O interruption. The automatic retry action is initiated when an analysis of status and sense bytes detects an error. If the command is not successfully executed in a maximum number of attempts, or if attempts to retry are not made, sense byte 3 contains an ERP number that defines further action or messages. An error that occurs while executing a data security erase operation causes ERP X'0E' to be set in sense byte 3.

Figure 9 shows the sequence for testing sense bits, the automatic retry actions, and the ERP number for sense byte 3 when the retry is unsuccessful or is not performed.

Testing Priority	Sense		Description	Command	Automatic Retry		ERP*
	Byte	Bit			Action	Number of Retries	
1	9	2	Tag Bus Parity Check	Read or Write before tape motion occurs	Reissue the command that failed.	5	03
	11	1	Bus Out Register Check	Read or Write after tape motion occurs	1. Issue Backspace Block command. 2. Reissue the command that failed.	15	03
	9	1	Bus Out Parity Check				
			Forward Space Block Backspace Block Erase Gap Write Tape Mark	None		03	
			All others	Reissue the command that failed.	5	03	
2	9	3	Formatter Failure	Not Applicable	None		03
	9	4	Control Lines Sequence Check				
	9	5	Command Register Parity Check				
	9	6	Drive Control Parity Check				
	23	6	Sense Bus Parity Check				
3	20	2	Write Current Fail	Commands other than: Write Write Tape Mark Erase Gap	None		04
	20	3	Erase Current Fail				
4	22	0	BOT/EOT LED failure	Not applicable	None		03
	22	1	Tape Present LED failure				
	22	2	Reel Size LED failure				
	23	3	Power amplifier cable unseated				
* Placed in sense byte 3 when automatic retry was unsuccessful or none was required.							

Figure 9 (Part 1 of 3). Sense Data Error Summary for an IBM 8809 Attached to an IBM 4331 Processor

Test Priority	Sense		Description	Command	Automatic Retry		ERP*
	Byte	Bit			Action	Number of Retries	
5	18	2	Cover/Reel Latch Interrupt	Not Applicable	None		03
	18	4	Not Ready Due to Reset				06
6	18	1	Tension Check	Not applicable	None		03
	18	0	Load Check				
	21	3	Idler Tachometer Rotation Check				
7	9	7	Formatter Read Failure	Not applicable	None		03
	11	0	Write Bus Parity Check				
	11	2	Gap Control Check				
	11	3	Sync Out Check				
	11	4	Drive Response Check				
	12	1	Read Bus Parity Check	Read	1. Issue Backspace Block command. 2. Reissue the Read command that failed.	40 (See Note)	09
				Commands other than Read	None		
	16	5	Sequence Error	Not applicable	None		03
	17	3	Clock Parity Error				
	20	0	Servo Logic Failure				
	20	1	Servo Analog Failure				
	20	2	Write Current Fail	Write, Write Tape Mark, Erase Gap	None		03
	20	3	Erase Current Fail				
	21	0	Idler Tachometer Failure	Not Applicable	None		03
	21	1	Machine Tachometer Failure				
	21	2	File Tachometer Failure				
	22	3	Drive Control Failure				
	23	0	File Amplifier Saturation				
	23	1	Machine Amplifier Saturation				
8	8	3	Beginning of Tape	Backspace Block Backspace File	Issue Rewind command.	1	0D
9	17	2	PEID Velocity Check	Not applicable	1. Issue Rewind command. 2. Reissue the command that failed.	5	03
10	17	0	Start Velocity Check	Not applicable	Reissue the command that failed.	5	03
11	17	1	End Velocity Check	Not applicable	1. Issue Backspace Block command. 2. Reissue the command that failed.	15	03

\* Placed in sense byte 3 when automatic retry was unsuccessful or none was required.

**Note:** If the 8809 is in start/stop mode when the error is encountered, the retry procedure is attempted up to five times. If the error persists, the tape unit is changed to streaming mode and the retry attempts are repeated up to 40 times. If the tape unit mode was changed, it is changed back to start/stop mode before tape processing continues.

**Figure 9 (Part 2 of 3). Sense Data Error Summary for an IBM 8809 Attached to an IBM 4331 Processor**

Testing Priority	Sense		Description	Command	Automatic Retry		ERP*
	Byte	Bit			Action	Number of Retries	
12	11	5	Not Capable Space File	Not applicable	None		
	10	6	Not Capable	Write	1. Issue Rewind command. 2. Reissue the command that failed.	15 (See Note 2)	
					LWR Successful		0F
					LWR Unsuccessful		08
				All other commands	None		0A
13	10	0	Data Overrun	Not applicable	1. Issue Backspace Block command. 2. Reissue the command that failed.	15	10
14	10	1	Data Check	Read	1. Issue Backspace Block command. 2. Reissue the Read command that failed.	40 (See Note 1)	09
				Write	1. Issue Backspace Block command. 2. Issue Erase Gap 3. Reissue the Write command that failed.	15 (See Note 2)	
					LWR Successful		07
					LWR Unsuccessful		08
				Write Tape Mark	1. Issue Backspace Block command. 2. Issue Erase Gap command. 3. Reissue the Write Tape Mark command that failed.	15	07
15	11	7	Write Enable Error	Not applicable	None		0B
16	Not applicable	Not applicable	None of the previous testing priority bits.	Not applicable	None		03
<b>Host-Detected Errors**</b>							
17	Not applicable	Not applicable	Environmental data present	Not applicable	Record environmental (statistical) data on the host log device and reissue the command.	1	01
18	Not applicable	Not applicable	Selection failure	Not applicable	Reissue the command that failed.	5	03
19	Not applicable	Not applicable	Not Ready	Not applicable	None		06
20	Not applicable	Not applicable	Timeout waiting for device response	Not applicable	None		03
<p>* Placed in sense byte 3 when automatic retry was unsuccessful or none was required.</p> <p>** Host-detected errors are those conditions detected by the host for which no Device Error exists.</p> <p><b>Note 1:</b> If the 8809 is in start/stop mode when the error is encountered, the retry procedure is attempted up to five times. If the error persists, the tape unit is changed to streaming mode and the retry attempts are repeated up to 40 times. If the tape unit mode was changed, it is changed back to start/stop mode before tape processing continues.</p> <p><b>Note 2:</b> If the retry is unsuccessful, the Loop Write-to-Read command is issued.</p>							

**Figure 9 (Part 3 of 3). Sense Data Error Summary for an IBM 8809 Attached to an IBM 4331 Processor**



# The 8809 Magnetic Tape Unit in an IBM 8100 Information System

This chapter describes 8809 models and features that attach to an IBM 8100 system, the programmed operations and facilities of the 8809 adapter, and the programmed control of individual 8809 tape units that is provided by executing 8809 operations.

## Programming Support

Support for the 8809 tape unit is provided by two licensed programs in the 8100 system: Distributed Processing Control Executive (DPCX) and Distributed Processing Programming Executive/Base (DPPX/BASE). Each of these licensed programs includes a Standalone Disk Storage Dump/Restore utility.

## Attaching 8809s to an IBM 8100 System

Up to four 8809 tape units can be attached to an IBM 8100 system; the 8809 Model 1A or 1B is always the first tape unit in the series. The series of 8809 tape units attaches to the 8100 system in two ways:

- The 8809 Model 1A attaches to an 8100 system through an 8101 Storage and I/O Unit that contains the Magnetic Tape Attachment feature. The 8101 Storage and I/O Unit contains the 8809 adapter logic as part of the Magnetic Tape Attachment feature. Refer to the *8101 Storage and I/O Unit Description* for additional descriptions of the 8101.
- The 8809 Model 1B attaches directly to the 8100 processor's system control facility (SCF) signal bus. The 8809 Model 1B includes the secondary system control facility (SSCF) usage 4 and the 8809 adapter that are required for this direct connection. The SCF is introduced later in this section under "SCF Overview" and is described in detail in the *8130* and *8140 Processor Description* manuals.

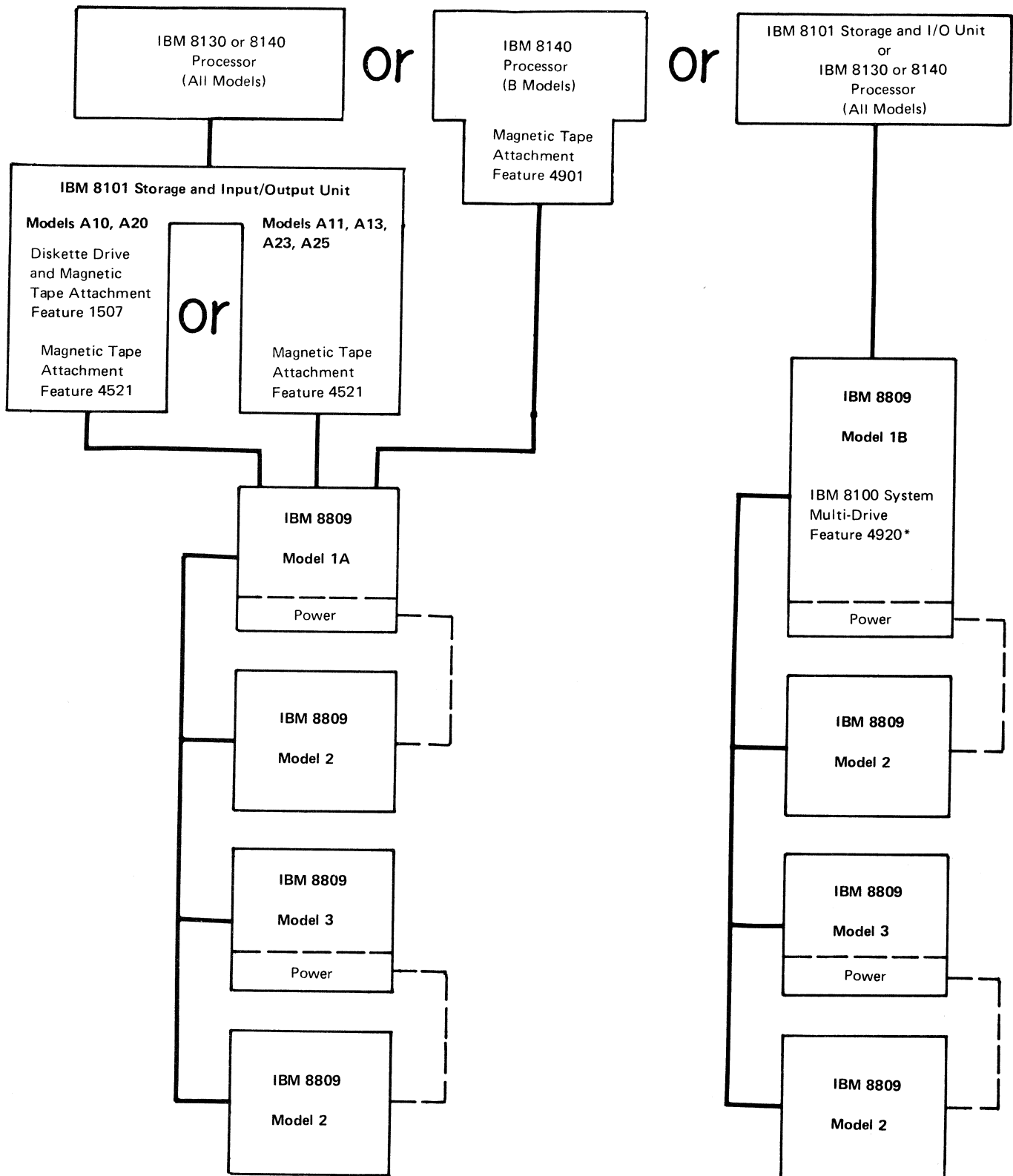
The two ways that the series of 8809 tape units attach to an IBM 8100 system are summarized in Figure 10. The 8101 and 8809 features required for these attachments are identified in this figure.

**Model 1A** is the first unit in a series of 8809 tape units. It contains power for itself and an 8809 Model 2. The 8809 Model 1A attaches to an 8101 Storage and I/O Unit Model A10, A11, or A13. In an 8100 system, the 8809 Model 1A and the Model 1B are mutually exclusive. The 8101 contains a Magnetic Tape Attachment feature that includes the 8809 adapter logic. The 8101 Model A10 also must contain the Diskette Drive and Magnetic Tape Attachment feature.

**Model 1B** is the first unit in a series of 8809 tape units. It contains power for itself and an 8809 Model 2. The 8809 Model 1B includes the SSCF usage 4 and the 8809 adapter logic. If additional tape units are to be included in the series (8809 Models 2 and 3), the 8809 Model 1B must include a multi-drive feature as shown in Figure 9. In an 8100 system, the 8809 Model 1B and the Model 1A are mutually exclusive.

**Model 2** is the second or fourth unit in a series and contains no power. It connects to an 8809 Model 1A, 1B, or 3.

**Model 3** is the third unit in a series. It connects to an 8809 Model 2 and contains power for itself and the fourth tape unit in the series, an 8809 Model 2.



\*Required if additional drives (Models 2 and 3) are attached.

Figure 10. Typical Configurations for an IBM 8809 Attached to an IBM 8100 Information System

## 8809 Adapter Introduction

The 8809 adapter implements both halfword programmed I/O (PIO) operations and channel I/O (CHIO) operations to transfer data and control information between a program and the 8809 adapter or an 8809 tape unit. The 8809 adapter includes a halfword basic status register (BSTAT) that records and controls the operational status of the adapter. Other registers control data transfers between individual tape units and processor storage. The 8809 adapter includes logic that receives control signals from the processor's channel logic during PIO and CHIO operations, and returns the appropriate responses to ensure that these operations go in the proper sequence.

The 8809 adapter includes two data buffers, each containing 256 bytes of temporary storage. These buffers are used during CHIO data transfer operations between a tape unit and processor storage to temporarily hold blocks of data being transferred. One buffer is also used during the programmed access of 8809 sense and status data.

When a CHIO operation or an 8809 operation is completed, or when an error condition is detected by the 8809 adapter and recorded in its basic status register, the 8809 adapter presents I/O interrupt requests to the processor to show that these conditions are present.

## 8100 System Control Facility (SCF) Overview

A brief introduction to the system control facility (SCF) follows to present the concepts about the SSCF usage 4 that is contained in the 8809 Model 1B and the SSCF usage 3 to which the 8809 adapter is attached when the 8809 Model 1A is a part of the 8100 system. The SCF resides logically between the processor's channel logic and the programmable I/O adapters and features of the 8100 system. The SCF is described in detail in the *8130* and *8140 Processor Description* manuals.

The SCF consists of one primary system control facility (PSCF) and one or more secondary system control facilities (SSCFs). The PSCF always resides in the 8130 or 8140 Processor; the SSCFs are contained in the processor, in all 8101 Storage and I/O Units, and in the 8809 Magnetic Tape Unit, Model 1B.

In each unit, the SSCFs are used in four distinct ways to attach specific groups of components or features. Because the SSCFs are individually addressable through programming, these four uses describe each SSCF, as shown in Figure 11. All SSCFs have the same functions and capabilities; each usage is separately identified to simplify the description and to eliminate confusion when the specific use of an SSCF is referred to.

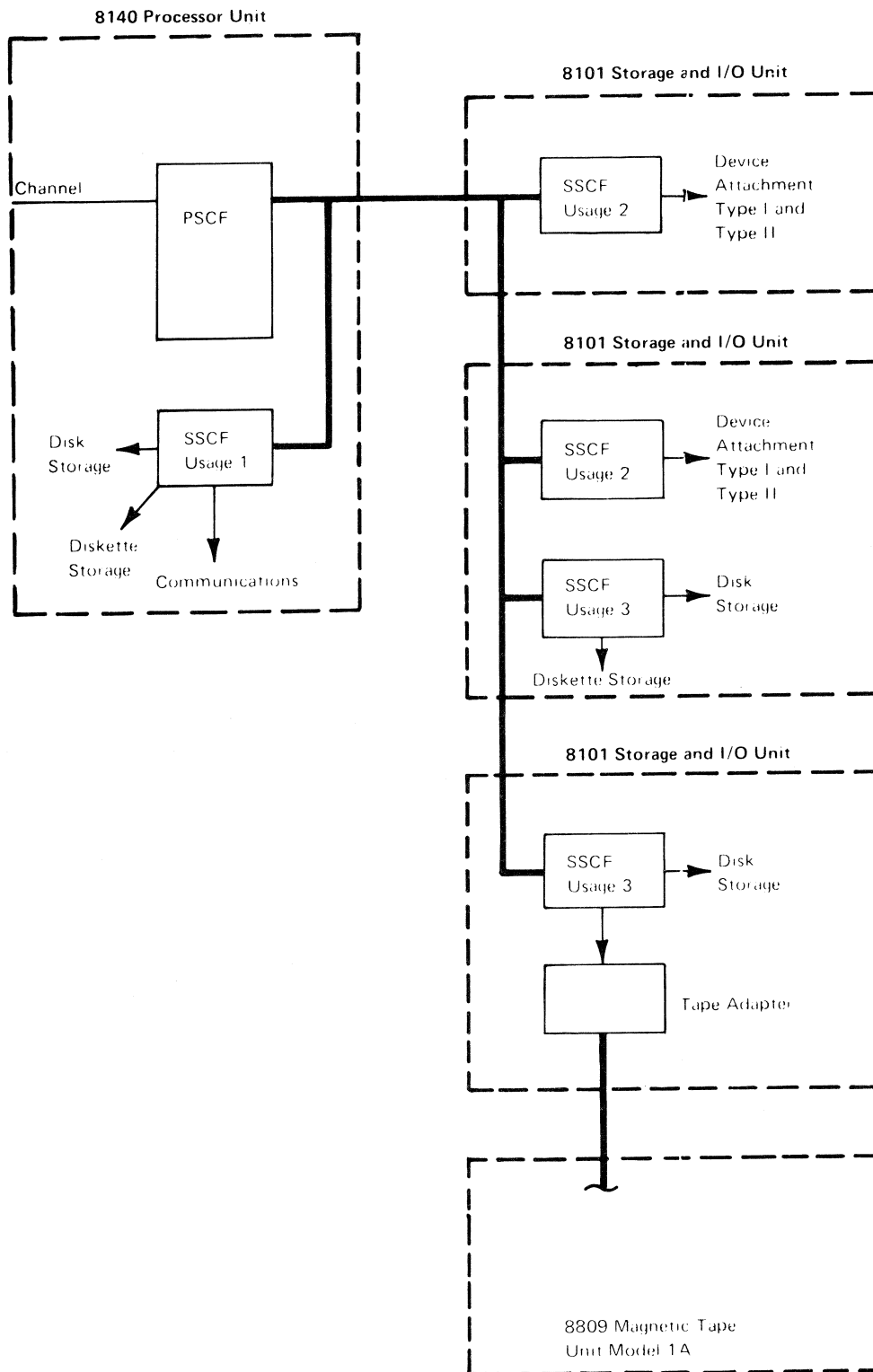
Figure 11 shows SSCFs classified according to use. The use identifies the components that can attach to that SSCF and provides a general guide to the location of that SSCF.

SSCF Usage	Attachable Components/Features	Location
Usage 1	Communications attachment features, disk storage, diskette storage	8130 Note
Usage 1	Communications attachment features, disk storage, diskette storage	8140
Usage 2	Communications attachment features, display and printer attachment feature	8101
Usage 3	Disk storage, diskette drive attachment feature, magnetic tape attachment feature	8101
Usage 4	8809 adapter	8809-1B
<b>Note:</b> For 8130 Processors without the System Expansion feature, SSCF functions are supplied through hardware, as described in the 8130 Processor Description manual.		

**Figure 11. SSCF Usage**

Figure 12 gives an overview of an 8100 system with an 8140 Processor, three 8101 Storage and I/O Units, and one Model 1A 8809 Magnetic Tape Unit. The SSCF usage 1 in the 8140 Processor attaches communications attachment features, disk storage, and diskette storage. The SSCF usage 2 in the upper 8101 attaches communications attachment features and the display and printer attachment feature (shown as Device Attachment Type I and Type II). The SSCF usage 2 in the center 8101 attaches communications attachment features. The SSCF usage 3 in that 8101 attaches disk storage and the diskette drive attachment feature. The SSCF usage 3 in the lower 8101 attaches disk storage and the tape adapter for the 8809 Model 1A.

The configuration shown in Figure 12 is provided only as an example of the SCF. This example is not to be used as a restrictive definition of an 8100 system configuration. As an alternative, magnetic tape units can be attached to the SCF signal bus using an 8809 Model 1B that contains an SSCF usage 4 and 8809 adapter.



**Figure 12. Example 8100 Configuration**

## 8809 PIO Address Assignments

A programmed I/O (PIO) address is defined for each SSCF and for each addressable adapter or feature contained in an 8101. The PIO address is specified as an operand of the three Input/Output instructions as described in the *8100 Principles of Operations* manual. These PIO addresses are used during programmed I/O operations to identify the specific adapter or feature to which the PIO command and data is being directed. The format of a PIO address follows:

### Programmed I/O Address

0 1 2 3    4 5 6 7

SSCF	Control
Address	Address
Field	Field

**SSCF Address Field** identifies the SSCF to which the selected adapter is attached, or to which the I/O instruction is directed.

**Control Address Field** identifies the specific adapter or feature to which the I/O instruction is directed. The value X'8' is assigned to the SSCF; the values X'0' through X'7' and X'9' through X'F' are assigned to the adapters and features that are attached to the SSCF.

The PIO address assignment for the 8809 adapter is determined by the 8100 system component in which it is contained. The 8809 adapter can be contained in an 8101 Storage and I/O Unit, or in an 8809 Model 1B; only one 8809 adapter can be included in an 8100 system.

The PIO address assignments for an 8809 adapter that is contained in an IBM 8101 follow:

Location	8809 Adapter PIO address (hex)
8101*1	93
8101*2	A3
8101*3	B3
8101*4	C3

Note that 8101\*1 through 8101\*4 are selected with a unique specify codes when the 8100 system is ordered. These specify codes define the address groups assigned to each 8101 and distinguish between 8101 units. Refer to the *8100 System Configurator* for additional information about configuring an 8100 system and placing an 8100 system order.

The 8809 adapter contained in an 8809 Model 1B tape unit is assigned the PIO address X'73' and is attached to the SSCF usage 4 that is also contained in the 8809 Model 1B. The SSCF usage 4 is separately addressable; it is assigned the PIO address X'78'.

## 8809 Tape Unit Addresses

Each 8809 is assigned a 3-bit binary tape unit address during installation. The 8809 tape unit address ranges from binary 000 through 111. It is used by a program to select the specific 8809 tape unit that is to perform one or more 8809 operations.

All 8809 tape units are manufactured with tape unit address binary 000. During installation, you must provide maintenance personnel with the tape unit address assignments to be used in your 8100 system. Both the licensed programs, DPPX/BASE and DPCX, require that the 8809 Model 1A or 1B be assigned tape unit address binary 000; the remaining 8809 tape units should be numbered sequentially as binary 001, 010, and 011, respectively.

The 8809 tape unit address is specified in the data operand that accompanies the PIO command Execute 8809 Selection Operation (X'6C'). Use of this command is described later in this chapter in "PIO Commands Used to Initiate 8809 Operations."

## Programmable Priority Levels

The SSCF provides the ability to assign the 8809 adapter to a specific priority level through programming. At the same time, the sublevel assignment provides a unique identification for interrupt requests presented by that adapter. The priority level assignment determines the processor priority level for which an interrupt request from a specific adapter is presented. The sublevel value does not participate in the presentation of an interrupt request; rather, it is accessed through programming after an interruption has occurred to determine specifically which adapter or adapters have interrupt requests active for a specific priority level.

The programmable priority levels are supplied through the interrupt translation array in each SSCF. Components are assigned to specific locations in the eight-position array by the control address field value of their PIO addresses.

The 8809 adapter is assigned to interrupt translation array location 3 in the SSCF usage 3 or 4 to which it is attached.

The use of the interrupt translation array in presenting I/O interrupts to the processor and the PIO commands used to load its locations is described in detail in the *8130* and *8140 Processor Description* manuals and is therefore not duplicated in this section.

## Requests to Initiate Channel I/O Operations

The SSCF defines the channel I/O request priority for each directly attached adapter or feature. This request priority is defined in two ways: through the channel request priority (CRP) value assigned to each SSCF, and by the assignment of each adapter that implements channel input/output (CHIO) operations to one of three request priority chains. These channel request chains are termed the CR-high, CR-medium, and CR-low chain. The SSCFs use their assigned CRP value, and the priority of the chain on which a CHIO request is presented, to resolve the request priority when more than one adapter is presenting a channel request. The resolution of CHIO request priority is described in detail in the *8130* and *8140 Processor Description* manuals and is therefore not duplicated here.

The SSCF usage 4 in the 8809 Model 1B is assigned the CRP value X'C'. The 8809 tape adapter is attached to the CR-low channel request chain.

The SSCF usage 3 in an 8101 that attaches the 8809 adapter for the 8809 Model 1A is assigned CRP value X'B'. The 8809 adapter is assigned to the CR-low channel request chain in this SSCF.

This SSCF may also attach disk, and/or diskette storage; the 8809 adapter is connected last on the CR-low channel request chain. The 8809 adapter is

therefore last to receive a channel grant signal for the CR-low channel request chain, and has the lowest channel request priority among the features and adapters that are attached to this SSCF.

## 8809 Adapter Registers

This section describes the registers in the 8809 adapter that are used during programmed operations and error recovery sequences. Each register is described by the significance of its contents, how it is accessed, and how it is changed through programming. All 8809 adapter registers are reset to X'00' during execution of the Reset 8809 Adapter command (X'02') and by system reset.

### *Basic Status Register (BSTAT)*

The 8809 adapter implements a halfword basic status register (BSTAT) that records error conditions detected by the 8809 adapter, or that are signaled by the 8809 tape unit. Other BSTAT bits control and record the operational status of the 8809 adapter. Figure 13 shows a summary of the BSTAT bits and is followed by the individual bit descriptions.

BSTAT Bit	Description
0	Control Channel Pointer (CHP) Update Halted
1	Invalid Command/FCB Error
2	Parity Check Detected
3	8809 Sequence Check
4	Poll Response/CHIO Check
5	Length Error
6	8809 Disconnect Operation
7	Overflow/Underflow
8	Normal End/End Op
9	8809 Ending Status Not Equal to Zero
10	Timeout
11	8809 End Error
12	Program-Requested Interrupt (PRI)
13	Tape Equipment Check
14	Tape Enabled
15	Tape Interrupt Request

**Figure 13. Basic Status Register Bit Summary**



<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Control Channel Pointer (CHP) Update Halted	Set when the halt signal is received during a channel I/O read direct operation to the control channel pointer.
1	Invalid Command/FCB Error	<p>Set when:</p> <ul style="list-style-type: none"> <li>• An invalid PIO signal sequence occurs.</li> <li>• An invalid PIO command is received; BSTAT bit 13 (tape equipment check) is also set.</li> <li>• 8809 operation bits 5 through 7, byte 0 halfword 0 do not match bits 1 through 3, byte 0 halfword 1 in the channel I/O control operation.</li> <li>• The data transfer operation does not follow an Execute 8809 read or write block control operation.</li> <li>• A new control operation is received and the end of data flag is 0 in the current data transfer operation.</li> <li>• If bit 4 equals 1, or if bits 5 through 7 in a CHIO control operation equals 011, this bit is set.</li> </ul>
2	Parity Check Detected	<p>Set when a parity error is sensed inside the 8809 adapter. If the error is on information to the processor, parity is corrected before transmission to the processor, and the operation is ended. If the error occurs on information to the tape unit, bit 3 is also set, parity is corrected before transmission, one byte is transferred, and the operation is ended.</p> <p>This bit is also set when the 8809 adapter senses a parity check on data received during a PIO write operation. In this case, the 8809 adapter sets this BSTAT bit and suppresses the response for the data, causing an I/O timeout. When the processor's channel logic senses the I/O timeout condition, it sends the halt signal to end the PIO operation and causes a system check interrupt request to be presented to the processor. When the halt signal is received, the 8809 adapter does not set BSTAT bit 13 (tape equipment check).</p>

Bit	Designation	Interpretation
3	8809 Sequence Check	<p>Set when:</p> <ul style="list-style-type: none"> <li>• The wrong 8809 tape unit responded to an 8809 selection operation.</li> <li>• A parity error is detected on information from the tape unit. Bit 2 is also set.</li> <li>• A lack of response causes a timeout error. BSTAT bit 10 is also set.</li> <li>• A programmed I/O command other than hexadecimal 02, 04, 06, 07, 08, 0A, 14, or 16 is received when the 8809 adapter is busy with a channel I/O operation or an 8809 operation.</li> <li>• No 8809 tape unit is selected when an 8809 operation, other than selection, is initiated.</li> <li>• A Select operation is received when an 8809 tape unit is selected.</li> <li>• An expected signal was not returned by the selected 8809 tape unit at the end of the operation.</li> </ul>
4	Poll Response/CHIO Check	<p>Set when a response to an 8809 Poll operation is received. This bit is also set when the halt signal is received during a (CHIO) read direct operation to the control CHP or CHIO access of the FCB.</p>
5	Length Error	<p>During an 8809 read block operation, this bit is set when the number of bytes transferred by the tape unit is not equal to the byte count, and the suppress incorrect length flag is not set.</p>
6	8809 Disconnect Operation	<p>Set when the 8809 adapter initiated an 8809 immediate disconnect operation with the selected 8809 tape unit.</p>
7	Overrun/Underrun	<p>Set when service to the processor is delayed, and the 8809 adapter does not have sufficient buffer space or data to continue transferring data from or to the tape unit.</p>
8	Normal End/End Op	<p>Set when an 8809 operation completes normally. This bit is set when:</p> <ul style="list-style-type: none"> <li>• The operation completes normally, but the 8809 ending status does not equal X'0'.</li> <li>• The 8809 immediate disconnect operation is initiated with the selected 8809 tape unit.</li> <li>• A CHIO control operation, End Op, completes.</li> </ul>
9	8809 Ending Status Not Equal to Zero	<p>Set when an 8809 operation completes normally, but the 8809 ending status is not equal to X'00'. Bit 8 or bit 11 is also set. CHIO operations are ended when this condition is sensed. The contents of the control line bus in register identify why this bit is set.</p>

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
10	Timeout	Set when: <ul style="list-style-type: none"> <li>Approximately one second has elapsed since receipt of the PIO command, Enable 1-Second Interrupt.</li> <li>An 8809 operation did not complete within 6 seconds. BSTAT bit 3 is also set.</li> </ul>
11	8809 End Error	Set when the 8809 tape unit signals that an error was sensed during execution of an 8809 operation.
12	Program-Requested Interrupt (PRI)	Set when the program-requested interruption (PRI) flag is one in a CHIO control operation.
13	Tape Equipment Check	Set when the 8809 adapter receives the halt signal during a CHIO operation or receives an invalid PIO command. This bit is not set when a PIO command is received in even parity or when the halt signal is received during a PIO operation. This bit does not cause an interrupt request to be presented to the processor.
14	Tape Enabled	Set to allow the 8809 adapter to make interrupt requests and initiate channel requests. When the bit is reset, the 8809 adapter cannot perform CHIO operations or present interrupt requests. This bit does not cause an interruption.
15	Tape Interrupt Request	This bit is set when any BSTAT bit 0 through 12 is one, and when BSTAT bit 13 is set by an invalid PIO command.

### ***Burst Length Register***

The burst length register contains a 3-bit binary code that determines the length of each channel I/O burst transfer. The Load Burst Length Register command (X'2C') provides a means to load a new burst length value into this register; the Read Burst Length Register command (X'2F') returns the contents of the burst length register to the program. The contents of this register follows:

<b>Burst Length Value</b>	<b>Number of Halfwords Per Burst</b>	<b>Number of Bytes Per Burst</b>
000	2	4
001	2	4
010	4	8
011	8	16
100	16	32
101	32	64
110	64	128
111	128	256

### ***Processor Buffer Address Register***

The processor buffer address register determines the location of data that is accessed from the 8809 adapter's data buffer being used to transfer data to or from processor storage. It is one byte in length. The PIO command, Set

Processor Buffer Address Register (X'34'), places a new value into this register; the command, Read Processor Buffer Address Register (X'37'), returns the contents of this register to the program. The processor buffer address register is usually controlled by the 8809 adapter; however, when 8809 tape unit sense and/or status data is being retrieved, the contents of this register must be set to X'00' by the program so the desired 8809 tape unit sense and status data can be accessed. This programmed sequence is described later in this chapter in "8809 Tape Unit Sense and Status Data."

### ***Byte Count Register***

The byte count register contains a hexadecimal value that represents the number of bytes of data that remain to be transferred during a channel I/O operation. It is two bytes in length; bits 0 through 3 are not implemented, bits 4 through 15 contain the byte count value. When a CHIO operation is initiated, the byte count value is loaded using either of the following CHIO data transfer operations: Load New Byte Count or Load New Address into Data CHP Bytes 2, 3. As the CHIO burst transfers occur, the 8809 adapter automatically updates the contents of this register until it contains zero. If the End-of-Data flag is active when the byte count value is decremented to 0, the CHIO data transfer is ended; if the End-of-Data flag is inactive, the 8809 adapter accesses the next data transfer operation from the function control block (FCB) to define the next byte count value. The PIO command, Read Byte Count Register (X'4B'), returns the contents of the byte count register to the program.

### ***Control Channel Pointer (CHP) Number Register***

This register contains the number of the channel pointer (CHP) that is used to access control operations and data transfer operations from the function control block (FCB) during subsequent channel I/O operations. The 8809 adapter uses the contents of this 8-bit register to generate the CHP value in the control channel control vector (CHCV) that is returned to the processor's channel logic as each CHIO burst is initiated to access the contents of the FCB. The contents of this register are numbered as bits 8 through 15.

The PIO command, Load Control CHP Number Register (X'50'), causes the 8809 adapter to load byte 1 of the data received from the program into the control CHP number register. The PIO command, Read Control CHP Number Register (X'53'), returns the contents of the control CHP number register to the program.

**Programming Note:** Bits 8 and 9 of this register must contain zeros. If bit 8 or 9 contains a one during CHIO operations, a system check will occur. Bits 10 through 15 contain the CHP number.

### ***Data Channel Pointer (CHP) Number Register***

This register contains the number of the channel pointer (CHP) that is to be used to access a data area or data areas during subsequent channel I/O (CHIO) operations. The contents of this register are numbered as bits 8 through 15. The 8809 adapter uses the contents of this register to generate the CHP value used in the data channel control vector (CHCV) that is returned to the processor's channel logic as each CHIO burst is initiated to transfer data to or from processor storage.

The PIO command, Load Data CHP Number Register (X'58'), causes the 8809 adapter to load byte 1 of the data received from the program into the data CHP number register. The PIO command, Read Data CHP Number Register (X'5B'), returns the contents of the data CHP number register to the program.

**Programming Note:** Bits 8 and 9 of this register must contain zeros. If bit 8 or 9 contains a one during CHIO operations, a system check will occur. Bits 10 through 15 contain the CHP number.

### ***Control Line Bus In Register***

This register provides programmed access to certain conditions detected by the 8809 tape unit as 8809 operations are being performed. When an 8809 operation ends with BSTAT bit 11 (8809 end error) set, the contents of this register are as follows:

Bit 0	Data Overrun
Bit 1	Data Check
Bit 2	Not Used
Bit 3	Beginning-of-Tape (BOT)
Bit 4	End-of-Tape (EOT)
Bit 5	Tape Mark Detected (read or space block operation)
Bit 6	Not Capable
Bit 7	Not Used

When an 8809 operation ends with BSTAT bit 9 (8809 ending status does not equal 0), only bits 3 (BOT) and 4 (EOT) have significance; the remaining bits are reserved in this case. The PIO command, Read Control Line Bus In Register (X'61') causes the contents of this register to be returned to the program. The 8809 adapter and the selected 8809 tape unit determine the contents of this register as a result of 8809 operations.

## **8809 Programmed Input/Output (PIO) Operations**

Programs running in the 8130 or 8140 processor initiate PIO operations with the 8809 adapter by executing I/O instructions to direct a byte or halfword of data to the 8809 adapter. The processor's channel logic exchanges control signals with the 8809 adapter to ensure that data and control information are presented in the correct sequence. The PIO command issued by the program determines whether data is transferred to or from the 8809 adapter. The specific PIO commands executed by the 8809 adapter are described in this section; all other PIO commands are invalid. A system check interruption in the processor results from sending an invalid PIO command code to the 8809 adapter.

**Note:** *The 8809 adapter does not implement byte controls for write-type PIO commands. Only the PIO commands, hex 02, 04, 06, and 07, should be issued using byte-type I/O instructions. All other PIO commands should be issued to the 8809 adapter using the Input/Output Halfword (IOH) instruction.*

The description of individual PIO commands is preceded by a summary of all the PIO command implemented by the 8809 adapter. Some PIO commands are used to access or change the contents of a register in the 8809 adapter because they transfer only a byte or a halfword of data during their execution. Other PIO commands are used to prepare the 8809 adapter for a channel I/O (CHIO) operation, to initiate a CHIO operation, and to terminate a CHIO operation in progress. These commands are described in "PIO

Command Description.” A third category of PIO commands is used to select a specific 8809 tape unit and to initiate one of several categories of 8809 operations. These commands are included sequentially in the PIO command summary, and are described at the end of the PIO description in “PIO Commands Used to Initiate 8809 Operations.”

**Programming Note:** Only the following PIO commands can be issued to the 8809 adapter when a CHIO operation or an 8809 operation is in progress. The 8809 adapter is busy with an 8809 operation from the time the operation is begun until either BSTAT bit 8 (normal end/end op) or BSTAT bit 11 (8809 end error) is set. Issuing any other PIO commands when the 8809 adapter is busy with a CHIO operation or an 8809 operation results in setting basic status register bit 3 (8809 sequence check) and 15 (tape interrupt request). The response for the command is suppressed, forcing an I/O timeout. When the processor’s channel logic detects the I/O timeout condition, it sets bit 1 (I/O timeout check) in the processor’s error interrupt request vector to cause a system check interruption. The only commands permitted when the 8809 adapter is busy are:

- Reset 8809 Adapter (X’02’)
- Reset BSTAT 8-15 Under Mask (X’04’)
- Set BSTAT 8-15 Under Mask (X’06’)
- Read Basic Status Register (X’07’)
- Enable 1-Second Interrupt (X’08’)
- Terminate CHIO (X’0A’)
- Reset BSTAT Under Mask (X’14’)
- Set BSTAT Under Mask (X’16’)

PIO Command	Hex	Data Transferred			
		Byte 0		Byte 1	
		0	7	8	15
Reset 8809 Adapter	02	No data transferred			
Reset BSTAT 8-15 Under Mask	04	Ignored		Mask	
Set BSTAT 8-15 Under Mask	06	Ignored		Mask	
Read Basic Status Register	07	BSTAT Byte 0		BSTAT Byte 1	
Enable 1-Second Interrupt	08	No data transferred			
Terminate CHIO	0A	No data transferred			
Reset BSTAT Under Mask	14	Mask Byte 0		Mask Byte 1	
Set BSTAT Under Mask	16	Mask Byte 0		Mask Byte 1	
Load Burst Length Register	2C	Bits 0-12 are ignored; bits 13-15 – C C C			
Read Burst Length Register	2F	Bits 0-12 are zeros; bits 13-15 – C C C			
Disconnect 8809	30	No data transferred			
Set Processor Buffer Address Register	34	Ignored		X'00'	
Read Processor Buffer Address Register	37	X'00'		BAR value	
Read Byte Count Register	4B	Bits 0-3 – 0; bits 4-15 – Byte Count			
Load Control CHP Number Register	50	Ignored		CHP Number	
Read Control CHP Number Register	53	X'00'		CHP Number	
Load Data CHP Number Register	58	Ignored		CHP Number	
Read Data CHP Number Register	5B	X'00'		CHP Number	
Read Control Line Bus In Register	61	X'00'		Register Data	
Execute 8809 Poll Operation	66	X'12'		X'00'	
Read Buffer	69	Buffer Data		Buffer Data	
Execute 8809 Selection Operation	6C	X'A3'		8809 address	
Execute 8809 Immediate Operation	6E	X'31'		8809 operation	
Execute 8809 Immediate Disconnect Operation	74	X'41'		8809 operation	
Execute 8809 Non-Data Operation	76	X'51'		8809 operation	
Initiate CHIO	7C	No data transferred			
<b>Note:</b> The following hexadecimal command codes are reserved for maintenance use: 10, 24, 27, 38, 3A, 3C, 3F, 48, 54, 57, 5C, 5F, 62.					

**Figure 14. 8809 PIO Command Summary**

## **8809 PIO Command Description**

### **Reset 8809 Adapter X'02'**

The 8809 adapter stops any current CHIO operation, ends selection of the 8809 tape unit, resets BSTAT, resets all mode and condition latches, and disables the 1-second interrupt logic. The following registers are initialized to hex zeros. The system reset input line performs the same function.

- Basic Status Register
- Burst Length Register
- Byte Count Register
- Control Channel Pointer Number Register
- Control Line Bus In Register
- Data Channel Pointer Number Register
- Processor Buffer Address Register

### **Reset Basic Status Register 8-15 Under Mask X'04'**

8809 BSTAT bits 8-15 are reset when their corresponding mask bits are one. BSTAT bits 0-7 are unaffected. BSTAT bit 15 is not reset if any BSTAT bit from 0 through 12 is one when this command is completed.

### **Set Basic Status Register 8-15 Under Mask X'06'**

8809 BSTAT bits 8-15 are set when their corresponding mask bits are one. BSTAT bits 0-7 are unaffected. BSTAT bit 15 is set if any BSTAT bit from 0 through 12 is one when this command is completed.

### **Read Basic Status Register X'07'**

The contents of the basic status register are returned to the program in the specified register. If this command is issued with a byte-type I/O instruction, bits 8-15 of the 8809 BSTAT are returned to the program in byte 1 of the specified register.

### **Enable 1-Second Interrupt X'08'**

Approximately 1 second after executing this command, the 8809 adapter sets BSTAT bits 10 (timeout) and 15 (8809 interrupt request) to present an interrupt request to the processor.

### **Terminate CHIO X'0A'**

The 8809 adapter terminates the current CHIO operation at the completion of the current control operation or data transfer operation.

### **Reset Basic Status Register Under Mask X'14'**

8809 BSTAT bits 0 through 15 are reset when their corresponding mask bits are one. BSTAT bit 15 is not reset if any BSTAT bits from 0 through 12 are one when this command is completed.

### **Set Basic Status Register Under Mask X'16'**

8809 BSTAT bits 0 through 15 are set when their corresponding mask bits are one. BSTAT bit 15 is also set if any BSTAT bits from 0 through 12 are one at the completion of this command.



### **Load Burst Length Register X'2C'**

Bits 0 through 12 of the data operand received from the program are ignored; bits 13 through 15 are set in the burst length register. The significance of bits 13 through 15 for determining the burst length follows:

<b>Burst Length Register</b>	<b>Number of Halfwords per Burst</b>	<b>Number of Bytes Transferred per CHIO Burst</b>
000	2	4
001	2	4
010	4	8
011	8	16
100	16	32
101	32	64
110	64	128
111	128	256

### **Read Burst Length Register X'2F'**

Byte 0 of the returned data is set to X'00'. Byte 1, bits 8 through 12 are also set to zeros. Byte 1, bits 13 through 15 contain the present value in the burst length register.

### **Disconnect 8809 X'30'**

This command may be issued when an 8809 tape unit is performing the delayed portion of an 8809 immediate disconnect operation. The Disconnect 8809 command ends selection with the selected 8809 tape unit to permit the selection of another 8809 tape unit and other 8809 operations to proceed while the original 8809 tape unit completes the delayed portion of an immediate disconnect operation such as rewind, rewind unload, and so on.

8809 operations are described later in this chapter in "8809 Operations."

### **Set Processor Buffer Address Register X'34'**

This command permits the program to reset the 8809 adapter's processor BAR to X'00' during an 8809 sense and status retrieval sequence that is described later in this book in "8809 Tape Unit Sense and Status Data." Byte 0 of the data received is ignored. This command is used by maintenance Use of this command to set values other than X'00' into the processor BAR is reserved for maintenance use.

### **Read Processor Buffer Address Register X'37'**

The contents of the processor buffer address register are returned to the program in byte 1 of the returned data; byte 0 is returned as X'00'.

### **Read Byte Count Register X'4B'**

The contents of the byte count register are returned to the program in bits 4 through 15 of the returned data; bits 0 through 3 are returned as zeros. This command provides a means to determine the residual byte count when an incorrect length indication is returned at the end of an 8809 read block operation.

### **Load Control Channel Pointer Number Register X'50'**

This command causes the 8809 adapter to load byte 1 of the data received from the program into the control CHP number register. Byte 0 of the received data is ignored. Bits 8 and 9 of byte 1 must be set to zeros; bits 10 through 15 of byte 1 contain the CHP number in binary.

**Programming Note:** A system check interruption is caused by the processor's channel logic because of a CHCV format violation if control CHP number register bits 8 or 9 are one during CHIO operations.

### **Read Control Channel Pointer Number Register X'53'**

The contents of the control CHP number register are returned to the program in byte 1; byte 0 is returned as X'00'.

### **Load Data Channel Pointer Number Register X'58'**

This command causes the 8809 adapter to load byte 1 of the data received from the program into the data CHP number register. Byte 0 of the received data is ignored. Bits 8 and 9 of byte 1 must be set to zeros; bits 10 through 15 of byte 1 contain the CHP number in binary.

**Programming Note:** A system check interruption is caused by the processor's channel logic because of a CHCV format violation if data CHP number register bits 8 or 9 are one during CHIO operations.

### **Read Data Channel Pointer Number Register X'5B'**

The contents of the CHP number register are returned to the program in byte 1 of the returned data; byte 0 is returned as X'00'.

### **Read Control Line Bus In Register X'61'**

The contents of the control line bus in register are returned to the program in byte 1 of the returned data; byte 0 is returned as X'00'.

### **Read Buffer X'69'**

This command causes the 8809 adapter to return a halfword of data from its data buffer to the program. The location of the halfword of data that is returned is the value in the processor buffer address register.

**Programming Note:** This command is used to retrieve 8809 sense and status data as described later in this book in "8809 Tape Unit Sense and Status Data." Use of this command to retrieve other information from the data buffer is reserved for maintenance use.

### **Initiate Channel I/O X'7C'**

This command causes the 8809 adapter to begin a CHIO operation when the execution of this command is completed. The 8809 adapter ignores any data sent by the program. CHIO operations are described later in this chapter in "8809 Channel I/O Operations."

**Programming Note:** This command causes the 8809 adapter to become busy and to remain busy until the CHIO operation is completed. During the time the 8809 adapter is busy, only the following PIO commands can be executed: hexadecimal 02, 04, 06, 07, 08, 0A, 14, 16. If other PIO commands are sent to the 8809 adapter while it is busy, a system check interruption occurs because the 8809 adapter suppresses the response for the command to cause an I/O timeout condition.

## ***PIO Commands Used to Initiate 8809 Operations***

The programmed I/O (PIO) commands described in this section transfer an 8809 operation to the 8809 adapter and begin execution of that 8809 operation. When one of these commands is issued, the 8809 adapter is busy until the command is completed. Completion of one of the 8809 operations is indicated by an interrupt request from the 8809 adapter to the program. The 8809 adapter's basic status register (BSTAT) indicates whether the 8809 operation was completed without error, or if an error condition was detected during the execution of that 8809 operation.

**Programming Note:** The following PIO commands are the only ones that are permitted during the execution of an 8809 operation or a CHIO operation. If other PIO commands are received when the 8809 adapter is busy, that is, before it presents an interrupt request at the completion of the operation, a system check interruption is caused by the 8809 adapter. The PIO command codes that can be issued when the 8809 adapter is busy are: hexadecimal 02, 04, 06, 07, 08, 0A, 14, 16.

This section does not describe individual 8809 operations; only the PIO commands that send 8809 operations from the program to the 8809 adapter are described here. The individual 8809 operations are described later in this section in "8809 Operations." The 8809 operations listed in this section identify the data that is transferred during the execution of the PIO commands.

**Note:** *Only the 8809 operations listed in this section are valid. If other codes are sent to the 8809 adapter as 8809 operations, unpredictable 8809 operation can result.*

Each PIO command described in this section identifies one category of 8809 operation that is to be performed. Some PIO commands can specify only a single operation such as Execute 8809 Poll Operation and Execute 8809 Selection Operation. Other commands identify the category of command that is to be executed, and specify the selected 8809 operation in the halfword of data that is transferred during execution of the PIO command. The Execute 8809 Immediate Operation, Execute 8809 Immediate Disconnect Operation, and the Execute 8809 Non-Data Operation are each issued to send one specific 8809 operation from the selected category to the 8809 adapter for execution.

The remainder of this section describes the format of the PIO commands that send 8809 operations to the 8809 adapter. The PIO command code is shown in the leftmost column, followed by a description of each command code.

## PIO Command Code

(in hex)

66

### Description

Execute 8809 Poll Operation. This operation identifies the tape unit(s) in which the 8809 status bit 5 (operation complete) is equal to 1. The 8809 tape unit status bit 5 is set at the completion of the second stage of an immediate disconnect operation, and when a new tape is mounted and made ready on the tape unit. The program sends X'1200' as the data transferred during execution of this command; this data causes the 8809 adapter to perform a poll operation with the attached tape units. Each 8809 tape unit with status bit 5 (operation complete) equal to 1 sets a unique bit in the control line bus in register that corresponds to its 8809 tape unit address as follows:

Tape Unit Address	Control Line Bus In Register Bit Activated
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

The 8809 adapter places the contents of the control line bus in register into byte 0 of the buffer. If one or more 8809 tape units responded to the poll operation, the 8809 adapter sets BSTAT bit 4 (poll response/CHIO check), bit 8 (normal end/end op), and bit 15 (tape interrupt request) to notify the program that the operation is complete. If no 8809 tape units respond to the poll operation, the 8809 adapter does not set BSTAT bit 4.

**Programming Note:** The 8809 Poll Operation can begin only with the PIO command X'66'; it cannot begin during a CHIO operation. Byte 0 of the 8809 adapter's buffer identifies the address or addresses of 8809 tape units that can perform 8809 operations at this time. This byte of data is accessed as follows:

- Issue the PIO command Set Processor Buffer Address Register (X'34') to set the BAR to X'00'.
- Issue the Read Buffer command X'69' to retrieve the data in the buffer. Active bits in byte 0 of the returned data reflect the tape unit address(es) of the tape unit(s) that responded to the poll operation; byte 1 contains information from byte 1 of the buffer and should be ignored.

**PIO Command Code****(in hex)****Description**

6C

Execute 8809 Selection Operation. This command causes the 8809 adapter to begin a selection operation with the 8809 tape unit identified in byte 1 of the data operand sent with this command. Byte 0 of the data must contain X'A3'; bits 8 through 10 of the data contain the 3-bit binary address of the 8809 tape unit that is to be selected. Bits 11 through 15 must be zeros. The 8809 selection operation causes the Select light to turn on at the selected 8809 tape unit. Only one 8809 tape unit can be selected at a time. When the selection operation is complete, the 8809 adapter sets BSTAT bit 8 (normal end/end op) and bit 15 (tape interrupt request) to notify the program.

**Programming Note:** This command must be sent to an 8809 tape unit before other 8809 operations are sent. The tape unit does not perform 8809 operations until it is selected. The 8809 selection operation can only begin with the PIO command X'6C'; this operation cannot be sent during a CHIO operation

The completion of this command is indicated by an interrupt request to the processor. The BSTAT is set to X'0083' (normal end/End Op, tape enabled, and tape interrupt request). After the program reads the BSTAT to determine the cause of the interrupt request, the selected 8809 tape unit's status byte should also be read to verify that the tape unit is ready to perform 8809 operations. Tape unit status bits 3 (beginning of tape) and 5 (operation complete) identify when the operator performs a load rewind operation. Reading the 8809 status byte is described under "8809 Tape Unit Sense and Status Data."

**PIO Command Code****(in hex)****Description**

6E

Execute 8809 Immediate Operation. This command causes the 8809 adapter to begin the 8809 operation that is identified in the halfword data operand transferred during execution of this command. The specified 8809 immediate operation is executed by the selected 8809 tape unit. The 8809 immediate operations that can be specified using this command follow in hex:

310C - diagnostic set ready

3180 - read 8809 status

3181 - read 8809 sense byte 1-15/status

3182 - read 8809 sense byte 2-15/status

**PIO Command Code**

(in hex)	Description
6E	3183 - read 8809 sense byte 3-15/status
(continued)	3184 - read 8809 sense byte 4-15/status
	3185 - read 8809 sense byte 5-15/status
	3186 - read 8809 sense byte 6-15/status
	3187 - read 8809 sense byte 7-15/status
	3188 - read 8809 sense byte 8-15/status
	3189 - read 8809 sense byte 9-15/status
	318A - read 8809 sense byte 10-15/status
	318B - read 8809 sense byte 11-15/status
	318C - read 8809 sense byte 12-15/status
	318D - read 8809 sense byte 13-15/status
	318E - read 8809 sense byte 14-15/status
	318F - read 8809 sense byte 15/status
	31E0 - check reset
	31E8 - set long gap
	31E9 - reset long gap

When the specified 8809 immediate operation is completed, the 8809 adapter sets BSTAT bit 8 (normal end/end op) with bit 15 (tape interrupt request) to notify the program.

**Programming Note:** The read 8809 status and read 8809 sense byte operations result in the specified data being loaded into the buffer of the 8809 adapter. Accessing this data is described later in this chapter "8809 Tape Unit Sense and Status Data."

These 8809 immediate operations can only start using the PIO command X'6E'; they cannot begin during a CHIO operation.

**PIO Command Code**

(in hex)	Description
74	Execute 8809 Immediate Disconnect Operation. This command causes the 8809 adapter to begin the 8809 operation that is identified in the halfword of data transferred during execution of this command. The specified 8809 immediate disconnect operation is executed by the selected 8809 tape unit in two stages. The first stage is signaled by the 8809 adapter with an interrupt request when the operation begins; the selected 8809 tape unit then completes the delayed part of the operation. 8809 immediate disconnect operations that can be specified using this command follow in hex:
	4122 - forward space file
	412A - backward space file
	41E1 - data security erase
	41E2 - set low speed

## PIO Command Code

(in hex)	Description
74	41E3 - set high speed
(continued)	41E4 - rewind
	41E5 - rewind unload

When the specified 8809 immediate disconnect operation has begun, the 8809 adapter sets BSTAT bits 6 (8809 disconnect operation) and bit 8 (normal end/end op) with bit 15 (tape interrupt request) to notify the program.

After the 8809 adapter has set BSTAT bits 6, 8, and 15, it is no longer busy with the 8809 operation. The selected 8809 tape unit, however, remains busy until the delayed part of the specified immediate disconnect operation is completed. Only 8809 immediate operations can be executed with the selected tape unit until either the selected 8809 completes the current immediate disconnect operation, or the program issues the PIO command Disconnect 8809 X'30'. (The set and reset long gap operations can be executed only when the tape unit is selected; they cannot be performed after the Disconnect 8809 command has executed.) The PIO command, Disconnect 8809, ends selection of an 8809 tape unit while the tape unit completes the delayed portion of the immediate disconnect operation in progress. After the Disconnect 8809 command has been executed, the program can select another 8809 tape unit and perform other 8809 operations with that 8809 tape unit.

When the original 8809 immediate disconnect operation is completed by the 8809 tape unit, regardless of whether it was disconnected or remained selected throughout the operation, the tape unit sets status bit 5 (operation complete). No indication is signaled by the 8809 adapter; that is, no interrupt request is presented to notify the program that the operation has completed. A programmed sequence is required to find out when the 8809 tape unit has completed the delayed part of an immediate disconnect operation. The programmed sequences that can be used are described in the following programming note.

**Programming Note:** 8809 immediate disconnect operations can begin using either the PIO command X'74' or, during a CHIO operation, using the control operation Execute 8809 Immediate Disconnect Operation.

**PIO Command Code**

(in hex)	Description
74 (continued)	<p>The presence of 8809 status bit 5 (operation complete) can be sensed using one of two programmed sequences. After an immediate disconnect operation has been sent to the selected tape unit and the initial interrupt request has been received identifying that the disconnected operation was started by the tape unit, the program can issue the PIO command, Enable 1-Second Interrupt. This command can be used to determine the rate at which either of the following programmed sequences is issued. Either sequence can be used periodically to check when the operation complete status bit is equal to 1.</p> <ol style="list-style-type: none"><li>1. The PIO command, Execute 8809 Immediate Operation (X'6E'), specifies that the read 8809 status operation can be issued to load the current status byte value of the selected tape unit into location 0 of the 8809 adapter's data buffer. The 8809 status byte can then be retrieved by issuing the PIO command, Set Processor Buffer Address Register (X'34'), to set the BAR to 0, and then issuing the PIO command, Read Buffer (X'69').</li><li>2. The PIO command, Execute 8809 Poll Operation (X'66'), can be issued to load the tape unit's poll response(s) into byte 0 of the 8809 adapter's data buffer. The PIO command, Set Processor Buffer Address Register (X'34'), must then be issued to set the BAR to 0. The tape unit's poll response(s) can then be retrieved using the PIO command, Read Buffer (X'69'). The active bits in the byte of data returned to the program from the poll operation identify the address(es) of tape units with status bit 5 (operation complete) equal to 1.</li></ol>

**PIO Command Code**

(in hex)	Description
76	<p>Execute 8809 Non-Data Operation. This command causes the 8809 adapter to begin the 8809 non-data operation identified in the halfword data operand transferred during execution of this command. The specified 8809 non-data operation is executed by the selected 8809 tape unit. 8809 non-data operations that can be specified using this command follow in hex:</p> <ul style="list-style-type: none"><li>5120 - forward space block</li><li>5128 - backward space block</li><li>5141 - erase gap</li><li>5147 - write tape mark (WTM)</li></ul>



**PIO Command Code****(in hex)****Description**76  
(continued)

When the specified 8809 non-data operation has completed, the 8809 adapter sets BSTAT bit 8 (normal end/end op) with bit 15 (tape interrupt request) to notify the program.

**Programming Note:** 8809 non-data operations can be started using either the PIO command X'76' or, during a CHIO operation, using the control operation Execute 8809 Non-Data Operation.

**8809 Channel I/O Operations**

The 8809 adapter uses channel input/output (CHIO) operations as the primary means to transfer data between processor storage and the magnetic tape. A program uses PIO commands to prepare the 8809 adapter for a CHIO operation and to identify when that CHIO operation is to be started. The 8809 adapter transfers the data asynchronously with program execution in the processor. CHIO operations are described in detail in the *8100 Principles of Operations* and are reviewed at an overview level in this section.

The 8809 adapter implements a special set of data protocols, used only during CHIO operations, that define additional control functions and specify data transfer operations that are to be performed during one CHIO operation. These control and data transfer operations are specified in processor storage in an area called a function control block.

***Function Control Block (FCB)***

The function control block (FCB) is an area in processor storage where a program has specified a list of one or more control and data transfer operations to be accessed and performed by the 8809 adapter during a subsequent CHIO operation.

The location of an FCB is identified in one of the processor's 64 channel pointers (CHPs). This CHP is termed the *control CHP*. The control CHP number is stored in the 8809 adapter's control CHP number register.

The FCB can contain two types of operations: *control operations* and *data transfer operations*.

Control operations permit the program to issue 8809 operations to a selected 8809 tape unit during a CHIO operation and to perform other 8809 adapter control functions. Data transfer operations can only follow a control operation that issues one of the 8809 data operations such as the 8809 read block or 8809 write block operation. Data transfer operations specify the amount of data that is to be transferred, and a new address to be loaded into the data CHP. (The data CHP is identified in the data CHP number register in the 8809 adapter.) The data CHP identifies the location in processor storage to which or from which data is transferred to or from the 8809 tape unit.

The control CHP is used to access control operations and data transfer operations from the FCB; the data CHP is used only during CHIO bursts to transfer data between the tape unit and processor storage.

Control operations are described in this section under two headings: “Channel I/O Control Operations” and “Channel I/O Control Operations Used to Initiate 8809 Operations.” Data transfer operations are summarized in Figure 15 and described at the end of this section in “Channel I/O Data Transfer Operations.”

Only the control operation formats shown in Figure 15 are implemented by the 8809 adapter. Use of any other control operation format results in unpredictable 8809 adapter operation.

Bit positions that contain an X are ignored and may equal 0 or 1.

### ***Control Operation Formats***

	Halfword 0				Halfword 1	
	Byte 0		Byte 1		Byte 0	Byte 1
NOP	10	P R I	X0000	XXXXXXXX	XXXXXXXX	XXXXXXXX
End Op	1X	P R I	X0001	XXXXXXXX	XXXXXXXX	XXXXXXXX
Load New Address into Control CHP Bytes 2,3	10	P R I	X0010	XXXXXXXX	FCB Address (Bytes 2,3)	
Load New Address into Control CHP Bytes 0,1	11	P R I	X0010	XXXXXXXX	FCB Address (Bytes 0,1)	
Execute 8809 Immediate Disconnect Operation	1X	P R I	X0100	XXXXXXXX	X'41'	8809 Operation
Execute 8809 Non-Data Operation	1X	P R I	X0101	XXXXXXXX	X'51'	8809 Operation
Execute 8809 Read Block Operation	1X	P R I	I L	0110	XXXXXXXX	X'61' X'21'
Execute 8809 Write Block Operation	1X	P R I	X0111	XXXXXXXX	X'71'	X'44'

**Figure 15 (Part 1 of 2). Channel I/O Control and Data Transfer Operation Formats**

## Data Transfer Operation Formats

	Halfword 0				Halfword 1	
	Byte 0		Byte 1		Byte 0	Byte 1
Load New Byte Count	00	E O D	0	Byte Count	XXXXXXXX XXXXXXXX	
Load New Address into Data CHP Byte 2,3	00	E O D	1	Byte Count	Data Area Address (Bytes 2,3)	
Load New Address into Data CHP Byte 0,1	01	E O D	1	XXXX XXXXXXXX	Data Area Address (Bytes 0,1)	

**Note:** PRI = program-requested interrupt (may be 0 or 1). IL = suppress.

**Figure 15 (Part 2 of 2). Channel I/O Control and Data Transfer Operation Formats**

## Channel I/O Control Operations

This section describes four CHIO control operations: NOP, End Op, Load New Address into Control CHP Bytes 2,3, and Load New Address into Control CHP Bytes 0,1. When each control operation is accessed, a second halfword of data is accessed by the 8809 adapter. This halfword may not be used in all cases, but the result is that each control operation is four bytes long in the FCB in which it is defined.

### Program-Requested Interrupt (PRI) Flag

All control operations include the program-requested interrupt (PRI) flag in bit 2 of the operation format. When the PRI flag is one, the 8809 adapter sets BSTAT bit 12 (program-requested interrupt) and bit 15 (tape interrupt request) to notify the program that the control operation has been accessed. This interrupt request is presented concurrently with the execution of the control operation in which the active PRI flag was accessed. The presence of the PRI flag does not modify execution of a control operation.

### NOP

Halfword 0				Halfword 1	
Byte 0		Byte 1		Byte 0	Byte 1
10	P R I	X0000	XXXXXXXX	XXXXXXXX	XXXXXXXX

When this control operation is received, the 8809 adapter does not perform any operation unless the program-requested interrupt flag is set. The next control operation is accessed by the 8809 adapter. If the PRI flag is set, the 8809 adapter also presents an interrupt request to the program concurrently with the access of the next control program.

## End Op

Halfword 0				Halfword 1			
Byte 0			Byte 1	Byte 0			Byte 1
1X	P R I	X0001	XXXXXXXX	XXXXXXXX			XXXXXXXX

When this control operation is received, the 8809 adapter ends the CHIO operation and sets BSTAT bit 8 (normal end/end op) and bit 15 (tape interrupt request) to notify the program that the CHIO operation has been completed. This control operation must be the last in an FCB.

## Load New Address into Control CHP Bytes 2,3

Halfword 0				Halfword 1			
Byte 0			Byte 1	Byte 0			Byte 1
10	P R I	X0010	XXXXXXXX	FCB Address (Bytes 2,3)			

This control operation causes the 8809 adapter to load bytes 2 and 3 of the control CHP with the contents of the second halfword of this operation. Bytes 0 and 1 of the control CHP are not changed during execution of this operation unless the Load New Address into Control CHP Bytes 0 and 1 has been received. The control CHP is identified in the control CHP number register. Either bytes 2 and 3 alone, or bytes 0 through 3 of the CHP are loaded in one CHIO burst transfer during execution of this operation.

**Programming Note:** When all four bytes of the control CHP are to be changed, this control operation must follow the Load New Address into Control CHP Bytes 0 and 1. Failure to follow this procedure results in unpredictable values being loaded into the control CHP.

## Load New Address into Control CHP Bytes 0,1

Halfword 0				Halfword 1			
Byte 0			Byte 1	Byte 0			Byte 1
11	P R I	X0010	XXXXXXXX	FCB Address (Bytes 0,1)			

This control operation must be the first of a pair of control operations used to load a new address value into bytes 0 through 3 of the control CHP. This control operation sends bytes 0,1 of the new address value to the 8809 adapter. The 8809 adapter does not modify the contents of the control CHP during execution of this control operation; instead, address bytes 0,1 are saved in the 8809 adapter.

When the 8809 adapter has saved address bytes 0,1, it continues the CHIO burst to retrieve the second control operation of the pair, Load New Address into Control CHP Bytes 2,3, from the FCB. The new FCB address is loaded into the control CHP bytes 0 through 3 in a single CHIO read-direct burst, after both control operations have been retrieved from the FCB.

**Programming Note:** This control operation cannot be issued by itself; it can be used only with the Load New Address into Control CHP Bytes 2,3 to modify the entire control CHP.

When bytes 0 through 3 of the control CHP are to be modified, this control operation must precede the Load New Address into Control CHP Bytes 2,3 control operation. Failure to follow this procedure results in unpredictable values being loaded into the control CHP.

### ***Control Operations Used to Initiate 8809 Operations***

This section describes four CHIO control operations: Execute 8809 Immediate Disconnect Operation, Execute 8809 Non-Data Operation, Execute 8809 Read Block Operation, and Execute 8809 Write Block Operation. When each control operation is accessed by the 8809 adapter, a second halfword of data is also accessed. Byte 0 of this second halfword identifies the category of 8809 operation that is to be executed; byte 1 identifies the specific 8809 operation that is to be initiated. These control operations implement the program-requested interrupt (PRI) flag as described in "Control Operations." The 8809 Read Block Operation includes an additional flag in bit 3, incorrect length (IL), of the control operation.

**Programming Note:** Before any of these control operations can be issued to an 8809 tape unit, that tape unit must be selected using the PIO command Execute 8809 Selection Operation X'6C'. Failure to follow this procedure results in no operation being performed by the 8809 tape unit(s) because no 8809 tape unit is selected.

#### **Execute 8809 Immediate Disconnect Operation**

Halfword 0				Halfword 1	
Byte 0			Byte 1	Byte 0	Byte 1
1X	P R I	X0100	XXXXXXXX	X'41'	8809 Operation

This control operation causes the 8809 adapter to start the specified immediate disconnect operation with the selected 8809 tape unit. 8809 immediate disconnect operations are performed in two stages; first, the 8809 adapter ends the CHIO operation, sets BSTAT bits 6 (8809 disconnect operation), 8 (normal end/end op), and 15 (tape interrupt request) to notify the program that the operation began with the selected 8809 tape unit. The selected 8809 tape unit then completes the second part of the operation without a need for further interaction with the 8809 adapter. The program can issue the PIO command Disconnect 8809 X'30' if 8809 operations are to be started with the remaining 8809 tape unit or units. The PIO command, Disconnect 8809 (X'30') ends selection with an 8809 tape unit and frees the 8809 adapter to select another tape unit and perform other 8809 operations. If the Disconnect 8809 command is not sent, the selected 8809 tape unit remains selected while it completes the second part of the operation.

The tape unit sets status bit 5 (operation complete) when the second part of the Immediate Disconnect operation is completed. This operation complete status does not cause the 8809 adapter to present an interrupt request to the processor. A programmed sequence is required to identify when the tape unit sets status bit 5 (operation complete). This sequence is described in the programmed note at the end of this section.

These 8809 operations are described later in this chapter in “8809 Operations.”

The 8809 immediate disconnect operations that can be started using this control operation follow in hex:

4122 - forward space file  
 412A - backward space file  
 41E1 - data security erase  
 41E2 - set low speed  
 41E3 - set high speed  
 41E4 - rewind  
 41E5 - rewind unload

**Programming Note:** This control operation ends the current CHIO operation. However, it can be followed by other control operations in the FCB. After this operation is completed, tape unit status bit 5 (operation complete) is reset with the 8809 operation, check reset, and the resulting interrupt request has been processed, the program can restart the channel I/O operation at the next control operation in the FCB by issuing the programmed I/O command, Initiate CHIO X'7C'.

The presence of 8809 status bit 5 (operation complete) can be sensed using one of two programmed sequences. After an immediate disconnect operation has been sent to the selected tape unit and the initial interrupt request has been received signifying that the disconnected operation was started by the tape unit, the program can issue the PIO command, Enable 1-Second Interrupt. This command can be used to determine the rate at which either of the following programmed sequences is issued. Either sequence can be used periodically to check when the operation complete status bit is equal to 1.

1. The PIO command, Execute 8809 Immediate Operation (X'6E'), specifies that read 8809 status operation can be issued to load the current status byte value of the selected tape unit into location 0 of the 8809 adapter's data buffer. The 8809 status byte can then be retrieved by issuing the PIO command, Set Processor Buffer Address Register (X'34'), to set the BAR to 0, and then issuing the PIO command, Read Buffer (X'69').
2. The PIO command, Execute 8809 Poll Operation (X'66'), can be issued to load the tape unit's poll response(s) into byte 0 of the 8809 adapter's data buffer. The PIO command, Set Processor Buffer Address Register (X'34'), must then be issued to set the BAR to 0. The tape unit's poll response(s) can then be retrieved using the PIO command, Read Buffer (X'69'). The active bits in the byte of data returned to the program from the poll operation identify the address(es) of tape units with status bit 5 (operation complete) equal to 1.

### Execute 8809 Non-Data Operation

Halfword 0				Halfword 1	
Byte 0			Byte 1	Byte 0	Byte 1
1X	P R I	X0101	XXXXXXXX	X'51'	8809 Operation

This control operation causes the 8809 adapter to start the specified non-data operation with the selected 8809 tape unit.

The 8809 non-data operations that can be started using this control operation follow in hex:

- 5120 - forward space block
- 5128 - backward space block
- 5141 - erase gap
- 5147 - write tape mark (WTM)

These 8809 operations are described later in this chapter in “8809 Operations.”

At the completion of the 8809 operation, the 8809 adapter accesses the next control operation from the FCB if the operation was completed successfully. If, however, the 8809 tape unit detected an error, the 8809 adapter sets BSTAT bit 9 (8809 ending status does not equal 0), bit 8 (normal end/end op) or bit 11 (8809 end error), and bit 15 (tape interrupt request) to notify the program. The CHIO operation is ended in this case.

#### Execute 8809 Read Block Operation

Halfword 0					Halfword 1	
Byte 0				Byte 1	Byte 0	Byte 1
1X	P R I	I L	0110	XXXXXXXX	X'61'	X'21'

This control operation prepares the 8809 adapter to start a read block operation with the selected 8809 tape unit. The 8809 adapter accesses the next four bytes in the FCB; a data transfer operation must follow this control operation to define at least the amount of data to be transferred between processor storage and the magnetic tape. Data transfer operations are described in the section “Channel I/O Data Transfer Operations.”

When the data transfer operation has been accessed and the byte count value loaded into the byte count register, the 8809 adapter starts the read block operation with the selected 8809 tape unit. If the data transfer operation specified that the contents of the data CHP were to be modified, the CHIO read direct operation occurs before the data transfer from the 8809 tape unit is begun. The first 256-byte data buffer is loaded from the 8809 tape unit before a CHIO burst transfer to processor storage occurs. The data transfer continues into the second data buffer from the tape unit while the 8809 adapter is sending the contents of the first data buffer to processor storage.

The Execute 8809 Read Block Operation implements the incorrect length (IL) flag to let the program suppress an incorrect length error, if detected, by making the IL flag in this control operation 1. If the IL flag is 0, an incorrect length condition results in BSTAT bit 5 (length error) being set at the end of the data transfer.

The 8809 read block operation continues until the byte count is 0 from the data transfer operation whose end-of-data (EOD) flag is 1.

### Programming Notes:

1. The data transfer operations performed by the 8809 adapter permit a program to read segments of data from the magnetic tape into noncontiguous areas in processor storage. When this type of data transfer operation is performed, *only the last data transfer operation (EOD flag is 1) can contain an odd byte count*. Failure to follow the above procedure results in unpredictable data transfers with no errors indicated by either the 8809 tape unit or the 8809 adapter.
2. Regardless of the state of the IL flag, when a data block to be read is shorter than the block of data on the magnetic tape, the byte count should contain an even value. If the byte count contains an odd value, and less than the total data block is to be read from the magnetic tape, the last byte of data is transferred incorrectly, and no error is indicated by the 8809 tape unit or the 8809 adapter.
3. This control operation cannot be executed immediately following the control operation, Execute 8809 Write Block Operation. If a read block operation is sent to a tape unit after a write block operation, the results are unpredictable.

### Execute 8809 Write Block Operation

Halfword 0				Halfword 1	
Byte 0		Byte 1		Byte 0	Byte 1
IX	P R I	X0111	XXXXXXXX	X'71'	X'44'

This control operation causes the 8809 adapter to prepare to start a write block operation with the selected 8809 tape unit. The 8809 adapter accesses the next four bytes from the FCB; a data transfer operation must follow this control operation to define at least the amount of data to be transferred between processor storage and the magnetic tape. Data transfer operations are described in the section "Channel I/O Data Transfer Operations."

When the data transfer operation has been accessed, and the byte count value has been loaded into the byte count register, the 8809 adapter begins a CHIO burst to load the first data buffer from processor storage. If the data transfer operation specified that the contents of the data CHP were to be modified, the 8809 adapter performs the CHIO direct read operation into the data CHP before the write block data is accessed. The value in the burst length register determines how many CHIO bursts are required to load the first 256-byte data buffer. After the first 256-byte data buffer has been loaded, the 8809 adapter starts the write block operation with the selected 8809 tape unit. The 8809 adapter loads the second data buffer while the contents of the first data buffer are being written on the magnetic tape. This overlapped transfer operation continues until the 8809 adapter exhausts the byte count for the last data transfer operation (EOD flag = 1).

When the write block operation is complete, the 8809 adapter accesses the next control operation from the FCB, unless an error was detected by the 8809 tape unit. If an error was detected, the 8809 adapter sets the appropriate BSTAT bits, ends the CHIO operation, and notifies the program of the error by presenting an interrupt request.



## ***Channel I/O Data Transfer Operations***

This section describes the three CHIO data transfer operations performed by the 8809 adapter: Load New Byte Count, Load New Address into Data CHP Bytes 2,3, and Load New Address into Data CHP Bytes 0,1. At least one data transfer operation is automatically accessed by the 8809 adapter when either the control operation, Execute 8809 Read Block Operation or Execute 8809 Write Block Operation, is accessed from the FCB. Each data transfer operation is four bytes long.

### **Programming Notes:**

1. CHIO data transfer operations can only follow a control operation that specifies a read block or a write block operation. If a data transfer operation is accessed in an FCB and is not preceded by either a write block or a read block operation, the 8809 adapter ends the CHIO operation and sets BSTAT bit 1 (invalid command/FCB error) and bit 15 (tape interrupt request) to notify the program.
2. When bytes 0–3 of the data CHP are to be modified, the Load New Address into Data CHP Bytes 0,1 operation must precede the Load New Address into Data CHP Bytes 2,3 operation. If this procedure is not followed, unpredictable values are loaded into the data CHP and no error is indicated by the 8809 adapter.
3. When several data transfer operations are used to read data into processor storage, only the last data transfer operation (EOD flag = 1) can contain an odd byte count. Failure to follow this procedure results in unpredictable data transfers, and no error is indicated by either the 8809 tape unit or the 8809 adapter.
4. When the total byte count read from an 8809 block is less than the actual number of bytes in that block, the byte count must total an even value. If an odd number of bytes is transferred, the last byte is transferred incorrectly and no error is indicated by either the 8809 tape unit or the 8809 adapter.

### **End-of-Data (EOD) Flag**

Each data transfer operation includes the end-of-data (EOD) flag in bit 2 of the operation format. The EOD flag indicates the data transfer operation in which the final byte count is specified. If the entire byte count for the read or write block operation is specified in one data transfer operation, the EOD flag must be 1 to prevent a length error condition. Several data transfer operations can be used to read or write data into or from noncontiguous areas in processor storage. In this case, only the last data transfer operation should include the EOD flag with a value of 1. When the 8809 adapter completes the transfer of the number of data bytes specified in the byte count field of that data transfer operation and the EOD flag is 1, the data transfer ends. If fewer bytes are read than are contained in the tape block, a length error is indicated by the 8809 adapter and the CHIO operation ends.

## Load New Byte Count

Halfword 0					Halfword 1				
Byte 0			Byte 1		Byte 0			Byte 1	
00	E O D	0	Byte Count		XXXXXXXX XXXXXXXX				

This data transfer operation identifies the byte count value for the current read block or write block operation. The data CHP must have been previously loaded with the logical address of the data area in processor storage from which or to which the data is to be transferred. The byte count field can specify a value up to 4,096 bytes; if a block is to be read or written that is longer than 4,096 bytes, additional Load New Byte Count data transfer operations must be included in the FCB following the read or write block control operation.

After the 8809 adapter has loaded the byte count value into the byte count register, the first CHIO burst transfer begins. The CHIO burst transfers continue until the number of bytes specified in the byte count field have been transferred to or from processor storage. If the EOD flag is 1, the 8809 adapter ends the data transfer and reads the next control operation from the FCB. If, however, the EOD is 0, when the byte count is exhausted, the 8809 adapter reads the next data transfer operation from the FCB. This process continues until a data transfer operation is read with the EOD flag set to 1. When the byte count from that data transfer operation is exhausted, the 8809 adapter then ends the data transfer and reads the next control operation from the FCB.

If an error is detected during the data transfer, the 8809 adapter ends the data transfer, ends the CHIO operation, and sets the appropriate BSTAT bits to notify the program with an interrupt request.

## Load New Address into Data CHP Bytes 2,3

Halfword 0					Halfword 1		
Byte 0			Byte 1		Byte 0		Byte 1
00	E O D	1	Byte Count		Data Area Address (Bytes 2,3)		

This data transfer operation causes the 8809 adapter to load the contents of the byte count field into the byte count register, and to begin a CHIO read direct operation to the data CHP. The new data area address is loaded into the channel pointer (CHP) that is identified in the data CHP number register. This operation can be used alone, to load only bytes 2 and 3 of the data CHP, or it can be issued following the data transfer operation, Load New Address into Data CHP Bytes 0,1, to load bytes 0–3 of the data CHP with a new data area address.

**Programming Note:** When this operation is used with the Load New Address into Data CHP Bytes 0,1 to load bytes 0–3 of the data CHP with a new data area address, these two data transfer operations must be contiguous in the FCB, and the data transfer operation, Load New Address into Data CHP Bytes 0,1, must precede this data transfer operation. Failure to follow this procedure results in unpredictable addresses being loaded into the data CHP.

The execution of this data transfer operation is similar to the execution of the data transfer operation, Load New Byte Count. If the EOD flag is 1, the byte

count field specifies the total number of bytes that are to be read or written. If the EOD flag is 0, the 8809 adapter accesses the next data transfer operation from the FCB when the byte count has been exhausted. This operation continues until the 8809 adapter either exhausts the byte count from a data transfer operation with the EOD flag set to 1, or until the 8809 adapter detects an error. If an error is detected, the 8809 adapter ends the data transfer, ends the CHIO operation, and sets the appropriate BSTAT bits to notify the program with an interrupt request that the error occurred.

#### Load New Address into Data CHP Bytes 0,1

Halfword 0				Halfword 1	
Byte 0			Byte 1	Byte 0	Byte 1
01	E O D	1	XXXX XXXXXXXX	Data Area Address (Bytes 0,1)	

This data transfer operation must be the first of a pair of data transfer operations used to load a new address value into bytes 0–3 of the data CHP. This data transfer operation sends bytes 0,1 of the new address value to the 8809 adapter. The 8809 adapter does not load these address bytes into the data CHP when they are received; instead, these address bytes are saved in the 8809 adapter until the second data transfer operation of the pair, Load New Address into Data CHP Bytes 2,3, is accessed from the FCB.

When the 8809 adapter has saved address bytes 0,1, it continues the CHIO burst to retrieve the second data transfer operation of the pair, Load New Address into Data CHP Bytes 2,3, from the FCB. The new data address is loaded into bytes 0–3 of the data CHP in a single CHIO read-direct burst, after both data transfer operations have been retrieved from the FCB.

This data transfer operation does not load a new value into the byte count register; the contents of bits 4–15 (halfword 0) are ignored by the 8809 adapter.

**Programming Note:** When this data transfer operation is used with the data transfer operation, Load New Address into Data CHP Bytes 2,3, to alter bytes 0–3 of the data CHP, these two data transfer operations must be contiguous in the FCB, and this data transfer operation must precede the data transfer operation, Load New Address into Data CHP Bytes 2,3. The EOD flag, if specified, must be set to 1 in both data transfer operations in this case. Failure to follow this procedure results in unpredictable addresses being loaded into the data CHP.

## 8809 Operations

8809 operations are individual operations that are performed by the 8809 tape unit. This section presents an overview of how 8809 operations can be started, followed by a description of each 8809 operation separated into one of six categories. These categories are identified in the first byte of the

halfword that contains an 8809 operation. The individual 8809 operation categories and the hex codes with which they are identified follow:

8809 Operation Category	Hex Code
8809 Poll Operation	12
8809 Selection Operation	A3
8809 Immediate Operation	31
8809 Immediate Disconnect Operation	41
8809 Non-Data Operation	51
8809 Data Operation	61/71

Some categories of 8809 operations can be initiated only by using programmed I/O (PIO) commands, some categories can be initiated only during channel I/O (CHIO) operations using CHIO control operations, and some categories of 8809 can be initiated using a PIO command or during a CHIO operation. The following list identifies each category of 8809 operation and how each can be initiated:

8809 Operation Category	PIO Command	CHIO Control Operation
8809 Poll Operation	Execute 8809 Poll Operation (X'66')	None
8809 Selection Operation	Execute 8809 Selection Operation (X'6C')	None
8809 Immediate Operation	Execute 8809 Immediate Operation (X'6E')	None
8809 Immediate Disconnect Operation	Execute 8809 Immediate Disconnect Operation (X'74')	Execute 8809 Immediate Disconnect Operation
8809 Non-Data Operation	Execute 8809 Non-Data Operation (X'76')	Execute 8809 Non-Data Operation
8809 Data Operation	None	Execute 8809 Read Block Operation
	None	Execute 8809 Write Block Operation

These PIO commands and CHIO control operations are described earlier in this chapter in "PIO Commands Used to Initiate 8809 Operations" and "Channel I/O Control Operations Used to Initiate 8809 Operations," respectively.

**Programming Note:** All 8809 immediate disconnect operations set tape unit status bit 5 (operation complete) when the disconnected operation is completed. The 8809 immediate operation, Check Reset, must be issued to the selected tape unit to reset tape unit status bit 5 before another 8809 operation is sent to that tape unit. Failure to reset tape unit status bit 5 before another 8809 operation is issued results in unpredictable operation of the tape unit.

Figure 16 shows individual 8809 operations organized by category of 8809 operation, in hexadecimal. Only the 8809 operations described in this section are valid. These 8809 operations are described in “8809 Operations Description.” Sending other 8809 operations to an 8809 tape unit results in unpredictable operation of the 8809 tape unit.

Operation	Category	8809 Operation
<b>8809 Poll Operation</b>	<b>12</b>	
Poll (for operation complete status)	12	00
<b>8809 Selection Operation</b>	<b>A3</b>	
Select 8809 n	A3	Address
<b>8809 Immediate Operations</b>	<b>31</b>	
Diagnostic Set Ready	31	0C
Read 8809 Sense Byte	31	80
Read 8809 Sense Byte 1-15/Status	31	81
Read 8809 Sense Byte 2-15/Status	31	82
Read 8809 Sense Byte 3-15/Status	31	83
Read 8809 Sense Byte 4-15/Status	31	84
Read 8809 Sense Byte 5-15/Status	31	85
Read 8809 Sense Byte 6-15/Status	31	86
Read 8809 Sense Byte 7-15/Status	31	87
Read 8809 Sense Byte 8-15/Status	31	88
Read 8809 Sense Byte 9-15/Status	31	89
Read 8809 Sense Byte 10-15/Status	31	8A
Read 8809 Sense Byte 11-15/Status	31	8B
Read 8809 Sense Byte 12-15/Status	31	8C
Read 8809 Sense Byte 13-15/Status	31	8D
Read 8809 Sense Byte 14-15/Status	31	8E
Read 8809 Sense Byte 15/Status	31	8F
Check Reset	31	E0
Set Long Gap	31	E8
Reset Long Gap	31	E9
<b>8809 Immediate Disconnect Operations</b>	<b>41</b>	
Forward Space File	41	22
Backspace File	41	2A
Data Security Erase	41	E1
Set Low Speed	41	E2
Set High Speed	41	E3
Rewind	41	E4
Rewind Unload	41	E5
<b>8809 Non-Data Operations</b>	<b>51</b>	
Forward Space Block	51	20
Backspace Block	51	28
Erase Gap	51	41
Write Tape Mark (WTM)	51	47
<b>8809 Data Operations</b>	<b>61/71</b>	
8809 Read Block	61	21
8809 Write Block	71	44
Loop Write-to-Read	71	01

**Figure 16. 8809 Operation Summary**

## 8809 Operations Description

### 8809 Poll Operation

**Poll (for operation complete status)** requests each tape unit with status bit 5 (operation complete) equal to 1 to return to the 8809 adapter the bit in the range 0–7 that corresponds to its tape unit address. Tape units that do not have status bit 5 (operation complete) active do not respond to this operation.

### 8809 Selection Operation

**Select 8809 n** is directed to a specific tape unit to select it for subsequent 8809 operations. A tape unit is selected by including its tape unit address in the byte that identifies the 8809 operation in other PIO commands that send 8809 operations to the 8809 adapter.

Tape Unit Address	Address Byte Value
000	X'00'
001	X'20'
010	X'40'
011	X'60'
100	X'80'
101	X'A0'
110	X'C0'
111	X'E0'

### 8809 Immediate Operations

**Diagnostic Set Ready** sets tape unit status bit 0 (ready) to 1.

**Read 8809 Status** causes the selected tape unit to return only the 8809 status byte to the 8809 adapter.

**Read 8809 Sense Byte 1–15/Status** are 15 operations; each causes the selected tape unit to return the selected sense byte, followed by the remaining sense bytes through sense byte 15, with the 8809 status byte returned last to the 8809 adapter.

**Check Reset** resets check conditions, the operation complete status bit, and puts the 8809 tape unit in a state to allow selection of the 8809 tape unit and normal execution of 8809 operations.

**Set Long Gap** sets the 8809 tape unit to generate an IBG of 30.5 millimeters (1.2 inches), independent of speed setting.

**Reset Long Gap** resets the 8809 tape unit to generate a standard IBG of 15.2 millimeters (0.6 inch).

### 8809 Immediate Disconnect Operations

**Forward Space File** searches for the next tape mark in the forward direction. If no tape mark is found, the search continues until the tape is unwound from the file reel, causing an error condition to interrupt the 8130 or 8140 processor.

**Backspace File** searches for the next tape mark in the backward direction. If no tape mark is detected, the search continues until the BOT mark is detected, causing an error condition to interrupt the 8130 or 8140 processor.

**Data Security Erase** erases the tape in the forward direction from the point where the operation is begun to a point approximately one meter beyond the EOT mark.

**Set High Speed** sets tape velocity to 2.54 meters per second (100 inches per second) streaming mode.

**Set Low Speed** sets tape velocity to 0.318 meter per second (12.5 inches per second) start and stop mode.

**Rewind** rewinds the tape to the beginning-of-tape mark.

**Rewind Unload** rewinds the tape to the beginning-of-tape mark, releases tension, and unloads the tape leader from the machine reel.

## 8809 Non-Data Operations

**Forward Space Block** spaces over the next block in the forward direction.

**Backspace Block** spaces over the next block in the backward direction.

**Erase Gap** erases a gap of 100 millimeters (3.9 inches) in the forward direction. This operation increases the gap preceding a block in order to position the head beyond a point on the tape containing a defect.

**Write Tape Mark** erases a gap of 90 millimeters (3.6 inches) and then writes a tape mark in the forward direction. If this operation is sent when the tape is at the beginning-of-tape mark, the 1600-BPI format identification burst is written ahead of the gap and the tape mark.

## 8809 Data Operations

**Read Block** reads the next block of data in the forward direction.

**Write Block** measures a gap and writes a block of data in the forward direction. If this operation is received when the tape is at the beginning-of-tape mark, the 1600-BPI format identification burst is written ahead of the data block. Before writing the data, the 8809 tape unit creates the proper length gap and writes the preamble. After the data, the 8809 tape unit writes the postamble and completes the readback check.

**Loop Write-to-Read** logically connects the write path and the read path to help isolate data path failures. No tape motion begins.

## 8809 Data Transfer Examples

This section presents two examples of data transfers between the 8809 tape unit and processor storage. In the first example, one block of data, 4K bytes in length, is read into two 2K-byte data areas, designated A and B. The two data areas are not contiguous; the data area address in the data CHP must be redefined during the CHIO operation to send the second 2K bytes to data area B.

In the second example, data from two areas in processor storage, also designated A and B, is written on the tape as a single block, 8K bytes long. Data area A is 6K bytes long and causes the byte count register to be loaded twice in order to write that portion of the tape data block. Data area B is 2K bytes long, and is located in a separate area in processor storage. The data area address in the data CHP must be redefined during the CHIO operation to access the data from data area B.

For both examples, each element of the FCB defined for that example is numbered to identify the elements as they are retrieved during the CHIO operation. The programmed sequences used to read and write data to or from the tape unit are shown in these examples. After the CHIO operations are started, the type of CHIO burst that is being requested by the 8809 adapter is identified by the type of CHCV that is sent to the processor's channel logic. The two types of CHCVs generated are the control CHCV and the data CHCV. The control CHCV uses the control CHP to access elements from the FCB and the data CHCV uses the data CHP to access data from processor storage, or to send data to processor storage. In these examples, an arrow indicates the direction of data transfer; data transfer direction is towards the arrow.

The read data transfer example is shown in Figure 17 and the write data transfer example in Figure 18. Both examples are divided roughly into three vertical columns labeled from left to right, Program/Processor Storage, 8809 Adapter, and Tape Unit. The leftmost column shows activities performed by the program, and data transfer sequences to or from processor storage. The center column lists activities performed by the 8809 adapter. The rightmost column shows data transfer sequences to or from the tape unit. Neither figure is intended to be a restrictive example of 8809 adapter programming; rather, each shows one way of programming these functions.

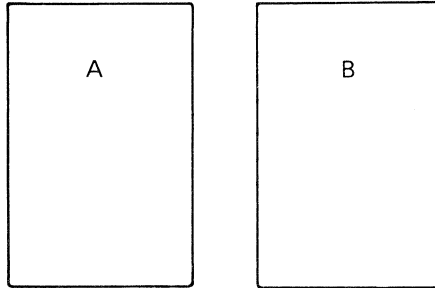
The 8809 adapter is assumed to have been enabled for CHIO operations and interrupt request presentation (BSTAT bit 14 - tape enabled - is active). The CHIO burst length is set to 256 bytes (burst length register equals binary 111).

Before the CHIO operation can be started, the program must define the FCB in processor storage and load the starting address of the FCB into the control CHP. The starting address of the first data area could be loaded into the data CHP during the CHIO operation, using a CHIO read direct burst. In this example, however, the program loads the starting data address into the data CHP before the CHIO operation begins.



For this example, the FCB is defined in processor storage as shown below. The two data areas, A and B, are also shown.

- 1 Execute 8809 Read Block Operation
- 2 Load New Byte Count (for data area A)
- 3 Load New Address into Data CHP Bytes 0,1 (data area B)
- 4 Load New Address into Data CHP Bytes 2,3 (data area B)
- 5 End Op



The program uses two PIO commands to load the control and data CHP number registers with the respective CHP numbers that are to be used during this CHIO operation.

Load Control CHP Number Register  
X'50' ————— PIO —————> control CHP number

Load Data CHP Number Register  
X'58' ————— PIO —————> data CHP number

The desired 8809 tape unit is selected using the PIO command, Execute 8809 Selection Operation (X'6C').

X'6C' ————— PIO —————> tape unit address

The 8809 adapter selects the specified tape unit, sets the BSTAT to X'0083' (normal end/end op, tape enabled, tape interrupt request) and presents an interrupt request to the processor to notify the program that the selection operation is complete.

←————— interrupt request

The program reads the BSTAT to check the cause of the interrupt request and then clears the interrupt request status.

Read BSTAT X'07' ←————— PIO —————> X'0083' is returned to the program.

Reset BSTAT 8-15 Under Mask X'04'  
mask X'0081' ————— PIO —————> BSTAT new value is X'0002' (tape enabled).

**Figure 17 (Part 1 of 4). Example of an IBM 8809 Read Block Operation**

The program checks the selected tape unit's status byte to determine if the tape unit is ready to perform 8809 operations.

Execute 8809 Immediate  
Operation (X'6E')

PIO

→ The PIO data sent with this command is X'3180', identifying a read 8809 status operation. The 8809 adapter reads the status byte from the selected tape unit and loads it into location 0 of the data buffer.

The program accesses the 8809 status byte using the following sequence:

Set Processor Buffer Address  
Register (X'34')

PIO

→ The PIO data is X'0000'; the processor buffer address register is set to 0 to access buffer location 0.

Read Buffer (X'69')

PIO

→ The 8809 adapter returns the 8809 status byte in byte 0 of the returned data; byte 1 should be ignored.

After the program checks the status byte to verify that the selected tape unit can perform 8809 operations, the CHIO operation is started by issuing the PIO command, Initiate CHIO.

X'7C'

PIO

→ The 8809 adapter generates the control CHCV using the contents of the control CHP number register, and begins a CHIO burst to retrieve the first control operation from the FCB.

control CHCV ←

CHIO burst

**1** Execute 8809  
Read Block  
Operation

→ The 8809 adapter begins another CHIO burst to retrieve the data transfer operation from the FCB.

control CHCV ←

CHIO burst

**Figure 17 (Part 2 of 4). Example of an IBM 8809 Read Block Operation**

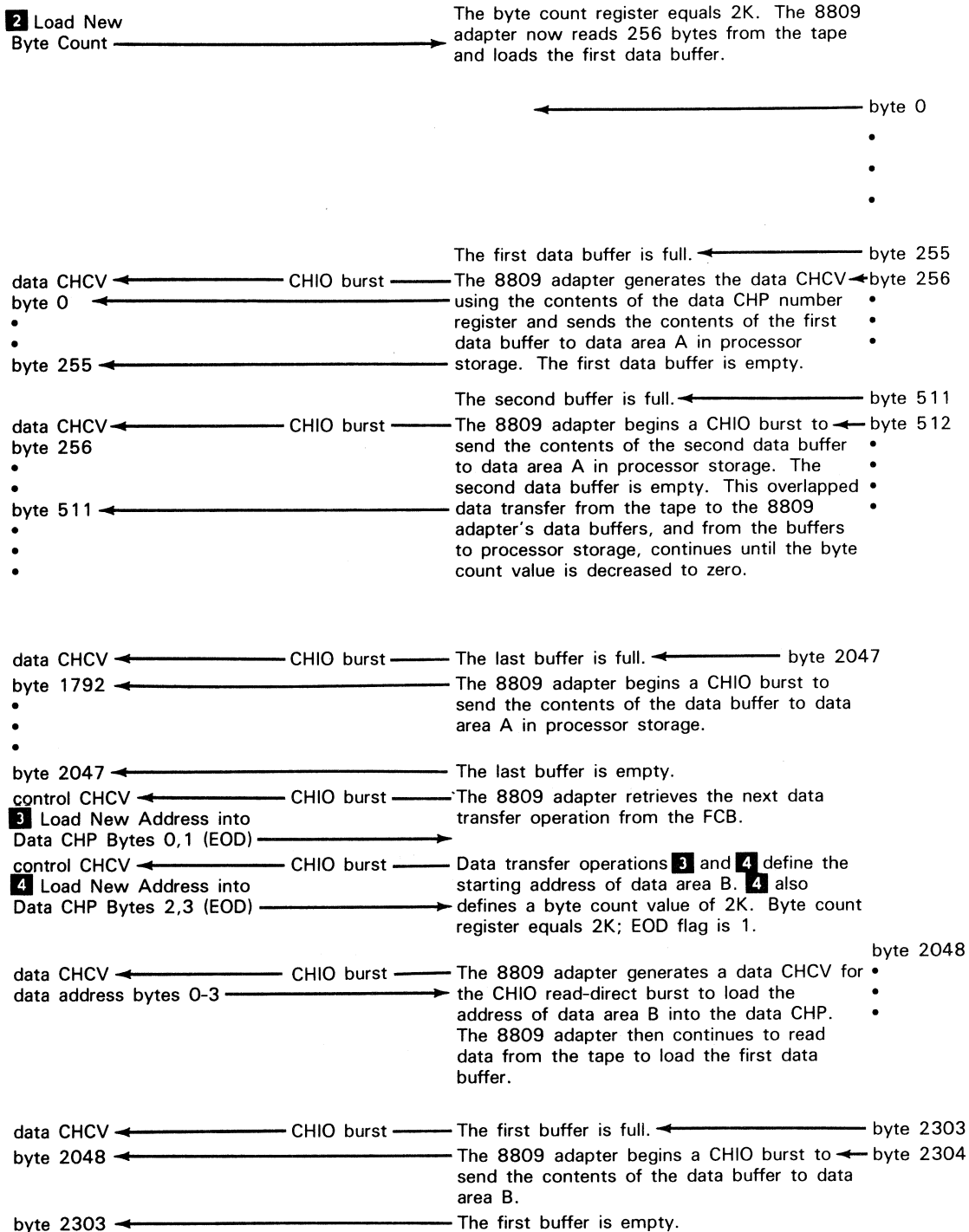
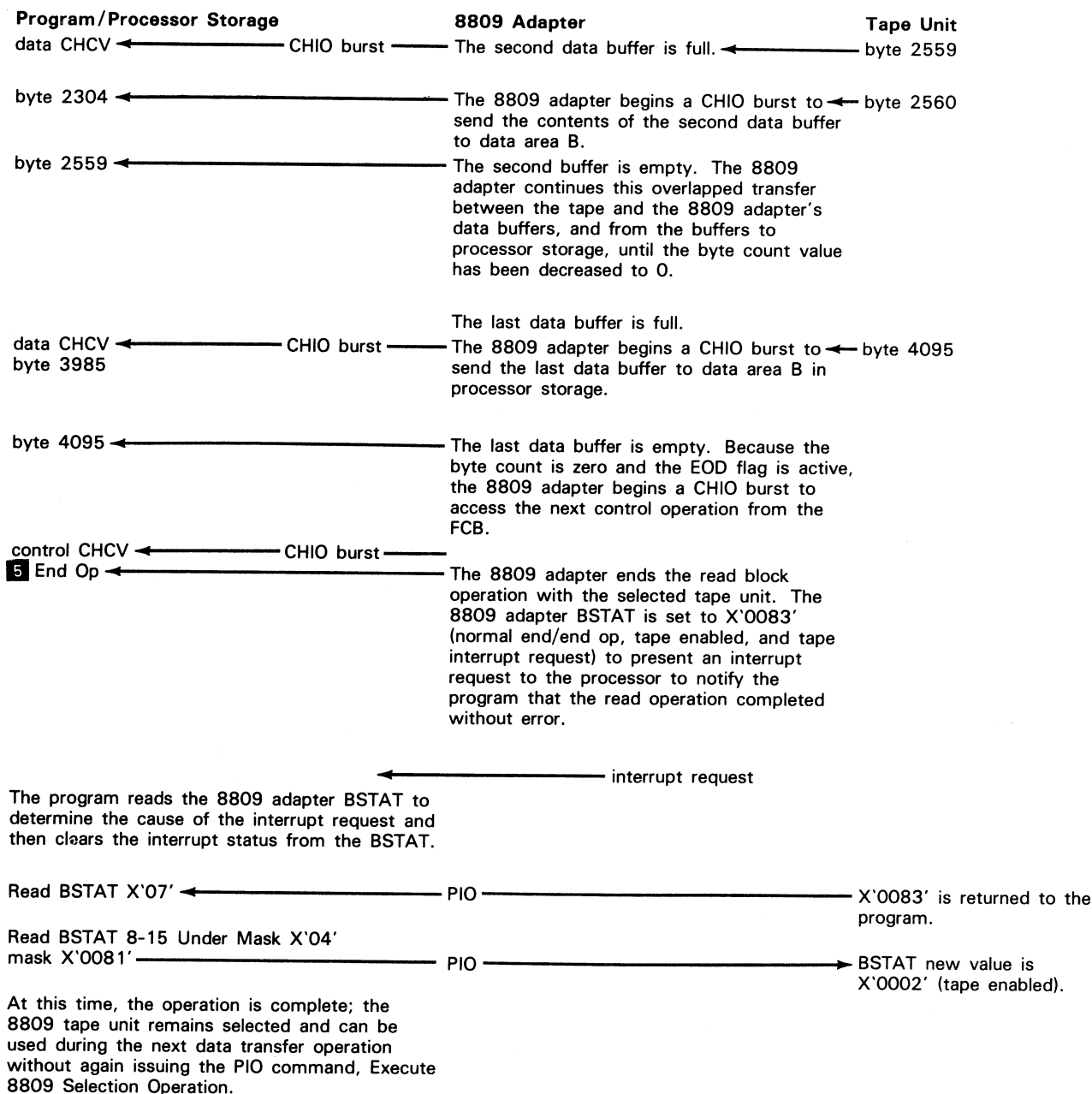


Figure 17 (Part 3 of 4). Example of an IBM 8809 Read Block Operation

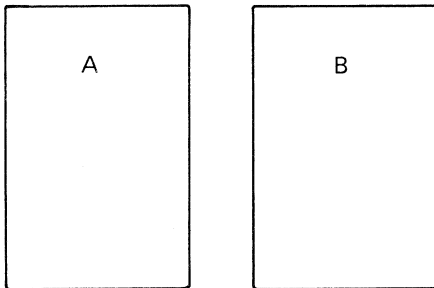


**Figure 17 (Part 4 of 4). Example of an IBM 8809 Read Block Operation**

The 8809 adapter is assumed to have been enabled for CHIO operations and interrupt request presentation (BSTAT bit 14 - tape enabled - is active). The CHIO burst length is set to 256 bytes (burst length register equals binary 111). Before the CHIO operation can be started, the program must define the FCB in processor storage and load the starting address of the FCB into the control CHP. The program could load the starting data area address into the data CHP before the CHIO operation is begun. In this example, however, the data CHP is loaded using a CHIO read direct burst into the data CHP.

For this example, the FCB is defined in processor storage as shown below. The two data areas, A and B, are also shown.

- 1 Execute 8809 Write Block Operation
- 2 Load New Address into Data CHP Bytes 0,1 (data area A)
- 3 Load New Address into Data CHP Bytes 2,3 (data area A)
- 4 Load New Byte Count
- 5 Load New Address into Data CHP Bytes 0,1 (data area B)
- 6 Load New Address into Data CHP Bytes 2,3 (data area B)
- 7 End Op



The program uses two PIO commands to load the control and data CHP number registers with the respective CHP numbers that are to be used during this CHIO operation.

Load Control CHP Number Register  
X'50' ————— PIO —————> control CHP number

Load Data CHP Number Register  
X'58' ————— PIO —————> data CHP number

The desired 8809 tape unit is selected using the PIO command, Execute 8809 Selection Operation (X'6C').

X'6C' ————— PIO —————> tape unit address

The 8809 adapter selects the specified tape unit, sets the BSTAT to X'0083' (normal end/end op, tape enabled, and tape interrupt request) and presents an interrupt request to the processor to notify the program that the selection operation is complete.

←————— interrupt request

The program reads the BSTAT to check the cause of the interrupt request and then clears the interrupt request status.

Read BSTAT X'07' ←————— PIO —————> X'0083' is returned to the program.

Read BSTAT 8-15 Under Mask X'04'  
mask X'0081' ————— PIO —————> BSTAT new value is X'0002' (tape enabled).

**Figure 18 (Part 1 of 4). Example of an IBM 8809 Write Block Operation**

The program checks the selected tape unit's status byte to determine if the tape unit can perform 8809 operations.

Execute 8809 Immediate Operation (X'6E')

PIO

The PIO data sent with this command is X'3180', identifying a read 8809 status operation. The 8809 adapter reads the status byte from the selected tape unit and loads it into location 0 of the data buffer.

The program accesses the 8809 status byte using the following sequence:

Set Processor Buffer Address Register X'34'

PIO

The PIO data is X'0000'; the processor buffer address register is set to 0 to access buffer location 0.

Read Buffer X'69'

PIO

The 8809 adapter returns the tape unit status byte in byte 0 of the returned data; byte 1 should be ignored.

After the program checks the status byte to verify that the tape unit can perform 8809 operations, the CHIO operation is started by issuing PIO command, Initiate CHIO.

X'7C'

PIO

The 8809 adapter generates the control CHCV using the contents of the control CHP number register, and begins a CHIO burst transfer to access the first control operation from the FCB.

control CHCV

CHIO burst

**1** Execute 8809 Write

Block Operation

The 8809 adapter begins a CHIO burst to retrieve the data transfer operation from the FCB.

control CHCV

CHIO burst

**2** Load New Address into Data CHP Bytes 0,1

In this example, data transfer operations **2** and **3** define the starting address of data area A; **3** also defines a byte count value of 4K.

control CHCV

CHIO burst

**3** Load New Address

into Data CHP Bytes 2,3

The byte count register equals 4K. The 8809 adapter generates a data CHCV for the CHIO read-direct burst to load the data address into the data CHP. Before the tape is started for the write block operation, the 8809 adapter loads the first 256-byte data buffer from data area A in processor storage.

data CHCV

CHIO burst

data address bytes 0-3

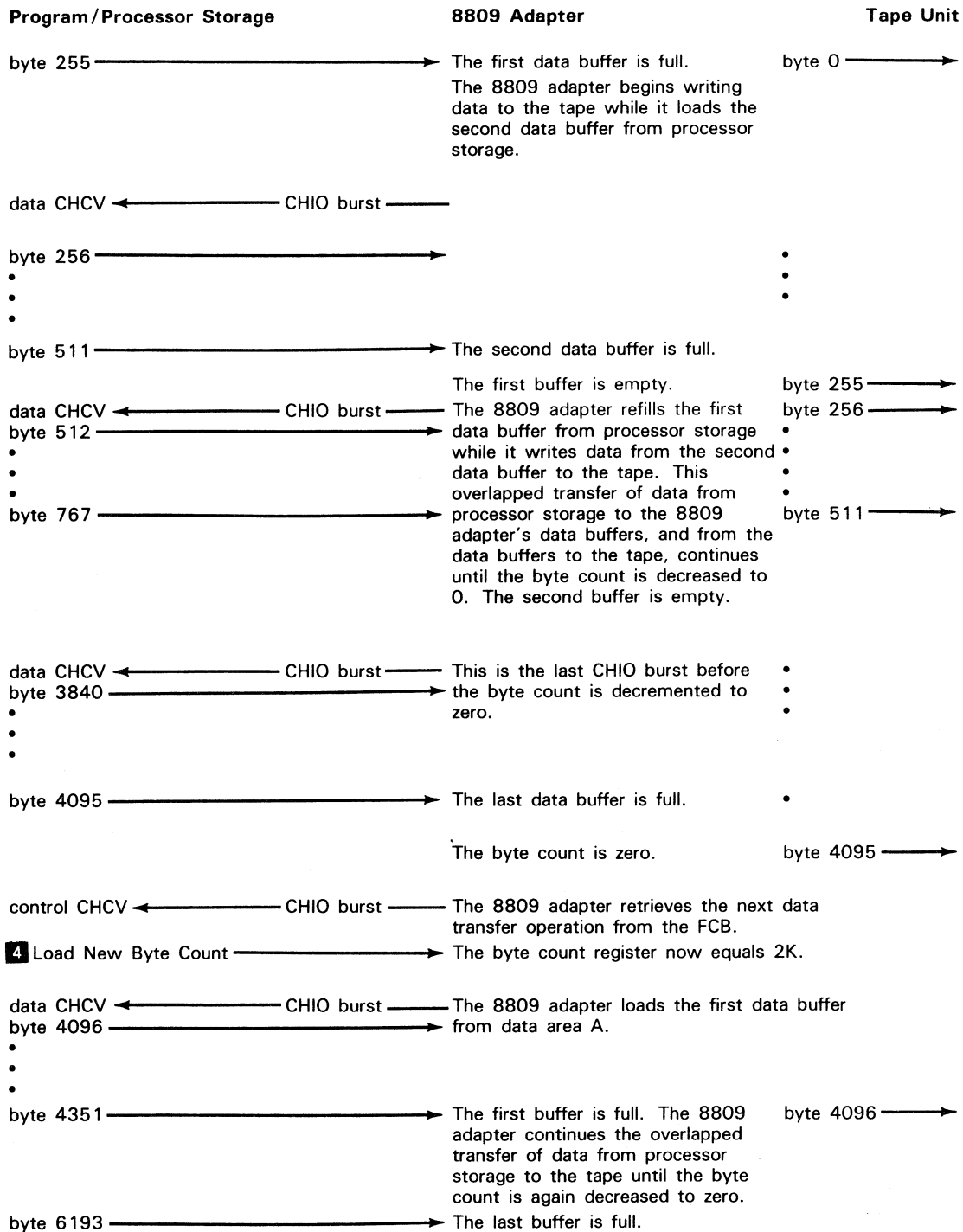
data CHCV

CHIO burst

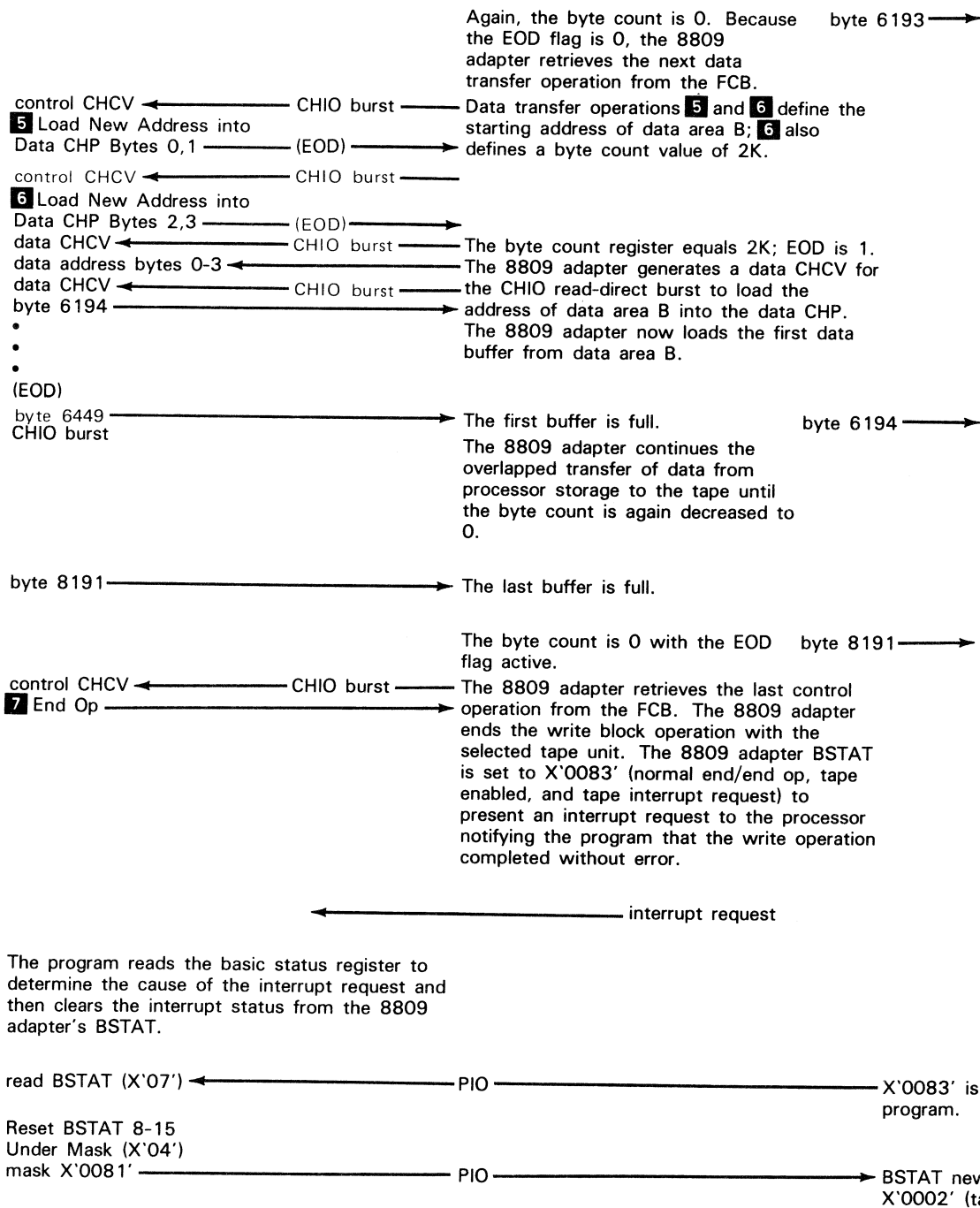
byte 0

•  
•  
•

Figure 18 (Part 2 of 4). Example of an IBM 8809 Write Block Operation



**Figure 18 (Part 3 of 4). Example of an IBM 8809 Write Block Operation**



At this time, the operation is complete; the 8809 tape unit remains selected and can be used during the next data transfer operation.

**Figure 18 (Part 4 of 4). Example of an IBM 8809 Write Block Operation**



## 8809 Tape Unit Sense and Status Data

The 8809 tape unit provides 15 bytes of sense data and one byte of status information. 8809 sense and status data is not automatically presented by the 8809 tape unit; it must be specifically requested by the program using the programmed I/O (PIO) command, Execute 8809 Immediate Operation (X'6E'). The halfword data operand transferred during execution of this PIO command must contain one of the read 8809 sense data or read 8809 status operations (X'3180' or X'3181-318F'). The 8809 adapter then reads the specified data from the selected 8809 tape unit into its data buffer. If only the 8809 status byte is read, the status byte from the selected 8809 tape unit is loaded into the data buffer location 0. If the 8809 adapter is directed to read 8809 sense byte 1 through 15, followed by the 8809 status byte, the 8809 sense data is loaded into data buffer locations 0 through 14, and the 8809 status byte is loaded into buffer location 15. At this time, the 8809 adapter presents an interrupt request to notify the program that the operation is complete. The program must then perform a sequence of PIO commands to retrieve the sense and status data from the data buffer of the 8809 adapter. This programmed sequence is described in the following programming note.

**Programming Note:** After the 8809 sense or status data or both are loaded into locations 0 through 15 of the 8809 adapter's data buffer, the following sequence of PIO commands retrieves this information:

1. Set the processor buffer address register to X'00' using the Set Processor Buffer Address Register command (X'34').
2. Retrieve the 8809 tape unit status byte, or the first halfword of 8809 tape unit sense data using the Read Buffer command (X'69'). If only the 8809 tape unit status byte was read and is now being accessed, byte 0 of the data returned to the program contains the 8809 tape unit status byte; ignore byte 1.
3. Issue the Read Buffer command (X'69') seven more times if all 15 bytes of 8809 sense data and the 8809 tape unit status byte are being retrieved. Each time the Read Buffer command is issued, the 8809 adapter returns the next sequential halfword of sense data to the program. The eighth time the Read Buffer command is issued, the 8809 adapter returns 8809 sense byte 15 in byte 0 and the 8809 tape unit status byte in byte 1 of the data returned to the program.

If the 8809 sense and status data were accessed from the 8809 tape unit using a PIO command that accessed fewer than fifteen 8809 sense bytes, the first sense byte accessed is retrieved from data buffer location 0. In this case, the total number of 8809 sense and status bytes that were accessed determine the number of times the Read Buffer command must be repeated to retrieve the 8809 sense and status data from the 8809 adapter's data buffer.

## Sense Data

Sense data supplies detailed information about the selected tape unit and the last operation performed. Fifteen read sense operations are provided to specify reading from 1 to 15 bytes of sense data from the 8809 tape unit. Information transferred by the read sense operation is more detailed than that supplied by the tape unit status byte. Figure 19 summarizes the status and sense information; the remainder of this section contains a description of the tape unit sense and status data. An asterisk (\*) indicates that the bit so noted serves as a flag but does not cause Basic Status Register bit 11 (end error) to be set.

Sense Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	Check End Sense*	Bus Out Parity Check	Tag Bus Parity Check	Formatter Failure	Control Lines Sequence Check	Command Register Parity Check	Drive Control Parity Check	Formatter Read Failure
2	Data Overrun*	Data Check*	Not Used	Beginning of Tape*	End of Tape*	Tape Mark Detected*	Not Capable*	Not Used
3	Write Bus Parity Check	Bus Out Register Parity Check	Gap Control Check	Sync Out Check	Drive Response Check	Not Capable Space File	Track in Error P*	Write Enable Error
4	Write Bus Parity Check	Read Bus Parity Check	Gap Control Check	Sync Out Check	Not Used	Not Used	Track in Error P*	Write Enable Error
5*	Track in Error 0	Track in Error 1	Track in Error 2	Track in Error 3	Track in Error 4	Track in Error 5	Track in Error 6	Track in Error 7
6	Nonwrite-type Operation	No Track Pointer	Multitrack Error	End Data Check	Start Read Check	Crease	Not Used	Skew Error
	Write- type Operation	PEID Check				Read Back Failure	Envelope Check	Write Tape Mark Error
7	This byte contains all zeros.							
8	Transport State*					Sequence Error	Sense Bus Parity Check	Not Used
9	Start Velocity Check	End Velocity Check	PEID Velocity Check	Clock Parity Error	Servo State		Sense Bus Parity Check	Not Used
10	Load Check	Tension Check	Cover/Reel Latch Interrupt	Tension Status*	Not Ready Due to Reset	Long Gap Mode*	Sense Bus Parity Check	Not Used
11	Present Transport State*					Cover/Reel Latch Status	Sense Bus Parity Check	Not Used
12	Servo Logic Failure	Servo Analog Failure	Write Current Failure	Erase Current Failure	Present Servo State*		Sense Bus Parity Check	Not Used
13	Idler Tachometer Failure	Machine Tachometer Failure	File Tachometer Failure	Idler Tachometer Rotation Check	Not Used	Not Used	Sense Bus Parity Check	Not Used
14	BOT/EOT LED Failure	Tape Present LED Failure	Reel Size LED Failure	Drive Control Failure	Not Used	Not Used	Sense Bus Parity Check	Not Used
15	File Amplifier Saturation	Machine Amplifier Saturation	Write Status*	Power Amplifier Cable Unseated	Not Used	Not Used	Sense Bus Parity Check	Not Used
Tape Unit Status	Ready	Busy	Write Enable	Beginning of Tape	End of Tape	Operation Complete	Low Speed	Positioning

Figure 19. Sense Byte Information Summary, IBM 8809 Attached to an IBM 8100 Information System

### ***Sense Byte 1***

An asterisk (\*) means that the noted bit or bits serve as indicators, but do not set Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Check End Sense*	Set when any of sense byte 2 bits 0, 1, 5, and 6 are set.
1	Bus Out Parity Check	Set when even parity is detected on command or data transfer from the 8100 system.
2	Tag Bus Parity Check	Set when even parity is detected on a command transfer from the 8100 system.
3	Formatter Failure	Set when there is a logic hardware failure.
4	Control Line Sequence Check	Set when improper sequencing occurs on control lines from the 8100 system.
5	Command Register Parity Check	Set when there is a logic hardware failure.
6	Drive Control Parity Check	Set when there is a logic hardware failure.
7	Formatter Read Failure	Set when there is a logic hardware failure.

### ***Sense Byte 2***

This byte is valid only when sense byte 1 bit 0 is set. An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Data Overrun*	Set when a data transfer to or from the 8100 system did not occur within the time specified for the 8809.
1	Data Check*	Set when one or more of the conditions occur as defined in sense byte 6.
2	Not Used	This bit contains a zero.
3	Beginning of Tape*	Set when the beginning-of-tape mark is sensed. This condition also sets bit 3 in the status byte.
4	End of Tape*	Set when the end-of-tape mark is sensed. This condition also sets bit 4 in the status byte.
5	Tape Mark Detected*	Set when a tape mark is detected during a Read, Forward Space Block, or Backspace Block command.
6	Not Capable*	Set when: <ul style="list-style-type: none"><li>• A PEID burst is not detected while reading or spacing the tape forward from the beginning-of-tape mark.</li><li>• A PEID burst is not correctly recorded while writing from the beginning-of-tape mark.</li></ul>
7	Not Used	This bit contains a zero.

### ***Sense Byte 3***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

Bit	Designation	Interpretation
0	Write Bus Parity Check	Set when there is a logic hardware failure.
1	Bus Out Register Parity Check	Set when there is a logic hardware failure.
2	Gap Control Check	Set when there is a logic hardware failure.
3	Sync Out Check	Set when the control lines used for data transfer do not operate correctly.
4	Drive Response Check	Set when there is a logic hardware failure.
5	Not Capable Space File	Set when 1600-BPI identification burst is not detected while executing a Space File operation from the BOT mark. This condition also sets sense byte 2 bit 6 and sense byte 1 bit 0.
6	Track in Error P*	Set when the error correction pointer for track P is on at the end of the last operation for which a data check condition occurred.
7	Write Enable Error	Set when a write operation is attempted and the tape is mounted without a write-enable ring.

### ***Sense Byte 4***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

Bit	Designation	Interpretation
0	Write Bus Parity Check	Set when there is a logic hardware failure.
1	Read Bus Parity Check	Set when there is a logic hardware failure.
2	Gap Control Check	Set when there is a logic hardware failure.
3	Sync Out Check	Set when the control lines used for data transfer do not operate correctly.
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Track In Error P*	Set when the error correction pointer for track P is on at the end of the last operation on which data check condition occurred.
7	Write Enable Error	Set when a write operation is attempted and the tape is mounted without a write-enable ring.

### ***Sense Byte 5\****

This byte contains the track-in-error pointers for tracks 0 through 7. It indicates track(s) for which pointers were active at the end of the last operation in which a data check condition occurred. It is reset during the next read block or space file operation. An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

## ***Sense Byte 6\****

The definition of sense byte 6 depends on the operation in progress at the time the sense bytes are set. Bit 0 indicates this operation and the meaning that is given to the remaining bits. An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

### **Nonwrite-type Operations**

For all operations other than write block, erase gap, or write tape mark, sense byte 6 has the following meaning:

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Nonwrite-type Operation	This bit contains a 0 for a non-write operation.
1	No Track Pointer	Set when a parity error is detected with no accompanying track pointer.
2	Multitrack Error	Set when a multiple track error (more than one pointer) is detected. The data error could not be corrected.
3	End Data Check	Set when an interblock gap IBG is detected earlier or later than expected.
4	Start Read Check	Set when a partially recorded data block is detected.
5	Crease	Set when a temporary loss of data is detected in all tracks of a data block.
6	Not Used	This bit contains a zero.
7	Skew Error	Set when the skew buffer exceeds its capacity.

### **Write-type Operations**

During a write block, erase gap, or write tape mark operation, sense byte 6 has the following meaning:

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Write-type Operation	This bit contains a 1 for a write-type operation.
1	PEID Check (with Data Check)	Set when a PEID burst is not correctly recorded while writing from the beginning-of-tape mark.
2	Multitrack Error	Same as for nonwrite operations except it applies to readback check.
3	End Data Check	Same as for nonwrite operations except it applies to readback check.
4	Start Read Check	Same as for nonwrite operations except it applies to readback check.
5	Read Back Failure	Set when readback data does not occur when expected during a write block or write tape mark operation. Set when a temporary loss of data is detected in all tracks of a data block.
6	Envelope Check	Set when a data error is detected during readback check.
7	Write Tape Mark Error	Set when the tape mark is not written correctly during a write tape mark operation.

### ***Sense Byte 7***

This byte contains all zeros.

### ***Sense Byte 8***

Sense Byte 8 shows the encoded state of the 8809 when an 8809 Sequence Error (byte 8 bit 5) occurs. Bits 0 through 4 contain the transport state sequences and bit 5 indicates a sequence error. An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

Bit	Designation	Interpretation
0–4	Transport State*	Used for machine failure diagnosis.
5	Sequence Error	Set when there is a logic hardware failure.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 9***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

Bit	Designation	Interpretation
0	Start Velocity Check	Set when a velocity problem occurs before a write data transfer. This bit indicates that the 8809 did not move the tape. The previous operation can again be sent without repositioning the tape.
1	End Velocity Check	Set when a velocity problem occurs during a write data transfer. The tape must be repositioned before rewriting data.
2	PEID Velocity Check	Set when a velocity problem occurs during an attempt to write a 1600-BPI PE identification burst.
3	Clock Parity Error	Set when an internal parity error is detected in the clock generation module.
4, 5	Servo State*	Used for machine failure diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 10***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Load Check	Set when there is a logic hardware failure.
1	Tension Check	Set when there is a logic hardware failure.
2	Cover/Reel Latch Interrupt	Set when the cover is opened after tape is loaded and tape tension is established.
3	Tension Status*	Set when the tape is correctly loaded in the tape path.
4	Not Ready Due to Reset	Set when a command is received and the 8809 is not ready. It is also set when the Reset pushbutton is pressed and the tape is not at the beginning-of-tape mark.
5	Long Gap Mode*	Set when the 8809 is in long gap mode.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 11***

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0-4	Present Transport State*	Used for machine diagnosis.
5	Cover/Reel Latch Status*	Used for machine diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 12***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Servo Logic Failure	Set when there is a logic hardware failure.
1	Servo Analog Failure	Set when there is a logic hardware failure.
2	Write Current Failure	Set when there is a logic hardware failure.
3	Erase Current Failure	Set when there is a logic hardware failure.
4, 5	Present Servo State*	Used for machine diagnosis.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 13***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Idler Tachometer Failure	Set when there is a logic hardware failure.
1	Machine Tachometer Failure	Set when there is a logic hardware failure.
2	File Tachometer Failure	Set when there is a logic hardware failure.
3	Idler Tachometer Rotation Check	Set when there is a logic hardware failure.
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

### ***Sense Byte 14***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	BOT/EOT LED Failure	Set when there is a logic hardware failure.
1	Tape Present LED Failure	Set when there is a logic hardware failure.
2	Reel Size LED Failure	Set when there is a logic hardware failure.
3	Drive Control Failure	Set when there is a logic hardware failure.
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.



## ***Sense Byte 15***

An asterisk (\*) indicates that the bit so noted serves as a flag but does not set the Basic Status Register bit 11 (end error).

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	File Amplifier Saturation	Set when there is a logic hardware failure.
1	Machine Amplifier Saturation	Set when there is a logic hardware failure.
2	Write Status*	Set when the tape unit has executed a Write, Write Tape Mark, Erase Gap, or Data Security Erase operation.
3	Power Amplifier Cable Unseated	Set when there is a logic hardware failure.
4	Not Used	This bit contains a zero.
5	Not Used	This bit contains a zero.
6	Sense Bus Parity Check	Set when there is a logic hardware failure.
7	Not Used	This bit contains a zero.

## ***8809 Status Byte***

The 8809 status byte is retrieved by executing the 8809 operation, Read 8809 Status Byte, or with the 8809 sense data, using one of the read sense byte/status operations. The read 8809 status operation can be executed repeatedly; however, the read 8809 sense byte/status operations should be executed only one time.

<b>Bit</b>	<b>Designation</b>	<b>Interpretation</b>
0	Ready	Set when the tape unit has a tape loaded and tape tension is established. Ready is set when the tape is loaded and positioned at the beginning-of-tape mark. It is reset when tension is lost or when the cover is opened. Ready is also reset when the Reset pushbutton is pressed at the operator panel. The 8809 tape unit must be ready before transmitting any operations except check reset, read 8809 status, or any of the read 8809 sense byte operations.
1	Busy	Set when a disconnected operation is initialized and remains set until it is reset with the check reset operation or until the Operation Complete bit is set. Busy is set while the tape unit is executing the operation panel functions of load rewind or unload rewind. When the 8809 tape unit is busy and Basic Status Register bit 11 (end error) is not set, only 8809 immediate operations can be performed.
2	Write Enable	Set when the tape is not file protected (write-enable ring installed), thus allowing write operations. Write operations issued to the 8809 tape unit without a write-enable ring installed sets the Basic Status Register bit 11 (end error).

3	Beginning of Tape	Set when the tape is positioned at the beginning-of-tape mark and is ready to read the format identification burst. This bit is reset when forward movement occurs. A backspace block or backspace file operation issued to the 8809 tape unit when the beginning-of-tape bit is set sets the Basic Status Register bit 11 (end error). The 8809 tape unit sets the beginning-of-tape bit, terminates the backward operation, and sets the Basic Status Register bit 11 (end error) if the beginning-of-tape mark is detected during a backspace block or backspace file operation.
4	End of Tape	Set when the end-of-tape mark is sensed in the forward tape direction and is reset when the end-of-tape mark is sensed in the backward tape direction. All operations can be sent to the 8809 tape unit when this bit is set. A data security erase operation, issued when the end-of-tape bit is set, erases tape approximately 1 meter (40 inches) and then sets status bit 5 (operation complete).
5	Operation Complete	Set when an immediate disconnect operation (other than space file) is completed. This bit is also set when a tape mark has been sensed during a space file operation. When the operator panel functions of load rewind and unload rewind are completed, the operation complete bit is set. This bit causes the 8809 tape unit to respond to a Poll operation. This bit is reset by a check reset operation.
6	Low Speed	Set when the 8809 tape unit is at a speed of 0.318 meter per second (12.5 inches per second). This bit is reset when the 8809 tape unit is at a speed of 2.54 meters per second (100 inches per second).
7	Positioning	Set when the 8809 tape unit is positioning as described in Figure 2.

## 8809 Adapter Error Detection and Reporting

This section summarizes the error-detection capabilities of the 8809 adapter and describes how errors are reported to the processor and to the program.

The 8809 adapter checks the parity of all information received from or sent to the program. If a parity check is sensed on PIO write data, the 8809 adapter suppresses the response for the data to cause an I/O timeout. The 8809 adapter sets BSTAT bit 2 (parity check detected) and bit 15 (tape interrupt request) to notify the program that the error was sensed. The I/O timeout condition causes a system check interrupt request to be presented to the processor. If a parity check is sensed on a PIO command, the 8809 adapter suppresses the response for the command and sets no bits in the BSTAT. The lack of a response causes an I/O timeout and a system check interrupt request to be presented to the processor.

If a parity check is sensed on the PIO address byte, the 8809 adapter does not respond to the PIO operation; in this case, no adapters respond to the processor's channel logic, and no adapters set error status bits in their BSTATs. Again, the lack of a response to the processor's channel logic causes an I/O/ timeout condition and a system check interrupt request to be presented to the processor.

If a parity error is sensed on data that is sent to or from a tape unit, the 8809 adapter sets BSTAT bits 2 (parity check detected), 3 (8809 sequence check), and 15 (tape interrupt request). The data transfer to or from the tape unit ends, and an interrupt request is presented to the processor to notify the program that the error was detected, and that the CHIO operation ended prematurely.

Errors sensed during CHIO operations are identified with one or more of the following bits being set with BSTAT bit 13 (tape equipment check): bit 0 (control CHP update halted), bit 1 (invalid command/FCB error), and bit 4 (poll response/CHIO check). The CHIO operation ends when the error is sensed, or when the halt signal is received. BSTAT bit 15 (tape interrupt request) is also set to present an interrupt request to the processor and to notify the program that the error was detected.

Figure 20 summarizes the error conditions sensed by the 8809 adapter. Additional information about some errors can be gathered by reading the contents of the control line bus in register. For other errors, the tape unit sense and status data must be retrieved and analyzed by the program to determine the specific cause of the error.

In this figure, the hexadecimal value recorded in the BSTAT for each error appears presented in the leftmost column. The BSTAT bits that are set to record the error are shown in the next column. The next two columns identify whether the control line bus in register and the tape unit sense and status data provide additional information about the error. The next column specifies the errors that cause a system check interrupt request. The last column describes each error condition.

BSTAT Hex Value	BSTAT Bits 0 through 15	Read CLBI Register	Read Sense and Status	System Check Interrupt	Error Description
8807	1 0 0 0 1 0 0 0 0 0 0 0 0 1 1 1	No	No	Yes	Halt received during control CHP update.
0807	0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 1	No	No	Yes	Halt received during FCB access.
0007	0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1	No	No	Yes	Halt received during CHIO data access.
4007	0 1 0 0 0 0 0 0 0 0 0 0 0 1 1 1	No	No	Yes	Invalid PIO sequence/Invalid PIO command received.
4003	0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1	No	No	Yes	FCB format check.
2003	0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 1	No	No	No	PIO write parity check/8809 adapter parity check.
3003	0 0 1 1 0 0 0 0 0 0 0 0 0 0 1 1	No	No	No	Tape unit-to-adapter parity check.
1023	0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1	No	Yes	No	8809 operation timeout.
1003	0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 1	No	No	No	Selection error, restricted PIO command received with tape unit busy, incomplete signal sequence at end of 8809 operation.
0403	0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1	No	No	No	Length error on read.
0103	0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 1	Yes	Yes	No	Overflow/underrun.
00C3	0 0 0 0 0 0 0 0 1 1 0 0 0 0 1 1	Yes	Yes	No	BOT sensed after a backspace operation, or a read block operation encountered a tape mark instead of data.
0093	0 0 0 0 0 0 0 0 1 0 0 1 0 0 1 1	No	Yes	No	Tape unit error sensed after completion of an 8809 operation.
0053	0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 1	Yes	Yes	No	EOT sensed during a write operation.
0013	0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1	No	Yes	No	A tape unit error was detected.
<b>Note:</b> BSTAT bit 6 (8809 disconnect operation) may be 1 in addition to the BSTAT bits described above.					

**Figure 20. 8809 Basic Status Register (BSTAT) Error Summary**

## 8809 Error Recovery Procedures

This section identifies the errors recorded in the 8809 tape unit's sense data. These errors are summarized in Figure 21. When the error is detected, an interrupt request is presented from the 8809 adapter with BSTAT bit 11 (end error) equal to 1. The sequence in which a program determines the sense bit that is active is shown in Figure 21, in the "Testing Priority" column. Recovery actions are identified with a Roman numeral in the "Action" column of Figure 21, and are described in the accompanying text under the action number. Recovery for an error when executing a data security erase operation is described by Action XVI.

Testing Priority	Sense		Description	Recovery Action
	Byte	Bit		
1	1	2	Tag Bus Parity Check	V
	3	1	Bus Out Register Parity Check	V
	1	1	Bus Out Parity Check	V
2	1	3	Formatter Failure	V
	1	4	Control Lines Sequence Check	V
	1	5	Command Register Parity Check	V
	1	6	Drive Control Parity Check	V
	15	6	Sense Bus Parity Check	V
3	12	2	Write Current Failure (read status)	IV
	12	3	Erase Current Failure (read status)	IV
4	14	0	BOT/EOT LED Failure	VI
	14	1	Tape Present LED Failure	VI
	14	2	Reel Size LED Failure	VI
	15	3	Power Amplifier Cable Unseated	VI
5	10	2	Cover/Reel Latch Interrupt	V
	10	4	Not Ready Due to Reset	XV
6	10	1	Tension Check	V
	10	0	Load Check	V
	13	3	Idler Tachometer Rotation Check	V

**Figure 21 (Part 1 of 2). Sense Data Error Summary for an IBM 8809 Attached to an IBM 8100 Information System**

Testing Priority	Sense		Description	Recovery Action
	Byte	Bit		
7	1	7	Formatter Read Failure	V
	3	0	Write Bus Parity Check	V
	3	2	Gap Control Check	V
	3	3	Sync Out Check	V
	3	4	Drive Response Check	V
	4	1	Read Bus Parity Check	V
	8	5	Sequence Error	V
	9	3	Clock Parity Error	V
	12	0	Servo Logic Failure	V
	12	1	Servo Analog Failure	V
	12	2	Write Current Failure (write status)	V
	12	3	Erase Current Failure (write status)	V
	13	0	Idler Tachometer Failure	V
	13	1	Machine Tachometer Failure	V
	13	2	File Tachometer Failure	V
	14	3	Drive Control Failure	V
	15	0	File Amplifier Saturation	V
	15	1	Machine Amplifier Saturation	V
8	Status	3	Beginning of Tape	VIII
9	9	2	PEID Velocity Check	IX
10	9	0	Start Velocity Check	II
11	9	1	End Velocity Check	III
12	3	5	Not Capable Space File	XIII
	2	6	Not Capable (write operation)	XII
	2	6	Not Capable (read status)	XIII
13	2	0	Data Overrun	VII
14	2	1	Data Check (read status)	XI
	2	1	Data Check (write status)	X
15	3	7	Write Enable Error	XIV
16	N/A	N/A	No previous error condition	V

**Figure 21 (Part 2 of 2). Sense Data Error Summary for an IBM 8809 Attached to an IBM 8100 Information System**

## **8809 Error Recovery Actions**

### **Action I**

Retries from 8809 adapter errors can be attempted at the user's option.

### **Action II**

Retry the operation until it completes successfully, or until 15 retries are attempted. If 15 retry attempts fail, the error is unrecoverable.

**Note:** *8809 status and sense data is not provided for failures that occur during selection operations.*

### **Action III**

Retry the operation until it completes successfully, or until 15 retries are attempted. To retry:

1. Issue the Backspace Block operation.
2. Reissue the failing operation.

If 15 retry attempts fail, the error is unrecoverable.

### **Action IV**

This error is unrecoverable; do not attempt a recovery action.

**Caution:** The operator must take care while rewinding the tape reels to avoid erasing the entire reel in case the write head or the erase head is energized. One way is to remove the write-enable ring from the file reel before rewinding the tape. This will remove power from the write and erase heads and prevent any accidental erasure of data.

### **Action V**

This error is unrecoverable; the position of the tape is undetermined.

The operator must inspect the tape unit to see that the tape is correctly threaded and to ensure that there is no excess tape in the tape path.

### **Action VI**

This error is unrecoverable; do not attempt a recovery action.

**Note:** *To process the tape, rewind the tape, unload the reel, and move it to another tape unit.*

### **Action VII**

Retry the operation until it completes successfully, or until 15 retries are attempted. To retry:

1. Issue the Backspace Block operation.
2. Reissue the operation that failed.

If 15 retry attempts fail, the error is unrecoverable.

## Action VIII

Issue the Rewind operation to the selected tape unit before continuing.

**Note:** *Reaching the beginning of tape (BOT) mark following a Backspace Block or a Backspace File operation, if not expected, indicates a possible programming error.*

Failing to issue the Rewind operation before issuing other 8809 operations to the tape unit results in unpredictable operation of the 8809 tape unit.

## Action IX

Retry the operation until it completes successfully, or until 15 retries are attempted. To retry:

1. Issue the Rewind operation.
2. Reissue the operation that failed.

If 15 retry attempts fail, the error is unrecoverable.

## Action X

Retry the operation until it completes successfully, or until 15 retries are attempted. To retry:

1. Issue the Backspace Block operation.
2. Issue the Erase Gap operation.
3. Reissue the operation that failed.

If 15 retries fail, the error is unrecoverable.

## Action XI

Retry the operation until it completes successfully, or until the following retry criteria are met:

If the error occurs in low-speed mode, retry the operation up to five times.  
If five retries fail, set the tape unit to high-speed mode, and retry the operation 35 additional times.

If the error occurs in high-speed mode, retry the operation up to 40 times.

To retry:

1. Issue the Backspace Block operation.
2. Reissue the operation that failed.

If 40 retries fail during low- or high-speed operation, the error is unrecoverable.

**Note:** *Tape cleaner action occurs with each Backspace Block operation in high-speed mode. The normal repositioning action during reversal of tape direction causes the failing data block to pass over the tape cleaner.*

## Action XII

Retry the operation until it completes successfully, or until 15 retries are attempted. To retry:

1. Issue the Rewind operation to reposition the tape.
2. Reissue the operation that failed.

If 15 retry attempts fail, the error is unrecoverable.



**Action XIII**

Retries can be attempted at the user's option. To retry:

1. Issue the Rewind operation.
2. Reissue the operation that failed.

**Action XIV**

This error is not recoverable through programming. To continue, a file reel with a write-enable ring is required.

**Action XV**

The tape unit is not ready. The operator must inspect the tape unit to see that tape is correctly threaded and to ensure there is no excess tape in the tape path. To continue, the operator must rewind the tape.

**Action XVI**

This error is not recoverable through programming. Notify the operator that an error occurred during a Data Security Erase operation.



# Glossary

This glossary includes definitions developed by the American National Standards Institute (ANSI) and the International Organization for Standardization (ISO). These definitions are marked by an asterisk and identified in a footnote at the bottom of each page where they occur. This material is reproduced from the *American National Dictionary for Information Processing*, copyright 1977 by the Computer and Business Equipment Manufacturers Association, copies of which may be purchased from the American National Standards Institute, 1430 Broadway, New York, New York 10018.

Most entries in this glossary are defined as they apply to the 8809 Magnetic Tape Unit and the 8100 Information System.

**basic status register (BSTAT):** A 1- or 2-byte register that contains adapter status information.

**byte operand:** An eight-bit unit of data referenced as an operand of an instruction.

**CG:** See *channel grant*.

**CG-high:** Channel grant high; the first priority channel grant.

**CG-low:** Channel grant low; the third priority channel grant.

**CG-medium:** Channel grant medium; the second priority channel grant.

**channel:** The facility that controls the transmission of information between the processor or main storage and an I/O device.

**channel control vector (CHCV):** The formatted information that specifies the controlling parameters, such as the channel I/O command, used during a channel I/O operation.

**channel grant (CG):** A signal from the processor granting an adapter or feature permission to start a previously requested channel I/O operation. The signal can be one of three priorities, listed from lowest to highest: channel grant low (CG-lo), channel grant medium (CG-med), and channel grant high (CG-hi).

**channel I/O (CHIO) burst operation:** That portion of a channel I/O operation during which the channel and an I/O device are logically connected for transferring information.

**channel I/O command:** The field of a channel control vector that directs the processor's channel logic and an adapter or feature to perform a channel I/O burst operation.

**channel I/O (CHIO) operation:** The transfer of data between processor storage and an adapter or feature. The operation consists of one or more channel I/O burst operations. It is initiated by a program and is controlled by the processor's channel logic. Processor instruction execution is temporarily suspended while a CHIO burst operation is in progress.

**channel mask:** The one-bit processor mask used to suspend channel I/O operations.

**channel pointer (CHP):** The principal register containing the logical address of data in processor storage that is to be transferred during a channel I/O operation.

**channel pointer number:** The field of a channel control vector that designates which channel pointer is to be used during a channel I/O operation.

**channel request:** A signal from an adapter or feature to the processor requesting permission to start a channel I/O operation.

**channel request priority (CRP):** Logic in the system control facility that establishes the priority of each adapter's requests to initiate channel I/O operations.

**CHCV:** See *channel control vector*.

**CHIO:** See *channel I/O (CHIO) operation*.

**CHP:** See *channel pointer*.

**command overrun:** The time between the end of the command instruct interval and the stopped state.

**control block:** (ISO) A storage area used by a computer program to hold control information.

**CR-high:** Channel request high priority; the first level of priority.

**CR-low:** Channel request low priority; the third level of priority.

**CR-medium:** Channel request medium priority; the second level of priority.

**CRP:** See *channel request priority*.

**current priority level:** The number of the active or controlling priority level. Contrast with *last priority level*.

**data area:** A storage area used by a program to hold information.

**Distributed Processing Control Executive (DPCX):** A licensed program designed to control the IBM 8100 Information System. DPCX manages the 8100 system resources (devices, storage, and processing time) in such a way as to provide central control of a distributed processing system and application programming capability.

**Distributed Processing Programming Executive (DPPX):** A comprehensive collection of program products that make up an operating system for 8100 Information System hardware. DPPX includes the DPPX base and other program products that provide programming languages, application support, and System/370 network access.

**Distributed Processing Programming Executive Base (DPPX/Base):** A program product that schedules and supervises the execution of programs written for 8100 Information System processing. DPPX base provides I/O control, storage management, data management, execution scheduling, application development tools, and related services.

**DPCX:** See *Distributed Processing Control Executive*.

**DPPX:** See *Distributed Processing Programming Executive*.

**EIRV:** See *error interrupt request vector*.

**end of chain (EOC):** A signal sent by control logic during a channel I/O operation to indicate that the CHIO burst operation is complete.

**EOC:** See *end of chain*.

**error interrupt request vector (EIRV):** The formatted information used to indicate an interrupt request generated by the processor when a system-check condition is detected, and to identify the system-check condition.

**file reel:** A reel of magnetic tape that can be temporarily mounted on a tape unit.

**general register:** A 32-bit register, in the primary or secondary register set, generally used for storage-address modification and generation, fixed-point (binary) arithmetic, and logical (boolean) operations.

**hex:** hexadecimal.

**input/output (I/O):** (1) (ISO) Pertaining to a device whose parts can be performing an input process and an output process at the same time. (2) Pertaining to either input or output, or both.

**interface:** \*A shared boundary. An interface might be a hardware component to link two devices or it might be a portion of storage or registers accessed by two or more computer programs.

**interrupt request:** A request for processing on a particular priority level. It may be generated by the active program, the processor, or an I/O device.

**I/O:** See *input/output*.

**I/O interrupt request vector (IOIRV):** The formatted information used to indicate an interrupt request generated by an I/O device.

**I/O tag:** A signal that is activated when a channel I/O operation or programmed I/O operation is beginning.

**IOIRV:** See *I/O interrupt request vector*.

**ITA:** Interrupt translation array.

**KDO:** Control direct out.

**logical address:** The storage address that is either supplied to or by a program during the fetching and execution of an instruction, or is used as a channel pointer during a channel I/O operation. Contrast with *relocated address*.

**machine reel:** A reel that is permanently mounted on a tape unit.

**main storage:** (ISO) Program-addressable storage from which instructions and other data can be loaded directly into registers for subsequent execution or processing.

**PIO:** See *programmed I/O*.

**primary system control facility (PSCF):** System control facility circuitry associated with the processor.

**principal register:** A 32-bit register used as a general register, as storage for half of a program status vector, or for storage of a channel pointer.

**principal register group:** All principal registers available to the processor.

**principal register set:** A set of eight principal registers located consecutively in the principal register group.

**priority level:** One of eight levels on which instruction execution occurs in the processor. Priority level 0 is the highest precedence; priority level 7 is the lowest. Processing on one priority level can be temporarily suspended when an interrupt request is received for a higher priority level than is currently active.

**program exception:** The condition recognized by the processor resulting from execution of a program, including the improper specification or use of instructions, operands, or control information.

**programmed I/O (PIO) address:** The information specified as an operand of an I/O instruction that identifies the adapter or feature to be selected for a programmed I/O (PIO) operation.

**programmed I/O (PIO) command:** The information specified as an operand of an I/O instruction that directs an adapter or feature to perform a programmed I/O operation.

**programmed I/O (PIO) operation:** The transfer of data between the processor and an adapter or feature as part of the execution of an I/O instruction. The I/O instruction designates the address of the adapter or feature, the PIO command to be performed, and the register into or from which the data is transferred.

**PSCF:** See *primary system control facility*.

**real address:** The address of a physical main storage location.

**register:** (ISO) A storage device having a specified storage capacity such as a bit, a byte, or a computer word, and usually intended for a special purpose.

**SCF:** See *system control facility*.

**secondary system control facility (SSCF):** System control facility circuitry associated with an I/O adapter or feature.

**SSCF:** See *secondary system control facility*.

**start and stop mode:** An operating mode of the 8809 Magnetic Tape Unit for application such as processing and journaling data base and data communication information.

**streaming mode:** An operating mode of the 8809 Magnetic Tape Unit to move data to or from direct access storage devices at high speed.

**system control facility (SCF):** An 8100 system component consisting of one primary system control facility and one or more secondary system control facilities. **vector:** One or more related fields of information, in a specified format, associated with the control of the processor, its channel logic, or floating-point facility.

**8100 Information System:** A collection of processors and devices that can be connected together to form a system for general use. These systems can be used standalone, connected to other 8100 Information Systems, and connected to a System/370.

**8809 Magnetic Tape Unit:** A two-speed tape unit designed to move tape directly reel-to-reel, without a capstan or vacuum columns.

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\*American National Dictionary for Information Processing

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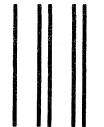
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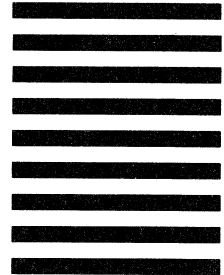
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