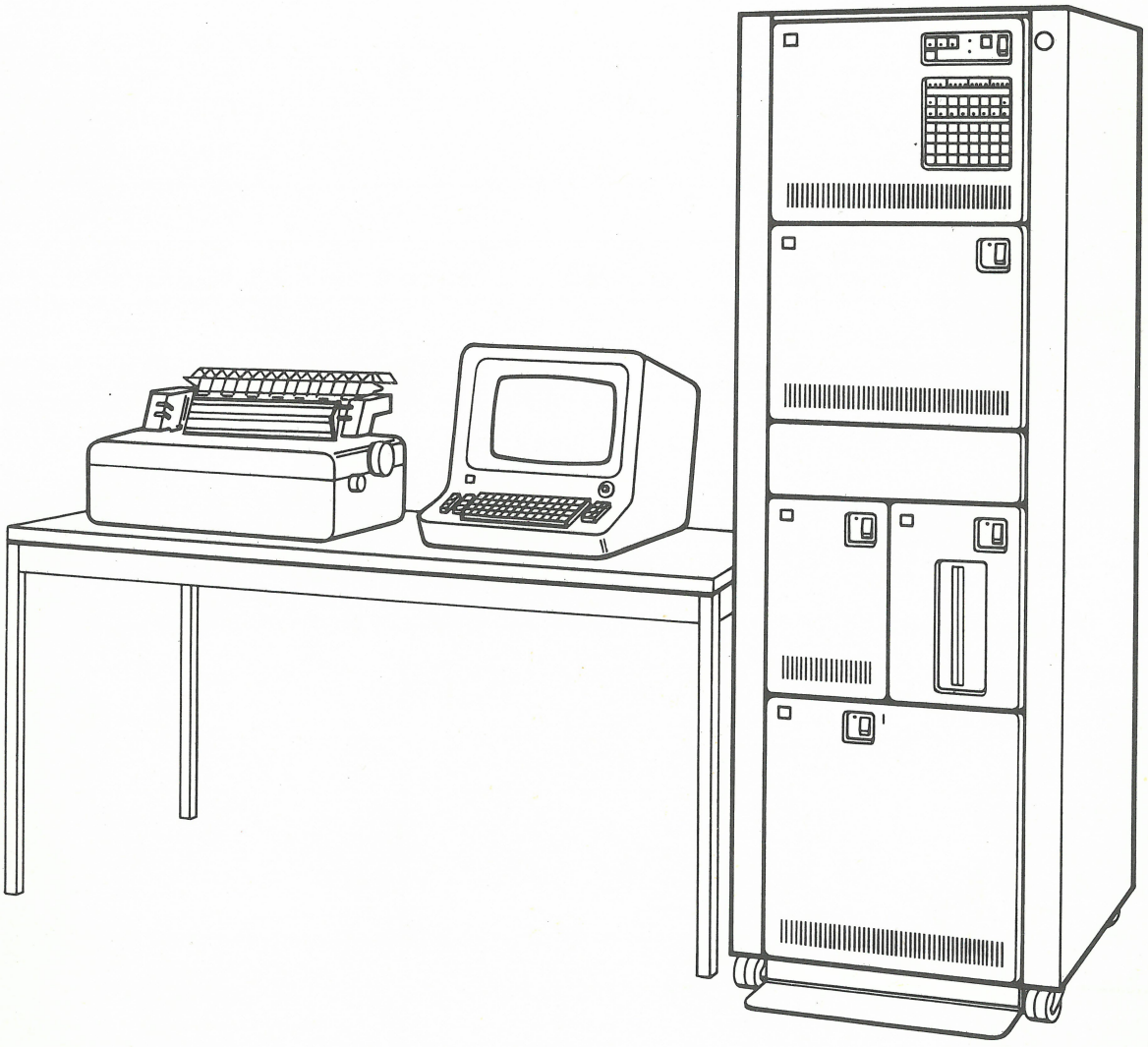
IBM

Series/1

GA34-0031-1

File No. S1-13

IBM Series/1
Attachment Features
Description



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Second Edition (March 1977)

This is a major revision of, and obsoletes, GA34-0031-0. Significant changes in this new publication include the combining of all Series/1 User Attachment Features into one manual. All information has been updated, and new material has been added.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters. Before using this publication in connection with the operation of IBM systems, have your IBM representative confirm editions that are applicable and current.

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Contents

Preface

This publication provides brief functional descriptions of the various IBM Series/1 Attachment Features and their associated machine-language programming support. These attachment features allow the IBM Series/1 user to communicate with the processor via his own input/output (I/O) devices. Presently, this publication contains:

- Chapter 1, "Introduction," gives a general description of the processor input/output (I/O) channel, an introduction to each of the attachment features, and a brief overview of the channel socket adapter feature, the channel repower feature, and the customer access panel.
- Chapter 2, "Timer Feature," describes the timer and includes data flow within the attachment, I/O commands, condition codes, and status information.
- Chapter 3, "Teletypewriter Adapter Feature," describes the use of this feature with an input or output device. The topics covered include bit transfer rates, I/O commands, condition codes, and status information.
- Chapter 4, "Integrated Digital Input/Output Non-Isolated Feature," provides a description of the commands, operations, condition codes, and status information associated with this feature.
- Chapter 5, "Customer Direct Program Control Adapter Feature," describes this feature and provides adapter-directed commands, device-directed commands, condition codes, and status information.

The information in this manual is written for experienced programmers who use assembler language and who also require a knowledge of machine language. Design engineers/technicians and programmers desiring electrical and technical descriptions of the attachment features should refer to *IBM Series/1 User's Attachment Manual,* GA34-0033.

Prerequisite Publications

IBM Series/1 Model 3 4953 Processor and Processor Features Description, GA34-0022
IBM Series/1 Model 5 4955 Processor and Processor Features Description, GA34-0021

Related Publications

IBM Series/1 System Summary, GA34-0035
IBM Series/1 User's Attachment Manual, GA34-0033
IBM Series/1 Installation Manual–Physical Planning, GA34-0029

Chapter 1. Introduction

The IBM Series/1 provides attachment features which allow the user to attach unique input/output (I/O) devices and equipment to an IBM 4953 or 4955 Processor. These attachment features communicate directly with the processor via the processor I/O channel.

The following attachment features have distinct I/O functions:

1. Timer feature
2. Teletypewriter adapter feature
3. Integrated digital I/O non-isolated feature

The customer direct program control (DPC) adapter feature has generalized I/O functions and connects any user device that is compatible with the signal lines provided.

Two other features, the channel repower and the channel socket adapter, are physical extensions of the processor I/O channel. Because they have no programming considerations, these two features are mentioned only briefly in the next section of this manual.

The customer access panel feature provides an assembly for mounting optional, quick-disconnect connectors for I/O equipment. Figure 1-1 shows the relationship of the user attachments to the processor I/O channel.

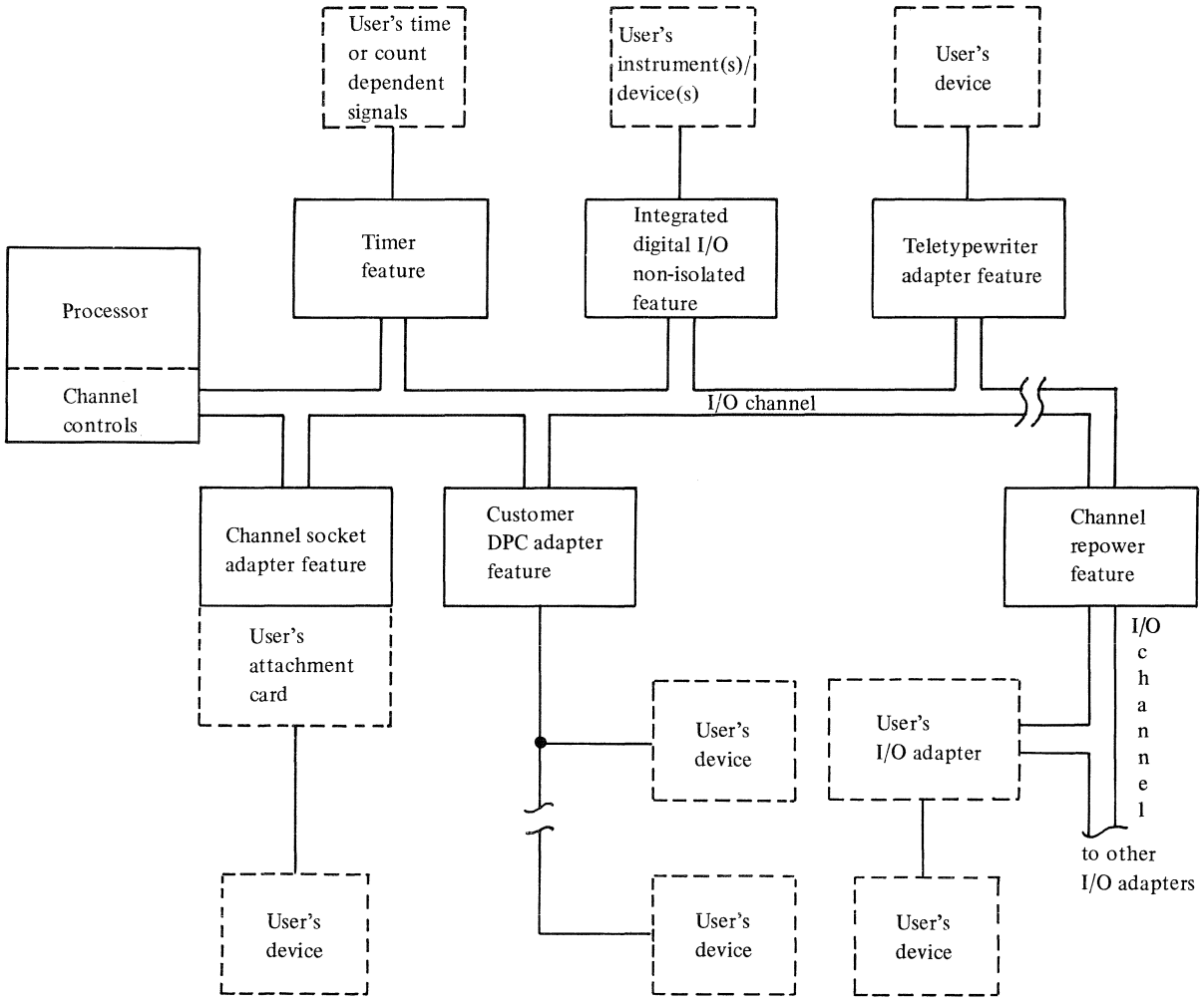


Figure 1-1. Relationship of user attachments to the processor I/O channel

Processor I/O Channel

The processor I/O channel provides a link between the I/O devices and the processor. The I/O devices are attached to the channel by an attachment card (feature). Up to 256 devices can be addressed by the channel.

The processor I/O channel supports the following basic operations:

- *Direct program control (DPC) operations.* During a DPC operation, an immediate data transfer is made between main storage and the device for each Operate I/O instruction. The data may consist of one byte or one word. The operation may or may not terminate with an interrupt.
- *Cycle steal operations.* The user attachment features are designed to perform only direct program control (DPC) operations. Refer to the applicable IBM Series/1 processor document listed in the "Preface" for an explanation of cycle-steal operations.
- *Interrupt servicing.* Four preemptive priority-interrupt levels are available to facilitate device service. The device-interrupt level is assignable by the program. In addition, the device-interrupt capability can be masked under program control.
- *Initial program load (IPL) operations.* During an IPL operation, a record consisting of initial instructions for the processor is read into storage from either a local I/O device or from a host system.

The channel provides comprehensive error checking including timeouts, sequence checking, and parity checking. Reporting of errors, exceptions, and status is accomplished by (1) recording condition codes in the processor during execution of operate-I/O instructions, and (2) recording condition codes and an interrupt information byte (IIB) in the processor during interrupt acceptance. Additional status words may be used by the device as necessary to describe its status.

The I/O channel is asynchronous (no timing restrictions are inherent in the architecture) and multidropped. Except in cases where timeout conditions are used for error detection, each sequential action is triggered by the response from a given I/O device rather than by a specified timing condition.

All of the I/O channel signal lines are transistor-transistor level (TTL) compatible. This allows the user to attach a wide variety of I/O devices having various speeds and delays.

The two features that connect directly to the channel and have no machine-code programming considerations are:

1. Channel socket adapter feature—this feature consists of an IBM printed-circuit card that plugs into the backpanel of the processor unit or the I/O expansion unit. An industry standard connector on the IBM printed-circuit card accepts the user's I/O adapter card. For further information, see *IBM Series/1 User's Attachment Features Manual,* GA34-0033.
2. Channel repower feature—this feature is a logic card that repowers and isolates the channel signal lines. This card must be installed as the last series element on the channel. For further information, see *IBM Series/1 User's Attachment Manual,* GA34-0033.

Customer Access Panel

The customer access panel feature provides an assembly for mounting optional, quick-disconnect type connectors for I/O equipment. The assembly can accommodate one timer connector, one teletypewriter connector, and up to four connectors for either the integrated digital input/output feature, or the customer direct program control feature.

The assembly mounts to the standard rack mounting screw holes at the rear of the enclosure frame. The other attachment features are discussed in the following sections.

Timer Feature

The timer feature is a printed-circuit card which has two separately addressable 16-bit timers each of which can generate periodic or aperiodic interrupts with or without control signals from the user's device. External timebase and gating signals can be user-supplied via connectors (jumpers) on the feature card.

In addition to operating as an interval timer or pulse counter, each timer can operate as a self-contained pulse-duration counter with end-interrupt.

Teletypewriter Adapter Feature

The teletypewriter adapter feature is a printed-circuit card which provides circuitry for attaching a serial I/O device to the processor I/O channel. This adapter is primarily designed for Teletype* Models ASR33, KSR33, and ASR35; however, any serial-by-bit I/O device that meets the interface requirements of the adapter can be attached. The adapter is capable of performing full duplex operations and initial program load (IPL).

Three attachment options are available: (1) TTL compatible, (2) Electronic Industries Association (EIA) RS232-C signal level equivalent, and (3) contact sense (isolated and non-isolated). These options are selectable by jumper wires or by using the card-connector pins.

The jumper-wire selectable device bit rates are:

50	150	1200
75	200	2400
100	300	4800
110	600	9600

*Trademark of Teletype Corporation

Integrated Digital Input/Output Non-Isolated Feature

The integrated digital I/O feature printed-circuit card contains:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI)
- Two 16-point groups of non-isolated digital output (DO)

Each group of DI/PI and DO have ready and sync lines for synchronizing their operations with the attached devices. The digital points for each group and their associated ready and sync lines are available at three card connectors.

Customer Direct Program Control Adapter

The customer direct program control adapter feature printed-circuit card provides a convenient means of attaching I/O devices and subsystems to the processor. The adapter is designed to perform direct program control (DPC) functions only; cycle-steal operations cannot be performed. The feature card can be configured to accommodate 4, 8, or 16 I/O device addresses. The adapter allows for interrupt vectoring of 16 interrupt sources.

User attachment is through three card connectors. There are 75 signal lines: 18 data bus out, 18 data bus in, 16 interrupt request in, 3 function bits, 4 modifier bits, 4 device address bits, and 12 control and response lines. The data flow is always 16 bits without parity option or 18 bits with parity option (2 parity bits).

Chapter 2. Timer Feature

This chapter provides a functional description of and machine-level programming information for the Timer User Attachment Feature card (referred to as the timer feature). Examples of timer feature applications along with the chronological steps required to effect each application are presented at the end of this chapter.

Each timer has a 16-bit auto-load register that can be set by program control. This register automatically reloads the timer when the timer has counted past zero. This reloading provides the capability of generating periodic interrupts on 65,536 possible base values of the timer without program intervention.

Functional Description

The timer feature has two separately addressable 16-bit timers on one attachment card (Figure 2-1). Each timer can be used as (1) an interval timer, (2) a pulse counter, or (3) a pulse duration counter. (See "Application Examples" at the end of this chapter for more details of these uses.)

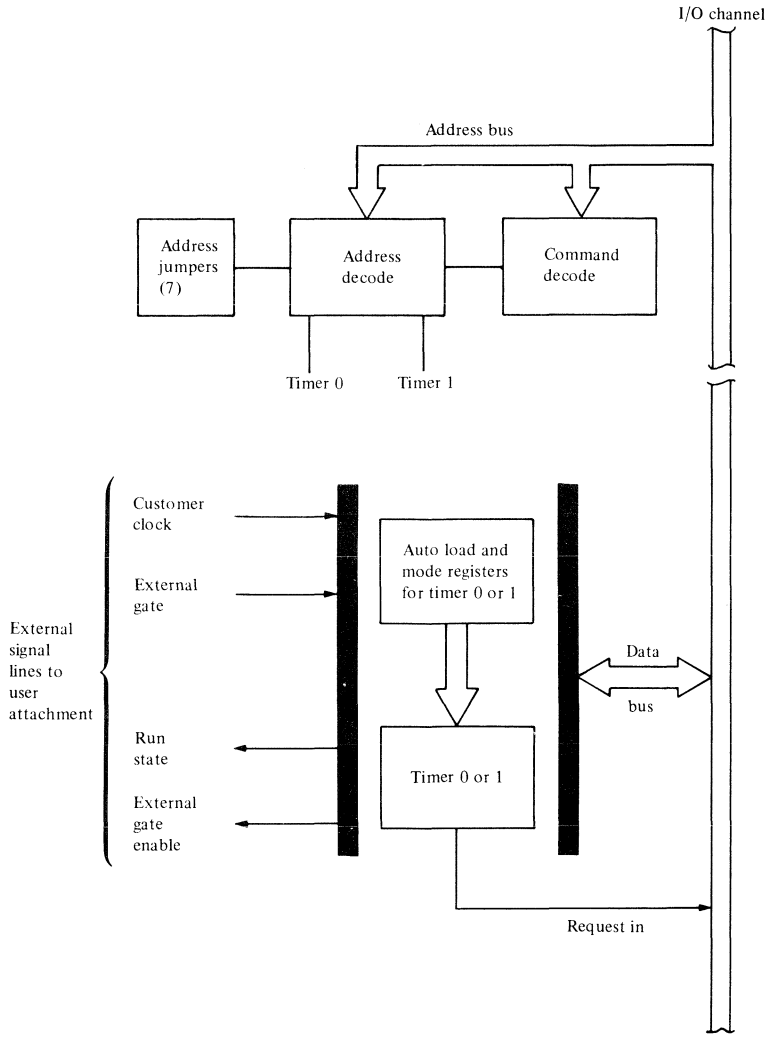


Figure 2-1. Timer feature block diagram

Each timer has a mode register that selects one of four standard internal timebases or a single external timebase. The four standard timebases are 1, 5, 25, and 50 microseconds. The external timebase, provided by the user, can be equal to or greater than 1 microsecond (less than 1000 kHz) with the filter inactive. Worst case is 20 microseconds with the filter active.

External Signal Lines

As shown in Figure 2-1, each timer has four external signal lines for user attachments. These signal lines permit control of the timer by a user-provided timebase and gate. The signal lines are described in the following sections.

Customer Clock

The customer clock line allows input for a user-supplied clock or a random pulse train.

External Gate

The external gate line provides input for the user-supplied gate signal. The signal and line are only effective when the external gate control is enabled.

Run

The run line carries the output signal that indicates the timer is in the run state. The primary purpose of the signal is to provide state synchronization of the external gate cycle. The run signal becomes active with a Start Timer command and remains active until either a Stop Timer command is accepted, or the external gate signal becomes inactive, or a halt/reset occurs. (These commands and resets are discussed in the "Programming Information" section of this chapter.)

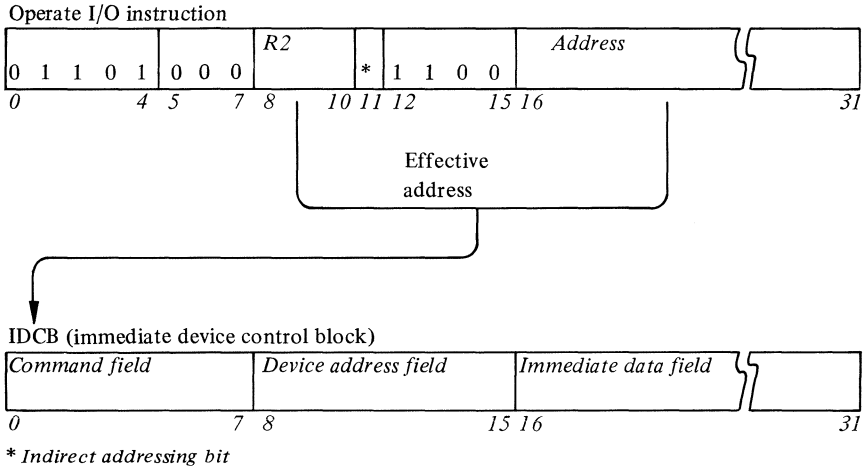
External Gate Enable

The external gate enable line carries the signal that indicates the external gate has been enabled through bit 15 of the Set Timer Mode command.

Programming Information

Operate I/O

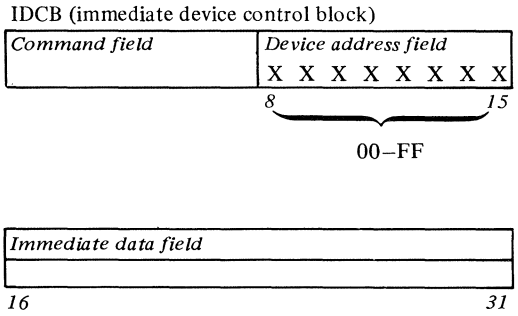
Communication between the processor and the timer attachment is initiated by the processor. All timer functions (control, read) must be initiated with an Operate I/O instruction.



The address field (bits 16–31) and the contents of the register specified in the R2 field (bits 8–10) of the Operate I/O instruction generate an effective address that points to a main-storage location containing an immediate device control block (IDCB). IDCBs are doubleword blocks of storage reserved by programs for storage of device-directed commands.

Addressing

Either timer on the attachment card can be addressed by the 8-bit address field in the IDCB (bits 8–15).



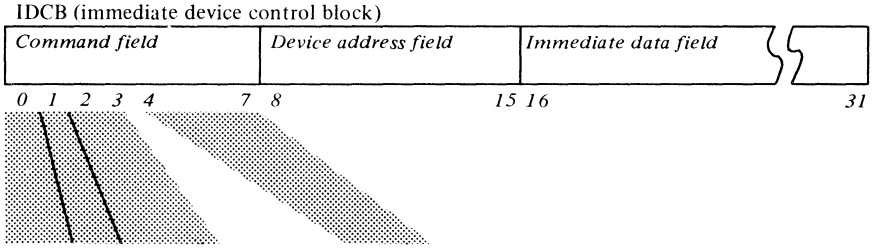
Bits 8–14 address the attachment card. Individual timer addresses are selected at installation time. These addresses are programmed on the cards by field-installable connectors (jumpers). These jumpers allow any 7-bit address (using bits 8–14) to be selected.

Bit 15 of the IDCB selects one of the two timers on the attachment card. If bit 15 is 0, timer 0 is selected. If bit 15 is 1, timer 1 is selected. The status of bit 15 is program dependent. There is no jumper on the attachment card for bit 15.

Commands

As shown below, IDCB command-field bits 0–7 define the various control and read functions issued to the timer by the processor. The specific commands are described in the following sections. Refer to the "Status Information" section of this chapter for an explanation of the condition codes reported for each command.

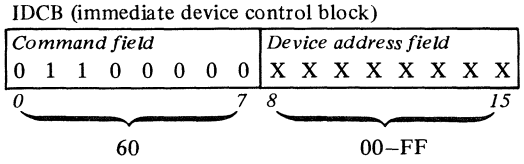
IDCB (immediate device control block)

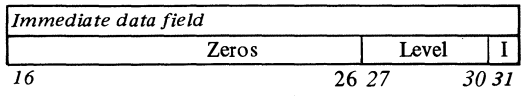


Chan	*R/W*	*Function*	*Modifier*	*Hex*	*Specific command*
0	1	10 Control	0000	60	Prepare'
0	1	10 Control	0100	64	Set timer period and initial value
0	1	10 Control	0101	65	Set timer mode
0	1	10 Control	0110	66	Start timer periodic
0	1	10 Control	0111	67	Start timer aperiodic
0	1	10 Control	1110	6E	Stop timer
0	1	10 Control	1111	6F	Device reset
0	0	10 Read status	0000	20	Read ID
0	0	10 Read status	0100	24	Read timer value
0	0	10 Read status	0101	25	Read timer mode

Prepare

IDCB (immediate device control block)





Bits 27–30	*Level*	*Bit 31*
0000	0	0 = interrupts not allowed
0001	1	
0010	2	1 = interrupts allowed
0011	3	

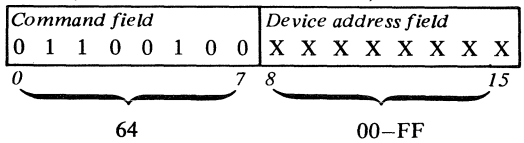
The Prepare command loads the interrupt level and I bit into the prepare register located on the attachment card. Both timers share one prepare register and are prepared simultaneously by the one Prepare command. The device-address field (bits 8–15) in the IDCB can indicate either timer.

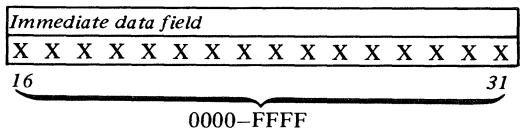
The I bit (bit 31) determines if the timer can report an I/O interrupt. If the I bit equals 0, I/O interrupts are not reported. If the I bit equals 1, I/O interrupts are reported. The timer reports I/O interrupts on the interrupt levels determined by bits 27–30. Level 0 is the highest priority level; level 3 is the lowest.

Condition code 1 (busy) is not reported for the Prepare command, and if condition code 5 (interface data check) is reported, the command was not successfully executed.

Set-Timer-Period and Initial-Value

IDCB (immediate device control block)



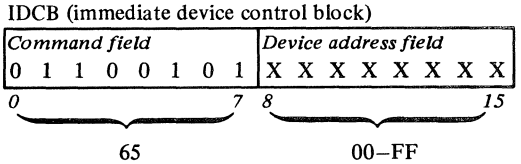


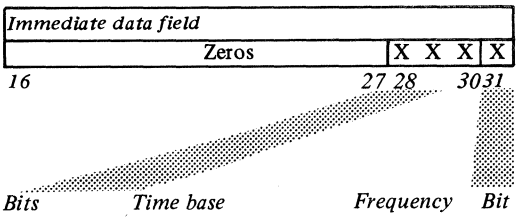
The Set-Timer-Period and Initial-Value command loads bits 16–31 of the IDCB into the auto-load register of the addressed timer. The data in the auto-load register is then loaded into the timer. This 16-bit value is user selected and can be any value from 0 to 65,536 (0000–FFFF hex). This value, in conjunction with the timebase selected by the Set Timer Mode command, establishes the time interval for device-end interrupts. (See "I/O Interrupt" in this chapter.)

No interrupt is reported by the timer to the Set-Timer-Period and Initial-Value command. If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

Set Timer Mode

IDCB (immediate device control block)





Bits 28–30	*Time base (microseconds)*	*Frequency (kHz)*	*Bit 31*
0 0 0	50	20	0 = external gate
0 1 0	25	40	not enabled
1 0 0	5	200	1 = external gate
1 1 0	1	1000	enabled
x x 1	user selected time base		

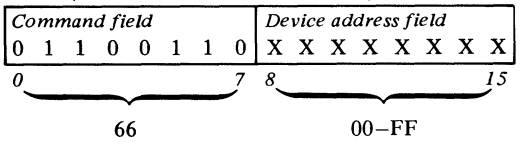
The Set Timer Mode command loads bits 16–31 of the IDCB into the mode register for the addressed timer. The desired timebase can be selected by bits 28–30; for example, if bits 28–30 are set to 010, the timer counts once every 25 microseconds at a frequency of 40,000 cycles per second. If the user-selected timebase is specified, (bits 28–30 set to XX1), any external timebase greater than 1 microsecond (less than 1000 kHz) for TTL input or 20 microseconds (worse case) for filtered TTL can be supplied to the timer. The timebase selected, in conjunction with the value used in the Set-Timer-Period and Initial-Value command, establishes the time interval for device-end interrupts. (See "I/O Interrupt" in this chapter.)

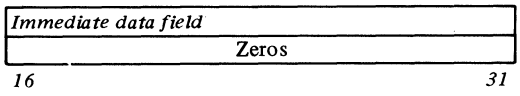
Bit 31 allows the user to provide an external gate to the timer. When this gate is enabled and activated by the user, the timer counts with the selected timebase. When the external gate is deactivated, the timer stops. No interrupt is reported by the timer for the Set Timer Mode command. If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

Start Timer, Periodic

As described below, the timer response to the Start Timer, Periodic command is dependent upon the state of the external gate control lines.

IDCB (immediate device control block)





External Gate Not Enabled

With the external gate not enabled, the addressed timer is set to run state and is started. When the timer decrements from zero to minus 1 (timer receives a pulse after it has reached zero), a device-end interrupt is reported and the value of the auto-load register is set into the timer. Any selected timebase can be used. If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

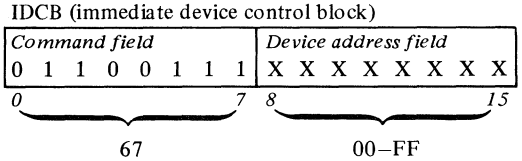
External Gate Enabled

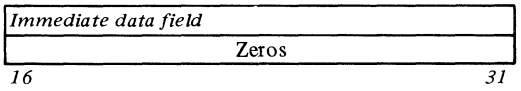
If the external gate is enabled, the addressed timer is set to run state, but is not started. The timer starts when the external gate becomes active after receipt of the Start Timer, Periodic command. When the timer decrements from zero to minus 1, a device-end interrupt is reported and the value of the auto-load register is set into the timer. When the external gate becomes inactive, the timer stops, the run state is reset, and an interrupt is reported. (See "Condition Codes Reported for an I/O Interrupt" in this chapter.) If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

Start Timer, Aperiodic

As described below, the timer response to the Start Timer, Aperiodic command is dependent upon the state of the external gate control lines.

IDCB (immediate device control block)





External Gate Not Enabled

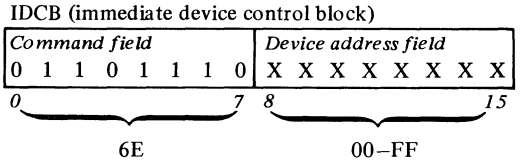
When the external gate is not enabled, the addressed timer is set to run state and is started. When the timer is decremented from zero to minus 1, a device-end interrupt is reported. However, unlike the Start Timer, Periodic command, the value of the auto-load register is not set into the timer. In this instance, the time period for the first device-end interrupt depends on the initial value set in the timer and the timebase selected. The time period for subsequent device-end interrupts depends on the timer maximum value and the timebase selected. Any selected timebase can be used. If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

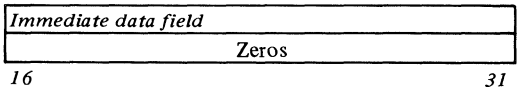
External Gate Enabled

If the external gate is enabled, the addressed timer is set to run state, but is not started. The timer starts when the external gate becomes active after receipt of the Start Timer, Aperiodic command. When the timer is decremented from zero to minus 1, a device-end interrupt is reported. However, unlike the Start Timer, Periodic command, the value of the auto-load register is not set into the timer. When the external gate becomes inactive, the timer stops, the run state is reset, and an interrupt is reported. (See "Condition Codes Reported for an I/O Interrupt" in this chapter.) If either condition code 1 (busy) or 5 (interface data check) is reported, the command was not successfully executed.

Stop Timer

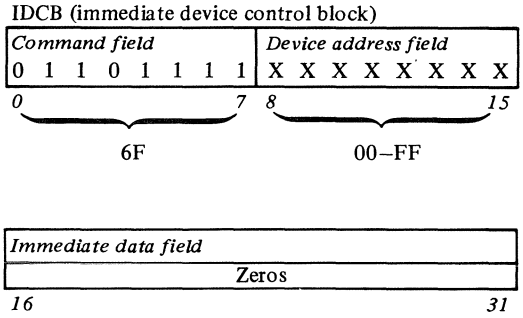
IDCB (immediate device control block)





The Stop Timer command causes the addressed timer to stop and the timer run state to reset. Also, any residual interrupts detected are reset. (A residual interrupt is caused by either (1) a pulsing of the timer, or (2) the dropping of the external gate, just after the timer has made a decision to accept and execute the Stop Timer command.) If the timer has an interrupt pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Device Reset

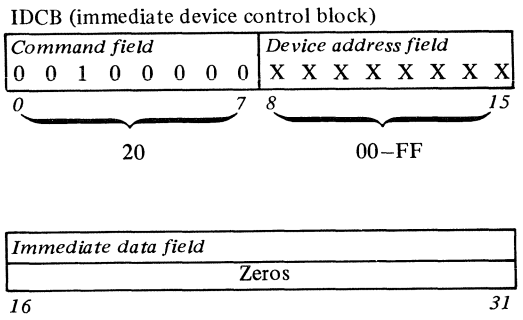


The Device Reset command stops the addressed timer and resets the timer run state. The mode register and any pending or residual interrupts for the addressed timer are reset. However, the timer and auto-load registers are not reset. Condition codes 1 (busy) and 5 (interface data check) are not reported to this command.

Halt I/O

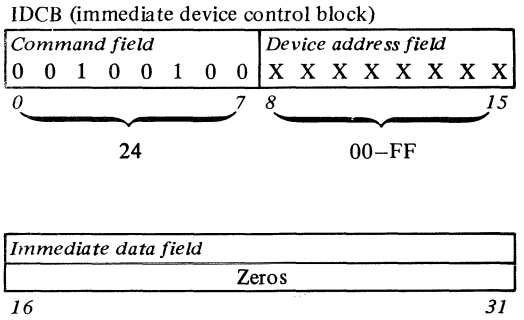
The timer feature responds to the channel-directed Halt I/O command by resetting the mode register, all pending interrupts, and the timer run status (see "Status After Resets" in this chapter).

Read ID



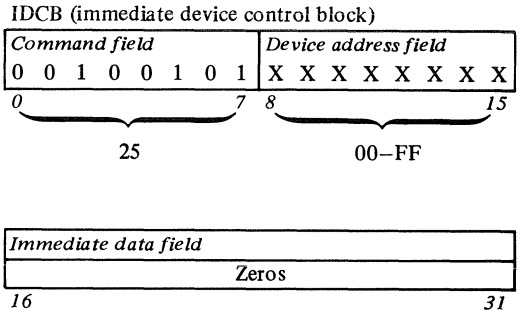
The Read ID (identification) command causes the ID word from the addressed timer to be loaded into bits 16–31 of the IDCB. The timer ID word is 0028 (hex). No interrupt is reported by the timer to this command. The device identification word contains a unique identification code and physical information about the device and can be used to determine the devices that are attached to the system. Condition code 1 (busy) is not reported. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read Timer Value



The Read Timer Value command causes the value of the addressed timer to be loaded into bits 16–31 of the IDCB. No interrupt is reported by the timer to this command. Condition code 1 (busy) is not reported. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read Timer Mode



The Read Timer Mode command causes the value of the mode register in the addressed timer to be loaded into bits 16–31 of the IDCB in the same format as specified by the Set Timer Mode command. No interrupt is reported by the timer to this command. Condition code 1 (busy) is not reported. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Status Information

Condition codes containing the status of the I/O operation are reported to the processor. These codes are explained in the following sections.

Condition Codes Reported for an Operate I/O Instruction

The following condition codes are reported during an Operate I/O instruction.

Condition code	*Meaning*
0	*Device not attached*—reported if the timer feature is addressed but is not installed on the system.
1	*Busy*—reported when the timer is unable to execute a command because it is in the busy state. A timer is in the busy state when the timer is in the run state or in an interrupt-pending state.
2	*Not reported*
3	*Command reject*—reported if the command issued is outside the defined command set for the timer feature.
4	*Not reported*
5	*Interface data check*—reported if a parity error occurs on the data bus during data transfer.
6	*Not reported*
7	*Satisfactory*—reported when a command is accepted.

I/O Interrupt

The timer feature initiates an I/O interrupt if the I bit (bit 31 of the IDCB) in the prepare register was set to 1 by the Prepare command.

When the timer is decremented from zero to minus 1, a device-end interrupt is reported. The timebase selected and the initial value set in the timer establish the time intervals for device-end interrupts. The relationship of these values is:

B(V+1) = T

where

B	=	timebase selected by the Set Timer Mode command (decimal).
V	=	value set into the timer by the Set-Timer-Period and Initial-Value command.
T	=	time interval of device-end interrupts (decimal).

The constant 1 is added to the value V because device-end interrupts are not reported until the timer has been pulsed once more after the count has reached zero.

Example: The user wants device-end interrupts reported every 100 microseconds and elects to use a timebase of 5 microseconds. Using the formula B(V+1) = T, the value to be set into the timer by a Set-Timer-Period and Initial-Value command is 13 (hex).

$$V = \frac{T}{B} - 1$$

$$V = \frac{100}{5} - 1$$

$$V = 20 - 1$$

V = 19 (decimal) : 13 (hex)

The time interval of the first device-end interrupt reported after the timer accepts a start command, or the external gate becomes active, may vary by as much as the value of the timebase selected. This variance is due to the asynchronous condition between the internal free-running oscillator or external-user clock, and the program setting of the timer run state or the activation of the external gate. This time variance occurs only when the timer is started.

The condition code reported during interrupt acceptance defines the interrupt.

Condition Codes Reported for an I/O Interrupt

The following condition codes are reported for an I/O interrupt.

Condition code	*Meaning*
0	*Not reported*
1	*Not reported*
2	*Exception*—reported when an overrun has occurred in the timer. Overrun means a device-end interrupt occurs while a previous device-end interrupt is pending in the timer.
3	*Device end*—reported when the timer is decremented from zero to minus 1.
4	*Attention*—reported when an external gate cycle ends prior to a device-end interrupt. Timer run state is reset.
5	*Not reported*
6	*Attention and exception*—reported if an external gate cycle ends and an overrun condition is present in the timer. Timer run state is reset.
7	*Attention and device end*—reported if an external gate cycle ends and device end are detected at the same time. Timer run state is reset.

Status After Resets

The following table lists the resets caused by the various resetting conditions.

Condition	*Reset*					
	Timer	*Auto-load reg.*	*Prepare reg.*	*Mode reg.*	*Pending interrupts*	*Timer run state*
Power-on reset	X (to all 1's)	X (to all 1's)	X	X	X	X
System reset			X	X	X	X
Halt I/O				X	X	X
Device reset				Y	Y	Y

X = reset in both timers

Y = reset in addressed timer only

Application Examples

The timer has several applications. The following are examples of how the timer feature could be used and a typical application sequence that can be followed.

Interval Timing

To utilize a clock of any arbitrary accuracy or frequency up to 1000 kHz, the customer clock input can be used, and the timer mode controls set to select a customer timebase.

The following steps apply when the timer application is an interval timer using an external timebase (customer clock input):

1. Prepare timer.
2. Set timer period and initial value.
3. Set timer mode (external time base—bit 14 of the IDCB data word set to one).
4. Start timer periodic.

The timer starts counting pulses and interrupts when the timer is decremented from zero to minus 1.

Pulse Counting

For pulse or event counting, the customer clock input can be used, and the timer mode controls set to select a customer timebase. The number of pulses recorded prior to an interrupt being posted is dependent on the value set into the timer and the chosen run mode. For example, if the timer (and thus the auto-load register) were set to all zeros and the chosen run mode was periodic, the timer would interrupt on each pulse counted. If under these same conditions, the timer was set to 100, it would interrupt on every 101st pulse. Pulses are recorded and interrupts generated at the leading edge of the pulse. Also, except for power-on reset, every pulse is counted only once even though the timers could be stopped and started many times during the active duration of a given pulse. Note that pulse inputs for the customer clock input can be pulses of very low frequency or even pulses with a random duty cycle.

The following steps apply when the timer application is a pulse counter using the external customer clock input.

1. Prepare timer 0 to interrupt in internal mode with the timer base at some prescribed interval; for example, 1 second.
2. Load a value into timer 1 that is larger than the number of expected external pulses.
3. Have timer 1 set up to receive customer clock (external timebase) in a periodic mode.
4. Have the interrupts from timer 0 initiate a Read Timer 1 Value command in the processor. Subtract the present value of timer 1 from the original value of timer 1.
5. Reload the starting value into timer 1 to repeat the cycle.

Thus, the counts per second of the customer clock can be read into the processor.

Pulse Duration Counting

The external gate input can be used for the pulse duration counting. A standard internal timebase can be used. A clock of arbitrary accuracy or frequency can also be used and connected to the customer clock input. The timer mode controls should be set to arm the external gate and to select the timebase desired. The measure of the pulse duration is a function of (1) the initial and end values of the timer, (2) a known timebase, (3) the type of interrupt returned, and (4) the run mode used. The user should ensure that the external gate input is inactive before the timer is set to run state, or an error in measuring will occur. The outputs from the timer card are available for this purpose. For example, assume clock inputs were occurring every 1 microsecond and an initial value of 1000 was loaded into the timer. The external gate input going active causes the timer to start. When the external gate goes inactive, the timer stops and an attention interrupt occurs. The timer is read and it is found to contain a value of 500. Therefore, the pulse width of the external gate pulse was 500 ± 1 microseconds.

The following steps apply when the timer application is a pulse duration counter.

1. Prepare timer.
2. Set timer period and initial value for a value greater than the width of the expected pulse.
3. Set timer mode for external gate control (bit 15 of the IDCB data word set to one).
4. Start timer.
5. Run state to customer interface becomes active.
6. Turning external gate on starts the timer, and it starts counting.
7. Upon the drop of external gate, the timer stops running and an attention interrupt is presented to the channel. Read the timer and subtract present value from original value. The result is the pulse duration of the external gate line in terms of the timebase selected.
8. Reload the starting value into the timer to repeat the cycle.

Chapter 3. Teletypewriter Adapter Feature

This chapter provides a functional description of and machine-language programming information for the Teletypewriter Adapter User Attachment Feature card (referred to as the teletypewriter adapter in the remainder of this chapter). Also included is information on operational characteristics including (1) data transmission and (2) transmit and receive operations. This material can be found at the end of this chapter.

Functional Description

The teletypewriter adapter is an input/output device attachment. This attachment was designed primarily to attach a teletypewriter I/O device such as a Teletype* Model ASR33, ASR35, or KSR33. However, the adapter may be used to attach other devices that satisfy the interface requirements. Some of the commercially available devices that can be attached to this feature include:

Printer - keyboards
Keyboard - display units
Keyboard - display - printer units
Printers
Tape cassettes
Tape units
Card readers
Badge readers
Plotters

Note. The interrupt mask time of the program support system that is used may preclude operation at the bit rate required by any of the above devices. Unbuffered devices whose input is from the keyboard are generally much less affected by the interrupt mask time of the program support system. See *IBM Series/1 User's Attachment Manual*, GA34-0033, Chapter 4, for details.

One of the following bit-transfer rates can be selected:

Bits per second	
50	300
75	600
100	1200
110	2400
150	4800
200	9600

Note. The interrupt mask time of the program support system may preclude operation at bit rates higher than 110 bps.

The bit-transfer rate that the teletypewriter adapter can accept is selectable at installation time by a field-installable connector (jumper) on the attachment logic card. The jumper can be changed if a different I/O device is attached that operates at another bit-transfer rate.

Attachment options between the teletypewriter adapter and the attached device are also selectable at installation time by field-installable jumpers on the attachment logic card. These jumpers can be changed to accommodate a different I/O device if desired. Four input options—isolated and non-isolated contact sense, TTL, and EIA—and three output options—solid state switch/TTL, current driver, and EIA—are available.

Also, three outputs—solid state switch/TTL for write control, solid state switch/TTL for read control, and EIA data terminal ready—are available to the user. Write control and read control are controlled by modifier bit 7 in the Write and Read commands. (See "Write" command and "Read" command in this chapter.) The EIA data terminal ready output is active when power is applied to the teletypewriter adapter.

The teletypewriter adapter supports full duplex operation. Data can be concurrently transmitted and received between the teletypewriter adapter and the attached device. Any of the 256 hex data codes can be transmitted or received.

The teletypewriter adapter does not *transmit* break characters. *Received* break characters will appear to the program support system as a series of all zero characters followed by one unpredictable character.

Note. If this feature is in a prepared condition and the associated TTY unit is powered-off or disconnected from the line, a continuous stream of interrupts is presented to the program at the teletypewriter adapter character rate. Processing of the interrupts can use too much processor time which causes the application program to fail. To avoid this condition, ensure that all devices attached to the Series/1 via Feature Code #7850 are connected with power on at all times when the system is operating.

*Trademark of Teletype Corporation

Programming Information

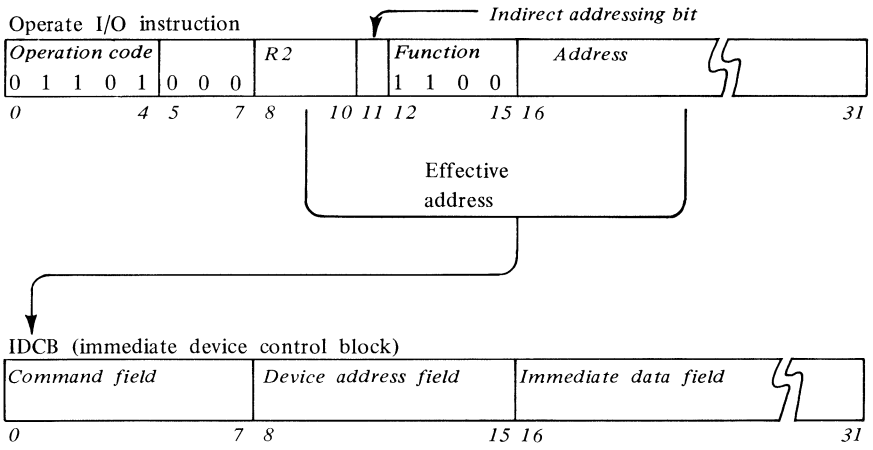
Initial Program Load (IPL)

The teletypewriter adapter can perform initial program load (IPL) as either the primary or alternate IPL source. During installation, this option is selected by a field-installable connector (jumper) on the attachment logic card. If Primary is selected on the attachment card and the IPL Source switch on the console is in the Primary position, the teletypewriter adapter is selected to perform the IPL when the Load key is pressed. If the connector is installed in the Alternate position, the IPL Source switch on the console must be in the Alternate position for the teletypewriter adapter to perform IPL.

The IPL record length is 256 bytes and starts loading into main storage at location zero. When IPL is completed, control is turned over to the instruction at main-storage location zero on interrupt level zero.

Operate I/O Instruction

Communication between the processor and the device attached to the teletypewriter adapter is initiated by the processor. All teletypewriter adapter functions (control, write, and read) must be initiated with Operate I/O instructions stored in the processor.



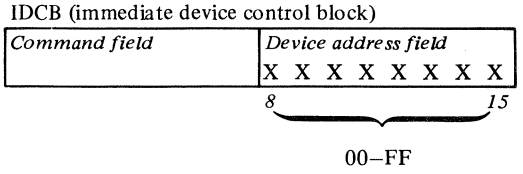
The address field (bits 16–31) and the contents of the register specified in the R2 field (bits 8–10) of the Operate I/O instruction generate an effective address that points to a main-storage location containing an immediate device control block (IDCB). IDCBs are doubleword blocks of storage reserved by programs for storage of device-directed commands.

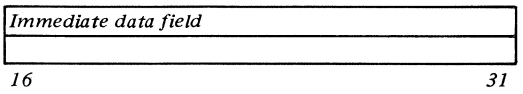
If bit 11 of the instruction (the indirect addressing bit) is a 1, the effective address address points to a main storage location containing the *address* of the IDCB.

Addressing

The attached device is addressed by the 8-bit address field in the IDCB (bits 8–15).

IDCB (immediate device control block)





Field-installable jumpers on the teletypewriter adapter attachment card provide the capability of selecting any one of 256 addresses (00–F hex) for the attached device.

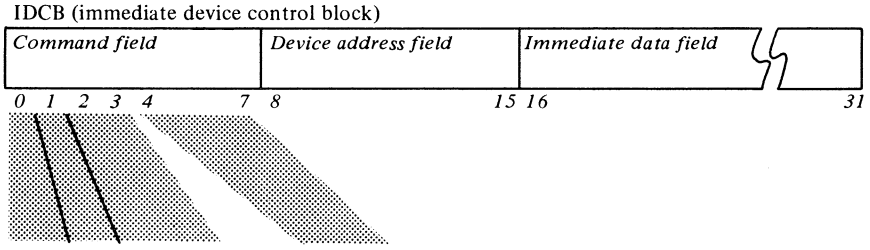
Commands

The teletypewriter adapter performs two types of receive operations. An understanding of these two types is necessary before discussing commands and condition codes.

- Normal receive operation.
  During a normal receive operation, a byte of data from the attached device is loaded into the receive-data register. An attention interrupt is reported at the completion of the operation. The data remains in the receive-data register until (1) read at least once by the program and (2) a subsequent normal receive operation is initiated.
- Overrun receive operation.
  An overrun receive operation is initiated if the attached device begins to transmit data to the teletypewriter adapter, and the adapter receive-data register, previously loaded by a normal receive operation, has not been read at least once by the program. The character in the receive-data register is not lost. However, the character that caused the overrun is lost. An exception interrupt is reported at the completion of an overrun receive operation.

As shown below, IDCB command-field bits 0–7 define the various control and read functions issued to the teletypewriter adapter by the processor. The specific commands are described in the following sections.

IDCB (immediate device control block)



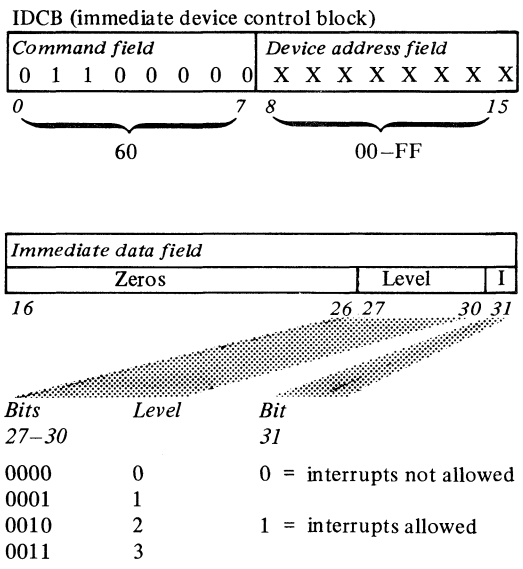
Chan	*R/W*	*Function*	*Modifier*	*Hex*	*Specific command*
0	1	10 Control	0000	60	Prepare
0	1	10 Control	1111	6F	Reset device
0	1	10 Control	1110	6E	Reset to diagnostic wrap
0	1	01 Write	000X	50,51	Write
0	0	01 Read	000X	10,11	Read
0	0	10 Read status	0000	20	Read ID

Write bit 7 = 0 Write control interface line is disabled
1 Write control interface line is enabled

Read bit 7 = 0 Read control interface line is disabled
1 Read control interface line is enabled

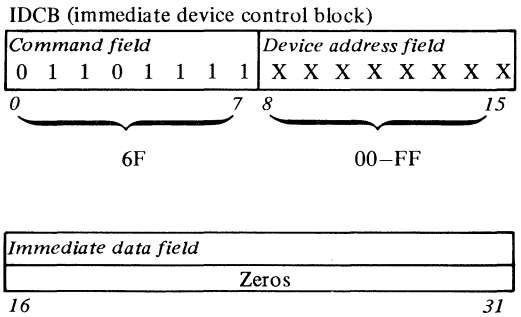
The condition codes referred to in the following I/O command descriptions are listed in the "Condition Codes Reported for an Operate I/O Instruction" section of this chapter.

Prepare



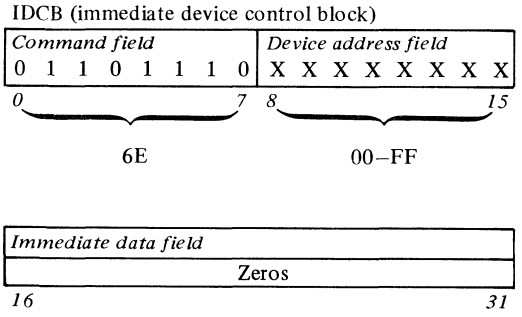
The Prepare command loads the interrupt level and I bit into the teletypewriter adapter prepare register. The I bit (bit 31) determines if the teletypewriter adapter can report an I/O interrupt. If the I bit equals 0, I/O interrupts are not reported. If the I bit equals 1, I/O interrupts are reported. The interrupt level (bits 27–30) is the level on which the teletypewriter adapter reports I/O interrupts. Level 0 is the highest-priority level; level 3 is the lowest. The teletypewriter adapter does not report condition code 1 (busy) to this command. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Device Reset



The Device Reset command resets all registers except the prepare-field register and the transmit-data register. The write- and read-control interface lines are disabled. Pending interrupts and condition codes are reset. The teletypewriter adapter does not report condition codes 1 (busy) and 5 (interface data check) to this command.

Reset-to-Diagnostic-Wrap



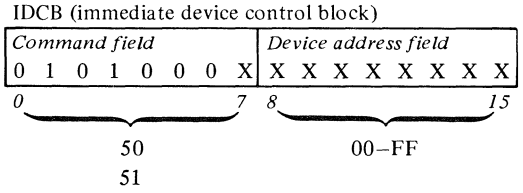
The Reset-to-Diagnostic-Wrap command places the teletypewriter adapter in the diagnostic-wrap state by (1) resetting pending interrupts, condition codes, and all registers in the teletypewriter adapter except the prepare register, and (2) disabling the read- and write-control interface lines.

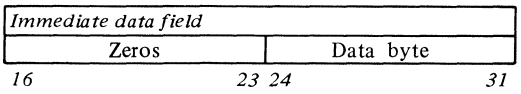
In the diagnostic-wrap state, commands can be issued to the teletypewriter adapter for testing purposes. A device may or may not be attached to the teletypewriter adapter during testing. If a Write command is issued, data is sent to the teletypewriter adapter transmit-data register and, if attached, to the device. At the completion of the transmit operation, a device-end interrupt is reported. The data is also sent to the teletypewriter adapter receive-data register, and at the completion of the receive operation an attention interrupt is reported. For checking purposes, the teletypewriter adapter can be forced into an overrun condition by not reading the receive-data register after the attention interrupt is accepted, and then issuing another Write command. The teletypewriter adapter does not report condition codes 1 (busy) and 5 (interface data check) to this command.

The diagnostic-wrap state is exited by issuing a Reset Device or Halt I/O command, a system reset, or a power-on reset.

Write

IDCB (immediate device control block)





Bit 7 = 0 Write control interface line is disabled

Bit 7 = 1 Write control interface line is enabled

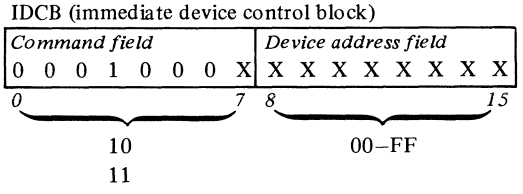
The Write command loads bits 24–31 of the IDCB into the teletypewriter adapter transmit-data register. The teletypewriter adapter then transfers the byte serially by bit to the attached device. If command-field bit 7=0, the write-control interface line is disabled (open). If command-field bit 7=1, the write-control interface line is enabled (closed). A device-end interrupt is reported at the completion of the data transfer. If the teletypewriter adapter is in a write-busy or interrupt-pending state, condition code 1 (busy) is reported and the command is not executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

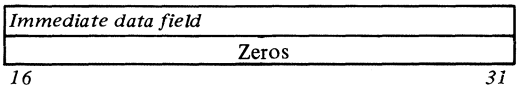
Halt I/O

The teletypewriter adapter responds to the channel-directed Halt I/O command by resetting all registers (except the prepare-field register), pending interrupts, and pending condition codes (see "Status After Resets" in this chapter).

Read

IDCB (immediate device control block)





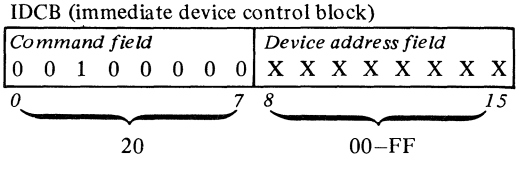
Bit 7 = 0 Read control interface line is disabled

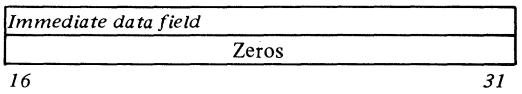
Bit 7 = 1 Read control interface line is enabled

The Read command loads the byte contained in the teletypewriter adapter receive-data register into bits 24–31 of the IDCB. If command-field bit 7=0, the read-control interface line is disabled. If command-field bit 7=1, the read-control interface line is enabled. No interrupts result from the execution of this command. If the teletypewriter adapter is in a read-busy or interrupt-pending state, condition code 1 (busy) is reported and the command is not executed. If condition code 5 (interface data check) is reported, the command is not executed. Note that the byte in the receive-data register is not changed as a direct result of a Read command. The data in the receive-data register is changed only by a normal receive operation.

Read ID

IDCB (immediate device control block)





The Read ID (identification) command loads the device-ID byte into bits 24–31 of the IDCB. The device ID for the teletypewriter adapter is 10 hex. The device-identification word contains a unique identification code and physical information about the device, and can be used to determine the devices that are attached to the system. The teletypewriter adapter does not report condition code 1 (busy) to this command. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Status Information

Condition codes containing the status of the I/O operation are reported to the processor. These codes are explained in the following sections.

Condition Codes Reported for an Operate I/O Instruction

The following condition codes are reported during an Operate I/O instruction.

Condition code	*Meaning*
0	*Device not attached*—reported if the teletypewriter adapter is addressed, but is not installed on the system.
1	*Busy*—reported by the teletypewriter adapter under the following conditions: 1. To a Write command—the teletypewriter adapter is executing a transmit operation to the attached device or has a device-end interrupt pending (write busy or interrupt pending). 2. To a Read command—the teletypewriter adapter is executing a normal receive operation or has an attention or exception interrupt pending (read busy or interrupt pending). The teletypewriter adapter is not busy to a Read command by reason of executing an overrun receive operation. Busy is reported to any command outside of the defined command set for the teletypewriter adapter if the teletypewriter adapter is in the write-busy, read-busy, or interrupt-pending states. Since the teletypewriter adapter supports full duplex operation (simultaneous read and write), it can be write busy and read busy, write busy and interrupt pending, or read busy and interrupt pending at the same time.
2	*Not reported*
3	*Command reject*—reported if the command issued is outside the defined command set for the teletypewriter adapter.
4	*Not reported*
5	*Interface data check*—reported if a parity error occurs on the data bus during data transfer.
6	*Not reported*
7	*Satisfactory*—reported when a command is accepted.

I/O Interrupt

The teletypewriter adapter initiates an I/O interrupt when the Prepare command sets the I bit in the prepare register to 1, and the following interrupts occur:

- Attention—a normal receive operation has been completed
- Exception—an overrun receive operation has been completed
- Device end—a transmit operation has been completed

Attention, exception, and device-end interrupts can be pending at the same time. If an exception interrupt and a device-end interrupt are pending at the same time, the exception interrupt takes precedence at interrupt-reporting time. The reporting and acceptance of the exception interrupt does not reset a pending device-end interrupt. The interrupt is defined by the condition code reported during interrupt acceptance. The teletypewriter adapter does not utilize the interrupt information byte (IIB) of the interrupt-ID word. The IIB is always presented as zeros.

Condition Codes Reported for an I/O Interrupt

The following condition codes are reported during an I/O interrupt.

Condition code	*Meaning*
0	*Not reported*
1	*Not reported*
2	*Exception*—reported when the teletypewriter adapter has completed at least one overrun receive operation. A device-end interrupt may be pending, but exception interrupt takes precedence in reporting.
3	*Device end*—reported at completion of the execution of a Write command or completion of an IPL operation. No exception interrupt is pending at interrupt-reporting time.
4	*Attention*—reported when the teletypewriter adapter has completed a normal receive operation.
5	*Not reported*
6	*Attention and exception*—reported when the teletypewriter adapter has completed a normal receive operation and has completed at least one overrun receive operation.
7	*Attention and device end*—reported after executing either a Write command or an IPL operation, and the teletypewriter adapter has completed a normal receive operation.

Status After Resets

The following table lists the resets caused by the various resetting conditions.

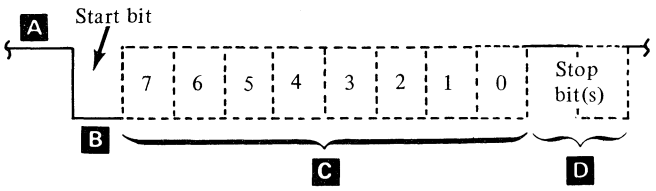
Condition	*Reset*				
	Pending interrupts	*Condition codes*	*Prepare level and I bit*	*Transmit data register*	*All other registers Except prepare level and transmit data*
Power-on reset	X	X	X	X	X
System reset	X	X	X	X	X
Halt I/O command	X	X		X	X
Reset to diagnostic wrap	X	X		X	X
Reset device	X	X			X

Operational Characteristics

Data Transmission

The teletypewriter adapter is fully duplexed and transmits and receives data serially by bit in 11-bit frames. Each frame contains a start bit, eight data bits, and one or two stop bits. All 256 combinations of the eight data bits can be transmitted/received.

As shown in Figure 3-1, each eight-bit data character is preceded by one start bit and followed by either one or two stop bits. Characters being transmitted by the teletypewriter adapter to a device are always followed by two stop bits; however, characters being received by the teletypewriter can have either one or two stop bits.



A The line is always held in a 'mark' condition when no data is being transmitted.

B The start bit is always a 'space' (logical zero).

C Eight data bits are transmitted for each character. Each bit is either a mark or a space, depending on the character code. Note that the least significant bit is transmitted first.

D The stop bit is always a mark (logical one). On transmit, two stop bits are always used. On receive, one or two stop bits can be used.

Figure 3-1. Character format

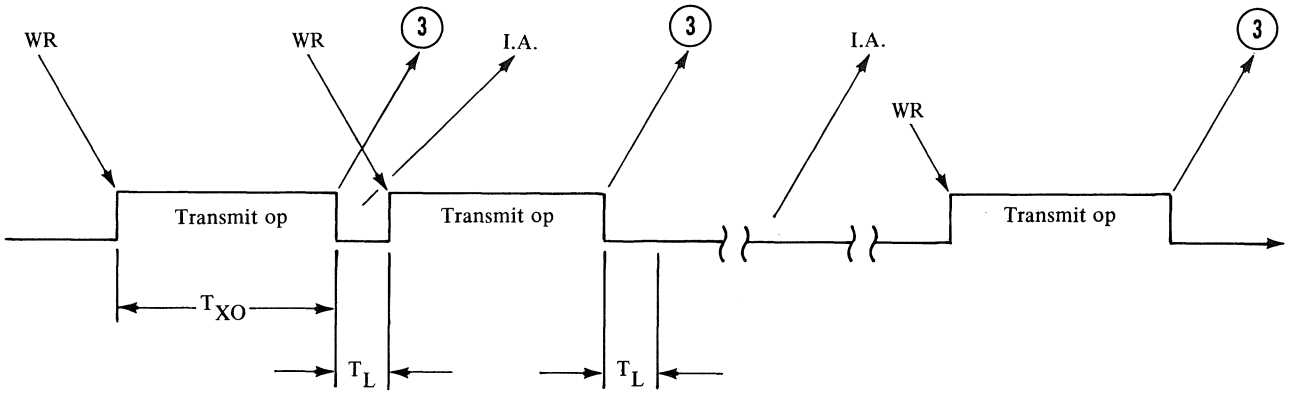
The teletypewriter adapter is code transparent and no error checking is done on transmitted or received data.

It is impossible to overrun on data being transmitted by the teletypewriter adapter, but it is possible to overrun on data being received. If a second character is received before the first character is serviced by the software, the first character will not be lost, but the second character will be lost.

Transmit Operation

Figure 3-2 is a timing diagram for transmit operations. "WR" on the figure denotes a Write command accepted; a circled 3 denotes the device-end interrupt; and "I.A." denotes interrupt acceptance by the processor.

TXO is the transmit time from initiation of a transmit operation to posting of the device-end interrupt. TXO is nine bit times at the selected bit rate. At 9600 BPS (bits per second), TXO is 0.936 ms; at 110 BPS it is 81.9 ms. TL is the transmit load time, measured from the posting of the device-end interrupt to the time at which the interrupt is accepted and another Write command can be issued to the adapter without loss of rated performance. TL is two bit times at the selected bit rate. For 9600 BPS, TL is 0.208 ms; at 110 BPS, it is 18.2 ms. If a new Write command is executed within time TL, the character rate is determined by the adapter clocking; that is, a new transmit operation is not initiated in less than time TL from the posting of the device-end interrupt. The adapter, however, is "write busy" upon successful execution of the Write command. If a new Write command is delayed beyond time TL, the transmit operation is initiated immediately upon successful receipt of the Write command.



Key:

(3)	=	Post device end interrupt (condition code 3)
I.A.	=	Interrupt accept
WR	=	Write command accepted

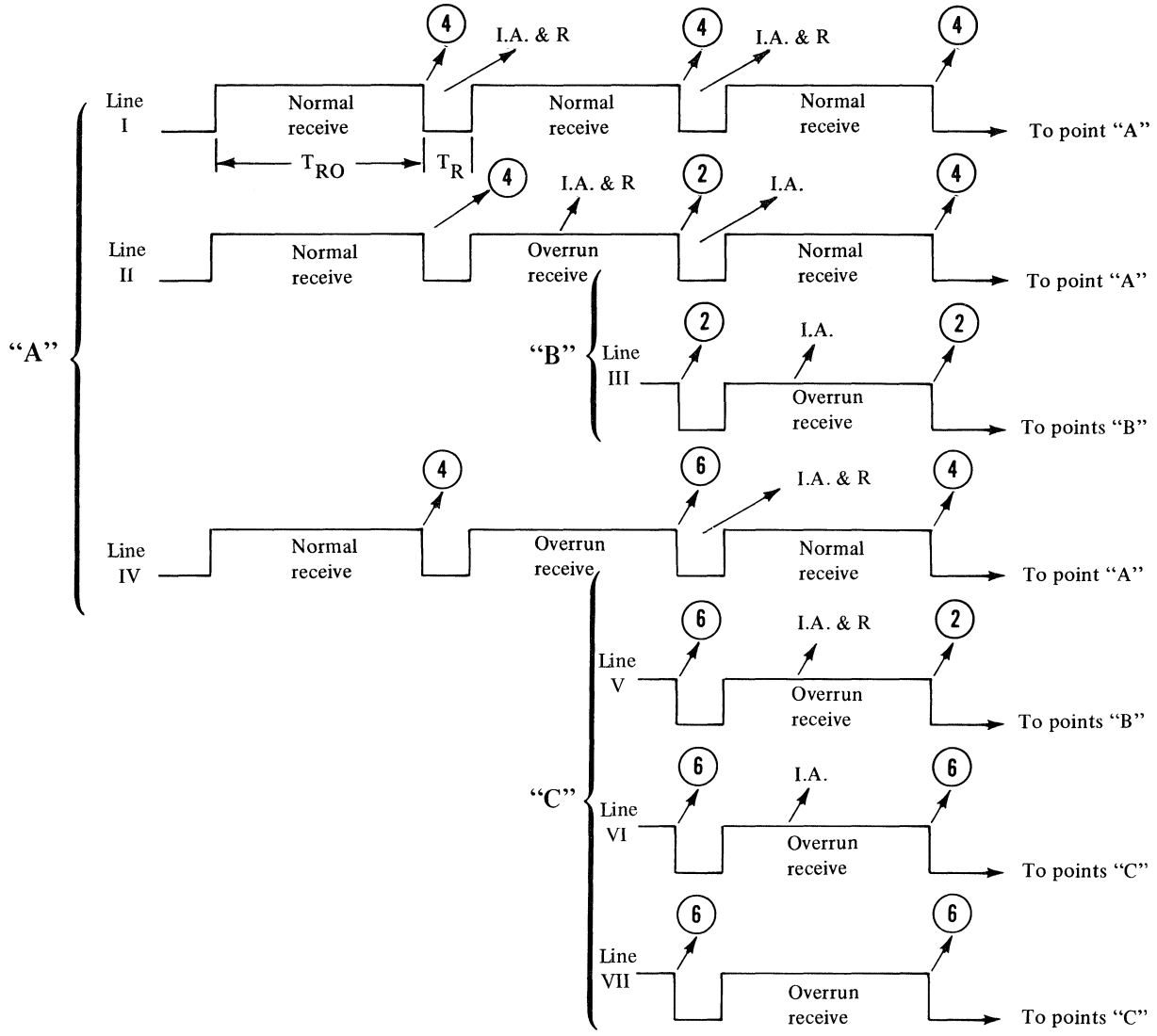
Baud rate	T_{XO} *(milliseconds)*	T_L *(milliseconds)*
9600	.936	.208
4800	1.87	.416
2400	3.74	.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{XO} and T_L are ±0.1%

Figure 3-2. Transmit operation timing diagram

Receive Operations

Figure 3-3 is a state and timing diagram for several possible receive operations. Three entry points on the left side of the diagram are identified by bracketed A, B, and C. All exits from the right enter at one of the points on the left. As shown in the key below the diagrams, a circled number denotes an interrupt and its associated condition code; an I.A. or an I.A.&R. denotes an interrupt accepted or interrupt accepted and read by the processor. Normal and overrun receive time envelopes are also shown.



Key:

"A" "B" "C" = Entry points on right side of diagram

(2) (4) (6) = Interrupt with circled condition code

I.A. = Interrupt accept

I.A. & R = Interrupt accept and execute read command

Baud rate	T_{RO} *(milliseconds)*	T_R *(milliseconds)* *
9600	.936	.208
4800	1.87	.416
2400	3.74	.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{RO} and T_R are ±0.1%

* This value of T_R is for attached devices generating two stop bits. If the attached device generates only one stop bit, T_R is one-half the value listed in this table.

Figure 3-3. State and timing diagram for possible receive operations

The figure also includes a table for the various device bit rates. The time for a receive operation from initiation by the device to the posting of an interrupt is called TRO. TRO is nine bit times at the selected frequency. For example, at 9600 BPS, TRO is 0.936 ms; at 110 BPS, TRO is 81.9 ms. The maximum time between receive operations is TR. TR is, on the average, two bit times at the selected frequency. For example, at 9600 BPS, TR is 0.208 ms average; at 110 BPS TR is 18.2 ms average. Any TR average calculations should be reduced by 15 percent to allow for device characteristics such as clock jitter, drift, etc.

The sequences shown in Figure 3-3 start from point A with a normal receive operation that ends with an attention interrupt being posted. The top line (line I) depicts interrupt acceptance and reading of the receive-data register within time TR. The second line (line II) depicts a delay in the interrupt acceptance and reading beyond time TR, or the initiation of another receive operation by the device if the device is not transmitting at rated speed. In this case, although the receive-data register can be read, the adapter has committed to an overrun receive operation; this results in an exception interrupt (condition code 2) when the current operation is completed. A Read command is not necessary following the acceptance of condition code 2. The extension of lines II and III depicts two other possibilities following a condition code 2; (1) the interrupt is accepted and the receive data register is read within time TR, leading to condition code 4, and (2) another delay in interrupt acceptance, leading to another condition code 2.

Line IV depicts a case of a very long delay in interrupt acceptance and reading, leading to condition code 6. The extension of lines IV, V, VI, and VII shows other possibilities following a condition code 6.

Note that some connections of basic sequences to entry points on the timing diagram can result in sequences that may be very long, depending upon the number of characters transmitted from the device.

Programming Considerations For Maximum Transmission-Receive Rates

The following list provides some examples of how to obtain maximum transmission rates.

- Interrupt servicing.
  At the beginning of the first stop bit, the teletypewriter adapter sends an interrupt request to the processor to signal the completion of the current character transmission. This interrupt must be serviced and another transmit operation initiated by the end of the second stop-bit time if maximum transmission rate is to be maintained.
- Device stop bits.
  Devices that are designed to receive either one or two stop bits may be attached to the teletypewriter adapter card. If the device is designed for only one stop bit, the second stop bit appears to be a one-bit-time separation between character frames. Therefore, if a device is programmable for either one or two stop bits, it should be programmed for only one stop bit. This programming will increase the receive data rate of the teletypewriter adapter by approximately 9 percent.
- Device data rates.
  If a device is programmable for several different data rates that can be supported by the teletypewriter adapter, the device should be programmed for the highest data-transfer rate that results in reliable operation in the environment in which the system is placed.
- Duplex operation.
  The teletypewriter adapter is a full duplex attachment. It can transmit and receive data simultaneously. Therefore, devices attached to the teletypewriter adapter should be configured for full duplex operation.

Chapter 4. Integrated Digital Input/Output Non-Isolated Feature

This chapter provides a functional description of and machine-language programming information for the Integrated Digital Input/Output Non-Isolated User Attachment Feature Card (referred to as the integrated digital I/O feature).

Functional Description

The Integrated Digital I/O Non-isolated Feature allows the user to add digital sensor I/O or non-IBM devices to the processor I/O channel.

The integrated digital I/O feature has the following general characteristics:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI).
- Two 16-point groups of non-isolated digital output (DO).
- Four device addresses—one for each DI/PI and DO group. All four devices are prepared for interrupts with one prepare command.
- External synchronization for each group of DI and DO—this user attachment feature permits asynchronous data transfers.
- Interrupts can be initiated by an external-sync input (one input for each DI or DO group) or by a "0"-to-"1" transition on a PI point.
- The feature is contained on one logic card and can be plugged into either the processor unit or an IBM 4959 I/O Expansion Unit.
- Commands for this feature are compatible with the digital commands for the Sensor Input/Output Unit (except for those commands associated with diagnostic programs). However, the sensor input/output unit does not have DO external synchronization.

Figure 4-1 shows a simplified data flow for the integrated digital I/O feature. Refer to this figure while reading the following sections.

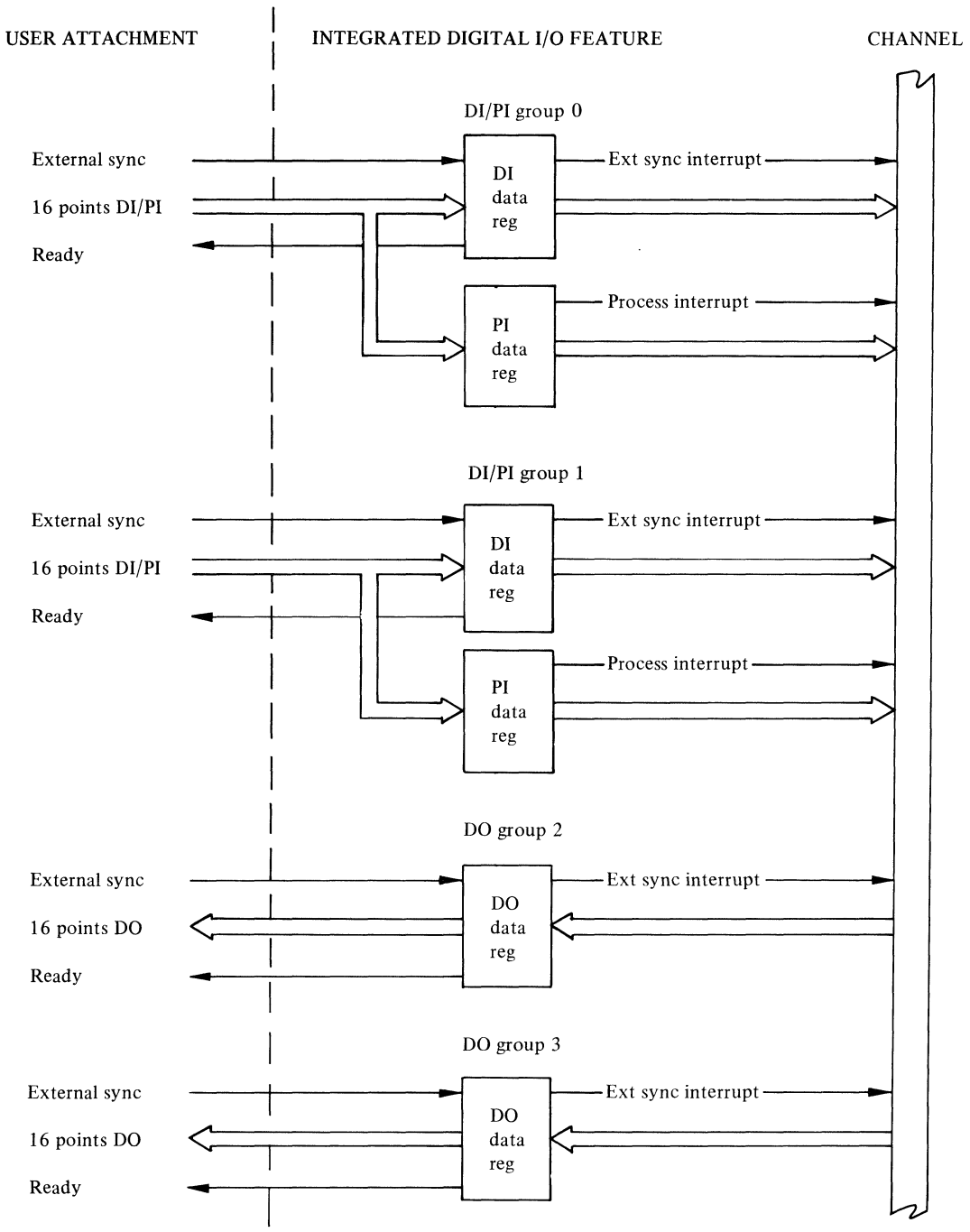


Figure 4-1. Digital I/O simplified data flow

Digital Input

The integrated digital I/O feature has two groups of digital input/process interrupt. Each group has:

- 16 non-isolated input points that sense voltage input
- One 16-position DI data register for reading unlatched data
- One 16-position PI data register for reading latched data
- An external-sync input line and a ready output line
- Interrupt capability from either external sync or process interrupt

Latched data causes the PI data register to latch up when its corresponding input goes active. The register holds this value until the program reads and resets it. This mode tells the user that an input signal changed at some time prior to the read instruction.

Non-latched data causes the DI data register contents to follow the changes on the corresponding input points. A read instruction in this mode checks the present condition of the customer input signals.

Each DI/PI group has a unique device address and responds to specific commands. Addressing and commands are discussed in subsequent sections of this chapter. The data registers and the functions performed by DI/PI are described in the remainder of this section.

Each position of the DI data register follows the state of the corresponding user-input point until the register is read. The data in the register is held (1) during a read command or (2) when the external-sync input becomes active while in external-sync mode. In the second case, the data remains held until the resulting interrupt is serviced and the ready line is activated. (For additional information, see "DI External Sync.")

Each position of the PI data register records, with a 1 bit, the first "0" bit to "1" bit transition on the corresponding user-input point. The data remains in the register until one of the following is executed:

1. Read-PI-with-Reset command
2. Arm PI command
3. Device Reset command
4. System reset
5. Power-on reset

When a bit in the PI data register becomes active, a process interrupt is generated if PI mode was previously set with an Arm PI command. (For additional information, see "Process Interrupt.")

A DI/PI group can be tested using two special commands: (1) Set Test Ones, and (2) Set Test Zeros. When the appropriate command is executed, the user inputs are disabled, either ones or zeros are placed on the input receivers, and the external-sync receiver is pulsed. Then, when subsequent read commands are issued, the group responds exactly as if the actual user inputs had been set, including the PI and external-sync functions.

DI External Sync

The DI external-sync capability consists of two signal lines, an input line called external sync, and an output line called ready (Figure 4-2). A DI group is set to external-sync mode by execution of the Arm-DI-External-Sync command. When external-sync mode is armed and the system is ready for more DI data, the ready line from the DI group is set active. The user places data on the input points, then activates the external-sync line. When the external-sync line becomes active, the data in the DI data register is assumed to be good, and the contents of the register are held. Then an interrupt is posted, and the ready line becomes inactive and stays inactive until the appropriate command, normally read DI, is executed. The external-sync line must then perform another transition from the "0" state to the "1" state to cause another interrupt.

External-sync mode is reset by an Arm PI command, a Device Reset command, a Halt I/O command, or any reset condition. (See "Status after Power Transitions or Resets" in this chapter.)

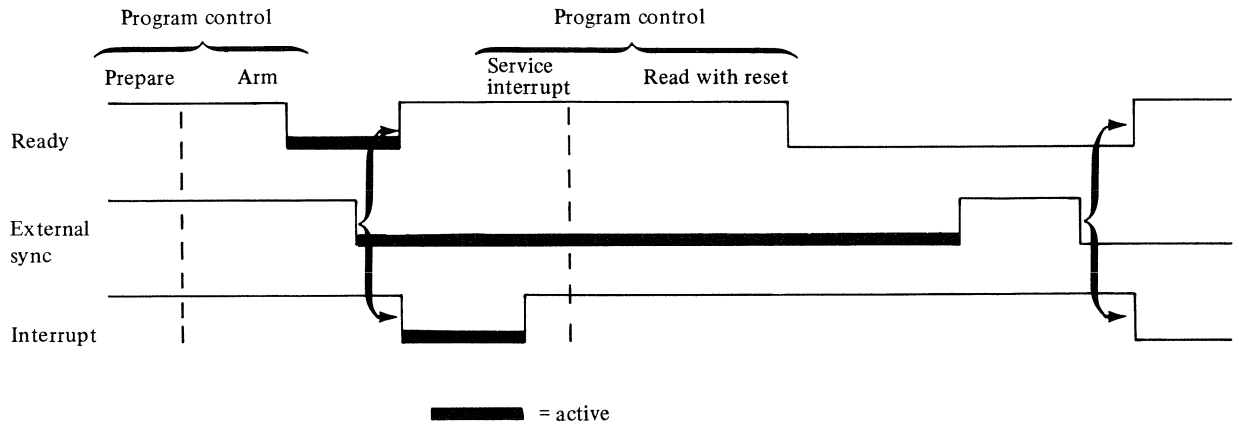


Figure 4-2. DI external sync timing diagram

Process Interrupt (PI)

A digital-input group is set to PI mode using the Arm PI command. The process-interrupt function is performed by logically ORing the bits in the PI data register of the DI group. That is, any bit in the register becoming active generates an interrupt.

PI mode is reset by an Arm-DI-External-Sync command, a Device Reset command, a Halt I/O command, or any reset condition. (See "Status after Power Transitions or Resets" in this chapter.)

Digital Output

The integrated digital I/O feature has two groups of digital output. Each DO group has:

- 16 output points to the user. Each point provides a non-isolated, unipolar current switch or TTL-compatible output voltage.
- One 16-position DO data register.
- An external-sync input line and a ready output line.
- Interrupt capability from the external-sync input line.

Each digital-output group has a unique device address and responds to the commands discussed later in this chapter. Data is stored in the DO data register by the Write DO command. The DO data register is reset only by a power-on reset.

A DO group can be tested using three special commands: (1) Disable DO (2) Read DO, and (3) Set-Diagnostic-External-Sync. The Disable DO command disables the user outputs. The Read DO command reads the contents of the DO data register. The Set-Diagnostic-External-Sync command disables the user outputs and simulates the user's external-sync line.

DO External Sync

The DO external sync interface consists of two signal lines, an input line called external sync and an output line called ready (Figure 4-3). A DO group is set to external-sync mode by execution of the Arm-DO-External-Sync command. When a Write DO command is executed in external-sync mode and the data on the DO output is good, an active level on the external-sync input line causes the ready line to become active. The user signifies receipt of the data by deactivating the external-sync line. Then an interrupt is posted, and the ready line becomes inactive. The ready line stays inactive until another Write DO command is executed and the external-sync input becomes active again. The external-sync line must perform another transition from the "1" state to the "0" state to cause another interrupt.

External-sync mode is reset by a Device Reset command, a Halt I/O command, or any reset condition. (See "Status after Power Transitions or Resets" in this chapter.)

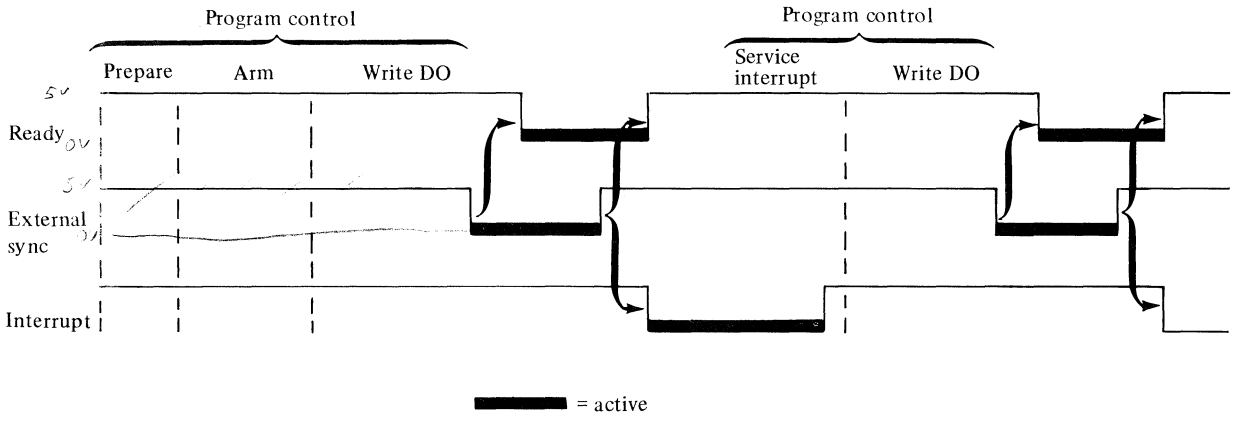


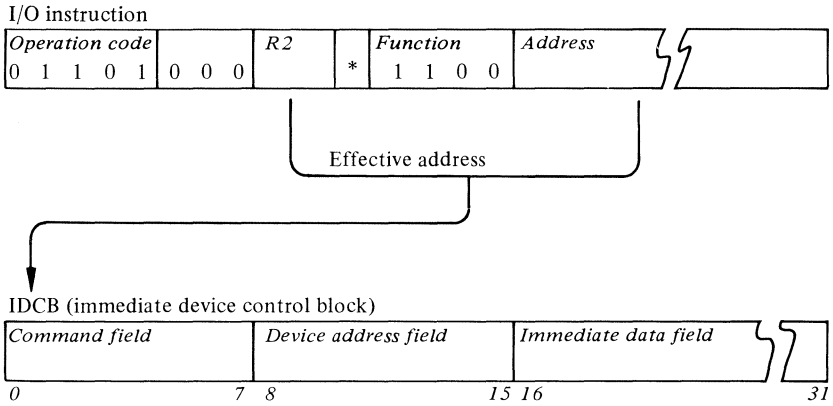
Figure 4-3. DO external sync timing diagram

Programming Information

The integrated digital I/O feature is connected to the processor through the I/O channel. Direct program control (DPC) commands are used for all I/O operations; cycle-steal mode is not implemented.

Operate I/O

Communication between the processor and the device attached to the integrated digital I/O feature is initiated by the processor. All integrated digital I/O feature functions (control and read) must be initiated with Operate I/O instructions stored in the processor.

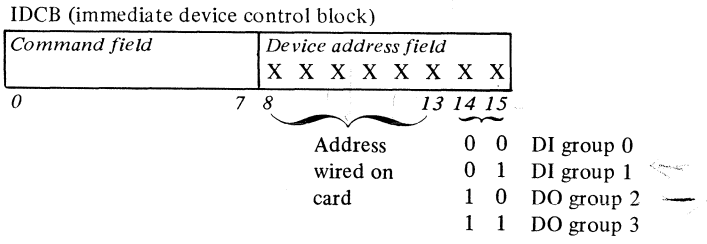


*Indirect addressing bit

The address field (bits 16–31) and the contents of the register specified in the R2 field (bits 8–10) of the Operate I/O instruction generate an effective address that points to a main-storage location containing an immediate device control block (IDCB). IDCBs are doubleword blocks of storage reserved by programs for storage of device-directed commands.

Addressing

The integrated digital I/O feature has four device addresses: one for each 16-point group.

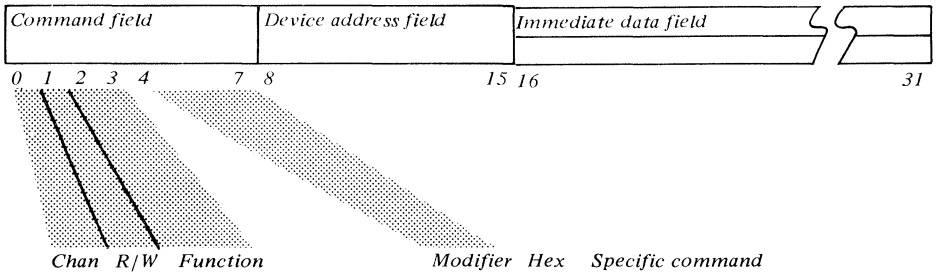


The first six (high-order) bits of the device-address field of the IDCB are defined by field-installable connectors (jumpers) on the integrated digital I/O feature card. The last two bits of the field define the DI groups. Bit values of 00 and 01 in bits 14 and 15 define the DI groups, and bit values of 10 and 11 define the DO groups.

Summary of Digital Input Commands

The two DI groups execute the device-directed commands shown in the following illustration and described in the following sections.

IDCB (immediate device control block)

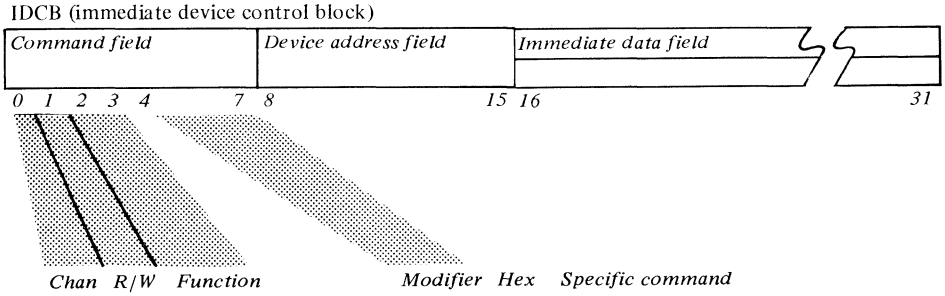


Chan	R/W	Function	Modifier	Hex	Specific command
0	0	00 Read	0000	00	Read DI
0	0	00 Read	0001	01	Read PI
0	0	00 Read	0010	02	Read PI with reset
0	0	10 Read status	0000	20	Read ID
0	0	10 Read status	1000	28	Read status
0	1	10 Control	0000	60	Prepare
0	1	10 Control	1000	68	Arm PI
0	1	10 Control	1001	69	Arm DI external sync
0	1	10 Control	1010	6A	Set test 0
0	1	10 Control	1011	6B	Set test 1
0	1	10 Control	1111	6F	Device reset

Summary of Digital Output Commands

The two DO groups execute the device-directed commands shown in the following illustration and described in the following sections.

IDCB (immediate device control block)



Chan	R/W	Function	Modifier	Hex	Specific command
0	0	10 Read status	0000	20	Read ID
0	0	10 Read status	0001	21	Read DO
0	0	10 Read status	1000	28	Read status
0	1	00 Write	1000	48	Write DO
0	1	10 Control	0000	60	Prepare
0	1	10 Control	1001	69	Arm DO external sync
0	1	10 Control	1011	6B	Set diagnostic external sync
0	1	10 Control	1100	6C	Disable DO
0	1	10 Control	1111	6F	Device reset

Commands, Digital Input

Prepare

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	0	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

60

Immediate data field		
Zeros	Level	I
16	*26 27*	*30 31*

Bits 27–30 Level Bit 31

0000	0	0 = interrupts
0001	1	not allowed
0010	2	1 = interrupts
0011	3	allowed

Execution of the Prepare command enables the integrated digital I/O feature to interrupt on the level defined in the immediate data field of the IDCB. All groups of DI and DO (four device addresses) are prepared to the same level and are enabled by the same I bit. Previous Prepare commands are overridden.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Arm PI

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

68

Immediate data field
Zeros
16 *31*

Execution of the Arm PI command sets the addressed digital-input group to the PI mode. If external-sync mode was armed, it is reset.

If an interrupt is pending, condition code 1 (busy) is reported and the command is not executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

See "Process Interrupt" in this chapter for information about the use of this command.

Arm-DI-External-Sync

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

69

Immediate data field
Zeros
16 *31*

Execution of the Arm-DI-External-Sync command sets the addressed DI group to the external-sync mode. If PI mode was armed, it is reset. The ready line is activated.

If an interrupt is pending, condition code 1 (busy) is reported and the command is not executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

See "DI External Sync" in this chapter for information about the use of this command.

Set-Test-0

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	1	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

6A

Immediate data field
Zeros
16 *31*

The Set-Test-0 command sets a diagnostic mode that disables the user inputs including external sync. The ready line is disabled. This command places 0 bits in the digital-input registers and pulses the external-sync input. If external sync is armed, an interrupt is posted.

Subsequent read commands result in all 0 bits from the DI and PI data registers.

If an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Set-Test-1

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

6B

Immediate data field
Zeros
16 ... *31*

The Set-Test-1 command sets a diagnostic mode that disables the user inputs including external sync. The ready line is disabled. The command places 1 bits in the DI and PI registers and activates the external-sync registers. If external sync is armed, an interrupt is posted.

Subsequent read commands result in all 1 bits from the DI data register. The data in the PI data register is all 1 bits until reset.

If an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Device Reset

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

6F

Immediate data field
Zeros
16 ... *31*

Execution of this command resets the following items for the addressed digital-input group:

1. Any pending interrupt
2. Arm condition for PI mode
3. Arm condition for external-sync mode
4. Status word
5. PI data register
6. DI data register

Read DI

IDCB (immediate device control block)

Command field								*Device address field*							
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

00

Immediate data field
Data from DI group
16 ... *31*

The Read DI command transfers the 16 bits from the DI data register into the immediate data field of the IDCB. If external-sync mode is armed, the ready line of the addressed DI group is activated to indicate that the system is ready for more data.

If external-sync mode is armed and an interrupt is pending, condition code 1 (busy) is returned and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read PI

IDCB (immediate device control block)

Command field								*Device address field*							
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

01

Immediate data field
Data from PI
16 ... *31*

The Read PI command transfers the 16 bits from the PI data register into the immediate data field of the IDCB. The PI data register is not reset.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read-PI-With-Reset

IDCB (immediate device control block)

Command field	*Device address field*
0 0 0 0 0 0 1 0	X X X X X X X X
0 ... *7*	*8* ... *15*

02

Immediate data field
Data from PI
16 ... *31*

The Read-PI-With-Reset command transfers the 16 bits from the PI data register into the immediate data field of the IDCB. At the end of the command cycle, the data latched in the PI data register is reset.

If PI mode is armed and an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read ID

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*

20

Immediate data field
1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0
16 ... *31*

C 0 1 0

The Read ID (identification) command transfers a one-word identification field, called the DI ID word, into the immediate data field of the IDCB. The hexadecimal value of the integrated digital I/O feature DI ID word is C010. The device-identification word contains a unique identification code and physical information about the device, and can be used to determine the devices that are attached to the system.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read Status

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 1 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*

28

Immediate data field
Status word from DI group
16 ... *31*

The Read Status command transfers the DI status word from the adapter into the immediate data field of the IDCB.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

After the Read Status command is executed, the DI status word bits in the second word of the IDCB have the following meaning:

Immediate data field															
0	0	X	X	X	X	X	X	0	0	0	0	0	0	0	0
16	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*							*31*

00 = No interrupt is pending.

01 = The interrupt has been serviced, but either the PI register has not been reset (PI mode) or ready has not been set (external - sync mode).

10 = Invalid bit combination.

11 = The device is in an interrupt state. If the device is prepared, an interrupt is being presented to the channel.

1 = Set - test - 0 mode is set.

1 = Set - test - 1 mode is set.

1 = External - sync mode is armed.

1 = PI mode is armed.

Commands, Digital Output

Prepare

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	0	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

60

Immediate data field		
Zeros	Level	1
16	*26 27*	*30 31*

Bits 27–30	Level	Bit 31
0000	0	0 = interrupts
0001	1	not allowed
0010	2	1 = interrupts
0011	3	allowed

Execution of the Prepare command enables the integrated digital I/O feature to interrupt on the level defined in the immediate data field of the IDCB. All groups of DI and DO (four device addresses) are prepared to the same level and are enabled by the same I bit. Previous Prepare commands are overridden.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Arm-DO-External-Sync

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

69

Immediate data field
Zeros
16 *31*

Execution of the Arm-DO-External-Sync command sets the addressed DO group to the external-sync mode.

If an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Write DO

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	0	0	1	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

48

Immediate data field
Data to DO
16 *31*

The Write DO command transfers the contents of the immediate data field of the IDCB into the DO data register. If external-sync mode is armed and no interrupt is pending, the ready line for the DO group is enabled.

If an interrupt is pending or ready is active in the external-sync mode, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read ID

IDCB (immediate device control block)

Command field								*Device address field*							
0	0	1	0	0	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

20

Immediate data field															
1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
16															*31*
C				0				1				8			

ID word from a DO group

The Read ID (identification) command transfers a one-word identification field, called the DO ID word, into the immediate data field of the IDCB. The hexadecimal value of the integrated digital I/O feature DO ID word is C018. The device-identification word contains a unique identification code and physical information about the device and can be used to determine the devices that are attached to the system.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read DO

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 1	X X X X X X X X
0 ... *7*	*8* ... *15*

21

Immediate data field
Data from DO group
16 ... *31*

The Read DO command transfers the contents of the DO data register into the immediate data field of the IDCB. This command is used primarily for diagnostic purposes.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Read Status

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 1 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*

28

Immediate data field
Status word from DO group
16 ... *31*

The Read Status command transfers the DO status word from the adapter into the immediate data field of the IDCB.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

After the Read Status command is executed, the DO status word bits in the second word of the IDCB have the following meanings:

Immediate data field
0 0 X X X 0 X X 0 0 0 0 0 0 0 0
16 17 18 19 20 21 22 23 24 ... *31*

- *00 = No interrupt is pending.*
- *01 = The interrupt has been serviced, but ready has not been enabled.*
- *10 = Invalid bit combination.*
- *11 = The device is in an interrupt state. If the device is prepared, an interrupt is being presented to the channel.*
- *1 = Diagnostic external sync was set.*
- *1 = External - sync mode is armed.*
- *1 = Disable mode is set.*

Set-Diagnostic-External-Sync

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 0 1 1	X X X X X X X X
0 ... *7*	*8* ... *15*

6B

Immediate data field
Zeros
16 ... *31*

Execution of the Set-Diagnostic-External-Sync command sets a diagnostic mode that disables the user's external-sync input. The ready line and the DO outputs are also disabled. This command activates external sync. With the external-sync mode armed, a Disable DO command executed, and no interrupt is pending, an interrupt is posted.

If an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Disable DO

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*

6C

Immediate data field
Zeros
16 ... *31*

The Disable DO command sets a diagnostic mode that disables the output lines for the 16 digital outputs, the ready line, and the user's external-sync input. A zero level is forced on all outputs.

If an interrupt is pending, condition code 1 (busy) is reported and the command was not successfully executed. If condition code 5 (interface data check) is reported, the command was not successfully executed.

Device Reset

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 1 1 1	X X X X X X X X
0 ... *7*	*8* ... *15*

6F

Immediate data field
Zeros
16 ... *31*

Execution of the Device Reset command resets the following items for the addressed digital-output group:

1. Any pending interrupt
2. Arm condition for DO external-sync mode
3. Status word
4. Diagnostic mode

The DO data register is not reset.

Condition Codes Reported During the Operate I/O Instruction

The following table is a summary of the condition codes that can be reported when the Operate I/O instruction is executed.

		Condition code values							
Command		*CC0*	*CC1*	*CC2*	*CC3*	*CC4*	*CC5*	*CC6*	*CC7*
00	Read DI	X	X				X		X
01	Read PI	X					X		X
02	Read-PI-With-Reset	X	X				X		X
20	Read ID	X					X		X
21	Read DO	X					X		X
28	Read Status	X					X		X
48	Write DO	X	X				X		X
60	Prepare	X					X		X
68	Arm PI	X	X				X		X
69	Arm-DI-External-Sync	X	X				X		X
69	Arm-DO-External-Sync	X	X				X		X
6A	Set-Test-0	X	X				X		X
6B	Set-Test-1	X	X				X		X
6B	Set-Diagnostic-Ext-Sync	X	X				X		X
6C	Disable DO	X	X				X		X
6F	Device Reset	X							X

Legend:

CC0 = Device not attached
CC1 = Busy
CC2 = Busy after reset
CC3 = Command reject
CC4 = Intervention required
CC5 = Interface data check
CC6 = Controller busy
CC7 = Satisfactory

Interrupt Presentation and Status Words

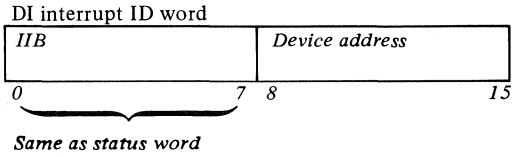
The integrated digital I/O feature presents only interrupt condition code 4 (attention). Interrupts for a DI group are initiated by (1) the external-sync input becoming active while in external-sync mode, or (2) any bit in the PI register becoming active while in PI mode. Interrupts for a DO group are initiated by the external-sync input becoming inactive while in external-sync mode.

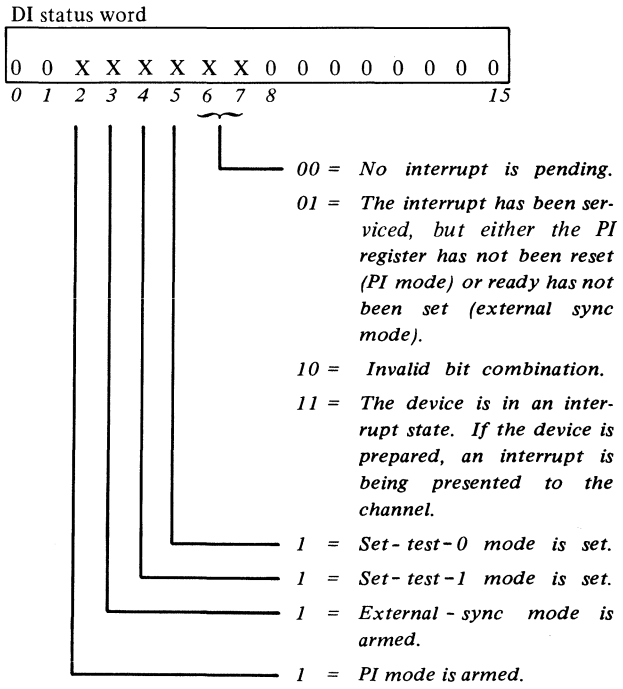
Because all devices are prepared to interrupt on the same level, interrupts from more than one device are stacked. The device with the lowest device address presents its interrupt first. All other interrupts waiting in the stack at that time are cleared before the same device can present a second interrupt. That is, if devices 0, 1, and 2 have interrupts stacked, device 0 presents its interrupt first. Device 0 cannot present another interrupt until the interrupts for devices 1 and 2 have been presented.

When an interrupt is accepted by the channel, the digital group presents an interrupt ID word. This word contains an IIB (interrupt information byte) in bits 0–7 and the device address in bits 8–15. The format of the IIB for the DI groups and for the DO groups appears in the following sections. Note that the IIB presented in the interrupt ID word has the same format as the first byte of the status word transferred into the immediate data field of the IDCB when a Read Status command is executed.

DI Status Word and Interrupt ID Word

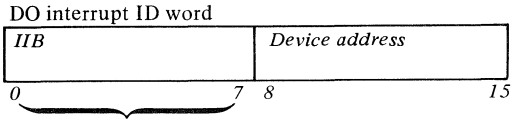
As previously stated, bits 0–7 in the DI status word have the same meaning as those in the IIB. The meanings of each bit are defined as follows:

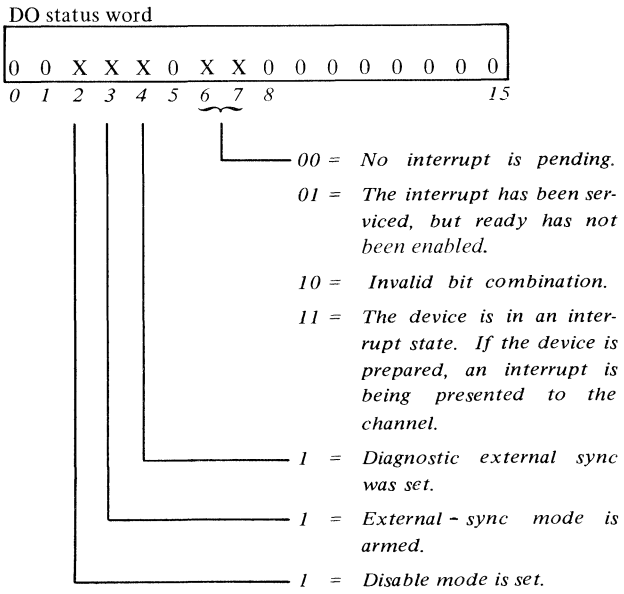




DO Status Word and Interrupt ID Word

Bits 0–7 in the DO status word have the same meanings as those in the IIB. The meanings of each bit are defined as follows:





Status After Power Transitions and Resets

The following table lists the resets for the various resetting conditions.

Condition	*Reset*						
	Arm conditions for PI or external sync modes	*Diagnostic modes*	*Ready lines*	*Any pending interrupts*	*Prepared level and I bit*	*PI and DI data registers (DI resets only)*	*DO Data registers (DO resets only)*
Power-on reset	X	X	X	X	X	X	X
System reset	X	X	X	X	X	X	
Halt I/O command or machine check reset	X	X	X	X			

Chapter 5. Customer Direct Program Control Adapter Feature

This chapter provides a functional description of and machine-language programming information for the Customer Direct Program Control Adapter User Attachment Feature card (referred to as the customer DPC adapter).

Functional Description

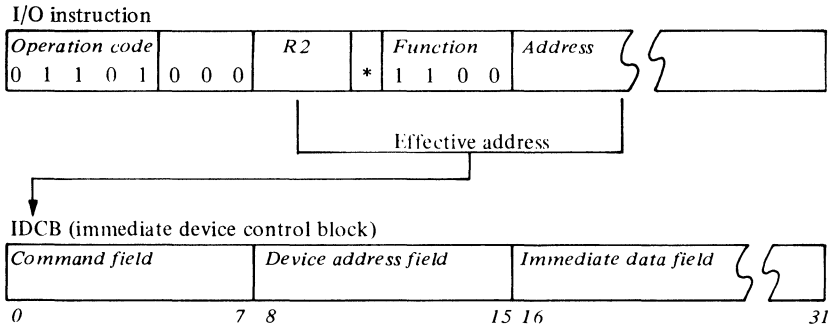
The customer DPC adapter feature card provides a convenient means of attaching I/O devices and subsystems to a Series/1. It is connected to the processor via the processor I/O channel. The adapter is designed to perform direct program control (DPC) functions only; cycle-steal operations cannot be performed. This feature card can be configured to accommodate 4, 8, or 16 I/O device addresses. The customer DPC adapter provides interrupt vectoring of 16 interrupt sources.

There are 75 signal lines including: 18 data bus out, 18 data bus in, 16 interrupt request in, 3 function bits, 4 modifier bits, 4 device address bits, and 12 control and response lines. The data flow is always 16 bits without parity option or 18 bits with parity option (2 parity bits).

Programming Information

Operate I/O

Communication between the processor and the device attached to the customer DPC adapter is initiated by the processor. All customer DPC adapter functions (control, write, and read) must be initiated with Operate I/O instructions stored in the processor.



*Indirect addressing bit

The address field (bits 16–31) and the contents of the register specified in the R2 field (bits 8–10) of the Operate I/O instruction generate an effective address that points to a main-storage location containing an immediate device control block (IDCB). IDCBs are doubleword blocks of storage reserved by programs for storage of device-directed commands.

Addressing

The customer DPC adapter can be configured for 4, 8, or 16 device addresses by field-installable connectors (jumpers).

The first four (high-order) bits of the device address field of the IDCB are defined by field-installable jumpers on the feature card. The next two bits are defined by field-installable jumpers only if the feature card is configured for four or eight devices. The low-order bits that are not used to address the adapter card are used for device addressing within the domain established by the feature-card address.

Condition Codes Reported During the Operate I/O Instruction

The following table is a summary of the condition code values that can be reported when the Operate I/O instruction is executed.

Command		Condition code values CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
0X	Read Data	X	X	X	X	X	X	X	X
1X	Read Data	X	X	X	X	X	X	X	X
20	Read ID	X					X		X
2X	Read Status	X	X	X	X	X	X	X	X
2E	Read Adapter Status Word	X					X		X
2F	Read Adapter Diagnostic Data	X					X		X
4X	Write Data	X	X	X	X	X	X	X	X
60	Prepare	X					X		X
61	Set Diagnostic Mode	X					X		X
62	Reset Diagnostic Mode	X					X		X
6X	Write Control	X	X	X	X	X	X	X	X

Legend:

CC0 = Device not attached
CC1 = Busy
CC2 = Busy after reset
CC3 = Command reject
CC4 = Operator intervention required
CC5 = Interface data check
CC6 = Controller busy
CC7 = Satisfactory

Commands

Commands to the customer DPC adapter are of two kinds: adapter directed and device directed.

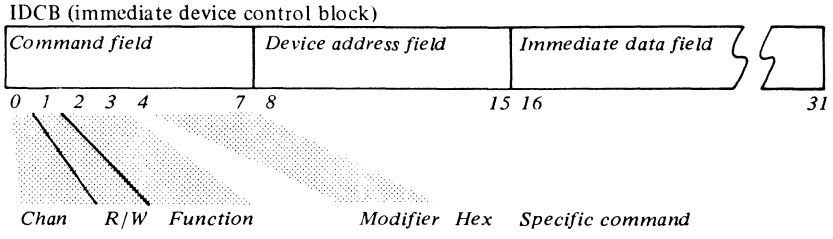
Adapter-directed commands are IBM defined and perform specific actions using only the adapter. These commands must use the function and modifier codes specified.

Device-directed commands are defined by the user. Because IBM does not know what device will be attached to the feature card, the adapter-directed commands can be defined only in a general way that specifies whether information will be transferred from the processor to the device or from the device to the processor. For specific information about device-directed commands, consult the specifications for the device being connected.

Commands, Adapter Directed

The customer DPC adapter card executes the adapter-directed commands shown in the following illustration.

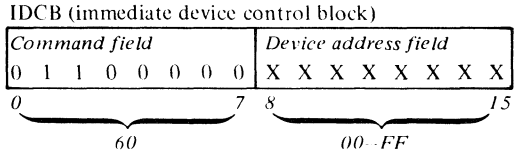
IDCB (immediate device control block)

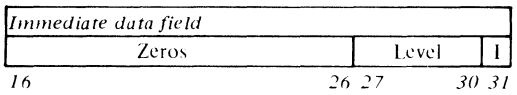


Chan	R/W	Function	Modifier	Hex	Specific command
0	0	10	1110	2E	Read status word
0	0	10	1111	2F	Read diagnostic data
0	1	10	0000	60	Prepare
0	1	10	0001	61	Set diagnostic mode
0	1	10	0010	62	Reset diagnostic mode

Prepare

IDCB (immediate device control block)



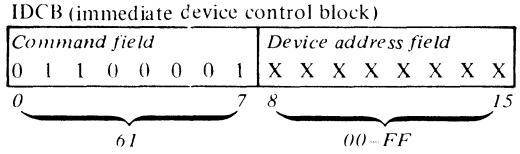


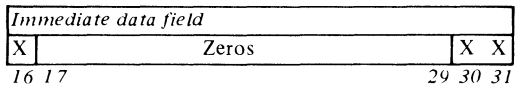
Execution of this command prepares the customer DPC adapter to interrupt on the level defined in the immediate data field of the IDCB. All devices are prepared to the same level and are enabled by the same I bit. Previous Prepare commands are overridden.

If condition code 5 (interface data check) is reported, the command was not successfully executed.

Set Diagnostic Mode

IDCB (immediate device control block)





Execution of the Set Diagnostic Mode command sets the adapter into diagnostic mode and resets the diagnostic register. The diagnostic mode provides wrap-back to the diagnostic register of the adapter control and data lines which are available to the attached devices. This mode also controls the generation of interrupts. The particular diagnostic functions performed are controlled by the bits in the immediate data field of the IDCB.

IDCB Bit 16 = 0

When bit 16 of the immediate data field is 0, the Set Diagnostic Mode command is directed to the adapter card. This command places the adapter in the local-diagnostic mode. When the adapter is in local-diagnostic mode, output and input parity-error bits in the status word are always zero, all interrupts from the attached I/O devices are masked, data from the I/O devices is ignored, and the data and control lines from the adapter to the I/O devices are inactive. Any subsequent device-directed commands are responded to by the adapter. Within these parameters, further responses are controlled by bits 30 and 31 of the immediate data field.

IDCB Bits 30 and 31 = 00

With bits 30 and 31 = 0, the adapter initiates an attention interrupt. The interrupt information byte (IIB) presented is all zeros and the device address is either DDDD0000 for a 16-device, DDDDD000 for an 8-device, or DDDDDD00 for 4-device configuration (the Ds are high-order bits of the device address on the adapter card). After the interrupt is serviced by the channel, the interrupt request will be reset. If an additional interrupt request is desired, another Set Diagnostic Mode command with the same data format must be issued.

IDCB Bits 30 and 31 = 01

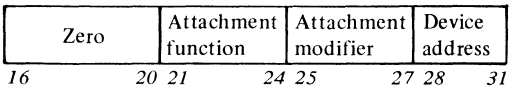
With bits 30 and 31 = 01, the adapter loads data into the diagnostic register during any subsequent device-directed command. The data loaded is device-directed command dependent.

Write-or-Write-Control Command. The Write-or-Write-Control command loads the immediate data field of the IDCB into the diagnostic register. The contents of the diagnostic register can be read by issuing a Read Diagnostic Data command. If an interface parity error is detected, condition code 5 (interface data check) is returned, the command is not executed, and the data in the diagnostic register is not changed.

Read-or-Read-Status Command. The Read-or-Read-Status command loads all zeros into (1) the immediate data field of the IDCB and (2) the diagnostic register. If condition code 5 (interface data check) is reported, the data in the IDCB is not valid and the data in the diagnostic register is not changed.

IDCB Bits 30 and 31 = 10

With bits 30 and 31 = 10, the adapter loads the information from the I/O devices into the diagnostic register. This loading is done during any subsequent device-directed command. Under this mode of operation, the data in the diagnostic register is formatted as follows:



The attachment function, attachment modifier, and device address shown above represent control lines between the adapter and the attached devices. The attachment-function and modifier bits are equivalent to bits 1 through 7 of the command field in the IDCB.

The data loaded into the diagnostic register depends upon the subsequent device-directed command.

Write-or-Write-Control Command. The Write-or-Write-Control command loads the information from the adapter-to-I/O device control lines into the diagnostic register. The contents of the diagnostic register are read when a Read Diagnostic Data command is issued.

If an interface parity error is detected, condition code 5 (interface data check) is returned, the command is not executed, and the data in the diagnostic register is not changed.

Read-or-Read-Status Command. The Read-or-Read-Status command loads (1) all zeros into the immediate-data field of the IDCB and (2) the information from the adapter-to-I/O device control lines into the diagnostic register. The contents of the diagnostic register is read when a Read Diagnostic Data command is issued.

If an interface parity error is detected, condition code 5 (interface data check) is reported, the data in the immediate data field of the IDCB is not valid, and the data in the diagnostic register is not changed.

IDCB Bits 30 and 31 = 11

The control lines described in "IDCB Bits 30 and 31 = 01" and in "IDCB Bits 30 and 31 = 10" are logically ANDed for any subsequent device-directed command, and the result is loaded into the diagnostic register. The data loaded into the diagnostic register depends upon the subsequent device-directed command.

Write-or-Write-Control Command. The Write-or-Write-Control command loads the data resulting from the AND operation (described above) into the diagnostic register. The contents of the diagnostic register is read when a Read Diagnostic Data command is issued.

If an interface parity error is detected, condition code 5 (interface data check) is returned, the command is not executed, and the data in the diagnostic register is not changed.

Read-or-Read-Status Command. The Read-or-Read-Status command loads all zeros into (1) the immediate data field of the IDCB and (2) the diagnostic register. The contents of the diagnostic register is read when a Read Diagnostic Data command is issued.

If an interface parity error is detected, condition code 5 (interface data check) is reported, the data in the immediate data field is not valid, and the data in the diagnostic register is not changed.

IDCB 16 = 1

When bit 16 = 1, the customer DPC adapter is placed in the external-diagnostic mode. While in the external-diagnostic mode, device-directed commands are passed to the I/O devices, the control and data lines between the adapter and the I/O devices function normally, and the data received by the adapter from the I/O devices is loaded into the diagnostic register.

Bits 30 and 31 of the immediate data field of the set-diagnostic-mode IDCB provide variables for the external-diagnostic mode. For example, when bit 30 is on, all I/O devices attached to the adapter are reset. Bit 31 functions as a diagnostic-mode modifier.

The I/O-device designer defines the specific external-diagnostic-mode commands. Consult the literature for the particular device for exact command definitions.

Reset Diagnostic Mode

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 1 0	X X X X X X X X
0 ... 7	8 ... 15
62	00–FF

Immediate data field
Zeros
16 ... 31

The Reset Diagnostic Mode command resets the customer DPC adapter diagnostic mode and diagnostic register. The immediate data field of the IDCB is not used, but parity is checked.

If condition code 5 (interface data check) is reported, the command was not successfully executed. If the adapter is not in diagnostic mode, the command is accepted, but no resetting is performed.

Read-Adapter-Status-Word

IDCB (immediate device control block)

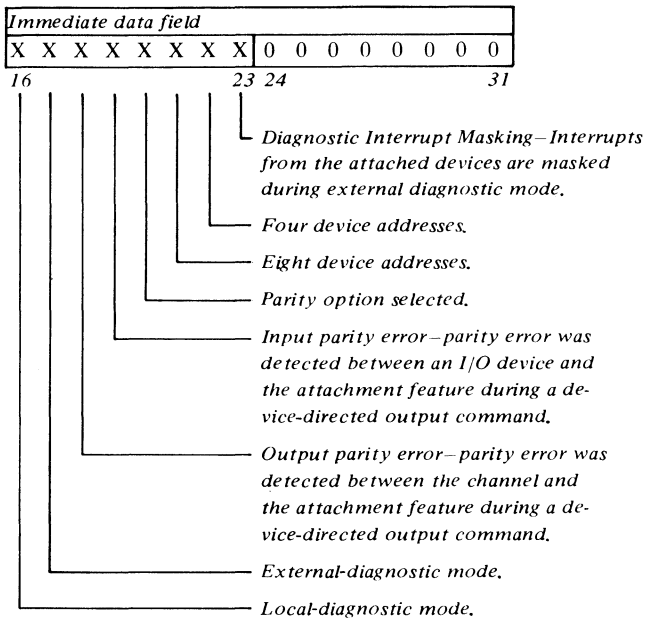
Command field	*Device address field*
0 0 1 0 1 1 1 0	X X X X X X X X
0 ... 7	8 ... 15
2E	00–FF

Immediate data field
Status word from attachment
16 ... 31

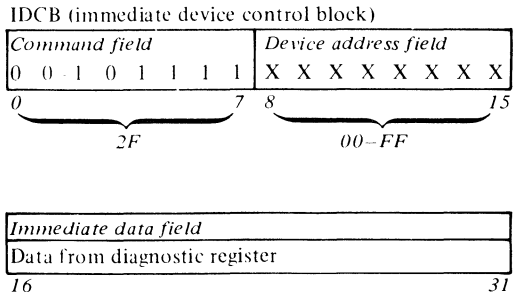
The Read-Adapter-Status-Word command transfers the 16 bits of the adapter-status word to the immediate data field of the IDCB. The output and input parity-error bits are reset. (These two bits are also reset by the successful execution of any other I/O command.)

If condition code 5 (interface data check) is reported, the status word in the IDCB data field is not valid.

After the Read-Adapter-Status-Word command is executed, the status-word bits in the second word of the IDCB have the following meaning:



Read Diagnostic Data



The Read Diagnostic Data command transfers the 16 bits from from the diagnostic register into the immediate data field of the IDCB. The diagnostic register is not reset.

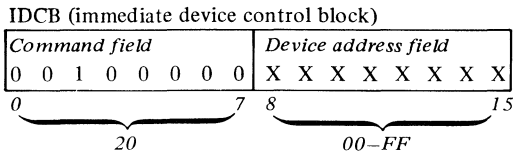
If condition code 5 (interface data check) is reported, the data in the IDCB is not valid.

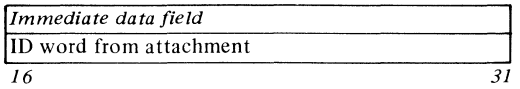
If the adapter is not in diagnostic mode, execution of this command will transfer all zeros to the IDCB immediate data field.

Commands, Device Directed

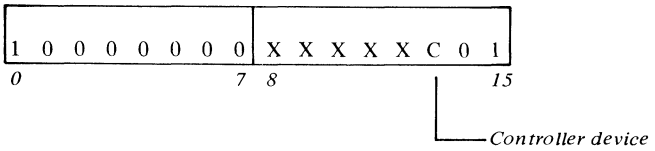
IBM defines two device-directed commands: Read ID and Device Reset. All other device-directed commands are defined by the I/O-device being connected.

Read ID

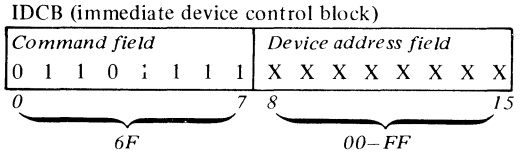


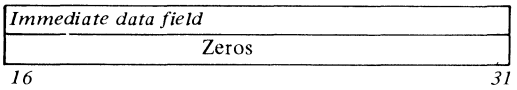


The Read ID (identification) command transfers the ID word from the device and the customer DPC adapter to the immediate data field of the IDCB. The contents of the ID word are:



Device Reset





The Device Reset command resets the addressed device. Any pending interrupts are cleared.

Designer-Defined Device-Directed Commands

The following designer-defined commands (except those combinations of XXXXs that result in IBM-defined commands) are available for use with the customer DPC adapter. Note that any unspecified or IBM-defined bit combinations for the IDCB command field are reserved, and must not be used.

Command field	*Command type*
0000 xxxx	Read data
0001 xxxx	Read data
0010 xxxx	Read status
0100 xxxx	Write data
0101 xxxx	Write data
0110 xxxx	Write control

Read Data

The Read Data command transfers 16 bits of data from the addressed device to the immediate data field of the IDCB.

Read Status

The Read Status command transfers 16 bits of status from the addressed device to the immediate data field of the IDCB.

Write Data

The Write Data command transfers 16 bits of data from the immediate data field of the IDCB to the addressed device.

Write Control

The Write Control command initiates a control action in the addressed device. A word transfer from the immediate data field of the IDCB may or may not accompany a Write Control command.

Interrupt Presentation and Status Words

The I/O devices attached to the customer DPC adapter may be designed as interrupting devices capable of executing commands that initiate operations which continue beyond the execution of the Operate I/O instruction. Processor interrupt is effected by these devices at the termination of the operation specified by the initiating command.

When a device presents an interrupt, it also presents a condition code that at least specifies the general cause of the interrupt, and may present an interrupt status byte that specifies the exact cause of the interrupt.

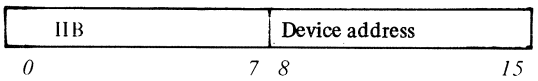
Interrupt Condition Codes

When a device presents an interrupt, it also presents one of the condition codes listed in the table below. Refer to the documentation supplied with the I/O device for information not presented in the following explanations.

Condition Code	*Meaning*
0	*Controller end**—reported by a controller after it has successfully reported condition code 6 (controller busy) to an I/O instruction. Controller end signifies that the controller is free to accept I/O commands for the devices it controls. The device address reported with the controller-end interrupt is the lowest numerical value of the group of devices controlled by that controller domain. The IIB (defined below) will be zero. * The controller is the customer DPC adapter card control logic circuits.
1	*Not reported.*
2	*Exception interrupt*—reported when an error or exception condition is associated with the interrupt. The condition is described in the interrupt-status byte (defined below) and in device-dependent status words, if required.
3	*Device end*—reported when no error, exception, or attention conditions occur during the I/O operation.
4	*Attention*—reported when the interrupt was caused by an external event rather than execution of an I/O command. If the event has a singular meaning, no further status recording is required.
5	*Not reported.*
6	*Attention and exception*—reported when attention and exception conditions occur simultaneously.
7	*Attention and device end*—reported when attention and device-end conditions occur simultaneously.

Interrupt-Information Byte

Each interrupting device presents an interrupt-information byte (IIB) to the processor. The IIB contains status information that cannot be indicated to the program via condition codes. Each IIB is device dependent. For IIB information on specific customer DPC adapter applications, refer to the documentation supplied by the I/O-device designer. The IIB for devices has the following format:



Interrupt-Status Byte

The interrupt-status byte (ISB) is a special format of the IIB and is presented only when interrupt condition codes 2 and 6 are reported. Unless the condition code presentation of 2 or 6 is singular in meaning, the ISB will never be zero.

The ISB is set when status errors which cannot be reported by a condition code occur during a command-initiated operation. After the interrupt request has been taken by the processor, the adapter resets the ISB.

The ISB for devices has the following format:

Bit 0	Device-dependent status available
Bit 1	Delayed command reject
Bits 2–7	Device dependent

Status After Power-On Transitions and Resets

The following table lists the resets for the various resetting conditions.

Condition	*Reset*		
	Diagnostic mode	*Diagnostic register*	*Status register*
Power-on reset	X	X	X
System reset	X	X	X
Halt-I/O command or machine check	X	X	X

Refer to the documentation supplied by the I/O-device designer for reset conditions that apply to each device attached to the adapter.

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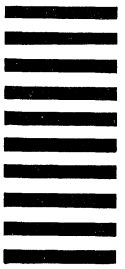

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