MOS INTEGRATED CIRCUITS

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MAPS

microprogrammable arithmetic processor system

general description

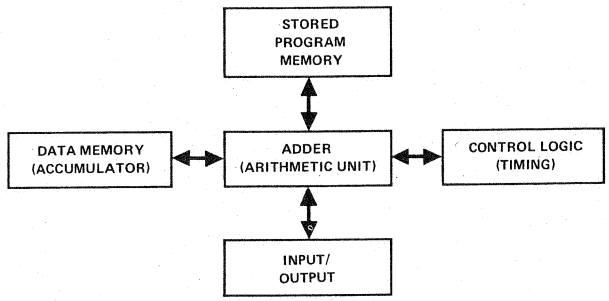
Microprogrammable Arithmetic Processor System devices (MAPS) are MOS/LSI elements that represents a general purpose serial data processor (see Figure 1). The system can be programmed to operate in binary or BCD up to a 76 bit one cycle data word. The system provides a wide variety of data word formating and is applicable to any serial arithmetic control system from machine and process control to business machines.

The basic system is comprised of five MOS/LSI sub-system elements:

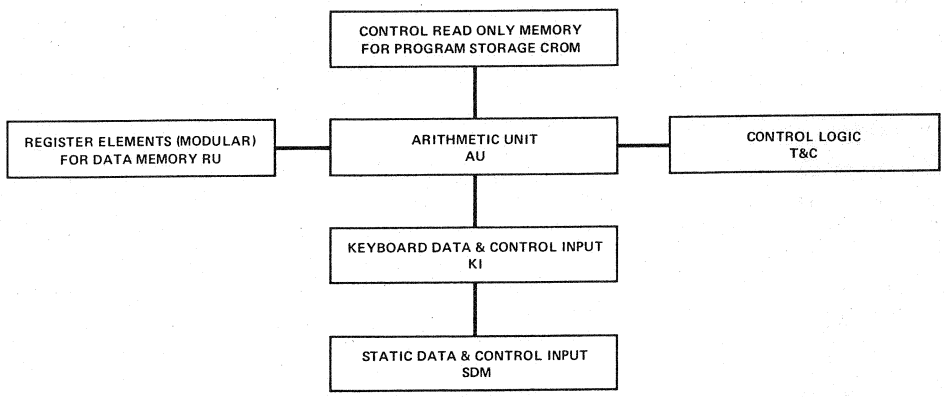
- MM5700 Arithmetic Unit
- MM5701 Register Unit
- MM5702 Timing and Control Unit
- MM5704 Keyboard Interface Unit
- MM5705 Control Read Only Memory

Additional elements for system expansion are:

- MM5703 Control Read Only Memory
- MM5706 Static Data Monitor



1a. General Computer Organization



1b. MAPS Organization

FIGURE 1. General Purpose Computer Organization Compared to MAPS

The five basic elements are interconnected by a serial bit bus-organized distribution system with three data buses, and three command buses (see block diagram Figure 2). The basic cycle of the system is 76 bits, controlled by a set of 32 data micro-instructions stored in the arithmetic and register unit.

packages for easy handling and test. Compatibility with the keyboard, data codes, timing and programs required for the system application is obtained during wafer fabrication by mask programming. A preprogrammed calculator kit with 14-digit display outputs is available for evaluation and general use.

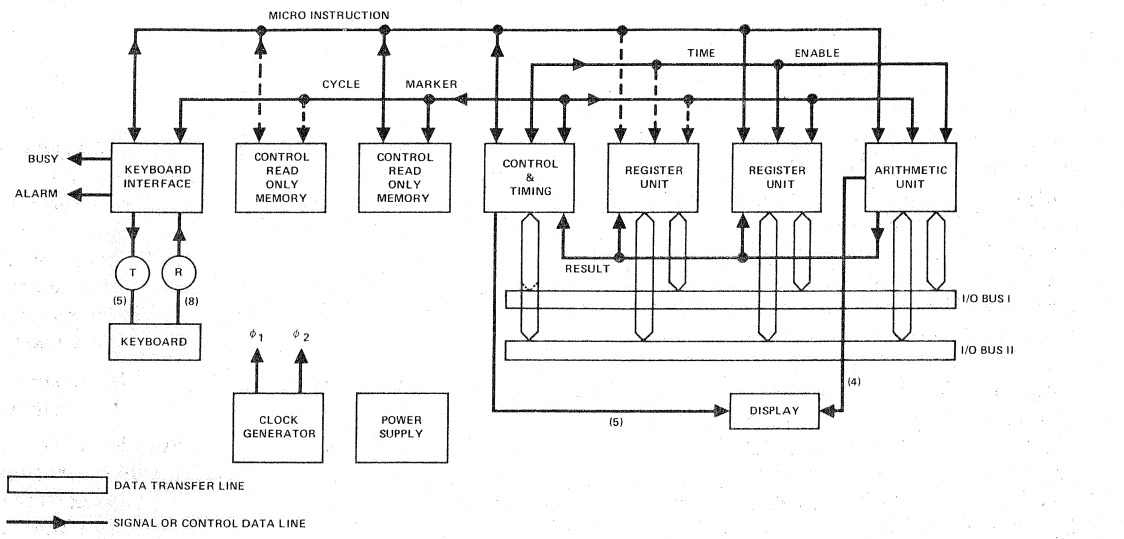


FIGURE 2. MAPS Block Diagram

Data between these elements is passed serial over the three data buses. The logic sequence of data handling is programmed in the CROM element, each CROM provides the system 256 words of a 10-bit command. The T&C element interpolates each command and generates proper time synchronization and time enable signals for performing the command, thus allowing the data in the AU and RU elements to be acted upon. To perform data result tests and control operations, 32 command microinstructions are stored in the T&C element. The format and function performed by each command instruction is programmable by storing the proper bit pattern for the op-code in CROM storage. This allows the same basic command instruction to be programmed differently for a wide variety of machine applications. The keyboard encoder will accept up to 32 dynamic keys and 8 static switch inputs and the static data monitor will scan two banks of 8 data points.

The specific system configuration is expandable since additional RU, CROM, KI and SDM elements can be added on the data and command bus system. The system will accommodate up to 32 CROMs or a total of 8192 microprogrammed instructions. Access from microprogrammed instructions in RAM and mass storage can be performed and controlled. This allows the MAPS elements to function as mini-processors within a larger system.

The system is dynamic two phase logic fabricated with National's bipolar compatible, P-channel enhancement mode, low threshold technology. All elements are in small 16 and 24 pin dual-in-line

features

- Bus-organized for easy expansion and interface with external systems
- Keyboard input
- Static data monitor binary or BCD input
- Error-free keyboard decoding (see MM5704AA data sheet)
- Data and display control outputs
- Clock rates to 750 kHz two phase logic
- DTL/TTL compatible on output for display
- Standard +5V and −12V supplies
- Standard 16-pin and 24-pin DIPs

applications

- General purpose serial computers
- "Smart" data terminals
- Numerical controls
- Electronic business machines
- Point of sales equipment
- Electronic scales
- Electronic calculators
- Traffic controls
- Medical electronics (analyzers, patient monitoring, etc.)

Pin	Arithmetic Unit (AU) MM5700	Register Unit (RU) MM5701	Timing & Control (T&C) MM5702	Control ROM (CROM) MM5703	Keyboard Interface Chip (KI) MM5704
1		RES	μI		$\overline{\text{AL OUT}}$
2	ϕ2		$\overline{\text{CM}}$		CS
3	RES	IO2	$\overline{\text{TE}}$	ϕ2	R7
4	IO2			μI	R6
5	IO1	IO1		$\overline{\text{CM}}$	R5
6	μI	ϕ1		ϕ1	R4
7	ϕ1		P1		R3
8	V_{SS}	V_{SS}	P2	V_{SS}	R2
9	$\overline{\text{CM}}$	ϕ2	ϕ1		Idle Key Reset
10	$\overline{\text{TE}}$	$\overline{\text{TE}}$			R1
11	$\overline{\text{PO2}}$		ϕ2		R0
12	$\overline{\text{PO1}}$	$\overline{\text{CM}}$	V_{SS}		V_{SS}
13	$\overline{\text{PO8}}$		FFO		ϕ1
14	$\overline{\text{PO4}}$		RES		ϕ2
15		μI			$\overline{\text{CM}}$
16	V_{GG}	V_{GG}		V_{GG}	T4
17			IO		T1
18					T2
19			DS		T3
20			B+9		T5
21					μI
22					$\overline{\text{BUS1}}$
23			A		$\overline{\text{BUS2}}$
24			V_{GG}		V_{GG}

FIGURE 1. MAPS Pin Assignments

WHAT IT DOES

In addition to the 32 character key switch closures that may be encoded, there are 8 static switches that may be interrogated. These static switches may be controlled by the user to form an 8-bit word which upon command will be sent via the keyboard interface output to the rest of the system. These switch closures are used to perform control functions. They may be used to form any desired data word especially if it is to be varied from time to time.

The output of this device is presented at Pin 21 in a bit serial fashion. This organization was required to be compatible with the bus structured organization of the five chip MAPS. The bit serial, digit serial, organization of this system was designed to keep to a minimum the number of pins required for each MOS-LSI chip used in this system. Actually, Pin 21 is a bidirectional bus, with input capability for controlling static switch interrogation, data interrogation, or control of the alarm and shift functions. In a system this is accomplished with time multiplexing. (Figure 5)

If a system contains more than 32 character key closures, the functions performed by the MM5704 may be expanded by paralleling two or more of these devices. Two devices will provide 64 key closures (128 data words), three provide 96, etc. The two key rollover and three key alarm functions will continue to function by paralleling the busy 1 (Pin 22) and busy 2 (Pin 23) signal lines. The alarm signal will be available at Pin 1 of the devices. This signal is not OR-tieable.

TWO KEY ROLLOVER

If a second key is depressed before the first key is released, a condition exists that is defined as two key rollover. In this situation, the device will acknowledge and transmit the encoded word generated by the initial key closure then acknowledge and transmit the encoded data word generated by the second key closure. At the time that the system responds to the initial key closure, the "busy 1" signal line becomes true (MOS logic "1" condition). This informs any parallel keyboard interface chips that a key closure has been detected. The "busy 1" signal will remain true until the encoded data word resulting from initial key closure has been transmitted and the key released.

If during the time that the "busy 1" signal is true and a second key closure is detected, the system will flag this condition by causing "busy 2" to go true. "Busy 2" will remain true until the encoded data word generated by the initial key closure has been transmitted and one key released. "Busy 1" will remain true until all keys are released. A key once depressed and acknowledged by the system must be released and depressed again before it will be accepted and acknowledged as valid by the system for the second time.

THREE KEY ALARM

If three or more keys are depressed, a condition exists that will be detected by the system and interpreted as the alarm condition. Because the KI chip cannot process more than two key closures, depression of more than two must alarm the system. When the alarm condition exists, a

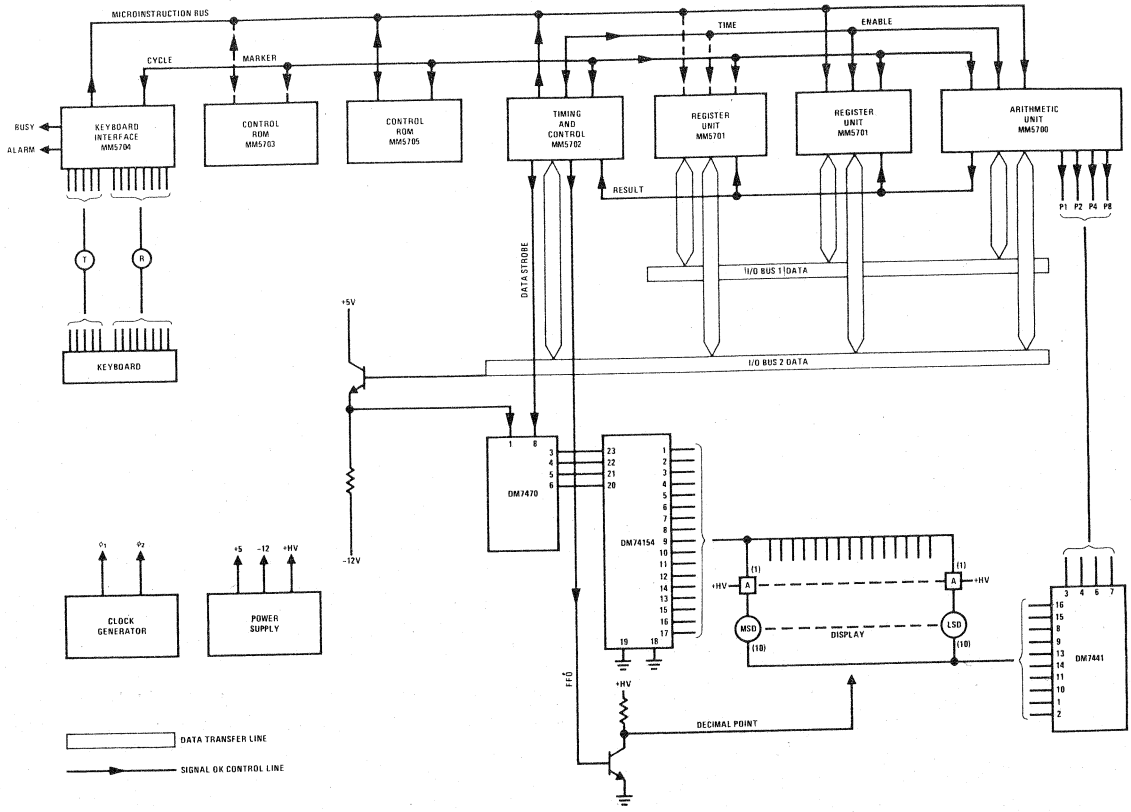


FIGURE 6. MAPS Block Diagram

four keyboard interface chips and associated static switches in parallel. The device user may specify which time slot will be used with a given device. This is especially important when two or more of these devices are to be used in a system. If this is left unspecified in a single keyboard interface chip system, this will generally be programmed to the Xmit static 1 time slot. It is an illegal condition for both a static transmit and key code transmit request to occur in the same word cycle.

THE KEYBOARD INTERFACE AS USED IN MAPS

The natural environment for this device is to operate in conjunction with the "timing and control" (T&C) chip (MM5702) of MAPS. MAPS (Microprogrammable Arithmetic Processing System) is a five MOS-LSI chip, mini-processor system. The block diagram shown in Figure 6 illustrates the system's primary components and their interconnections. Besides the clock lines and power supplies, the keyboard interface chip has a cycle marker (CM) input from the MAPS system. This signal (CM) is generated in the T & C chip from a master timing clock and is used to synchronize the entire system including the KI. This procedure is mandatory in a system, such as this, where all data as well as command and operation signals are transmitted in a serial by bit and serial by digit basis. The exchange of all information between the system blocks is time multiplexed onto single wire buses; therefore, all of the system components must be in step. The cycle marker flags the beginning of a 76 bit word cycle time. The important bit times for the KI chip in MAPS are, for example, 11 through 30. These are the bit times in any given word cycle that are allotted for the KI to communicate with the rest of the system through the T & C chip. The detailed nature of this time period is more completely defined and illustrated in Figure 5.

The various time slots are logically defined and implemented within the KI chip as follows: The CM initiates a delay line composed of a series of MOS inverters. The outputs of these inverters become true in a sequential fashion, one after another in step with each clock transition. Therefore, once the sequence is initiated at the proper time (CM) the MOS delay line will behave as a special decoded counter in step with the master counter in the T & C chip. The output of each stage will define a precise bit time with respect to the CM. This occurs within the housekeeping block (Figure 2). When the KI has acknowledged a key closure it will send out a character ready signal (bit time 20), and continue to send it until it is acknowledged by the T & C chip. The T & C chip will receive this and, in some subsequent word cycle at bit time 12, will send a transmit key