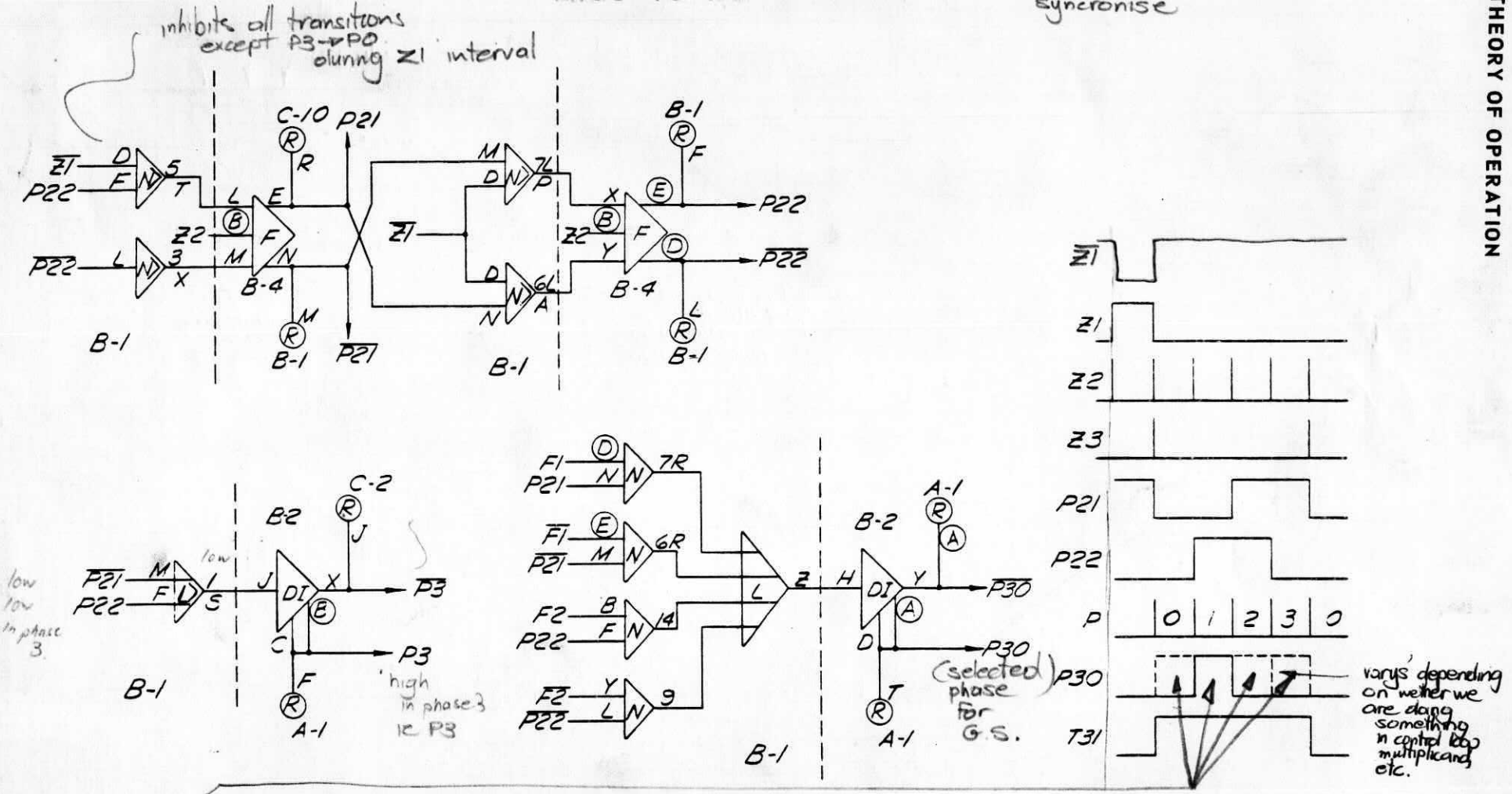
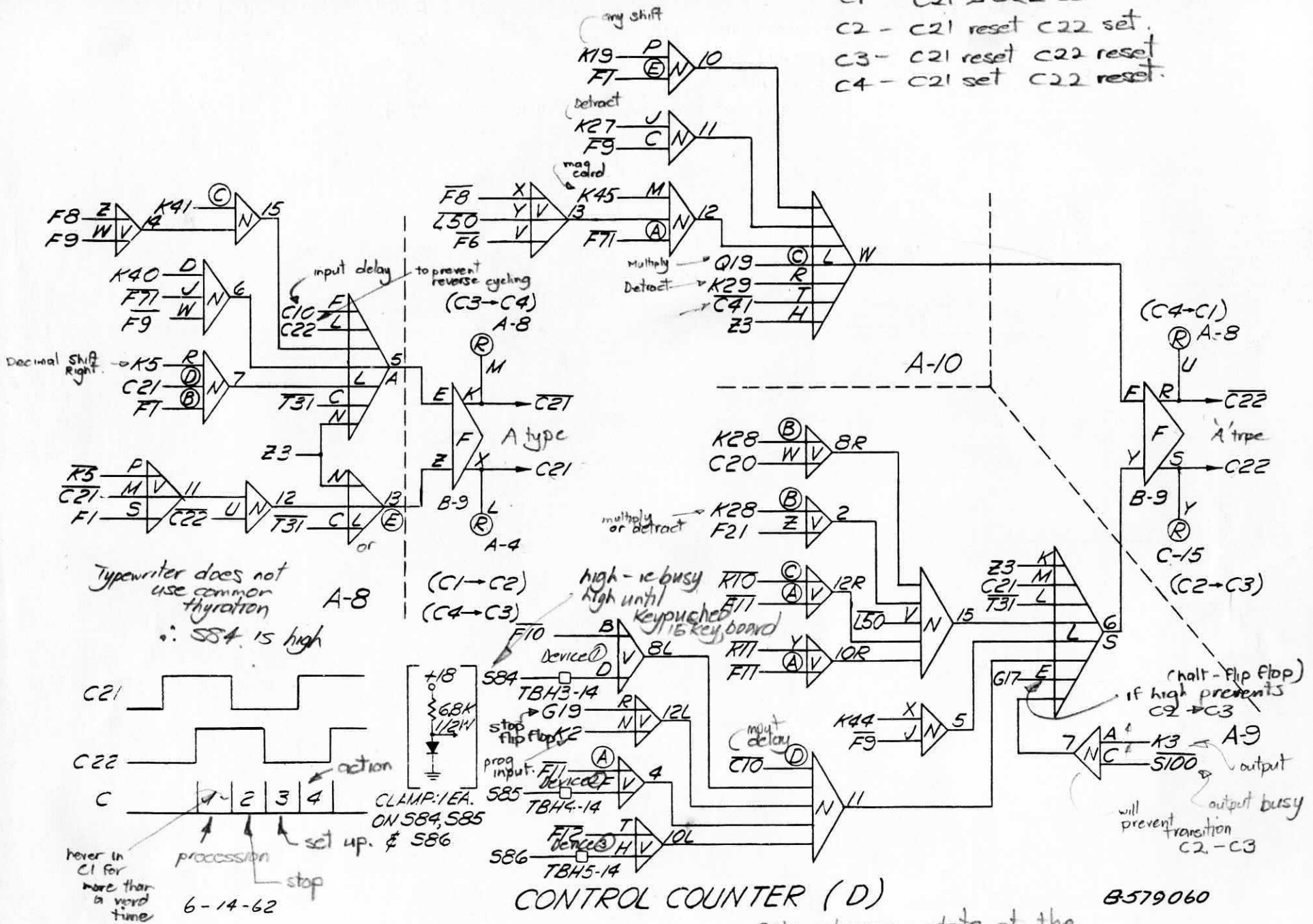
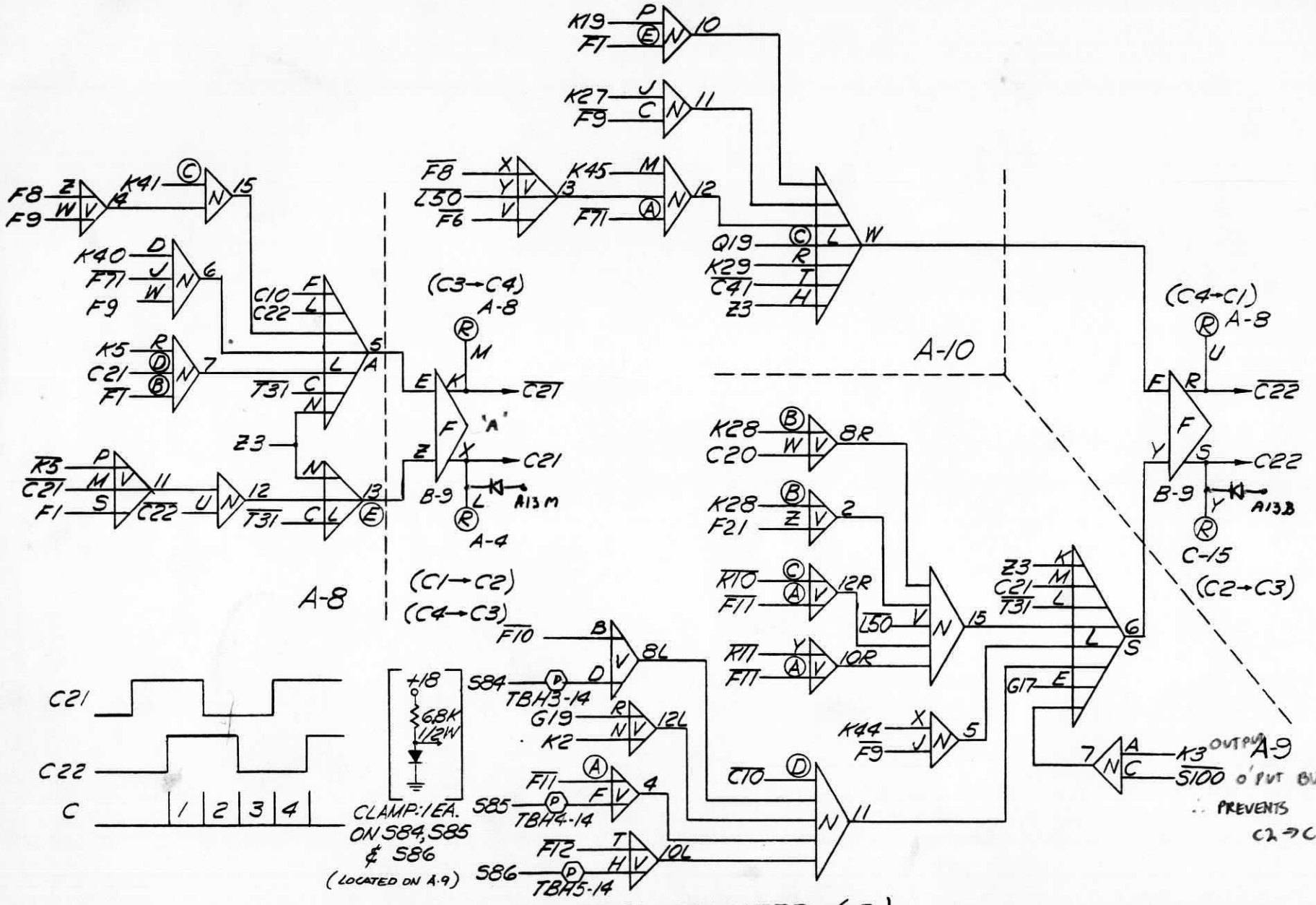
Takes no more than 8 Z1 pulses to syncronise




C1 – C21 & C22 set
C2 – C21 reset C22 set.
C3 – C21 reset C22 reset
C4 – C21 set C22 reset.
any shift
K19
F7
detract
K27
F9
mag card
K45
F8
L50
F6
F71
Multiply
Detract
Q19
K29
C41
Z3
A-10
input delay
to prevent reverse cycling
(C3→C4)
A-8
C10
C22
K40
F71
F9
Decimal Shift Right
K5
C21
F1
T31
A type
C21
B-9
A-4
(C4→C1)
A-8
C22
C-15
(C2→C3)
K28
C20
8R
K28
F21
multiply or detract
2
K10
E11
12R
K11
F11
10R
L50
Z3
C21
T31
G17
(halt - Flip flop)
If high prevents C2→C3
A-9
K44
F9
K3
S100
output
output busy
will prevent transition C2→C3
Typewriter does not use common thyration
∴ S84 is high
A-8
(C1→C2)
(C4→C3)
high - ic busy high until keypushed 16 key board
F10
S84
TBH3-14
Device 1
8L
G19
stop flip flop K2
12L
prog input
F11
S85
TBH4-14
Device 2
4
F12
S86
TBH5-14
Device 3
10L
C10
mpt delay
11
+18
68K 1/2W
CLAMP: 1 EA. ON S84, S85
C21
C22
C
1
2
3
4
action
set up. ¢ S86
processing
stop
never in C1 for more than a word time
6-14-62
CONTROL COUNTER (D)
B-579060
only change state at the end of a word time ie note T31
S84 - Input busy device 1
S85 " " " 2
S86 " " " 3



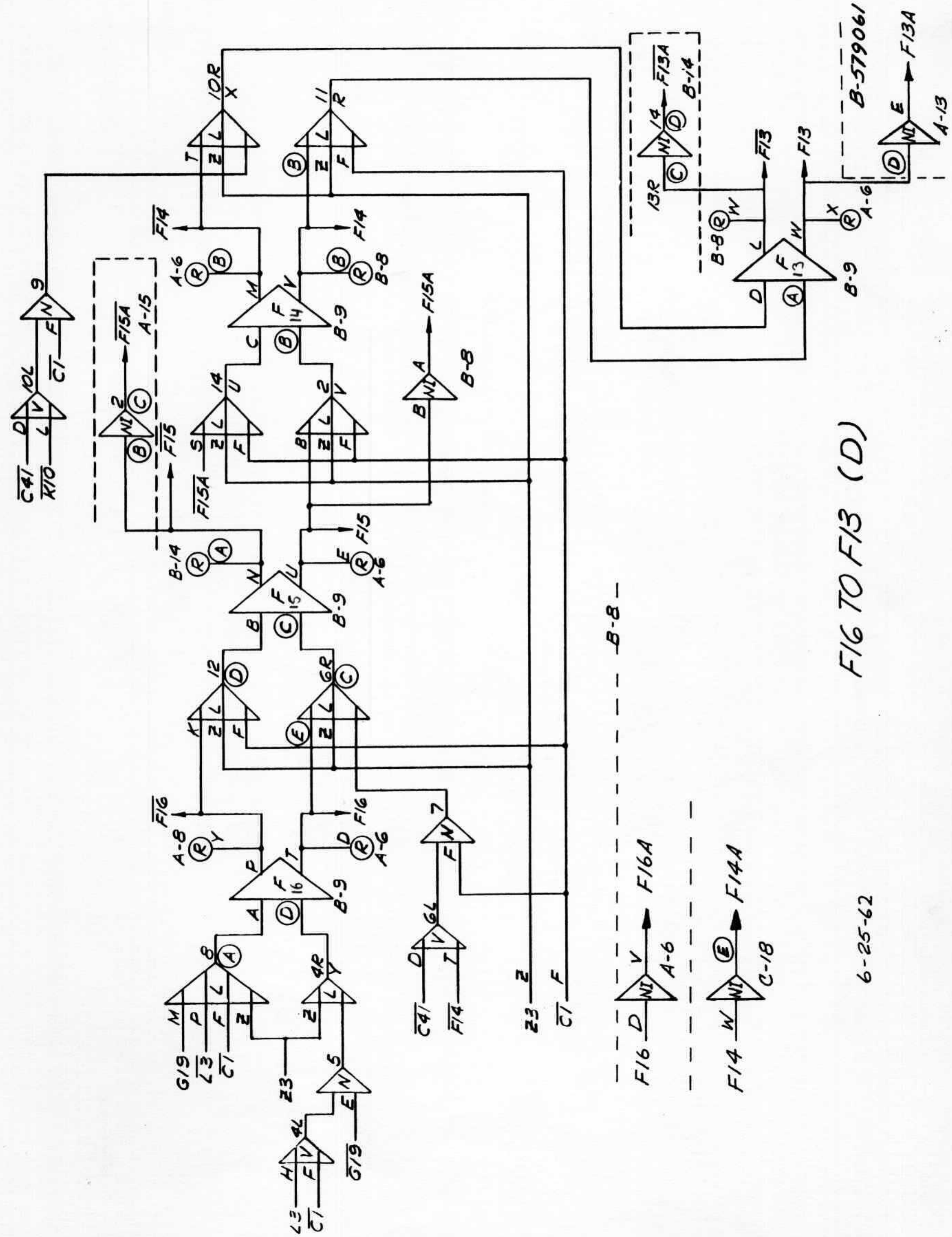
8-31-64

CONTROL COUNTER (D)

(WITH IMPROVEMENT NOTICE #16)

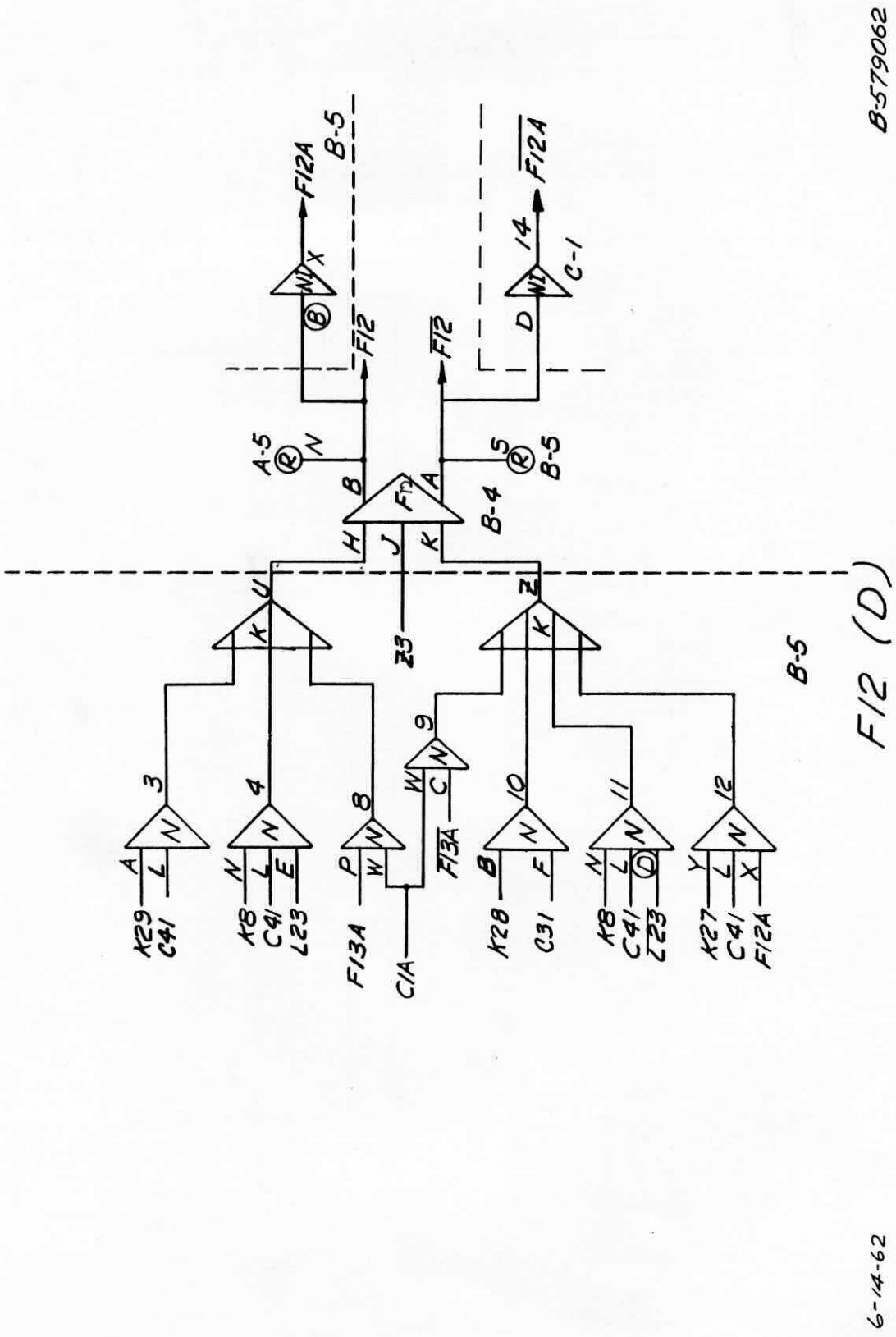
B-579060-B

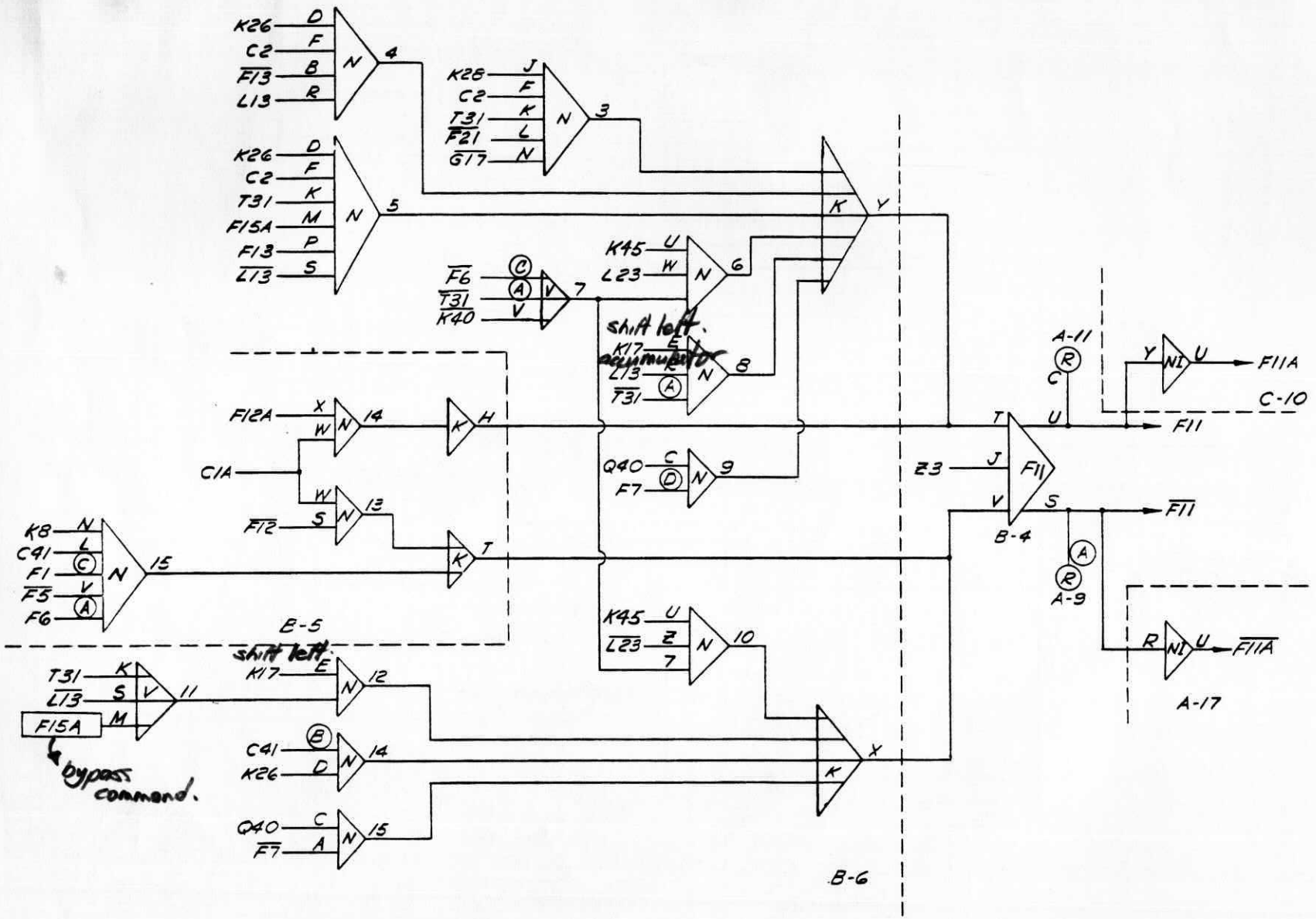
A F/F -VE
B F/F +VE



F16 TO F13 (D)

6-25-62

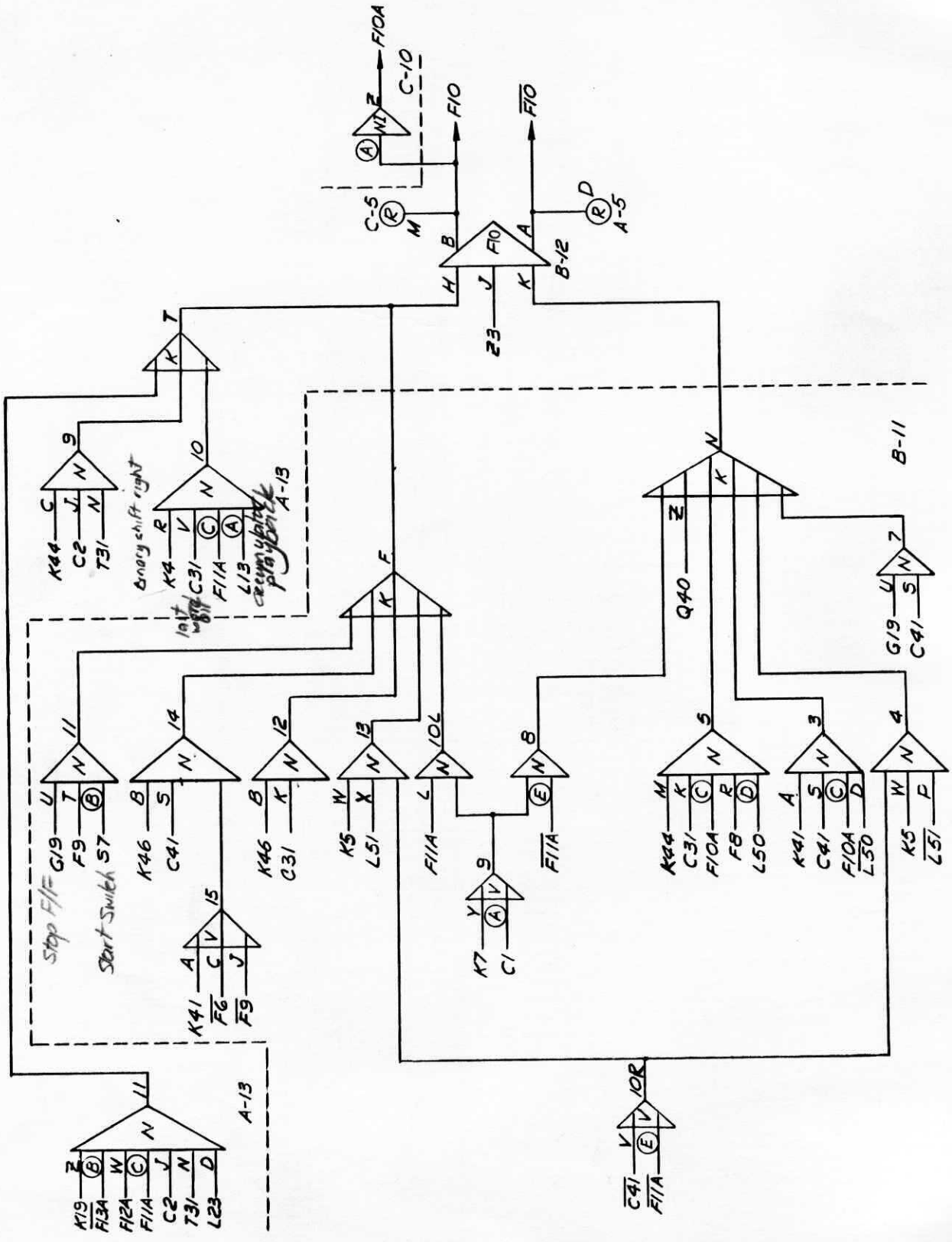

B-579062
F12A
B-5
F12
A-5
N
B
A
B-4
5
B-5
F12
F12A
14
C-1
D
X
H
J
K
U
Z
23
B-5
3
4
8
9
10
11
12
A
L
K29
C41
N
L
E
K8
C41
L23
P
W
F13A
C1A
W
C
F13A
B
F
K28
C31
N
L
D
K8
C41
L23
Y
L
X
K27
C41
F12A
F12 (D)
6-14-62

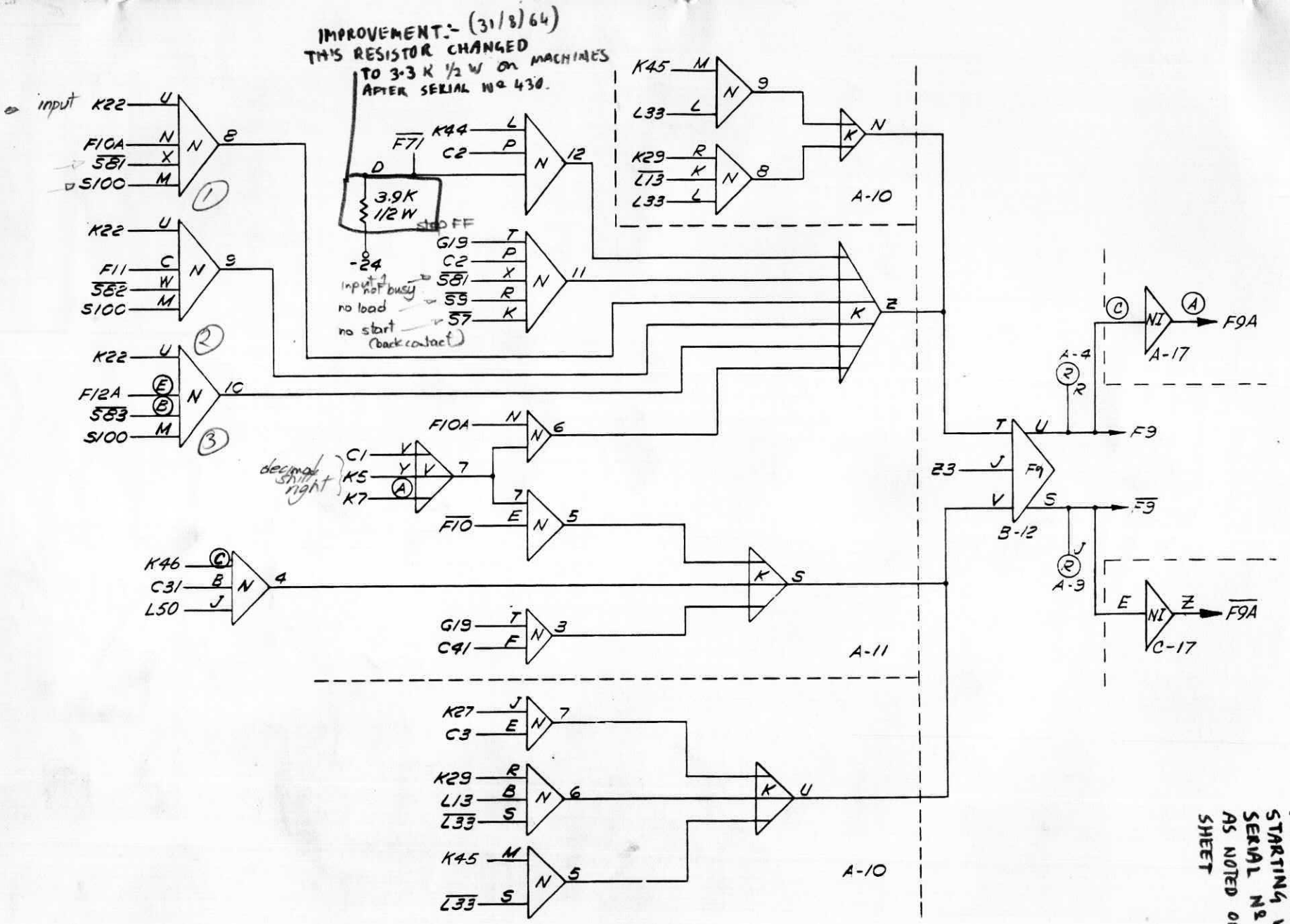


6-14-62

F11 (D)

B-579063


F10A
C-10
F10
C-5
M
B
F10
A
B-12
D
A-5
H
J
K
23
T
K
9
N
K44
C2
T31
10
N
R
K4
V
C31
C
F11A
A
L13
A-13
Energy shift right
last wire
Stop F/F
Start Switch S7
G19
F9
B
11
N
U
T
K46
C41
B
S
14
N
15
V
A
K41
F6
F9
C
J
K46
C31
B
K
12
N
F
K
K5
L51
W
X
13
N
F11A
L
10L
N
9
V
A
K7
C1
Y
8
N
E
F11A
Q40
Z
N
K
B-11
K44
C31
F10A
F8
L50
M
K
C
R
D
5
N
K41
C41
F10A
L50
A
S
C
D
3
N
K5
L51
W
P
4
N
G19
C41
U
S
7
N
K19
F13A
F12A
F11A
C2
T31
L23
Z
B
W
C
J
N
D
11
N
A-13
C41
F11A
V
E
10R
V
8-579064
F10 (D)
6-14-62

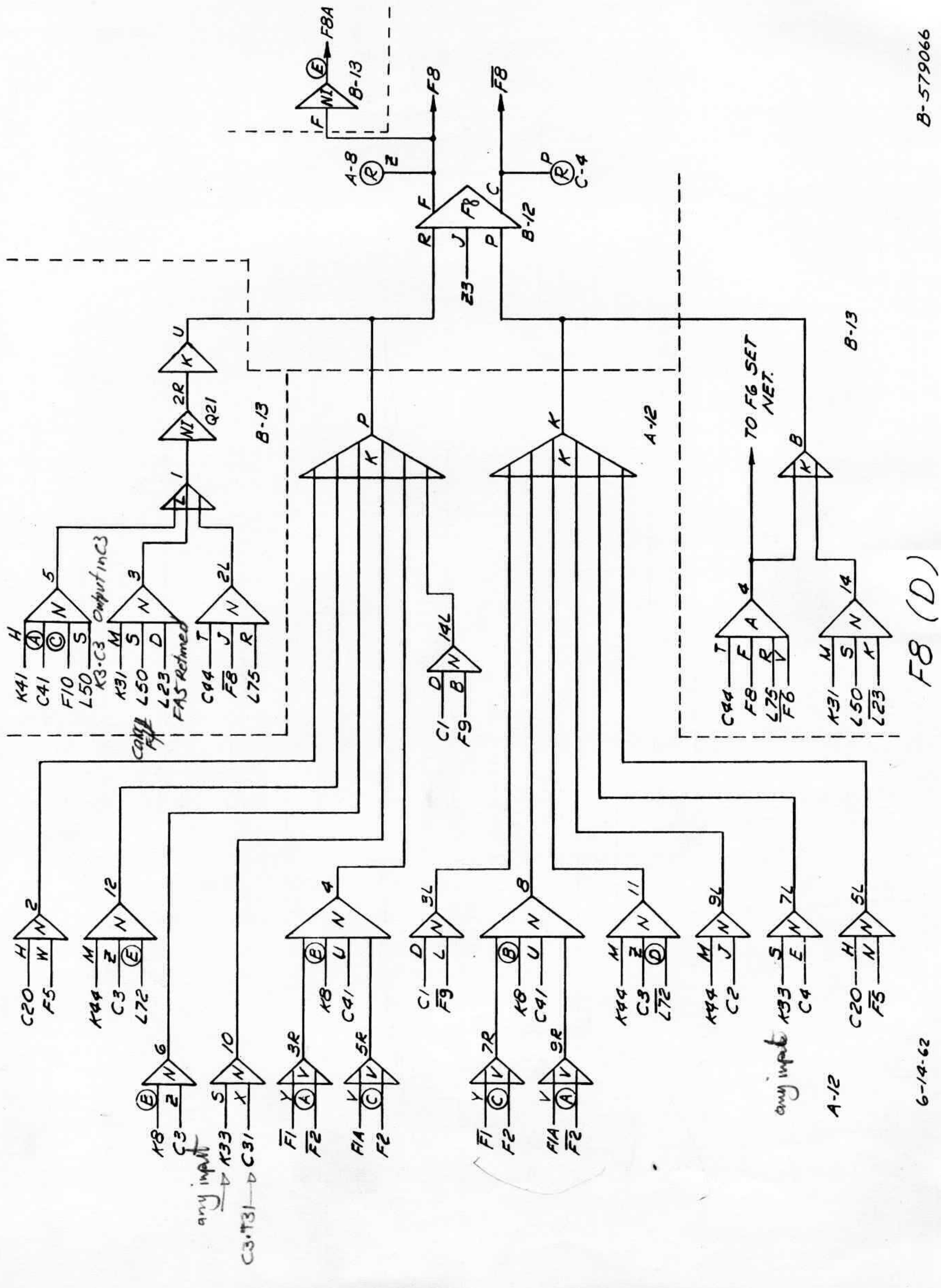


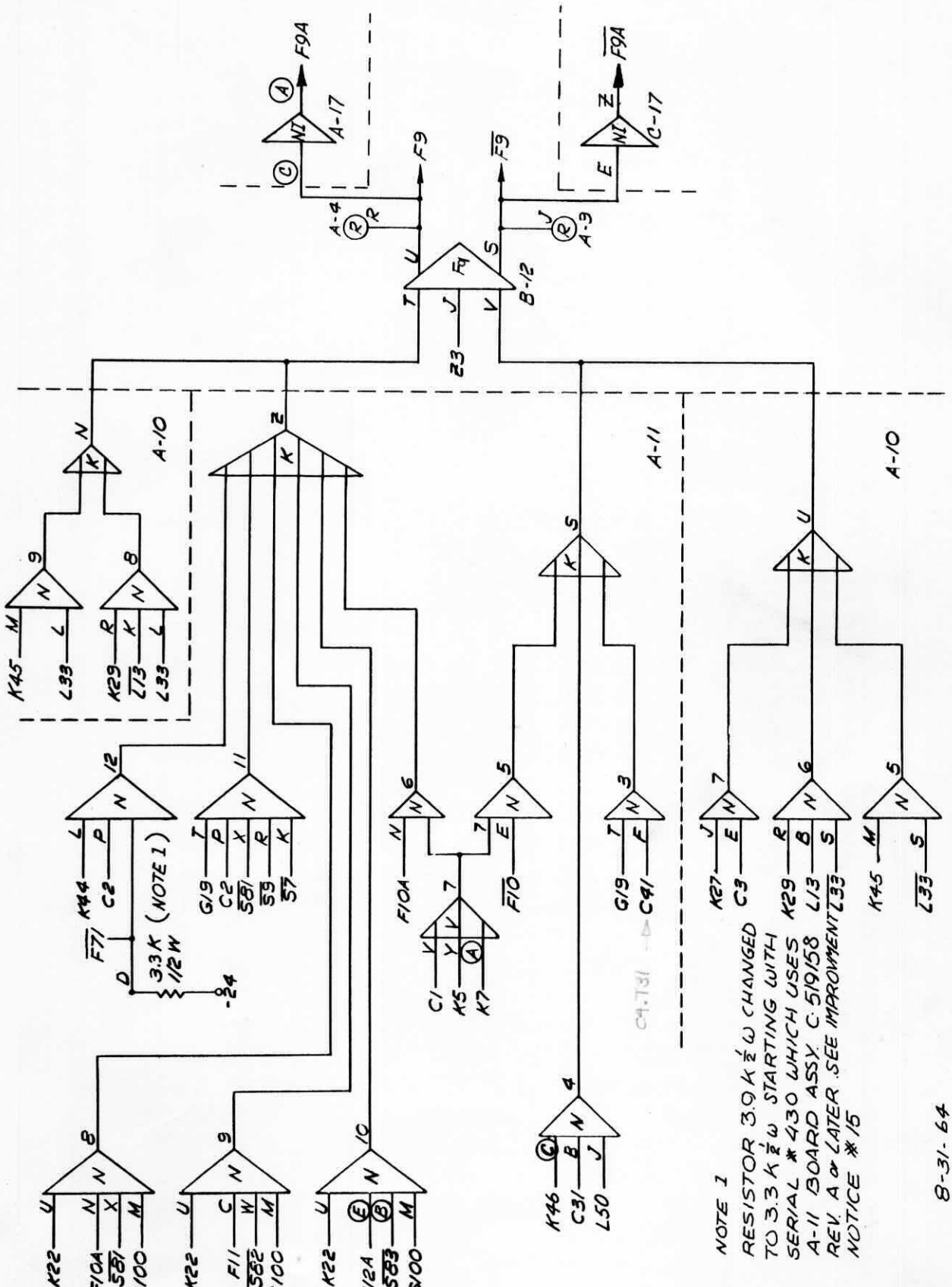
6-14-62

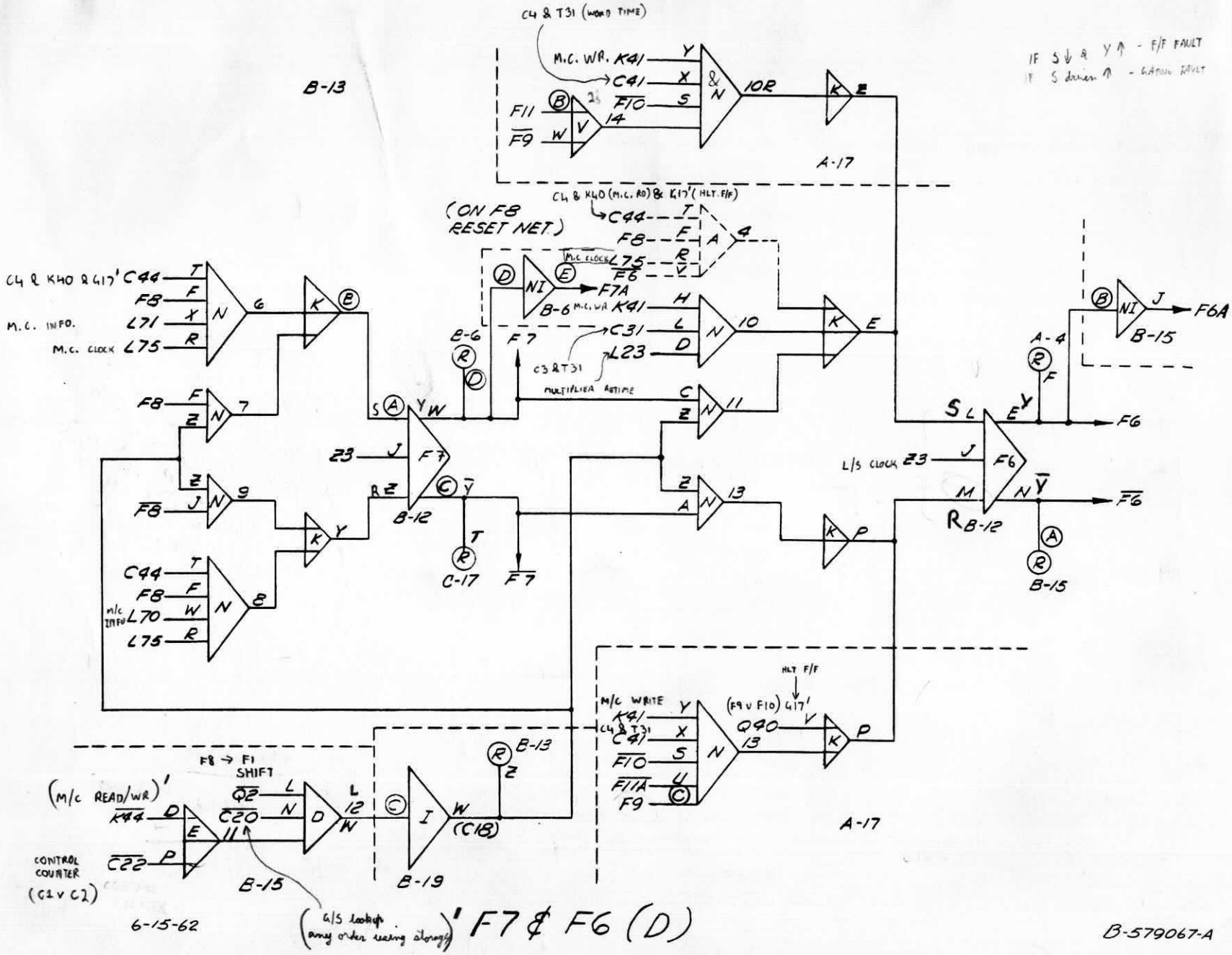
F9 (D)

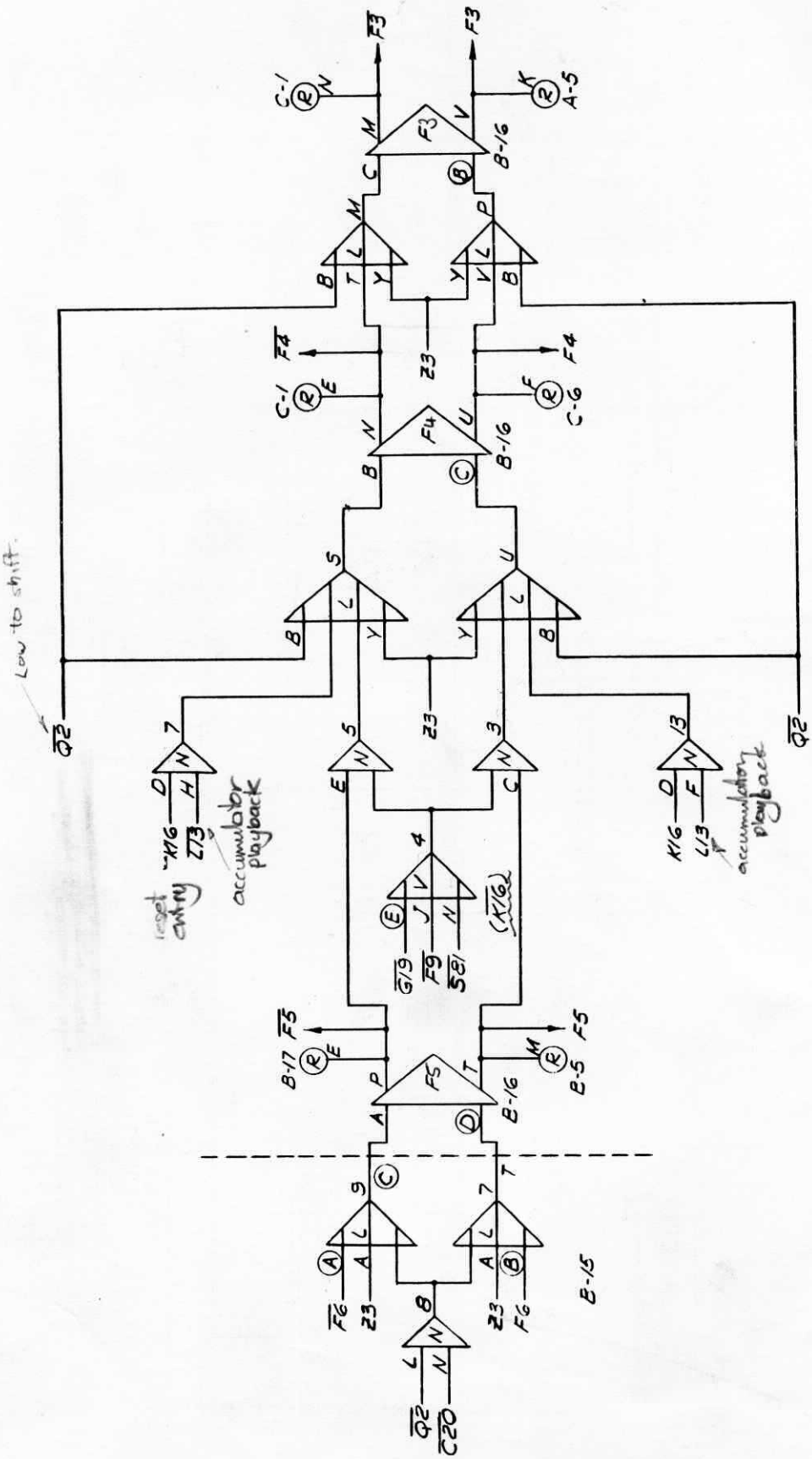
B-579065-A

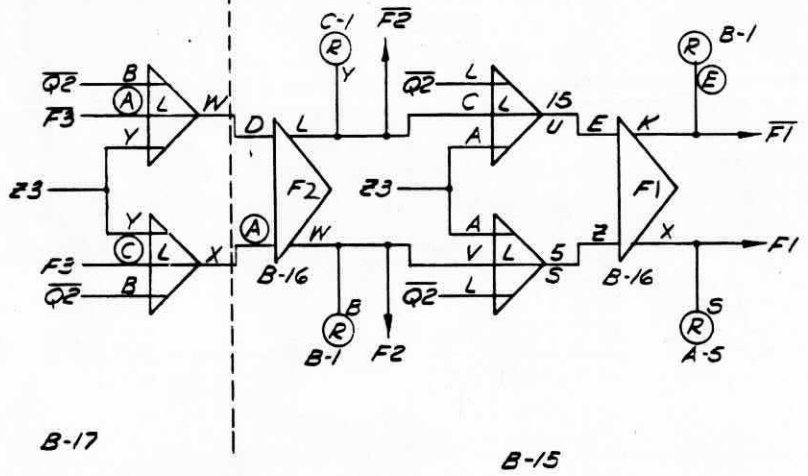
3-121
SEE P 121A FOR ALTERATIONS STARTING WITH SERIAL No 430 AS NOTED ON THIS SHEET


F8 (D)
B-579066
6-14-62
TO F6 SET NET.


F9A
A-17
F9
F9
F9A
C-17
A-4
A-9
B-12
A-10
A-11
A-10
K45 M
L33 L
K29 R
L13 K
L33 L
K44 L
C2 P
F7I
3.3K (NOTE 1)
1/2 W
-24
G/9 T
C2 P
SB1 X
S9 R
S7 K
F10A N
C1 Y
K5 Y
K7 Y
F10 E
G/9 T
C41 F
K27 J
C3 E
K29 R
L13 B
L33 S
K45 M
L33 S
K22 U
F10A N
SB1 X
S100 M
K22 U
F11 C
SB2 W
S100 M
K22 U
F12A E
SB3 B
S100 M
K46 B
C31 J
L50
C41 T
NOTE 1
RESISTOR 3.9 KΩ CHANGED TO 3.3 KΩ STARTING WITH SERIAL # 430 WHICH USES A-11 BOARD ASSY. C: 519158 REV. A or LATER. SEE IMPROVEMENT NOTICE #15
8-31-64
F9 (D)
B-579065-B


C4 & T31 (WORD TIME)
M.C. WR. K41
C41
F10
F11
F9
10R
A-17
B-13
IF S ↓ & Y ↑ - F/F FAULT
IF S down ↑ - GATING FAULT
K41 MC CD WR
C4 & K40 (M.C. RD) & K17' (HLT. F/F)
(ON F8 RESET NET.)
C44
F8
L75
F6
F7A
B-6
M.C. WR K41
C31
L23
C3 & T31
MULTIPLIER ARTIME
F7
B-6
C4 & K40 & K17' C44
M.C. INFO. L71
M.C. CLOCK L75
F8
23
B-12
C-17
F7
C44
F8
m/c INFO L70
L75
L/S CLOCK 23
F6
A-4
B-15
F6A
F6
R B-12
B-15
M/C WRITE K41
C41
F10
F11A
F9
(F9 v F10) K17'
Q90
13
HLT F/F
A-17
F8 → F1 SHIFT
(M/C READ/WR)'
K44
C20
Q2
C22
CONTROL COUNTER (C1 v C2)
B-15
B-19
(C18)
B-13
6-15-62
(L/S lookup any order using storage)
F7 & F6 (D)
B-579067-A


F5 TO F3 "X/4 D"
579,009-A
6-1-60
Low to shift.
accumulator playback
accumulation playback
F8 + F1 shift.
B-17
B-15
B-16
B-5
A-5
C-1
C-6

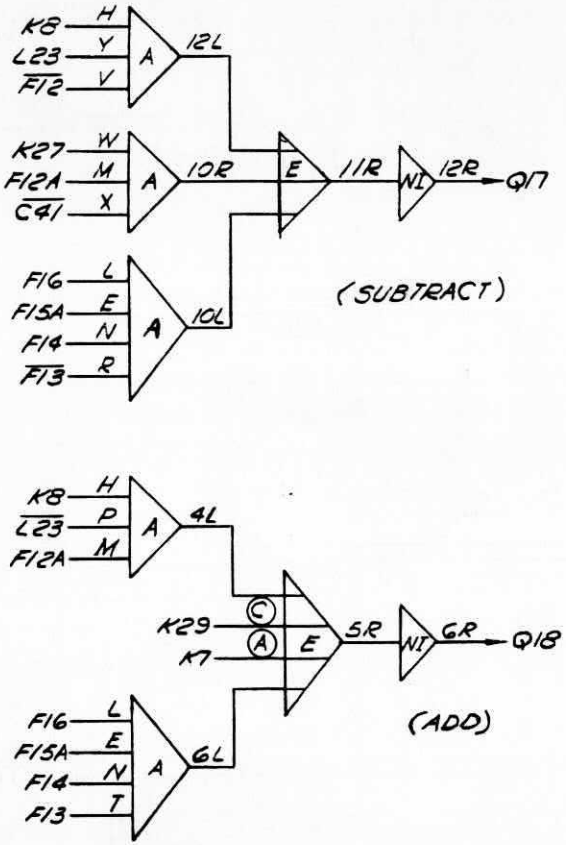


B-17

B-15

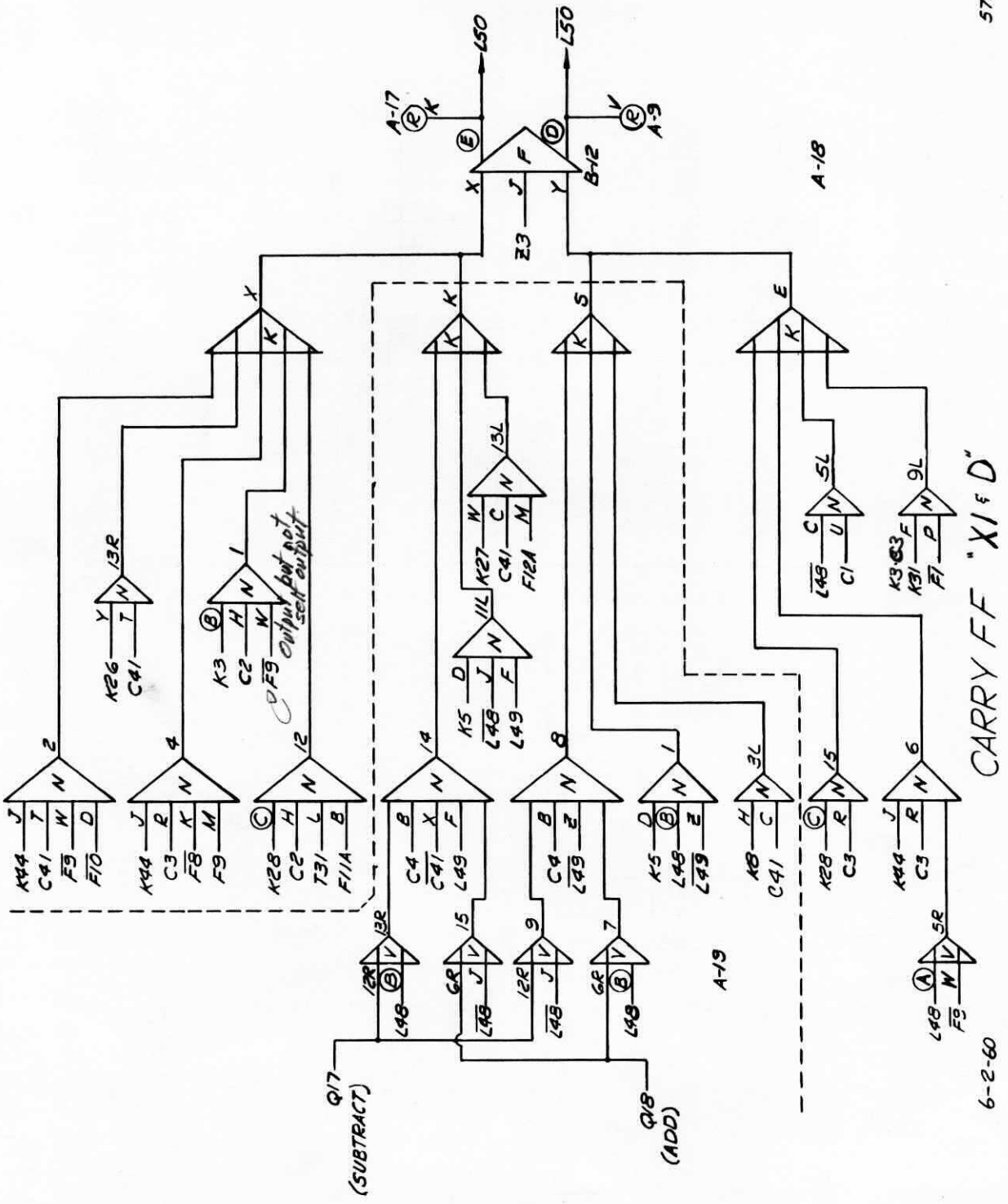
F2 & F1

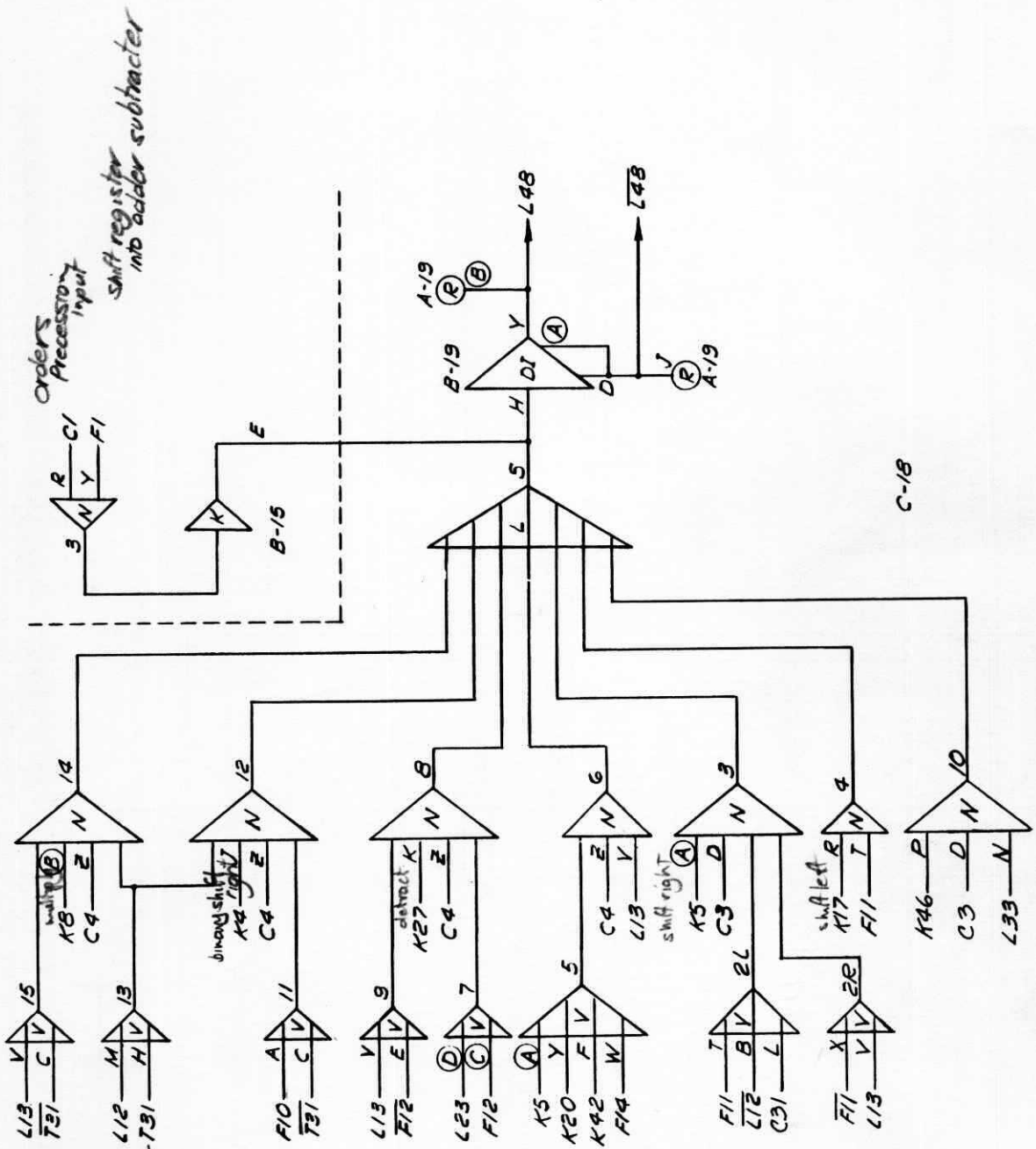
6-2-60

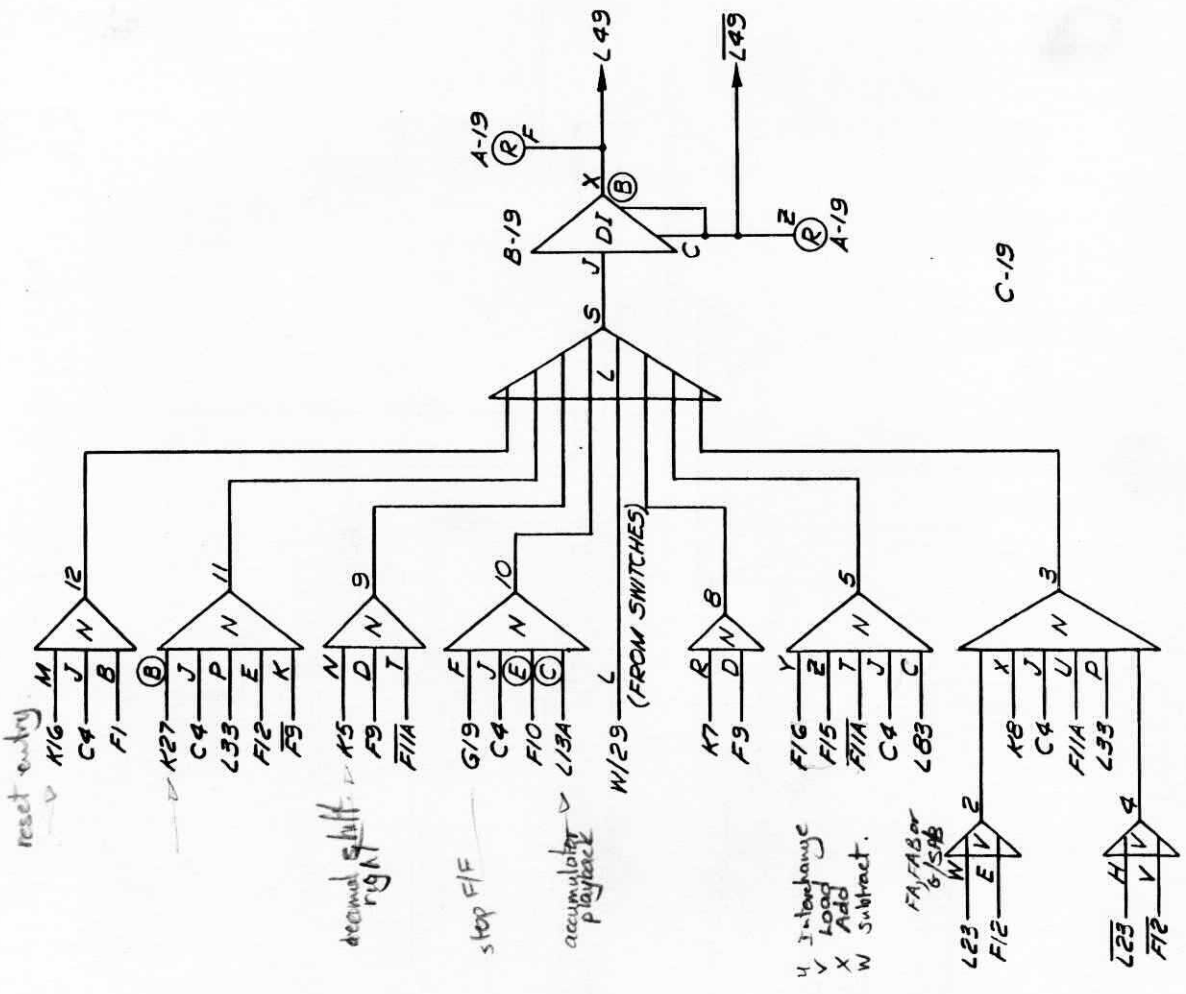


A-19

"X1 & D" ADD-SUBTRACT GATES 579,010-A


579,011-A
CARRY FF "XI & D"
6-2-60
A-17
A-18
A-19
B-12
L50
L50
Z3
Q17
(SUBTRACT)
Q18
(ADD)
Output pulse not sent out first

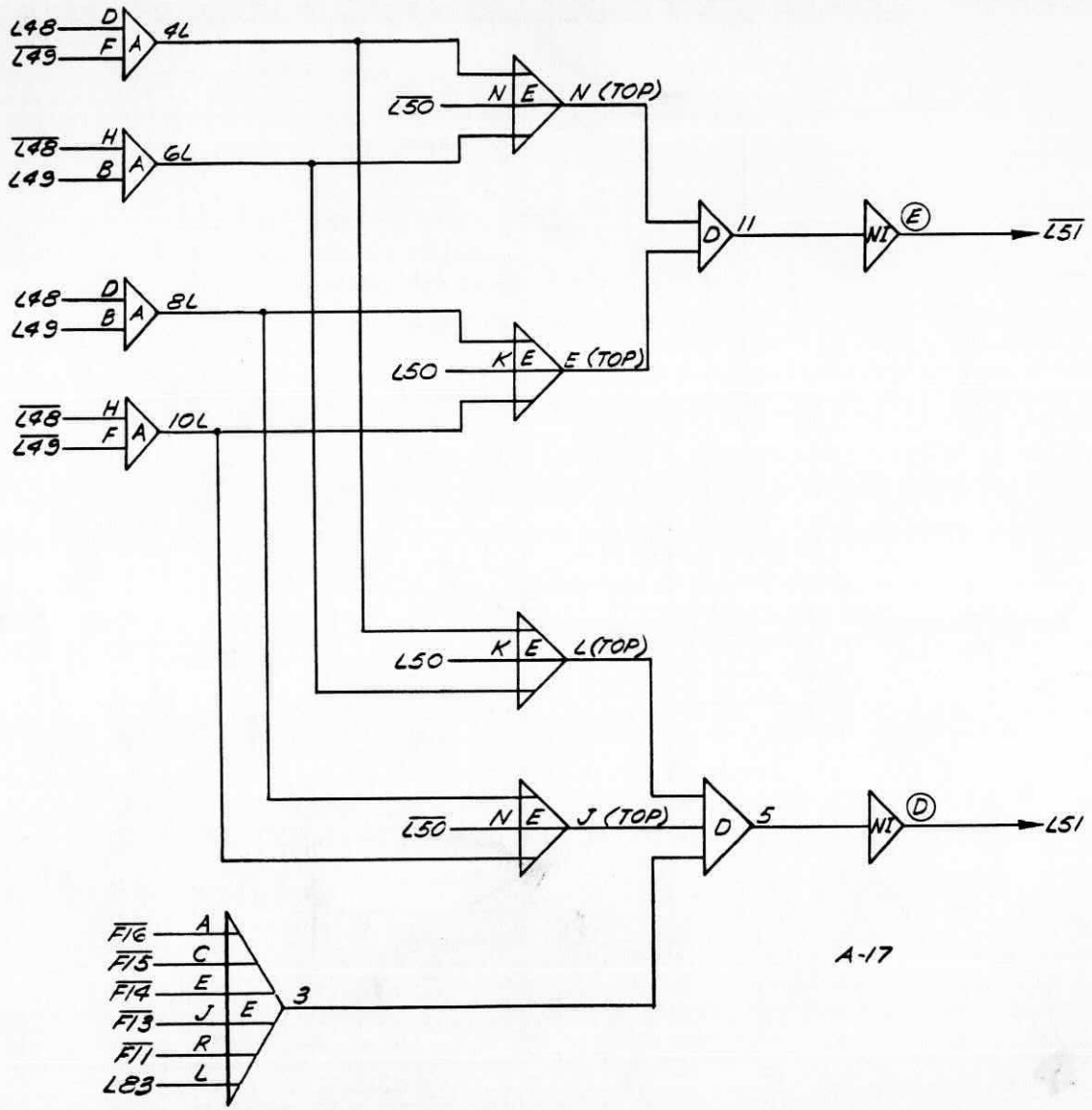

orders Processor input
shift register into adder subtracter
A GATE (D)
6-19-62
B-579068
C-18
B-15
B-19
A-19
L48
L13 T31
L12 T31
early accum
F10 T31
attach last bit recorded
L13 F12
L23 F12
K5 K20 K42 F14
F11 L12 C31
F11 L13
K46 C3 L33
K8 C4
K4 C4
K27 C4
C4 L13
K5 C3
K17 F11
shift right
shift left
binary shift right
attach K



B GATE "XI+D"

6-3-60

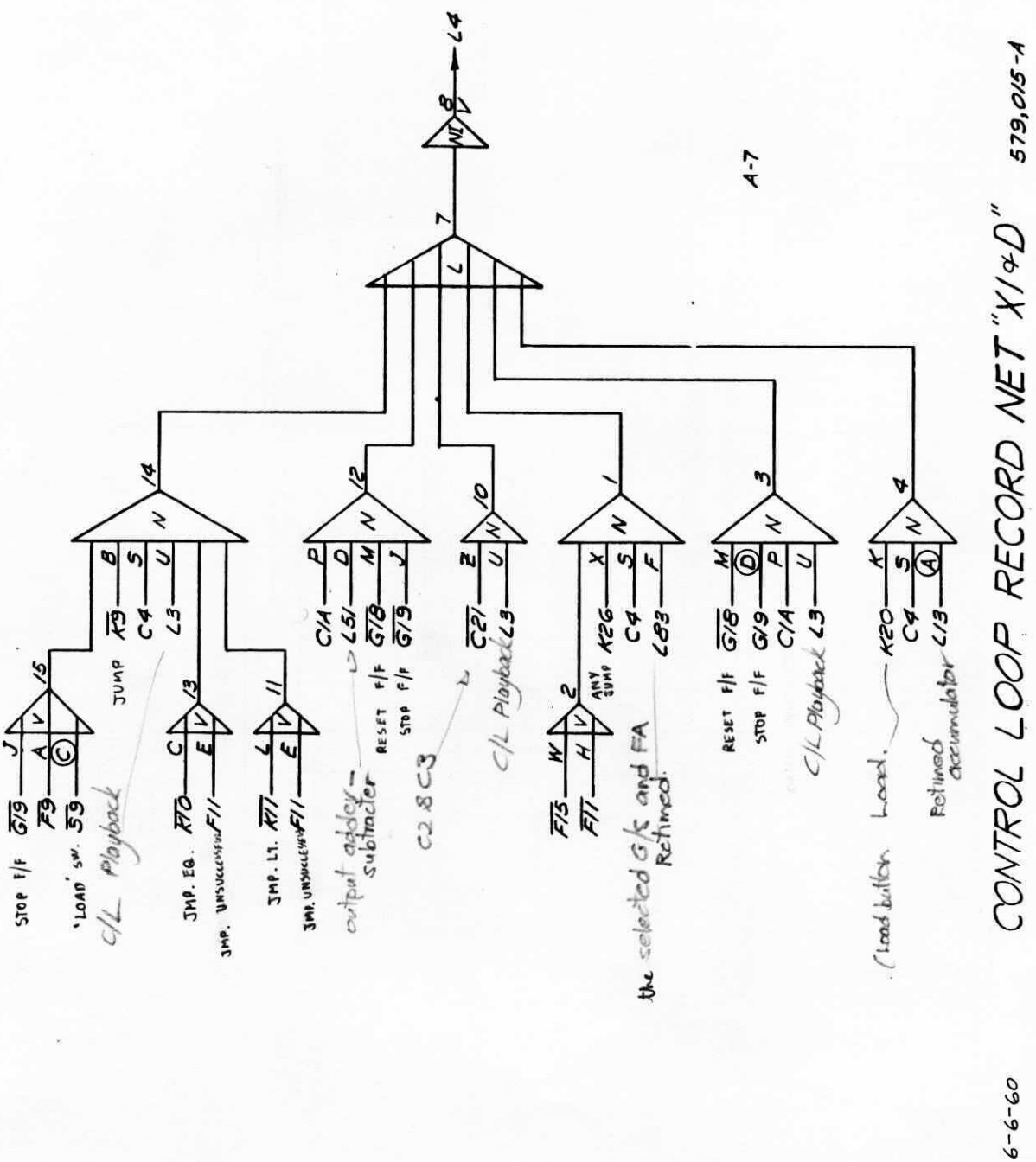
579013-A

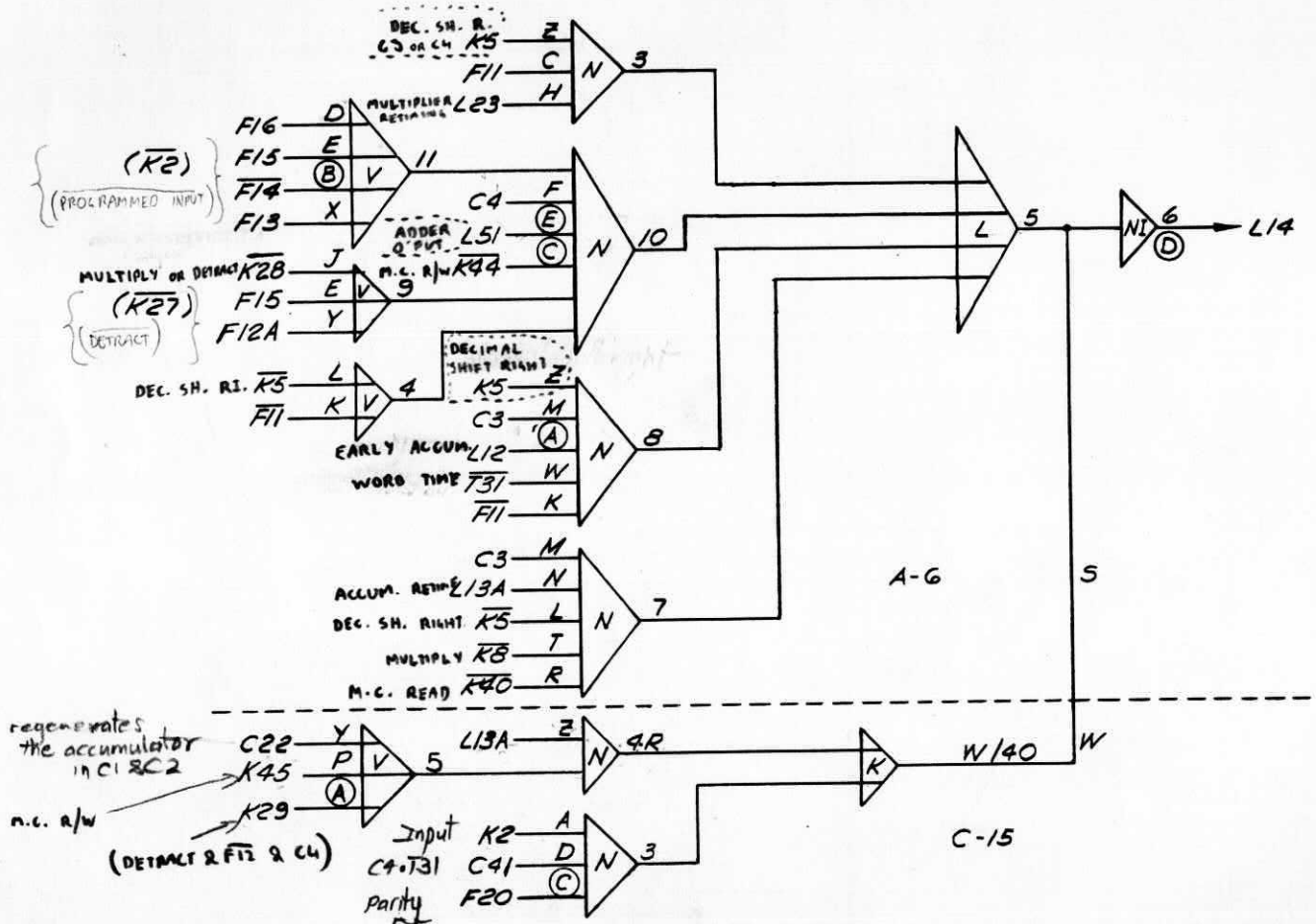


6-6-60

ADDER SUBTRACTER NET "X1+D"

579014-A


CONTROL LOOP RECORD NET "XI & D"
579,015-1
6-6-60
A-7
STOP F/F
'LOAD' SW.
C/L Playback
JUMP
JMP. EQ.
JMP. UNSUCCESSFUL
JMP. LT.
JMP. UNSUCCESSFUL
output adder-subtracter
RESET F/F
STOP F/F
C2 & C3
C/L Playback
the selected G/S and FA Retimed.
ANY JUMP
RESET F/F
STOP F/F
C/L Playback
Load button
Load.
Retimed accumulator

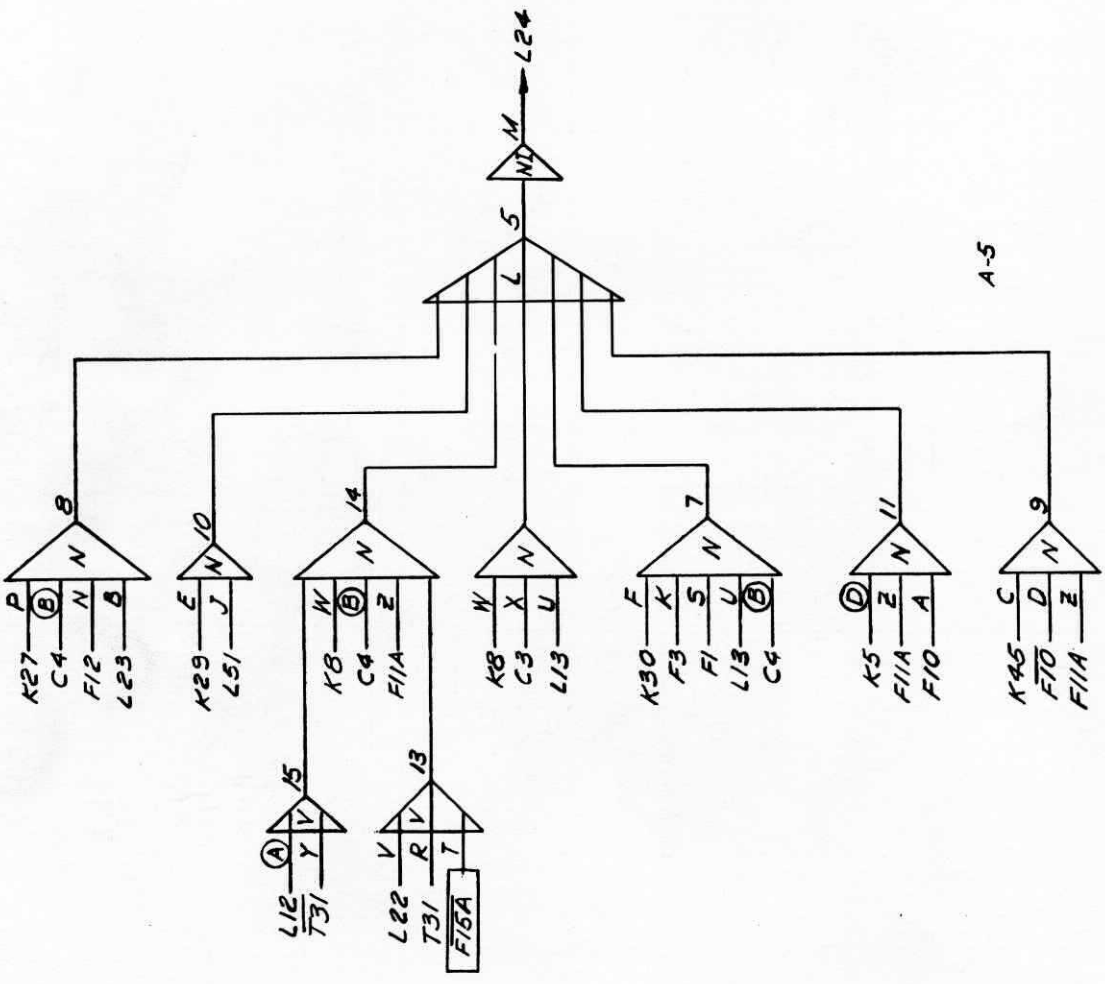


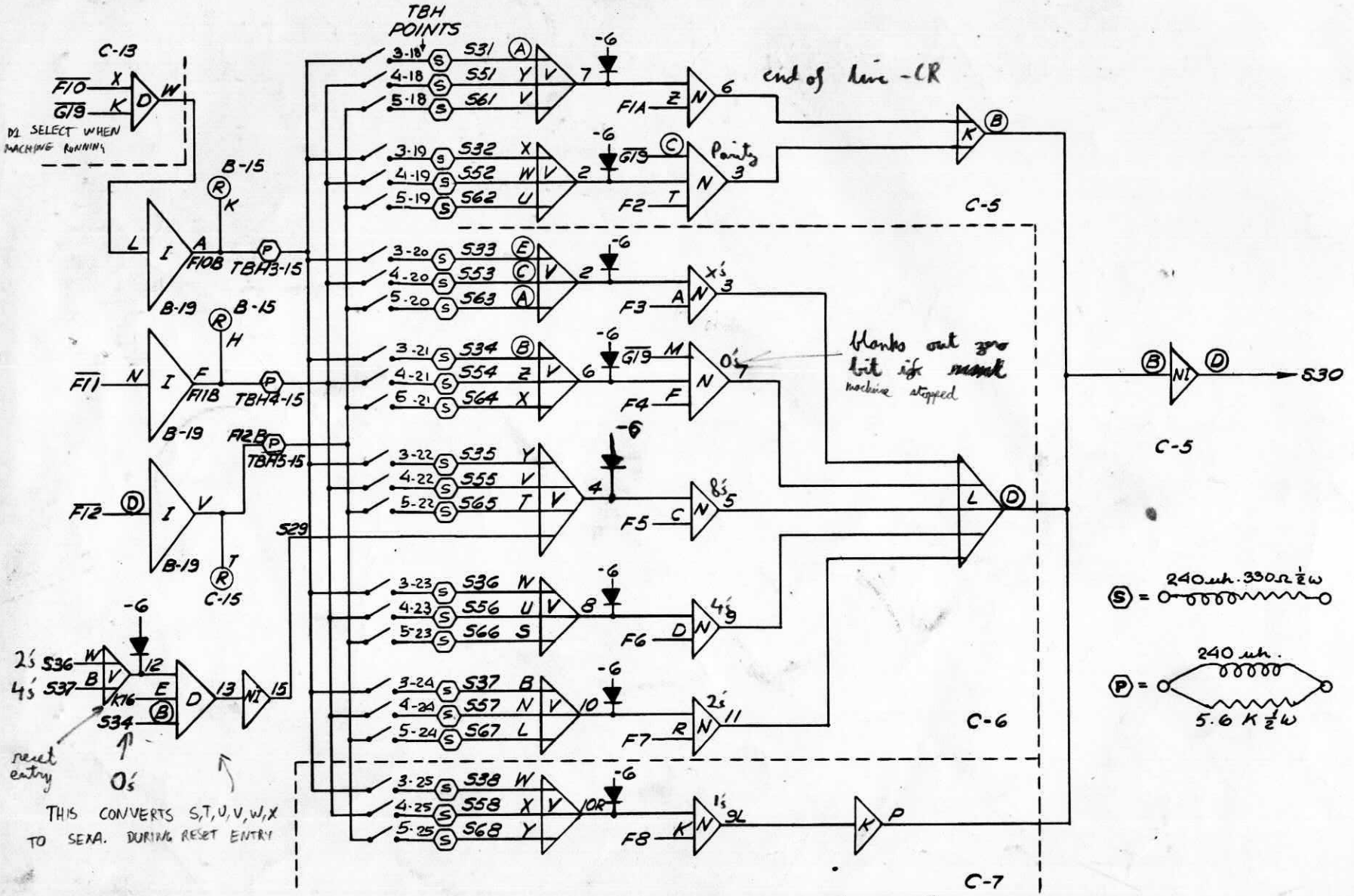
6-15-62

ACCUMULATOR RECORD NET (D)

B-579069

RECORDS ACCUM IN FAA DURING PH. Ø


MULTIPLIER RECORD NET (D) B-579070
A-5
6-15-62

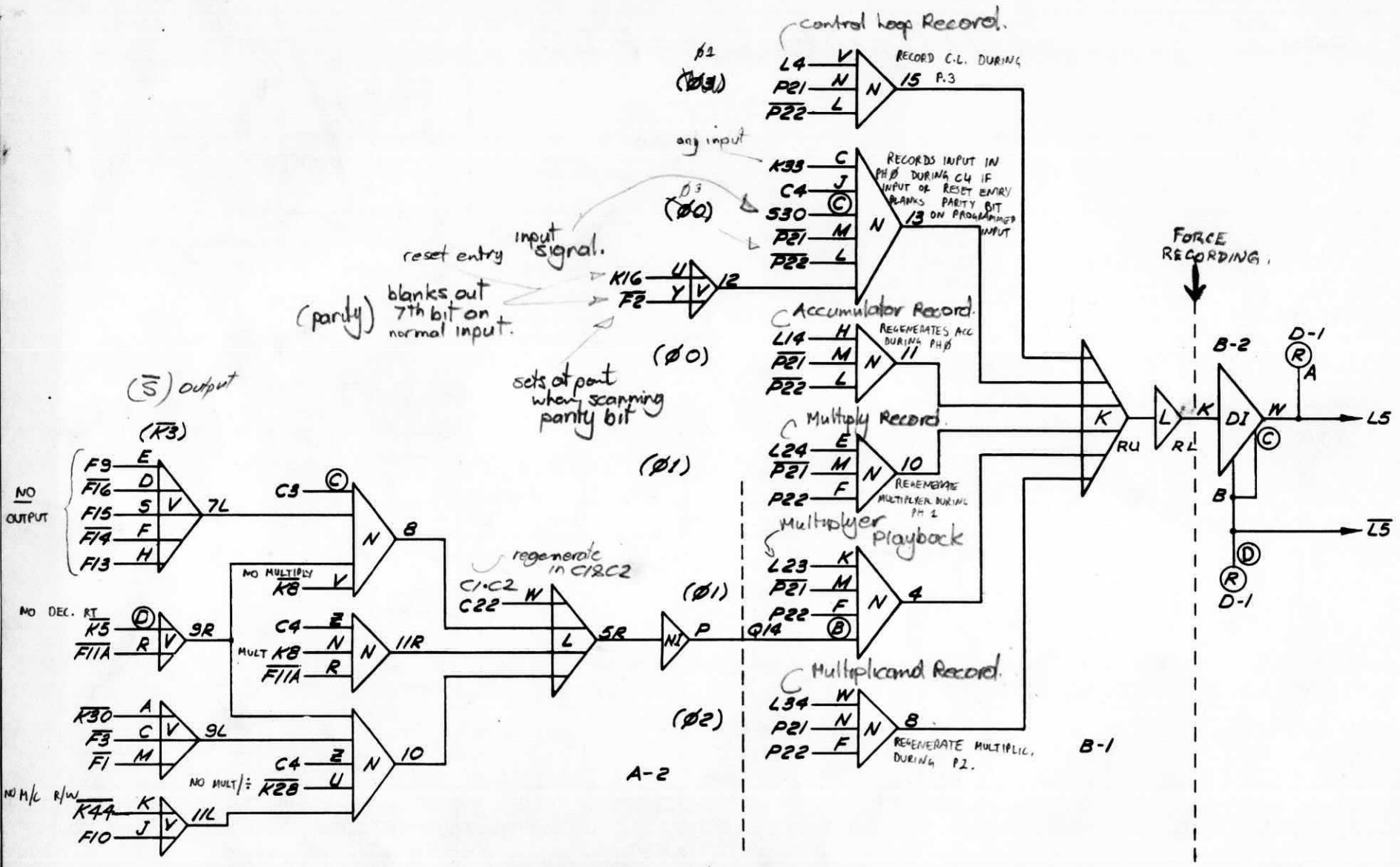


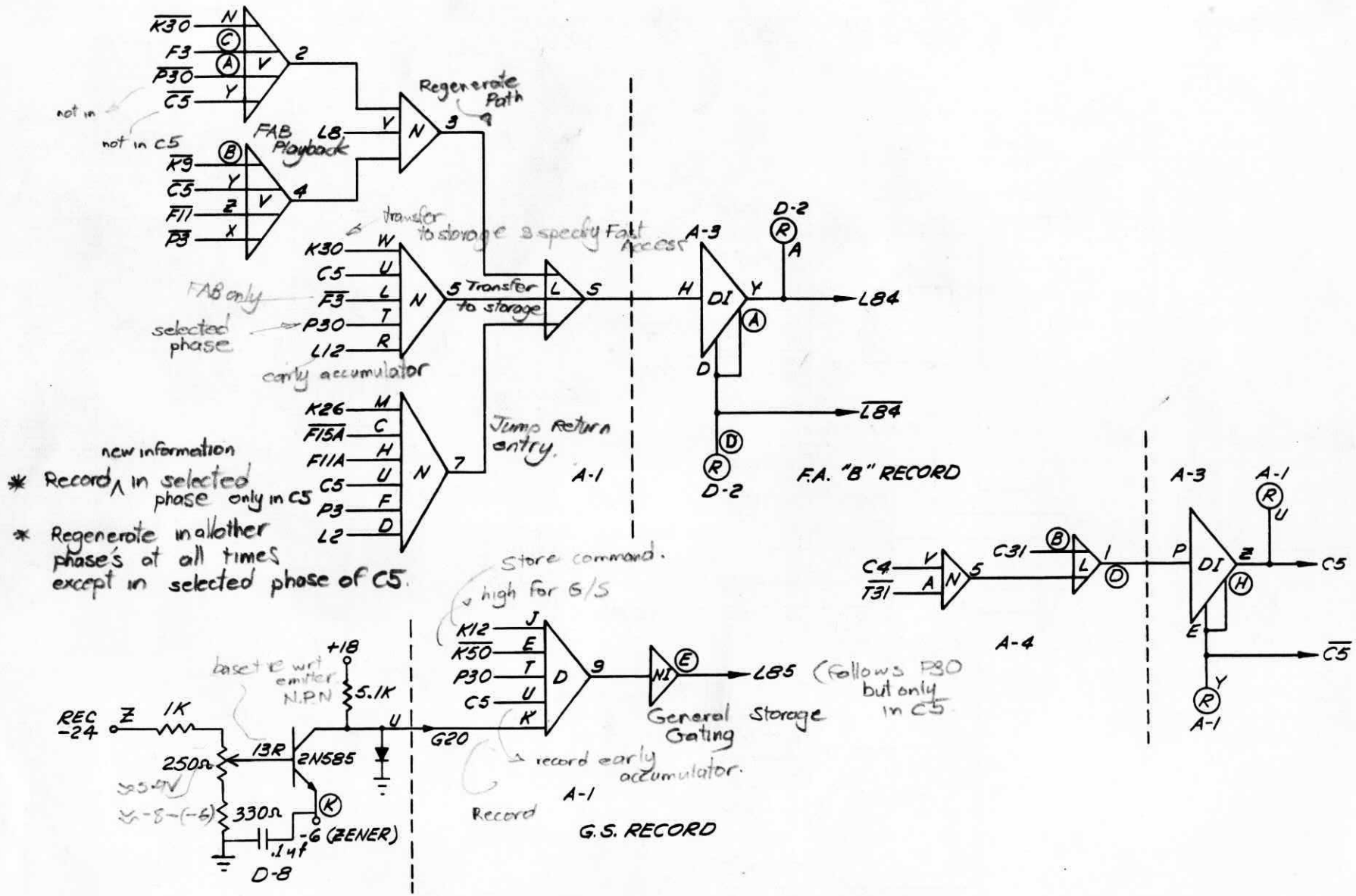
8-31-64

INPUT NET "XI & D"

(WITH IMPROVEMENT NOTICE * 15)

579,019-B

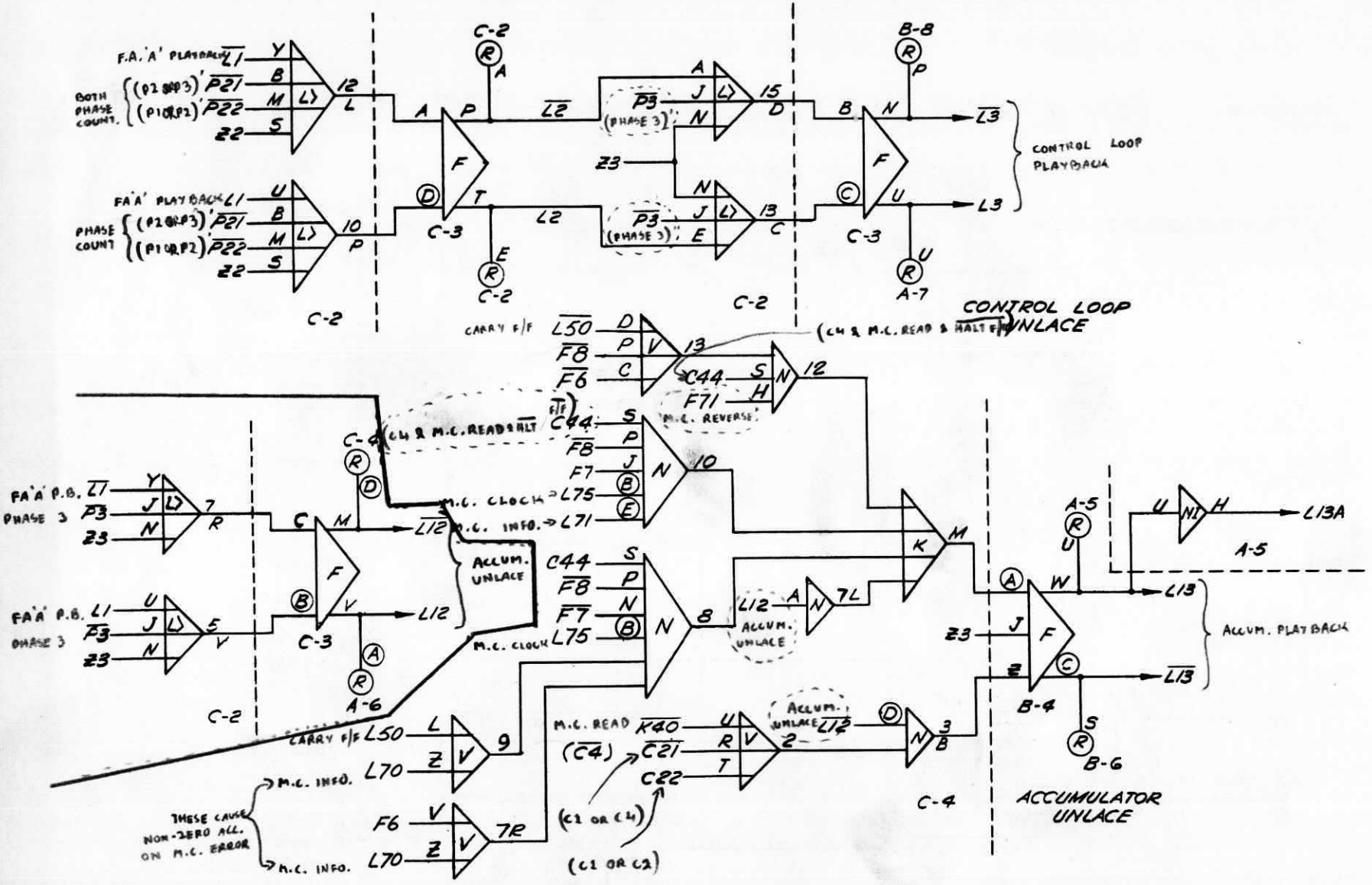

control loop Record.
RECORD C.L. DURING 15 P.3
any input
RECORDS INPUT IN PHØ DURING C4 IF INPUT OR RESET ENTRY BLANKS PARITY BIT ON PROGRAMMED INPUT 13
reset entry
input signal.
(parity)
blanks out 7th bit on normal input.
sets at part when scanning parity bit
Accumulator Record.
REGENERATES ACC DURING PHØ 11
Multiply Record.
REGENERATE MULTIPLYER DURING PH 1 10
Multiplyer playback
Multiplicand Record.
REGENERATE MULTIPLIC. DURING P2.
FORCE RECORDING.
(S) output
NO OUTPUT
NO DEC. RT
NO MULTIPLY
MULT
NO MULT/÷
NO M/C R/W
regenerate in C1&C2
C1·C2
A-2
B-1
B-2
REV. 8-31-64
F.A. A RECORD NET (D)
B-579072



6-19-62

G.S. & F.A. "B" RECORD (D)

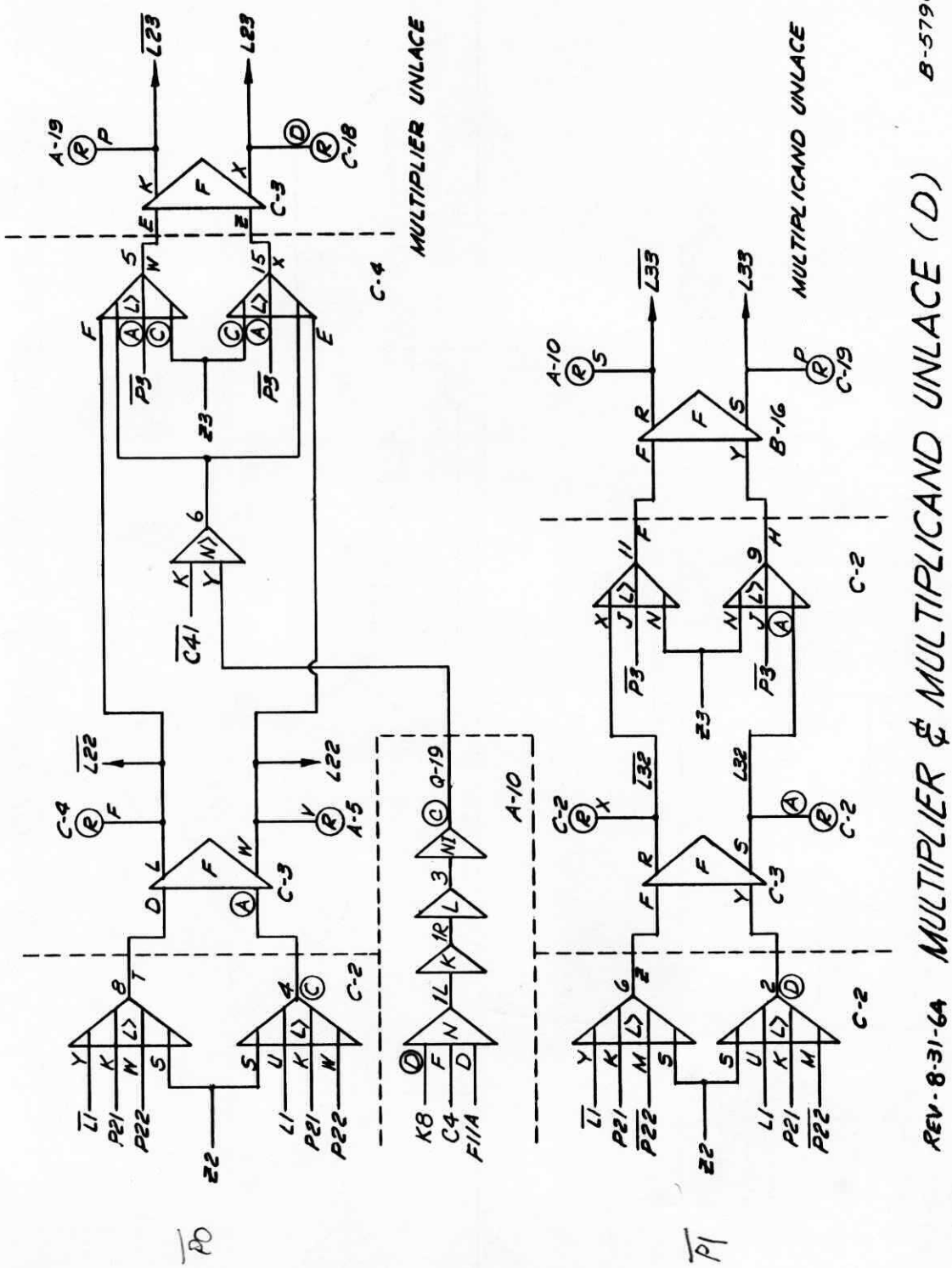
B-579073



6-15-62

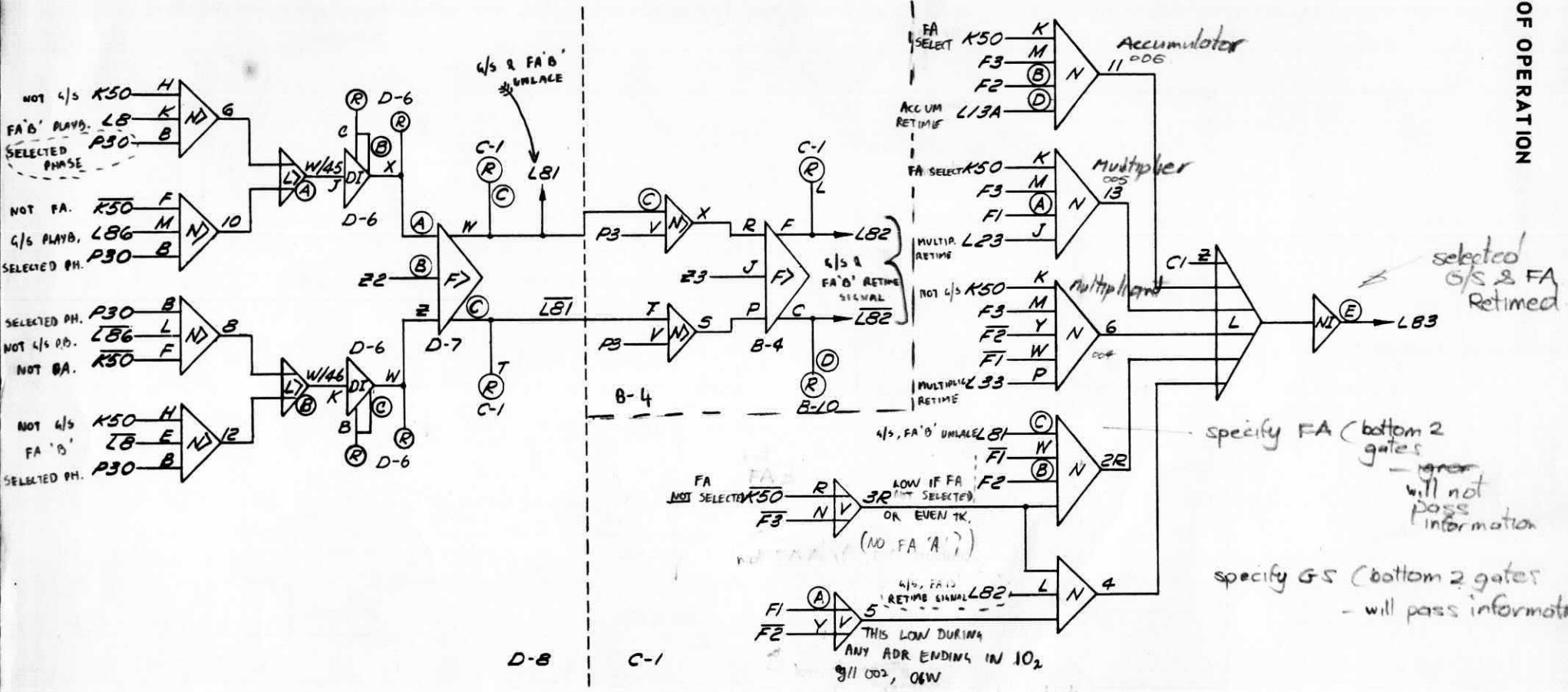
CONTROL LOOP & ACCUMULATOR UNLACE (D)

B-579,074



REV. 8-31-64 MULTIPLIER & MULTIPLICAND UNLACE (D) B-579075

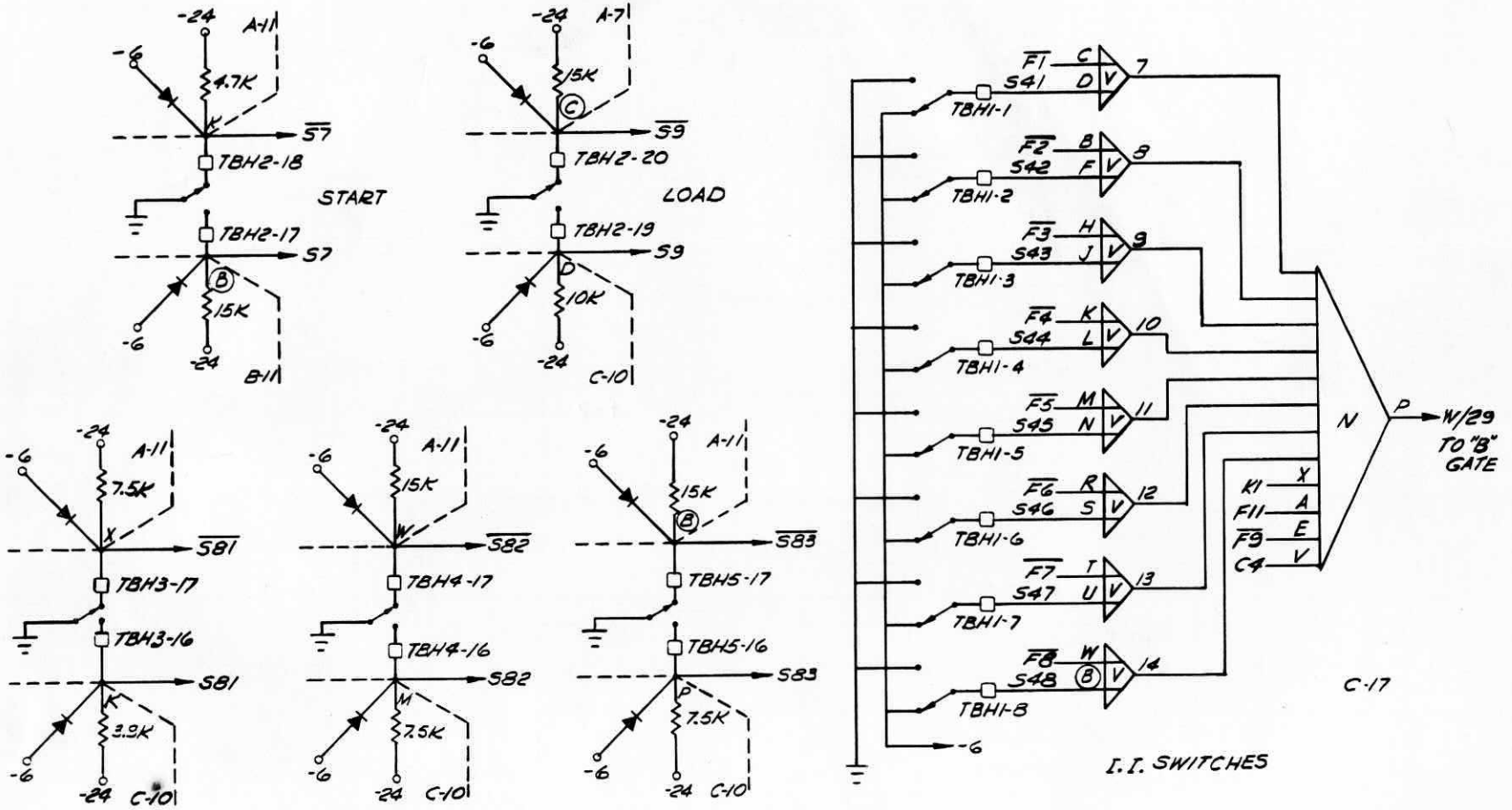
C.L does not appear since it is not addressable



8-3-62

G.S. PLAYBACK (D)

B-579076-A

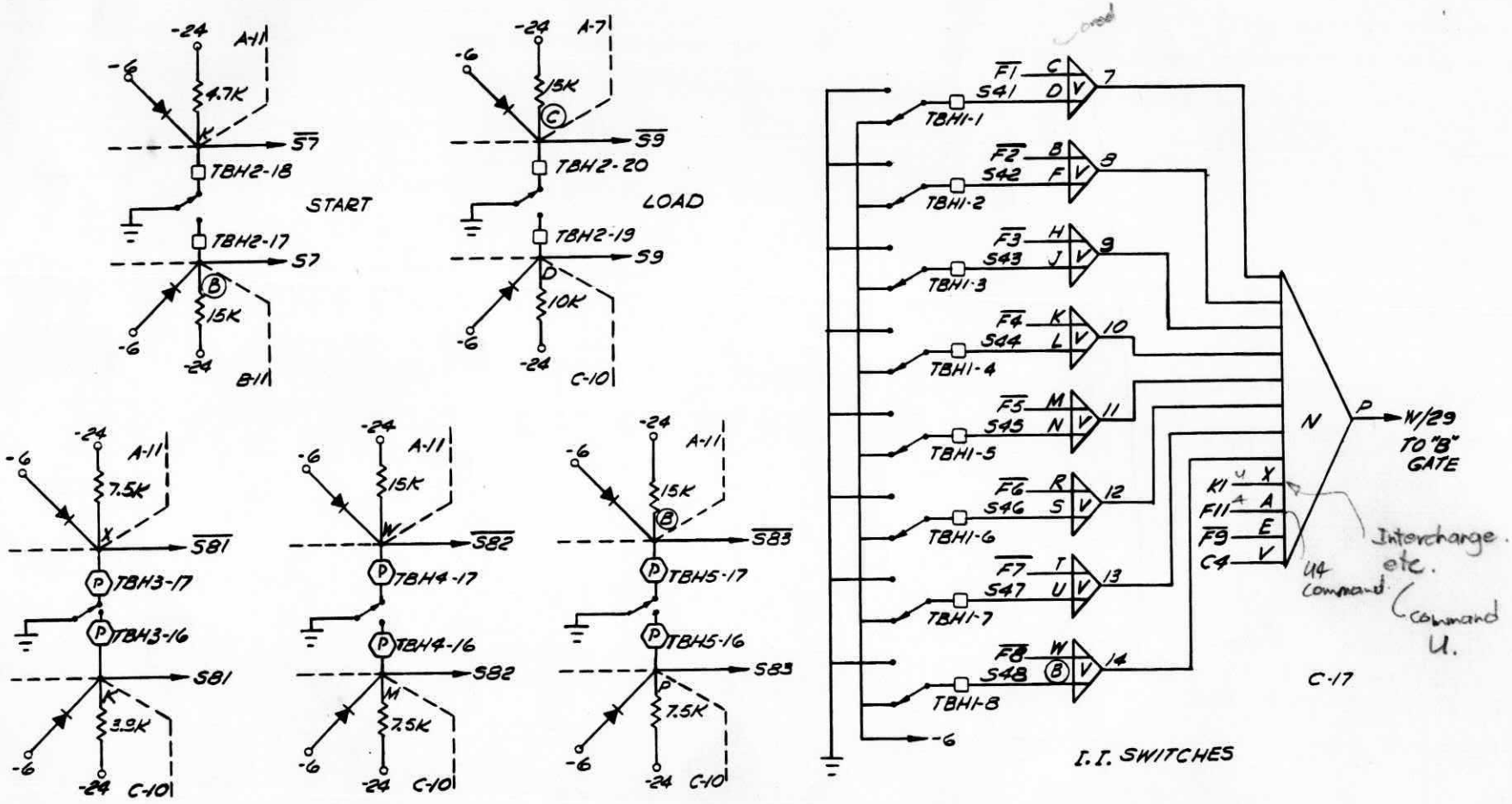


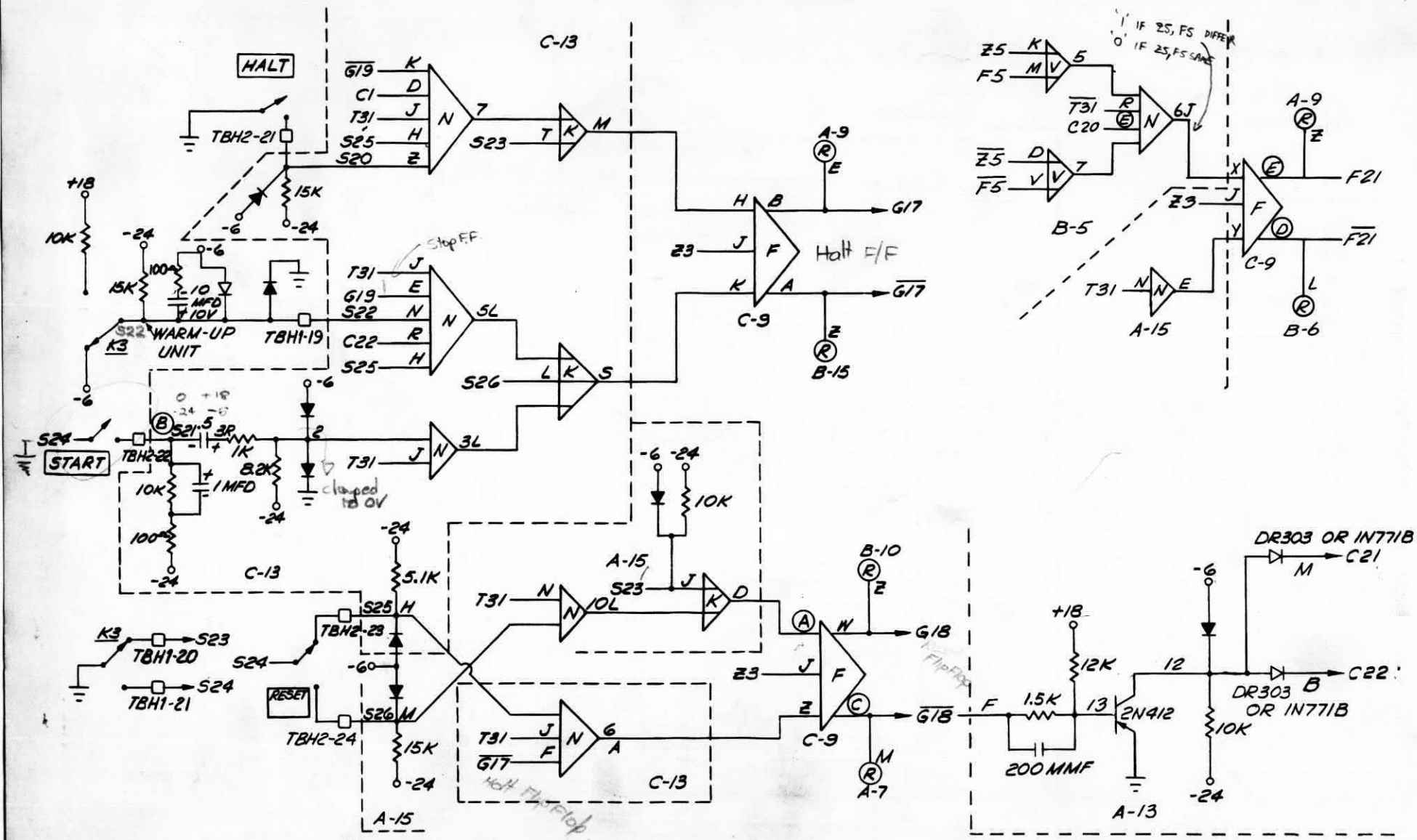
6-20-60

SWITCHES "X1 & D"

579,025-A

SEE P 3-140A FOR IMPROVEMENTS AS PER IMPROVEMENT NOTICE #15


-24
A-11
4.7K
S7
TBH2-18
START
TBH2-17
S7
15K
-6
-24
B-11
-24
A-7
15K
S9
TBH2-20
LOAD
TBH2-19
S9
10K
-6
-24
C-10
F1
S41
TBH1-1
F2
S42
TBH1-2
F3
S43
TBH1-3
F4
S44
TBH1-4
F5
S45
TBH1-5
F6
S46
TBH1-6
F7
S47
TBH1-7
F8
S48
TBH1-8
-6
I.I. SWITCHES
N
P
W/29
TO "B"
GATE
K1
F11
F9
C4
Interchange
etc.
U4
command
(command
U.
C-17
7.5K
S81
TBH3-17
TBH3-16
S81
3.9K
-6
-24
C-10
15K
S82
TBH4-17
TBH4-16
S82
7.5K
-6
-24
C-10
15K
S83
TBH5-17
TBH5-16
S83
7.5K
-6
-24
C-10
240 mh
5.6K ½ w
SWITCHES "X1 & D"
(WITH IMPROVEMENT NOTICE *15)
8-31-64
579,025-B

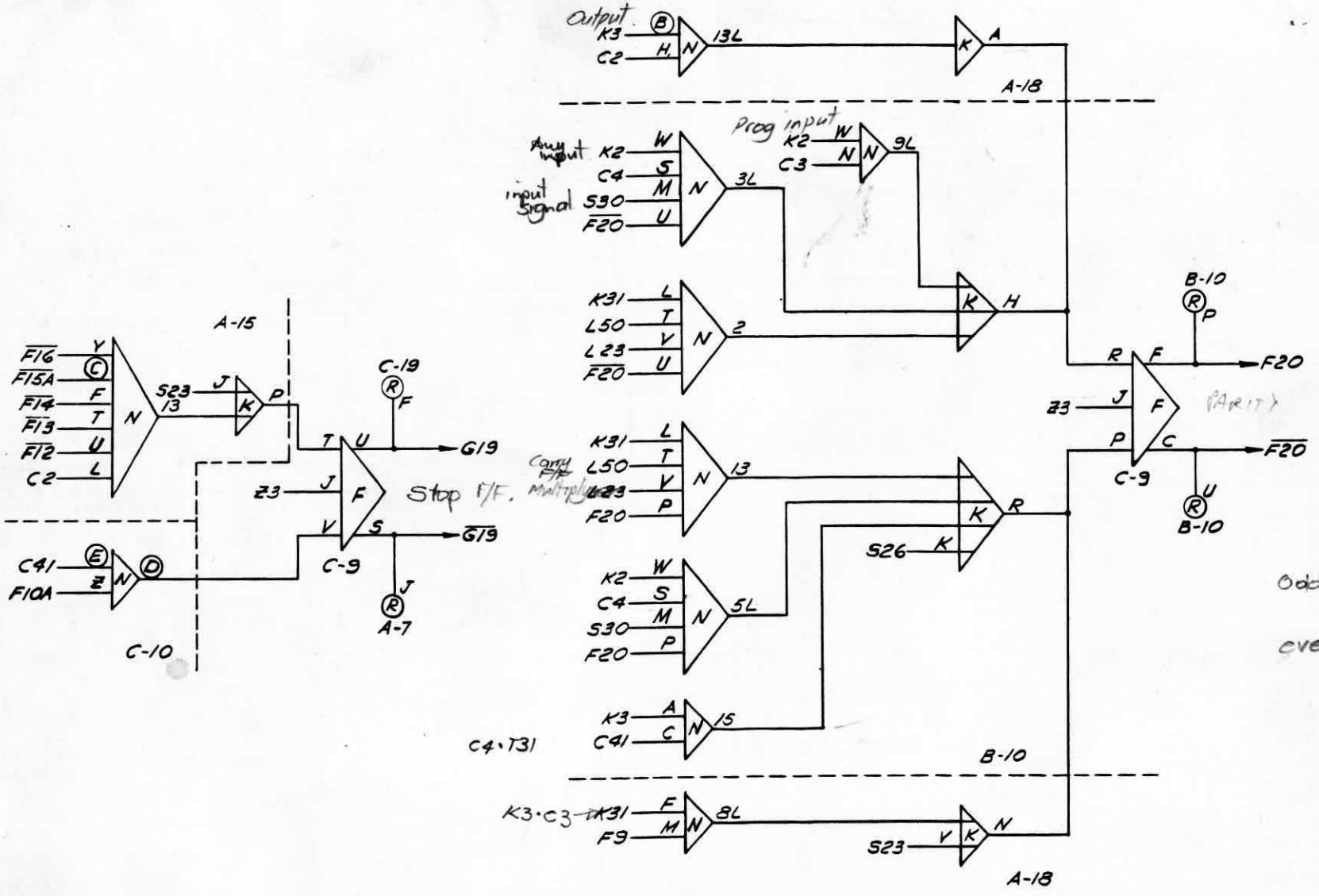


REV. 8-31-64

SEE REVISED VERSION.

HALT F.F. & RESET F.F. (D)

B-579077-A



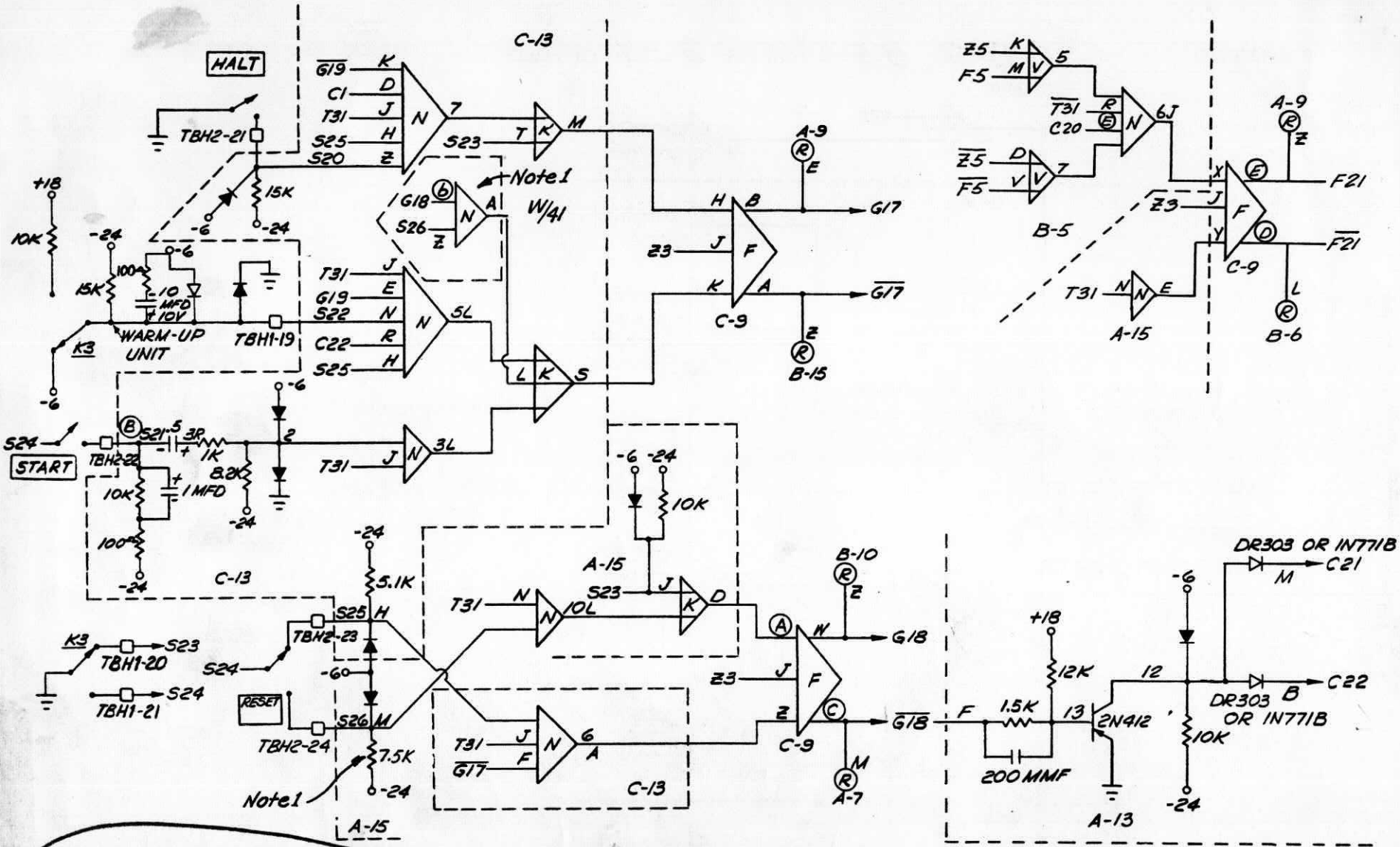
Odd number bits – reset

even number bits – set

6-23-60

STOP F.F. & PARITY F.F. "X1 & D"

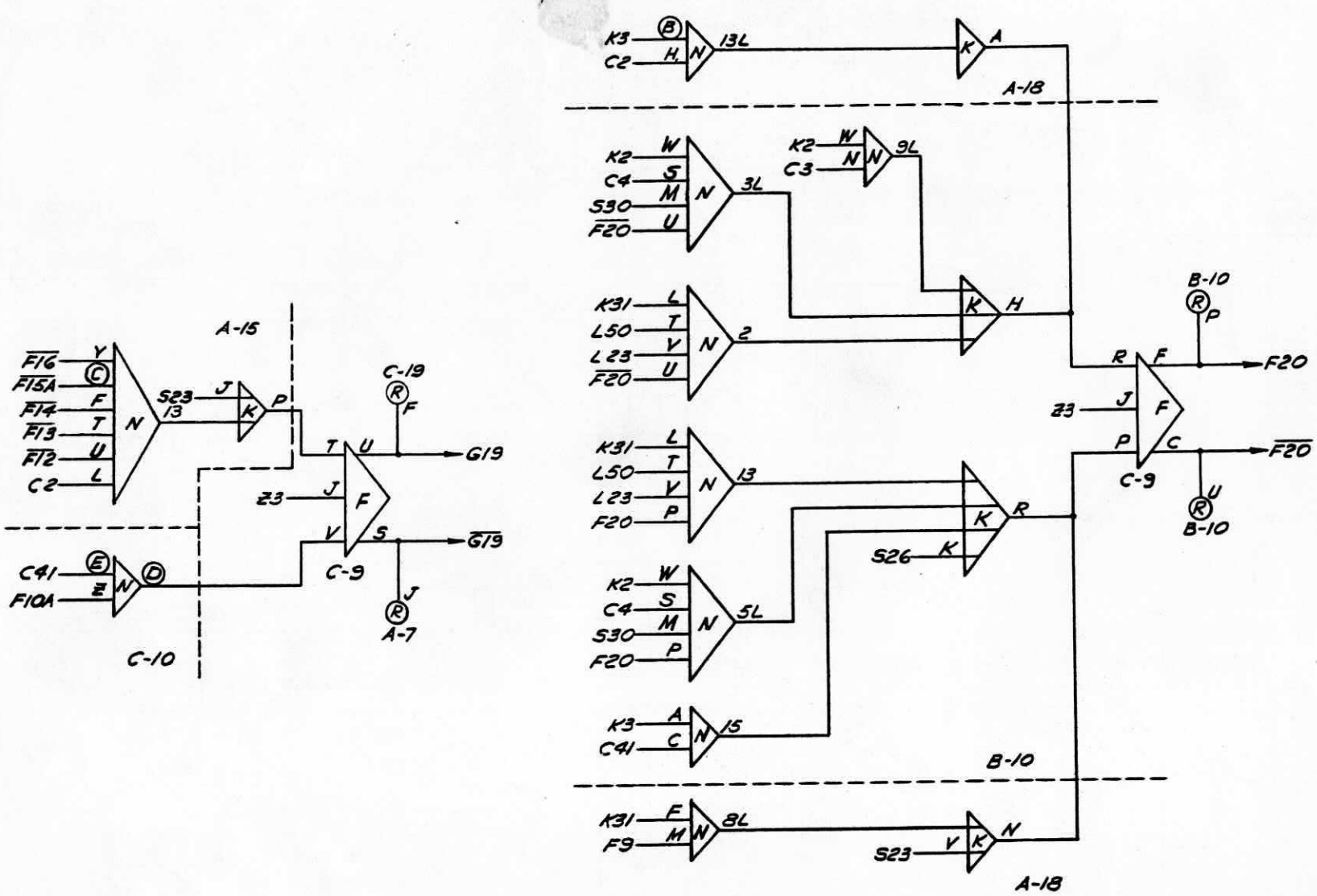
579,027-A



Note 1: M.I.N. No. 24 (Eng. Ch. #35)
Serial No. XXX630 & up.
Revised 1-5-66

HALT F.F. & RESET F.F. (D)

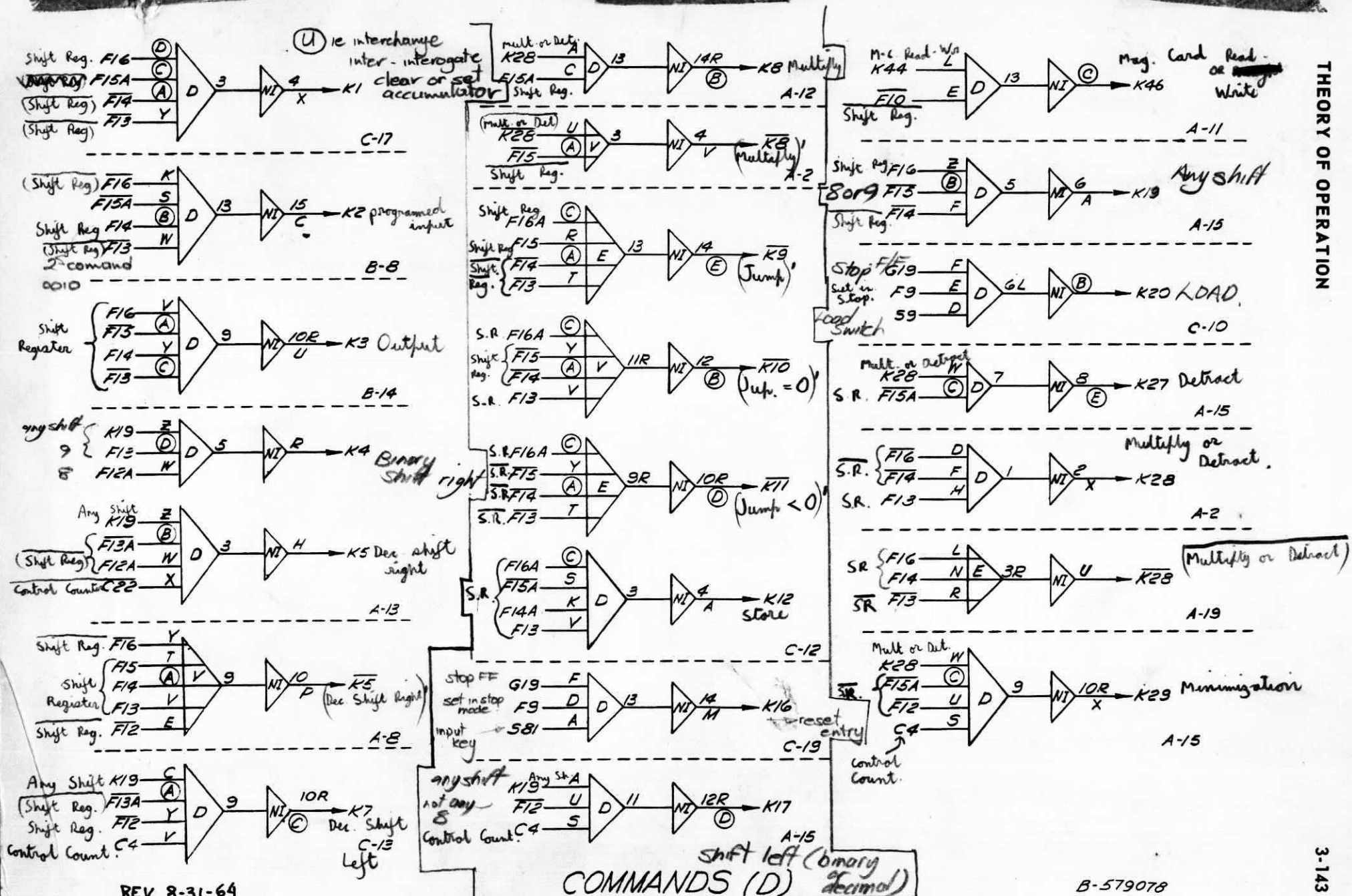
B-579077-A



6-23-60

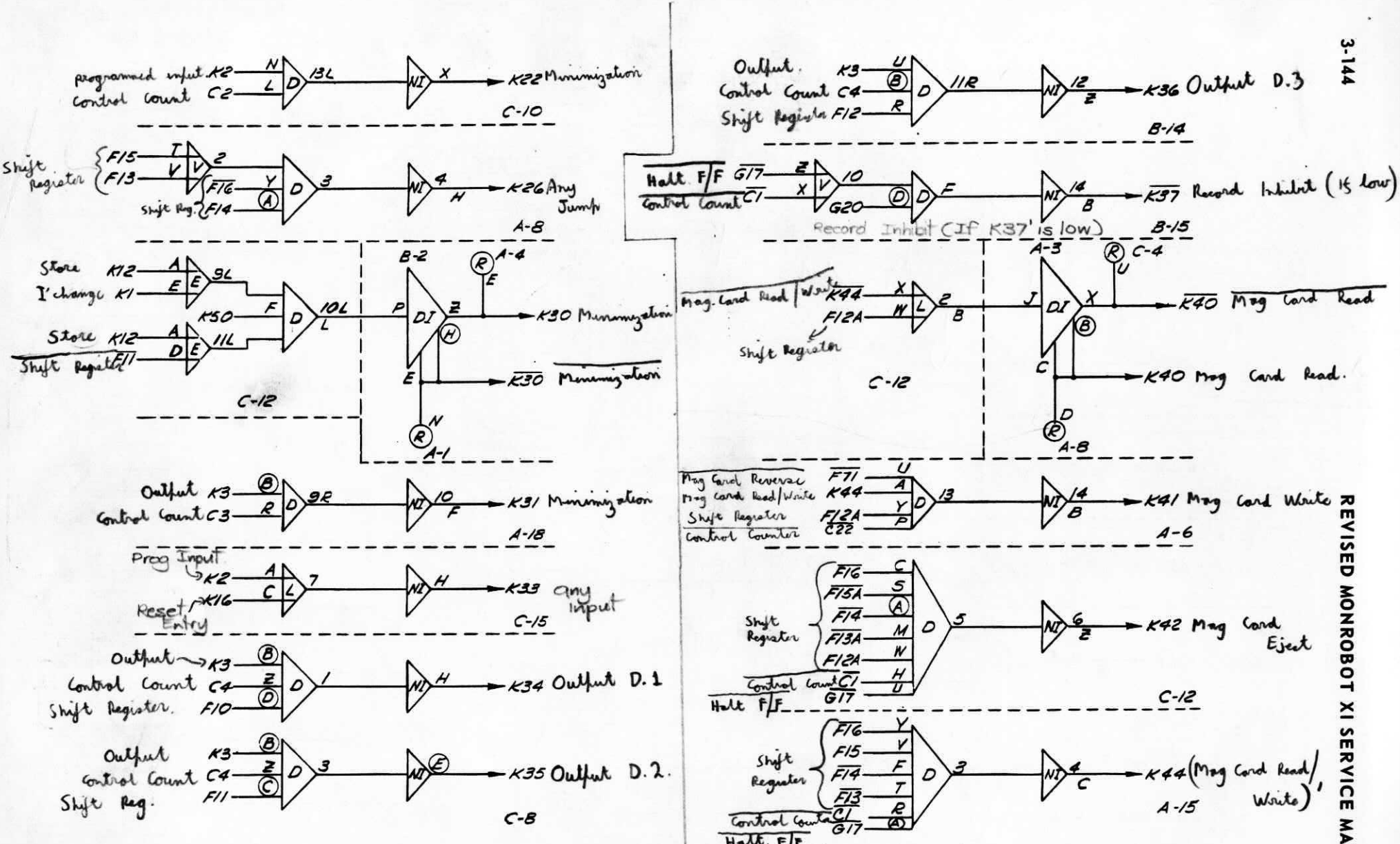
STOP F.F. & PARITY F.F. "XI & D"

579,027-A



COMMANDS (D)

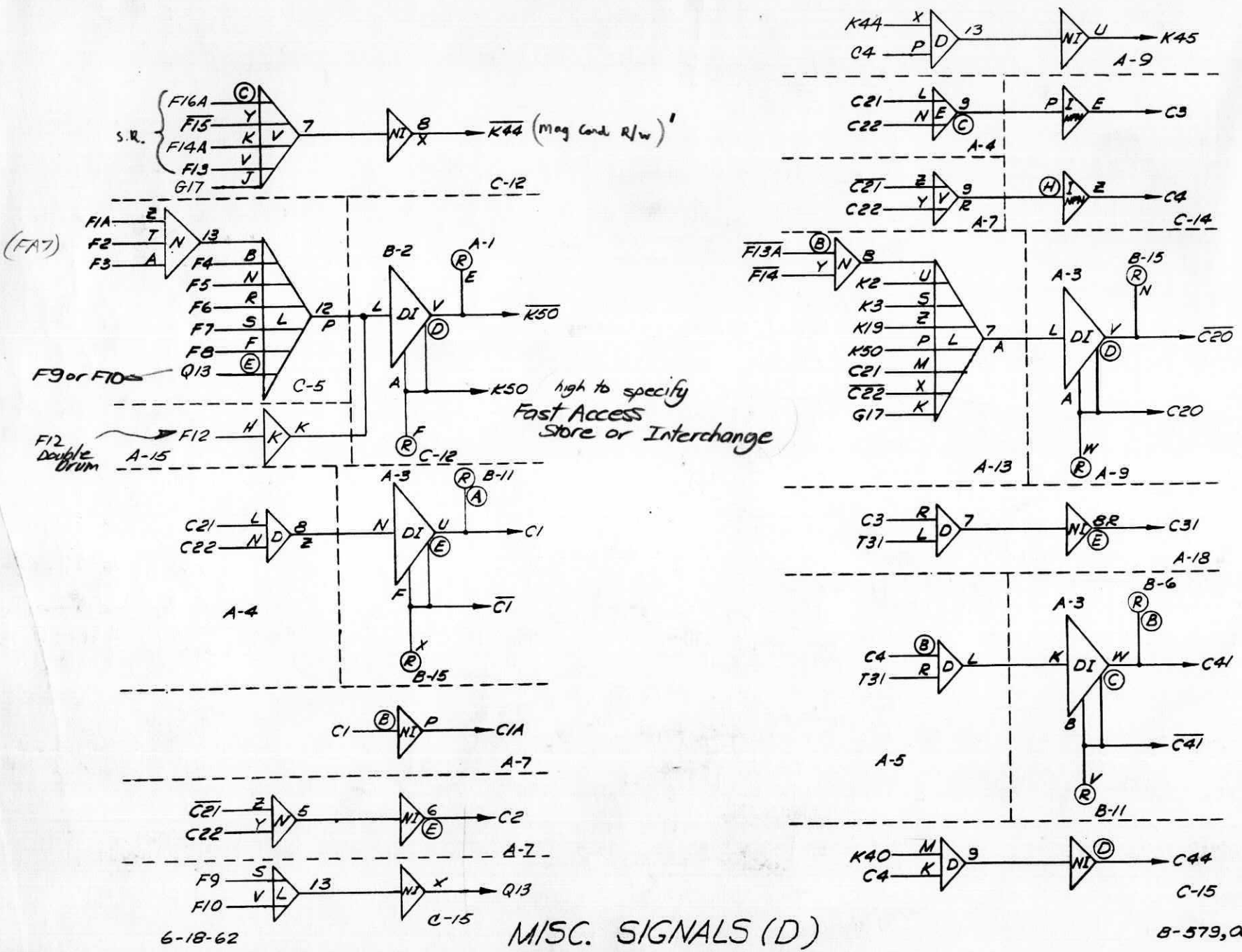
B-579078

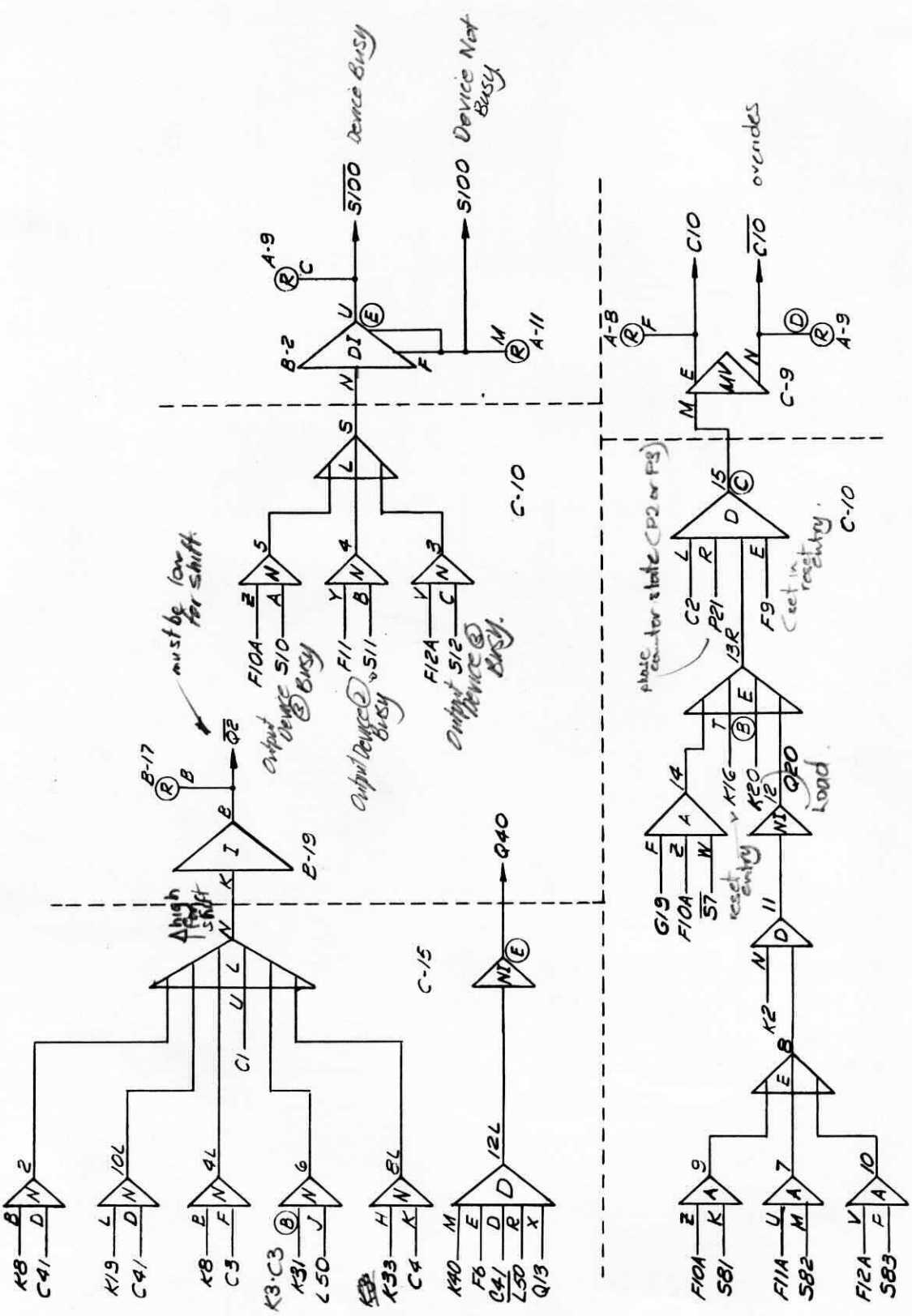


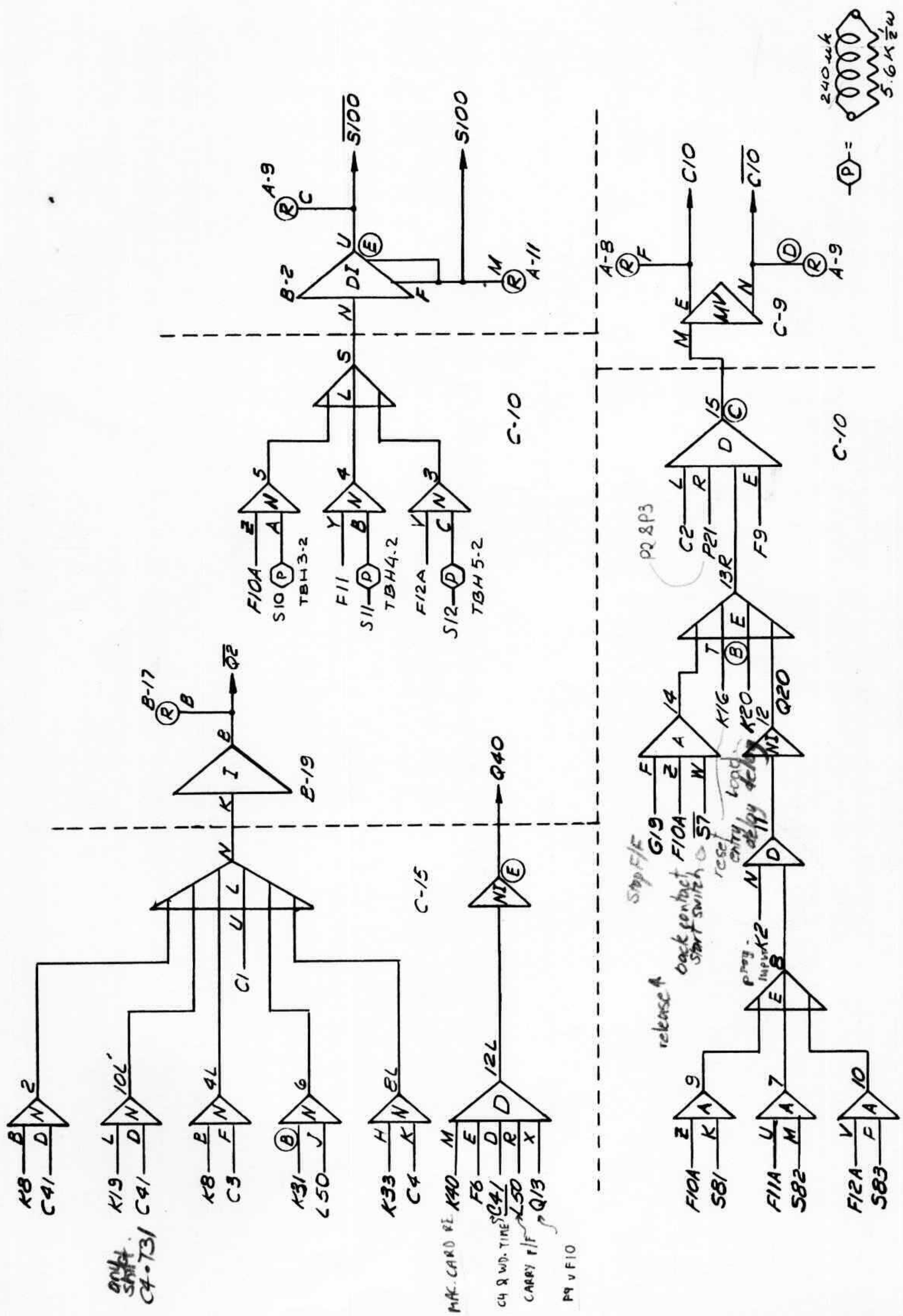
6-18-62

COMMANDS (D)

B-579079


S.R.
F16A
F15
F14A
F13
G17
7
NI
K44 (Mag Core R/W)'
C-12
(FA7)
F1A
F2
F3
F4
F5
F6
F7
F8
Q13
F9 or F10
C-5
F12 Double Drum
A-15
DI
K50
A-1
B-2
C-12
high to specify Fast Access Store or Interchange
C21
C22
A-4
C1
B-11
B-15
C1A
A-7
C2
A-7
F9
F10
Q13
C-15
6-18-62
MISC. SIGNALS (D)
K44
C4
A-9
K45
C21
C22
A-4
C3
A-4
C21
C22
A-7
C4
C-14
F13A
F14
K2
K3
K19
K50
C21
C22
G17
A-13
A-3
B-15
C20
C20
A-9
C3
T31
A-18
C31
C4
T31
A-5
A-3
B-6
C41
C41
B-11
K40
C4
C-15
C44
B-579,080

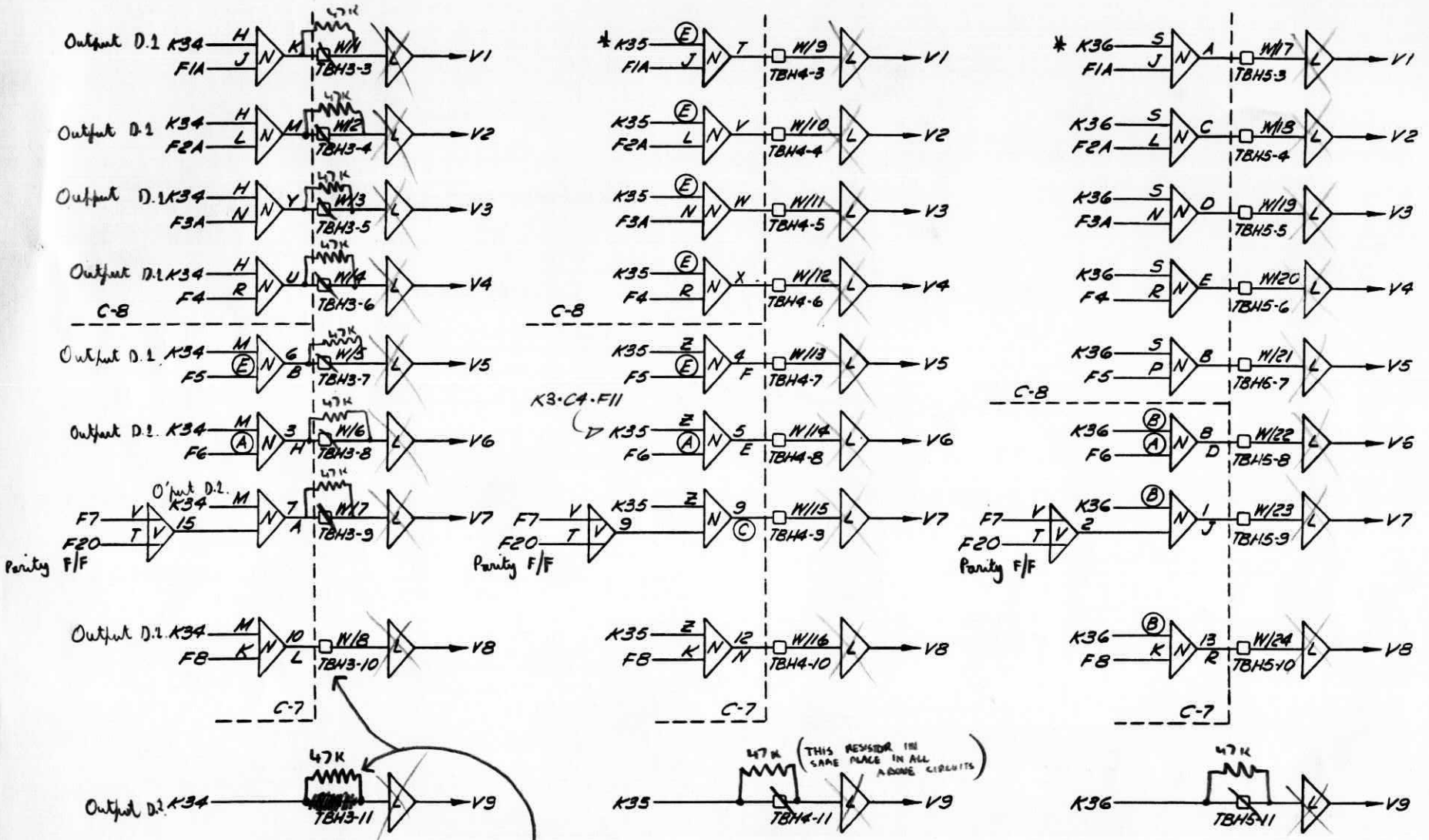

MISC. SIGNALS (D)
B579081
6-18-62
must be low for shift
Output Device Busy
Device Busy
Device Not Busy
overides
reset entry
Load
C-10
C-15
C-9
A-8
A-9
A-11
B-2
B-17
E-19



MISC. SIGNALS (D)

B579081

8-31-64



GRID DRIVES (X1 & D)

579,032-A

K34 = Output D.1
K35 = Output D.2.
K36 = Output D.3.

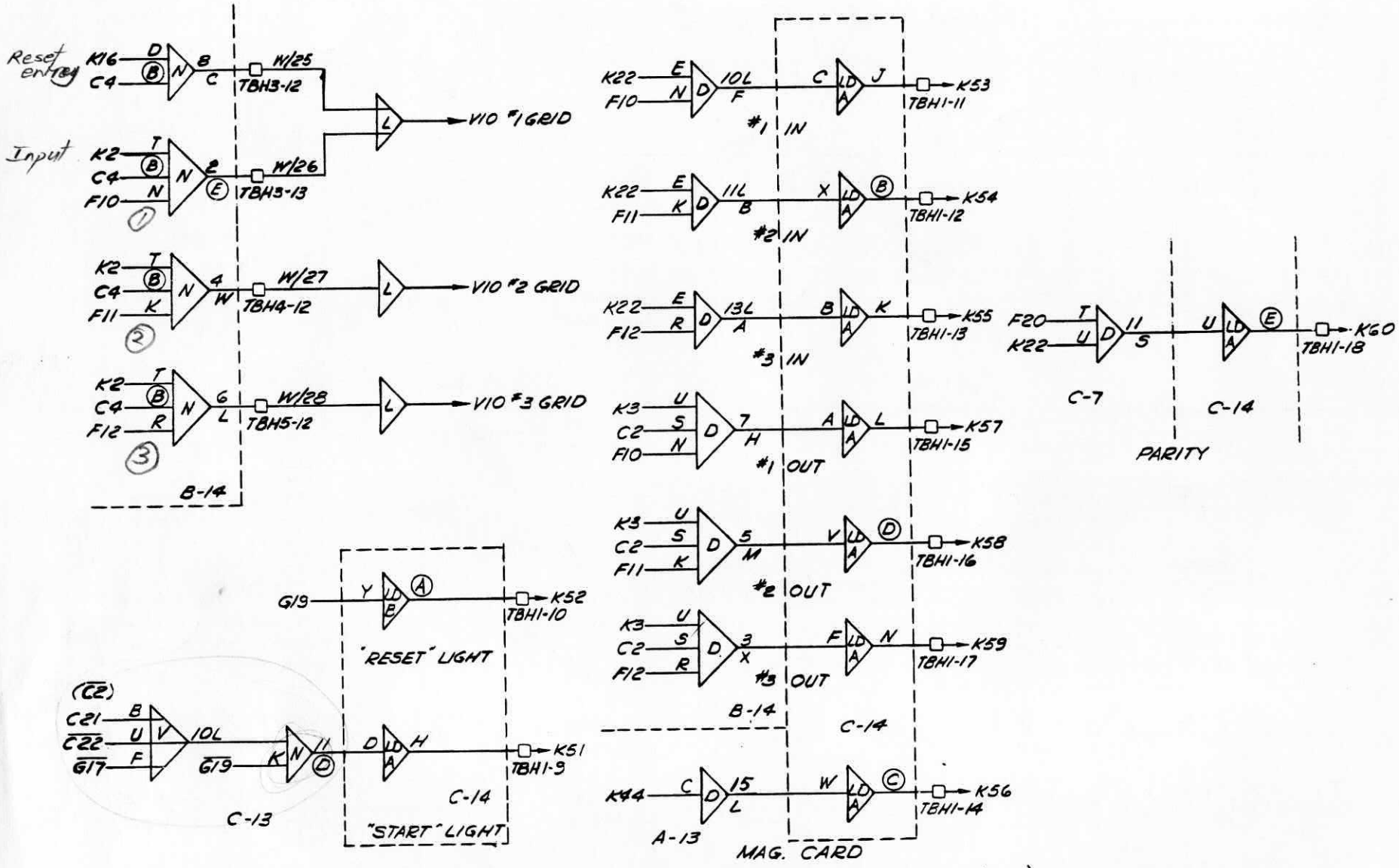
F1 - 8 = Orders Shift Register F/F's

IMPROVEMENT 6-20-60 (31/8/64) (Notice #15)

One 47K, ½ W resistor added at box boards dotted dividing line. In ALL circuits.

Also, All OR gates on outputs were REMOVED (as shown)

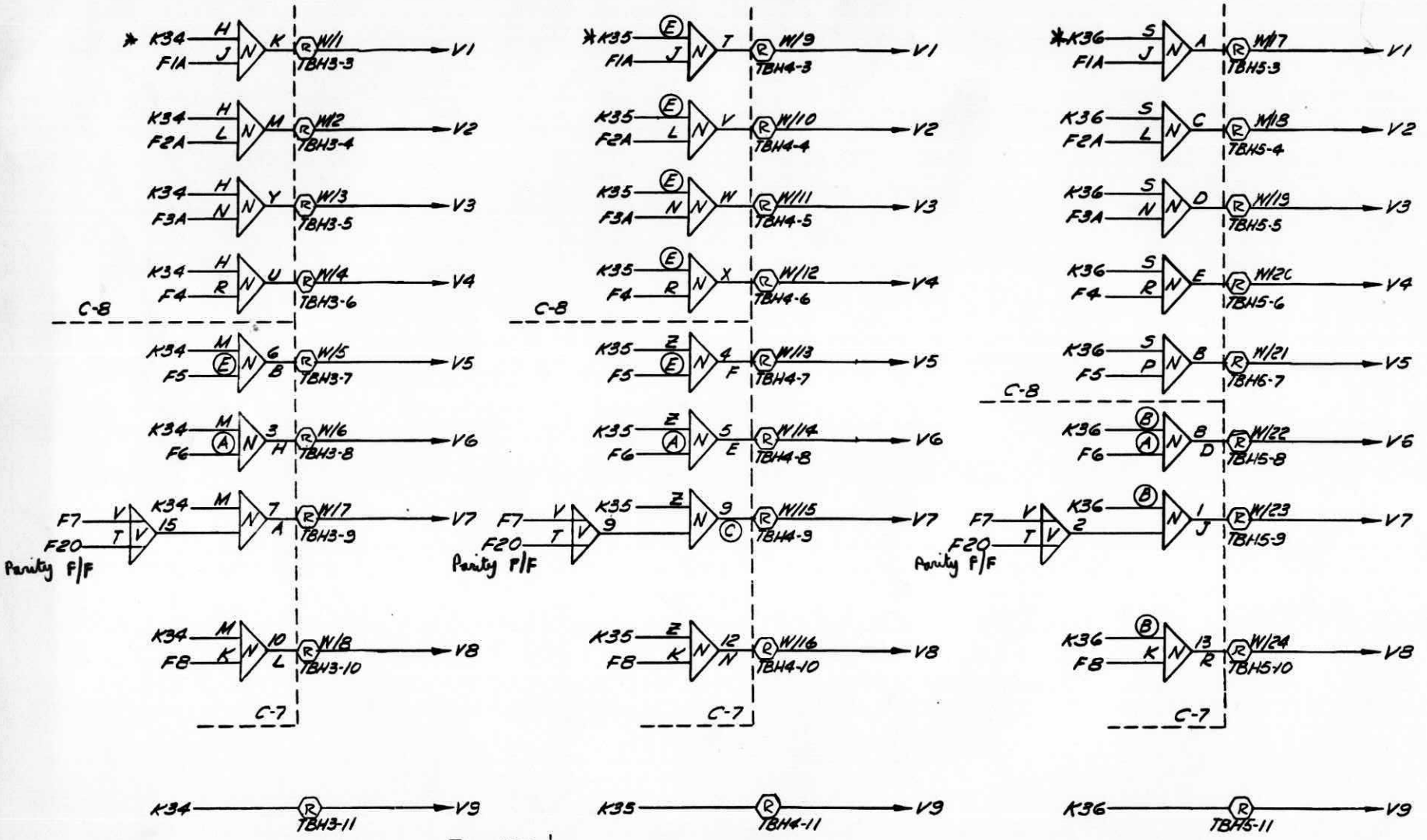
3-147
SEE ρ 147A
FOR IMPROVEMENTS



8-3-62

LIGHT & INPUT THYRATRON DRIVERS (D)

B-579082



8-31-64

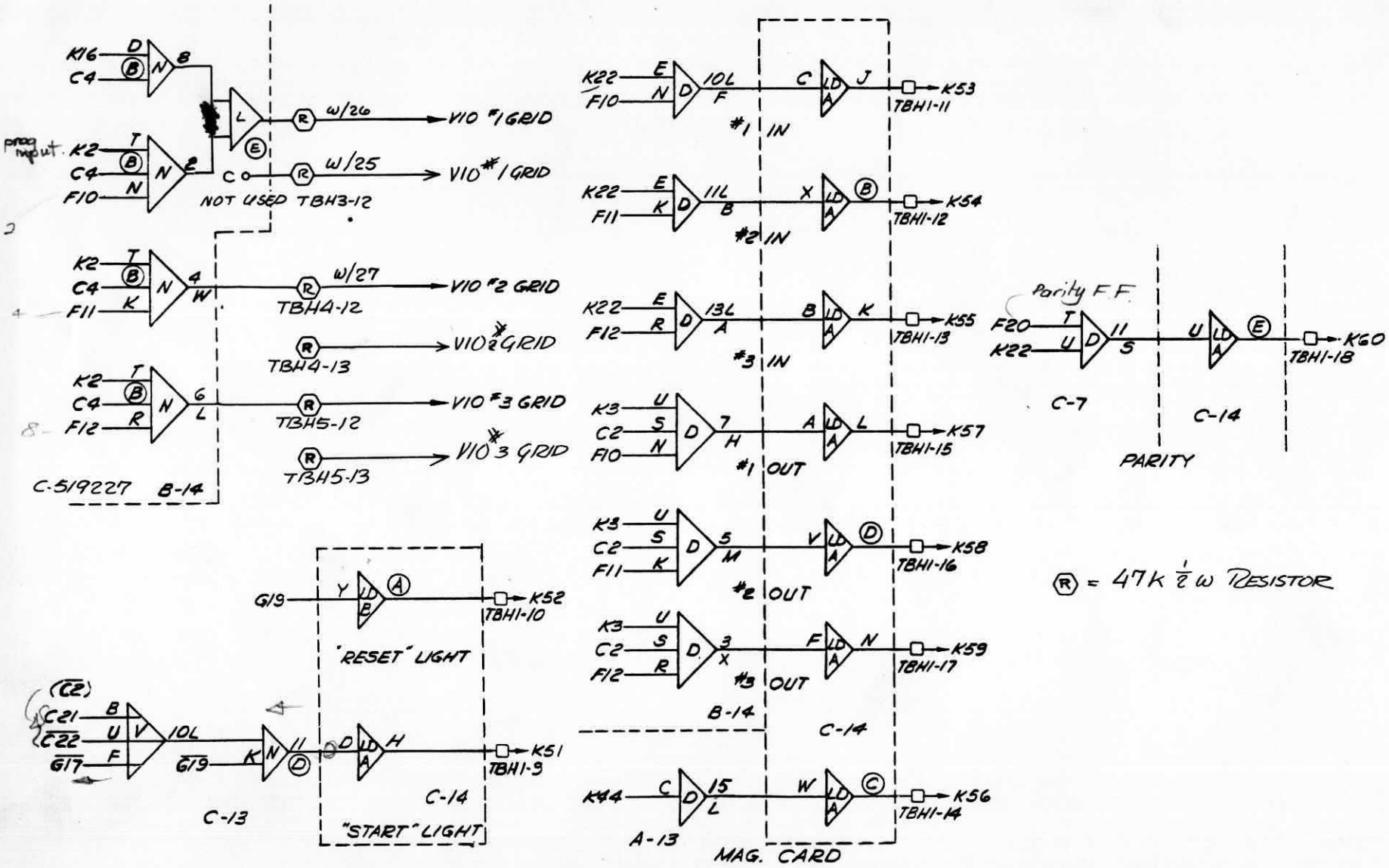
GRID DRIVES (X1 & D)

(WITH IMPROVEMENT NOTICE #16)

579,032-

K34 = Output D.1.
K35 = Output D.2.
K36 = Output D.3.

F1-8 = Orders Shift Register. F/F's 1-8.

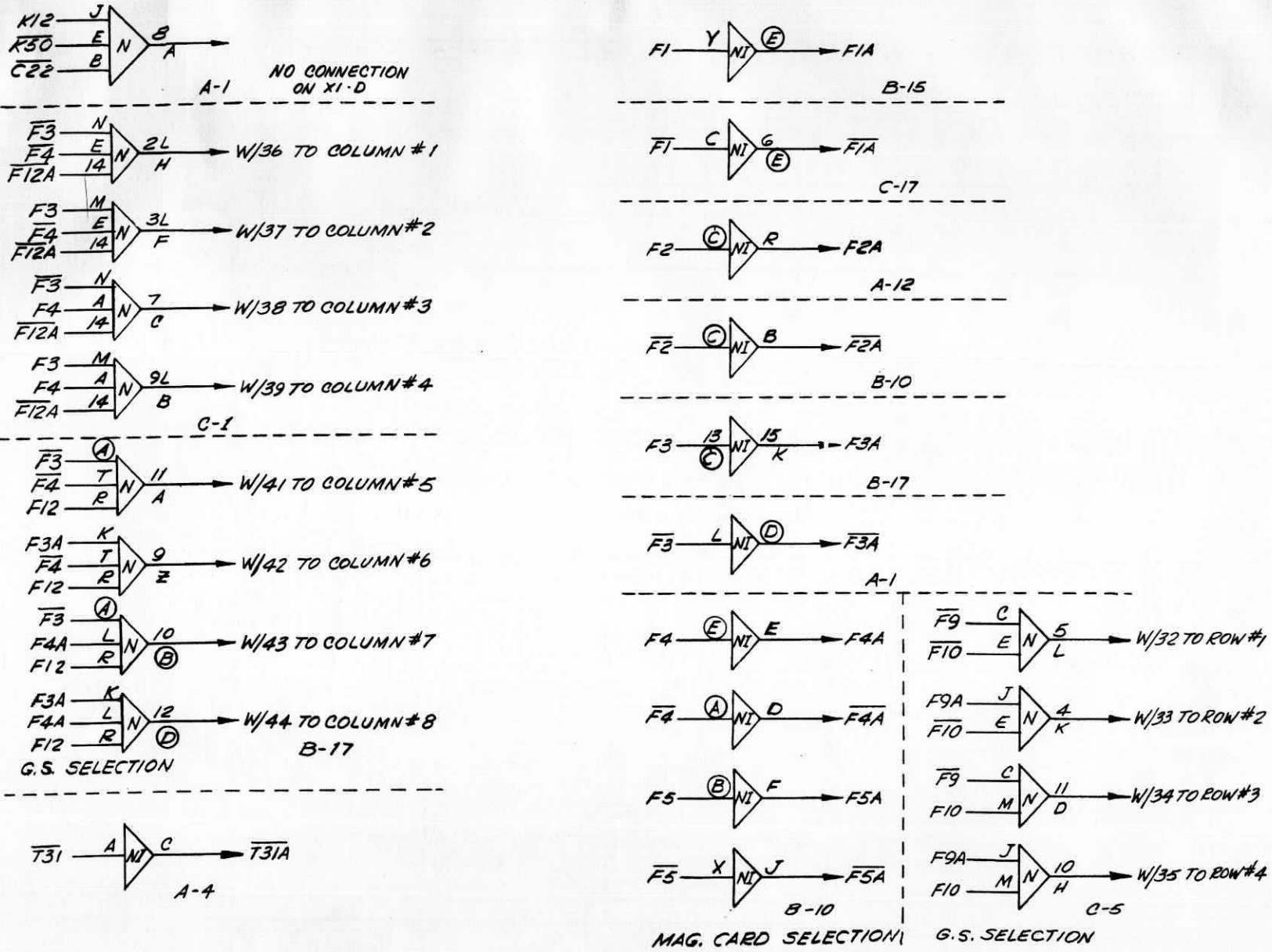


8-31-64

LIGHT & INPUT THYRATRON DRIVERS (D)

(WITH IMPROVEMENT NOTICE #15)

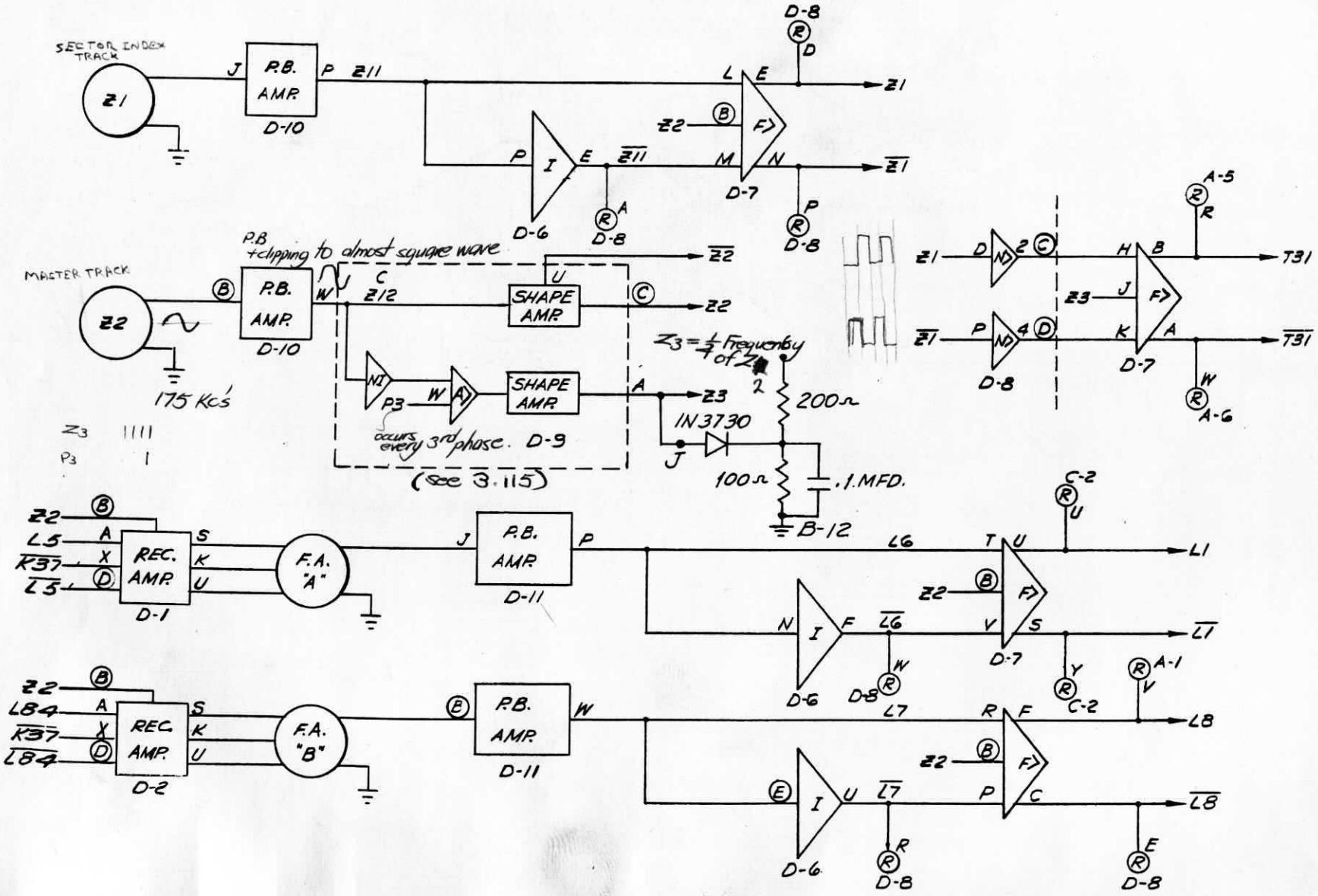
B-579082 A



6-19-62

G.S. & MAG. CARD SELECTION SIGNALS (D)

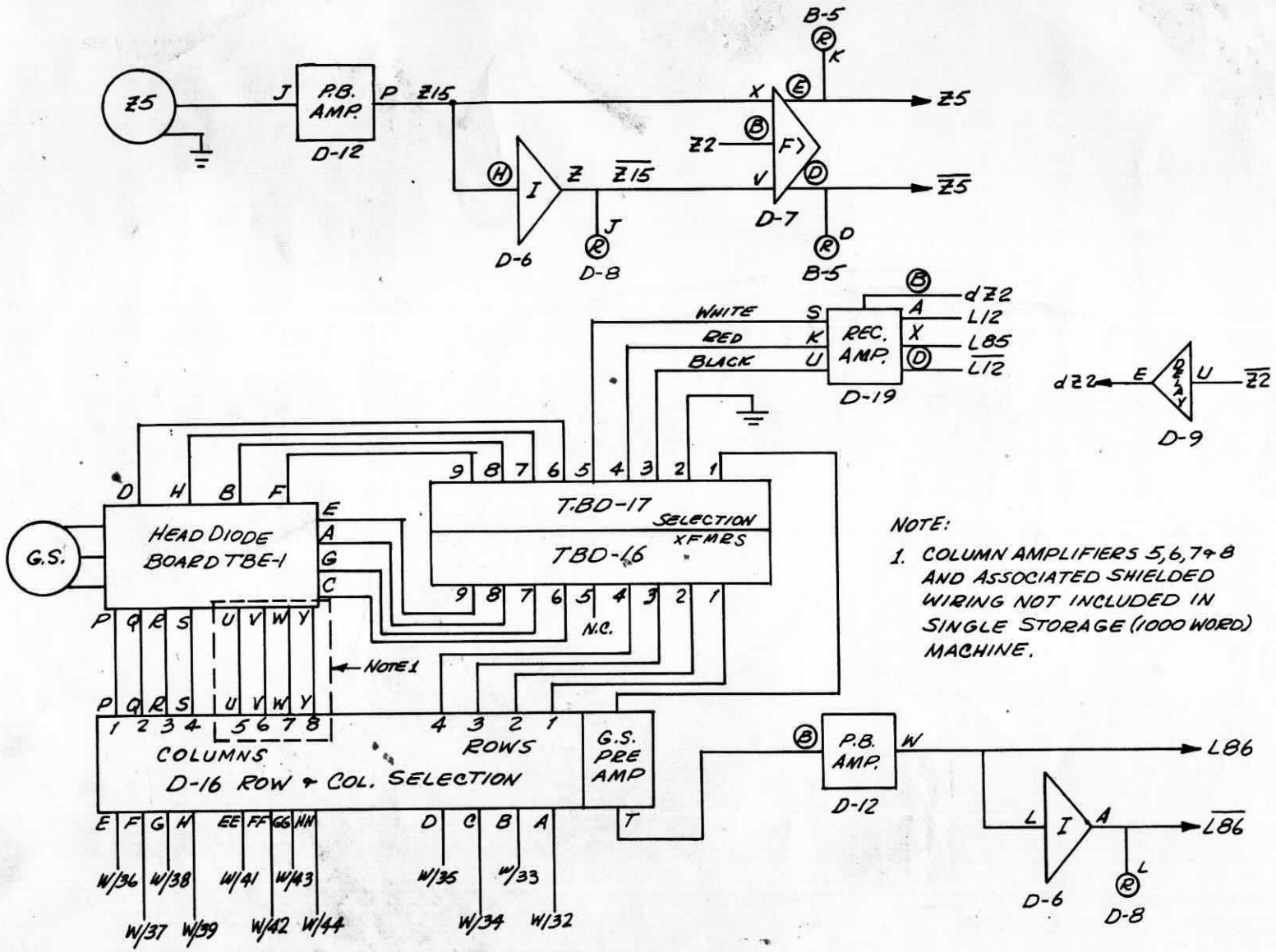
B-579,083A



3-15-63

P.B. & REC. LOGIC T31 "X1 & D"

579,035-A



NOTE:

1. COLUMN AMPLIFIERS 5,6,7+8 AND ASSOCIATED SHIELDED WIRING NOT INCLUDED IN SINGLE STORAGE (1000 WORD) MACHINE.

8-23-62

Z5 & G.S. P.B. LOGIC (D)

B-579084

SIGNAL GLOSSARY

1. All signals used on Monrobot XI are listed with the following exceptions:

   (a) Signals whose suffix is "A" which indicates a non-inverter (NI) used to share the load of a flip-flop (FF) or inverter (I).

   (b) The prime side of flip-flops (FF), double inverters (DI) or multivibrator (MV).

2. In general, the signal prefixes have the following meanings:

C	Timing Control
F	Shift Register Flip-Flops
G	Machine Control Flip-Flops
K	Command
L	Information
P	Phase
Q	Miscellaneous
S	Switch
T	Word Time
W	Wire (Not Used For Amplifiers)
Z	Clock

3. Under function; "Minimization" refers to a signal which was generated in order to save diodes and/or loading.

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
C1	DI	3-145	Control Count	C21·C22
C2	NI	3-145	Control Count	C21'·C22
C3	I(npn)	3-145	Control Count	C21'·C22'
C4	I(npn)	3-145	Control Count	C21·C22'
C5	DI	3-136	General Storage and fast access B record word time	C31 v C4·T31'
C10	MV	3-146	Input Delay	
C18	I	3-123	Minimization	Q2 v C20 v K44·C2

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
C20	DI	3-145	General storage address lookup	C2·G17'·K50'·(any order using storage)
C21	FF	3-116	Control Counter	C1 v C4
C22	FF	3-116	Control Counter	C1 v C2
C31	N1	3-145	Minimization	C3·T31
C41	DI	3-145	Minimization	C4·T31
C44	NI	3-145	Minimization	C4·K40·G17'
F1	FF	3-125	Shift Register	
F2	FF	3-125	Shift Register	
F3	FF	3-124	Shift Register	
F4	FF	3-124	Shift Register	
F5	FF	3-124	Shift Register	
F6	FF	3-123	Shift Register	
F7	FF	3-123	Shift Register	
F8	FF	3-122	Shift Register	
F9	FF	3-121	Shift Register	
F10	FF	3-120	Shift Register	
F10B	I	3-134	Drive Input Contacts	
F11	FF	3-119	Shift Register	
F11B	I	3-134	Drive Input Contacts	
F12	FF	3-118	Shift Register	
F12B	I	3-134	Drive Input Contacts	
F13	FF	3-117	Shift Register	
F14	FF	3-117	Shift Register	
F15	FF	3-117	Shift Register	
F16	FF	3-117	Shift Register	
F20	FF	3-142	Parity Flip-Flop	
F21	FF	3-141	Sector Comparison	
F71	FF	7-	Magnetic Card Reverse	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
G17	FF	3-141	Halt Flip Flop	
G18	FF	3-141	Reset Flip Flop	
G19	FF	3-142	Stop Flip Flop	
G20	Amp.	3-136	Record Inhibit.	
K1	NI	3-143	Interchange, etc.	
K2	NI	3-143	Programmed Input	
K3	NI	3-143	Output	
K4	NI	3-143	Binary shift right	
K5	NI	3-143	Decimal shift right· (C3 v C4)	
K5'	NI	3-143	(Decimal shift right)'	
K7	NI	3-143	Decimal shift left· (C4)	
K8	NI	3-143	Multiply	
K8'	NI	3-143	(Multiply)'	
K9'	NI	3-143	(Jump)'	
K10'	NI	3-143	(Jump if Accumulator = 0)'	
K11'	NI	3-143	(Jump if Accumulator is less than 0)'	
K12	NI	3-143	Transfer to storage	
K16	NI	3-143	Reset Entry	G19·F9·S81
K17	NI	3-143	Shift Left. (C4)	
K19	NI	3-143	Any Shift	
K20	NI	3-143	Load	G19·F9·S9
K22	NI	3-144	Minimization	K2·C2
K26	NI	3-144	Any Jump	K9 v K10 v K11
K27	NI	3-143	Detract	
K28	NI	3-143	Multiply or detract	K8 v K27
K28'	NI	3-143	(Multiply or detract)'	K8'·K27'

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
K29	NI	3-143	Minimization	K27·F12'·C4
K30	DI	3-144	Minimization	K50 (K12 v K1·F11')
K31	NI	3-144	Minimization	K3·C3
K33	NI	3-144	Any Input	K2 v K16
K34	NI	3-144	Output to Device #1	K3·C4·F10 –
K35	NI	3-144	Output to Device #2	K3·C4·F11
K36	NI	3-144	Output to Device #3	K3·C4·F12
K37'	NI	3-144	Record Inhibit if Low.	(G17' v C1') G20
K40	DI	3-144	Magnetic Card Read	K40·G17'
K41	NI	3-144	Magnetic Card Write	K41 (C3vC4) G17'·F71'
K42	NI	3-144	Magnetic Card Eject	K42·C1'·G17'
K44	NI	3-144	Magcard Read or Write	(K40 v K41) C1'·G17'
K44'	NI	3-145	(Magcard Read or Write)'	(K40'·K41') v G17
K45	NI	3-145	Magcard Read or Write	(K40 v K41) G17'·C4
K46	NI	3-143	Magcard Read or Write	(K40vK41) C1'·G17'·F10'
K50	DI	3-145	Fast Access Addressed	(F1'vF2'vF3') F4'·F5'·F6'·F7'· F8'·F9'·F10'·F12'
K51	LD	3-148	"Start Light"	G19' (G17' v C2')
K52	LD	3-148	"Reset Light"	G19
K53	LD	3-148	Input #1 Light	K2·C2·F10
K54	LD	3-148	Input #2 Light	K2·C2·F11
K55	LD	3-148	Input #3 Light	K2·C2·F12
K56	LD	3-148	Magnetic Card Light	K44
K57	LD	3-148	Output #1 Light	K3·C2·F10
K58	LD	3-148	Output #2 Light	K3·C2·F11
K59	LD	3-148	Output #3 Light	K3·C2·F12
K60	LD	3-148	Parity Error Light	F20·K22
L1	FF	3-150	Fast Access A Playback	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
L2	FF	3-137	Control Loop Unlace	
L3	FF	3-137	Control Loop Retiming	
L4	NI	3-130	Control Loop Record	
L5	DI	3-135	Fast Access A Record	
L6'	I	3-150	Fast Access A Inverter	
L7'	I	3-150	Fast Access B Inverter	
L8	FF	3-150	Fast Access B Playback	
L12	FF	3-137	Accumulator Unlace	
L13	FF	3-137	Accumulator Retiming	
L14	NI	3-131	Accumulator Record	
L22	FF	3-138	Multiplier Unlace	
L23	FF	3-138	Multiplier Retiming	
L24	NI	3-132	Multiplier Record	
L32	FF	3-138	Multiplicand Unlace	
L33	FF	3-138	Multiplicand Retiming	
L34	NI	3-133	Multiplicand Record	
L48	DI	3-127	Adder A Gate	
L49	DI	3-128	Adder B Gate	
L50	FF	3-126	Carry Flip Flop	
L51	NI	3-129	Adder Output	
L51'	NI	3-129	(Adder Output)'	
L70	Pb		Magnetic Card Information	
L71	Pb		Magnetic Card Information	
L72	MV		Magnetic Card Hole	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
L75	FF		Magnetic Card Clock	
L81	FF	3-139	G. S. & F. A. B. Unlace	
L82	FF	3-139	G. S. & F. A. B. Retime	
L83	NI	3-139	G. S. & F. A. Retimed	
L84	DI	3-136	Fast Access B Record	
L85	NI	3-136	G. S. Record	
L86	Pb	3-151	G. S. Playback	
L86'	I	3-151	(General Storage Playback)'	
P3	DI	3-115	Phase 3	P21•P22'
P21	FF	3-115	Phase Counter	P2 v P3
P22	FF	3-115	Phase Counter	P1 v P2
P30	DI	3-115	Selected Phase Pulse	
Q2'	I	3-146	F8 to F1 Shift	
Q13	I	3-145	Minimization	F9 v F10
Q14	NI	3-135	Minimization (Multiplier Regeneration)	
Q15	NI	3-133	Minimization (Multiplicand Regeneration)	
Q17	NI	3-125	Subtract Gate for Carry Flip-Flop	
Q18	NI	3-125	Add Gate for Carry Flip-Flop	
Q19	NI	3-138	Minimization	K8•C4•F11A
Q20	NI	3-146	Minimization	
Q21	NI	3-122	Minimization	
Q40	NI	3-146	Minimization	K40•C41•F6•L50' (F9vF10) G17'
S7	Switch	3-140	"Start" switch	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
S7'	Switch	3-140	"Start" Switch Back Contact	
S9	Switch	3-140	"Load" Switch	
S9'	Switch	3-140	"Load" Switch Back Contact	
S10			Output Device #1 Busy	
S11			Output Device #2 Busy	
S12			Output Device #3 Busy	
S20	Switch	3-141	"Halt" On -Off	
S21	Switch	3-141	"Start" Switch for 1-Shot	
S22	Relay Contact	3-141	Delay On Warm-Up	
S23	"	3-141	Relay Warm-Up	
S24	"	3-141	Relay Warm-Up	
S25	Switch	3-141	"Reset" Switch Back Contact	
S26	Switch	3-141	"Reset" Switch	
S29	NI	3-134	Input Decode	
S30	NI	3-134	Input Signal	
S31 to S38	Input Contacts	3-134	Input Contacts	
S41 to S48	Inter-vention Switches	3-140	Intervention Switches	
S51 to S58	Input Contacts	3-134	Input Contacts	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
S61 to S68	Input Contacts	3-134	Input Contacts	
S73	I		Magnetic Card Home	
S81	Switch	3-140	Input Device #1 Common	
S81'	Switch	3-140	Input Device #1 Common Back Contact	
S82	Switch	3-140	Input Device #2 Common	
S82'	Switch	3-140	Input Device #2 Common Back Contact	
S83	Switch	3-140	Input Device #3 Common	
S83'	Switch	3-140	Input Device #3 Common Back Contact	
S84		4-50	Input Device #1 Busy	
S85		4-50	Input Device #2 Busy	
S86		4-50	Input Device #3 Busy	
S100	DI	3-146	Output not busy	
T31	FF	3-150	Word Time	
W/1 to W/8	N	3-147	V1-V8 #1 Grid Drive	
W/9 to W/16	N	3-147	V1-V8 #2 Grid Drive	
W/17 to W/24	N	3-147	V1-V8 #3 Grid Drive	

SIGNAL	SOURCE	PAGE	FUNCTION	EQUIVALENCE
W/25	N	3-148	V10 #1 Grid	
W/26	N	3-148	V10 #1 Grid	
W/27	N	3-148	V10 #2 Grid	
W/28	N	3-148	V10 #3 Grid	
W/29	N	3-140	Intervention Switch Net to B Gate	
W/32 to W/35	N	3-149	Row #1 - #4 Gates	
W/36 to W/39	N	3-149	Column #1 - #4 Gates	
W/40	N	3-131	Parity Record in Accumulator	
W/41 to W/44	N	3-149	Column #5 - #8 Gates	
Z1	FF	3-150	Sector Index	
Z2	Shaper	3-150	High Speed Clock	
dZ2	Amp.	3-151	Delayed Z2 Clock	
Z3	Shaper	3-150	Low Speed (Logical) Clock	
Z5	FF	3-151	Sector Address	
Z11	PB Amp.	3-150	Sector Index Playback	
Z11'	I	3-150	(Sector Index Playback)'	
Z12	PB Amp.	3-150	Master Track Playback	
Z15	PB Amp.	3-151	Sector Address Playback	
Z15'	PB Amp.	3-151	(Sector Address Playback)'	

LOAD RESISTOR GLOSSARY

Signal	Resistor To -24V	Resistor To +18V	Location
C1	1.8 K		B11 - ⓐ
C1A		4.3 K	A7 - P
C1'	1.8 K		B15 - X
C2		6.8 K	A7 - ⓔ
C5	1.2 K		A1 - U
C5'	1.5 K		A1 - Y
C10	1.5 K		A8 - F
C10'	3.6 K		A9 - ⓓ
C18	1.2 K		B13 - Z
C20	1.5 K		A9 - W
C20'	1.2 K		B15 - N
C21	1.5 K		A4 - L
C21'	1.8 K		A8 - M
C22	2.0 K		C15 - Y
C22'	1.5 K		A8 - U
C31		4.3 K	A18 - ⓔ
C41	1.2 K		B6 - ⓑ
C41'	1.8 K		B11 - V
C44		5.1 K	C15 - ⓓ
F1	1.5 K		A5 - S
F1A		6.8 K	B15 - ⓔ
F1'	1.8 K		B1 - ⓔ
F1A'		3.3 K	C17 - ⓔ
F2	1.5 K		B1 - B
F2A		3.0 K	A12 - R
F2'	2.2 K		C1 - Y
F2A'		2.4 K	B10 - B
F3	1.5 K		A5 - K
F3A		4.3 K	B17 - K
F3'	2.0 K		C1 - N
F3A'		2.4 K	A1 - ⓓ
F4	1.5 K		C6 - F
F4A		2.7 K	B10 - E
F4'	1.5 K		C1 - E
F4A'		2.4 K	B10 - D
F5	1.5 K		B5 - M
F5A		2.4 K	B10 - F
F5'	1.5 K		B17 - E
F5A'		2.4 K	B10 - J

LOAD RESISTOR GLOSSARY

Signal	Resistor To -24V	Resistor To +18V	Location
F6	1.5 K		A4 - F
F6A		6.8	B15 - J
F6'	2.2 K		B15 - ⓐ
F7	1.8 K		B6 - ⓓ
F7A		2.0 K	B6 - ⓔ
F7'	1.5 K		C17 - T
F8	1.5 K		A8 - Z
F8A		2.0 K	B13 - ⓔ
F8'	1.8 K		C4 - P
F9	1.5 K		A4 - R
F9A		2.4 K	A17 - ⓐ
F9'	1.8 K		A9 - J
F9A'		4.3 K	C17 - Z
F10	1.8 K		C5 - M
F10A		5.1 K	C10 - Z
F10B	4.7 K		B15 - K
F10'	1.5 K		A5 - D
F11	1.8 K		A11 - C
F11A		12 K	C10 - U
F11B	3.3 K		B15 - H
F11'	2.4 K		A9 - ⓐ
F11A'		3.0 K	A17 - U
F12	1.5 K		A5 - N
F12A		5.1 K	B5 - X
F12B	3.3 K		C15 - T
F12'	1.8 K		B5 - S
F12A'		4.3 K	C1 - 14
F13	1.8 K		A6 - X
F13A		4.3 K	A13 - E
F13'	1.5 K		B8 - W
F13A'		3.0 K	B14 - ⓓ
F14	1.5 K		B8 - ⓑ
F14A		5.1 K	C18 - ⓔ
F14'	1.5 K		A6 - ⓑ
F15	2.4 K		A6 - E
F15A		4.3 K	B8 - A
F15'	2.2 K		B14 - ⓐ
F15A'		5.1 K	A15 - ⓒ
F16	1.5 K		A6 - D
F16A		2.4 K	A6 - V

LOAD RESISTOR GLOSSARY

Signal	Resistor To -24 V	Resistor To +18 V	Location
F16'	1.5 K		A8 - Y
F20	1.8 K		B10 - P
F20'	1.2 K		B10 - U
F21	1.5 K		A9 - P
F21'	1.2 K		B6 - L
G17	1.5 K		A9 - E
G17'	1.5 K		B15 - Z
G18	1.2 K		B10 - Z
G18'	1.2 K		A7 - M
G19	1.5 K		C19 - F
G19'	1.5 K		A7 - J
G20		5.1 K	D8 - U
K1		2.2 K	C17 - X
K2		4.3 K	B8 - C
K3		6.8 K	B14 - U
K4		2.4 K	A13 - R
K5		3.0 K	A13 - H
K5'		2.2 K	A8 - P
K7		2.2 K	C13 - ⓒ
K8		12 K	A12 - ⓑ
K8'		2.4 K	A2 - V
K9'		4.3 K	C12 - ⓔ
K10'		2.0 K	C12 - ⓑ
K11'		4.3 K	C12 - ⓓ
K12		2.4 K	C12 - A
K16		3.3 K	C19 - M
K17		2.7 K	A15 - ⓓ
K19		5.1 K	A15 - A
K20		2.2 K	C10 - ⓑ
K22		3.0 K	C10 - X
K26		4.3 K	A8 - H
K27		4.3 K	A15 - ⓔ
K28		3.0 K	A2 - X
K28'		4.3 K	A19 - U
K29		2.7 K	A15 - X
K30	1.2 K		A4 - E
K30'	1.8 K		A1 - N
K31		4.3 K	A18 - F

LOAD RESISTOR GLOSSARY

Signal	Resistor To -24 V	Resistor To +18 K	Location
K33		68 K	C15 - H
K34		4.3 K	C8 - H
K35		4.3 K	C8 - ⓔ
K36		4.3 K	B14 - Z
K37'		10 K	B15 - B
K40	1.2 K		A8 - D
K40'	1.5 K		C4 - U
K41		4.3 K	A6 - B
K42		2.7 K	C12 - Z
K44		12 K	A15 - C
K44'		2.2 K	C12 - X
K45		4.3 K	A9 - U
K46		4.3 K	A11 - ⓒ
K50	1.5 K		C12 - F
K50'	1.5 K		A1 - E
L1	1.5 K		C2 - U
L1'	1.5 K		C2 - Y
L2	1.5 K		C2 - E
L2'	1.5 K		C2 - A
L3	1.5 K		A7 - U
L3'	1.5 K		B8 - P
L4		12 K	A7 - V
L5	1.5 K		D1 - A
L5'	1.5 K		D1 - ⓓ
L6'	1.5 K		D8 - W
L7'	1.5 K		D8 - R
L8	1.2 K		A1 - V
L8'	1.2 K		D8 - E
L12	1.5 K		A6 - ⓐ
L12'	1.5 K		C4 - ⓓ
L13	1.8 K		A5 - U
L13A		2.7 K	A5 - H
L13'	1.5 K		B6 - S
L14		12 K	A6 - ⓓ
L22	1.5 K		A5 - V
L22'	1.5 K		C4 - F
L23	1.5 K		C18 - ⓓ
L23'	1.5 K		A19 - P
L24		12 K	A5 - M

LOAD RESISTOR GLOSSARY

Signal	Resistor To -24 V	Resistor To +18 K	Location
L32	1.5 K		C2 - ⓐ
L32'	1.5 K		C2 - X
L33	1.2 K		C19 - P
L33'	1.2 K		A10 - S
L34		12 K	A4 - H
L48	1.8 K		A19 - ⓑ
L48'	1.5 K		A19 - J
L49	1.2 K		A19 - F
L49'	1.2 K		A19 - Z
L50	1.5 K		A17 - K
L50'	1.8 K		A9 - V
L51		27 K	A17 - ⓓ
L51'		12 K	A17 - ⓔ
Set L81	2.0 K		D6 - X
(Set L81)'	1.5 K		D6 - C
L81	1.2 K		C1 - ⓒ
Reset L81	2.0 K		D6 - W
(Reset L81)'	1.5 K		D6 - B
L81'	1.2 K		C1 - T
L82	1.2 K		C1 - L
L82'	1.2 K		B10 - ⓓ
L83		12 K	C1 - ⓔ
L84	1.5 K		D2 - A
L84'	1.5 K		D2 - ⓓ
L85		3.9 K	A1 - ⓔ
L86'	1.2 K		D8 - L
P3	1.2 K		A1 - F
P3'	2.0 K		C2 - J
P21	1.5 K		C10 - R
P21'	1.5 K		B1 - M
P22	1.5 K		B1 - F
P22'	1.5 K		B1 - L
P30	1.2 K		A1 - T
P30'	1.5 K		A1 - ⓐ
Q2'	1.5 K		B17 - B
Q13		12 K	C15 - X
Q14		12 K	A2 - P
Q15		12 K	A2 - ⓑ

LOAD RESISTOR GLOSSARY

Resistor To

Signal	-24 V	+18 K	Location
Q17		4.3 K	A19 - 12R
Q18		4.3 K	A19 - 6R
A19		27 K	A10 - ⓒ
Q20		8.2 K	C10 - 12
Q21		8.2 K	B13 - 2R
Q40		27 K	C15 - ⓔ
S7	15 K		B11 - ⓑ
S7'	4.7 K		A11 - K
S9	10 K		C10 - D
S9'	15 K		A7 - ⓒ
S20	15 K		C13 - Z
S25	5.1 K		C13 - H
S26	15 K		A15 - M
S29		2.4 K	C6 - 15
S30		27 K	C5 - ⓓ
S73	15 K		A11 - D
S81	3.9 K		C10 - K
S81'	7.5 K		A11 - X
S82	7.5 K		C10 - M
S82'	15 K		A11 - W
S83	7.5 K		C10 - P
S83'	15 K		A11 - ⓑ
S84		6.8 K	A9 - D
S85		6.8 K	A9 - F
S86		6.8 K	A9 - H
S100	1.2 K		A11 - M
S100'	1.2 K		A9 - C
T31	1.5 K		A5 - R
T31'	2.0 K		A6 - W
T31A'	2.0 K		A4 - C
Z1	1.2 K		D8 - D
Z1'	1.2 K		D8 - P
Z5	1.5 K		B5 - K
Z5'	1.5 K		B5 - D
Z11'	1.5 K		D8 - A
Z15'	1.5 K		D8 - J