SENSING.

The purpose of sensing is to ensure that recording and playback of drum pulses are carried out in the correct phase at the right time. Sensing is achieved by moving the respective heads on the radial shoes of their supports.

GENERAL INFORMATION:

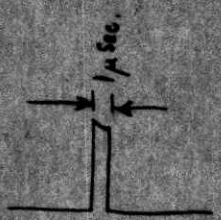
1. Z2 MASTER TRACK IS USED AS A REFERENCE when making sensing adjustments therefore the Z2 head should not be moved.

2. Z2 pulses must be linear to obtain correct sensing

a) Pulse linearity is corrected by adjusting the Schmidt trigger circuit in the playback amplifier.

b) New playback boards do not have a Schmidt trigger and if linearity is incorrect the last two stages of the playback amplifier should be checked.

3. a) Z2 PULSE WIDTH SHOULD BE 1 MICROSECOND and should not exceed 1.3 microseconds.



b) The purpose of the shaper amplifier is to differentiate the pulse and build up power to drive logic.

c) Z2 width adjustment is made with the Amperite delay relay K2 removed to prevent recording. If a pulse is recorded on the drum with a wide Z2 and after adjustment Z2 is narrower it would not erase all the old pulse. The

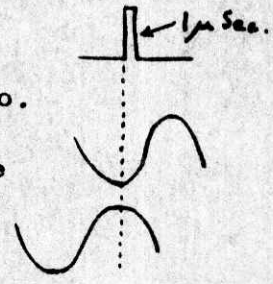
entire drum (except master tracks) would then have to be erased. Erasure may be necessary anyway if Z2 was originally too wide. Adjustment is made with the left trimpot on board D9.

NOTE: If Z2 width is altered, DZ2 must also be adjusted.

4. $\overline{Z2}$ is available on pin U on board D9, but is used only on this board. If $\overline{Z2}$ is to be viewed a probe can be used on D9-U.

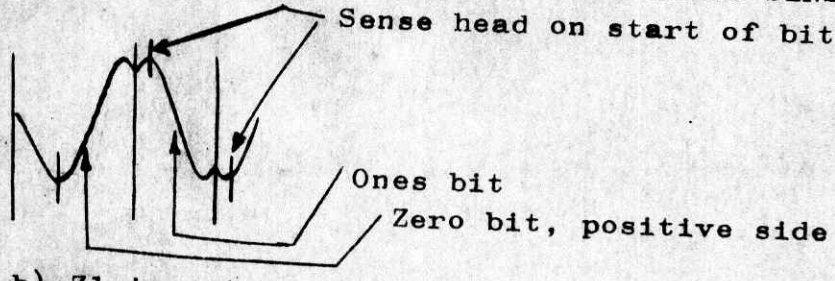
5. Z3 IS ALSO ADJUSTED TO 1 MICROSECOND.

6. It is possible to sense a one for a zero.



7. Z1 SENSING:
Z1 sensing is very important since Z1 CONTROLS THE PHASE COUNTER AND T31.

a) Z1 head is adjusted to sense ones as ones and zeros as zeros. To do this, look for a reversal in the Z1 signal - there is a ones bit every 127 zero bits. IF Z1 REAL RESEMBLES THE PRIME, ZEROS ARE BEING SENSED AS ONES.



b) Z1 is set on the 128th pulse of Z2 and reset on the 129th thus giving 16 evenly spaced pulses around the drum.

c) IF Z1 IS CORRECTLY SENSED, T31 SENSING SHOULD BE CORRECTED AUTOMATICALLY.

MONROBOT XI

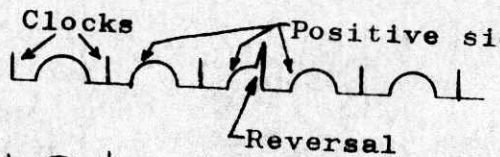
TIMING TRACK RE-SENSING (Z1)

TOP VIEW BOARD D-7

∪ Reset Z I ∪ Set	∪ Reset F.A. "B" ∪ Set	∪ Reset T31 ∪ Set
∪ Reset Z 5 ∪ Set	∪ Reset L81 ∪ Set	∪ Reset F.A. "A" ∪ Set

Monitoring points beneath board D-7

Set:

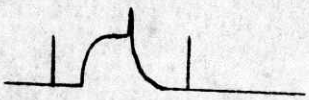


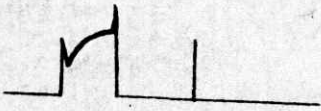

Correct

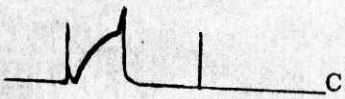

Incorrect


Incorrect

Reset:


Information hanging on after pulse

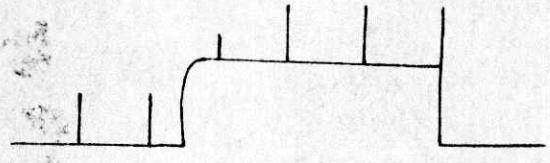

Clock pulse riding up information


Compromise condition

8. OPTIMUM SENSING IS A COMPROMISE:

a) The reset side of the flip flops should be checked after adjustments have been made on the set side, because some reset signals are delayed by inverters through which they pass. This is particularly true in the case of fast access A.

b) When information is high for more than one clock pulse, the pulse that set the flip flop will have the lowest amplitude. This is because some current flows to set the flip flop.



9. Separate ground references apply to the playback and the matrix boards. The playback boards use the inner strip on the D rack whilst the matrix boards are grounded to the outer strip.

10. PRECAUTIONS TO BE EXERCISED WHEN VIEWING DRUM TRACKS.

a) Always look at the drum playback at the output of the 1st stage of the playback amplifier to isolate the track in the event of a charge being present on the probe. General storage tracks may be viewed at the output of the pre-amplifier.

b) The above precaution is primarily for master tracks. If the other tracks are accidentally erased or "clobbered" they could be replaced. Z2, Z1 and Z5 cannot be replaced.

c) If there is no output from the first stage of the playback amplifier, and it is necessary TO LOOK AT THE OUTPUT OF THE HEAD TAKE THE FOLLOWING STEPS:-

1. Turn computer off.
2. Place jumper wire across the head leads.
3. Place probe on the lead from the head.
4. Remove jumper.
5. Turn on the computer.

This ensures that the probe is discharged. To remove the probe it is advisable to reverse the above procedure.

SENSING PROCEDURE WHEN ALL TIMING IS INCORRECT:-

1. Z2 SENSING:- Before switching on the machine lock down the Z2 replay head.

A. Check the Z2 head clearance using Mylar strip.
   1. Blow out dust.
   2. Examine head closely.
   3. Check General Storage head clearance.
   4. Check Fast Access A & B replay heads together - move drum to low spot.
   5. Check Fast Access A & B record heads together.
   6. Check master track head clearances. If clearance is too great but replay signals are satisfactory do not adjust head clearance.

Amplitudes at 1st stage of playback amplifiers:-

Z2 - 1 volt.
Z1 - .5 volt.
Z5 - .5 volt.

B. Remove Amperite (K2 relay) and turn on power.

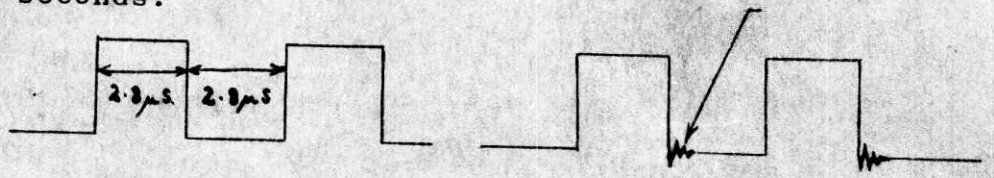
C. Scope trigger - internal synch.
time base - .5 millisec or adjust to get full drum revolution.

D. Monitor Z2 output from 1st stage of amplifier.

1. Check amplitude is about 1 volt.
2. Expand trace and look for blivets.

E. Moni... at playback amplifier output (D10-W).

1. Care ... t be taken not to put probe on input pin which is also a white wire. This would discharge the probe across the head.
2. Measure output voltage - about 8 volts. (6 volts would be sufficient).
3. Check width of ones and zeros pulses. These should be ...e same at mid point. If any great difference ...ists check the final two stages of the amplifier. (Schmidt trigger on early models). Pulse width should be approximately 2.8 micro seconds.



F. Check output of shaper amplifier.

1. Width of pulse at mid-point is 1 microsecond.
2. To adjust pulse width, use left trimpot on board D9. Always ensure that K2 relay is removed when making this adjustment.

   RANGE: 1 to 1.3 microseconds.
3. Refer C.R.O. to true ground then check Z2 which should be ½ volt below ground at peak, although it can be as much as one volt. The level rises on logic rack through lead inductance.

2. Z1 (SECTOR INDEX) SENSING:-

A. Monitor 1st stage of playback amplifier.

1. Check that signal amplitude is about ½ volt.
2. Expand trace and check for blivets.
   (C.R.O. settings 500 milliseconds/cm, 0.05V.)
   adjust variable time.

B. Monitor output of playback amplifier with C.R.O. vertical setting of 0.2V/cm.

1. Check pulse shape.
2. Measure voltage - about 8V for logic level.

C. Monitor trigger circuit of flip flop for sensing. This is the only point at which the clock pulse can be seen superimposed on the information. To monitor this point fasten a stiff piece of insulated wire to the "look loops" beneath board D7 playback amplifier.

1. Monitor set side and set positive side of zero pulse midway between clock pulses. Check reset side after making adjustments.

2. Z1 is set on the 128th Z2 pulse and reset on the 129th to give 16 pulses per drum revolution.

3. If Z1 is correctly sensed, T31 and the phase counter will also be correct.

4. If Z1 looks like the prime, zeros have been sensed as ones and Z1 must be re-sensed.

D. The output of the flip flop (D7-E) shows all lows except where ones are sensed.

3. Z3 SENSING:- Monitor output of shaper amp. (D9-A)

A. Check shape and width - 1 microsecond at centre.

B. Refer scope to true ground and check Z3. Level should be 0.5 below ground. Z2 should be similar. If the level were not kept low an inductive "kick" might trigger flip flops.

4. T31 CHECKING:-

A. Monitor T31 output to ensure its presence.

B. Monitor the trigging circuit as a check on Z1 sensing.

5. PHASE COUNTER:-

Check the relationship of P21 and P22 to each other using T31 as a reference. (Use T31 on positive external synch.) This check also shows if T31 has its correct phases.

6. Replace Amperite (K2 relay).

7. FAST ACCESS A SENSING: Everything going into or coming from the computer goes through this loop. It is called the arithmetic loop.

A. ROUGH ADJUSTMENT FOR CORRECT DELAY: ~~Remove K2.~~

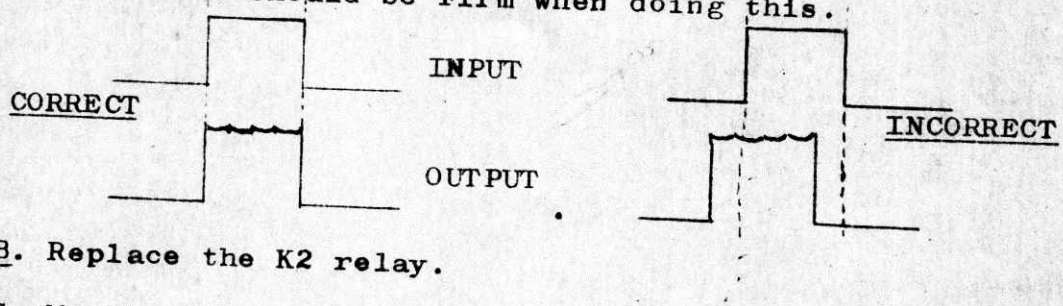
1. Record T31 into L5 double inverter by removing taper pin from B2-K (input to L5) and run a jumper wire from T31 (A5-R) to B2-K. This records T31 in all phases of fast access A.

2. Refer the C.R.O. to the rise of T31 then monitor the output of the OR gate of F.A. "A" record gate on the pin removed from B2-K.

ADJUST E4 HEADS ONLY
NEVER ADJUST E3 HEADS

3. Head adjustment - NEVER ADJUST RECORD HEAD - adjust replay head only. If the record head is ever to be moved, erase the track under it before moving the head. If this is not done and the head is moved to a new position the previously recorded information cannot be erased.

4. Sensing: The output should correspond to the input. If it does not correspond, tap the replay head with a hammer until input and output match. Screws should be firm when doing this.



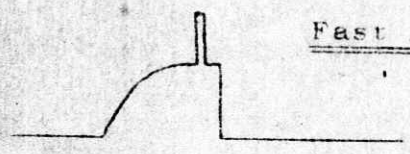
B. Replace the K2 relay.

C. Monitor each phase through the view box.

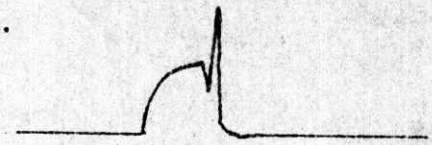
D. Final adjustment is achieved by monitoring the pulses at the loops beneath the playback amplifier.

1. Tighten head mounting screws.
2. Set side is adjusted on information or positive swing of zero.
3. Reset side usually requires a compromise adjustment with clock pulses just at the foot of the rise in information.
4. Recheck set side after compromise reached on reset pulses.
5. Check each loop on control box for a T31 logic bit.
6. Erase fast access A track.

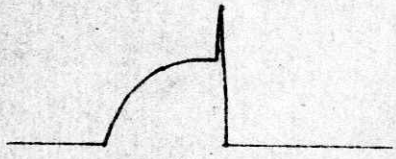
Fast Access A.



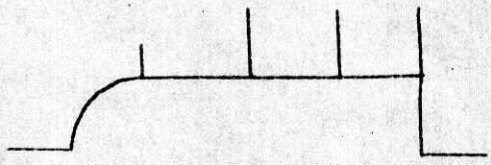
Tap head counterclockwise



Tap head clockwise



Desired adjustment



All four phases

8. FAST ACCESS B. SENSING:

A3-H

A. Remove pin in [illegible] (L84) and force T31 into taper pin socket. T31 is available at A5-R. Always turn machine off before removing or replacing pins. The pulse is monitored at the pin removed from A4-H.

B. Proceed as for fast access A.

C. One shot V000 V001 and V002 V003 through the shift register whilst viewing the accumulator. See that each has a pulse at T31 time.

D. Erase fast access B.

9. Erase all general storage tracks then proceed to sense the sector address track (Z5). When Z5 is correct the general storage tracks are sensed as detailed later.

10. Z5 SECTOR ADDRESS.

A. Preliminary inspection: Monitor 1st stage of playback amplifier. Amplitude should be 0.5 Volts. Adjust C.R.O. to give full drum revolution on screen and check for blivets. Z5 may be monitored on pin B5-K.

B. Sensing:-

1. Programme: 000 V0V03000
   1st ext. synch: C4.K12 or use F16.C4 (B9-T)
   2nd ext synch: C41.K12 or use F16.C4.T31(A5-R)

2. Start programme and use 1st trigger and line up fall of sector 15 with fall of trigger (adjust C.R.O. with 1st ext. synch to view same pulse). Monitor Z5 replay (B5-K) and move Z5 head for rough adjustment.

3. Use 2nd ext. synch for fine sensing. Recheck rough adjustment by monitoring Z5 replay. Expand reference pulse on C.R.O. and check the flip flop set trigger for fine sensing.

11. GENERAL STORAGE SENSING:-

1. Check all tracks for physical damage.

   A. Programme (one shot) V010, V014, V019, V01U.

   B. C.R.O. Trigger with T31.
      Time base adjusted for 1 drum revolution.
      Ground probe on shield ground wire on lower part of board D-17.

   C. Monitor output of pre-amp.
      Amplitude - 180 to 200 millivolts (.2V)
      Check for blivets and for sectors with no information recorded. Include dead registers when checking.

      NOTE: When checking playback use a short lead on probe and ground probe clip to playback board ground. (See P3-9).

The amplitude at the output of the head should be 8 to 15 millivolts.

2. Check DZ2 width, it should be 3 milliseconds. Whenever Z2 master clock width is changed DZ2 adjustment should be checked. Do not adjust DZ2 until sensing is checked.

3. Record known information in all four phases of a pre-chosen track. Do not erase the track for this check.

   Programme: T010T011, T012T013 Head 5

   Information: in accumulator 00007777 Bank 2(E2).

4. Sensing check - replay known information.

   A. Programme: 000 V0103000

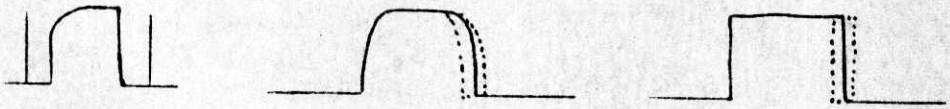
   B. C.R.O. trigger: 1st T31 to look at accumulator.
   2nd C4.F16 (B9-T)

   C. Monitor accumulator to ensure that correct information is being replayed (1st trigger). If the information is correct, sensing must be almost correct and should need only fine adjustment.

   D. Monitor L81 trigger circuit (2nd trigger). Only one phase will be played back and seen at this point because of P30.
   Check sensing: Note that the zero pulse should be midway between two clock pulses.
   Since the fall of P30 is irregular, the information pulse fall may also vary. Monitor the sensing on the rise of the pulse.
   A push pull non-inverter is used for L81 trigger because P30 has slow rise and fall times. The 'P'

circuit has rapid rise and fall characteristics and improves pulse shape.

Correct sense P30 pulse "P" circuit output



NOTES:-

A. There are some registers that are not addressable and these require K50 to be held high for information to record in them. These registers are known as dead registers and are located in 000 to 006.

B. If a track is clobbered it must be erased. After erasure enter the programme to record in all registers ofgeneral storage so that no sector is missed on the erased track. Include dead registers by holding K50 high. This is necessary because the location of registers is staggered.

C. "OR" gates can be held high by grounding the output. Never try to hold an OR circuit low.
AND gates can be held low by using - 6V on the output. Never try to hold the output of an AND gate high.

D. Check drum base, lower right, to ensure that there is a wire between the base and the ground board (the sheet metal strip on base of computer). If there is no wire install one. Without the wire noise can be recorded on the drum.

5. ADJUSTING GENERAL STORAGE SENSING:

A. Erase preselected track - Head 5, Bank 2 010

B. Record know information in 010 (See step 3 previous page.) Use same procedure.

C. Replay known information to check sensing.

Programme: 000 V0103000

Trigger: 1st. T31 to look at accumulator and full drum.

2nd. C4.F16 (B9-T)

Monitor output of preamplifier. Output should look like this:-

Sector 1 2 3 4

Check accumulator for correct playback.
Monitor trigger circuit of L81 with C4.F16 as external synch. to C.R.O. P30 allows only one of the four phases to be seen.
Adjust rise of DZ2 for earlier or later recording.

NOTE: Transients occur in continuously running programme while playback switch is not operating. Playback switch operates when we are reading - mostly in C4.

D. Record, with new adjustment, 2 sectors later. T030T031, T032T033 with same information.

E. 1. Replay is checked at output of preamplifier with T31 as trigger to C.R.O.

Sector 1 2 3 4

2. Monitor L81 trigger circuit.

Programme: 000 V0303000

Trigger: C4. F16 (B9-T)

Check sensing.

Compare with first sector.

E. If additional adjustment is necessary, continue procedure by recording two sectors later. (050, 070, 090, etc.) until sensing is correct.

6. When sensing adjustments have been completed:-

A. Erase all general storage tracks.

B. Record in all registers.

1. This to eliminate amplitude changes when recorded ones or zeros must completely charge the trigger capacitor rather than just add to its charge.

2. Programme 1:

```
000  T007V000
001  X003T000
002  30000000
003  00010000
```

NOTE: After this programme has run its course hold K50 high, address 000 to 006 and enter information into these dead registers. Dead storage registers are located on tracks addressed by 010 and 100

Programme 2: With K50 held high enter

```
000 V003T004
001 V000X003
002 T0003000
003 00000001
```

3. By holding K50 high, information goes to dead registers instead of Fast Access "A" and "B". This is done by grounding the output of the "OR" gate at pin C5-P. The pin need not be removed.

4. When the programme has recorded in all registers it is self destructive as it reaches programme registers.

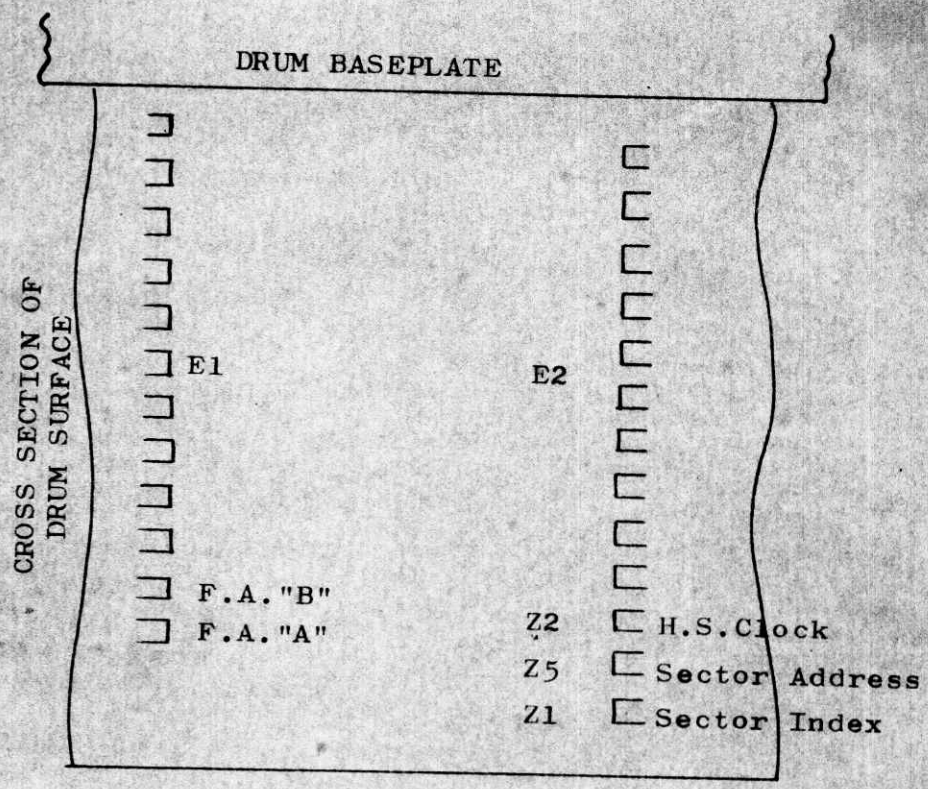
12. SELECTION MATRIX:

A. Checking selection of column amplifier:-

1. One shot V010 V014 V018 V01U
   Each instruction chooses a column amplifier.
2. Check input and output of selected column amplifier.
   a) If selection is correct output will be high (Zero)
   b) If selection is not being made output tends to - 24V.

B. Checking selection of row amplifier:-

1. One shot V010 V110 V210 V310
2. Check input and output of selected row amplifier
   a) If selection is correct output will be high (0.5V)
   b) If selection is incorrect output will tend to + 18V.



TRACK POSITIONS AND HEAD INTERLACE ASSEMBLY ON DRUM

PLAYBACK CIRCUIT (PB AMP)

The playback circuit (Fig. 430) is used to amplify the low millivolt level head signals to logical 6 volt level. It includes a head damping resistor of 470 ohms which is large enough to only slightly degrade the resolution of the head. When used on the higher millivolt information from the general storage pre-amp a non-linear limiting net is inserted in front of the first stage to compensate for head to head variation in playback (Fig.431). Two amplifiers are mounted on one printed board.

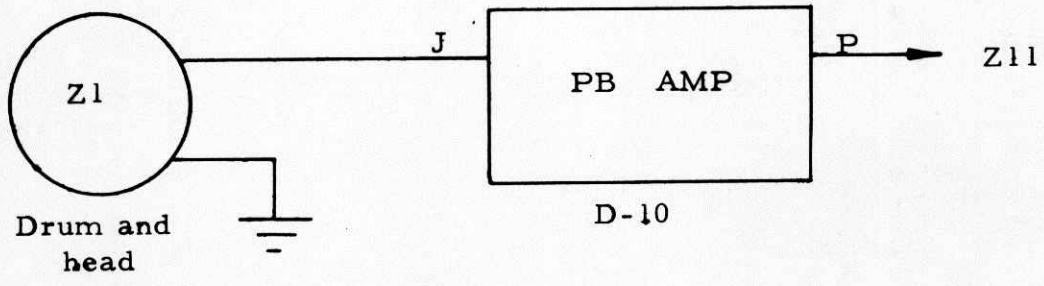


FIGURE 429 PLAYBACK AMPLIFIER SYMBOL

Refer to the schematic (Fig. 430). The first stage of the amplifier is a common emitter connection. The DC operating point is approximately 6 ma (3K to + 18) Ie and the DC voltage at the collector should be approximately -8 volts DC, $\pm$ 20%. The AC gain of the first stage is unpredictable because such a low value of emitter resistor (10 ohms) is necessary to have sufficient gain at the lower input level. Increasing this resistor increases the maximum allowable input level. The nonlinear load, which also affects gain, will be described later. The AC signal at the collector of the first stage should be an approximate replica of the input signal voltage, amplified on the order of 40 to 80 times, 180° phase reversed with an additional delay of not more than one microsecond, and possible compression at the peaks. Approximately 1 db of attention of the clock frequency with respect to the change bit frequency can be expected.

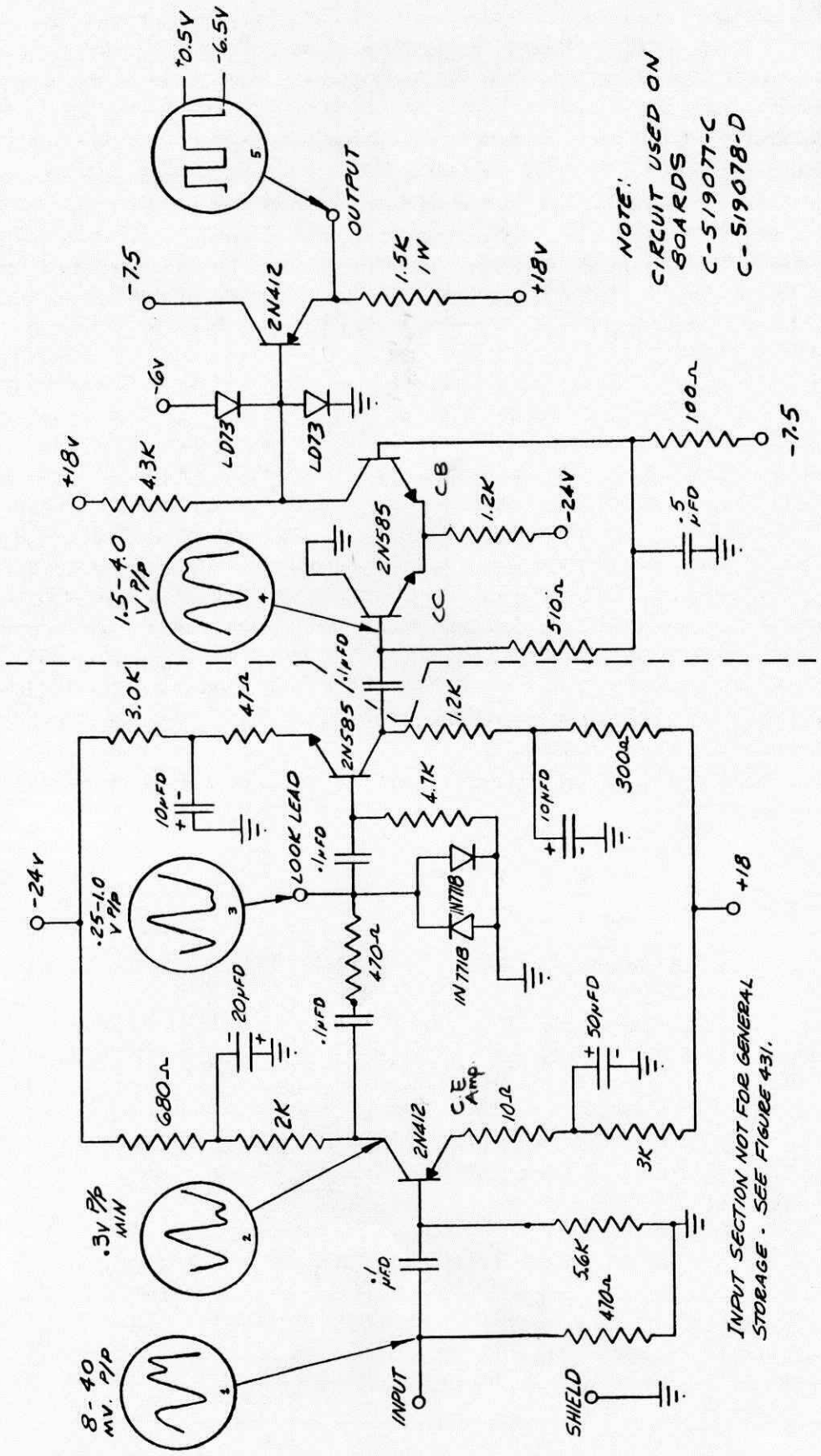


Fig. 430 PLAYBACK CIRCUIT DIAGRAM

The second stage is a NPN common emitter connection whose input is AC coupled to the output of stage one through a voltage limiter. These 1N771B diodes present a non-linear load to the first amplifier and prevent peak to peak amplitudes in excess of one volt from being introduced to the second stage input. The voltage gain of the second stage is well controlled at approximately 6 by the 47 ohm emitter resistor. As a result, the maximum output level of the second stage is predictable and limited to safe values for the input of the next stage. The AC signal at the collector is again in phase with the output from the head but may be delayed as much as one microsecond. A nominal DC emitter current of 8 ma places the collector voltage of the second stage at approximately plus 6. 0 volts.

The next stage is a two transistor current switch which is AC coupled to the second stage output. Under no signal conditions the base voltages of both transistors are controlled by the -7. 5 volt supply and the output is not predictable. The injected playback signal forces the base of the first transistor positive and negative with respect to the second base which is still fixed at the supply level. When the driven base is positive with respect to the supply, the first transistor will provide the current required by the 1. 2K ohm resistor to -24 volts. This holds the second transistor off and its collector will rise to the upper clamp level of plus . 5 volts. When the driven base is forced negative the first transistor is forced off and the 1. 2K ohm current source turns the fixed base unit on. The collector drops to the lower clamp level, approximately -6. 5 volts. Note that this clamping action is essential in preventing saturation of the fixed base transistor (1. 0 volt VCB). The AC signal at the driven base should be positioned approximately symmetrically around the DC level of the voltage at the fixed base.

The final stage, is a common emitter follower which needs no further description.

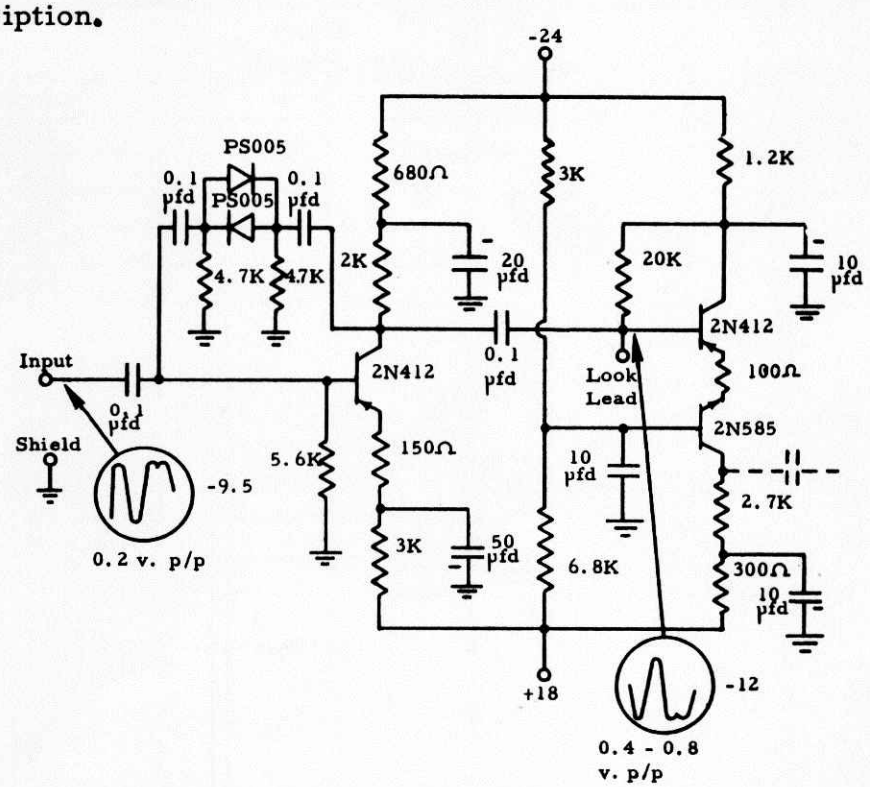


Fig. 431 General Storage Input Section

The general storage playback amplifier uses the general storage input section Fig. 431 in place of the input section shown in Fig. 430.

The first stage is a grounded emitter amplifier, which provides voltage and power gain to the signal and includes a circuit to give a degree of automatic gain control. At the low levels present the PS005 diode pair decreases in impedance as signal level increases. This provides more negative feedback on larger signals from the general storage pre-amp and keeps the first playback stage level within design limits.

The second stage is a grounded collector amplifier. This stage provides current gain and matches the high output impedance of the first stage with the low input impedance of the next stage. The third stage of the general storage input section is a grounded base amplifier, which provides sufficient voltage gain to the signal to drive the two transistor current switch which already has been described.

Typical ranges of amplitudes at various points in the amplifier are shown on the drawings (Figs. 430 & 431) except on the output of the first stage where only a minimum is given. The values shown allow for "worst case" components so any signal not falling within these limits is reason for investigation.

When the input information is continuous (ones or zeros), the dissymmetry of the final output square wave should not exceed 10%, measured at the points where switching commences. The dissymmetry in the area of change bits is usually due to head resolution but should not be increased more than 10% by the amplifier.

Board Location	Input	Output	Signal Designation	Name
D10	J	P	Z11	Sector Index
D10	ⓑ	W	Z12	Master Clock
D11	J	P	L6	FA "A"
D11	ⓑ	W	L7	FA "B"
D12	J	P	Z15	Sector Address
D12	ⓑ	W	L86	General Storage

POWER	
Pins	Power
A, ⓚ	Ground
E, U	-24
C, ⓗ	+18
ⓔ	-7.5
5 Y	-6 Ground (High Level)

Fig. 432 PLAYBACK CIRCUIT PIN CONNECTIONS

THE GENERAL STORAGE PLAYBACK PRE-AMPLIFIER

Playback from the selected head is directed to the general storage pre-amp located on the same board as the rest of the matrix. The gain of this stage produces a signal large enough to overcome the noise introduced in transmission to the playback amplifier from the weakest inputs of about 4 mv. Stronger inputs produce larger outputs which are then limited by the special input net of the general storage playback amplifier forcing the signal on the first stage of that amplifier to fall within design limits.

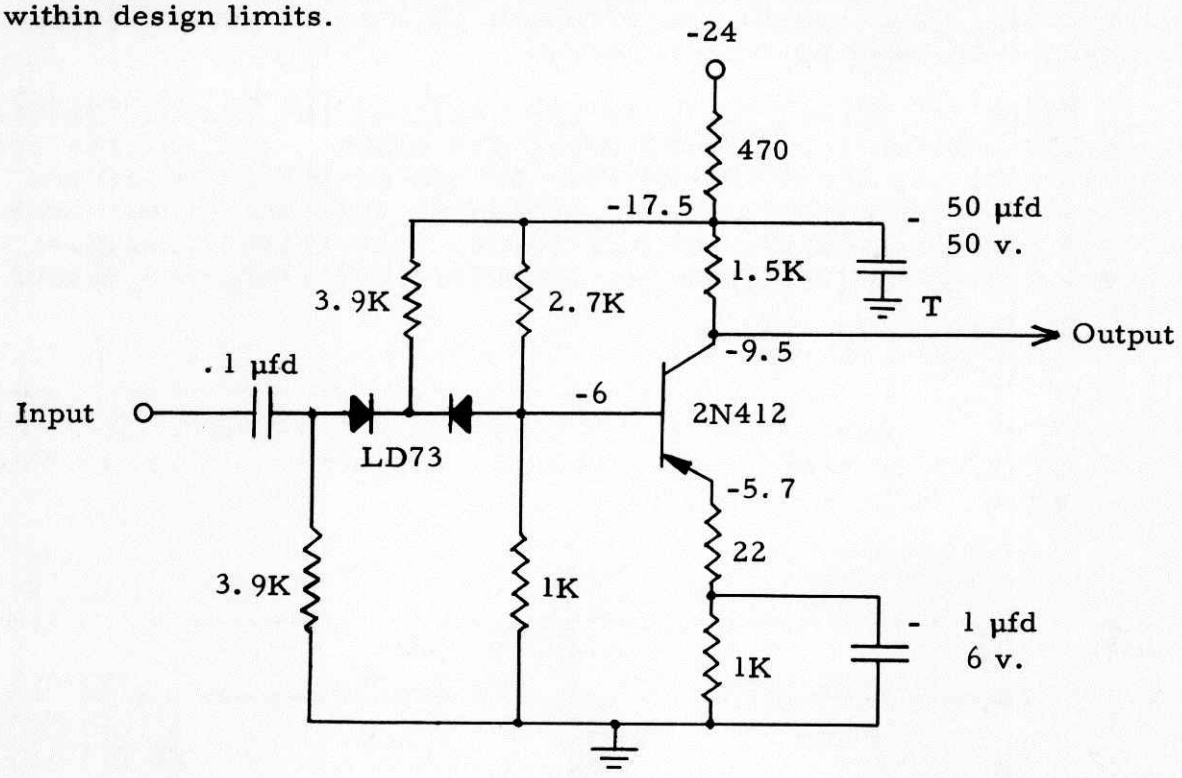


Fig. 440 GENERAL STORAGE PLAYBACK PRE-AMPLIFIER

The pre-amplifier (Fig. 440) is a single class A stage with a nominal emitter current of 6 ma. The base is held at -6v by the input divider (1K and 2. 7K) which also provides 1. 5 ma forward bias current to one of the LD 73 limiting diodes. The other diode is similarly held on by the 3. 9K to ground. The 'input' terminal is attached to the playback winding of the selection transformer. The millivolt level playback signals cause current variations which pass right through these diodes to the transistor base. Volt level signals, however, will cut off one or the other diode depending on polarity and the current flows through a 3. 9K resistor. The result is to limit the voltage excursion on the base to 3V P-P when switching transients and record pulses are in the matrix transformer. Unless this is done the recovery time of the playback system would be too long to pass information located with minimum access.

The 1K emitter resistor establishes the DC operating point. The 1 ufd capacitor is required to provide an AC ground and prevent loss of gain.

RECORD CIRCUITS

The computer uses the record circuits to provide the proper drive to the recording heads under the control of the logical information to be recorded, a record gate, and the clock. A record board consists of two identical record circuits. Each half of the record board drives half of the recording head. Since the windings of the two halves of the record head are 180° out of phase, a pulse generated in one half of the board will cause the field to build up in the opposite direction. Thus one of the circuits is used to record ones and the other is used to record zeros.

There are three inputs to each half of the board. The inputs are information, record gate, and clock. The information supplied to the zeros record side of the record board is the inversion of the information supplied to the ones side. Each record circuit consists of four parts: the trigger circuit, record one-shot, complementary symmetry amplifier, and output stage.

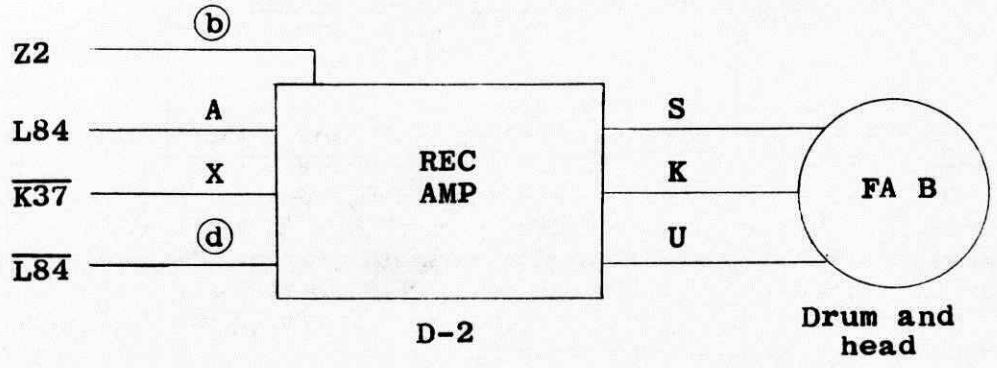


FIG. 433. RECORD CIRCUIT SYMBOL

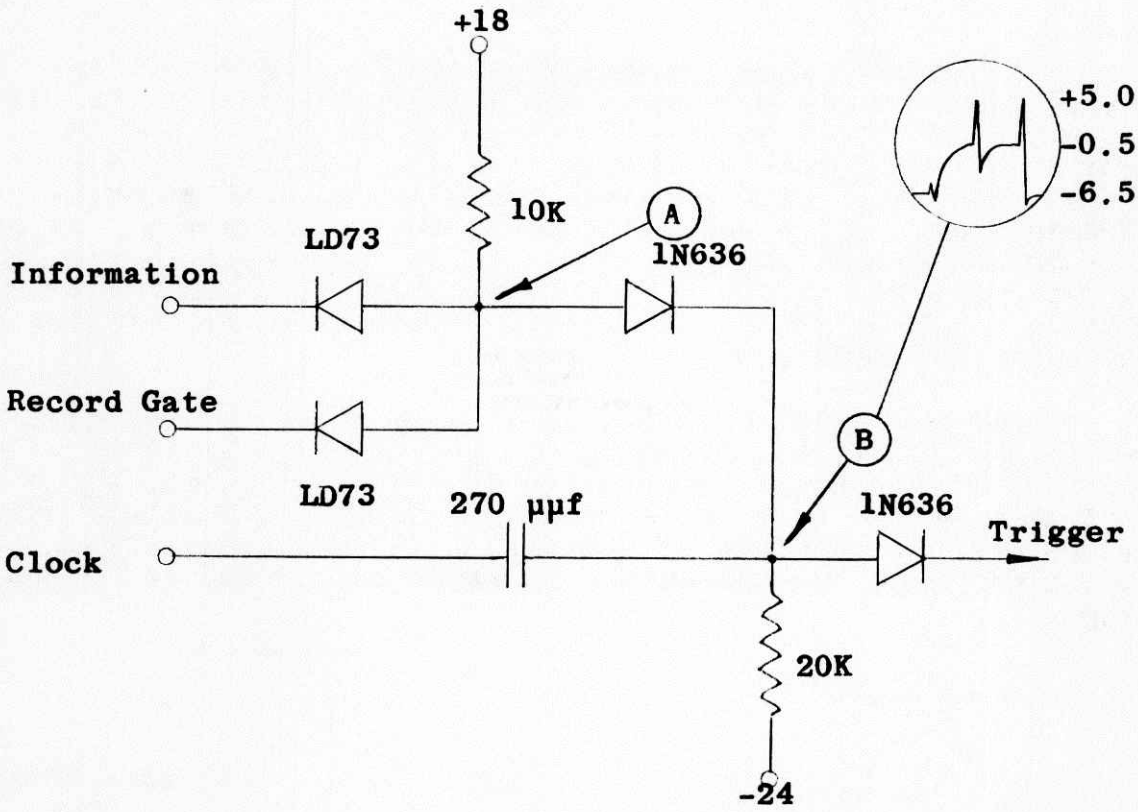


Fig. 434 RECORD TRIGGER CIRCUIT

When either the information or the record gate is low, point A is held at -6 volts and point B will also be -6 volts. If both the record gate and the information are high simultaneously, point A is allowed to rise to zero volts. Point B also rises to zero volts charging the condenser through the 10K resistor and the internal impedance of the driving circuit. During this time it is assumed that the clock is low (-6).

The clock will not arrive until after the information has been high long enough to charge the capacitor. When the clock arrives, the voltage on the capacitor is added to the clock voltage and causes point B to rise above ground towards about +5 volts. The record one-shot requires a trigger which is a few volts positive so this rise is sufficient to trigger the one-shot.

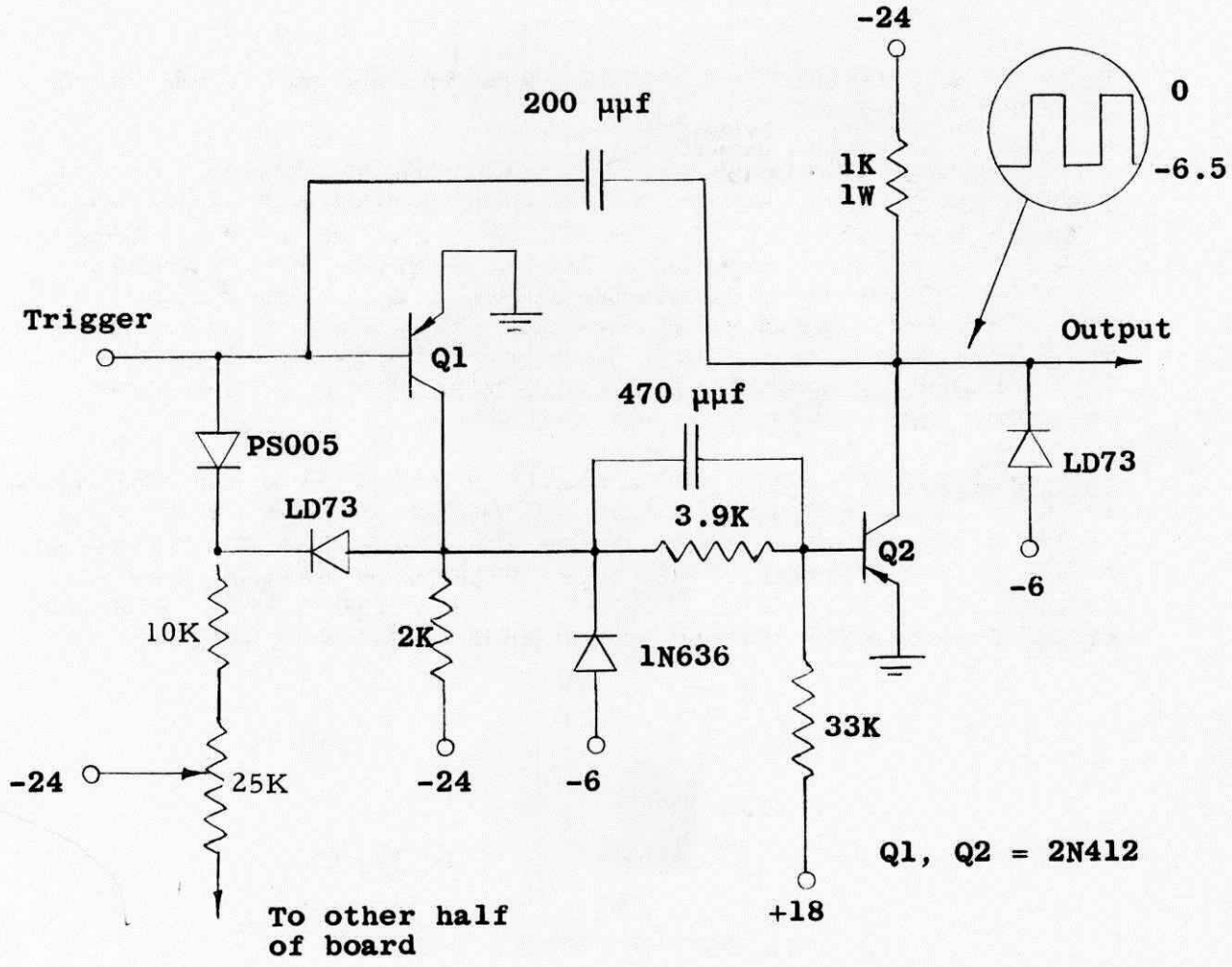


FIG. 435. RECORD ONE SHOT

The circuit that generates the actual record pulse is a monostable multivibrator. In the stable state, Q1 is turned on and is held on by the -24 volts connected to its base through the 25K trimpot, 10K resistor, and PS005 diode. This clamps the collector of the transistor almost to ground. Q2 is kept turned off by the +18 volts connected through the 33K and 3.9K voltage divider. Since one end of the 3.9K resistor is held at ground, the base of Q2 is held slightly positive keeping it turned off and the output is, therefore, clamped to -6 volts.

When the trigger occurs, the base of Q1 is driven positive, turning the transistor off. This causes the collector to go more negative until it is clamped at -6 volts by the diode. This voltage is transmitted to the

base of Q2, turning it on and causing its collector to be clamped to ground.

The positive rise in the collector voltage is transmitted to the base of Q1 keeping it turned off after the trigger goes away. The circuit will maintain this state until the 200 mmf capacitor has discharged sufficiently to allow Q1 to turn on again (about 1.5 microseconds). At that time, the circuit regains its stable state and will hold that state until another trigger occurs. The 25K trimpot allows for pulse width matching of the two circuits that comprise a record board.

The output from the circuit is taken from the collector of Q2. After a trigger, the collector voltage of Q2 will rise to ground and remain there for about 1.5 microseconds. which is determined by the discharge time of the feedback capacitor. After that interval, the voltage will drop to -6 volts and will remain there until the next trigger.

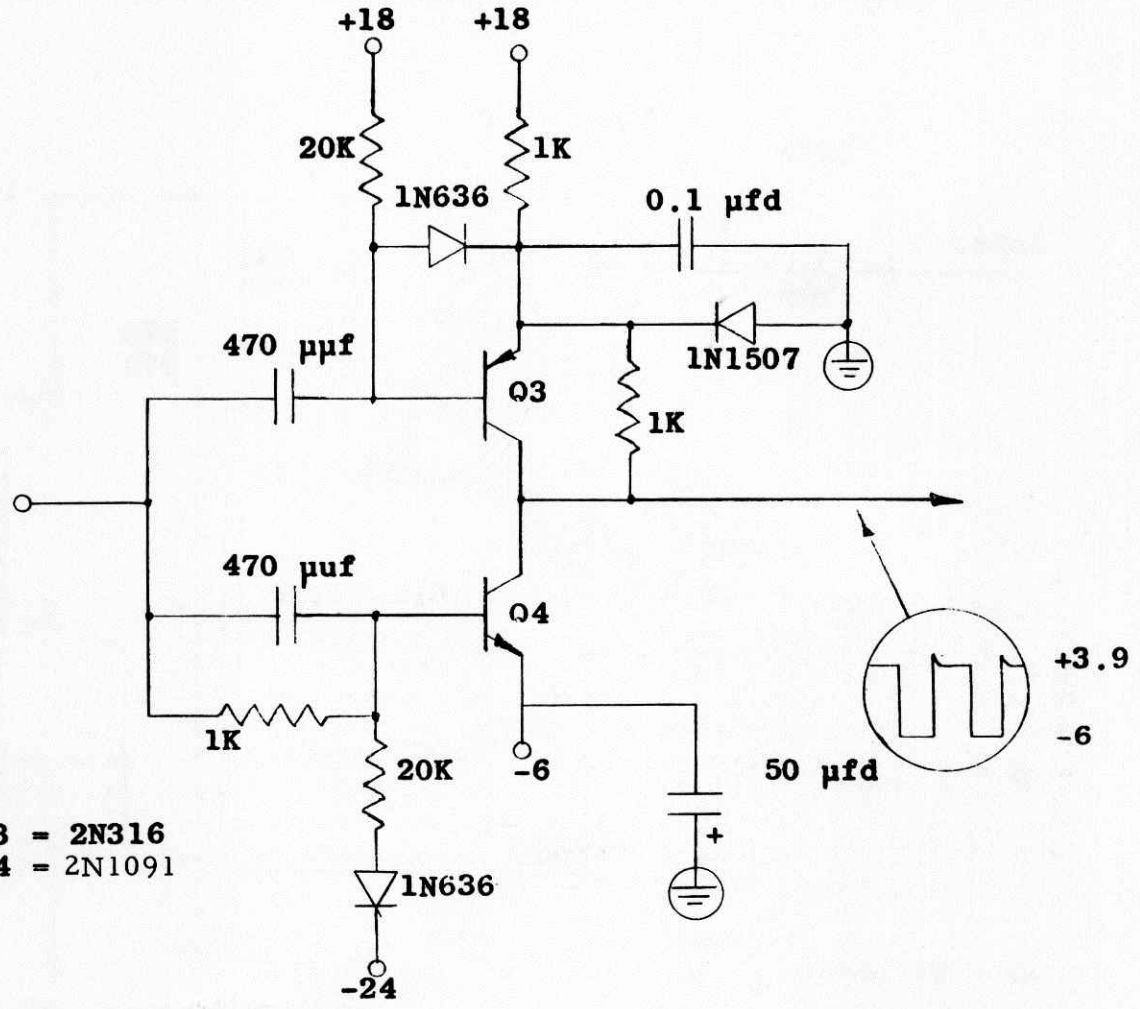


FIG. 436 RECORD COMPLEMENTARY SYMMETRY AMPLIFIER

The next stage is a complementary symmetry power amplifier. When the input is at -6, as it will be any time there has been no trigger, Q4 is kept turned off by the 1K and 20K voltage divider. The emitter voltage of Q3 is maintained at +3.9 volts by the 1N1507 zener diode Q3 is kept turned off by the forward voltage drop of the 1N636 diode. When a trigger occurs, the voltage on the input rises to 0 volts which turns on Q4. Q4 clamps the output to -6 volts. After a short interval, the output of the one-shot goes low. This turns off Q4 and turns on Q3, bringing the output voltage up to +3.9 volts. After the coupling capacitor, that is in the base circuit of Q3 charges, Q3 turns off. The output remains at +3.9 volts because of the connection to the Q3 emitter through the 1K resistor.

The last stage in the record circuit is the output stage. This stage provides the record head with the .5 ampere, 1.5 microsecond pulse needed for recording.

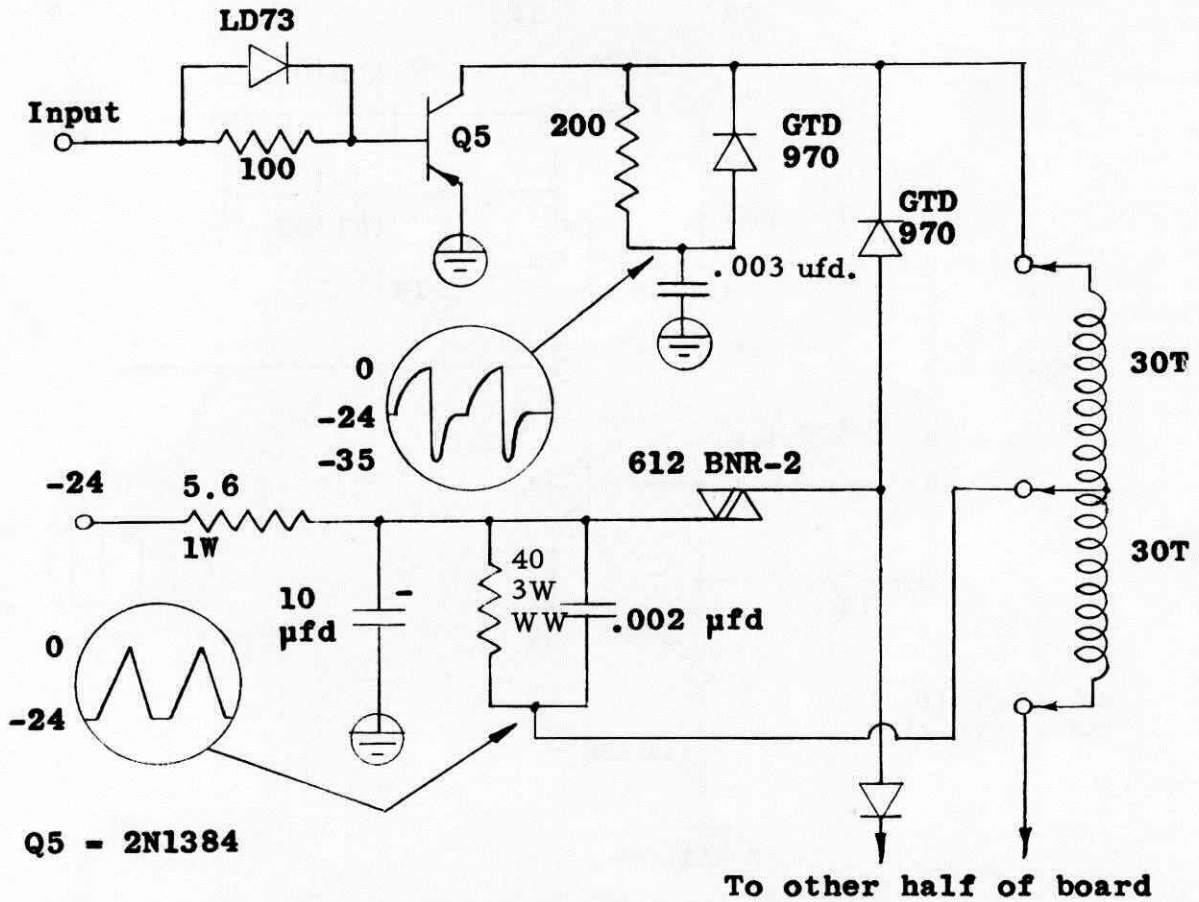


FIG. 437 RECORD OUTPUT STAGE

After a trigger has occurred, the input to Q5 goes low (-6 volts). The base of Q5 will be slightly negative turning the transistor on and causing the collector of Q5 to rise from -24 volts to ground. Current then flows through Q5, one half of the record head, and the current limiting resistor to the -24 volt record supply. This current is the record pulse. When the interval is over, the input to the base of Q5 goes to +3.9 volts. The transistor turns off causing the current flowing through the record head to cease, terminating the record pulse. The collector of Q5 at this time will go to approximately -35 volts because of the inductive kick of the head before returning to -24 volts.

The 33 ohm resistor in the general storage record circuit controls the maximum record current. The additional resistors, diodes, and varistor are in the circuit to provide damping and thus control the transistor peak power dissipation.

There are three record boards used in the computer. They are located in board locations D1, D2, and D19.

Signal	Pin
Information	A
Information'	(d)
Record Gate	X
Clock	(b)
Record Ones	S
Record Zeros	U
Record Center Tap	K
-6	(k)&P
Record -24	M
+18	(f)
-24	(j)
Ground ⏚	(h)
Ground (⏚)	Z

FIG. 438. RECORD BOARD PIN CONNECTIONS

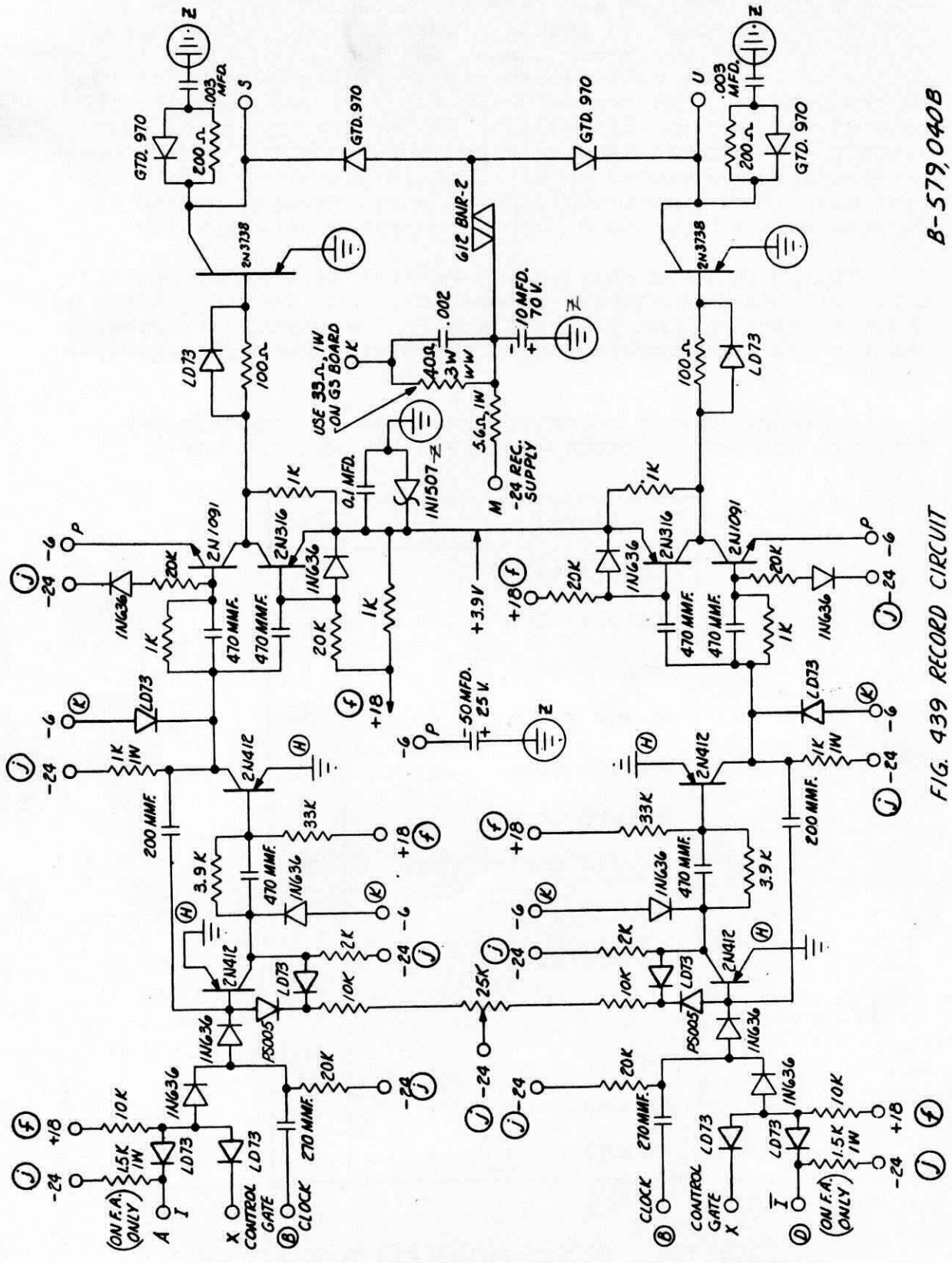


FIG. 439 RECORD CIRCUIT

B-579,0408

REV. 8-31-64

THE SHAPING AMPLIFIER

Two shaping amplifiers are in the computer to produce the logic clock (Z3) and the record rate or high speed clock (Z2). They reform the low power square wave master track playback (Z12) into the high power pulse trains which are the clocks. The amplifiers are located on board D-9 with the dZ2 circuit. They share a -1v level and a specially filtered -6v level both generated on board D-9 (points XX and YY in Figs. 442 and 443).

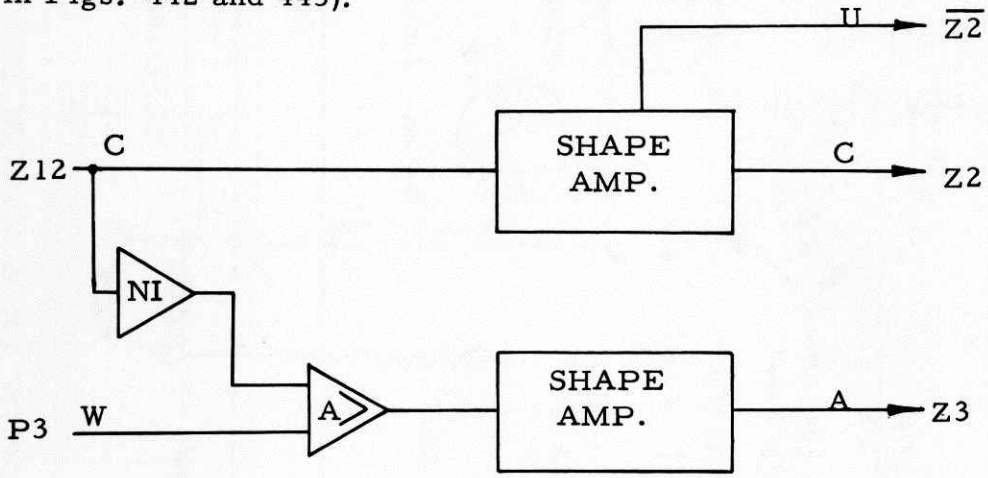
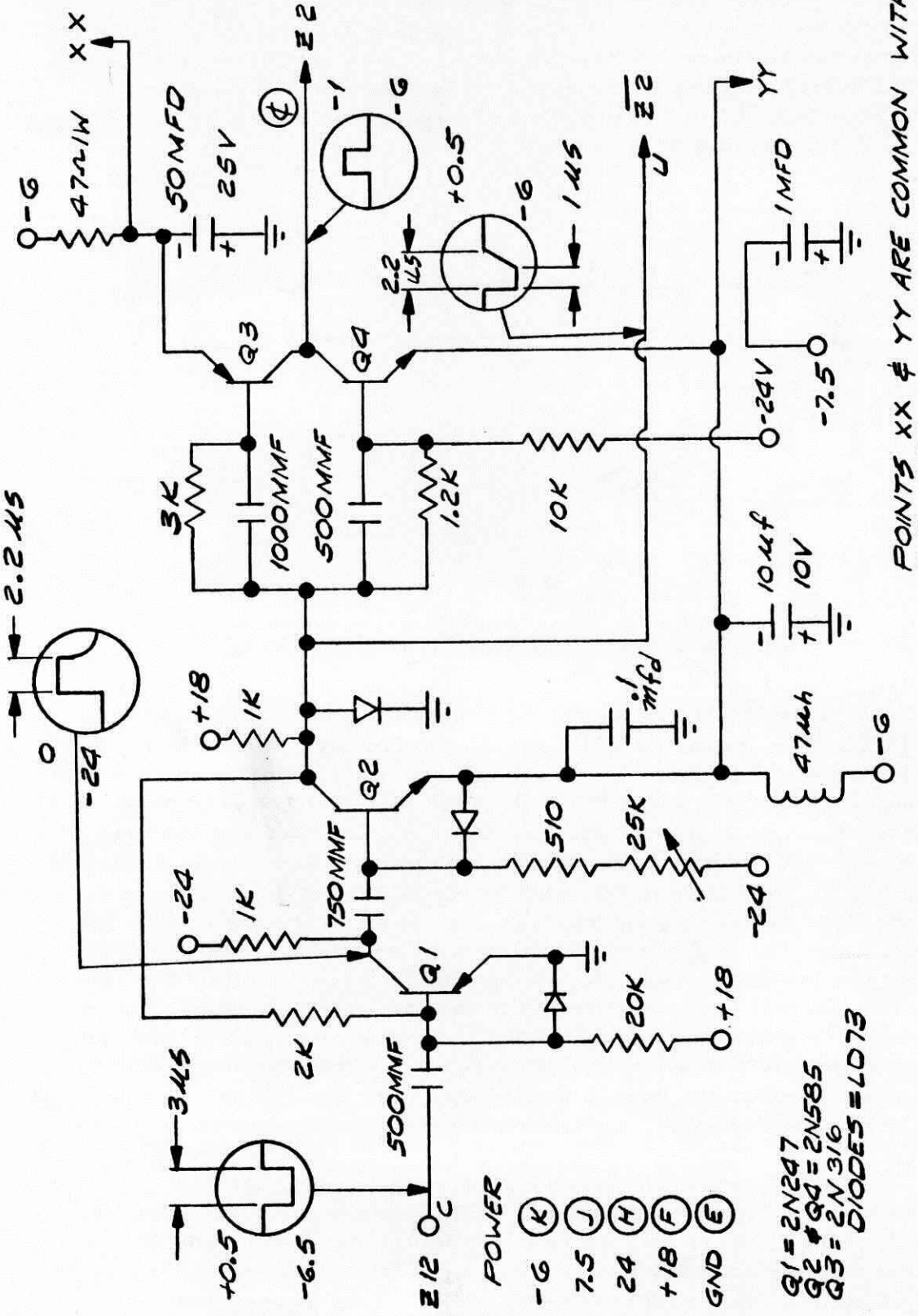


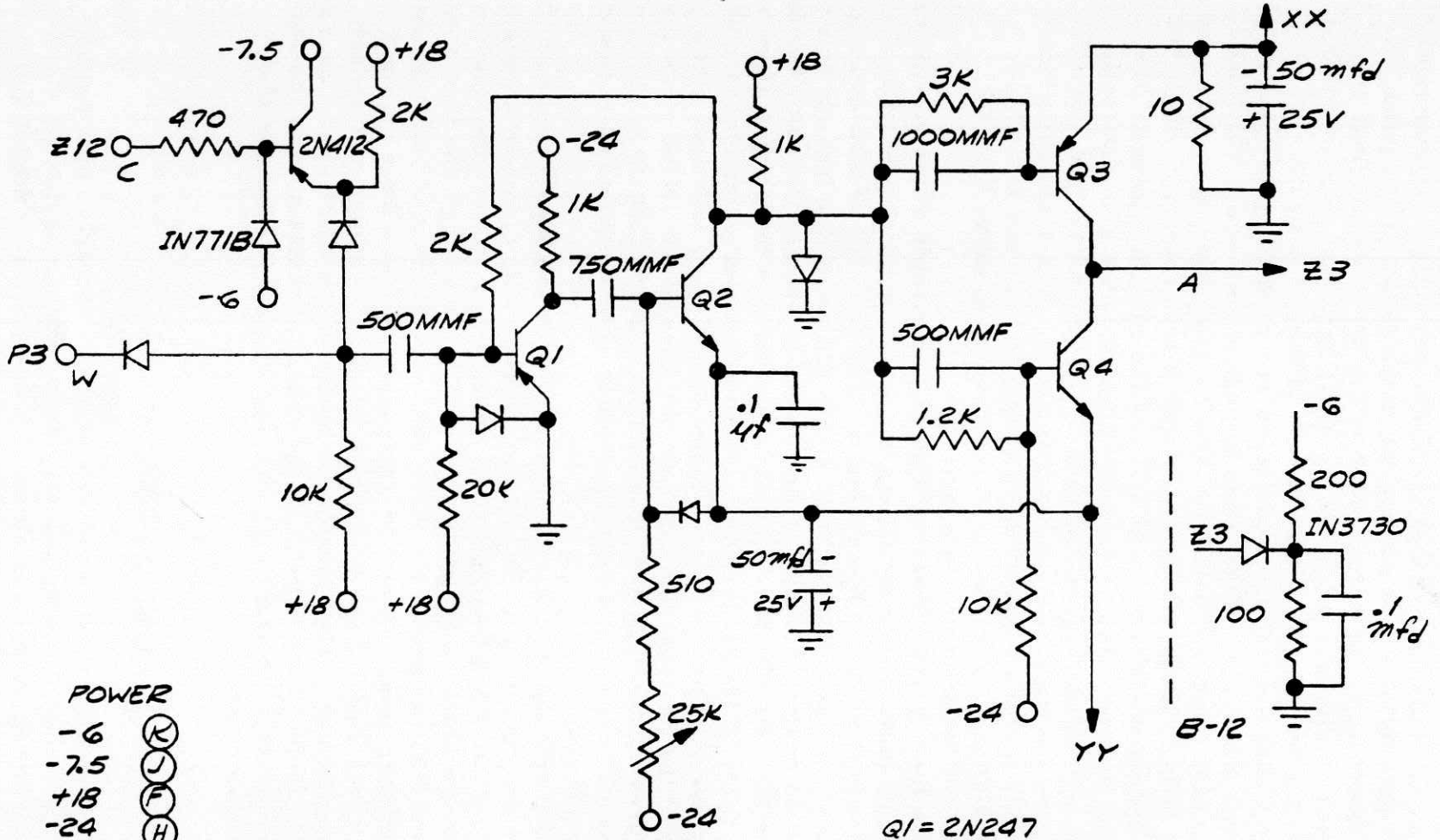
FIG. 441 SHAPING AMPLIFIER SYMBOL

The first two stages of the Z2 shaper (Q1 and Q2 Fig. 442) are held off by the forward drop of the diodes from emitter to base, and Q3 is biased off by point XX which is -1v. Q4 is held on saturated by some of the current supplied by the 1.2K resistor and clamps the clock line to -6v. Since the collector of Q1 is at -24 volts and the base of Q2 at -6v the charge on the 750 mmfd capacitor is 18v. the differentiated fall of Z12 turns on Q1 bringing its collector to ground and turning on Q2. As soon as Q2 has turned on the voltage across the 750 mmfd capacitor will become 6 volts with the polarity reversed because the forward biased Q2 base-emitter junction clamps the base to -6v. Q2 will stay on while the capacitor continues being charged through the 25K trimpot and 510 ohm series resistor until the base reaches a potential low enough to turn off the emitter-base junction. Pulse width may, therefore, be adjusted with the 25K pot but the range is limited because a significant amount of capacitor current is absorbed by Q2.

Q1 and Q2 return to their original state waiting for another trigger pulse and the 750 mmfd capacitor charge reverses through the LD 73 diode on the Q2 base and the 1k Q1 collector resistor. The 2k resistor between Q1 and Q2 provides positive feedback which speeds the switching of the two transistors both on and off. This also improves width stability because the Q1 collector is clamped at ground until the capacitor initiates turn-off.



REV. 8-31-64 FIG 442 Z2 SHAPING AMPLIFIER CIRCUIT A-579096



REV. 8-31-64

FIG 443 Z3 SHAPING AMPLIFIER CIRCUIT A-579,097

When Q2 turns on both output stage bases are driven negative. Drive and bias are designed so that Q4 which was fully on is substantially off before Q3 gets fully on and clamps the clock to the -1v of point XX. When Q2 turns off again the output stage is driven to its original state. The 3K resistor in the base of Q3 allows additional base current so that Q3 stays fully on until driven off at the end of the clock pulse.

At anytime that both output transistors are conducting large currents flow from XX to YY. This tends to happen with every clock pulse. Q2 turning on also pulls YY positive. The careful filtering of this point is necessary to keep these fast positive spikes under control. Both the electrolytic capacitors (for the 180 KC) and the .1 mfd ceramics are located in each shaper circuit where the current paths are physically short. Noise pulses on the -6v supplied to flip-flops have the same effect as trigger pulses if they are large enough. The 1mfd capacitor on the -7.5v has nothing to do with the shaper circuit and is located here for convenience. The $\overline{Z2}$ output is provided to drive the dZ2 circuit and is not used outside this board.

The Z3 shaper (Fig. 443) begins with an and circuit which selects one Z12 pulse out of four. When P3 (from the phase counter) goes high charge is removed from the 500 mmfd capacitor. The next fall of Z12 will cause the 2N412 class transistor to pull one end of the capacitor low and trigger Q1. Generation of the Z3 clock then proceeds in exactly the same manner as did that of Z2. P3 will fall immediately after Z12 but always after because of the delay in its generation. Thus the two computer clocks rise together because they are generated from one pulse by identical circuits. The function of the resistor and diode on the base of the 2N412 class transistor is to prevent oscillation of this emitter-follower which might otherwise occur since it is being driven by another emitter-follower in the Z12 playback circuit.

Inductance and capacitance in the wires transmitting Z3 cause an overshoot on the rise of up to 2v . A high speed diode clamp in a physically central location on board B-12 clips off most of this spike. Its location is a compromise which combines with the established high and low levels (points XX and YY) to answer the different requirements of both type A and type B trigger nets. Type A triggers operate when their nominal D.C. level is reached. Type B triggers are A.C. coupled and operate on the change in level. The meaningful levels of the clock are of course those actually found at the flip-flops and record circuits so that the output at the shaper is of interest only because of what it becomes elsewhere in the computer.

THE dZ2 CIRCUIT

The dZ2 circuit is used in the production of an early clock pulse. The circuit generates an early clock by delaying the regular Z2 clock enough so that it can be used as an early clock the following bit time. The delayed clock is not a narrow pulse like the original clock, but since only the positive rise is used, the shape of the rest of the pulse is not important.

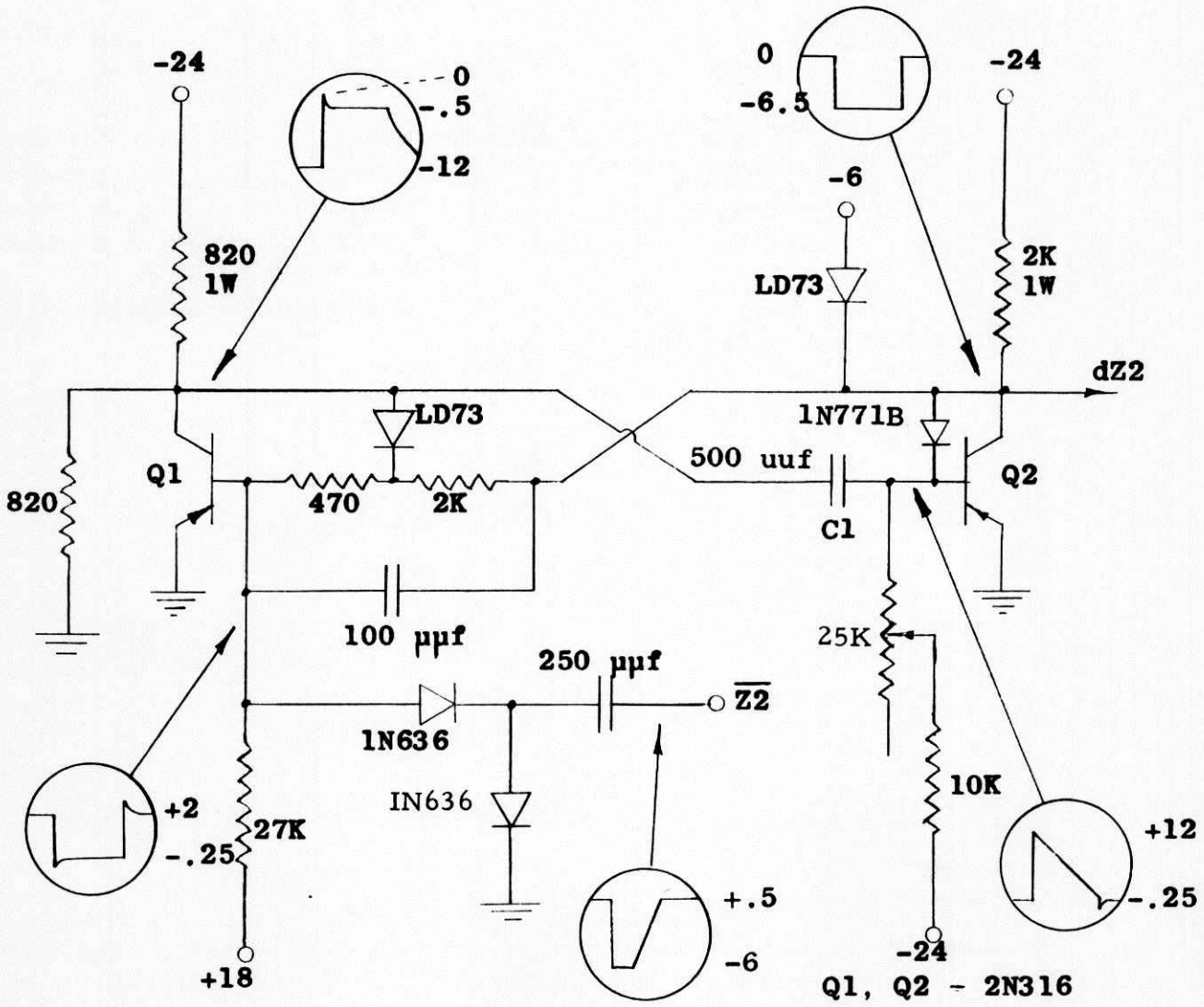


FIG. 444. dZ2 CIRCUIT DIAGRAM

In the steady state condition, Q1 is turned off and Q2 is turned on. The trigger circuit operates the same as that in the C10 circuit. The Z2' pulse goes high first and must go low to trigger the circuit. During the steady state condition the capacitor C1 charges to about 12 volts. This is due to one side being clamped to ground and the other side being connected to a -12 volt point on a voltage divider. When a trigger occurs, Q1 is turned on, and its collector voltage becomes clamped to ground. The rise in voltage at the collector of Q1 is transmitted to the base of Q2 turning that transistor off. The collector voltage of Q2 drops to -6 volts and is clamped at that level by a diode. The negative going voltage is transmitted to the base of Q1 keeping that transistor turned on.

The charge on C1 causes the transistor Q2 to remain turned off until current through the trimpot brings the base back below ground. Q2 turning on causes return to the stable state.

The trimpot is nominally adjusted to make dZ2 rise about 3.6 microseconds before the rise of the normal clock (Z2). A final adjustment is then made with the proper sensing of general storage information the final goal. Readjustment of dZ2 necessitates erasure of all of general storage.

The Z2 circuit is constructed on the shaping amplifier board, D-9, and its symbol is shown below.

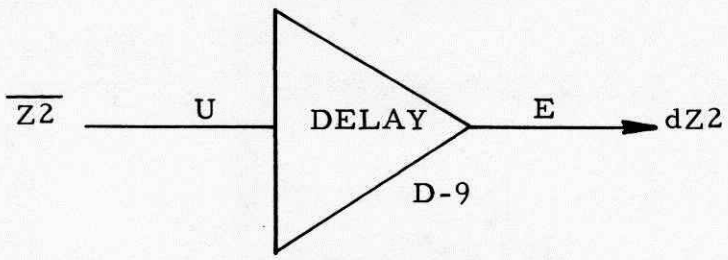


Fig. 445 dZ2 Symbol

GENERAL STORAGE SELECTION MATRIX MODEL D

The function of the general storage selection matrix is to connect one and only one head to the playback and record amplifiers. The head desired is specified by the logical signals which control the matrix. It is built on a single printed circuit board the two areas of which are designated D16 and D17. It consists of a transformer pair, isolation diodes, and transistor switches. The general storage pre-amplifier previously described is physically part of this board for engineering reasons. The board for the 2048 word memory (32 heads) is used without the parts for Col. 5-8 in the 1024 word memory (16 heads) machines. The somewhat arbitrary arrangement of heads facilitates this. A table of correspondence between head and memory address is on Page 3-18. Terminal designations have been preserved so that the 1024 word assembly may also be used as a replacement part in machines before serial #315. Discussion herein assumes a 2048 word matrix. The complete smaller matrix is shown in Fig. 447. Its operation is self-evident if the 2048 word input is understood.

Fig. 446 shows the selection matrix including the transistorized switches called row amplifiers (RA) and column amplifiers (CA) (these circuits are described in detail later), and the record and playback amplifiers which are shown for reference only as they are not part of the matrix. The 1's transformer and 0's transformer are packaged into the unitary-appearing selection transformer mounted on TBD 16-17. As will appear separate magnetic structures for 1's and 0's are essential to recording. They are connected in aiding polarity for playback.

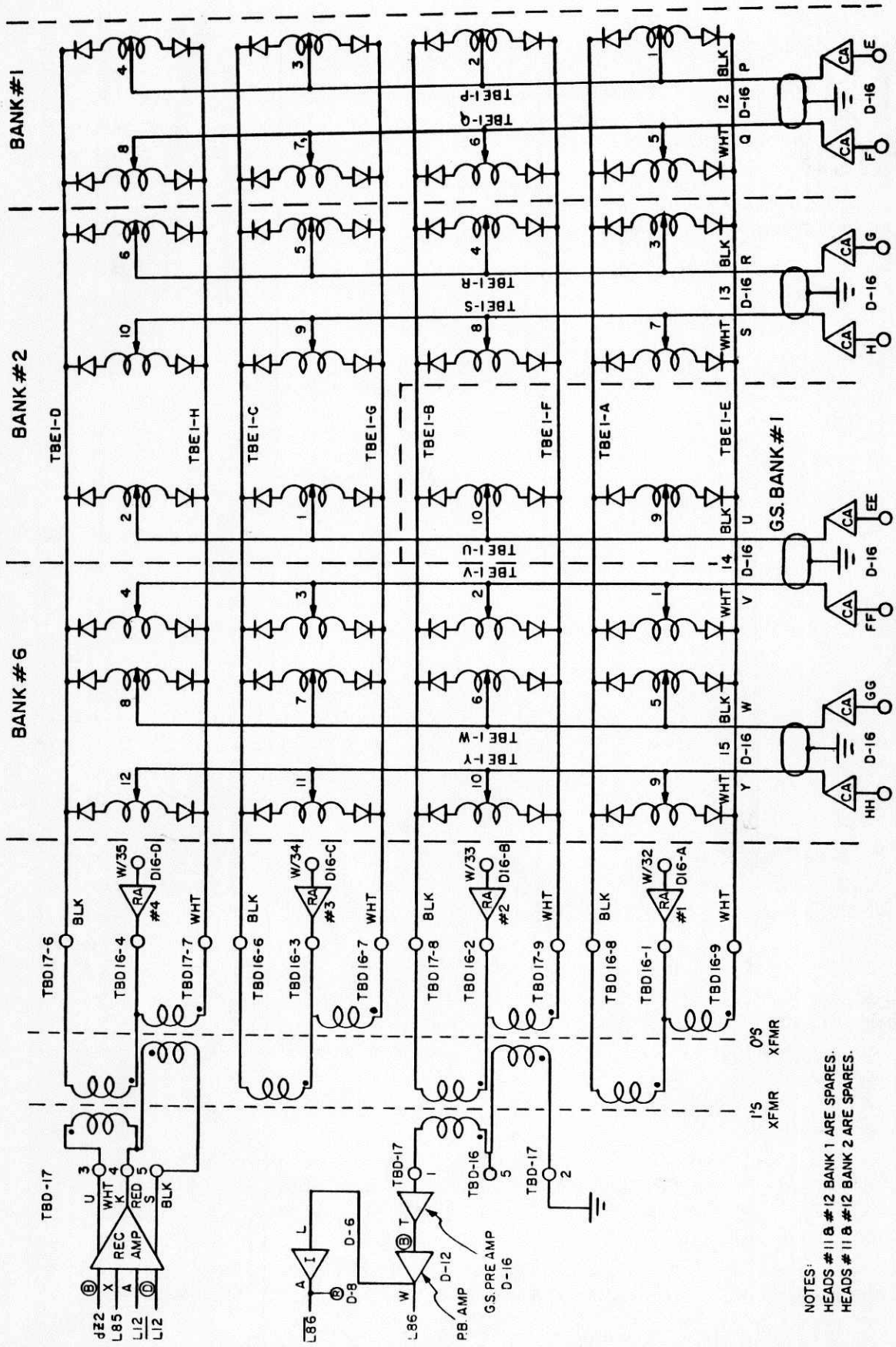

BANK #1
BANK #2
BANK #6
TBE1-D
TBE1-H
TBE1-C
TBE1-G
TBE1-B
TBE1-F
TBE1-A
TBE1-E
TBE1-P
TBE1-Q
TBE1-R
TBE1-S
TBE1-T
TBE1-U
TBE1-V
TBE1-W
TBE1-X
TBE1-Y
G.S. BANK #1
TBD17-6
TBD16-4
TBD17-7
TBD16-6
TBD16-3
TBD16-7
TBD17-8
TBD16-2
TBD17-9
TBD16-8
TBD16-1
TBD16-9
BLK
WHT
RA
#4
#3
#2
#1
DI6-D
DI6-C
DI6-B
DI6-A
W/35
W/34
W/33
W/32
TBD-17
REC AMP
GS PRE AMP D-16
PB AMP
D-12
D-8
D-6
L86
dZ2
L85
L12
L12
I'S XFMR
O'S XFMR
CA
D-16
W/36
W/37
W/38
W/39
W/41
W/42
W/43
W/44
COL.1
COL.2
COL.3
COL.4
COL.5
COL.6
COL.7
COL.8
NOTES:
HEADS #11 & #12 BANK 1 ARE SPARES.
HEADS #11 & #12 BANK 2 ARE SPARES.
B 579087 2000 WORD G.S. MATRIX MXD

Fig. 446

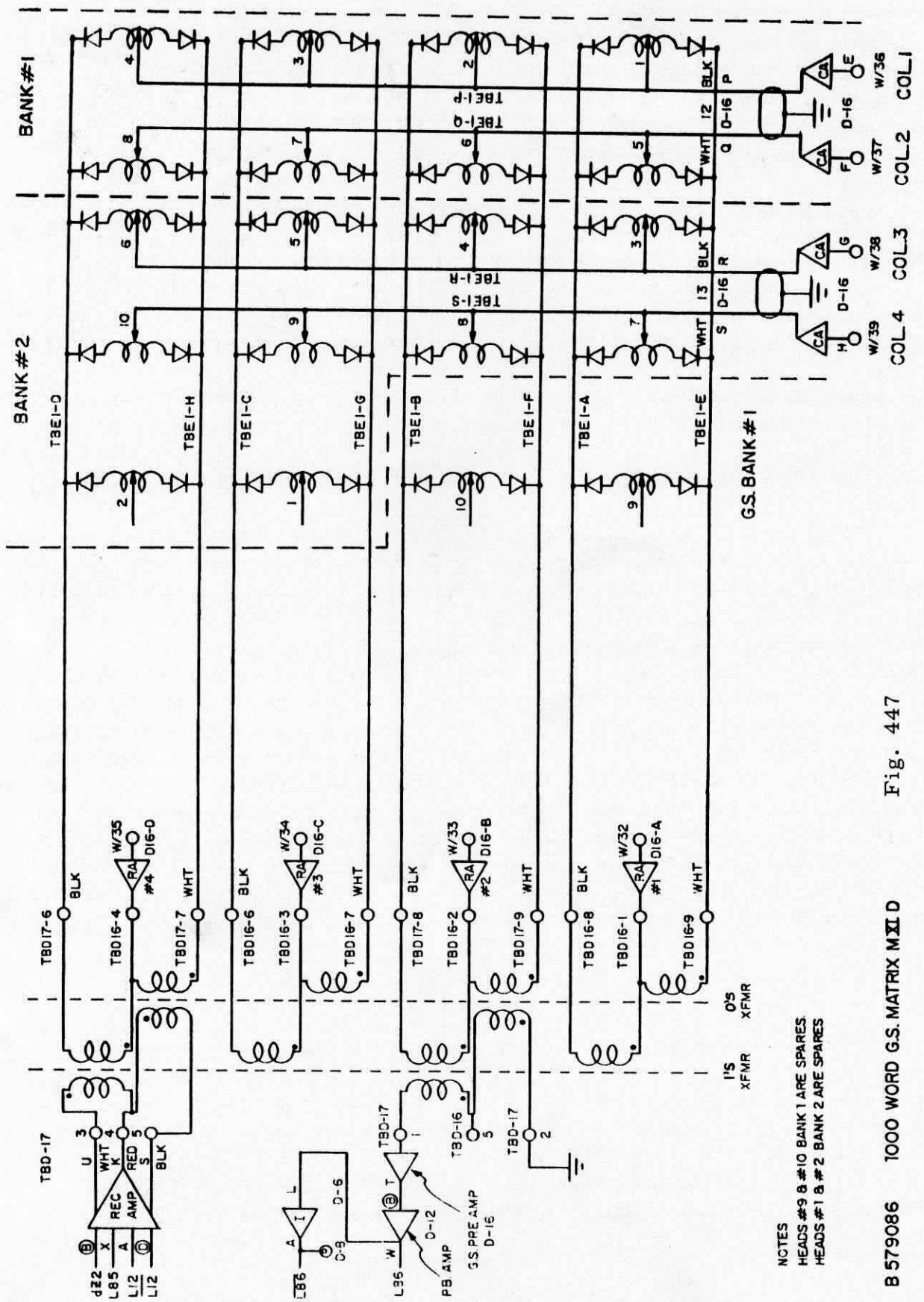


Fig. 447

B 579086 1000 WORD G.S. MATRIX MXI D

NOTES
HEADS #9 & #10 BANK 1 ARE SPARES
HEADS #1 & #2 BANK 2 ARE SPARES

Wire Nos. 32 through 39 and 41 through 44 bring the control voltages to the row and column amplifiers from the logic rack. Only one row and one column signal can be high at any time. The column amplifier whose input wire is high acts like a switch and grounds the center taps of all the heads in that column. All other center taps are connected through a resistor to -24v. The row amplifier whose input is high acts like a switch and connects the common point of the transformer windings for that row to a -5/10v supply. All other points are connected through a resistor to +18v. This means that all the head diodes except two are back biased with up to 40v. These two are on the head selected and are biased to full conduction by a small d.c. current flowing from ground at the head center tap through each half of the head and each transformer winding to the -5/10v supply. The net flux in the head from this current is of course zero because the direction of current is opposite in each half of the head. Playback voltage is induced across the entire head and therefore appears across both the transformer windings. Since the windingsare aiding and turns ration is 1:1 playback appears also on all other windings including the series aiding windings connected to the general storage playback pre-amplifier. Terminal 5 of TBD-16 is used only as a tie point.

To record a 1 or a 0 the record amplifier drives its winding of the appropriate transformer and the pulse appears on all the other windings. The only complete low impedance load consists of one half of the selected head in series with diode and -5/10v supply as connected by the driven row and column amplifiers. The record current pulse, then, passes through the selected head. Current flowing in the forward direction for the head diode of only 1/2 of the selected head induces, by mutual coupling, a small opposing current in the opposite leg which slightly reduces the strength of the magnetizing field. If the 1's and 0's windings were on one transformer capacitive coupling between windings would supply enough more current in this direction to materially degrade the recording. Since current direction in the head is opposite for 1's and 0's the polarity of the recorded bit is opposite also. The record pulses may develop as much as 2v across the -5/10 supply. The back bias on the unselected head diodes isolates the head and wireing capacitance of these heads improving the rise time of the current in the selected head.

COLUMN AMPLIFIER

The function of a column amplifier is to ground all the head center taps in one matrix column upon logical stimulation and to open this connection when the logical input is low. The circuit of one of the eight amplifiers is shown in Fig. 448. All of them are built on the selection matrix board.

When the input is high the emitter of the first stage rises toward ground turning the second stage on. The second stage absorbs about 50 ma of base current from the output transistor turning it on hard

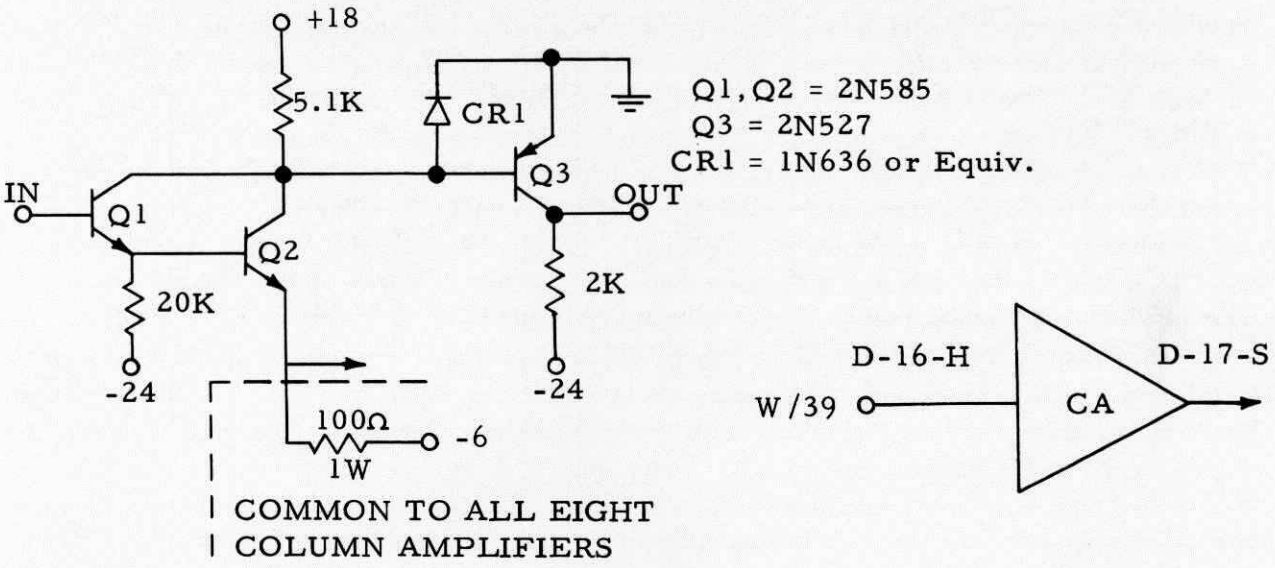


FIG.448 COLUMN AMPLIFIER AND SYMBOL

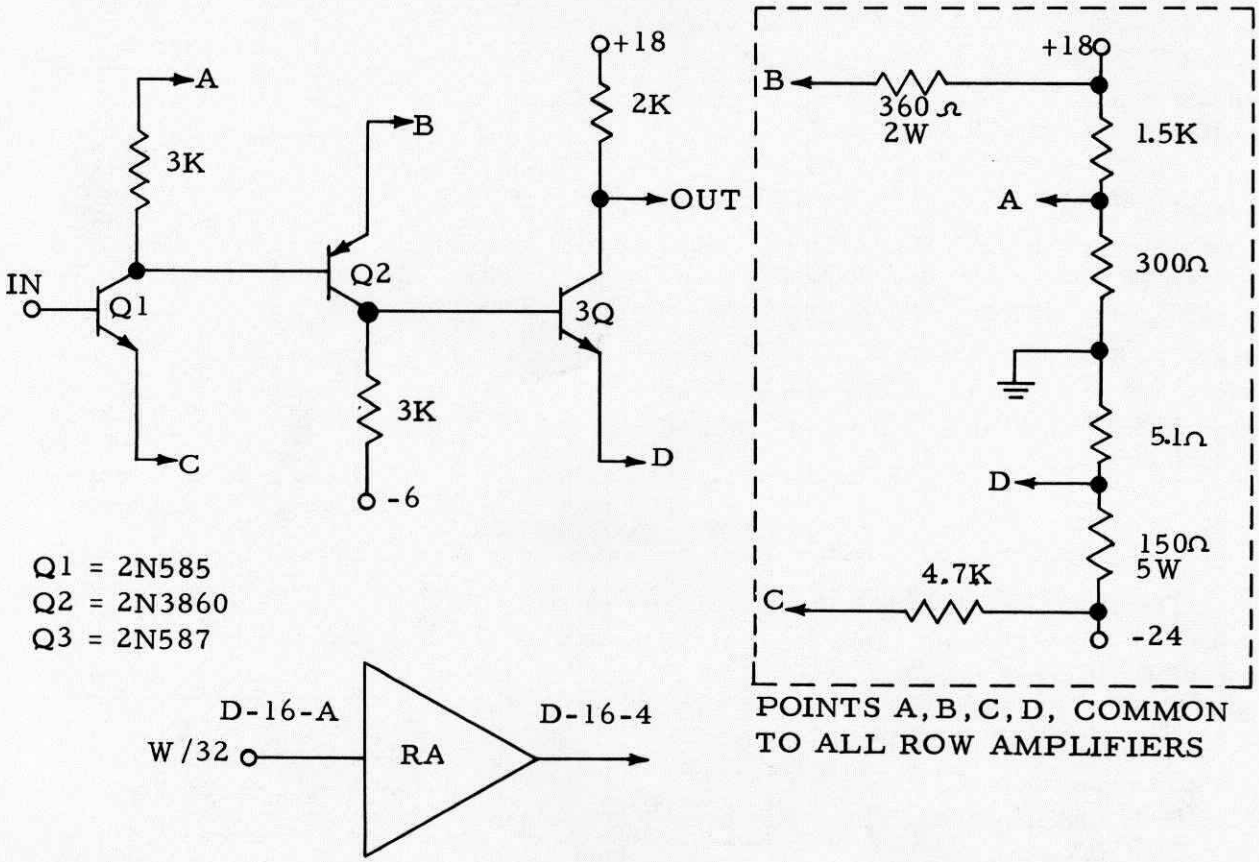


FIG. 449 ROW AMPLIFIER AND SYMBOL

enough to pass the record pulse with no drop. The emitter of the second stage rises to a nominal -. 9v. This level is fixed because the 100 ohm resistor is common to all eight amplifiers and whichever amplifier is on will hold this level. When the input is low the emitter of the first stage falls below -6v. This cuts off the second stage because its emitter is held at -. 9v by whichever other amplifier has been turned on. The output transistor turns off and the head center taps connected to the output terminal are pulled to -24v by the 2K resistor. The collector of the first two stages rise towards +18v but the level is clamped by the diode to ground. The diode limits the dissipation in the first stage and voltage on the output base which would otherwise rise high enough for permanent damage.

THE ROW AMPLIFIER

The function of the row amplifier is to connect the -5/10 volt source to the transformer common points in a single matrix row when its logical input is high and to disconnect these points when the logical input is low. All amplifiers are built on the selection matrix board and four are used. The circuit is shown in Fig. 449.

There are six resistors common to all row amplifiers. As in the column amplifier the levels at these resistors are set at one nominal value by whichever amplifier that is on. One amplifier will always be on and hold the other three off.

When the input is high the first stage is on pulling the second base low enough so that the second stage turns on and supplies about 50 ma to turn on the output transistor. As in the column amplifier this large base drive is provided to allow 500 ma of collector current. Therefore the record pulses pass through with minimal loss.

The row amplifiers have four points in common. The d. c. level at these points is fixed by divider action and/or the fact that one of the amplifiers is always on. Point A (Fig. 449) is simply a low voltage collector supply for the first stage. Its nominal 2. 5v keeps the junction voltages on the first two stages at low dissipation values. It was made common to save power drain in the total matrix. Point B will be close to ground and this common resistor also saves power. Point C will be just below the highest matrix row input (W/32-W/35). Point D is held at about -5/10 volt by divider current and the bias current flowing through the head diodes via the output emitter of the amplifier. Its function is to force this bias current to flow. The point becomes much more positive when the record current pulse is actually flowing.

When the input to the amplifier is low the first stage is cut off because point C is more positive than the input. The first collector rises to +2. 5v which is sufficient to cut off the second transistor because point B is held near ground. The output base falls to -6v supply and cuts off because point D is -5/10v. The 2K resistor pulls the output collector to +18v and back biases the head diodes in the row.

THE G20 CIRCUIT

A circuit is provided in the computer which prevents recording on the drum if the record -24 volt supply is low enough to cause a bad recording. This circuit prevents recording by holding the record gates (L85 and K37') low if the record supply is less than about -19 volts.

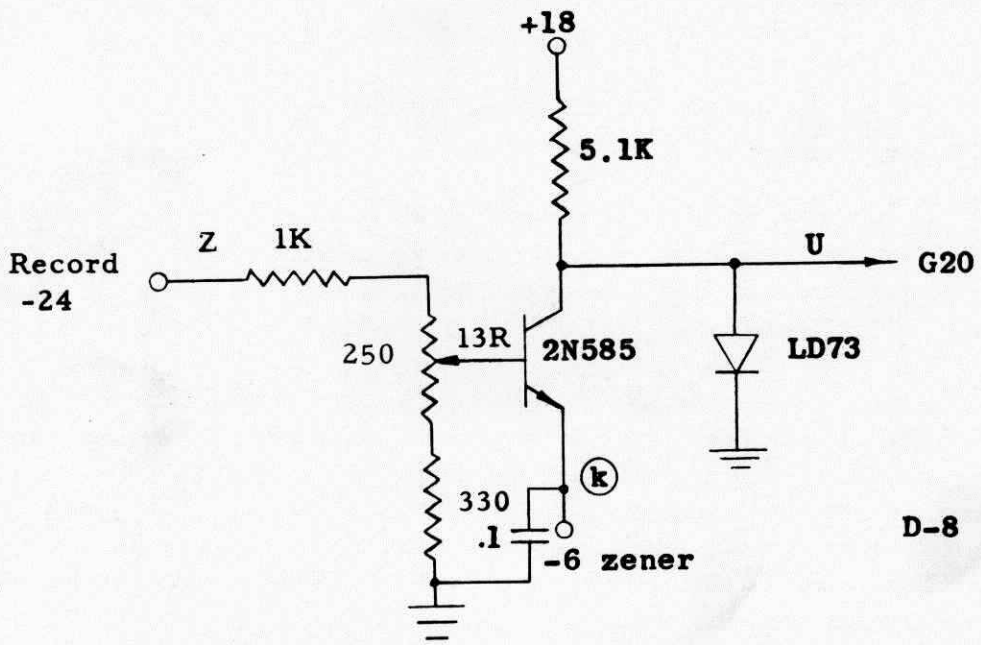


FIG. 450 G20 CIRCUIT

When the -24 record voltage is at normal levels, the base of the transistor is held more negative than the emitter, keeping the transistor turned off. The output voltage is then clamped to ground by the clamp diode. If the -24 record voltage drops below approximately -19 volts, the base of the transistor becomes more positive than the emitter and the transistor turns on, clamping the output to -6 volts. The capacitor removes ripple from -6 zener which would otherwise appear on the collector when -24 record is very close to the level set to trip G20.

The G20 circuit is constructed on diode logic board D-8.

Board Location	Input	Alternate Input	Output	Signal Designation	Name
D10	J	H	P	Z11	Sector Index
D10	ⓑ	ⓒ	W	Z12	Master Clock
D11	J	H	P	L6	FA "A"
D11	ⓑ	ⓒ	W	L7	FA "B"
D12	J	H	P	Z15	Sector Address
D12	ⓑ	ⓒ	W	L86	General Storage

POWER	
Pins	Power
A, ⓚ	Ground
E, U	-24
C, ⓗ	+18
ⓔ	-7.5
S	-6
Y	Ground (High Level)

Fig. 432 PLAYBACK CIRCUIT PIN CONNECTIONS

RECORD CIRCUITS

The computer uses the record circuits to provide the proper drive to the recording heads under the control of the logical information to be recorded, a record gate, and the clock. A record board consists of two identical record circuits. Each half of the record board drives half of the recording head. Since the windings of the two halves of the record head are 180° out of phase, a pulse generated in one half of the board will cause the field to build up in the opposite direction. Thus one of the circuits is used to record ones and the other is used to record zeros.

There are three inputs to each half of the board. The inputs are information, record gate, and clock. The information supplied to the zeros record side of the record board is the inversion of the information supplied to the ones side. Each record circuit consists of four parts: the trigger circuit, record one-shot, complementary symmetry amplifier, and output stage.

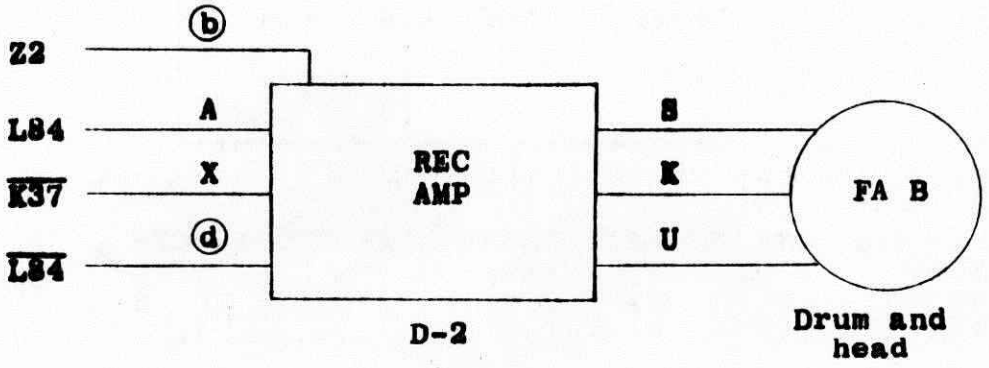


FIG. 433. RECORD CIRCUIT SYMBOL

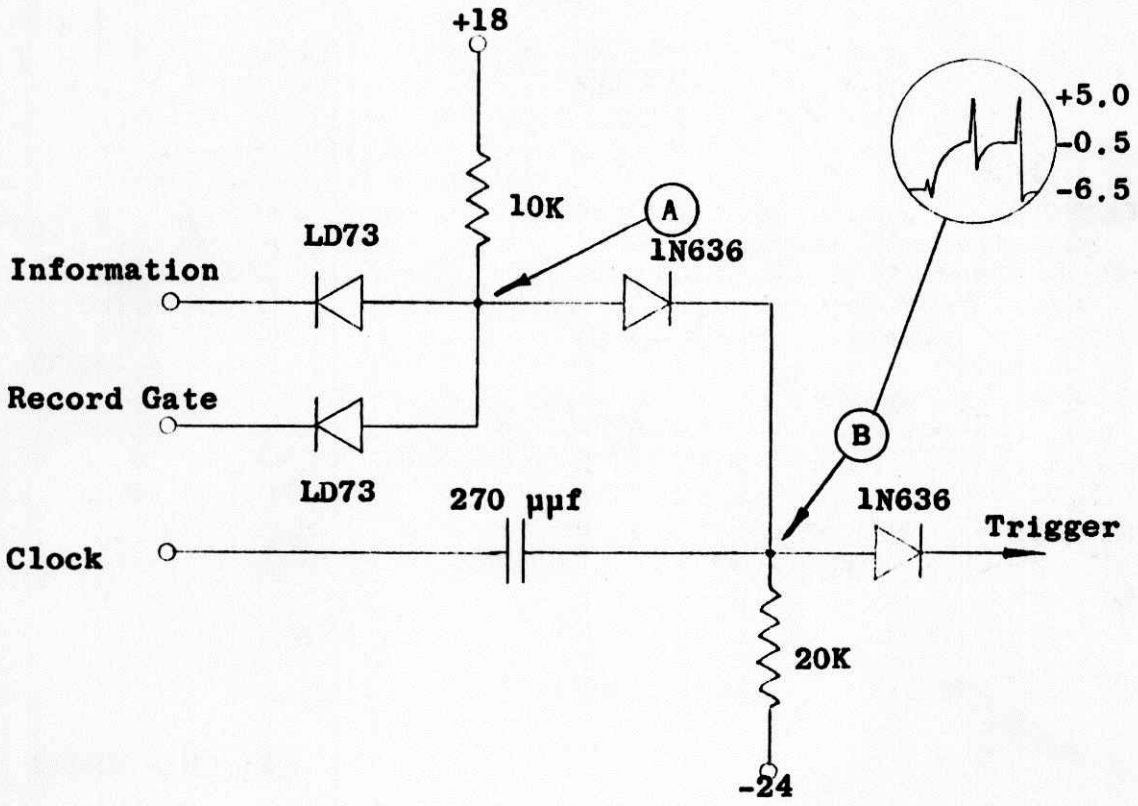


Fig. 434 RECORD TRIGGER CIRCUIT

When either the information or the record gate is low, point A is held at -6 volts and point B will also be -6 volts. If both the record gate and the information are high simultaneously, point A is allowed to rise to zero volts. Point B also rises to zero volts charging the condenser through the 10K resistor and the internal impedance of the driving circuit. During this time it is assumed that the clock is low (-6).

The clock will not arrive until after the information has been high long enough to charge the capacitor. When the clock arrives, the voltage on the capacitor is added to the clock voltage and causes point B to rise above ground towards about +5 volts. The record one-shot requires a trigger which is a few volts positive so this rise is sufficient to trigger the one-shot.

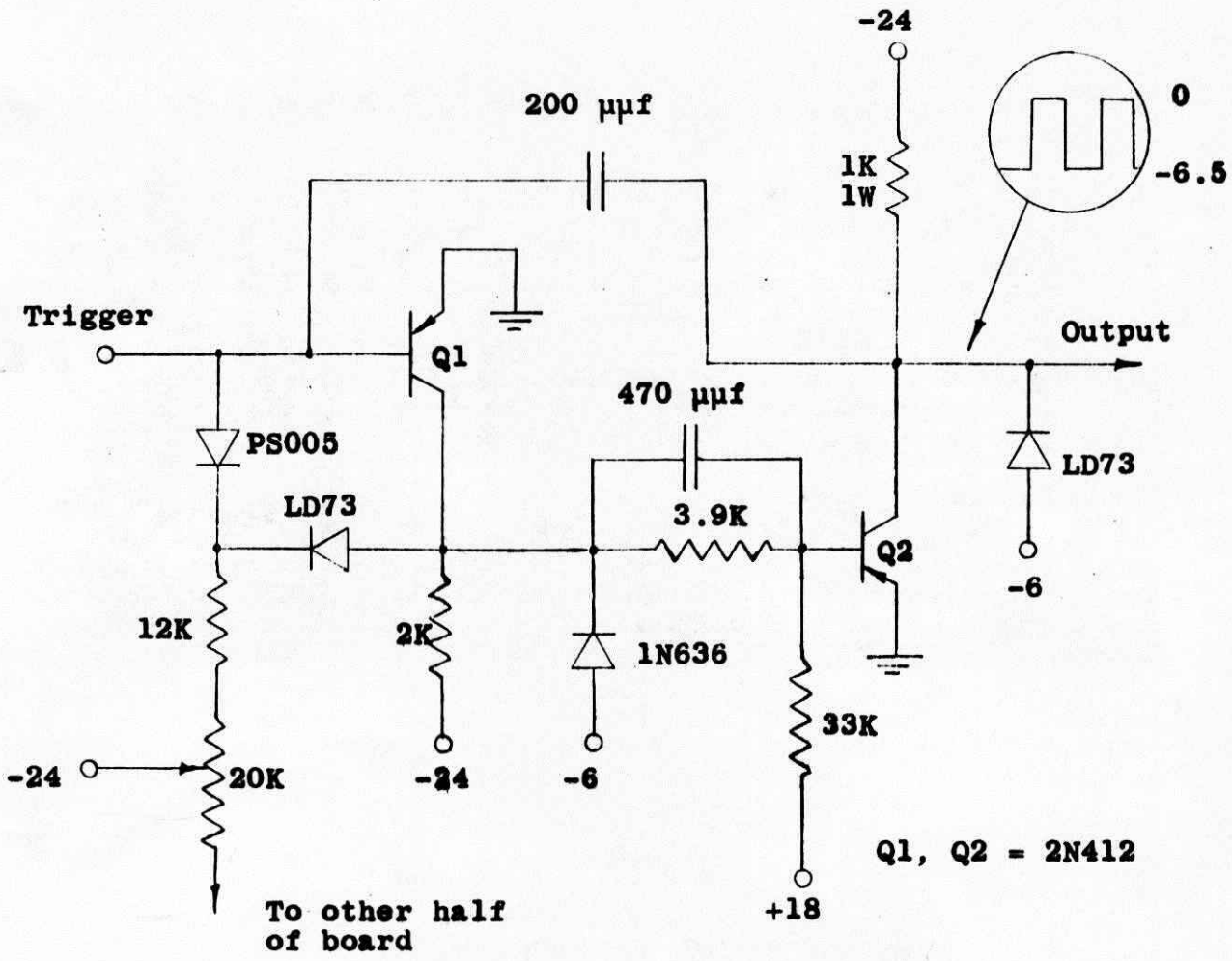


FIG. 435. RECORD ONE SHOT

The circuit that generates the actual record pulse is a monostable multivibrator. In the stable state, Q1 is turned on and is held on by the -24 volts connected to its base through the 20K trimpot, 12K resistor, and PS005 diode. This clamps the collector of the transistor almost to ground. Q2 is kept turned off by the +18 volts connected through the 33K and 3.9K voltage divider. Since one end of the 3.9K resistor is held at ground, the base of Q2 is held slightly positive keeping it turned off and the output is, therefore, clamped to -6 volts.

When the trigger occurs, the base of Q1 is driven positive, turning the transistor off. This causes the collector to go more negative until it is clamped at -6 volts by the diode. This voltage is transmitted to the

base of Q2, turning it on and causing its collector to be clamped to ground.

The positive rise in the collector voltage is transmitted to the base of Q1 keeping it turned off after the trigger goes away. The circuit will maintain this state until the 200 mmf capacitor has discharged sufficiently to allow Q1 to turn on again (about 1.5 microseconds). At that time, the circuit regains its stable state and will hold that state until another trigger occurs. The 20K trimpot allows for pulse width matching of the two circuits that comprise a record board.

The output from the circuit is taken from the collector of Q2. After a trigger, the collector voltage of Q2 will rise to ground and remain there for about 1.5 microseconds. which is determined by the discharge time of the feedback capacitor. After that interval, the voltage will drop to -6 volts and will remain there until the next trigger.

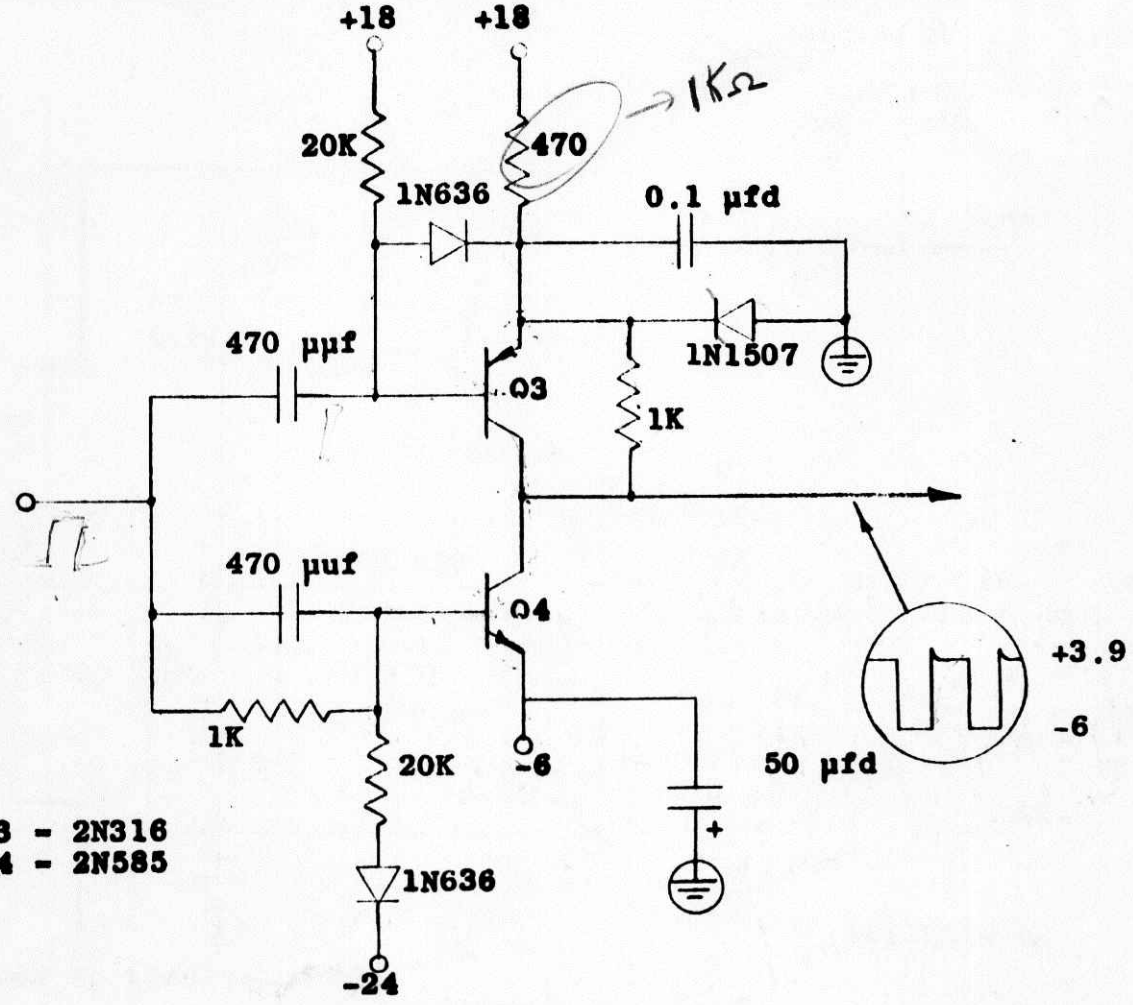


FIG. 436 RECORD COMPLEMENTARY SYMMETRY AMPLIFIER

The next stage is a complementary symmetry power amplifier. When the input is at -6, as it will be any time there has been no trigger, Q4 is kept turned off by the 1K and 20K voltage divider. The emitter voltage of Q3 is maintained at +3.9 volts by the 1N1507 zener diode. Q3 is kept turned off by the forward voltage drop of the 1N636 diode. When a trigger occurs, the voltage on the input rises to 0 volts which turns on Q4. Q4 clamps the output to -6 volts. After a short interval, the output of the one-shot goes low. This turns off Q4 and turns on Q3, bringing the output voltage up to +3.9 volts. After the coupling capacitor, that is in the base circuit of Q3 charges, Q3 turns off. The output remains at +3.9 volts because of the connection to the Q3 emitter through the 1K resistor.

The last stage in the record circuit is the output stage. This stage provides the record head with the .5 ampere, 1.5 microsecond pulse needed for recording.

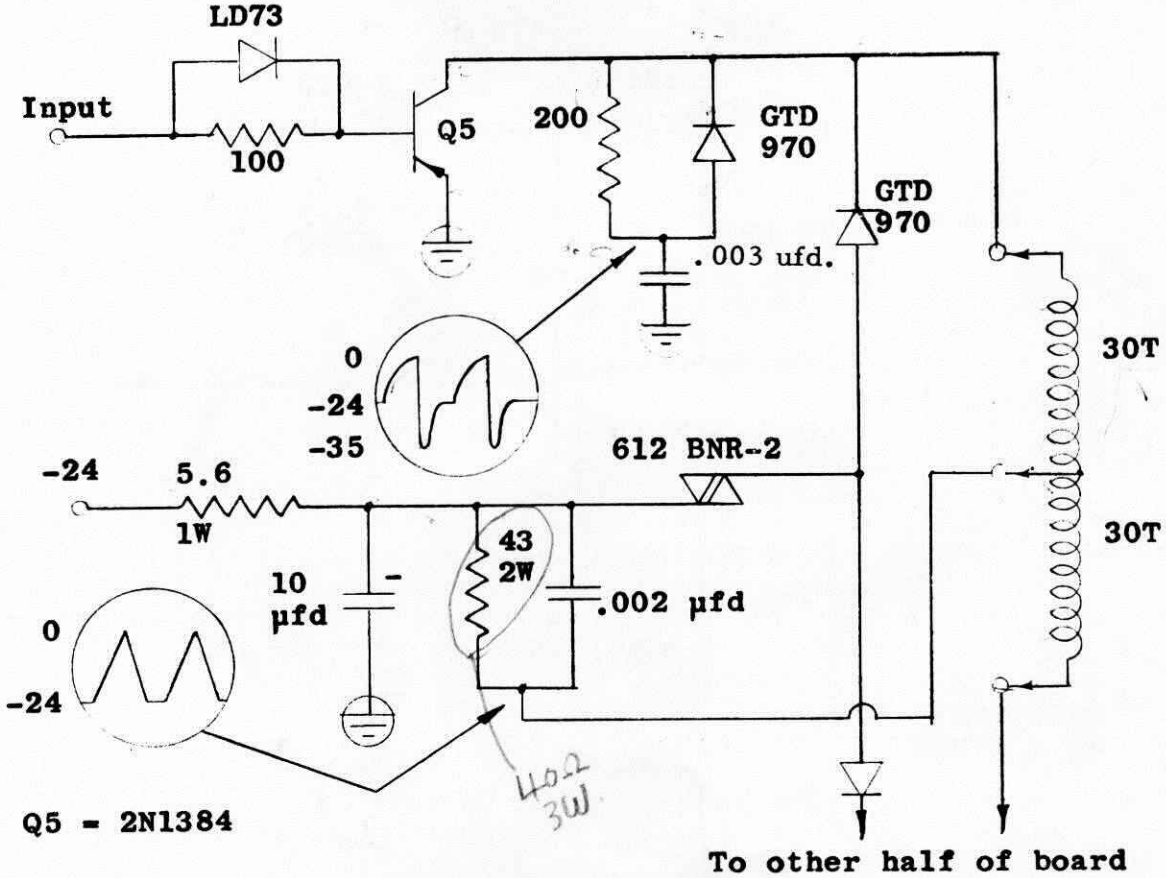


FIG. 437 RECORD OUTPUT STAGE

After a trigger has occurred, the input to Q5 goes low (-6 volts). The base of Q5 will be slightly negative turning the transistor on and causing the collector of Q5 to rise from -24 volts to ground. Current then flows through Q5, one half of the record head, and the current limiting resistor to the -24 volt record supply. This current is the record pulse. When the interval is over, the input to the base of Q5 goes to +3.9 volts. The transistor turns off causing the current flowing through the record head to cease, terminating the record pulse. The collector of Q5 at this time will go to approximately -35 volts because of the inductive kick of the head before returning to -24 volts.

The 33 ohm resistor in the general storage record circuit controls the maximum record current. The additional resistors, diodes, and varistor are in the circuit to provide damping and thus control the transistor peak power dissipation.

There are three record boards used in the computer. They are located in board locations D1, D2, and D19.

Signal	Pin
Information	A
Information'	(d)
Record Gate	X
Clock	(b)
Record Ones	S
Record Zeros	U
Record Center Tap	K
-6	(k)&P
Record -24	M
+18	(f)
-24	(j)
Ground ⏚	(h)
Ground (⏚)	Z

FIG. 438. RECORD BOARD PIN CONNECTIONS

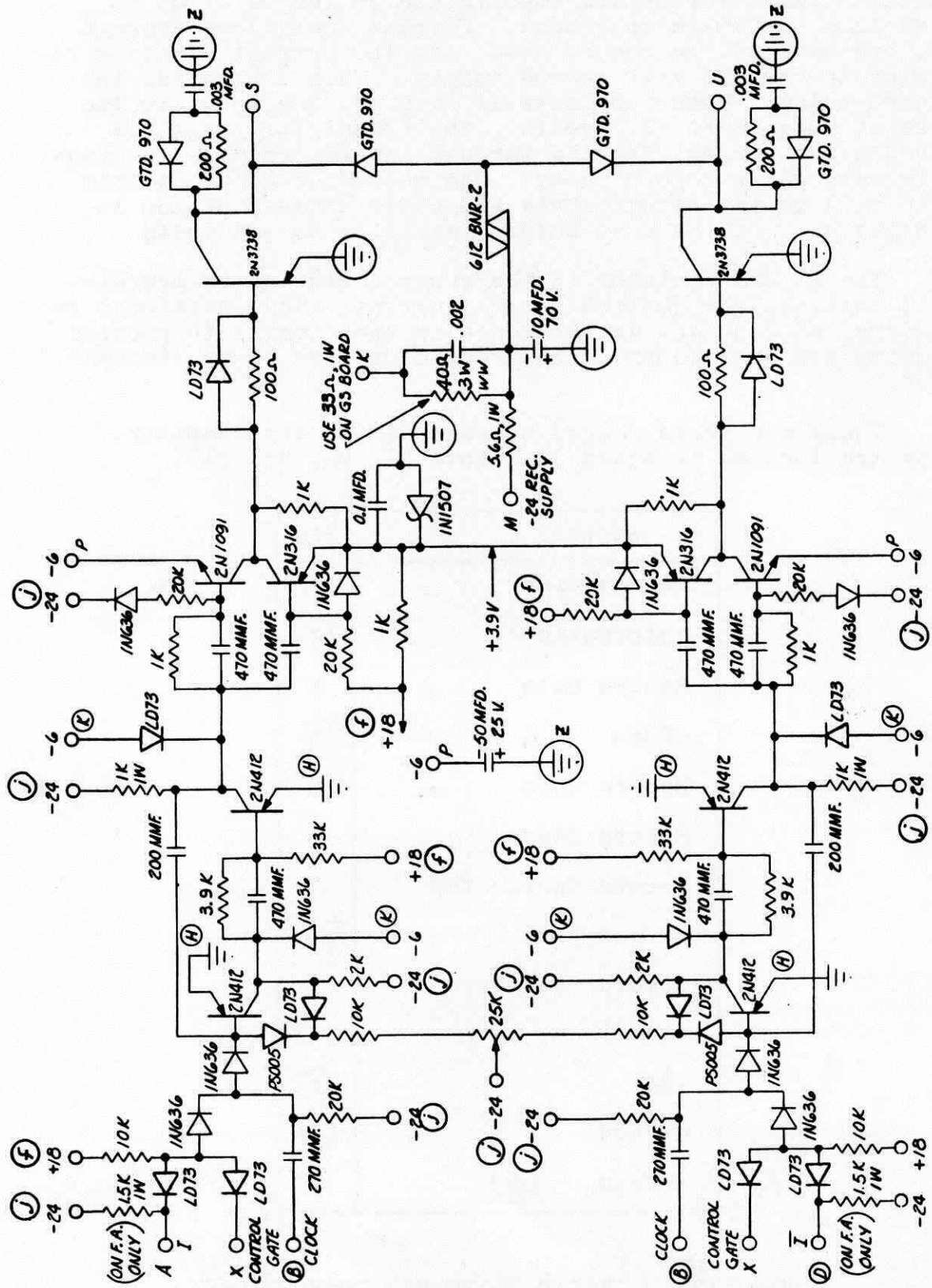


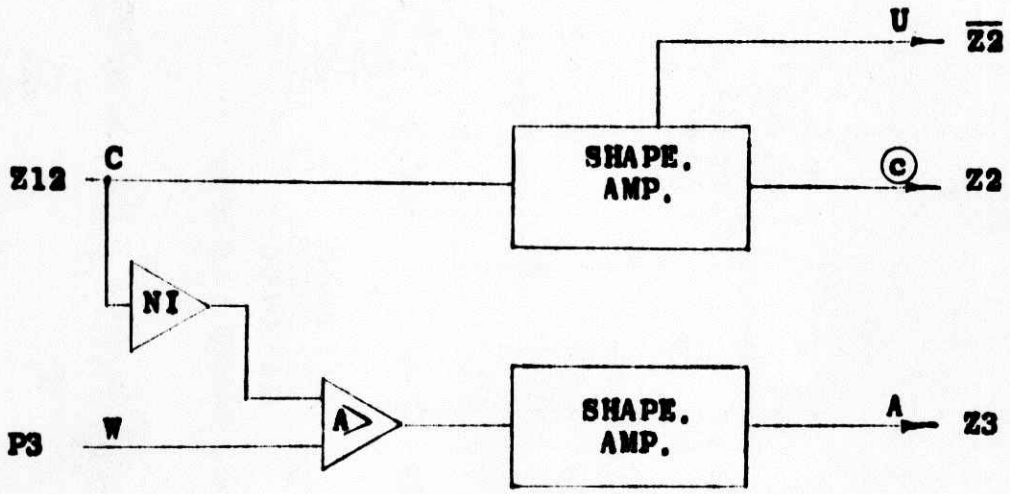
FIG. 439 RECORD CIRCUIT B-579 0408

Revised.

REV. 8-31-64

THE SHAPING AMPLIFIER

The computer contains two shaping amplifiers. They are used to reshape the playback from the master clock track into the proper shape for use in the machine logic. The shaping amplifier also raises the power level of the clock pulse to a level sufficient to drive the required logic. The shaping amplifiers used for the Z2 and the Z3 clocks are slightly different from one another. The Z3 shaping amplifier uses the P3 signal in an "and" gate to select every fourth pulse from the Z2 playback amplifier to produce the low speed clock. The Z2 shaping amplifier has an additional output used to drive the delayed Z2 circuit.



D-9

Fig. 440. Shaping Amplifier Symbols

The clock track playback information from the playback amplifier is applied to the input of the shaper circuit. In the first stage the information is amplified and differentiated very slightly. In the second stage the pulse is differentiated by a very short time constant coupling circuit. The bias of Q_8 is set at a point where only the positive peaks of the differentiated input signal are able to cause it to conduct. The 5k trimpot varies the time constant

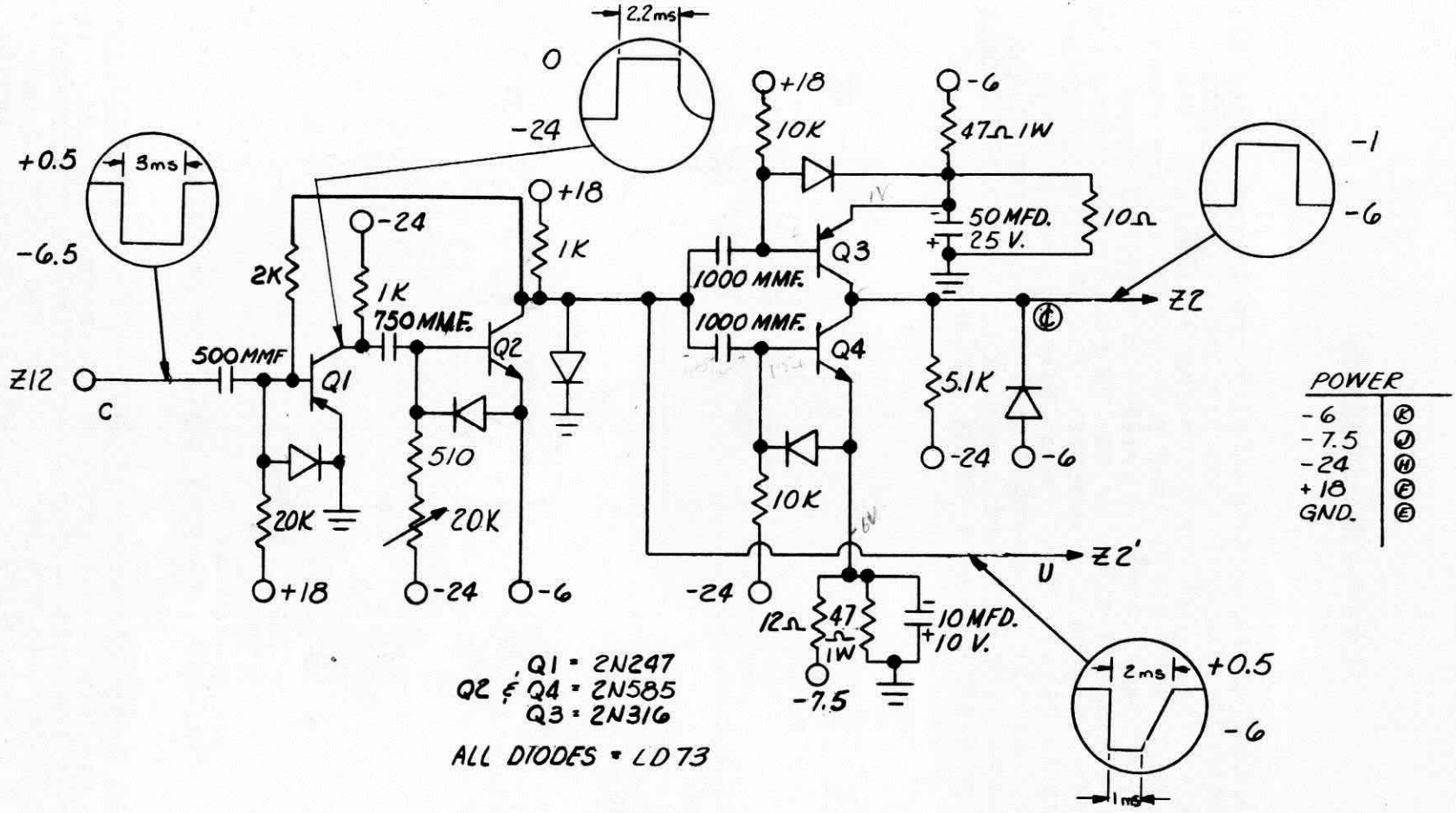


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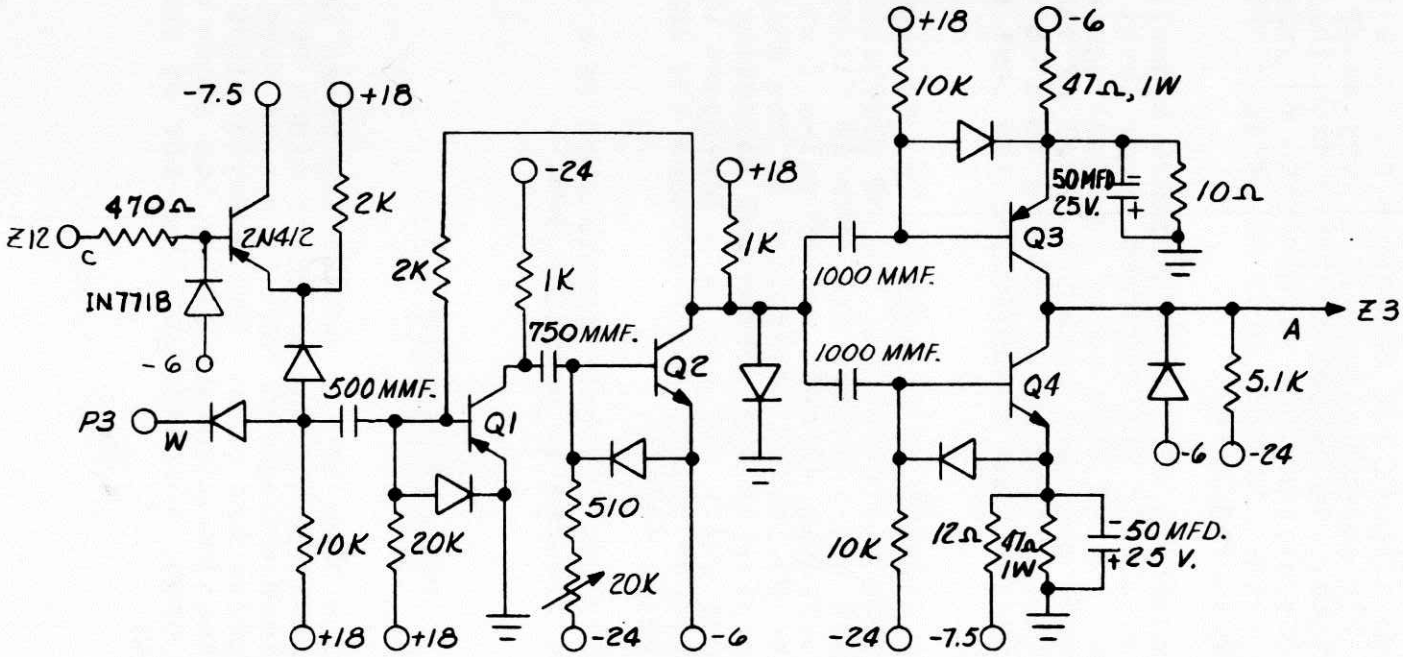
FIG. 441 Z2' SHAPING AMPLIFIER CIRCUIT

B-579041-A

With_____ Scale_____ Layout No._____



POWER	
-6	K
-7.5	J
+18	F
-24	H
GND.	J & K

Q1 = 2N247
Q2 & Q4 = 2N585
Q3 = 2N316

ALL DIODES = LD 73

11/10/60 FIG. 442 Z3 SHAPING AMPLIFIER CIRCUIT B-579,042-A

Scale_____ Layout No._____

of the differentiating circuit and therefore controls the width of the pulse. The output, then, is a very sharp pulse with an adjustable width. An output is taken from the collector of Q_2. This output consists of inverted Z2 pulses called Z2'. As this signal is used only to trigger the dZ2 circuit, little power is required.

The last stage consists of a complementary symmetry push-pull amplifier to obtain the required power level. The emitter of Q_3 returns to a -1 volt point on a voltage divider. This establishes the most positive level of the pulse at -1 volts. The emitter of Q_4 returns to a -6 volt point on a voltage divider thus establishing the most negative value of clock.

The Z3 shaping amplifier is similar to the Z2 amplifier except for the following differences. The Z2 playback is amplified by a standard non-inverter and then is "anded" with P3. With this arrangement only the Z2 pulse that occurs at the end of the P3 period is applied to the shaping amplifier. This accomplishes the purpose of selecting every fourth high-speed clock pulse for use as a low-speed clock and establishes the proper relationship between the low-speed clock and the phase pulses.

The shaping amplifiers are both constructed on a single printed circuit board located in position D-9.

THE dZ2 CIRCUIT

The dZ2 circuit is used in the production of an early clock pulse. The circuit generates an early clock by delaying the regular Z2 clock enough so that it can be used as an early clock the following bit time. The delayed clock is not a narrow pulse like the original clock, but since only the positive rise is used, the shape of the rest of the pulse is not important.

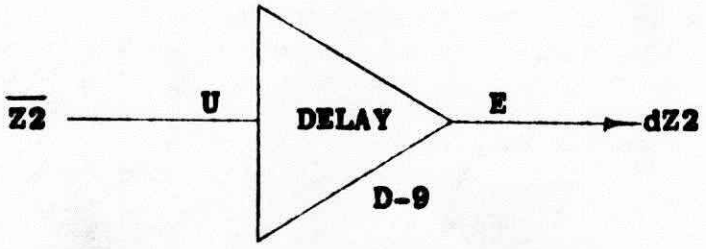


Fig. 443. dZ2 Symbol

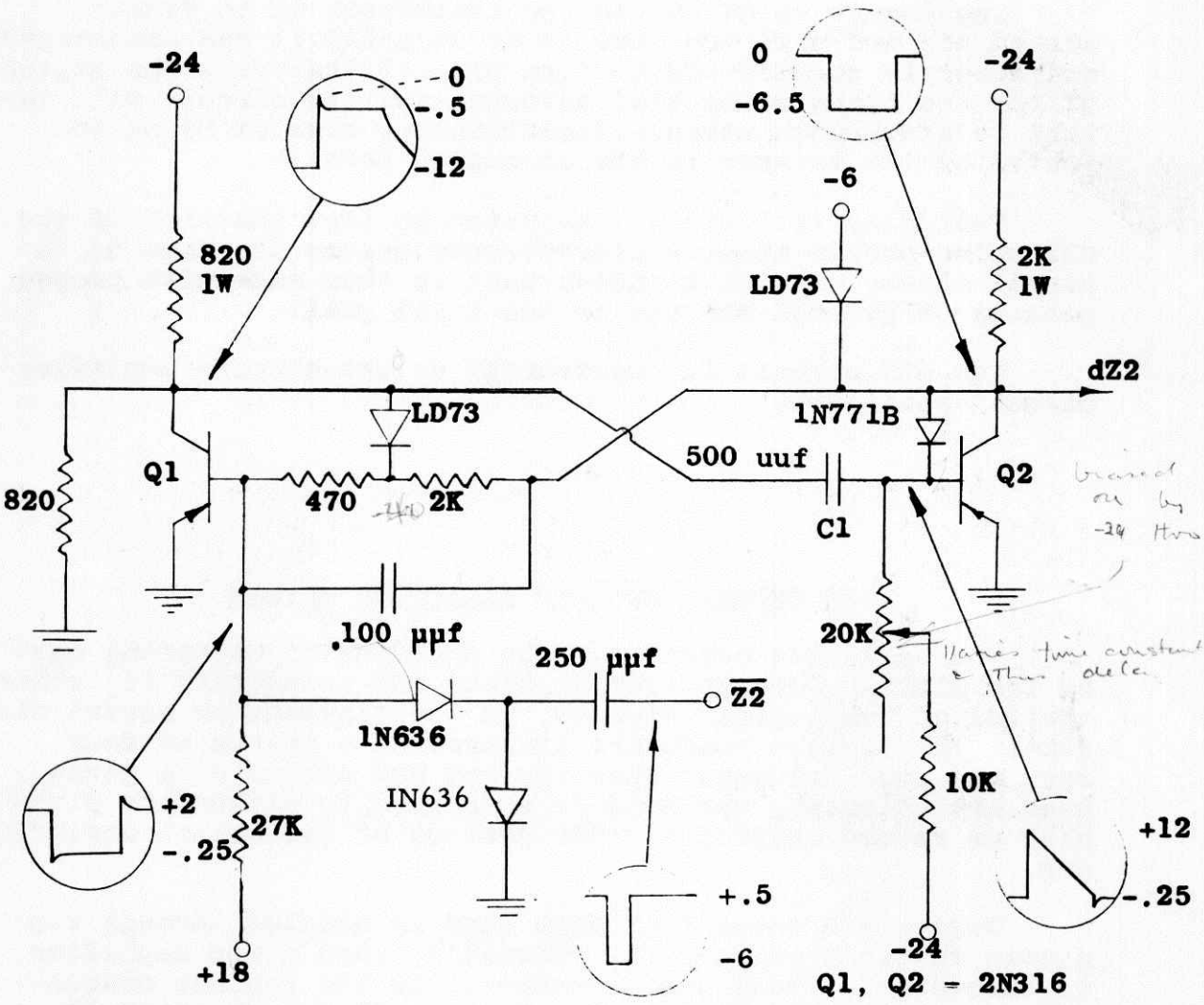


FIG. 444. dZ2 CIRCUIT DIAGRAM

In the steady state condition, Q1 is turned off and Q2 is turned on. The trigger circuit operates the same as that in the C10 circuit. The Z2' pulse goes high first and must go low to trigger the circuit. During the steady state condition the capacitor C1 charges to about 12 volts. This is due to one side being clamped to ground and the other side being connected to a -12 volt point on a voltage divider. When a trigger occurs, Q1 is turned on, and its collector voltage becomes clamped to ground. The rise in voltage at the collector of Q1 is transmitted to the base of Q2 turning that transistor off. The collector voltage of Q2 drops to -6 volts and is clamped at that level by a diode. The negative going voltage is transmitted to the base of Q1 keeping that transistor turned on.

The charge on C1 causes the transistor Q2 to remain turned off and will continue to do so until it has discharged sufficiently to allow Q2 to turn on. At that time the states of the two transistors will reverse, and the circuit will revert to its stable state. The discharge time of C1 is adjusted by the trimpot in the discharge path.

The delay is nominally adjusted so that the rise of the dZ2 pulse occurs about 3 microseconds before the rise of the normal clock. The final adjustment is then made with proper sensing of general storage as the final goal.

The dZ2 circuit is constructed on the shaping amplifier circuit board D-9.

THE GENERAL STORAGE SELECTION MATRIX

The selection matrix has the function of selecting one of the sixteen general storage heads and connecting it, under control of the logical signals, to the playback or record circuit. The sixteen heads are arranged in a matrix of four rows and four columns. When the row and column of a given head are selected, the head is connected to either the playback or record amplifier under control of two switch amplifiers.

Figure 445 shows that each head is coupled through two diodes to two transformers. Normally, when a row amplifier is turned off, those heads connected to the row are disconnected because the diodes will be back biased by about 18 volts from the row amplifier output. As the output of a head is a very low level signal, it cannot overcome this back bias. When a column amplifier is turned off, the voltage at its output is approximately -24 volts, which also back biases the head diodes connected to it. Three of the four column amplifiers and three of the four row amplifiers are always turned off. This back biases all the heads except the one which is at the intersection of the "on" row and column amplifiers. The column and row amplifiers, when turned on, are very low impedance paths to ground so that one half of the selected head is connected to one transformer and the other half is connected to the other transformer. When the row amplifier is turned on, its output is slightly negative, so the diodes are forward biased to make an easier path for the signal.

Since the heads serve the dual purpose of recording and playback, a provision is made to disconnect the playback amplifier while the record circuit is in use. The record switch amplifier grounds the input to the playback amplifier, and the playback switch amplifier turns off to prevent loss of record signal through a shorted winding.

CIRCUITS

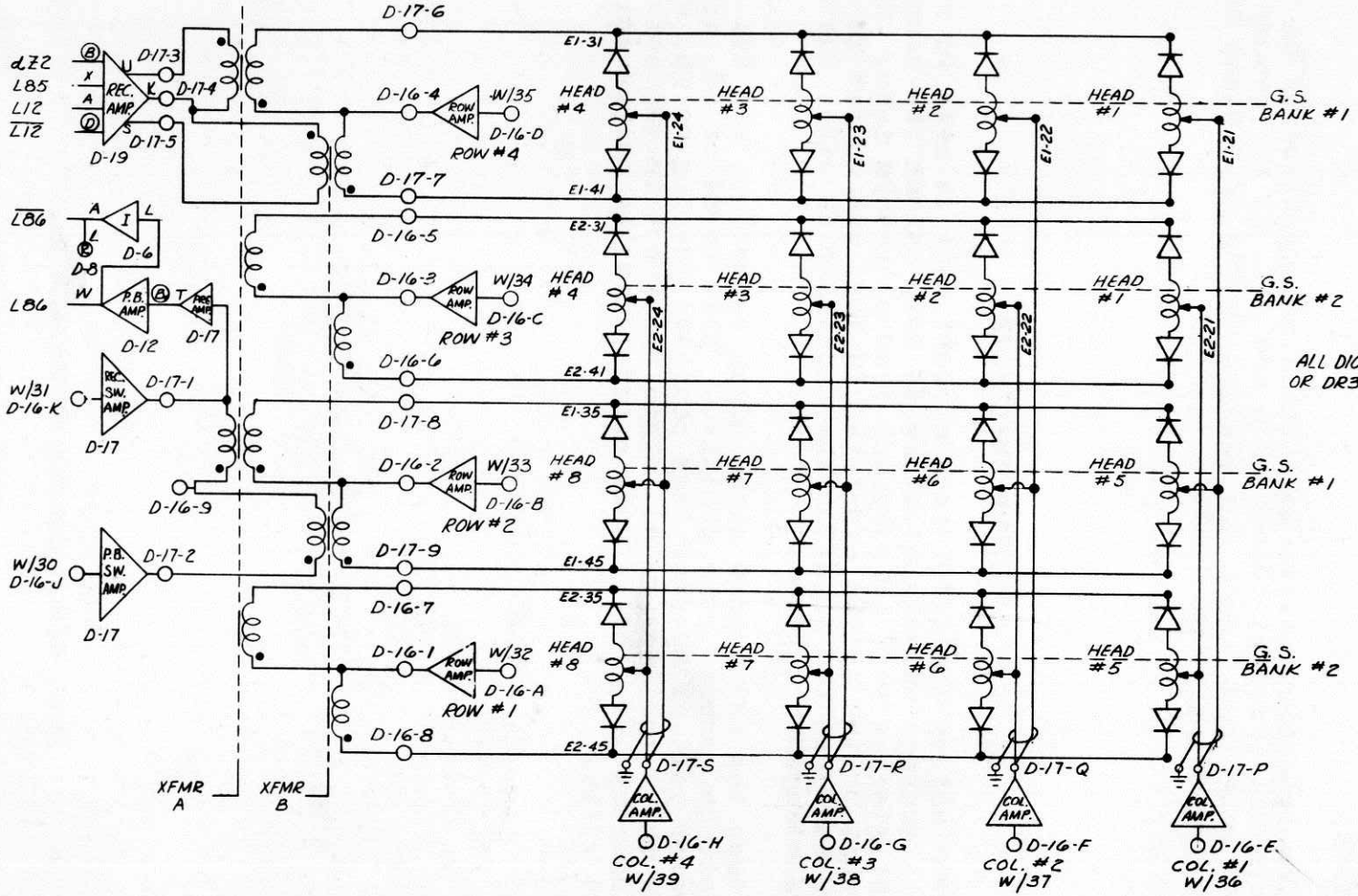


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FIG. 445 GENERAL STORAGE SELECTION MATRIX

B-579,043-A

4-43

When playing back, the situation is changed. The record switch amplifier is turned off, and the playback switch amplifier is turned on. This grounds one end of the transformer and ungrounds the input to the playback amplifier.

In addition to the selection amplifiers, there is playback pre-amp (Page 4 - 48) which is used to provide additional gain before the signal is amplified by the general storage amplifier.

The selection matrix amplifiers are constructed on the two vertical terminal boards, D16 and D17, in the memory rack, and the selection diodes are mounted on the drum plate next to the general storage heads.

COLUMN AMPLIFIER

The column amplifier is a circuit that is used in the general storage selection matrix to help select the proper general storage head to playback from or record into. When the input to the column amplifier is low, the output is -24 volts, and when the input to the amplifier is high, the output is clamped to ground.

When the input goes high, Q1 is turned on, and its emitter voltage becomes more positive. This turns on Q2, and its collector voltage becomes less positive turning on Q3, which clamps the output to ground. When the input to the column amplifier is low, the reverse occurs, and the output voltage is -24 volts.

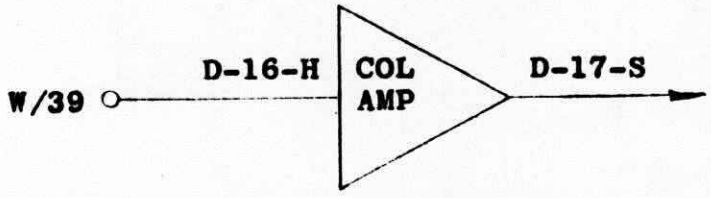

FIG. 446. COLUMN AMPLIFIER SYMBOL

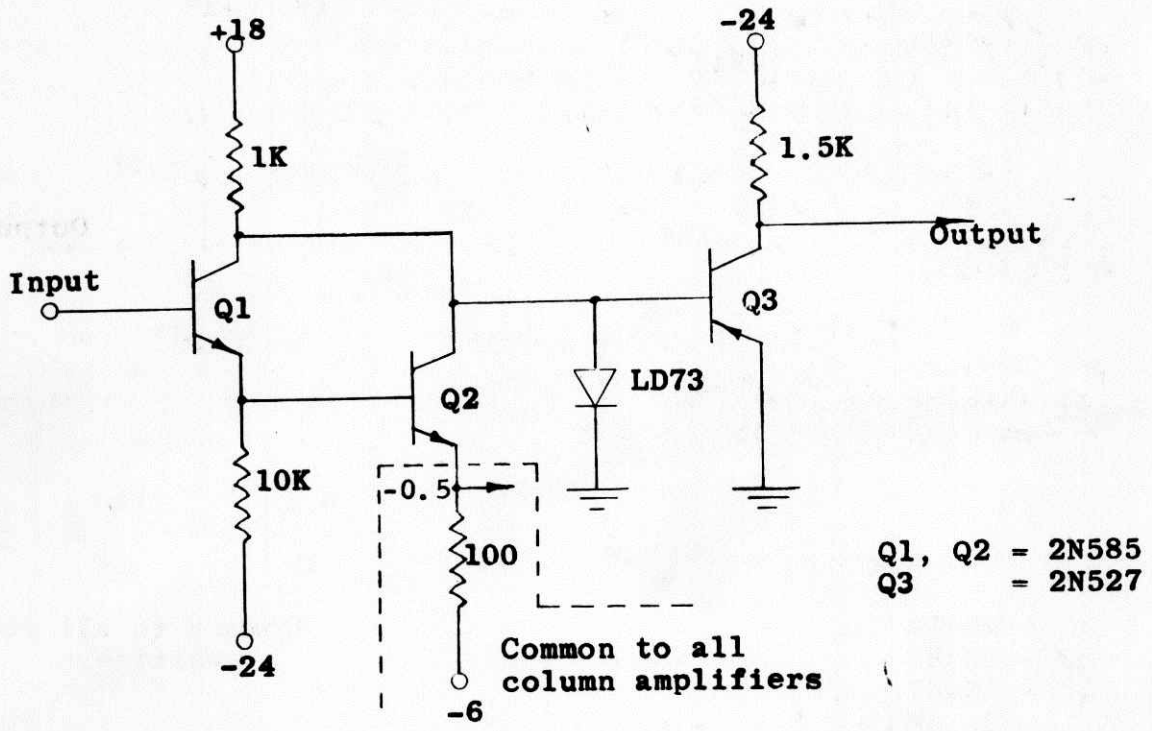

FIG. 447. COLUMN AMPLIFIER CIRCUIT

ROW AMPLIFIER

The row amplifier is a circuit used in the general storage selection matrix to help select the proper general storage head to playback from or record into. When the input to the row amplifier is high, the output voltage will be -0.5 volt, and when the input is low, the output will be +18 volts.

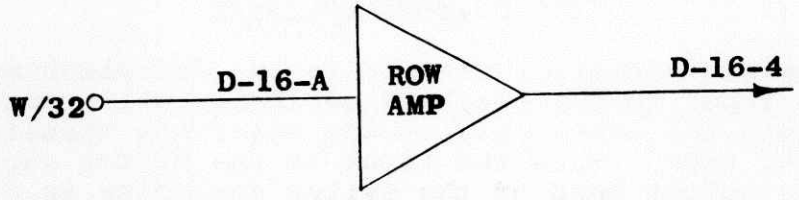

FIG. 448. ROW AMPLIFIER SYMBOL

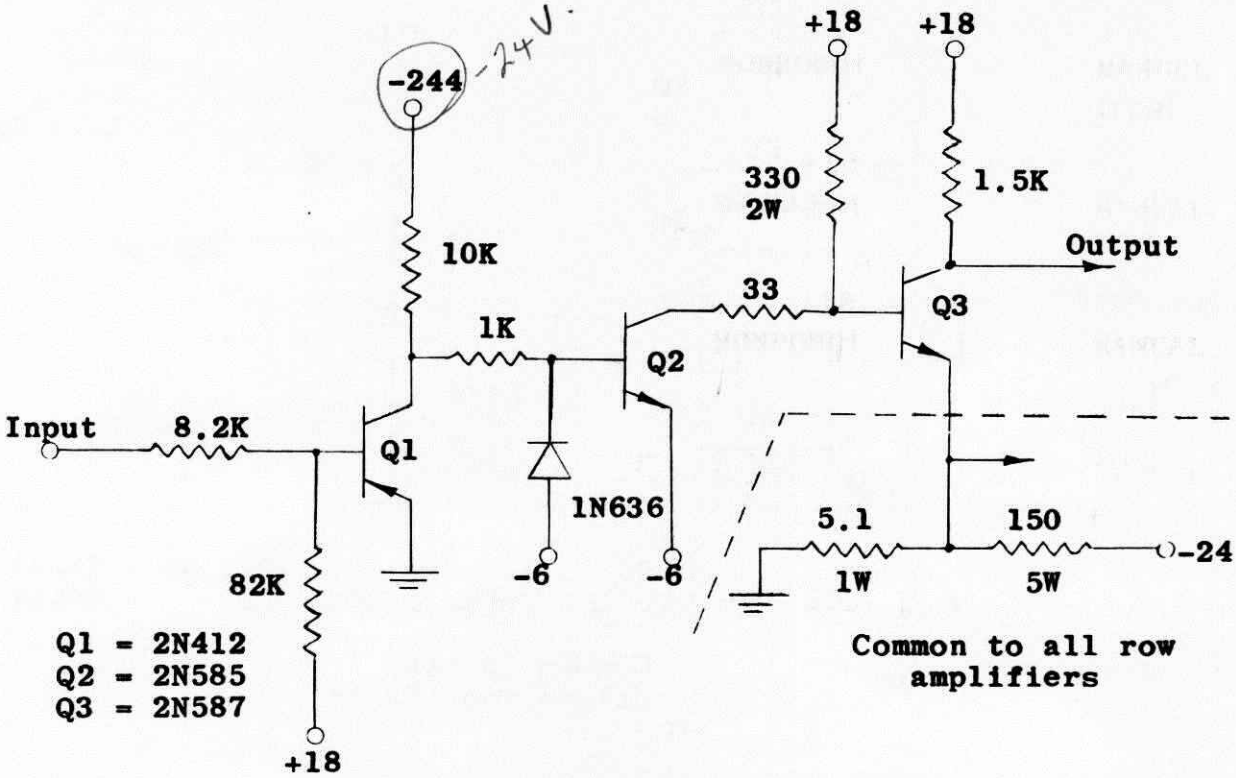

FIG. 449. ROW AMPLIFIER CIRCUIT

When the input goes high, Q1 turns off which causes the Q1 collector voltage to go more negative. This negative voltage on the base of Q2 turns Q2 off, which causes the Q2 collector voltage to rise turning on Q3. This causes the collector voltage of Q3 to be clamped to the voltage existing at the junction of the 5.1 and 150 ohm voltage divider which is approximately -0.5 volts. When the input to the row amplifier is low, the reverse occurs, and the output voltage is +18 volts.

THE SWITCH AMPLIFIER

The switch amplifier is used in the selection matrix to ground the input to the playback amplifier while recording and to ground the other side of the selection transformer when playing back. When the input to the switch amplifier is low, the output lead of the switch amplifier is effectively an open circuit to ground. When the input is high, the output lead is grounded.

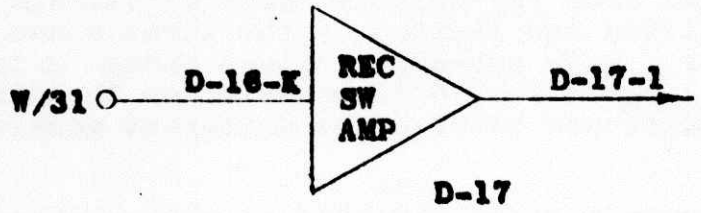

FIG. 450. SWITCH AMPLIFIER SYMBOL

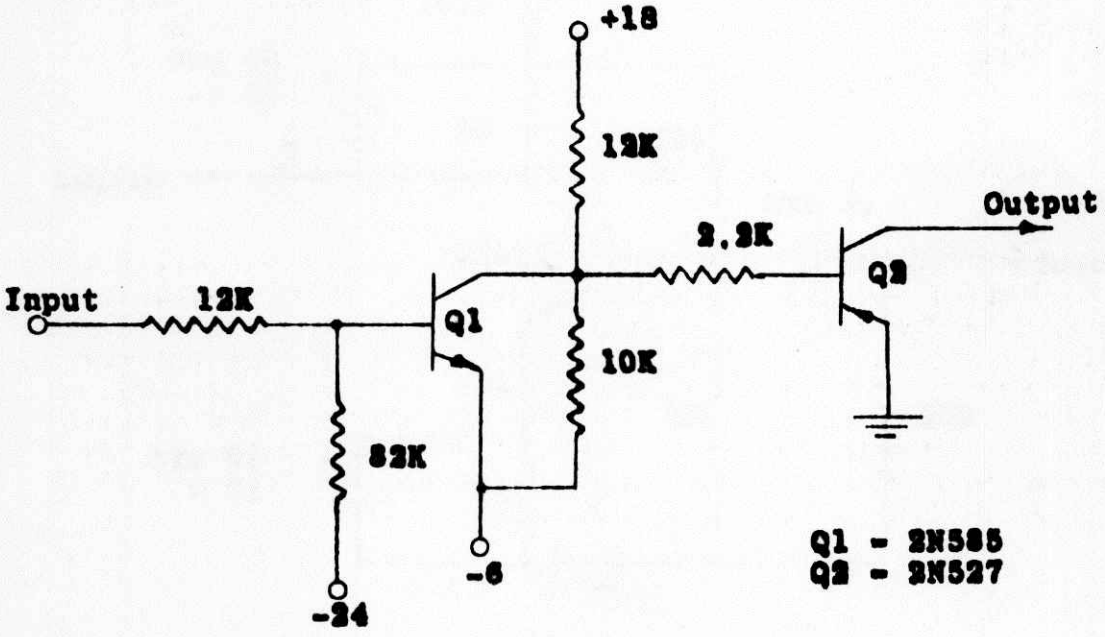

FIG. 451. SWITCH AMPLIFIER CIRCUIT

When the input to the switch amplifier goes high, transistor Q1 is turned on causing its collector voltage to become less positive. This turns on Q2, which grounds the output lead. If the input signal is low, Q1 is turned off, and the positive collector voltage of Q1 turns Q2 off. This makes the output lead an open circuit.

THE GENERAL STORAGE PLAYBACK PRE-AMP

The general storage playback pre-amp is used to amplify the playback signal from the selected general storage head before it is amplified and limited by the first stage of the playback amplifier. This pre-amp provides enough gain to allow the playback amplifier to compensate for the differences in signal amplitude between the different general storage heads.

The amplifier is a Class A amplifier with a phase reversal between the input and output.

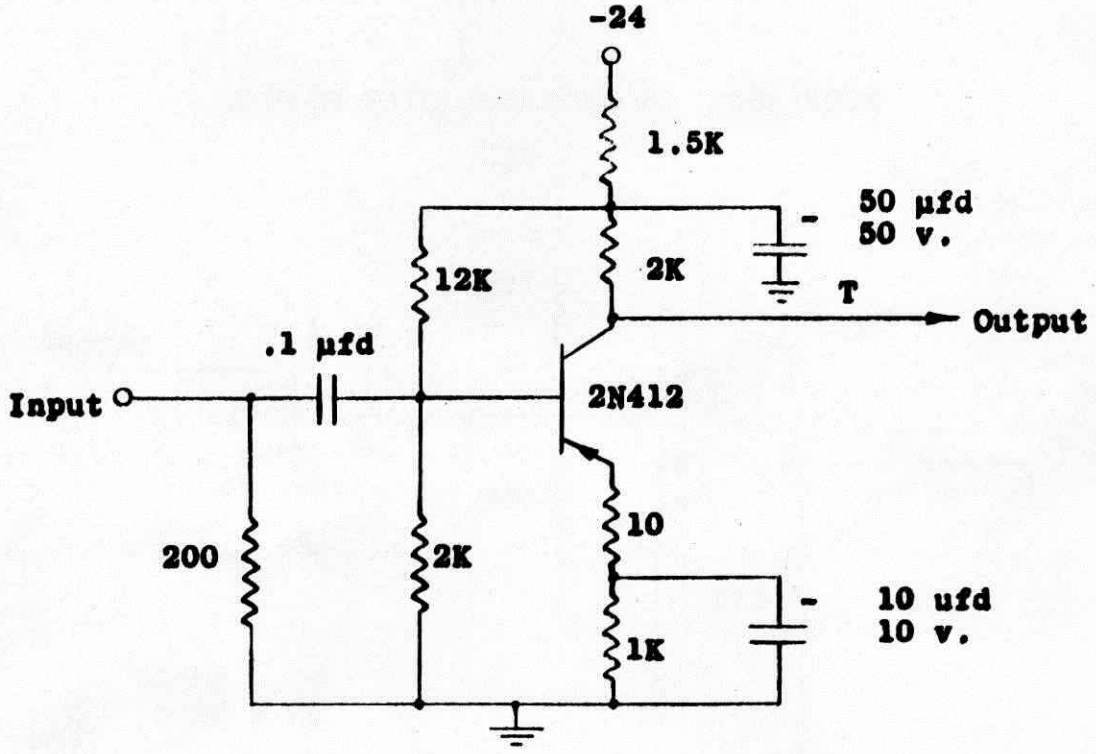

FIG. 452. GENERAL STORAGE PLAYBACK PRE-AMP

THE G20 CIRCUIT

A circuit is provided in the computer which prevents recording on the drum if the record -24 volt supply is low enough to cause a bad recording. This circuit prevents recording by holding the record gates (L85 and K37') low if the record supply is less than about -19 volts.