NANOCOMPUTER® TRAINING SYSTEM TECHNICAL MANUAL

2nd EDITION

W A R N I N G ! !

We don't want to spoil your enjoyment of this new world of computing but we must warn you of new dangers when using these complex and sensitive electronic components.

THE CIRCUIT BOARDS

Although the boards are made of tough fibre-glass, the fine circuit tracks on both sides can be damaged by physical shocks or flexing/bending the board. Take care when first unpacking and when plugging or unplugging not to put too severe a strain on the circuit boards.

THE COMPONENTS

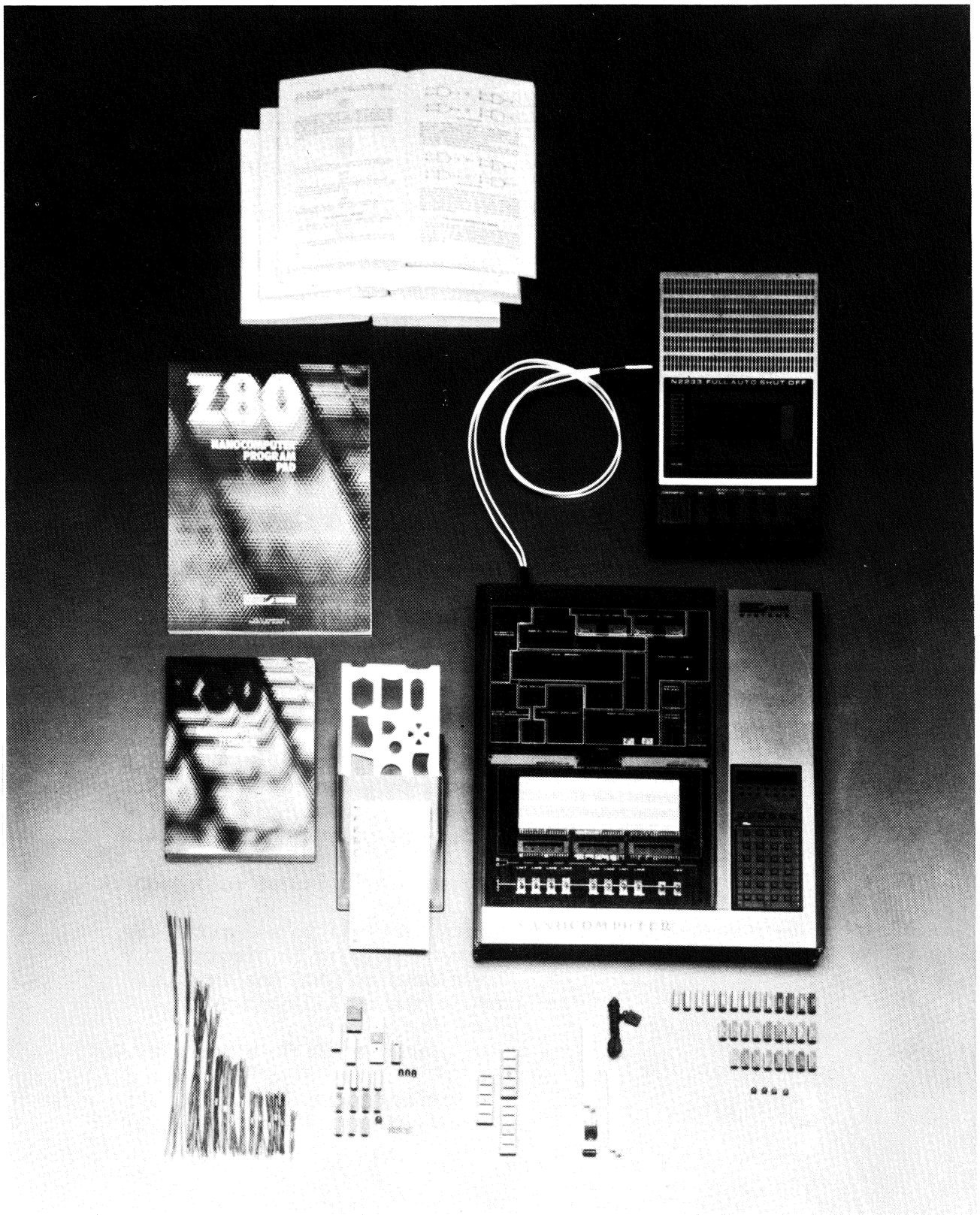
Many of the components on the boards are MOS (Metal-Oxide-Silicon) IC's. These IC's are sensitive to static electricity.
Do not unplug any IC's from the board without taking the proper precautions.
We recommend you only handle MOS circuits on a metal topped table which is earthed, use only earthed soldering irons and avoid clothing materials which generate static electricity.
Don't, of course, operate the circuit boards on a metal surface which could short circuit components.
When handling the NBZ80 or NEZ80 boards, particularly when inserting or removing external connections ensure that there are no high voltages present which can damage the circuit components.

Take care and you will enjoy the new world of the Z80.

N A N O C O M P U T E R T R A I N I N G S Y S T E M

ENCLOSURES

* Electrical diagrams, list and lay-out CLZ80/NC components
* Dimensions of CLZ80/NC and NEZ80 boards and of keyboard/display
* Electrical diagrams, list and lay-out of NEZ80 components
* DN 314
* DN 340


Z80
N2233 FULL AUTO SHUT OFF

NANOCOMPUTER® TRAINING SYSTEM

Welcome to the world of the best 8-bit microprocessor, the SGS-ATES Z80(*).

The Z80 family of LSI components consists of :

Z80 CPU - Central processing Unit

Z80 PIO - Peripheral Input/Output

Z80 CTC - Counter Timer Circuit

Z80 SIO - Serial Input/Output

Z80 DMA - Direct Memory Access

The Nanocomputer Training System was designed, using members of this family, for education and training on the Z80 microprocessor.

The system covers :

* programming in Z80 assembler language

* digital electronics for microcomputers

* interfacing between CPU, memories, PIO and CTC.

A full set of documentation in three volumes, covering all these subjects, is provided with the system to meet all the needs of the student and educator.

® Nanocomputer is a registered trade mark of SGS-ATES.

(*) Z80 is a registered trade mark of Zilog Inc.

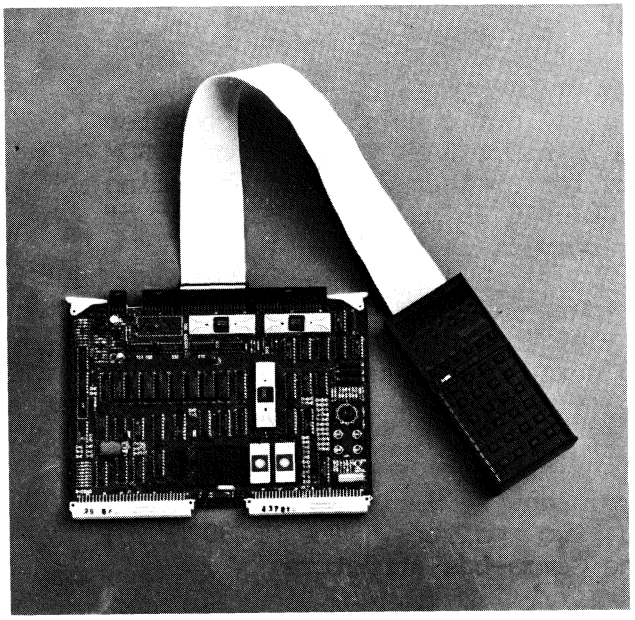
The Nanocomputer training system components, hardware and sofware support are:

Type	Description
H a r d w a r e	
NBZ80	Z80 based Nanocomputer formed by : - CLZ80/NC board with 4Kb of RAM, 8Kb of EPROM with monitor programs (NC-Z9 - NKZ80 keyboard-display - Technical manual - Vol. 1 "Z80 Microprocesssor Book 1 Programming"
NBZ80-A	As the NBZ80 plus the power supply NSZ80
NBZ80-B	As the NBZ80 plus the NPZ80 card frame (including power supply)
NBZ80-S	As the NBZ80-B plus the NEZ80 board, the K1Z80 wire kit and Vol. 3 "Z80 Microprocessor Book 3 Interfacing"
UPZ80-S	Upgrading kit : alows upgrading from NBZ80 to NBZ80-S Includes : - NEZ80 board - NPZ80 supply and card frame - W15Z80 connection cable - Vol. 3 "Z80 Nanobook Interface" - K1Z80 wire kit for experiments
NBZ80-HL	As the NBZ80-S system plus the video terminal, aphanumeric keyboard and guide to BASIC language
UPZ80-HL	Upgrading kit : allows upgrading from NBZ80-S to NBZ80-HL
NEZ80	Interface hardware experiment board
TVZ80	12" video monitor for use with the video terminal
RCZ80	Cassette recorder with automatic control (requires cable W10Z80 for connection to system)
SSZ80	Serial printer. Centronics model 779 for standard 8 1/2" paper with 80 - 132 coloums (60 - 96 char/sec)

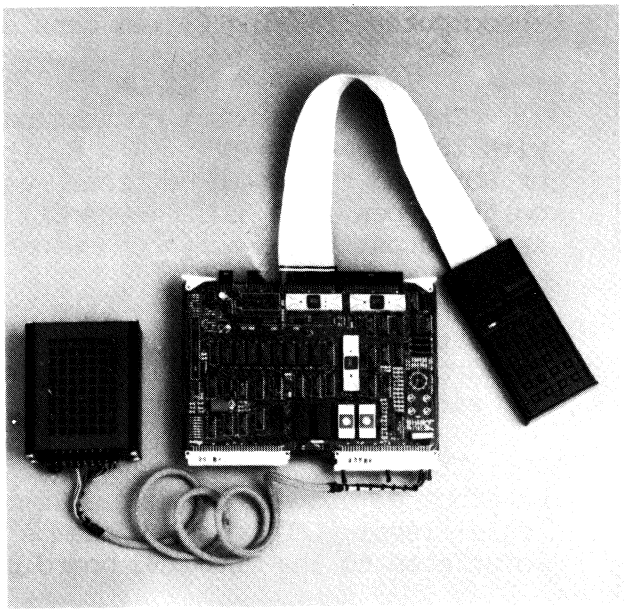
Type	Description
Accessories	
NSZ80	Mini supply for the NBZ80
NPZ80	Card frame for CLZ80/NC and NEZ80 boards with supply incorporated
KNZ80	Conversion kit. Allows conversion of a CLZ80/NC board to a CLZ80 4/2 microcomputer. Includes : UART, DC-DC converter, control PROM, MO-Z monitor on EPROM and connector.
NKZ80	Keyboard-display complete with connection cable
K1Z80	Cable kit for connecting circuits to NEZ80 board.
K2Z80	Passive semiconductor components for NEZ80 board
K3Z80	Three 40-pin sockets for NEZ80
K4Z80	Connectors for upgrading Gamma-bus on NEZ80 board
K5Z80	Active and passive components kit for experiments described in training book Vol. 2 "Z80 Microprocessor Book 2 Digital Electronics"
W6Z80	Cable for connecting NBZ80-HL to antenna input of a commercial TV
W8Z80	As W6Z80 but for input of a TV monitor
W10Z80	Cable for connecting a cassette recorder to the NBZ80/NBZ80-S/ NBZ80-HL
W12Z80	Cable for connection of printer SSZ80 to the NBZ80-HL system
W15Z80	Cable for connecting NEZ80 to CLZ80/NC PIO ports C and D.

Type	Description
Software	
NC-Z	2K monitor for NBZ80 supplied on two M2708 EPROMs or one M2316E ROM.
NE-Z	2K experiment software for the NBZ80-S and NBZ80-HL systems. Available on two M2708 EPROMs or one M2316E ROM.
BAS-Z/N	8K BASIC interpreter for the NBZ80-HL system. Available on 4 M2716 EPROMs
NCHESS	4K chess program supplied in two EPROM/ROM's. Six levels of play.
Manuals	
1	Z80 Microprocessor Book 1 Programming
2	Z80 Microprocessor Book 2 Digital Electronics
3	Z80 Microprocessor Book 3 Interfacing

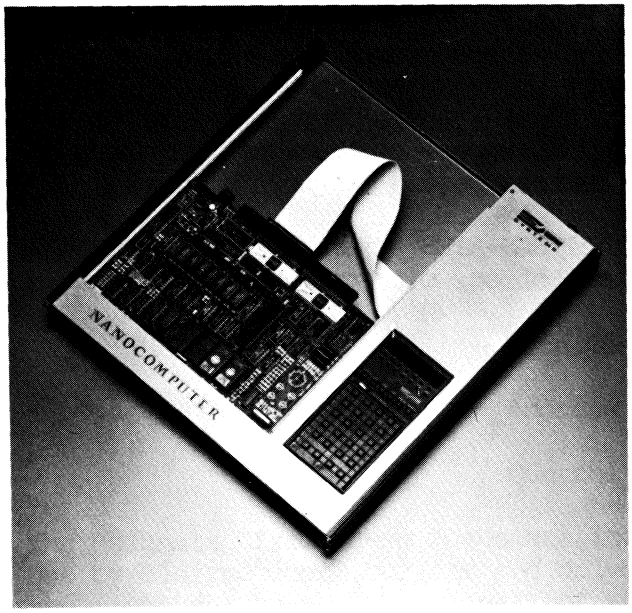
Enquiries about all of these components, accessories and books should be made to your local SGS-ATES distributor or Sales Office.



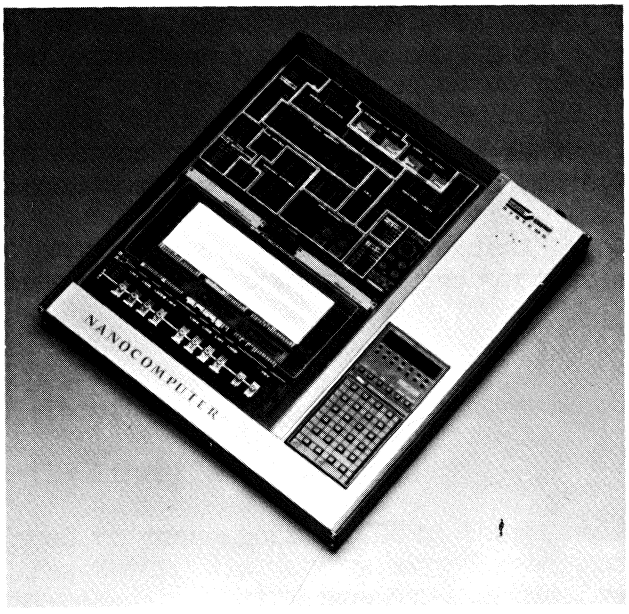
NBZ80



NBZ80-A



NBZ80-B



NBZ80-S

(1) INTRODUCTION TO NANOCOMPUTER TRAINING SYSTEM

The Nanocomputer Training System consists of :

The CLZ80/NC board containing a small but complete microcomputer with Z80CPU, 4K bytes (4K x 8 bit) of dynamic RAM, 2K bytes of EPROM or ROM (and two or three other sockets for another 2K or 6K depending on the types of EPROM/ROM used), 2 x Z80 PIO chips giving 32 lines of input/output and a buffered Gamma-bus compatible interface.

The input/output of the Nanocomputer is provided by the NKZ80 keyboard display (pocket calculator style) including a display with 8 hexadecimal digits, 14 indicators, 16 hexadecimal keys and 14 keys for various control functions.

The NEZ80 experiment board containing a special solderless breadboard, connectors to the Gamma-bus signals, 8 logic switches, 8 logic level LED display lamps and two pulsers. The NEZ80 board interfaces to the CLZ80/NC board on the Gamma-bus structure.

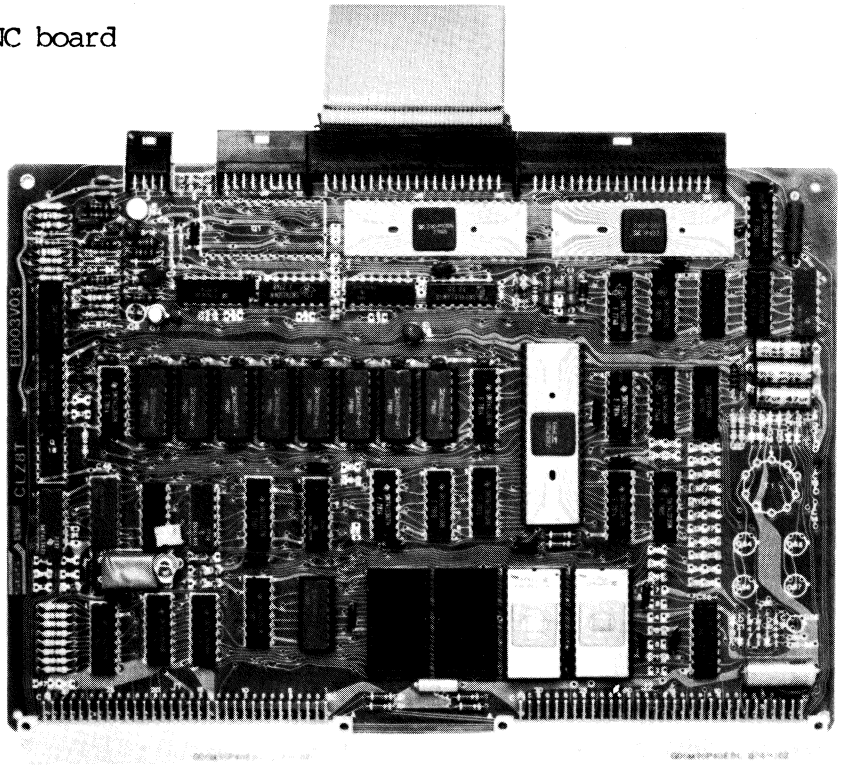
The NPZ80 card cage, for boards CLZ80/NC and NEZ80, with AC power supply incorporated.

The RCZ80 cassette recorder with connection cable W10Z80, two NE-Z ROMs with programmed experiments and various component kits.

Together these parts form a complete NBZ80-S (Super) or Nanocomputer Training System, as shown in the photograph on the previous page.

Note that 'Gamma-bus' is the name of the SGS-ATES standard European Z80 microcomputer bus structure and is used in all of our microcomputer products.

(1.1) CLZ80/NC board



CLZ80/NC BOARD PHOTOGRAPH

The CLZ80/NC board of the NBZ80 Nanocomputer is in double Eurocard format with a Z80 CPU. The microcomputer is assembled on a double sided printed circuit board.

The board carries 4K RAM and 2K EPROM or ROM but can be expanded to up to 16K RAM and 8K EPROM/ROM by modifying some links on the board. The CLZ80/NC board is also laid out for easy upgrading to a CLZ80 microcomputer using kit KNZ80 which adds a USART, DC-DC converter and other components as well as the MO-Z monitor software.

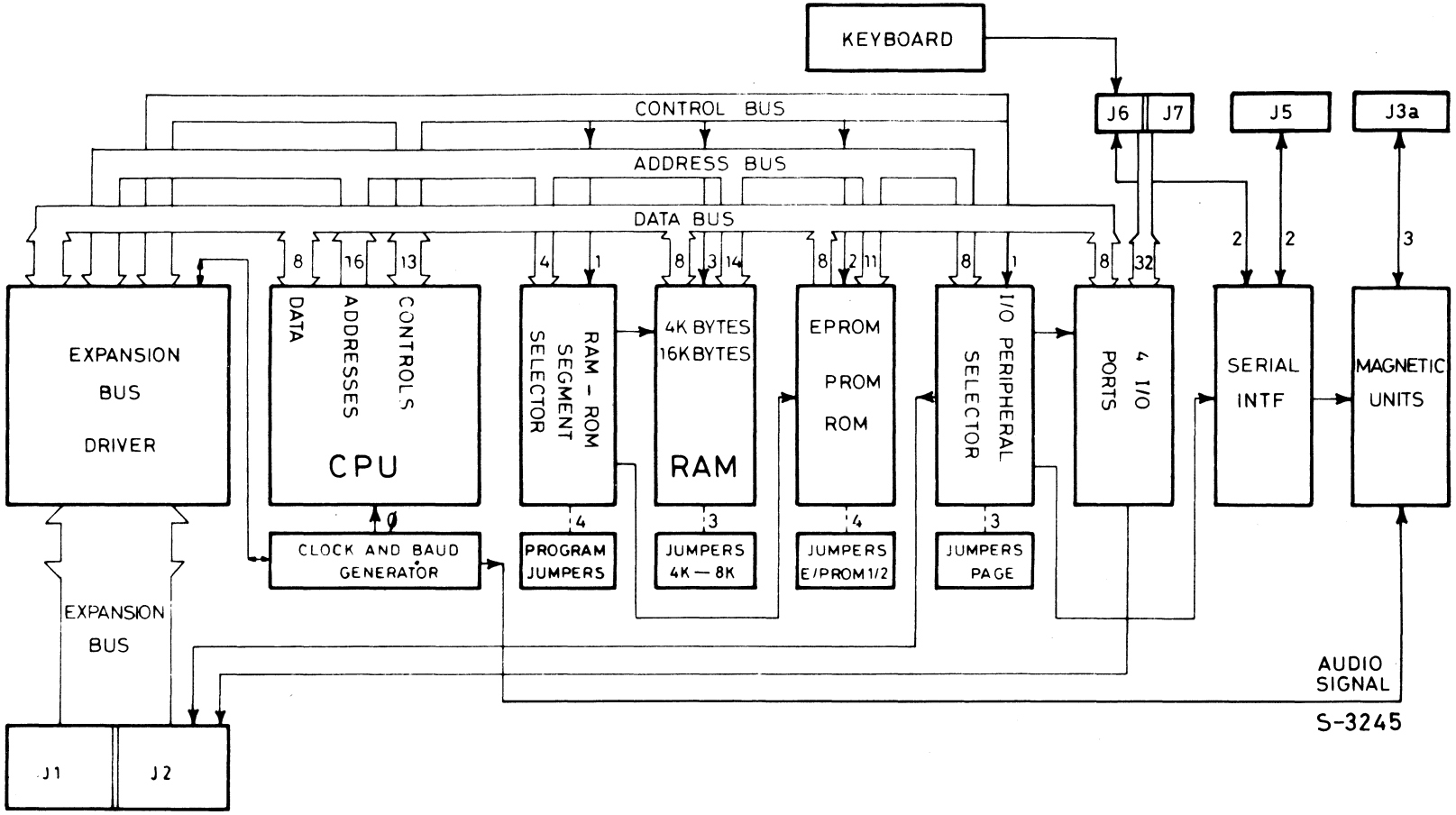
The internal bus structure consists of three buses :

Data Bus (8 bits)

Address Bus (16 bits)

Control bus (13 lines)

The signals from these buses are interfaced to connectors J1/J2 of the Gamma-bus by bidirectional buffers and drivers. The Z80CPU is connected directly to the internal buses. The signal for the NMI (Non-Maskable Interrupt) comes from the BREAK key of the keyboard via connector J6. The RESET signal comes in the same way from the RESET key. The Z80 CPU uses a 2.4756MHz clock (the odd frequency is because in the upgraded CLZ80 version this clock signal is divided down to obtain the various transmission and reception speeds (baud rates) for



CLZ80-NC BLOCK DIAGRAM

serial communications with the USART).

The ROM and RAM memories can be mapped anywhere in the range 0-FFFF(Hex), 0-64K(Dec), address space by the RAM and ROM memory segment selector. The various partitions are selected by links on the board.

The addresses of the ports of the PIO's are determined by the "device select" and can be mapped via links in segments of 32 addresses inside the space 0-FF (Hex) 0-256 (Dec).

The user who wants to use the board with his own programs (without NC-Z monitor) has freedom of memory mapping and address assignment of I/O ports.

The reset circuit provides a small program in ROM with a jump instruction which is executed by the CPU when the Reset key is pressed. The Reset key resets the CPU (see Z80CPU Technical Manual for details) and activates the Reset Circuit. The jump made is to the start address of the NC-Z operating system program memorized in EPROM or ROM.

An interface circuit for a serial terminal suitable for communications in RS-232 mode, in 20mA current loop or at TTL levels is provided. Using the TTY<->CASS switch on the keyboard display it is also possible to select the Audio Cassette interface.

The serial signals for both "TTY" and "CASS" are generated by the software and the input/output is taken from the PIO (Q2) port A.

A control signal for start-stop of the cassette recorder is provided by the software. The standard NBZ80 Nanocomputer with NC-Z software controls the RCZ80 cassette recorder connected to connector J3.

(1.2) NKZ80 KEYBOARD/DISPLAY

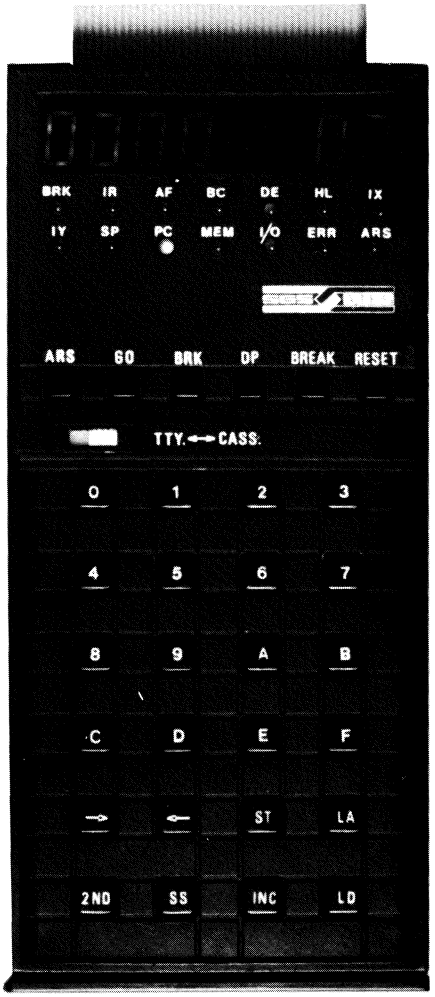
The NBZ80 Nanocomputer with NC-Z software program uses the portable NKZ80 keyboard/display as input/output unit.

The keyboard display enables the user to communicate in hexadecimal machine language with the microcomputer.

The 8-digit display provides data and address information.

The single LEDs indicate the registers displayed. The keys allow the input of data and addresses as well as the activation of various control functions.

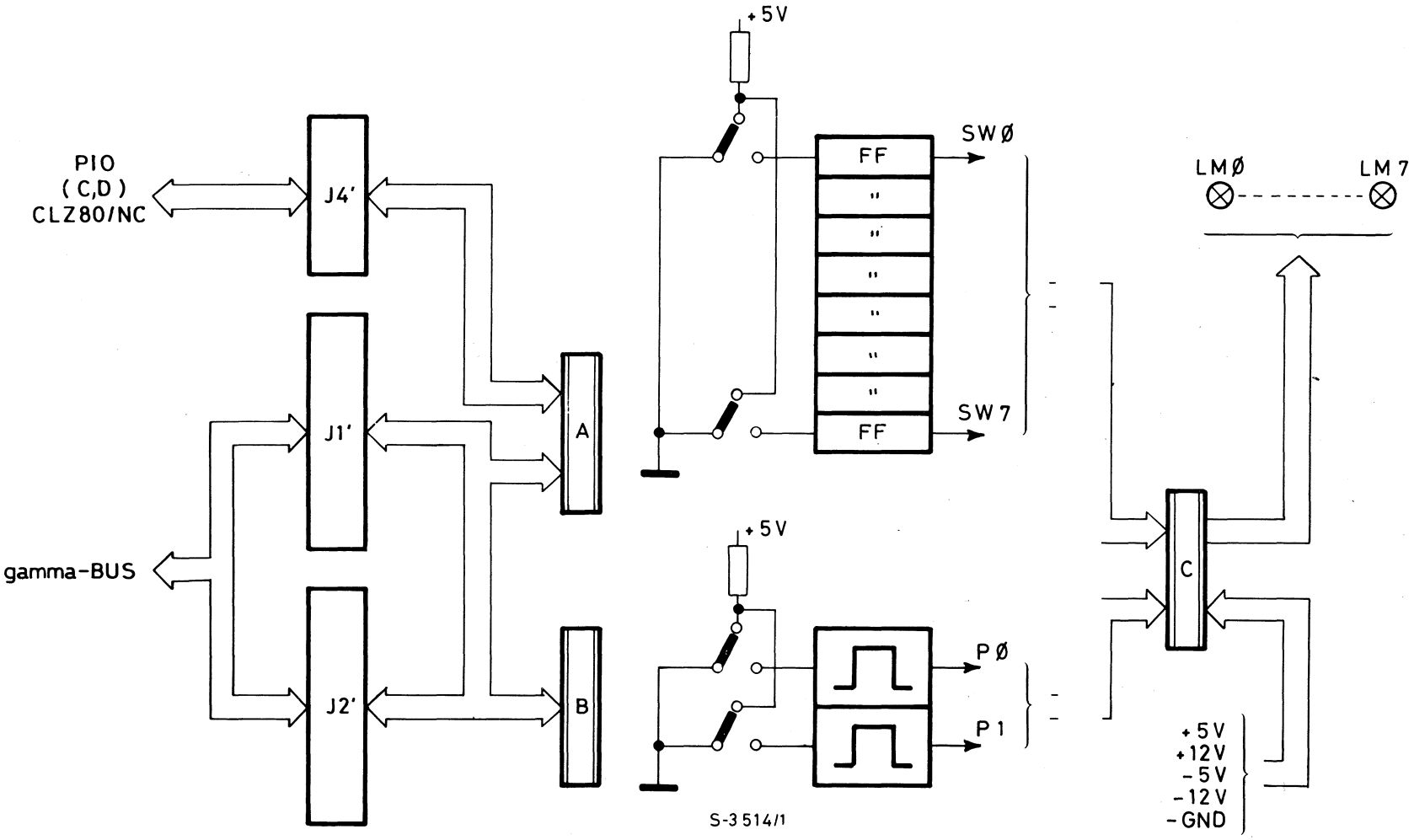
The keyboard/display is connected to connector J6 of the CLZ80/NC board. The female connector on the flat cable has pin 1 identified by an arrow.



NKZ80 KEYBOARD/DISPLAY

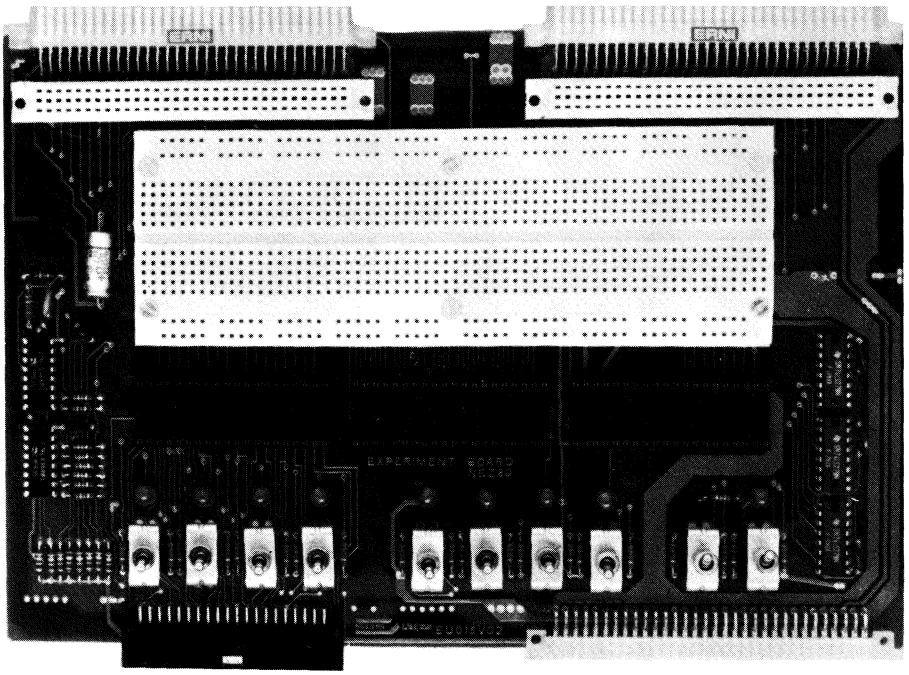
*** IMPORTANT ***

If the female connector is inserted the wrong way round the keyboard/displays can be damaged. There are arrowheads on the connectors indicating the correct orientation.



NEZ80 BLOCK DIAGRAM

(1.3) NEZ80 EXPERIMENT BOARD



NEZ80 BOARD PHOTOGRAPH, WITH SOCKETS K4Z80 FITTED

The NEZ80 experiment board has been designed to allow the user to carry out interface experiments using the signals available on the CLZ80/NC Gamma-bus together with an 8-bit word generated by 8 switches and two positive or negative strobe pulses generated by two spring loaded switches. It is also possible to display the logic level of 8 signals by means of LED lamps.

The NEZ80 board is in double eurocard format with a double side printed circuit board and contains :

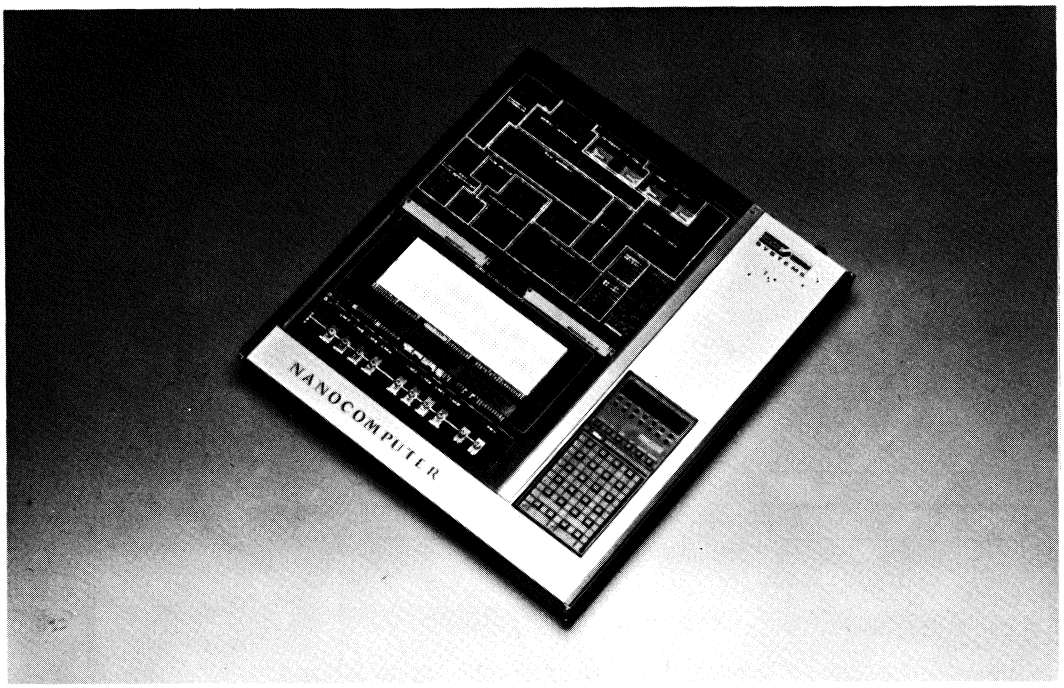
- a solderless board on which to insert user connections and components
- 8 debounced logic switches
- 8 LED logic indicators and drivers
- 2 debounced pulsers
- 2 sockets for experiment Gamma-bus to board interfacing
- 1 socket for signal interfacing and supplies

The signals coming from the CLZ80/NC Gamma-bus through connectors J1 and J2 are wired to two 40-pin sockets on the board.

The signals on J4 coming from the PIO (ports C and D) of the CLZ80/NC board via a multiway cable are also connected to the 40-pin sockets.

The 8 switches with debounce logic provide TTL logic levels '1' or '0' on the 40-pin sockets. Eight logic inputs to the LED drivers are available on the 40-pin sockets where logic level '1' = LED 'ON' and logic level '0' = LED 'OFF'.

(1.4) NANOCOMPUTER SUPER NBZ80-S



NBZ80-S PHOTOGRAPH

The Nanocomputer super NBZ80-S is a system formed by

CLZ80/NC + NKZ80	Nanocomputer with keyboard display
NEZ80	Experiment board
NPZ80	Card frame with supply incorporated

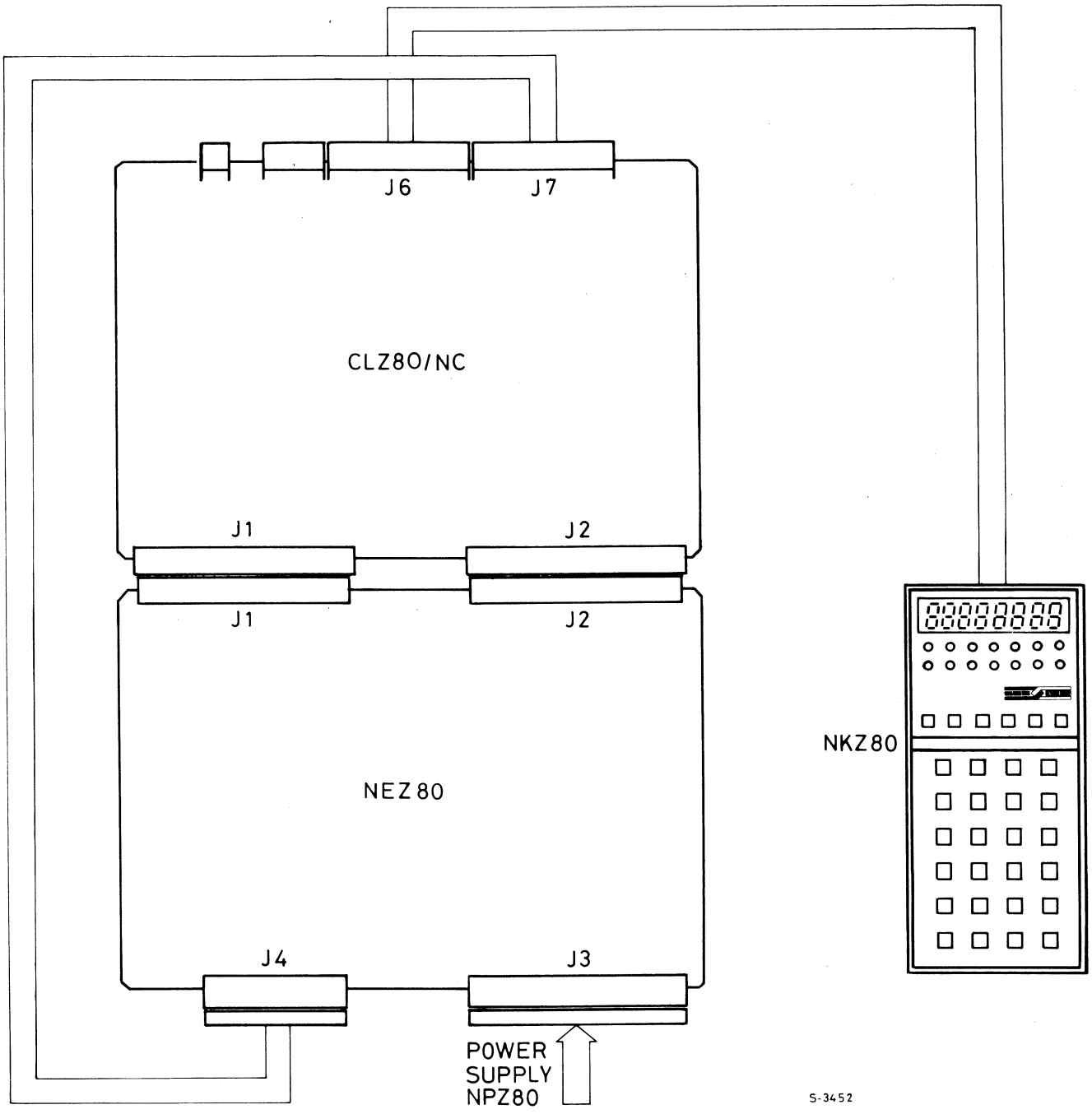
The two cards CLZ80/NC and NEZ80 are inserted in series into the flat card frame NPZ80.

A flexible multiway cable is used to carry PIO signals from connector J7 on the CLZ80/NC board to the NEZ80 board connector J4.

This cable has pin 1 of the female connector identified by an arrow. One end of the cable should be plugged into NEZ80 J4 before this board is mounted in the

card frame.

The supply for the NEZ80 board is provided on connector J3.

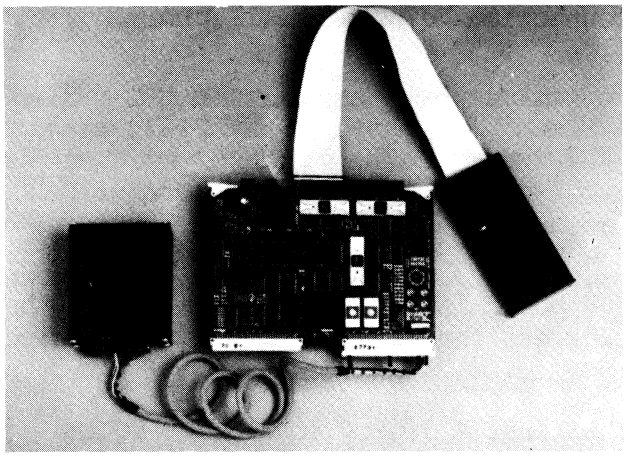


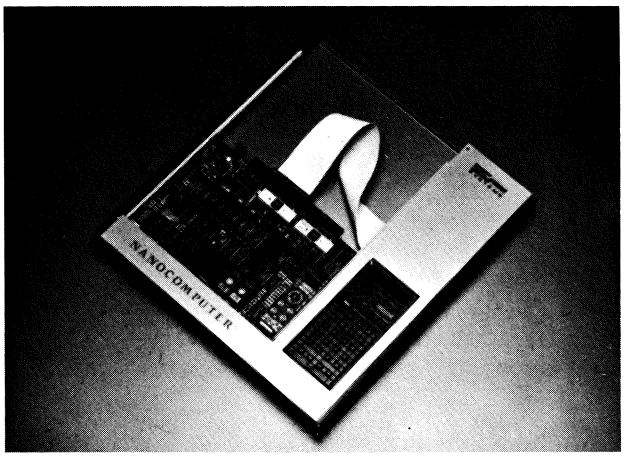
(2) INSTALLATION OF THE SYSTEM

For the single CLZ80/NC board a supply with the following ratings is required :

+ 5V +/- 5%	800mA
- 5V +/- 5%	200mA
+12V +/- 5%	100mA
-12V +/- 5%	100mA

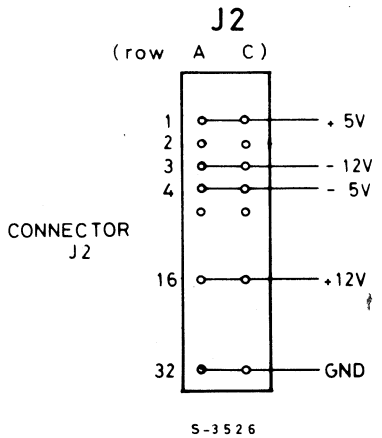
It is recommended to use the NSZ80 supply, which has an output cable provided and plugs directly into J2 (CLZ80/NC).





NBZ80A AND NBZ80B CONNECTIONS

If other supplies are used a suitable female connector is required to carry the supply to connector J2 of the Nanocomputer as shown



POWER CONNECTIONS

For the NBZ80-S verify that the boards are mounted correctly in the card frame and the Data input/Display station and PIO/NEZ80 cables are connected before powering up the Nanocomputer.

(2.1) AC MAINS CONNECTION

The NPZ80 and NSZ80 supplies have European standard cable. The supplies are internally adjusted for 220 - 240V operation (or 110 - 120V operation, if specifically requested by the user).

The supply connections are :

Green/Yellow	EARTH
Brown	SUPPLY live
Blue	SUPPLY neutral

It is strongly recommended that an earth connection be used at all times.

(2.2.) SYSTEM SWITCH-ON AND RESET

When the connections have been made

CHECK THEM AGAIN!

Then apply power to the system. If the NEZ80 board is included in the system the LED indicating the +5V supply will light. Press the RESET button once or twice to 'wake up' the Nanocomputer.

The display should light with 0000 in the first 4 digits from the left and a number displayed in the first 2 digits from the right. The PC LED indicator should be lit. If the display does not come on properly try again. Should the trouble persist call your supplier for help.

(3) CLZ80/NC - CIRCUIT DESCRIPTION

The schematic diagram of the CLZ80/NC Nanocomputer board is included at the end of this book in a fold-out form (EEU00325 and EEU00326). Also included is a component layout diagram (EEU00327). EEU00325 shows the CPU, Gamma-Bus interface, EPROM/ROM and RAM with relative control and timing circuits and the pin connections for J1 and J2. EEU00326 shows the input/output ports, interface circuits (RS232, TTL, 20mA current loop & cassette recorder interface) the initialization and clock generation circuits as well as the pin connections for J3, J5, J6 and J7 and the tables showing the links for selecting various configurations.

(3.1.) CPU

The Z80 CPU Q29 address bus outputs AD0 to 15 are connected to the 3-state buffers T74LS365/7 Q40/41/42. The local CPU is able to address the buffered address lines BAD0-15 (also called BA0-15 on the Experiment Board NEZ80) when $\overline{\text{BUSAK}}$ is not true. This is always the case for the Nanocomputer system but if the board were included in a system with more processors then another CPU could access the local memory after a $\overline{\text{BBUSRQ}}$ and acknowledgement by the local CPU ($\overline{\text{BUSAK}}$ true). The data bus D0-7 is buffered by T74LS365/7 Q44/46/30 for input and output transfers. These gates are enabled by $\overline{\text{DBOUT}}$ and $\overline{\text{DBIN}}$ described later.

The CPU $\overline{\text{HALT}}$ output is buffered by T74LS367 Q39 and the signal $\overline{\text{BHALT}}$ is available on the Gamma-Bus at J1-18C and on the Experiment board. The output drive is sufficient to drive a LED monitor lamp to indicate a software HALT State.

The CPU $\overline{\text{BWAIT}}$ (wait) input comes directly from the Gamma-Bus J2-26C. There is a pull-up resistor R52 of 910 ohms to +5V so $\overline{\text{BWAIT}}$ should be activated only by an open collector gate.

The CPU $\overline{\text{BINT}}$ (interrupt) input is derived from the PIO chips via the wired-or open collector gates, T7417 Q32 (EEU00326) or from an external interrupt input on the Gamma-bus J2-24c. There is a pull-up resistor R46 of 910 ohm to +5V so this input sould be activated only by an open collector gate.

The CPU $\overline{\text{BNMI}}$ (non maskable interrupt) comes from the Gamma-bus J2-23c and from the $\overline{\text{BREAK}}$ signal via the open collector buffer T7417 Q32. There is a pull-up resistor R45 of 910 ohm to +5V so $\overline{\text{BNMI}}$ should be activated only by an open collector gate.

The open collector buffer T7417 Q3 drives the $\overline{\text{BNMI}}$ input from the $\overline{\text{BREAK}}$ signal. The $\overline{\text{BREAK}}$ signal is generated by the keyboard 'Break' key which connects the $\overline{\text{BREAK}}$ input J6-18c to ground via a 47nF capacitor. This, together with the resistor R32 of 33 ohm, produces the narrow (<400nS) NMI pulse needed by the

CPU.

The CPU $\overline{\text{RESET}}$ signal is generated from the $\overline{\text{BRESET}}$ input on J1-28c. J6-4 or J7-4 In the Nanocomputer system the 'RESET' key on the keyboard connects J6-4 via a 47nF capacitor to ground to produce a reset pulse. This pulse is inverted by the T74LS14 Q11 and stretched by the 1KpF capacitor on the output of the inverter Q11 pin 2 to generate the CPU reset pulse. Other reset signals can be sent to this line via open collector gates. The $\overline{\text{BRESET}}$ line is protected from overvoltage transients by D8/C7/D9. it is pulled up by a 910 ohm resistor R17 to +5V so this input should be activated by open collector IC drivers only.

Finally the CPU $\overline{\text{BBUSRQ}}$ (Bus request) comes from the Gamma-Bus J2-25c. There is a pull-up resistor R53 of 910 ohm to +5V so $\overline{\text{BBUSRQ}}$ should be activated only by an open collector gate.

The 2.4576 MHz CPU clock comes from the clock generator F4702 Q34.

(3.2.) Gamma-Bus interface

The Gamma-Bus interface is a complete set of buffered input/output signals that enable the board to be used in bus orientated microcomputer systems For a complete definition of the pin connections see chapter 5 and for the signal specifications and timing see also chapter 5.

The T74LS365 and 367 gates Q40/41/42/45/46 and Q30/39 provide the bus buffering for the Gamma-bus signals.

The address bus BAD0-15 (the same as BA0-15) and the memory and I/O control signals $\overline{\text{BMREQ}}$, $\overline{\text{BIORQ}}$, $\overline{\text{BRD}}$, $\overline{\text{BWR}}$, $\overline{\text{BM1}}$ and $\overline{\text{BRFSH}}$ are disabled only by the local CPU $\overline{\text{BUSAK}}$ output.

The data bus outputs BD0-7 are enabled by $\overline{\text{DBOUT}}$ and the data bus inputs by $\overline{\text{DBIN}}$. These two signals are derived from the decoder T74LS156 Q12 which adjudicates the various requests both internal and external (via $\overline{\text{BUSAK}}$) for access to the bidirectional data and address buses.

The system clock (= 2.4576 MHz) and the FCU signal (equal to clock/8 = 307.2kHz), which is used in the upgraded systems (CLZ80) to drive the DC-DC power supply converters, are available on the Gamma-bus buffered by T74LS367 Q39.

The interrupt enable output IEO J1-13c is derived from the two Z80 PIO chips and can be used to extend the interrupt priority daisy chain with the on - board PIOs always defined as having highest (Q2) and next highest (Q3) priority

The partially decoded signals $\overline{\text{IOQ0}}$-3, $\overline{\text{IOE0}}$-3 and $\overline{\text{IOU0}}$-3 are described later under Device Select decoding.

(3.3.) EPROM/ROM

The Nanocomputer board is designed for using either 1Kx8 or 2Kx8 memories, for example M2708, M2716 or M2316E types. Both EPROMs, requiring multiple supplies, or ROMs, using single +5V supplies, can be used.

The sockets Q49-52 carry the memory chips and the electrical connections are selected by the jumpers, 1 to 8.

The CLZ80/NC board may be supplied in one of two versions, using either two M2708 (1Kx8) EPROMs for the NC-Z program, or using an M2316E (2Kx8) ROM. The alternative jumper connections are shown in the table which also gives the type of device supplied and the links.

The memories are addressed by the buffered address lines BAD0-10 and the data is read onto the internal data bus D0-7. In this way an off-board circuit (CPU or DMA for example) can read the memories as well as the local CPU (after enabling the data bus to the outside).

(3.4.) ROM CONTROL

Section A of the T74LS139 Q58 decoder is used to select, via jumpers 9 or 10, whether the ROM address segmentation is 4 or 8K. The CLZ80/NC board is supplied with 4K segmentation for M2708 or 8K for M2316E, but either can be changed if the user wants to insert another type of memory. The address of the segment is fixed by the MEMORY SELECT (see below).

(3.5.) RAM

The CLZ80/NC board provides 4Kx8 dynamic RAM (upgradeable to 16K) with refresh by the Z80CPU. The RAM chips M4027 Q20-27 require multiplexed addressing which is provided by MA0-5 (& MA6 for 16K chips) from RAM CONTROL. These lines provide two addresses to the RAMs for each memory read or write operation, one for ROW and one for COLUMN of the RAM memory. Latching of the row and column addresses is by the inputs $\overline{RAS}$ and $\overline{CAS}$. These signals are generated by RAM TIMING.

The RAM data inputs are connected to the internal data bus D0-7. The outputs MO0-7 are buffered onto the internal data bus by the 3-state gates T74LS367 Q19 and Q28. These 3-state gates are enabled by the $\overline{LETRA}$ signal (lettura RAM = read RAM) from RAM TIMING. Writing to the RAM is made by the $\overline{WRM}$ signal.

(3.6.) RAM TIMING

In a Z80 system a memory access is signalled by a $\overline{MREQ}$ output and an $\overline{RD}$ or $\overline{WR}$ signal. When using dynamic RAMs the Z80 CPU also provides refresh address on A0-A6 and a control signal $\overline{RFSH}$ which must be used to enable only the ROW addresses of the RAM (via $\overline{RAS}$).

The lower part of the timing circuit formed by Q33 generates the $\overline{RAS}$ signal following the input PAGRA (Page of RAM) from MEMORY SELECT. After a delay due to the propagation time of T74LS04 Q36 and two T74LS04 Q36 the $\overline{SELAD}$ signal is produced which goes to RAM CONTROL to switch the address from ROW to COLUMN on MA0-6 (7). After a further delay, for the multiplexer Q37, Q47 to switch and the RAM address set-up time, the $\overline{ICAS}$ signal is generated.

The $\overline{ICAS}$ signal is passed through the multiplexer T74LS157 Q37 which gives a further delay before outputting the $\overline{CAS}$ signal on output ZD to the RAMS.

If only a memory refresh is required then the T74LS02 Q33 NOR gate with inputs $\overline{BMREQ}$ and $\overline{BRFSH}$ generates an input to the next gate pin 2 which generates $\overline{RAS}$. The $\overline{SELAD}$ and $\overline{ICAS}$ signals are however inhibited by the application of $\overline{BRFSH}$ to the gate T74LS00 Q35.

To read the RAM output data onto the data bus a $\overline{LETRA}$ signal is generated by T74LS00 Q35 pin 8. This signal is generated by $\overline{BRD}$ and PAGRA but is inhibited by the presence of PROMSEL. The reason for this is that PROMSEL is generated when the RESET PROM Q48 is outputting data and this must not clash with RAM outputs. The RAM and the Reset PROM can have the same address space (0000-0002) so the Reset signal, which clears the T74LS74 Q4, generates PROMSEL (active high) and switches the active data stream from the RAM to the Reset PROM.

Finally the RAM timing for write signal $\overline{WRM}$. The generation of $\overline{WRM}$ is delayed in case an off-board CPU or DMA wants to write to the internal RAM. In this case the data will not be present until the decoder T74LS156 Q12 has enabled $\overline{DBIN}$ to bring the BD0 - 7 data into D0-7. To overcome this decoding delay and ensure the RAM data is set up, the $\overline{BWR}$ signal is delayed by the capacitor of 100pF C8 on the output of T74LS04 Q36 pin 10. This delay has no effect on internal CPU write cycles as there is always an adequate timing margin with the Z80 CPU operating at 2.5MHz.

(3.7.) RAM CONTROL

The two multiplexers T74LS157 Q37 and Q47 switch the buffered address lines for row and column addressing of the RAM memory. The jumpers 39 to 44 select the correct address lines for 4K or 16K RAMs according to the table .

(3.8.) MEMORY SELECT

In the Nanocomputer the EPROM or ROM is located in the upper address area between 60K and 64K and the RAM is located in the lower address area between 0 and 4K.

The NC-Z monitor is designed for ROM and RAM located at these positions, however for completeness the tables show the position for the links 11-26 for alternative memory mapping.

(3.9.) DEVICE SELECT

The Z80 CPU addresses up to 256 I/O parts (by a decode of BAD0 to 7) and by activating the $\overline{IORQ}$ and either $\overline{RD}$ or $\overline{WR}$ signals. This means that the I/O ports can have the same addresses as memory locations (for which $\overline{MREQ}$ is active).

On the CLZ80/NC board partial decoding is provided for the I/O ports.
The signals $\overline{IOQ0}$-3 and $\overline{IOE0}$-3 from T74LS138 (Q53) are decodes of the address lines BAD2 to BAD7 giving active signals for page 0 addresses in the range 0 to 31 as follows :

Addresses	Active (low)	Addressess	Active (low)
0 - 3	$\overline{IOQ0}$	16 - 19	$\overline{IOE0}$
4 - 7	$\overline{IOQ1}$	20 - 23	$\overline{IOE1}$
8 - 11	$\overline{IOQ2}$	24 - 27	$\overline{IOE2}$
12 - 15	$\overline{IOQ3}$	28 - 31	$\overline{IOE3}$

In the CLZ80/NC using NC-Z software it is incorrect to select a page other than page 0 since the keyboard would no longer be addressed by the NC-Z monitor software.

The user however, with his own software, might need to select another page so by means of jumpers according to the table the decoded page can be changed in blocks of 32 addresses. The internal composition of each page remains unchanged.

The signals $\overline{IOU0}$-3 from T74LS139 Q38 are decodes of BAD0, BAD1 enabled by $\overline{BIORQ}$ which are thus active only for I/O operations but not for memory access. These signals are decoded if $\overline{BIORQ}$ is active :

Addresses	Active
0	$\overline{IOU0}$
1	$\overline{IOU1}$
2	$\overline{IOU2}$
3	$\overline{IOU3}$

Obviously each single peripheral address can be decoded by a simple two input gate :

Some addresses however are already assigned to devices as shown in the table below :

	$\overline{IOU0}$	$\overline{IOU1}$	$\overline{IOU2}$	$\overline{IOU3}$	
$\overline{IOQ0}$	00	01	02	FLAG IN	
$\overline{IOQ1}$	Data A	Data B	Cont.A	Cont.B	PIOQ2
$\overline{IOQ2}$	Data C	Data D	Cont.C	Cont.D	PIOQ3
$\overline{IOQ3}$	0C	0D	0E	0F	
$\overline{IOE0}$	10	11	12	13	
$\overline{IOE1}$	14	15	16	17	
$\overline{IOE2}$	18	19	1A	1B	
$\overline{IOE3}$	1C	1D	1E	1F	

(3.10.) FLAG INPUT

An unusual feature of the NBZ80 design is the ability to read the status of the PIO 'Ready' lines.

The PIO Ready lines are :

PIO signal	CLZ80/NC sig.	NEZ80 sig.
PIO(Q2) ARDY	FLPA	-
BRDY	FLPB	-
PIO(Q3) ARDY	FLPC	CRDY
BRDY	FLPD	DRDY

The I/O address 03H (H = Hexadecimal) is decoded by the 'OR' gate T74LS32 Q16 pin 2 (EEUO0326) and with the $\overline{BRD}$ signal generates $\overline{LETF}$ (Lettura Flag= read flags). This signal is applied to the 3-state buffers T74LS367 Q28 and Q19 (EEUO0325) to gate the state of the PIO flags onto the data bus during the read cycle.

Flag	DB bit
FLPA	D0
FLPB	D1
FLPC (CRDY)	D2
FLPD (DRDY)	D3

(3.11.) INPUT/OUTPUT PORTS A-B-C-D

The two Z80 PIOs on the CLZ80/NC board provide 32 lines of I/O.

The PIO address input for selection of gates A or B or C or D are direct from address bus BAD0 - BAD1 and the chip enable CE is a direct connection to IOQ1 and IOQ2.

The Input/Output data for the PIO Q2 are available on connector J6 and for PIO Q3 on J7.

In the Nanocomputer system the PIO Q2/J6 is connected to the keyboard.

The keyboard provides the following links :

signal		connected to	
J6-21	PA5	ICAS1	J6-5
J6-19	PA6	ICAS2	J6-6
J6-17	PA7	RxD	J6-7
J6-23	PA4	TxD	J6-3

(3.12.) INTERRUPT

The PIO Q2 IEI (Interrupt Enable Input) is connected to +5V making this the highest priority in the interrupt daisy chain. IOE1 is the daisy chain output of the first PIO Q2. The two PIO output signals IOE1 and IOE2 are combined to form a single output IEO by T74LS08 Q15. The $\overline{\text{INTAB}}$ output from PIO Q2 and the $\overline{\text{INTCD}}$ from PIO Q3 are combined to activate the $\overline{\text{BINT}}$ line by T7417 Q32.

(3.13.) CASSETTE CONTROL

The motor on/off of the audio cassete recorder is controller by T7416 Q8. The $\overline{\text{ICAS}}$ signals come via the keyboard, plugged into J6, from the PIO Q2A.

PIO (Q2)	Signal	Cassette control
PA5	ICAS1	$\overline{\text{CA1ON}}$
PA6	ICAS2	$\overline{\text{CA2ON}}$

However only $\overline{\text{CA1ON}}$ is used by the Nanocomputer. When $\overline{\text{CA1ON}}$ is low (PA5 high, ICAS1 high) the motor is stopped.

(3.14.) CLOCK AND BAUD GENERATOR

The F4702 Q34 oscillator at 2.4576 MHz is the master clock.

The divided outputs are :

SICK - Serial interface clock (f = 9.6kHz for the 600 baud setting of jumpers 45 and 51), used by Nanocomputer to generate an audio signal of 4.8kHz

FCU - Signal used by DC-DC converters (when fitted) at f = 307kHz.

The Multiplexer T74LS157 Q44, used very little on the NBZ80 board, is used to switch the baud rate between 110 - 9600 baud serial I/O and 600 band Audio I/O when the board is upgraded to a CLZ80 Microcomputer and uses a USART.

(3.15.) SERIAL INTERFACES

There are three types of serial interface at RS232, 20mA current loop and TTL levels. These are supplied by circuits T74LS14 Q11, T74LS04 Q9 and T74LS00 Q10 for input and by T74LS04 Q31 Q9, T74LS32 Q13, T7416 Q8 and BSX36 Q7 for output. The jumpers set the interface standard according to the table.

A second interface is for an audio cassette. The output signal UM1 of 4.8 KHz is generated by the T74LS74 Q17 which divides SICK by 2. This signal is gated by the transmit data signal TXD. The audio level can be adjusted by potentiometer R54. The nominal amplitude of UM1 is 200mV p-p from a impedance of 100 ohm .

The audio input is to the OUTPUT RECORDER RECTIFIER which is a full wave peak detector using two op-amps LS147 Q5. The input impedance is about 20 Kohms and a signal of 300-400mV is required. The received data signal INM leaving amplifiers Q5 goes to the data selector T74LS00 Q10 via the schmidt trigger gate T74LS14 Q11. The signal MAG which switches the system from serial I/O to Audio Cassette comes from the keyboard on J6-1. $\overline{\text{MAG}}$ low = Audio cassette.

(3.16.) INITIALIZATION CONTROL

To make the Z80 CPU execute a jump instruction to the entry point of the NC-Z program when the Reset key is pressed the PROM 6331 Q48 contains the op.codes

C3 02 FC (FC02 = entry point address).

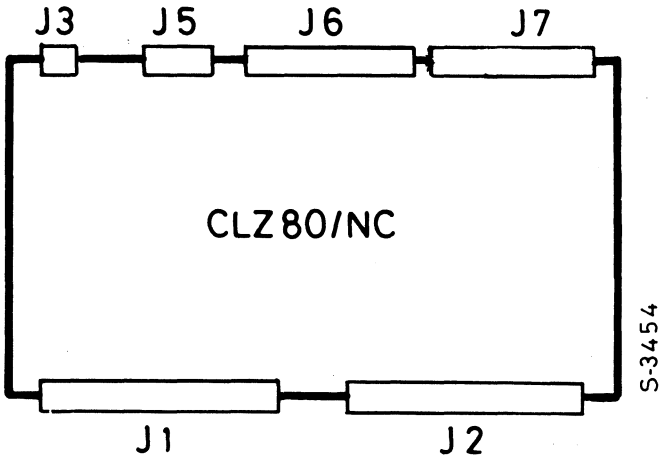
When the $\overline{\text{RESET}}$ signal is active the 2 stage shift register made up of T74LS74 Q4 is reset and the PROM Q48 is enabled ($\overline{\text{PROMSEL}}$ signal low). The contents of Q48 locations 0, 1 and 2 are read by the CPU onto the data bus in three successive op-code fetch M1 cycles thus executing a jump to NC-Z program. After the three op-codes for the jump have been fetched and there have been three M1 pulses the '0' input on pin 2 will have been shifted along to the output pin 9 and $\overline{\text{PROMSEL}}$ is deactivated.

(4) CONNECTORS, CABLES AND BOARD LINKS ON THE CLZ80/NC

(4.1.) CONNECTORS

The CLZ80/NC board has six multiple connectors as shown in diagram EEU00327.

The two connectors on the lower edge of the board, J1 and J2, are standard Euroconnectors with two rows (a and c) of 32 pins each. These connectors are used for the Gamma-bus interface and power supply input.



CLZ80/NC BOARD CONNECTORS

Along the top of the board are 4 connectors as follows :

J3 Audio cassette input/output and control signals

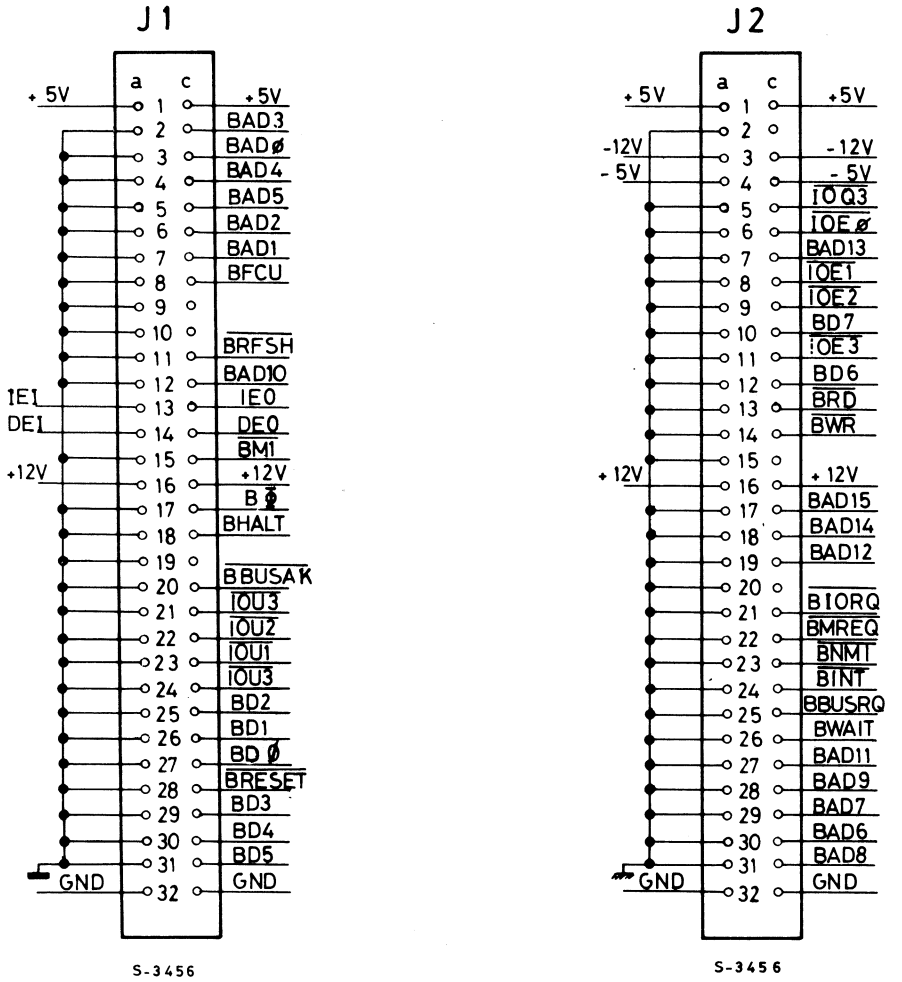
J5 Serial terminal interface

J6 PIO Q2 input/output and system control signals. The keyboard/display is connected to this connector.

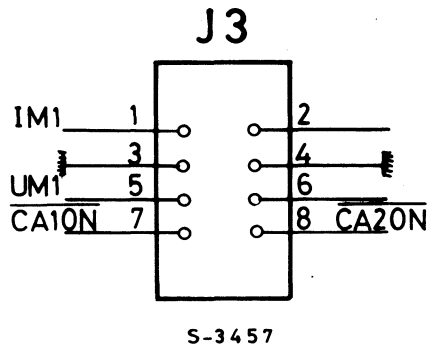
J7 PIO Q3 Input/output and system control signals. The signals from J7 are taken via a flat flexible cable to connector J4 of the experiment board.

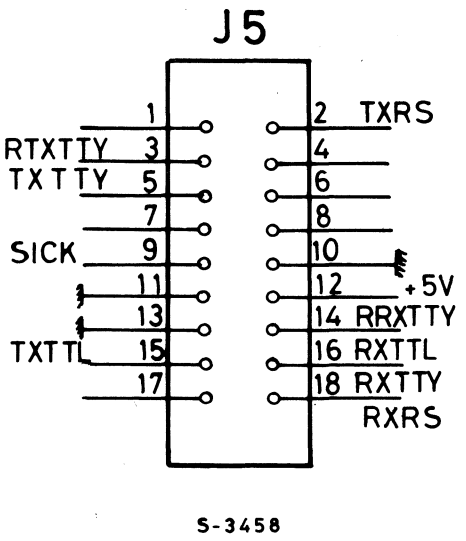
Mating plugs are available in two kits for J1 to J7 as follows :

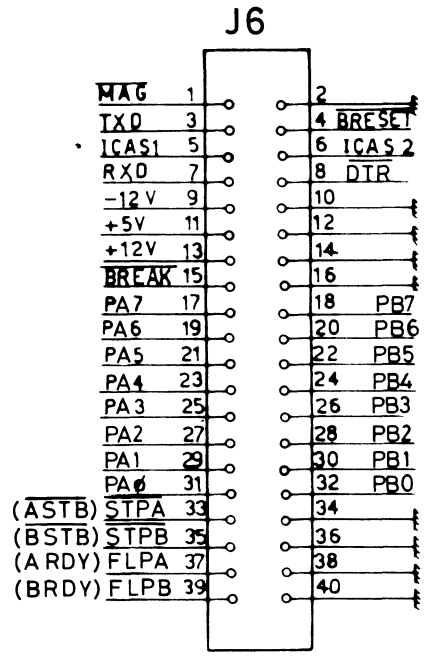
Connector	Kit	Description
J1, J2	C2Z80 C3Z80 C4Z80	Two female connectors - wire wrap - PCB mounting - solder
J3, J5, J6, J7	C1Z80	Set of shells and 120 pins for these connectors

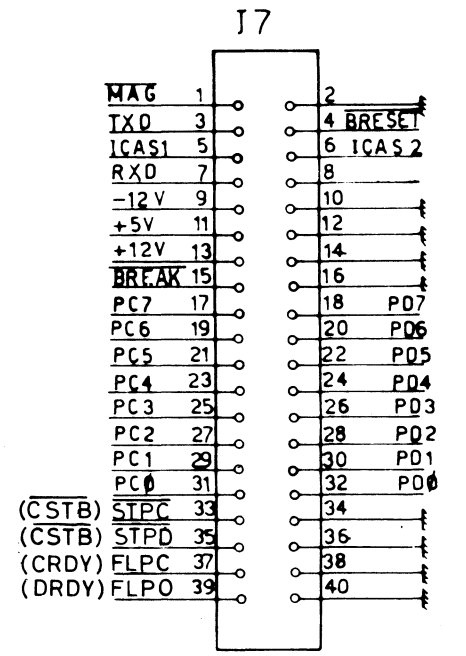


CONNECTIONS OF J1 & J2









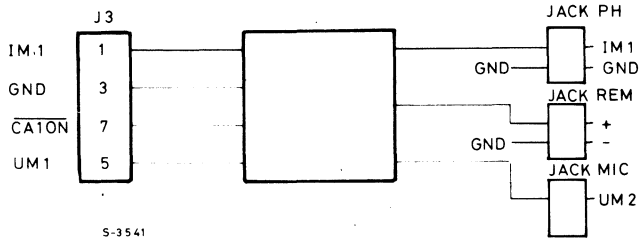
CONNECTIONS OF J3,J5,J6 & J7

(4.2.) CABLES

Some ready made cables are available for connection to the CLZ80/NC board and peripherals.

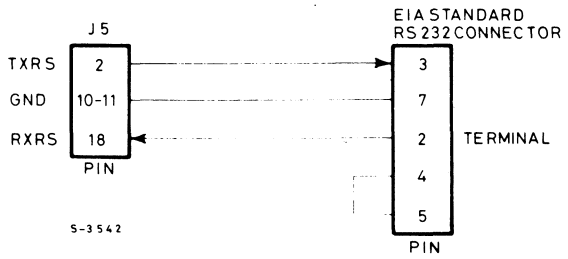
W10Z80 Cable for connecting the RCZ80 cassette recorder to the CLZ80/NC board.

W15Z80 Cable for connection of the PIO Q3 signals (ports C & D) from the CLZ80/NC board J7 to the NEZ80 board J4.



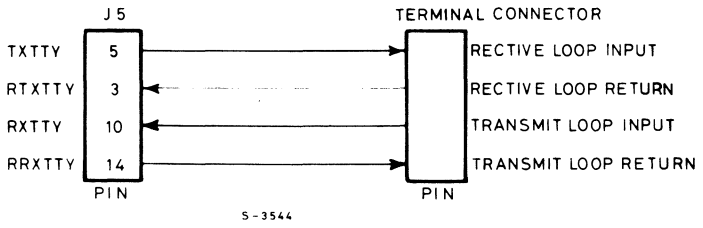
CONNECTION OF A RECORDER TO J3 - W10Z80

RS232 standard EIA interface cable is not available however connections for this use are as follows :



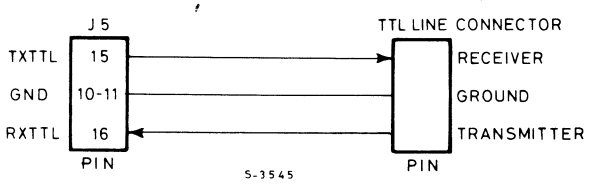
RS232 CABLE CONNECTIONS TO J5

The cable for connecting the CLZ80/NC J5 to a TTY terminal with 20mA current loop must has the following connections :



20mA LOOP CONNECTIONS TO J5

The cable for connecting the CLZ80/NC J5 to a TTL level peripheral has the following connections.



TTL INTERFACE CONNECTION TO J5

(4.3.) BOARD LINKS

The CLZ80/NC board can be adapted for :

(1) RAM type : 4K (M4027) or 16K (M4116) with RAM address in the range 0000-FFFF(Hex)

EPROM/ROM type : 1K (M2708) or 2K (M2716 or M2316E) with address in the range 0000-FFFF(Hex).

(2) Serial communication standards

- RS232

- 20mA current loop

- TTL

(3) Generation of blocks of 32 I/O addresses in the range :

```
  0   -   31
 32   -   63
      .....
224   -  255
```

A board layout showing the link positions is given at the end of this technical manual. The links are joined by a blob of solder across the exposed track areas.

MEMORY TYPE

The RAMs used on the CLZ80/NC board are 4K M4072s but these can be replaced by 16K M4116s and the links changed according to table 4.

The EPROMs/ROMs used on the CLZ80/NC board are eithe two M2708s (1K) or one M2316E (2K) for both NC-Z and NE-Z programs.

The links for these or other ROMs are shown in table 1.

The address sequence for the EPROM/ROM sockets is shown in table 3A.

TABLE 1

EPROM-PROM-ROM SELECT	JUMPERS
2708	1 - 3 - 6
6381	2 - 4 - 7
2716-1(2)	68 - 5 - 8
2716	1 - 5 - 8
2316E	1 - 5 - 8

TABLE 2

4K EPROM PROM-ROM PARTITION START-END		JUMPERS			
		9 26	9 25	9 24	9 23
JUMPERS	30 15	ØK 4K	4K 8K	8K 12K	12K 16K
	30 16	16K 20K	20K 24K	24K 28K	28K 32K
	30 17	32K w 36K	36K 40K	40K 44K	44K 48K
	30 18	48K 52K	52K 56K	56K 60K	60K 64K

TABLE 3

8K EPROM PROM-ROM PARTITION START-END		JUMPERS			
		15 10	16 10	17 10	18 10
JUMPERS	27 30	ØK 8K	16K 24K	32K 40K	48K 56K
	28 29	8K 16K	24K 32K	40K 48K	56K 64K

TABLE 3A

1K EPROM/ROM		2K EPROM/ROM		
1	Q49	1	Q49	low address
2	Q50	2	Q50	
3	Q51	3	Q51	
4	Q52	4	Q52	high address

MEMORY ADDRESSING

The RAM address for the 4K or 16K RAMs

TABLE 4

RAM CONNECTIONS		JUMPERS	SIZE
DEVICE	4027	39 - 40 - 41	4K x 8
	4116	42 - 43 - 44	16K x 8

can be selected using the links shown in tables 5 and 6.

The EPROM/ROM address for 4 x M2708 (4K EPROM) or 4 x M2316 (8K ROM) or other types can be selected using the links shown in tables 2 and 3.

TABLE 5

4K - RAM PARTITION START-END		JUMPERS			
		22	21	20	19
JUMPERS	11	ØK / 4K	4K / 8K	8K / 12K	12K / 16K
	12	16K / 20K	20K / 24K	24K / 28K	28K / 32K
	13	32K / 36K	36K / 40K	40K / 44K	44K / 48K
	14	48K / 52K	52K / 56K	56K / 60K	60K / 64K

TABLE 6

16K - RAM PARTITION	JUMPERS			
	31 11	31 12	31 13	31 14
START-END	ØK / 16K	16K / 32K	32K / 48K	48K / 64K

I/O ADDRESSING

The board can generate partial I/O addresses in 32 address blocks. Each block can be selected by the links shown in table 7.

TABLE 7

INITIAL DEVICE-CODE SELECTOR		JUMPERS			
		36-37	34-38	36-66	35-38
JUMPERS	32	Ø	32	64	96
	33	128	160	192	224

SERIAL I/O

Standards of serial I/O can be selected using the links shown in table 8.

TABLE 8

ASCII SERIAL INTERFACE	TRANSMISSION LINE TYPE		
	TTY	RS232	TTL
JUMPERS	65 54 58	60 54 59	58
SERIAL INPUT	RXTTY	RXRS	RXTTL
RETURN	RRXTTY	GND	GND
SERIAL OUTPUT	TXTTY	TXRS	TXTTL
RETURN	RTXTTY	GND	GND

The transmission rate is software selected by loading memory locations as follows :

Baud rate	0FAE(Hex)	0FAF(Hex)	Notes
600	9A	00	Reset value
300	35	01	
110	55	03	

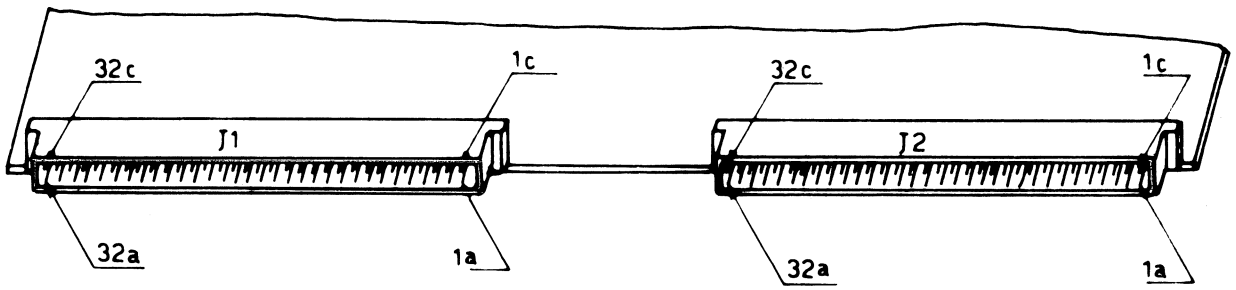
The Audio signal generated by the Baud Rate generator F4702 Q34 is fixed by links 45 and 51 to the input of multiplexer T74LS157 Q44. Links 51 and 45 give a SICK signal of 9.6 kHz and an audio output signal of 4.8 kHz.

(5) SIGNAL SPECIFICATIONS OF CLZ80/NC BOARD

This chapter identifies all the external connections of the CLZ80/NC board, defines all the signals present on the board connectors and gives their electrical characteristics and interconnection rules.

(5.1.) Gamma-bus interface

The Gamma-bus interface signals are available on connectors J1 and J2.



CONNECTIONS OF J1 & J2

This interface bus has been designed to provide optimum noise and speed performance and wide adaptability when expanding the microcmputer system. Many of the pins on connectors J2 and J2 are interconnected to form a grounded shield for the bus signals. When the bus is extended on a mother board, each signal is shielded by two ground lines.
The following tables show the pin connections, the signal name, the identity of input or output and the category (see para 5.1.2.) of the electrical specification.

CONNECTOR J1

	Row 'a'			Row 'c'			
pin	signal	In/out	cat	pin	signal	In/out	cat
1	+ 5V	in	-	1	+5V	in	-
2	GND	-	-	2	BAD3	in/out	1
3	GND	-	-	3	BAD0	in/out	1
4		-	-	4	BAD4	in/out	1
5		-	-	5	BAD5	in/out	1
6		-	-	6	BAD2	in/out	1
7		-	-	7	BAD1	in/out	1
8		-	-	8	BFCU	out	3
9		-	-	9	N/C		
10		-	-	10	N/C		
11		-	-	11	$\overline{\text{BRFSH}}$	out	1
12	GND	-	-	12	BAD10	in/out	1
13	IEI	in	5*	13	IEO	out	5
14	DEI	in	5*	14	$\overline{\text{DE0}}$	out	5*
15	GND	-	-	15	$\overline{\text{BM1}}$	out	1
16	+12	in	-	16	+12V	in	-
17	GND	-	-	17	$\overline{\text{B0}}$	out	3
18		-	-	18	$\overline{\text{BHALT}}$	out	3
19		-	-	19	N/C	-	-
20		-	-	20	$\overline{\text{BBUSAK}}$	out	3
21		-	-	21	$\overline{\text{IOU3}}$	out	5
22		-	-	22	$\overline{\text{IOU2}}$	out	5
23		-	-	23	$\overline{\text{IOU1}}$	out	5
24		-	-	24	$\overline{\text{IOU0}}$	out	5
25		-	-	25	BD2	in/out	2
26		-	-	26	BD1	in/out	2
27		-	-	27	BD0	in/out	2
28		-	-	28	$\overline{\text{BRESET}}$	in	4
29		-	-	29	BD3	in/out	2
30		-	-	30	BD4	in/out	2
31	GND	-	-	31	BD5	in/out	2
32	0V	-	-	32	0V	-	-

CONNECTOR J2

Row 'a'				Row 'c'			
pin	signal	in/out	cat	pin	signal	in/out	cat
1	+ 5V	in	-	1	+ 5V	in	-
2	GND	-	-	2	N/C	-	-
3	- 12V	in	-	3	- 12V	in	-
4	- 5V	in	-	4	- 5V	in	-
5	GND	-	-	5	$\overline{\text{IOQ3}}$	out	5
6		-	-	6	$\overline{\text{IOE0}}$	out	5
7		-	-	7	BAD13	in/out	1
8		-	-	8	$\overline{\text{IOE1}}$	out	5
9		-	-	9	$\overline{\text{IOE2}}$	out	5
10		-	-	10	BD7	in/out	2
11		-	-	11	$\overline{\text{IOE3}}$	out	5
12		-	-	12	BD6	in/out	2
13		-	-	13	$\overline{\text{BRD}}$	in/out	1
14		-	-	14	$\overline{\text{BWR}}$	in/out	1
15	GND	-	-	15	N/C		
16	+ 12V	in	-	16	+ 12V	in	-
17	GND	-	-	17	BAD15	in/out	1
18		-	-	18	BAD14	in/out	1
19		-	-	19	BAD12	in/out	1
20		-	-	20	N/C		
21		-	-	21	$\overline{\text{BIORQ}}$	out	1
22		-	-	22	$\overline{\text{BMREQ}}$	out	1
23		-	-	23	$\overline{\text{BNMI}}$	in	1
24		-	-	24	$\overline{\text{BINT}}$	in	4
25		-	-	25	$\overline{\text{BBUSRQ}}$	in	4
26		-	-	26	$\overline{\text{BWAIT}}$	in	
4							
27		-	-	27	BAD11	in/out	1
28		-	-	28	BAD9	in/out	1
29		-	-	29	BAD7	in/out	1
30		-	-	30	BAD6	in/out	1
31		-	-	31	BAD8	in/out	1
32	0V	in	-	32	0V	in	-

Notes :

GND = Signal shield ground

0V = power supply ground or common

(*) Signals IEI, DEI and DEO are permanently connected to +5V on the NBZ80 board.

N.C. = No connection

(5.1.1.) Signal descriptions for Gamma-bus interface

All signals with a (bar) are active low, all others are active high. For further information on the signals in a Z80 CPU based microcomputer system see the Z80CPU Technical Manual.

BAD0 - 15 Address bus, input or output. 16 lines driven by 3-state buffers which are only disabled by the $\overline{\text{BUSAK}}$, bus acknowledge, signal generated by the local CPU.
The external address inputs can only be applied following a $\overline{\text{BUSRQ}}$, bus request and $\overline{\text{BUSAK}}$ signal response.
Lines BAD0-7 can be used for peripheral addressing (up to 256 max) as an alternative to the partial decodes IOE, IOQ and IOU. The lines BAD0-6 carry the refresh memory address when $\overline{\text{BRFSH}}$ is active.

BD0-7 Data bus, input or output.8 lines with 3-state drivers and receivers enabled by $\overline{\text{DBOUT}}$ and $\overline{\text{DBIN}}$ signals. These lines carry all the system data transfers.

$\overline{\text{BM1}}$ Machine cycle 1 output. A 3-state buffered output which is only disabled by $\overline{\text{BUSAK}}$ active and indicating the Z80CPU op. code fetch cycle.

$\overline{\text{BMREQ}}$ Memory request output. A 3-state buffered output which is only disabled by $\overline{\text{BUSAK}}$ active and indicates a memory access for read or write. When $\overline{\text{BMREQ}}$ is active BAD0-15 hold a valid address for memory.

$\overline{\text{BIORQ}}$ Input/Output request output. A 3-state buffered which is only disabled by $\overline{\text{BUSAK}}$ active and indicates a peripheral access for read or write. When $\overline{\text{BIORQ}}$ is active BAD0-7 hold a valid address for the perihperal and IOE, IOQ, IOU hold a valid partially decoded address for an I/O part.

$\overline{\text{BRD}}$ Read output. A 3-state buffered output which is only disabled by $\overline{\text{BUSAK}}$ active and indicates that the memory or I/O part should place data on the data-bus for the local CPU to read.

$\overline{\text{BWR}}$ Write output. A 3-state buffered output which is only disabled by $\overline{\text{BUSAK}}$ active and indicates that the data bus will supply the data to

be written into the memory or into the peripheral by the local CPU. Note that there is a small timing shift on this signal. $\overline{BWR}$ becomes valid about 60ns before the data on the data bus becomes valid.

$\overline{RFSH}$ Refresh output. A 3-state buffered output which is only disabled by $\overline{BUSAK}$ active and indicates that the address lines BAD0-6 (BAD7=H) hold a valid refresh address for dynamic RAMs. During the refresh cycle the $\overline{BMREQ}$ signal is also active.

$\overline{BHALT}$ Halt output. A buffered output that is active when the CPU executes a software HALT instruction

$\overline{BWAIT}$ Wait input. An input signal direct to the CPU $\overline{WAIT}$ input with a 910 ohm pull-up resistor to +5V.

$\overline{BINT}$ Interrupt input. An input direct to the CPU $\overline{INT}$ input with a 910 ohm pull-up resistor to +5V.

$\overline{BNMI}$ Non-maskable interrupt input. An input direct to the CPU $\overline{NMI}$ input with a 910 ohm pull-up resistor to +5V.

$\overline{BRESET}$ Reset input. Reset of the CLZ80/NC board which resets the CPU and activates the initialization control circuit for a restart jump to the NC-Z program entry point.

$\overline{BBUSRQ}$ Bus request input. An input direct to the CPU $\overline{BUSRQ}$ input with a 910 ohm pull-up resistor to +5V.

$\overline{BBUSAK}$ Bus acknowledge output. A buffered output from the CPU $\overline{BUSAK}$ output. The $\overline{BUSAK}$ signal disables the BAD0-15, $\overline{BMREQ}$, $\overline{BIORQ}$, $\overline{BRD}$, $\overline{BWR}$, $\overline{BM1}$ and $\overline{BFRSH}$ 3-state output buffers so that an external circuit can access the on-board memories or I/O.

B0 Clock. A buffered output of the 2,4576 MHz clock.

BFCU Clock/8. A buffered output of the DC-DC convertor driver clock (307KHz).

$\overline{IOQ0-3}$
$\overline{IOE0-3}$ Partial peripheral address decode outputs. These decode the BAD0-7 lines to provide blocks of 32 I/O addresses when used with $\overline{IOU0-3}$.

$\overline{IOU0-3}$ Partial peripheral address decode outputs timed by $\overline{BIORQ}$ and used with $\overline{IOQ0-3}$ or $\overline{IOE0-3}$ to generate peripheral addresses.

IEI Interrupt enable input to PIO Q2 IEI pin, connected internally to +5V thus making PIOQ2 part A the highest priority in any interrupt daisy chain.

IEO Interrupt enable output from PIO Q2/Q3, used to extend the interrupt daisy chain.

DEI,DEO Bus enable daisy chain. These signals are used only in larger systems to form a daisy chain defining the priority for bus requests. They are internally connected to +5V on the CLZ80/NC board.

(5.1.2.) Electrical specification

The table of signals on J1 and J2 making up the Gamma-bus show categories for each signal corresponding to the electrical specification.

For all Gamma-bus signals the drive and load currents (mA) for the categories are as follows :

Cat	Description	Output GIiol	Output GIoh	Input GIil	Input Gih	3-state GIzol,zoh
1	Address bus T74LS367 drivers	23 (1)	-2,6	-0,8 (2)	0,2	+/-0,02
2	Data bus T74LS367 buffers	23 (3)	-2,6	-0,42 (4)	0,06	-
3	Buffered outputs T74LS367	23	-2,6	-	-	-
4	Resistor pull-up 910 ohm to +5V	-	-	-4,6	-	-
5	Decoder outputs T74LS138, 139	7,5	-0,4	0,36	-	-

Notes :

GIol = Current absorbed by output which is low
GIoh = Current supplied by output which is high
GIzol,zoh = Current supplied or absorbed by disabled output in the third state
GIil = Current supplied by an input at a low state voltage
GIih = Current absorbed by an input at a high state voltage

The current values are maximums and :

(1) BUSAK not active
(2) BUSAK active
(3) Input data
(4) Input data

- means current out of pin, + means current into pin

The voltage levels for all the Gamma-bus signals are :

Output	high level > 2.4V
	low level < 0.5V
Input	high level > 2.0V
	low level < 0.8V

Description of the categories :

cat1 The address Bus and some control signals.
Output active (when $\overline{\text{BUSAK}}$ non-active): these lines are outputs from T74LS367 buffers but are loaded by some on-board circuits which reduce the full T74LS367 drive capbility to the value shown.
Input active (when $\overline{\text{BUSAK}}$ active) : these lines drive the on-board ROM & RAM address lines and decoders and the Peripheral Device select decoders. BAD0-1 also drive the PIO chips Q1 and Q2. The load presented is as shown in the table.

cat2 The data bus.
This is 3-state but the load presented in the input state and the inactive state is the same since it is the input current and output leakage of one T74LS367.
The drive in the output state is almost the full T74LS367 output capability as shown in the table.

cat3 Outputs from T74LS367 buffers, giving the full T74LS367 drive capability These outputs are always active.

cat4 Input for wired-or use with on board 910ohm pull-up resistors to +5V.

cat5 Outputs which are not buffered but come direct from the T74LS138 or 9 decoders and have a smaller drive capability.

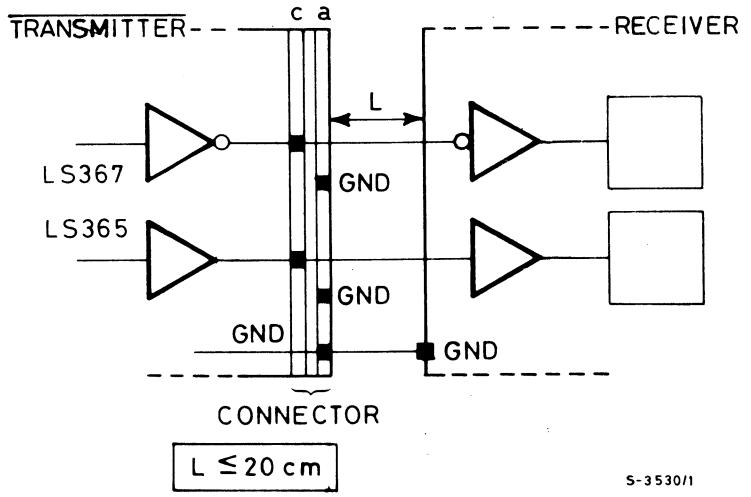
All of the normal rules for input and output loading and driving must be respected when using the Gamma-bus signals.

(5.1.3) Rules for Gamma-BUS signal expansion.

There is a maximum recommended length for connections to the Gamma-BUS signals in order to avoid problems of reflections or noise.

The methods recommended are as follows:

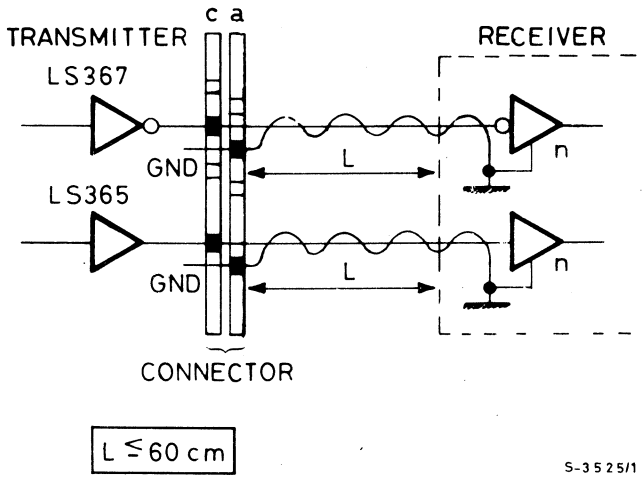
(1) Connections by single wires with a common ground return.



CONNECTION TO THE GAMMA-BUS WITH SINGLE WIRES

For connections made on the Experiment Board NEZ80 the signal B0 (clock) should always be made with a twisted pair as shown below.

(2) Connections with twisted pairs.



CONNECTION TO THE GAMMA-BUS WITH TWISTED PAIRS

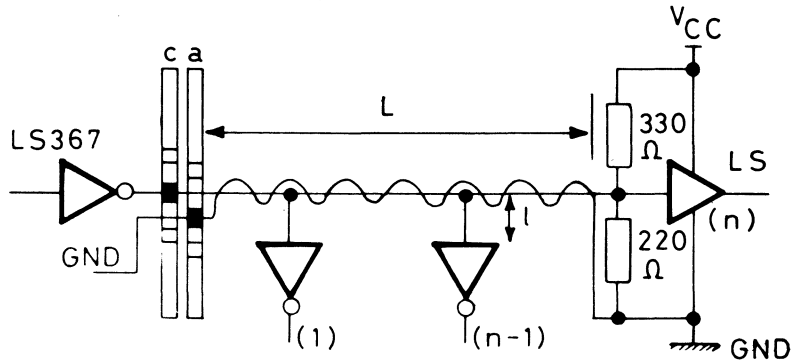
The ground connection should be made at both ends for each pair.

(3) Connections with terminated lines.

CONNECTION TO THE GAMMA-BUS WITH TERMINATED LINES

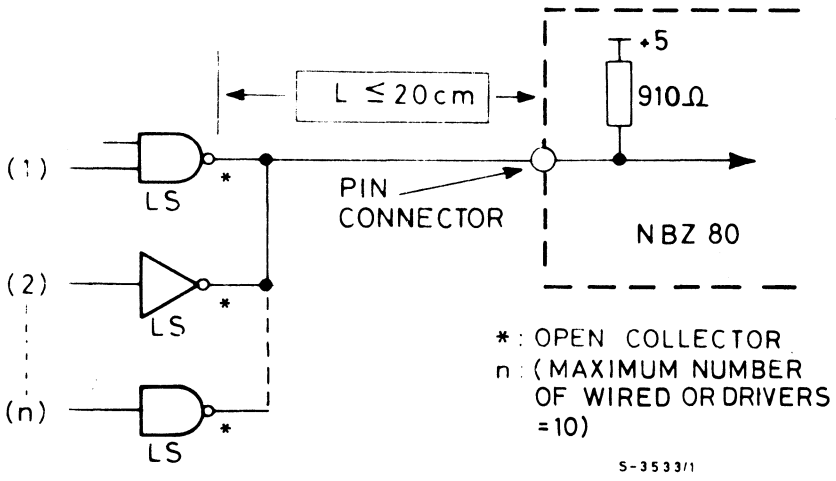
The line must be terminated at the far end. Additional outputs can be taken from the line at intermediate points.

(4) Connection of Wired-OR circuits



CONNECTION OF WIRED-OR CIRCUITS

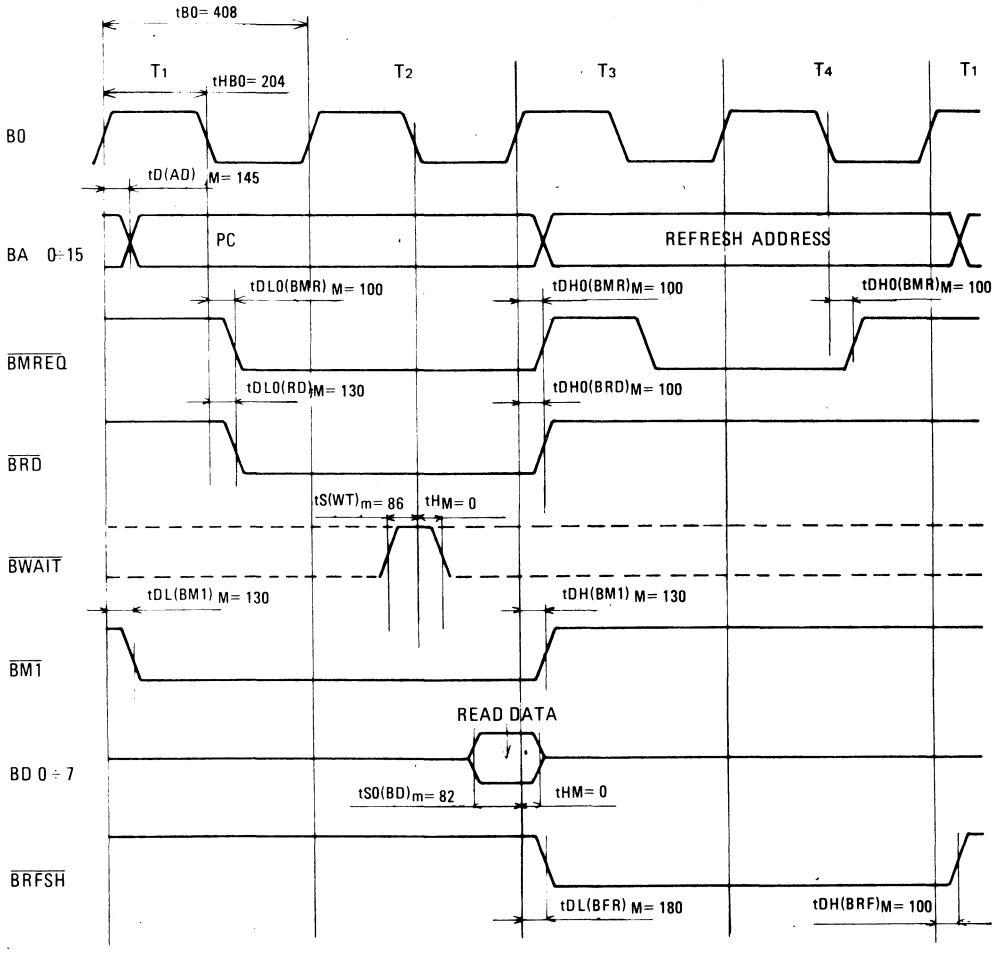
The maximum length of the connections is the same as (2) above.



(5.1.4.) Timing of Gamma-bus signals

The timing of the signals on the Gamma-bus is not the same as for the Z80CPU chip because of delays introduced by the buffers and some of the decoder circuits.

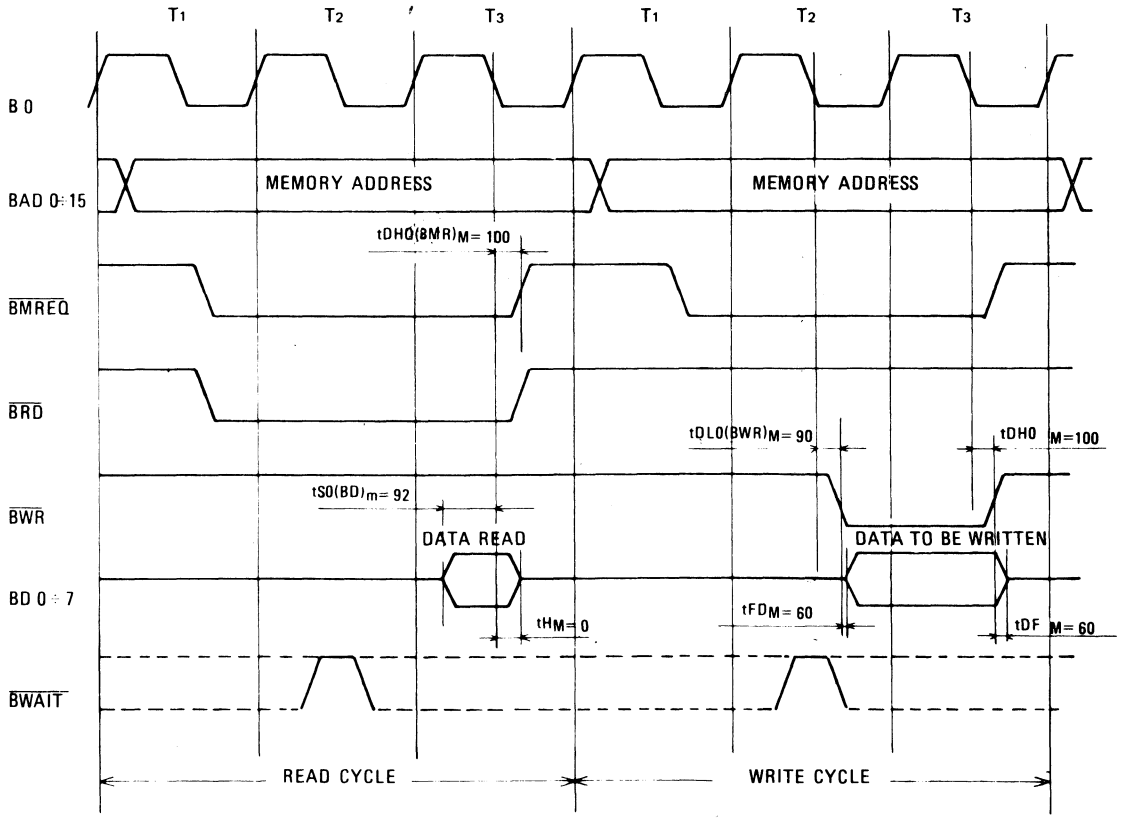
Op.code fetch or M1 cycle.



OP CODE FETCH OR M1 CYCLE

The program counter contents are put on the address bus BAD0-15 at the beginning of T1 cycle. Half a cycle later the $\overline{\text{BMREQ}}$ signal goes active indicating this is a memory request. $\overline{\text{BRD}}$ goes active at almost the same time to tell the memory to place its data on the data bus BD0-7.
The CPU reads the data at the end of T2/beginning-of-T3 and immediately disables $\overline{\text{BMREQ}}$ and $\overline{\text{BRD}}$.
During T1/T2 $\overline{\text{BM1}}$ is active indicating this is an op code fetch cycle.
During T3/T4 the CPU provides a refresh address for dynamic memories and activates $\overline{\text{BMREQ}}$ again and $\overline{\text{BRFSH}}$.

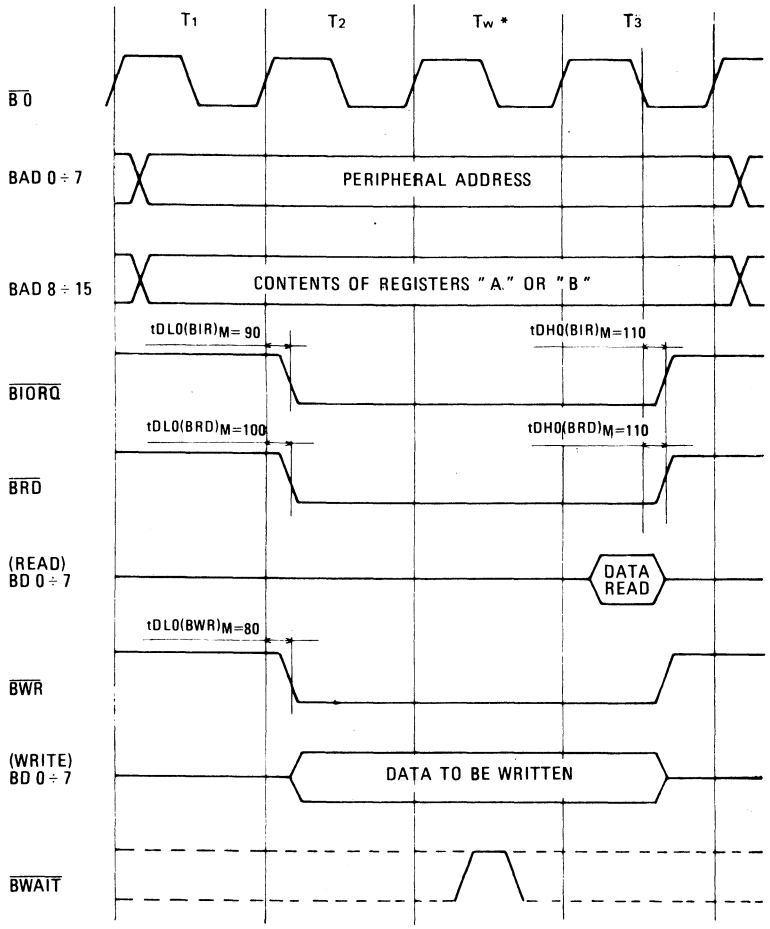
Memory read and write cycles.



MEMORY READ/WRITE CYCLES

The memory address is put on the address bus BAD0-15 at the beginning of a read or write cycle.
For a read cycle $\overline{\text{BMREQ}}$ and $\overline{\text{BRD}}$ are activated in the middle of cycle T1 and the data is read by the CPU in the middle of T3.
For a write cycle the $\overline{\text{BMREQ}}$ signal is active from the middle of T1 but the $\overline{\text{BWR}}$ does not go active until the middle of the T2 cycle. The delays in the T74LS156 Q12 decoder which activates $\overline{\text{DBOUT}}$ mean that the data to be written is not valid until after $\overline{\text{BWR}}$ is active. For this reason any memories connected to the Gamma-bus must apply a delay of 100-200 nS on $\overline{\text{BWR}}$ before using the signal for a RAM write command.

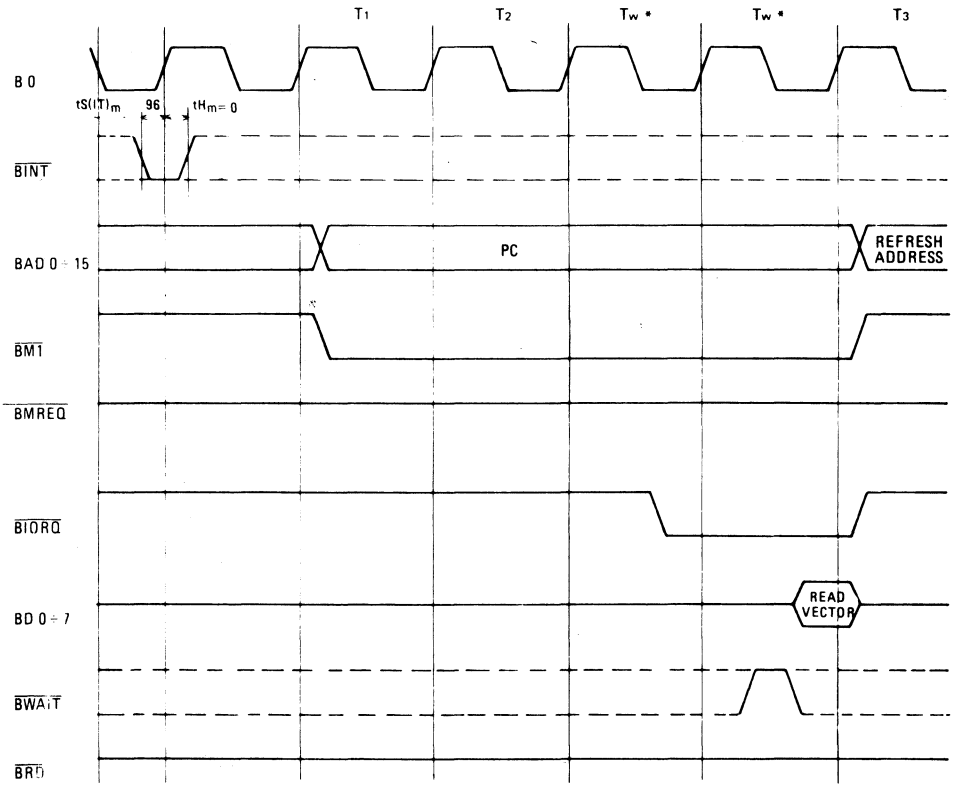
Peripheral read and write cycles.



PERIPHERAL READ/WRITE CYCLES

The peripheral address is placed on the address bus BAD0-7 at the beginning of Tl cycle. For a read or write cycle at the beginning of T2 the $\overline{\text{BIORQ}}$, $\overline{\text{BRD}}$ or $\overline{\text{BWR}}$ are active. The CPU outputs data to be written at the same time, but reads input data in the middle of T3.
The main difference to the memory cycles is the automatic insertion of a wait state not caused by a $\overline{\text{BWAIT}}$ signal. This special wait state is called Tw*.

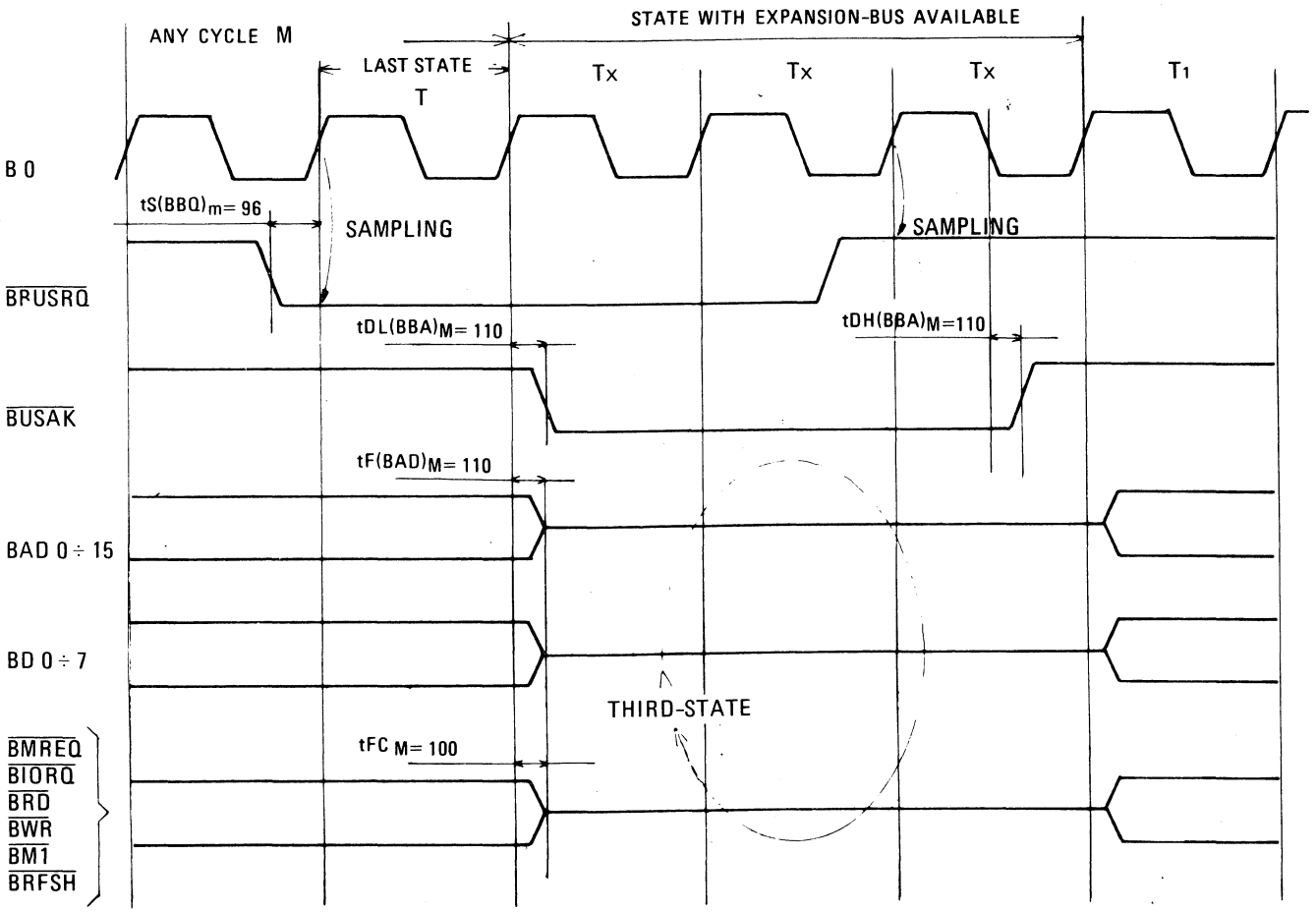
Interrupt and acknowledge cycles.



INTERRUPT/ACKNOWLEDGE CYCLE

The BINT line is sampled by the CPU during the positive edge of the last clock cycle of the execution of each instruction. An interrupt accepted by the CPU generates a special M1 cycle in which BIORQ is active instead of BMREQ. The PIO chip generating the interrupt reponds to this by outputting the interrupt vector on the data bus lines BD0-7, which is subsequently read by the CPU at the beginning of T3. Two wait cycles TW* are inserted automatically to allow for daisy chain ripple priority timing.

Bus request and acknowledge



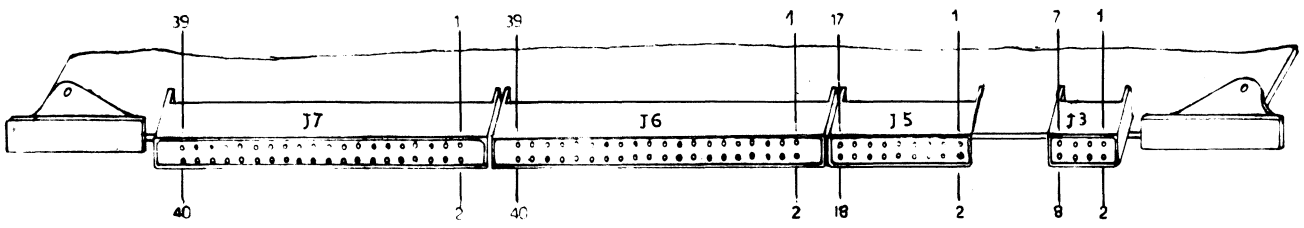
BUS REQUEST/ACKNOWLEDGE CYCLE

A request for the buses is made at any time by activating $\overline{\text{BBUSRQ}}$. The $\overline{\text{BUSRQ}}$ input on the CPU is sampled at the end of each M cycle just before the last T state. The bus drivers will be forced into the high impedance state at the end of the current M cycle and will remain in this state as long as $\overline{\text{BBUSRQ}}$ is active.

The dynamic RAM's are NOT refreshed by the local CPU during a Bus request/acknowledge cycle and this function must be taken over by the unit making the request.

(5.2.) PIO Interface

The PIO interface signals are available on connectors J6 and J7.



The following tables give the pin connections, the signal name, the identity of Input or Output and the category of the electrical specification.

CONNECTORS J6 & J7

pin	signal	in/out	cat	pin	signal	in/out	cat
1	$\overline{\text{MAG}}$	in	1	2	GND	-	-
3	TXD	in	1	4	$\overline{\text{BRESET}}$	-	4
5	ICAS1	in	2	6	ICAS2	in	2
7	RXD	out	3	8		O/C	
9	-12V	out	-	10	GND	-	-
11	+5V	out	-	12	GND	-	-
13	+12V	out	-	14	GND	-	-
15	$\overline{\text{BREAK}}$	in	4	16	GND	-	-
17	PA7	in/out	5	18	PB7	in/out	5
19	PA6	in/out	5	20	PB6	in/out	5
21	PA5	in/out	5	22	PB5	in/out	5
23	PA4	in/out	5	24	PB4	in/out	5
25	PA3	in/out	5	26	PB3	in/out	5
27	PA2	in/out	5	28	PB2	in/out	5
29	PA1	in/out	5	30	PB1	in/out	5
31	PA0	in/out	5	32	PB0	in/out	5
33	$\overline{\text{STPA}}$ ($\overline{\text{ASTB}}$)	in	5	34	GND	-	-
35	$\overline{\text{STPB}}$ ($\overline{\text{BSTB}}$)	in	5	36	GND	-	-
37	FLPA(ARDY)	out	5A	38	GND	-	-
39	FLPB(BRDY)	out	5A	40	GND	-	-

Notes :

(1) The following signals are connected internally to the keyboard-display :

PA4	->>	TXD
PA5	->>	ICAS1
PA6	->>	ICAS2
PA7	<<-	RXD

(5.2.1.) PIO interface signal decriptions

A signal with a "(bar)" is active low, all others are active high.
For further information on the signals of the Z80PIO see the Z80PIO technical manual.
This is a summary of the PIO connector signals :

PA0-7,PB0-7 Input/output lines
16 lines of the parallel interface coming directly from the PIO Q2 port A (address 04H) and port B (address 05H). Some of the lines of port A are used by the keyboard/display.

PC0-7,PD0-7 Input/output lines
16 lines of parallel interface coming directly form PIO Q3 port C (address 08H) port D (address 09H).
These lines are directly available to the user on connector J7.

$\overline{\text{STPA}}$,B,C,D Strobe pulse (sync.) inputs.
These represent the sync signals coming from the PIO's, one for each port.

FLPA,B,C,D Ready pulse output.
Represents the data ready signals/coming from the PIO's one for each port.

RXD Receive data serial input.
Data coming from serial peripherals (terminal or audio cassette) is read through port A bit 7 (connection PA7 <<- RXD is made via the keyboard).

TXD Transmit data serial output.
The data output from the PIO port A bit 4 (connection PA4 ->> TXD is made via the keyboard) is sent to the peripheral (terminal or audio cassette).

$\overline{\text{MAG}}$ Cassette select input.
This signal comes from the CASS/TTY switch located on the keyboard and transfers the data input (RXD) and output (TXD) from the serial terminal J5 (TTY) to the cassette recorder J3 (CASS). With $\overline{\text{MAG}}$ not active (high) the serial terminal (TTY) is selected.

ICAS1,2 Cassette recorder control signal output.
These are the signals at the output of PIO (PA5, PA6) for start/stop of recorder motors, In the CLZ80/NC only ICAS1 is controlled by resident NC-Z program (connections PA5->>ICAS1 and PA6->>ICAS2 are made in the keyboard).

$\overline{\text{BREAK}}$ Non-maskable interrupt, input.
Input for generating a a non-maskable interrupt. The input pulse width required is 80-400ns. A 33 ohm pull-up resistor to +5V is incorporated on the CLZ80/NC board.

$\overline{\text{BRESET}}$ Reset input.
A 910 ohm pull-up resistor to +5V is incorporated on the CLZ80/NC board.

(5.2.2.) Electrical characteristics of PIO interface

WARNING

Inputs/outputs PA,B,C,D(0-7), FLPA,B,C,D and $\overline{\text{STPA}}$,B,C,D on connectors J6 and J7 are MOS inputs/outputs.

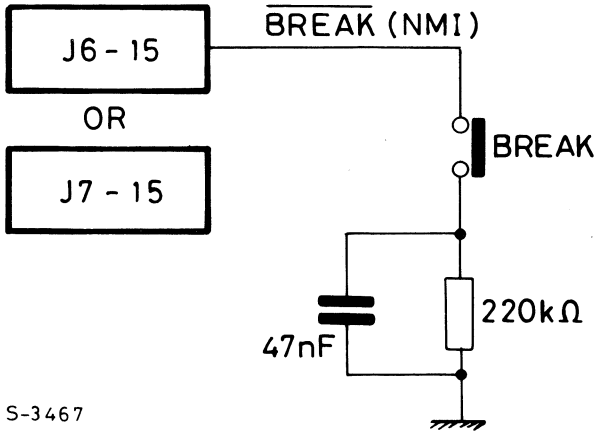
Care should be taken not to allow static electricity to damage the circuits. The Z80PIO chip has built-in protection against static electrical charge build-up but users must take the usual precautions when connecting to the MOS circuits.

The following table gives the load current and threshold voltage levels for each category.

Cat	Description	Threshold Vl	Vh	Loading output Iol	Ioh	Loading Input Iil	Iih
1	LS input	<0,8	>2.0	-	-	-0,36	0,02
2	TTL input	<0,8	>2.0	-	-	-1,6	0,04
3	LS output	<0,5	>2.7	8,0	-0,4	-	-
4	Resistor pull up						
	$\overline{\text{BREAK}}$ (33ohm) (1)	<0,8	>2.0	-	-	-130	-
	$\overline{\text{BRESET}}$ (910ohm)	<0,8	>2.0	-	-	-4,6	-
5	PIO input	<0,8	>2.0	-	-	-0,01	-0,01
	output(2)	<0,4	>2.4	2,0	-0,25	-	-
5A	PIO FLP output	<0,4	>2.4	1,6	-0,23	-	-
		V	V	mA	mA	mA	mA

Notes :

(1) This input should be used as follows :



This circuit produces the required narrow (80-400ns) pulse required for NMI.

(2) Port B of the PIO chips can drive IOH>-1,5mA at Voh=1,5V for direct drive of darlington transistors.

(3) Input $\overline{MAG}$ has a load of Iil=-2.2mA, Iih=0.06mA

Description of categories

Cat1 Inputs to T74LS gates on the board.

Cat2 Inputs to T74 gates on the board.

Cat3 Outputs from T74LS gates on the board.

Cat4 Resistive pull-up. Note the use of the line $\overline{BREAK}$ described above. If a $\overline{BREAK}$ input is required direct from a logic gate output the signal line $\overline{BNMI}$ on the Gamma-bus should be used, driven by an open collector gate output with a 80-400ns pulse.

Cat5 PIO input/output signals - for further information see the Z80PIO data sheet and the Z80 technical manual.

Cat5A PIO outputs FLP have to drive one on-board T74LS367 input so the drive capability is less than other PIO outputs.

(5.2.3.) Interconnection rules

A maximum wire length of 30cm is recommended for reliable input/output connections. For greater interconnection lengths insert a T74LS365 or T74LS367 driver circuit near the PIO connector. If bidirectional I/O lines are used the T74LS245 driver transceiver circuits can be used.

(5.2.4.) Timing

For timing of PIO signals see Z80PIO technical manual.

(5.3.) AUDIO INTERFACE

For recording data or programs onto audio cassettes and reading the material back into the Nanocomputer RAM an audio interface is provided on the CLZ80/NC board.
The audio interface signals are available on connector J3.
The following table gives the pin connections, signal names and input/output identity.

pin	signal	in/out	pin	signal	in/out
1	IM1	in	2	-	
3	GND		4	GND	
5	UM1	out	6	-	
7	$\overline{\text{CA1ON}}$	out	8	$\overline{\text{CA2ON}}$	

(5.3.1.) Signal description

IMI Recorder input.
Input signal coming from recorder.

UMI Recorder output.
Output signal for cassette recorder.

$\overline{\text{CA1ON}}$ Recorder control output, Low = motor off

$\overline{\text{CA2ON}}$ Second start/stop control signal for cassette recorder (not used).

(5.3.2.) Electrical characteristics of cassette interface

signal	description	specification
IM1	Audio input	0.8V p-p into 22Kohm
UM1	Audio output (adj. by R54)	0.2V p-p from 100ohm
$\overline{\text{CAlON}}$	Motor control T7416 OC output	Vol<0,4V, Iol=16mA Vol<0,7V, Iol=40mA

The audio signals can be interfaced to any recorder that can accept the audio input shown and provide the output required.

The serial data is transmitted to the recorder input in the following way :

'1' logic (high) = silence
'0' logic (low) = tone at 4.8 KHz

(5.3.3.) Recording format

The serial data is generated by the NC-Z software in the following format :

(1) Each byte of hexadecimal memory is coded in two ASCII characters.
(2) The data is recorded in blocks of ASCII characters in the following format :

CR LF : NNIIIIXXDDDD ....DDCC

CRLF = Carriage return/line feed
: = Colon
NN = Number of bytes in block (10H)
IIII = Address of first byte of data DD
XX = Two zero characters
DD..DD = Data - 32 characters (16 bytes)
CC = Checksum

(3) Each block of data is recorded as follows :

100NULLS/BLOCK/CRLF/100NULLS

Start of record = "NULLCRLF" . End of record = "CRLFNULL"

There are no sync. characters or control codes in the format.

(4) The characters are in 8 bit ASCII code with one start bit, two stop bits and a zero (0) parity bit.

S-3536

SERIAL SIGNAL

The transmission speed is initialized at 600 baud by the content of memory locations and may be user modified (see 4.3.).

(5.4.) SERIAL INTERFACE SIGNALS

The serial interface provided on J5 can be used for RS232, 20mA current loop, or TTL level communications.
These are selected by links on the board (see table 8 on the schematic EEU00326). The delivered setting is for 20mA current loop standard.

The pin connections on J5 are :

pin	signal	function
1	-	N/C
2	TXRS	RS232 transmit data output
3	RTXTTY	20mA transmit loop return
4	-	N/C
5	TXTTY	20mA transmit loop
6	-	N/C
7	-	N/C
8	-	N/C
9	SICK	9,6KHz audio signal (serial interface clock)
10	GND	-
11	GND	-
12	+5V	-
13	GND	-
14	RRXTTY	20mA receive loop return
15	TXTTL	TTL level transmit data output
16	RXTTL	TTL level receive data input
17	-	N/C
18	RXTTY/RXRS	20mA receive loop and RS232 receive data input

N/C = No connection

(5.4.1.) Signal description

TXTTY-RTXTTY TTY transmission loop output and return.
This pair of signals is for transmission using a 20mA current loop.

RXTTY-RRXTTY TTY reception loop input and return.
This pair of signals is for reception using a 20mA current loop.

TXRS RS232 transmission output.
Data transmission according to RS232C with voltage levels of +/- 12V.

RXRS RS232C reception input.
Data reception according to RS232C with minimum voltage levels of +/- 3V.

TXTTL-RXTTL TTL transmission and reception.
Transmission and reception of data at TTL levels.

SICK Baud rate generator output.
Output frequency of 9.6 KHz. This frequency divided by two is used for audio cassette recording.

(5.4.2.) Electrical characteristics of serial interface

Interface signals for RS232C conform to EIA standards and have the following characteristics :

Input	level '0'	: > 3V
	level '1'	: < -3V
Output	level '0'	: 12V
	level '1'	: -12V

The current loop interface provides an output current of 20mA required to drive a TTY standard interface.

Specifications for the TTL interface are :

	signal level	Iol	Ioh	Iil	Iih	
output LS32	Vol<0.5V Voh>2.7V	6	0.34			mA
input LS14	Vil<0.8V Vih>1.6V			<-0.4	<0.02	mA

The input signal RXTTL is filtered for line reflections by a 0.luF capacitor and by two diodes which limit the excursion of the input signal to -0.5<Vin <5.5V.

The SICK signal is a TTL level signal of 9.6 kHz with the following specification :

	Signal level	Iol	Ioh
SICK out LS04	Vol <0,5V Voh >2,7V	7,2	-0,36 mA

(6) KEYBOARD - DISPLAY NKZ80 - CIRCUIT DESCRIPTION

The circuit diagram (drawing ENKZ 8001) of the keyboard is included at the back of this manual.

The keyboard-display is connected via a flat cable to the CLZ80/NC PIO Q2 inputs/outputs via connector J6.

Port B signals PB1-PB7 are used for multiplexing the display LED and 7-segments driven by BGY16 Q1.

Signals PB1-PB4 are used as input data for the 'FF latch/decoder'HCF4514 Q4 while signals PB0 is used to load data into the FFlatch and suitably delayed to inhibit the outputs of decoder Q4.

In another phase of the multiplex scan the signals PB1-PB7 are used to scan the rows of the keyboard. The closure of a key from I1-I28 is detected by lines PA0-PA3.

The remaining PIO port A bits PA4-PA7 are connected back to the CLZ80/NC board as follows :

PA4 to TXD	transmit serial data output
PA5 to ICAS1	cassette 1 motor control (CA1ON)
PA6 to ICAS2	cassette 2 motor control (not used)
PA7 to RXD	receive serial data input

The switch SW is used to ground the $\overline{\text{MAG}}$ line which changes the serial communication on the CLZ80/NC board from a terminal (connected to J5) to an audio cassette connected to J3.

The BREAK(I29) and RESET(I30) keys, connected to capacitor C3 47nF and to resistor R17 220K are used to produce a break (NMI) or reset pulse on the $\overline{\text{BREAK}}$ and $\overline{\text{RESET}}$ output lines.

(6.1.) Display and keys

The NKZ80 keyboard-display comprises :

- 8 hexadecimal digits for address (4 digits to the left) and for data (4 digits to the right)
- 14 LEDs which indicate :
  (1) which CPU register, memory location or I/O port is displayed
  (2) the condition of breakpoint, alternate register or error
- 16 hexadecimal keys (0-F)
- 4 keys for input and display (->/<-),(2ND),(ARS),(BRK)
- 4 keys for program control (SS),(GO),(BREAK),(RESET)
- 3 keys for input functions (LA),(ST),(INC)
- 2 keys for control of data dump or load from a serial terminal printer, paper tape reader or cassette recorder (LD),(DP)
- 1 switch for selecting cassette recorder or terminal (TTY<->CASS)

(7) NEZ80 EXPERIMENT BOARD - CIRCUIT DESCRIPTION

The circuit diagram for the NEZ80 board (drawing EEU01501) is included at the back of this manual.

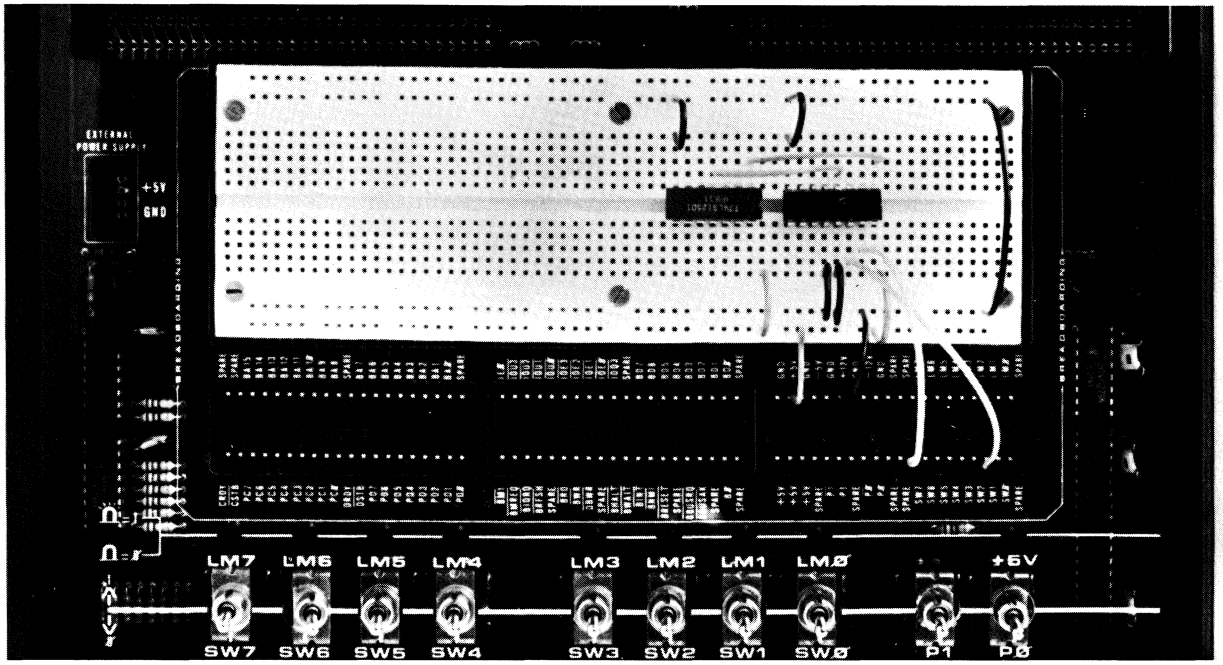
All of the Gamma-bus signals present on connectors J1 and J2 are connected to the 40-pin sockets A & B. The PIO signals of ports C and D are also present on socket A.

Socket C carries the supply outputs, logic level switch outputs SW0-7, pulser outputs P0, $\overline{P0}$ and P1, $\overline{P1}$ and the inputs to the LED indicators LM0-7. The +5V LED shows the presence of the main +5V supply.

Logic switches SW0-7 are debounced by set-reset flip flops T74LS279 Q3,Q4,Q5. Pulses from P0 and P1 are shaped with the same logic, the pulse width is not fixed because it is determined manually. Inverted outputs $\overline{P0}$ and $\overline{P1}$ are also generated by T74LS368 Q2.

The LED monitors LM0-7 are driven by the T74LS368 Q1 and Q2. When the inputs LM0-7 are open the gate inputs are pulled to a logic '0' by 33K resistors R1-8 connected to -12V.

The Gamma-bus BWR signal is delayed by the network formed by R38,R39,C1 and gate T74LS368 Q2 to give DBWR which is delayed by 400nS.



EXPERIMENT BOARD PHOTOGRAPH

(7.1.) Use of experiment board

The board allows insertion of components and connection wires without soldering Each hole is connected internally to the ajacent hole according to the electrical diagram (EEU01501). The hole spacing is designed to match dual-in-line ICs of 8 to 40 pins.

Wiring on the board is made with insulated wire and the wire kit K1Z80 is recommended.

The sockets A,B and C use a double socket arrangement to reduce wear on those mounted directly on the board. A replacement kit of sockets K3Z80 is available.

(7.2.) Description of user signals

The Gamma-bus and PIO signals available to the user on sockets A and B have already been described in sections 5.1 and 5.2. However the following signal name changes must be borne in mind :

Signal name table

CLZ80	NEZ80
BAD0-15	BA0-15
FLPC	CRDY
$\overline{\text{STPC}}$	$\overline{\text{CSTB}}$
FLPD	DRDY
$\overline{\text{STPD}}$	$\overline{\text{DSTB}}$

The signals available on socket C are :

SW0-7 User signals, outputs
The logic level signals handled by the user via switches SW0-SW7 mounted on the NEZ80 board.

LM0-7 Monitor lamps, inputs.
TTL logic level inputs of LED lamp drivers available to the user.
A logic level "1" input means lamp 'on'.

P0,P1 Pulse signals, output.
Output pulses and TTL logic levels generated by the user via buttons P0 and P1 on the NEZ80 board.

Button pressed = positive output pulse, logic level '1'.
Button released = output at logic level '0'

$\overline{P0}$ $\overline{P1}$ Negated pulse signals, outputs.

Power Supply outputs available to the user for supplying the circuits mounted on the experiment board.

(7.3.) Electrical characteristics of user signals

The following table shows the electrical characteristics of the user signals present on sockets A,B and C.

Signal	Output Iol	Output Ioh	Input Iil	Input Iih	
BA0-15 (1)(2) $\overline{BMI}$ $\overline{BIORQ}$ $\overline{BRD}$	23	-2,6	-0,8	0,2	mA
$\overline{BMREQ}$ $\overline{BRFSH}$ $\overline{BWR}$	23	-2,6	-0.8	0.2	mA
BD0-7 (3)(4)	23.5	-2,6	-0,42	0,06	mA
$\overline{BHALT}$ $\overline{BBUSAK}$ B0	23	-2,6			
$\overline{BRESET}$ (5) $\overline{BBUSRQ}$ $\overline{BWAIT}$ $\overline{BINT}$ $\overline{BNMI}$			-4,6		mA
IEO $\overline{IOU0}$-3 $\overline{IOE0}$-3 $\overline{IOQ3}$	7.5	-0,4	-0,36		mA
PD0-7(6) PC0-7	2	-0,25	-0,01	-0,01	mA
CRDY,DRDY	1.6	-0,23			mA
$\overline{CSTB}$ $\overline{DSTB}$			-0,01	0,01	mA
SW0-7	8	-0,4			mA
P0,P1	7.6	-0,35			mA
$\overline{PQ}$ $\overline{P1}$	24	-2,6			mA
LM0-7			-0,4	0,06	mA

Power supply available : +5V /500mA
+12V/100mA
-12V/100mA

Notes :

(1) $\overline{\text{BUSAK}}$ not active
(2) $\overline{\text{BUSAK}}$ active
(3) Output data
(4) Input data
(5) Inputs with 910ohm resistor to be driven with open collector device in cabled-OR connection
(6) Each of the outputs PC0-7 can directly drive a Darlington transistor and have the following characteristics :

Ioh > -1.5mA at Voh = 1.5V

With maximum load the voltage levels for all the signals are :

Outputs	Vol <0.5V Voh >2.4V
Inputs	Vil <0.8V Vih >2.0V

(8) OPERATING SYSTEM NC-Z AND EXPERIMENT PROGRAMS NE-Z

The NBZ80 Nanocomputer includes a powerful operating system covering :

- keyboard and display handling
- memory and register access
- pass pass program execution
- RAM and display self test
- execution of LOAD and DUMP operations

Many of the routines used are available to the user and can be called by user programs.

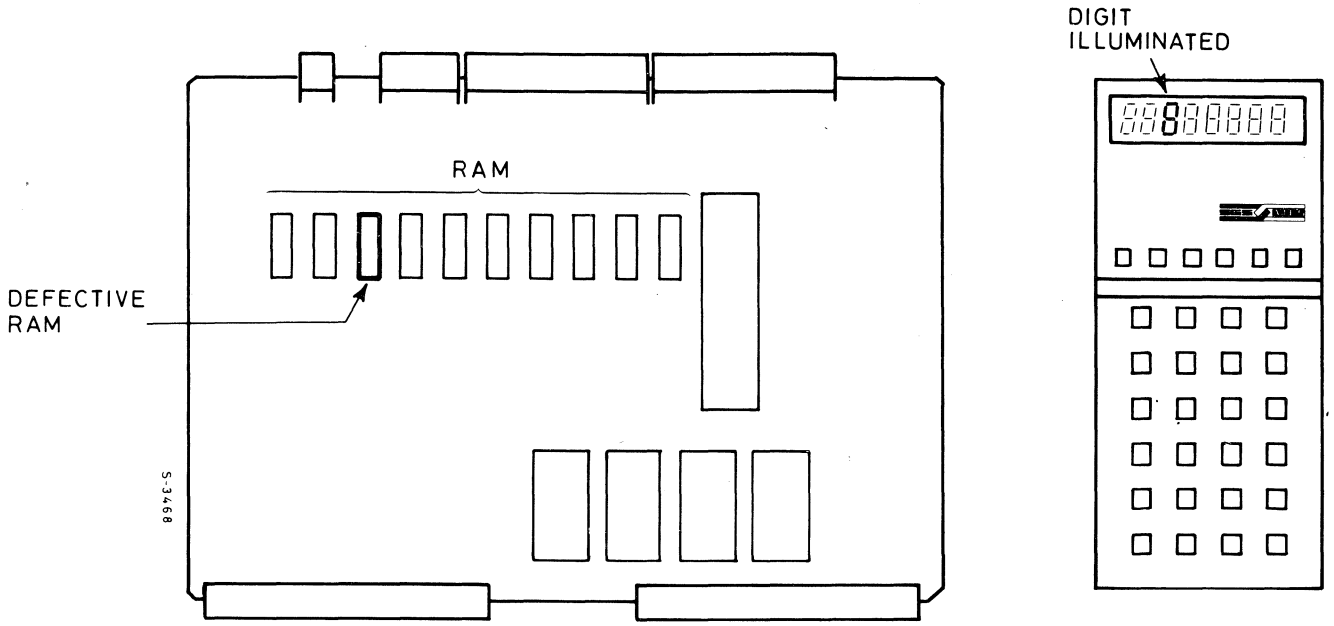
SGS-ATES design note DN314 covering the subroutines that can be used by the user is included at the back of this manual.

Design Note DN340 which describes the experiment routines is also included at the back of this manual.

(8.1.) RAM test program

A test program is included for testing the 4K RAM chips mounted on the CLZ80/NC board.

A partial memory test of the RAM area between 0FAB and 0FFF(Hex), used by the NC-Z operating system, is made automatically every time the RESET key is pressed. If any bit of memory is defective the ERR light and one or more of the display digits will come on. The display shows a figure 8 in the location corresponding to the position on the board of the defective RAM.



If the chip is defective, in addition to the ERR light and the digit being lit, other lights and display segments may also come on.

A test of the RAM area 0000 to 0FAA(Hex) can be made by running a program included in the NC-Z O/S : The entry point of this test routine is FADC(Hex) To execute this test follow the sequence below :

Step	Key	Data	LED	Comments
1	<RESET>		PC	System reset and system RAM test.
2		FADC	PC	Entry point of user RAM test.
3	<GO>			Run user RAM test program.

The display will be off for a few moments while the RAM is tested, if no locations are faulty the display will reappear :

0000 00

If a faulty location is found then the display will show :

LLLL XXYY

LLLL = address location of the faulty memory byte.
XX = data written to the location.
YY = data read from the location.

If there are more locations suspected to be faulty they can be found by pressing any key on the keyboard (except BREAK and RESET of course) to proceed with the RAM test.

(8.2.) Keyboard display and LED test programs

The NC-Z software also contains programs to test the keyboard, display and LEDs Each segment of the 7-segment displays, each LED and all of the keys (except BREAK and RESET) cam be tested by a program whose entry point is FB43(Hex).

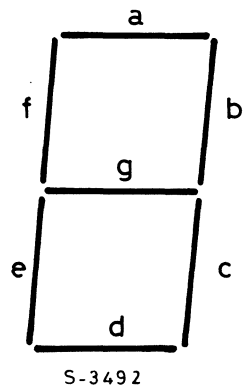
To make the test follow the sequence as follows :

Step	Key	Data	LED	Comments
1	<RESET>		PC	Reset the system.
2		FB43	PC	Enter starting address of program.
3	<GO>			Run the program - see below

This program will illuminate all of the segments and LED's.

The individual 7-segment display bars and two selector LED's can be switched on using the sequence as follows :

any key in row	selector LED lit	segment lit
1	BRK,IR	a
2	IY,ARS	g
3	ERR,IX	f
4	SP,HL	e
5	PC,DE	d
6	BC,MEM	c
7	AF,I/O	b



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SEGMENT NAMES

To end the test press RESET.

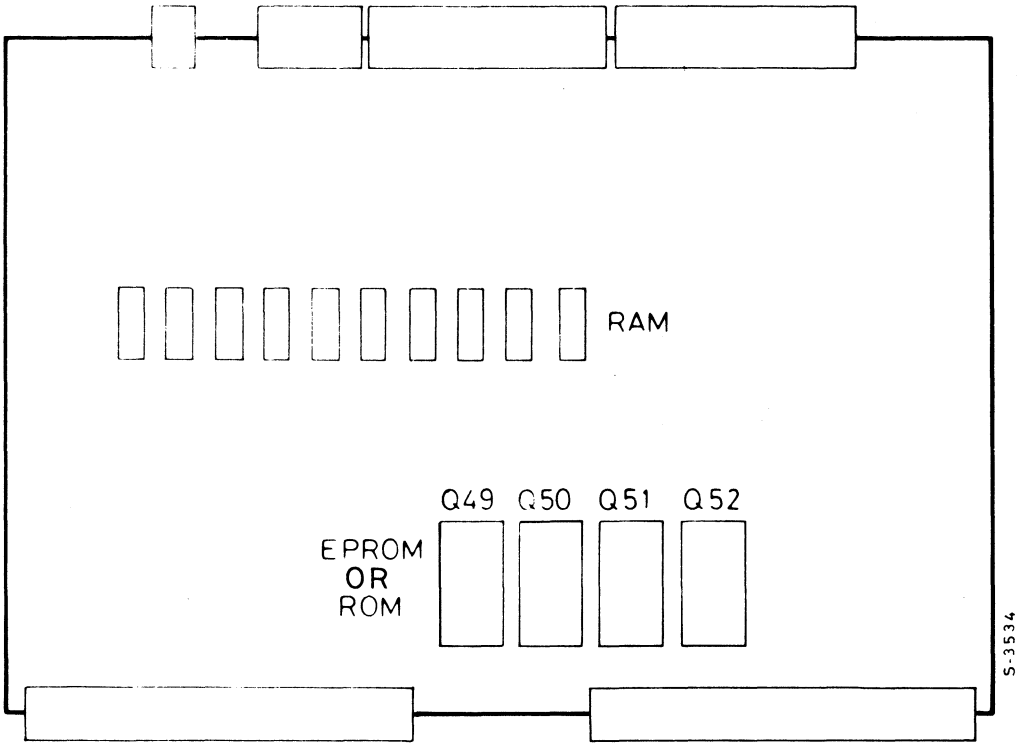
(8.3.) Experiment program NE-Z

SGS-ATES Design Note 340 included in this manual describes the NE-Z program for experiments NE-Z is resident in two EPROM (M2708) or one ROM (M2316E) device with 2K bytes of program.

The NE-Z programs are down located to RAM and used when studying the "Z80 Micrprocessor Book 3 Interfacing". The Design Note Describes their use and gives a complete listing.

(8.4.) System EPROM/ROM layout

The EPROM/ROM layout of the NC-Z operating system and in the NE-Z experiment program is as follows :



LOCATION OF EPROM/ROMS ON THE CLZ80/NC BOARD

	EPROM (M2708)	ROM (M2316E)
NC-Z	Q51,Q52	Q52
NE-Z	Q49,Q50	Q51

9. OPERATING DESCRIPTION

Key functions

<RESET> Key for reseting the Nanocmputer. The software initializes the memory stack pointer and resets the CPU and breakpoints.

<0-F> Keys for data/address inputs in hexadecimal. Data input is displayed on the right hand 4 digits of the display.

<ST> Key to store the input data in the register selected (indicated by the LEDs or in the memory location or I/O port whose address is shown in the left hand 4 digits of the display.
When data is stored in memory the address is auto-incremented.

<LA> Key to load an address of meory or I/O port written. The address can be 4 digits for memory 0000-FFFF(Hex) or 2 digits 00-FF(Hex) for I/O ports.

<2ND> Key to transfer the function of the (ST) key from the lower 8bit CPU register, of a pair, to the upper 8bit register :

2nd	normal
A	F
A´	F´
B	C
B´	C´
D	E
D´	E´
H	L
H´	L´
I	R

<ARS> Key (on/off) for displaying or selecting the alternative register pair AF´,BC´,DE´,HL´,

<<-->> Keys to more the LED indicator lamps right or left. If held depressed the display steps along at about 3/second.

<INC> Key for incrementing the address of memory or I/O port displayed. if this key is held depressed the address auto-movements at about 3/second.

<SS> Key to run a program starting frorm the address indicated by the Program counter in single steps. If held depressed the program

executes slowly at about 3 instructions/second.

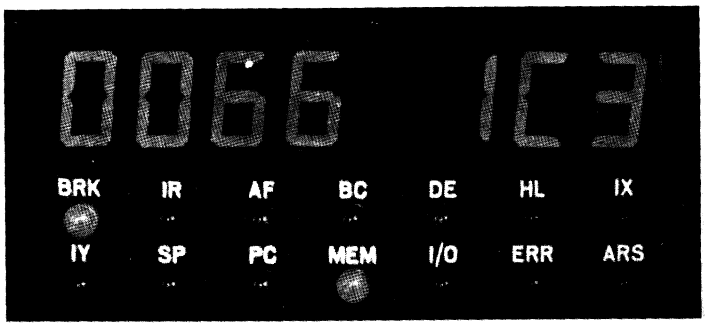
<GO> Key to execute a user program from the start address stored in the Program Counter register. It is sufficient to select PC and enter the start address then press GO.

<BREAK> Key to stop a user program by NMI. Control is transferred back to the operating system NC-Z program. The contents of the CPU registers are saved.

<BRK> Key to program a breakpoint. When this key is pressed the display shows the number of the breakpoint 0-7 and changes the function of 3 other keys as follows :

<LA> to load the address of a breakpoint (max 4digits)
<INC> to increment the breakpoint number
<GO> to cancel a breakpoint

Example of a breakpoint mode display.

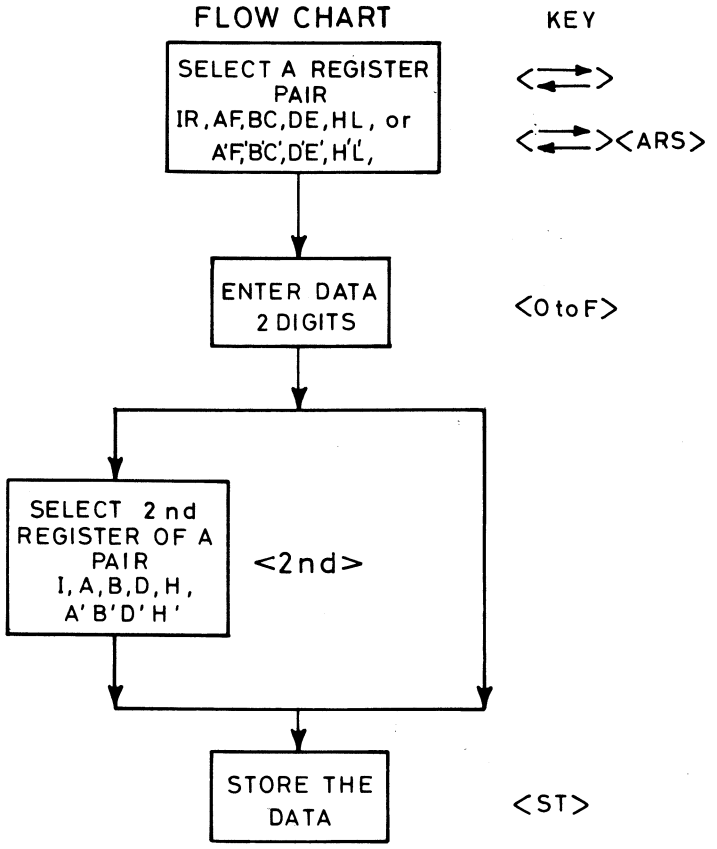


The BRK key is pressed again to exit from the breakpoint mode.

<CASS-TTY> Switch to select the serial input/output of audio cassette (J3) or serial terminal (J5)

(9.1) Examples of register loading

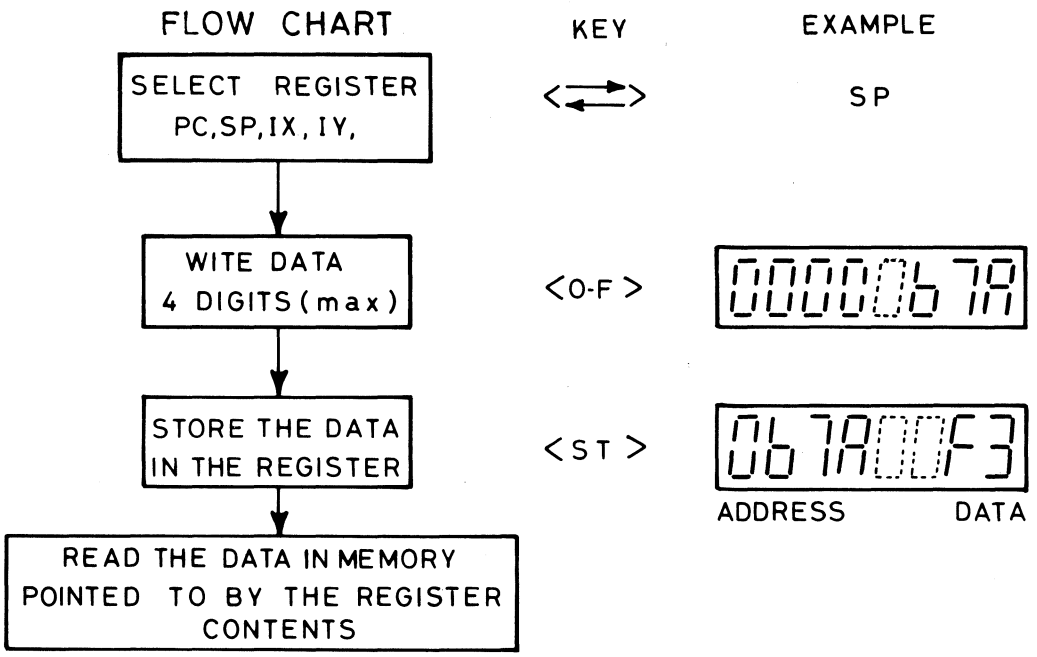
(1) Direct loading of 8-bit CPU registers.



LOADING OF CPU REGISTERS

When writing data in step 2 if there are more than two input digits only the two displayed on the right are stored. If only one digit is written the second (more significant) is stored as zero.

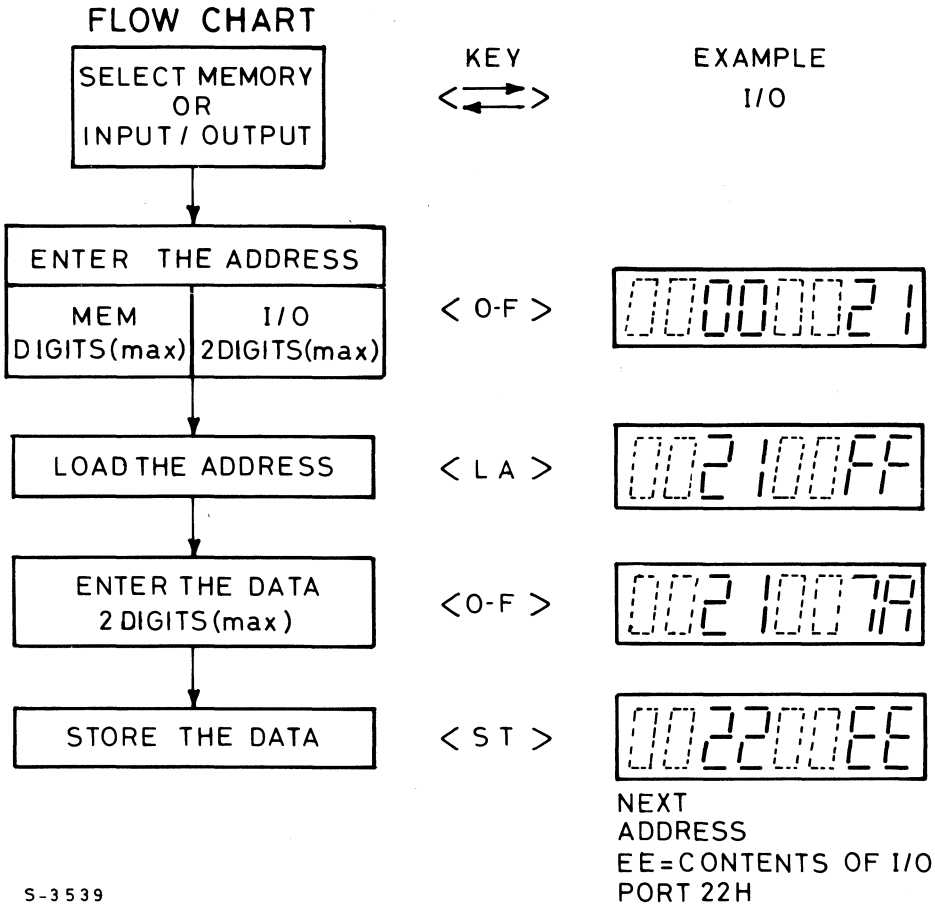
(2) Direct loading of 16-bit registers



LOADING CPU 16 BIT REGISTERS

The data stored in the register represents the memory address for the registers selected. The piece of data read on the right of the display is the content of the memory at that address.

(3) Loading of data in memory or in I/O port

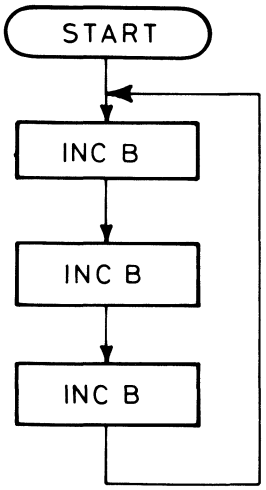


LOADING DATA IN MEMORY OR I/O PORTS

(9.2) Example of the creation of a program, execution and debugging

This is a simple program loop that includes two jump instructions. Each time the loop is completed the C register is incremented once and the B register twice.

Label	Instr		MEM Addr	Op code	Comments
STR:	INC	B	010F	04	Inc. reg. B
	JP	DWN	0110	C3	Jump to 130
			0111	30	
			0112	01	
DWN:	INC	B	0130	04	Inc. reg. B
	INC	C	0131	OC	Inc. reg. C
	JP	STR	0132	C3	Jump to 10F
			0133	0F	
			0134	01	



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FLOW CHART

(A) The program is entered as follows, note that the memory address is autoincremented after each (ST) store command.

Load example program in memory

Step	Key	Data	Display		LED	Comments
1	<RESET>		0000	00	PC	Reset system & CPU
2	-->>		0000	??	MEM	Select memory
3		010F		010F	MEM	Enter memory address
4	<LA>		010F	??	MEM	Load memory address
5		04	010F	04	MEM	Enter data - lst op code.
6	<ST>		0110	??	MEM	Store data & incr. mem. addr.
7		C3	0110	C3	MEM	Enter next op code
8	<ST>		0111	??	MEM	Store data & incr. mem. addr.
9	Continue to enter op codes 30,01... pressing <ST> each time to store and increment the memory address.					
10		0130		0130	MEM	Enter new memory address
11	<LA>		0130	??	MEM	Load new address
12		04	0130	04	MEM	Enter next op code
13	<ST>		0131	??	MEM	Store data and inc. mem. addr.
14	Continue to enter op codes up to the end of the program.					

before executing this program it is a good idea to check that the memory content is correct. To do this proceed as follows :

step	action
1	Select MEM
2	Enter start address (010F)
3	Load address (LA) and display first op.code
4	Movement the address (INC) and check the next code
5	Repeat, then check from (0130) up to (0134)

(B) Execution of this program using single step :

Execution of this program in single step

Step	Key	Data	Display	LED	Comments
1(*)	<RESET>		0000 ??	PC	Reset & clear registers
2		010F	010F	PC	Enter start address
3	<ST>		010F 04	PC	Store start address, display shows first op code.
4(**)	<<--		0000	BC	Display BC registors
5	<SS>		0100	BC	Execute lst instruction, this increments B
6	<SS>		0100	BC	Execute 2nd instruction, This is a jump to 0130
7	-->>		0130 04	PC	Look at PC to see that the jump was made
8	<<--		0100	BC	Display BC again
9	<SS>		0200	BC	Execute 3rd instruction
10	<SS>		0201	BC	Next instr. increments C
11	<SS>		0201	BC	Jump back to 010F
12	<<--		010F 04	PC	Check jump was made
13	Reapeat the <SS> single step and monitor that B increments twice, while C increments once for each loop.				

If (SS) is held pressed the program will be executed again and the content of registers B & C will increase slowly.

Notes :

(*) Step 1 can be used when the final result does not depend on the previous content of the registers or when each register concerned with the program is reset before execution.

(**) If command SS is used, with PC selected rather than BC, the program will jump along from instruction to instruction.

(C) Break points

To control the program (especially long programs) it is extremely useful to be able to insert Breakpoints. The use of the BRK command is illustrated in the first part of the following table. The second port shows the GO function in the execution of a progran with breakpoints. The <GO> key allows program execution at full speed.

Breakpoints

Step	Key	Data	Display	LED	Comments
1	<RESET>		0000 ??	PC	Reset system etc.
2	<BRK>		0	PC,BRK	Enter breakpoint mode at BP 0
3		0110	0110	PC,BRK	Enter BP address - this must correspond to the first op code of an instruction
4	<LA>		0110 0 C3	PC,BRK	Load address, display shows BP number and op code
5	<INC>		1	PC,BRK	Increment BP number - there are Eight BP's
6		0132	0132	PC,BRK	Enter next BP address
7	<LA>		0132 1 C3	PC,BRK	Load address of BP
8	<BRK>		0000 ??	PC	Leave BP mode
9		010F	010F	PC	Enter program start address
10	<GO>		0110 C3	PC	Run the program - it executes and stops at the 1st BP
11	<<--		0100	BC	Look at BC, it has incremented
12	-->>		0110 C3	PC	Back to PC
13	<GO>		0132 C3	PC	Continue execution up to the 2nd BP
14	<<--		0201	BC	Look at BC to confirm execution
15	-->>		0132 C3	PC	Back to PC
16	<SS>		010F 04	PC	Try a single step

Notes :

Use of the breakpoint in conjunction with <GO> and <SS> is indispensable when you have to check that a program is logically correct and when partial results (intermediate steps) are to be displayed. If only <GO> is used these would not be visible.

(9.3) Execution of DUMP and LOAD ON cassette

Programs previously stored in RAM can be recorded on cassette, DUMP, and if necessary reloaded, LOAD, into RAM.

The cassette recorder must be connected to J3 on the CLZ80/NC board. A high quality tape free from drop-outs must be used in the recorder. The correct sequence of steps for the LOAD and DUMP operations are listed below :

DUMP CASSETTE

(1) switch the keyboard switch TTY-CASS to CASS.
(2) position the tape where the recording is to be made.
(3) select -->> MEM mode
(4) Enter the starting address for the dump <AAAA>(Hex)
(5) Load the address <LA>
(6) Enter the length of the block to be dumped (number of bytes) <LLLL>(Hex), the display will show the entry point on the left and the length of the block on the right.
(7) Press the dump key <DP>. The display wll go off.
(8) Make sure the recorder is ready. Select RECORD - if autocontrol is used the cassette motor will remain OFF.
(9) Press <GO> to start the dump or output of data. The motor will start and after about a 20 sec. pause the data recording will begin. During the pause a tone is sent to allow the recorder AGC to settle and the tape leader to pass the head.
(10) The recorder will stop at the end of the dump.
(11) Switch off the recorder.
(12) Press any key on the keyboard to return control to the operating system.

LOAD CASSETTE

The Nanocomputer can load programs stored on a cassette written in two different record formats : FR-Z, the SGS-ATES Monitor/Editor/Assembler which uses 2x4 bit nibbles per character recorded, or NC-Z format described in 5.3.3, page 59.

(1) Switch the keyboard switch TTY-CASS to CASS.
(2) Position the tape where the data to be loaded commence.
(3) To load a cassette written in the FR-Z format press the following keys : <2ND><LD>.
To load a cassette written in NC-Z format press only the key : <LD>
(4) Start the tape playback.
(5) The tape will stop automatically if automatic cassette motor control is used at the end of the data record.
(6) Switch off the recorder.
(7) Press any key on the keyboard to return control to the opeating system.

During a load operation the program checks for the correct checksum recorded with each data block. If any error occurs the tape stops and the ERR light is switched on. In this case repeat the load.

(9.4) DUMP and LOAD on serial terminal (TTY printer and tape reader)

The serial TTY must be connected to J5 on the CLZ80/NC board.

DUMP TTY (printer or tape punch)

(1) Switch the keyboard switch TTY-CASS to TTY.
(2) Select the speed of serial transmission by loading two memory locations as follows :

Band rate	OFAE	OFAF	Notes
600	9A	00	preset value
300	35	01	
110	55	03	

(3) Select -->> MEM mode.
(4) Enter the starting address for the dump <AAAA>(Hex).
(5) Press the <LA> key to load the address.
(6) Enter the number of bytes to be dumped <LLLL>(Hex).
(7) Press the <DP> key and switch on the tape punch.
(8) Press the <GO> key & after a delay of 20 secons the data transmisson will start to the terminal.
(9) Press any key on the keyboard to return control to the operating system.

LOAD from TTY(tape reader)

(1) Switch the keyboard switch CASS/TTY to TTY, and set the baud rate.
(2) Insert punched tape in reader.
(3) Press <LD>, the display will go off.
(4) Start the reader.
(5) Wait until end of recorded tape.
(6) Stop reader.
(7) Press any key on the keyboard to return control to the operating system.

If the ERR light remains off the LOAD operation has been successfull.

LOAD from TTY (terminal keyboard)

Although manual data input operation is possible it is not recommended as the error rate will undoubtedly be higher than using the input data station and the checksum must be manually calculated. The input data must be in the correct format including the checksum byte.

10. EXPANSION OF THE SYSTEM

The Nanocomputer boards use a bus structure, the Gamma-bus, which is compatible with a full range of boards in the CLZ80 Microcomputer range.

10.1 HARDWARE

The CLZ80/NC board has some components missing in order to reduce the cost and adapt it to Education needs. The board can be upgraded to a CLZ80-4/2 microcomputer with a component kit KNZ80.

The KNZ80 kit contains :

- a UART 8251 for serial communications
- a DC-DC convertor for on board generation of the +/-12V and -5V supplies, so that the board needs only a single +5V supply
- 2K ROM program MO-Z which is a monitor, debug, loader (audio cassette)
- a PROM for the reset jump to the entry point of the MO-Z program.
- a connector J4 for the WIZ80 mini control panel.

The CLZ80 Microcomputer range is based on a bus structure and two card cages are available, 4 slot CPZ80 and 8 slot CTZ80. These card cages provide a shielded Gamma-bus interconnect for the following boards of the microcmputer family :

VDZ80 Video display board

FLZ80 Floppy disk rlontroller board

PPZ80 EPROM programmer board

RAZ80 Memory expansion (16-48K byte) board

PIZ80 Input/output expansion board (4 PIO, lSIO and lCTC)

A complete set of cables, power supplies, peripherals - floppy drives, printers, terminals etc - is available.

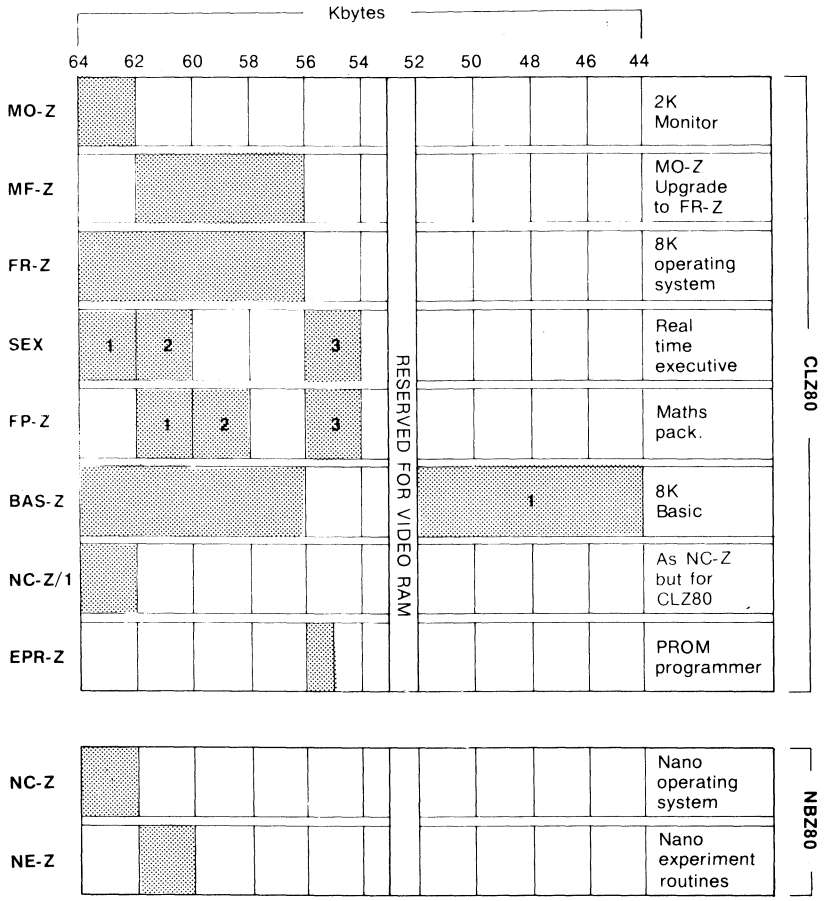
The RAM memory of the CLZ80 board can be expanded from 4k up to 16k by replacing the M4027 RAM's with M4116 16K dynamic RAM's no further components are required.

10.2 SOFTWARE

The software for the microcomputer range which can be used on the CLZ80 card is as follows :

MO-Z	2K byte Monitor, debug, loader in one M2316E ROM
MF-Z	6K byte Editor, assembler in three M2316E ROM's
BAS-Z	8K byte BASIC high level language in four M2316E ROM's
SEX	2K byte multiuser executive in one M2716E EPROM
FP-Z	2K byte floating point maths package in one M2716E EPROM
EPR-Z/0	1K byte EPROM programmer for the PPZ80 board in one M2708 EPROM

The MO-Z plus MF-Z together make up the FR-Z 8K operating system. Some software is available in different versions mapped to different locations as shown in the memory map below.



A version of the Nanocomputer program NC-Z/1 is available which has been adapted for use on a CLZ80 board. This enables users who have upgraded the CLZ80/NC to a CLZ80 board to continue to use the microcomputer as a Nanocomputer data input/display station.

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Printed in Italy