ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

PREFACE

This Technical Guide contains a detailed explanation of the operation of the CPU module, the floppy disk controller, display/keyboard, disk drives, and power supplies for the computer. General checkout procedures to aid you in tracing problems to a specific subassembly or PC board but no further are included. Information on the hard disk controller board, floppy disk drive, and hard disk drive is also provided. In addition, you will find data sheets for several of the integrated-circuit chips used in this computer.

This guide limits repair procedures to replacement of subassemblies only. A parts list containing part numbers for major subassemblies may be found in Section 1, item 8. Additionally, a detailed parts list for each subassembly may be found at the end of each section. Using the part numbers, you can order the major subassemblies and some components through your Panasonic Service Office.

To aid you in recognizing problem areas, we recommend that you obtain a diagnostics disk and an RS-232C loop-back plug from the Panasonic Service Office.

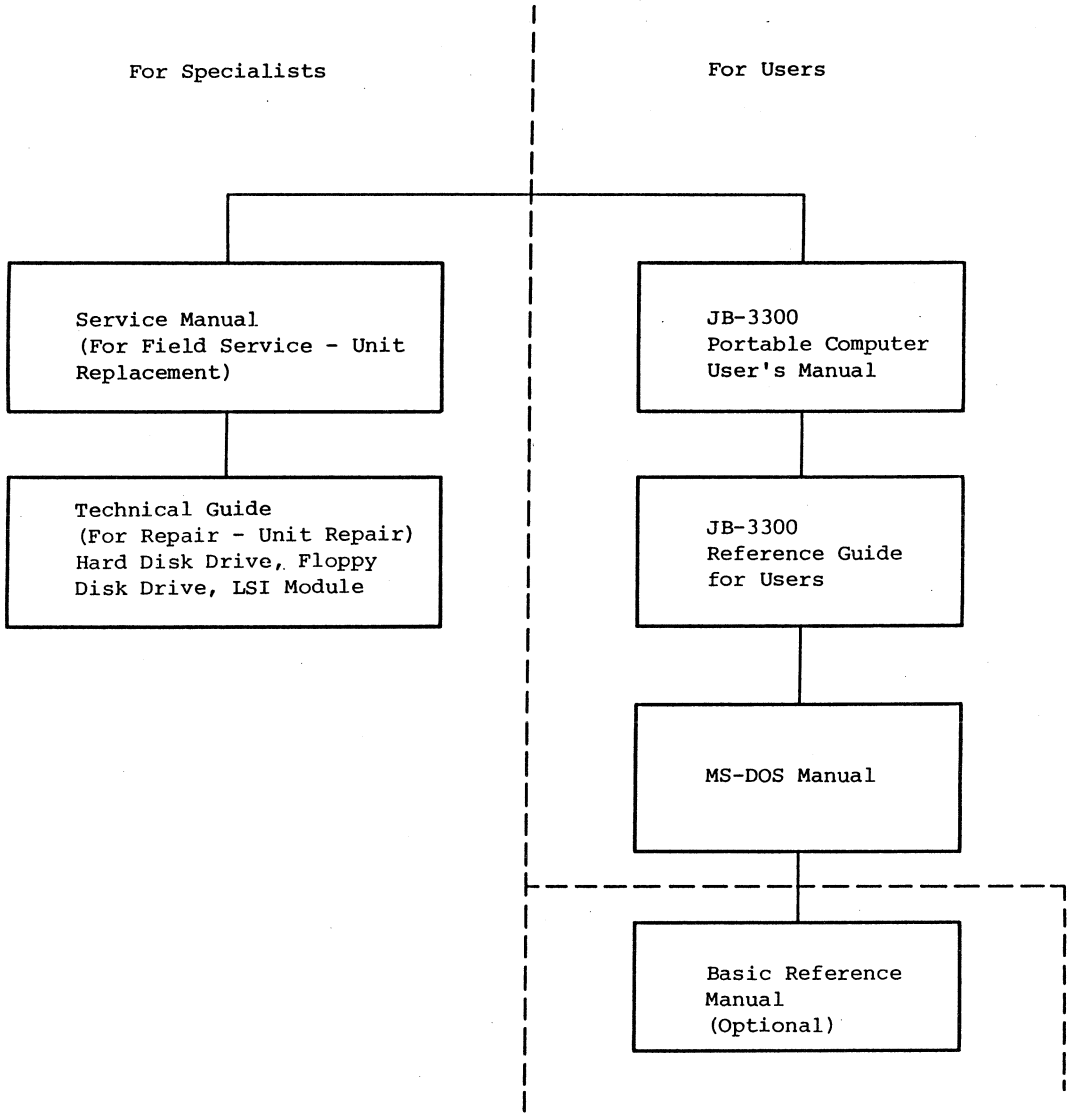
If you have any problems with the computer, contact the service office.

IMPORTANT NOTICE

This Technical Guide is written for engineers who have a thorough understanding of electronics and computer circuitry and who are authorized to repair the computer. It is not intended for the beginner.

If an unauthorized person should use this guide to repair, modify, or alter the computer, Panasonic cannot be held responsible or liable for any damage caused or alleged to be caused. We strongly suggest that for proper servicing, the computer be returned to Panasonic.

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Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

I. GENERAL

1. SPECIFICATIONS

1.1 Logic Unit

CPU	8088 4.77 MHz
Math Co-processor	8087 (Optional)
ROM	16K bytes EPROM in socket (27128)
RAM	256K bytes Standard extendable to a total of 640K bytes
RAM Expansion	Up to 512K bytes on main P.C.B. 128K bytes optional (512-640K bytes) inserting RAM board for PC or XT into option slots
Interrupt	IBM-XT Compatible
DMA	IBM-XT Compatible
Timer	IBM-XT Compatible
Sound Logic	IBM-XT Compatible
Floppy Disk Controller	IBM-XT Compatible
Hard Disk Controller (Hard Disk version)	IBM-XT Compatible Option slot is not occupied
Display Controller	IBM-XT Compatible Special for Plasma Panel
Character Mode	25 x 80 characters 400 x 640 pixels 16 x 8 char. box or 25 x 40 characters 400 x 320 pixels 16 x 8 char. box
Graphic Mode	200 x 320 pixels 200 x 640 pixels or 400 x 640 pixels

Serial Port	RS-232C IBM-XT Compatible
Parallel Port for Printer	IBM-XT Compatible
Option Slots	2 slots 13-inch Card is acceptable IBM-XT Compatible
Plasma Display Select Switch	Selecting Plasma Display ON or OFF RGB color CRT is available with its adapter card in option slot, by selecting "plasma-off" of this switch

1.2 Plasma Display

Resolution	640(H) x 400(V) dots
Panel Size	Dot pitch 0.3(H) x 0.36(V) mm Viewing are 192(H) x 144(V) mm (Equivalent to 12-inch CRT) Aspect Ratio 4(H) : 3(V)
Color	Neon Orange
Residual Image	NO

Intensity Control for the Whole Screen

1.3 FLoppy Disk Drive

Type	5.25-inch (JA-551-035N) (SA455) Double Sided and Double Density
Number of Drives	2 drives (Floppy Disk Version) or 1 drive and 1 Hard Disk (Hard Disk Version)
Capacity	Double sided and double density 500K bytes (unformatted) 320K bytes or 360K bytes (formatted)
Access Time	
Average	68 ms
Track to Track	4 ms
Settling Time	15 ms
Average Latency	100 ms

Motor Start Time	250 ms
Track Density	48 TPI
Number of Track	(40 tracks + extra 1 track) x 2

1.4 Hard Disk Drive (Hard Disk Version)

Type	3.5-inch (JU-104)
Number of Drive	1 drive
Capacity	12.75 MB (unformatted) 10 MB (formatted)
Access Time	
Average	85 ms
Track to Track with Settling	18 ms
Average Latency	8.3 ms
Track Density	500 TPI (Fourteen tracks are reserved in addition as alternate tracks)
Number of Track	306 tracks

1.5 Keyboard

Number of Keys	IBM-XT Compatible 84 keys
Keyboard Scan Codes	IBM-XT Compatible
Interface	IBM-XT Compatible Serial DIN connector
Layout	IBM-XT Compatible Cylinderical Sculpture Type
Additional Features	Wider Return key Long Return key next to Ten key pad Lighted indicators on CAPS LOCK and NUM LOCK keys Finger homing bumps on F, J, and 5 key of Ten key pad
National Versions	ASCII, English, Swedish/Finish, French, German

Stroke	4 mm ±0.5 mm
Key Pitch	19.05 mm
Interlock	N key Rollover
Dimension	430(W) x 28(H) x 155(D) mm
Detachable	Yes

1.6 Power Supply

Input	(220 to 240 VAC) ±10% 50 to 60 Hz or (110 to 120 VAC) ±10% 50 to 60 Hz (Switchable)
Consumption	220 VAC 1.5 A max 110 VAC 2 A max 160 W
Output	5 VDC 10.4 A max 12 VDC 1.6 A max -12 VDC 0.26 A max -5 VDC 0.3 A max -205 VDC 0.15 A max -200 VDC 0.1 A max

1.7 Fan

Input	12 VDC
Consumption	0.08 A

* Power is supplied from the CPU board.

1.8 Software

1.8.1 System Software

DOS	MS-DOS Version 2.11
BIOS	IBM-XT Compatible Identical function call Identical values returned from Bios functions Same variable address

1.8.2 Program Languages

BASIC	IBM-XT Compatible (ROM BASIC is not available)

1.9 Dimensions

Width	430 mm
Depth	312 mm
Height	155 mm

1.10 Weight

FDD Version	Approx. 11.5 kg
HDD Version	Approx. 11.5 kg

1.11 Environmental Limits

	Operating	Storage
Temperature	5°C to 35°C	-15°C to 50°C
Humidity	35 to 80%RH (No condensation)	5 to 95%RH (No condensation)
Temperature gradient	15°C/hour	15°C/hour
Shock	0.5G	40G
Vibration	0.2G	1G (except resonant frequency)
Height	0 to 2134 (7000 ft)	

1.12 Destinations vs. Model Names

Destinations	Model Names
West Germany	JB-330*1ED*2
Great Britain	JB-330*1EE*2
France	JB-330*1EF*2
Sweden/Finland	JB-330*1ES*2
Holland	JB-330*1EL*2
Australia	JB-330*1EA*2
Hong Kong	JB-330*1EH*2

*1: 1: FD version
5: HD version

*2: 0: 256K byte memory
1: 512K byte memory

2. SYSTEM CONFIGURATION

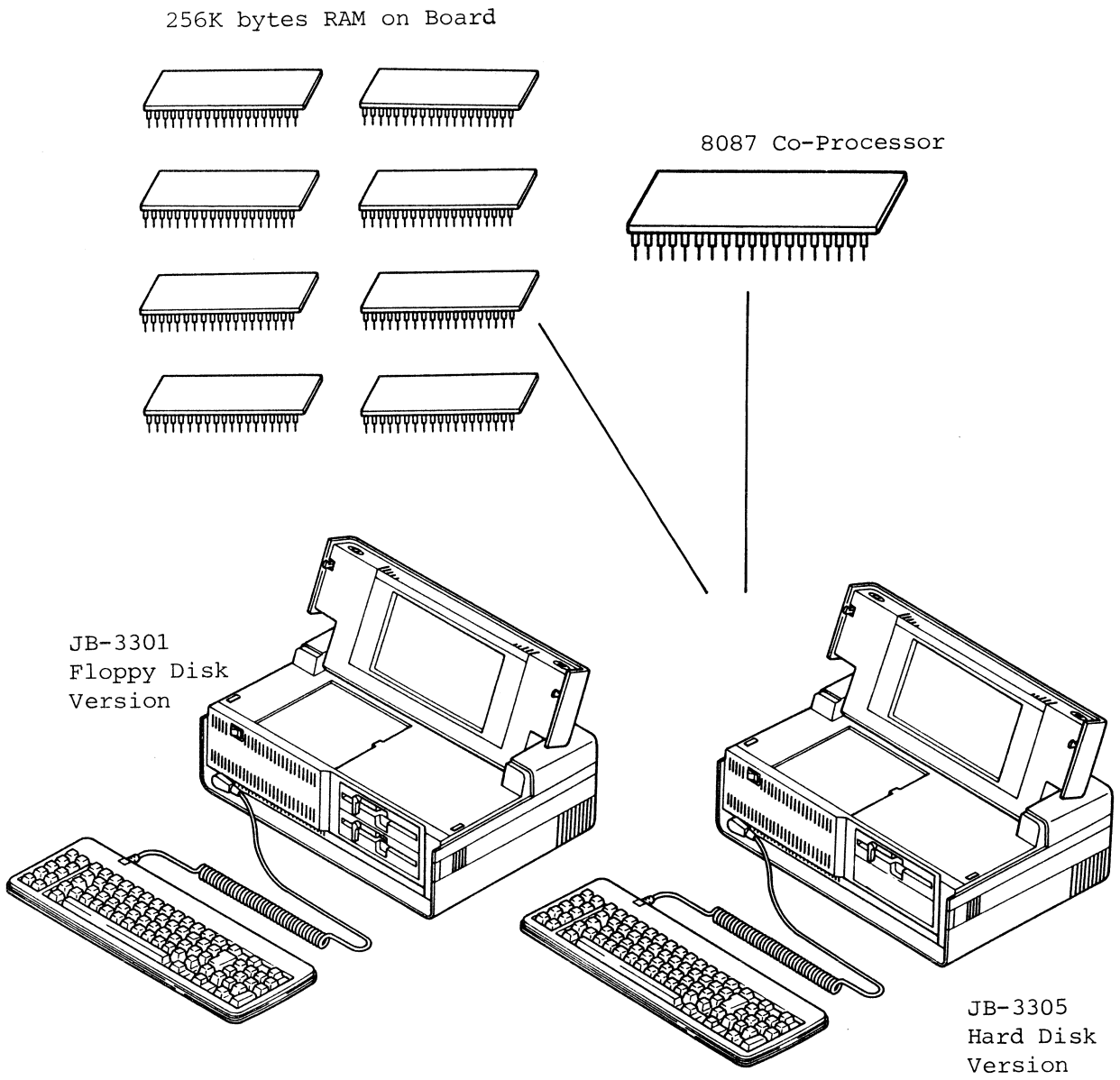


Figure 2-1 System Configuration

Appearance

(a) JB-3301

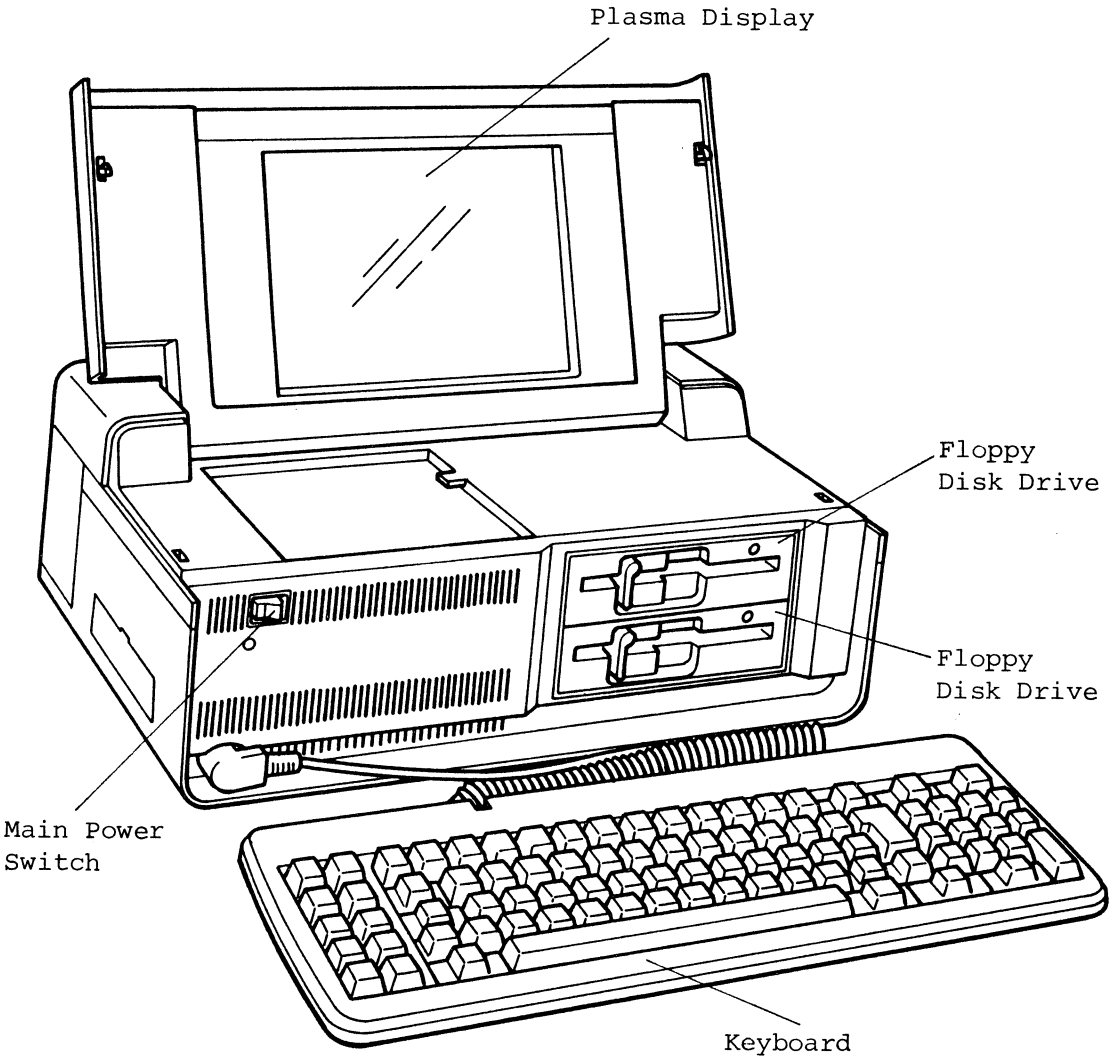


Figure 2-2

(b) JB-3305

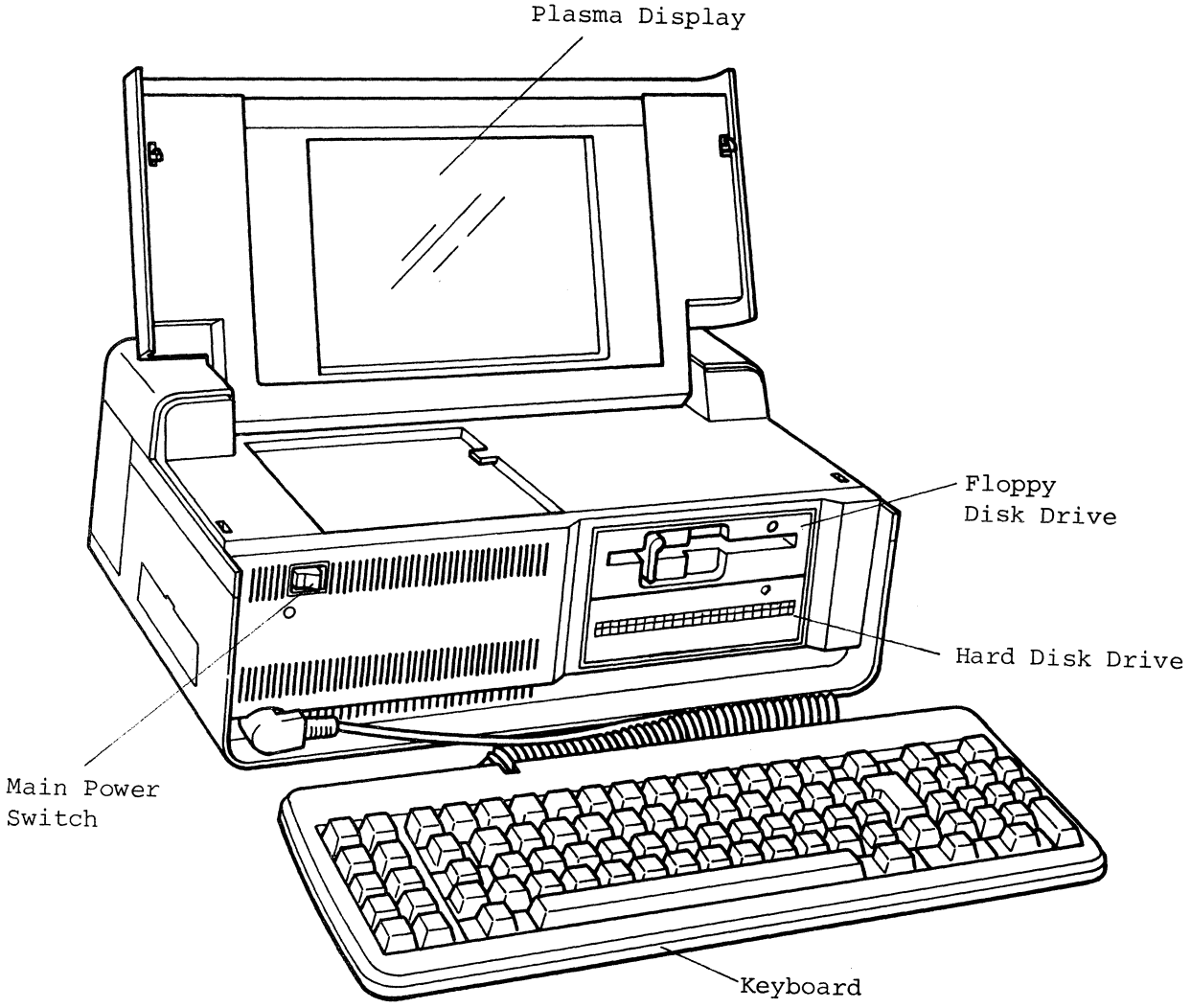


Figure 2-3

3. BLOCK DIAGRAM

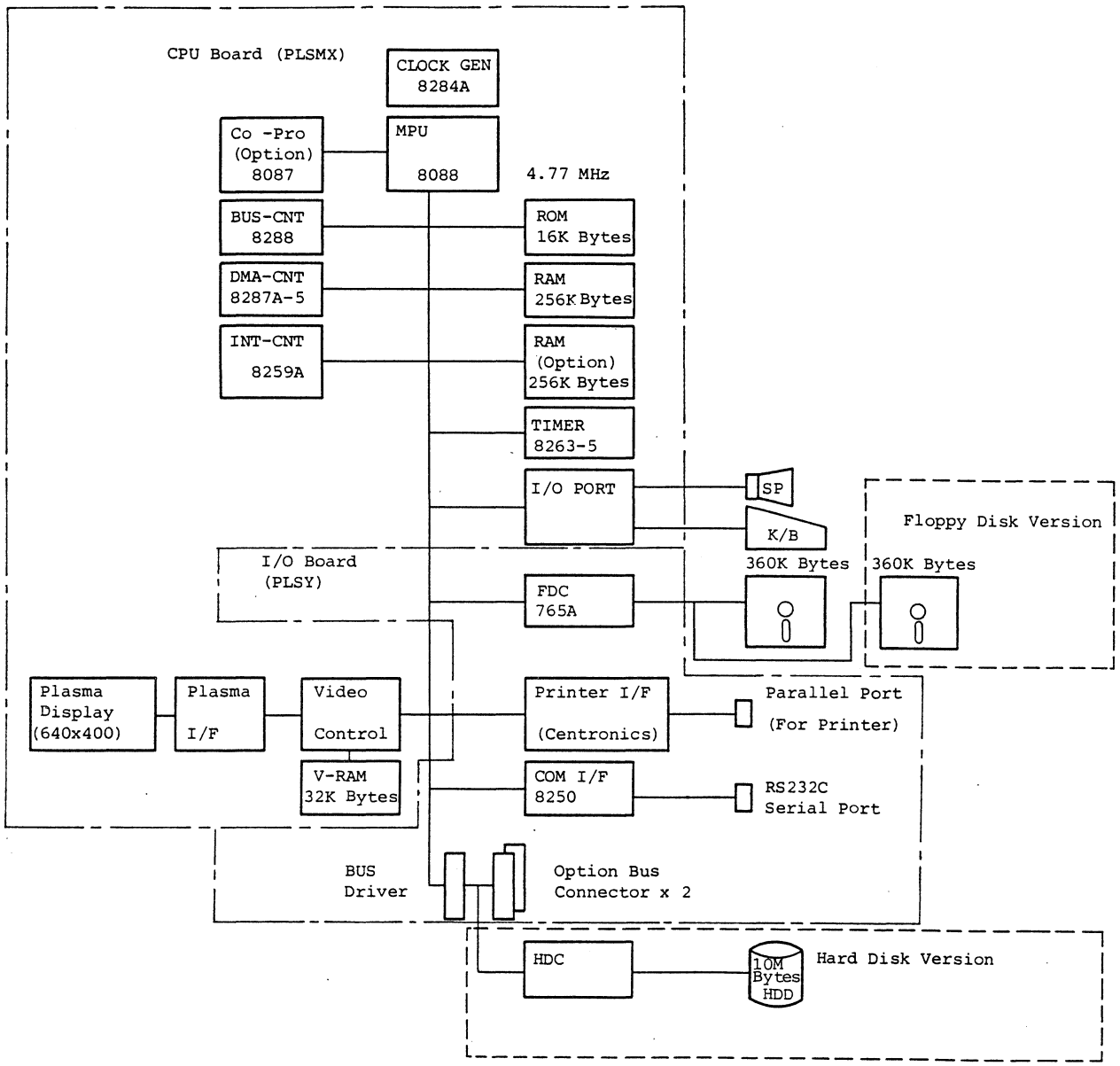


Figure 3-1 Block Diagram

4. HARDWARE OUTLINE

4.1 General Description

This computer comprises two units: the system unit containing the plasma display panel (PDP) and disk drives, and the keyboard unit.

The system unit consists of five units:

- o CPU Board (PC board marking: PLSMX)
- o I/O Board (PC board marking: PLSY)
- o Power Supply Unit (PSU)
- o Plasma Display Panel (PDP)
- o Disk Drives

  Two floppy disk drives
  (Floppy disk version: JB-3301)
  One floppy disk drive and one hard disk drive
  (Hard disk version: JB-3305)

Figure 4-1 shows an internal view of the system unit.

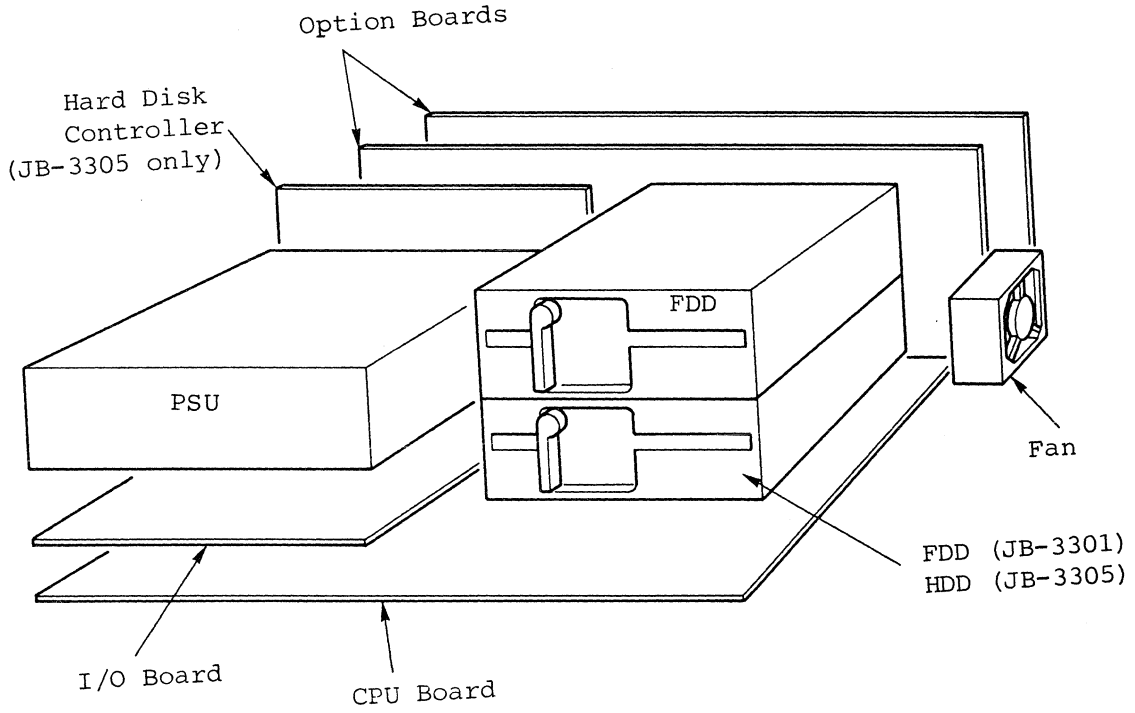


Figure 4-1 Internal View

4.2 Ventilation

This computer is provided with a fan for ventilation. Air enters through intake vents at the top of the plasma display unit, and also at the bottom of the display unit, and is forced out the side of the system unit by the fan. The following diagram illustrates the ventilation mechanism.

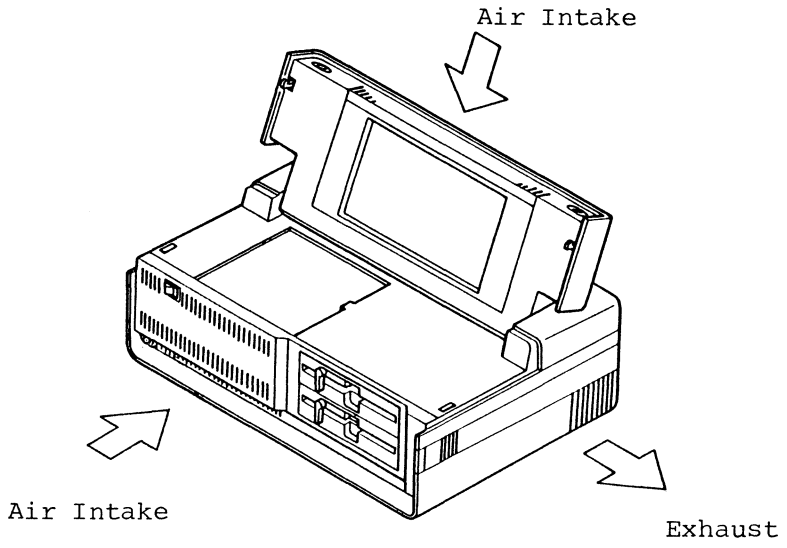


Figure 4-2 Ventilation Diagram

4.3 Memory Configuration

Standard memory configuration for the computer is: 256K-bytes RAM, 32K-bytes video RAM, and 16K-bytes ROM. This minimum standard memory is called the 256K-bytes system.

Memory can be increased to 512K bytes with optional 256K RAM chips inserted in the IC sockets on the CPU board. This is called the 512K-bytes system.

Memory can be increased further to 640K bytes with an optional 128K RAM board (for PC or XT) inserted into the option slot.

Figure 4-3 shows the memory map of both the 256K-byte and 512K-byte systems.

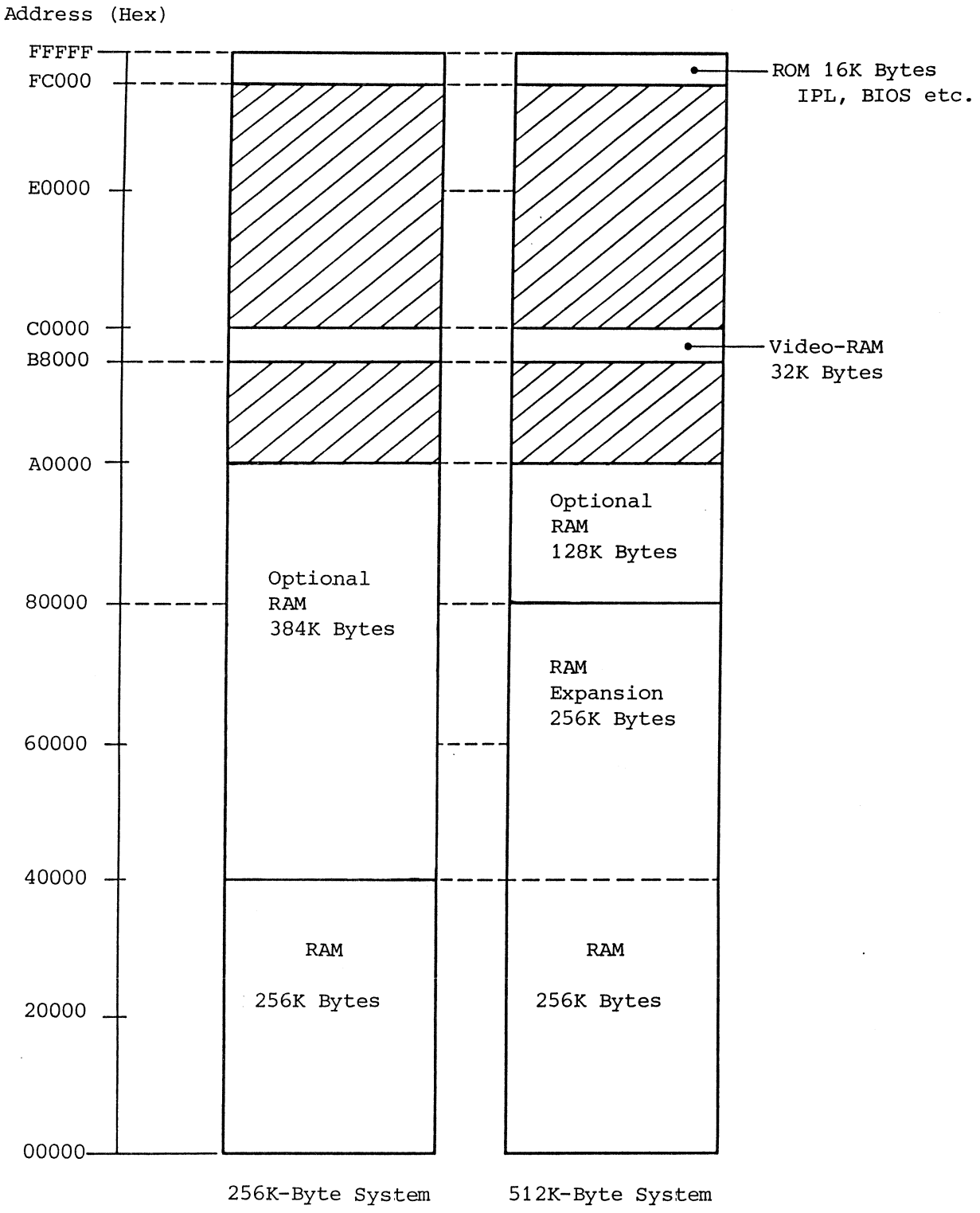


Figure 4-3 System Memory Map

4.4 Input/Output Structure

The computer I/O structure uses the lower eleven bits of an MPU address when issuing an I/O command, and all I/O addresses are allocated to spaces in addresses 000(HEX) to 3FF(HEX).

Table 4-1 shows an I/O address map.

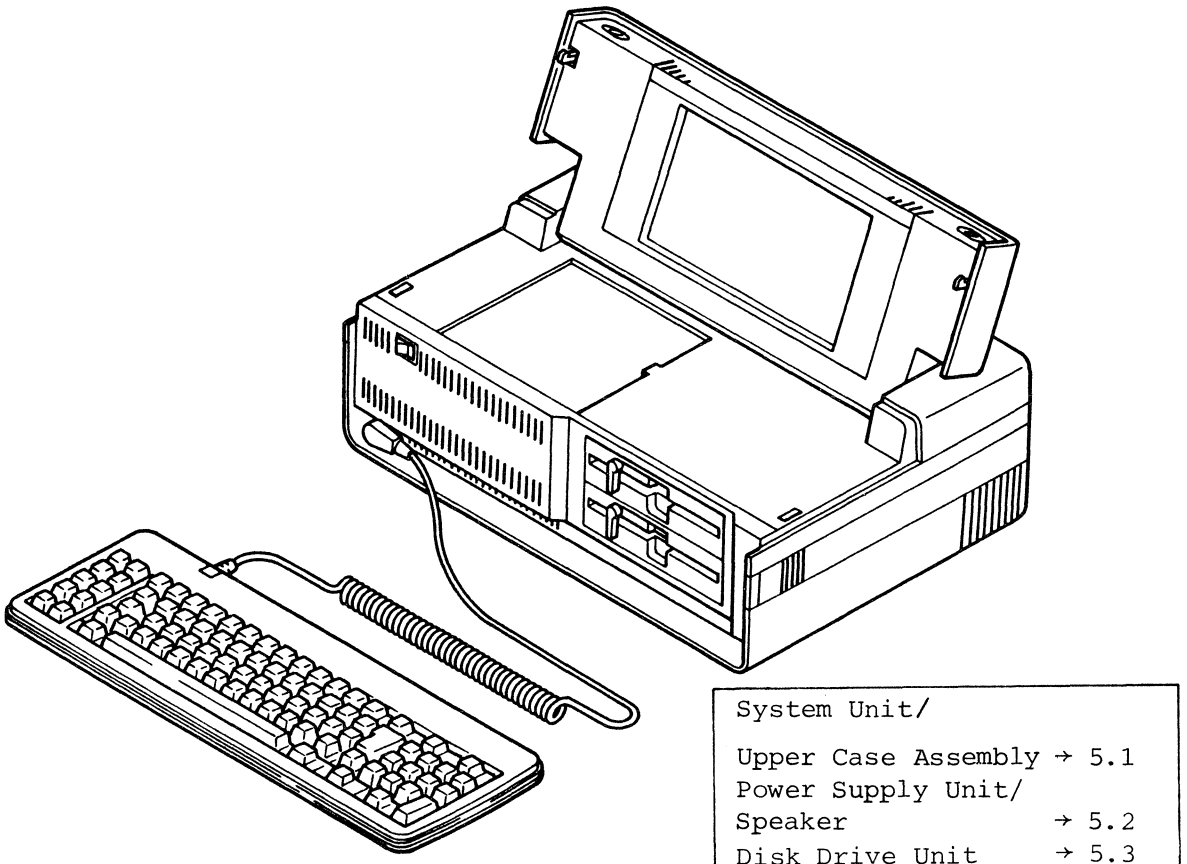
Table 4-1 Input/Output Address Map

Hex Range	Usage
000 - 00F	DMA chip 8237A-5
020 - 021	Interrupt chip 8259A
040 - 043	Timer chip 8253-5
060 - 063	PPI chip 8255A-5
080 - 083	DMA page registers
0AX	NMI mask register
320 - 323	Hard disk
378 - 37F or 278 - 27F	Parallel port (Centronics printer) strap select
3D0 - 3DF	Display (Color/Graphics)
3F0 - 3F7	Floppy disk
3F8 - 3FF or 2F8 - 2FF	Serial port (Asynchronous communications) strap select

5. DISASSEMBLY PROCEDURE

To use this section, please consult the index page that follows, choosing the area that corresponds to your problem by referring to the page numbers after each heading.

Important: For the hard disk version, execute the SHIP command before starting disassembly.



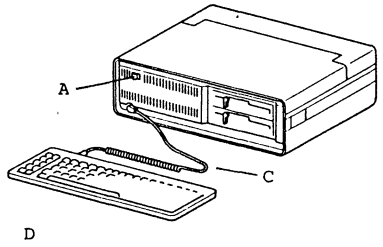
System Unit/	
Upper Case Assembly	→ 5.1
Power Supply Unit/ Speaker	→ 5.2
Disk Drive Unit	→ 5.3
Fan/I/O Board	→ 5.4
CPU Board	→ 5.5

Figure 5-1

5.1 System Unit/Plasma Display Unit

Step 1

Preparation for Disassembly



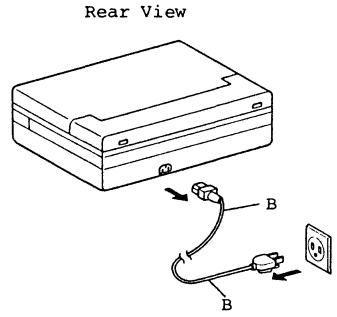


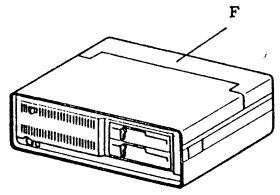
Figure 5-2

1. Set Main Power Switch [A] to OFF.
2. Unplug AC Cable [B] from outlet.
3. Disconnect all cables (AC Power Cord [B], Keyboard Cable [C], and all optional unit cables) from System Unit.
4. Move Keyboard [D] and all optional units away from working area.

Caution: When removing the keyboard cable [C], hold the connector part and pull it toward you. Do not pull the cord directly.

Step 2

Removing Rear Cover



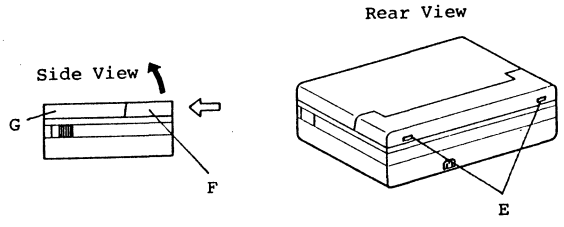


Figure 5-3

1. Press down on thumbsets [E] of Rear Cover [F] and unlatch claws inside, then lift Rear Cover [F] up from Plasma Display Unit [G].

Note: Do not use screwdriver to wedge apart Rear Cover from Plasma Display Unit.

Step 3

Removing Front Panel

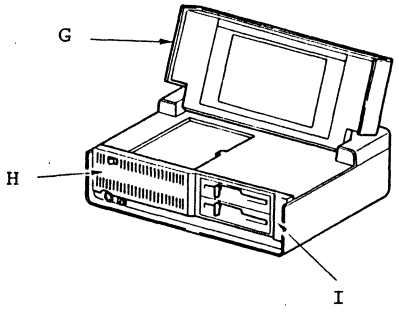


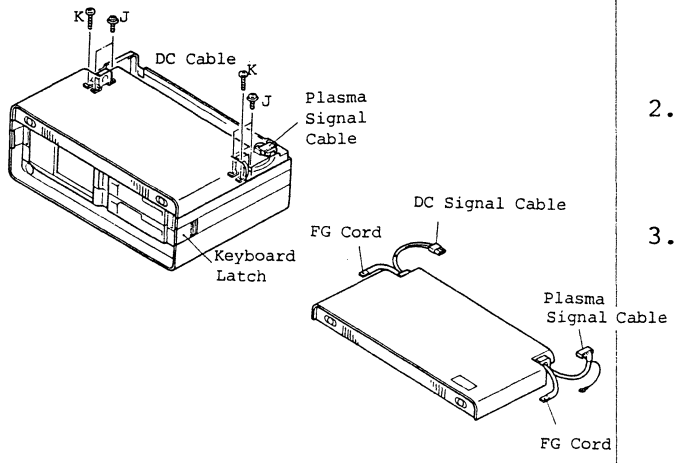
Figure 5-4

1. Lift up Plasma Display Unit [G].
2. Pull up Left Front Panel [H] from the bottom, lifting it up from System Unit.
3. Pull up Right Front Panel [I] from the bottom, lifting it up from System Unit.

Note: By pressing the top portions of front panels [H] and [I] downward with both hands, claws on their bottoms can be released from System Unit.

Step 4

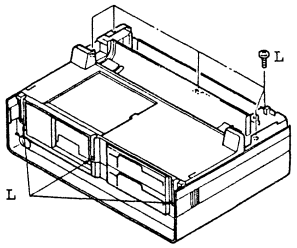
Removing Plasma Display Unit



1. Remove the four screws [J] on the softeners attached to either side of the plasma display.
2. Remove the FG wires at both ends of the softener (by loosening screw K).
3. Remove the DC single cable and plasma signal cable.

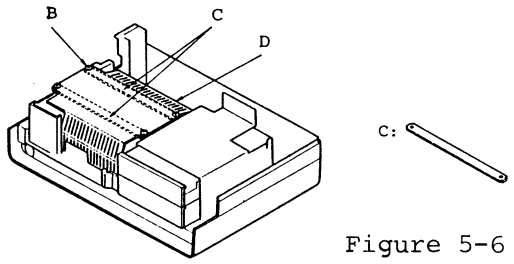
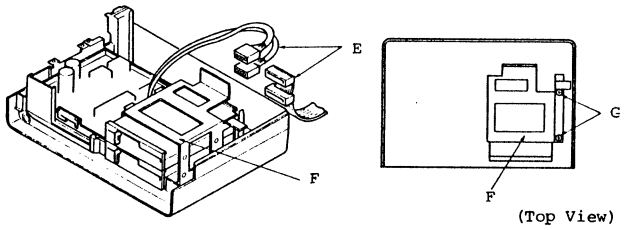
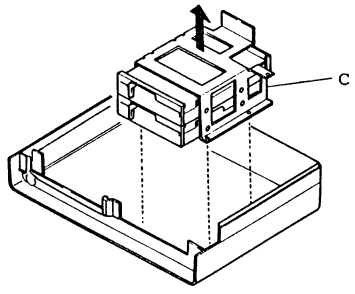
Step 5

Removing Upper Cover



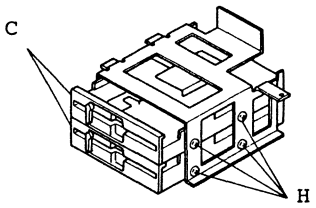
1. Remove mounting screws [L] from Upper Cover.
2. Remove Option Connector Door [E].
3. Remove Keyboard Latch Assemblies [F].

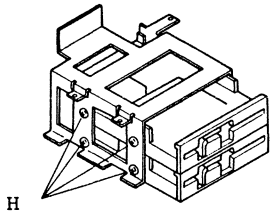
5.2 System Unit/Floppy Disk Drive Unit

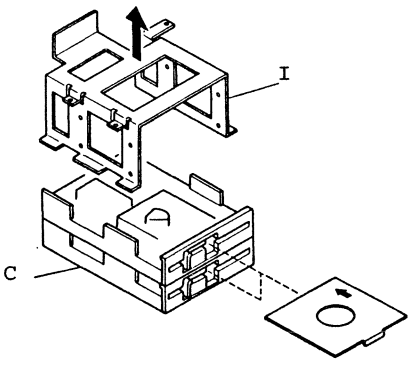
Step 1 Removing Plasma Display Unit	1. Remove Plasma Display Unit (see 5.1 Steps 1 through 5).
Step 2 Removing Reinforcement Plates  Figure 5-6	1. Remove screws [B] retaining Reinforcement Plates [C]. 2. Remove PSU Shield Plate [D]. 3. Remove Reinforcement Plates [c].
Step 3 Removing Floppy Disk Drive Unit  Figure 5-7	1. Disconnect Connectors [E] from Floppy Disk Drive Unit [F]. 2. Remove mounting screws [G]. 3. Slide Floppy Disk Drive Unit [F] to the right as indicated by arrow, then lift it up from System Unit.
Step 4  Figure 5-8	1. Remove Floppy Disk Drive Unit [C].

Step 5

Removing Floppy Disk Drive Stay







Head Protection Sheet

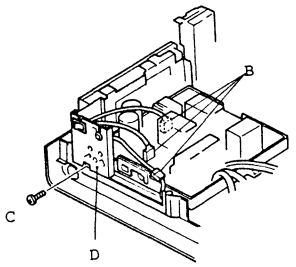
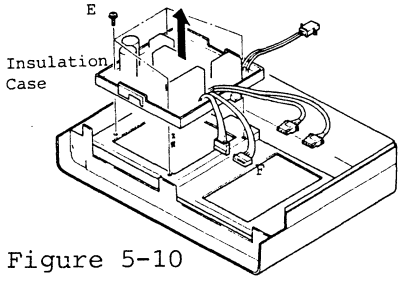
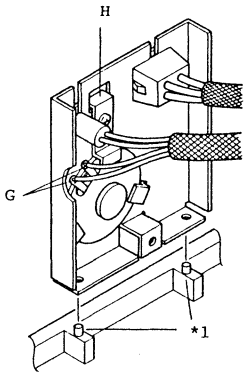
Figure 5-12

1. Remove screws [H] on both sides of Floppy Disk Drive Unit [C].
2. Remove Floppy Disk Drive Stay (Support Plate) [I] from Floppy Disk Drive Unit [C].
3. Insert the head protection sheets in the floppy disk drive [C].

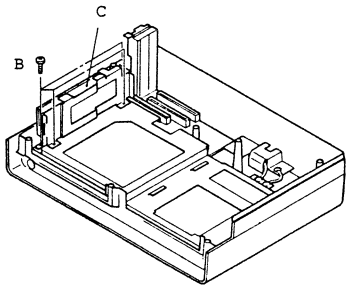
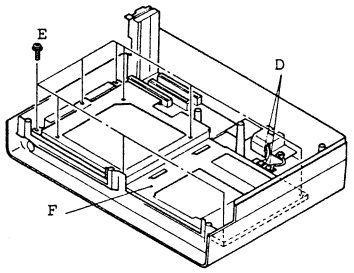
* Reverse steps for reassembly.

Caution: The Drive with the terminator must be placed on the top when reassembling.

5.3 System Unit/Power Supply Unit/Speaker

Step 1 1. Removing Plasma Display Unit 2. Removing Flppy Disk Drive Unit	1. Remove Plasma Display Unit [A] (see 5.1 Steps 1 through 5). 2. Remove Floppy Disk Drive Unit (see 5.2 Steps 1 through 4).
Step 2 Removing Power Switch Plate  Figure 5-9	1. Disconnect Connectors [B]. 2. Remove mounting screw [C]. 3. Remove Power Switch Plate [D]. Note: Before removing the switch plate, lift it once to prevent the claw from being broken.
Step 3 Removing Power Supply Unit  Figure 5-10	1. Remove screws [E] mounting system unit. 2. Disconnect connectors [F] from CPU and I/O Boards. 3. Remove Power Supply Unit. 4. Remove Power Supply Board with Insulation Case.
Step 4 Removing Speaker  Figure 5-11	1. Suck solders [G]. 2. Remove screw [H]. 3. Slide up and remove the speaker.

5.4 System Unit/Handle Mounting Assembly/I/O Board

Step 1 1. Removing Plasma Display Unit 2. Removing Floppy Disk Drive Unit 3. Removing Power Supply Unit	 1. Remove Plasma Display Unit (see 5.1 Steps 1 through 5). 2. Remove Floppy Disk Drive Unit (see 5.2 Steps 1 through 4). 3. Remove Power Supply Unit (see 5.3 Steps 1 through 3).
Step 2 Removing Handle Mount Assembly  Figure 5-13	 1. Remove mounting screws [B]. 2. Remove Handle Mount Assembly [C].
Step 3 Removing Base Plate  Figure 5-14	 1. Detach FG Cable [D]. 2. Remove mounting screws [E]. 3. Lift up Base Plate [F].

Step 4

Removing I/O Board

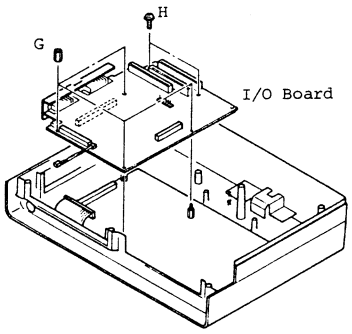


Figure 5-15

1. Disconnect Connectors from I/O Board.

2. Remove plate supports [G] and screws [H].

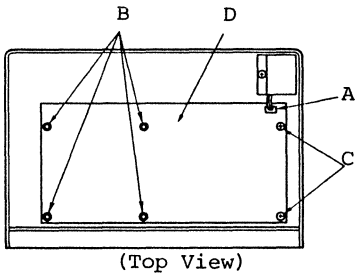
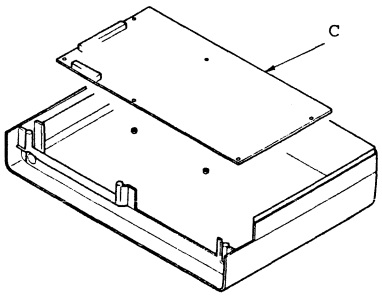
3. Lift up I/O Board [B].

Note: When removing I/O Board [B] pull it from the I/O connector side (left side of the bottom) as the serial and parallel ports slightly lifted while the bottom is retained.

* Reverse Steps for reassembly.

Important: When reassembling the I/O board, be sure to properly connect the connectors between the I/O board and the CPU board.

5.5 System Unit/CPU Board

Step 1	
1. Removing Plasma Display Unit	1. Remove Plasma Display Unit (see 5.4 Steps 1 through 5).
2. Removing Floppy Disk Drive	2. Remove Floppy Disk Drive (see 5.2 Steps 2 through 4).
3. Removing Power Supply Unit	3. Remove Power Supply Unit (see 5.3 Steps 2 through 3).
4. Removing I/O Board	4. Remove I/O Board (see 5.4 Steps 2 through 4).
Step 2 Removing CPU Board  (Top View)  Figure 5-16	1. Disconnect Connector [A] from CPU Board [D]. 2. Remove PCB support [B] and screws [C] retaining CPU Board [D]. 3. Lift up CPU Board [D] from Base Unit.

* Reverse Steps for reassembly.

Important: When reassembling the I/O board, be sure to properly connect the connectors between the I/O board and the CPU board.

5.6 Precautions New Handling MOS ICs

The LSI used on the control board is called MOS IC, which requires handling different from that for other ICs because of its structure. Its internal electrodes break because of voltage (static electricity and leakage from a soldering iron) from the exterior. Although reliability is increased by providing protective transistors for internal electrodes, there are cases where protective transistors are broken when the voltage is too large. When servicing, storing and during return shipment, the MOS IC should be handled with extreme care, with thorough attention paid to the following points:

(a) There are cases where voltage is due to leakage from the soldering iron during soldering. Use a high insulation type soldering iron, or if an ordinary soldering iron is used, ground it to the chassis as shown in Figure 5-17.

(b) Do not carry out soldering or replacement while the power is on.

(c) Be sure to attach the MOS IC to a black electroconductive sponge during storage or return shipment. (The MOS IC to be repaired should be attached to the electroconductive sponge before shipment (Figure 5-28).)

(d) Do not place the MOS IC on plastics liable to be charged with static electricity. Do not attach it to styrofoam instead of an electroconductive sponge.

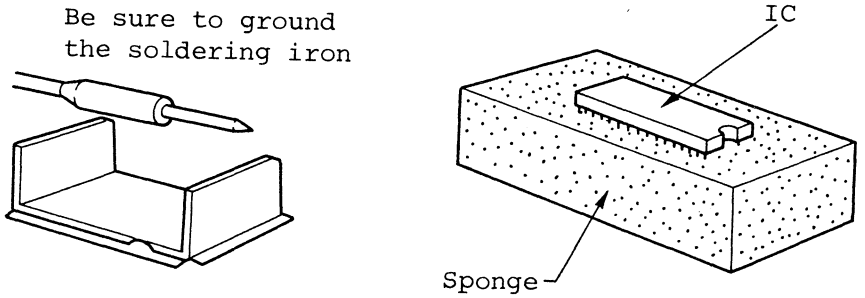


Figure 5-17

LSI IC Replacing Procedures

Use a soldering iron with a fine tip of around 30 W and a solder sucker. If the soldering iron is not a suction type, suck the solder by using a plunger or braided wire used to coat the display unit grounding.

6. PARTS LOCATION

System Unit

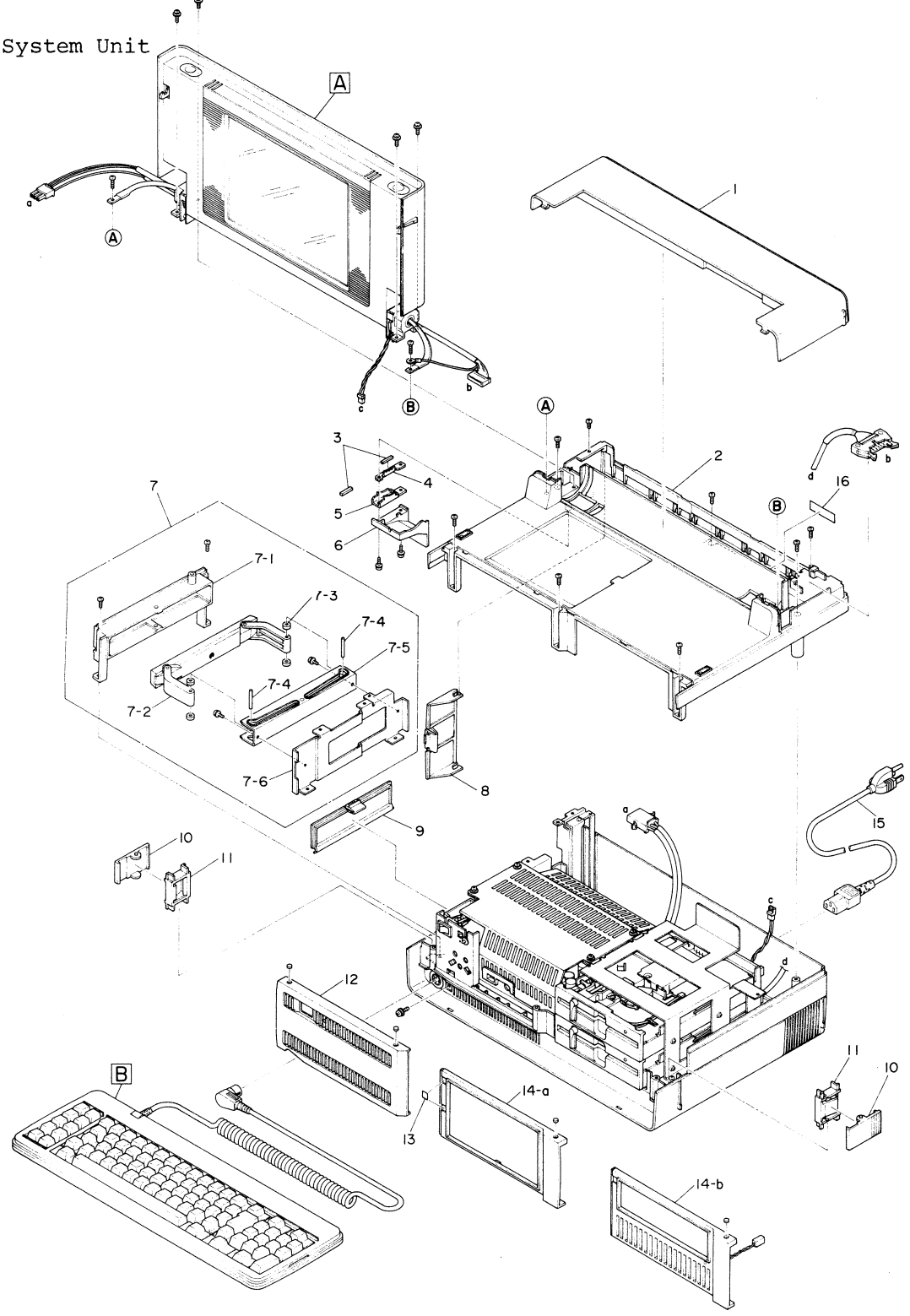
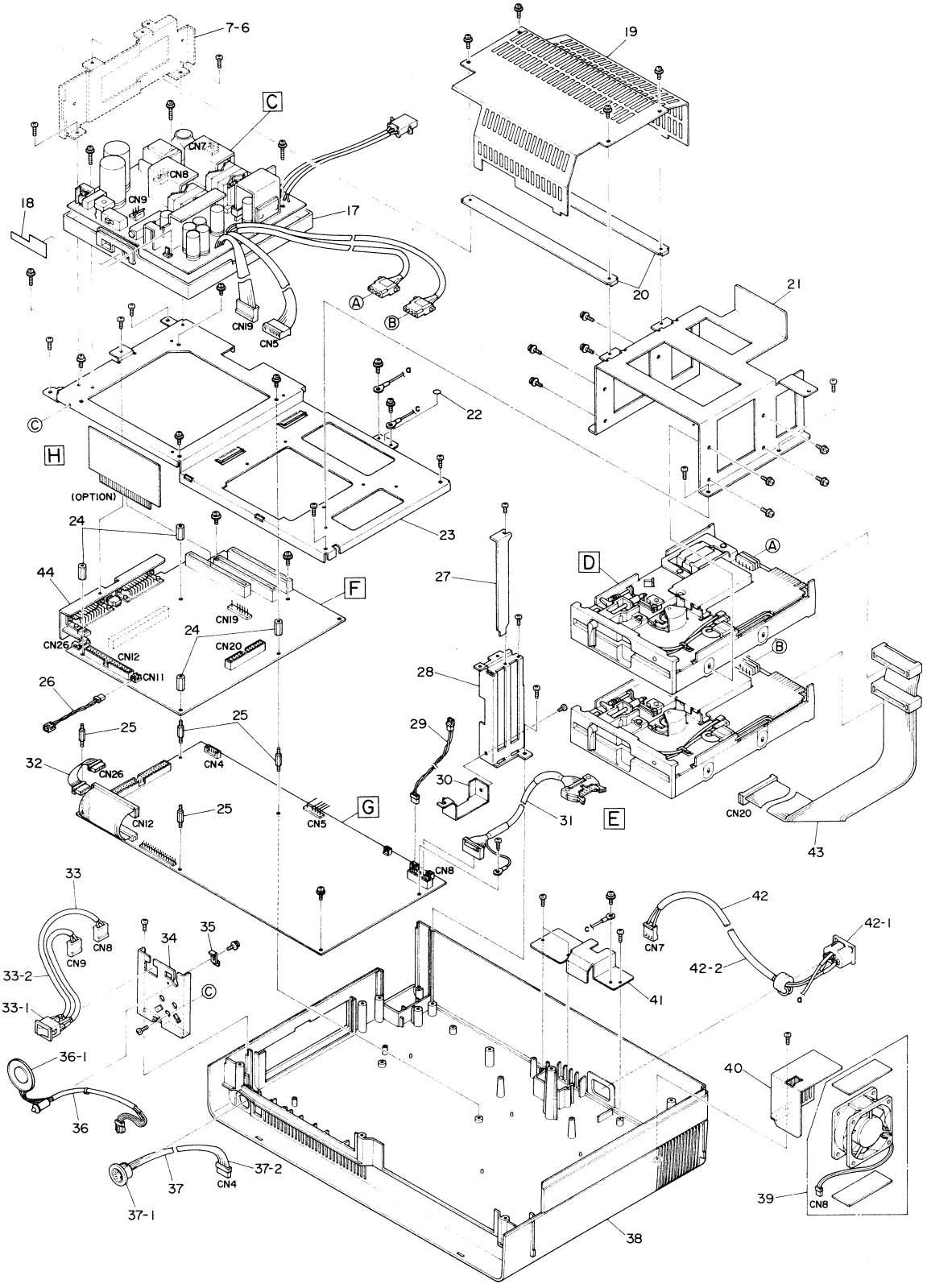


Figure 6-1 Exproded View


7-6
19
C
CN7
CN8
CN9
18
17
20
21
CN19
CN5
A
B
22
H
(OPTION)
23
24
44
F
CN19
CN26
CN12
CN11
CN20
27
D
28
29
26
25
32
CN4
CN5
G
30
31
E
CN20
43
33
CN8
CN9
33-2
33-1
34
35
42
CN7
42-1
42-2
41
36-1
36
37
37-1
CN4
37-2
38
40
39
CN8

7. WIRING CONNECTION

7.1 JB-3301

PLSMX CN2 • PLSY CN21

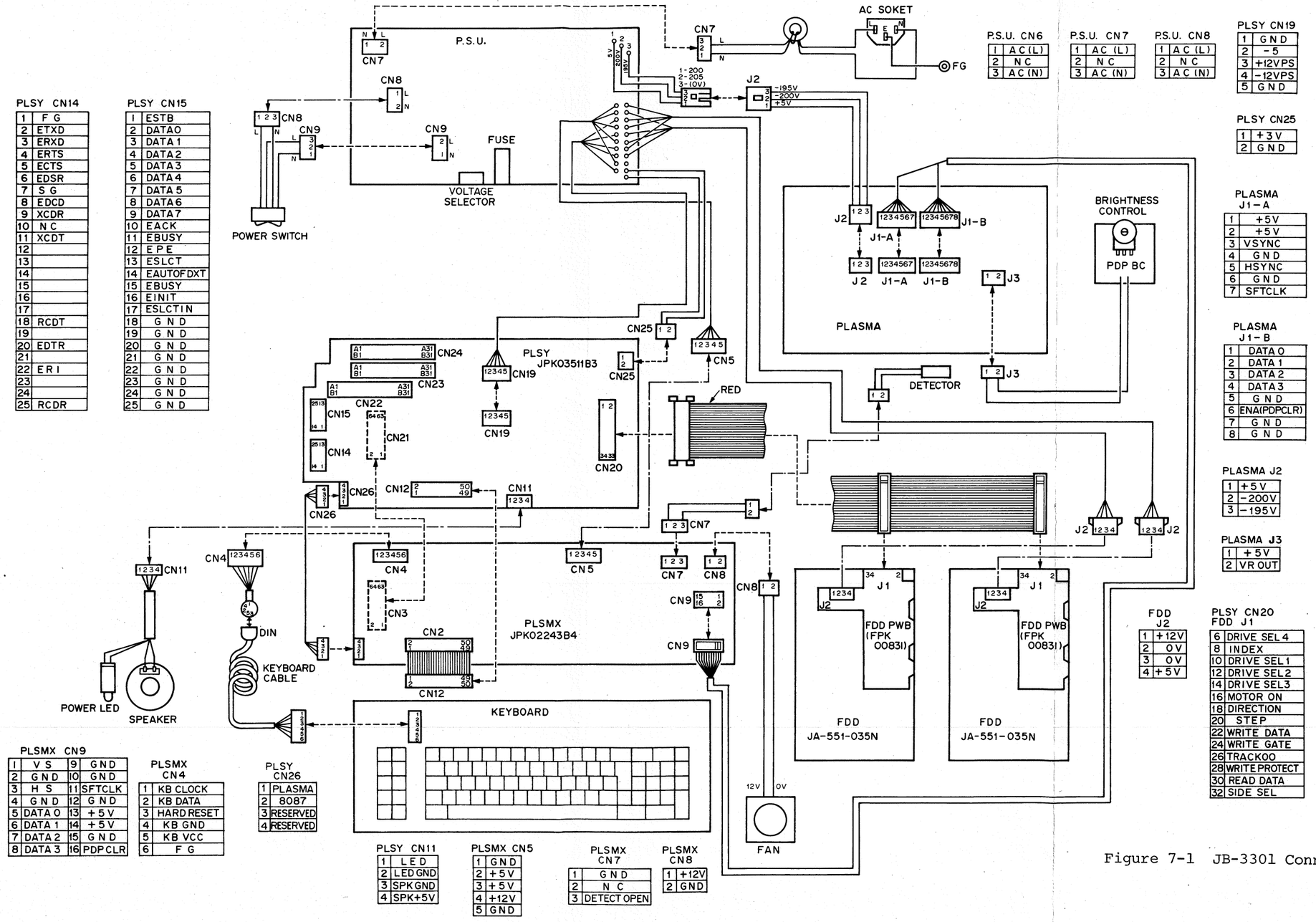
1	IOCHCK	33	AB 14
2	GND	34	DACK1
3	DB 7	35	AB 13
4	RESET	36	DREQ1
5	DB 6	37	AB 12
6	+5V	38	DACK0
7	DB 5	39	AB 11
8	IRQ2	40	CLK
9	DB 4	41	AB 10
10		42	IRQ7
11	DB 3	43	AB 9
12		44	IRQ6
13	DB 2	45	AB 8
14	INTIO	46	IRQ5
15	DB11	47	AB 7
16	EXPDCS	48	IRQ4
17	DB 0	49	AB 6
18	RAMASEL	50	IRQ3
19	IOCHRDY	51	AB 5
20	GND	52	DACK3
21	AEN	53	AB 4
22	MEMW	54	TC
23	AB19	55	AB 3
24	MEMR	56	ALE
25	AB18	57	AB 2
26	IOW	58	+5V
27	AB17	59	AB 1
28	IOR	60	VRAMSEL
29	AB16	61	AB 0
30	DACK3	62	GND
31	AB15	63	ROMS
32	DREQ3	64	RDKSEL

PLSY CN22 ~ CN24

A01	IOCHCK	B01	GND
A02	EDB 7	B02	RESET
A03	EDB 6	B03	+5V
A04	EDB 5	B04	IRQ2
A05	EDB 4	B05	-5V
A06	EDB 3	B06	DREQ2
A07	EDB 2	B07	-2V
A08	EDB 1	B08	
A09	EDB 0	B09	+12V
A10	IOCHRDY	B10	GND
A11	EAEN	B11	EMEMW
A12	EAB19	B12	EMEMR
A13	EAB18	B13	EIOW
A14	EAB17	B14	EIOR
A15	EAB16	B15	EDACK3
A16	EAB15	B16	DREQ3
A17	EAB14	B17	EDACK1
A18	EAB13	B18	DREQ1
A19	EAB12	B19	EDACK0
A20	EAB11	B20	ECLK
A21	EAB10	B21	IRQ7
A22	EAB 9	B22	IRQ6
A23	EAB 8	B23	IRQ5
A24	EAB 7	B24	IRQ4
A25	EAB 6	B25	IRQ3
A26	EAB 5	B26	EDACK2
A27	EAB 4	B27	ETC
A28	EAB 3	B28	EALE
A29	EAB 2	B29	+5V
A30	EAB 1	B30	EOSC
A31	EAB 0	B31	GND

PLSMX CN2 • PLSY CN12

1	+5V	26	XAB3
2	+5V	27	XAB2
3	DB7	28	XAB1
4	RESET	29	XAB0
5	DB6	30	XIOW
6	+5V	31	XIOR
7	DB5	32	RESET
8	GND	33	DACKZ
9	DB4	34	FDDCS
10	GND	35	FDCCS
11	DB3	36	PSCCS
12	DREQZ	37	PRTCS
13	DB2	38	CALDCS
14	GND	39	PCLK
15	DB1	40	RSCLK
16	GND	41	TC
17	DB0	42	IRQ4
18	DO7	43	IRQ6
19	DO6	44	IRQ7
20	DO5	45	POR
21	DO4	46	GND
22	DO3	47	GND
23	DO2	48	GND
24	DO1	49	SPK
25	DO0	50	SECOND DRIVE



PLSY CN14

1	F G
2	ETXD
3	ERXD
4	ERTS
5	ECTS
6	EDSR
7	S G
8	EDCD
9	XCDR
10	N C
11	XCDT
12	
13	
14	
15	
16	
17	
18	RCDT
19	
20	EDTR
21	
22	ERI
23	
24	
25	RCDR

PLSY CN15

1	ESTB
2	DATA0
3	DATA1
4	DATA2
5	DATA3
6	DATA4
7	DATA5
8	DATA6
9	DATA7
10	EACK
11	EBUSY
12	EPE
13	ESLCT
14	EAUTOFDXT
15	EBUSY
16	EINIT
17	ESLCTIN
18	G N D
19	G N D
20	G N D
21	G N D
22	G N D
23	G N D
24	G N D
25	G N D

P.S.U. CN6

1	AC(L)
2	NC
3	AC(N)

P.S.U. CN7

1	AC (L)
2	NC
3	AC (N)

P.S.U. CN8

1	AC (L)
2	NC
3	AC (N)

PLSY CN19

1	GND
2	-5
3	+12VPS
4	-12VPS
5	GND

PLSY CN25

1	+3V
2	GND

PLASMA J1-A

1	+5V
2	+5V
3	VSYNC
4	GND
5	HSYNC
6	GND
7	SFTCLK

PLASMA J1-B

1	DATA0
2	DATA1
3	DATA2
4	DATA3
5	GND
6	ENA(PDPCLR)
7	GND
8	GND

PLASMA J2

1	+5V
2	-200V
3	-195V

PLASMA J3

1	+5V
2	VR OUT

FDD J2

1	+12V
2	0V
3	0V
4	+5V

PLSY CN20 FDD J1

6	DRIVE SEL4
8	INDEX
10	DRIVE SEL1
12	DRIVE SEL2
14	DRIVE SEL3
16	MOTOR ON
18	DIRECTION
20	STEP
22	WRITE DATA
24	WRITE GATE
26	TRACK00
28	WRITE PROTECT
30	READ DATA
32	SIDE SEL

PLSMX CN9

1	V S	9	GND
2	GND	10	GND
3	H S	11	SFTCLK
4	GND	12	GND
5	DATA 0	13	+5V
6	DATA 1	14	+5V
7	DATA 2	15	GND
8	DATA 3	16	PDPCLR

PLSMX CN4

1	KB CLOCK
2	KB DATA
3	HARD RESET
4	KB GND
5	KB VCC
6	F G

PLSY CN26

1	PLASMA
2	8087
3	RESERVED
4	RESERVED

PLSY CN11

1	LED
2	LED GND
3	SPK GND
4	SPK+5V

PLSMX CN5

1	GND
2	+5V
3	+5V
4	+12V
5	GND

PLSMX CN7

1	GND
2	NC
3	DETECT OPEN

PLSMX CN8

1	+12V
2	GND

Figure 7-1 JB-3301 Connection Diagram

7.2 JB-3305

HDC CN1 HDD CN1

1	G N D
2	SPARE
3	G N D
4	SPARE
5	G N D
6	WRITEGATE
7	G N D
8	SEEKCOMPLETE
9	G N D
10	TRACK 00
11	G N D
12	WRITE FAULT
13	G N D
14	-HEAD SELECTO
15	G N D
16	RESERVED
17	G N D
18	-HEAD SELECT 1
19	G N D
20	INDEX
21	G N D
22	-READY
23	G N D
24	-STEP
25	G N D
26	-DRIVE SELECT
27	G N D
28	-DRIVE SELECT 2
29	G N D
30	-DRIVE SELECT 3
31	G N D
32	-DRIVE SELECT 4
33	G N D
34	-DIRECTION IN

HDC CN2 HDDJ2

1	-DRIVE SELECT
2	G N D
3	
4	G N D
5	N C
6	G N D
7	RESERVED
8	G N D
9	N C
10	G N D
11	G N D
12	G N D
13	WRITE DATA
14	WRITE DATA
15	G N D
16	G N D
17	READ DATA
18	READ DATA
19	G N D
20	G N D

PLSMX CN2 • PLSY CN12

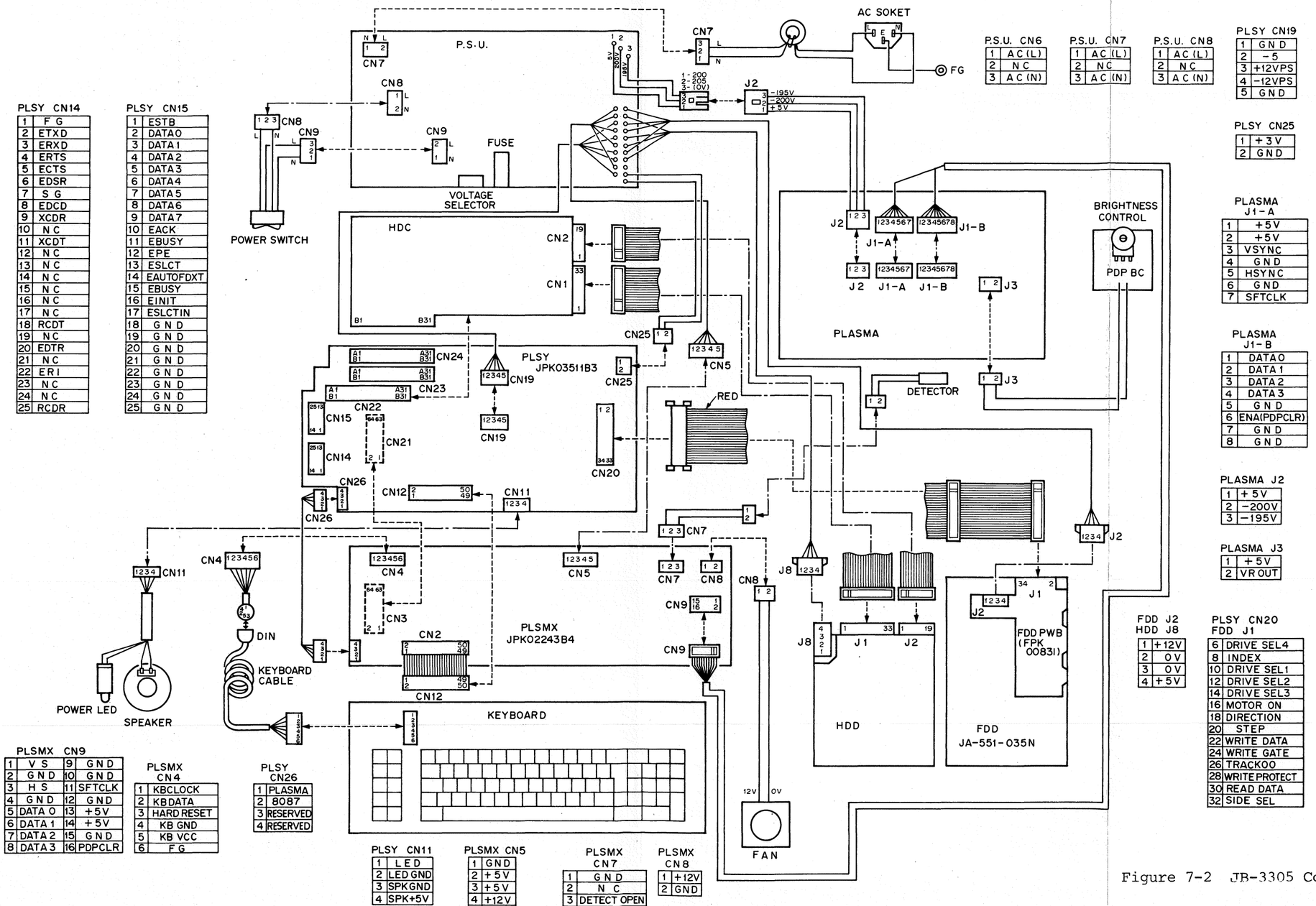
1	+5V	26	XAB3
2	+5V	27	XAB2
3	DB7	28	XAB1
4	RESET	29	XAB0
5	DB6	30	X IOW
6	+5V	31	X IOR
7	DB5	32	RESET
8	GND	33	DACKZ
9	DB4	34	FDDCS
10	GND	35	FDCCS
11	DB3	36	PSCCS
12	DREQZ	37	PRTCS
13	DB2	38	CALDCS
14	G N D	39	PCLK
15	DB1	40	RSCLK
16	G N D	41	TC
17	DB0	42	IRQ4
18	D07	43	IRQ6
19	D06	44	IRQ7
20	D05	45	POR
21	D04	46	GND
22	D03	47	GND
23	D02	48	GND
24	D01	49	SPK
25	D00	50	SECOND DRIVE

PLSMX CN2 • PLSY CN21

1	IOCHCK	33	AB14
2	GND	34	DACK1
3	DB7	35	AB13
4	RESET	36	DREQ1
5	DB6	37	AB12
6	+5V	38	DACK0
7	DB5	39	AB11
8	IRQ2	40	CLK
9	DB4	41	AB10
10		42	IRQ7
11	DB3	43	AB9
12		44	IRQ6
13	DB2	45	AB8
14	INTIO	46	IRQ5
15	DB1	47	AB7
16	EXPDCS	48	IRQ4
17	DB0	49	AB6
18	RAMASEL	50	IRQ3
19	IOCHRDY	51	AB5
20	GND	52	DACK3
21	AEN	53	AB4
22	MEMW	54	TC
23	AB19	55	AB3
24	MEMR	56	ALE
25	AB18	57	AB2
26	IOW	58	+5V
27	AB17	59	AB1
28	IOR	60	VRAMSEL
29	AB16	61	AB0
30	DACK3	62	GND
31	AB15	63	ROMS
32	DREQ3	64	RDKSEL

PLSY CN22 ~ CN24

A01	IOCHCK	B01	G N D
A02	EDB7	B02	RESET
A03	EDB6	B03	+5V
A04	EDB5	B04	IRQ2
A05	EDB4	B05	-5V
A06	EDB3	B06	DREQ2
A07	EDB2	B07	-12V
A08	EDB1	B08	
A09	EDB0	B07	+12V
A10	IOCHRDY	B10	G N D
A11	EAEN	B11	EMEMW
A12	EAB19	B12	EMEMR
A13	EAB18	B13	EIOW
A14	EAB17	B14	EIOR
A15	EAB16	B15	EDACK3
A16	EAB15	B16	DREQ3
A17	EAB14	B17	EDACK1
A18	EAB13	B18	DREQ1
A19	EAB12	B19	EDACK0
A20	EAB11	B20	ECLK
A21	EAB10	B21	IRQ7
A22	EAB9	B22	IRQ6
A23	EAB8	B23	IRQ5
A24	EAB7	B24	IRQ4
A25	EAB6	B25	IRQ3
A26	EAB5	B26	EDACK2
A27	EAB4	B27	ETC
A28	EAB3	B28	EALE
A29	EAB2	B29	+5V
A30	EAB1	B30	EOSC
A31	EAB0	B31	GND



PLSY CN14

1	F G
2	ETXD
3	ERXD
4	ERTS
5	ECTS
6	EDSR
7	S G
8	EDCD
9	XCDR
10	N C
11	XCDT
12	N C
13	N C
14	N C
15	N C
16	N C
17	N C
18	RCDT
19	NC
20	EDTR
21	NC
22	ERI
23	NC
24	NC
25	RCDR

PLSY CN15

1	ESTB
2	DATAO
3	DATA1
4	DATA2
5	DATA3
6	DATA4
7	DATA5
8	DATA6
9	DATA7
10	EACK
11	EBUSY
12	EPE
13	ESLCT
14	EAUTOFDXT
15	EBUSY
16	EINIT
17	ESLCTIN
18	G N D
19	G N D
20	G N D
21	G N D
22	G N D
23	G N D
24	G N D
25	G N D

P.S.U. CN6

1	AC(L)
2	N C
3	AC(N)

P.S.U. CN7

1	AC(L)
2	NC
3	AC(N)

P.S.U. CN8

1	AC(L)
2	NC
3	AC(N)

PLSY CN19

1	GND
2	-5
3	+12VPS
4	-12VPS
5	GND

PLSY CN25

1	+3V
2	GND

PLASMA J1-A

1	+5V
2	+5V
3	VSYNC
4	GND
5	HSYNC
6	GND
7	SFTCLK

PLASMA J1-B

1	DATAO
2	DATA1
3	DATA2
4	DATA3
5	GND
6	ENA(PDPCLR)
7	GND
8	GND

PLASMA J2

1	+5V
2	-200V
3	-195V

PLASMA J3

1	+5V
2	VR OUT

FDD J2
HDD J8

1	+12V
2	0V
3	0V
4	+5V

PLSY CN20
FDD J1

6	DRIVE SEL4
8	INDEX
10	DRIVE SEL1
12	DRIVE SEL2
14	DRIVE SEL3
16	MOTOR ON
18	DIRECTION
20	STEP
22	WRITE DATA
24	WRITE GATE
26	TRACK00
28	WRITE PROTECT
30	READ DATA
32	SIDE SEL

PLSMX CN9

1	V S	9	G N D
2	G N D	10	G N D
3	H S	11	SFTCLK
4	G N D	12	G N D
5	DATA 0	13	+5V
6	DATA 1	14	+5V
7	DATA 2	15	G N D
8	DATA 3	16	PDPCLR

PLSMX CN4

1	KBCLOCK
2	KBDATA
3	HARD RESET
4	KB GND
5	KB VCC
6	F G

PLSY CN26

1	PLASMA
2	8087
3	RESERVED
4	RESERVED

PLSY CN11

1	LED
2	LED GND
3	SPKGND
4	SPK+5V

PLSMX CN5

1	GND
2	+5V
3	+5V
4	+12V
5	GND

PLSMX CN7

1	G N D
2	N C
3	DETECT OPEN

PLSMX CN8

1	+12V
2	GND

Figure 7-2 JB-3305 Connection Diagram

REPLACEMENT PARTS LIST (Logic Unit)

NOTE:
- **When ordering replacement parts indicate Part No. and Name of Parts.**
- **⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.**

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
1		YJJ5E08450D1	Rear Cover	1	
2		YJJUE04020B1	Upper Case Ass'y	1	
3		YJJXG01171B4	Magnet	2	
4		YJJ4E01200B4	Gear	1	
5		YJJ2X08761B4	Gear Cover	1	
6		YJJ5E09170B3	Gear Cover (2)	1	
7		YJJ4034990A4	Handle UNIT	1	
7-1		YJJ5K08680B1	Handle Case	(1)	
7-2		YJJUX03790B4	Handle Sub Ass'y	(1)	
7-3		YJ80B-0404	Pin Bush	(4)	
7-4		YJJ1H00870B4	Handle Pin (2)	(2)	
7-5		YJJ2E09151B3	Pin Guide Plate	(1)	
7-6		YJJ2T09171B2	Support Plate	(1)	
8		YJJ5W08530B3	Option CN Door	1	
9		YJJ5W08540B3	PR. CN. Door	1	
10		YJJ6D08490B3	K/B Hook	2	
11		YJJ4J01220B3	K/B Look Spring	2	
12		YJJUJ03360B2	Front Panel (L)	1	
13		YJJ7S12670B4	FD. NO. Sheel	1	
14a		YJJ5W09610B1	Front Panel (FDD)	1	
14b		YJJ5W09720B1	Front Panel (FHD)	1	
15		YJJDA01140B4	Ac Cord	1	
16		YJJ7Q02050B4	Caution Lever	1	
17		YJJ2P09111B2	Insulation Case	1	
18		YJJ7T11870B4	Lavel	1	
19		YJJ2H09101B2	PSU Shield Plate	1	
20		YJJ3B09120B3	Roinforcement Plate	1	
21		YJJ2S09090B2	Support Plate	1	
22		YJJ7T05950B4	Earth Lavel	1	
23		YJJ2T09201B1	Base Plate	1	
24		YJJ2J09190B4	Plate Support	4	
25		YJJ2J10040B4	PCB Support	4	
26		YJJDK02860B4	LED-SP Sub Cable	1	
27		YJJ6G09620B4	Masking Plate	2	
28		YJJ2T09141B3	Option CN Holder	1	
29		YJJDK02600B4	Detector Sub Cable	1	
30		YJJ6G09890B4	S.E. Plate	1	
31		YJJDK02521B3	Plasma Display Sub Cable	1	
32		YJJDK02870B4	X-Y SW Cable	1	
33		YJJ4034920A4	AC SW UNIT	1	
33-1		YJJWC00330B4	AC Switch	(1)	
33-2		YJJDK02840B4	SW Cable (1)	(1)	
33-3		YJJDK02851B4	SW Cable (2)	(1)	
34		YJJ2T09230B4	SW Holder	1	
35		YJJ2T10140B4	Speaker Holder	1	
36		YJJ4034940A4	LED-SP UNIT	1	
36-1		EAS-3P108S	Speaker	(1)	
36-2		YJJDK02540B4	Power Indicator Cable	(1)	
37		YJJ4034910A4	Keyboard Cable Ass'y	1	
37-1		YJJJC00630B4	Connector	(1)	
37-2		YJJDK02530B4	K/B Cable	(1)	
38		YJJUF03350B1	Bottom Case Ass'y	1	
38-1		YJJ2T10170B4	HDC Holder	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
39		YJJ7E12631B4	Fan	1	
39-1		YJJ2F09210B4	Fan Cussion	2	
40		YJJ2C09130B3	Hold Plate	1	
41		YJJ2C09180B3	Inlet Cover	1	
42		YJJ4037120A4	Inlet Unit	1	
42-1		YJJZZ00090B4	Inlet	(1)	
42-2		YJJDK02830B4	Inlet Cable	(1)	
42-3		YJESDR-19	Ferrite Core	(1)	
43		YJJDK02611B4	FDD Signal Cable	1	
44		YJJ6G08691D3	PR:CN Plate	1	(PLSY)
45		YJJ7T13280B4	Main Lavel	1	
A		YJJ2006590A4	Plasma Display Unit	1	
B		YJJ2007100A4	Keyboard Unit (G)	1	
		YJJ2006600A4	(SW, Fin)	1	
		YJJ2007130A4	(UK)	1	
		YJJ2007140A4	(F)	1	
		YJJ2007150A4	(NE, HK, FA, AU)	1	
C		YJJUS03280B4	Power Supply Unit	1	
D		YJJA-551-035	Floppy Disk Drive	1	
E		YJJU-104	Hard Disk Drive	1	
F		YJJ4039430A4	PLSY P.C.B. Ass'y	1	
G		YJJ3006420A4	PLSMX P.C.B. Ass'y	1	
H		YJNDC-5027M	Hard Disk Controller	1	
15		YJJDA02160B4	AC Cord (UK, H.K, AF)	1	
15		YJJDA00160B4	AC Cord (AU)	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks

9. TROUBLESHOOTING

9.1 Preface

This chapter describes how to shoot, analyze, and correct failures on the system.

Use the Troubleshooting Hints as an aid to analyze failure. It is recommendable to analyze the error event, environment, and peripheral circuits during troubleshooting.

When a failure occurs on the power supply unit (PSU), the whole power supply unit must be replaced by a new one (except a blown-fuse failure). (The defective power supply unit must be sent back to our factory.)

WARNING:

This computer uses some special parts for safety and protection. They are marked by the international safety mark ⚠ in drawings and replacement parts lists. Always use Matsushita's parts to avoid unpredictable damages (X-ray exposure, electrical shock, burning, etc.).

Note: The diagnostic program consists of several units. Diagnose each unit successfully and efficiently by using these diagnostic program units.

Grasp and record the failure event correctly.

Write down the condition the defective unit, and report it after repairing the unit.

9.2 Tools for Troubleshooting

Oscilloscope (50 MHz or more)	1 unit
RS-232C loop back plug	1 piece
Floppy disks	3 or more
o Diagnostic program disk	1
o Read/Write check disks (Scratch disks)	2 or more

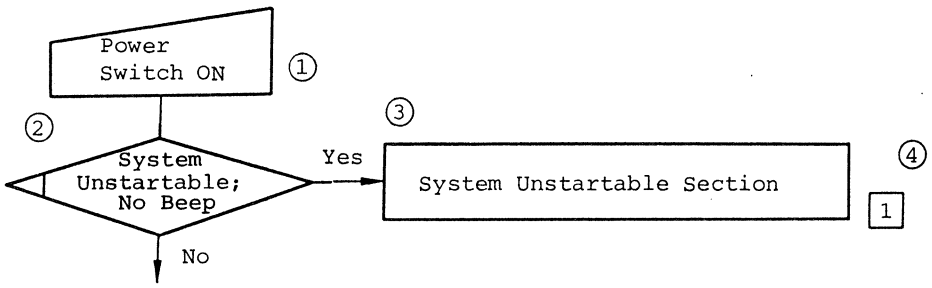
Note: The plug for a loop back test must be wired as follows:
(Panasonic Part No. RHC-515)
Connect Pin 2 and Pin 3
Connect Pin 4, Pin 5 and Pin 8
Connect Pin 6, Pin 20 and Pin 22

Note: A scratch disk is a blank disk or one that doesn't contain any files that you will need. It must be formatted for DOS.

9.3 How to Use Troubleshooting Hints

Before using the troubleshooting hints, see the following and learn how to read it.

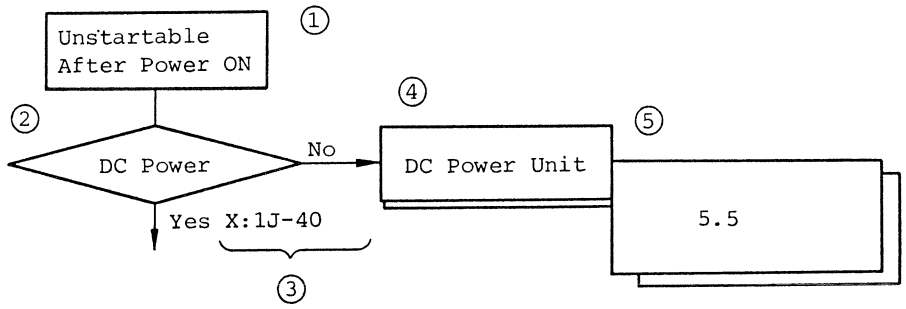
o Main flow chart



① Operation for troubleshooting
② Visual check item
③ Troubleshooting section
④ Reference troubleshooting block

Figure 9-1

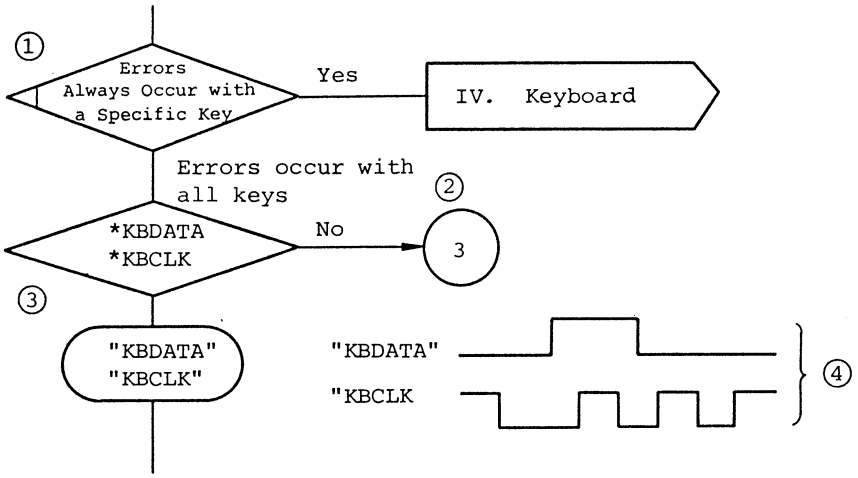
o Block flow chart No.1



① Section or block item
② Measurement or signal name
③ Check pin name or IC pin number (X/Y: PLSMX/PLSY)
④ Possible error unit
⑤ Reference explanation, drawing, table, and timing chart (These are listed in that sequence (in sections).)

Figure 9-2

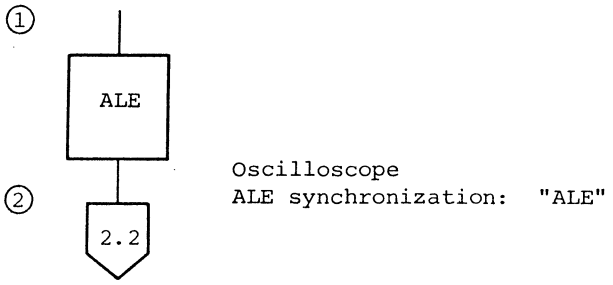
o Block flow chart No.2



① Visual check item
② Connector
③ Typical waveforms to be measured
④ Waveform diagram or condition
⑤ Possible error part or block

Figure 9-3

o Block flow chart No.3



① Preparation item
② Connector to the other page (2.2 is an item number.)

Figure 9-4

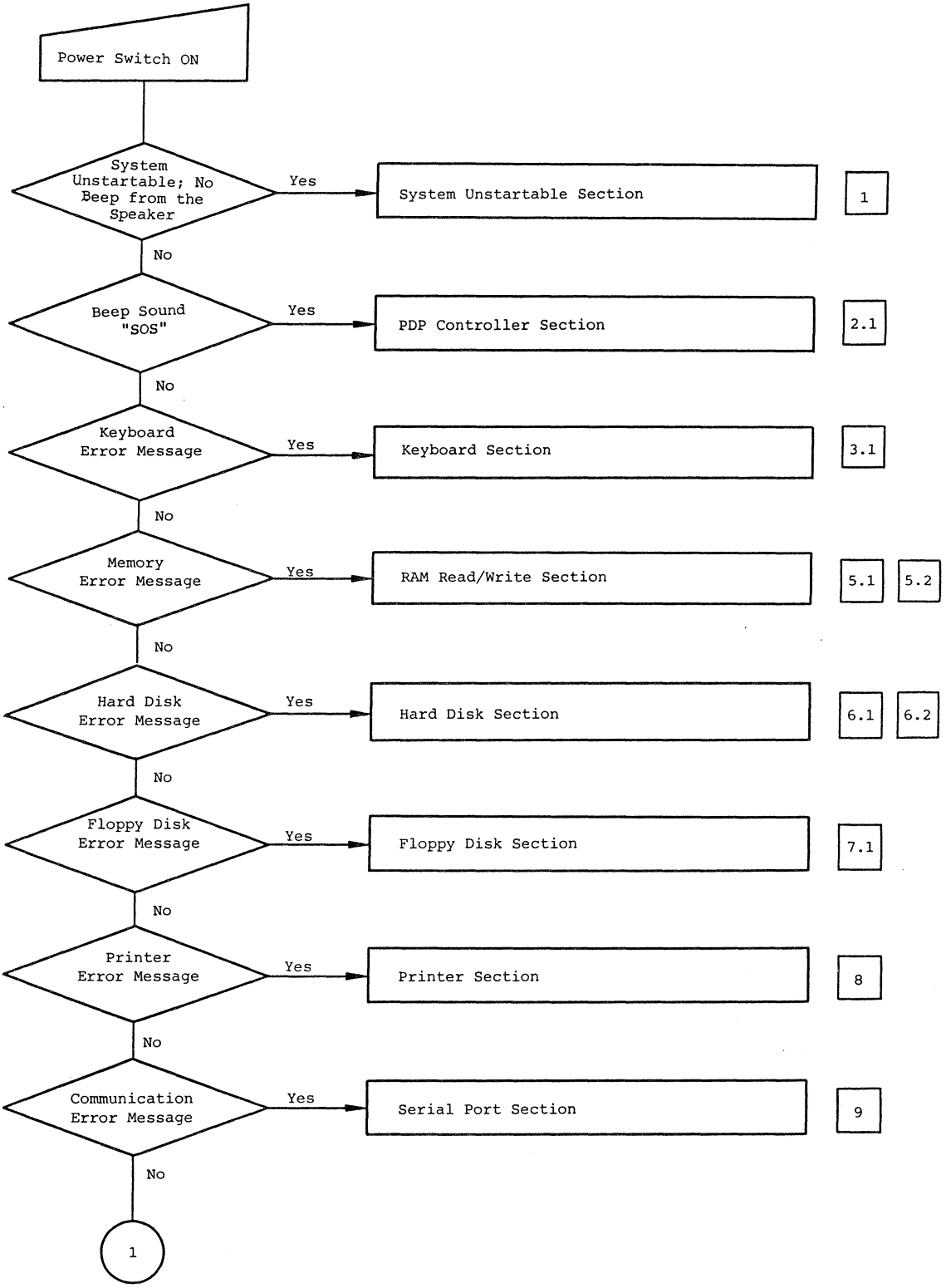

Power Switch ON
System Unstartable; No Beep from the Speaker
Yes
System Unstartable Section
1
No
Beep Sound "SOS"
Yes
PDP Controller Section
2.1
No
Keyboard Error Message
Yes
Keyboard Section
3.1
No
Memory Error Message
Yes
RAM Read/Write Section
5.1
5.2
No
Hard Disk Error Message
Yes
Hard Disk Section
6.1
6.2
No
Floppy Disk Error Message
Yes
Floppy Disk Section
7.1
No
Printer Error Message
Yes
Printer Section
8
No
Communication Error Message
Yes
Serial Port Section
9
No
1

Figure 9-5 (1/2)

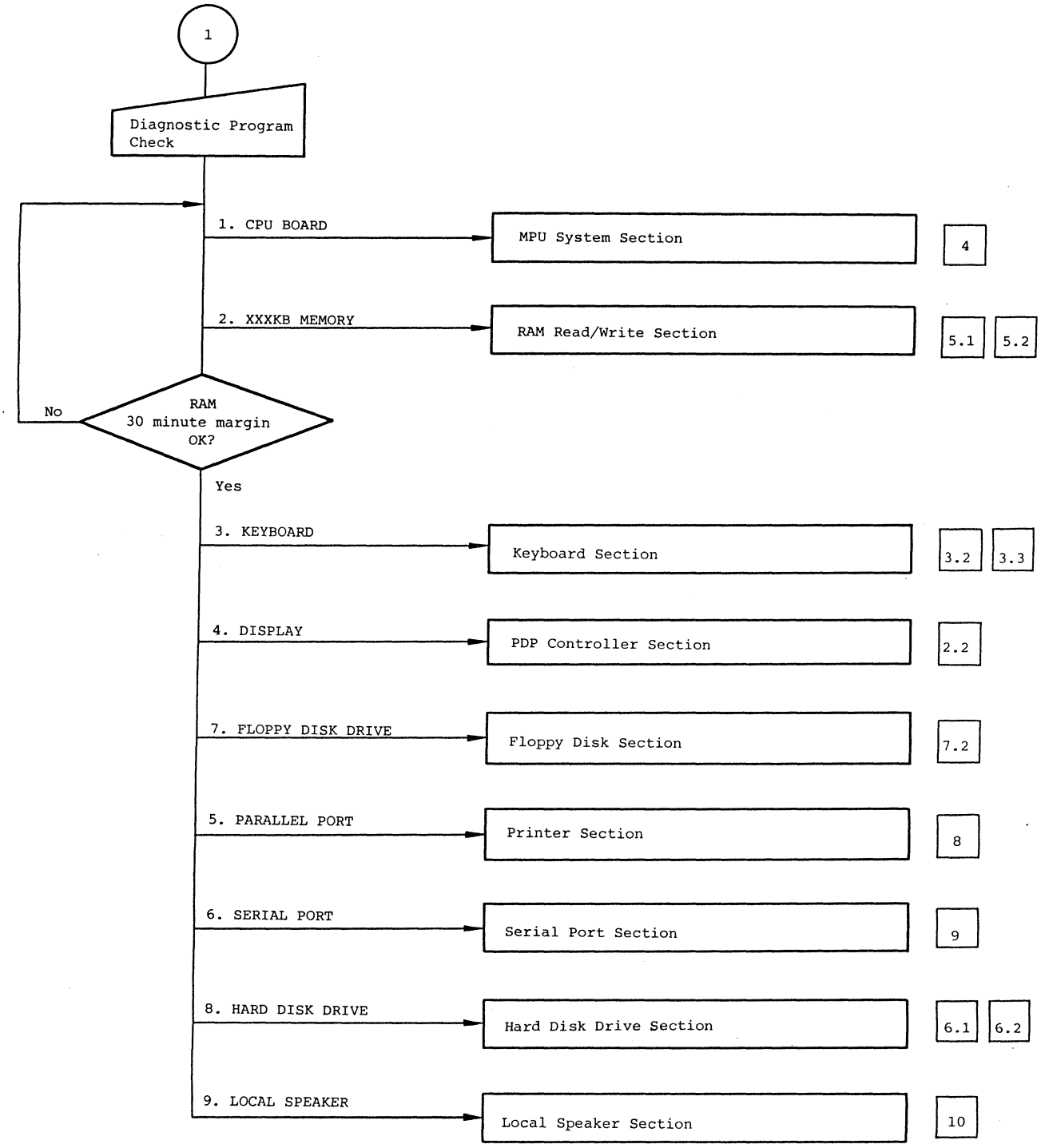

1
Diagnostic Program Check
1. CPU BOARD
MPU System Section
4
2. XXXKB MEMORY
RAM Read/Write Section
5.1
5.2
No
RAM 30 minute margin OK?
Yes
3. KEYBOARD
Keyboard Section
3.2
3.3
4. DISPLAY
PDP Controller Section
2.2
7. FLOPPY DISK DRIVE
Floppy Disk Section
7.2
5. PARALLEL PORT
Printer Section
8
6. SERIAL PORT
Serial Port Section
9
8. HARD DISK DRIVE
Hard Disk Drive Section
6.1
6.2
9. LOCAL SPEAKER
Local Speaker Section
10

Figure 9-5 (2/2)

[1] System Unstartable Section

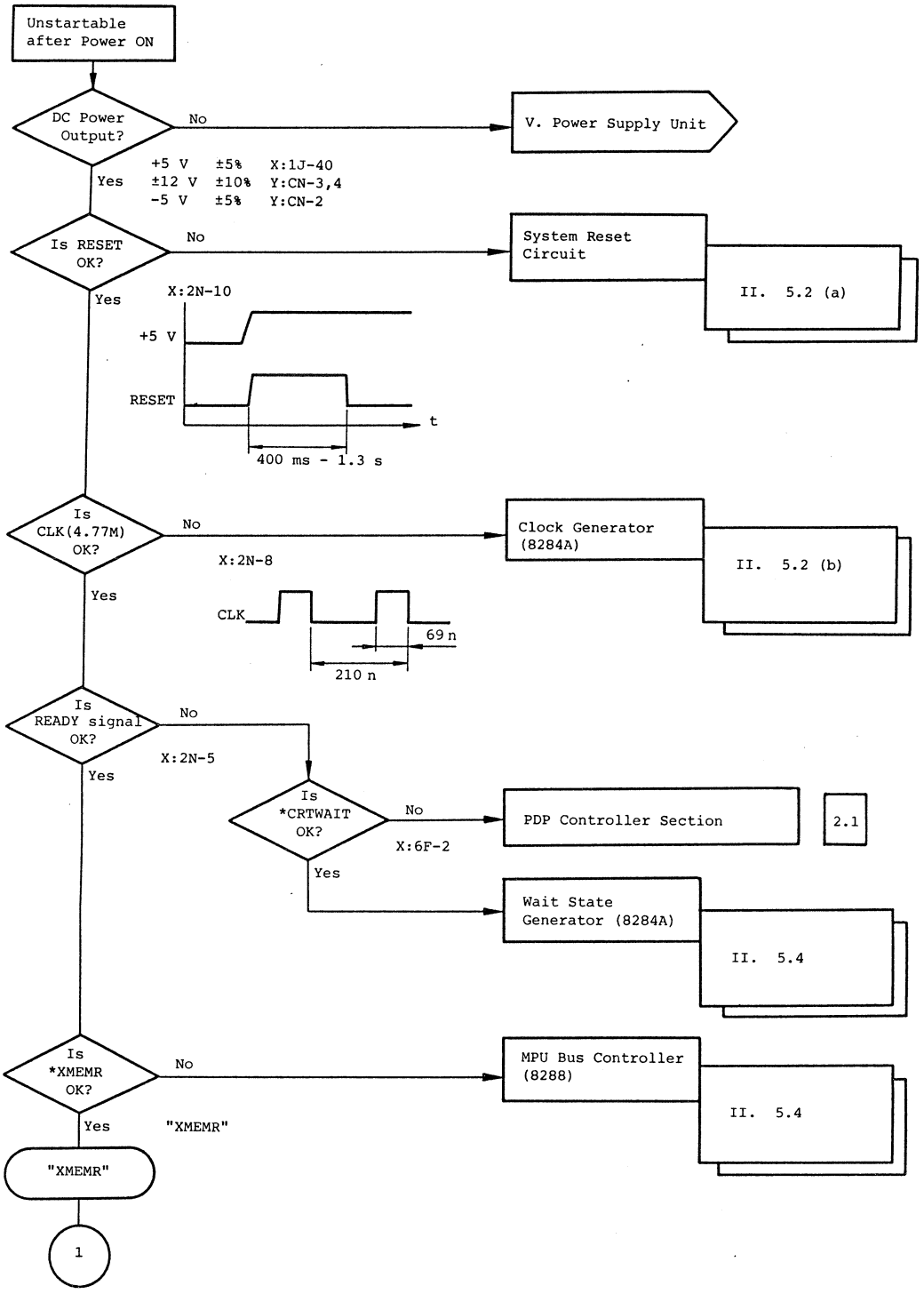


Figure 9-6 (1/2)

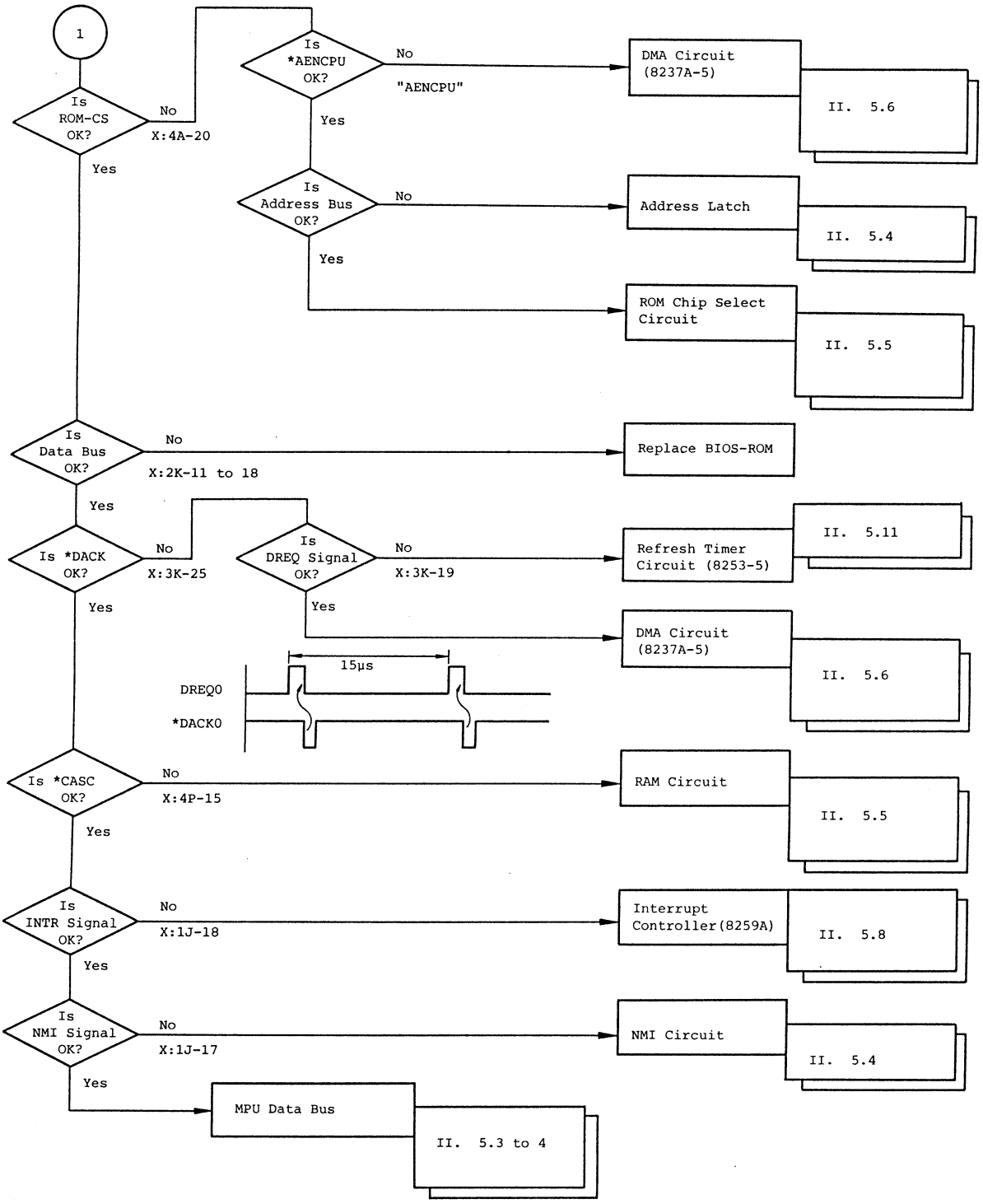

1
Is ROM-CS OK?
No
X:4A-20
Yes
Is *AENCPU OK?
No
"AENCPU"
DMA Circuit (8237A-5)
II. 5.6
Yes
Is Address Bus OK?
No
Address Latch
II. 5.4
Yes
ROM Chip Select Circuit
II. 5.5
Is Data Bus OK?
No
X:2K-11 to 18
Replace BIOS-ROM
Yes
Is *DACK OK?
No
X:3K-25
Is DREQ Signal OK?
No
X:3K-19
Refresh Timer Circuit (8253-5)
II. 5.11
Yes
Yes
DMA Circuit (8237A-5)
II. 5.6
15µs
DREQ0
*DACK0
Is *CASC OK?
No
X:4P-15
RAM Circuit
II. 5.5
Yes
Is INTR Signal OK?
No
X:1J-18
Interrupt Controller(8259A)
II. 5.8
Yes
Is NMI Signal OK?
No
X:1J-17
NMI Circuit
II. 5.4
Yes
MPU Data Bus
II. 5.3 to 4

Figure 9-6 (2/2)

[2] PDP Controller Section

[2.1] Power on Self-Diagnosis Error

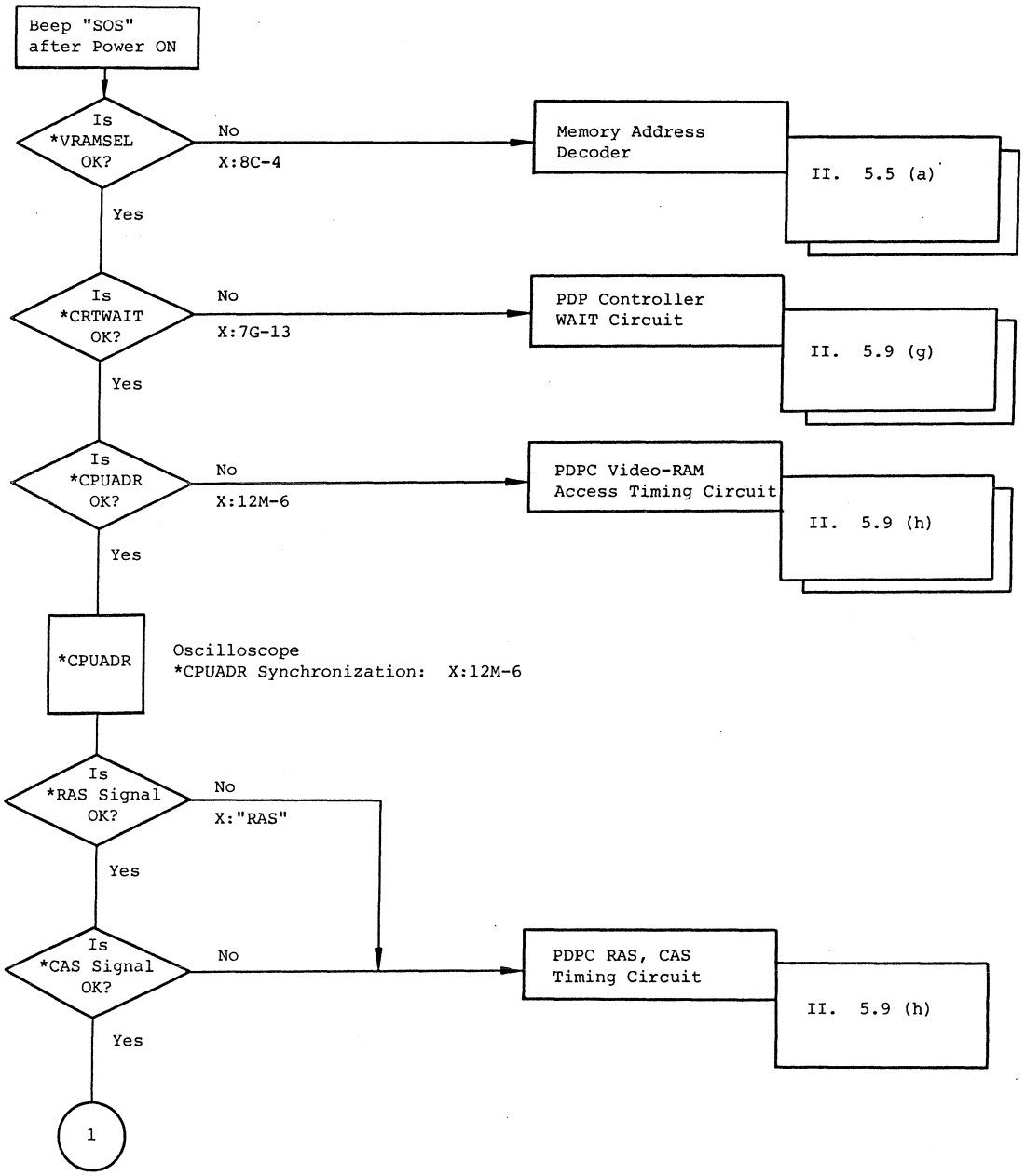


Figure 9-7 (1/2)

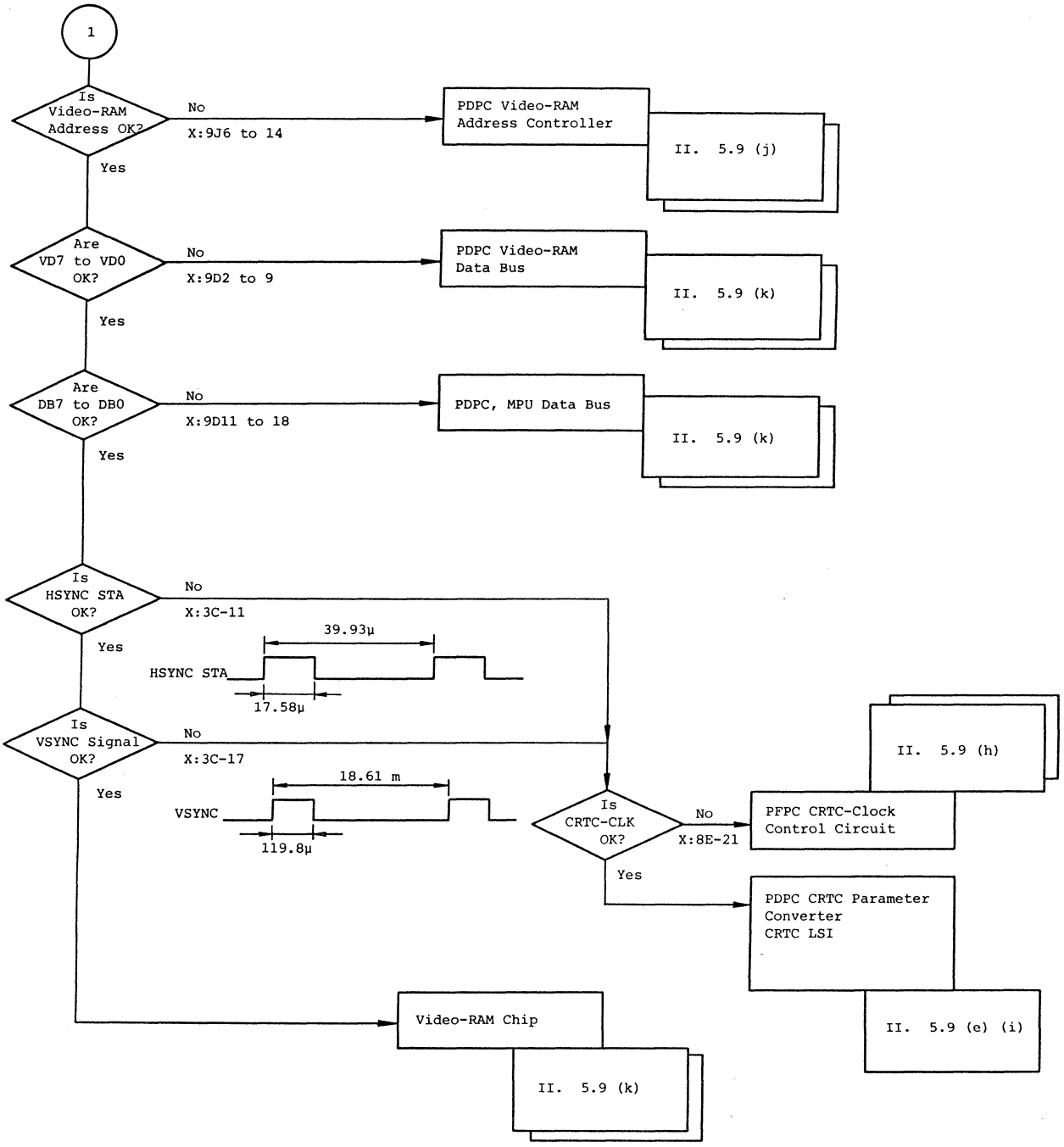

1
Is Video-RAM Address OK?
No
X:9J6 to 14
PDPC Video-RAM Address Controller
II. 5.9 (j)
Yes
Are VD7 to VD0 OK?
No
X:9D2 to 9
PDPC Video-RAM Data Bus
II. 5.9 (k)
Yes
Are DB7 to DB0 OK?
No
X:9D11 to 18
PDPC, MPU Data Bus
II. 5.9 (k)
Yes
Is HSYNC STA OK?
No
X:3C-11
39.93µ
HSYNC STA
17.58µ
Yes
Is VSYNC Signal OK?
No
X:3C-17
18.61 m
VSYNC
119.8µ
Yes
Is CRTC-CLK OK?
No
X:8E-21
II. 5.9 (h)
PFPC CRTC-Clock Control Circuit
Yes
PDPC CRTC Parameter Converter CRTC LSI
II. 5.9 (e) (i)
Video-RAM Chip
II. 5.9 (k)

Figure 9-7 (2/2)

[2.2] Black Indication

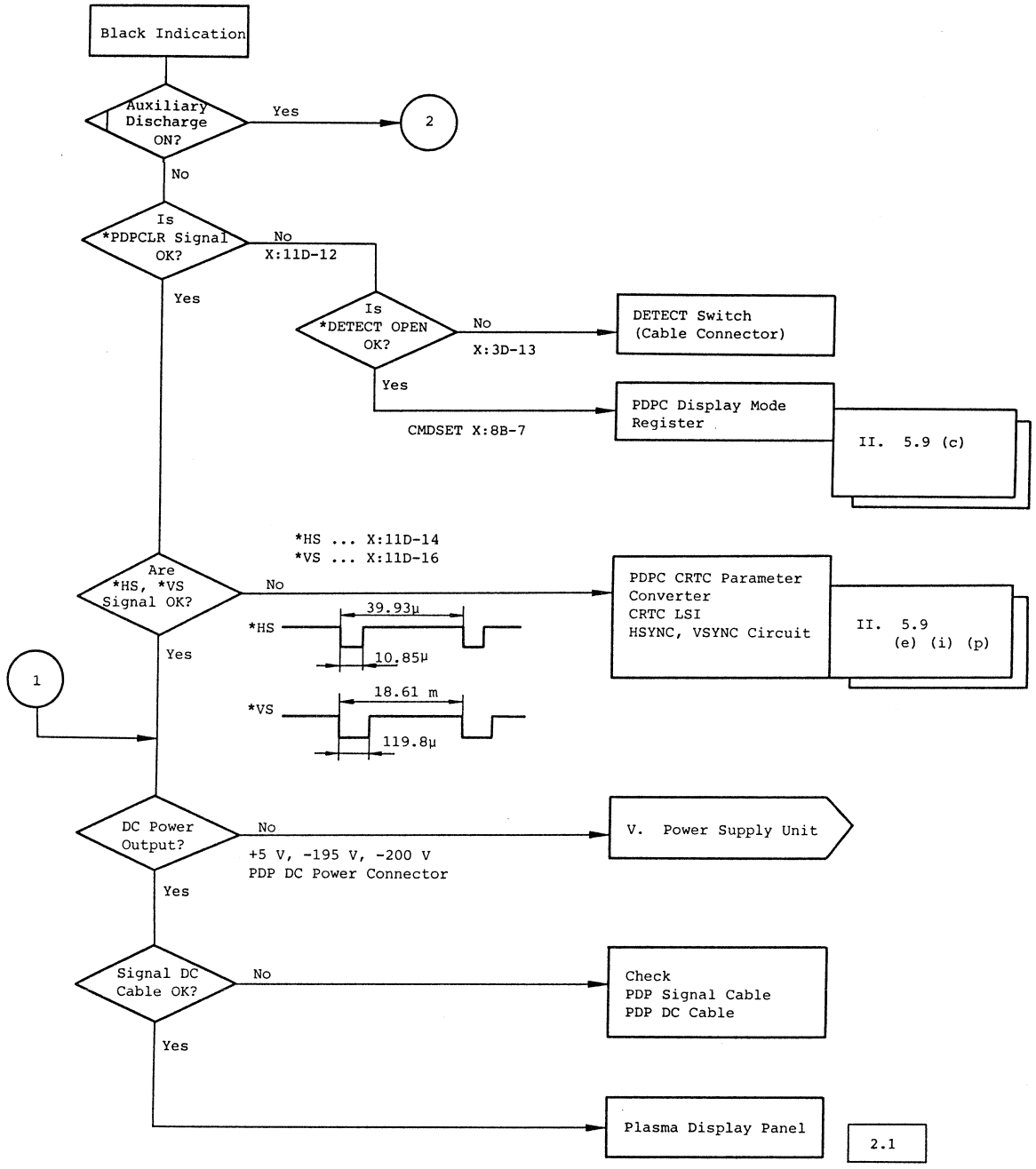


Figure 9-8 (1/2)

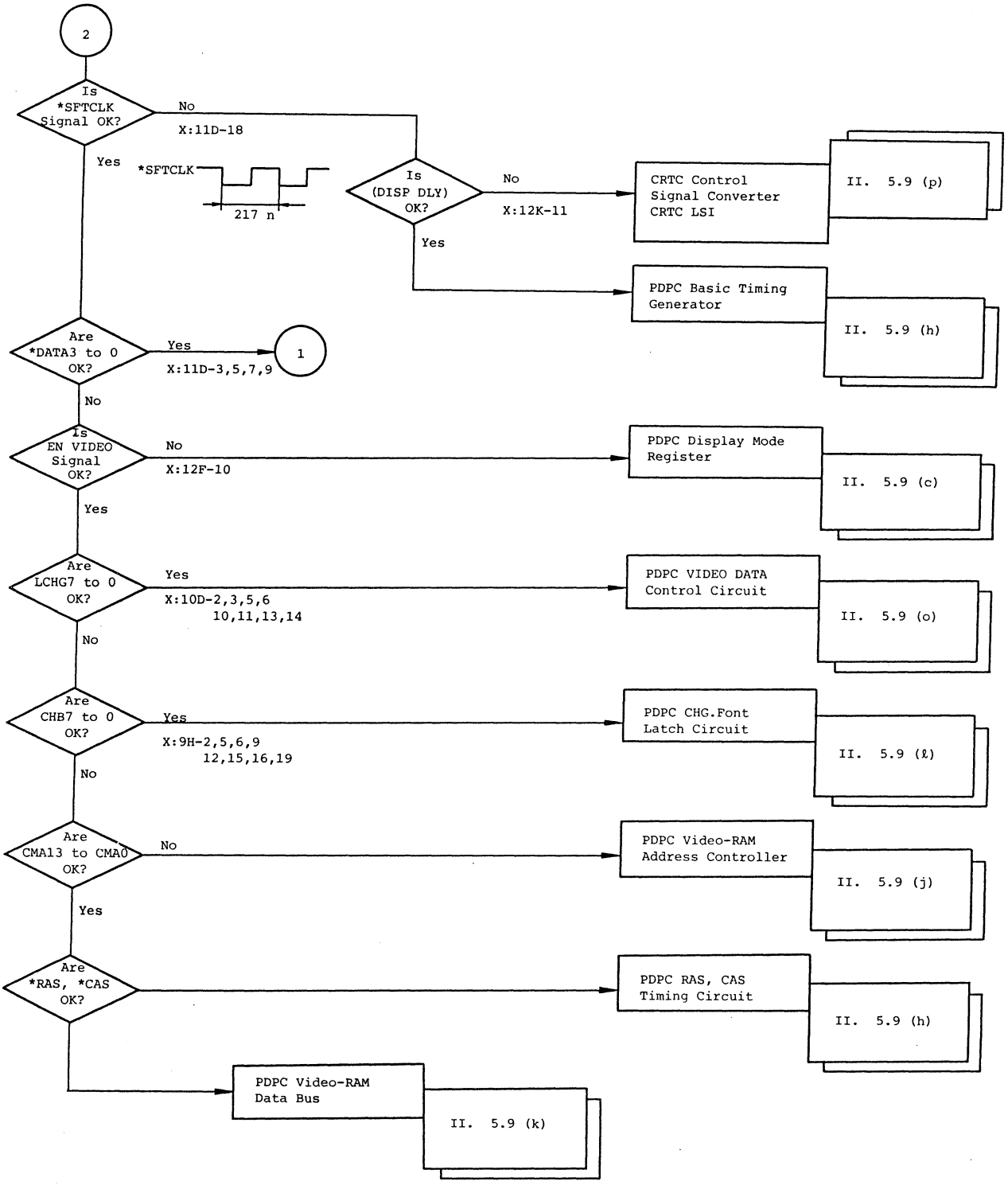

2
Is *SFTCLK Signal OK?
No
X:11D-18
Yes
*SFTCLK
217 n
Is (DISP DLY) OK?
No
X:12K-11
CRTC Control Signal Converter CRTC LSI
II. 5.9 (p)
Yes
PDPC Basic Timing Generator
II. 5.9 (h)
Are *DATA3 to 0 OK?
Yes
X:11D-3,5,7,9
1
No
Is EN VIDEO Signal OK?
No
X:12F-10
PDPC Display Mode Register
II. 5.9 (c)
Yes
Are LCHG7 to 0 OK?
Yes
X:10D-2,3,5,6 10,11,13,14
PDPC VIDEO DATA Control Circuit
II. 5.9 (o)
No
Are CHB7 to 0 OK?
Yes
X:9H-2,5,6,9 12,15,16,19
PDPC CHG.Font Latch Circuit
II. 5.9 (ℓ)
No
Are CMA13 to CMA0 OK?
No
PDPC Video-RAM Address Controller
II. 5.9 (j)
Yes
Are *RAS, *CAS OK?
PDPC RAS, CAS Timing Circuit
II. 5.9 (h)
PDPC Video-RAM Data Bus
II. 5.9 (k)

Figure 9-8 (2/2)

[2.3] Missed Dot Indication

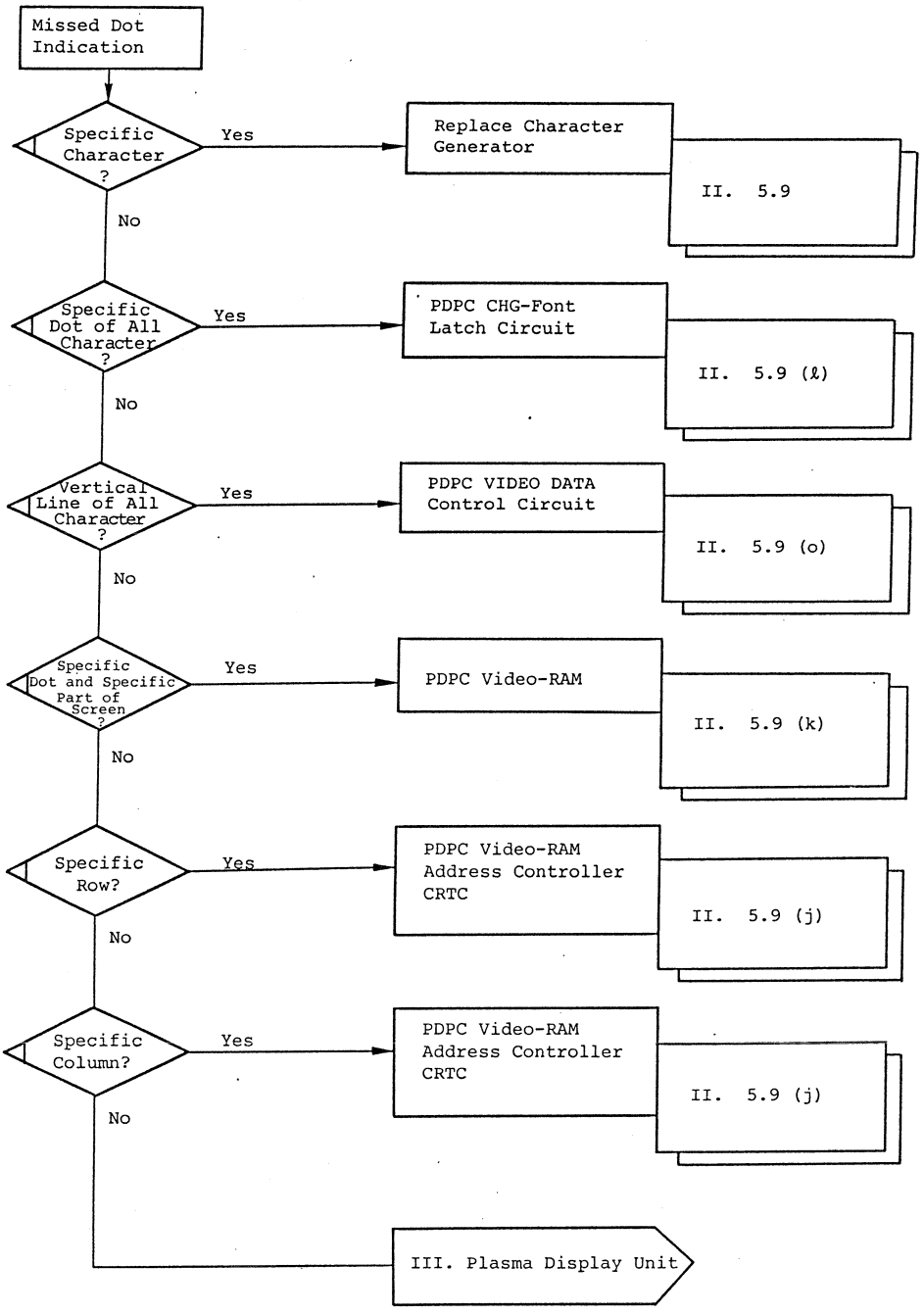


Figure 9-9

[2.4] Display Diagnosis Error

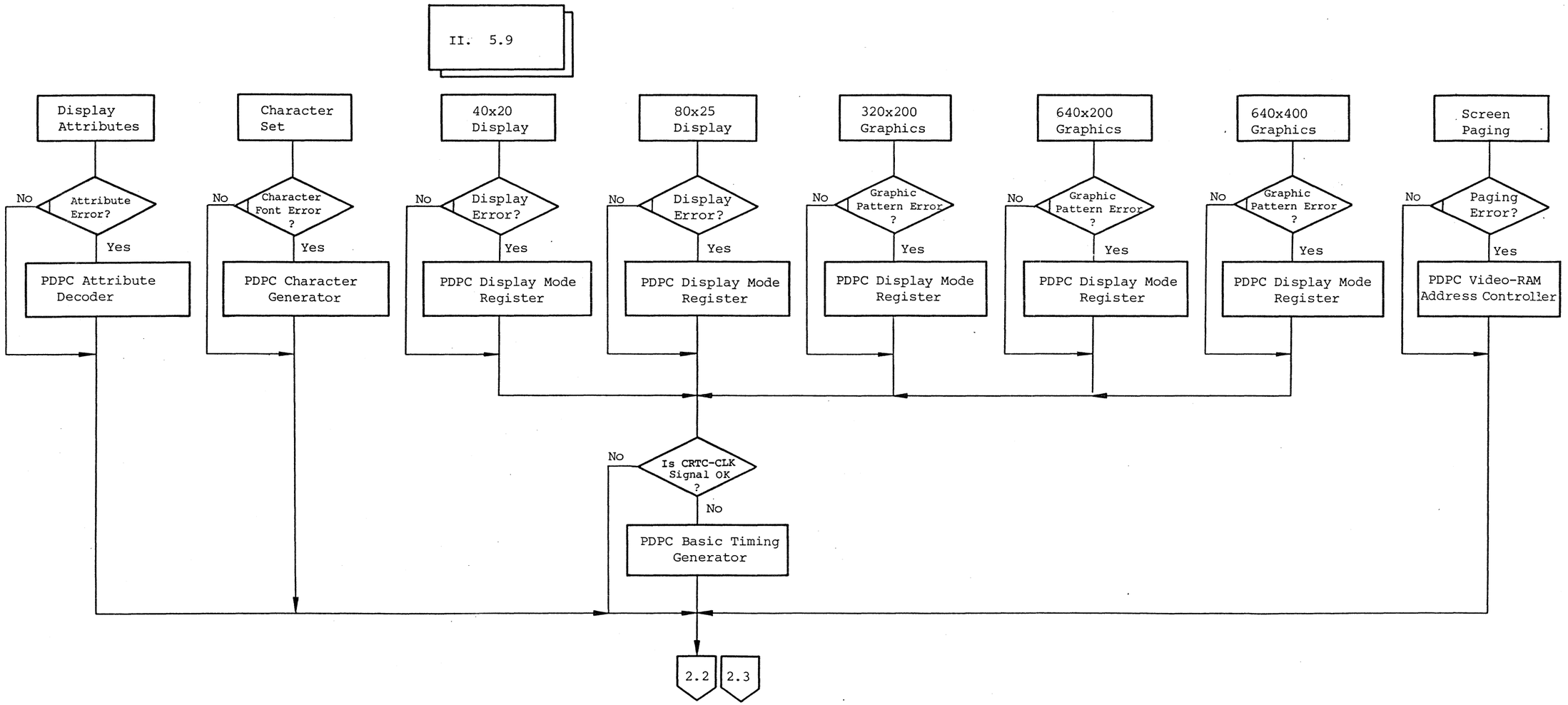


Figure 9-10

[3] Keyboard Section

[3.1] Power on Self-Diagnosis Error

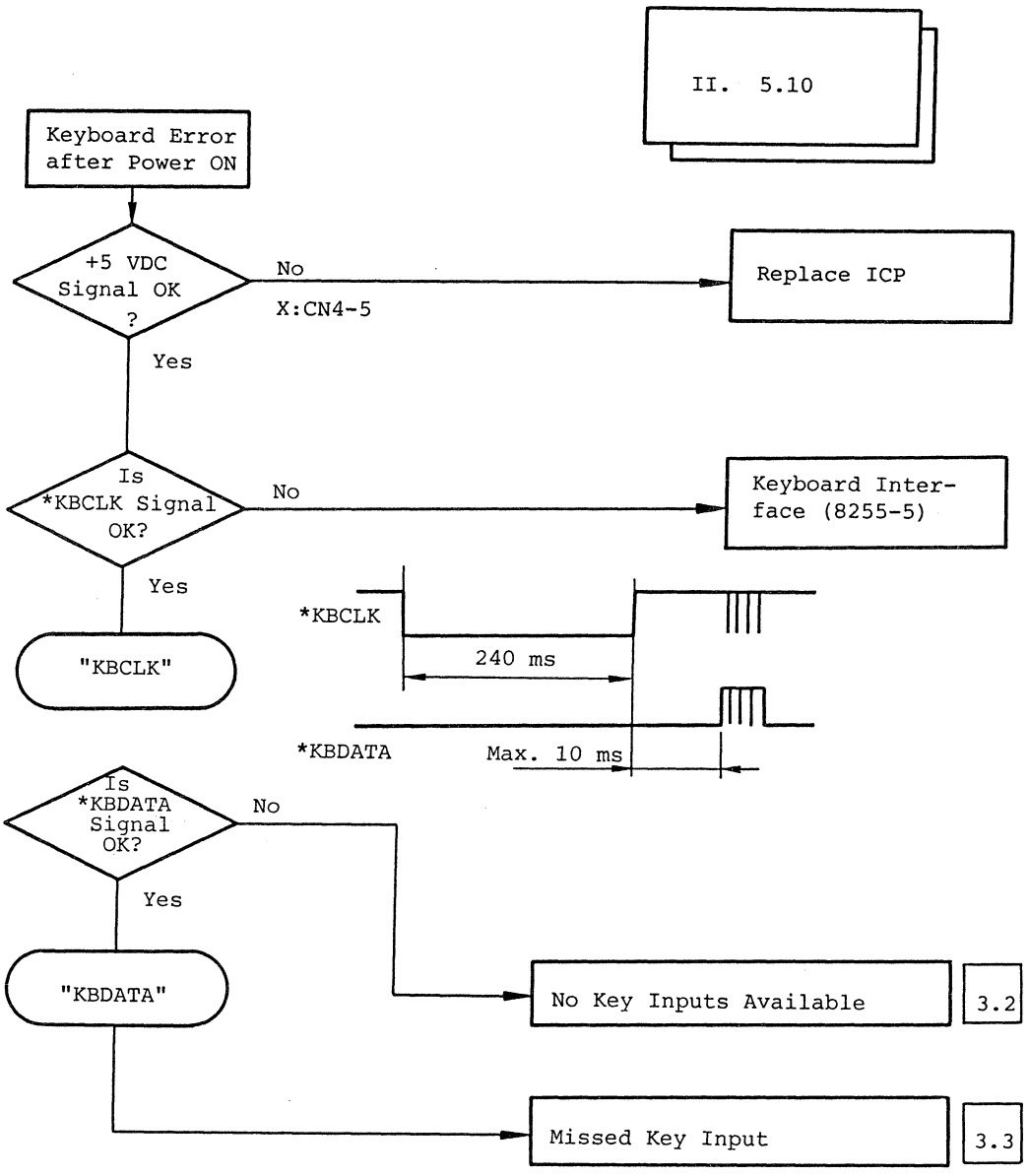


Figure 9-11 (1/2)

[3.2] No Key Inputs Available

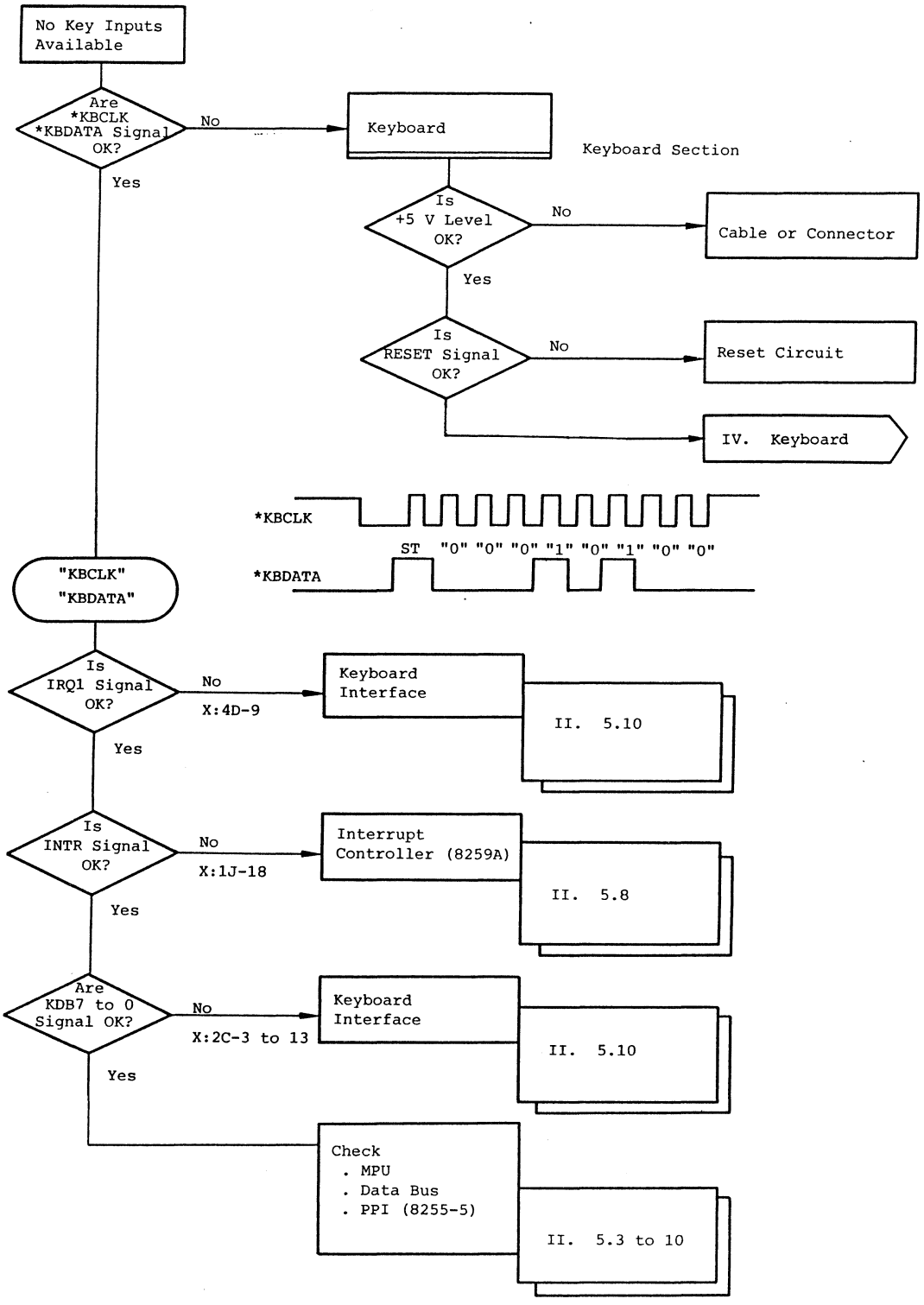


Figure 9-11 (2/2)

[3.3] Missed Key Input

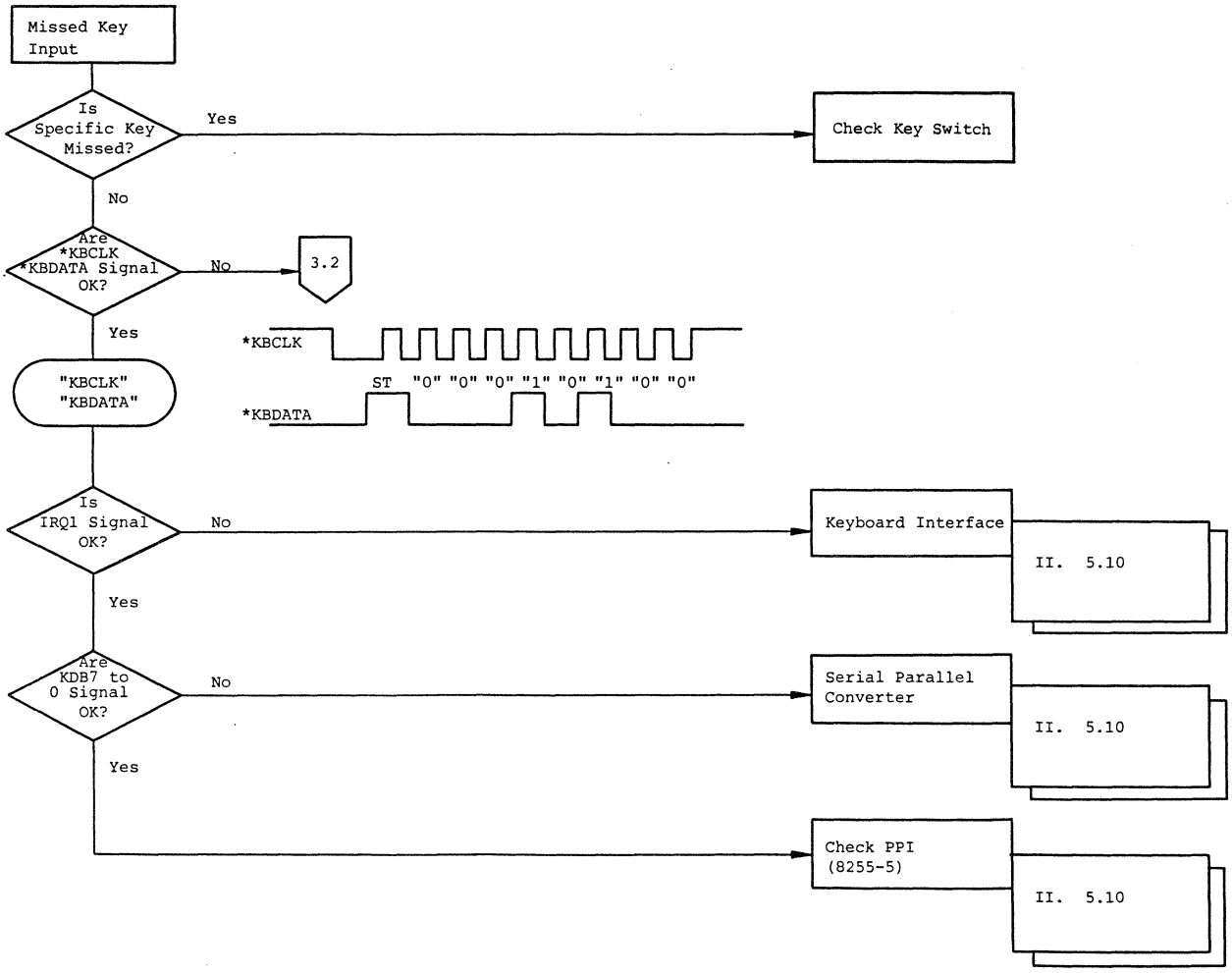


Figure 9-12

[4] MPU System Section

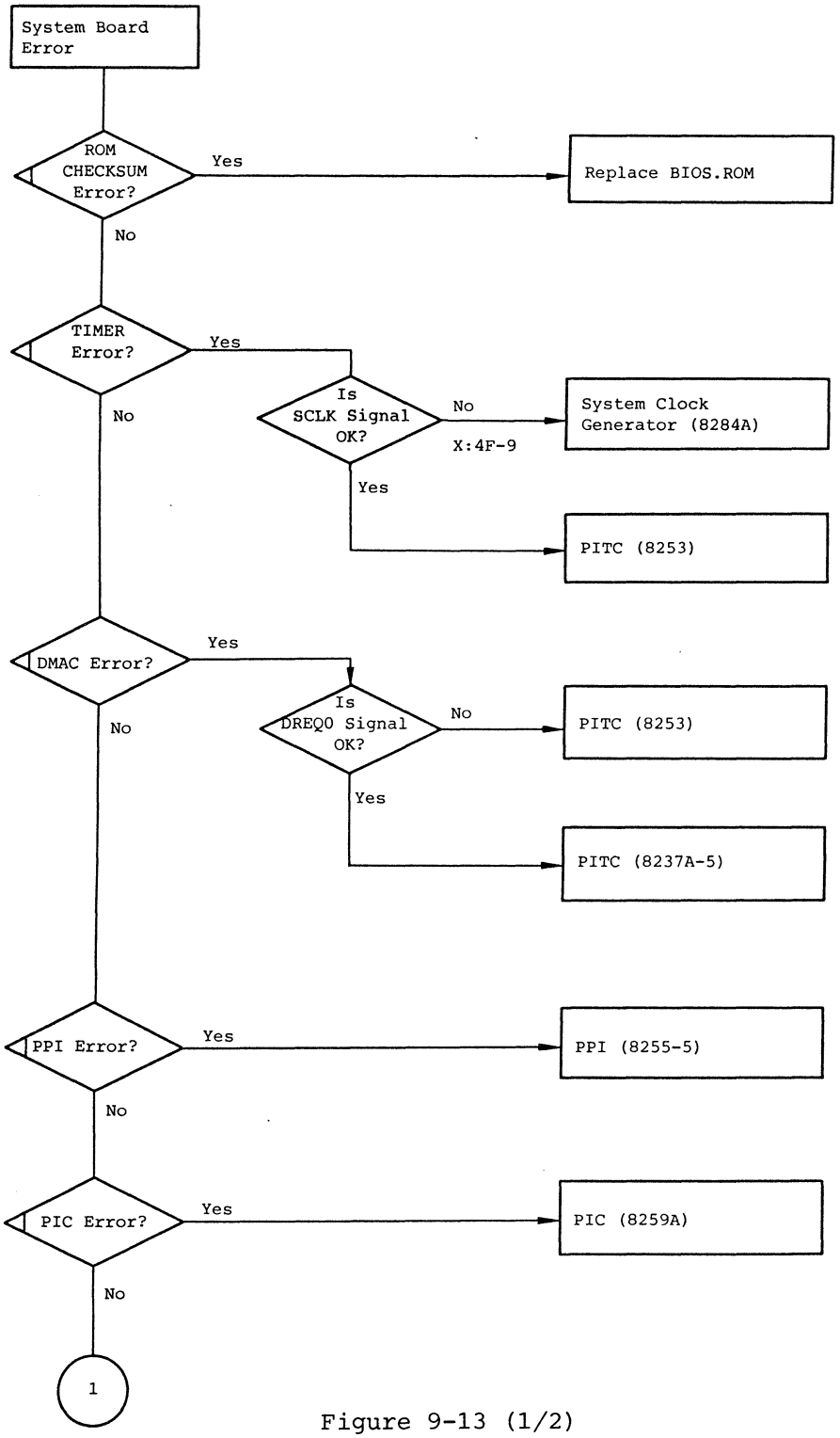


Figure 9-13 (1/2)

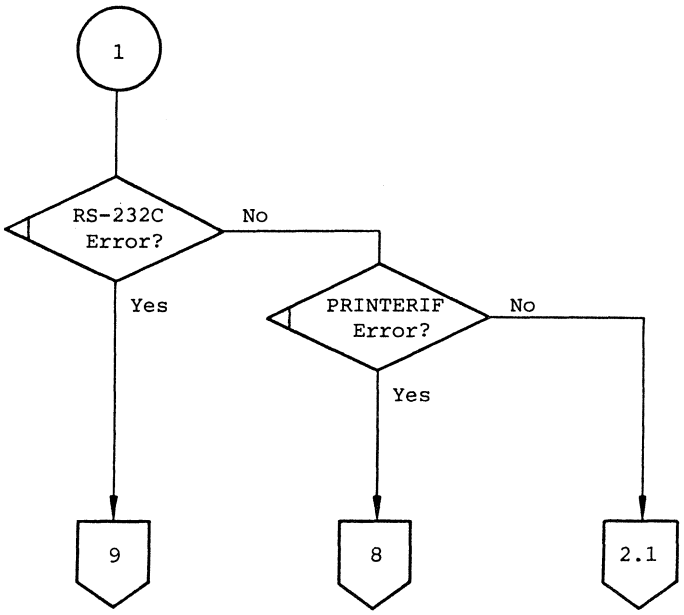


Figure 9-13 (2/2)

[5] RAM Read/Write Section

[5.1] Error in a Specific Bit or Address

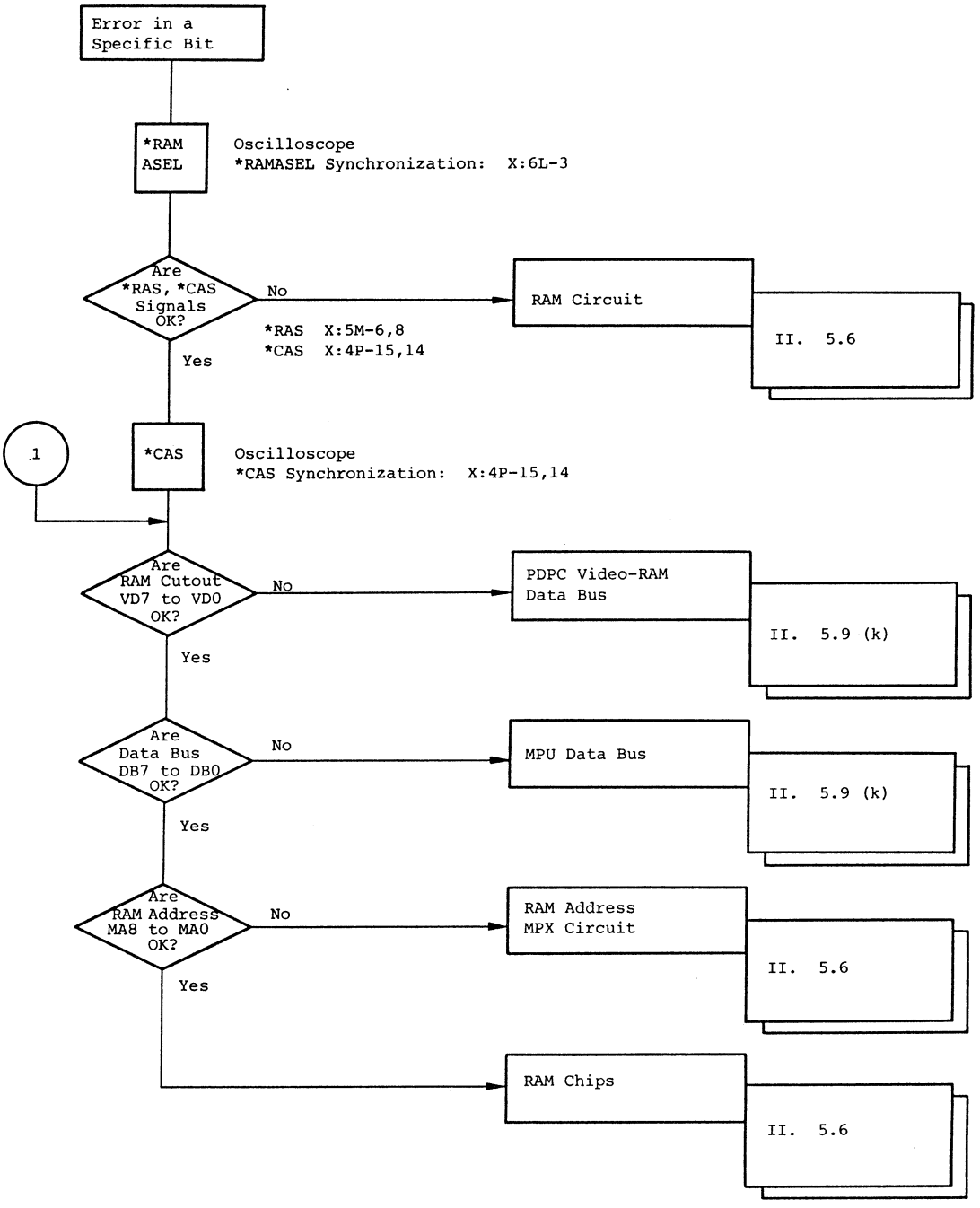
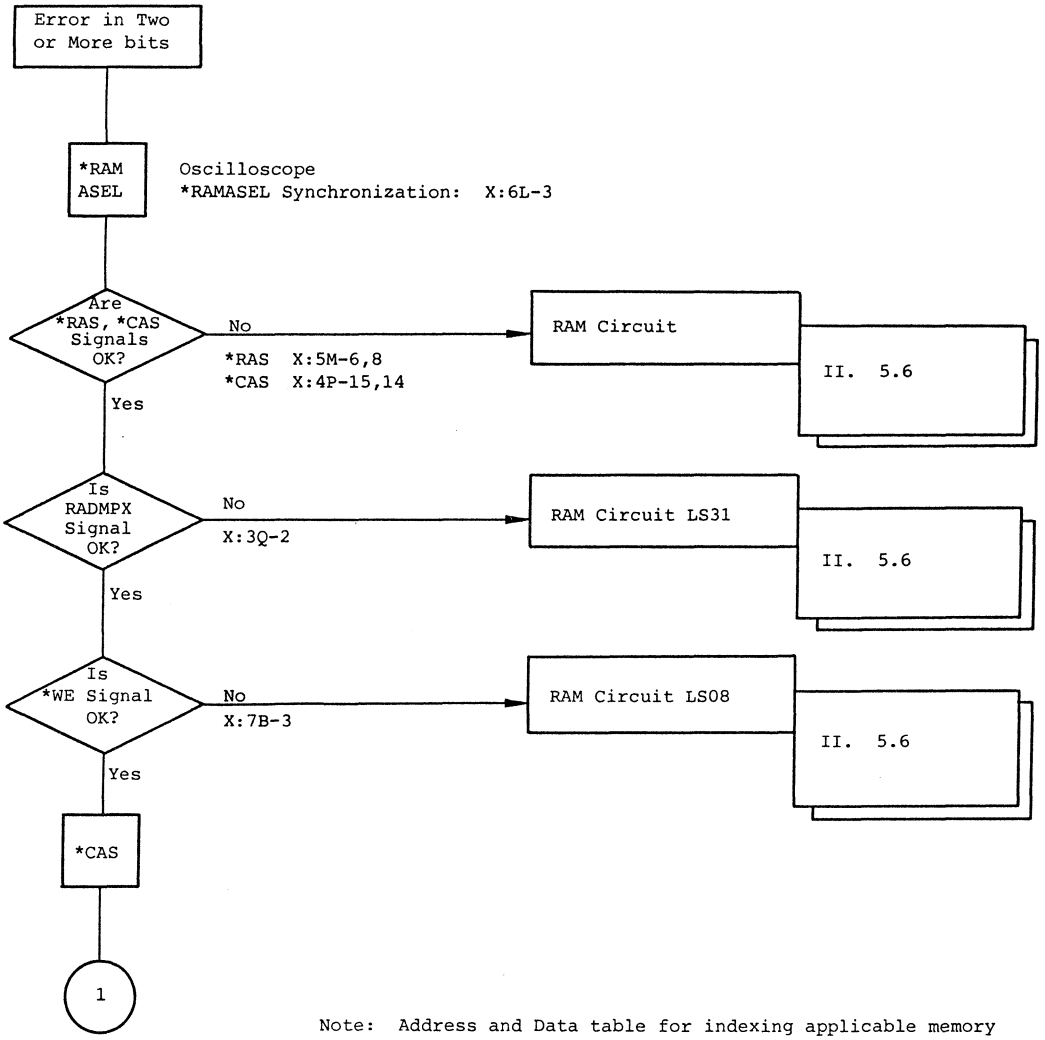


Figure 9-14 (1/2)

[5.2] Random Errors in Two or More Bits



Note: Address and Data table for indexing applicable memory

VD7	6N	7N	VD3	VD7	8N	9N	VD3
VD6	6P	7P	VD2	VD6	8P	9P	VD2
VD5	6Q	7Q	VD1	VD5	8Q	9Q	VD1
VD4	6R	7R	VD0	VD4	8R	9R	VD0

Address 00000H to 3FFFFH Address 40000H to 7FFFFH

Figure 9-14 (2/2)

[7] Floppy Disk Section

[7.1] Floppy Disk Error During Power-on Self Diagnosis

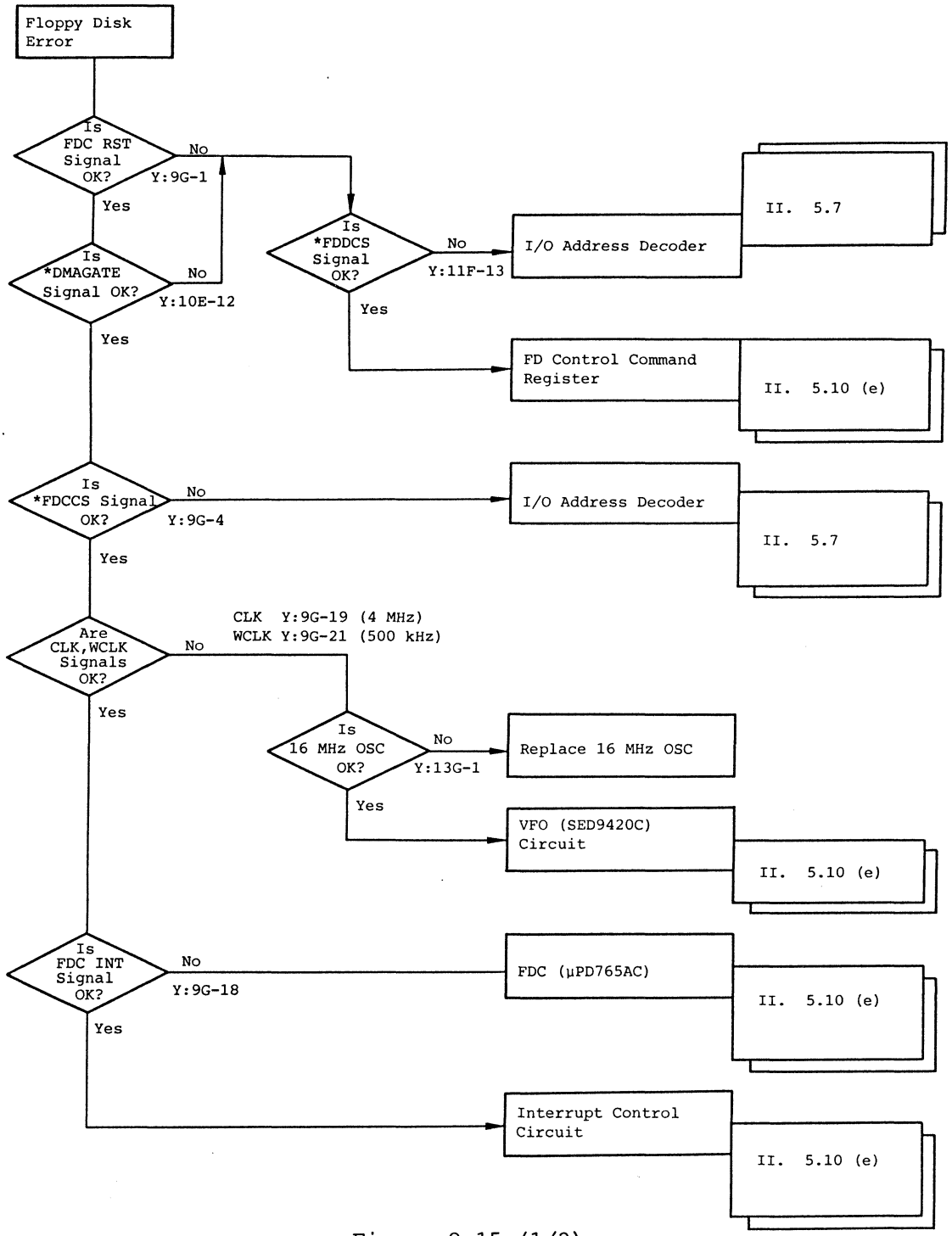


Figure 9-15 (1/2)

[7.2] DMA Overrun Error

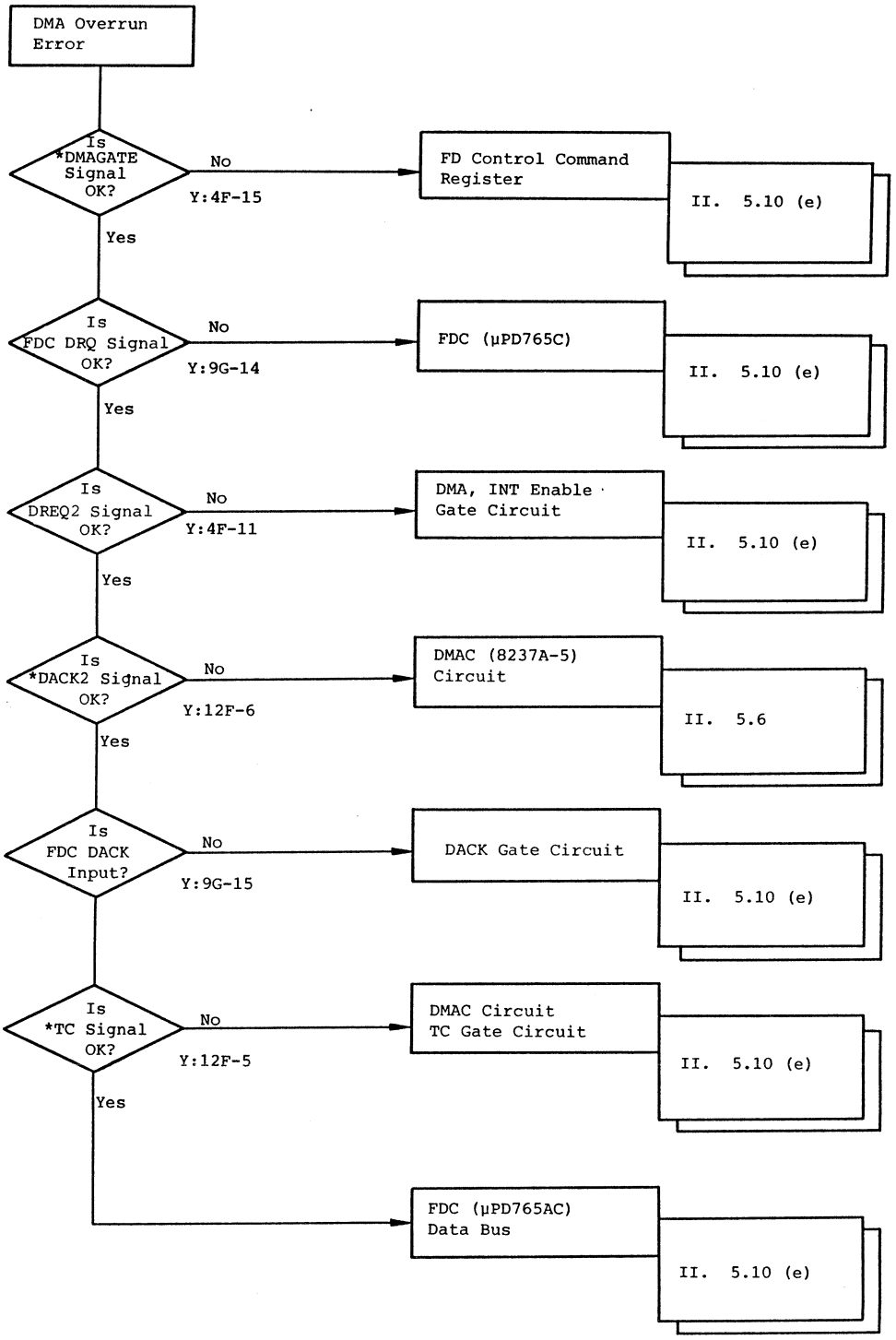


Figure 9-15 (2/2)

[7.3] Status Error

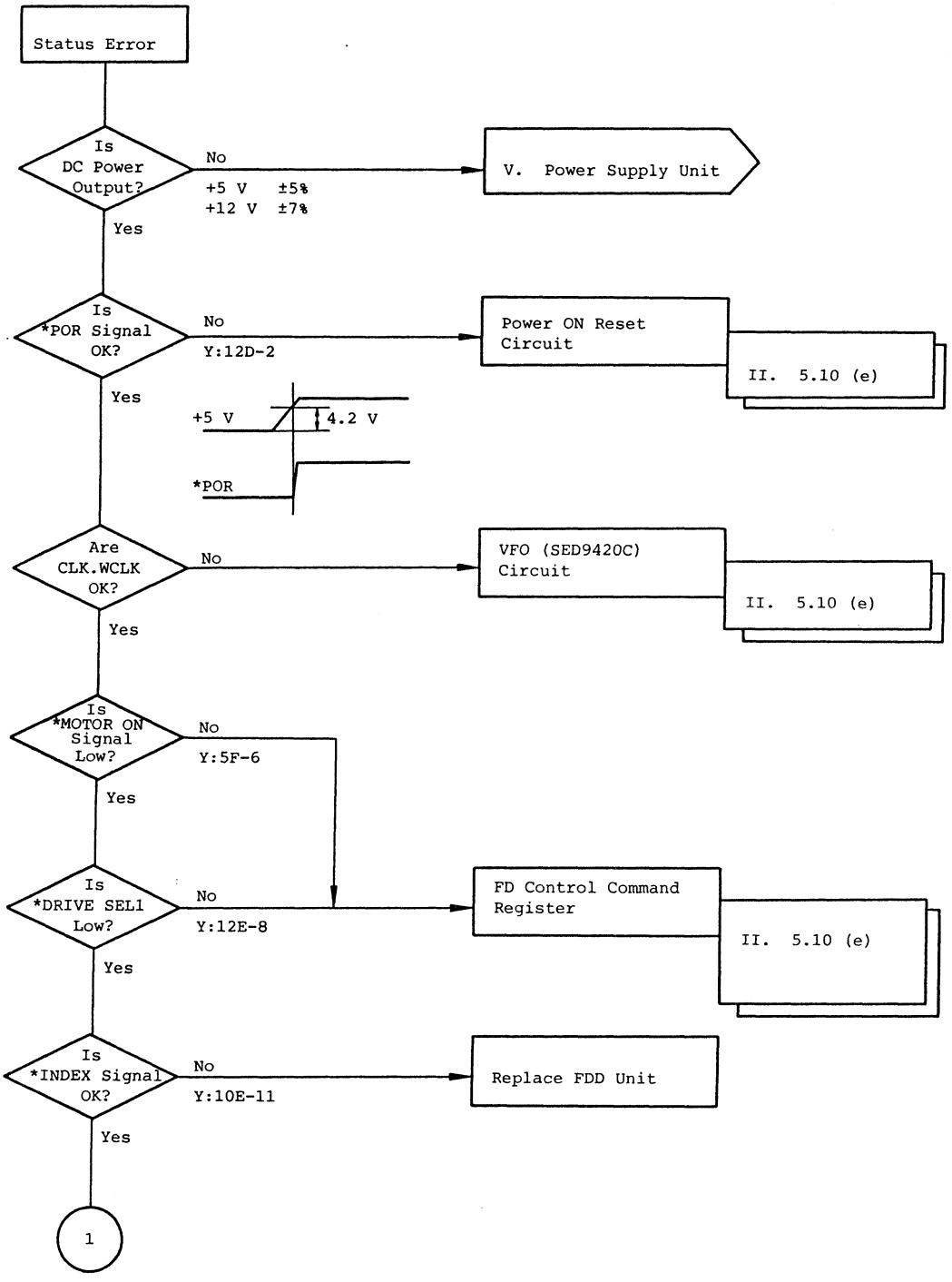


Figure 9-16 (1/2)

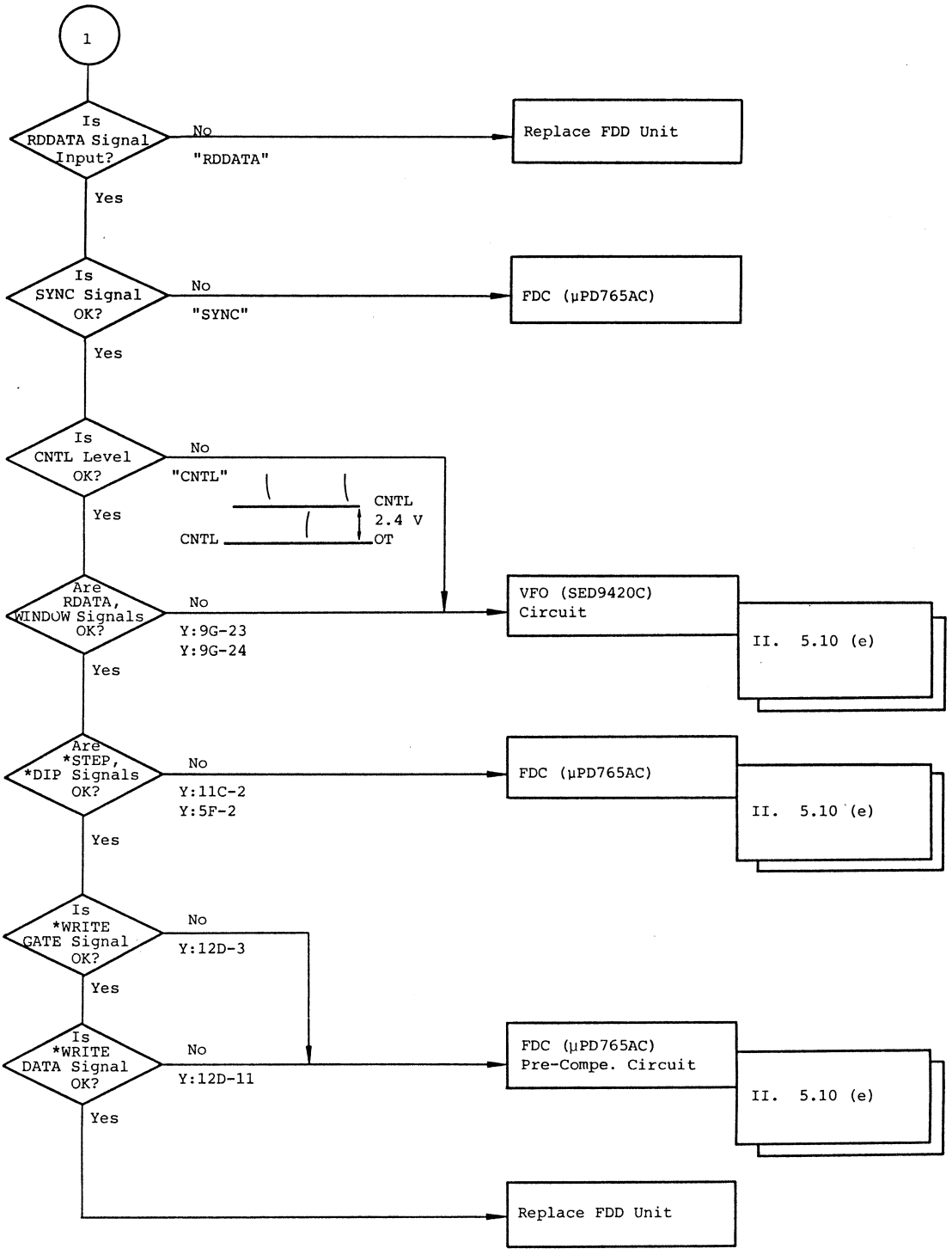


Figure 9-16 (2/2)

[8] Printer Section

[8.1] Not Available to Print or Status Error

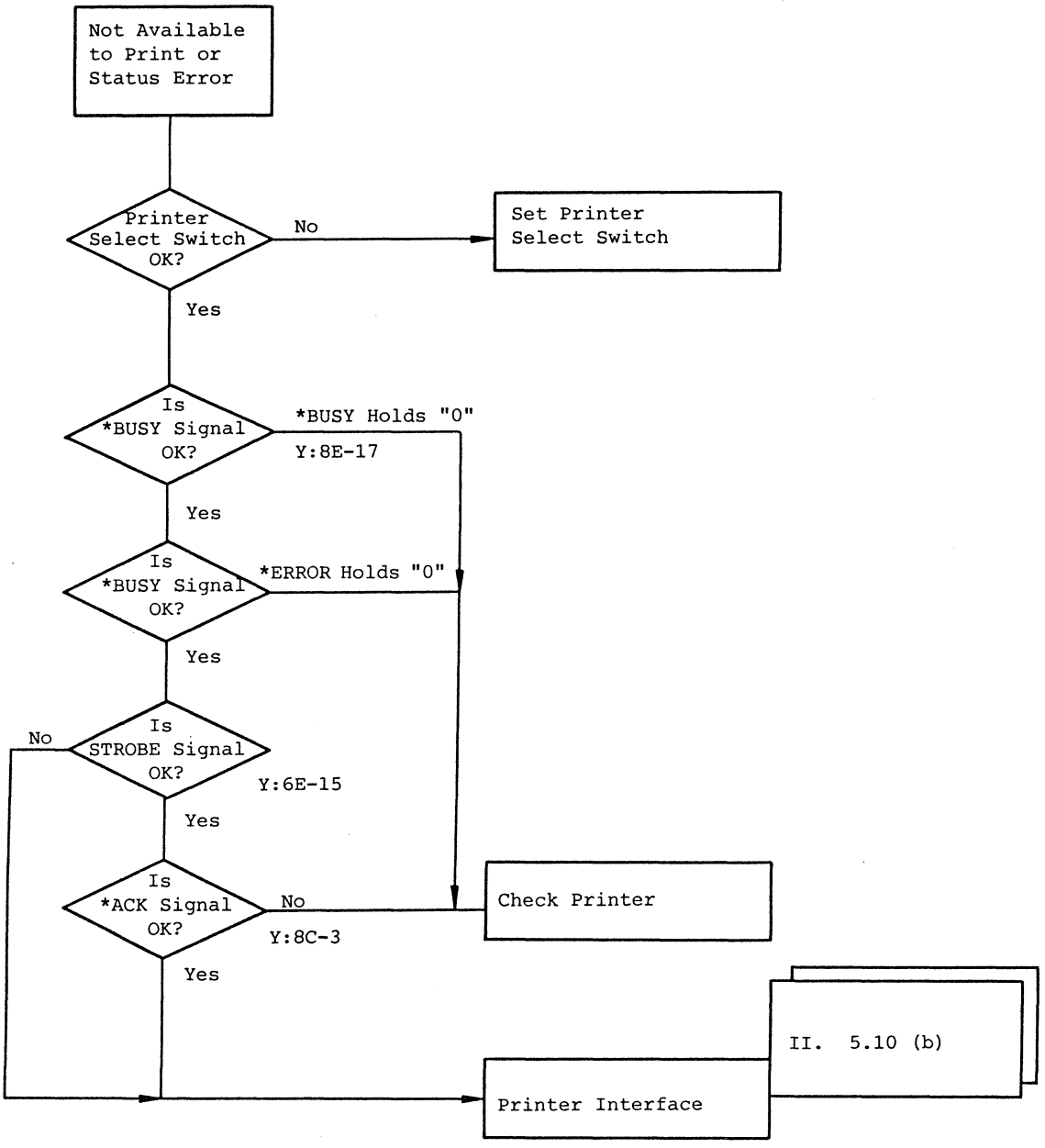


Figure 9-17 (1/2)

[8.2] Missed Character

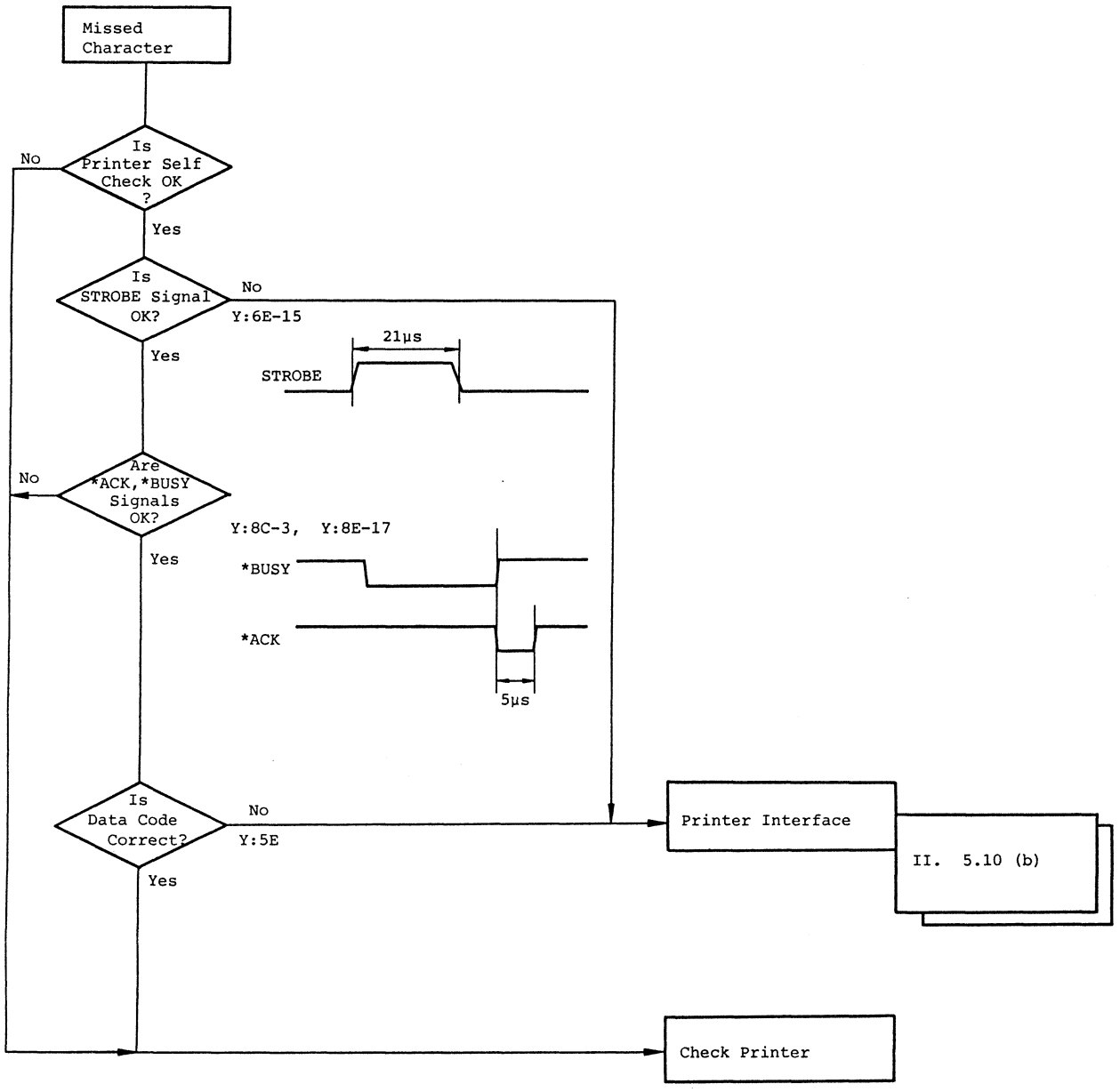


Figure 9-17 (2/2)

[9] Serial Port Section

[9.1] Time Out Error

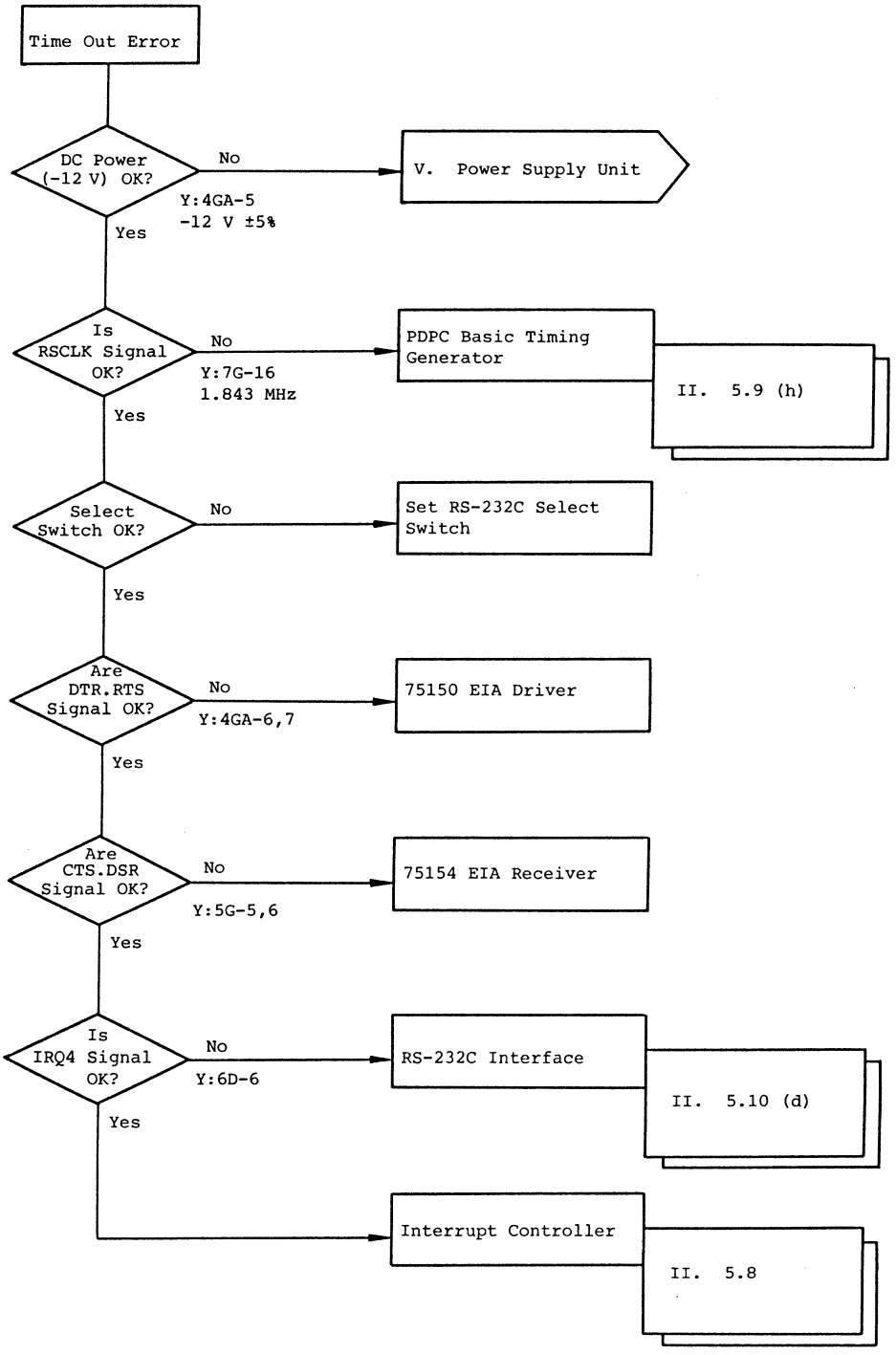


Figure 9-18 (1/2)

[9.2] Status Error

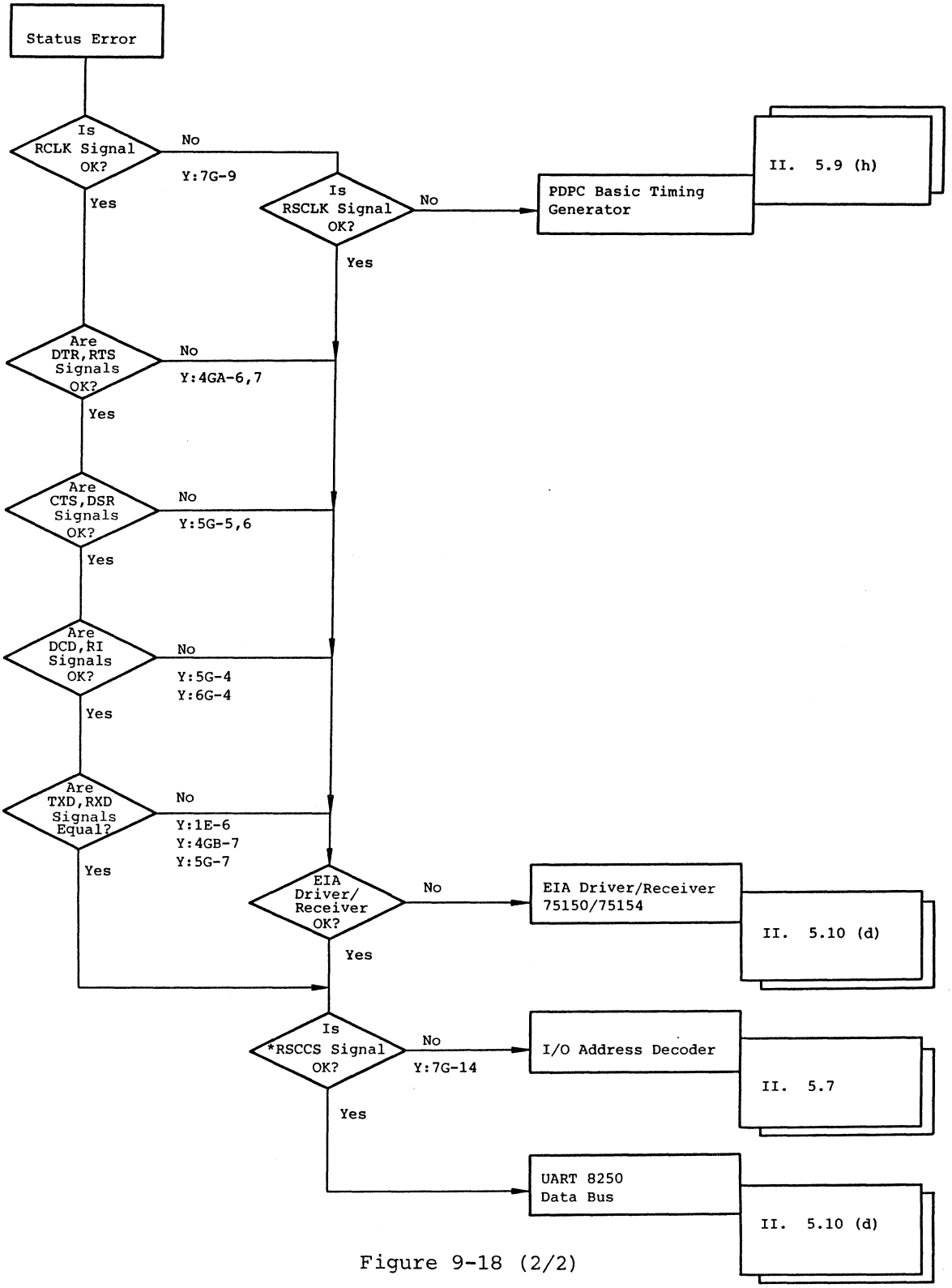


Figure 9-18 (2/2)

[10] Local Speaker Section

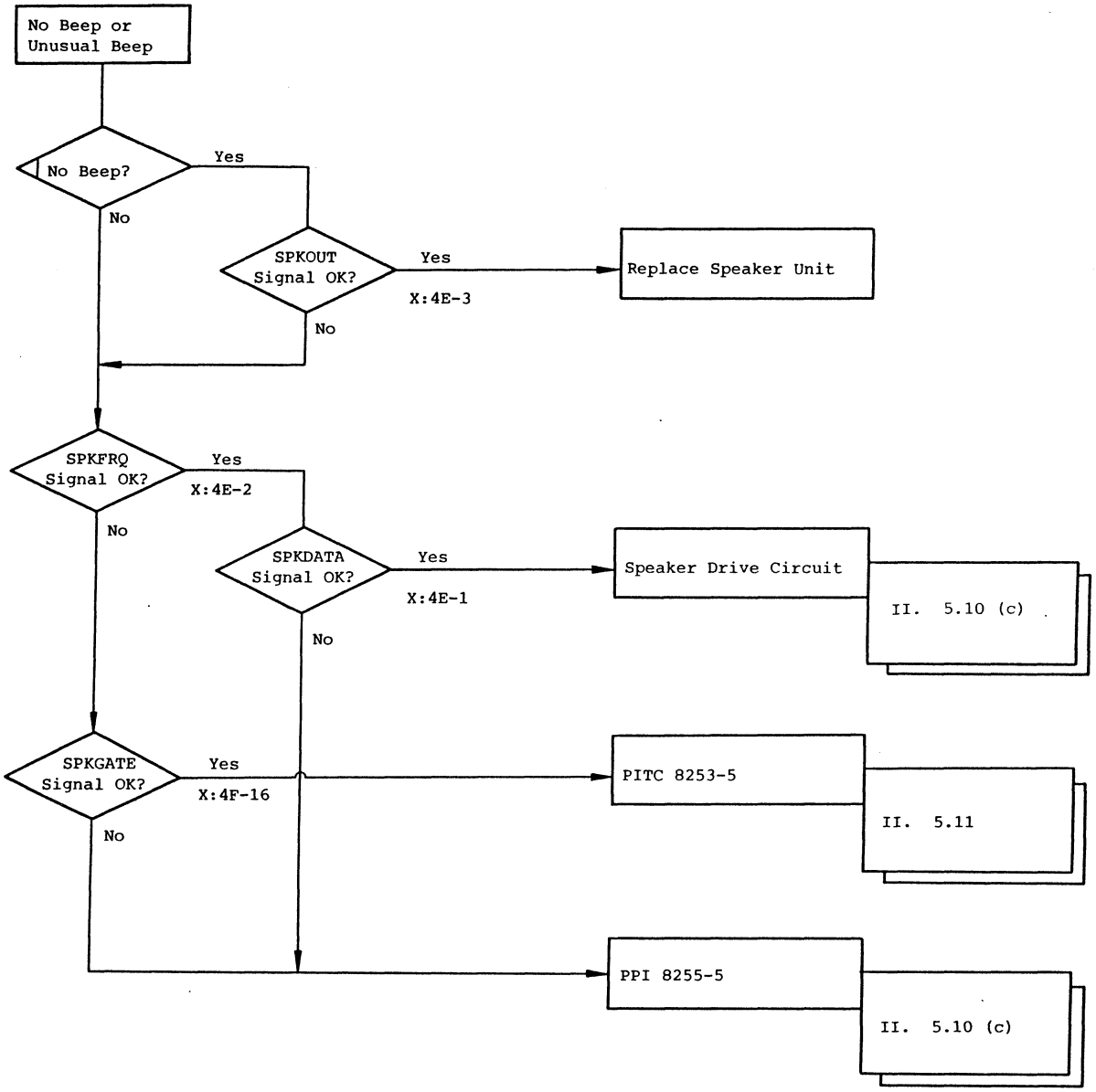


Figure 9-19

9.4 Self-Diagnostic Test

When power is supplied to the system the MPU performs a self-diagnosis starting at address FFFF0 (in hex) in ROM.

When an error is detected, a warning sound is generated or a warning message is displayed on the screen.

The power-on time self-diagnosis flow is shown in Figure 9-20.

The RAM read/write check is not carried out only if the ESC key on the keyboard is pressed at the power-on time.

Table 9-1 lists self-diagnostic error messages.

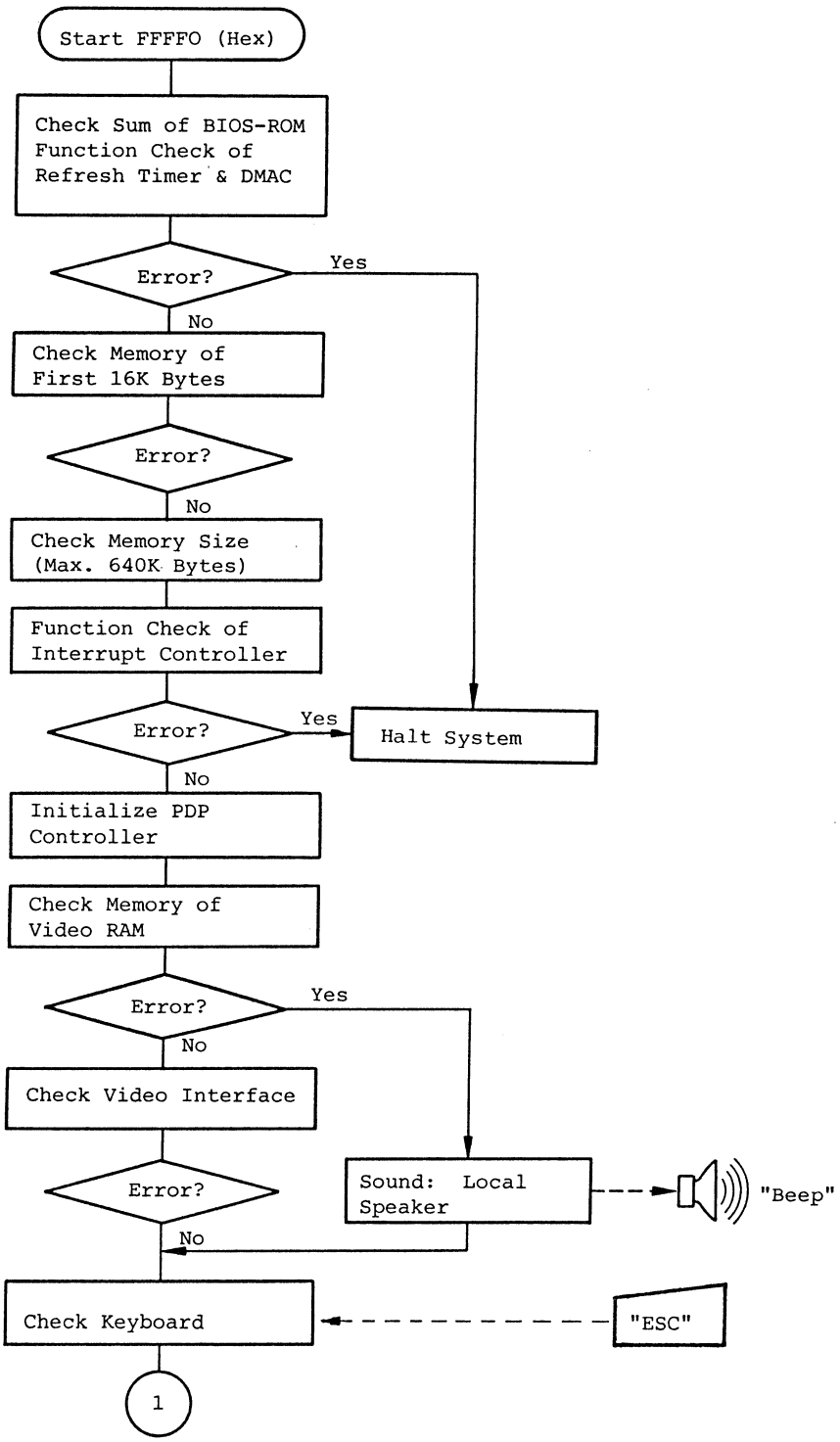


Figure 9-20 Self-Diagnosis Flow (1/2)

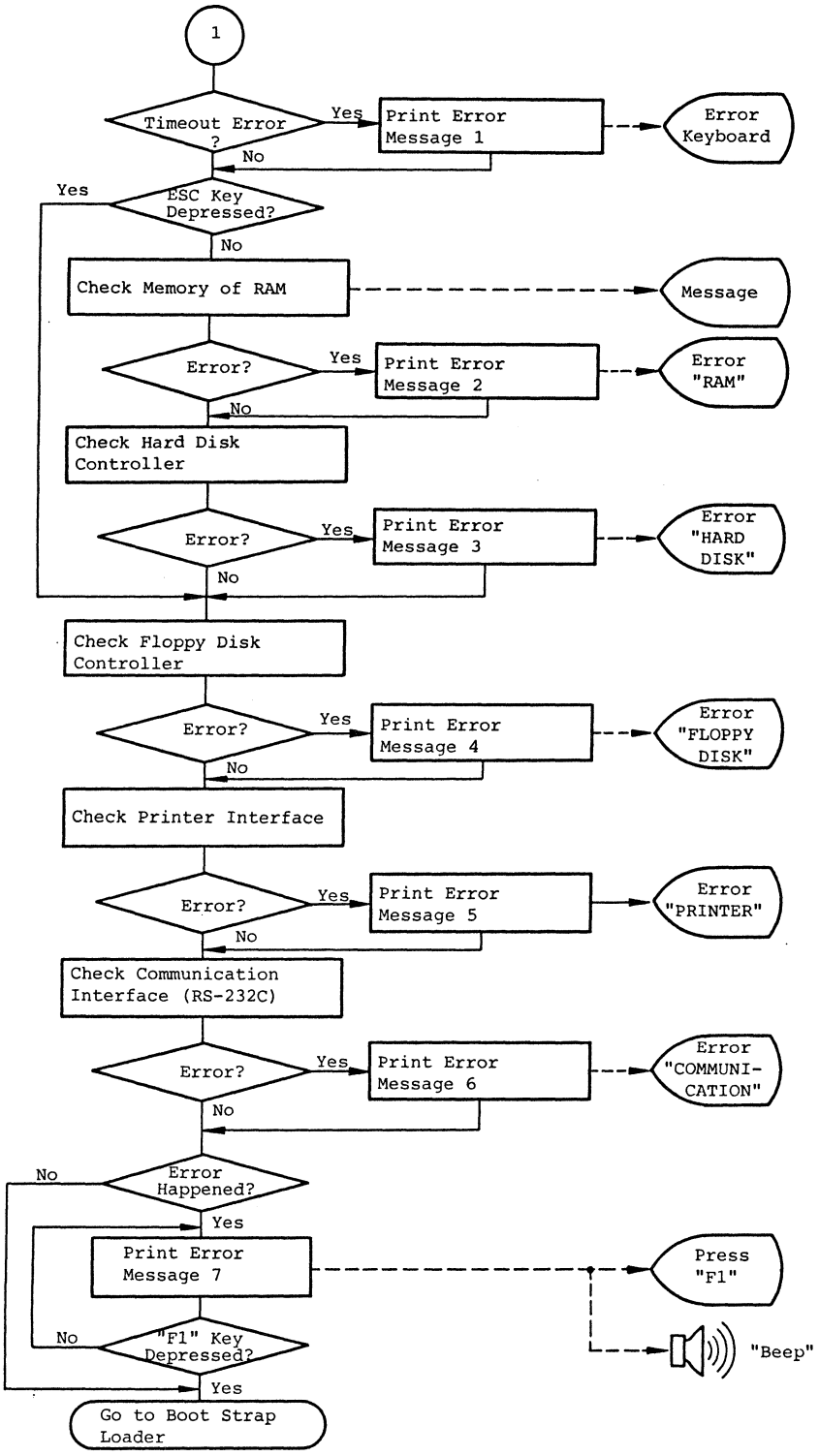


Figure 9-20 Self-Diagnosis Flow (2/2)

Table 9-1 Self-Diagnostic Error Messages

Message on Display		Beep or Halt System	Possible Causes
No.	Message		
1	KEYBOARD ERROR or XX KEYBOARD ERROR	——	Keyboard Reset Failed or Found Stuck keys XX: Scan code
2	XXXX XX XX ERROR	——	Memory (RAM) Failed 1st XXXX: Address 2nd XX: Read data 3rd XX: Write data
3	HARD DISK ERROR	——	Hand Disk Controller Failed
4	FLOPPY DISK ERROR	——	Floppy Disk Controller Failed
5	PRINTER ERROR	——	Printer Interface Failed
6	COMMUNICATION ERROR	——	Communication Interface Failed
7	PRESS F1 KEY	2 short Beep	Unknown error occurred
	——	3 short, 3 long, 3 short Beep "SOS"	VIDEO-RAM Failed
			HSYNC Signal Failed
			VSYNC Signal Failed
		Halt System	BIOS-ROM Failed (Check Sum Error)
			DMAC Failed
			Refresh Timer Failed
			Interrupt Controller Failed
	RAM CHECK EXECUTING	——	(RAM check executing)
	XXX KB OK	——	(Memory Size XX K Bytes)

9.5 DIAG Program

9.5.1 General

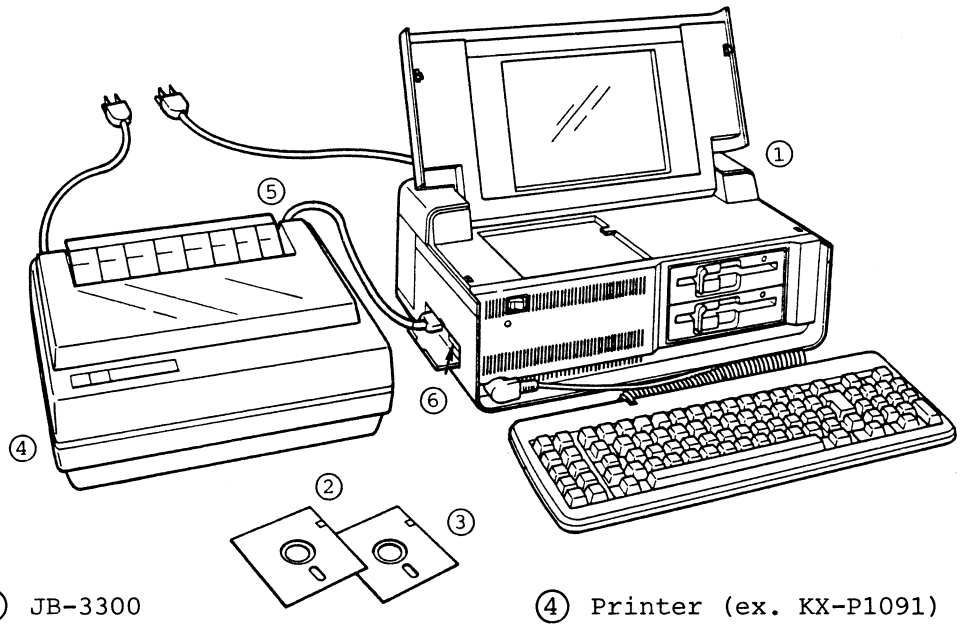
A diagnostic program tests a computer system's hardware. The diagnostic program for the computer tests all of the following devices and tells you if and where any errors occur:

1. System board
2. Memory
3. Keyboard
4. Display
5. Parallel port (printer)
6. Serial port (RS-232C)
7. Floppy disk
8. Hard disk
9. Local speaker

The program can be started once the MS-DOS system disk is loaded. At the end of the diagnosis, the DOS must be loaded again.

9.5.2 Preparation

Connection should be made as shown in the figure below:



① JB-3300
② Diagnostic Disk
③ Scratch Disks
④ Printer (ex. KX-P1091)
⑤ Printer Cable
⑥ RS-232C Loop-Back Plug

Figure 9-21

9.5.3 Loading diagnostic program

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Insert the DIAGNOSTIC disk in drive A, then turn the computer's power switch to ON.	Current date is x-xx-19xx Enter new date:_	If you don't see these messages, eject the disk from the drive. Make sure that the disk is labelled "DIAGNOSTIC" and that you inserted it into the drive correctly. If it is the correct disk and it was properly inserted, the problem could be in the disk drive or in the computer's logic unit. The system unit should be serviced.
2	Press [↵] key.	Current time is x:xx:xx.xx Enter new time:_	
3	Press [↵] key.	A> _	
4	Type [d] [;] [a] [g] ↓	ENTER THE TYPE OF KEYBOARD? (1=USA 2=SWEDEN 3=DENMARK ...)	Be sure to select the correct number corresponding to your countrys keyboard as displayed on the above screen. If you make an incorrect country keyboard. Selection, the screen will display different character during the keyboard test.
5	Type [1] ↓	DO YOU WANT A PRINTOUT	If you want to print the results ...
6	Type [y] ↓	STOP WHEN AN ERROR OCCURS?(Y/N)	If you want to stop the program after an error has been found. type y. Type n if you want the program to continue.
7	Press [y]	DIAGNOSTIC MENU 1. TEST ALL DEVICES 2. TEST AUTOMATICALLY 3. CHANGE MENU 4. ERROR LISTING 5. EXIT SELECT MENU? _	

9.5.4 Diagnostic Menu

Select and carry out any of the five diagnostic functions described below:

1. TEST ALL DEVICES

   To test all or some of the devices one by one, press 1 and ↵ .

2. TEST AUTOMATICALLY

   The second option, "TEST AUTOMATICALLY", tests all devices automatically without pausing between devices, and then returns to the diagnostic menu. Press 2 and ↵ to begin the automatic test.

3. CHANGE MENU

   The program must know what devices are installed in your system to test them. To obtain a menu of the installed devices, select "CHANGE MENU" by pressing 3 and ↵ .

4. ERROR LISTING

   To obtain the results of the diagnosis, select "ERROR LISTING" from the diagnostic menu by pressing 4 and ↵ .

5. EXIT

   When you have run all the tests you want to run, exit from the diagnostic program by pressing 5 and ↵ .

9.5.5 Test All Devices

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [1] [↵] into DIAGNOSTIC MENU.	SYSTEM DEVICES 1. MAIN BOARD 2. xxx KB MEMORY 3. KEYBOARD 4. DISPLAY 5. PRINTER 6. SERIAL PORT 7. FLOPPY DISK 8. HARD DISK 9. LOCAL SPEAKER 10. CO-PROCESSOR 16. EXIT ENTER DEVICE NUMBER?_	To test a device, key in its number and press [↵] . At the end of the test, the screen will return to the original display. In this way, you can test as many of the devices as you wish. Each of the ten tests is described below. When you have finished, press 16 and [↵] to return to the diagnostic menu. To terminate the test before it is completed, press the [Break] key while holding down the [Cntrl] key. The screen should return to the diagnostic menu.

1. MAIN BOARD Test*

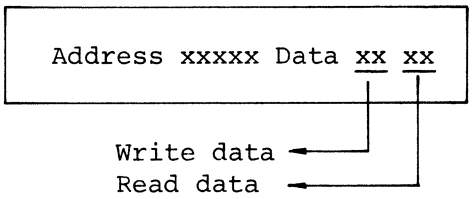
1	Type [1] [↵] into SYSTEM DEVICES MENU.	MAIN BOARD TEST Test complete Press any key to continue _	If any errors are found on the board, the screen will display: MAIN BOARD TEST *** ERROR *** You may get an additional error message. For example, if there is a problem with the floppy disk controller, you may see this message: FDC FAILED A problem on your main board means that the system unit should be serviced.

* Main board comprises two boards: CPU board and I/O board

1. MAIN BOARD Test (Continued)

Step	Test Procedures	CRT Displays or Printer Print Outs	
2	Press any key.	Return to the SYSTEM DEVICES MENU.	Press any key and you will then be asked to select the next device to be tested.* (Note: * When the system asks you to press any key, you should press the spacebar, the return key, or any of the letter, number, or punctuation mark keys. Caps lock, shift keys, and similar keys will not work as responses to this prompt.)

2. MEMORY Test

1	Type [2] [↵]	MEMORY TEST This test takes up to 2 minutes. Please stand by .... Test complete Press any key to continue _	If an error is found, you will see a message like this:  If there is a problem in the memory the system unit should be serviced.
2	Press any key to return to the menu.		

3. KEYBOARD Test

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [3] [↵]	* Refer to Figure 9-22.	This is then followed by a series of squares (■) each representing a key on the keyboard.
2	Press all keys.	* Refer to Figure 9-23.	Press each key in turn and watch the display. While the key is held down, the block representing that key should change to display the character on the key in reverse video (e.g. ■A). When the key is released, the character should be displayed normally (e.g. [A]). If the display does not look like this, press n and [↵] . Check the keyboard cord. If the cord connection is loose, plug the cord in firmly and run the keyboard test again. If the display is still not correct, the keyboard should be serviced. If the display is correct, press y and [↵] to continue the diagnostic test.

4. DISPLAY Test

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [4] [↵]	DISPLAY TEST OPTION 1. ATTRIBUTE TEST 2. DISPLAY CHARACTER 3. TEXT MODE (40 x 25) 4. TEXT MODE (80 x 25) 5. GRAPHICS MODE (320 x 200) 6. GRAPHICS MODE (640 x 200) 7. GRAPHICS MODE (640 x 400) 8. PAGE CHANGE TEST 9. EXIT SELECT OPTIONS?__	If you wish to run all the tests consecutively, without pausing between tests, press [↵] . The program will run through all the tests, and return you to the original display when finished. If you wish to run the tests individually, press the number of the first test you wish to run and [↵] . After each test, the screen will return to the original display. You can then run the next test. When you have run all the tests you want, press 9 and [↵] to return to the SELECT DEVICES menu. The following sections show the screen display and the action required for each display test.
2	[1] [↵]	* Refer to Figure 9-24.	Tests 2 and 8 are described in Figures 9-25 and 9-31, respectively. If your display failed any of the display tests, the display unit should be serviced.
3	[y] or [n]	Return to the Menu.	

5. PARALLEL PORT Test

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Make sure the printer is in the ONLINE mode. Type [5] [↵] into SYSTEM DEVICES MENU.	PARALLEL PORT TEST * Refer to Figure 9-32. Press any key to continue __	The program will perform the test you have selected and print diagnostic messages if there are any error. Error messages are described in Error Messages Section.
2	Press any key to return to the menu.		

6. SERIAL PORT Test

1	Type [6] [↵] into SYSTEM DEVICES MENU.	SERIAL PORT TEST Attach the loop back plug to the connector. Press any key when ready __	
2	Attach the loop back plug. Press any key when ready __	Press any key to continue __	The diagnostic program will perform the test you have selected, and print diagnostic messages if there are any errors. Error messages are described in Error Messages Section.
3	Press any key to return to the menu.		

7. FLOPPY DISK Test

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [7] [↵] into SYSTEM DEVICES MENU.	FLOPPY DISK TEST OPTION 1. SEQUENTIAL ACCESS 2. RANDOM ACCESS 3. VERIFY DISK 4. SPEED CHECK 5. EXIT SELECT OPTIONS? __	Each test takes up to 45 minutes. At the end of each test, press any key and go on to the next section.
2	Enter the number of the test you want to perform.	**** WARNING **** Disk will be over-written. Insert scratch disk in drive A: and press any key when ready.	A scratch disk is a blank disk or one that doesn't contain any files. It must be format-ted for the DOS.
3	Insert the scratch disk and press any key.		The diagnostic program will perform the test you have selected and print diagnostic messages if there are any errors. Error messages are described in Error Messages Section.

8. HARD DISK Test

Press 11 and ↵ to test the hard disk drive and controller. The screen will then display:

```
HARD DISK TEST

**** WARNING ****
Data on max cylinder will be overwritten

Do you want to include write test? (Y/N)
```

If you want to perform Read/Write test, press Y and ↵ .
If you do not want, press N and ↵ .

Then the diagnostic program perform. You will see the following message:

```
RANDOM SEEK TEST
```

The diagnostic program perform the random seek test.

```
DISK WRITE TEST
```

The diagnostic program perform the writing test on max cylinder.

The diagnostic program print diagnostic messages if there are errors, as in following examples:

```
**** ERROR ****
RECORD NOT FOUND
Command 82 H 01 C 205 S 01 Address 100 Wt DB Rd D6
```

These messages are described later.

The diagnostic program will be completed with the message as follows:

```
Test complete.

Press any key to continue
```

Diagnostic Messages

Diagnostic messages consist of two parts, as shown in the following examples:

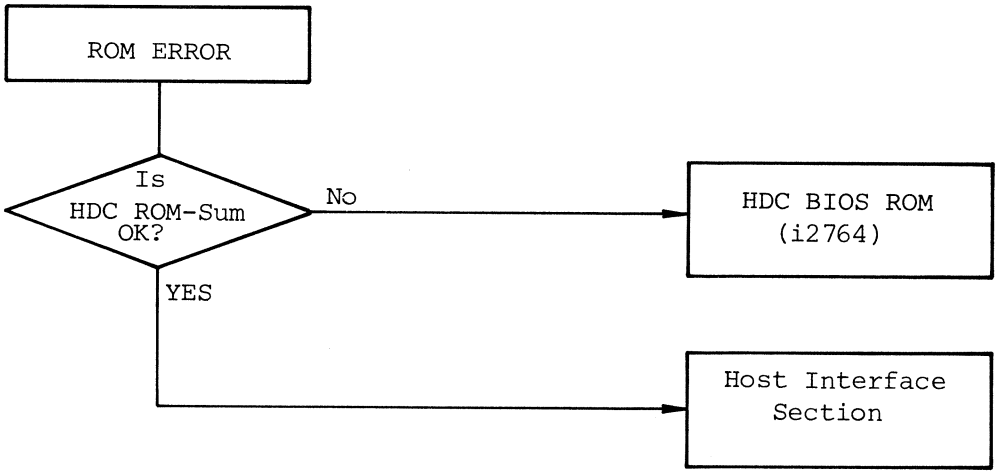
```
RECORD NOT FOUND
Command 82 H 01 C 205 S 01 Address 100 Wt DB Rd D6
```

1. RECORD NOT FOUND .... Type of error

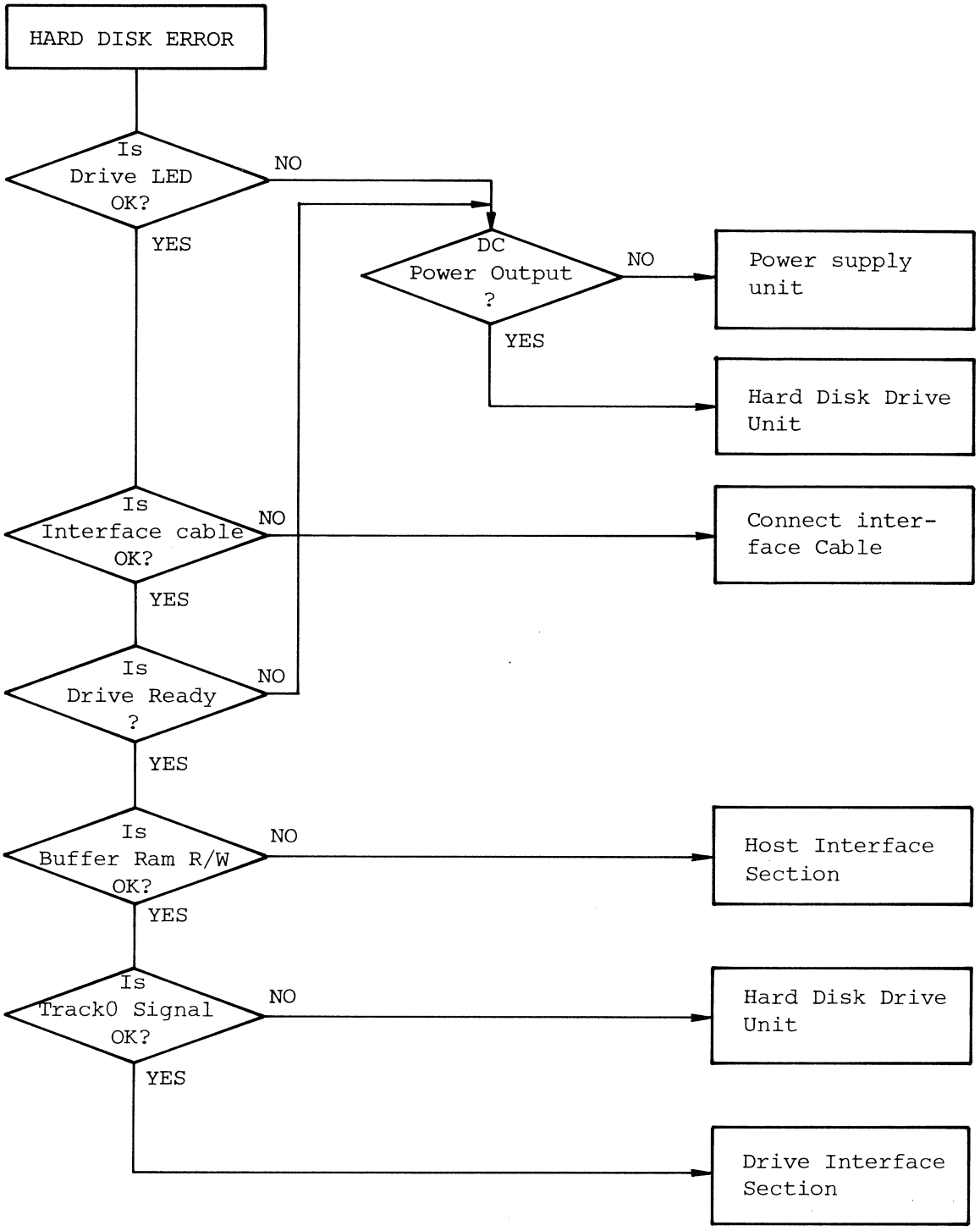
2. Command 82 Head 01 Cylinder 205 Sector 01 ... Error mode and location

Hard Disk Operation Section

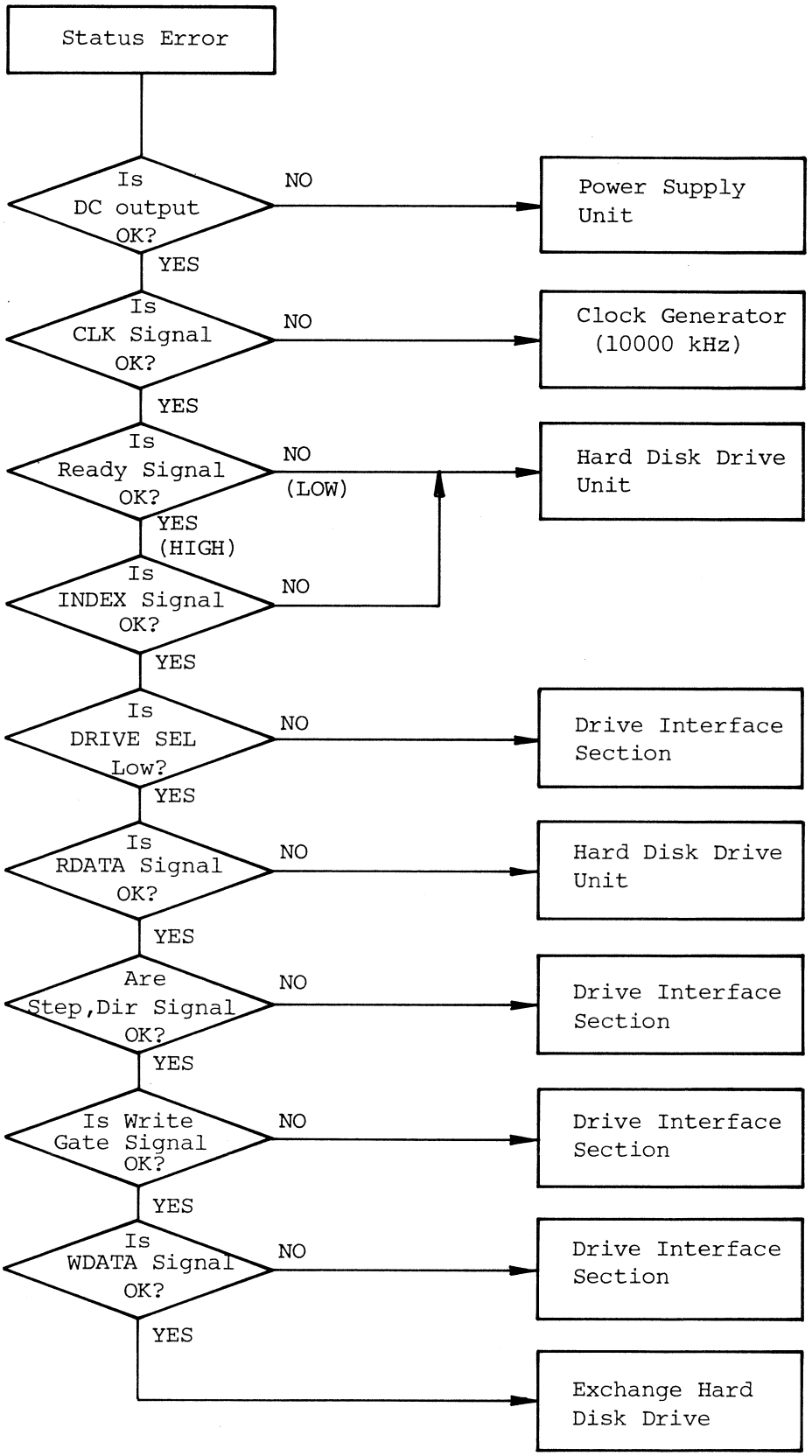
ROM Error During Basic Assurance Test



8.2 HARD DISK Error During Basic Assurance Test



8.3 Status Error



9. LOCAL SPEAKER Test

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [9] [↵] into SYSTEM DEVICES MENU.	LOCAL SPEAKER TEST	You should hear a series of ascending tones from the local speaker. If you don't hear any tones, the system unit should be serviced.
2		Press any key to continue _	
3	Press any key to return to the menu.		

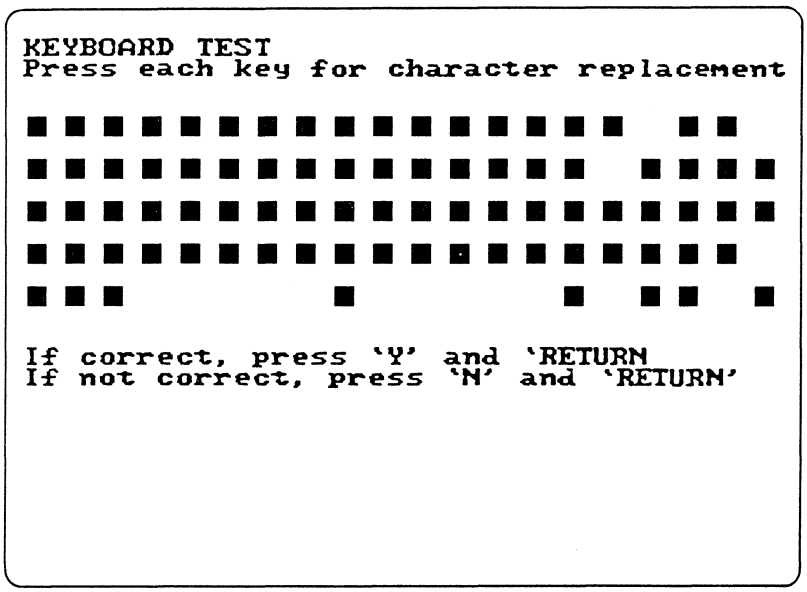


Figure 9-22 Keyboard Test

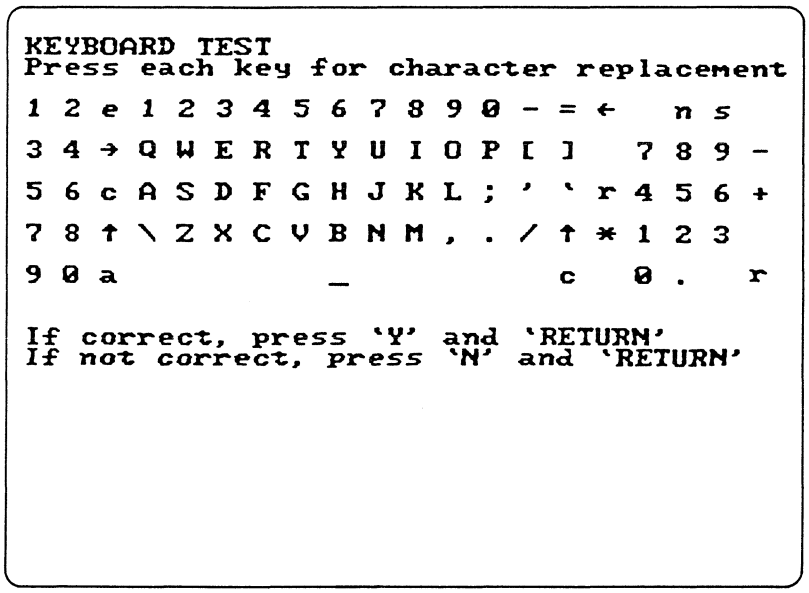


Figure 9-23 Keyboard Test

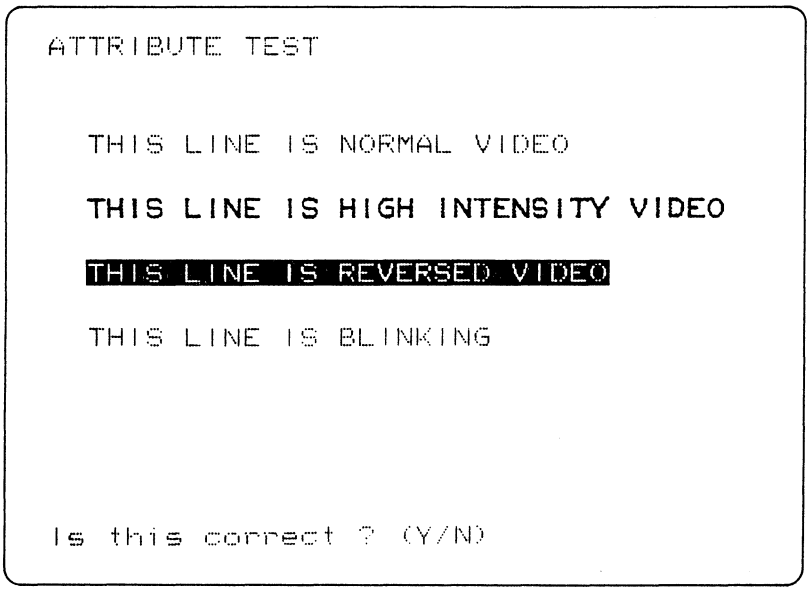


Figure 9-24 Attributes Test

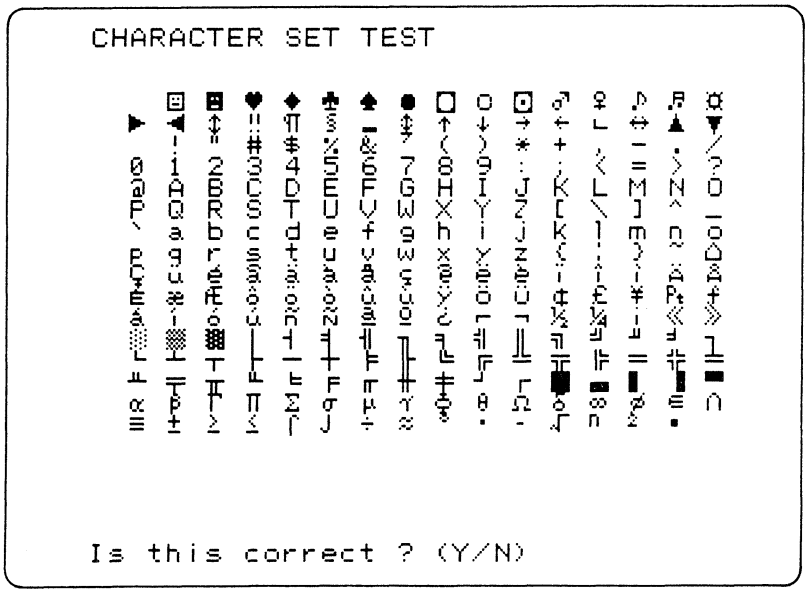


Figure 9-25 Character Set Test

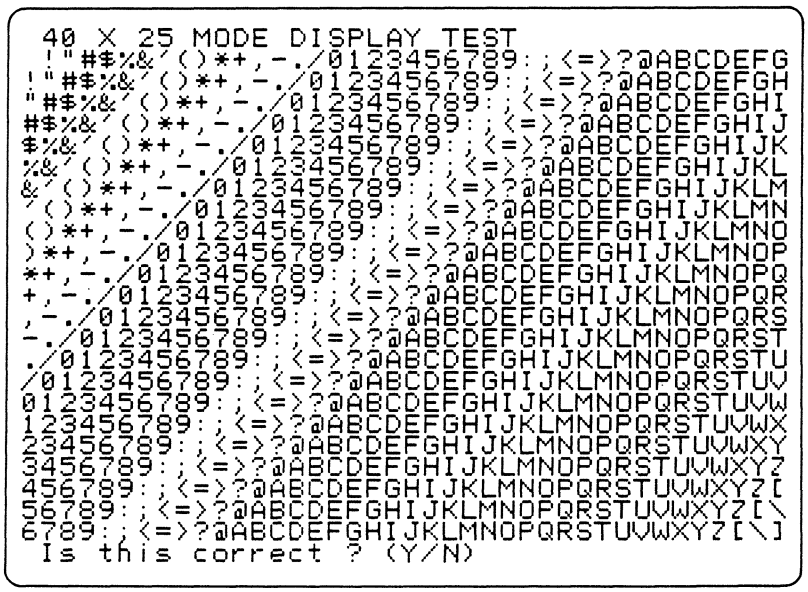


Figure 9-26 40x25 Mode Display Test

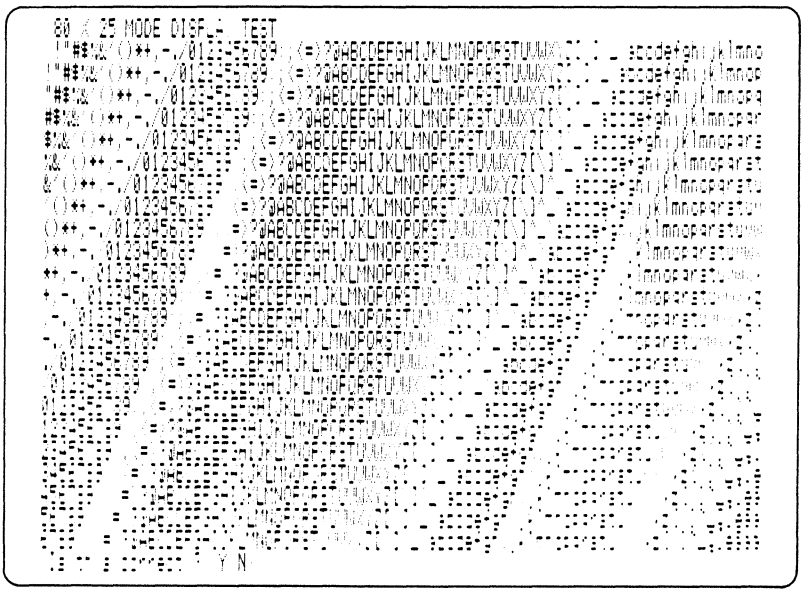


Figure 9-27 80x25 Mode Display Test

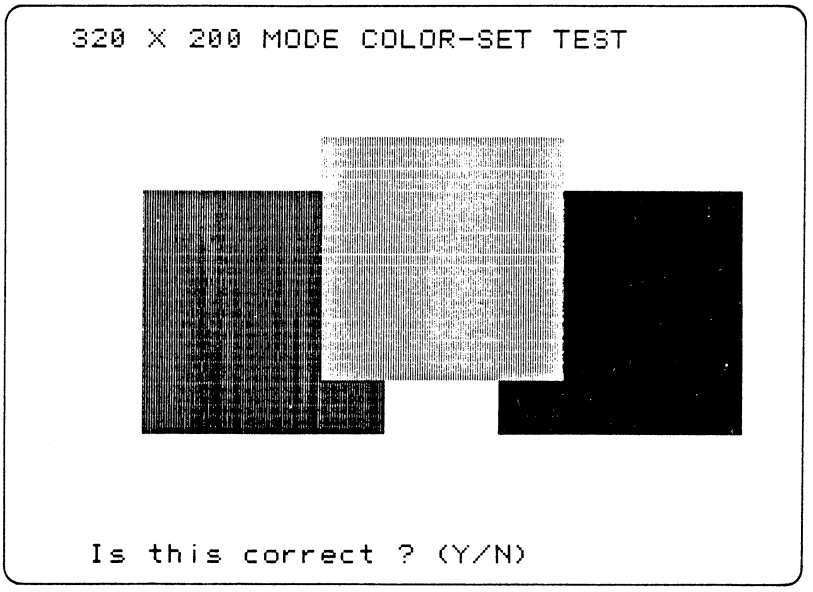


Figure 9-28 320x200 Graphic Display Test

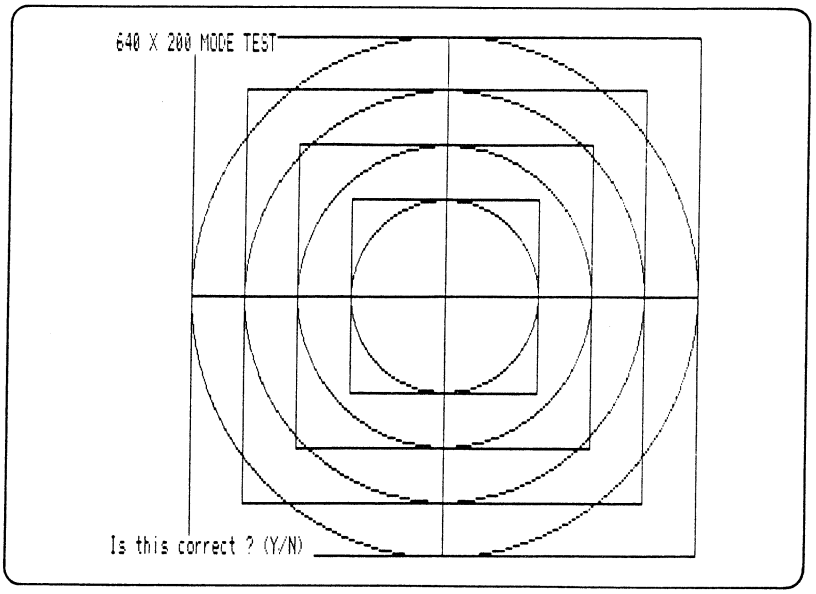


Figure 9-29 640x200 Graphic Display Test

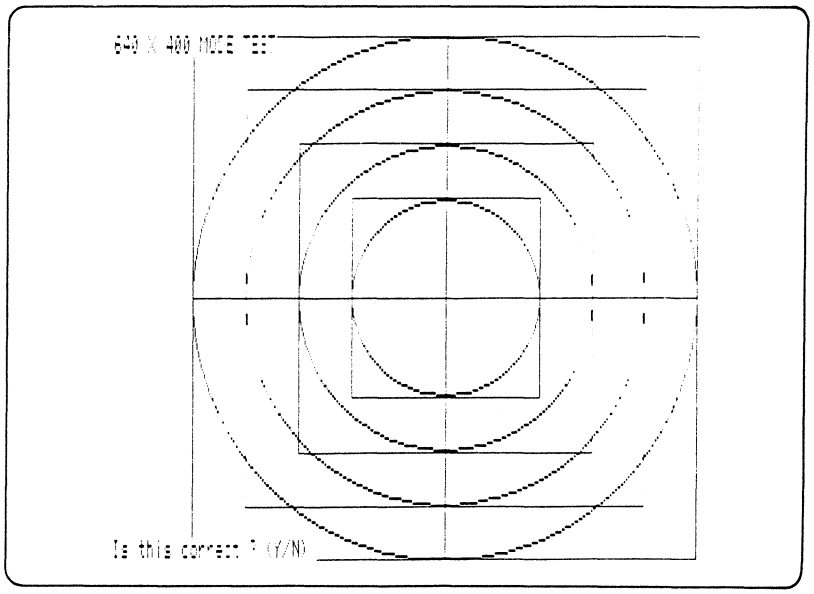
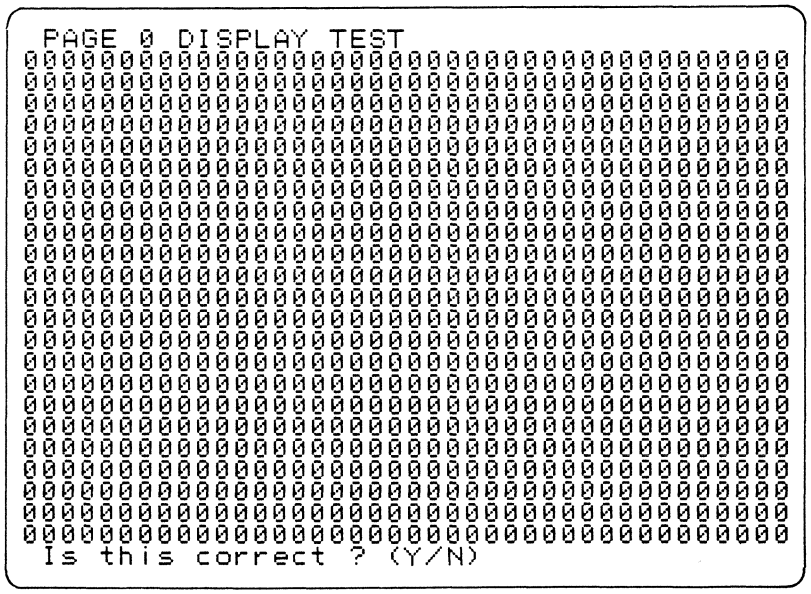


Figure 9-30 640x400 Graphic Display Test



PAGE 0 Display Test with all 0 Display
PAGE 1 Display Test with all 1 Display
PAGE 2 Display Test with all 2 Display
PAGE 3 Display Test with all 3 Display

Figure 9-31 Screen Paging Test

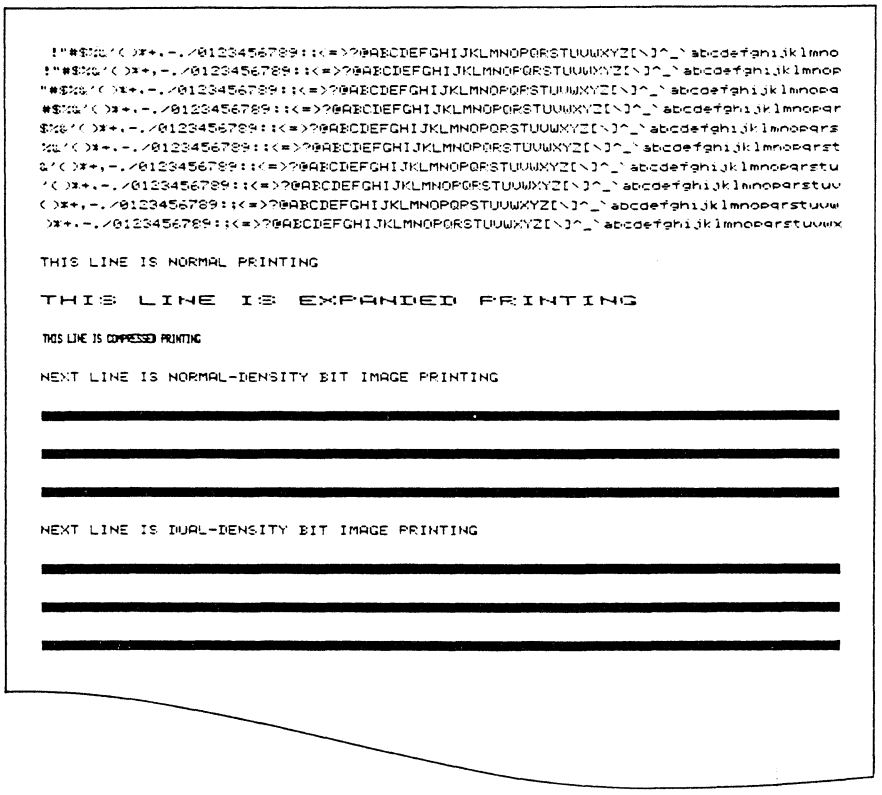


Figure 9-32 Parallel Port Test

9.5.6 Test automatically

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [2] [↵] into DIAGNOSTIC MENU.	ENTER THE NUMBER TO RUN THE TEST? __	
2	Key in the number of times you want the test to be repeated (up to a maximum of 99999) and press [↵] .		You will be asked to press various keys and to ensure that the devices are ready to be tested throughout the automatic test. Refer to the "TEST ALL DEVICES" section for details on the testing of each device. Note that the screen display may differ slightly because you don't need to press any keys to move from one test to the next. To terminate the automatic test before it is completed, press the [Break] key while holding down the [Cntrl] key. The screen should return to the diagnostic menu. If not, you may first have to respond to the current message on the screen.

When the instructions below appear on the display follow the instructions.

```
Attach the loop back plug to the connector.
Press any key when ready __
```

```
Insert scratch disk(s) in (all) drive(s)
and strike any key when ready
```

9.5.7 Change Menu

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [3] [↵] into DIAGNOSTIC MENU.	INSTALLED DEVICE(S) ARE 1. MAIN BOARD 2. xxx KB MEMORY 3. KEYBOARD 4. DISPLAY 5. PRINTER 6. SERIAL PORT 7. FLOPPY DISK 8. HARD DISK 9. LOCAL SPEAKER 10. CO-PROCESSOR Is this correct? (Y/N) __	If this is a list of the devices in the system, press y to return to the diagnostic menu. If not, press n.

DELETE

1	Press [n] .	Enter (D)elete or (A)dd? __	
2	Press [d] .	ENTER THE NUMBER OF THE DEVICE TO BE DELETED? __	If your system does not have all the devices listed, press d.
3	Press number key, [↵] .		Key in the number of the device on the list that is not in your system and press [↵] .

ADD

1	Press [n] .	Enter (D)elete or (A)dd? __	
2	Press [a] .	ENTER THE NUMBER OF THE DEVICE TO BE ADDED? __	If the list does not contain all the devices (including options) in your system, press a.
3	Press number key, [↵] .		You will see a list of devices on the screen. Key in the number of the device to be added to the list of the installed devices and press [↵] .

9.5.8 Error listing

Step	Test Procedures	CRT Displays or Printer Print Outs	
1	Type [4] [↵] into DIAGNOSTIC MENU.		If necessary, first exit from the SELECT DEVICES menu by pressing 16 and [↵] .

The screen will then display messages in the format shown in the following example:

```
ERROR LISTING

NUMBER   DEVICE                  EXECUTE   ERROR

  7    FLOPPY DISK                00001     00000

Press any key to continue or ESC to end _
```

Number of program executions and errors are also included in the above message, when a problem occurs.

If you want to see the details of Error Listing, press any key. The details of Error Listing will be displayed on the screen. However, the contents may differ depending on the cause of the problem.

If you want stop in the middle of the program, press the ESC key.

9.5.9 Error messages

When a problem is found, the following message is displayed along with details of the error:

```
**** ERROR ****
```

The details of the error message differ for each device as follows:

(1) Main Board Test

Error Message	Description
ROM CHECKSUM FAILED	The check sum for the BIOS ROM is not correct.
TIMER FAILED	Timer 8253-5 is not counting correctly.
DMAC FAILED	The memory refresh DMA failed.
PPI FAILED	The PPI (8255-5) did not read/write correctly.
PIC FAILED	An unexpected interrupt occurred in the interrupt controller or an interrupt was not correctly checked.
232C FAILED	The UART (8250) control read/write is not possible.
PRINTER I/F FAILED	Signals to the printer interface were not returned correctly.
CRTC FAILED	CRTC control read/write is not possible.

(2) Memory Test

ADDRESS xxxxx DATA xx1 xx2	Memory error occurred in address xxxxx. xx1 = Write Data xx2 = Read Data

(3) Printer Test (Parallel Port Test)

Error Message	Description
TIME OUT xx1 xx2 or STATUS xx1 xx2	xx1 = Last Output Data xx2 = Error Status (described below)

Meaning	Bit D7 6 5 4 3 2 1 D0
TIMEOUT	1
I/O ERROR	1
Printer is selected	1
Paper End	1
Acknowledge	1
Busy	0

(4) Serial Port Test

TIME-OUT Sd-data xx
Rcv-data xx
Status1 xx
Status2 xx
or
STATUS Sd-data xx
Rcv-data xx
Status1 xx
Status2 xx

Status1 byte (line status)

Meaning	Bit D7 D6 D5 D4 D3 D2 D1 D0
TIME OUT	1
Trans Shift Register is empty	1
Trans Holding Register is empty	1
Break detect	1
Framing error	1
Parity error	1
Overrun error	1
Data ready	1

Status2 byte (modem status)

Meaning	Bit D7 D6 D5 D4 D3 D2 D1 D0
Received line signal detect	1
Ring indicator	1
Data set ready	1
Clear to send	1
Delta rcv line signal detector	1
Trailing edge ring detector	1
Delta data set ready	1
Delta clear to send	1

(5) Floppy Disk Test

Diagnostic message consist of three parts, as shown in the following example:

```
RECORD NOT FOUND  Command 02 Track 00 Side 00 Sector 01
40020100000102
```

1. RECORD NOT FOUND --- Type of error

2. Command 02 Track 00 Side 00 Sector 01 --- Error mode and location

3. 40020100000102 --- Error status from the FD controller

① Type of Error

Error Message	Description
TIME OUT	Diagnostic processing not completed in time
FDC FAILED	Abnormal end for FD controller
CRC	"CRC error" detected at ID section or Data section
DMA BOUNDARY OVER	DMA transfer over 64KB
DMA OVERRUN	DMA transfer broken off halfway through
RECORD NOT FOUND	Designated track or sector not detected
WRITE PROTECT	Floppy disk write-protected
ADDRESS MARK NOT FOUND	Address mark not detected

② Error Mode and Location

Command	Abbreviation
In Read Command	02
In Write Command	03
In Verify Command (Error Status same as Read Command)	04

③ Error Status

The error status from the FD controller consists of seven parts, as shown in the following example:

40	02	01	00	00	01	02
ST0	ST1	ST2	T	H	S	N

ST0 -- Status byte 0

ST1 -- Status byte 1

ST2 -- Status byte 2

T -- Track number

H -- Head address

S -- Sector address

N -- Record sector length

Codes for the status bytes are shown in the next page.

④ In Read Command (02) and Verify Command (04)

Condition of Executing Ending		ST0	ST1	ST2
		D7 6 5 4 3 2 1 D0	D7 6 5 4 3 2 1 D0	D7 6 5 4 3 2 1 D0
Normal ending		0 0		
Not ready		0 1 1		
ID	IDAM isn't Detected	0 1	1	
	C doesn't correspond (not same as FFH)	0 1	1	1
	C doesn't correspond (same as FFH)	0 1	1	1
	H doesn't correspond	0 1	1	
	R doesn't correspond	0 1	1	
	N doesn't correspond	0 1	1	
	CRC doesn't correspond	0 1	1	
DATA	DAM isn't detected	0 1	1	1
	DDAM is detected	0 0		1
	CRC doesn't correspond	0 1	1	1
	Overrun	0 1	1	
Doesn't end at last sector		0 1	1	

⑤ In Write Command (03)

Condition of Executing Ending		ST0								ST1								ST2							
		D7	6	5	4	3	2	1	D0	D7	6	5	4	3	2	1	D0	D7	6	5	4	3	2	1	D0
Normal ending		0	0																						
Not ready		0	1			1																			
ID	IDAM isn't Detected	0	1													1									
	C doesn't correspond (not same as FFH)	0	1											1								1			
	C doesn't correspond (same as FFH)	0	1											1											1
	H doesn't correspond	0	1											1											
	R doesn't correspond	0	1											1											
	N doesn't correspond	0	1											1											
	CRC doesn't correspond	0	1									1													
DATA	Fault	0	1		1																				
	Overrun	0	1										1												
Doesn't end at last sector		0	1							1															
Write protected		0	1													1									

(6) Hard Disk Test

Message	Description
SENCE OPERATION FAILED	Sence operation failed
DATA COMPARE	Unexpected data was detected.
BUFFER RAM COMPARE	Unexpected data was detected in buffer ram area
UNDEFINED ERROR	Undefined error was detected.
TIME OUT	Diagnostic processing not completed in time.
SEEK	Seek processing not completed.
BAD CONTROLLER	Controller may be damaged.
ECC	"ECC Error" detected at ID section or Data section (unable correction).
BAD ECC	"ECC Error" detected at Data section, but corrected.
BAD TRACK	Designated track was formated with bad track flag.
DMA BOUNDARY OVER	DMA transfer over 64K bytes
INITIALIZE FAILED	Abnormal end of controller
RESET FAILED	Reset processing was failed.
RECORD NOT FOUND	Designated sector not detected.
ADDRESS MARK NOT FOUND	Address mark not found at ID section.
BAD COMMAND	Illegal command was detected.

Error Mode and Location

Command	Code
Reset Hard Disk controller	00
Read controller's buffer	0E
Write controller's buffer	0F
Test drive ready	10
Recalibrate the drive	11
Test controller's RAM	12
Test drive	13
Test controller	14
In read command	82
In write command	83
In seek command	8C
In compare command at controller's ram area	C1
In compare command at main ram area	C2

9.5.10 Exit

Step	Test Procedures	CRT Displays or Printer Print Outs	
	Type [5] [↵] into DIAGNOSTIC MENU.	Insert DOS diskette in drive A: and strike any key when ready.	DOS must then be reloaded before it can be used again. (This operation is equivalent to resetting the software.)

ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

II. LOGIC UNIT

1. SPECIFICATIONS

The CPU board and I/O board incorporate the MPU (microprocessor unit), and input/output device controllers and interfaces. The board logic circuits are:

CPU Board (PC board marking: PLSMX)

- o MPU (Microprocessor Unit)
- o RAM (Random Access Memory)

  1) Standard capacity: 256K bytes
  2) IC socket capacity: 256K bytes

  Total Max. 512K bytes

- o ROM (Read Only Memory): 16K bytes
- o Keyboard Interface
- o Interval Timer/Speaker Interface
- o System Switch ("DIP" Switch)
- o PDP Controller

I/O Board (PC board marking: PLSY)

- o FDD Controller
- o Parallel Port (Printer)
- o Serial Port (RS-232C/Current Loop)
- o Option Slots: 2 slots
- o Slot for HD Controller

(a) MPU

The computer uses an Intel 8088 MPU. The MPU clock frequency is 4.77 MHz.

(b) RAM

The standard RAM capacity is 256K bytes. The capacity can be increased to 512K bytes with optional RAM chips installed in the IC sockets on the printed circuit board.

(c) ROM

CPU board has 16K bytes of ROM. The ROM includes a self-test program that is executed automatically when the power is turned on. It also contains the ROM-BIOS (Basic Input/Output System).

(d) Keyboard Interface

Through this interface circuit, data is transferred serially from the keyboard to the MPU.

(e) Interval Timer/Speaker Interface

The CPU board contains a programmable counter circuit, which allows programming of an interval for the interval timer interrupt and a beep frequency.

The speaker is installed inside the system unit.

(f) System Switch (DIP Switch)

The CPU board has a 4-circuit DIP switch which establishes circuit operating conditions and program branch conditions.

(g) PDP Controller

The computer has a flat PDP (Plasma Display Panel) on its system unit.

The PDP controller controls the PDP display functions.

The PDP controller functions as a color display adapter, with its MC68B45P LSI working as a CRT controller (CTRC).

The PDP controller includes a 32K-byte video RAM.

(h) FDD Controller

A μPD765AC control LSI (FDC) in the I/O board controls up to two FDDs.

(i) Parallel Port

The parallel port in the I/O board controls the printer. It is Centronics compatible.

(j) HD Controller Slot

The I/O board has a edge connector for HD controller. In the HD version, an HD controller is installed to this connector.

(k) Serial Port

The serial port in the I/O board is used for communication with external device.

The serial port employs an INS8250 control LSI (UART) and is capable of communicating with an external device through either the RS-232C or current loop interface.

(ℓ) Option Slots

The I/O board has two option slots. Both are IBM-PC compatible; "13" option board for either an IBM-PC or IBM-XT can be connected.

2. APPEARANCE

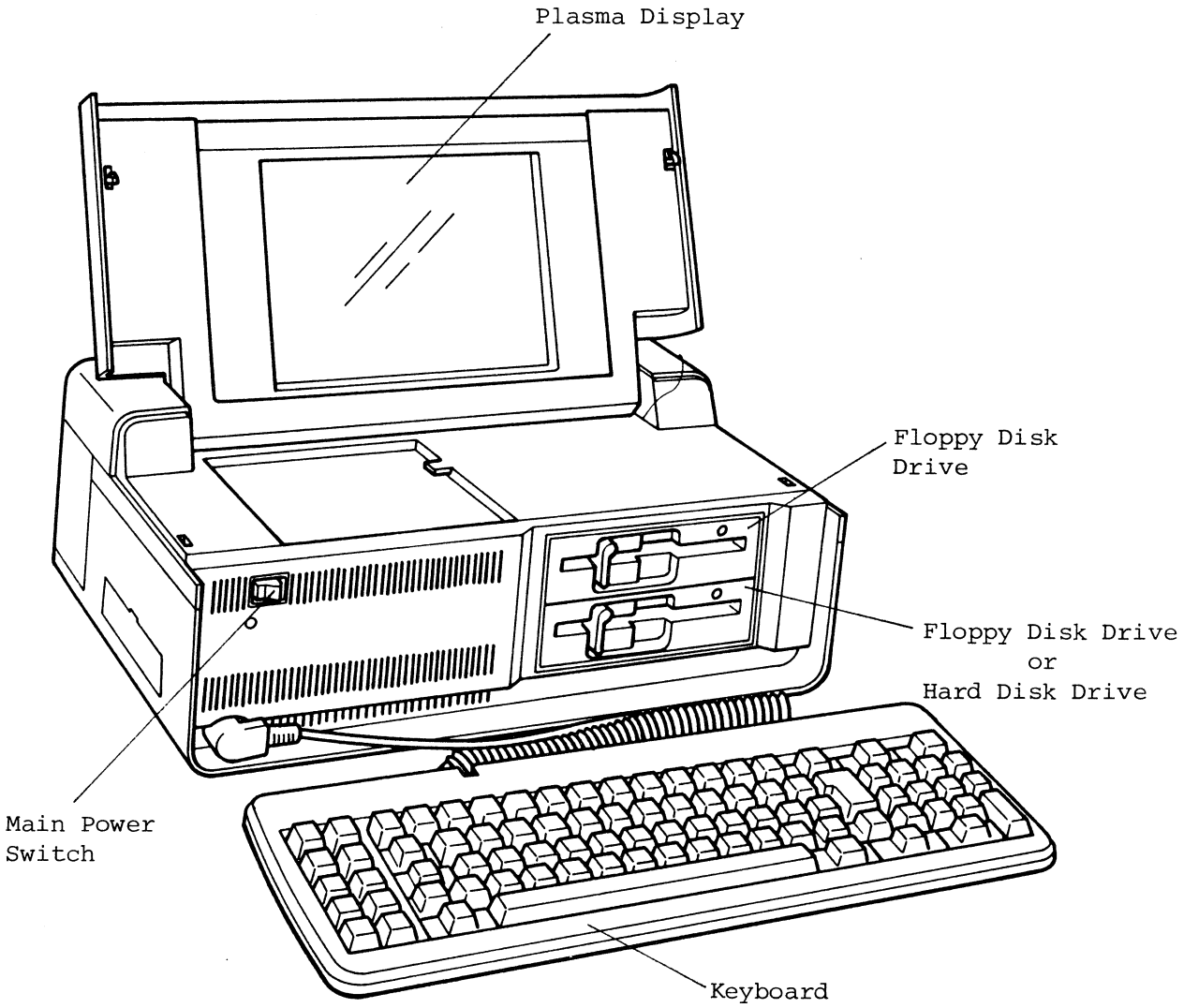


Figure 2-1

The system unit consists of a logic unit, two FDDs (or one FDD and one HDD), power supply unit, fan, and a speaker.

The CPU board is installed parallel to the bottom of the unit.

The I/O board and the FDDs are installing over the CPU board, the I/O board to the left and the FDD to the right.

3. BLOCK DIAGRAM

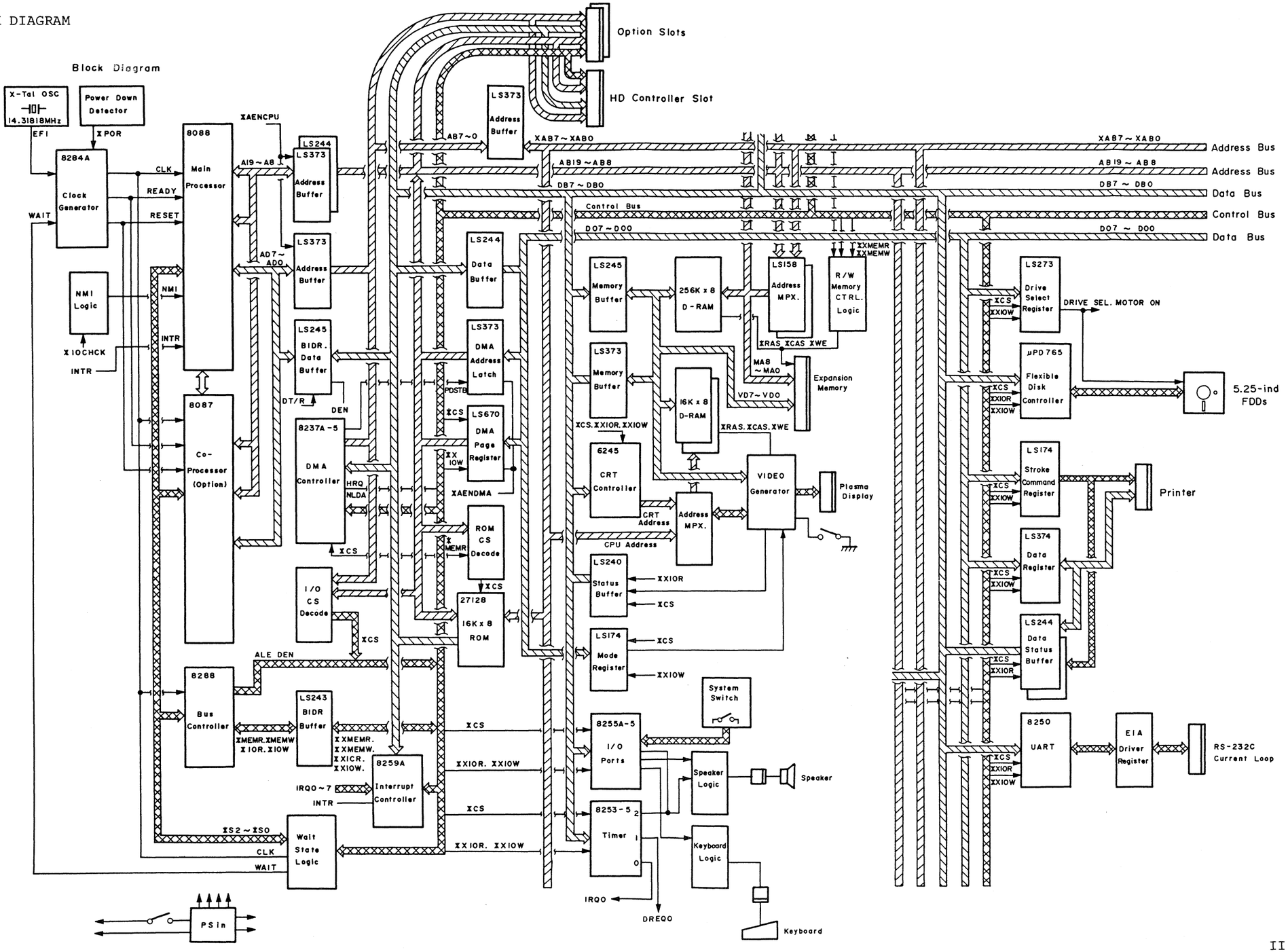


Figure 3-1

4. MEMORY USAGE

4.1 Memory Map

The microprocessor 8088 can address up to 1M bytes of memory space.

Standard memory configuration for the computer is: 256K-bytes RAM, 32K-bytes video RAM, and 16K-bytes ROM. This minimum standard memory is called the 256K-bytes system.

Memory can be increased to 512K bytes with optional 256K RAM chips inserted in the IC sockets on the CPU board. This is called the 512K-bytes system.

Memory can be increased further to 640K bytes with an optional 128K RAM board (for PC or XT) inserted into the option slot.

The 32K-bytes video RAM is the display memory. Character codes and graphic patterns in the video RAM are read out with PDP scanning timing and displayed on the plasma display.

A 16K-bytes ROM (equivalent to the Intel 27128) is standard in the CPU board. This ROM stores both a self diagnostic program, which functions when the power is turned on, and part of the BIOS (Basic Input Output System).

Figure 4-1 shows the memory map both of the 256K-bytes and 512K-bytes systems.

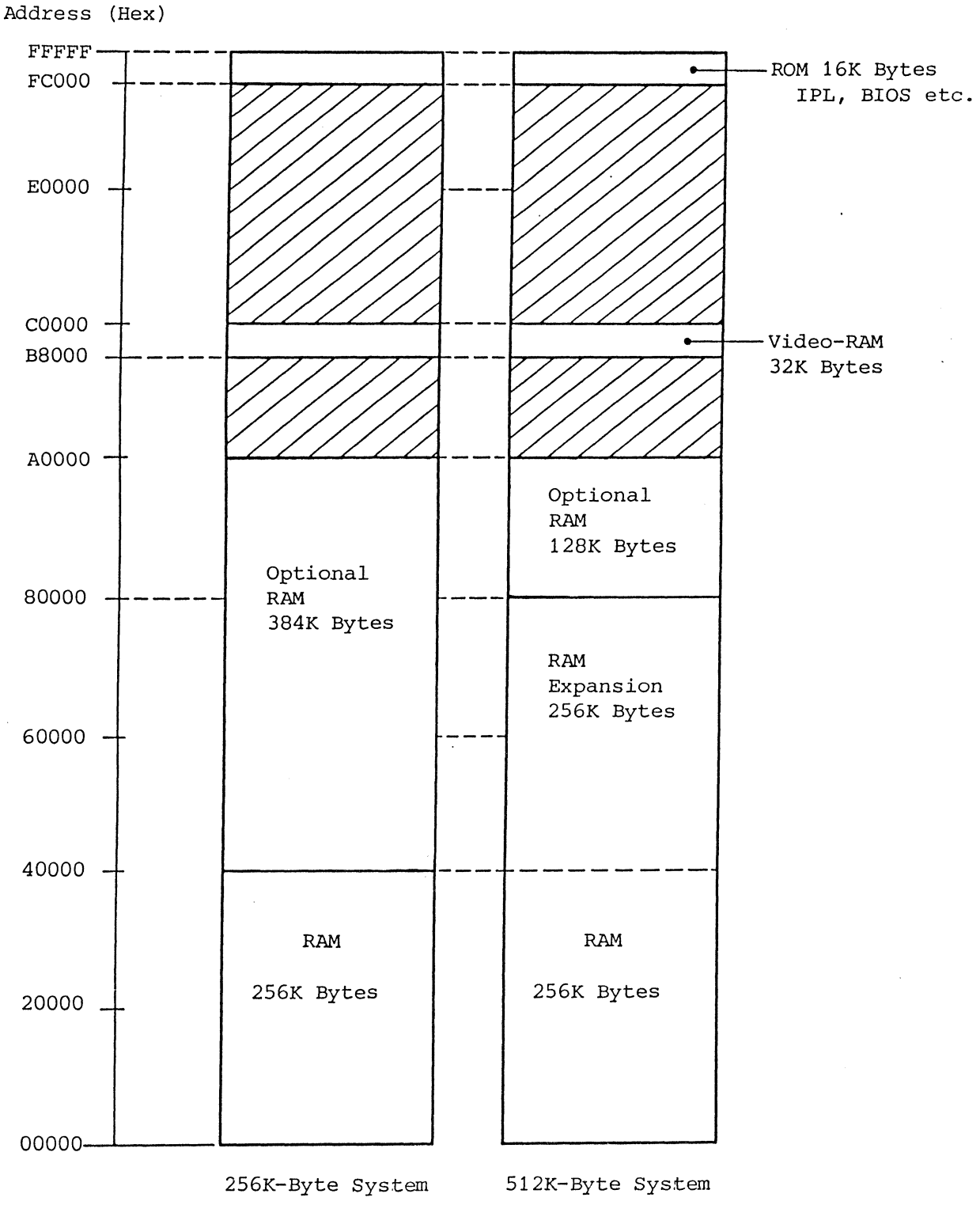


Figure 4-1 System Memory Map

4.2 Display and Video RAM Construction

4.2.1 Basic operation and display modes

The PDP controller employs an MC68B45P as a control LSI (CRTC). Its primary function is a color/graphic display adapter.

There are five display modes: 40x25 Text, 80x25 Text, 320x200 Graphics, 640x200 Graphics, and 640x400 Graphics. A mode can be selected by setting the corresponding bit of the mode resister with a software instruction. The video RAM usage varies with the display mode.

Display modes are listed in Table 4-1.

Table 4-1 Display Modes

Display Mode		No. of Display Memory Pages	Display	Character Box
TEXT	40 x 25	8	Attribute . Blink . Non-display . Normal . Reverse . Intensity	8 x 16
	80 x 25	4		8 x 16
GRA-PHICS	320 x 200	1	4 dots/pixel (4 gradations)	8 x 8
	640 x 200	1	2 dots/pixel	8 x 8
	640 x 400	1	1 dot/pixel	8 x 8

The video RAM is in an address space apart from that of the MPU RAM. A 32K-byte RAM is incorporated in the PDP controller as a dedicated display memory. Figure 4-2 outlines a block diagram of the PDP controller.

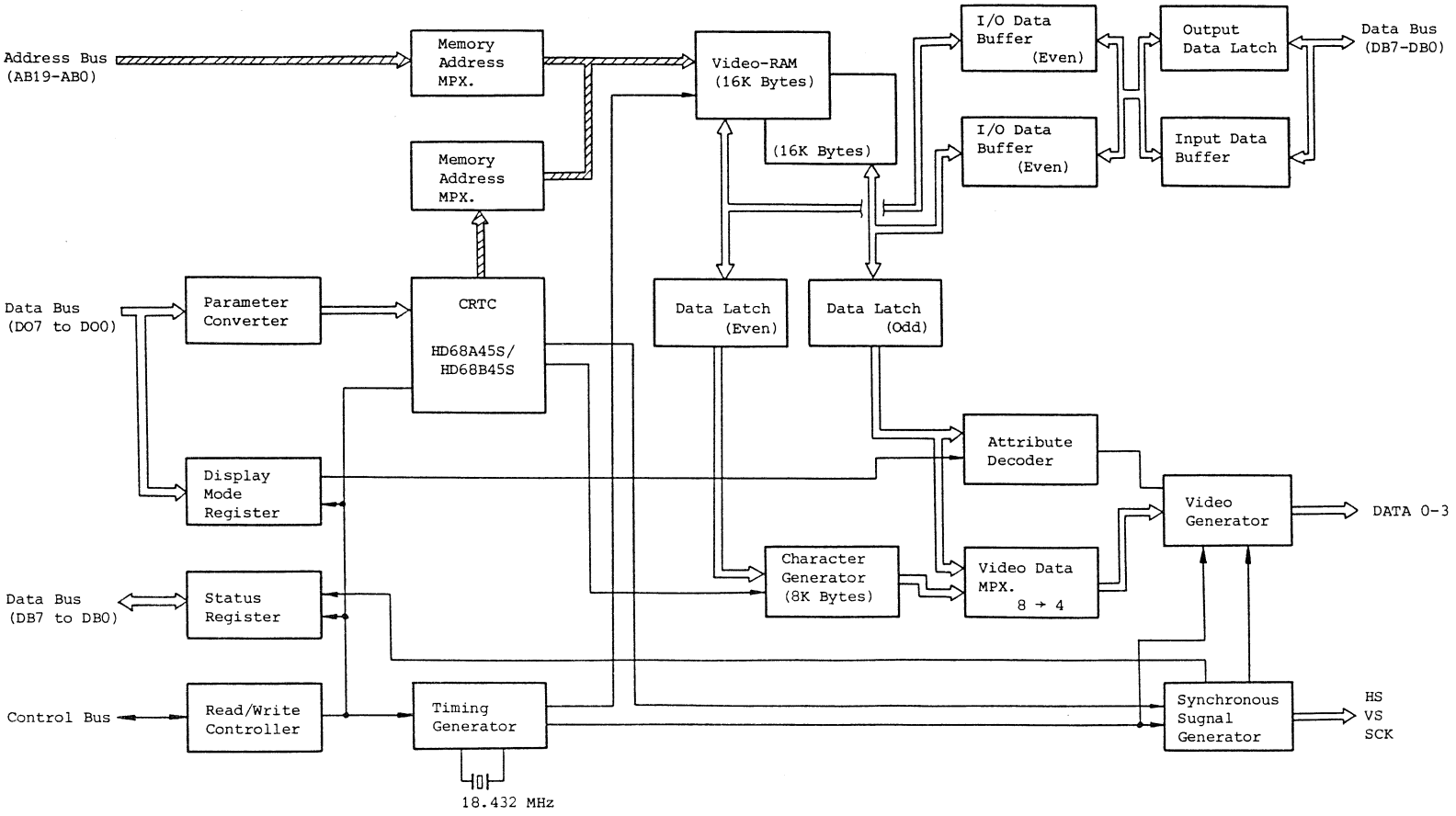


Figure 4-2 PDP Controller Block Diagram

The SYNC and address signals output by the CRTC refresh the PDP display. The CRTC outputs screen addresses (CMA13 to CMA0) and raster addresses (RA3 to RA0) to show positions to be displayed on the screen. The video RAM contents are accessed with these addresses to read display data, which is converted into video signals in the PDP interface for display on the PDP.

The data from the video RAM is read in two-byte units. In the text display mode, data corresponds to display character and attribute codes, while in the graphic display mode, data corresponds directly to graphic display dots.

The character generator ROM is accessed and display dots corresponding to display character codes and raster addresses are obtained in the text display mode to convert display character codes into display dots. Display dots are further divided into 1-digit (4-bit) units and are input to the video generator, which outputs these display dots as video signals to the PDP, after adding qualifications such as attributes and color designation.

The MPU writes in or reads from the video RAM by refreshing the display while the video RAM is not accessed, i.e., is idling.

The PDP controller outputs a WAIT signal to hold the MPU static while the video RAM has idle time, in case the MPU accesses the video RAM. The video RAM is accessed b switching the video RAM address from the CRTC to an MPU address with the address multiplexer when the video RAM is idle. The output of the WAIT signal to the MPU is stopped simultaneously to end video RAM accessing by the MPU.

4.2.2 Video RAM configuration and display dots

The PDP controller has a 32K-byte video RAM for a dedicated display memory.

The video RAM has been allocated addresses for 32K bytes, B8000 (HEX) to BFFFF (HEX).

The internal configuration of the video RAM varies with the display mode.

Figure 4-3 shows a video RAM configuration.

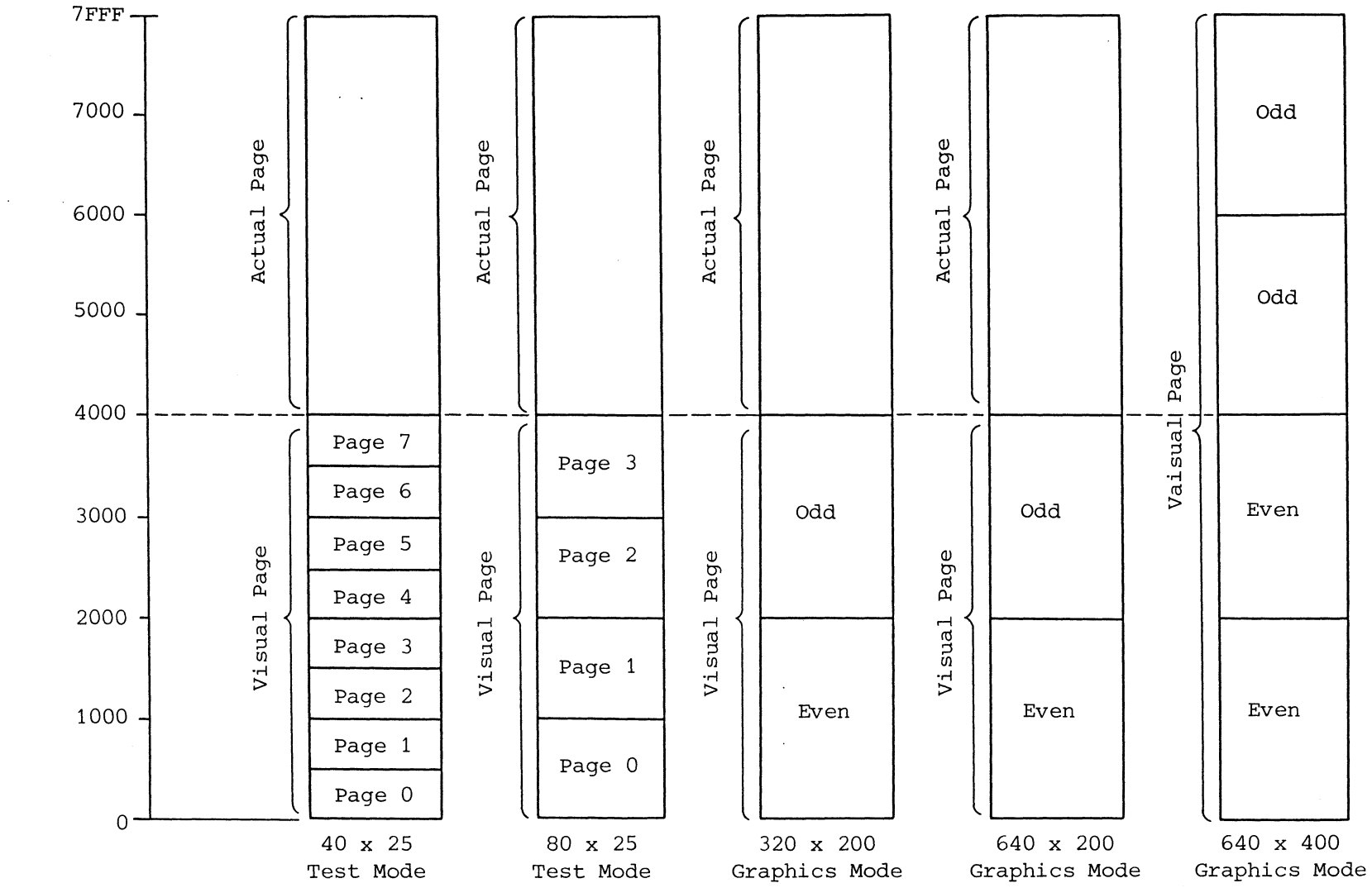


Figure 4-3 Video RAM Configuration

(a) 40x25 or 80x25 text mode

In the text display mode, character codes to be displayed are stored in the even addresses of the video RAM, attribute codes are stored in the odd addresses.

Figure 4-4 shows a video RAM configuration in the text mode.

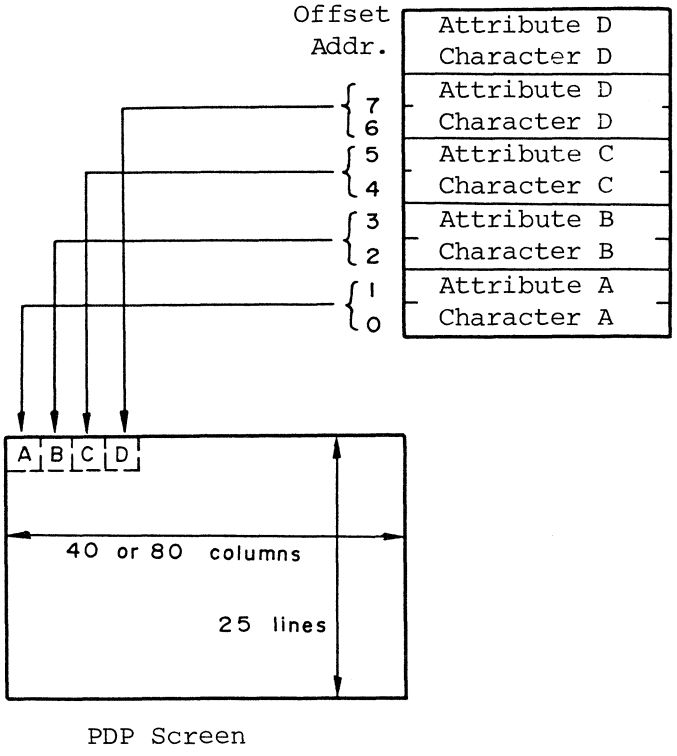
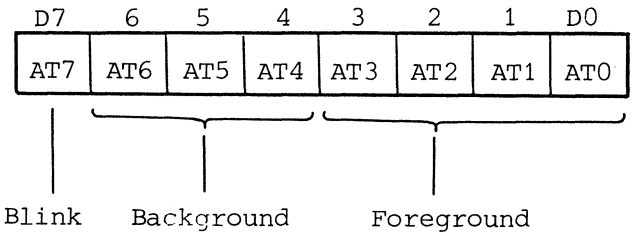


Figure 4-4 Video RAM Configuration in Text Mode

Figure 4-5 shows an attribute code in the text mode.



Attribute Code

AT7: Blinking
AT6: (B) Red
AT5: (B) Green
AT4: (B) Blue
AT3: (F) Intensity
AT2: (F) Red
AT1: (F) Green
AT0: (F) Blue

Back-ground & Blink Attribute \ Foreground Attribute					0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	AT3
					0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	AT2
					0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	AT1
					0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	AT0
Non-Blink or Blink (Turn On)	1	0	0	0	/	Ⓤ	—	—	—	—	—	—	—	Ⓤ	—	—	—	—	—	—	
	1	0	0	1	R	/	—	—	—	—	—	—	R	—	—	—	—	—	—	—	
	1	0	1	0	R	—	/	—	—	—	—	—	R	—	—	—	—	—	—	—	
	1	0	1	1	R	—	—	/	—	—	—	—	R	—	—	—	—	—	—	—	
	1	1	0	0	R	—	—	—	/	—	—	—	R	—	—	—	—	—	—	—	
	1	1	0	1	R	—	—	—	—	/	—	—	R	—	—	—	—	—	—	—	
	1	1	1	0	R	—	—	—	—	—	/	—	R	—	—	—	—	—	—	—	
	1	1	1	1	R	R	R	R	R	R	R	F	R	R	R	R	R	R	R	F	
Blink (Turn Off)	0	0	0	0	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	
	0	0	0	1	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	0	1	0	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	0	1	1	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	1	0	0	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	1	0	1	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	1	1	0	F	/	/	/	/	/	/	/	F	/	/	/	/	/	/	/	
	0	1	1	1	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	
	*	AT6	AT5	AT4	Single Dot Font								Boid Dot Font								

$$* = \overline{(AT7) \cdot (\text{Enable Blink}) \cdot (\text{Blinking Pulse}) \cdot (\overline{\text{Cursor}})}$$

Remarks:

- \- Normal
- R Reverse
- / Non-display or turned off
- U Normal (with underline when change the J11 short pin setting)
- F Full dots of character box illuminated

AT7	Blinking	
AT6	Background	Red color
AT5	Background	Green color
AT4	Background	Blue color
AT3	Foreground	Intensity
AT2	Foreground	Red color
AT1	Foreground	Green color
AT0	Foreground	Blue color

Figure 4-5 Attribute Codes in Text Mode

(b) 320x200 graphics mode

In the 320x200 graphics display mode, the video RAM stores graphic display dots, two bits per dot. Figure 4-6 shows the video RAM configuration in this mode.

One display dot in the video RAM corresponds to four dots on the PDP screen, and display dot color designation is expressed by the brightness of light and shade on the PDP screen.

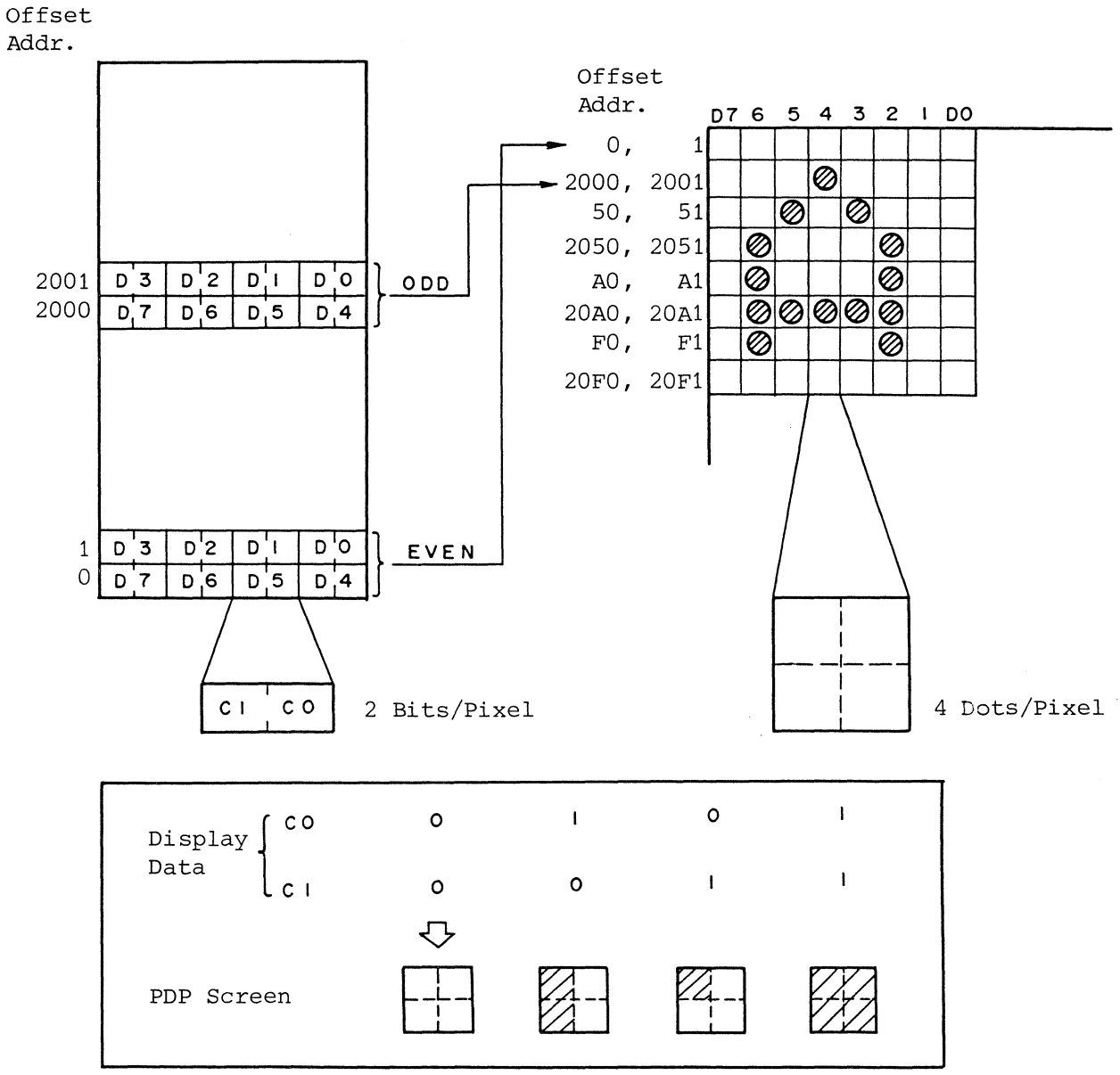


Figure 4-6 Video RAM Configuration in 320x200 Graphics Mode

(c) 640x200 graphics mode

Figure 4-7 shows a video RAM configuration in the 640x200 graphics display mode.

One display dot (one pixel) is shown as two dots on the PDP screen in this mode.

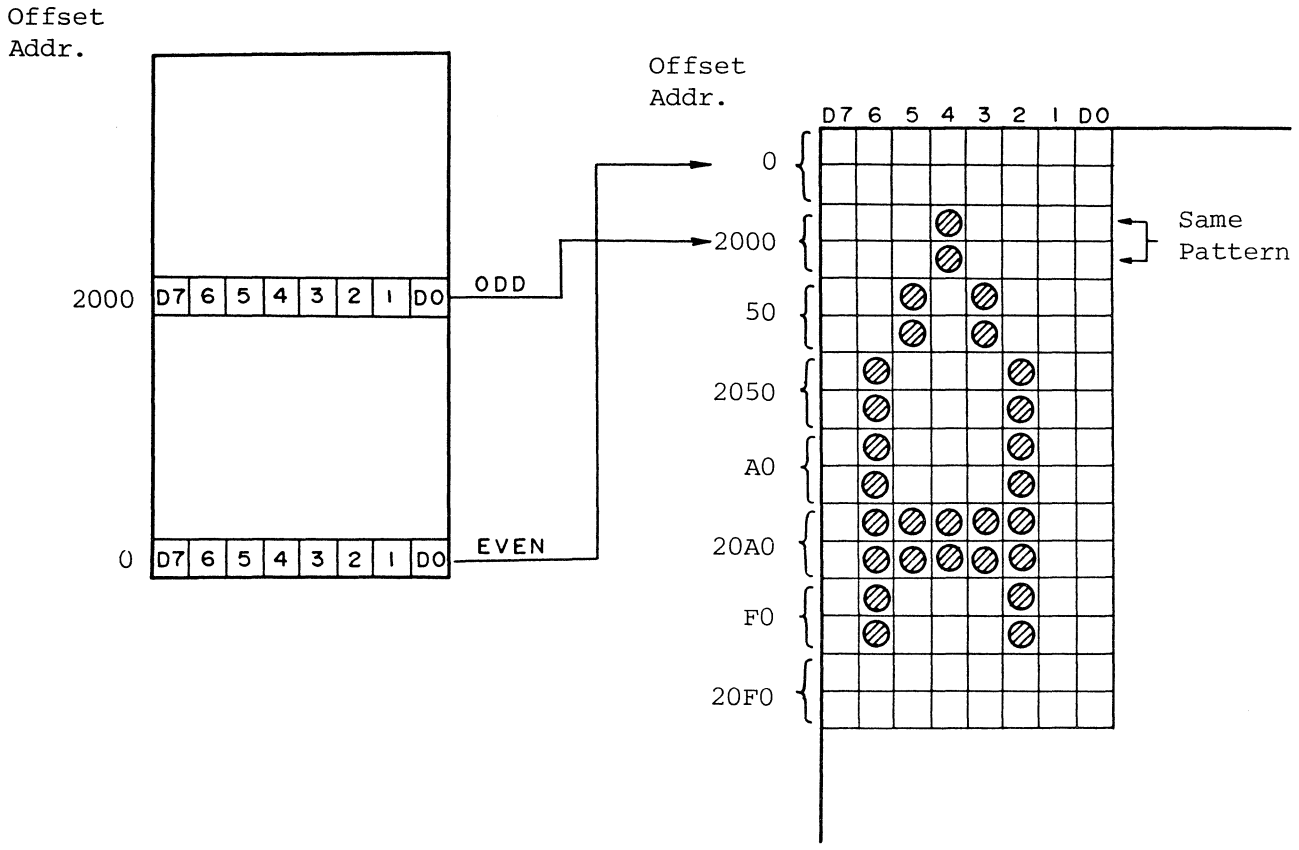


Figure 4-7 Video RAM Configuration in 640x200 Graphics Mode

(d) 640x400 graphics mode

Figure 4-8 shows a video RAM configuration in the 640x400 graphics display mode.

It is only in this display mode that all 32K bytes contained in this video RAM become a visual page.

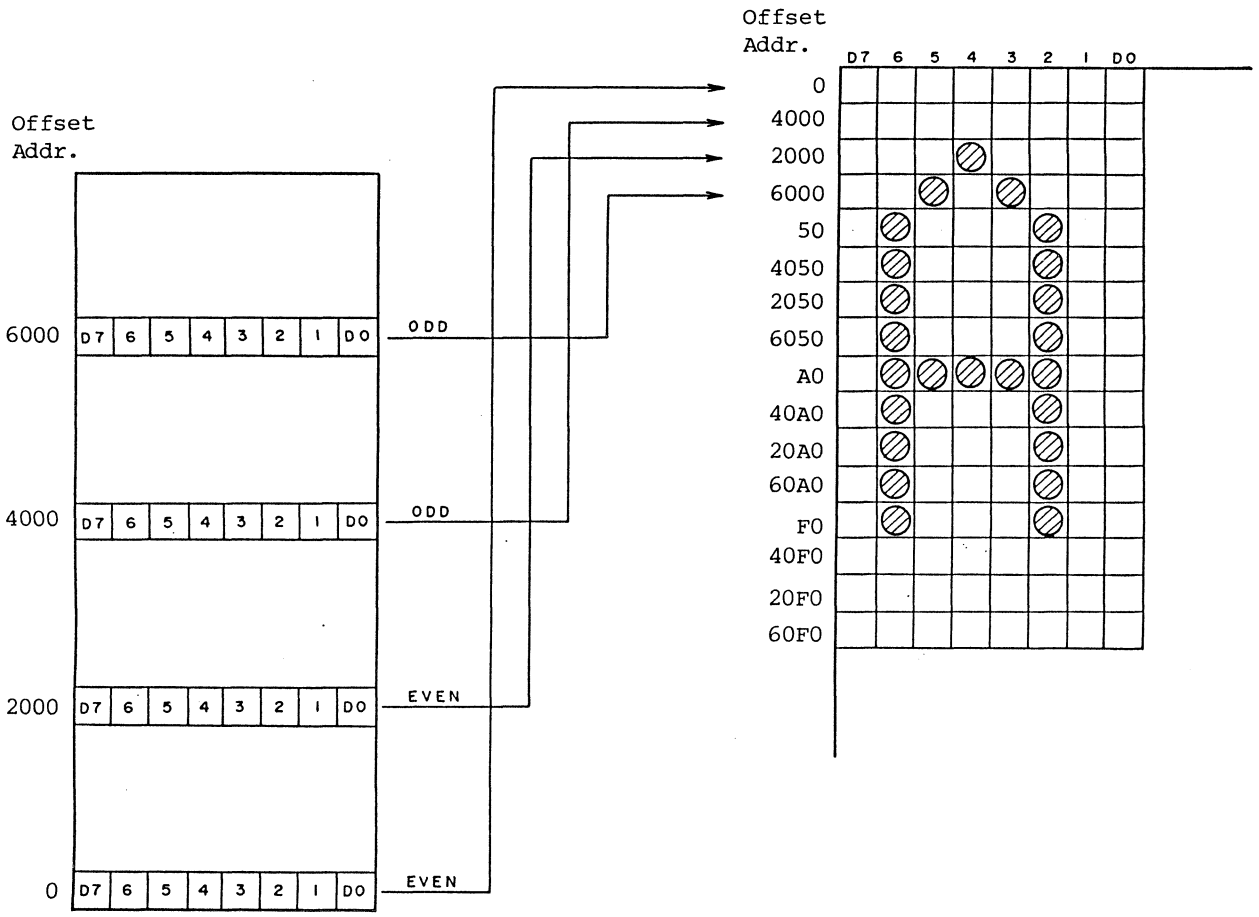


Figure 4-8 Video RAM Configuration in 640x400 Graphics Mode

5. THEORY OF OPERATION

5.1 General

The logic unit actually consists of two boards, the CPU board and the I/O board.

The nerve center of the logic unit has a microprocessor (8088) and DMA controller (8237A-5). The logic unit contains a controller for the memory and principal input and output equipment.

The principal functions of the logic unit are:

[CPU board]

① Accessing 16K bytes BIOS program ROM

② Control of standard 256K bytes, maximum 512K bytes, RAM

③ Direct memory access (DMA) between memory and I/O

④ Interrupt control of eight interrupt levels

⑤ Peripheral I/O interface

- o PDP controller
- o Keyboard interface
- o Interval timer/Speaker interface
- o "DIP" switch

[I/O board]

⑥ Peripheral I/O interface

- o FDD controller
- o Parallel port (printer)
- o Serial port (RS-232C)
- o Two option slots
- o Slots for HD controller board

5.2 System Resetting and System Clock Generation Circuits

(a) System reset circuit

Two reset signals automatically reset when the power is turned on.

(1) System reset signal (RESET)

The leading voltage edge of the +5 V power is integrated by register R9 and capacitor C17. Its level is detected by the 8284A circuit, and is output as a reset signal.

The duration of the reset signal at this time is approximately 400 ms to 1.3 sec.

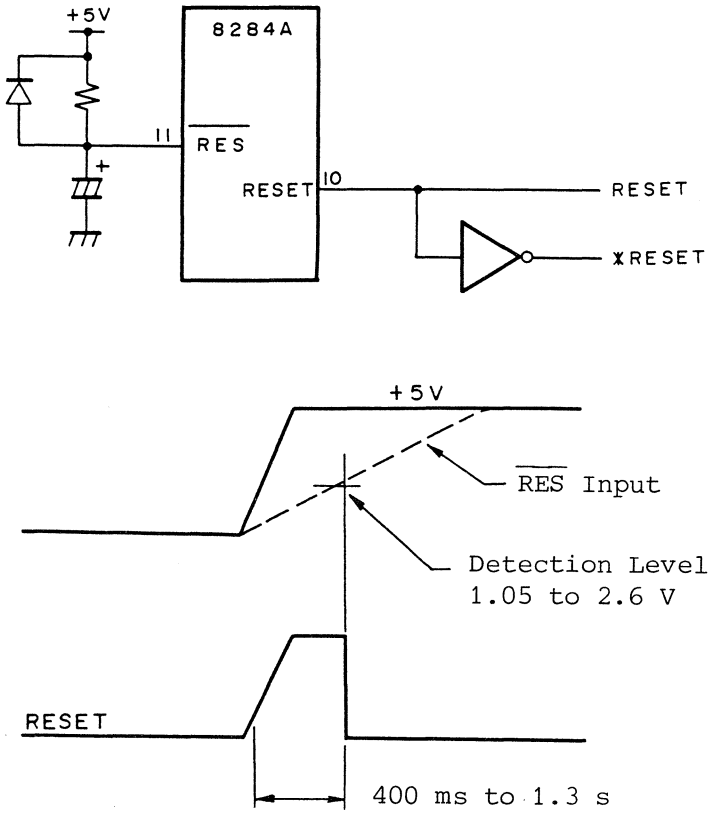


Figure 5-1 System Resetting Circuit and Operation

(2) Anti-malfunction reset signal (*POR)

The *POR signal is produced by a +5 V power voltage detection device (PST518A) to prevent circuit malfunctions when power is turned on or off.

The leading and falling edge voltages of the +5 V voltage are detected by 4.2 ±0.2 V.

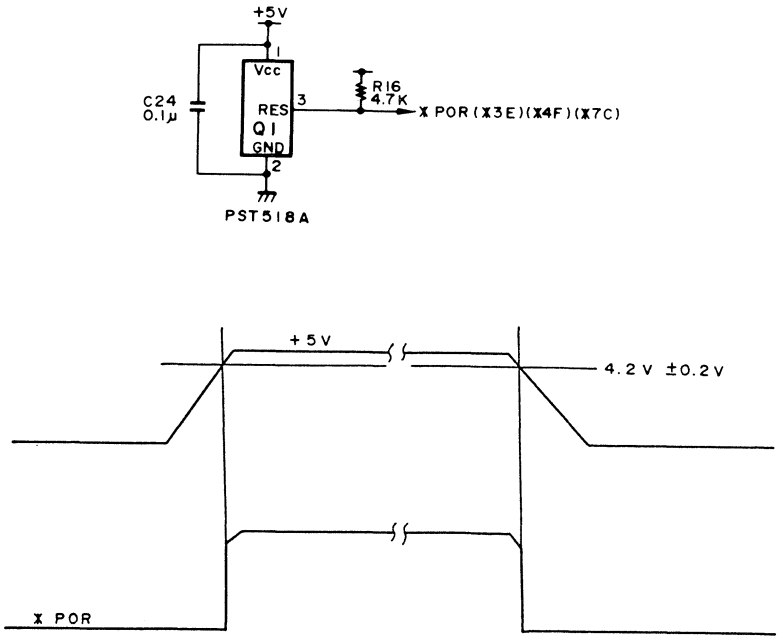


Figure 5-2 Anti-Malfunction Reset Circuit and Operation

The *POR signal is used only with the *WRITE GATE disable circuit (inside the FD controller) and the chip select circuit of the real time clock chip.

(b) System clock generation circuit

A quartz oscillation module is used for the clock oscillation source.

The oscillation frequency is 14.31818 MHz. The original oscillation frequency is demultiplied to produce MPU and other clock frequencies. Demultiplication is performed by 8284A and a demultiplier circuit.

- o Original oscillation frequency 14.31818 MHz
- o 1/3 demultiplication (8284A) 4.77 MHz
  CLK - microprocessor clock
- o 1/6 demultiplication (8284A) 2.3814 MHz
  PCLK - I/O control clock
- o 1/12 demultiplication 1.1932 MHz
  SCLK - Timer clock

A 4.77-MHz clock DCLK with a duty cycle of approximately 50% is produced from the microprocessor clock (CLK) using a delay device (LS31) for DMAC.

- o 1/3 demultiplication (50% duty cycle) 4.77 MHz
  DCLK - DMAC clock

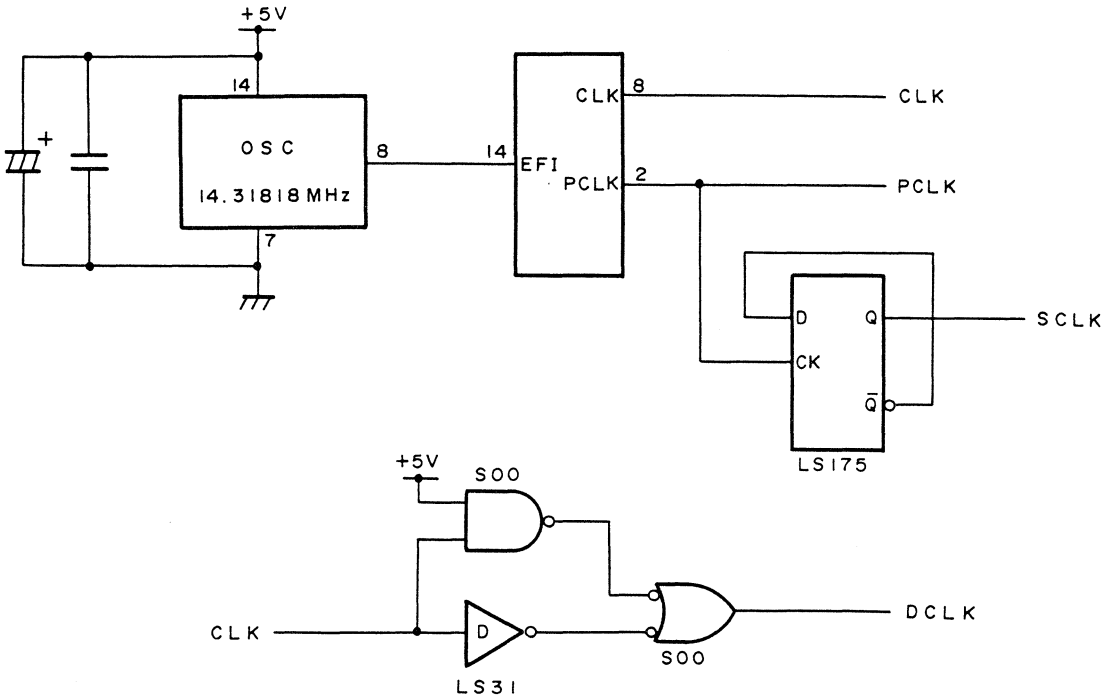


Figure 5-3 System Clock Generation Circuit

5.3 CPU

This system uses a 8088 microprocessor (MPU).

The 8088 has two operation modes -- minimum and maximum. This system uses the 8088 in the maximum mode, and operates the MPU clock at 4.77 MHz.

For details, see the data sheet attached to this manual.

5.4 Microprocessor Peripheral Circuits

Peripheral circuits, located in the periphery of he MPU 8088, are the MPU bus controller, address latch circuit, data bus circuit, and wait state generation circuit.

(a) MPU bus controller

A MPU bus controller, which generates MPU bus control signals, is required to operate the MPU 8088 in the maximum mode. This system uses the 8288 as the MPU bus controller.

The MPU bus controller refers to the control status signals (*S2 to *S0) output by the MPU, and produces the following control signals.

- o ALE ..... Address latch enable signal (ALE)
- o DEN ..... Data enable signal (DEN)
- o DT/$\overline{R}$ .... Data transfer direction control signal (DT/$\overline{R}$)
- o *MEMW ... Memory write signal ($\overline{AMWC}$)
- o *MWTC ... Memory write timing signal ($\overline{MWTC}$)
- o *MEMR ... Memory read signal ($\overline{MRDC}$)
- o *IOW .... I/O write signal ($\overline{AIOWC}$)
- o *IOR .... I/O read signal ($\overline{IORC}$)
- o *INTA ... Interrupt acknowledge signal ($\overline{INTA}$)

The MCE/$\overline{PDEN}$ and $\overline{IOWC}$ signals output by the 8288 are not used by this system.

In the DMA cycle, the MPU bus controller sets up the command signals *MEMW, *MWTC, *MEMR, *IOW, *IOR, and *INTA in a high impedance state and changes the DEN signals to inactive (LOW) with the *AEN and *AENCPU input signals.

(b) Address and data buses

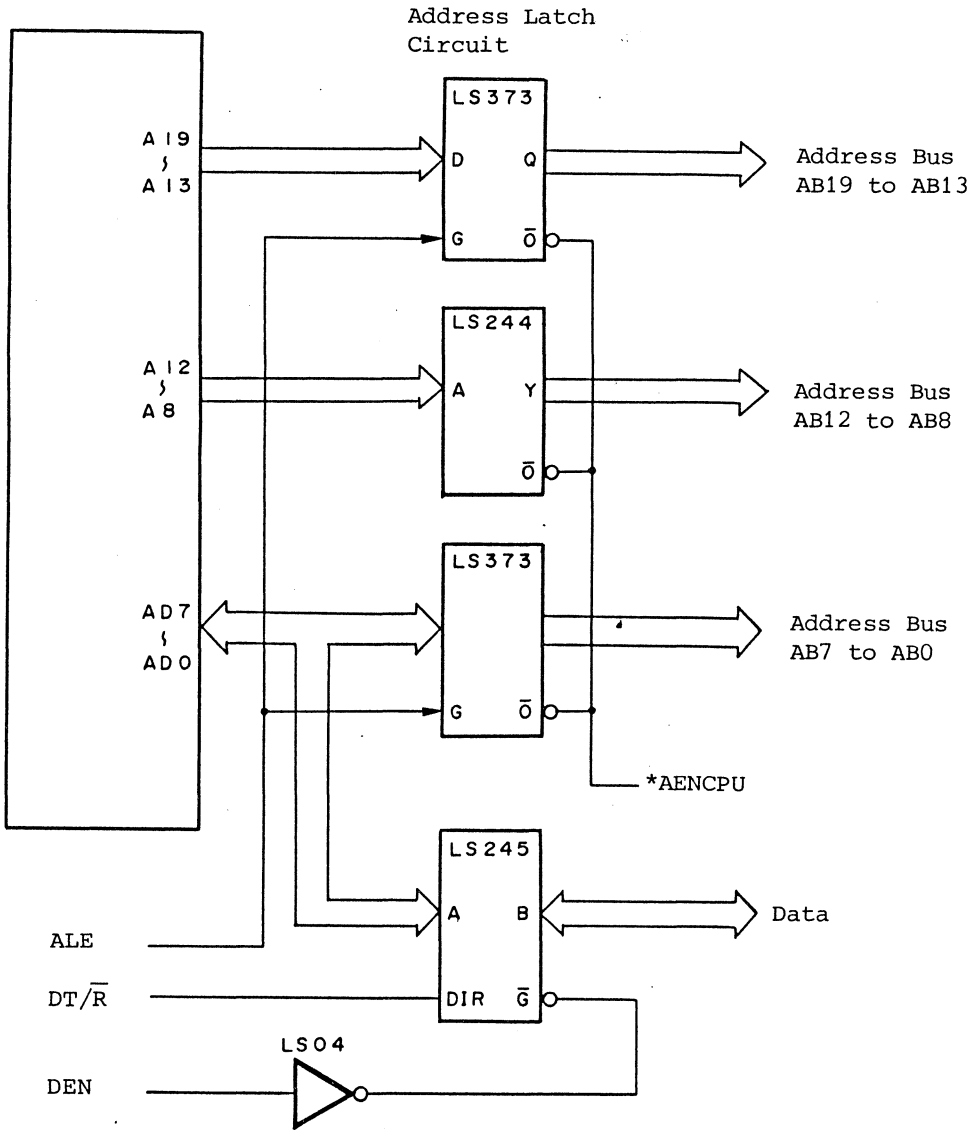


Figure 5-4 Address and Data Buses

Of address bus lines AB0 to AB19, AB0 to AB7 (eight bits) and AB13 to AB19 (seven bits) are fetched and output by the address latch enable signal (ALE), which is output by the MPU bus controller. Bits AB8 to AB12 are output via the bus amplifier. AB13 to AB15 need not be latched; in this circuit, however, they pass through an address latch circuit.

In DMA operation, the level of the *AENCPU signal goes HIGH, which in turn makes all address bus lines high impedance.

Two types of data buses are provided to increase fan-out: bi-directional and output-only data buses.

The bi-directional data bus is connected to I/O and memory for which both input and output operations occur. The DT/R and DEN signals output from the MPU bus controller control their directions and output gates.

The output-only data bus is connected to an I/O to which only I/O write occurs. The MPU cannot read data through this bus.

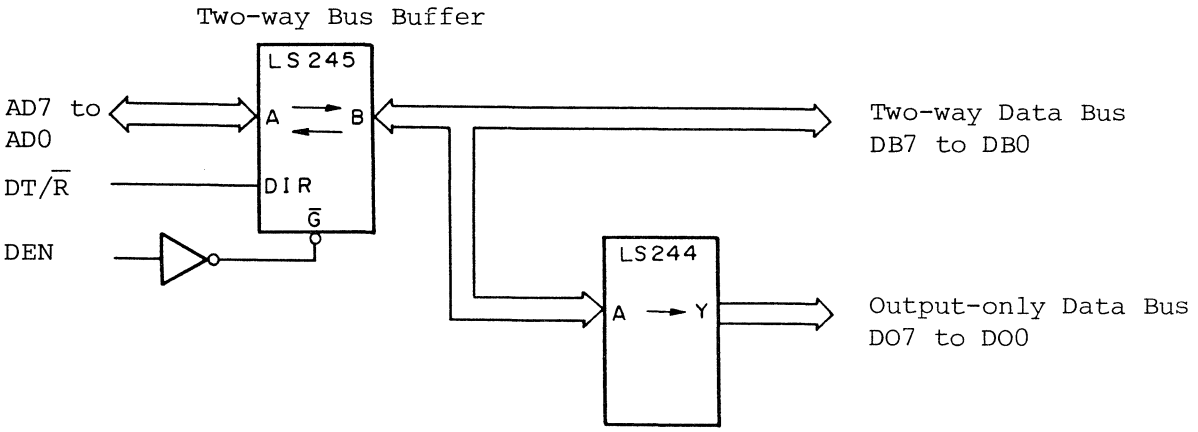


Figure 5-5 Block Diagram of Data Buses

The lower eight bits of the address bus are also connected via a bus buffer for the sake of fan-out, creating XAB7-XAB0.

(c) Wait state generation circuit

The wait state generation circuit has two functions: it generates wait cycles for the MPU, and it adjusts timing of the command signals *MEMR, *MEMW, *IOR, and *IOW, which are output from the MPU bus controller.

The timing of the command signals output from the MPU to the control LSI of a peripheral device has to be adjusted. When an I/O instruction is issued, therefore, the system generates two signals, *PADVNC and *ADVNC, adjusts their timing in the two-way buffer, and generates signals *XMEMR, *XMEMW, *XIOW, and *XIOR.

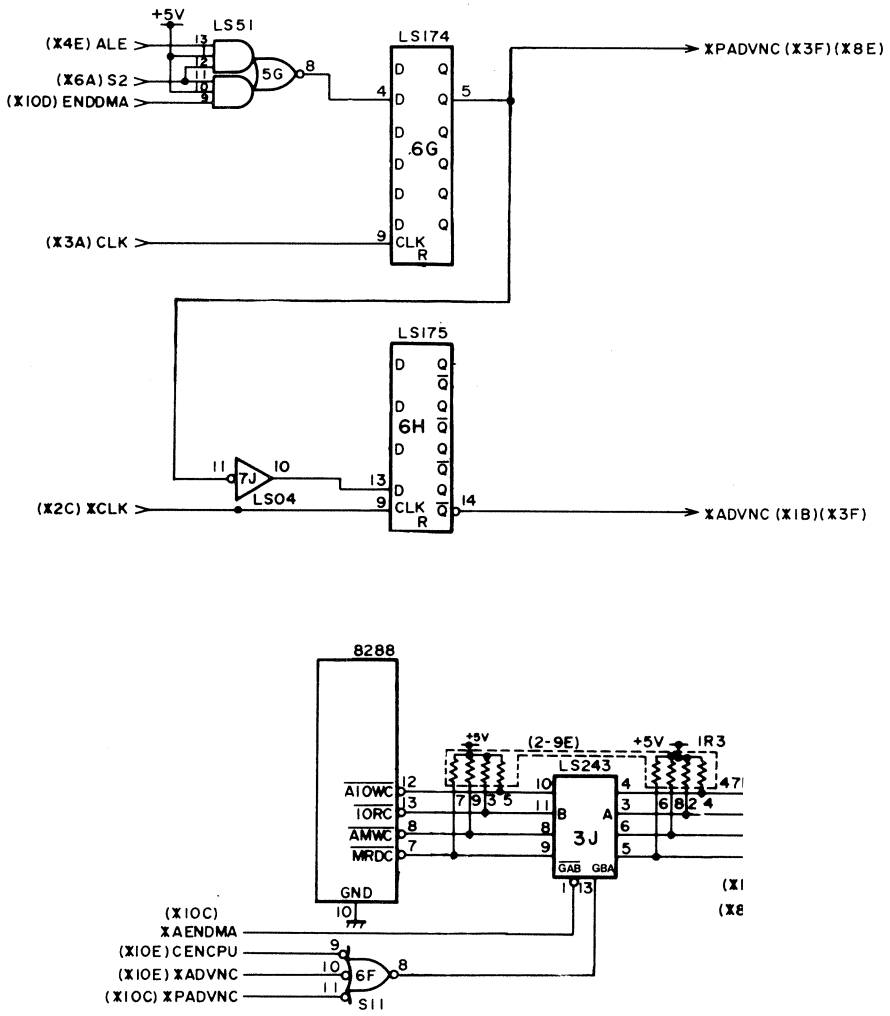


Figure 5-6 Timing Adjusting Circuit

Since the level of the status signal S2 is LOW when the MPU issues an I/O command, the levels of the ALE signal (ENDDMA signal immediately after a DMA cycle), as well as those of the *PADVNC and *ADVNC signals, go LOW one by one at each MPU clock pulse, and command signals are controlled by the input to the GBA pin of the bi-directional buffer (LS243).

The command signals *XMEMR, *XMEMW, *XIOW, and *XIOR are output by the trailing edge of the T2 clock cycle.

When memory or I/O access is slower than MPU operation, or when DMA is in progress, a wait state has to be requested from the MPU. This is another function of the wait state generation circuit.

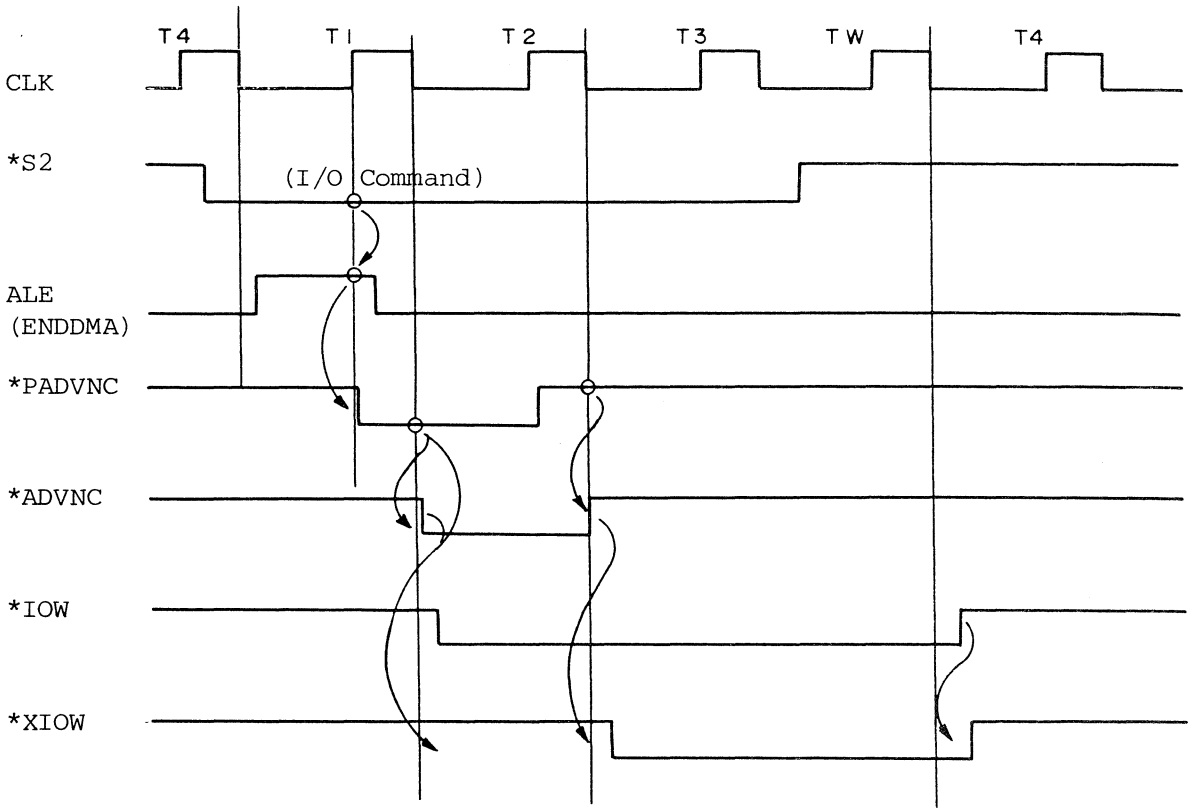


Figure 5-7 Timing Adjusting Timing Chart

A wait state is requested in the following cases:

(1) When the MPU has issued an I/O command, it waits one clock cycle (*ADVNC).

(2) When the MPU has accessed video RAM, it waits several clock cycles until the video RAM becomes idle (*CRTWAIT).

(3) When DMA is in progress, the MPU waits until DMA ends (DMAWAIT).

(4) When the internal bus connector makes a wait request, the MPU waits until the WAIT request is processed (*IOCHRDY).

All these WAIT requests are input to the 8284A circuit, and the 8284A asks the MPU for a wait state by turning off the READY signal.

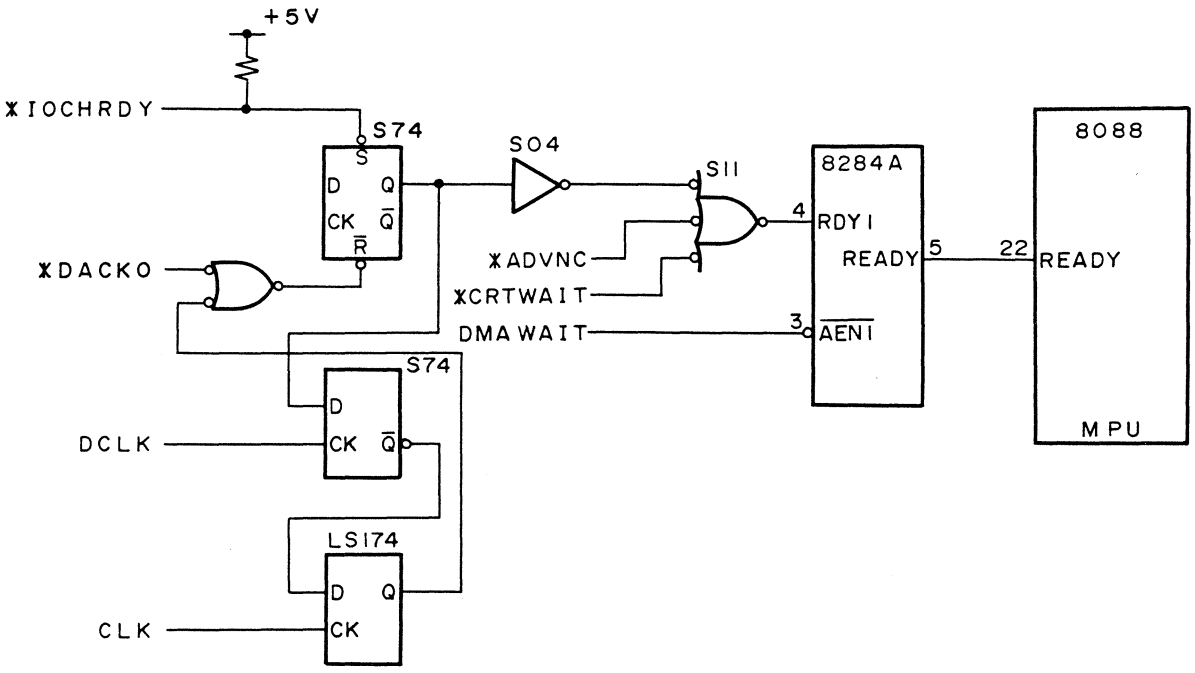


Figure 5-8 Wait State Generation Circuit

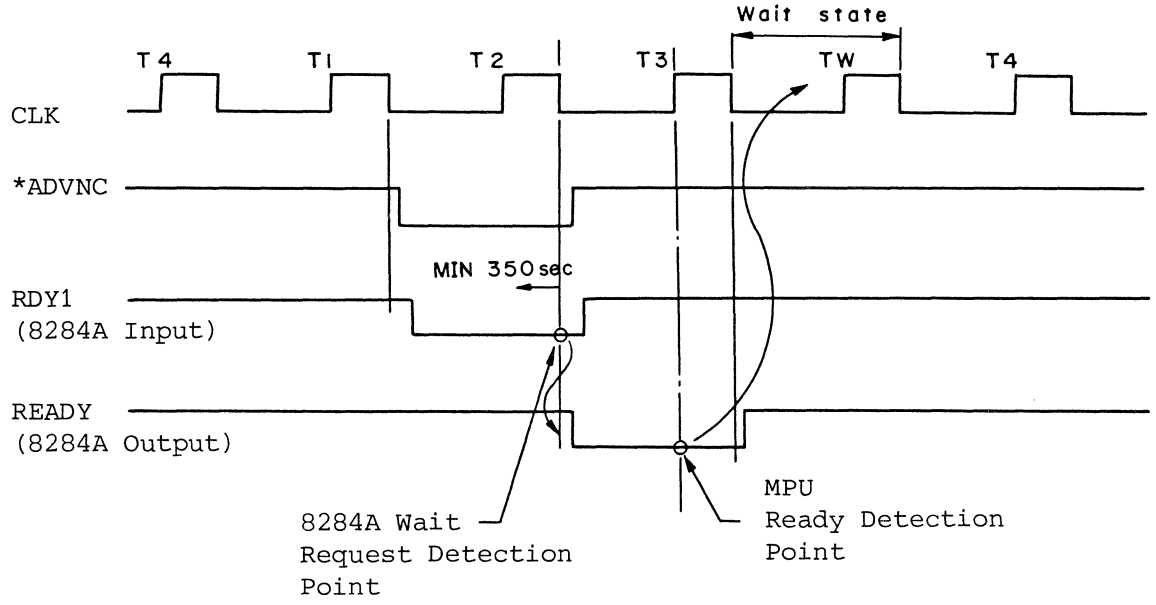


Figure 5-9 Wait State Generation Timing Chart

(d) NMI (non-maskable interrupt) generation circuit

This circuit generates an NMI under following conditions:

- o With co-processor 8087 installed and 8087 interrupt enabled, an unmasked interrupt occurs during numeric instruction execution.
- o The *IOCHCK signal is activated due to abnormal operation of the memory in an expansion unit or of other optional device.

The operation is outlined below.

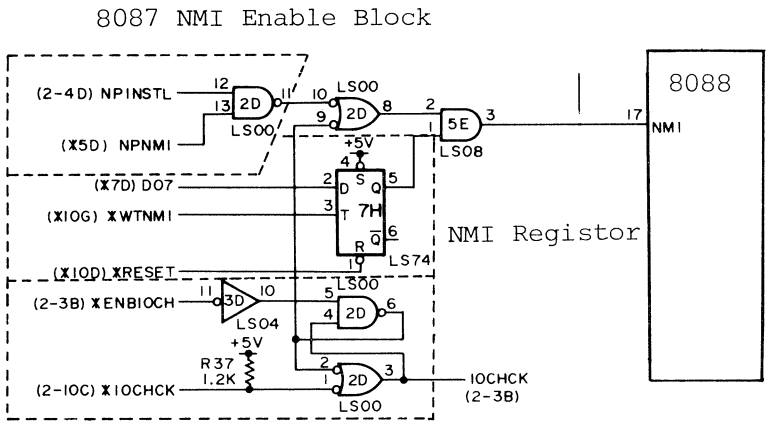


Figure 5-10 NMI Generation Circuit

(1) NMI register

NMIs are enabled with this register.

I/O address: 00A0 HEX

Command: To enable, 80HEX (OUT)
To disable, 00HEX (OUT)

(2) 8087 NMI ENABLE BLOCK

Setting DIP switch #2 to OFF enables NPNMI for faulty operation of the 8087.

(3) PARITY ENABLE BLOCK

When a memory device in an expansion unit or other optional device becomes faulty, the *IOCHCK line becomes active and an NMI is generated. This operation is enabled as follows:

I/O address: 0061(HEX)

Command: To enable, set bit 5 to "0".
To disable, set bit 5 to "1".

5.5 Memory Control Circuit

Memory devices in this logic unit are: 16K-byte ROM for BIOS programs, 256K-byte dynamic RAM as a standard provision, an expansion 256K-byte dynamic RAM, and 32K-byte video RAM in the PDP controller. All these memory devices are in the CPU board.

Figure 5-11 is the relationship between the memory devices and the memory map.

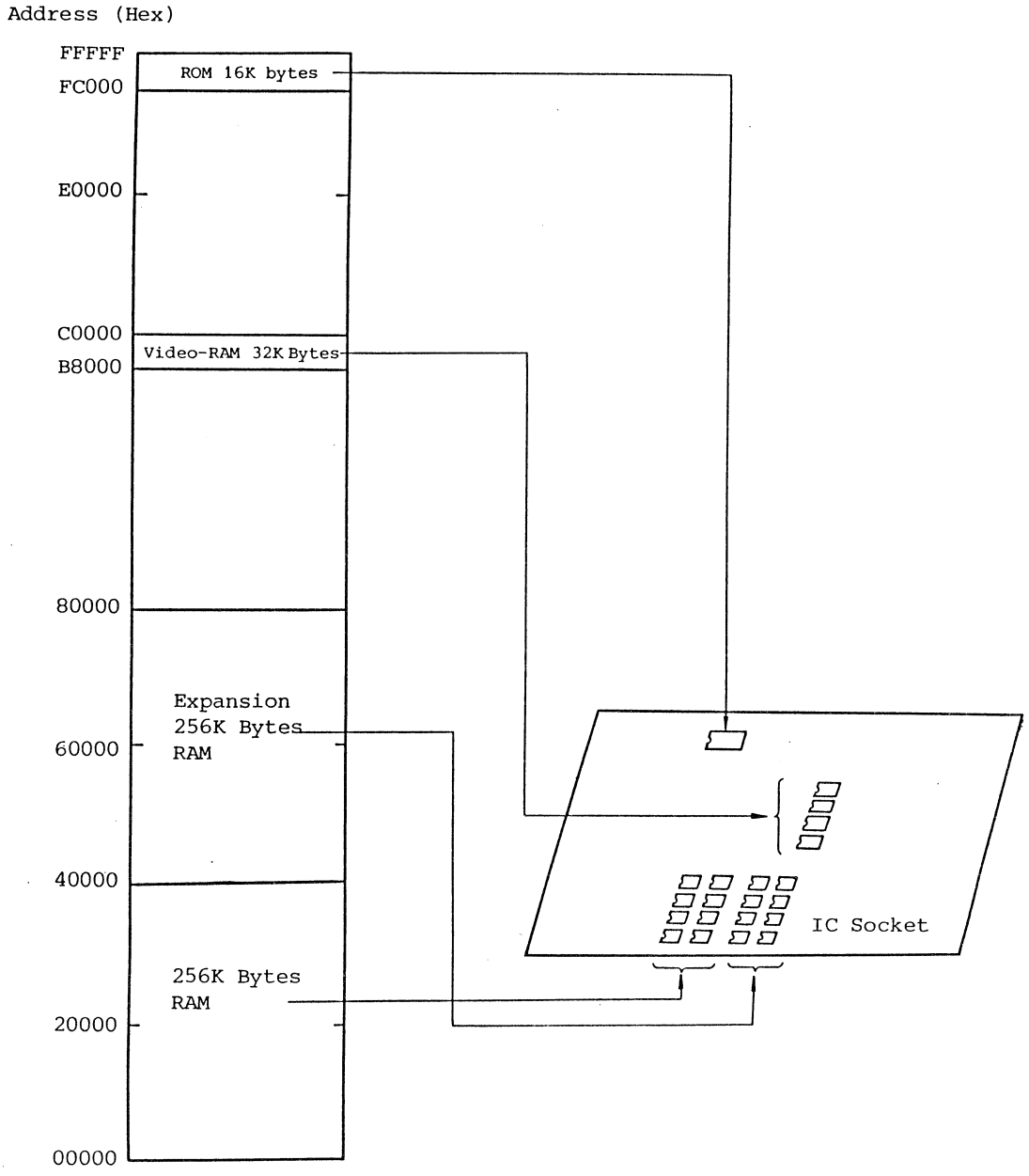


Figure 5-11 Relationship Between Memory Devices and Memory Map

(a) Memory address decoder

This circuit selects a memory device by decoding the contents of the MPU address when the MPU or DMAC accesses a memory device.

Decoded upper six bits, AB14 to AB19, of the address bus provide an MPU address.

Short plug J13 determines whether or not an expansion 256K RAM chips is installed. The output signal *DACK0 from the DMAC determines whether or not RAM refresh is taking place.

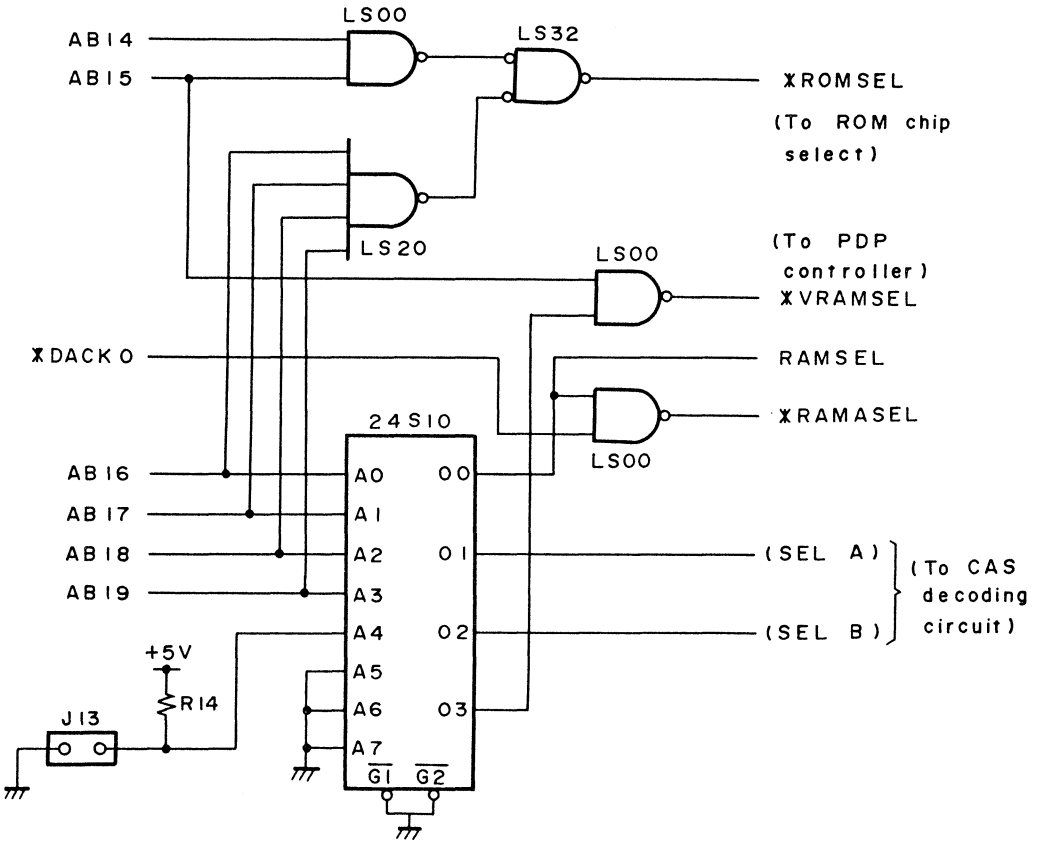


Figure 5-12 Memory Address Decoding Circuit

Short plug J13 has the following meanings:

o Short: Without an expansion 256K-byte RAM (256K-byte system)

o Open: With an expansion 256K-byte RAM (512K-byte system)

The memory address decoder is made up of a fuse ROM (24S10) and several gate logic circuits.

Table 5-1 shows the relationship between MPU addresses and decoder output.

Table 5-1 Memory Address Decoding

MPU Address						Short Plug J13	Refresh *DACK0	Output Signal
AB19	AB18	AB17	AB16	AB15	AB14			
0	0	x	x	x	x	x	"H"	RAMSEL ..... "HIGH" *RAMASEL ... "LOW" SELA ..... "LOW" SELB ..... "LOW" Standard 256K bytes selection
0	0	x	x	x	x	x	"L"	*RAMASEL ... "HIGH" Other output signals are the same as above. Refresh operation selection
0	1	x	x	x	x	Short	x	No selection output
0	1	x	x	x	x	Open	"H"	RAMSEL ..... "HIGH" *RAMASEL ... "LOW" SELA ..... "HIGH" SELB ..... "LOW" Expansion 256K bytes selection
1	0	1	1	1	x	x	x	*VRAMSEL ... "LOW" Video RAM selection
1	1	1	1	1	1	x	x	*ROMSEL .... "LOW" ROM selection

x: Do not care

(b) ROM circuit

The ROM circuit employs one ROM chip (equivalent to 27128) with a 16K-byte capacity (128K bits).

The ROM selection signal *ROMSEL is output from the memory address decoder and fed directly to the Chip Select (CS) Pin on the ROM chip, to output ROM data on the data bus upon receiving the memory read signal *XMEMR from the MPU.

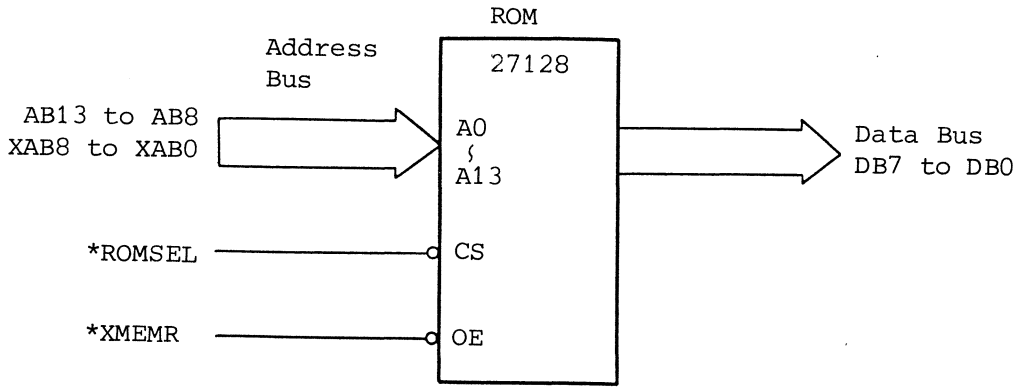


Figure 5-13 ROM Circuit

(c) RAM circuit

RAM is accessed by the DMAC, or through DMAC refresh.

Figure 5-14 shows a functional block diagram of a RAM access operation.

MPU addresses are converted into row and column addresses by the address multiplex circuit and are input to the RAM synchronized with the *RAS and *CAS timing signals.

In normal RAM access by the MPU and DMAC, input and output data is set in data bus lines DB7 to DB0 after *RAS and *CAS are input.

RAM is refreshed every 16 μs through Channel 0 of the DMAC. In RAM refreshing, *DACK0 is output from the DMAC, and the RAS address is input to the RAM synchronized with the *RAS signal. Because *CAS is not input, data is neither read nor written in.

The following operations are executed after RAM has been accessed by the MPU. Figure 5-15 outlines operational timing.

(1) MPU address is decoded, and RAM selection signals RAMSEL and *RAMASEL are output.

(2) The *RAS signal is output from the MPU command signals *XMEMR and *XMEMW, and the row address is input to the RAM from the address multiplex circuit.

(3) The row/column address switching signal RADMPX is output via the delay device (LS31) from the *RAS signal, and the address is switched to a column address.

(4) *CAS0 or *CAS1 is selected and input to the RAM with the address decoder output via the delay device (LS31) from RADMPX.

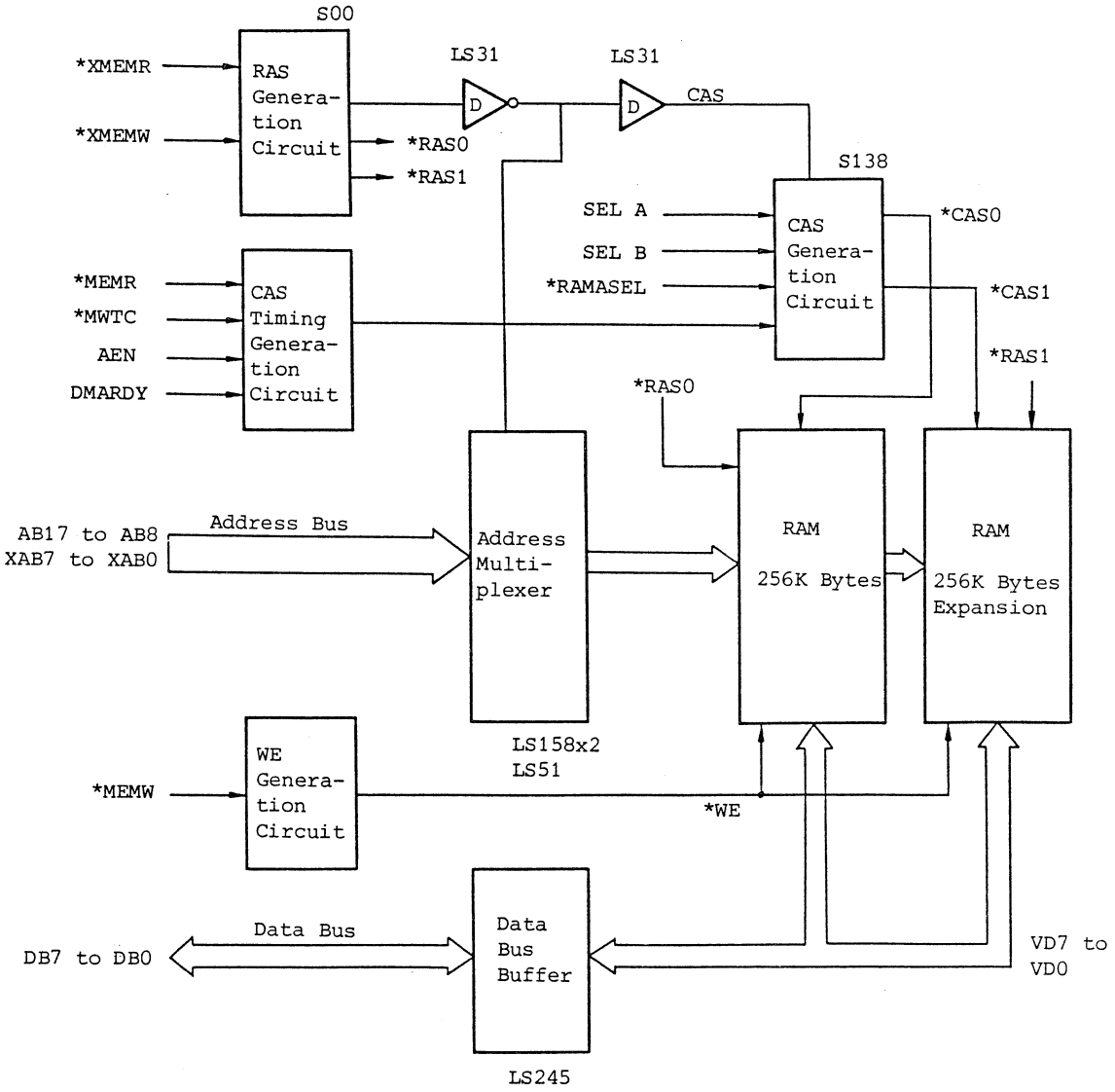


Figure 5-14 RAM Circuit Block Diagram

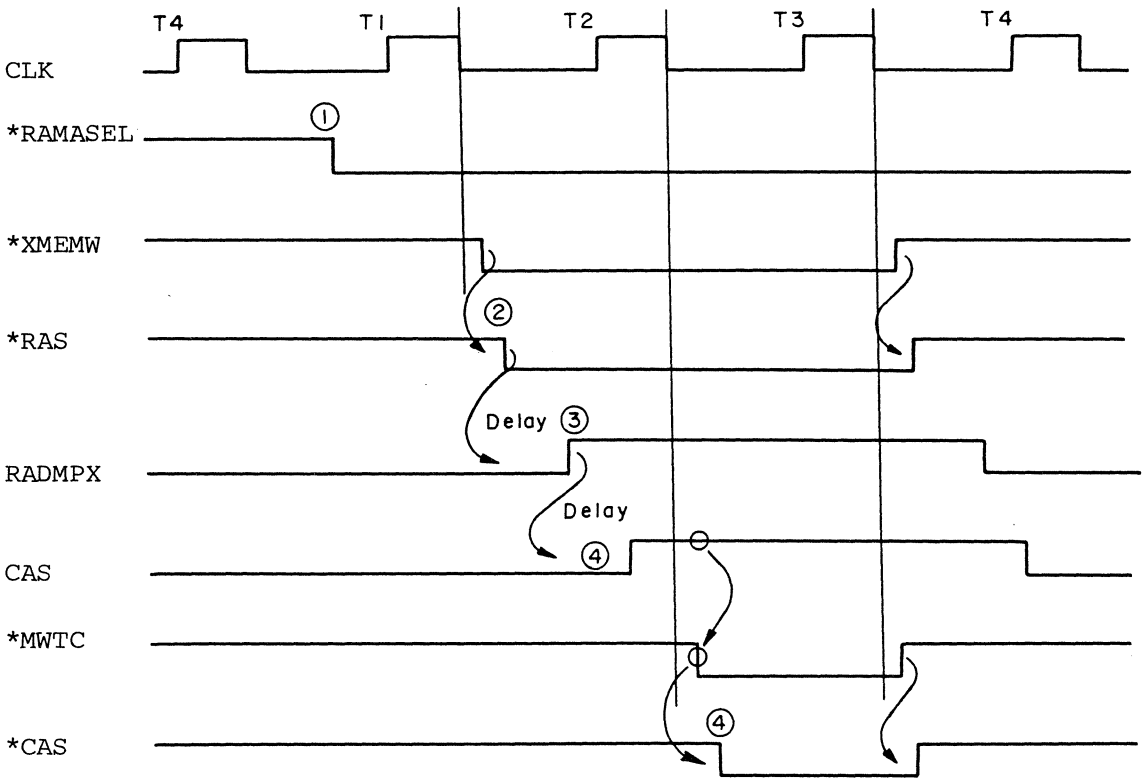


Figure 5-15 RAM Operation Timing Chart

5.6 DMA Circuit

The DMA controller 8237A-5 controls DMA operation. Figure 5-16 outlines the DMA cycle.

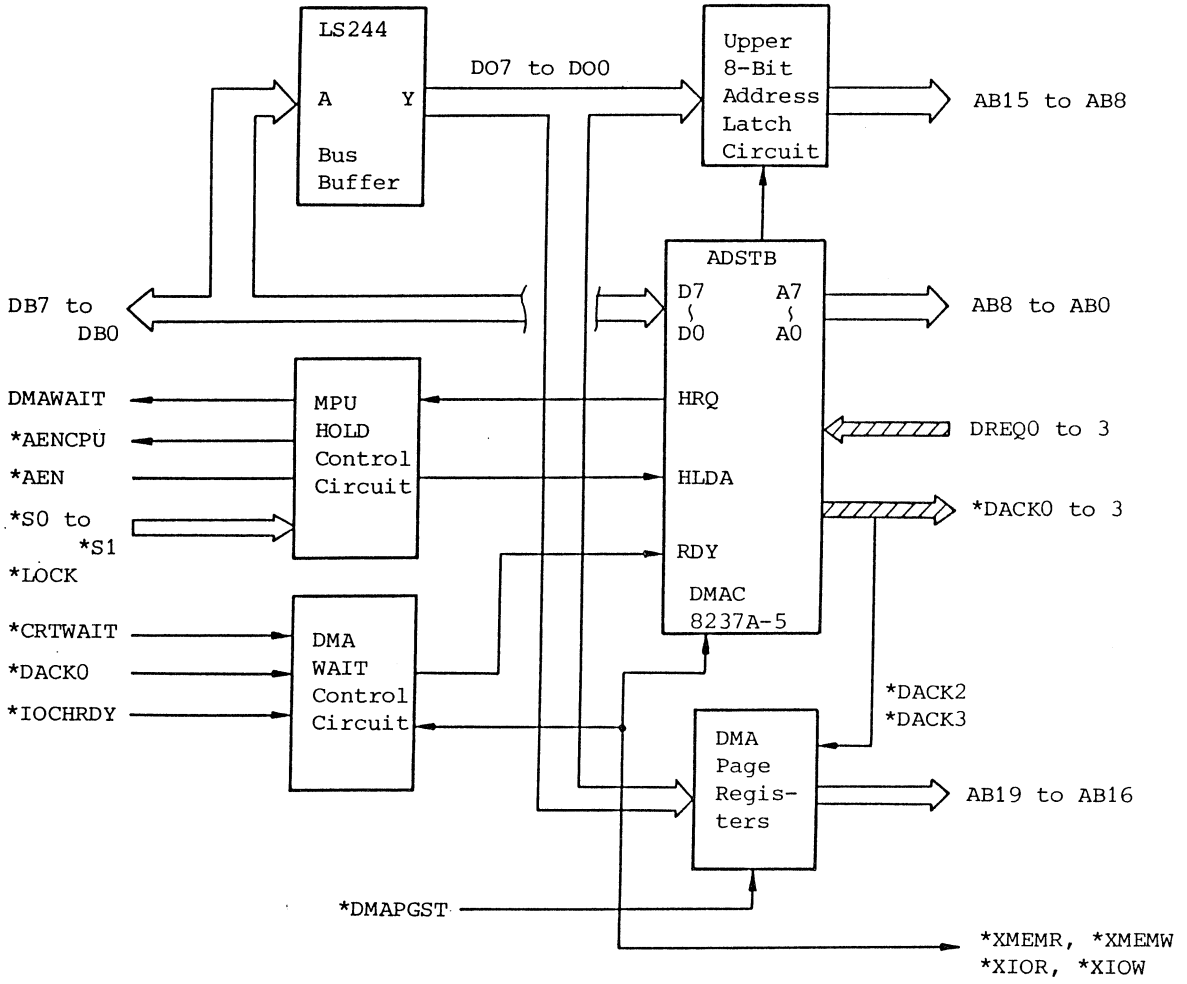


Figure 5-16 DMA Circuit Block Diagram

The DMAC 8237A-5 has a 16-bit address, and the DMA page registers produce the upper four bits, AB19 to AB16. There are three DMA page registers - one shared by Channels 0 and 1 and one each for Channels 2 and 3. The MPU I/O command is used to write data to the DMA page registers. The data is read from the DMAC in accordance with the *DACK command (*DACK0 to *DACK3), and output to address bus lines AB19 to AB16 in the DMA cycle.

The DMA operation is outlined below. DMA is carried out in the following sequence in response to the DMA request from the I/O.

(a) The DREQ signal requesting DMA is input to the relevant channel.

(b) The DMAC monitors the DREQ signal and outputs the HRQ signal to the MPU hold control circuit to obtain the bus use right.

(c) The MPU hold control circuit monitors the MPU bus usage at all times. If the MPU is using the bus, the circuit holds the current status. If the MPU is not using the bus, the circuit returns a hold answer signal (HLDA) to the DMAC.

(d) The MPU hold control circuit returns HLDA in synchronization with the MPU clock, and synchronizes and outputs the following signals.

- o *AENCPU (MPU is using bus) HIGH level during DMA cycle
- o *AENDMA (DMAC is using bus) LOW level during DMA cycle
- o *AEN (DMA cycle) LOW level during DMA cycle
- o DMAWAIT (DMA cycle wait) HIGH level during DMA cycle

(e) The *AENCPU and *AEN signals output by the MPU hold control circuit releases the MPU address bus and data bus, establishing a high impedance state. At the same time, the *MEMR, *MEMW, *IOR, and *IOW command signals are inhibited.

(f) When the MPU attempts to use the bus during a DMA cycle, the DMAWAIT signal is sent to set up a wait state until the DMA cycle is finished.

(g) The DMAC sends a DMA address when the HLDA signal is returned. The upper eight bits of the DMA are sent to the data bus and latched by the address strobe signal (ADSTB).

(h) *DACK is sent to the I/O that issued the DMA request.

(i) Then, the memory read/write signal (*XMEMR/*XMEMW) and I/O write/read signal (*XIOW/*XIOR) are output, and data transfer occurs between the memory and the I/O.

(j) If the DMA request is from an I/O other than Channel 0 (= refresh request), the DMAWAIT control circuit processes the DMARDY signal and produces a two-clock wait in the DMA cycle.

(k) When DMA transfer finishes, the DREQ signal from the I/O is reset, and relevant signals are reset one by one in the MPU hold control circuit, in synchronization with the MPU clock, returning the bus use right to the MPU. When the DMA cycle ends, the MPU hold control circuit generates an ENDDMA signal to notify the MPU peripheral circuit of the end of the DMA cycle.

Figure 5-17 outlines DMA operating timing.

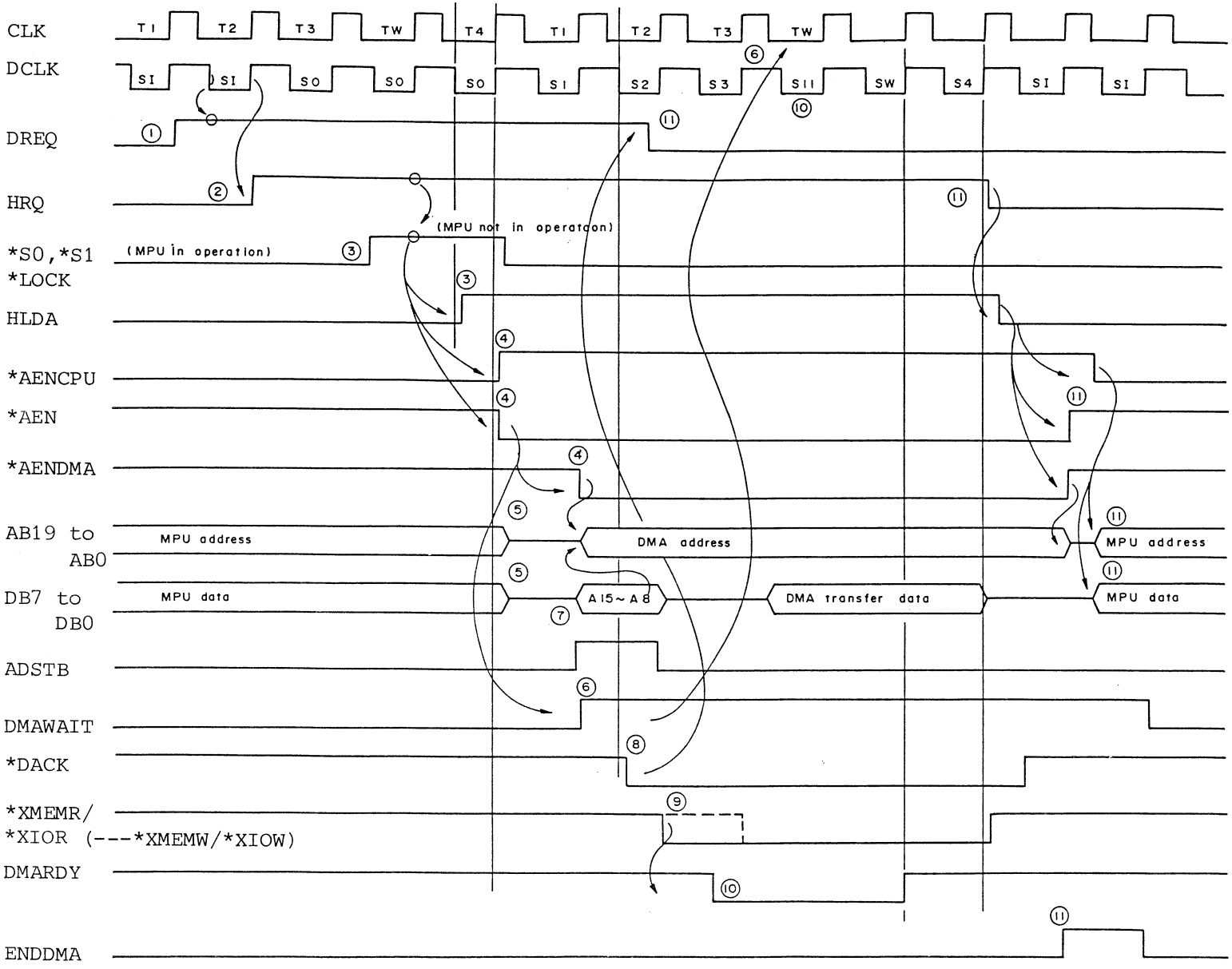


Figure 5-17 DMA Operation Timing Chart

5.7 I/O Address Decoder

This circuit decodes I/O addresses when the MPU performs I/O. Figure 5-19 shows the address map.

Table 5-3 shows the I/O command. The system uses indirect port addressing in which MPU general register DX designates I/O instructions.

Figure 5-18 shows the functional block diagram.

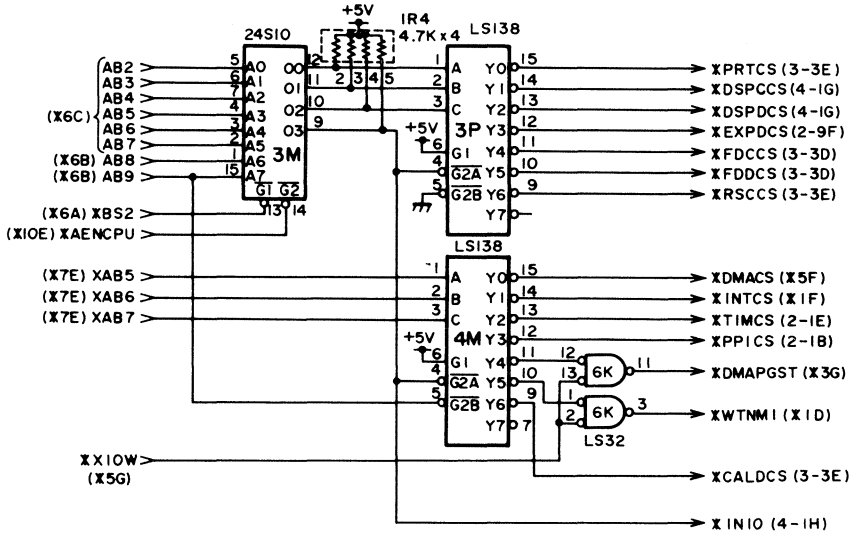


Figure 5-18 I/O Address Decoder Circuit

- During DMP operation, *AENCPU goes HIGH, and I/O address decoding is inhibited.

- During CPU operation, decoding is enabled or disabled as follows:

  In I/O access, interrupt acknowledge, and halt cycles, *BS2 goes low, and decoding is enabled.

  In fetch cycle, memory read/write, and reverse cycles, decoding is inhibited.

The I/O operation is described below.

An I/O address sent from the CPU is decoded by ROM 24S10. Table 5-2 shows the ROM data. The CPU status signal *BS0 and the DMA status signal *AENCPU enable the 24S10 to decode addresses. The decoder IC LS138 outputs a SELECT signal to each I/O using the 24S10 output and part of the address bus.

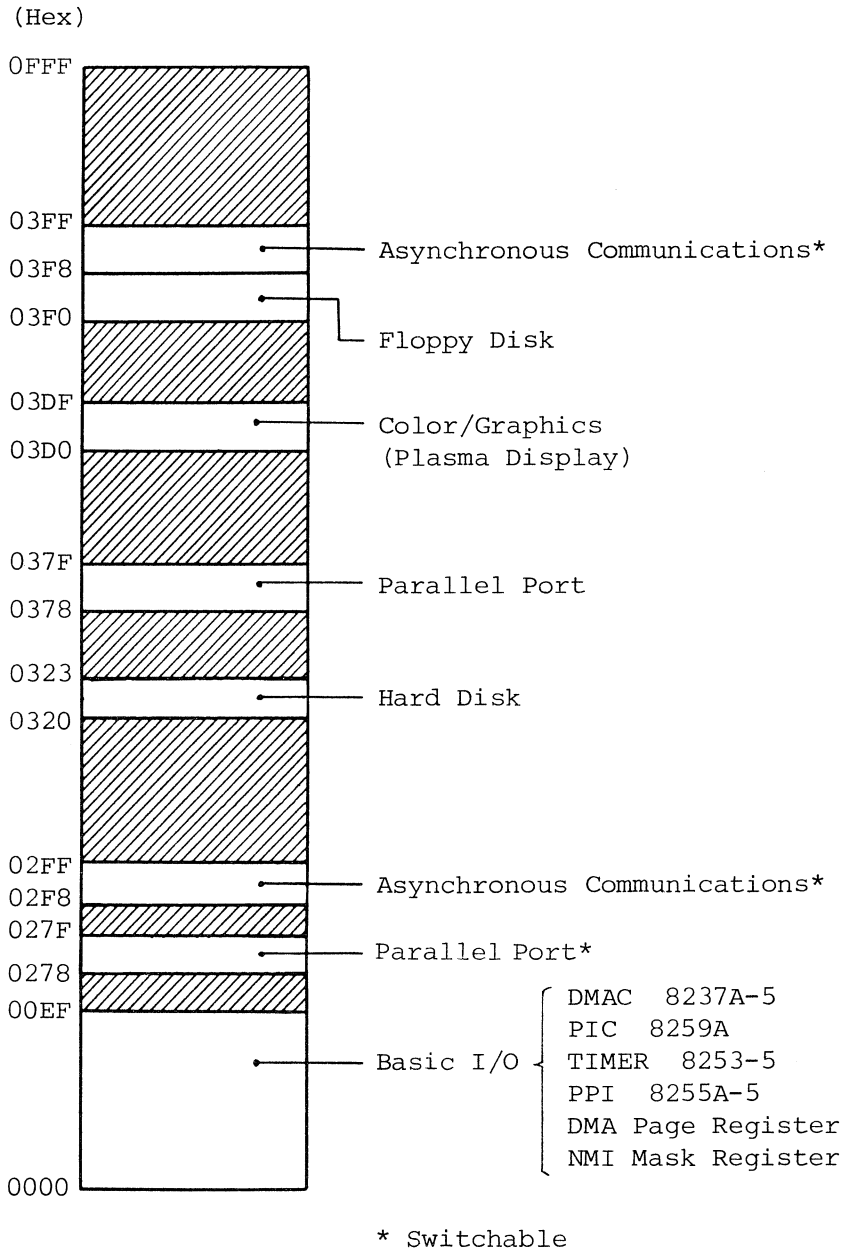


Figure 5-19 I/O Address Map

Table 5-2 I/O Decoder ROM Data

High-Order Address 4 Bits / Low-Order Address 4 Bits	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
1	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
2	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
3																
4																
5																
6																
7																
8					3											
9															0	0
A																
B															6	6
C																
D															0	0
E																
F					1	1	2						5	4	6	6

Note: All blanks are F. HEX values on the address bus differ from the ROM data HEX values in the previous table.

Address Bus	9	8	7	6	5	4	3	2	1	0	HEX
Bits	1	1	1	1	1	1	0	1	0	0	3FD
24S10 ROM Input terminal	A7	A6	A5	A4	A3	A2	A1	A0			FD
24S10 ROM Output terminal	O_3 0		O_2 1		O_1 0		O_0 0				4

Table 5-3 I/O Command Table (1/3)

I/O ADDRESS HEX	DESTINATION DEVICE	COMMAND IN (MSB D7 6 5 4 3 2 1 D0 LSB)	COMMAND OUT (D7 6 5 4 3 2 1 D0)
0000	DMAC 8237A-5	READ CH #0 CURRENT ADDRESS (F)LOWER(L)UPPER	SET CH=0 BASE & (F)LOWER(L) UPPER CURRENT ADDRESS
0001	〃	READ CH #0 CURRENT WORD COUNT (F)LOWER(L)UPPER	SET CH=0 BASE & (F)LOWER(L) UPPER CURRENT WORD COUNT
0002	〃	READ CH #1 CURRENT ADDRESS (F)LOWER(L)UPPER	SET CH #1 BASE & (F)LOWER(L) UPPER CURRENT ADDRESS
0003	〃	READ CH #1 CURRENT WORD COUNT (F)LOWER(L)UPPER	SET CH #1 BASE & (F)LOWER(L) UPPER CURRENT WORD COUNT
0004	〃	READ CH=2 CURRENT ADDRESS (F)LOWER(L)UPPER	SET CH #2 BASE & (F)LOWER(L) UPPER CURRENT ADDRESS
0005	〃	READ CH =2 CURRENT WORD COUNT (F)LOWER(L)UPPER	SET CH #2 BASE & (F)LOWER(L) UPPER CURRENT WORD COUNT
0006	〃	READ CH =3 CURRENT ADDRESS (F)LOWER(L)UPPER	SET CH # 3 BASE & (F)LOWER(L) UPPER CURRENT ADDRESS
0007	〃	READ CH =3 CURRENT WORD COUNT (F)LOWER(L)UPPER	SET CH # 3 BASE & (F)LOWER(L) UPPER CURRENT WORD COUNT
0008	〃	READ DMAC STATUS REQUEST #3 #2 #1 #0 REACHED TC #3 #2 #1 #0	SET DMAC COMMAND DACK DREQ FU PR TIM Er CHO M Do M L H Ad
0009	〃		SET REQUEST REG. DONT CARE SET/RESET CH SELECT
000A	〃		SET SINGLE MASK REGISTER BIT DONT CARE S/R CH SELECT
000B	〃		SET MODE REG. SELECT MOOE INK AUTO ∞ TRANS TYPE CH SELECT
000C	〃	READ TEMPORARY REGISTER 8 BIT DATA	CLEAR BYTE POINTER DONT CARE
000D	〃		MASTER CLEAR DONT CARE
000E	〃		CLEAR MASK REG. DONT CARE
000F	〃		SET#ALL MASK DEEISTER BIT DONT CARE SET/RESET #3 #2 #1 #0
0020	PIC 8259A	READ IRR, ISR	SET ICWI OCW2, OCW3
0021	〃	READ IMR	SET CCWI ICW2, ICW3
0040	TIMER 8253-5	READ COUNTER =0 (INTERVAL TIMER)	SET COUNTER=0 (INTERVAL TIMER)
0041	〃	READ COUNTER =1 (MEMORY REFRESH)	SET COUNTER#1 (MEMORY REFRESH)
0042	〃	READ COUNTER =2 (BEER FREQUENCY)	SET COUNTER#2 (BEEP FREQUENCY)

Table 5-3 I/O Command Table (2/3)

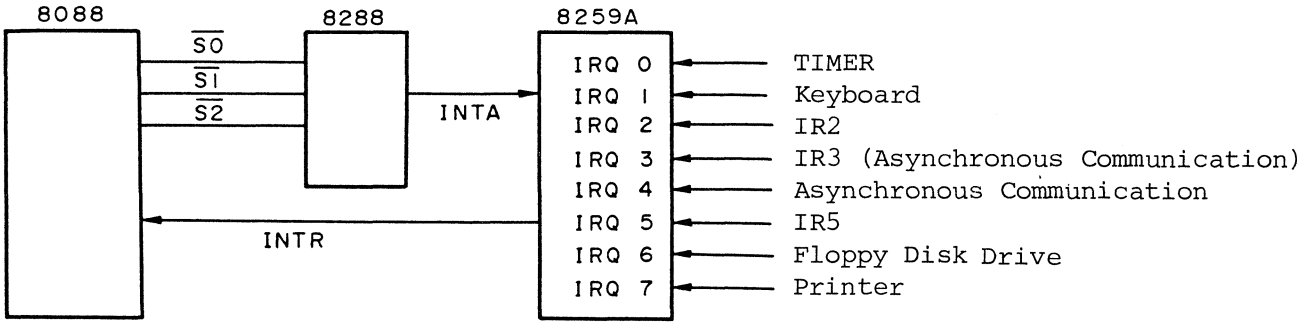
I/O ADDRESS HEX	DESTINATION DEVICE	COMMAND	
		IN MSB D7 6 5 4 3 2 1 D0 LSB	OUT MSB D7 6 5 4 3 2 1 D0 LSB
0043	TIMER 8253-5		SET 8253 CONTROL WORD REG: SC0 SC1 RL1 RL0 M2 M1 M0 BC
0060	PRI 8255A-5	READ KEY-IN DATA: KEY-IN DATA	
0061	"		SET PORT B: K/B EN, K/B CLK LOW, EN I/O CH, X, SW H OR L, X, SP EN, SP EN
0062	"	READ SYSTEM SW & I/O STATUS: X, I/O CH, SP, SP, NUMBER OF FDD, DISP TYPE, OUT, MB, SI, I	
0063	"		SET 8255A-5 MODE: 1 0 0 1 1 0 0 1
0081	DMA PAGE REG.		SET CH#2 PAGE: DONT CARE, A19 A18 A17 A16
0082	"		SET CH#3 PAGE: DONT CARE, A19 A18 A17 A16
0083	"		SET CH#0 PAGE: DONT CARE, A19 A18 A17 A16
00A0	NMI REG.		SET NMI REG: EN, DONT CARE
	PARALLEL PORT		Hard disk
0378 (0278)	"	READ PRINT DATA: Data	SET PRINT DATA: Data
0379 (0279)	"	READ I/O STATUS: PR ACK, BST, PE, SL, ER, X, X, X	
037A (027A)	"	READ PRINT STROBE: X, X, X, INT, SEL IN, INIT, AP, ST	SET PRINT STROBE: X, X, X, INT SEL EN, IN, AF, ST
03D0	CRTC 6845		SET CRTC INDEX REG: INDEX, X, X, X
03D1	"	READ CRTC DATA REG: Data	SET CRTC DATA REG: Data
03D8	DISPLAY		SET DISPLAY MODE: MODE, X, X
03DA	"	READ DISPLAY STATUS	
03F2	FDD CONTROL		SET FDD CONTROL REG: MODE EN #3 #2 #1 #0, INT EN, DRIVE SEL, RE-SET
03F4	FDC 765AC	READ FDC STATUS REG.: RQM, DIO, DMA, BSY, FDC #3 #2 #1 #0, FDD BUSY	
03F5	FDC 765AC	READ FDC DATA REG.: Data	SET FDC BUFFER: Data
03F8 (DLAB=0) (02F8)	RS-232C 8250B	READ RX9 BUFFER: Rx Data	SET. TXD: Tx Data

Table 5-3 I/O Command Table (3/3)

I/O ADDRESS HEX	DESTINATION DEVICE	COMMAND	
		IN (MSB D7 6 5 4 3 2 1 LSB D0)	OUT (MSB D7 6 5 4 3 2 1 LSB D0)
03F8 (DLAB=1) (02F8)	RS-232C 82503		SET DIVISOR LATCH (LSE) — Least Signification Byte
03F9 (DLAB=0) (02F9)	〃		SET INTERRUPT ENABLE — Modem Line Tx Rx; 0 0 0 0 INT IHT INT IHT
03F9 (DLAB=1) (02F9)	〃		Most Signification Byte
03FA (02FA)	〃	READ INTERRUPT IDENTIFICATION — 0 0 0 0 0 INT FUNC	
03FB (02FB)	〃		SET LINE CONTROL REG. — DL AB BR CN ST PRI ODD EIN PAR TY ST BI; Word Length
03FC (02FC)	〃		SET MODEM CONTROL REG. — OUTPUT 0 0 0 2 1 RTS STR
03FD (02FD)	〃	READ LINE STATUS — 0 Rx EMP Tx EMP Br IND Fr Er Par Er OV Er Data RDY	
03FE (02FE)	〃	READ MODEM STATUS — RLSB RI DSR CTS DRL SD TE RI DO SR DC TS	

5.8 Interrupt Control Circuit

The interrupt controller employs the 8259A, a programmable interrupt controller. Eight interrupt levels are available.



The IR2, IR3, and IR5 are to users.

Figure 5-20 Interrupt Control Circuit Block Diagram

The interrupt control circuit operates as follows:

(a) When an I/O requests an interrupt, a request signal enters the IR input.

(b) The 8259A checks the mask condition and priority, and sends an interrupt request INTR signal to the CPU.

(c) The CPU outputs status $\overline{S0}$ = L, $\overline{S1}$ = L, and $\overline{S2}$ = L to the bus controller 8288 in response to the interrupt request.

(d) The 8288 confirms that $\overline{S0}$ to $\overline{S2}$ are all "Ls," and outputs *INTA to the 8259A in response.

(e) The 8259A stops during the data bus.

(f) The 8088 issues the status "$\overline{S0}$ = L, $\overline{S1}$ = L, $\overline{S2}$ = L" to the 8288, and the 8288 outputs a second INTA.

(g) The 8259A outputs the vector address that has been programmed on the data bus, in synchronization with the second INTA.

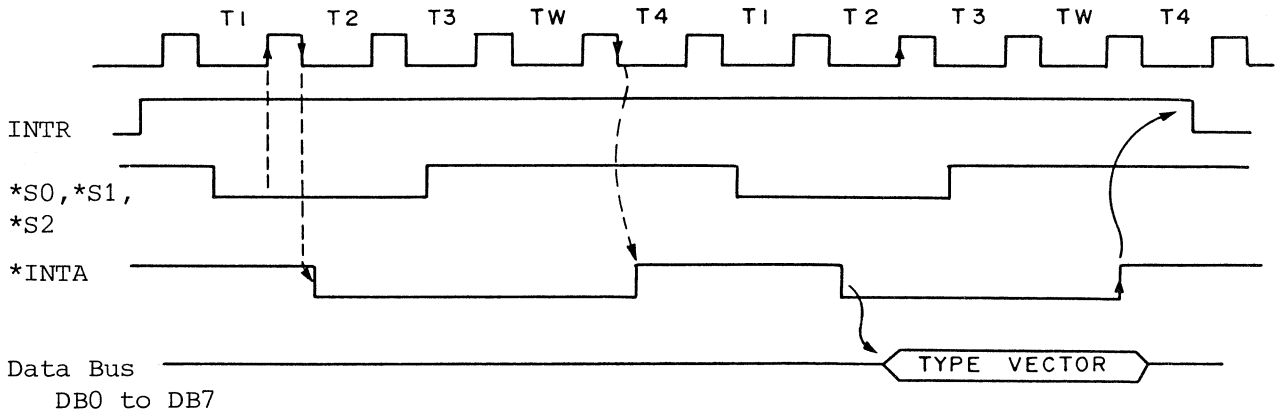


Figure 5-21 Interrupt Control Timing Chart

5.9 Display Circuit

The display circuit controls the plasma display unit. Figure 5-22 shows a block diagram of the display circuit. The blocks are described as follows:

(a) Interface with the CPU:

(1) Data bus transceiver

(2) VRAM data latch

(3) Display mode register

(4) Status gate

(5) CRTC parameter converter

(6) Memory address decoder

(7) WAIT circuit

a) Wait during VRAM access
b) Wait during I/O write

(b) Display control circuit

(8) Timing generator

a) Basic timing generator
b) CRTC clock control circuit
c) VRAM access timing circuit
d) RAS and CAS timing circuit

(9) CRTC

(10) VRAM address controller

a) VRAM address multiplexer
b) CRTC address selector
c) Refreshing address counter

(11) VRAM data transceiver data latch

a) VRAM
b) VRAM access by the CRTC

(12) CHG and font data latch

(13) Graphic data latch

(14) Attribute decoder

(15) Video data controller

a) First converter
b) Second converter
c) Third converter

(16) CRTC control signal converter

a) DISPTMG cursor circuit
b) HSYNC circuit
c) VSYNC circuit

(17) Blink timing circuit

(18) Plasma output driver

(19) Plasma reset control

(20) Plasma interface signal

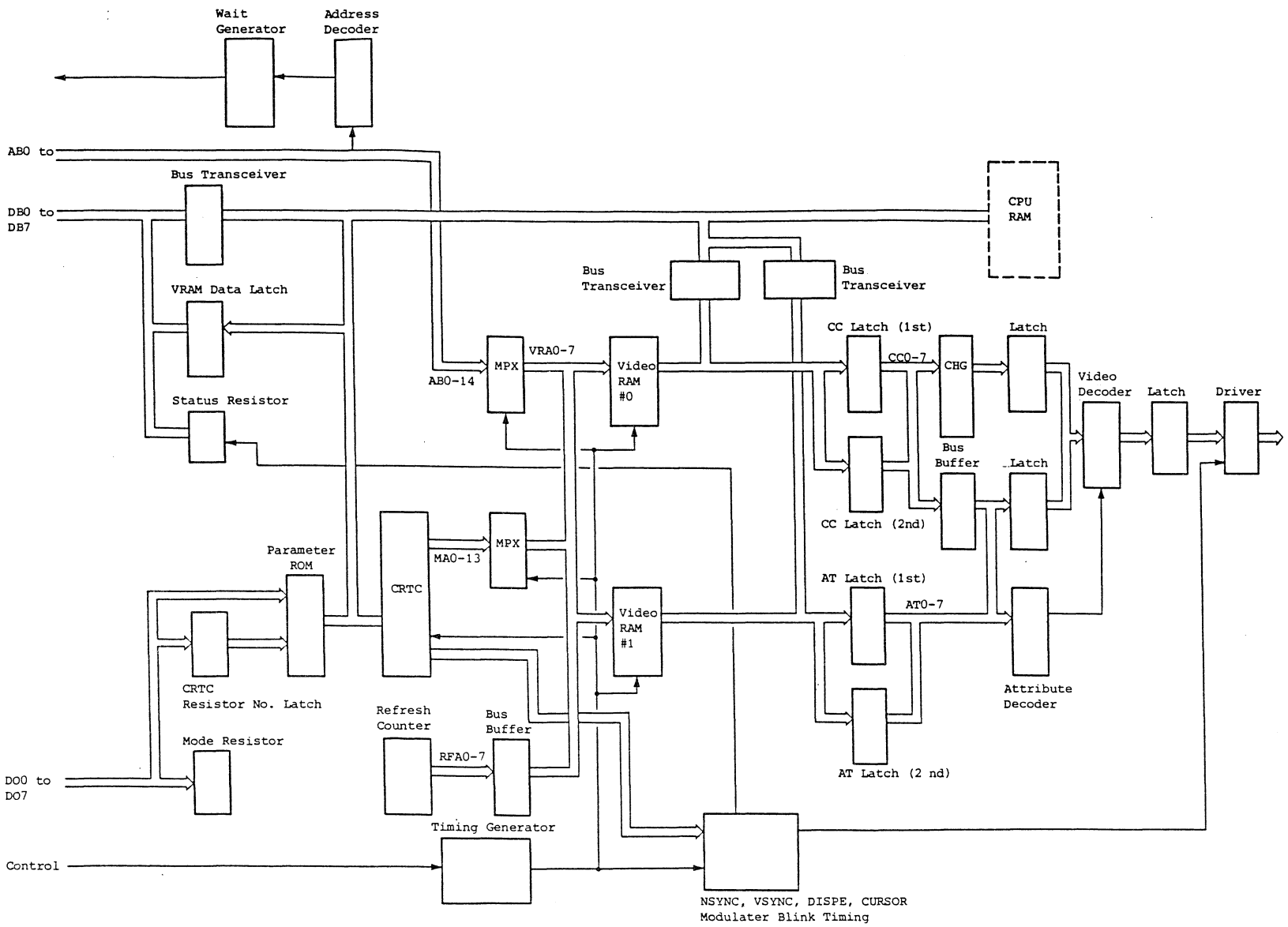


Figure 5-22 PDPC Block Diagram

(a) Data bus transceiver

The data bus transceiver is a bidirectional buffer that connects the CPU data bus (DB0 to DB7) with the main memory/display data bus (VD0 to VD7).

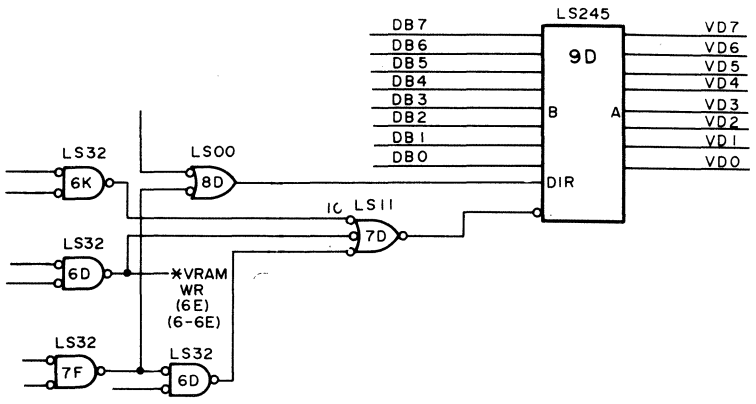


Figure 5-23 Data Bus Transceiver Circuit

The data bus transceiver functions only in the following three cases:

(1) When the main memory is accessed

(2) When data is written in VRAM

(3) When the CPU reads the CRTC register

The direction of data flow through the data bus transceiver is determined as follows:

Memory access by CPU:	From VD bus to DB bus
I/O read by CPU:	From VD bus to DB bus
Any other time:	From DB bus to VD bus

(b) VRAM data latch

When the CPU or DMAC reads VRAM, the data read out from VRAM onto the data bus is latched. Then the CPU (or DMAC) stops reading VRAM and begins reading the succeeding display data. The latched data is held on the DB data bus until the CPU (or DMAC) finishes the read. Figure 5-24 shows the data latch timing.

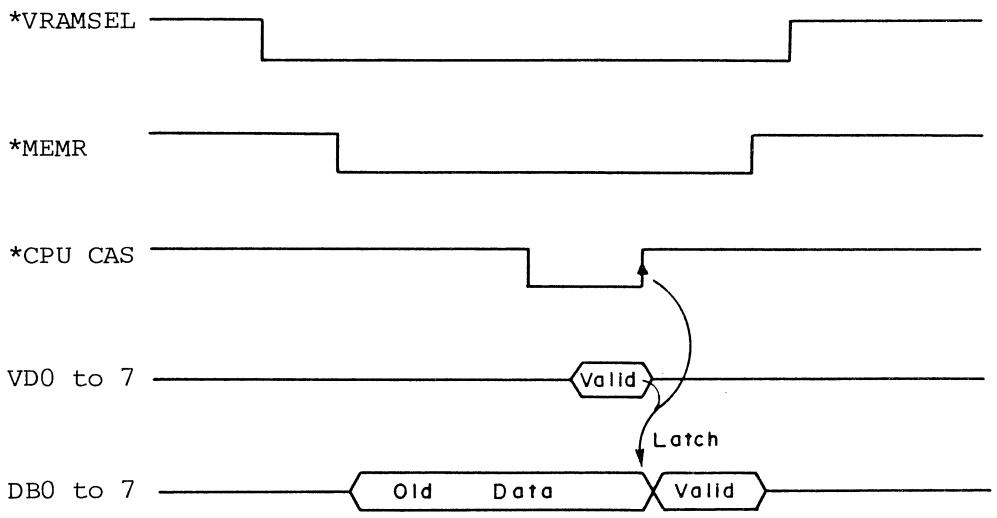


Figure 5-24 Data Latch Timing Chart

(c) Display Mode Register

The 6-bit Display Mode register sets the display mode of the plasma display panel. The Display Mode register is cleared by the *RESET signal when power is turned on. The display mode is set to TEXT 40x25.

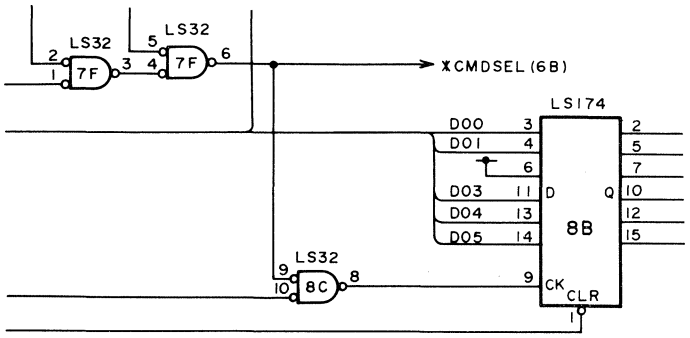


Figure 5-25 Display Mode Register Circuit

The write operation (into the Display Mode register) starts at the rising (leading) edge of the *WRTE signal, which is in synchronization with the CRTC clock.

The signals output to the Display Mode register are as follows:

(1) HIGH TEXT

HIGH in the TEXT 80x25 and GRAPHIC 640x400 modes

(2) GRAPHIC

HIGH in the GRAPHIC mode

(3) CMDSET

Stays HIGH after the WRITE instruction is executed to write into the Display Mode register (i.e., after power has been turned on).

(4) EN VIDEO

Enables or disables the screen display. HIGH when display is enabled.

(5) HIGH GRAPH

HIGH in the GRAPHIC 640x200 and 640x400 modes.

(6) EN BLINK

Enables blinking (bit 7 of attribute code) in TEXT mode. HIGH when blinking is enabled.

(d) Status gate

The 4-bit status gate reads the status of the CRTC (HSYNC and VSYNC states).

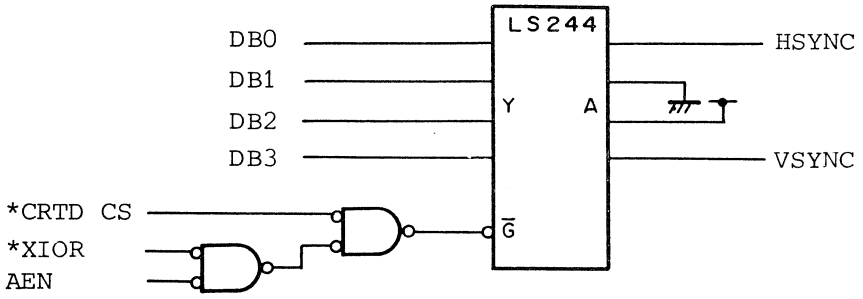


Figure 5-26 Status Gate Circuit

The status gate is enabled when it is read by the CPU. The states of the status register is as follows:

DB0: HSYNC
DB1: Always LOW
DB2: Always HIGH
DB3: VSYNC

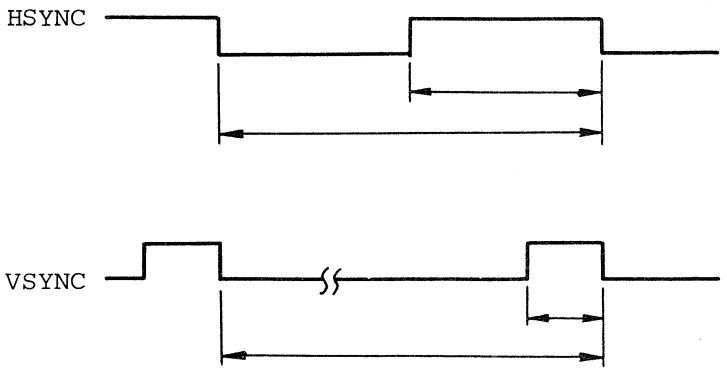


Figure 5-27 Status Gate Timing Chart

(e) CRTC parameter converter

The CRTC parameter converter converts CRTC parameter values into plasma display parameter values. The CRTC parameter converter circuit is shown below.

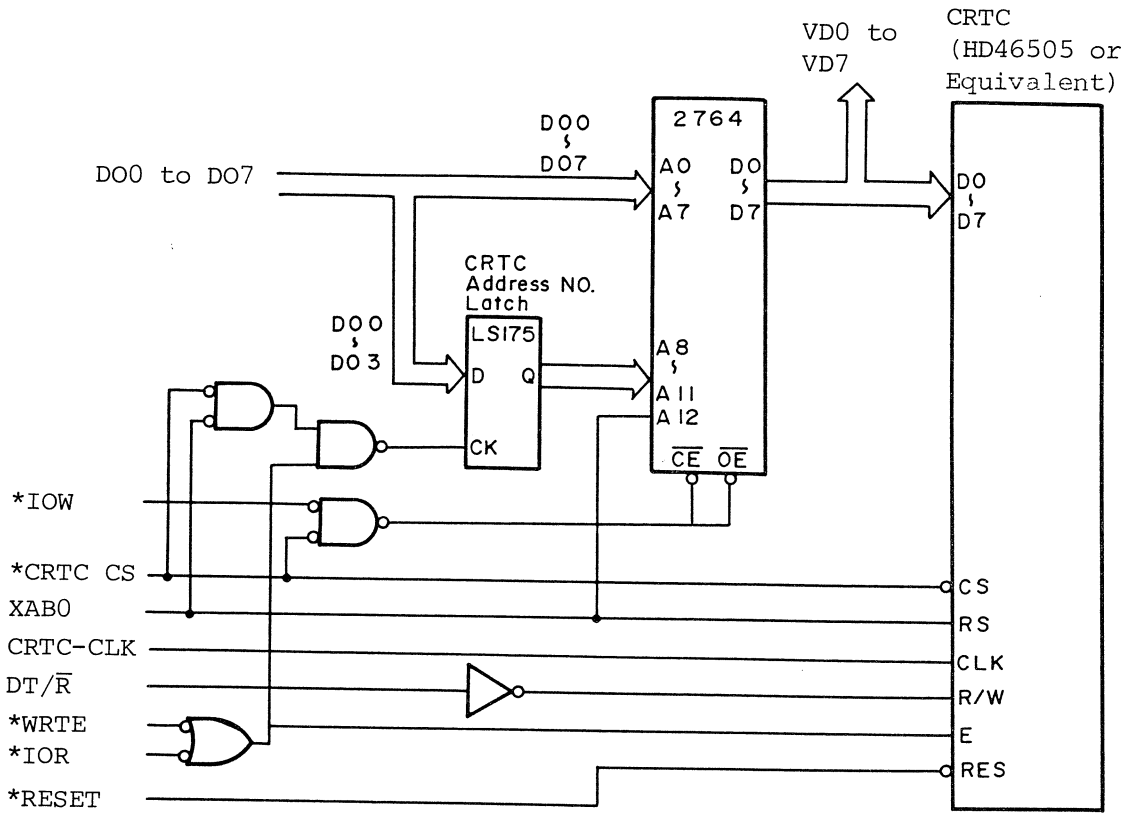


Figure 5-28 CRTC Parameter Converter Circuit

When written into the CRTC address register (XAB0 = LOW), the data is converted according to ROM address input XAB0, CRTC Address Number Latch, and DO0 to DO7 values, and output to VD0 to VD7. The converted data is latched on the CRTC address register at the rising edge of *WRTE (write timing signal), which is in synchronization with the CRTC clock pulse. At the same time, the data is written in the CRTC Address Latch. The value of input DO0 to DO7 is equal to the value of the converted data VD0 to VD7.

Writing to the CRTC control register (R0 to R15) (valid when XAB0 is HIGH) is performed in a similar manner. Data obtained from conversion using ROM address input XAB0, the latched CRTC address (latched when data is written in the address register), and DO0 to DO7 value is output to VD0 to VD7. The data is then written into the control register at the trailing edge of the CRTC-E signal. In this case, the CRTC address is not latched.

When the CRTC register is read, data is output from the CRTC to VD0 to VD7. In this case, the CRTC parameter converter is inoperative. Figure 5-29 shows timing for writing to the CRTC register.

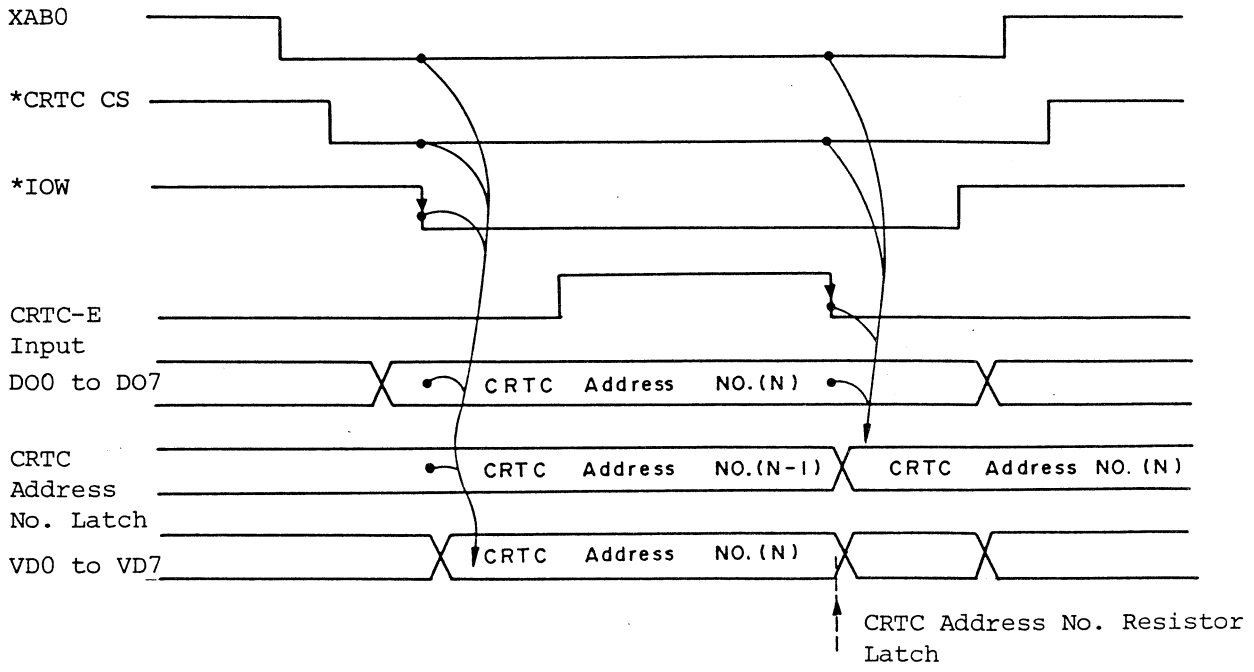


Figure 5-29 Writing to the CRTC Timing Chart

(f) Memory address decoder

When VRAM is accessed, the memory address decoder controls the data transfer by the bus transceiver between the VRAM and VD data buses. The decoder also controls the Write Enable signal for VRAM. The bus transceiver is enabled by *MEMR at read time, or when data is written to RAM.

The memory address decoder circuit is shown below.

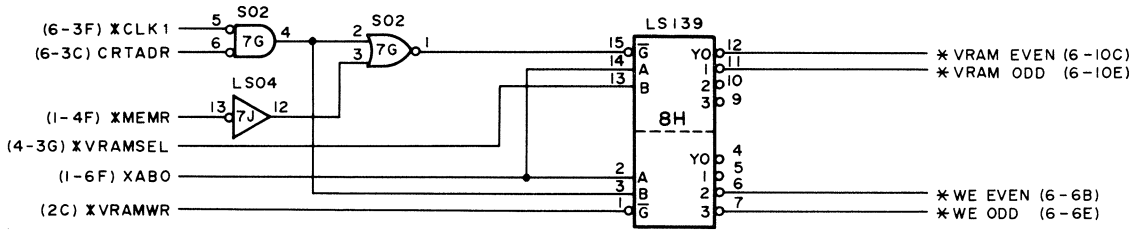


Figure 5-30 Memory Address Decoder Circuit

The memory address decoder outputs are:

(1) *VRAM EVEN

LOW when an even-numbered address of VRAM is accessed (when XAB0 is LOW). The bus transceiver of the even-numbered addresses is enabled.

(2) *VRAM ODD

LOW when an odd-numbered address of VRAM is accessed (when XAB0 is LOW). The bus transceiver of the odd-numbered addresses is enabled.

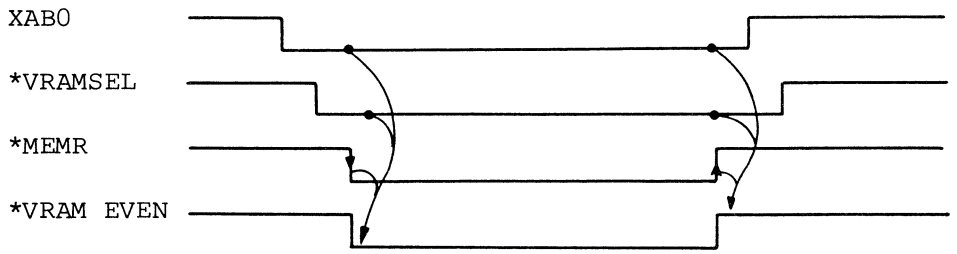
(3) *WE EVEN

LOW when data is written in a even-numbered address of VRAM (XAB0 is LOW). Makes RAM Write-Enabled.

(4) *WE ODD

LOW when data is written in an odd-numbered address of VRAM (XAB0 is HIGH). Makes RAM Write-Enabled. (Figure 5-31)

o VRAM read timing chart



o VRAM write timing chart

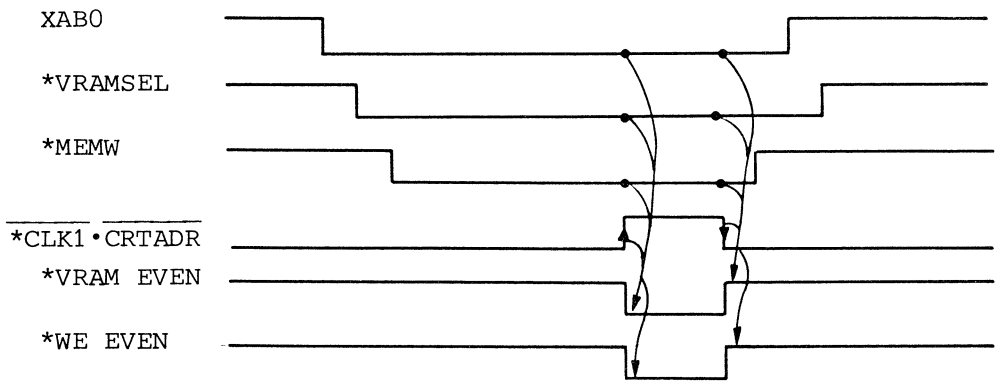


Figure 5-31 Memory Address Decorder Timing Chart

(g) WAIT circuit

The WAIT circuit holds the CPU or DMAC at wait state when I/O data is written to the display mode register and the CRTC, or when VRAM is accessed.

Figure 5-32 shows the WAIT operation timing.

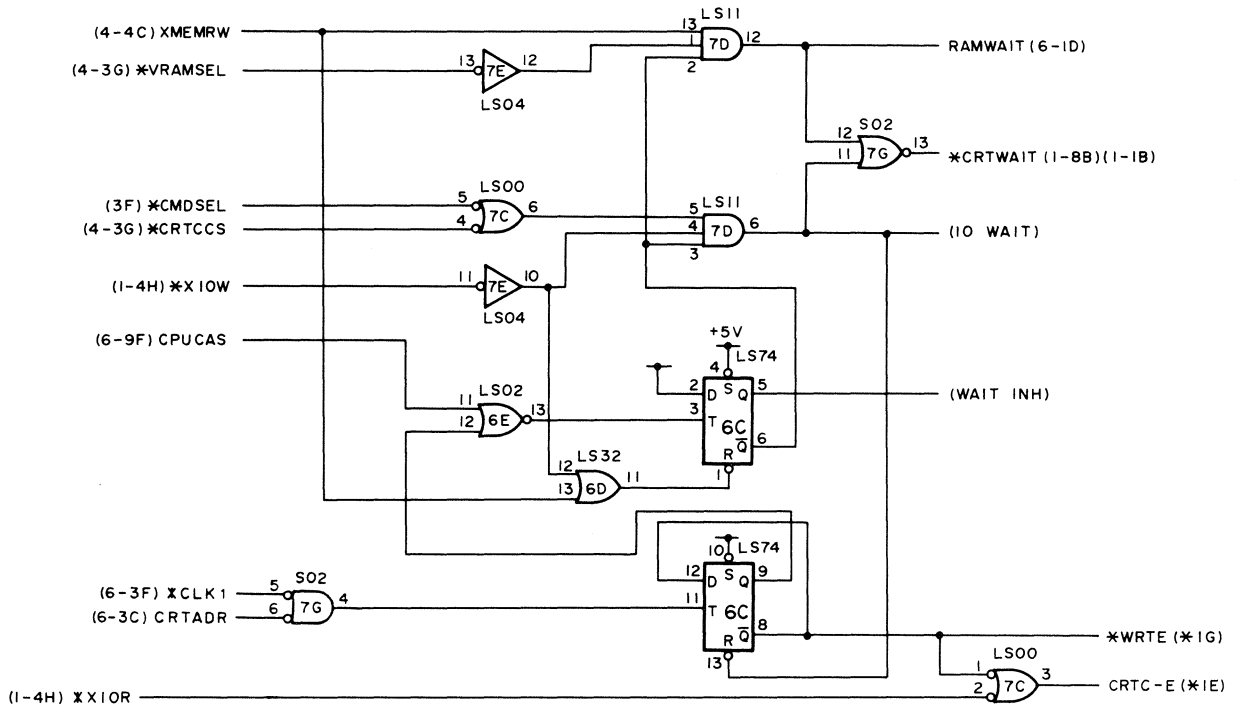


Figure 5-32 WAIT Circuit

(1) Wait during VRAM access

a) The WAIT circuit generates a RAM WAIT when VRAM is accessed for read/write. The WAIT circuit requests WAIT to the CPU or the DMAC by means of *CRT WAIT.

b) The access timing for VRAM changes from CRTC accessing to CPU (or DMAC) accessing. CPU CAS goes HIGH, then LOW. WAIT INH goes HIGH at the falling edge of CPU CAS.

c) When WAIT INH goes HIGH, *CRTC WAIT also goes HIGH thereby terminating the WAIT request. The CPU (or VRAM) also stops accessing VRAM.

d) Then, WAIT INH goes LOW and the RAM WAIT circuit is enabled.

(2) WAIT during I/O write

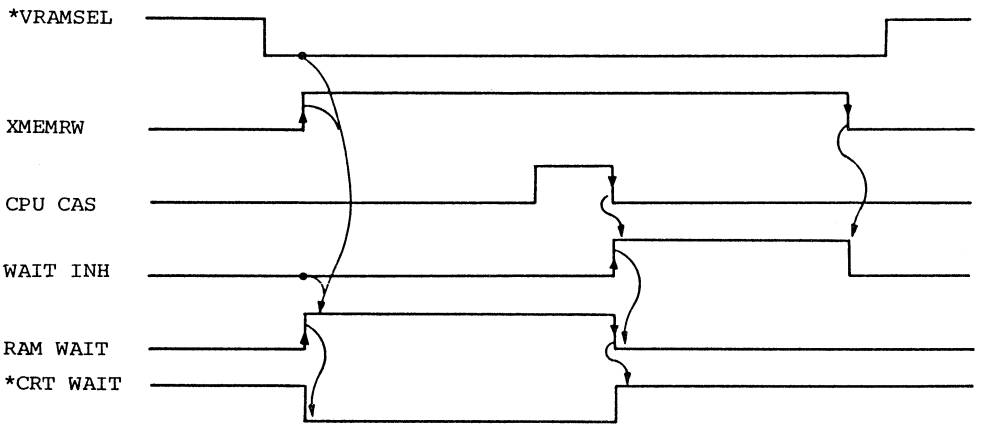
a) The WAIT circuit generates an I/O WAIT for an I/O write to the Display Mode register (or the CRTC). The circuit sends a WAIT to the CPU by means of *CRT WAIT.

b) *WRTE goes LOW, then HIGH in synchronization with CRTC. At the rising edge of *WRTE, WAIT INH goes HIGH.

c) Then, *CRTC WAIT goes HIGH and the WAIT request ends. The CPU also ends the I/O write operation.

d) WAIT INH then goes LOW and the I/O WAIT circuit is enabled.

o VRAM access timing chart



o I/O write timing chart

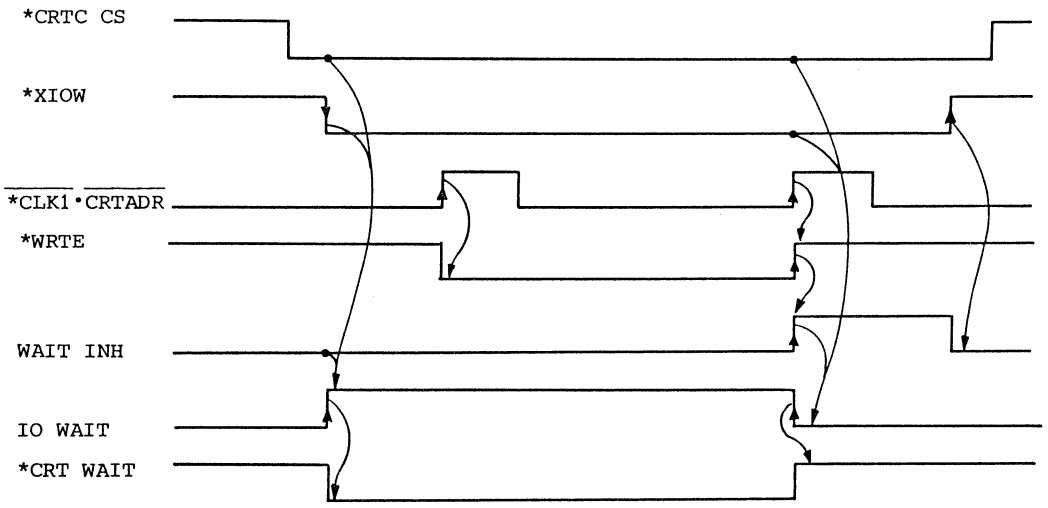


Figure 5-33 WAIT Circuit Timing Chart

(h) Timing generator

The timing generator generates and controls basic timing of the display circuit, CRTC clock pulses, VRAM access timing, RAS signal, and CAS signal. The following paragraphs describe the circuits that make up the timing generator block.

(1) Basic timing generator

The basic timing generator generates the clock pulses CLK1 to CLK4 (one eighth of the oscillator frequency) and the SHIFT clock pulse from the oscillator frequency (18.432 MHz). The generator also provides the RSCLK clock pulse (one tenth of the oscillator frequency) to the 8251.

Figure 5-34 shows the basic timing generator circuit and Figure 5-35 shows the signal timing.

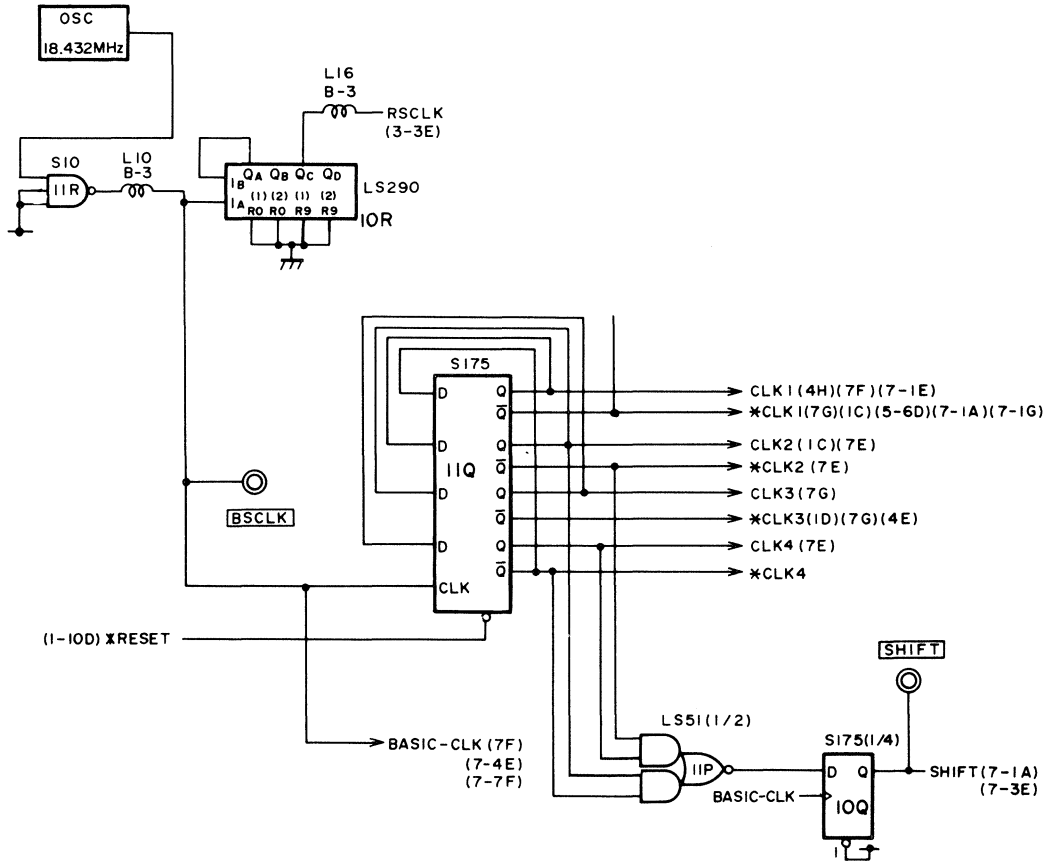


Figure 5-34 Timing Generator Circuit

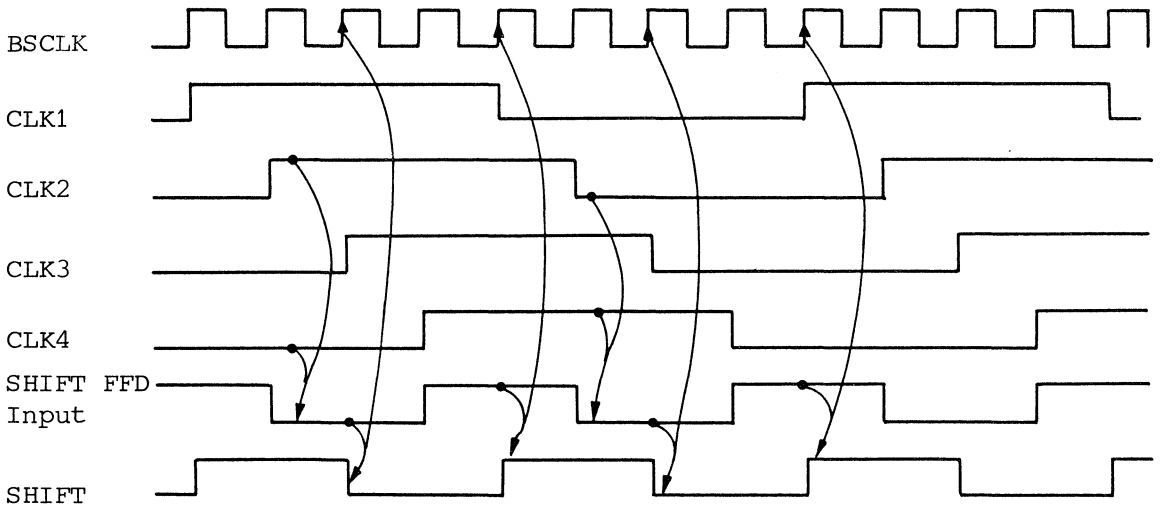


Figure 5-35 Timing Generator Timing Chart

(2) CRTC CLOCK control circuit

The CRTC clock control circuit controls clock pulses to be fed to the CLOCK input of the CRTC: clock pulses are 8 x BSCLK in the TEXT 80x25 display mode, and 16 x BSCLK in the other display modes. This circuit also generates the output enable signal EN EVEN for display latch data. The CRTC clock control circuit is shown below.

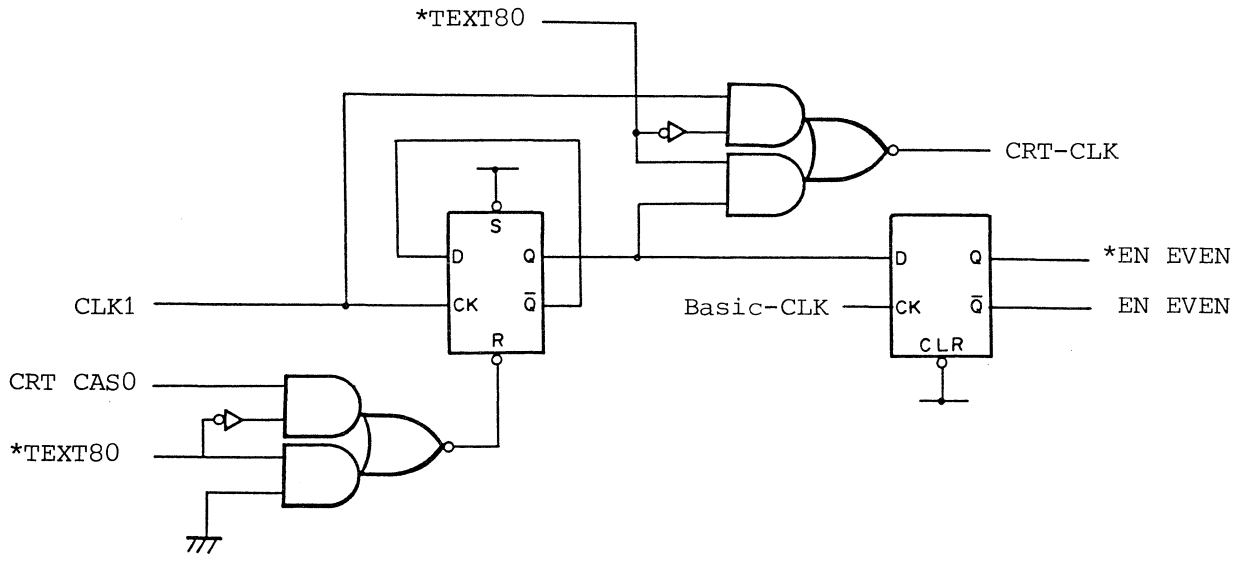


Figure 5-36 CRTC CLOCK Control Circuit

EN EVEN is synchronized to CRT Memory Access timing in the TEXT 80x25 display mode by CRT CASO. Signal timing is shown below.

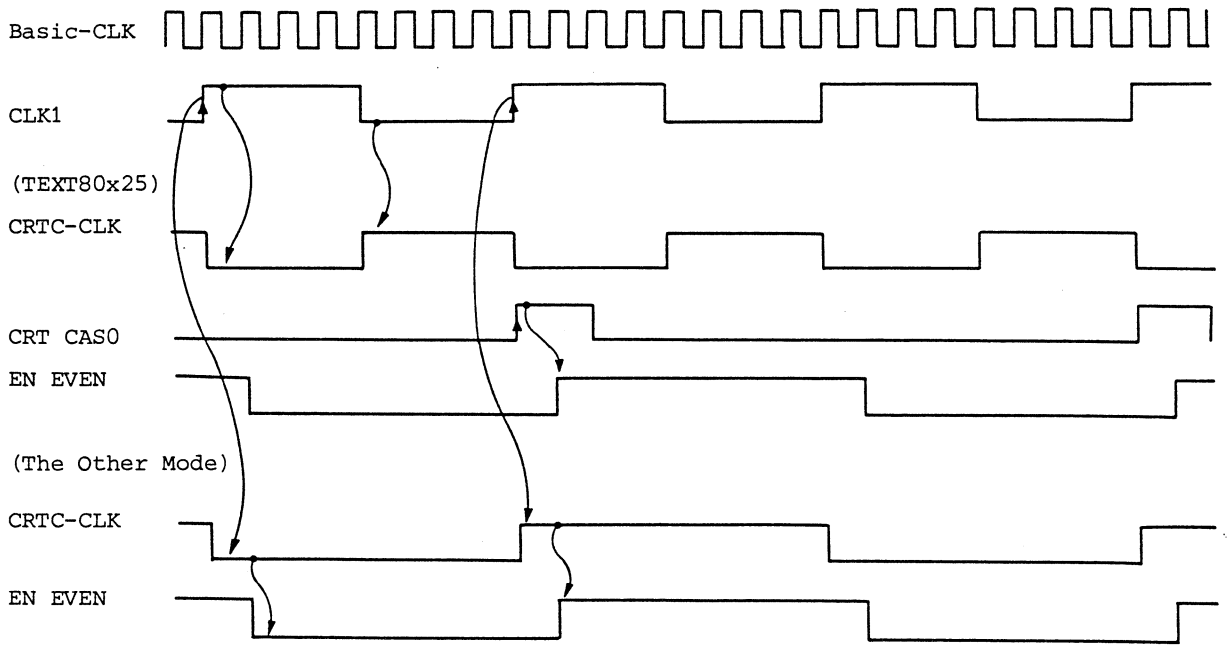


Figure 5-37 CRTC CLOCK Control Circuit Timing Chart

(3) VRAM access timing circuit

The VRAM access timing circuit controls the following:

- o VRAM access timing by the CRTC, CPU/DMAC
- o Refreshing
- o VRAM address multiplexer

The VRAM access timing circuit is shown below.

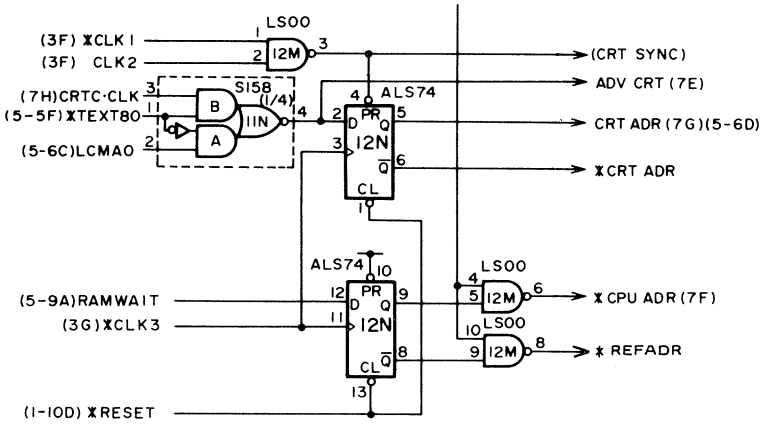


Figure 5-38 VRAM Access Timing Circuit

Output signals of the VRAM access timing circuit are:

a) CRT SYNC ..... LOW when VRAM access by the CRTC begins. Makes CATADR HIGH.

b) ADV CRT ..... Sampling signal to detect the end of the CRT cycle. Sampling starts at the rising edge of *CLK3. The CRT cycle ends when ADV CRT goes LOW.

c) CRT ADR ..... HIGH when the VRAM is accessed by the CRTC (CRT cycle). Enables the MA address output of the CRTC to the VRAM address.

d) *CPU ADR ..... LOW when VRAM is accessed by the CPU (CPU cycle). Enables the (X)AB address output of the CPU to VRAM address.

e) *REF ADR ..... LOW when VRAM is refreshed. Enables refresh RFA address output to the VRAM address.

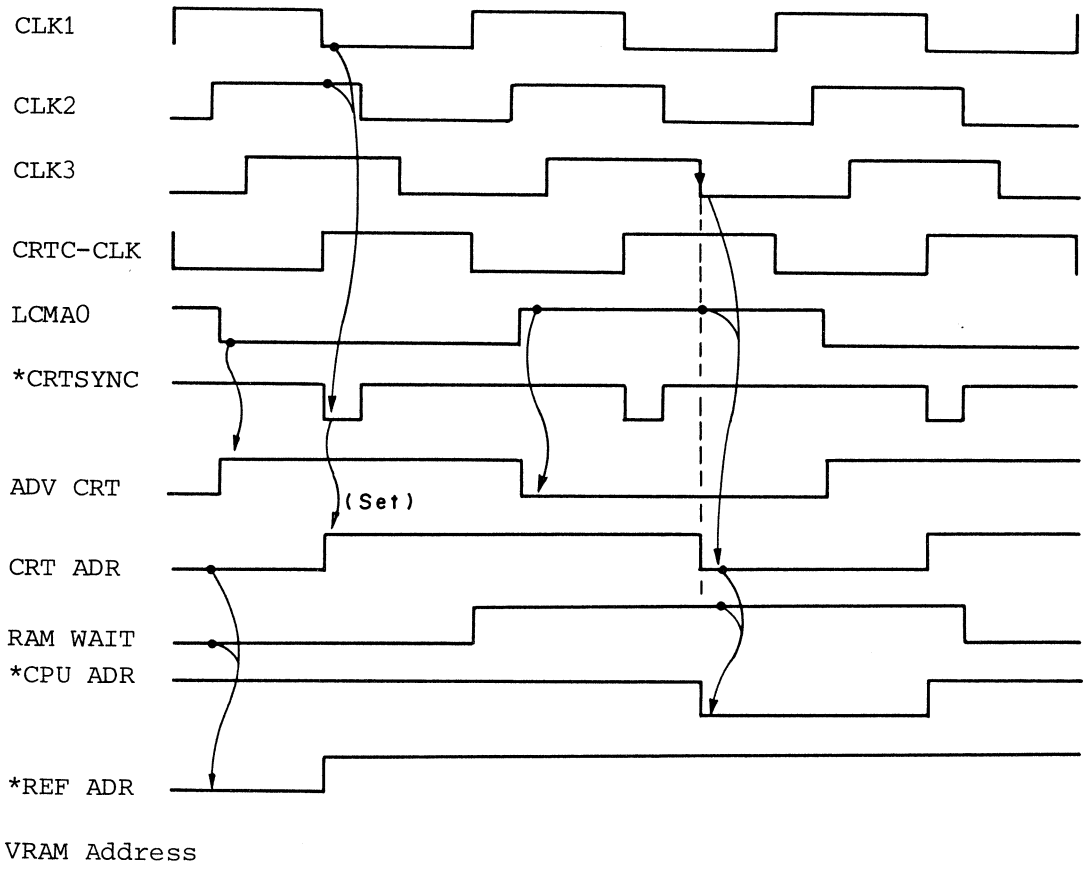


Figure 5-39 VRAM Access Timing Chart

(4) RAS, CAS timing circuit

The RAS, CAS timing circuit controls the RAS and CAS signals of VRAM according to the VRAM access timing. In the CRT cycle mode, the circuit performs a page mode read on RAM. In the CPU cycle mode, it performs a read or early write. In a refresh cycle, it performs a RAS-only refresh. Figure 5-40 shows the RAS, CAS timing circuit.

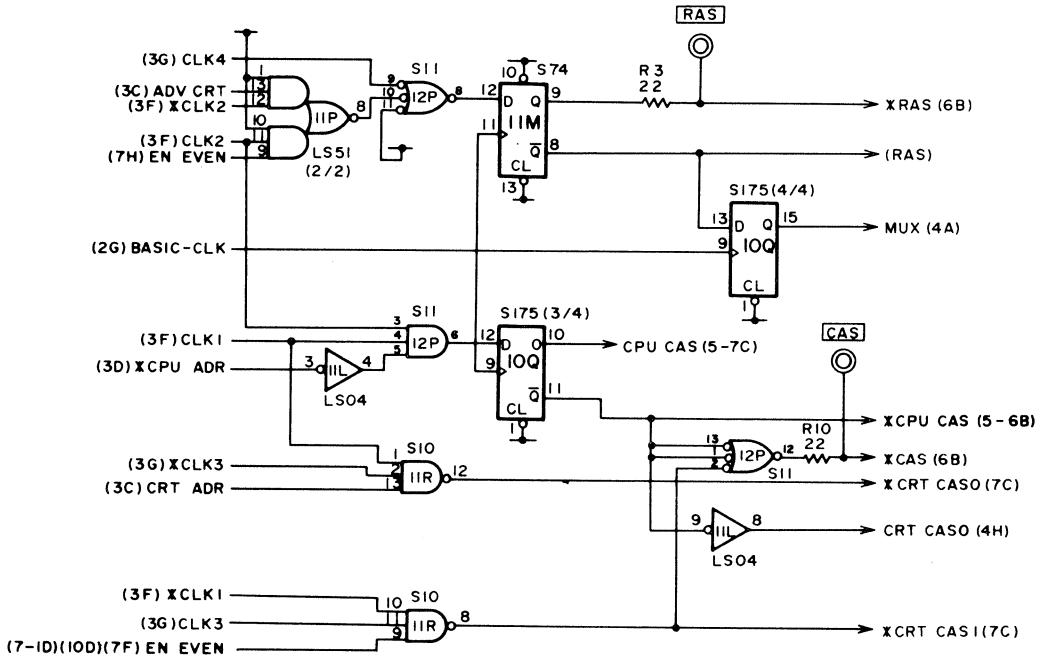


Figure 5-40 RAS, CAS Timing Circuit

Output signals are described below:

a) *RAS ..... A RAS input signal to VRAM; enabled at LOW. In the CRT cycle mode, the +RAS pulse width is read twice by page mode read; therefore, it is larger than the *RAS pulse width in the refresh cycle mode or in the CPU cycle mode in which Read/Write occurs only once.

b) MUX ..... A signal one pulse behind the RAS signal. It switches a low address to a column address or vice versa in the CRT cycle and CPU cycle modes. That is, low address when MUX goes LOW, and column address when MUX goes HIGH.

c) *CPU CAS ..... A *CAS signal to be output when VRAM is accessed in the CPU cycle mode.

d) *CRT CAS0 ..... The first *CAS output signal when VRAM is accessed in the CRT cycle mode.

e) *CRT CAS1 ..... The second *CAS output signal when VRAM is accessed in the CRT cycle mode.

f) *CAS ..... A CAS input signal to VRAM; enabled at low. Two *CAS signals, i.e., *CRT CAS0 and *CRT CAS1, are output in the CRT cycle mode. Only the *CPU CAS signal is output in the CPU cycle mode. No *CAS signals are output in the refresh cycle mode.

Figure 5-41 shows the timing chart.

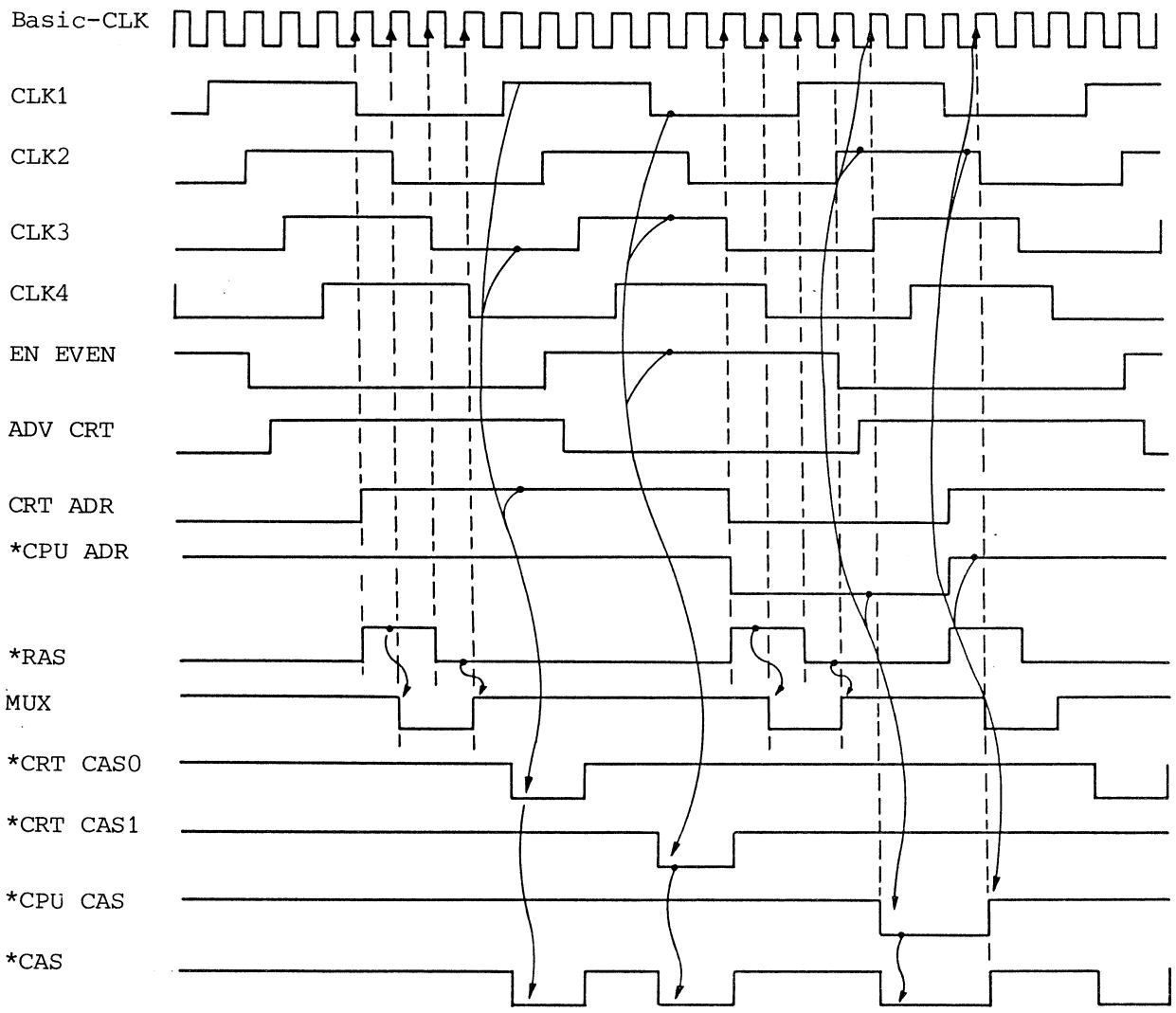


Figure 5-41 RAS, CAS Timing Chart

(i) CRTC

CRTC usually controls the raster scan CRT display. In this display circuit, however, it controls the plasma display.

(j) VRAM address control circuit

The VRAM address control circuit outputs XAB and AB addresses from CPU or DMAC, CMA and RA addresses from CRTC, and refresh RFA address to the VRAM address bus in synchronization with the VRAM access timing.

The circuit consists of a VRAM address MPX, CRTC address selector, and refresh address counter. Figure 5-42 shows block diagram.

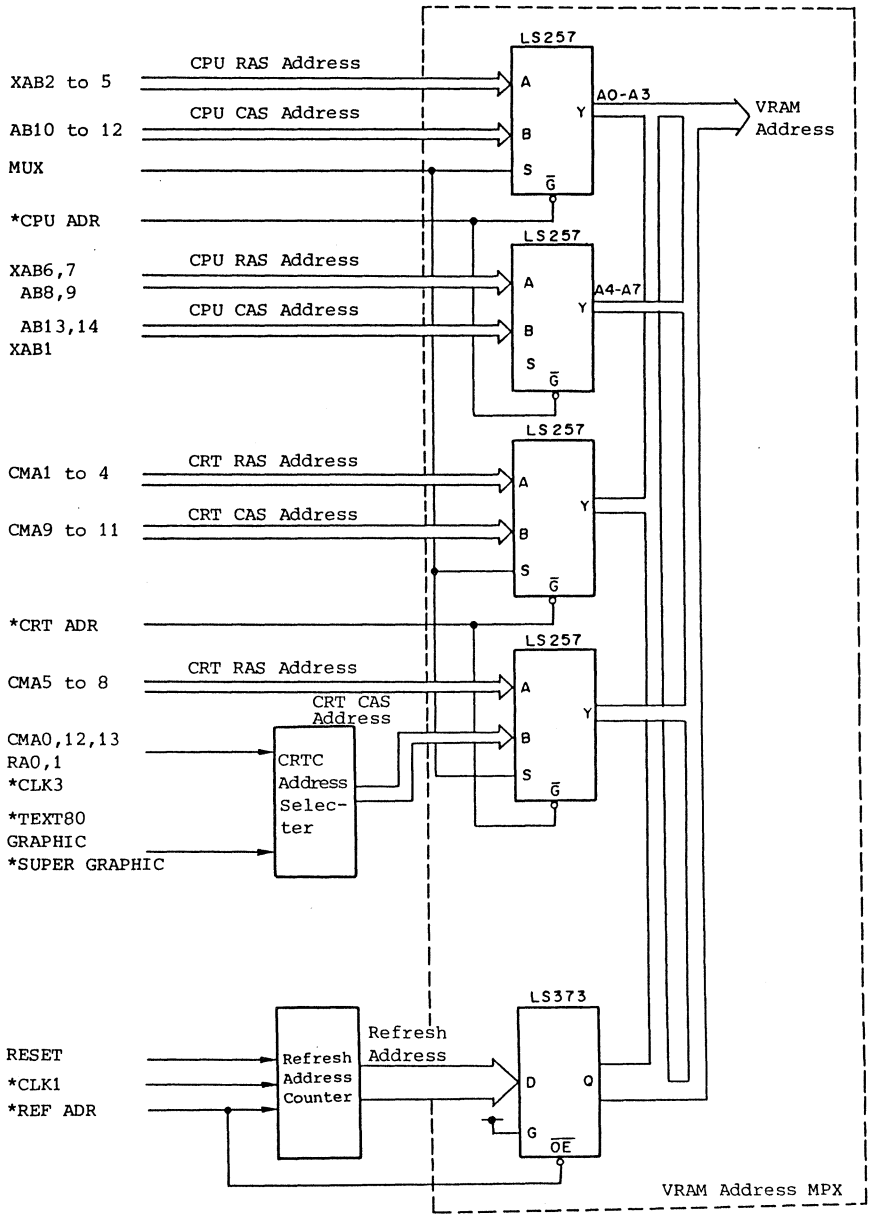


Figure 5-42 VRAM Address Control Circuit

Each circuit operation is described below:

(1) VRAM address MPX

Each address output to the VRAM address bus is controlled by the *CPU ADR, *CRT ADR, and *REF ADR signals that are output by the VRAM access timing circuit. Selection of the RAS address or the CAS address is made by the MUX output signal from the RAS/CAS timing circuit. Table 5-4 shows addresses and corresponding VRAM addresses.

Table 5-4

CPU Address		AB 0	AB 1	AB 2	AB 3	AB 4	AB 5	AB 6	AB 7	AB 8	AB 9	AB 10	AB 11	AB 12	AB 13	AB 14
CRTC ADDRESS	40x25 TEXT	-	MA 0	MA 1	MA 2	MA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11	MA 12	MA 13
	80x25 TEXT	-	CK	MA 1	MA 2	MA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11	MA 12	MA 13
	320x200 GRAPHIC	-	MA 0	MA 1	MA 2	MA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11	RA 12	RA 13
	640x200 GRAPHIC	-	MA 0	MA 1	MA 2	MA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11	RA 12	RA 13
	640x400 GRAPHIC	-	MA 0	MA 1	MA 2	MA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11	RA 12	RA 13
REFRESH ADDRESS		-	-	RF 0	RF 1	RF 2	RF 3	RF 4	RF 5	RF 6	RF 7	-	-	-	-	-
D-RAM ADDRESS		*	C 6	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	C 1	C 2	C 3	C 4	C 5

*: Chip select (AB0 only is valid)
RF: REFRESH ADDRESS
CK: CKL3
C: Column address
R: Row address

Figure 5-43 shows an operation timing chart.

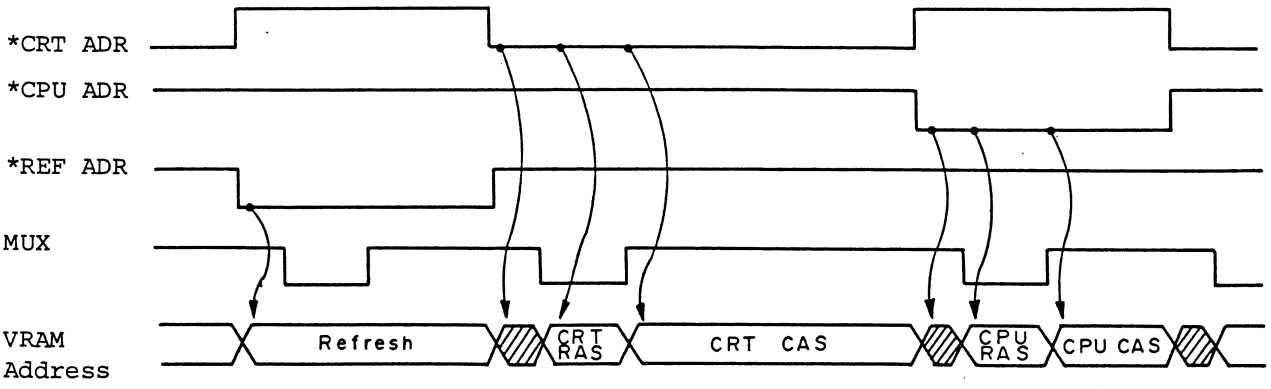


Figure 5-43 VRAM Address Control Circuit Timing Chart

(2) CRTC address selector

The CRTC address selector changes the relationship between the CPU addresses and the CRTC addresses. Figure 5-44 shows the CRTC address selector circuit.

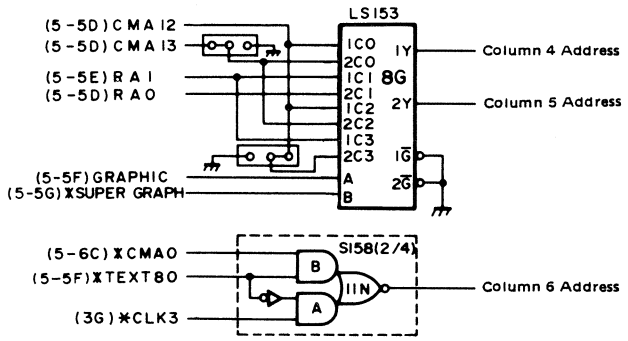


Figure 5-44 CRTC Address Selector Circuit

(3) Refresh address counter

The refresh address counter increments the VRAM refresh address count each time a refresh cycle ends. Figure 5-45 shows a refresh address counter circuit.

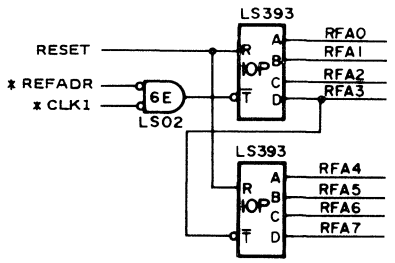


Figure 5-45 Refresh Address Counter Circuit

Figure 5-46 shows an operation timing chart.

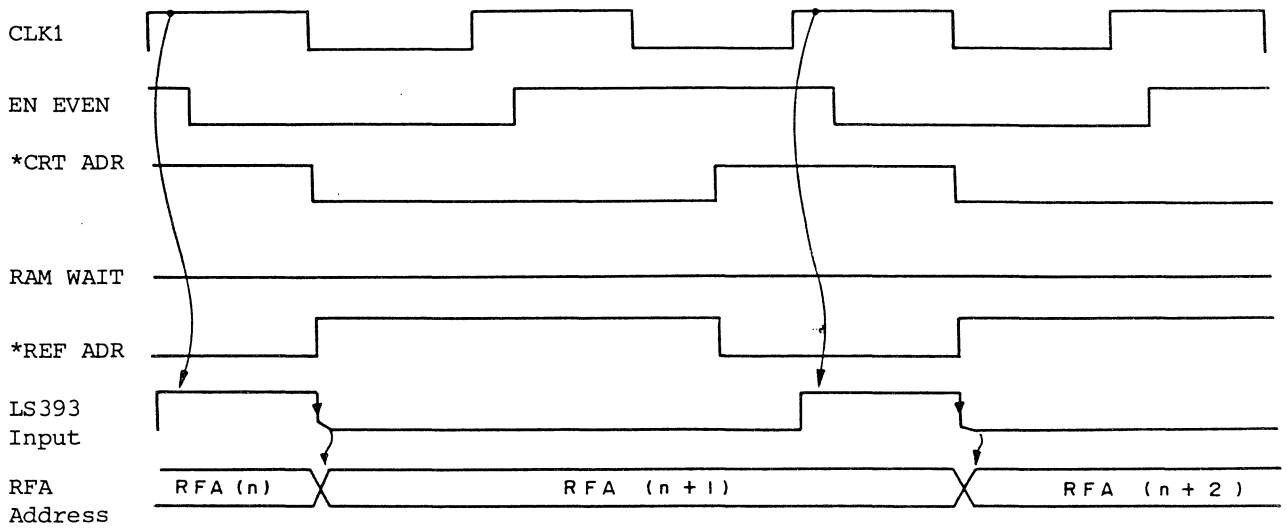


Figure 5-46 Refresh Address Counter Timing Chart

(k) VRAM data bus circuit

The VRAM data bus circuit consists of an even-numbered address memory block and an odd-numbered address memory block. Each of these blocks consists of 2 memory chips, 1 bus transceiver, and 2 data latches. Figure 5-47 shows a VRAM data bus circuit block diagram.

(1) VRAM

The VRAM has four 16K-word x 4-bit memory chips with a total capacity of 32K bytes. The CPU or DMAC accesses the even-address memory block of VRAM if the address is an even-numbered address (XAB0 = 0), or the odd-address memory block of VRAM if it is an odd-numbered address (XAB = 1). A bidirectional transceiver (LS245) is provided between the VRAM data bus and data bus lines VD0 to VD7. When reading VRAM, data is transferred from the VRAM data bus to data bus lines VD0 to VD7. When writing to VRAM, data is transferred in the opposite direction. The direction is controlled by the *VRAM WR signal.

(2) CRTC access to VRAM

In accessing VRAM from CRTC, an even address (address n) and an odd address (address n + 1) in VRAM are read simultaneously, and are latched to the first data latch at the rising edge of the *CRT CAS1 signal.

In the CRTC cycle mode, VRAM is read twice by page mode read; hence, the next even address (n + 2 address) and odd address (n + 3 address) are read, and latched to the second data latch at the rising edge of the *CRT CAS0 signal.

Except when the display mode is other than TEXT 80x25, the second and first memory addresses are the same; therefore, both read data are the same.

The latched even address data is output to data bus lines CHB0 to CHB7, and the latched odd address data to data bus lines ATB0 to ATB7. The first data latch and second data latch are switched from one to the other by the EN EVEN signal. In the graphic display mode, however, the first data latch is not output to data bus lines ATB0 to ATB7. Figures 5-48 and 5-49 show operation timing diagrams.

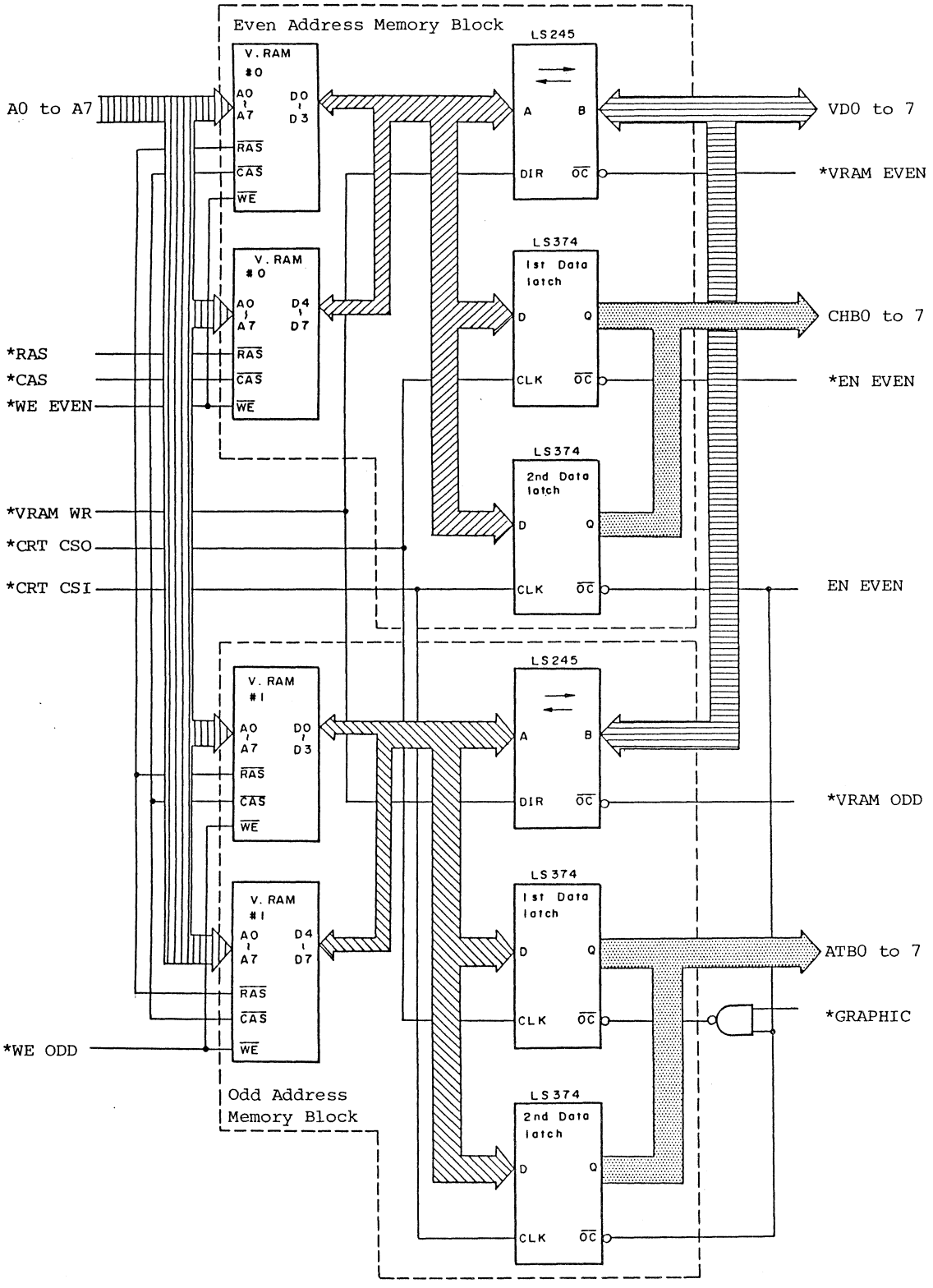


Figure 5-47 VRAM Address Block Diagram

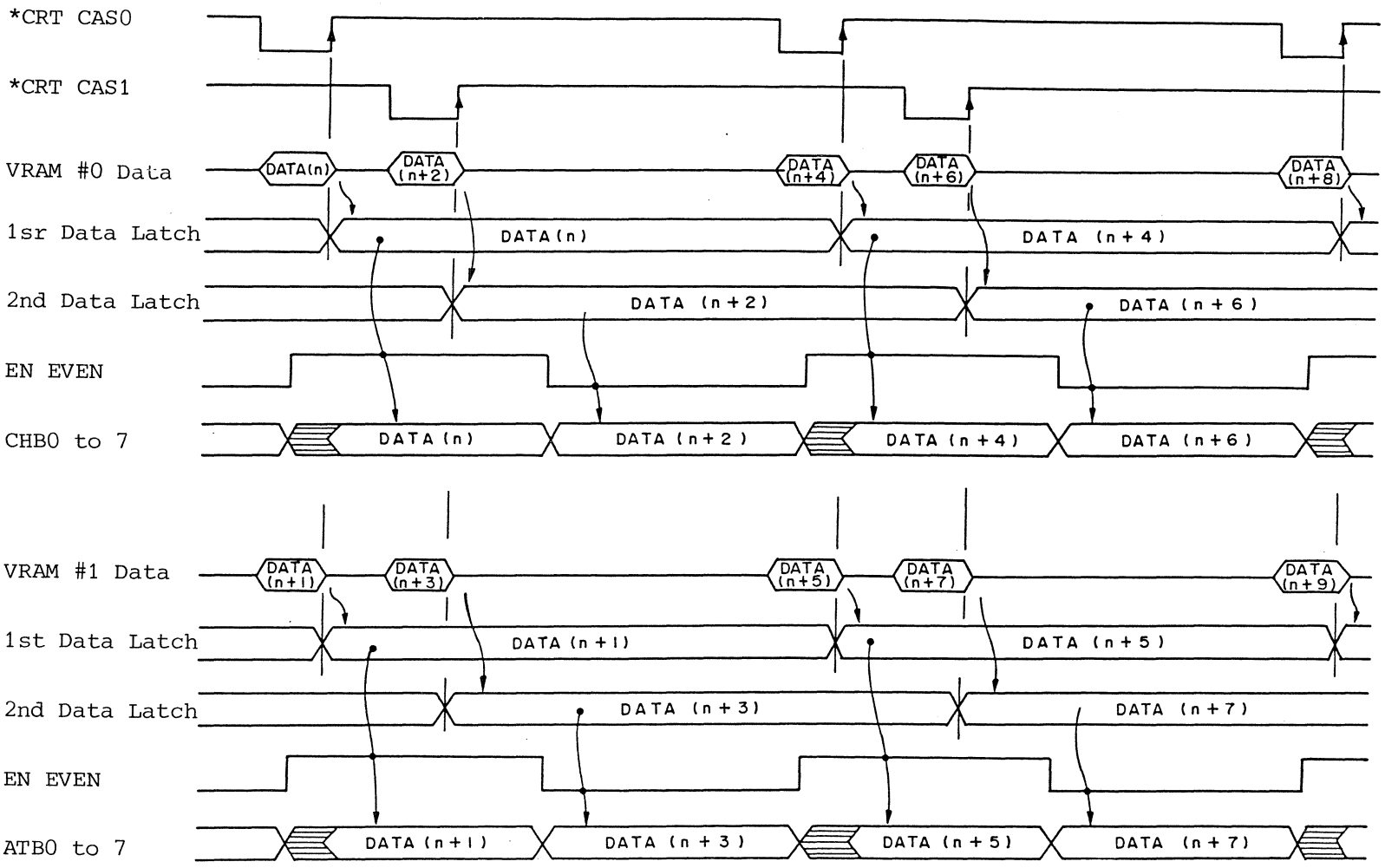


Figure 5-48 Timing Waveforms (TEXT 80x25)

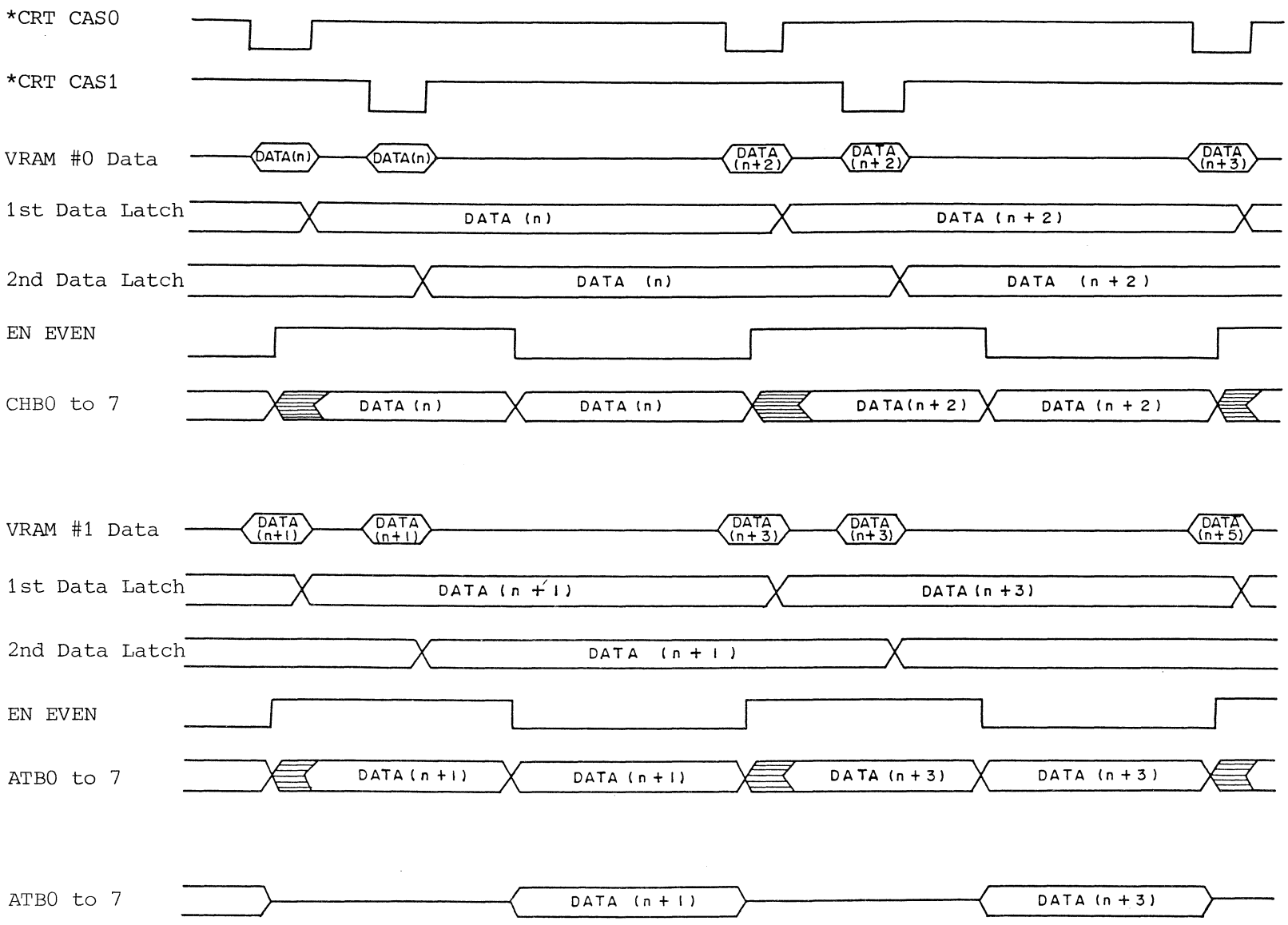


Figure 5-49 Timing Waveform (Not TEXT 80x25)

(ℓ) CHG font data latch circuit

In the TEXT display mode, the CHG font data latch circuit converts the character code on data bus lines CHB0 to CHB7 into individual font data and latches the converted data. The data is latched at the rising edge of the *CRTC-CLK signal, and output to LCHG0 to LCHG7. Figure 5-50 shows a CHG font data latch circuit.

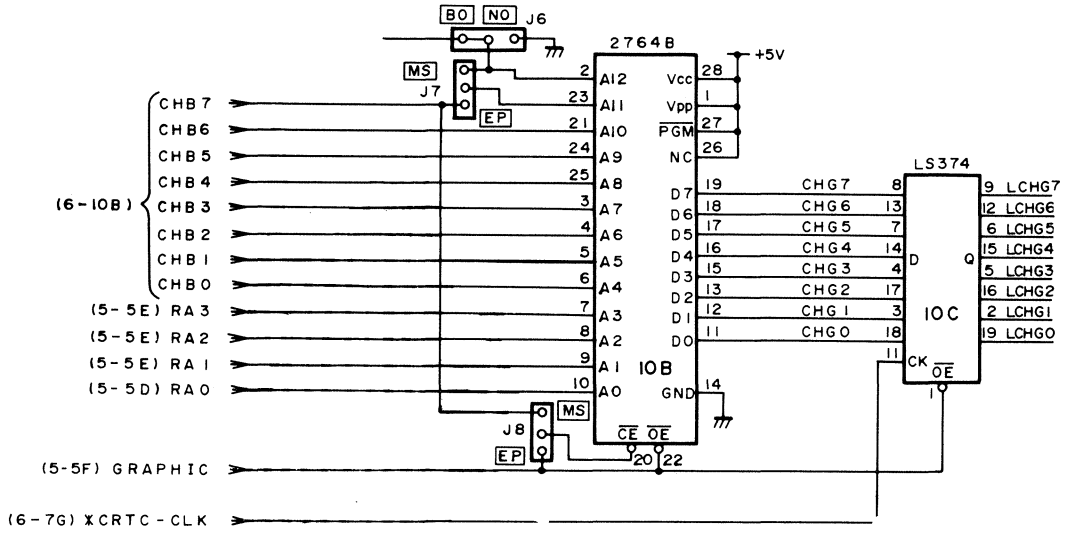


Figure 5-50 CHG Font Data Latch Circuit

The CHG (character generator) has two fonts, single font and bold font, each consisting of characters in an 8-dot x 16-dot character matrix. The single font and bold font are switched by the foreground intensity bit (AT3) of the attribute code. The single font is selected by AT3 = 0, and the bold font by AT3 = 1.

Connecting jumper J6 to B0 allows the bold font to be selected (AT3 = 1), and connecting it to NO inhibits the bold font. Jumper J6 is connected to B0 when shipped from the factory.

Short plugs J7 and J8 allow selection of either the 28-pin EP-ROM or the 24-pin mask ROM for the CHG. Connect them to EP to select EP-ROM, or to MS to select 24-pin mask ROM.

(m) Graphic data mix, data latch

The graphic data mix, data latch circuit combines the even address with the odd address in the GRAPHIC display mode, and latches the combined data. The data is latched at the rising edge of CLK1, and output to LCHG0 to LCHG7.

Figure 5-51 shows a graphic data mix, data latch circuit diagram.

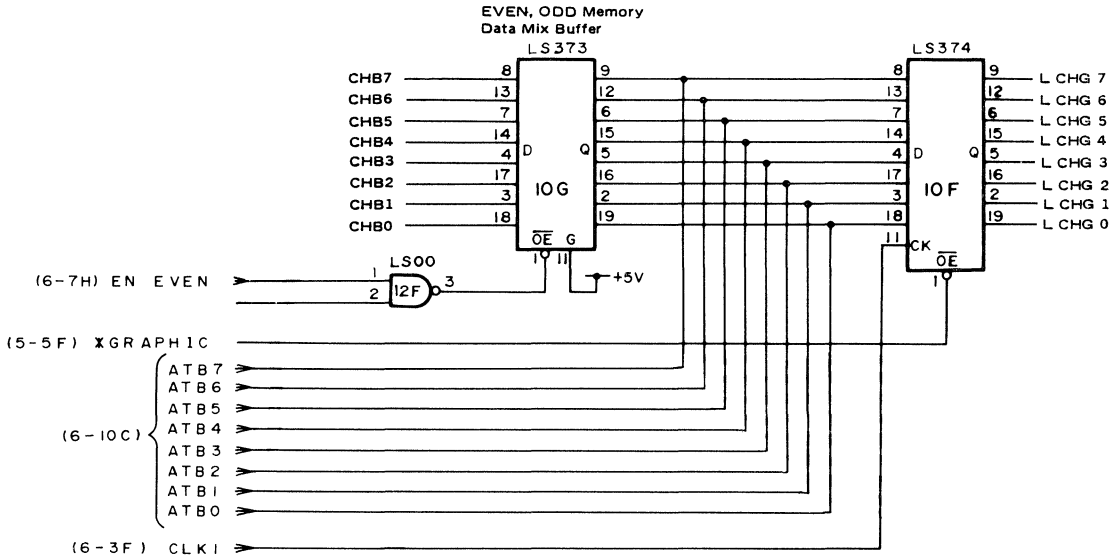


Figure 5-51 Graphic Data Mix, Data Latch Circuit

Figure 5-52 shows an operation timing chart.

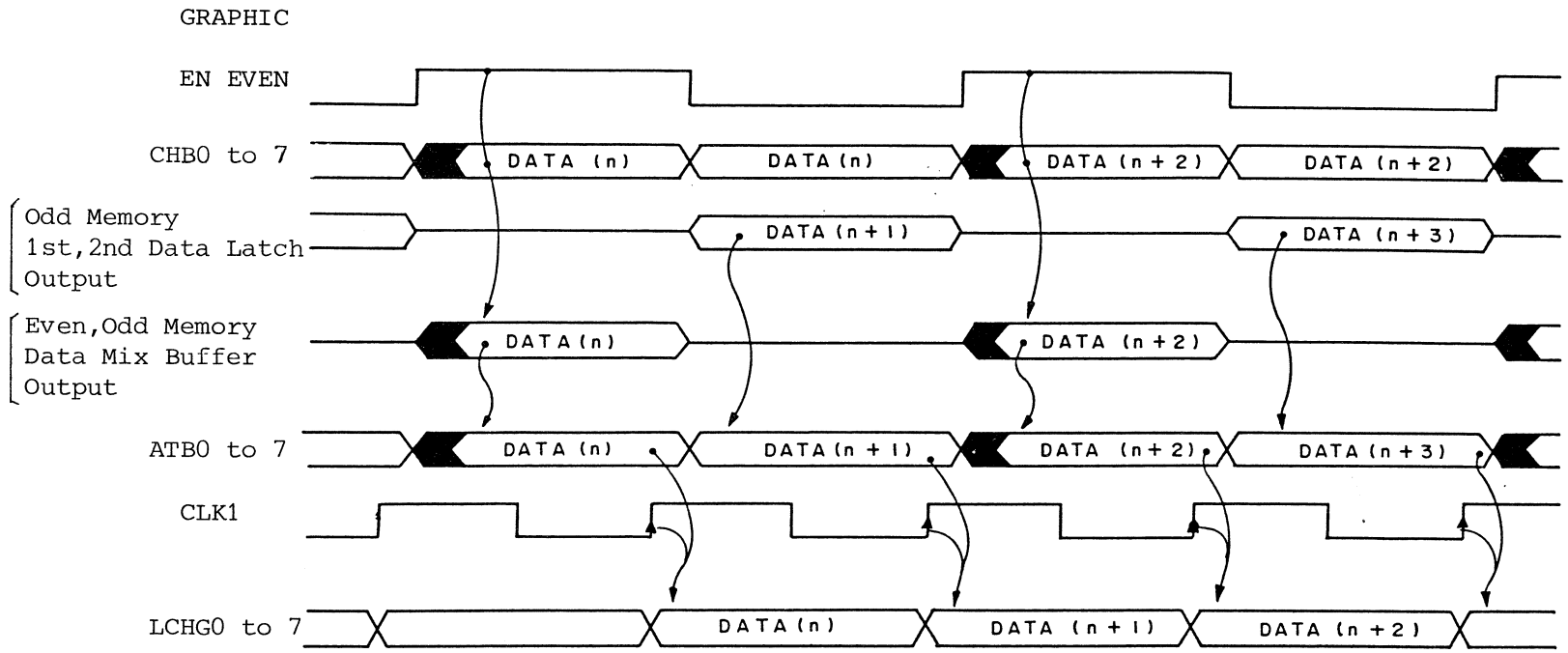


Figure 5-52 Graphic Data Mix, Data Latch Timing Chart

(n) Attribute decoder

In the TEXT display mode, the attribute decoder decodes the attribute code to obtain display modes for the plasma display: normal, reverse, non-display, full-dot character matrix, or blinking. The decoded data are latched to LS174 at the rising edge of *CRTC-CLK.

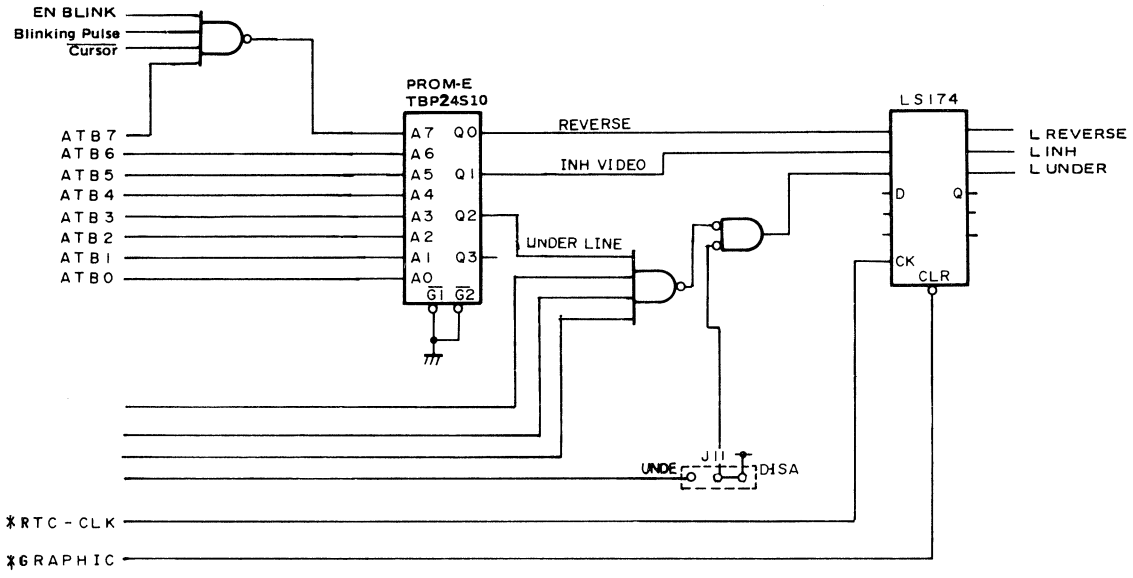


Figure 5-53 Attribute Decoder Circuit

Underlined display can be enabled or disabled by short plug J11. It is disabled when shipped from the factory.

(o) Video data control circuit

In the TEXT display mode, the video data control circuit converts font data and decoded attribute data to video data. In the GRAPHIC display mode, it converts graphic data to video data to be output to the plasma display. The converted video data is latched to the video data latch at the rising edge of the SHIFT signal.

Figure 5-54 shows a video data control circuit diagram.

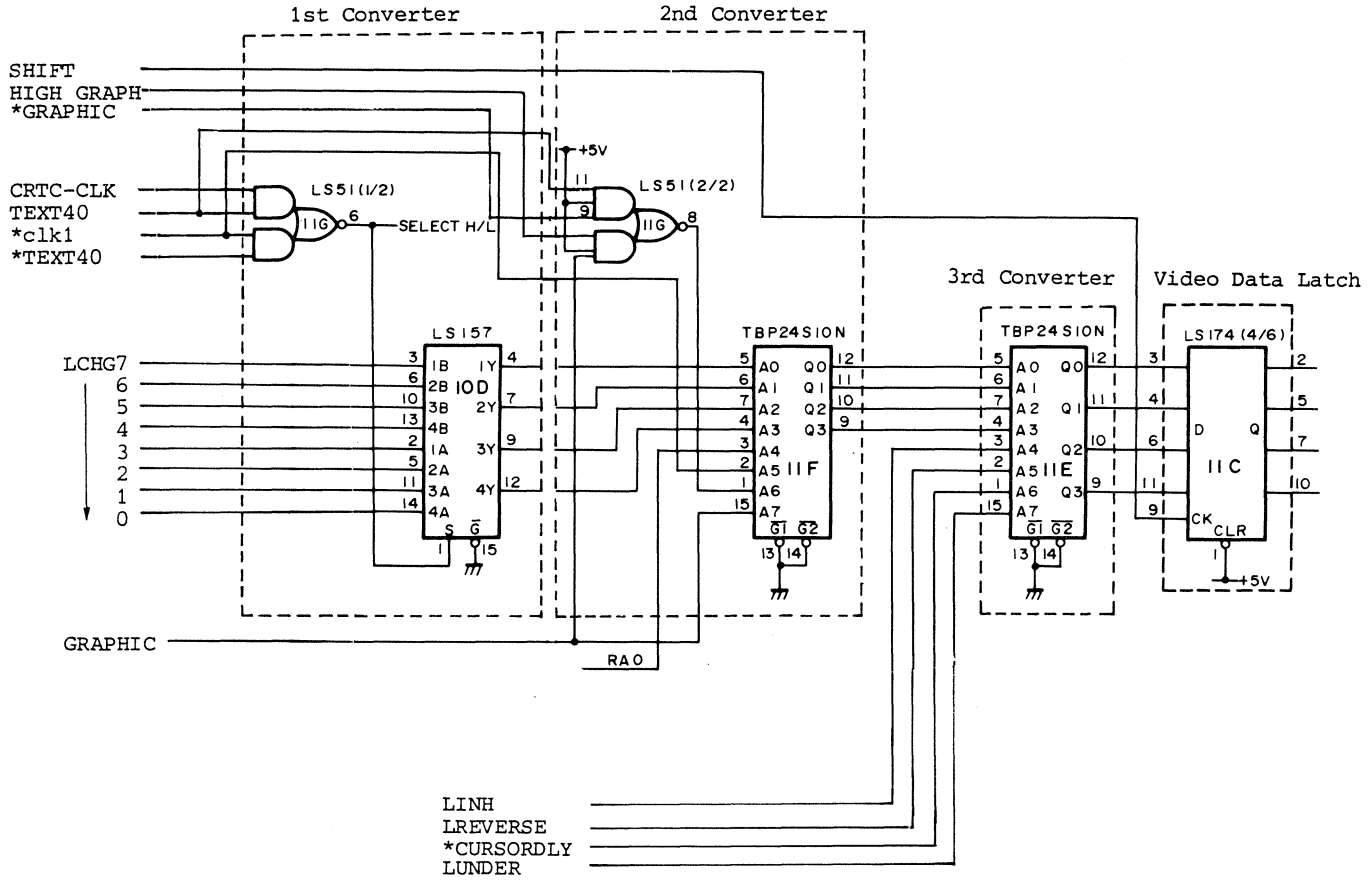
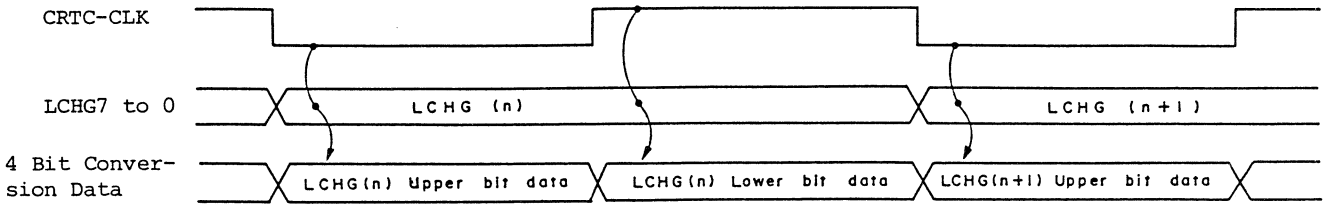


Figure 5-54 Video Data Control Circuit

(1) First converter

The first converter converts 8-bit data (LCHG7 to LCHG0) to 4-bit data. First, the upper 4 bits (LCHG7 to LCHG4) are sent, followed by the lower 4 bits (LCHG3 to LCHG0). Switching between the upper 4 bits and the lower 4 bits is done by the CRTC-CLK signal in the TEXT 40x25 display mode, or by the *CLK1 signal in other display modes. Figure 5-55 shows an operation timing chart.

o TEXT 40x25 Display Mode



o Other Display Modes

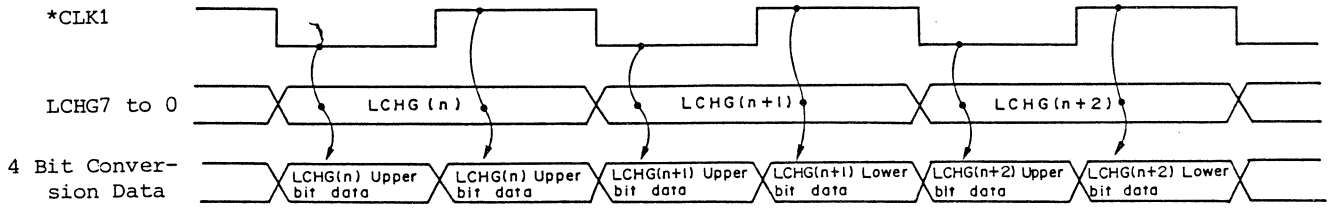


Figure 5-55 First Converter Timing Chart

(2) Second converter

The second converter enlarges each bit of 4-bit data, doubling it for conversion to 8-bit data in the TEXT 40x25 display mode. In the GRAPHIC 320x200 display mode, it converts the data to dot patterns according to the dot code (C0, C1) and raster address RA0.

No data conversion takes place in other display modes. Table 5-5 shows a conversion table.

Table 5-5 VIDEO1 ROM Data

VIDEO1 Function	Mode Condition Input				Video Data Input				VIDEO1 ROM Output			
	A7	A6	A5	A4	A3	A2	A1	A0	Q3	Q2	Q1	Q0
	GRAPHIC	*TEXT40 or *HIGH GRAPH	*CLK1	RA0	MD3	MD2	MD1	MD0	ND3	ND2	ND1	ND0
TEXT 40 (1st Data)	0	0	0	0	MD3	MD2	MD1	MD0	MD1	MD1	MD0	MD0
"	0	0	0	1	MD3	MD2	MD1	MD0	MD1	MD1	MD0	MD0
TEXT 40 (2nd Data)	0	0	1	0	MD3	MD2	MD1	MD0	MD3	MD3	MD2	MD2
"	0	0	1	1	MD3	MD2	MD1	MD0	MD3	MD3	MD2	MD2
TEXT 80	0	1	0	0	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"	0	1	0	1	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"	0	1	1	0	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"		1	1	1	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
GRAPH 640	1	0	0	0	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"	1	0	0	1	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"	1	0	1	1	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
"	1	0	1	1	MD3	MD2	MD1	MD0	MD3	MD2	MD1	MD0
GRAPH 320 EVEN RASTER	1	1	0	0	MD3	MD2	MD1	MD0	x MD2 MD3	+ MD2 MD3	x MD0 MD1	+ MD0 MD1
GRAPH 320 ODD RASTER	1	1	0	1	MD3	MD2	MD1	MD0	x MD2 MD3	MD3	x MD0 MD0	MD1
GRAPH 320 EVEN RASTER	1	1	1	0	MD3	MD2	MD1	MD0	x MD2 MD3	+ MD2 MD3	x MD0 MD1	+ MD0 MD1
GRAPH 320 ODD RASTER	1	1	1	1	MD3	MD2	MD1	MD0	x MD2 MD3	MD3	x MD0 MD1	MD1

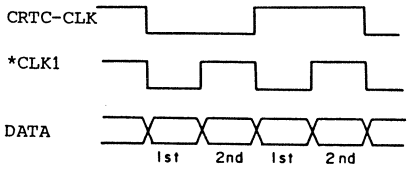
For dot pattern control in the GRAPHIC 320 mode

For dot enlarging in the TEXT 40 mode

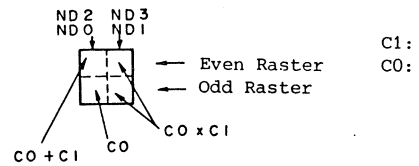
In the TEXT mode: *TEXT 40 (to control TEXT 40 and TEXT 80)
In the GRAPHIC mode: *HIGH GRAPH (to control GRAPHIC 320 and GRAPHIC 640)

To control TEXT and GRAPHIC

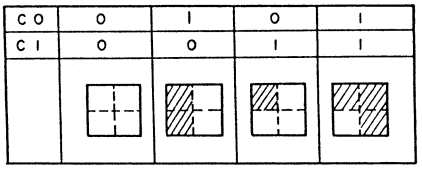
o For TEXT 40



o For GRAPHIC 320



C1: MD0, MD2
C0: MD1, MD3



(3) Third converter

The third converter converts font data to video data according to decoded attribute data in the TEXT display mode. No data conversion takes place in the GRAPHIC display mode.

Table 5-6 shows a conversion table.

Table 5-6 VIDEO2 ROM Data

Attribute Decode & Cursor Input				Video DATA Input				VIDEO2 ROM Output					Comment
A7	A6	A5	A4	A3	A2	A1	A0	Q3	Q2	Q1	Q0	HEX	
UNDER LINE DELAY	CURSOR DELAY	REVERSE DELAY	INHIBIT VIDEO DELAY	ND3	ND2	ND1	ND0	VID3	VID2	VID1	VID0		
0	0	0	0	ND3	ND2	ND1	ND0	1	1	1	1	F	Cursor in normal
0	0	0	1	ND3	ND2	ND1	ND0	1	1	1	1	F	Cursor in non-display
0	0	1	0	ND3	ND2	ND1	ND0	0	0	0	0	0	Cursor in reverse
0	0	1	1	ND3	ND2	ND1	ND0	1	1	1	1	F	Cursor in full dots
0	1	0	0	ND3	ND2	ND1	ND0	ND3	ND2	ND1	ND0	ND	Normal
0	1	0	1	ND3	ND2	ND1	ND0	0	0	0	0	0	Non-display
0	1	1	0	ND3	ND2	ND1	ND0	$\overline{ND3}$	$\overline{ND2}$	$\overline{ND1}$	$\overline{ND0}$	$\overline{ND}$	Reverse
0	1	1	1	ND3	ND2	ND1	ND0	1	1	1	1	F	Full dots
1	0	0	0	ND3	ND2	ND1	ND0	1	1	1	1	F	Under-line in normal
1	0	0	1	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)
1	0	1	0	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)
1	0	1	1	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)
1	1	0	0	ND3	ND2	ND1	ND0	1	1	1	1	F	Cursor in normal with underline
1	1	0	1	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)
1	1	1	0	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)
1	1	1	1	ND3	ND2	ND1	ND0	1	1	1	1	F	(Impossible)

(p) CRTC control signal converter circuit

The CRTC control signal converter circuit converts control signals DISPTMG, CURSOR, HSYNC, and VSYNC, all output from CRTC, and adjusts the display timing.

Each of these signals is described below.

(1) DISPTMG, CURSOR circuit

The DISPTMG, CURSOR circuit synchronizes the DISPTMG and CURSOR signals (output from CRTC) with video data.

Figure 5-56 shows the circuit diagram.

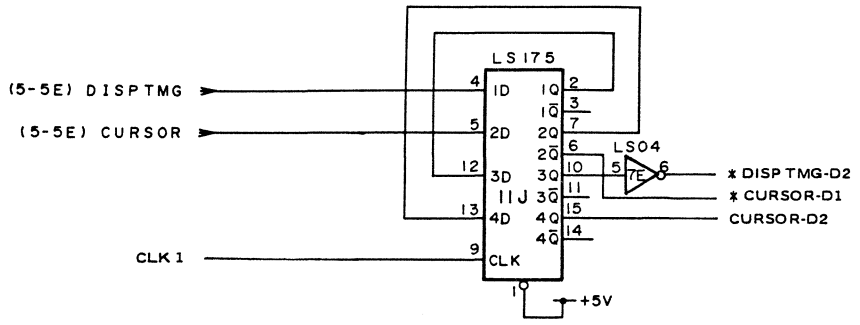


Figure 5-56 CRTC Control Signal Converter Circuit

(2) HSYNC circuit

The HSYNC circuit receives the HSYNC signal from CRTC and generates from it an HSYNC DLY signal (to be output to the plasma display) and a status signal HSYNC STA.

Figure 5-57 shows an HSYNC circuit diagram.

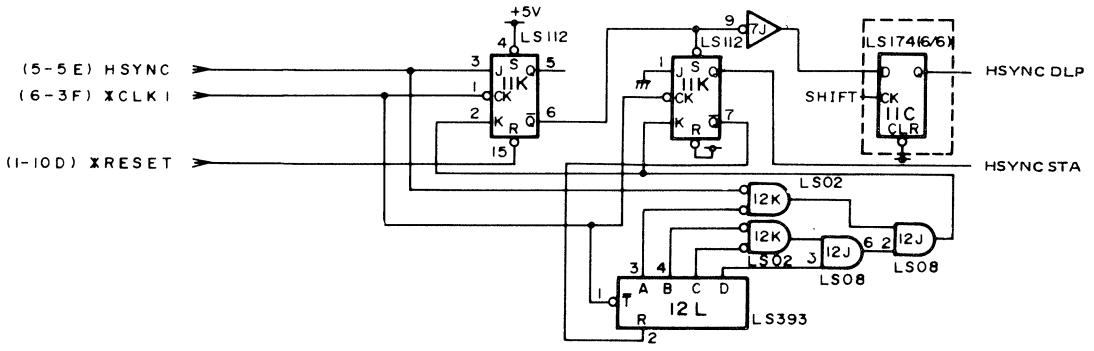


Figure 5-57 HSYNC Circuit

(3) VSYNC circuit

The VSYNC circuit receives the VSYNC signal from CRTC and generates from it a VSYNC DLY signal (to be output to the plasma display).

Figure 5-58 shows VSYNC circuit diagram.

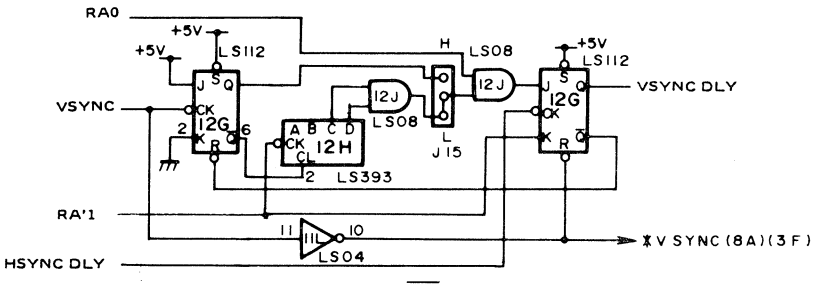


Figure 5-58 VSYNC Circuit

(q) Blink timing circuit

The blink timing circuit controls the blink timing of characters and cursor in the TEXT display mode. Both the cursor blink signal and character blink signal have the duty cycle of 50%. The cursor blink period is 16 fields and the character blink period is 32 fields. Figure 5-59 shows a blink timing circuit diagram.

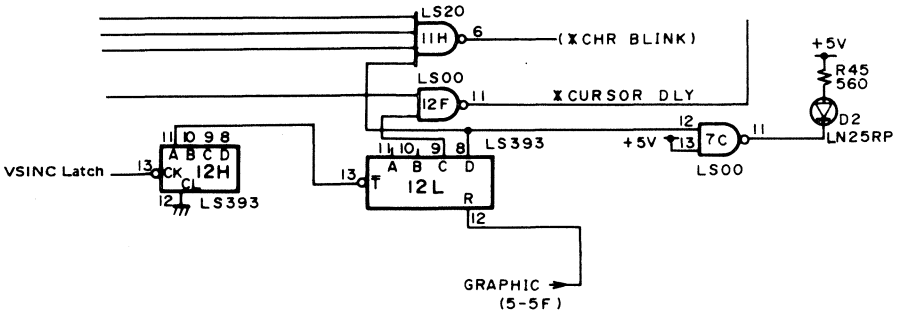


Figure 5-59 Blink Timing Circuit

Figure 5-60 shows an operation timing chart.

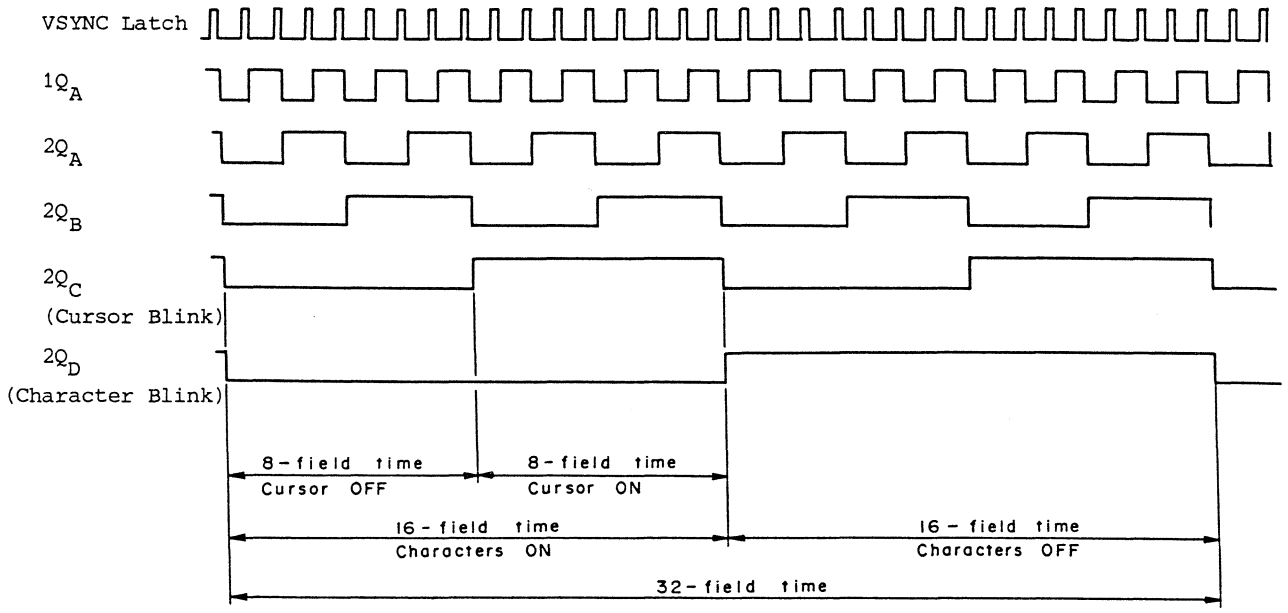


Figure 5-60 Blink Timing Timing Chart

(r) Plasma driver circuit

The plasma driver circuit outputs the signals generated at the display control circuit to the plasma via driver LS240. Each data line has a 47 k-ohm pullup resistance.

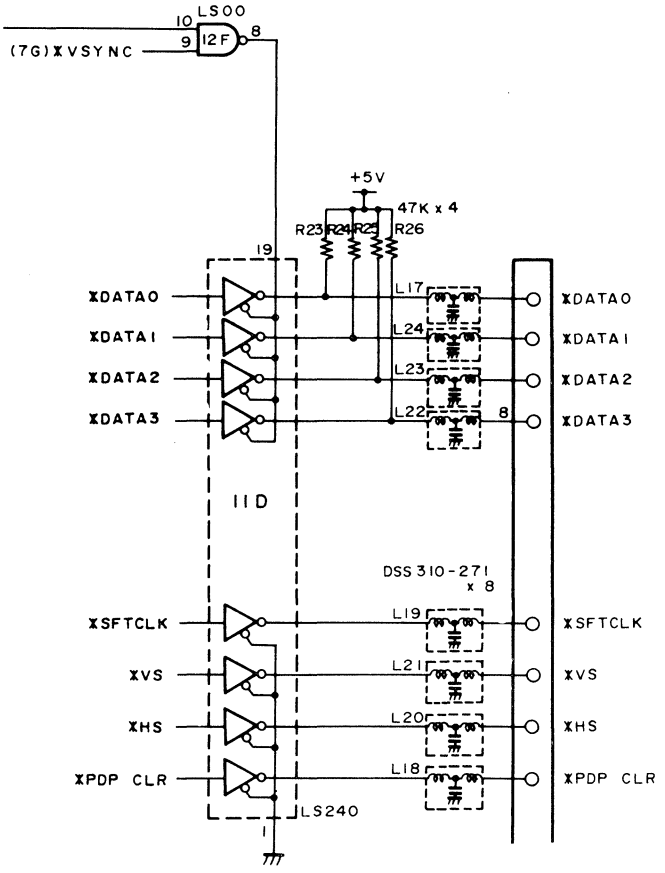


Figure 5-61 Plasma Driver Circuit

DATA0 to DATA3 output lines are enabled when both the EN VIDEO signal in the display mode register and the vertical sync signal (*VSYNC) are HIGH.

The other control signal outputs are kept enabled.

(s) Plasma reset circuit

The plasma reset circuit enables/disables the plasma display. The PDPCLR signal goes HIGH, and disables the plasma display in the following two cases:

- o When the CMDSET signal is LOW -- i.e., after power on and until the display mode register is set.
- o When the DETECT OPEN signal is LOW -- i.e., when the display is closed.

Figure 5-62 shows the plasma reset circuit.

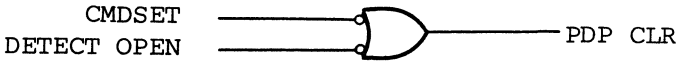


Figure 5-62 Plasma Reset Circuit

(t) Plasma interface signals

The five plasma interface signals are described as belows:

(1) *DATA0 to DATA3

4-bit parallel display data signal. The dot lights when the signal line is low.

(2) *SFT CLK

Data transfer shift clock to shift display data into the shift register.

(3) *VS

Vertical sync signal. Moves scanning to the top display line.

(4) *HS

Horizontal sync signal. Generates a data strobe signal and controls the 1-line display drive circuit.

(5) *PDP CLR

Operation inhibit signal. When this signal is low, the anode driver is turned off, the display is disabled.

5.10 I/O Interface Circuit

This chapter describes the interface capabilities and various options available in the computer.

A parallel port for communications with printer, and a serial port for asynchronous RS-232C communications are available. There are also two option slots for IBM-PC compatible boards.

The RAM expansion option is also described.

This chapter also describes the proper settings for the internal configuration DIP switches for the computer.

The following diagram illustrates the positions of the external ports found on the lower left-hand side of the computer.

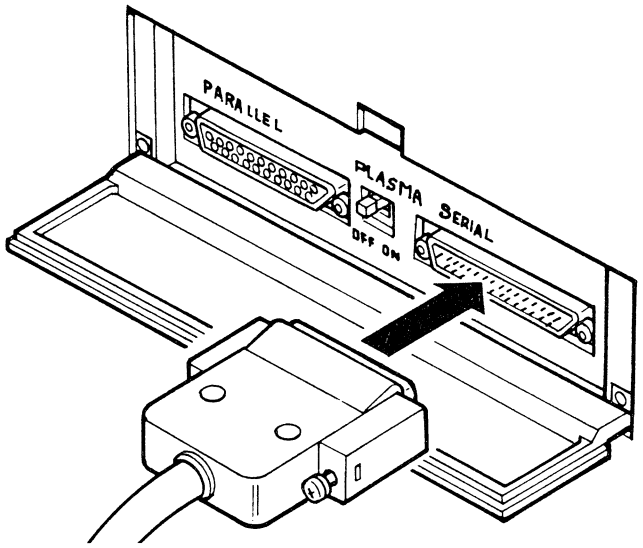
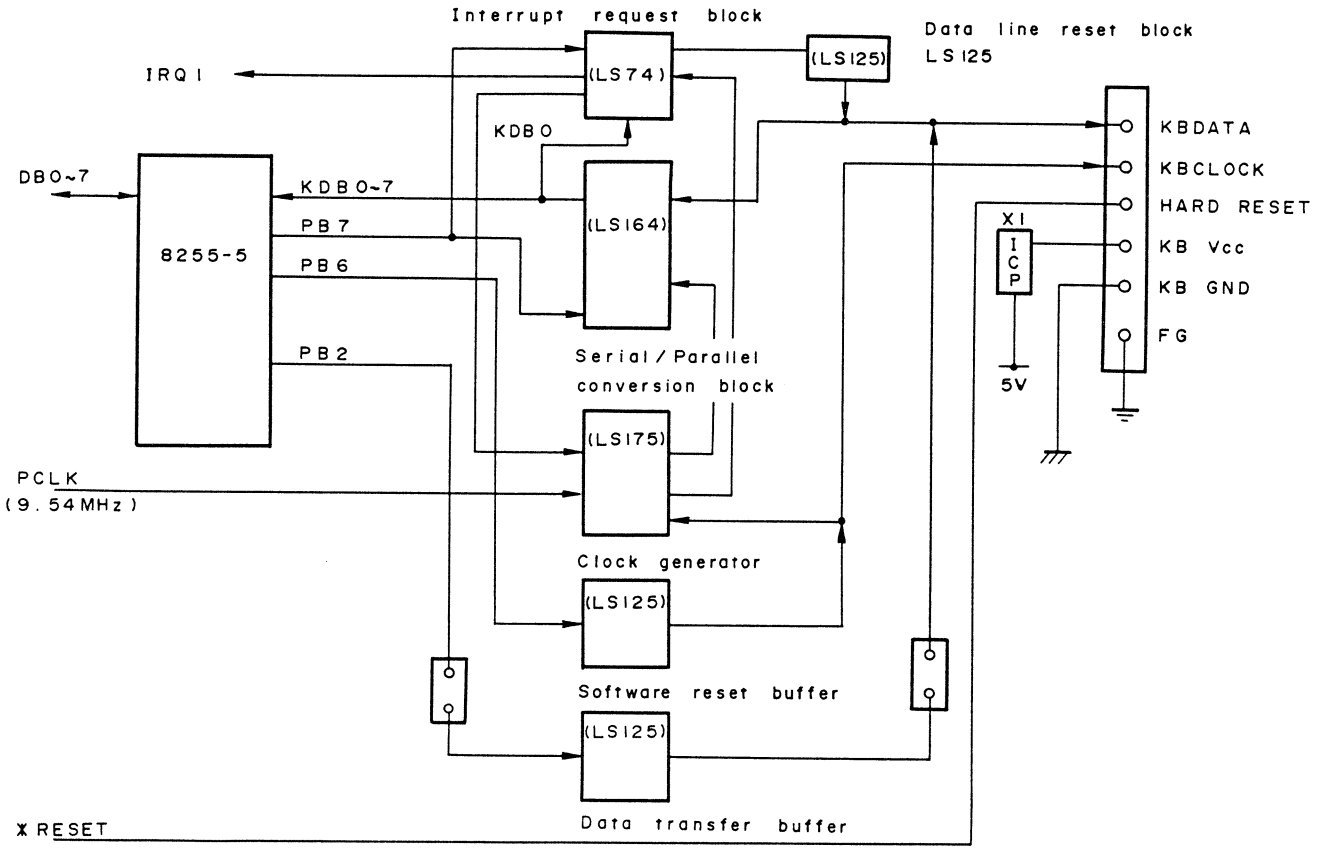


Figure 5-63

(a) Keyboard interface circuit

This circuit converts serial data input from the keyboard into parallel data. It interrupts the CPU so that the CPU can get data from the keyboard.



*1: I.C.P.: Overcurrent protective parts

Figure 5-64 Keyboard Interface Block Diagram

(1) Serial data creation

When a key is pressed, 2-byte data (*KBDATA) is input to this circuit in synchronization with the clock pulses (*KBCLOCK).

When the key is released, Key-Off data is input.

The input data enters the serial/parallel conversion block, where it is converted into parallel data using the clock pulses from the clock generator.

(2) Data read

When all serial data (8 bits) is input, the first data enters the interrupt request block and interrupts the CPU. The 8-bit data is then read into the CPU as parallel data.

During the interrupt request, the clock pulses being input to he serial/parallel conversion block are held LOW and stabilize the data in this block.

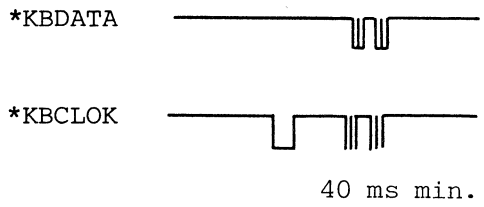
At this time, the data line reset block holds *KBDATA line of the L level, and disables this signal.

When the CPU finishes reading data through 8255-5, the CPU sets, through 8255-5, PB7 to the L level, resets the interrupt request block and the serial/parallel conversion block, sets *KBDATA to the H level to keep it in the ENABLE state, and prepares for the next data transfer.

When power is supplied, the 8255-5's output PB6 is set to the L level according to the programmed condition, and *KBCLOCK goes to L. With this signal, the keyboard performs self diagnosis. When no key is pressed, the keyboard outputs 00 to notify the CPU of the normal condition. If it is abnormal, it transfers an error code. The PB2 is in the service condition so that the CPU can use the data line.

The I.C.P. protects against current surge if a short-circuit occurs in the keyboard power line.

i) Keyboard timing at power on



ii) Keyboard timing during data transfer

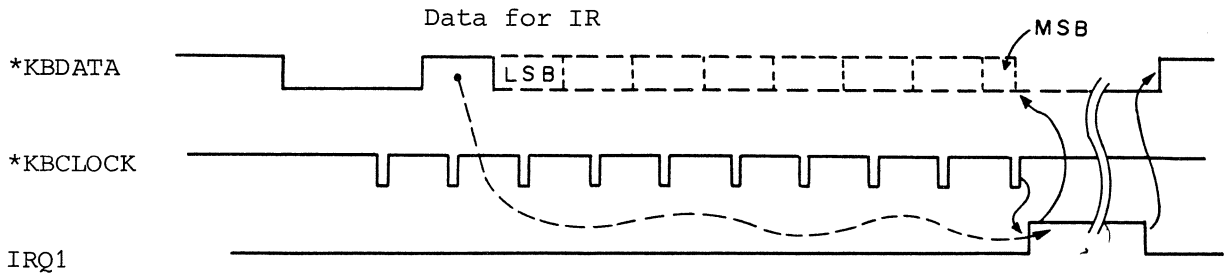


Figure 5-65 Keyboard Timing

(b) Parallel interface circuit

The printer interface, a parallel interface, connects a printer. It conforms to Centronics specifications.

Figure 5-66 shows a block diagram of the parallel interface circuit.

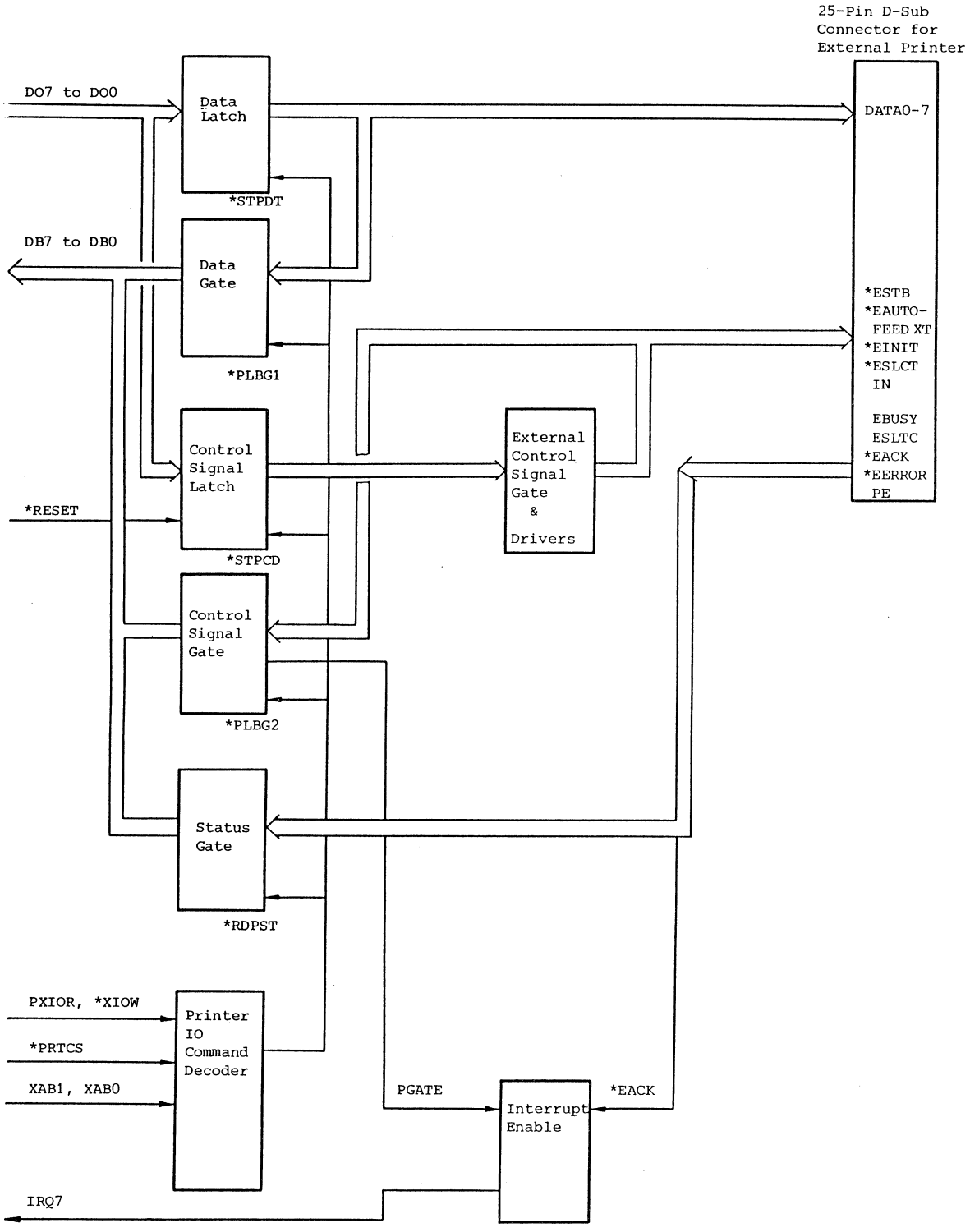


Figure 5-66 Parallel Interface Block Diagram

(1) Parallel interface signals

Outputs Signals

a) DATA0 to 7

These signal lines transfer data to be read by the printer. Data 0 is the least significant bit (LSB), and data 1 is the most significant bit (MSB).

b) *ESTB

This pulse is normally at a high level. The printer reads data while this line is LOW.

c) *EINIT

This signal is normally at a high level. When it goes to low level, the printer is reset to its initial state, and the printer buffer is cleared.

d) *ESLCT IN

When this signal is at a low level, the printer is possible to entry the data. But, this signal is fixed to low level by the printer.

e) *EAUTOFD XT

When this signal is at a low level, paper is automatically fed one line at a time after printing. This signal level can be fixed to a low level with a setting of the printer.

Input Signals

a) *EACK

This signal is normally at a high level and goes to a low level to indicate that the printer has received data and that it is ready to accept more data.

b) EBUSY

This signal is normally at a low level and goes to a high level to indicate that the printer cannot receive data.

HIGH in the following cases:

1) During data entry
2) During printing operation
3) In OFF-LINE mode
4) During printer error states

c) EPE

This signal goes to a high level to indicate that the printer is at paper end.

The level of the EPE signal is HIGH when the ribbon ends.

d) *EERROR

This signal is normally at a high level and goes to a low level to indicate that the printer is in paper end, off-line and/or error state.

The level of the *EERROR signal is LOW when the ribbon ends.

e) ESCLT

This signal indicates that the printer is in the selected state.

(2) Printer I/O command decoder

This circuit decodes each I/O command when the printer I/O is selected. Table 5-7 shows printer I/O commands.

Table 5-7

I/O Address HEX	Input			I/O	Printer I/O Command	Enable Command Signal
	*PRTCS-1	XAB1	XAB0			
0 3 7 8 (0 2 7 8)	L	L	L	O	SET PRINTER DATA	*STOP
0 3 7 8 (0 2 7 8)	L	L	L	I	READ PRINTER DATA	*PLBG1
0 3 7 9 (0 2 7 9)	L	L	H	I	READ PRINTER STATUS	*RDPST
0 3 7 A (0 2 7 A)	L	H	L	O	SET PRINTER COMMAND	*STPCD
0 3 7 A (0 2 7 A)	L	H	L	I	READ PRINTER COMMAND	*PLBG2

Note: Either of the I/O addresses 278H - 27FH or 378H - 37FH may be set by means of a short-circuit plug (J3). When the equipment is shipped, the I/O address is set to 378H - 37FH.

(3) Data latch and data gate

The data latch latches output data from the CPU to the printer. The CPU can also read output data by enabling the data gate.

(4) Control signal latch and control signal gate

The control signal latch latches control signals from the CPU to the printer. The CPU can also read control signals by enabling the control signal gate.

(5) Status gate

The CPU reads printer status by enabling the status gate.

(6) Interrupt enable circuit

Interrupt enable or disable to the CPU is selected by Bit 4, INT EN, of the I/O address 37A (HEX). For an interrupt, an interrupt request to the interrupt controller is generated by the *EACK signal of the printer using IRQ7.

(7) Data output timing

Figure 5-67 shows data output timing to the printer and printer response timing.

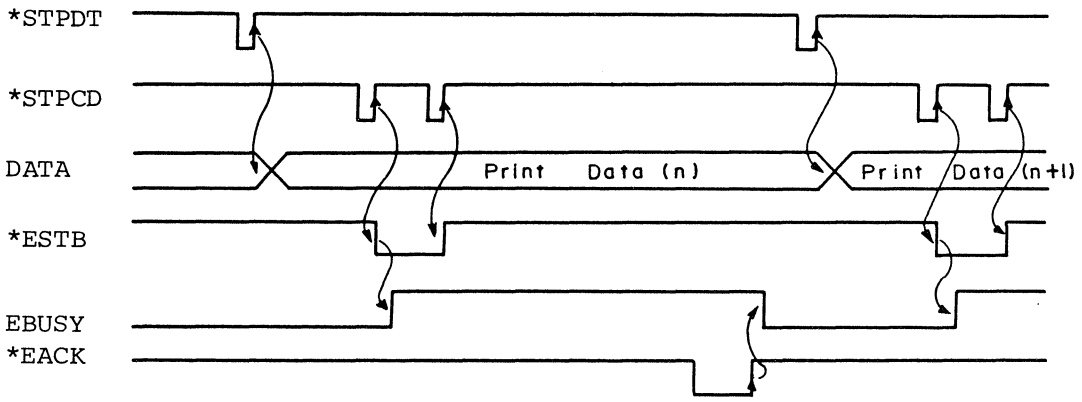
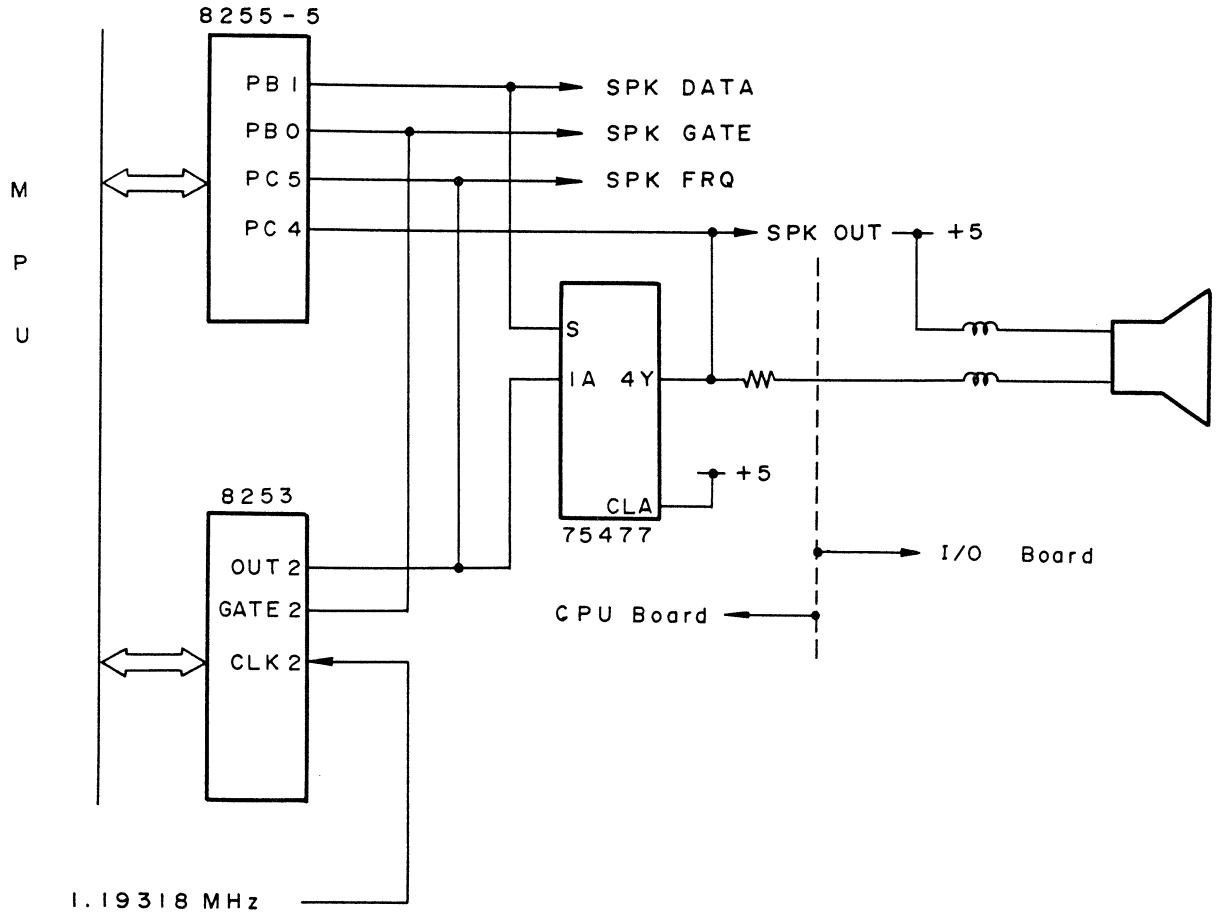


Figure 5-67 Parallel Interface Timing Chart

(c) Speaker interface

The speaker interface circuit amplifies the signal from the 8253 and outputs it to the speaker. Signal range of 7.4 Hz to 1.19318 MHz is possible.



Controlled by SPKDATA and SPKGATE output by 8255-5 and by SPKFRQ output by 8253. SPKFRQ and SPKOUT are input to 8255-5.

Figure 5-68 Speaker Interface Block Diagram

(d) Serial interface

Figure 5-69 shows a block diagram of the serial interface circuit.

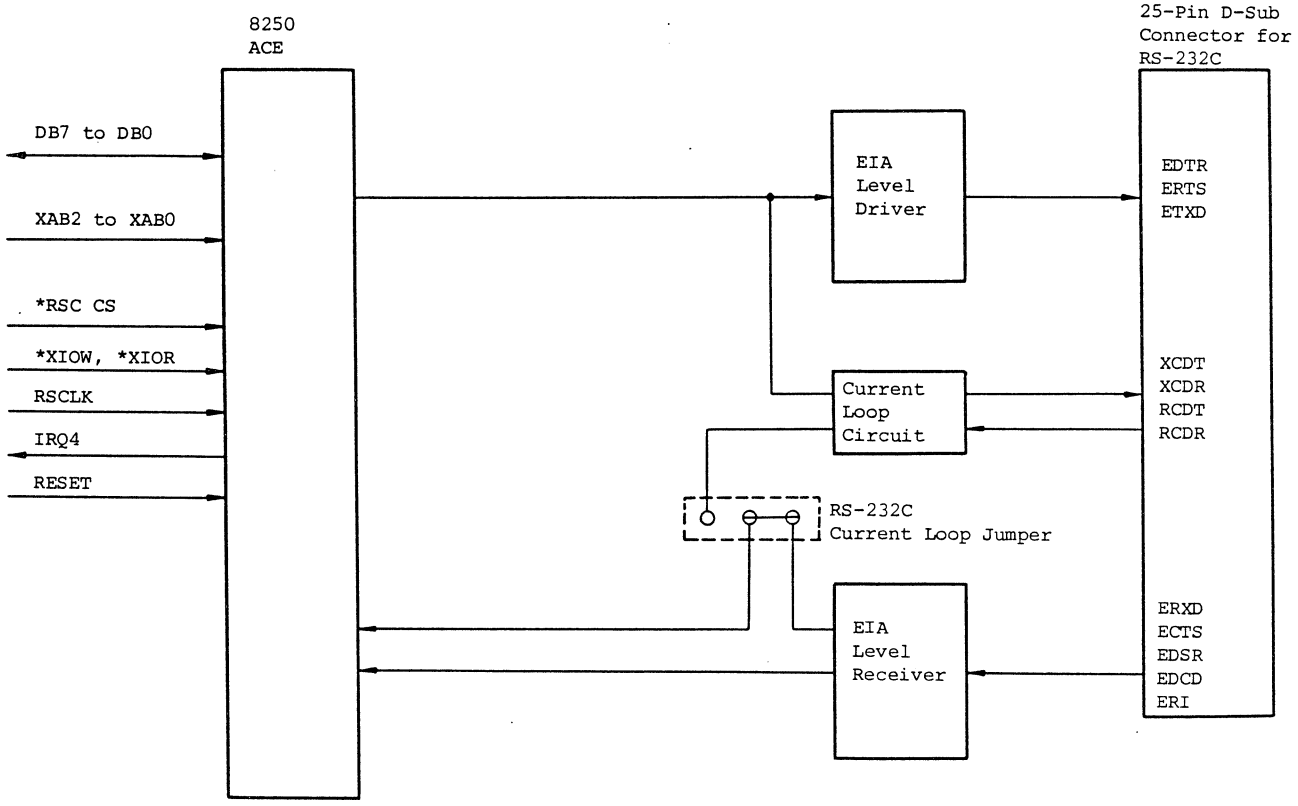


Figure 5-69 Serial Interface Block Diagram

(1) Selecting voltage and current loop interfaces

EIA DB-25, the connector for RS-232C, can be used for both voltage and current loop interfaces. Both interfaces are selected by the RS-232C current loop jumper. The initial setting is the RS-232C interface.

(2) EIA level driver and receiver

a) Transmission/receiving level converter circuit

This circuit converts the TTL level signal to the voltage level specified in RS-232 V.24.

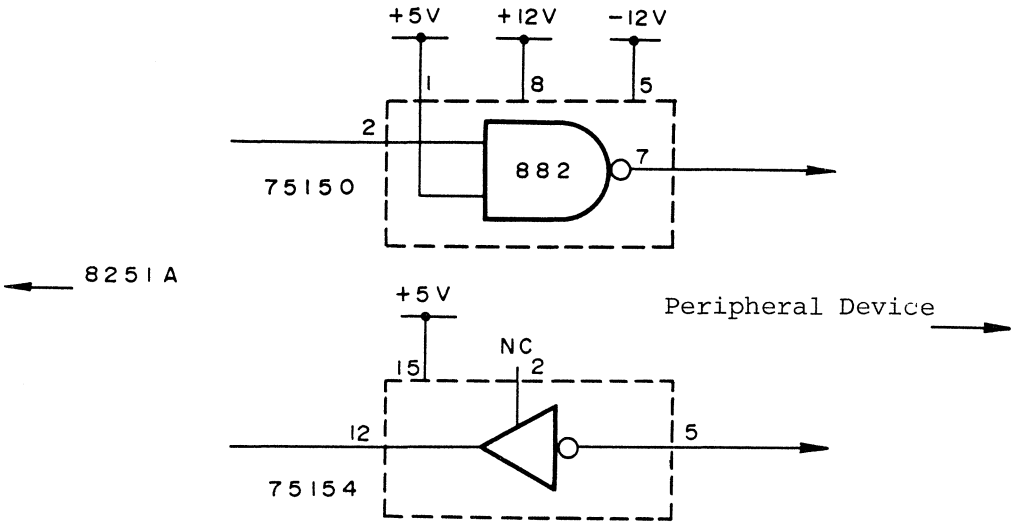


Figure 5-70 Voltage Interchange Circuit

(3) Current loop circuit

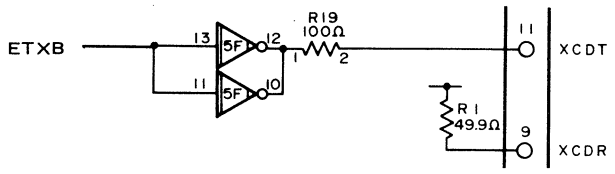


Figure 5-71 Transmit Circuit

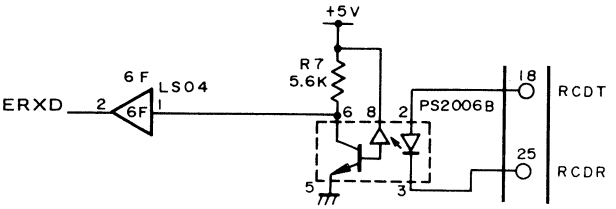


Figure 5-72 Receive Circuit

(4) Interrupt circuit

Set Bit 3 of the MODEM control register to "1" to enable an interrupt request from 8250. Interrupt requests are produced to the interrupt controller by IRQ4.

NOTE: Either of the interrupt level IRQ3 or IRQ4 may be set by means of a short-circuit plug (J6). When the equipment is shipped, the interrupt level is set to IRQ4.

(5) RS-232C I/O command

Table 5-8

I/O Address HEX	Input					I/O	RS-232C I/O Command
	*RSCCS-1	DLAB	XAB2	XAB1	XAB0		
0 3 F 8 (0 2 F 8)	L	L	L	L	L	O	SET TxD BUFFER
0 3 F 8 (0 2 F 8)	L	L	L	L	L	I	READ RxD BUFFER
0 3 F 8 (0 2 F 8)	L	H	L	L	L	O	SET DIVISOR LATCH (LSB)
0 3 F 9 (0 2 F 9)	L	L	L	L	H	O	SET INTERRUPT ENABLE
0 3 F 9 (0 2 F 9)	L	H	L	L	H	O	SET DIVISOR LATCH (MSB)
0 3 F A (0 2 F A)	L	X	L	H	L	I	READ INTERRUPT IDENTIFICATION
0 3 F B (0 2 F B)	L	X	L	H	H	O	SET LINE CONTROL REG.
0 3 F C (0 2 F C)	L	X	H	L	L	O	SET MODEM CONTROL REG.
0 3 F D (0 2 F D)	L	X	H	L	H	I	READ LINE STATUS
0 3 F E (0 2 F E)	L	X	H	H	L	I	READ MODEM STATUS

Note: Either of the I/O addresses 2F8H - 2FFH or 3F8H - 3FFH may be set by means of a short-circuit plug (J4). When the equipment is shipped, the I/O address is set to 3F8H - 3FFH.

(6) Data format

Figure 5-73 shows a typical asynchronous transfer format.

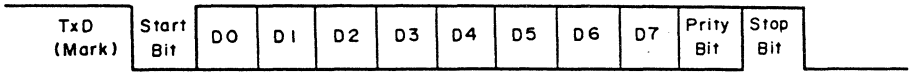


Figure 5-73 Asynchronous Transfer Format

(e) Floppy disk interface

The blocks are outlined below.

- o FDC (NEC μPD765)

  This is an LSI having a floppy disk formatter/controller function. Placed between the floppy disk drive and the microprocessor, this interface reads and writes data on floppy disks, drives the mechanical section, and detects control signals.

  Refer to the FDC data sheet for more detail.

- o FDD control command register buffer

  This is an FF circuit set with an I/O instruction. This buffer designates Drive Select, Motor Start, FDC Reset, or DMA Permission.

- o DREQ controller

  This controller creates an interface timing between DMAC and FDC in DMA transfer.

- o Clock generator

  This generates a 16-MHz clock frequency, and supplies it to the FDC and the VFO.

  The frequency is first supplied to the VFO, where it is frequency-divided into a 4-MHz clock, and supplied to the FDC.

- o VFO circuit

  This circuit separates data read from the floppy disk into data and clock, and creates data and windows.

  Refer to the data sheet for details on the VFO LSI (SED9420C).

- o Precompensation circuit

  This circuit prevents erroneous data read, which may occur when the write data peak shifts during magnetic recording.

- o Power-off reset circuit

  This reset circuit functions at a voltage below 4.4 V to prevent error data from being written into the floppy disk.

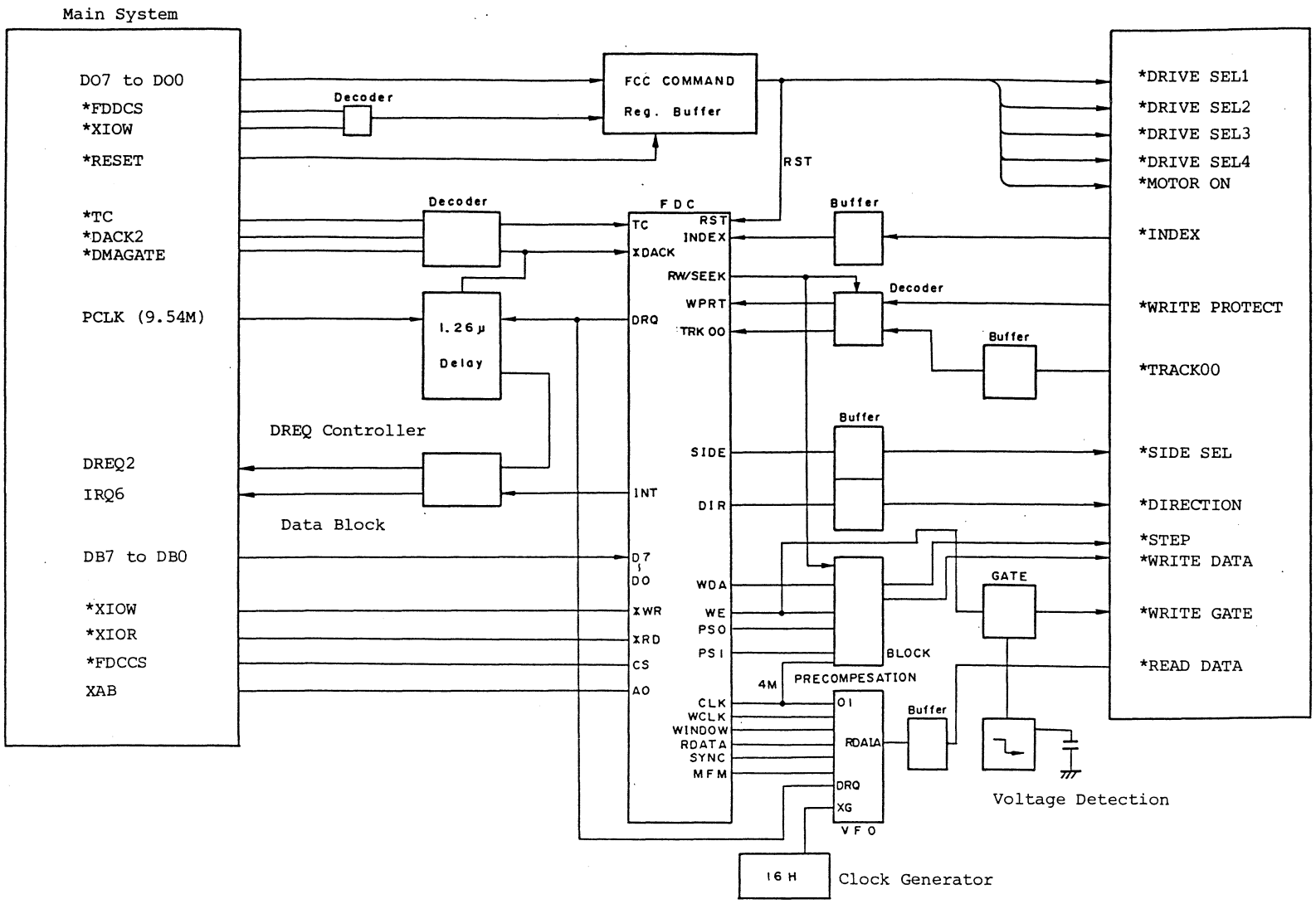


Figure 5-74 Floppy Disk Interface Block Diagram

(1) FDD control command register

The circuit consists of the FDD control command register, drive select decoder, and buffer.

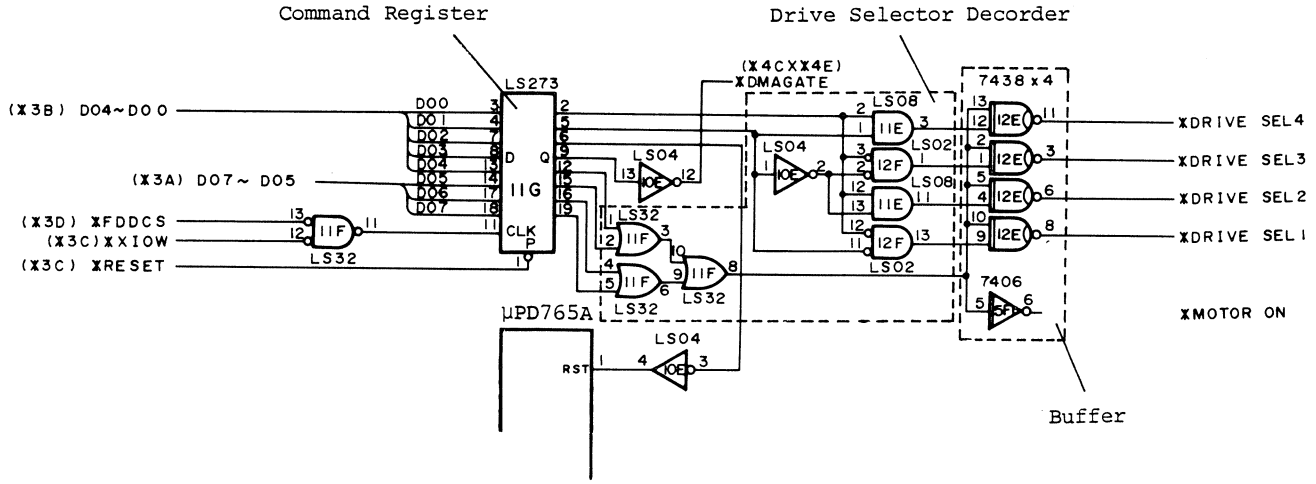
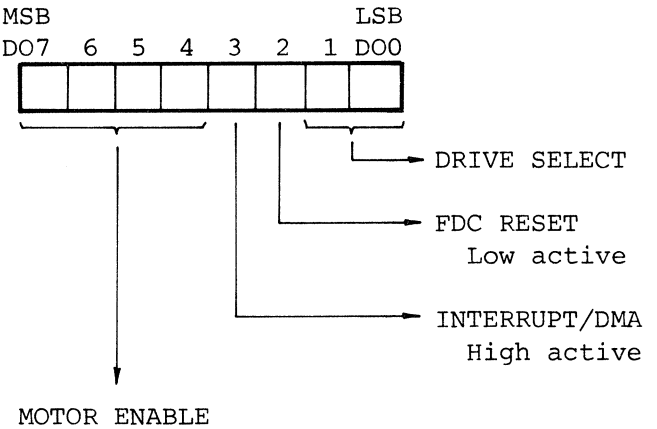


Figure 5-75 FDD Control Command Buffer Register Circuit



DO0	DO1	Drive No.
0	0	1
0	1	2
1	0	3
1	1	4

x: Do not care

DO4	DO5	DO6	DO76	* Motor on
1	x	x	x	0 (Low active)
x	1	x	x	
x	x	1	x	
x	x	x	1	

The motor rotates when any bit from DO4 to DO7 is on.

(2) DREQ controller

This controller produces interface timing between FDC (μPD765A) and DMAC (8237A).

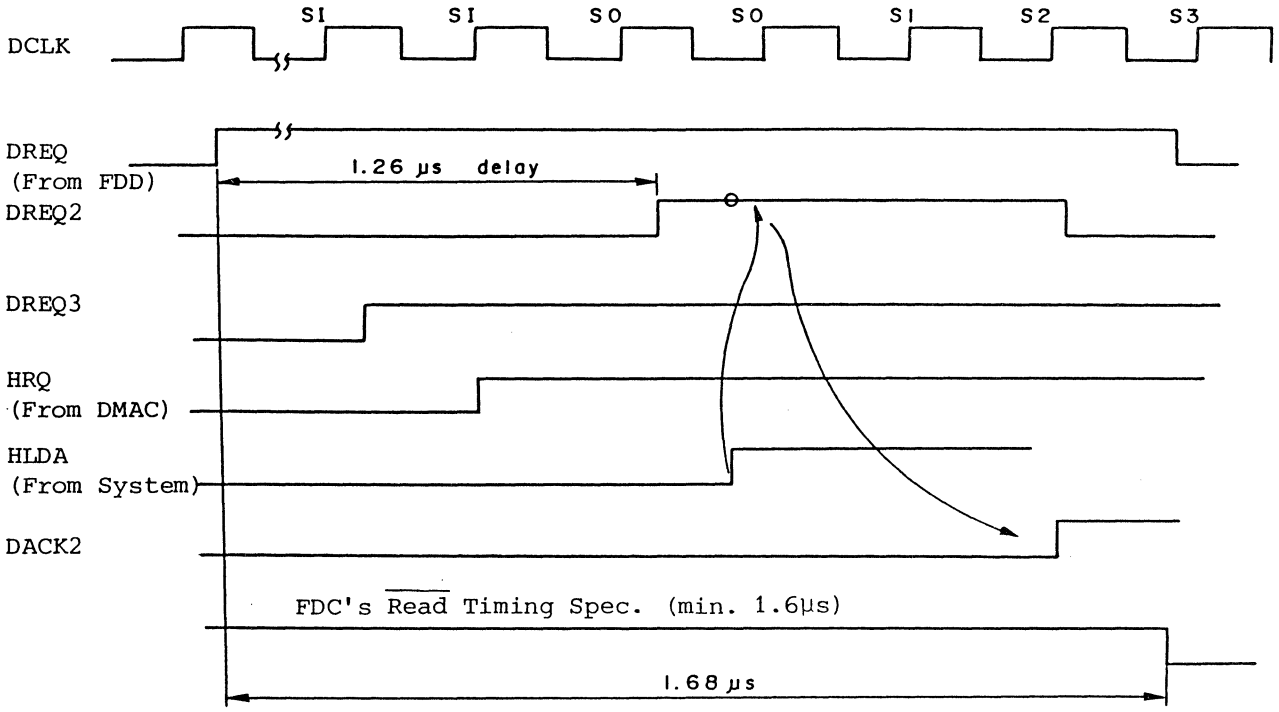


Figure 5-76 DREQ Signal Timing Chart

This block delays DREQ, which is a DMA request signal from the FDC, more than 1.26 μs and sends it to the DMAC for the following reason.

The minimum time for the DMA to return DACK after receiving a DMA request signal occurs when DREQ of a higher priority rank is generated after DREQ with a low priority rank is generated and is for two cycles of the DMAC clock (420 ns). At least 1.6 μs is required after the FDC generates DREQ and before reading. If the DMAC operation is too fast, data from the FDC cannot be read. This block delays DREQ by 1.260 μs to prevent this.

(3) Precompensation circuit

This circuit advances or delays data writing by 250 ns to obtain an time allowance during a read. It also acts as a gate for step signals.

Figure 5-77 shows a timing chart. The output signal WDA (write data) from the FDC synchronizes with the 4-MHz clock CLK in IC LS175 and is delayed by 250 µs. IC153 determines, using PS0 and PS1, which signal of LS175 should be selected.

The selected signal is resynchronized by LS175, and output to the FDD as a precompensated signal.

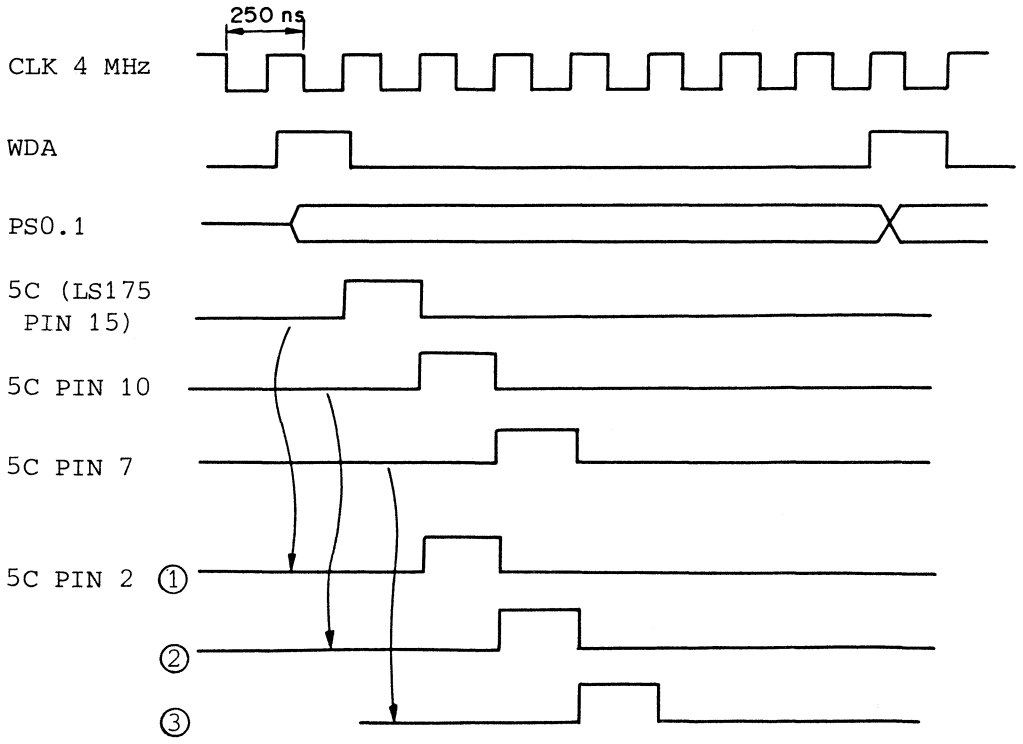


Figure 5-77 Precompensation Timing Chart

Table 5-91 Precompensation Table

PS0	PS1	Write Timing	Selected Signal
0	0	TYP.	②
0	1	LATE	①
1	0	EARLY	③
1	1	-----	GND

5.11 Programmable Internal Timer (8253-5)

This timer is a programmable counter/timer consisting of three of 16-bit counters. The uses of these counters are given below:

Table 5-10 Usage of the 8253-5 Counter Channels

8253-5 Channel	Usage	Mode	CLK (MHz)
0	Internal timer	2	1.19318
1	Memory refresh	2	1.19318
2	Beep frequency generator	3	1.19318

In Modes 2 and 3, OUT = "H" if GATE = "L".

Memories are refreshed every 4 msec.

Refer to the data sheet for more details on 8253-5.

5.12 Switches

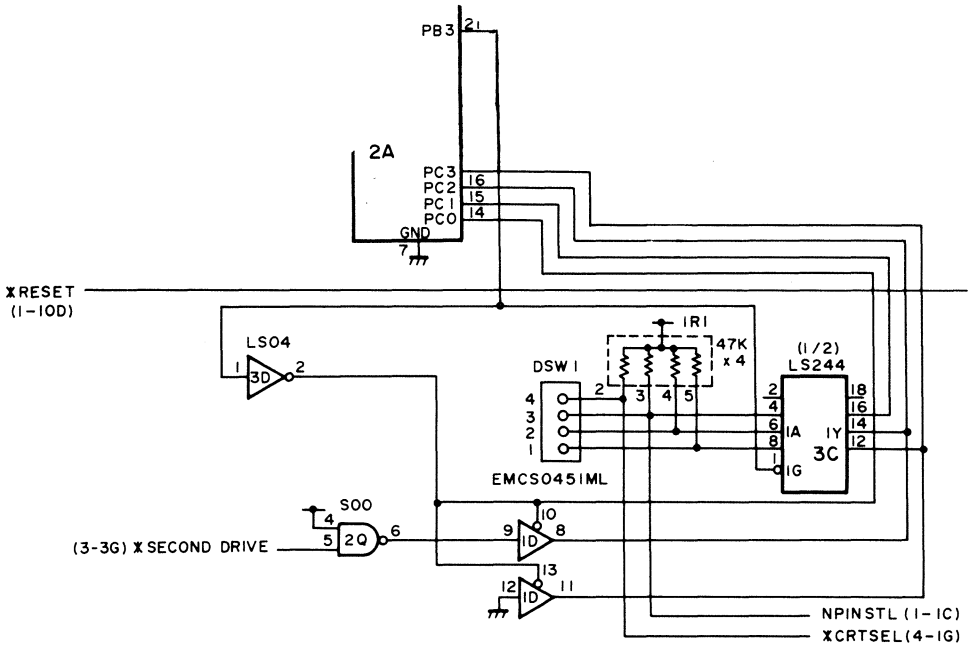
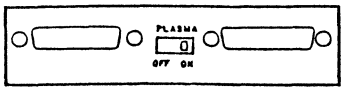


Figure 5-78 System Switch Circuit

(a) Definition of plasma display select switch (SW2)

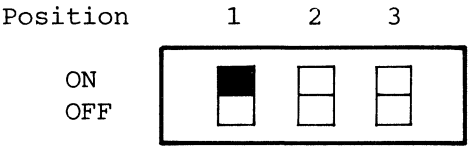
The plasma display select switch is located in the port compartment, at the lower left-hand side of the unit and can be operated from the outside.



Position ON ..... Plasma display ON
OFF ..... Plasma display OFF

(b) Definition of DIP switch (DIPSW1) and system configuration

The DIP switches are installed in the inside of the unit and cannot be operated from the outside.



Position 1 ..... 8087 enable: OFF
disable: ON (default)
2 ..... Reserved
3 ..... Reserved

The system configuration is defined by the input data of PPI 8255A-5 PC Register as follows:

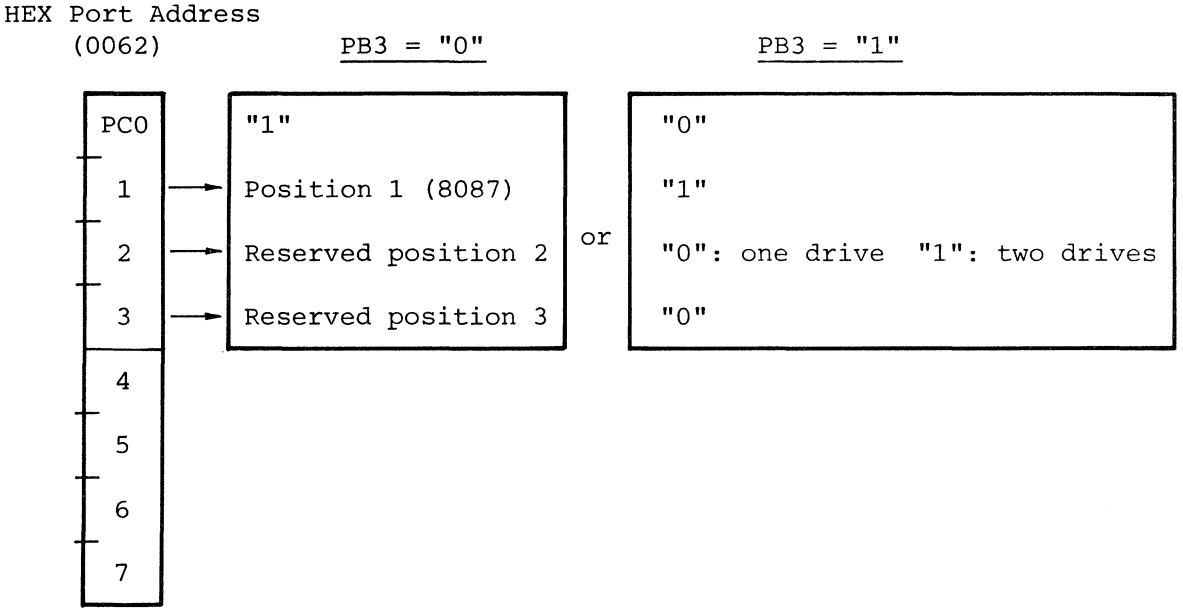


Figure 5-79

(c) Description of 8255A-5

The 8255A-5 is a programmable general-purpose I/O device incorporating 3 I/O ports (each 8 bits). It is used to internally and externally feed a variety of data via the Program Control Operation. Part [A] is connected to the keyboard interface, port [B] to the speaker unit, keyboard, and the DIP switch interface, and port [C] to the DIP switch interface, respectively. For more details, refer to the data sheet.

(d) Short plug setting

The short plugs on the CPU and I/O boards are set as follows when the equipment is shipped.

On the CPU board

J7 ..... EP	Short
J8 ..... EP	Short
J11 .... UNDE	Short
J13 .... with expansion memory	Short
without expansion memory	Open

On the I/O board

J2 ..... 232C	Short
J3 ..... 378H	Short
J4 ..... 3F8H	Short
J5 ..... FD version	Short
HD version	Open
J6 ..... IRQ4	Short

5.13 Option Slot Interface

(a) The circuit shown in Figure 5-80 has two main circuits; one applied (1) if the option slot of the equipment is used and the other, (2) if the option slot of the extension unit is used.

The circuit delays the generation of data bus gate and DIR signals by 150 ns if the option slot of the extension unit is used. This is because data input/output is delayed by 150 ns in the receiver card provided in the extension unit.

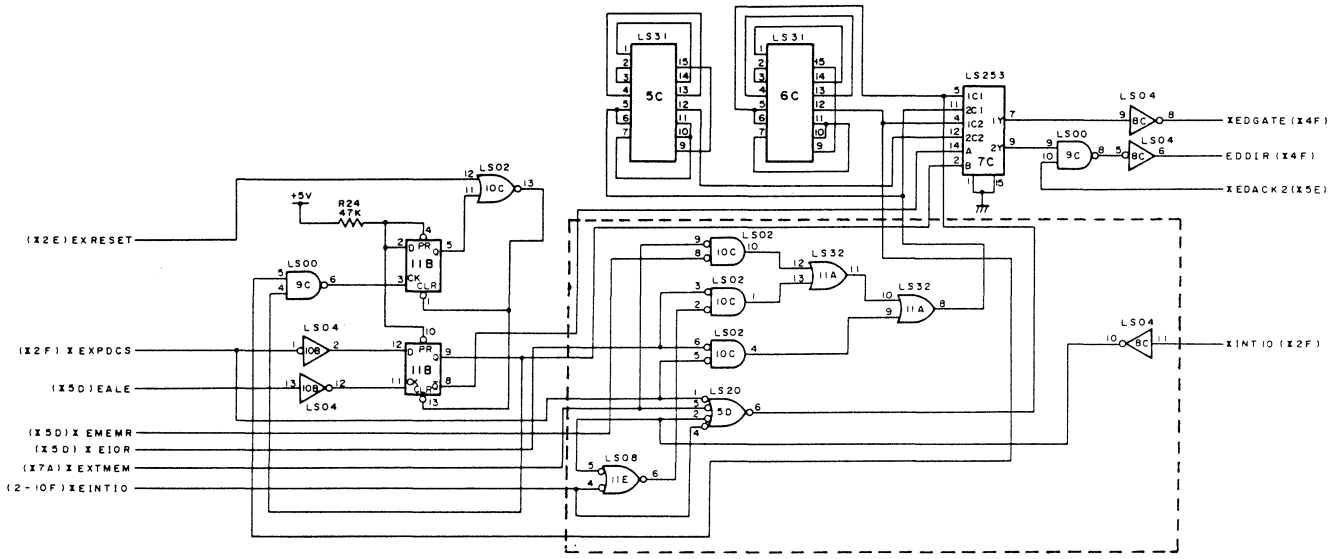


Figure 5-80

(b) Description of circuit

(1) The 74LS74 (11B-1) generates a select signal to switch the gate and DIR signals of the data bus.

This signal is input to the select signal of the 74LS253.

(2) The 74LS253 (7C) is used to switch a gate and DIR signals if the option slot of the equipment is used or the 150-ns delayed gate and DIR signals if the option slot of the extension unit is used.

Output Control		Select Input		Data Inputs				Output	
1G	2G	A	B	1C1	1C2	2C1	2C2	Y	2Y
L	L	H	L	H	X	H	X	H	H
				L	X	L	X	L	L
				H	X	L	X	H	L
				L	X	H	X	L	H
		L	H	X	H	X	H	H	H
				X	L	X	L	L	L
				X	H	X	L	H	L
				X	L	X	H	L	H

As the table above shows, input signals 1C1 and 2C1 are output to 1Y and 2Y respectively when A=H and B=L. This state is given if the option slot of the equipment is used.

Input signals 1C2 and 2C2 are output to 1Y and 2Y respectively when A=L and B=H. This state is given if the option slot of the extension unit is used, and a gate and DIR signals delayed 150 ns by the 74LS31 are output.

(c) The 74LS31 (5C) generates a DIR signal delayed by 150 ns.

(d) The 74LS31 (6C) generates a gate signal delayed by 150 ns.

(e) The 74LS74 (11B-2) generates a reset signal for the 74LS74 (11B-1).

(f) The circuit in the dotted-line square in Figure 5-80 generates the conditions of a gate and DIR signals.

The 74LS02 (10C-1) changes the direction of the data bus from A to B for option memory read.

The 74LS02 (10C-2) changes the direction of the data bus from A to B for option I/O read.

The 74LS02 (10C-3) changes the direction of the data bus from A to B for extender read.

The 74LS20 (5D) generates a gate signal. This gate signal is put in a high level when accessing the option memory, option I/O, and extender card.

5.14 Option Slot Connector

The table below and on the following pages describes the signals to the option slot connector.

Table 5-13 Option Slot Connector Signal Description (1/3)

Signal	I/O	Description
DB0-DB7	I/O	Data lines 0-7: Active high, 8-bit bidirectional data lines are used to transfer data among the processor, I/O devices, and memory. DB0 is the least significant bit (LSB).
AB0-AB19	O	Address lines 0-19: Active high, address lines are used to span 1 M byte memory or 64K bytes I/O address space. AB0 is the LSB, while AB19 is the MSB. The address may be generated by the 8088 processor or the DMA controller.
IRQ2-IRQ7	I	Interrupt request lines 2-7: Signals on these lines are input from I/O adapters to the interrupt controller to indicate interrupt request to the processor. IRQ2 has the highest priority, while IRQ7 has the lowest. While the rising leading edge of these signals causes an interrupt request, they may be held high until an acknowledge signal (*INTA) is returned from the processor.
DREQ1-DREQ3	I	DMA request lines 1-3: Active-high, used to request DMA services. DREQ1 has the highest priority, while DREQ3 has the lowest. These lines must be kept high until the DMA controller issues the acknowledgement signal *DACK.
*DACK0-*DACK3	O	DMA acknowledge lines 0-3: The DMA controller issues its acknowledgement through one of these four active-low lines. *DACK0 is used to refresh system dynamic memory.

Table 5-13 Option Slot Connector Signal Description (2/3)

Signal	I/O	Description
*MEMR	O	Memory read line: Active low, memory read signal. Data from memory must be placed on the data bus while this line is low. This signal is issued from the processor, or DMA controller.
*MEMW	O	Memory write line: Active low, memory write control signal. Data on the data bus must be written into memory while this line is low. This signal is issued from the processor or DMA controller.
*IOR	O	I/O read line: Active low, I/O read control signal. While this line is low, the addressed I/O device places its data on the data bus. This signal is issued from the processor or DMA controller.
*IOW	O	I/O write line: Active low, I/O write control signal. While this line is low, the addressed I/O device reads the data from the data bus. This signal is issued from the processor or DMA controller.
RESET	O	Reset: Active high signal synchronized with a falling/leading edge of the processor clock. Turning the power on activates the RESET line to provide initial reset to the circuitry. The RESET signal remains active until the +5 V supply line is completely stabilized.
OSC	O	Oscillator: This is a high-speed 70 ns clock with 50% duty cycle. The frequency is 14.31818 MHz.

Table 5-13 Option Slot Connector Signal Description (3/3)

Signal	I/O	Description
ALE	O	Address latch enable: Address latch signal output from the processor. The I/O device controllers and the memory use this control signal to synchronize their own operations. The trailing edge of this signal latches the address into the address latch.
AEN	O	Address latch: An active high line to indicate that a DMA controller has been started and the DMA controller has the bus access right. This line is also used to switch the bus between the processor and the DMA controller.
TC	O	Terminal count: An active high pulse to indicate that the terminal count on the pertinent DMA channel has reached zero.
CLK	O	Processor clock: The basic clock furnished to the microprocessor. It is created by dividing the master clock by three, and it has an interval of 210 ns with a duty cycle of 33%. The clock frequency is 4.77 MHz.
*IOCHRDY	I	I/O channel ready: Active low, this control signal is used by an I/O device to request the processor or DMA controller to prolong the bus cycle. The bus cycle is prolonged while this line is low.
*IOCHCK	I	I/O channel check: Active low, this control signal provides the processor with parity (error) information on memory or devices.

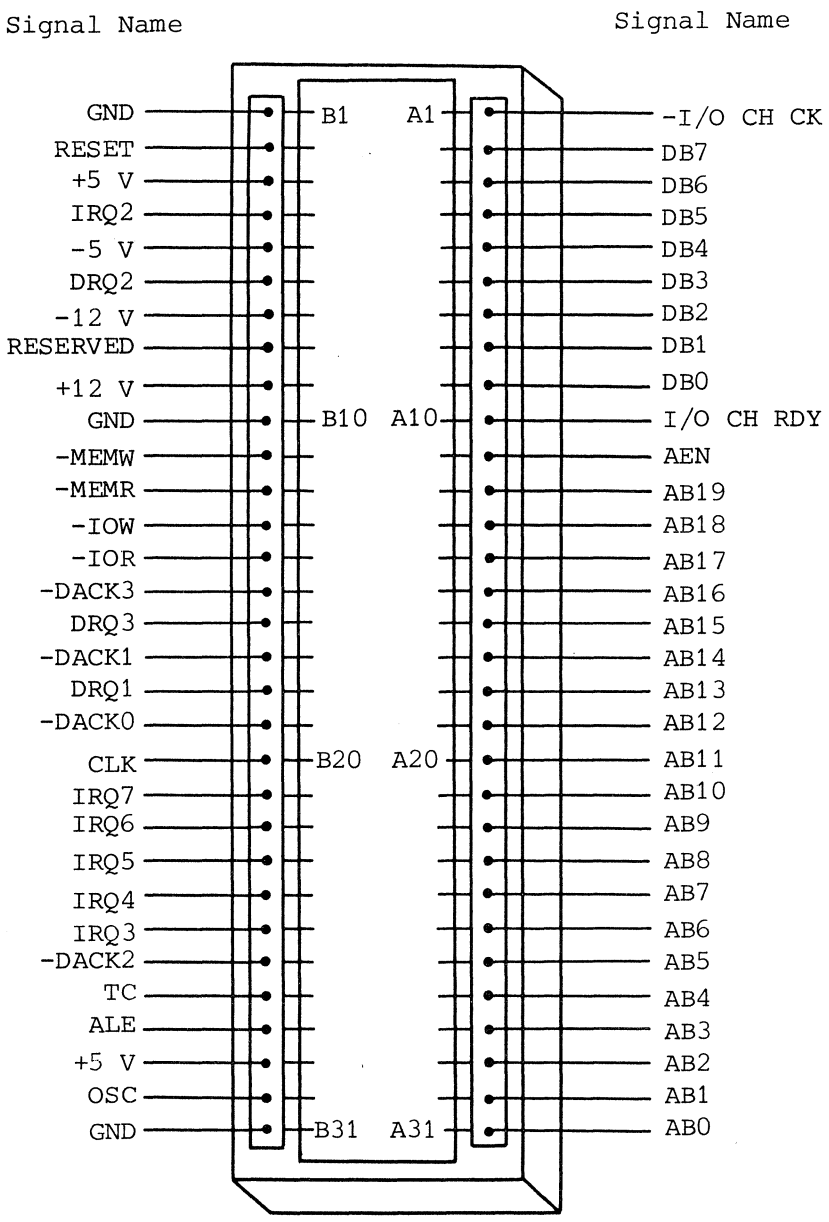


Figure 5-81 Connector Pin Assignment

Setting of DIPSW1 and Short Plugs

o CPU board

Short Plugs

J7	EP	Short
J8	EP	Short
J11	UNDE	Short
J13	with expansion RAM 256K	Short
	without expansion RAM 256K	Open

o I/O board

DIPSW1

Position 1	8087 enable	OFF
	8087 disable	ON
Position 2	Reserved	OFF
Position 3	Reserved	OFF

Short Plugs

J2	RS-232C/current loop select	
	RS-232C	Short (on shipment)
	Current loop	Open
J3	Printer I/O address select	
	378H	Short (on shipment)
J4	RS-232C I/O address select	
	3F8H	Short (on shipment)
J5	FD version	Short
	HD version	Open
J6	RS-232C interrupt select	
	IRQ4	Short (on shipment)

6. Replacement Parts List and Drawing

REPLACEMENT PARTS LIST (PLSMX)

NOTE:
- **When ordering replacement parts indicate Part No. and Name of Parts.**
- **⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.**

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
PLSMX P.B. Ass'y (YJJ3006420A4)					
C12,41,45 50,69,77 79		ECEB1CS100	Electrolytic Capacitor 16V 10μF	7	
C14,31,32 78,86		ECEB1CS330	Electrolytic Capacitor 16V 33μF	5	
C17		ECEB1CS470	Electrolytic Capacitor 16V 47μF	1	
C25		ECQV1H103JZ	Film Capacitor	1	
C1,C5 to C11 C13,C16,C18 to C24,C26 to C30,C33 to C40,C42 to C44,C46 to C49,C51 to C68,C70 to C76,C80 to C85,C87 to C94		ECQV1H104JZ	Film Capacitor	76	
C2,3,4 15		YJ104B102KF	Ceramic Capacitor 50V 1000PF	4	
CN6		EMCS0250M	Connector	1	
CN7		EMCS0252M	Connector	1	
CN8		EMCS0352M	Connector	1	
CN9		YJJJC00710B4	Connector 16P	1	
CN		EMCS0451ML	Connector	1	
CN		EMCS0651ML	Connector	1	
CN		YJ7664-62S	Connector (64P)	1	
CN5		YJ5276-05A	Connector	1	
D1		MA162	Diode	1	
D2		LN25RP	LED	1	
FILTER1		YJBNP002-02	Filter	1	
L17 to 24		YJJFA00210B4	Filter	8	
R5,6,8,9 11,12,14, 16 23 to 26 41 to 43		ERD25TJ473	Carbon Resistor 1/4W 47kΩ	15	
R15		ERD25TJ560	Carbon Resistor 1/4W 56Ω	1	
R45		ERD25TJ561	Carbon Resistor 1/4W 560Ω	1	
14.3M,INTR INTA,XMEMR XMEMW, XIOR,XOOW ALE,AENCPU KBCLK KBDATA GND,INTID BSCLK SHIFT,CRTC ENF7 CAS RAS,VS,HS		YJMT-027	Terminal Pin	25	
J4 to J6,J12		YJZ-128	Terminal Pin	4	
J7,J8,J11		YJZ-149-3P	Terminal Pin	3	
J13		YJZ-152-2P	Terminal Pin	1	

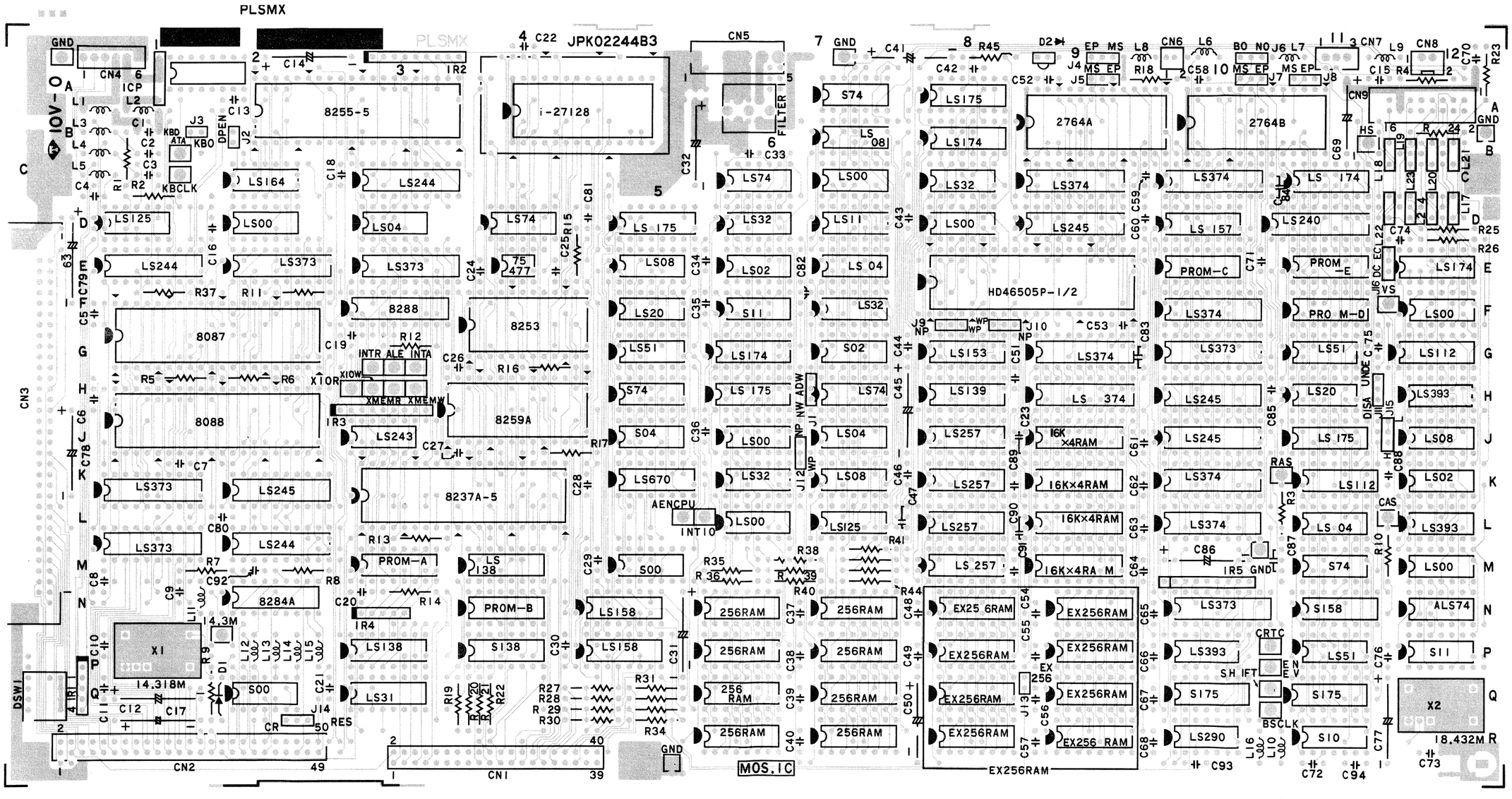
Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
8N,P.Q.R 9N,P.Q.R		YJDILB16P8JC	IC Socket 16P	8	
4(5)A.,9A 10(11)A		YJDILB28P8JC	IC Socket 28P	3	
8,9E.F		HD68A45P	LSI	1	
6N,6P,6Q, 6R,7N,7P 7Q,7R		MB81256-15	RAM IC	8	
3F		MPB8288D	LSI	1	
9J,9K,9L, 9M		MB81416-12	RAM IC	4	
5E,7B,7K, 12J		M74LS08P	IC	4	
1D,7P		M74LS125AP	IC	2	
		YJDILB40P8JC	IC Socket 40P	1	
6E,12K		M74LS02P	IC	2	
2D,6J,6L 7C,BD 12F,12 M		M74LS00P	IC	7	
2N		M5L8284AP	LSI	1	
1J		UPD8088D	LSI	1	
8H		M74LS139P	IC	1	
10D		M74LS157P	IC	1	
8G		M74LS153P	IC	1	
3D,7E,7J, 11L		M74LS04P	IC	4	
3M		YJJQM00350B4	Fuse ROM (P-POM A)	1	
11K,12G		M74LS112AP	IC	2	
7D		M74LS11P	IC	1	
4N		YJJQM00080B4	Fuse ROM (P–ROM B)	1	
10E		YJJQM00091B4	Fuse ROM (P–ROM C)	1	

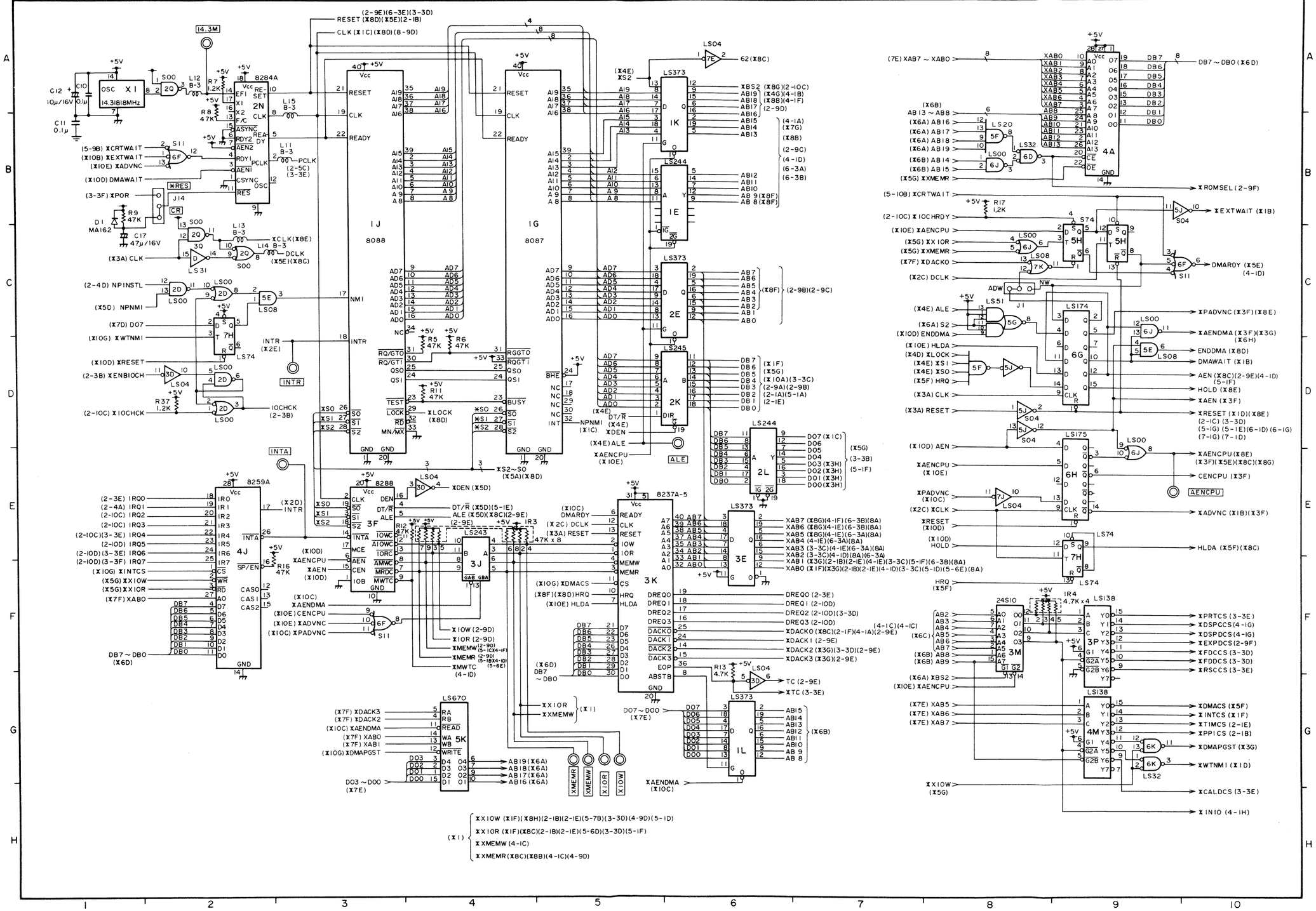
Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
11F		YJJQM00100B4	Fuse ROM (P–ROM D)	1	
11E		YJJQM00110B4	Fuse ROM (P–ROM E)	1	
4K		UPD8237AC5	LSI	1	
4D		SN74ALS74N	IC	1	
3Q		SN74LS31N	IC	1	
9C,9G,9H 10C,10F 10K,10L		SN74LS374N	IC	7	
5M,2Q		SN74S00N	IC	2	
7G		SN74S02N	IC	1	
5J		SN74S04N	IC	1	
11R		SN74S10N	IC	1	
6F,12P		SN74S11N	IC	2	
4P		SN74S138N	IC	1	
11N		SN74S158N	IC	1	
10Q,11Q		SN74S175N	IC	2	
7A,5H,11M		SN74S74N	IC	3	
4E		SN75477P	IC	1	
IR4		YJARB00071B4	Resistor Array	1	
IR2,35		YJARB00201B4	Resistor Array	3	
IR1		YJARB00501B4	Resistor Array	1	
L1 to L5,L7 L9 to L16		YJJNC00010B4	Choke Coil	14	
R7,R17,R19 R21,R35, R36,R37		ERD25TJ122	Carbon Resistor 1/4W 1.2kΩ	7	
R3,R20,R22 R27 to R34 R38 to R40 R44,R10		ERD25TJ220	Carbon Resistor 1/4W 22Ω	16	

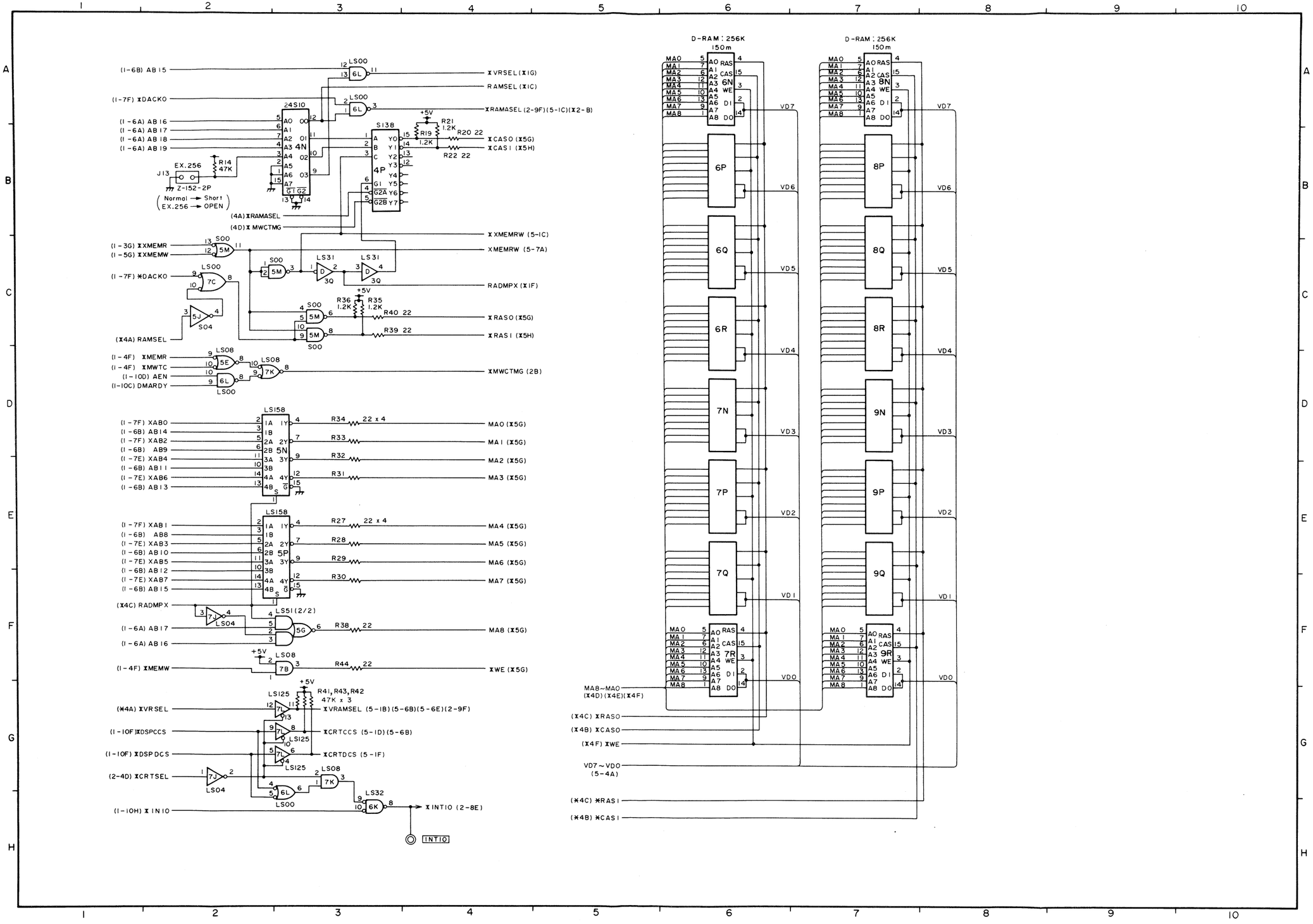
Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
R4		ERD25TJ221	Carbon Resistor 1/4W 220Ω	1	
R1,R2,R13		ERD25TJ472	Carbon Resistor 1/4W 4.7kΩ	3	
8A,5D 6H,11J		M74LS175P	IC	4	
8B,11C,12E 6G		M74LS174P	IC	4	
2C		M74LS164P	IC	1	
4M,3P		M74LS138P	IC	2	
8J,8K,8L, 8M		M74LS257AP	IC	4	
5F,11H		M74LS20P	IC	2	
3C,1E 2M		M74LS244P	IC	3	
3J		M74LS243P	IC	1	
11D		M74LS240P	IC	1	
5N,5P		M74LS158P	IC	2	
8C,6D 7F, 6K		M74LS32P	IC	4	
12L,10P,12H		M74LS393P	IC	3	
2E,3E,10G 1K,1L,10N		M74LS373P	IC	6	
9D,10H, 10J,2K		M74LS245P	IC	4	
X1		YJJFX00360B4	Crystal Oscillator	1	
X2		YJJFX00390B4	Crystal Oscillator	1	
5G,11G,11P		M74LS51P	IC	3	
6C,4D,7H		M74LS74AP	IC	3	
5K		M74LS670P	IC	1	
4G		M5L8253P-5	LSI	1	
3B		M5L8255AP5	LSI	1	
4J		M5L8259AP	LSI	1	

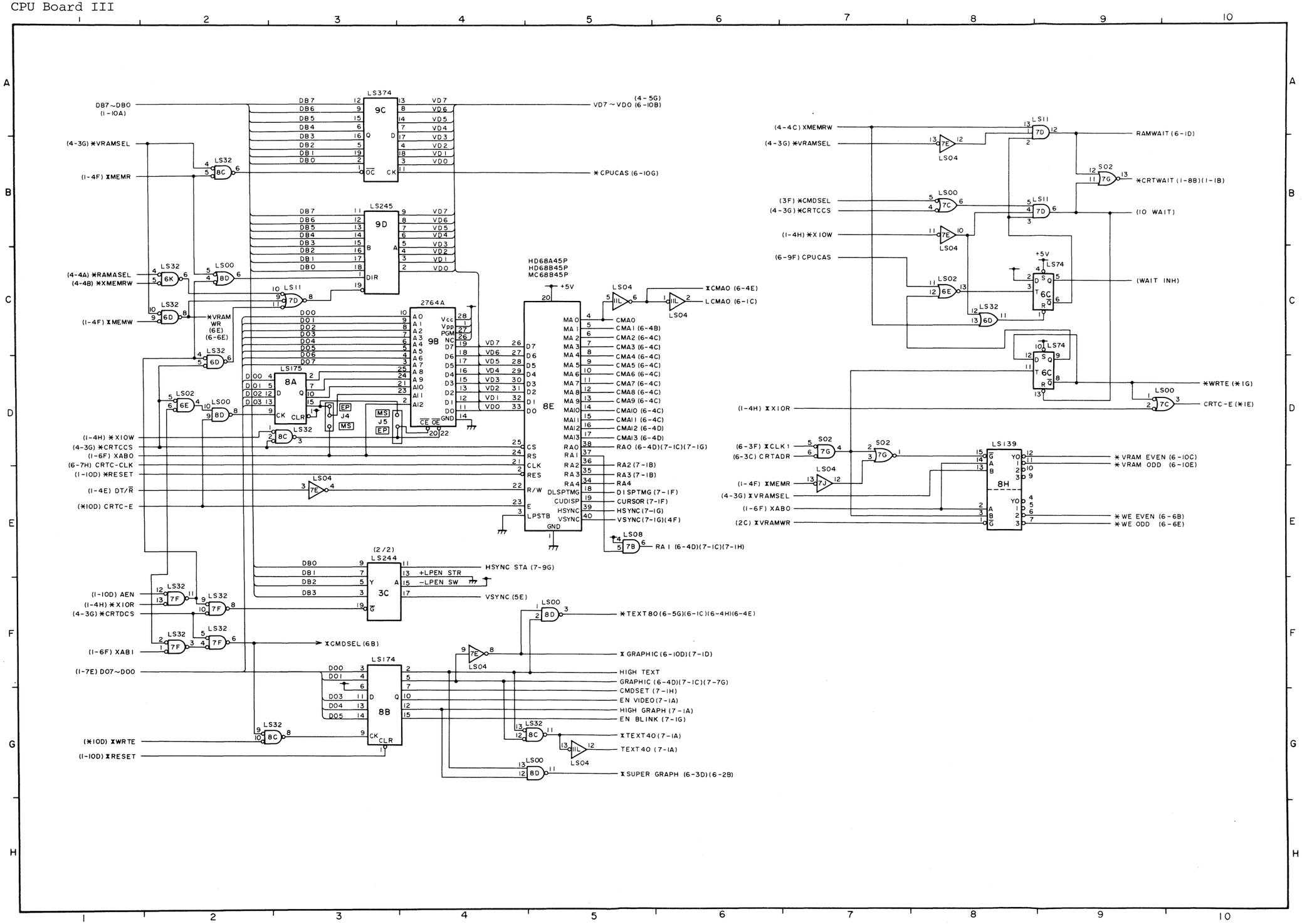
Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
10R		M74LS290P	IC	1	
ICP		YJSP5—2A	IC Protector	1	
4(5)A		YJJSE04820BR	Bios ROM (128k)	1	
10(11)A		YJJSE04780BR	CHG ROM (64k)	1	
9A		YJJSE04830BR	CON ROM (64k)	1	
CN		YJJDK02820B4	CN Cable	1	

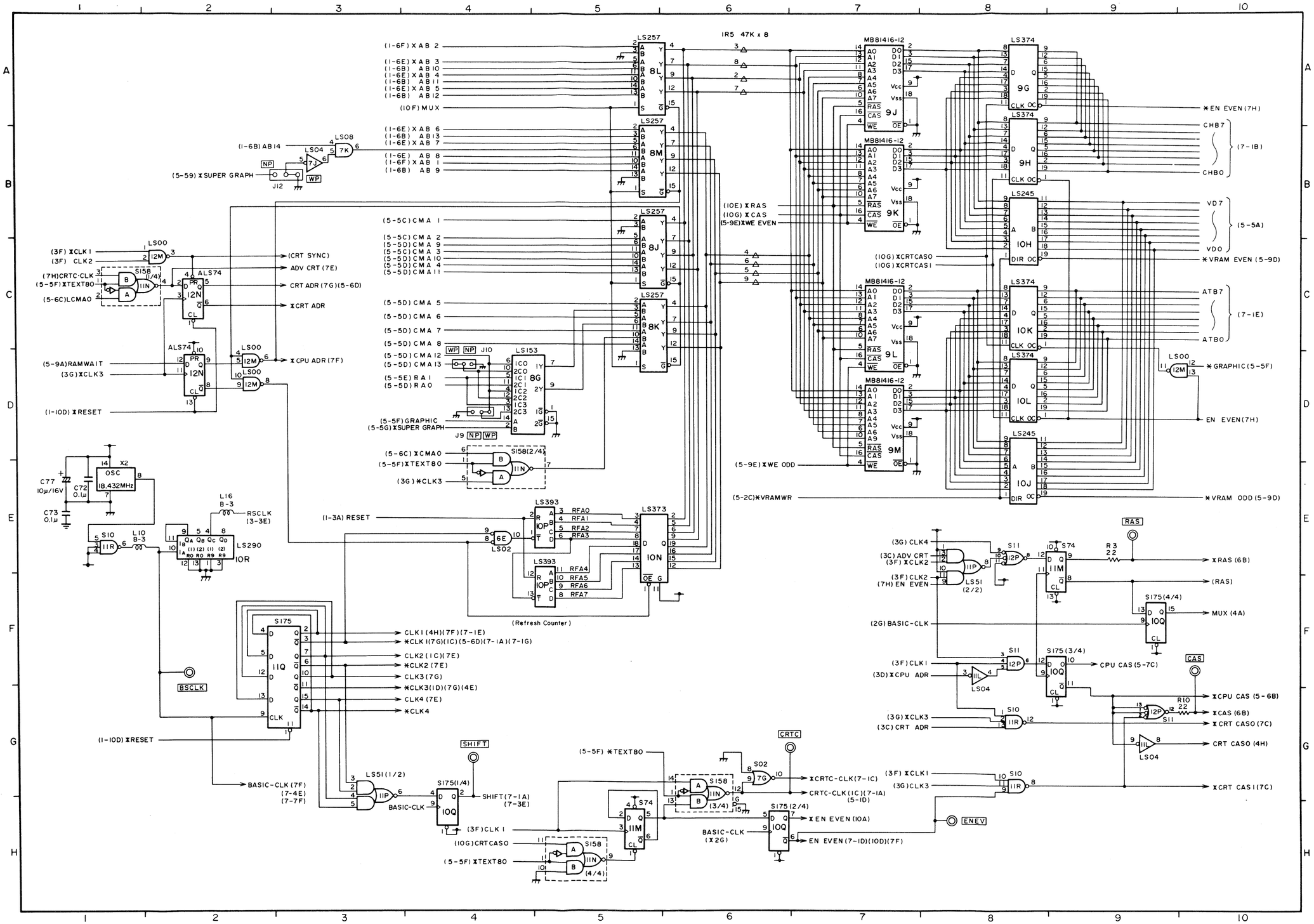
6.1 CPU Board (PLSMX)

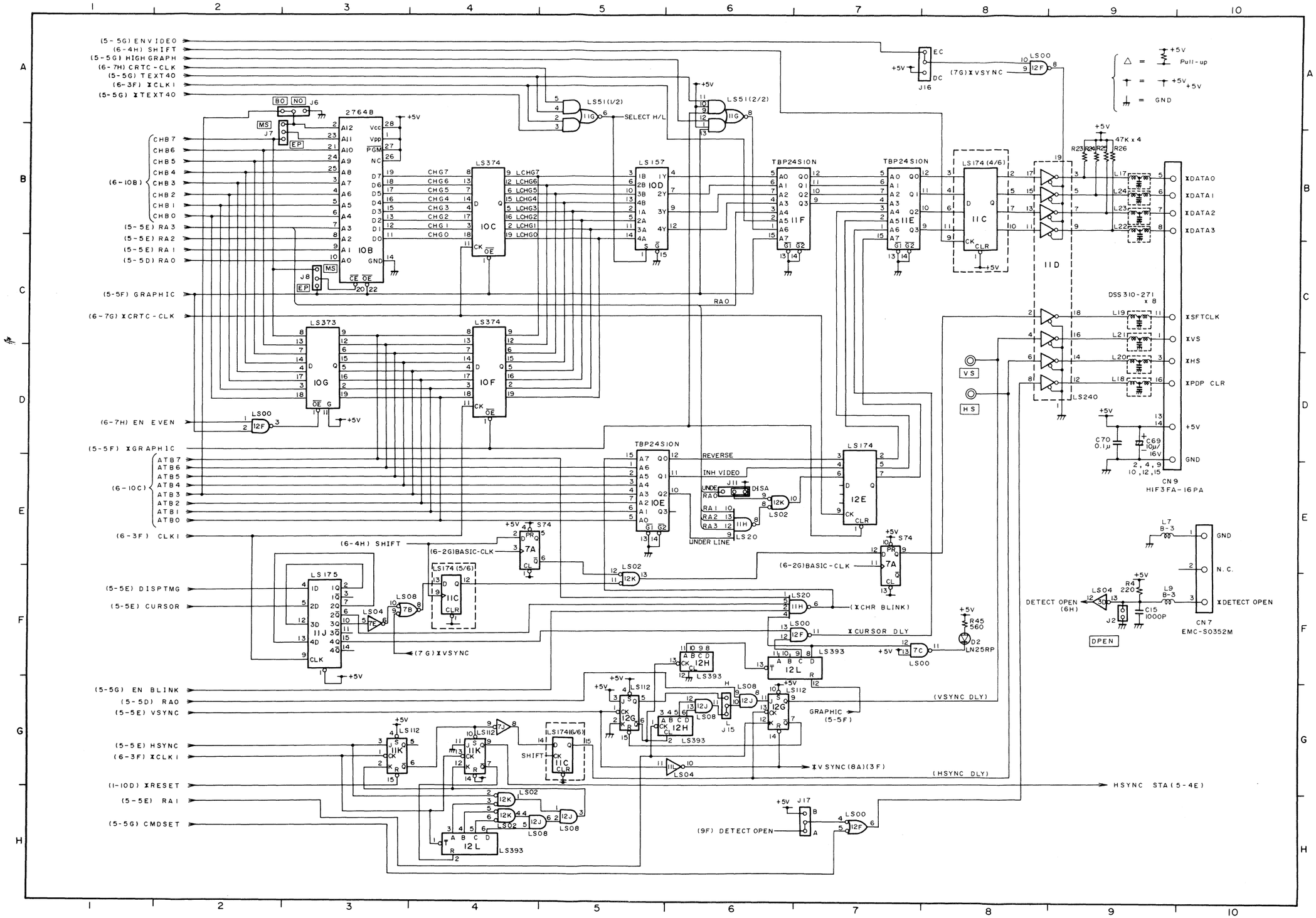


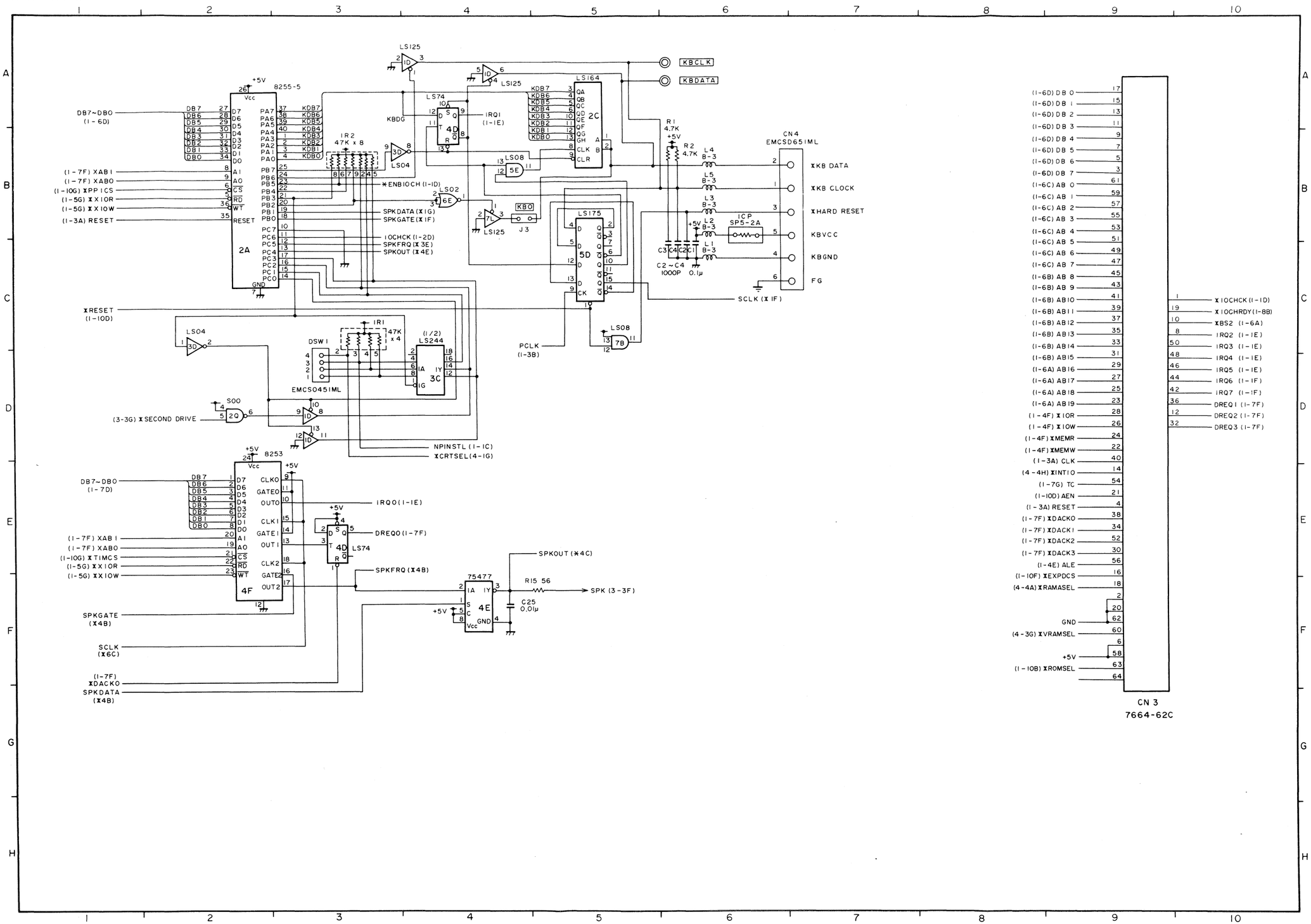

14.3M
OSC X1 14.31818MHz
C12 10μ/16V
C10 0.1μ
C11 0.1μ
8284A
2N
RESET
CLK
READY
RES
PCLK
DCLK
(2-5C) (3-3E)
(5-9B) XCRTWAIT
(X10B) XEXTWAIT
(X10E) XADVNC
(X10D) DMAWAIT
(3-3F) XPOR
*RES
CR
D1 MA162
R9 47K
C17 47μ/16V
(X3A) CLK
XCLK(X8E)
(X5E)(X8C)
LS31
(2-4D) NPINSTL
(X5D) NPNMI
(X7D) DO7
(X10G) XWTNMI
(X10D) XRESET
(2-3B) XENBIOCH
(2-10C) XIOCHCK
R37 1.2K
IOCHCK (2-3B)
INTR (X2E)
INTA
(2-9E)(6-3E)(3-3D)
RESET (X8D)(X5E)(2-1B)
CLK (X1C)(X8D)(8-9D)
1J
8088
1G
8087
NMI
INTR
RQ/GT0
RQ/GT1
LOCK
XLOCK (X8D)
MN/MX
RGGT0
RGGT1
BHE
BUSY
XS0 XS1 XS2
XS0~S0 (X5A)(X8D)
GND GND
LS04
(X4E) XS2
62(X8C)
LS373
1K
1E
2E
LS244
LS245
2K
ABS2 (X8G)(2-10C)
ABI9 (X4G)(4-1B)
ABI8 (X8B)(4-1F)
ABI7 (2-9D)
ABI6
ABI5
ABI4
ABI3
(4-1A) (X7G)
(X8B)
(2-9C)
(4-1D)
(6-3A)
(6-3B)
ABI2
ABI1
ABI0
AB 9 (X8F)
AB 8 (X8F)
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
(X8F)
(2-9B)(2-9C)
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
(X1F)
(X5G)
(X10A)(3-3C)
(2-9A)(2-9B)
(2-1A)(5-1A)
(2-1E)
DT/R
DEN
(X4E)
NPNMI (X1C)
XDEN
XAENCPU (X10E)
ALE
DO7(X1C)
DO6
DO5
DO4
DO3(X3H)
DO2(X3H)
DO1(X3H)
DO0(X3H)
(X5G)
(3-3B)
(5-1F)
8259A
4J
(2-3E) IRQ0
(2-4A) IRQ1
(2-10C) IRQ2
(2-10C) IRQ3
(2-10C)(3-3E) IRQ4
(2-10D) IRQ5
(2-10D)(3-3E) IRQ6
(2-10D)(3-3F) IRQ7
(X10G) XINTCS
(X5G) XX10W
(X5G) XX10R
(X7F) XABO
(X2D) INTR
SP/EN
R16 47K
CAS0
CAS1
CAS2
DB7~DBO (X6D)
8288
3F
XS0 XS1 XS2
IOWC
AIOWC
IORC
AMWC
MRDC
MWTC
(X10D) XAENCPU
XAEN (X10D)
(X10C) XAENDMA
(X10E) CENCPU
(X10E) XADVNC
(X10C) XPADVNC
X10W (2-9D)
X10R (2-9D)
XMEMW (2-9D) (5-1C)(4-1F)
XMEMR (2-9D) (5-1B)(4-1D) (5-6E)
XMWTC (4-1D)
8237A-5
3K
(X10C) DMARDY
(X2C) DCLK
(X3A) RESET
(X8F)(X8D) HRQ
(X10E) HLDA
DREQ0 (2-3E)
DREQ1 (2-10D)
DREQ2 (2-10D)(3-3D)
DREQ3 (2-10D)
DACK0 (X8C)(2-1F)(4-1A)(2-9E)
DACK1 (2-9E)
DACK2 (X3G)(3-3D)(2-9E)
DACK3 (X3G)(2-9E)
EOP
ABST
(4-1C)(4-1C)
TC (2-9E)
XTC (3-3E)
DO7~DO0 (X7E)
3E
3J
LS243
LS670
5K
(X7F) XDACK3
(X7F) XDACK2
(X10C) XAENDMA
(X7F) XABO
(X7F) XAB1
(X10G) XDMAPGST
DO3~DO0 (X7E)
AB19(X6A)
AB18(X6A)
AB17(X6A)
AB16(X6A)
XMEMR
XMEMW
X10R
X10W
XX10R
XXMEMW
(X1)
(X1) XX10W (X1F)(X8H)(2-1B)(2-1E)(5-7B)(3-3D)(4-9D)(5-1D)
XX10R (X1F)(X8C)(2-1B)(2-1E)(5-6D)(3-3D)(5-1F)
XXMEMW (4-1C)
XXMEMR (X8C)(X8B)(4-1C)(4-9D)
(7E) XAB7 ~ XABO
DB7 ~ DBO (X6D)
4A
(X6B) AB13 ~ AB8
(X6A) AB16
(X6A) AB17
(X6A) AB18
(X6A) AB19
(X6B) AB14
(X6B) AB15
(X5G) XXMEMR
XROMSEL (2-9F)
(5-10B) XCRTWAIT
(2-10C) XIOCHRDY
(X10E) XAENCPU
(X5G) XX10R
(X5G) XXMEMR
(X7F) XDACKO
(X2C) DCLK
R17 1.2K
XEXTWAIT (X1B)
DMARDY (X5E) (4-1D)
ADW
NW
(X4E) ALE
(X6A) S2
(X10D) ENDDMA
(X10E) HLDA
(X4D) XLOCK
(X4E) XS1
(X4E) XS0
(X5F) HRQ
(X3A) CLK
(X3A) RESET
(X10D) AEN
XAENCPU (X10E)
XPADVNC (X10C)
(X2C) XCLK
XRESET (X10D)
(X10D) HOLD
HRQ (X5F)
XPADVNC (X3F)(X8E)
XAENDMA (X3F)(X3G) (X6H)
ENDDMA (X8D)
DMAWAIT (X1B)
AEN (X8C)(2-9E)(4-1D) (5-1F)
HOLD (X8E)
XAEN (X3F)
XRESET (X1D)(X8E) (2-1C) (3-3D) (5-1G) (5-1E)(6-1D) (6-1G) (7-1G) (7-1D)
XAENCPU (X8E) (X3F)(X5E)(X8C)(X8G)
CENCPU (X3F)
AENCPU
XADVNC (X1B)(X3F)
HLDA (X5F)(X8C)
24S10
3M
IR4 4.7K x4
3P
4M
6K
LS32
(X6C) AB2
AB3
AB4
AB5
AB6
AB7
(X6B) AB8
(X6B) AB9
(X6A) XBS2
(X10E) XAENCPU
(X7E) XAB5
(X7E) XAB6
(X7E) XAB7
X10W (X5G)
XPRTCS (3-3E)
XDSPCCS (4-1G)
XDSPDCS (4-1G)
XEXPDCS (2-9F)
XFDCCS (3-3D)
XFDDCS (3-3D)
XRSCCS (3-3E)
XDMACS (X5F)
XINTCS (X1F)
XTIMCS (2-1E)
XPPICS (2-1B)
XDMAPGST (X3G)
XWTNM! (X1D)
XCALDCS (3-3E)
XINIO (4-1H)

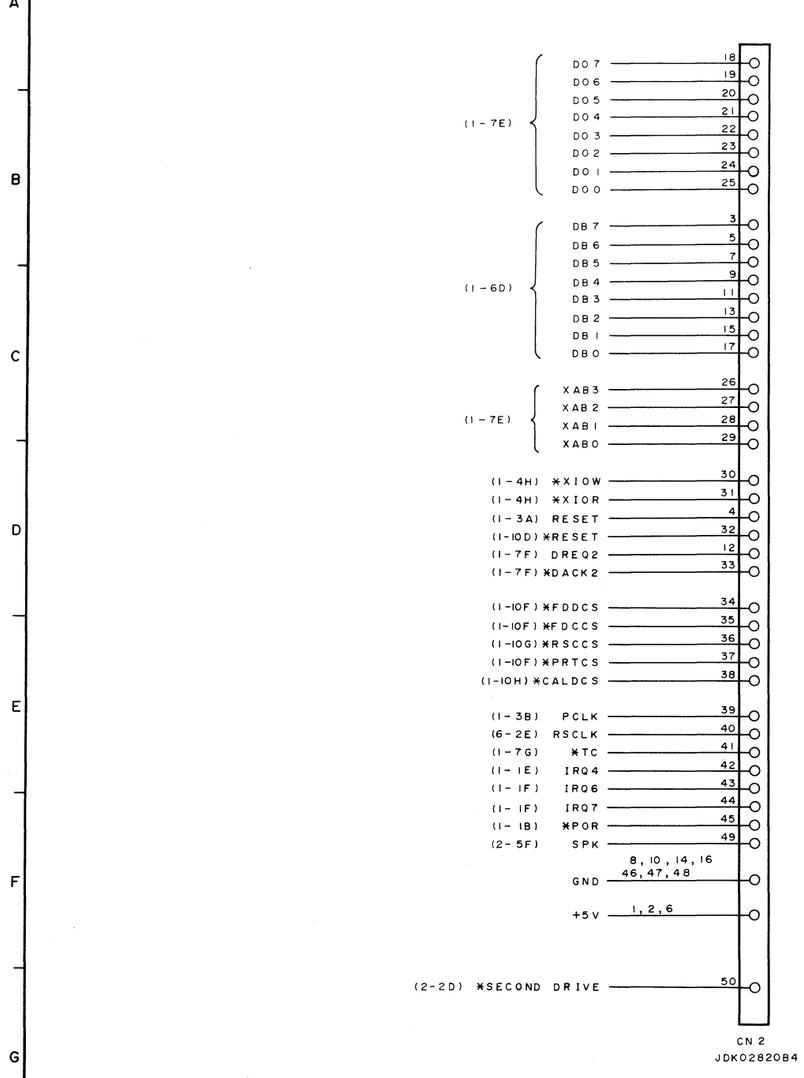

(1-6B) AB15
(1-7F) XDACKO
(1-6A) AB16
(1-6A) AB17
(1-6A) AB18
(1-6A) AB19
EX.256
J13
Z-152-2P
R14 47K
Normal → Short
EX.256 → OPEN
24S10
4N
S138
4P
+5V
R21 1.2K
R19 1.2K
R20 22
R22 22
XCASO (X5G)
XCAS1 (X5H)
XVRSEL (X1G)
RAMSEL (X1C)
XRAMASEL (2-9F)(5-1C)(X2-B)
(4A) XRAMASEL
(4D) X MWCTMG
XXMEMRW (5-1C)
XMEMRW (5-7A)
(1-3G) XXMEMR
(1-5G) XXMEMW
RADMPX (X1F)
(1-7F) *DACKO
(X4A) RAMSEL
S04
R36 1.2K
R35 1.2K
R40 22
R39 22
XRASO (X5G)
XRAS1 (X5H)
(1-4F) XMEMR
(1-4F) XMWTC
(1-10D) AEN
(1-10C) DMARDY
XMWCTMG (2B)
LS158
5N
5P
R34 22 x 4
R33
R32
R31
R27 22 x 4
R28
R29
R30
(1-7F) XAB0
(1-6B) AB14
(1-7F) XAB2
(1-6B) AB9
(1-7E) XAB4
(1-6B) AB11
(1-7E) XAB6
(1-6B) AB13
(1-7F) XAB1
(1-6B) AB8
(1-7E) XAB3
(1-6B) AB10
(1-7E) XAB5
(1-6B) AB12
(1-7E) XAB7
(1-6B) AB15
MA0 (X5G)
MA1 (X5G)
MA2 (X5G)
MA3 (X5G)
MA4 (X5G)
MA5 (X5G)
MA6 (X5G)
MA7 (X5G)
(X4C) RADMPX
LS51(2/2)
(1-6A) AB17
(1-6A) AB16
R38 22
MA8 (X5G)
(1-4F) XMEMW
R44 22
XWE (X5G)
(X4A) XVRSEL
R41, R43, R42 47K x 3
XVRAMSEL (5-1B)(5-6B)(5-6E)(2-9F)
(1-10F) XDSPCCS
XCRTCCS (5-1D)(5-6B)
(1-10F) XDSPDCS
XCRTDCS (5-1F)
(2-4D) XCRTSEL
(1-10H) X INIO
XINTIO (2-8E)
INTIO
D-RAM : 256K
150m
6P
6Q
6R
7N
7P
7Q
7R
8P
8Q
8R
9N
9P
9Q
9R
VD7
VD6
VD5
VD4
VD3
VD2
VD1
VD0
MA0~MA8
(X4D)(X4E)(X4F)
(X4C) XRASO
(X4B) XCASO
(X4F) XWE
VD7~VD0
(5-4A)
(*4C) *RAS1
(*4B) *CAS1

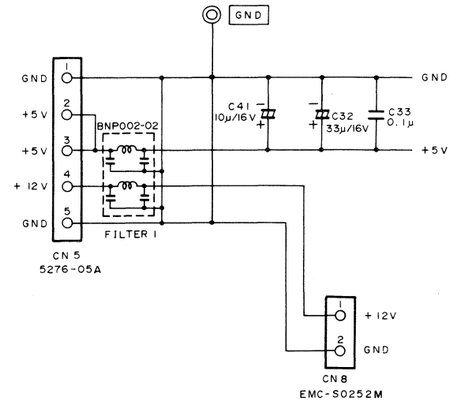

DB7~DB0 (1-10A)
(4-3G) *VRAMSEL
(1-4F) XMEMR
(4-4A) *RAMASEL
(4-4B) *XMEMRW
(1-4F) XMEMW
*VRAM WR (6E) (6-6E)
(1-4H) *X10W
(4-3G) *CRTCCS
(1-6F) XABO
(6-7H) CRTC-CLK
(1-10D) *RESET
(1-4E) DT/R
(*10D) CRTC-E
LS374
9C
LS245
9D
2764A
9B
LS175
8A
HD68A45P
HD68B45P
MC68B45P
8E
(4-5G) VD7~VD0 (6-10B)
*CPUCAS (6-10G)
XCMAO (6-4E)
LCMAO (6-1C)
CMA0
CMA1 (6-4B)
CMA2 (6-4C)
CMA3 (6-4C)
CMA4 (6-4C)
CMA5 (6-4C)
CMA6 (6-4C)
CMA7 (6-4C)
CMA8 (6-4C)
CMA9 (6-4C)
CMAI0 (6-4C)
CMAI1 (6-4C)
CMAI2 (6-4D)
CMAI3 (6-4D)
RA0 (6-4D)(7-1C)(7-1G)
RA1
RA2 (7-1B)
RA3 (7-1B)
RA4
DISPTMG (7-1F)
CURSOR (7-1F)
HSYNC (7-1G)
VSYNC (7-1G)(4F)
LS08
RA1 (6-4D)(7-1C)(7-1H)
(2/2)
LS244
3C
HSYNC STA (7-9G)
+LPEN STR
-LPEN SW
VSYNC (5E)
(1-10D) AEN
(1-4H) *X10R
(4-3G) *CRTDCS
XCMDSEL (6B)
(1-6F) XABI
(1-7E) D07~D00
LS174
8B
*TEXT80 (6-5G)(6-1C)(6-4H)(6-4E)
XGRAPHIC (6-10D)(7-1D)
HIGH TEXT
GRAPHIC (6-4D)(7-1C)(7-7G)
CMDSET (7-1H)
EN VIDEO (7-1A)
HIGH GRAPH (7-1A)
EN BLINK (7-1G)
XTEXT40 (7-1A)
TEXT40 (7-1A)
XSUPER GRAPH (6-3D)(6-2B)
(*10D) XWRTE
(1-10D) XRESET
(4-4C) XMEMRW
RAMWAIT (6-1D)
(3F) *CMDSEL
(4-3G) *CRTCCS
*CRTWAIT (1-8B)(1-1B)
IO WAIT
(1-4H) *X10W
(6-9F) CPUCAS
(WAIT INH)
*WRTE (*1G)
(1-4H) XX10R
CRTC-E (*1E)
(6-3F) XCLK1
(6-3C) CRTADR
(1-4F) XMEMR
(4-3G) XVRAMSEL
(1-6F) XABO
(2C) XVRAMWR
LS139
8H
*VRAM EVEN (6-10C)
*VRAM ODD (6-10E)
*WE EVEN (6-6B)
*WE ODD (6-6E)


IR5 47K x 8
LS257
8L
8M
8J
8K
LS153
8G
LS393
LS373
ION
LS02
LS00
LS04
LS08
LS10
LS11
LS51 (2/2)
LS74
LS158
LS175
LS245
LS290
LS374
MB8l416-12
9G
9H
9J
9K
9L
9M
10G
10H
10J
10K
10L
10M
10N
10P
10Q
10R
S158(2/4)
S175(1/4)
S175(2/4)
S175(3/4)
S175(4/4)
J9
J10
J12
X2
OSC
18.432MHz
C77 10µ/16V
C72 0.1µ
C73 0.1µ
L16 B-3
L10 B-3
RSCLK (3-3E)
BSCLK
SHIFT
CRTC
RAS
CAS
ENEV
R3 22
R10 22
(1-6F) XAB 2
(1-6E) XAB 3
(1-6B) AB10
(1-6E) XAB 4
(1-6B) AB11
(1-6E) XAB 5
(1-6B) AB12
(10F) MUX
(1-6E) XAB 6
(1-6B) AB13
(1-6E) XAB 7
(1-6E) AB 8
(1-6F) XAB 1
(1-6B) AB 9
(1-6B) AB14
(5-59) XSUPER GRAPH
(5-5C) CMA 1
(5-5C) CMA 2
(5-5D) CMA 9
(5-5C) CMA 3
(5-5D) CMA 10
(5-5D) CMA 4
(5-5D) CMA 11
(5-5D) CMA 5
(5-5D) CMA 6
(5-5D) CMA 7
(5-5D) CMA 8
(5-5D) CMA 12
(5-5D) CMA 13
(5-5E) RA 1
(5-5D) RA 0
(5-5F) GRAPHIC
(5-5G) XSUPER GRAPH
(5-6C) XCMA 0
(5-5F) XTEXT 80
(3G) *CLK3
(1-3A) RESET
(Refresh Counter)
(10E) XRAS
(10G) XCAS
(5-9E) XWE EVEN
(5-9E) XWE ODD
(5-2C) *VRAMWR
*EN EVEN (7H)
CHB7
CHB0
(7-1B)
VD7
VD0
(5-5A)
*VRAM EVEN (5-9D)
ATB7
ATB0
(7-1E)
*GRAPHIC (5-5F)
EN EVEN (7H)
*VRAM ODD (5-9D)
(3F) XCLK 1
(3F) CLK2
(7H) CRTC-CLK
(5-5F) XTEXT 80
(5-6C) LCMA 0
(5-9A) RAMWAIT
(3G) XCLK3
(1-10D) XRESET
(CRT SYNC)
ADV CRT (7E)
CRT ADR (7G)(5-6D)
XCRT ADR
XCPU ADR (7F)
CLK1 (4H)(7F)(7-1E)
*CLK1 (7G)(1C)(5-6D)(7-1A)(7-1G)
CLK2 (1C)(7E)
*CLK2 (7E)
CLK3 (7G)
*CLK3 (1D)(7G)(4E)
CLK4 (7E)
*CLK4
BASIC-CLK (7F) (7-4E) (7-7F)
SHIFT (7-1A) (7-3E)
(3F) CLK1
(10G) CRTCASO
(5-5F) XTEXT 80
(5-5F) *TEXT80
CRTC-CLK (7-1C)
CRTC-CLK (1C) (7-1A) (5-1D)
XEN EVEN (10A)
BASIC-CLK (X2G)
EN EVEN (7-1D)(10D)(7F)
(3G) CLK4
(3C) ADV CRT
(3F) XCLK2
(3F) CLK2
(7H) EN EVEN
(2G) BASIC-CLK
(3F) CLK1
(3D) XCPU ADR
(3G) XCLK3
(3C) CRT ADR
XRAS (6B)
(RAS)
MUX (4A)
CPU CAS (5-7C)
XCPU CAS (5-6B)
XCAS (6B)
XCRT CASO (7C)
CRT CASO (4H)
XCRT CAS1 (7C)


(5-5G) ENVIDEO
(6-4H) SHIFT
(5-5G) HIGHGRAPH
(6-7H) CRTC-CLK
(5-5G) TEXT40
(6-3F) XCLK1
(5-5G) XTEXT40
B0 N0 J6
MS J7 EP
2764B
CHB7
CHB6
CHB5
CHB4
CHB3
CHB2
CHB1
CHB0
(6-10B)
(5-5E) RA3
(5-5E) RA2
(5-5E) RA1
(5-5D) RA0
J8
(5-5F) GRAPHIC
(6-7G) XCRTC-CLK
LS373
LS374
LS157
TBP24S10
LS174 (4/6)
47K x 4
DSS310-271 x 8
VS
HS
LS240
CN9 HIF3FA-16PA
(6-7H) EN EVEN
LS00
(5-5F) XGRAPHIC
ATB7
ATB6
ATB5
ATB4
ATB3
ATB2
ATB1
ATB0
(6-10C)
(6-3F) CLK1
LS51(1/2)
SELECT H/L
REVERSE
INH VIDEO
UNDE RA0
DISA
RA1 RA2 RA3
LS02
LS20
UNDER LINE
LS174
12E
(7G)XVSYNC
J16
△ = +5V Pull-up
+ = +5V +5V
⏚ = GND
(6-4H) SHIFT
(6-2G)BASIC-CLK
LS74
LS175
LS174 (5/6)
(5-5E) DISPTMG
(5-5E) CURSOR
LS08
LS04
(7G)XVSYNC
(6-2G)BASIC-CLK
(XCHR BLINK)
XCURSOR DLY
LS393
R45 560
D2 LN25RP
(5-5G) EN BLINK
(5-5D) RA0
(5-5E) VSYNC
(5-5E) HSYNC
(6-3F) XCLK1
(1-10D) XRESET
(5-5E) RA1
(5-5G) CMDSET
LS112
SHIFT
(VSYNC DLY)
GRAPHIC (5-5F)
XVSYNC(8A)(3F)
(HSYNC DLY)
HSYNC STA(5-4E)
(9F) DETECT OPEN
J17
XDATA0
XDATA1
XDATA2
XDATA3
XSFTCLK
XVS
XHS
XPDP CLR
+5V
GND
C70 0.1μ
C69 10μ/16V
2,4,9 10,12,15
L7 B-3
GND
N.C.
XDETECT OPEN
R4 220
C15 1000P
J2
DPEN
CN7 EMC-S0352M


8255-5
2A
8253
4F
LS125
LS74
4D
LS164
2C
LS08
5E
LS02
6E
LS175
5D
LS04
LS244
3C
DSW1
EMCS0451ML
IR1
47K x 4
IR2
47K x 8
S00
LS08
7B
LS125
7L
KBO
J3
R1 4.7K
R2 4.7K
L4 B-3
L5 B-3
L3 B-3
L2 B-3
L1 B-3
ICP SP5-2A
C3 C4 C2 C1
C2~C4 1000P
0.1μ
CN4 EMCSD651ML
KBCLK
KBDATA
DB7~DB0 (1-6D)
KDB7
KDB6
KDB5
KDB4
KDB3
KDB2
KDB1
KDB0
KBDG
IRQ1 (1-1E)
(1-7F) XAB1
(1-7F) XAB0
(1-10G) XPPICS
(1-5G) XX10R
(1-5G) XX10W
(1-3A) RESET
XRESET (1-10D)
ENBIOCH (1-1D)
SPKDATA (X1G)
SPKGATE (X1F)
IOCHCK (1-2D)
SPKFRQ (X3E)
SPKOUT (X4E)
PCLK (1-3B)
SCLK (X1F)
(3-3G) XSECOND DRIVE
NPINSTL (1-1C)
XCRTSEL(4-1G)
DB7~DB0 (1-7D)
IRQ0(1-1E)
DREQ0(1-7F)
SPKFRQ(X4B)
SPKOUT(X4C)
(1-7F) XAB1
(1-7F) XAB0
(1-10G) XTIMCS
(1-5G) XX10R
(1-5G) XX10W
SPKGATE (X4B)
SCLK (X6C)
(1-7F) XDACKO
SPKDATA (X4B)
75477
4E
R15 56
C25 0.01μ
SPK (3-3F)
XKB DATA
XKB CLOCK
XHARD RESET
KBVCC
KBGND
FG
(1-6D) DB 0
(1-6D) DB 1
(1-6D) DB 2
(1-6D) DB 3
(1-6D) DB 4
(1-6D) DB 5
(1-6D) DB 6
(1-6D) DB 7
(1-6C) AB 0
(1-6C) AB 1
(1-6C) AB 2
(1-6C) AB 3
(1-6C) AB 4
(1-6C) AB 5
(1-6C) AB 6
(1-6C) AB 7
(1-6B) AB 8
(1-6B) AB 9
(1-6B) AB10
(1-6B) AB11
(1-6B) AB12
(1-6B) AB13
(1-6B) AB14
(1-6B) AB15
(1-6A) AB16
(1-6A) AB17
(1-6A) AB18
(1-6A) AB19
(1-4F) XIOR
(1-4F) XIOW
(1-4F) XMEMR
(1-4F) XMEMW
(1-3A) CLK
(4-4H) XINT10
(1-7G) TC
(1-10D) AEN
(1-3A) RESET
(1-7F) XDACKO
(1-7F) XDACK1
(1-7F) XDACK2
(1-7F) XDACK3
(1-4E) ALE
(1-10F) XEXPDCS
(4-4A) XRAMASEL
GND
(4-3G) XVRAMSEL
+5V
(1-10B) XROMSEL
XIOCHCK (1-1D)
XIOCHRDY(1-8B)
XBS2 (1-6A)
IRQ2 (1-1E)
IRQ3 (1-1E)
IRQ4 (1-1E)
IRQ5 (1-1E)
IRQ6 (1-1F)
IRQ7 (1-1F)
DREQ1 (1-7F)
DREQ2 (1-7F)
DREQ3 (1-7F)
CN 3
7664-62C


(1-7E) DO7 18
DO6 19
DO5 20
DO4 21
DO3 22
DO2 23
DO1 24
DO0 25
(1-6D) DB7 3
DB6 5
DB5 7
DB4 9
DB3 11
DB2 13
DB1 15
DB0 17
(1-7E) XAB3 26
XAB2 27
XAB1 28
XAB0 29
(1-4H) *XIOW 30
(1-4H) *XIOR 31
(1-3A) RESET 4
(1-10D) *RESET 32
(1-7F) DREQ2 12
(1-7F) *DACK2 33
(1-10F) *FDDCS 34
(1-10F) *FDCCS 35
(1-10G) *RSCCS 36
(1-10F) *PRTCS 37
(1-10H) *CALDCS 38
(1-3B) PCLK 39
(6-2E) RSCLK 40
(1-7G) *TC 41
(1-1E) IRQ4 42
(1-1F) IRQ6 43
(1-1F) IRQ7 44
(1-1B) *POR 45
(2-5F) SPK 49
8, 10, 14, 16
46, 47, 48
GND
1, 2, 6
+5V
(2-2D) *SECOND DRIVE 50
CN 2
JDK02820B4


GND
GND
+5V
+5V
+12V
GND
1
2
3
4
5
BNP002-02
FILTER 1
C41
10μ/16V
C32
33μ/16V
C33
0.1μ
GND
+5V
CN 5
5276-05A
+12V
GND
CN 8
EMC-S0252M

REPLACEMENT PARTS LIST (PLSY)

NOTE:
- When ordering replacement parts indicate Part No. and Name of Parts.
- ⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.

Ref. No.		Parts No.	parts Name & Description	Pcs/Set	Remarks
C9,C13,C29		ECEB1CS100	Electrolytic Capacitor 16V 10 μF	3	
C2,C45		ECEB1CS330	Electrolytic Capacitor 16V 33 μF	2	
C10,C43		ECEB1ES330	Electrolytic Capacitor 25V 33 μF	2	
C25		ECQM1H472KZ	Film Capacitor 4700PF	1	
C3,C5,C7, C8,C12,C24 C28,C30 to C38, C40 to C42,C44, C46,C48 to C50		ECQV1H104JZ	Film Capacitor 0.1 μF	24	
C21		ECQV1H473JZ	Film Capacitor 50V 0.047 μF	1	
CB2,CB3		EXFP8101MW	Capacitor Array 50V 100PF x 8	1	
CB1		EXFP8102ZW	Capacitor Array 50V 1000PF x 8	1	
C23		YJ104B471KF	Ceramic Capacitor 50V 470PF	1	
CN11,CN26		EMCS0451ML	Connector	2	
CN14		YJJJC00640B4	Connector	1	
CN15		YJJJC00650B4	Connector	1	
CN19		YJ5275-05A	Connector	1	
CN20		YJ7634-62S	Connector	1	
CN12		YJ7650-62S	Connector	1	
CN21		YJ8564-45C	Connector	1	
D6,D7,D5		MA162	Diode	3	
L6		YJBNP002-02	Filter	1	
13G		YJJQL00181B4	VFO LSI	1	
13E		PST518A	Reset IC	1	
5C,6C		SN74LS31N	IC	2	
5E		SN74LS374N	IC	1	
10A		SN74S00N	IC	1	
4G A , 4G B		SN75150P	IC	2	
5G,6G		SN75154N	IC	2	
9F		UPD765AC	LSI	1	
IR5		YJARB00041B4	Resistor Array	1	
IR1, IR2		YJARB00071B4	Resistor Array	2	
IR4		YJARB00081B4	Resistor Array	1	
IR6		YJARB00191B4	Resistor Array	1	
L1,L2,L3, L4,L7		YJBL02RN2R62	Choke Coil	5	
L5		YJFDL-101	Coil	1	
R10		ERD10TJ184	Carbon Resistor 1/8W 180kΩ	1	
R12		ERD10TJ222	Carbon Resistor 1/8W 2.2kΩ	1	
R11		ERD10TJ273	Carbon Resistor 1/8W 27kΩ	1	
R9		ERD10TJ332	Carbon Resistor 1/8W 3.3kΩ	1	
R13		ERD10TJ564	Carbon Resistor 1/8W 560kΩ	1	
R19		ERD25TJ101	Carbon Resistor 1/4W 100Ω	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
R30		ERD25TJ122	Carbon Resistor 1/4W 1.2kΩ	1	
R20		ERD25TJ151	Carbon Resistor 1/4W 150Ω	1	
R6,R16,R17 R22 to R27 R31		ERD25TJ472	Carbon Resistor 1/4W 4.7kΩ	10	
R21		ERD25TJ473	Carbon Resistor 1/4W 47kΩ	1	
R7		ERD25TJ562	Carbon Resistor 1/4W 5.6kΩ	1	
R29		ERD25TJ682	Carbon Resistor 1/4W 6.8kΩ	1	
R1		ERO25CKF49R9	Metal Oxide Resistor 1/4W 49.9Ω	1	
SW2		YJAS1D-6M	Switch	1	
DSW1		YJDTS-3H	Dip Switch	1	
SYNC, CNTL, WINDOW, RDDATA, GND,INDEX		YJTM-027	Check Pin	6	
		YJZ-128	Pin	5	
J2,J3,J4,J5		YJZ-149-3P	Pin	4	
J1		YJZ-152-2P	Pin	1	
9C		SN74LS00N	IC	1	
10C,11A, 12F		SN74LS02N	IC	3	
6F,8C,10B 10E,12C		SN74LS04N	IC	5	
11E		SN74LS08N	IC	1	
5D		SN74LS20N	IC	1	
9E,11A,12F		SN74LS32N	IC	3	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
6D		SN74LS125N	IC	1	
11D		SN74LS153N	IC	1	
8D		SN74LS155N	IC	1	
6E		SN74LS174N	IC	1	
9D,10D		SN74LS175N	IC	2	
7E		SN74LS240N	IC	1	
2B,3B,4B, 4E,5B,8E		SN74LS244N	IC	6	
1B		SN74LS245N	IC	1	
11G		SN74LS273N	IC	1	
4F		SN74LS367AN	IC	1	
5F,11C		SN7406N	IC	2	
7D		SN7407N	IC	1	
12D,12E		SN7438N	IC	3	
7F		INS8250N-B	IC	1	
1G		YJPS-2006B	Photo-coupler	1	
CN22 to CN24		YJAJC02910B4	Connector	3	
X2		YJJFX00421B4	Crystal Oscillator	1	
11B		SN74LS74AN	IC	1	
X1		YJJFX00350B4	Crystal Oscillator	1	
7C		SN74LS253N	IC	1	

6.2 I/O Board (PLSY)

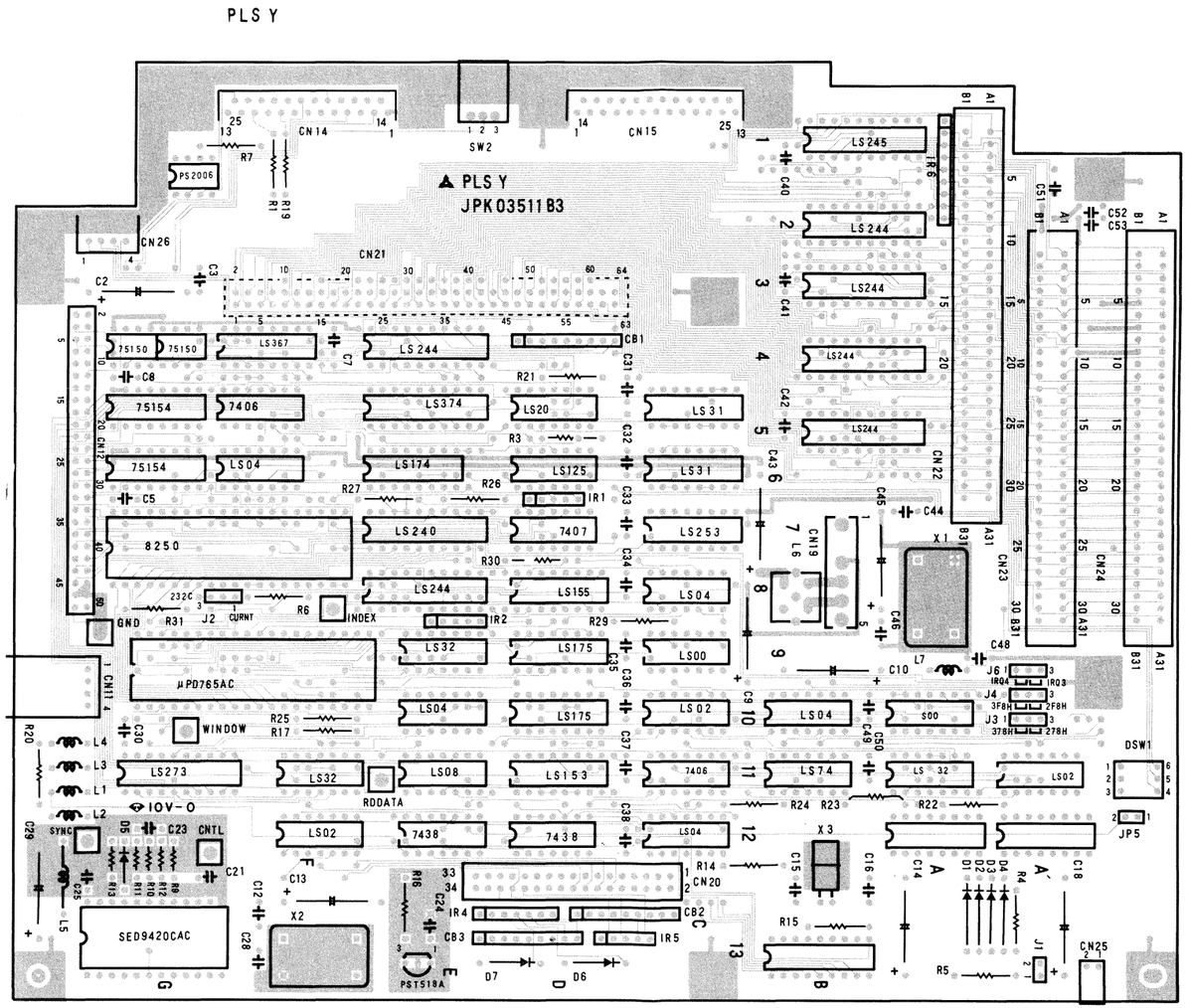
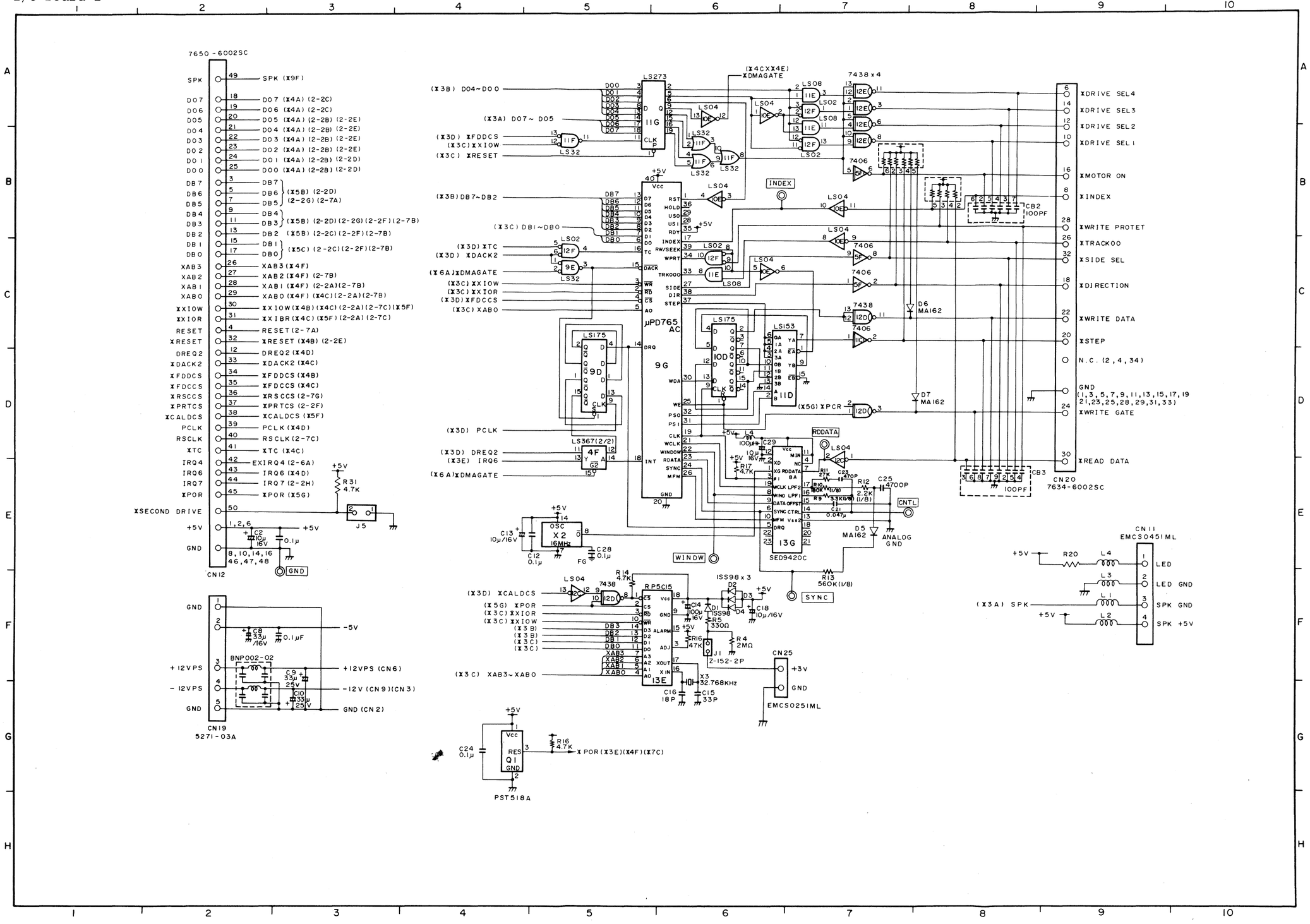
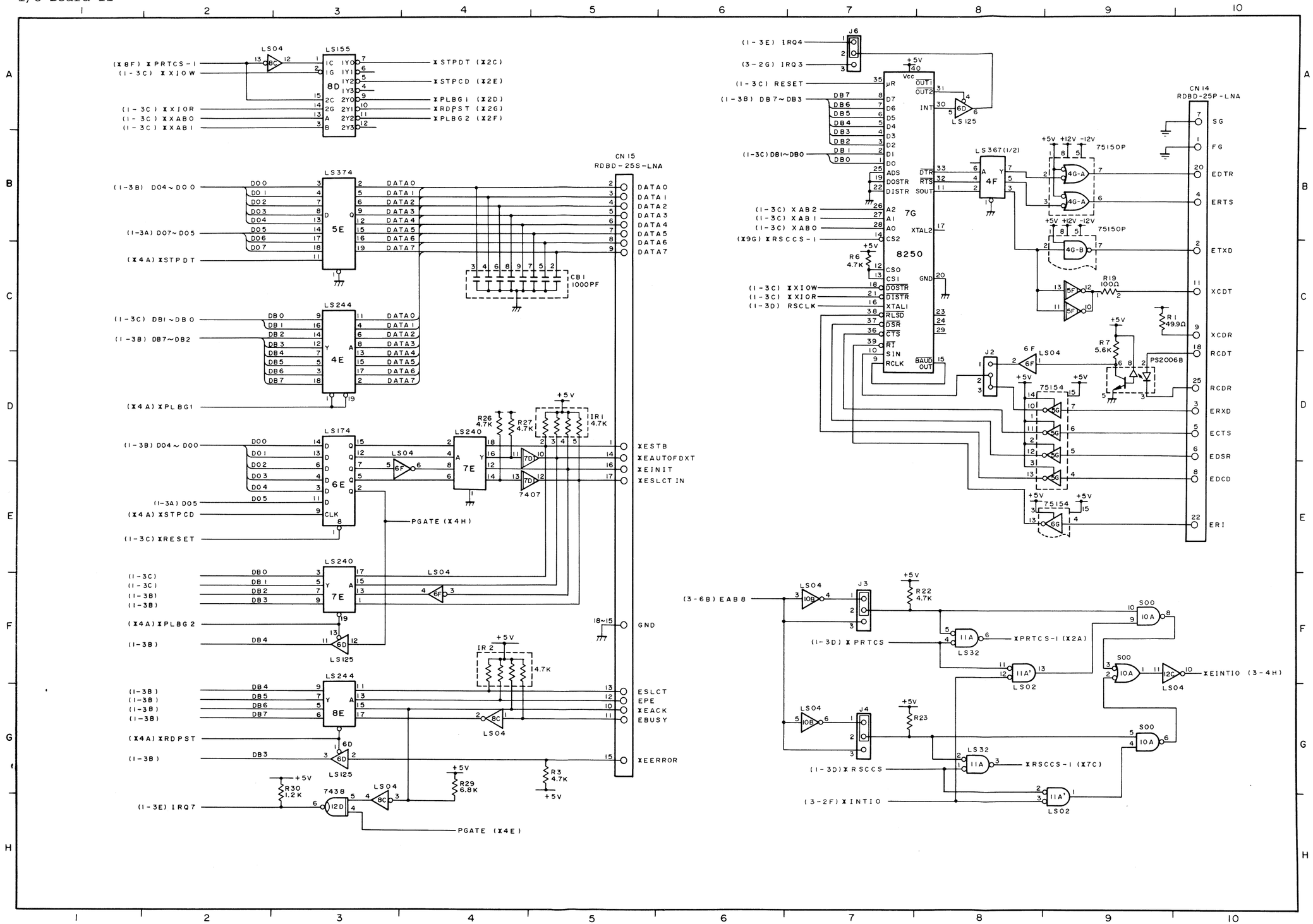


Figure 6-2 PLSY Parts Location


7650-6002SC
SPK
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
XAB3
XAB2
XAB1
XAB0
XXIOW
XXIOR
RESET
XRESET
DREQ2
XDACK2
XFDDCS
XFDCCS
XRSCCS
XPRTCS
XCALDCS
PCLK
RSCLK
XTC
IRQ4
IRQ6
IRQ7
XPOR
XSECOND DRIVE
+5V
GND
CN12
SPK (X9F)
DO7 (X4A) (2-2C)
DO6 (X4A) (2-2C)
DO5 (X4A) (2-2B) (2-2E)
DO4 (X4A) (2-2B) (2-2E)
DO3 (X4A) (2-2B) (2-2E)
DO2 (X4A) (2-2B) (2-2E)
DO1 (X4A) (2-2B) (2-2D)
DO0 (X4A) (2-2B) (2-2D)
DB7
DB6 (X5B) (2-2D)
DB5 (2-2G) (2-7A)
DB4
DB3 (X5B) (2-2D)(2-2G)(2-2F)(2-7B)
DB2 (X5B) (2-2C)(2-2F)(2-7B)
DB1
DB0 (X5C) (2-2C)(2-2F)(2-7B)
XAB3 (X4F)
XAB2 (X4F) (2-7B)
XAB1 (X4F) (2-2A)(2-7B)
XAB0 (X4F) (X4C)(2-2A)(2-7B)
XXIOW (X4B)(X4C)(2-2A)(2-7C)(X5F)
XXIBR (X4C)(X5F)(2-2A)(2-7C)
RESET (2-7A)
XRESET (X4B) (2-2E)
DREQ2 (X4D)
XDACK2 (X4C)
XFDDCS (X4B)
XFDCCS (X4C)
XRSCCS (2-7G)
XPRTCS (2-2F)
XCALDCS (X5F)
PCLK (X4D)
RSCLK (2-7C)
XTC (X4C)
EXIRQ4 (2-6A)
IRQ6 (X4D)
IRQ7 (2-2H)
XPOR (X5G)
R31 4.7K
J5
C2 10µ 16V
0.1µ
GND
CN19
5271-03A
GND
-5V
+12VPS
-12V
C8 33µ/16V
0.1µF
BNP002-02
C9 33µ 25V
C10 33µ 25V
+12VPS (CN6)
-12V (CN9)(CN3)
GND (CN2)
LS273
11G
(X3B) DO4~DO0
(X3A) DO7~DO5
(X3D) XFDDCS
(X3C) XXIOW
(X3C) XRESET
LS32
11F
(X4CXX4E) XDMAGATE
LS08
LS04
7438x4
7406
XDRIVE SEL4
XDRIVE SEL3
XDRIVE SEL2
XDRIVE SEL1
XMOTOR ON
XINDEX
XWRITE PROTET
XTRACK00
XSIDE SEL
XDIRECTION
XWRITE DATA
XSTEP
N.C. (2,4,34)
GND (1,3,5,7,9,11,13,15,17,19 21,23,25,28,29,31,33)
XWRITE GATE
XREAD DATA
CB2 100PF
CB3 100PF
CN20 7634-6002SC
INDEX
D6 MA162
D7 MA162
(X5G) XPCR
RDDATA
CNTL
D5 MA162
ANALOG GND
SYNC
WINDW
(X3D) DB7~DB2
(X3C) DB1~DB0
(X3D) XTC
(X3D) XDACK2
(X6A) XDMAGATE
(X3C) XXIOW
(X3C) XXIOR
(X3D) XFDDCS
(X3C) XABO
(X3D) PCLK
(X3D) DREQ2
(X3E) IRQ6
(X6A) XDMAGATE
µPD765 AC
9G
LS175
9D
10D
LS153
11D
LS367(2/2)
4F
9E
12F
11E
12D
LS02
LS08
LS04
7438
7406
OSC X2 16MHz
C13 10µ/16V
C12 0.1µ
C28 0.1µ
FG
SED9420C
13G
L4 100µH
C29 10µ 16V
R17 4.7K
R11 27K
R10 180K (1/8)
R9 3.3K (1/8)
C23 470P
C21 0.047µ
R12 2.2K (1/8)
C25 4700P
R13 560K (1/8)
(X3D) XCALDCS
(X5G) XPOR
(X3C) XXIOR
(X3C) XXIOW
(X3B)
(X3B)
(X3C)
(X3C)
(X3C) XAB3~XABO
R14 4.7K
RP5C15
13E
ISS98 x 3
D2
D1 ISS98
D3
D4
C14 100µ 16V
C18 10µ/16V
R5 330Ω
R16 47K
R4 2MΩ
J1 2-152-2P
CN25
+3V
GND
EMCS0251ML
X3 32.768KHz
C16 18P
C15 33P
C24 0.1µ
R16 4.7K
XPOR (X3E)(X4F)(X7C)
PST518A
CN11 EMCS0451ML
(X3A) SPK
R20
L4
L3
L1
L2
LED
LED GND
SPK GND
SPK +5V


LS04
LS155
(X8F) XPRTCS-1
(1-3C) XXIOW
(1-3C) XXIOR
(1-3C) XXABO
(1-3C) XXABI
XSTPDT (X2C)
XSTPCD (X2E)
XPLBG1 (X2D)
XRDPST (X2G)
XPLBG2 (X2F)
8D
CN15
RDBD-25S-LNA
LS374
(1-3B) D04~D00
(1-3A) D07~D05
(X4A) XSTPDT
5E
CB1
1000PF
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
LS244
(1-3C) DB1~DB0
(1-3B) DB7~DB2
4E
(X4A) XPLBG1
LS174
6E
(1-3A) D05
(X4A) XSTPCD
(1-3C) XRESET
PGATE (X4H)
LS240
7E
R26
4.7K
R27
4.7K
1R1
14.7K
+5V
7407
XESTB
XEAUTOFDXT
XEINIT
XESLCT IN
LS240
(1-3C)
(1-3C)
(1-3B)
(1-3B)
(X4A) XPLBG2
(1-3B)
LS125
LS244
8E
(X4A) XRDPST
(1-3B)
GND
ESLCT
EPE
XEACK
EBUSY
XEERROR
IR2
4.7K
R3
4.7K
R30
1.2K
7438
R29
6.8K
(1-3E) IRQ7
PGATE (X4E)
J6
(1-3E) IRQ4
(3-2G) IRQ3
(1-3C) RESET
(1-3B) DB7~DB3
(1-3C) DB1~DB0
(1-3C) XAB2
(1-3C) XAB1
(1-3C) XAB0
(X9G) XRSCCS-1
(1-3C) XXIOW
(1-3C) XXIOR
(1-3D) RSCLK
8250
7G
4F
LS367(1/2)
75150P
4G-A
4G-B
R6
4.7K
R19
100Ω
R1
49.9Ω
R7
5.6K
PS2006B
J2
75154
5G
6G
CN14
RDBD-25P-LNA
SG
FG
EDTR
ERTS
ETXD
XCDT
XCDR
RCDT
RCDR
ERXD
ECTS
EDSR
EDCD
ERI
(3-6B) EAB8
J3
J4
R22
4.7K
R23
(1-3D) XPRTCS
XPRTCS-1 (X2A)
(1-3D) XRSCCS
XRSCCS-1 (X7C)
(3-2F) XINTIO
XEINTIO (3-4H)
LS32
LS02
LS00
10A
11A
12C

8564 - 45000

CN21

LS244 5B

LS244 4B

LS244 3B

LS244 2B

LS245 1B

PSB4D31FC-1/2 or H421023-31

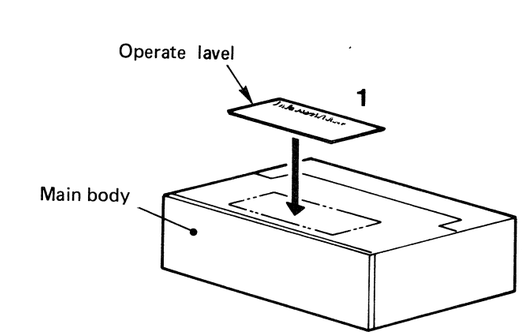
CN22 ~ CN24

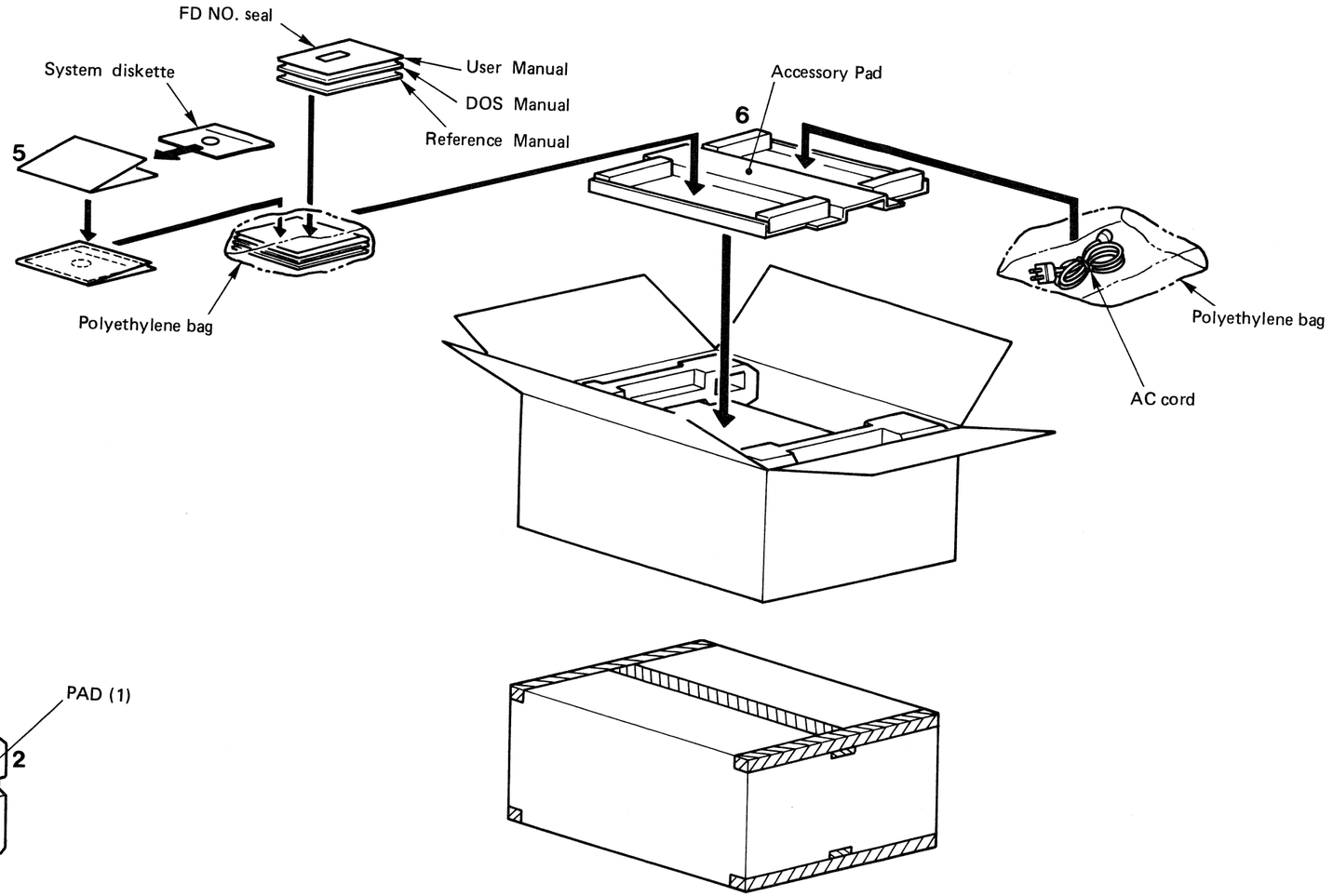
REPLACEMENT PARTS LIST (Packing)

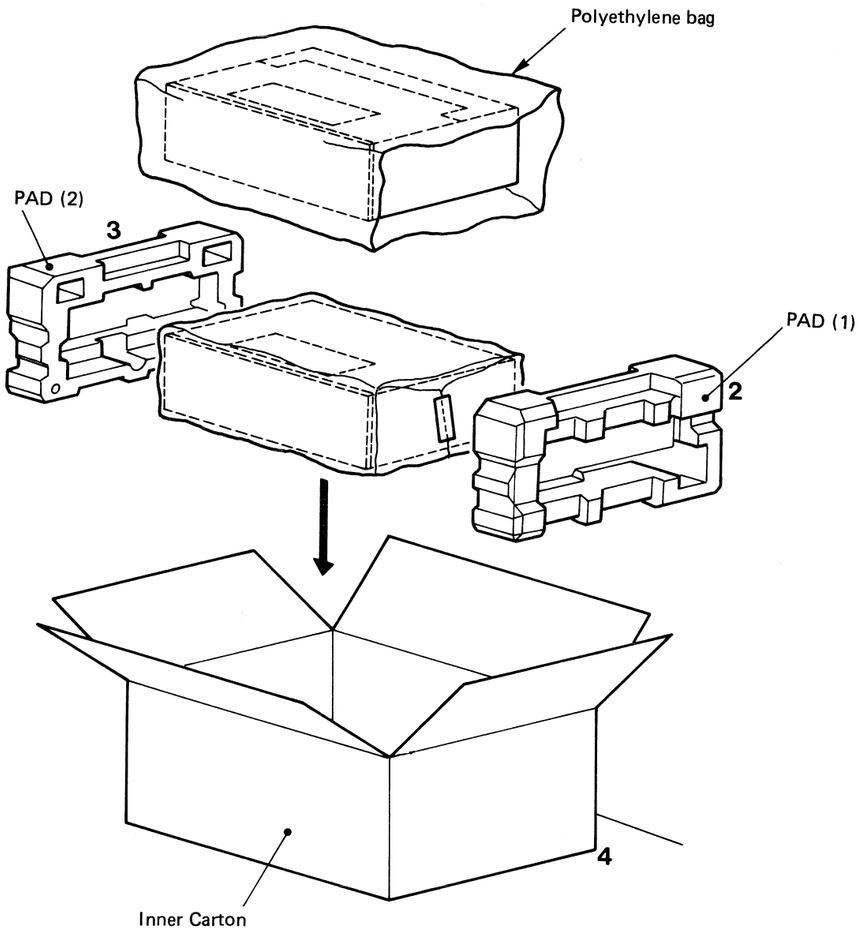
NOTE:
- When ordering replacement parts indicate Part No. and Name of Parts.
- ⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
1		YJJ7Q12680B4	Operate Lavel	1	
2		YJJ8C07550B2	Pad (1)	1	
3		YJJ8C07560B2	Pad (2)	1	
4		YJJ8B07540E3	Inner Carton	1	
5		YJJ8D07580B3	Diskette Wrap	1	
6		YJJ8D08020B4	Accessory Pad	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks


Operate lavel
1
Main body


FD NO. seal
System diskette
User Manual
DOS Manual
Reference Manual
5
Polyethylene bag
Accessory Pad
6
Polyethylene bag
AC cord


Polyethylene bag
PAD (2)
3
PAD (1)
2
4
Inner Carton

ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

III. PLASMA DISPLAY UNIT

1. SPECIFICATIONS

1.1 Display Panel

Number of dots: 400 dots (vert.) x 640 dots (horiz.) = 256,000 dots

Dot pitch: 0.36 mm (vert.) x 0.30 mm (horiz.)

Display area: 144 mm (vert.) x 192 mm (horiz.)

Display color: Neon orange

Display tilt: 90,100,110

Controllable plasma display intensity

1.2 Driver Unit

Refresh cycle: 53.8 Hz

Input/output signal level: TTL level

Power consumption: 34 W max

Characters and graphics can be displayed in specified size by inputting TTL-level vertical and horizontal sync signals, 4-bit data signals, and data-transfer shift clock signals.

The brightness can be controlled by the external potentiometer.

1.3 Power Supply

	Voltage	Current Capacity (max)
+V (for IC)	+5 V ±0.25 V	0.6 A
-VI (for IC)	-195 V ±5 V	60 mA
-V (for display)	-200 V ±5 V	150 mA

No specific make/break sequence is necessary for +V, -VI, and -V.

Handling Precautions

1) The panel has a glass container. Extreme care must be taken not to scratch, crack, or break the edges. Also take special care with the vent tube that protrudes from the rear of the glass container.

2) Install the unit with enough clearance to ensure good ventilation.

3) Protect the display unit from impact and extreme pressure.

4) Do not expose the display unit to strong electrostatic charges.

2. APPEARANCE

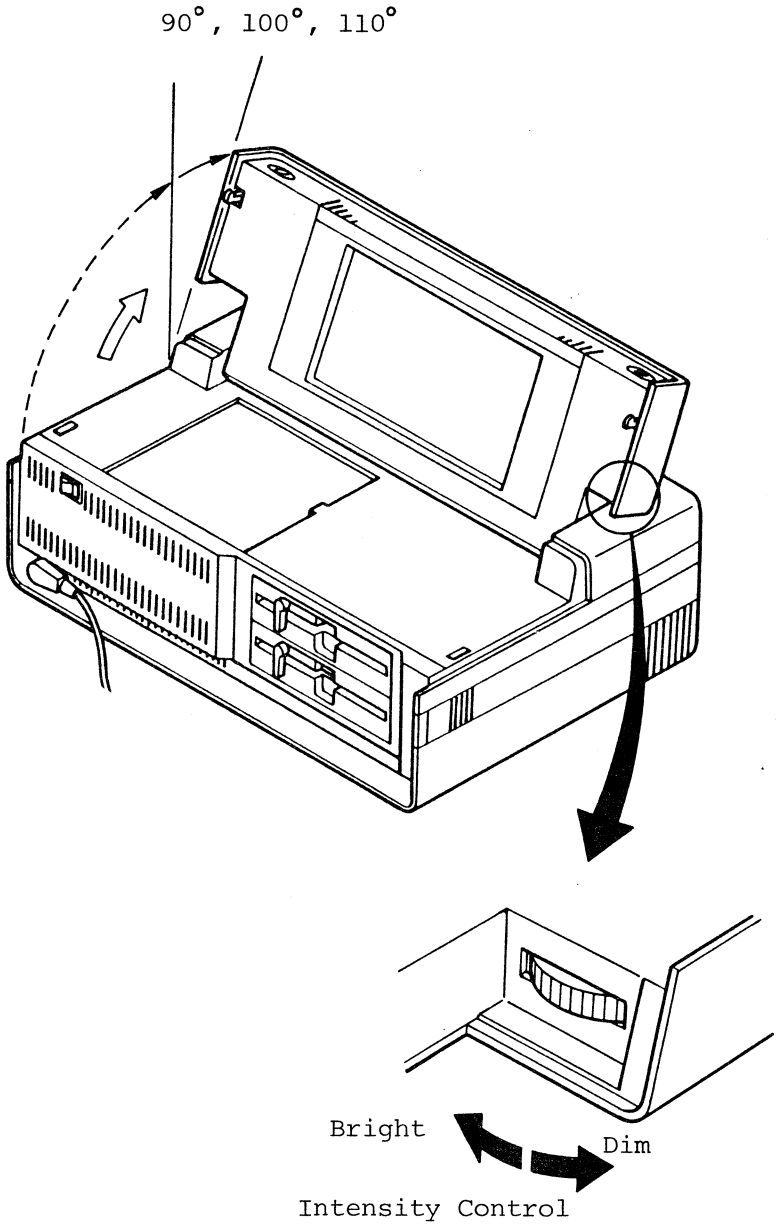


Figure 2-1 PDU Appearance

3. BLOCK DIAGRAM

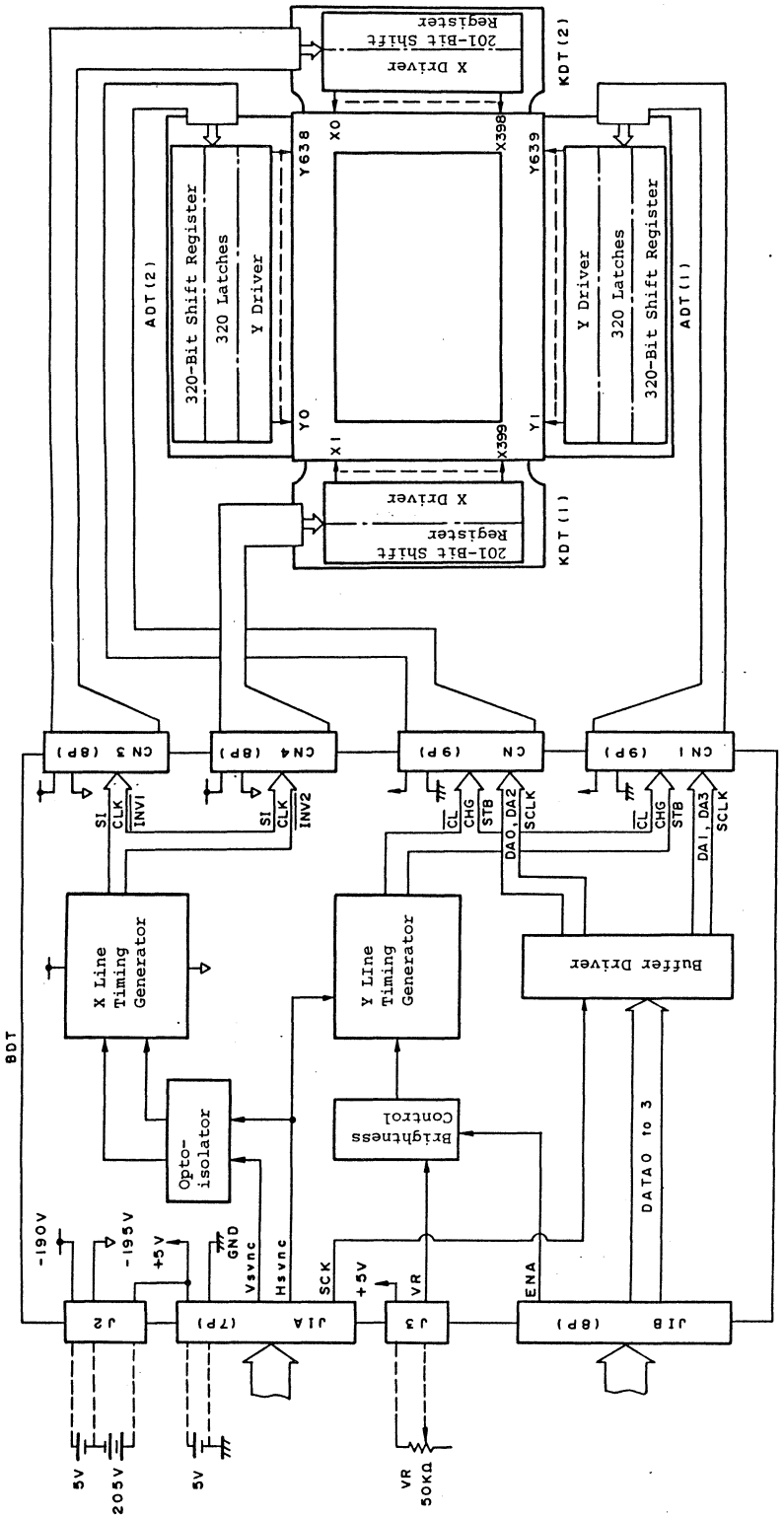


Figure 3-1 Display Unit Block Diagram

4. OPERATIONAL PRINCIPLES

4.1 Display Panel

The display panel is a DC plasma display panel (PDP) that utilizes the neon luminescence created by a DC discharge.

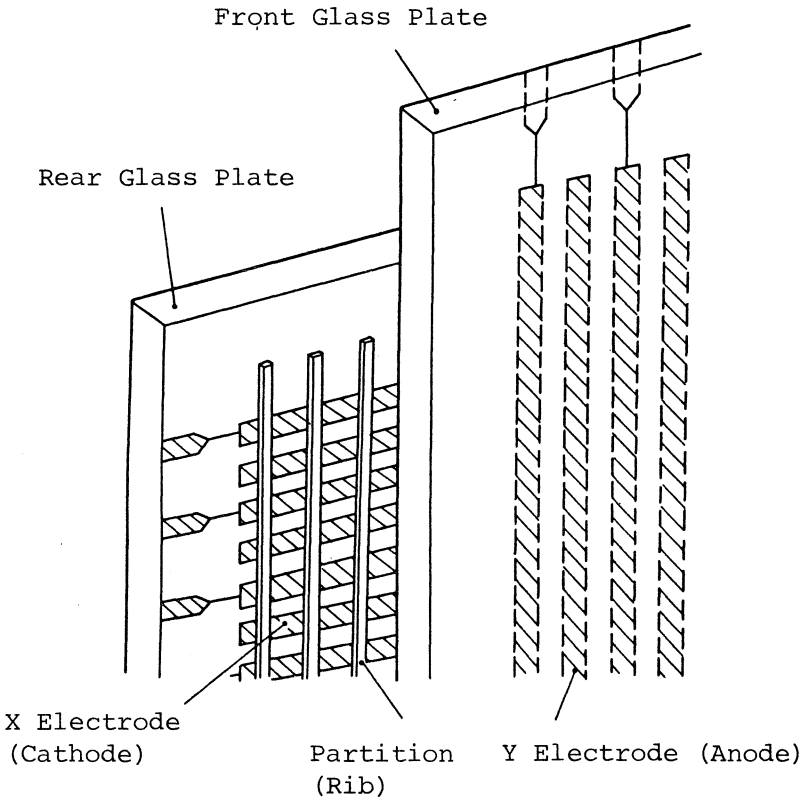


Figure 4-1 Structure of Display Panel

The structure of the panel is shown in Figure 4-1; 640 transparent Y electrodes are arrayed vertically on the front glass plate, while 401 X electrodes are arrayed horizontally on the rear glass plate. The uppermost X electrode is a reset electrode, and the remaining 400 X electrodes are display electrodes. Also, on the rear glass plate, partitions are installed. The peripheries of these two glass plates are sealed with frit (low-melting-point glass), to form a discharge space, which contains a Neon/Argon mixture and equivalent to 40 W fluorescent light.

The operation of the display panel is effected by linear sequential scanning. The X electrodes are sequentially scanned from top to bottom by time divisions, and a negative DC voltage (-205 V) is applied to the X electrode and a positive DC voltage to the Y electrode. A weak seed discharge is always transmitted, regardless of the presence or absence of a display discharge. This original method of operation provides a clear display with stable display discharge action and good contrast.

4.2 Display Unit

Figure 3-1 shows a block diagram of the display unit. The display unit is composed of a scanning circuit made up of the X driver devices KDT(1) and KDT(2), a display circuit made up of the Y driver devices ADT(1) and ADT(2), and an interface circuit made up of a timing generation/buffer device BDT used to connect the X and Y driver devices to the system unit.

Vertical and horizontal synchronous signals Vsync and Hsync 4-bit display data DA0 through DA3, and the shift clock pulse SCK (all TTL level) are entered as inputs into the interface circuit from the system unit. The signals Vsync and Hsync are converted from TTL level to a -200 V level by an optoisolator. Scanning signals Si, CLK, $\overline{INV1}$ and $\overline{INV2}$ are generated by an X line timing circuit. These signals are connected to the scanning circuits installed at the left and right of the display panel.

DATA0 through 3 and SCK are directly connected to the display circuit installed at the top and bottom of the display panel via a buffer driver. The operation signals STB, $\overline{CL}$ and CHG, generated by the Y line timing circuit from H sync are input to the display circuit.

4.3 Description of Operation

Figure 4-2 shows a block diagram of the scanning and display circuits. The following explanation refers to this figure.

A 201-bit shift register, NOR gates, and high voltage transistors, which are capable of sinking discharge currents of 640 bits, are installed in each of the left and right scanning circuits. The serial input Si and scanning clock CLK enter the left and right shift registers, and the contents of the registers shift from top to bottom, one-bit at a time. Based on the output inhibit signals $\overline{INV1}$ and $\overline{INV2}$, the left and right shift registers are alternately selected, and during the transition, a blanking period occurs, turning all the output transistors OFF.

As was previously mentioned, the X lines are sequentially scanned from above and a voltage of -200 V is applied. When the output transistors are OFF, the voltage is maintained at -95 V by the prebias resistors. The reset electrode XR is connected to the left and right driver circuits and remains ON for a period twice that of the other X lines, thus ensuring reset-discharging.

The following paragraph explains the operation of the display circuit, composed of Y driver circuits (Figure 4-2), during the horizontal scanning period (Figure 4-4).

First, the 4-bit parallel display data bits DA0 through DA3 are transmitted to the upper and lower 320-bit shift registers as 160 Y line data by the shift clock pulse SCLK. Then, the 640-bit display data of the shift registers is fetched to the latches at the trailing edge of the strobe STB. The blanking periods, tBn-1, tBn, ..., during which all the X lines are OFF, are provided within the respective horizontal scanning periods tHn-1, tHn, ... During these periods, the charge CHG forcibly switches the output transistors of the Y drivers to ON and charges the auxiliary discharge capacitors installed on each of the Y lines in the display panel.

Then, if, for example, Xn is switched ON when the latch output connected to Ym is "L" (LOW), the output transistor is switched OFF, and trigger signal is discharged based on the charge of the trigger capacitor (indicated by the broken lines in Figure 4-4). If this latch output is "H" (HIGH), the output transistor is switched ON, effecting a display discharge in which a fixed discharge current flows, constrained by the resistance RA. During this period, if the clear $\overline{CL}$ is made variable by means of the external volume, as shown in Figure 4-4, the output transistor is turned OFF regardless of the latch output, thus effecting luminance control. The discharge period is prolonged in the order ①, ②, ..., and the luminance rises, becoming 100% in the state indicated by ⑤.

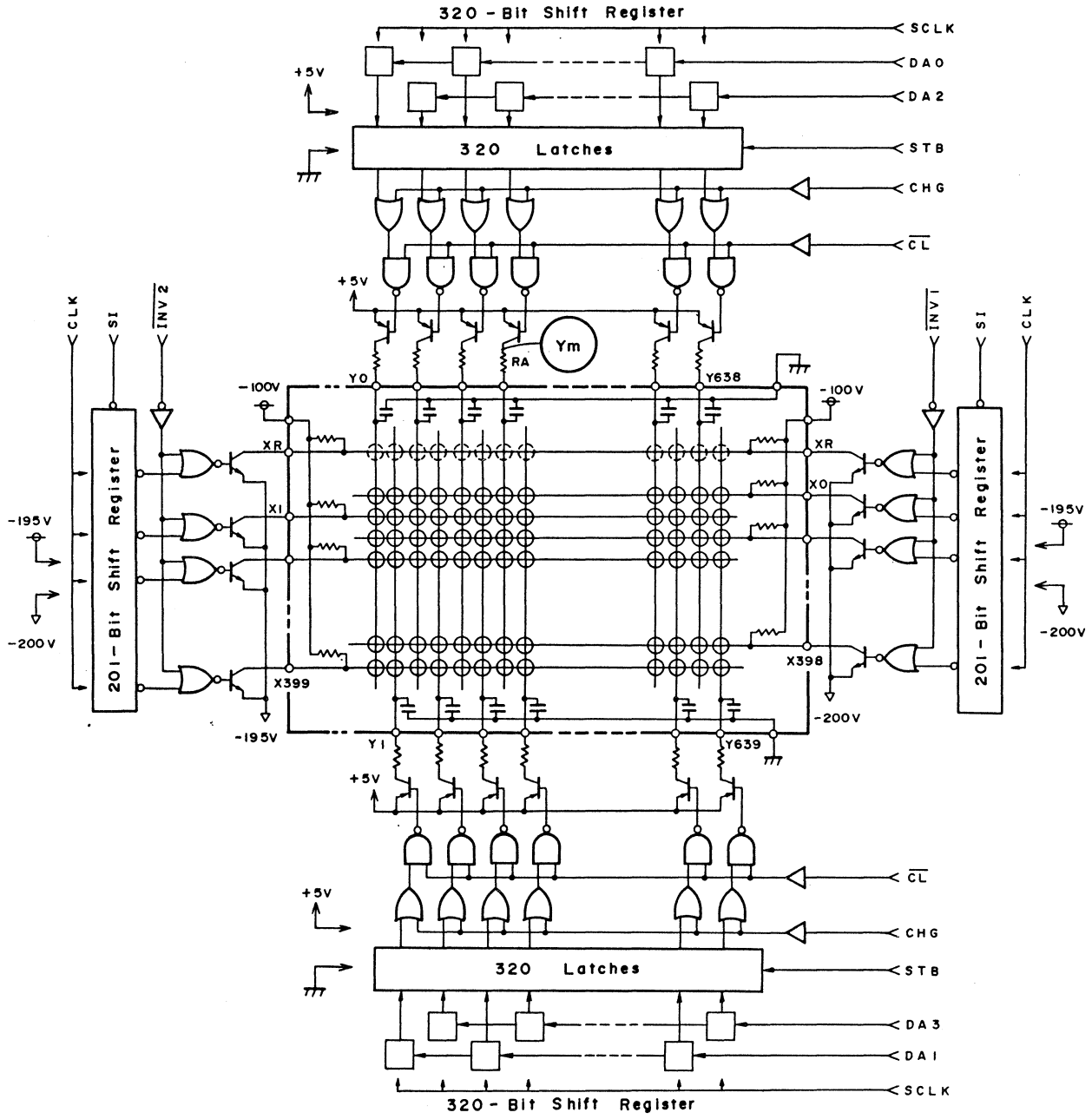


Figure 4-2 Logical Circuits of Scanning and Display

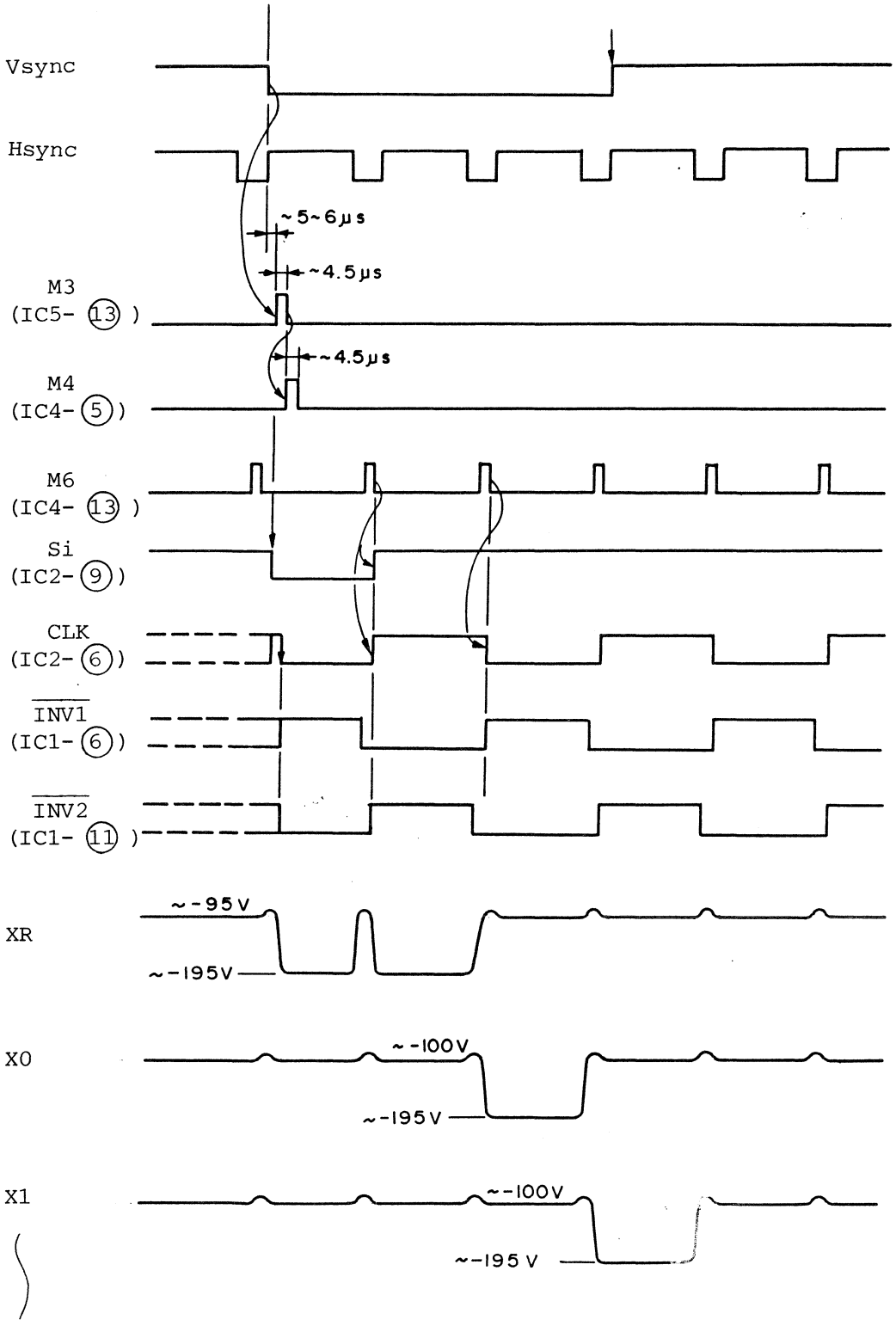


Figure 4-3 Timing Chart

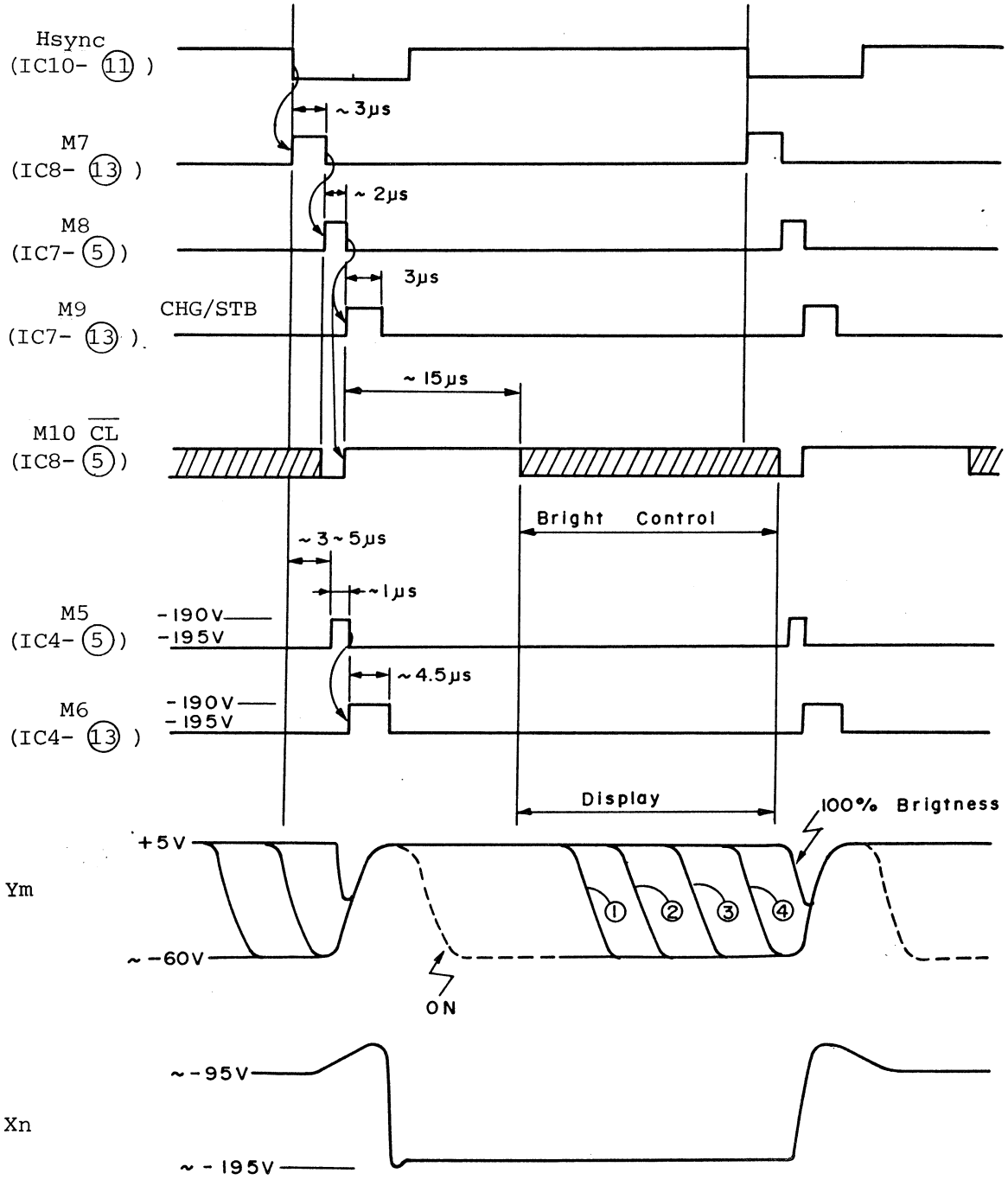


Figure 4-4 Operation During Horizontal Scanning Period

4.4 Names and Functions of Signals

Table 4-1

Signal Name	Symbol	Functions
Vertical synchronous signal	Vsync	Frame synchronous signal of display screen. Effects reset discharge.
Horizontal synchronous signal	Hsync	Clock signal scanning X lines.
Display data	DATA0 DATA3	4-bit parallel Y line display data, L: display, H: seed
Shift clock	SCK	Transmits DATA0 through DATA3 to Y line shift registers.
Enable	ENA	H: Ordinary display L: No voltage applied to Y lines

(Input Circuits)

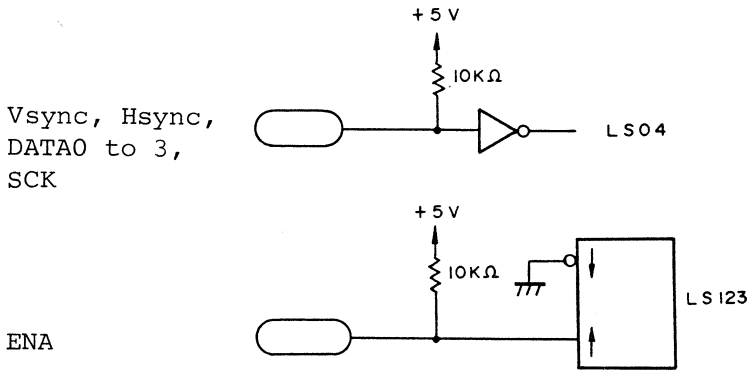


Figure 4-5

4.5 Notes

(1) Connect the 205 V (-205 V) and 5 V (-200 V) power sources to J2 in the floating state.

(2) The output stage of the optisolator of BDT, the X line timing generator, CN3, CN4, KDT(1) and KDT(2) are high voltage circuits; handle these circuits carefully. When checking the logic circuits, make certain that the plus side of the 205 V power source is OFF.

5. DISASSEMBLY PROCEDURE

5.1 Detaching Display from System Unit

Step 1

Preparation for Disassembly

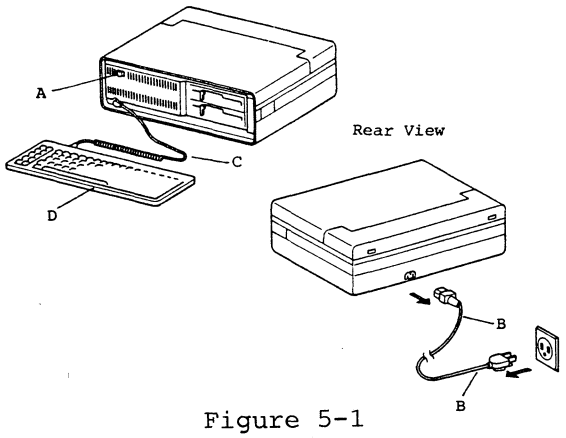
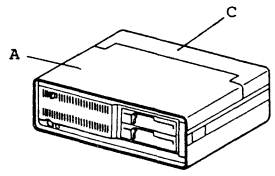


Figure 5-1

1. Set Main Power Switch [A] to OFF.
2. Unplug AC Cable [B] from outlet.
3. Disconnect all cables (AC Power Cord [B], Keyboard Cable [C], and all optional unit cables) from System Unit.
4. Move Keyboard [D] and all optional units away from working area.

Step 2

Removing Rear Upper Cover



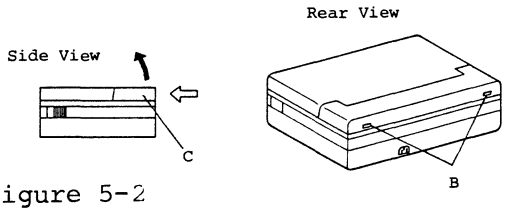
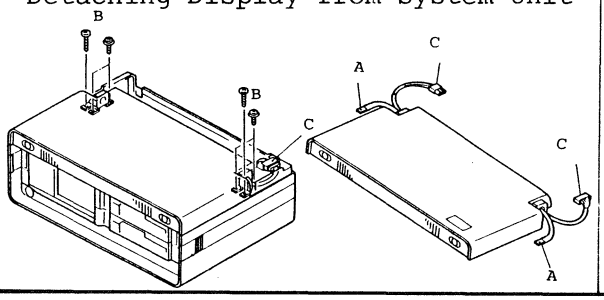


Figure 5-2

1. Press down on thumbsets [B] of Rear Upper Cover [C] and unlatch claws inside. Lift Rear Upper Cover [C] up from Upper Case.

Step 3

Detaching Display from System Unit



1. Detach Earth Cables [A] from System Unit.
2. Remove mounting screws [B].
3. Disconnect Connectors [C].
4. Lift Display up from System Unit.

Step 4

Disassembling Display Case

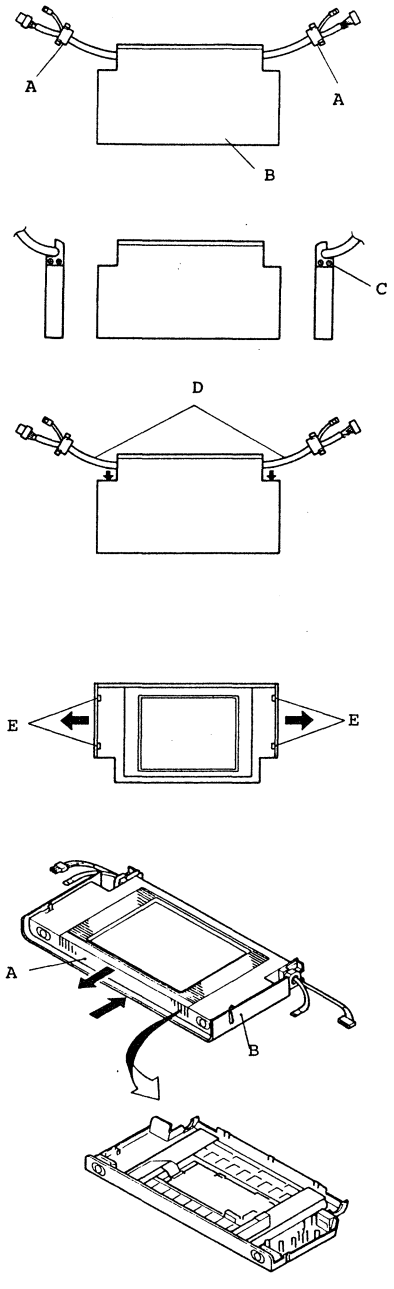


Figure 5-4 (continued)

1. Pull Softeners [A] approximately one inch away from Display [B].
2. Remove retaining screws [C].
3. Push cables [D] in direction indicated by arrows.
4. Turn over Display with screen up.
5. Unlatch side claws [E]. (Note: To unlatch side claws grasp both edges of display cover and pull out until the inside claws appear.)
6. Slide Display Unit [A] and Display Cover [B] in direction indicated by arrows.

Step 5

Removing Latch Assemblies

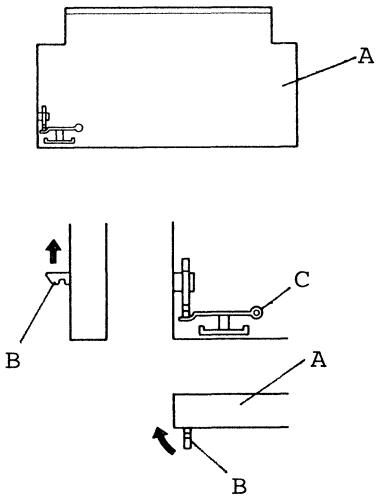


Figure 5-5

1. Place Display Unit [A] with screen down.
2. Slide hook [B] in direction indicated by arrow.
3. Remove lever [C].
4. Grasp hook [B] and pull up in direction indicated by arrow, then unclip from Display Unit [A].
5. Remove Spring from lever [C].
6. Remove Lock Button.

Step 6

Plasma

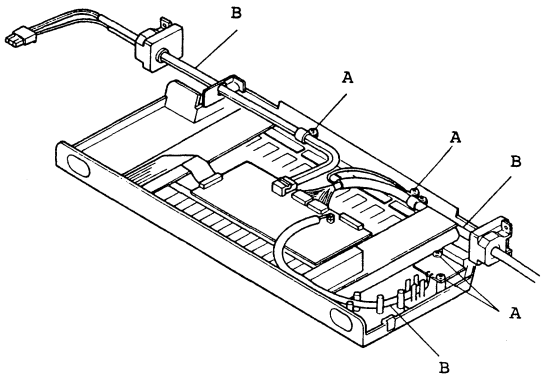


Figure 5-6

1. Remove mounting screws [A].
2. Disconnect connectors [B].

5.2 Driver Disassembly Procedure

Disassembling Procedure

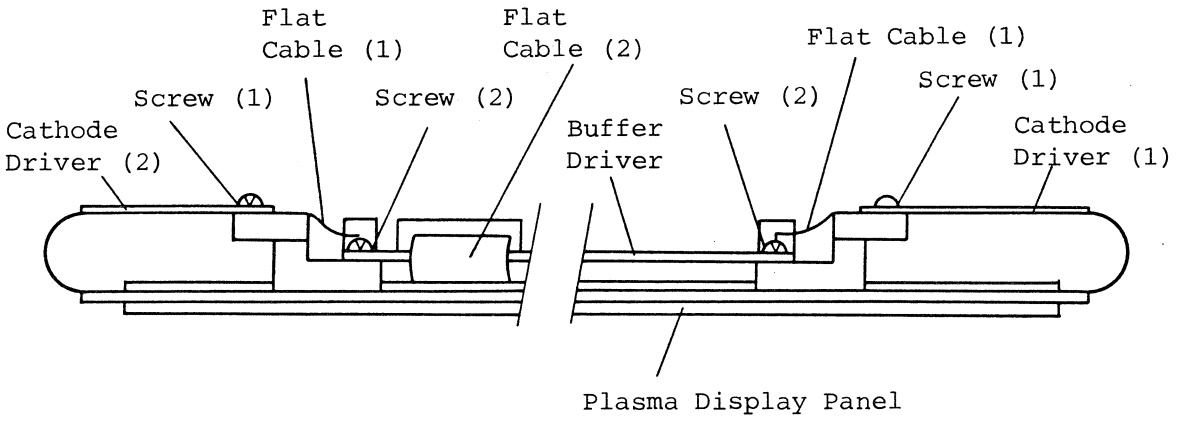
(a) Remove screws (2) and float the buffer driver.

(b) Disconnect the flat cables (1) and (2) from the buffer driver connector. This gives the configuration in the developed drawing on the attached sheet. See drawing on attached sheet for detail.

Installation Procedure

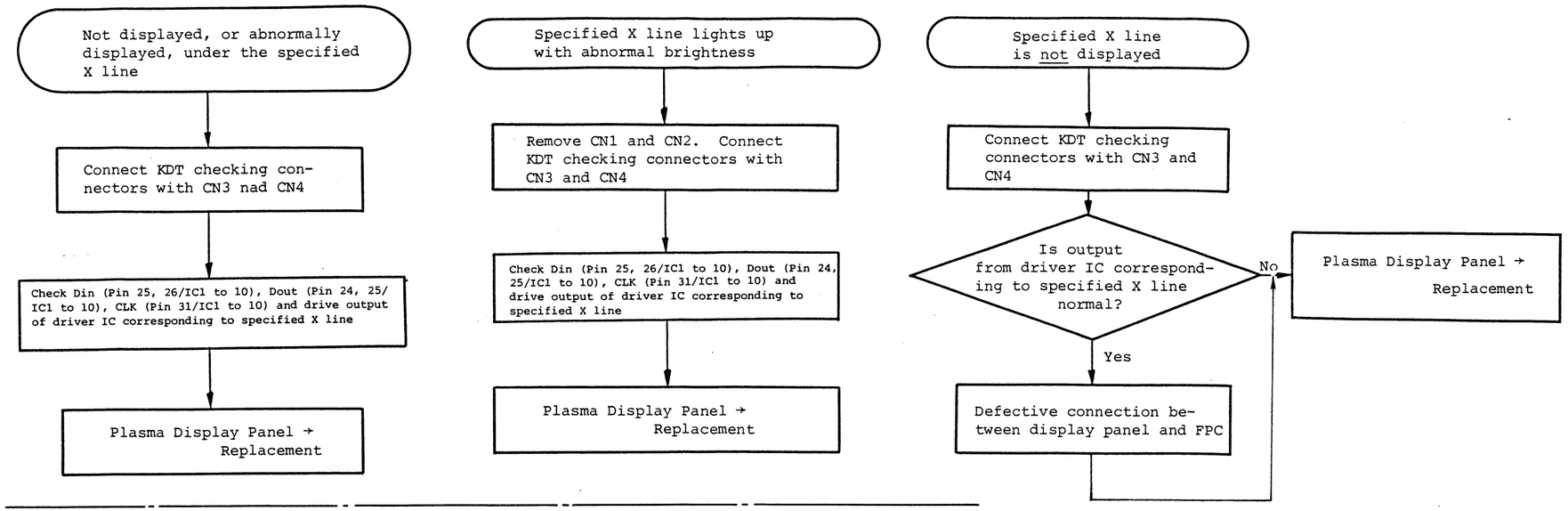
(a) Insert the flat cables (2) into the specified connector of the buffer driver.

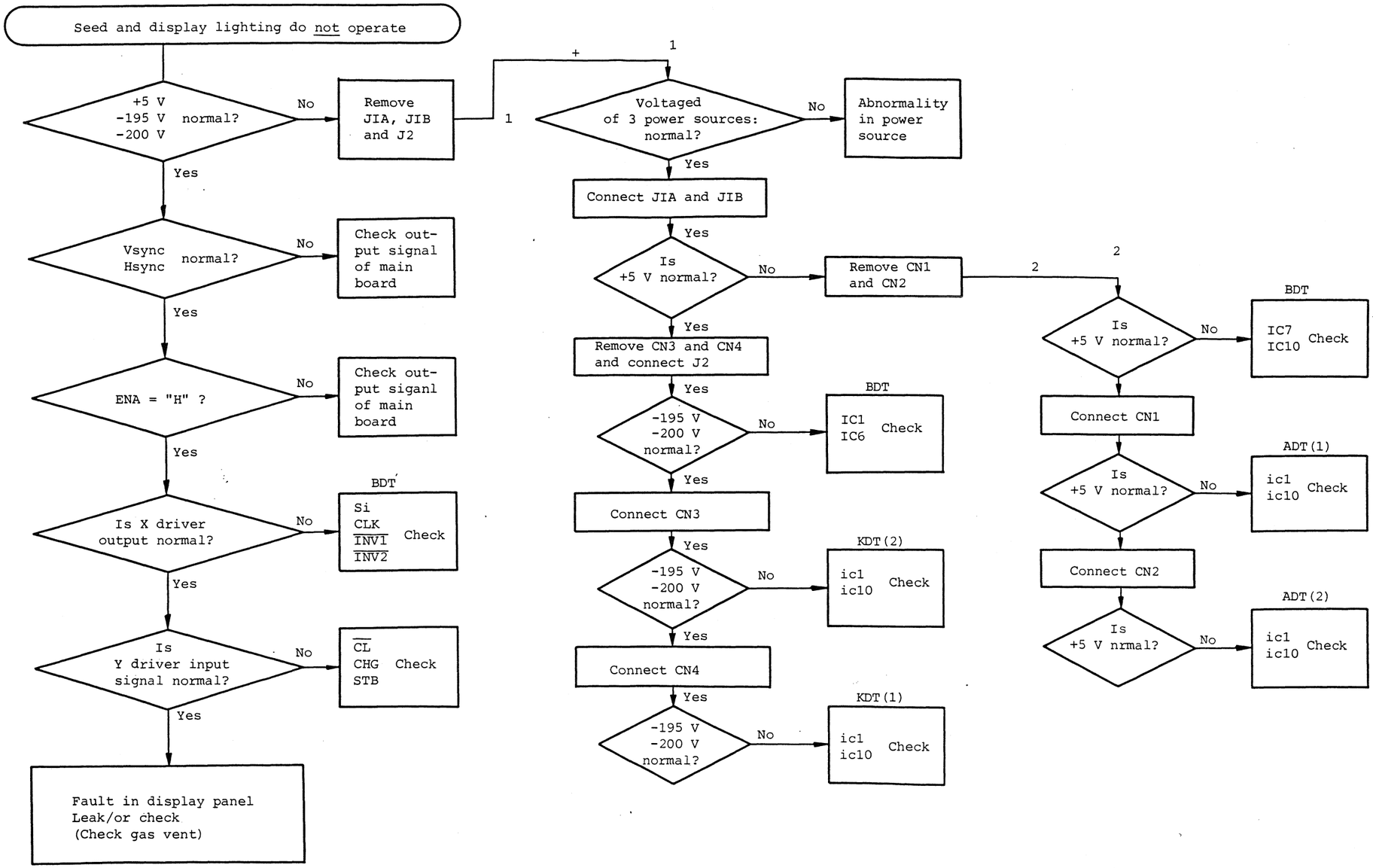
(b) Fasten the buffer driver with screw (2).



Note: Do not remove screws (1).

Figure 5-7


Not displayed, or abnormally displayed, under the specified X line
Connect KDT checking connectors with CN3 nad CN4
Check Din (Pin 25, 26/IC1 to 10), Dout (Pin 24, 25/IC1 to 10), CLK (Pin 31/IC1 to 10) and drive output of driver IC corresponding to specified X line
Plasma Display Panel → Replacement
Specified X line lights up with abnormal brightness
Remove CN1 and CN2. Connect KDT checking connectors with CN3 and CN4
Check Din (Pin 25, 26/IC1 to 10), Dout (Pin 24, 25/IC1 to 10), CLK (Pin 31/IC1 to 10) and drive output of driver IC corresponding to specified X line
Plasma Display Panel → Replacement
Specified X line is not displayed
Connect KDT checking connectors with CN3 and CN4
Is output from driver IC corresponding to specified X line normal?
No
Plasma Display Panel → Replacement
Yes
Defective connection between display panel and FPC
Unstable display, or no display, on left side of specified Y line
Alternately remove CN1 and CN2 and ascertain whether fault is on ADT(1) or on ADT(2) side
Check Din (Pin 25, 26/IC1 to 10), Dout (Pin 24, 25/IC1 to 10), CLK (Pin 31/IC1 to 10) and drive output of driver IC corresponding to specified Y line
Plasma Display Panel → Repalcement
Specified Y line is not displayed
Alternately remove CN1 and CN2 and ascertain whether fault is on ADT(1) or on ADT(2) side
Shunt the drive output of the driver IC corresponding to the specified Y line with the other drive output, and ascertain whether the drive output is normal
OK?
No
Plasma Display Panel → Replacement
Yes
Faulty connection of resistance module or faulty connection between display panel and FPC
Plasma Display Panel → Replacement


Seed and display lighting do not operate
+5 V
-195 V
-200 V
normal?
No
Remove JIA, JIB and J2
Yes
Vsync
Hsync
normal?
No
Check output signal of main board
Yes
ENA = "H" ?
No
Check output siganl of main board
Yes
Is X driver output normal?
No
BDT
Si
CLK
INV1
INV2
Check
Yes
Is Y driver input signal normal?
No
CL
CHG
STB
Check
Yes
Fault in display panel
Leak/or check
(Check gas vent)
+
1
1
Voltaged of 3 power sources: normal?
No
Abnormality in power source
Yes
Connect JIA and JIB
Yes
Is +5 V normal?
No
Remove CN1 and CN2
2
Yes
Remove CN3 and CN4 and connect J2
Yes
-195 V
-200 V
normal?
No
BDT
IC1
IC6
Check
Yes
Connect CN3
Yes
-195 V
-200 V
normal?
No
KDT(2)
ic1
ic10
Check
Yes
Connect CN4
Yes
-195 V
-200 V
normal?
No
KDT(1)
ic1
ic10
Check
2
Is +5 V normal?
No
BDT
IC7
IC10
Check
Connect CN1
Is +5 V normal?
No
ADT(1)
ic1
ic10
Check
Connect CN2
Is +5 V nrmal?
No
ADT(2)
ic1
ic10
Check

7. REPLACEMENT PARTS LIST AND DRAWING

7.1 Exploded View

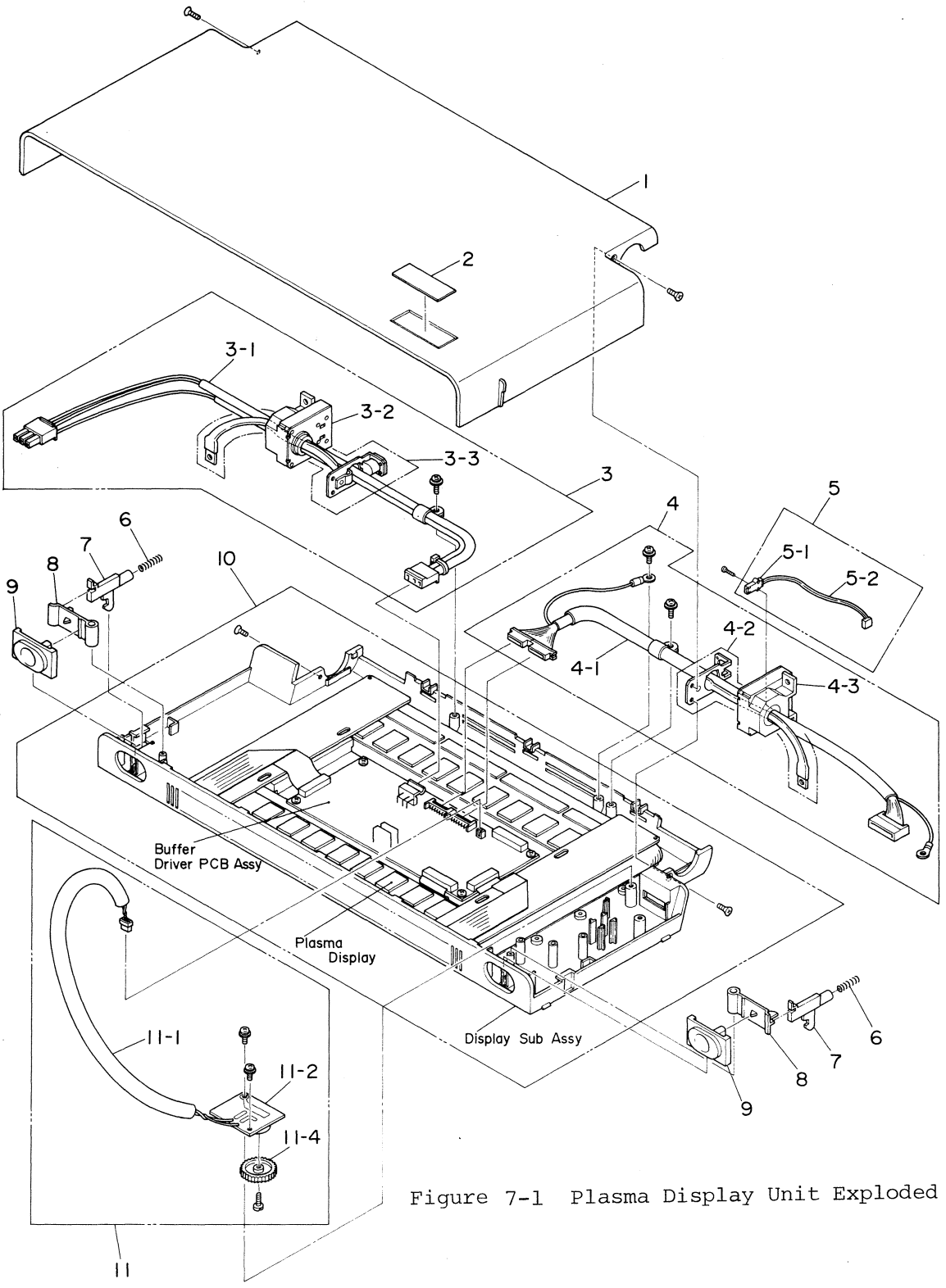


Figure 7-1 Plasma Display Unit Exploded View

REPLACEMENT PARTS LIST (Plasma Display)

NOTE:
- **When ordering replacement parts indicate Part No. and Name of Parts.**
- **⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.**

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
1		YJJ5E08470D1	Outside Cover	1	
2		YJJ7Q11810B4	Brand Badge	1	
3					
3-1		YJJDK02570B4	Plasma DC Cable	1	
3-2		YJJUX03340B3	Softner (L)	1	
3-3		YJJUX02850B4	ARM (L)	1	
4					
4-1		YJJDK02560B3	Plasma Signal Cable	1	
4-2		YJJUX02840B4	ARM (R)	1	
4-3		YJJUX03330B3	Softner (R)	1	
5		YJJ4035180A4	Detector Cable	1	
5-1		YJMQS-1AU	μ Switch	1	
5-2		YJJDK02590B4	Detector Cable	1	
6		YJJ4J01280B4	Spring	2	
7		YJJ6D08500B3	Plasma Hook	2	
8		YJJ4R01230B4	Hook Cover	2	
9		YJJ5R08510B4	Look Button	2	
10		YJJ3005950A4	Plasma Display Sub Ass'y	1	
11		YJJ4035030A4	Bright Control Ass'y	1	
11-1		YJJDK03030B4	Bright Cable	1	
11-2		YJJPK03500B4	P.C.B (Only)	1	
11-3		EVLEAAT12B54	Variable Resistor	1	
11-4		YJJ5R08650B4	Knob	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks

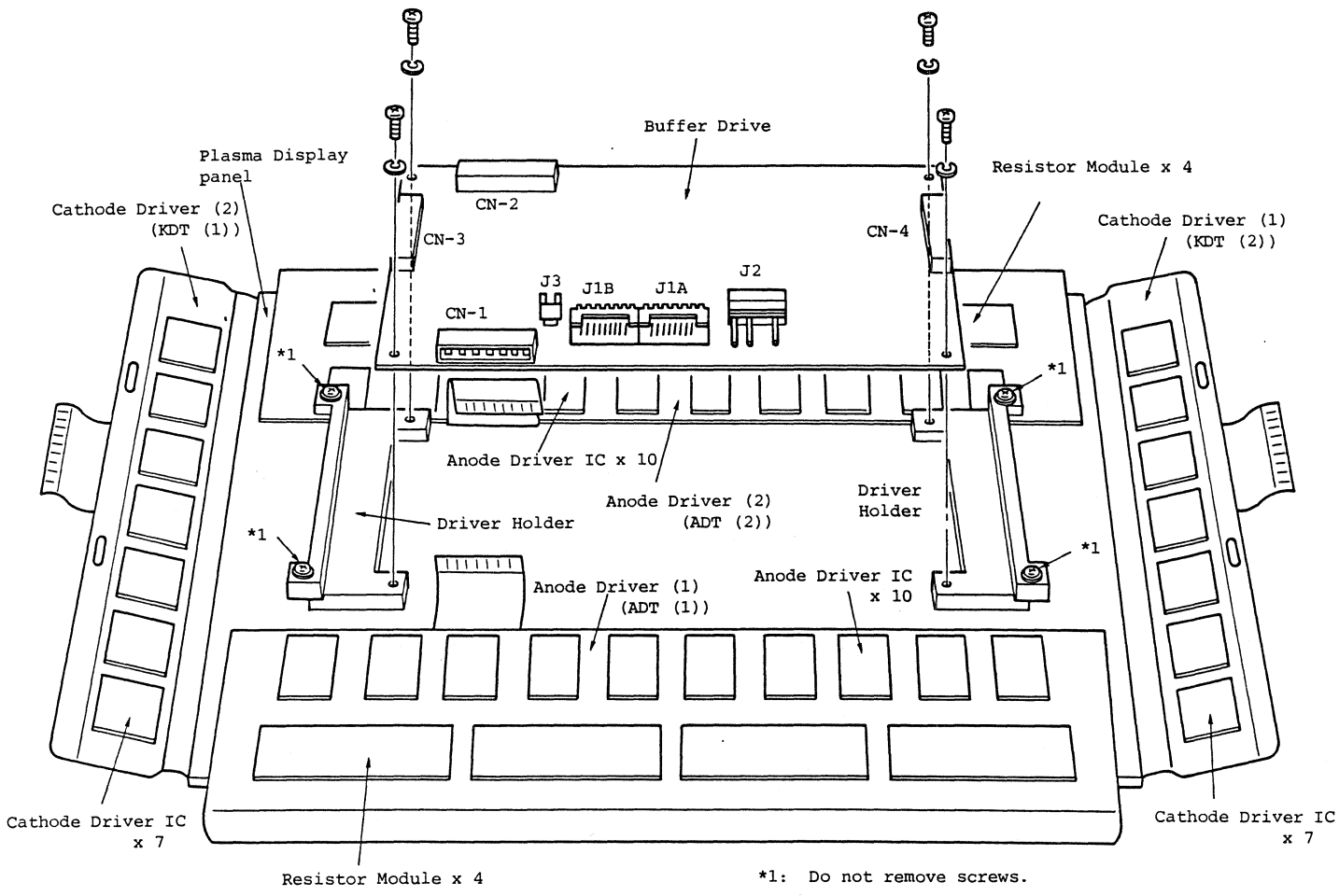


Figure 7-2 Plasma Display Panel Rear Side

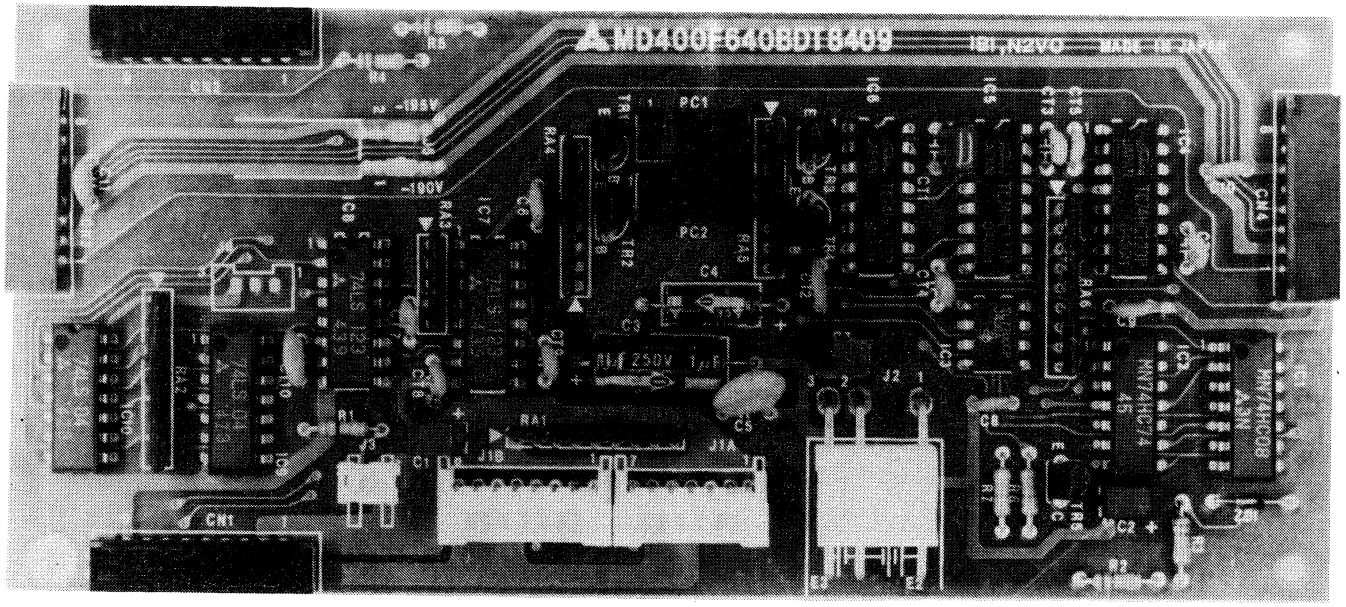
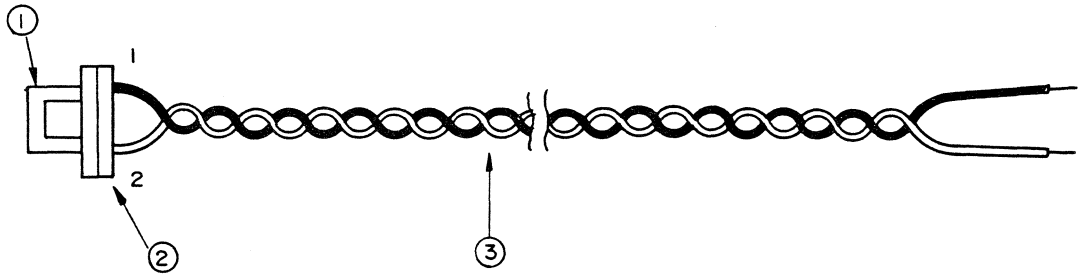


Figure 7-3 Buffer Driver Parts Layout

7.3 Connections



CN Pin No.	Wire Color
1	Red
2	Brown

Figure 7-4 Bright Control Cable

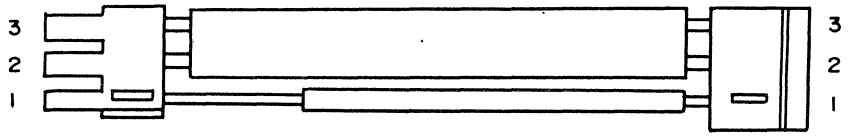
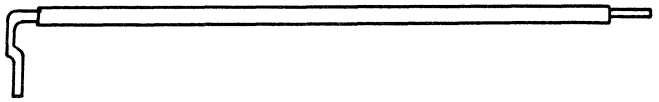
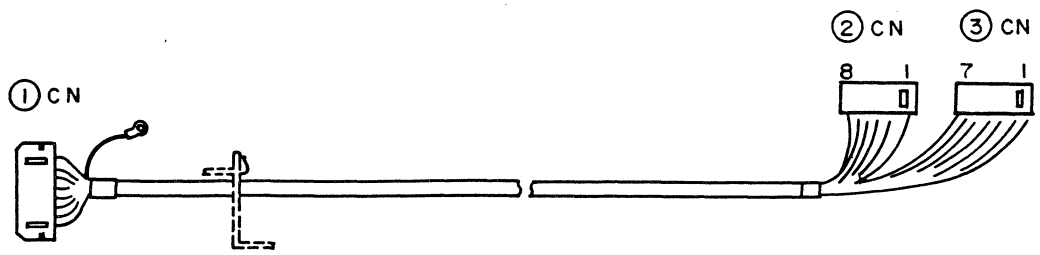


Figure 7-5 Plasma DC Cable



① CN Pin No.	② CN Pin No.	Wire Color	Signal Name
1	1	Red	+5 V
2	2	Yellow	-200 V
3	3	Brown	-195 V

Figure 7-6 Plasma FG Cable



Wire Color	① CN Pin No.	② CN Pin No.	③ CN Pin No.	Signal Name
Orange & Black (Spiral)	1		3	VSync
Read & Black (Spiral)	2		4	GND
Brown & Black (Spiral)	3		5	HSync
Black	4		6	GND
Gray	5	1		DATA0
Purple	6	2		DATA1
Blue	7	3		DATA2
Green	8	4		DATA3
Yellow	9	5		GND
Red	10	7		GND
White	11		7	SFTCLK
	12	NC	NC	NC
White & Black (Spiral)	13		1	+5 V
Yellow & Black (Spiral)	14		2	+5 V
Brown	15	8		GND
Orange	16	6		ENA

Figure 7-7 Signal Cable

REPLACEMENT PARTS LIST (Buffer Driver P.W.B.)

NOTE:
- **When ordering replacement parts indicate Part No. and Name of Parts.**
- **⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.**

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
*		MD400F640PD2	Buffer Driver P.W.B. Ass'y	1	
TR1-4		2SC828-R	Transistor	4	
IC9. 10		DN74LS04	I. C.	2	
IC7. 8		DN74LS123	I. C.	2	
C5		ECCD2H222ME	C.Capacitor	1	
C4		ECEB1EG100S	E.Capacitor	1	
C3		ECEB2EG2R2S	E. Capacitor	1	
C6.8-11		ECKD1H103ZF	C. Capacitor	5	
CT2.10		ECKF1H332KB	C. Capacitor	2	
CT3-9		ECKF1H471JT	C. Capacitor	8	
CT1		ECQV1H104JZ	F. Capacitor	1	
C1.2.7		ECSZ16HS10	Tantal Capacitor	3	
J3		EMCS0251ML	Connector 2P	1	
J1A		EMCS0751ML	Connector 7P	1	
J1B		EMCS0851ML	Connector 8P	1	
R1		ERD25TJ103	C. Resistor	1	
R4. 5		ERD25TJ224	C. Resistor	2	
R2. 3		ERD25TJ273	C. Resistor	2	
R6. 7		ERD25TJ472	C. Resistor	2	
RA3		EXBD84371S	Resistor Array	1	
RA4. 5		EXBD86372S	Resistor Array	2	
RA6		EXBD88373G	Resistor Array	1	
RA1		EXBP88103K	Resistor Array	1	
RA2		EXBP88472K	Resistor Array	1	
IC1		MN74HC08	I.C.	1	
IC4.5.6		MN74HC123	I.C	3	
IC2		MN74HC74	I.C.	1	
PC1. 2		ON3105	Isolator	2	
ZD1		RD100EB	Zener Diode	1	
IC3		TL 7700CP	I. C.	1	
J2		YJ5274-04A	Connector	1	
CN3. 4		YJHBLB8R-1J	Connector 8P	2	
CN1. 2		YJHBLB9R-1J	Connector 9P	2	

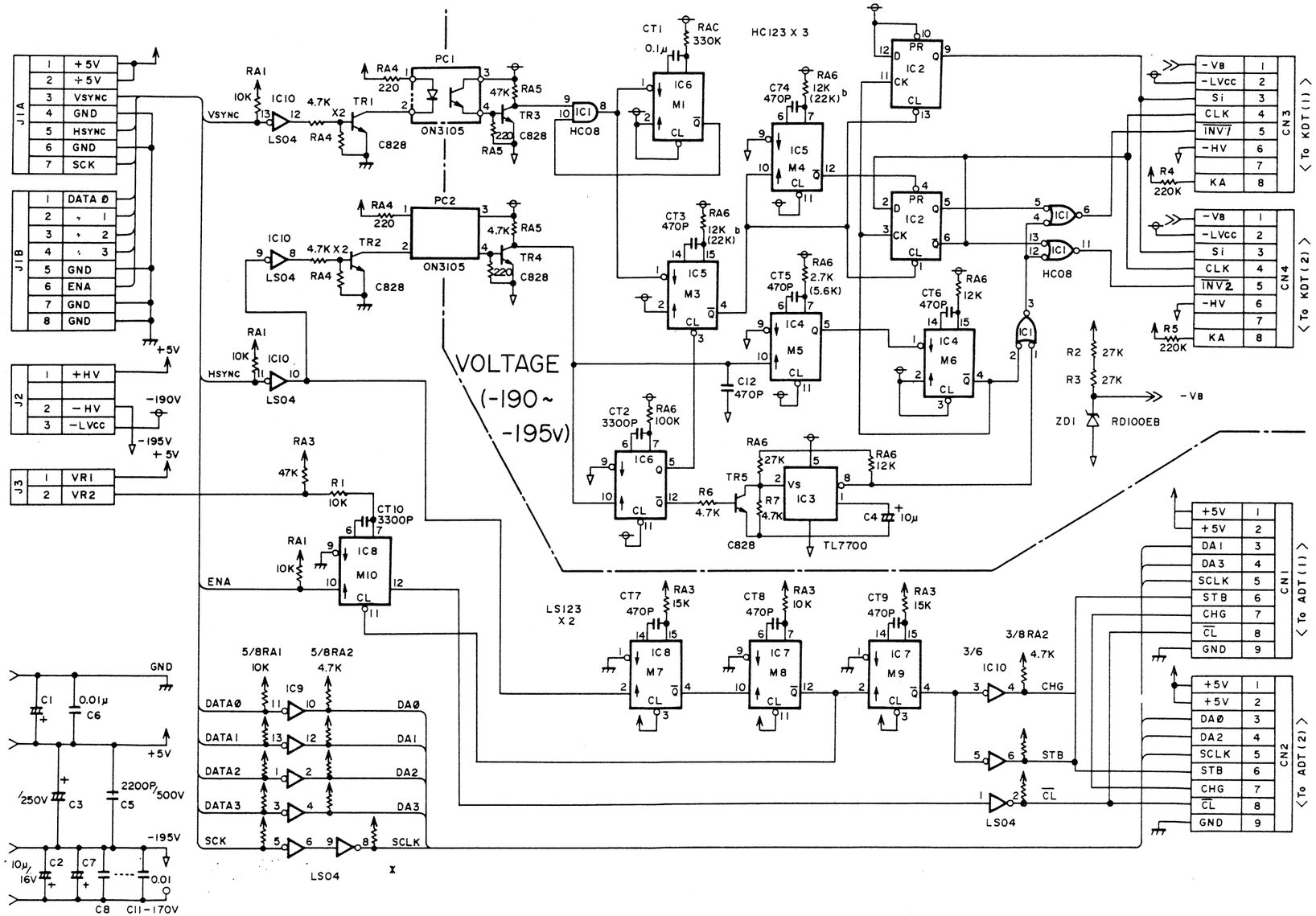
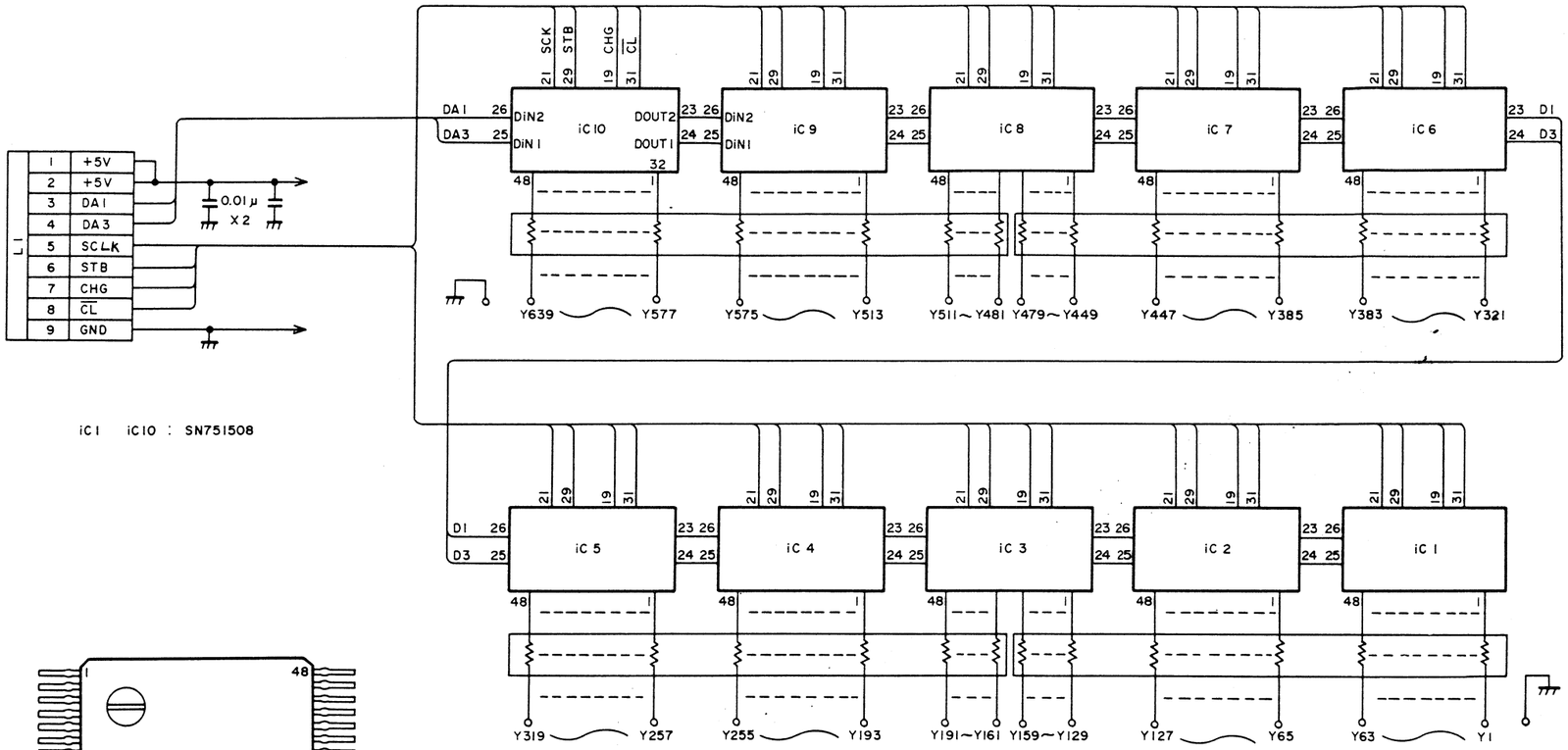


Figure 7-8 Buffer Driver Circuit Diagram



iC1 iC10 : SN751508

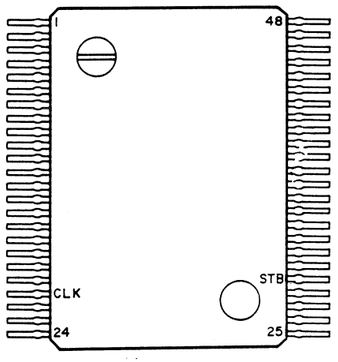
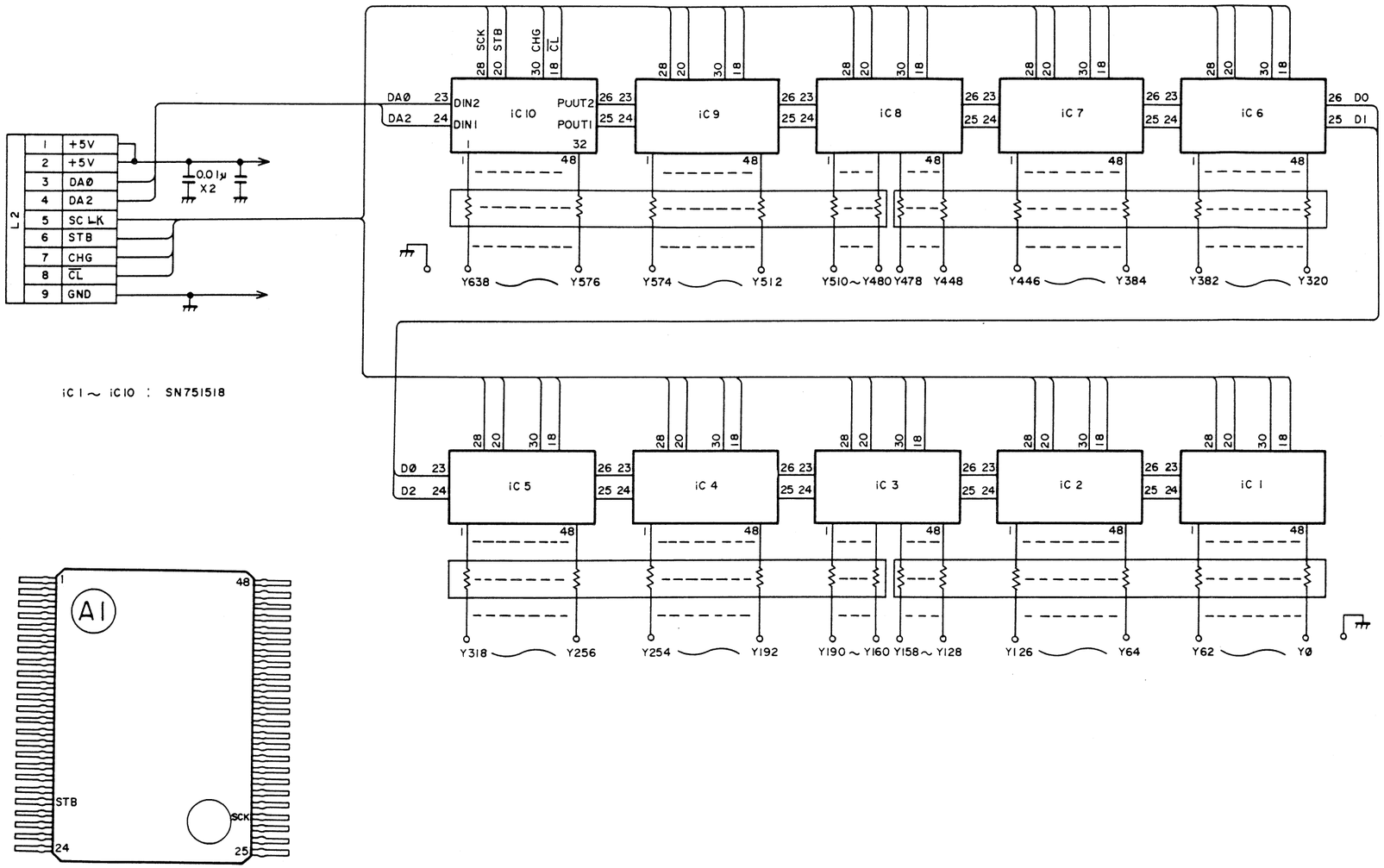


Figure 7-9 Anode Drive Circuit Diagram (ADT(1))



iC 1 ~ iC 10 : SN751518

Figure 7-10 Anode Drive Circuit Diagram (ADT(2))

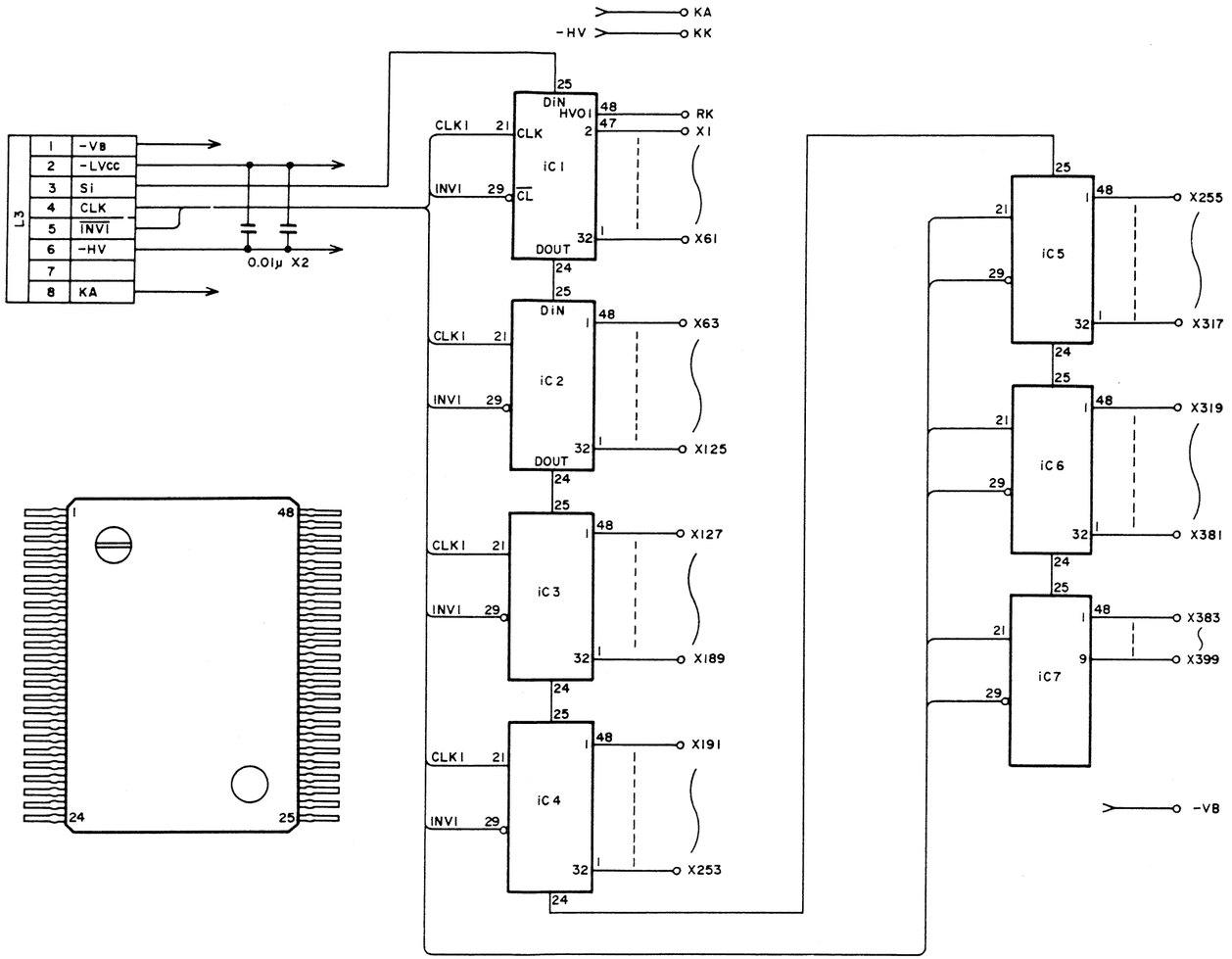


Figure 7-11 Cathode Drive Circuit Diagram (KDT(1))

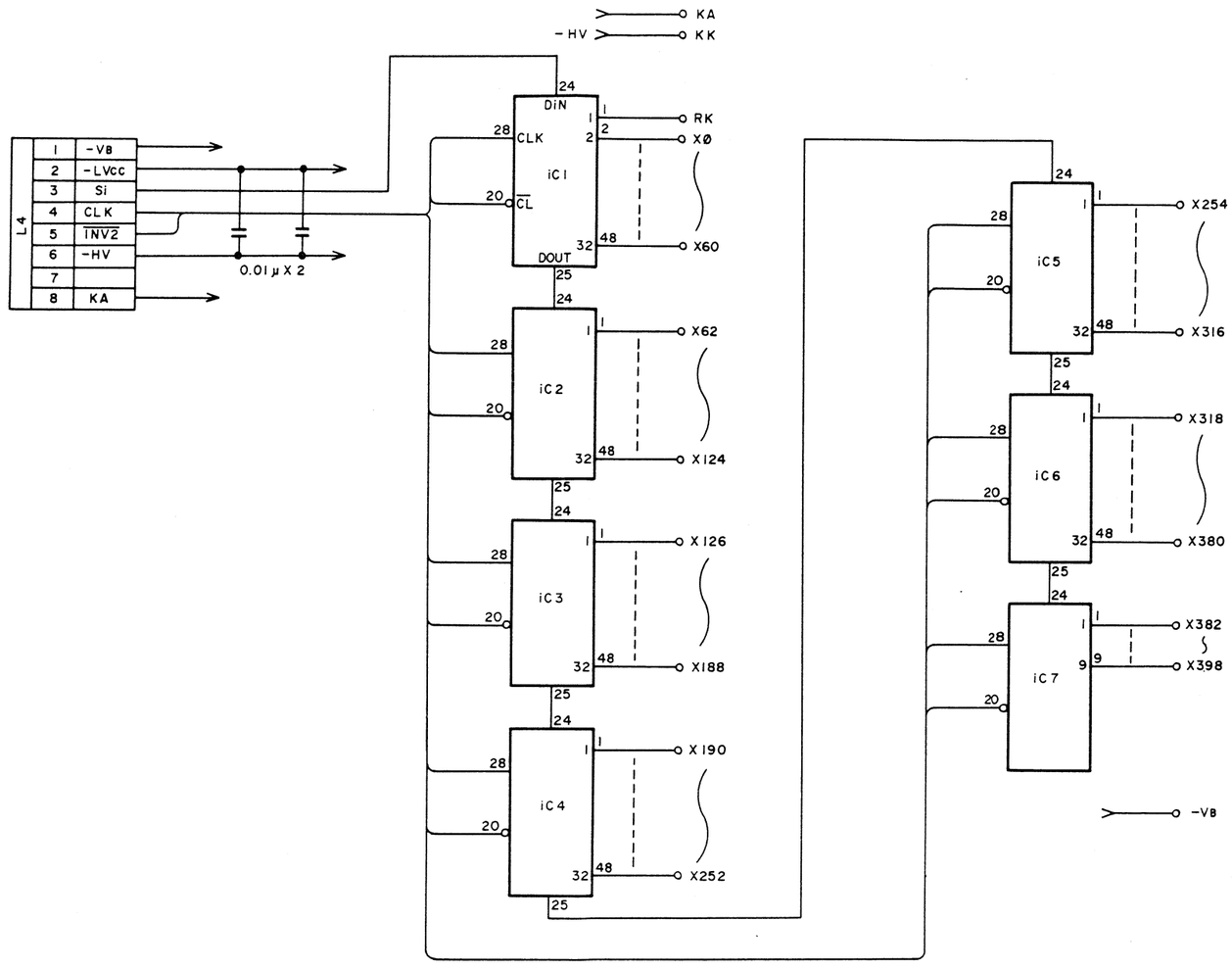


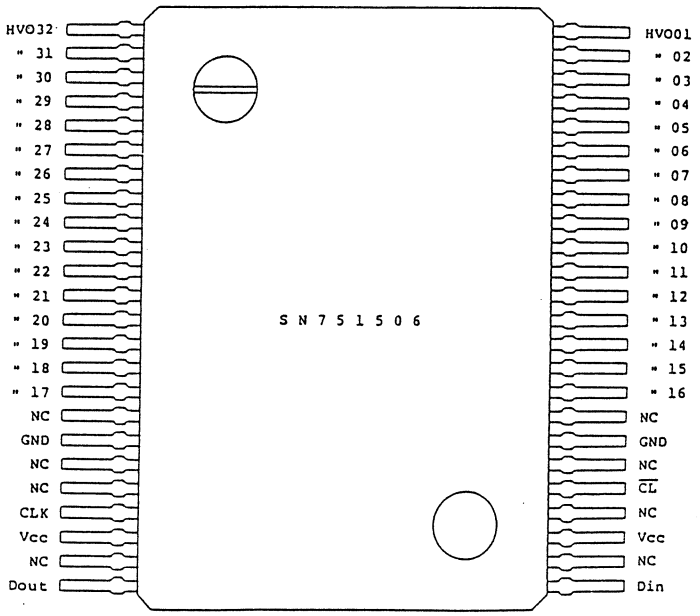
Figure 7-12 Cathode Drive Circuit Diagram (KDT(2))

APPENDIX

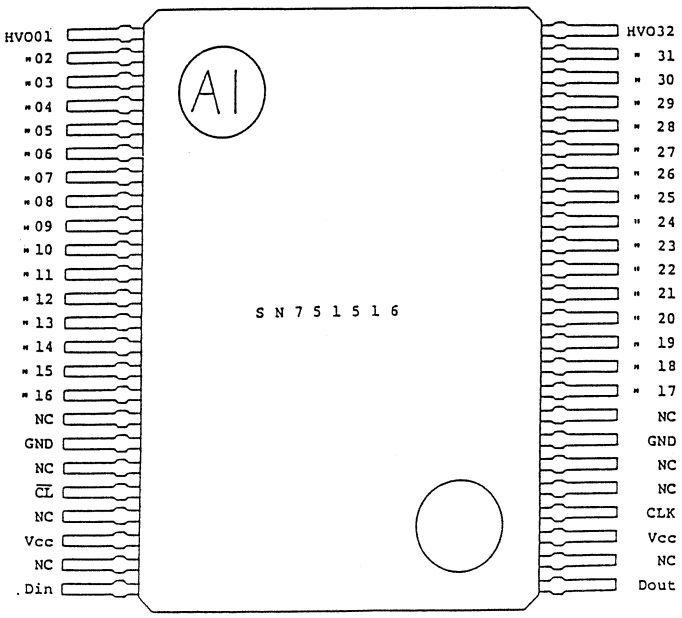
A. IC/LSI CATALOG

A.1 IC/LSI etc. Pin Assignment

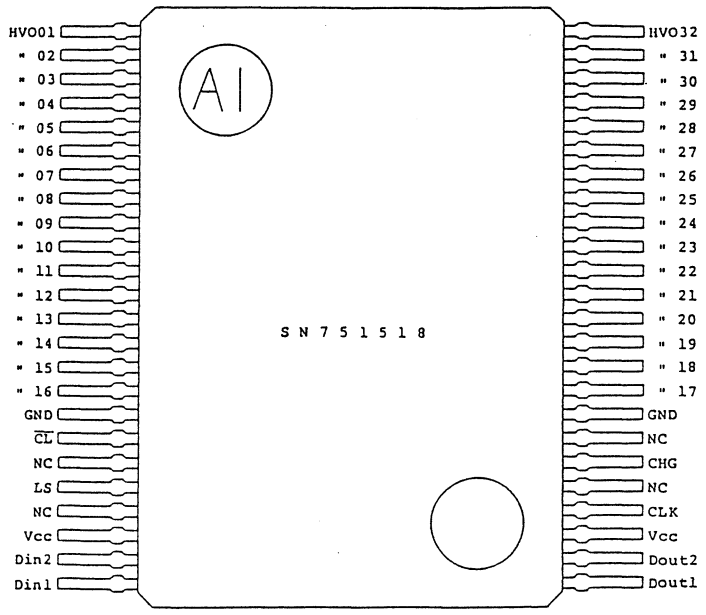
(a) SN751506 Pin Assignment



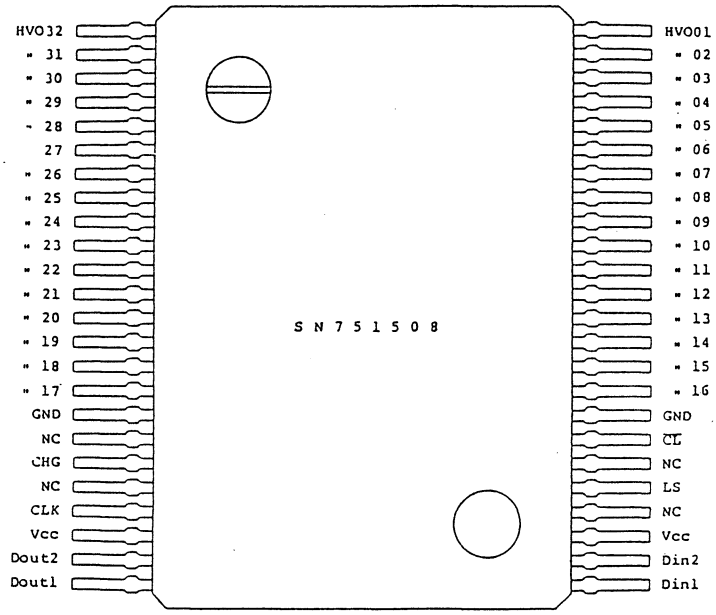
(b) SN751516 Pin Assignment



(c) SN751518 Pin Assignment



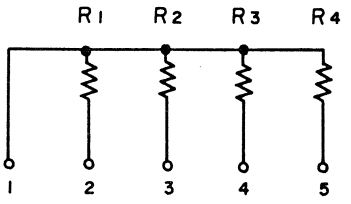
(d) SN751508 Pin Assignment



A.2 IC Specification

(a) Product No.: EXB-D84371S

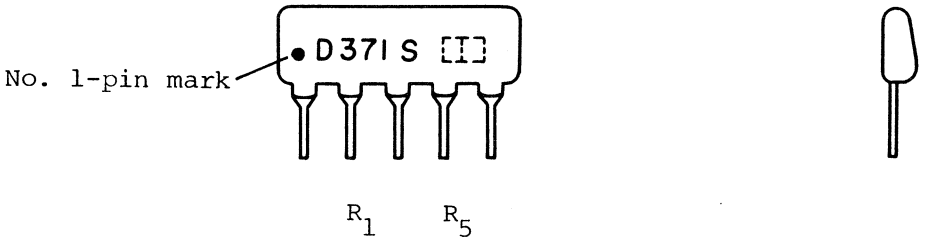
(b) Circuit Configuration



(c) Constants and Ratings

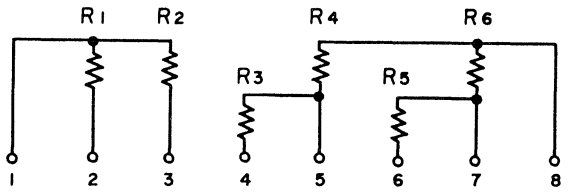
Element No.	R_1	R_2	R_3	R_4
Nominal resistance	47 kΩ	15 kΩ	15 kΩ	10 kΩ
Resistance tolerance	±10%	±2%		
Rated power for the element	1/8 W			

(d) Shape, Dimensions, and Marking



(a) Product No.: EXB-D86372S

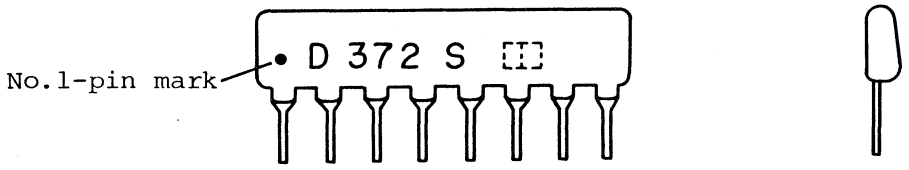
(b) Circuit Configuration



(c) Constants and Ratings

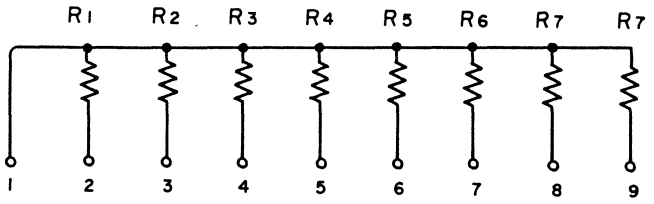
Element No.	R_1	R_2	R_3	R_4	R_5	R_6
Nominal resistance	220 Ω	220 Ω	4.7 kΩ	4.7 kΩ	4.7 kΩ	4.7 kΩ
Resistance tolerance	±5%		±10%			
Rated power for the element	1/8 W					

(d) Shape, Dimensions, and Marking



(a) Product No.: EXB-D88373G

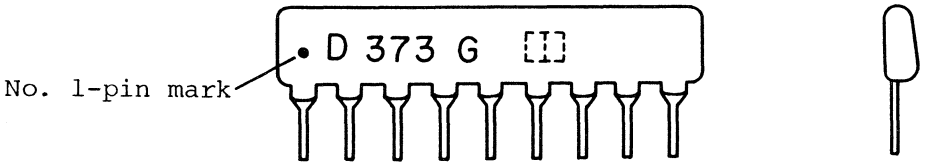
(b) Circuit Configuration



(c) Constants and Ratings

Element No.	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8
Nominal resistance	330 kΩ	100 kΩ	12 kΩ	12 kΩ	12 kΩ	12 kΩ	27 kΩ	2.7 kΩ
Resistance tolerance	±2%							
Rated power for the element	1/8 W							

(d) Shape, Dimensions, and Marking



ORDER NO. DATA 85012
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Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

IV. KEYBOARD

1. SPECIFICATIONS

Number of keys	84
Dimensions	430 (w) x 28 (h) x 155 (d) mm
Stroke	4 mm ±0.5 mm
Key Pitch	19.05 mm
Interlock	N key Rollover
Buffer Size	16 bytes
Detachable	Yes
National Versions	ASCII, English, Swedish/Finnish, French, German
Controller	μPD8048C One Chip Microprocessor

Connector Pin Assignment

Table 1-1 Pin Assignment

Pin No.	Signal Name	Signal Type
1	KBDATA	INPUT/OUTPUT
2	KBCLK	INPUT/OUTPUT
3	HARD RESET	INPUT
4	GND	POWER
5	+5 V	POWER
6	FG	Shared with the GND line

2. LAYOUT AND KEYBOARD MARKINGS

The keyboard consists of a 16-key numeric keypad 10 function keys, and a 58-key typewriter. The 16-key numeric keypad is standard for all versions of the keyboard.

**** Figure 2-1 ASCII (S)

**** Figure 2-2 English

**** Figure 2-3 Swedish/Finnish

**** Figure 2-4 French

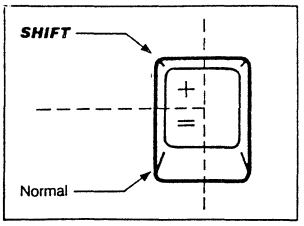
**** Figure 2-5 German

2.1 ASCII Version

For keys with two different characters on the keytop, refer to the example below:

=: Press this key alone.

+: Press this key together with the SHIFT key.



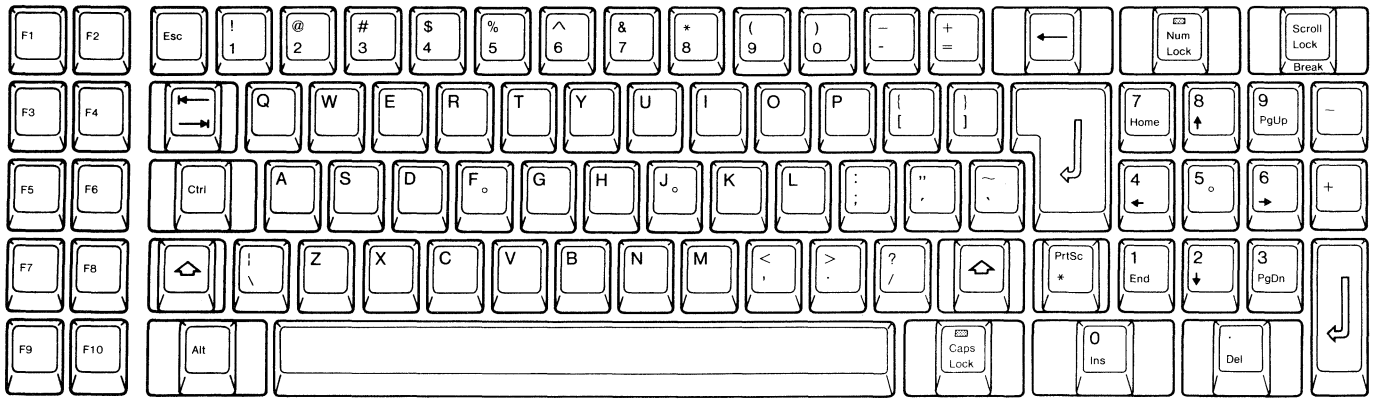


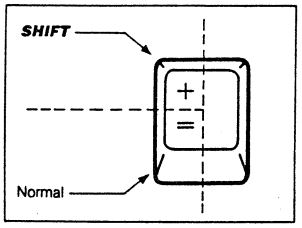
Figure 2-1 ASCII Version

2.2 English Version

For keys with two different characters on the keytop, refer to the example below:

=: Press this key alone.

+: Press this key together with the SHIFT key.



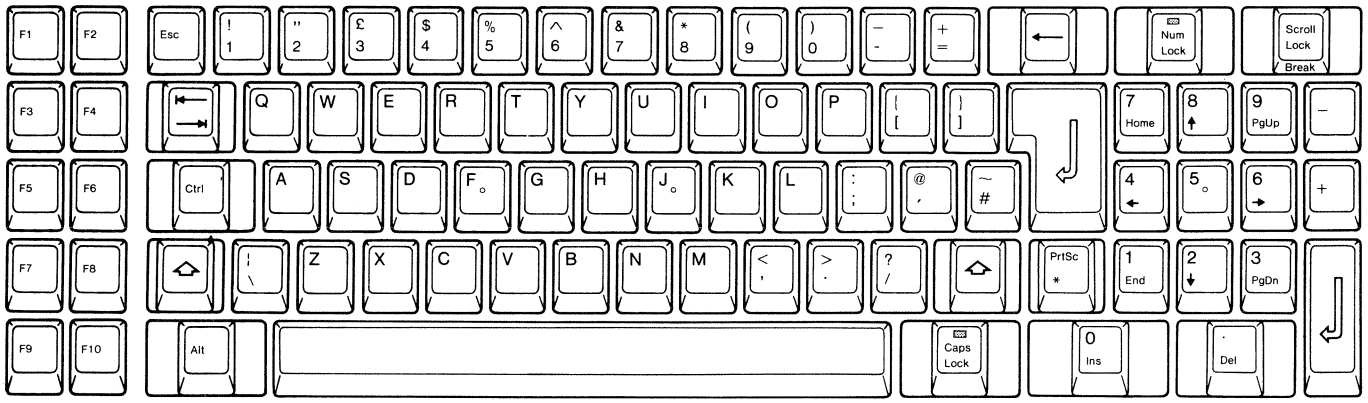
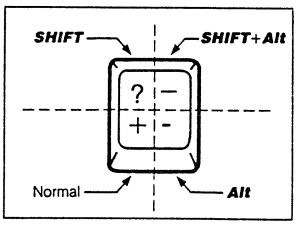


Figure 2-2 English Version

2.3 Swedish/Finnish Version

For keys that have three or four different characters on the keytop, refer to the example below:

+: Press this key alone.
?: Press this key together with the SHIFT key.
-: Press this key together with the Alt key.
_: Press this key together with the SHIFT and Alt keys.



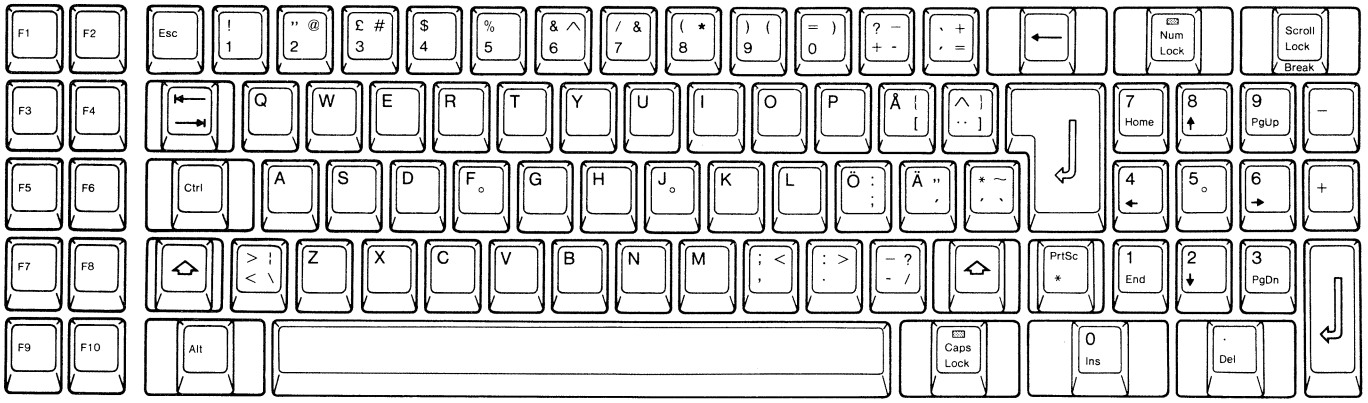
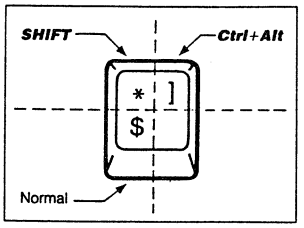


Figure 2-3 Swedish/Finnish Version

2.4 French Version

For keys that have three different characters on the keytop, refer to the example below:



$: Press this key alone.
*: Press this key together with the SHIFT key.
]: Press this key together with the Ctrl and Alt keys.

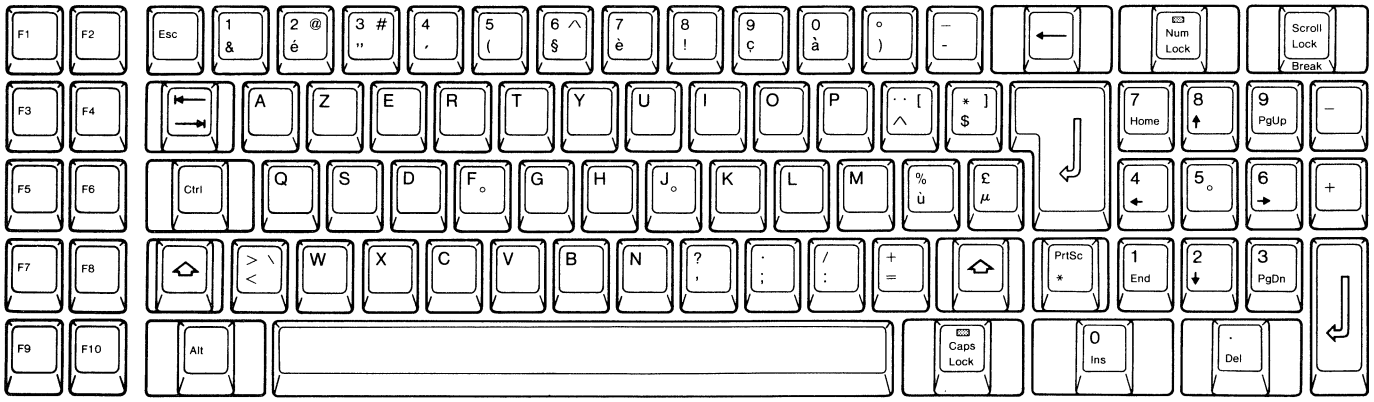
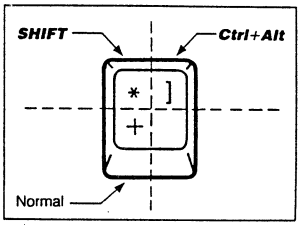


Figure 2-4 French Version

2.5 German Version

For keys that have three different characters on the keytop, refer to the example below:



+: Press this key alone.
*: Press this key together with the SHIFT key.
]: Press this key together with Ctrl and Alt keys.

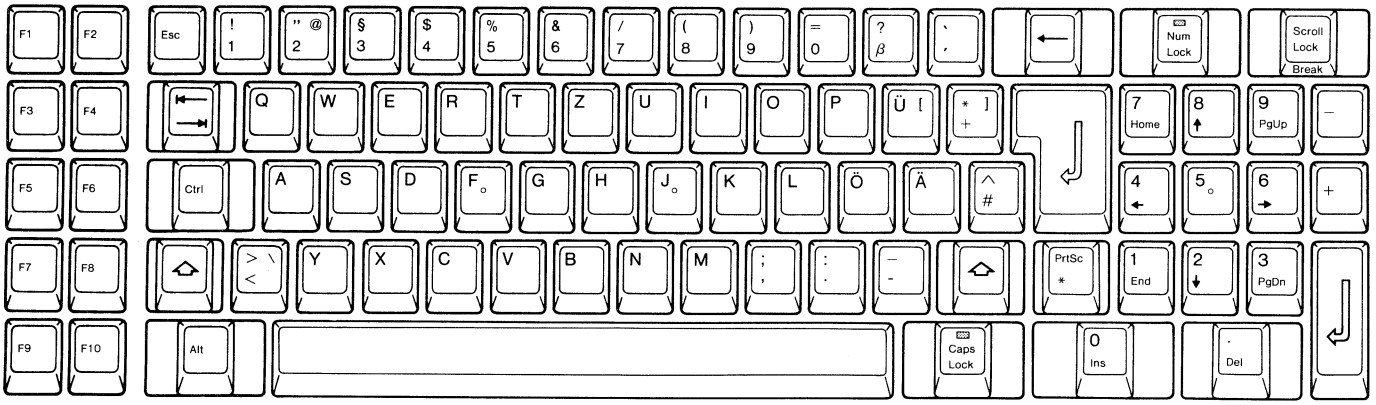


Figure 2-5 German Version

3. BLOCK DIAGRAM

Figure 3-1 shows a block diagram. The operation at each stage is portrayed by waveform photographs and circuit diagrams.

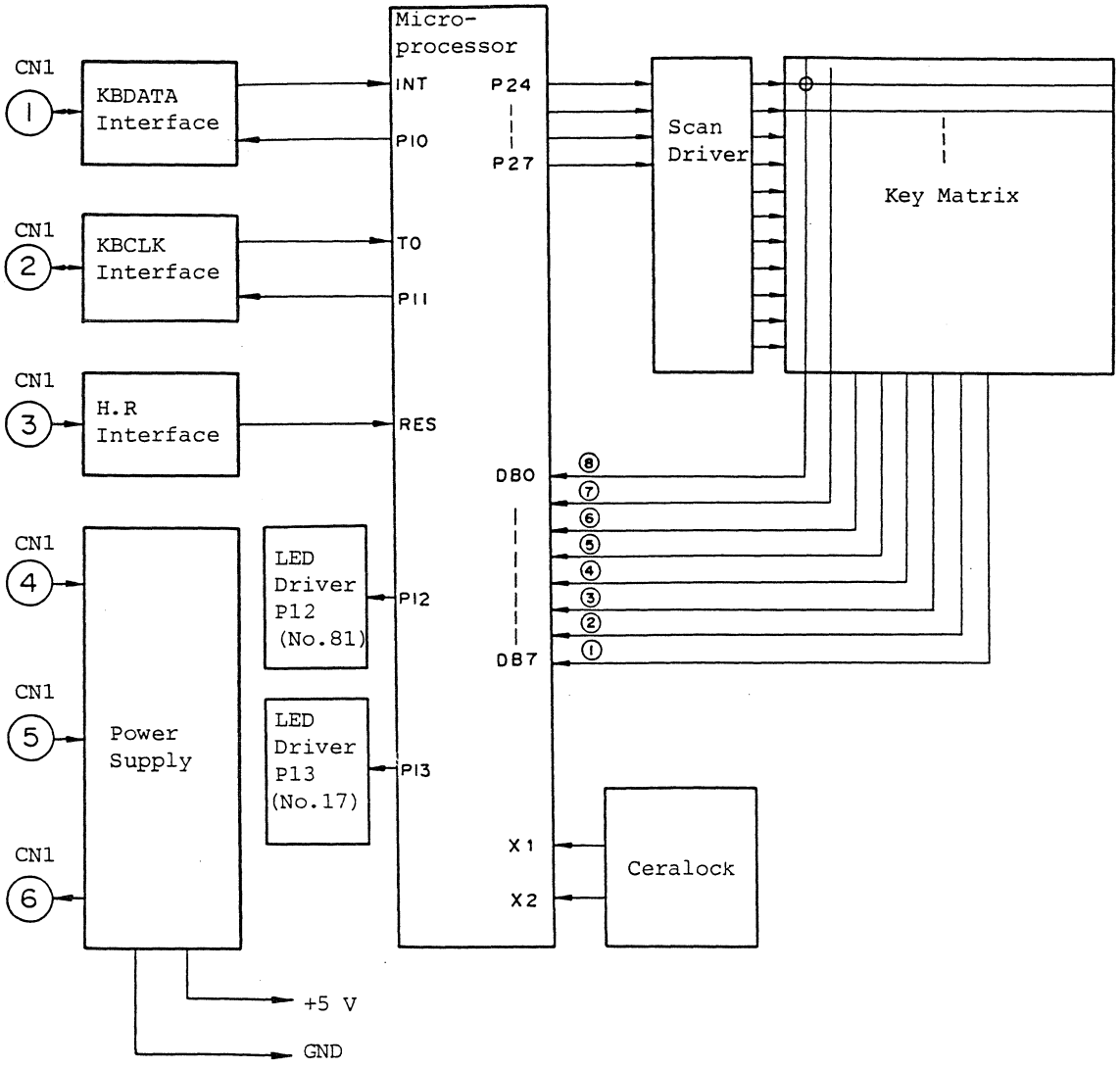


Figure 3-1 Block Diagram

4. CIRCUIT DESCRIPTION

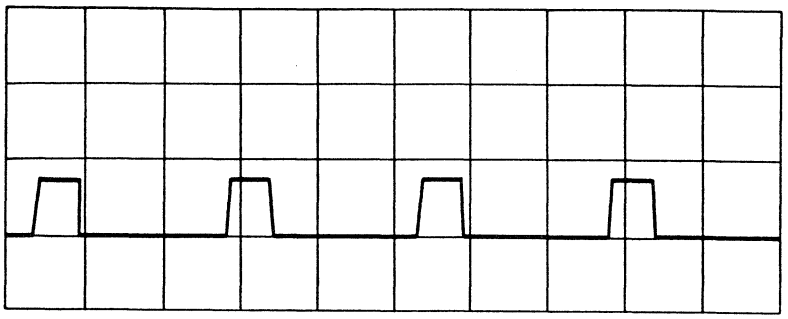
4.1 Power Supply

CN1 pin 4 is the unit circuit ground and the power supply ground. CN1 pin 5 is the +5 V power supply which supplies +5 VDC ±0.5% with a maximum of 200 mA.

FG is connected to the keyboard metal chassis to protect it from electrostatic charges.

4.2 Oscillator

6 MHz, the basic clock frequency cheated by the ceralock, is frequency-divided into a fifteenth. The resulting 400 kHz appears at pin 11 of the microprocessor (Figure 4-16).



Scale on the abscissa:
1 μs/div

Figure 4-1 ALE Waveform

This microprocessor operation can be checked by observing this waveform.

4.3 Data Type and Logic

① KBDATA: Data output signal from the keyboard: Positive logic
BUSY input signal from the system unit: Negative logic

o Data type

ON code: Key data output when key is pressed.

OFF code: Key data output when key is released. The OFF code is (80)(HEX) plus the corresponding key data when the key is pressed.

o Data logic

1) Keyboard output: 1 = High level 0 = Low level

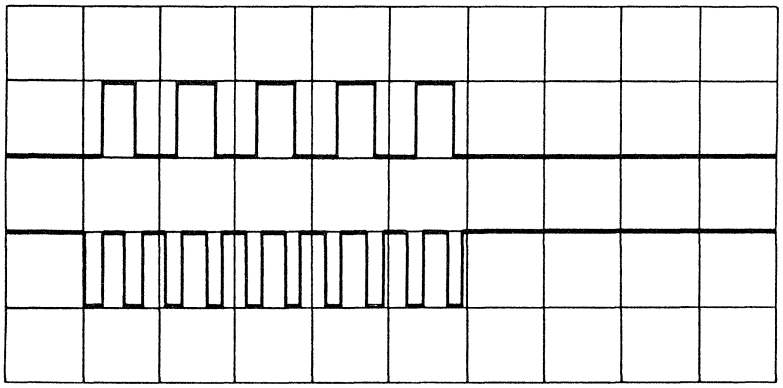
2) Unit output: Unit not-busy = High level
Unit busy = Low level

② $\overline{\text{KBCLK}}$: Clock signal output from the keyboard. Also the self-test signal input from the system unit. Negative logic.

4.4 KBDATA and $\overline{\text{KBCLK}}$ Output Timing

Both signals are bidirectional, and transfer data between the system unit and the keyboard under the following conditions:

(1) When KBDATA = H and $\overline{\text{KBCLK}}$ = H at the system unit:

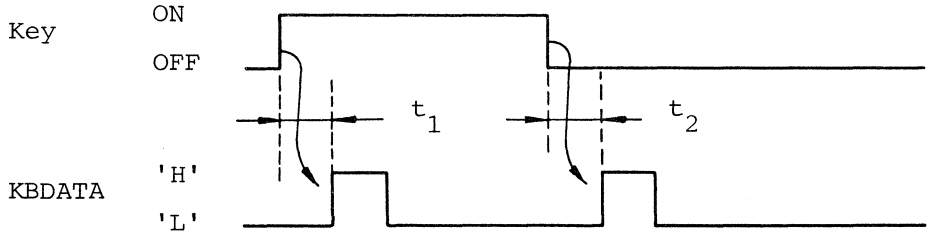


Scale on the abscissa: 0.1 ms/div

Top: KBDATA

Bottom: $\overline{\text{KBCLK}}$

Figure 4-2 KBDATA and $\overline{\text{KBCLK}}$ Outputs



t_1 = 30 ms max

t_2 = 30 ms max

Figure 4-3 KBDATA Output Timing

Figure 4-2 shows a sample output of KBDATA and KBCLK, when KBDATA = H (keyboard output permitted by the system unit) and KBCLK = H (the unit does not request keyboard self test). The KBDATA response to the key operation is shown in Figure 4-3. This output is controlled by microprocessors P10 and P11.

Figure 4-4 shows the timing of $\overline{\text{KBCLK}}$ and KBDATA.

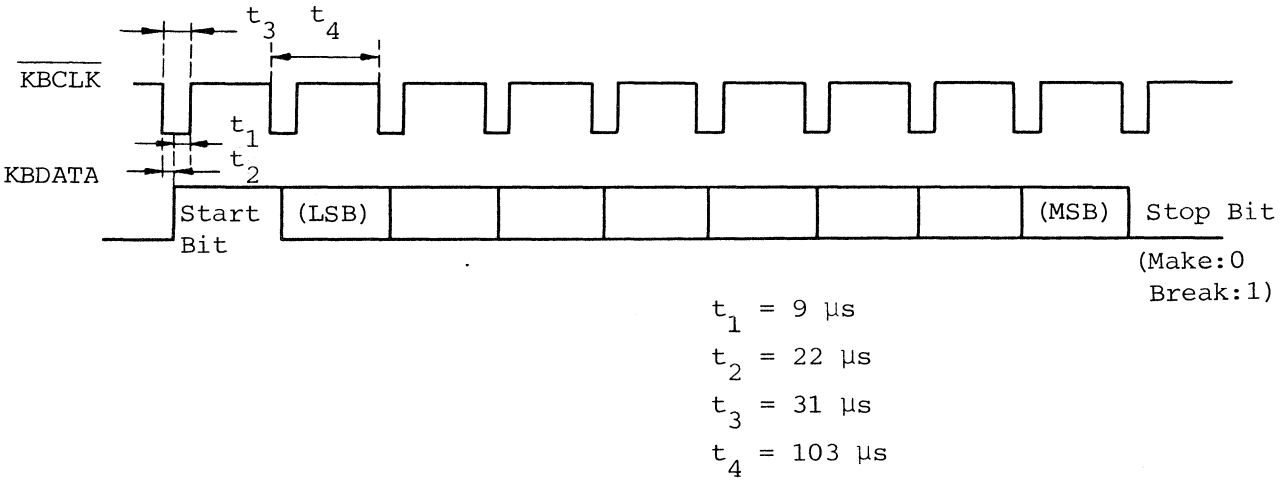


Figure 4-4 Timing of $\overline{\text{KBCLK}}$ and KBDATA

A unit of data from KBDATA consists of a start bit and 8 data bits followed by a stop bit. The 8-bit data is arranged from LSB to MSB.

As Figure 4-5 shows, KBDATA output is inhibited for 6 ms after it has been output.

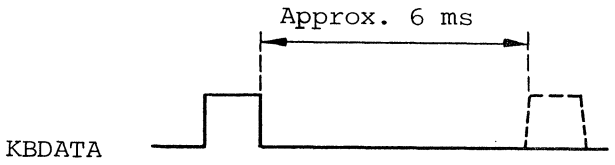


Figure 4-5 KBDATA Output Inhibit

(2) When KBDATA = L and $\overline{\text{KBCLK}}$ = H at the system unit:

When the system unit sets KBDATA to LOW, the keyboard does not output data to KBDATA; it stores the data in the buffer (16 bytes) on a first-in-first-out basis.

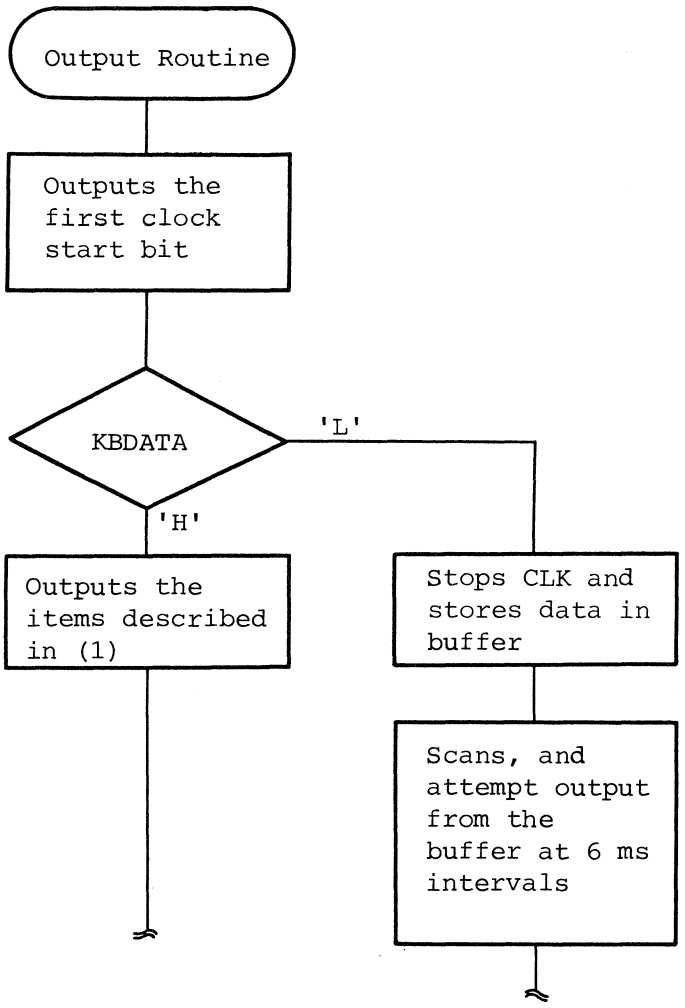


Figure 4-6 Output Condition

When KBDATA goes LOW, the keyboard attempts to output data from the buffer at 6 ms intervals (Figure 4-7).

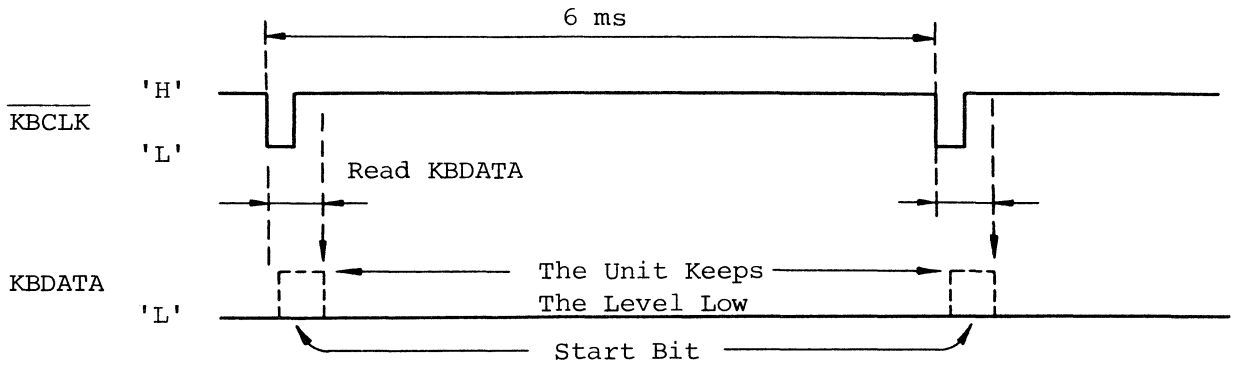


Figure 4-7 Sequence When KBDATA = L and $\overline{\text{KBCLK}}$ = H

When the buffer overflows (FF) HEX Is output at the 17th byte of the buffer.

(3) When KBDATA = H and $\overline{\text{KBCLK}}$ = L at the system unit:

When the system unit holds $\overline{\text{KBCLK}}$ to LOW for 67.5 ms or more, the keyboard performs self test. (See also the section entitled "Self Test.")

4.5 $\overline{\text{HARD RESET}}$: Input Signal to Reset the Keyboard. Negative Logic

The keyboard is reset when $\overline{\text{HARD RESET}}$ is received from the system unit. $\overline{\text{HARD RESET}}$ occurs at the timing shown in Figure 4-8, only after the number 5 +5 V terminal has reached 4.75 V or more.

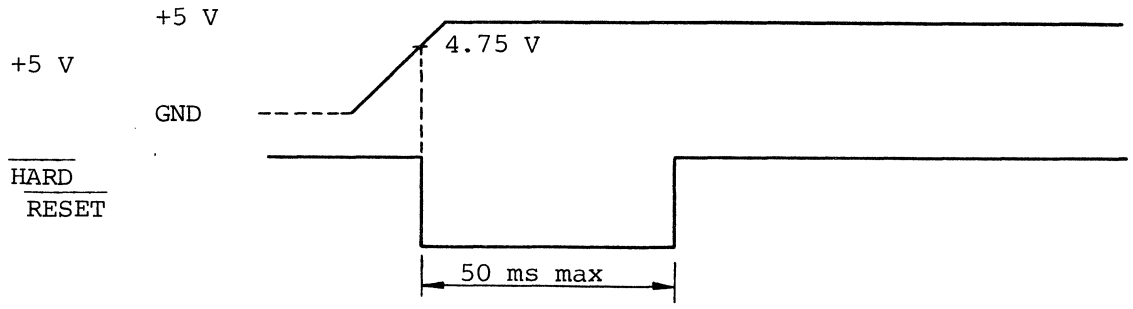
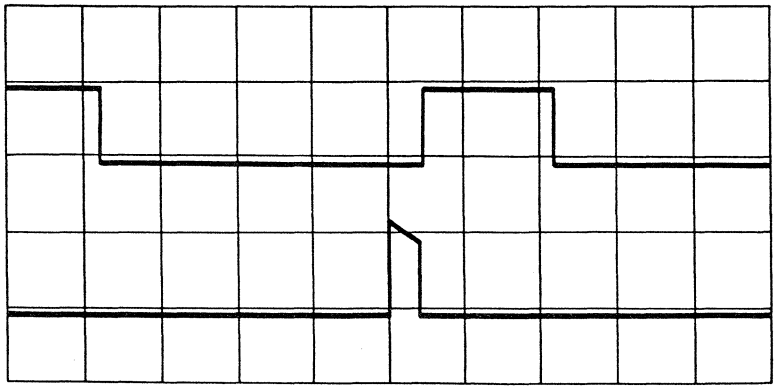


Figure 4-8 HARD RESET

4.6 Scanning

The circuit is a matrix composed of a scan driver and a scan detector (DB0 - DB7 of the microprocessor).

A low-active signal is output to the key matrix to detect which key is depressed in the corresponding line. Signals are output directly from the microprocessor to the driver. The output intervals differ slightly depending on whether or not a key is pressed. Figure 4-9 shows an average output interval.



Scale on the abscissa: 1 ms/div

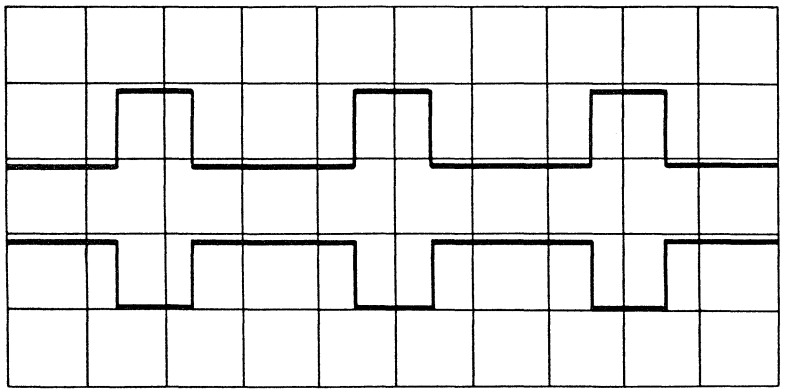
Top: Microprocessor P24 output

Bottom: Microprocessor P25 output

Figure 4-9 Microprocessor Output to Scan Driver

Figure 4-10 shows two of 11 microprocessor outputs to the scan driver. The scan driver changes the output into low-active signals and passes them to the key matrix. Therefore, the signals are high during scanning.

When there is a depressed key on the line being scanned, the other line belonging to this key (⑧ in the circuit diagram) goes low. In Figure 4.10, for example, the space key is pressed while ⓓ in the circuit diagram (Section 9) is being scanned.



Scale on the abscissa: 2 ms/div

Top: Microprocessor P24 output

Bottom: Microprocessor P25 output

Figure 4-10 Scan Detector

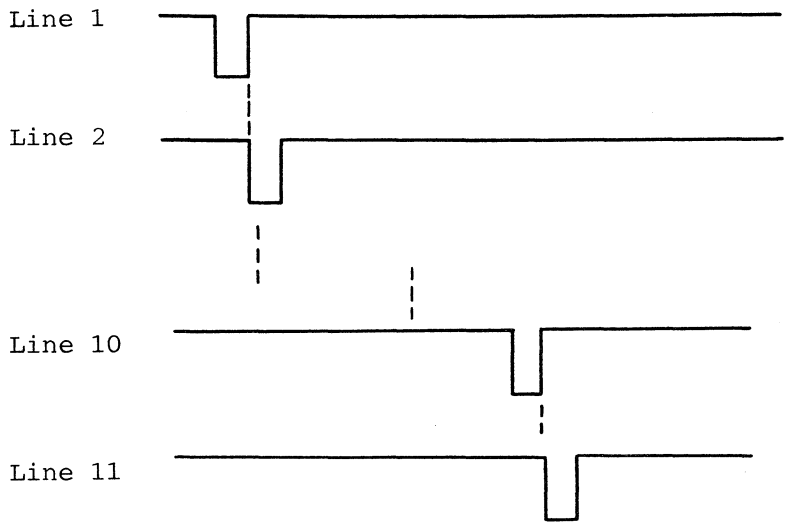


Figure 4-11 Scan Driver Output

As Figure 4-11 shows, a low-active signal is output from the scan driver only to one line on the X-axis of the key matrix at a time, checking the Y-direction each time.

When the key on line being scanned is pressed and the contact is closed, the current passes from the pull-up register, through the diode of the key being pressed, to the scan driver. This drops the potential of the Y-axis data bits (DB0-DB7 of the microprocessor) corresponding to the key, thus determining which key is being pressed.

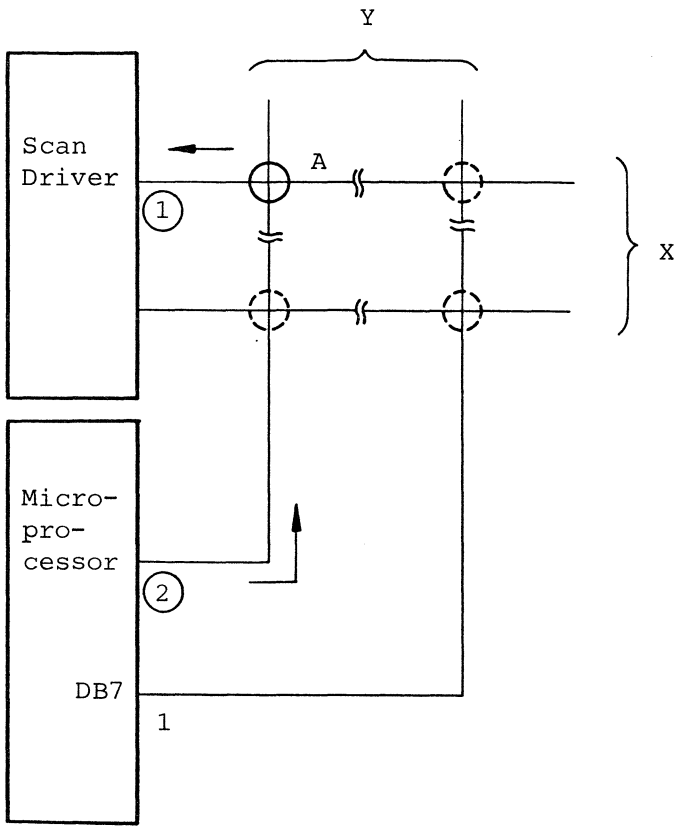
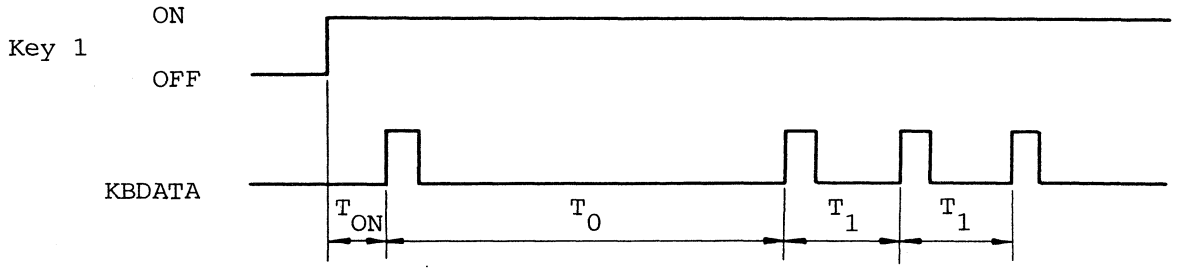


Figure 4-12 Scanning

As Figure 4-12 shows, when key A is pressed and line ① on the X-axis is scanned, the line ② on the Y-axis goes low. The microprocessor then detects that scanning lines ① and ② are low, and determines key A is being pressed.

4.7 Repeat Function

The repeat function applies to all keys. When a key is held down for more than 0.55 seconds, the ON code is output repeatedly at intervals of 100 ±10 ms. When the key being pressed is released the repeat function is terminated.



T_{ON} = 30 ms max
T_0 = 0.55 s ±0.05 s
T_1 = 100 ms ±10 ms

Figure 4-13 Start of Repeat Function

The key last recognized as ON is the key that effects the repeat function.

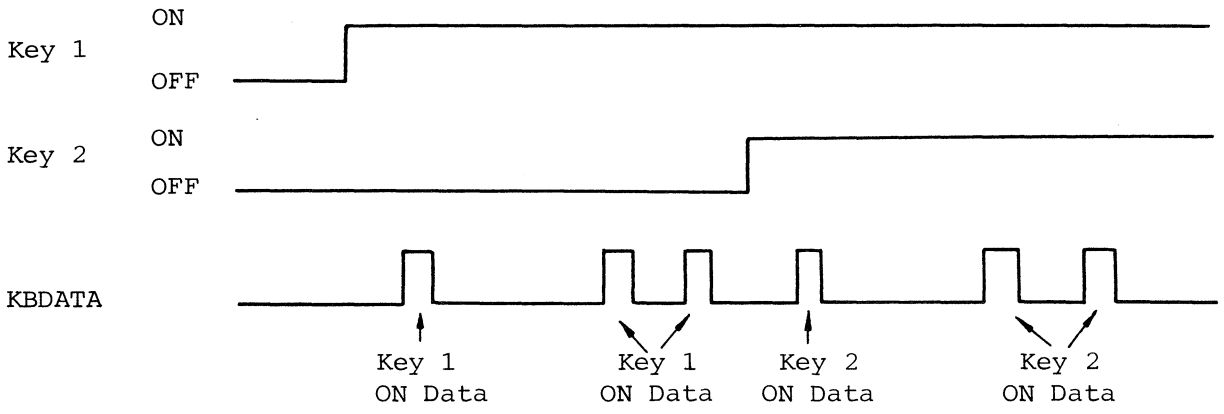


Figure 4-14 Repeat Shift

5. SELF TEST

5.1 Self Test Start Condition

When the system unit holds $\overline{\text{KBCLK}}$ LOW for 40 ms or more, a self test is requested. After checking that the keyboard is LOW for 1 ms or more, the system automatically enteres the self-check routine. KBCLK is sampled at 12.5 µs intervals to check that it is LOW for 1 ms or more.

Figure 5-1 shows the timing of a self test request.

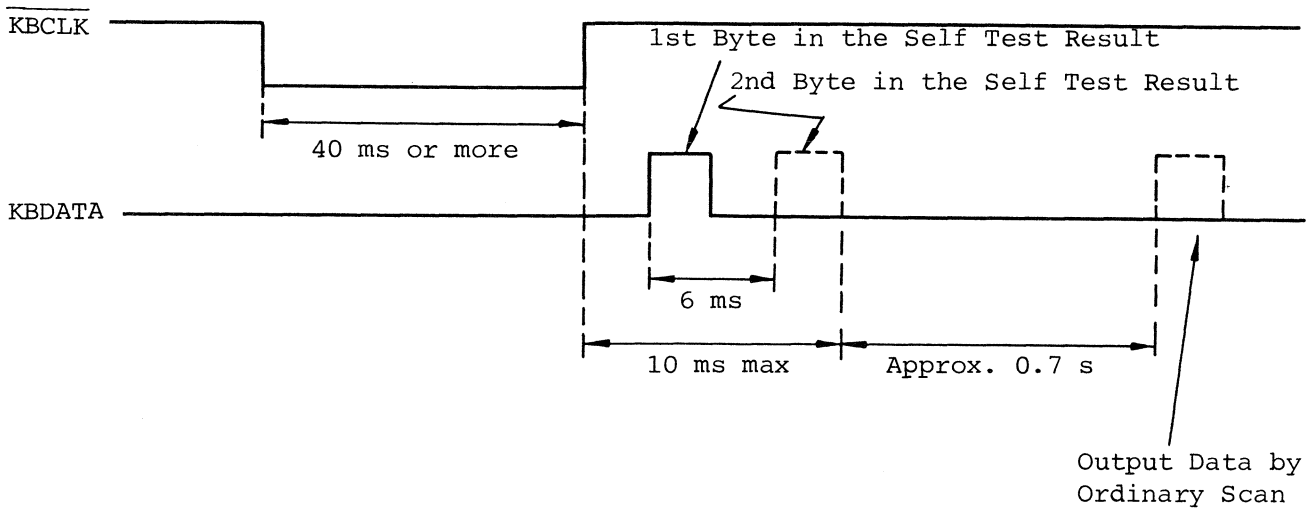


Figure 5-1 Self Test Request

① When $\overline{\text{KBCLK}}$ = L continues for 1 ms or more after it becomes LOW, the self test request is accepted.

② When $\overline{\text{KBCLK}}$ = L does not continue for 1 ms, the self test request is not accepted. Six miliseconds later, the keyboard tries again to output data.

5.2 Self Test Flowchart

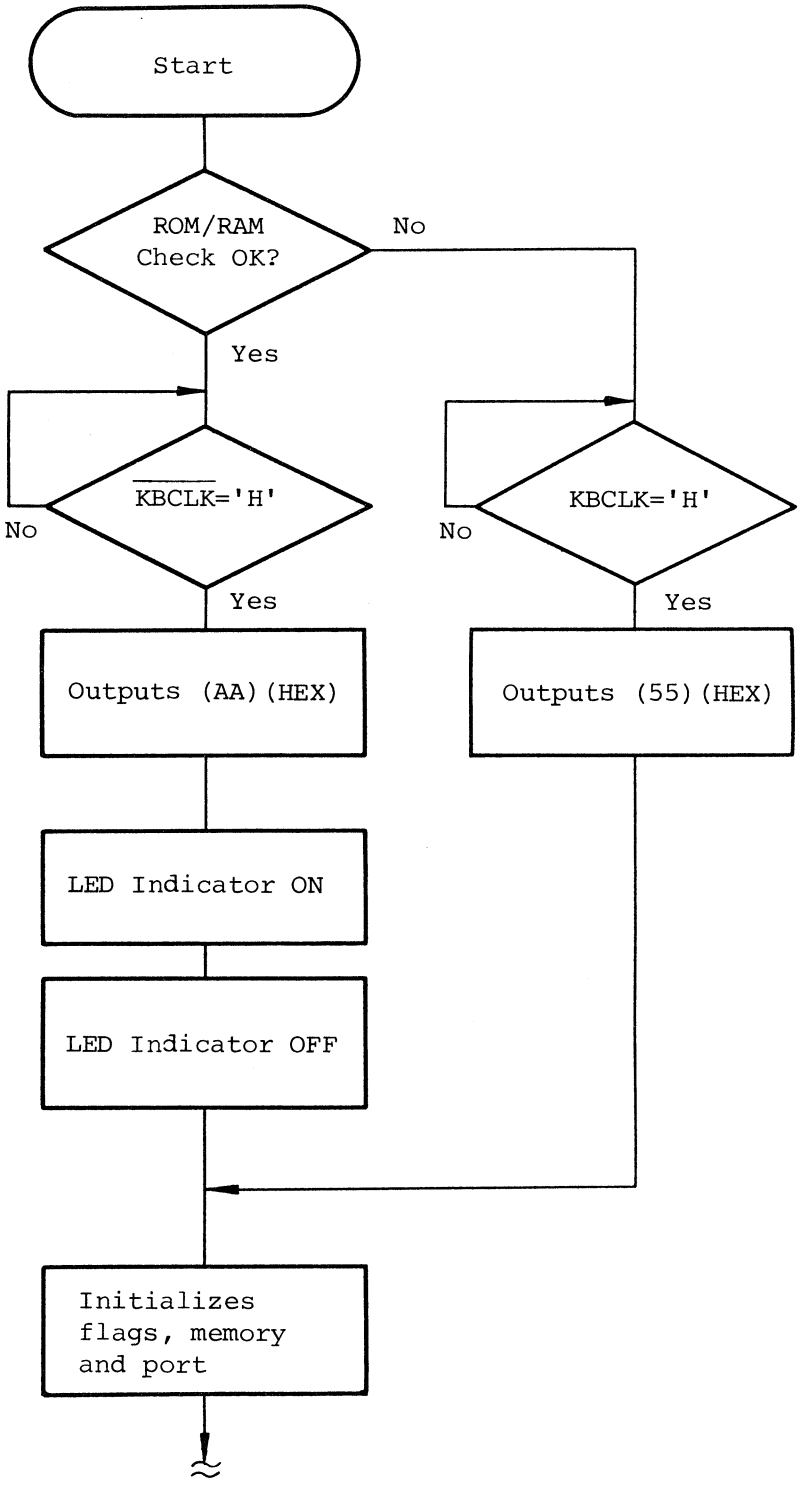


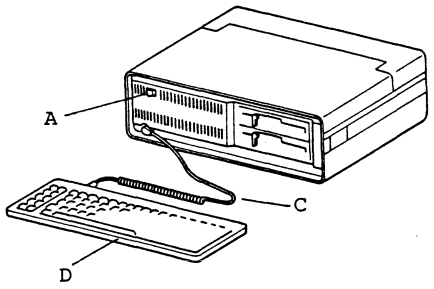
Figure 5-2 Self Test Sequence

6. DISASSEMBLY PROCEDURE

6.1 Keyboard

Step 1

Preparation for Disassembly



Rear View

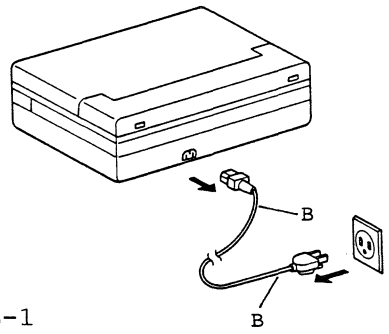


Figure 6-1

1. Set main power switch [A] to OFF.
2. Unplug AC power cord [B] from outlet.
3. Disconnect all cables (AC Power Cord [B], Keyboard Cable [C], and all optional unit cables) from System Unit.

Step 2

Removing Screws

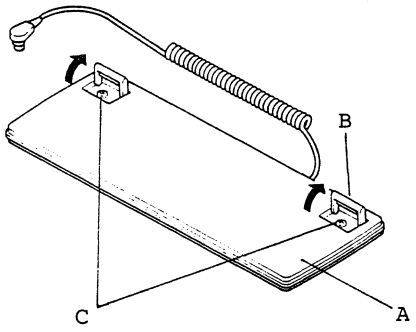


Figure 6-2

1. Press keyboard [A] with back side up.
2. Pull up retractable legs [B].
3. Remove screws [C].

Step 3

Disassembling Keyboard

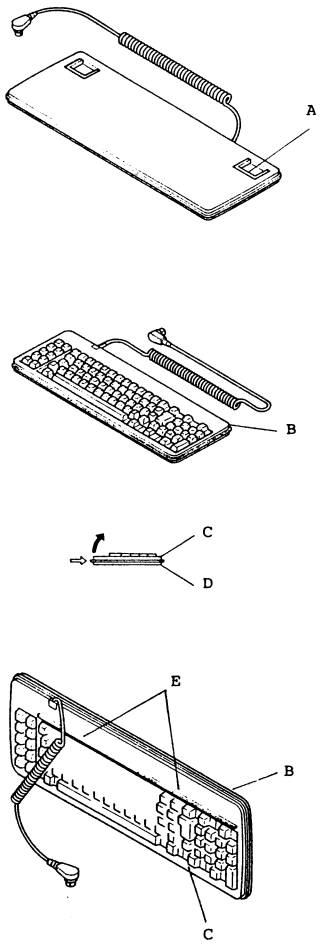


Figure 6-3

1. Put down retractable legs [A].
2. Return keyboard [B] to upright position.
3. Hold keyboard up on side and grasp cover [C] then pull apart to expose inside claw. Return keyboard to upright position and lift cover [C] up from keyboard base [D].

Step 4

Removing Keyboard Assembly

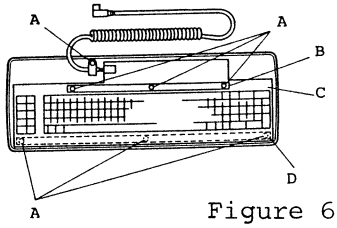


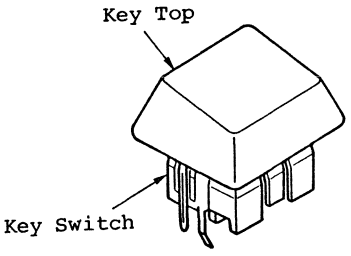
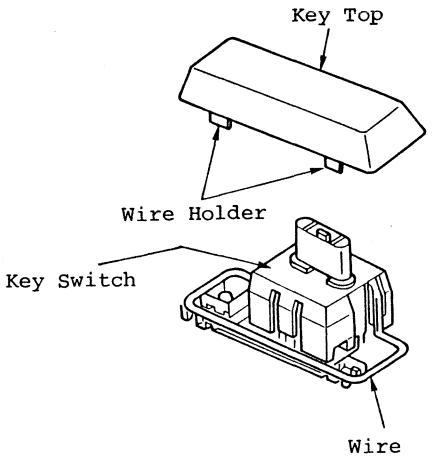
Figure 6-4

1. Remove screws [A].
2. Remove reinforcement plate [B] and pull up keyboard assembly [C] from keyboard base.

Note: Keep reinforcement plates [B] and [D] in safe place.

* Reverse steps for reassembly.

6.2 Key Switches

Replacement Part	Disassembly and Replacement
1. Key Top	(a) Key Top Below 1.75L Key: (i) Remove the key top from the key switch. (ii) Insert a new key top on to the key switch. Compare the key top height with other key top heights and check that it fits tightly.  Figure 6-5 (b) 2L Key Top (i) Remove the key top from the key switch. (ii) Hook the wire into the wire holder. (iii) Put the key top on the key switch. Check that the key top fits tightly.  Figure 6-6

Replacement Part	Disassembly and Replacement
	(c) Space Key Top

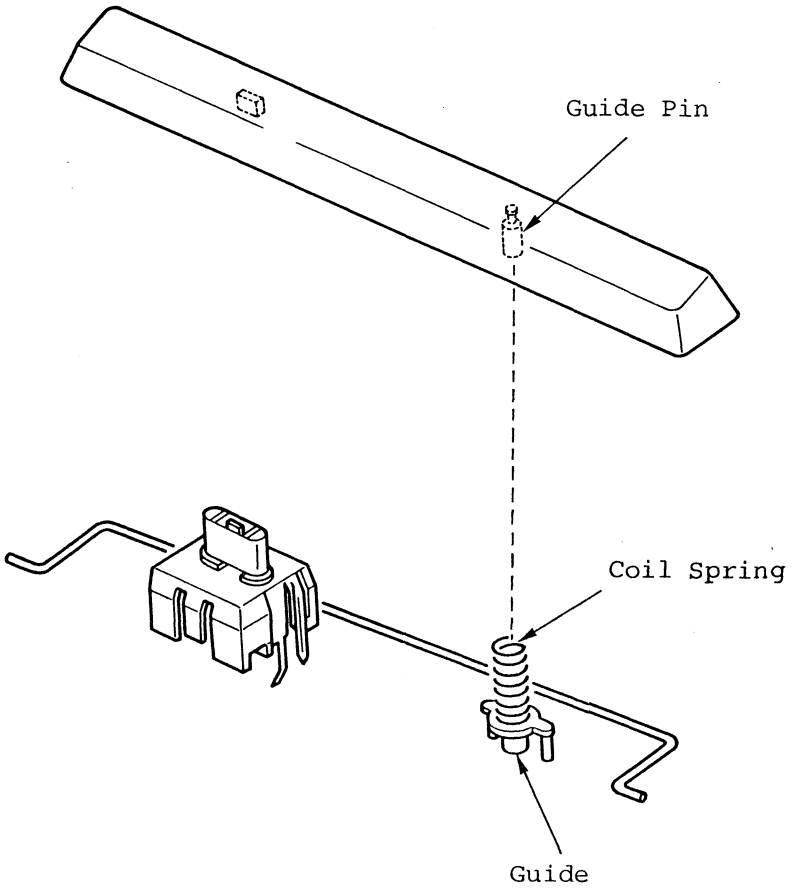


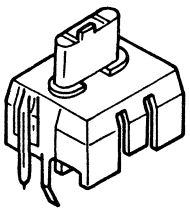
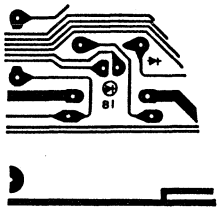
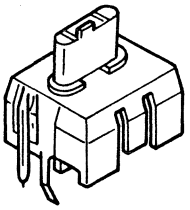
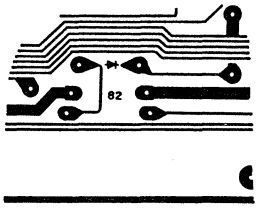
Figure 6-7

(i) Remove the key top from the key switch.

(ii) Hook the wire into the wire holder.

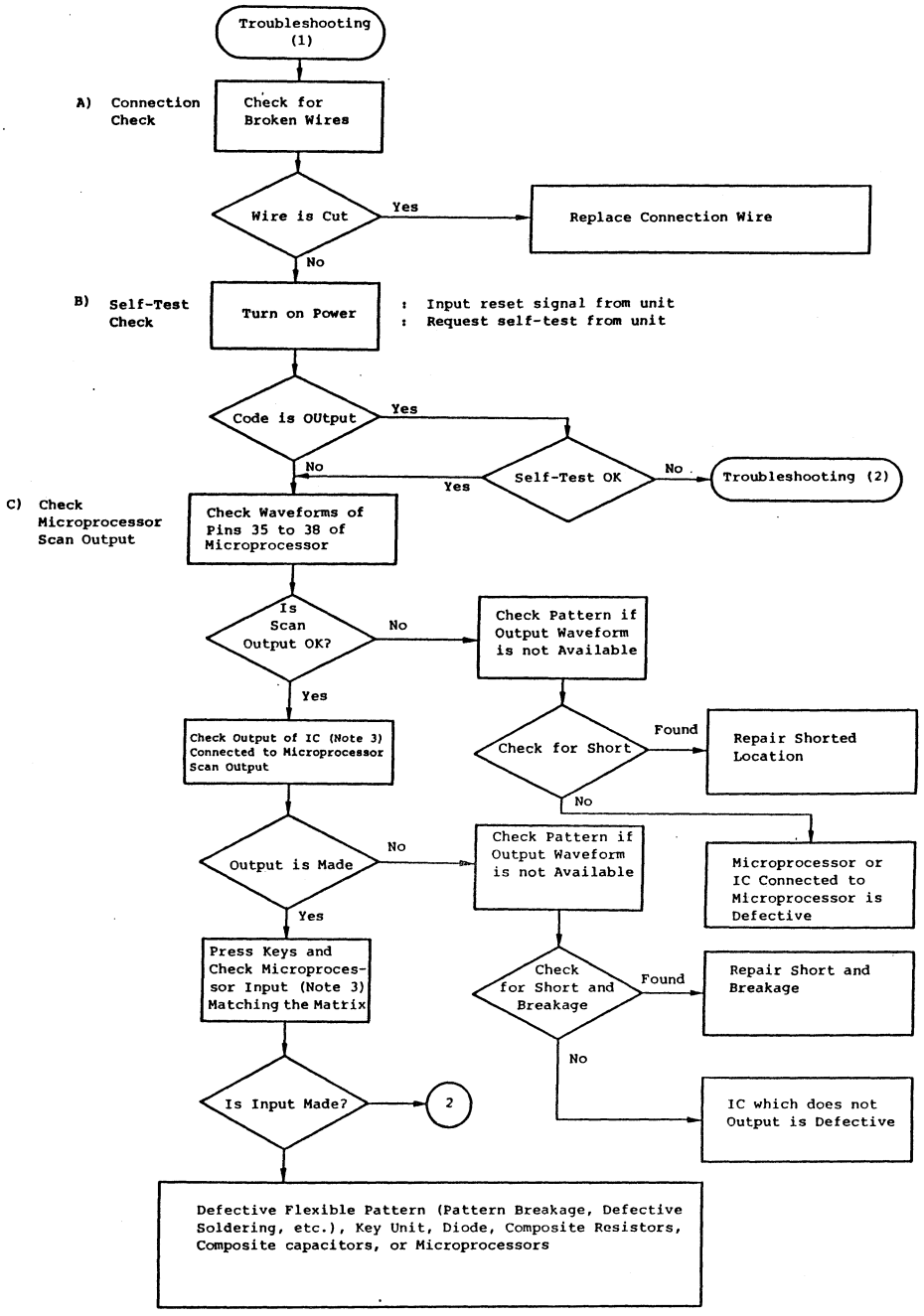
(iii) Put the key top into the key switch. Check that the key top fits tightly.

Note: Be careful not to allow the coil spring to jump out.

Replacement Part	Disassembly and Replacement
2. Key Switch	(a) Key Switches with LED Indicator (Key Numbers 17 and 18)  (i) Remove the key top as instructed in (i) and (ii) of 1.(a). (ii) Suck a solder (6 points) on the rear side. (iii) Remove a key switch.  (iv) Insert the new switch unit and solder the six points. (v) Insert the key top on the sliding body as instructed in (v) and (vi) of 1.(a). Figure 6-8 (b) Key Switches Without LED Indicator  (i) Remove the key top as instructed in (i) and (ii) of 1.(a). (ii) Remove solder (at 4 points) from the reverse side and pull out the key on the front side.  (iii) Insert the new switch unit and solder the four points. (iv) Insert the key top on the sliding body as instructed in (v) and (vi) of 1.(a). Figure 6-9

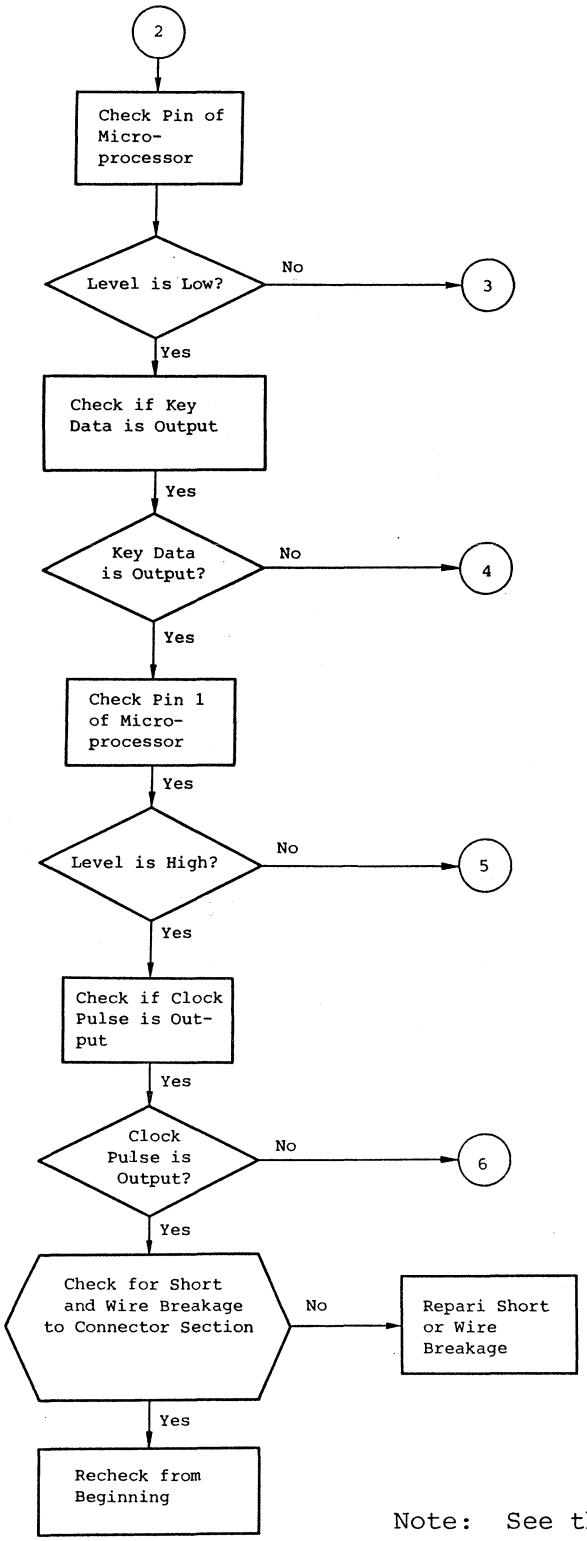
7. TROUBLESHOOTING

This is the troubleshooting method when operation of the unit corresponding to the pressed key is found to be faulty (i.e., the unit not reacting, keys not repeating, or the system unit recognizing different key output).



Note: Pins 1 to 11 of microprocessor of IC"B"

Figure 7-1 Troubleshooting



Note: See the circuit diagram.

Figure 7-1 Troubleshooting

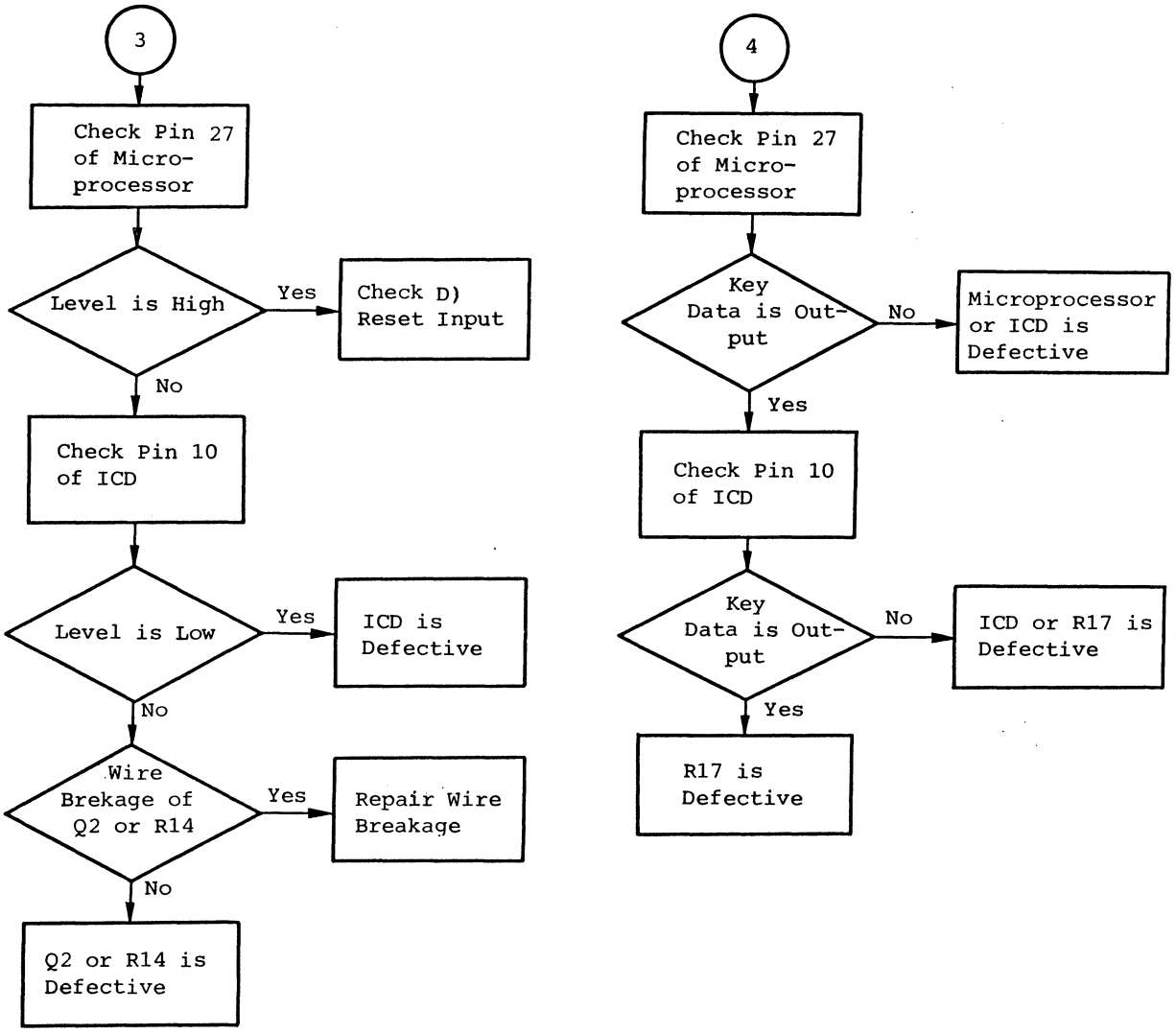


Figure 7-1 Troubleshooting

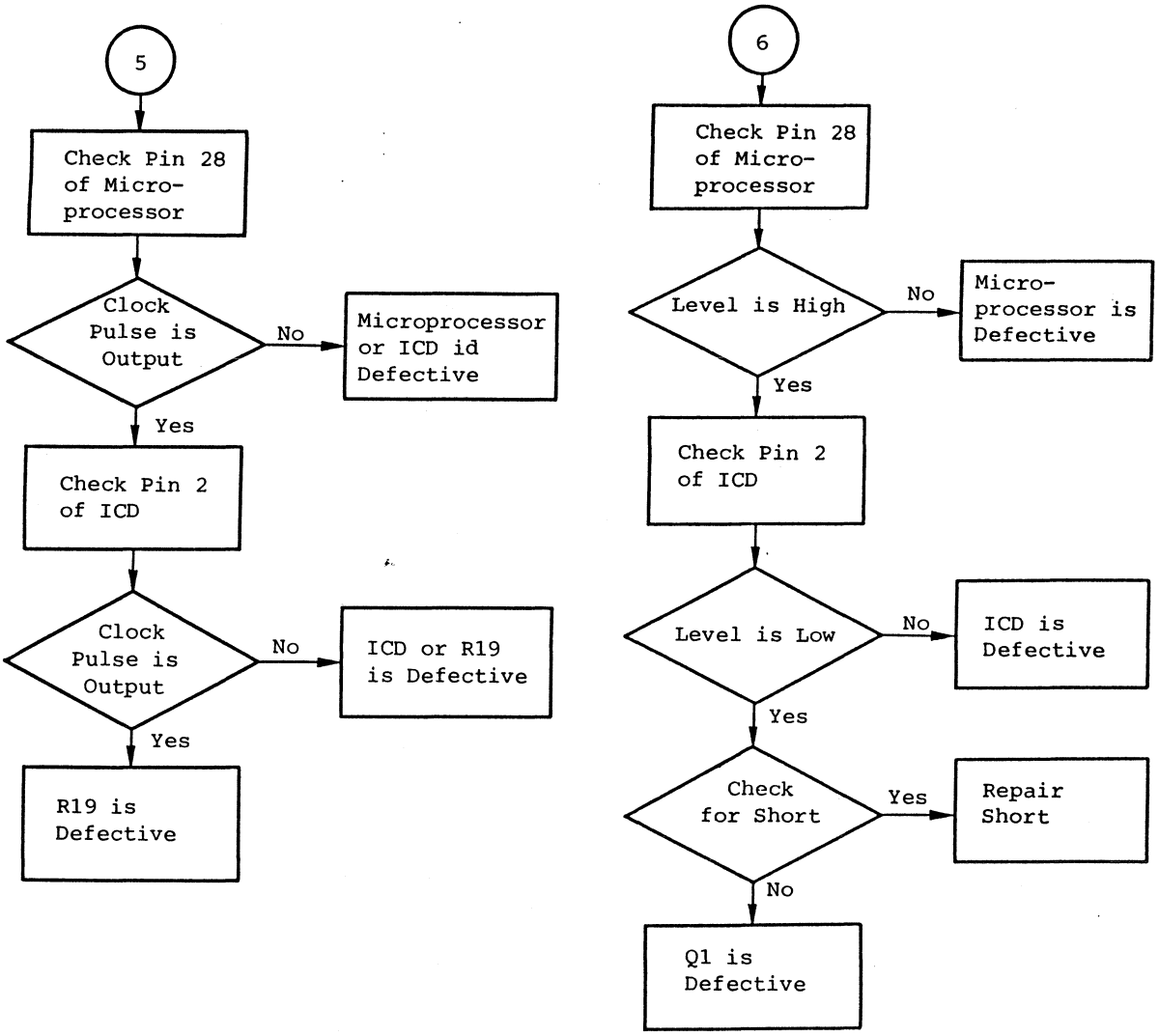


Figure 7-1 Troubleshooting

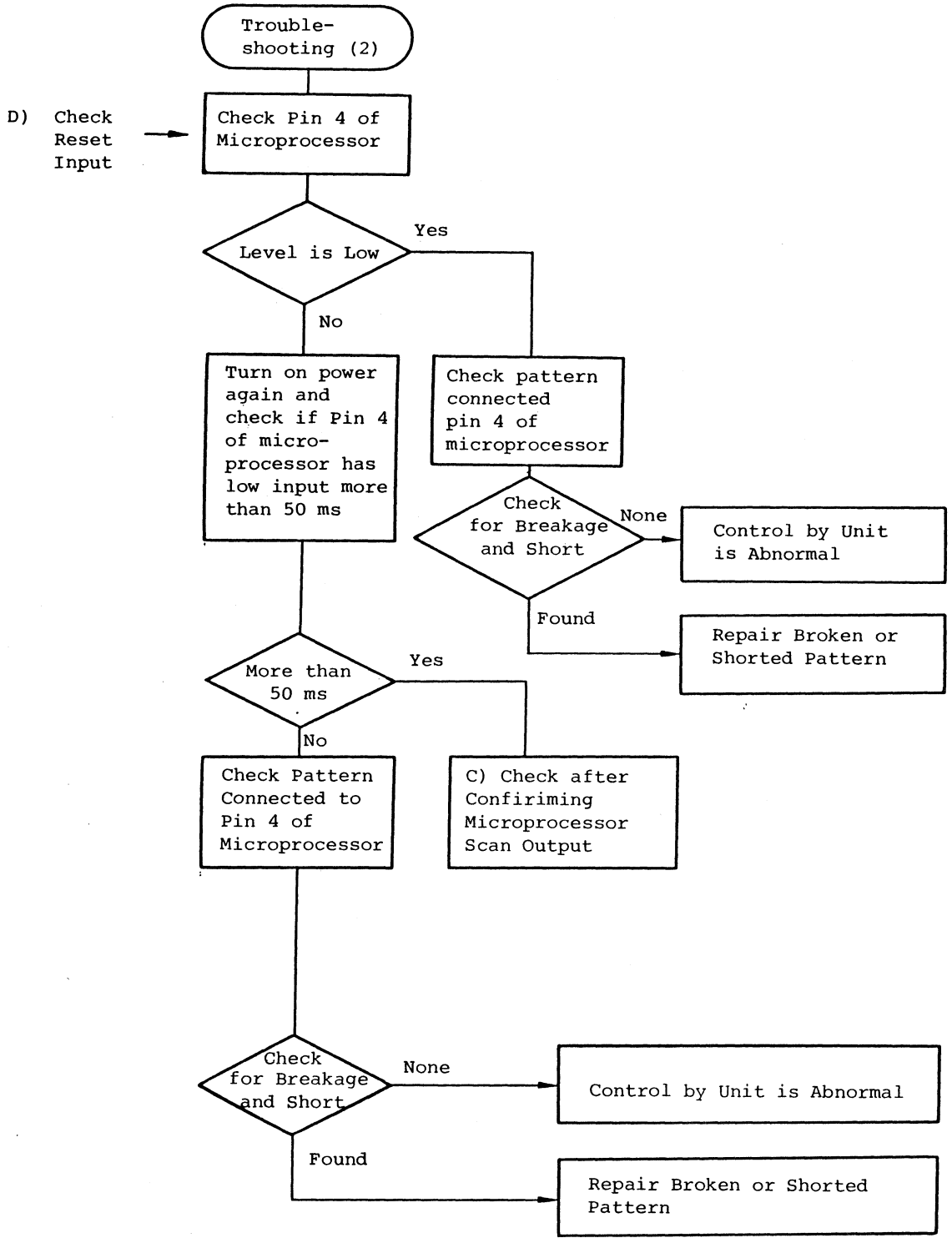


Figure 7-1 Troubleshooting

8. REPLACEMENT PARTS LIST AND DRAWING

8.1 Exploded View

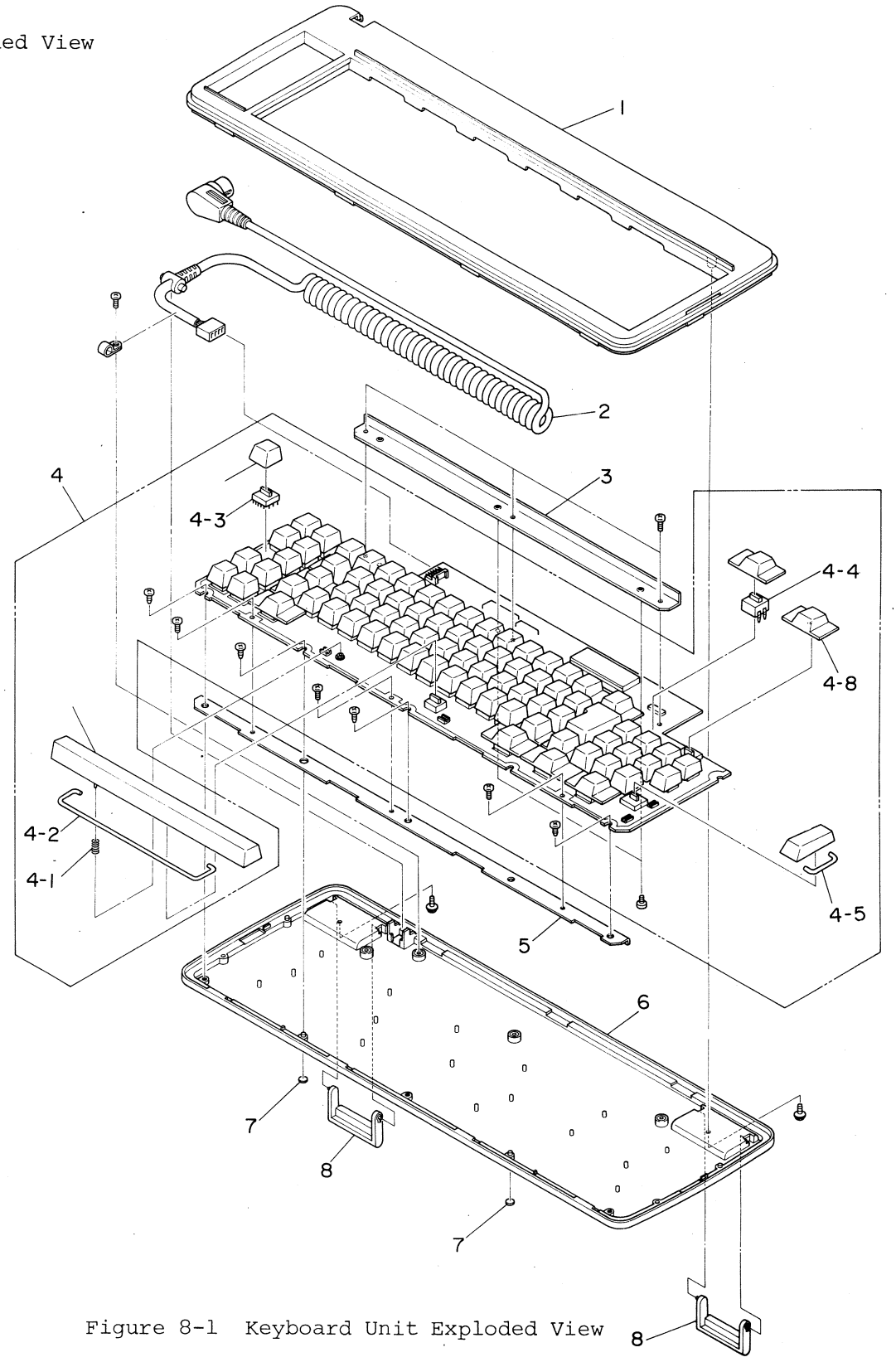


Figure 8-1 Keyboard Unit Exploded View

REPLACEMENT PARTS LIST (Keyboard)

NOTE:
- **When ordering replacement parts indicate Part No. and Name of Parts.**
- **⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.**

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
1		YJJ5E08570D1	Upper Case	1	
2		YJJDK02580B3	Curl Cord	1	
3		YJJ3B10250B3	Reinforcing Plate 1	1	
4		YJJUK03870B4	Keyboard Sub Ass'y	(1)	ASC Version
		YJJUK03800B4	Keyboard Sub Ass'y	(1)	German
		YJJUK03840B4	Keyboard Sub Ass'y	(1)	English
		YJJUK03290B4	Keyboard Sub Ass'y	(1)	Suedish/ Finish
		YJJUK03860B4	Keyboard Sub Ass'y	(1)	French
4-1		YJ27KF021A	Spring	1	
4-2		YJ21KF009A	Lever		
4-3		YJSKFLAC000A	Push Switch	82	
4-4		YJSKFLAF000A	Push Switch (LED)	2	
4-5		YJ21KF008A	Lever	2	
5		YJJ3B10260B3	Reinforcing Plate 2	1	
6		YJJUX03300B1	Lower Case	1	
7		YJJ5V08620B4	Pad	(2)	
8		YJJ5N08560B3	Tilt Leg	(2)	
		1S2075K	Diode	85	
A		UPD8048HC169	Lsi	1	
B		SN74159N	IC	1	
C		SN74LS132N	IC	1	
D		SN7417N	IC	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
CERA LOCK		YJKMFC1005T1	Crystal Oscillator	1	
R14,15		ERD25TJ271	Carbon Resistor L70Ω 1/4W	2	
R10,11,1, 18,12,13,16		FRD25TJ472	Carbon Resistor 4.7kΩ 1/4W	7	
R17,18,20		ERD25TJ470	Carbon Resistor 47Ω 1/4W	3	
R.ARY		YJARB01770B4	Resistor Arry 4.7kΩ	1	
C1,4		ECEB1CS470	Electrolitic Capacitor 47μF 16V	2	
C2,3,10		YJ104B102KS	Ceramic Capacitor 1000PF 50V	3	
C11		YJ4C24020A	Ceramic Capacitor 100PF 50V	1	
C6,8,9		YJ408SR4MS	Ceramic Capacitor 0.1μF 16V	3	
C5,7		YJR22F104ZF	Ceramic Capacitor 0.1μF 50V	2	
FB1		BL02RN2-R62.	Core	1	
CN		YJILG6PS3L2E	Connector	1	
		YJCB16413A	Lavel	1	

REPLACEMENT PARTS LIST (PLS K/B)

NOTE:
- When ordering replacement parts indicate Part No. and Name of Parts.
- ⚠ indicates that only parts specified by the manufactures to be used for replacement in critical circuits.

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
		YJ86N1C44017	Key Top ! 1	1	
		YJ86N1C44018	@ 2	1	
		YJ86N1C44019	# 3	1	
		YJ86N1C44020	$ 4	1	
		YJ86N1C44021	% 5	1	
		YJ86N1C44022	6	1	
		YJ86N1C44023	& 7	1	
		YJ86N1C44024	* 8	1	
		YJ86N1C44025	(9	1	
		YJ86N1C44026	) 0	1	
		YJ86N1C44027	_ -	1	
		YJ86N1C44028	+ =	1	
		YJ86N2C44013	Q	1	
		YJ86N2C44014	W	1	
		YJ86N2C44015	E	1	
		YJ86N2C44016	R	1	
		YJ86N2C44017	T	1	
		YJ86N2C44018	Y	1	
		YJ86N2C44019	U	1	
		YJ86N2C44020	I	1	
		YJ86N2C44021	Keytop O	1	
		YJ86N2C44022	P	1	
		YJ86N2C44023	{ [	1	
		YJ86N2C44024	7 Home	1	
		YJ86N2C44025	8 ↑	1	
		YJ86N2C44026	9 PgUp	1	
		YJ86N2C44027	}]	1	
		YJ86N3C44014	A	1	
		YJ86N3C44015	S	1	
		YJ86N3C44016	D	1	
		YJ86N3C44018	G	1	
		YJ86N3C44019	H	1	
		YJ86N3C44021	K	1	
		YJ86N3C44022	L	1	
		YJ86N3C44023	: ;	1	
		YJ86N3C44024	" '	1	
		YJ86N3C44025	~	1	
		YJ86N3C44026	4 ←	1	
		YJ86N3C44028	6 →	1	
		YJ86P6C44001	F	1	
		YJ86P6C44002	J	1	
		YJ86P6C44003	5	1	
		YJ86N4C44012		1	
		YJ86N4C44013	Z	1	
		YJ86N4C44014	X	1	
		YJ86N4C44015	C	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
		YJ86N4C44016	Key Top V	1	
		YJ86N4C44017	B	1	
		YJ86N4C44018	N	1	
		YJ86N4C44019	M	1	
		YJ86N4C44020	< ,	1	
		YJ86N4C44021	> .	1	
		YJ86N4C44022	? /	1	
		YJ86N4C44023	1 End	1	
		YJ86N4C44024	2 ↓	1	
		YJ86N4C44025	3 PgDn	1	
		YJ81W4C44001	• Del	1	
		YJ86N1C25058	F1	1	
		YJ86N1C25059	F2	1	
		YJ86N1C25060	Esc	1	
		YJ86N2C25018	F3	1	
		YJ86N2C25019	F4	1	
		YJ86N2C25020	—	1	
		YJ86N3C25036	F5	1	
		YJ86N3C25037	F6		
		YJ86N3C25043	+	1	
		YJ86N4C25020	F7	1	
		YJ86N4C25021	F8	1	
		YJ86N5C25010	F9	1	
		YJ86N5C25011	F10	1	
		YJ84F1C25001	⇧ (small)	1	
		YJ84F1C25002	Prt Sc *	1	

Ref. No		Parts No.	Parts Name & Description	Pcs/Set	Remarks
		YJ83N3C25003	Key Top ⇤ ⇥	1	
		YJ83N4C25002	⇧ (large)	1	
		YJ82H3C25002	Ctr1	1	
		YJ81W4C25002	Alt	1	
		YJ80L5C25001	⏎ (large)	1	
		YJ81U5C25003	⏎ (Small)	1	
		YJ81W3C25003	←	1	
		YJ81CHC44001	0 1ns	1	
		YJ81Y7CNU	Num Lock	1	
		YJ81Y6CCA	Caps Lock	1	
		YJC5KF090A	Scroll Lock	1	
		YJ86N1C44035	"@ 2	1	Germany
		YJ86N1C44036	§ 3	1	
		YJ86N1C44037	& 6	1	
		YJ86N1C44038	/ 7	1	
		YJ86N1C44039	(8	1	
		YJ86N1C44040	) 9	1	
		YJ86N1C44041	= 0	1	
		YJ86N1C44042	? ß	1	
		YJ86N1C44034	´ '	1	
		YJ86N2C44028	Z	1	
		YJ86N2C44029	u[	1	
		YJ86N2C44030	*] +	1	
		YJ86N3C44032	ö	1	
		YJ86N3C44033	Ä	1	
		YJ86N3C44034	#	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
		YJ86N4C44030	Key Top > < \	1	Germany
		YJ86N4C44026	Y	1	
		YJ86N4C44027	; ,	1	
		YJ86N4C44028	: .	1	
		YJ86N4C44029	_ -	1	English
		YJ86N1C44043	" 2	1	
		YJ86N1C44044	£ 3	1	
		YJ86N1C44045	£ # 3	1	Swedish/ Finish
		YJ86N1C44046	& 6 ^	1	
		YJ86N1C44047	/& 7	1	
		YJ86N1C44048	(* 8	1	
		YJ86N1C44049	) (9	1	
		YJ86N1C44050	=) 0	1	
		YJ86N1C44051	? _ + -	1	
		YJ86N1C44052	' + =	1	
		YJ86N2C44031	Å {]	1	
		YJ86N2C44032	¨ }]	1	
		YJ86N3C44037	ö :	1	
		YJ86N3C44038	Ä "	1	
		YJ86N4C44031	> < \	1	
		YJ86N4C44032	: . >	1	
		YJ86N4C44033	_ ? -	1	
		YJ86N4C44027	; ,	1	
		YJ86N1C44053	1 &	1	French
		YJ86N1C44054	2 @ é	1	
		YJ86N1C44055	3 # "	1	

Ref. No.		Parts No.	Parts Name & Description	Pcs/Set	Remarks
		YJ86N1C44056	Keytop 4 $ 5 (6 § ^ 7 é	1	French
		YJ86N1C44057		1	
		YJ86N1C44058		1	
		YJ86N1C44059		1	
		YJ86N1C44060	8 !	1	
		YJ86N1C44061	9 ç	1	
		YJ86N1C44062	0 à °	1	
		YJ86N1C44063	) [	1	
		YJ86N2C44033	¨ Ä *]	1	
		YJ86N2C44034	$	1	
		YJ86N2C44035	A	1	
		YJ86N3C44030	Q	1	
		YJ86N3C44031	M	1	
		YJ86N3C44040	% ù	1	
		YJ86N3C44041	£ µ	1	
		YJ86N4C44035	? '	1	
		YJ86N4C44036	. ;	1	
		YJ86N4C44037	/ :	1	
		YJ86N4C44038	+ =	1	
		YJ86N4C44039	W	1	
		YJ86N4C44034	> < \	1	
		YJ80P5C44000	Space Key	1	

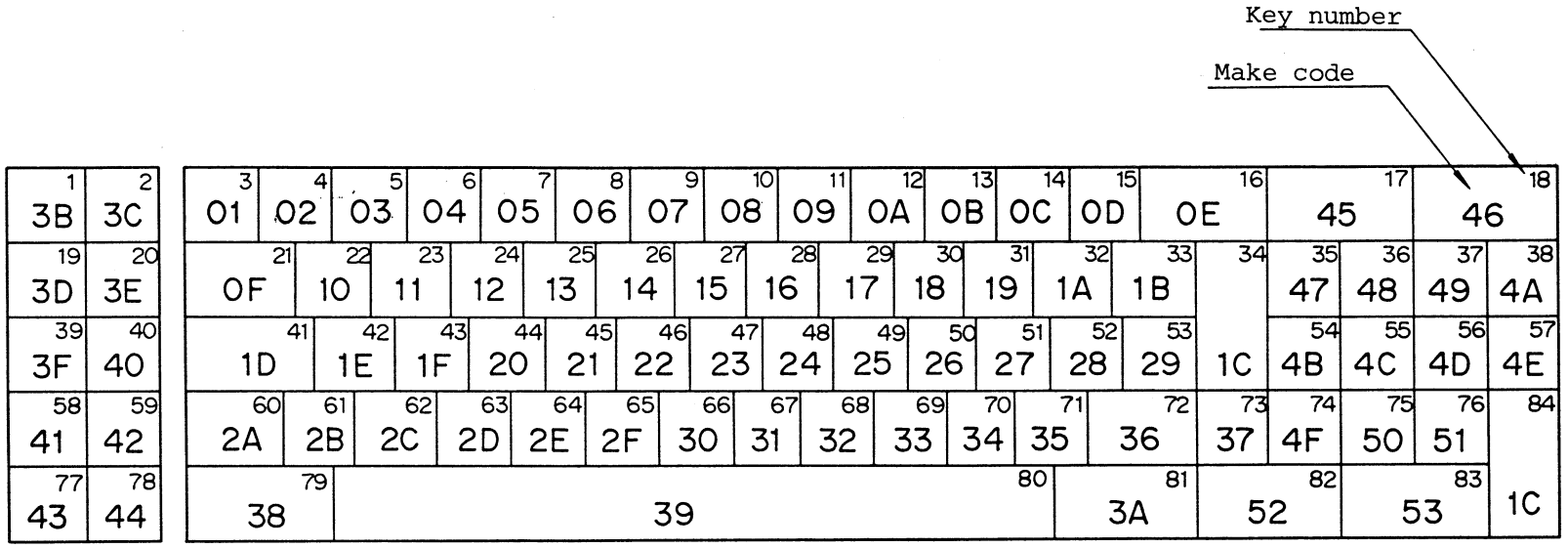


Figure 8-2 Coard Table

8.3 Circuit Diagram

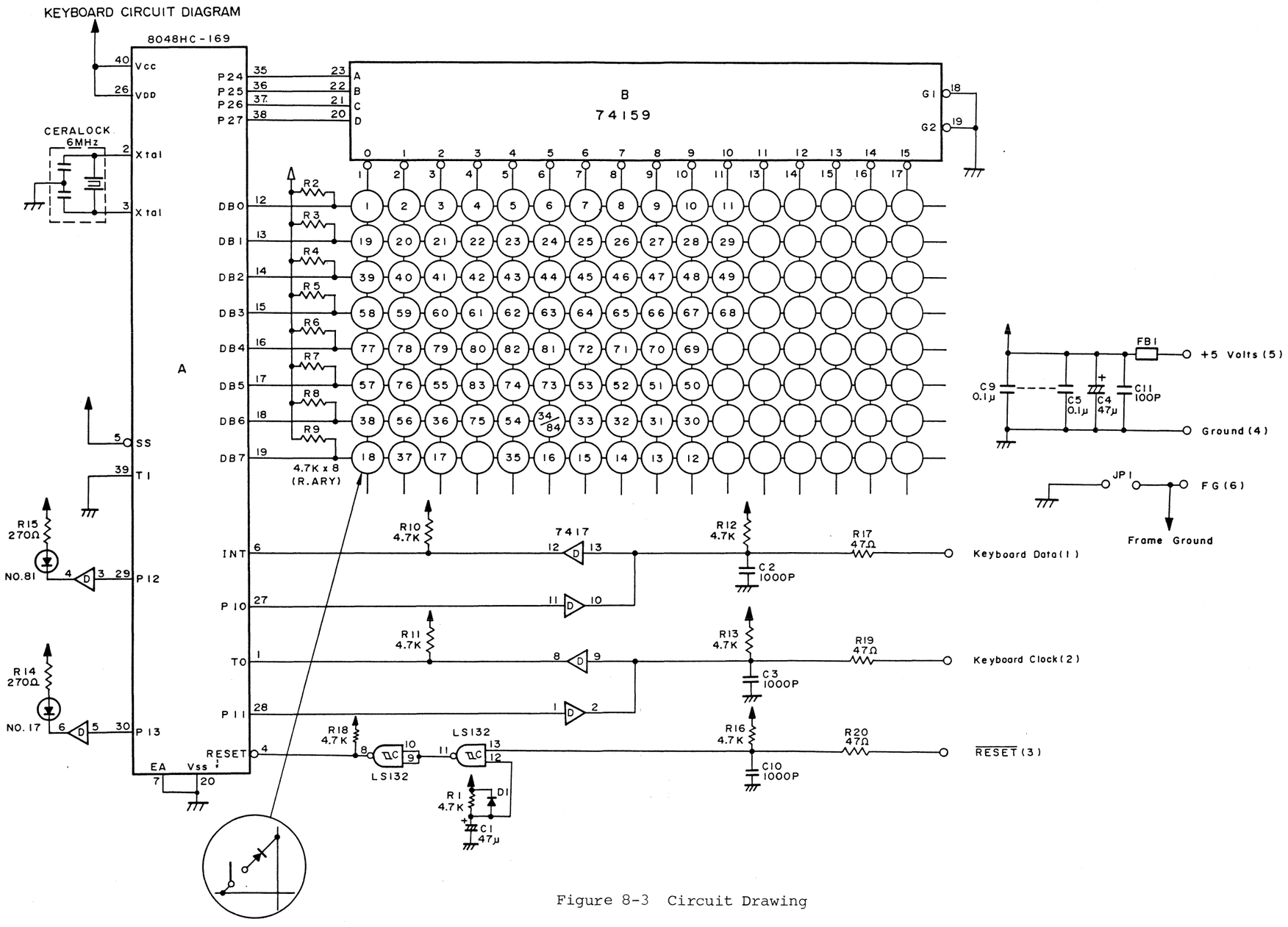


Figure 8-3 Circuit Drawing

ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

V. POWER SUPPLY UNIT

1. SPECIFICATIONS

Table 1-1 DC Output

DC Output Voltage	Current Min.	Max.	Peak
+5 V	3.9 A	10.4 A	
-5 V	10 mA	300 mA	
+12 V	0.1 A	1.6 A	4.2 10 minutes after powering on
-12 V	10 mA	260 mA	
-205 V*1 (plasma display)	10 mA	150 mA	
-200 V*1 (plasma display)	0 mA	60 mA	

Note: *1 When the power supply is connected to the equipment, the -205 V becomes -200 V and the -200 V becomes -195 V respectively.

Input Voltage (Switch Selectable)

220 to 240 V ±10% 50/60 Hz
110 to 120 V ±10% 50/60 Hz

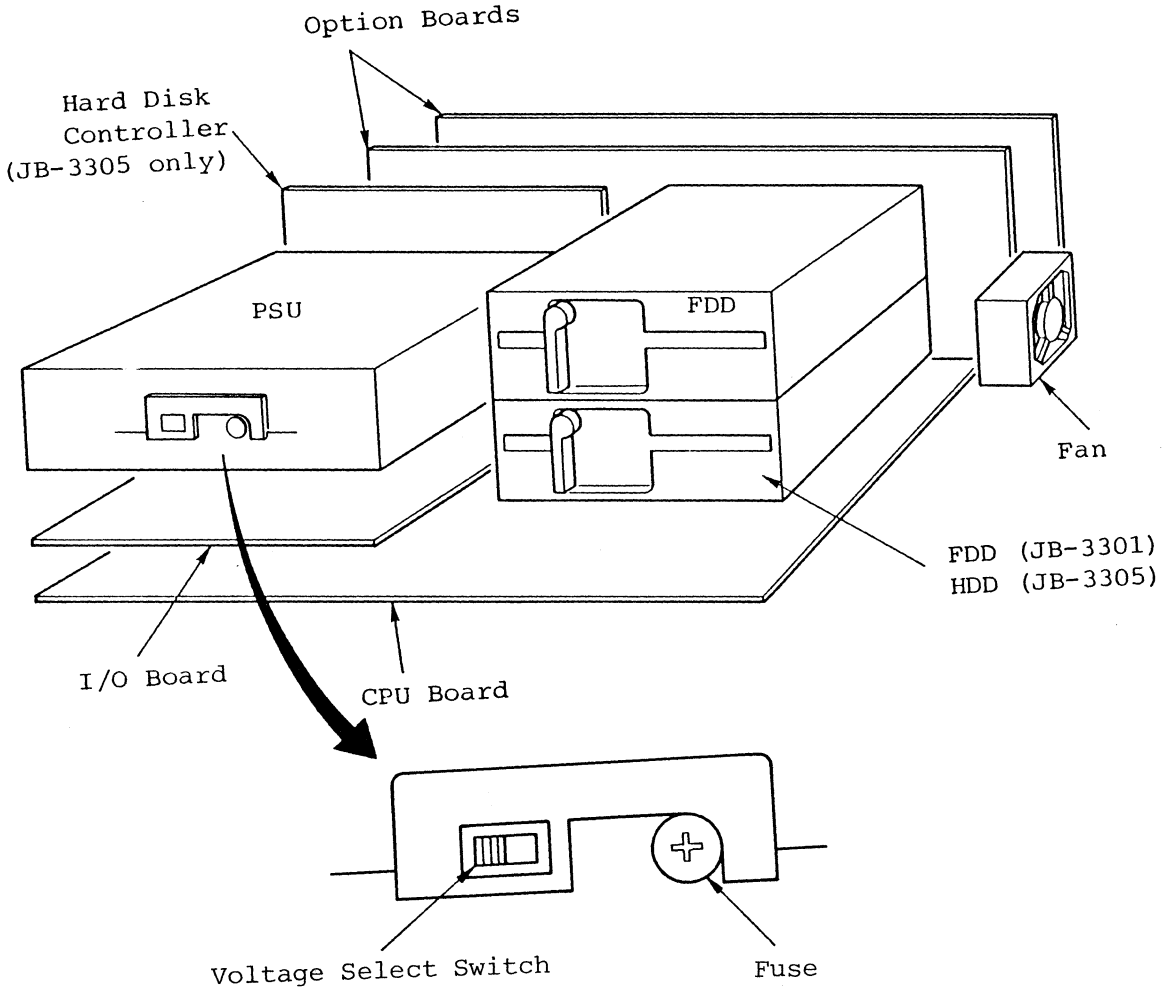
Input Consumption

220 V 1.4 A max
110 V 2 A max

Fuse

Europe standard BET-5A miniature fuse

2. APPEARANCE



3. BLOCK DIAGRAM

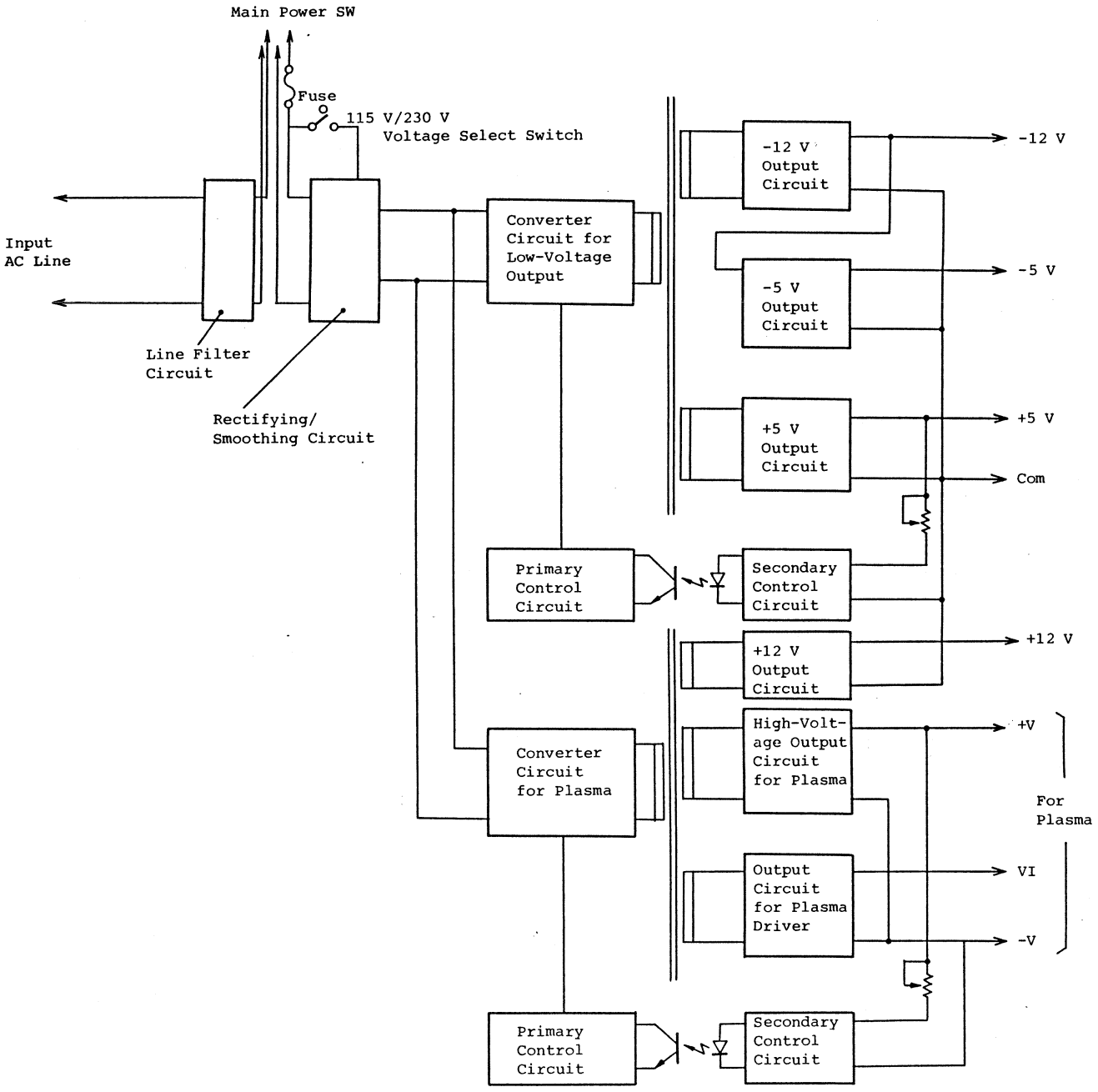


Figure 3-1 System Block Diagram

4. HARDWARE OUTLINE

4.1 General

The power supply is controlled by an ON/OFF switch. Additionally, the plasma display screen must be in a raised position for the power supply to operate.

This power unit is an input/output insulating type switching regulator employing two flyback converters. The first flyback converter stabilizes the low voltage outputs (+5 V, -5 V, -12 V); the other provides a high voltage (-205 to -200 V) output for plasma display and +12 V. Since the mode of rectification can be changed with the input voltage selector switch, input voltages of either 115 V or 230 V can be used. Also, an erroneous input voltage (i.e., an input of 230 V at the 115 V setting) simply blows the input fuse; the main body of the power unit is protected. Reinforced insulation is employed for parts such as transformers, photocouplers, and printed boards which require insulation between primary and secondary circuits.

4.2 Input Block

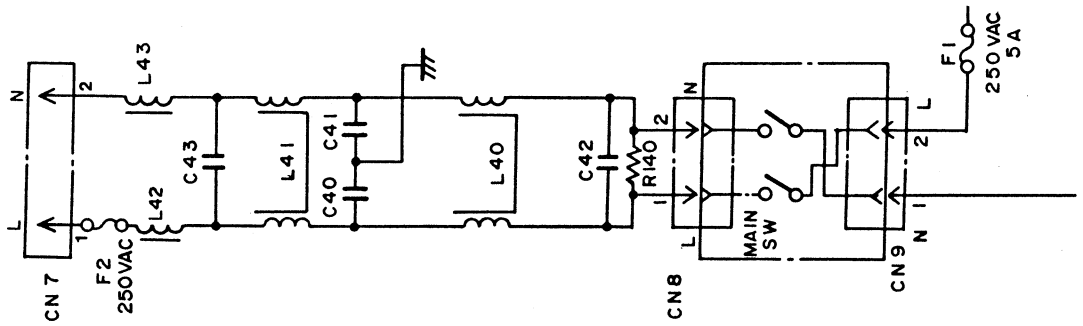


Figure 4-1 Power Supply Circuit

A rush resistant input fuse F1 is employed to withstand input rush current.

The line filter is composed and C43 of choke coils L40, L41, L42 and L43, and capacitors C40, C41, C42 and C43, which reduce input terminal noise. The line filter also suppresses impulse noises from the AC line.

4.3 Rectifying/Smoothing Circuit

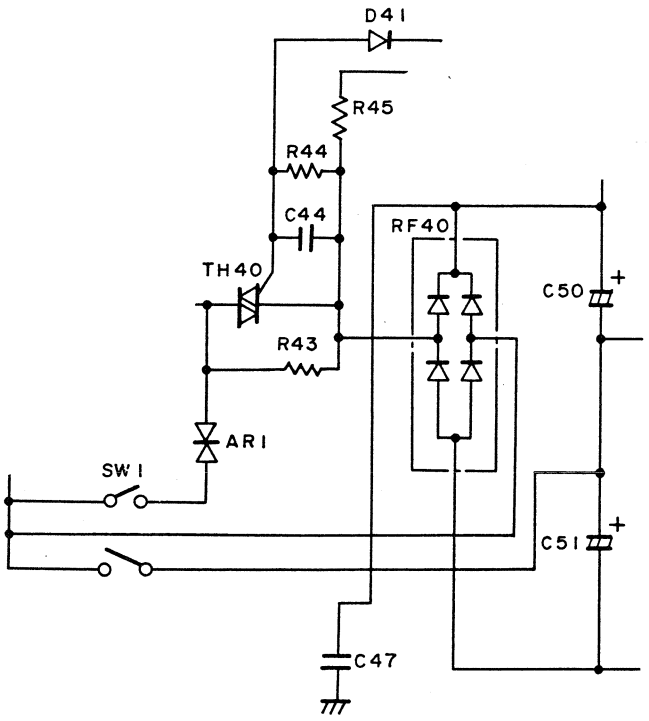


Figure 4-2 Rectifying/Smoothing Circuit

The current is rectified by diode RF40 and smoothed by capacitors C50 and C51.

By changing the mode of rectification with SW1, the voltages provided to the smoothing capacitors C50 and C51 are equalized for both 115 V and 230 V inputs. That is, full wave voltage doubler rectification is effected for 115 V input and full wave rectification for 230 V input.

When 230 V is applied at the 115 V setting, the arrester AR1 is discharged and melts the fuse F1, protecting the converter circuits. To restore this unit to normal set the input voltage and replace fuse F1. The arrester AR1 is separated from the circuit by the 1 circuit of the selector switch SW1 when the input is set for 115 V.

TH40, F3, and R43 comprise an inrush current restriction circuit. In this circuit, R43 restricts the volume of the charging current flowing through C50 and C51 when the input voltage is applied. C44, R44, R46, and D41 supply the gate signal to trigger TRIAC TH40 during operation.

4.4 Converter and Output Circuits for Low Voltage Output

The primary converter is a flyback. Power is transmitted by storing energy in transformer T40 while switching transistor Q40 is ON and transmitting the energy to the secondary while Q40 is OFF.

Each DC output is provided by rectifying and smoothing the pulse voltage obtained from the secondary winding of transformer T40. The +5 V output voltage is sensed and regulated to a constant value. -12 V and -5 V outputs are stabilized by Voltage Regulator ICs. The Voltage Regulator ICs stabilize -5 V and -12 V outputs.

4.5 Converter and Output Circuits for Plasma

As in the case of the low voltage output, a flyback converter circuit is employed for the plasma. The -205 V output voltage for the plasma is likewise sensed and regulated for stability. A voltage regulator IC stabilizes the -205 V and +12 V output voltages.

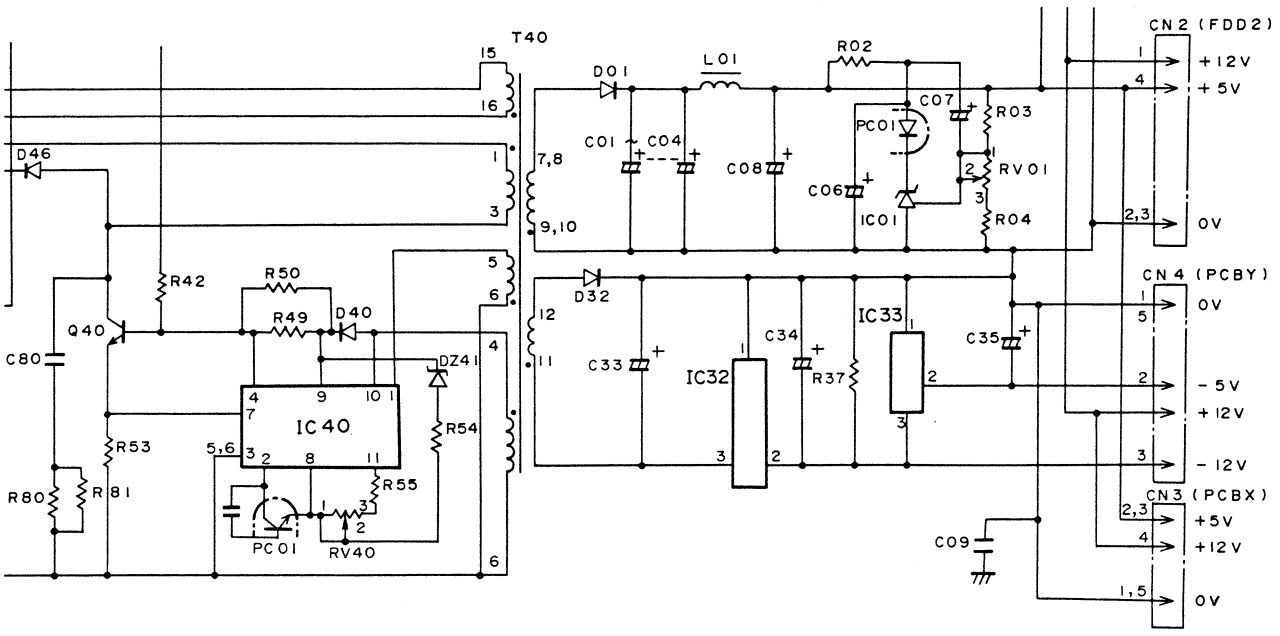


Figure 4-3 Converter and Output Circuit

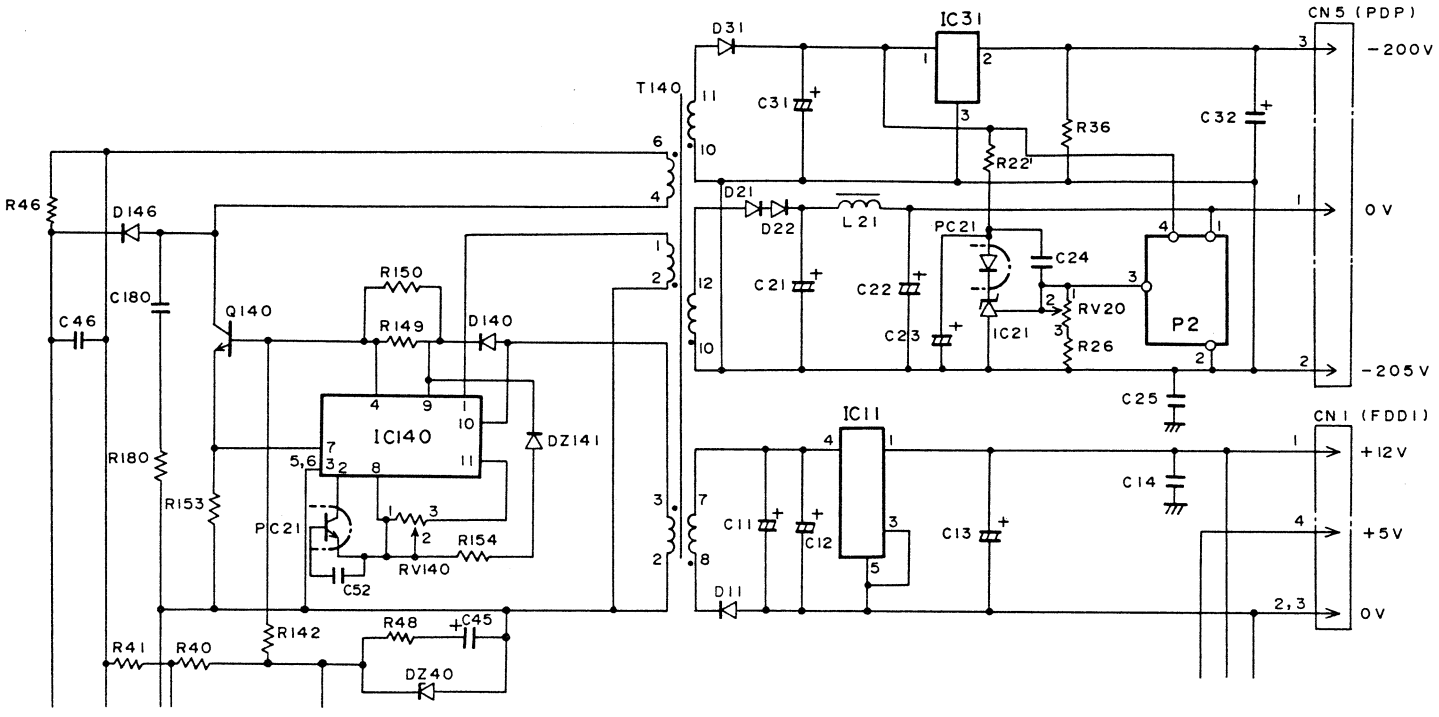


Figure 4-4 Converter and Output Circuits (For Plasma)

4.6 Primary Control Circuits

Similar primary control circuits are employed for both the low voltage output and plasma. The control circuits, which are entirely incorporated in IC40 and IC140, are of the variable frequency self-oscillation type with ON period control. These circuits control the timing of the absorption, by IC40 and IC140, of the drive current from the base drive windings of transformers T40 and T140. The control signals are transmitted from the secondary side via photocouplers PC01 and PC21. IC40 and IC140 also have built-in surge current protection functions.

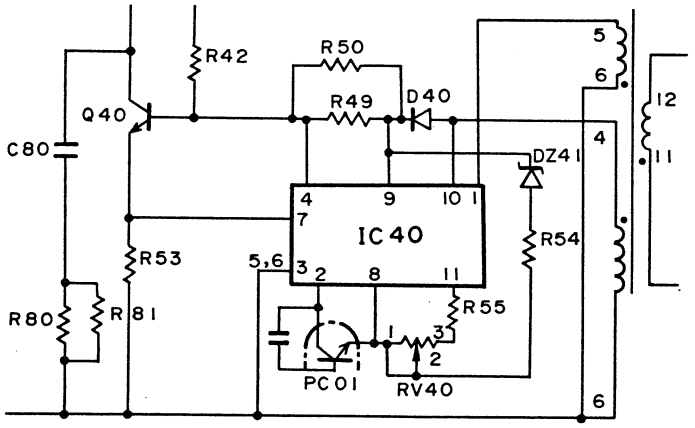


Figure 4-5 Primary Control Circuit for Low Voltage

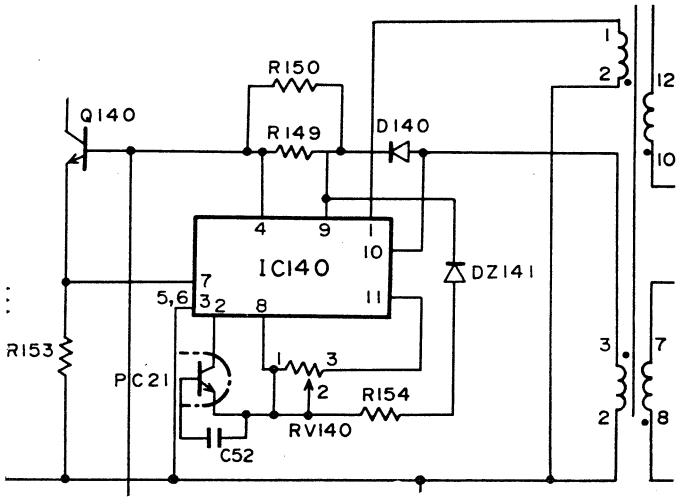


Figure 4-6 Primary Control Circuit for Plasma

4.7 Secondary Control Circuits

As shown in Figure 4-7, the secondary control circuit for low voltage output senses the +5 V output voltage, feeds it into IC01 volume RV01, compares it with the reference voltage incorporated in the IC, interprets any discrepancy as a current change, creates a current flow in the photocoupler PC01 diode, and transmits it to the primary control circuit. Figure 4-8 shows the secondary control circuit for the plasma. The principle of operation of this circuit is similar to that just described above.

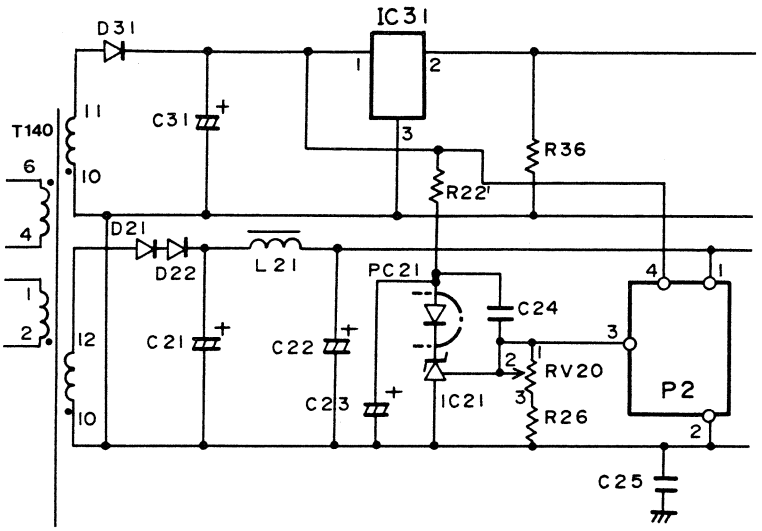


Figure 4-7 Secondary Control Circuits for Low Voltage

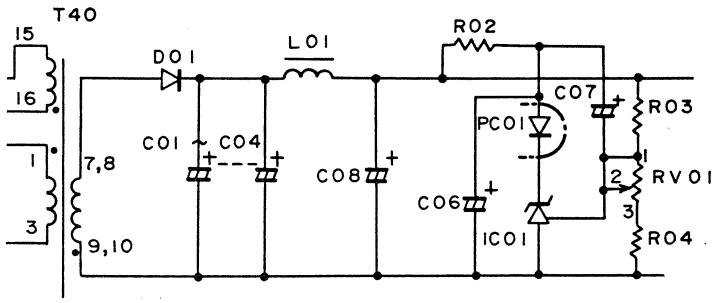


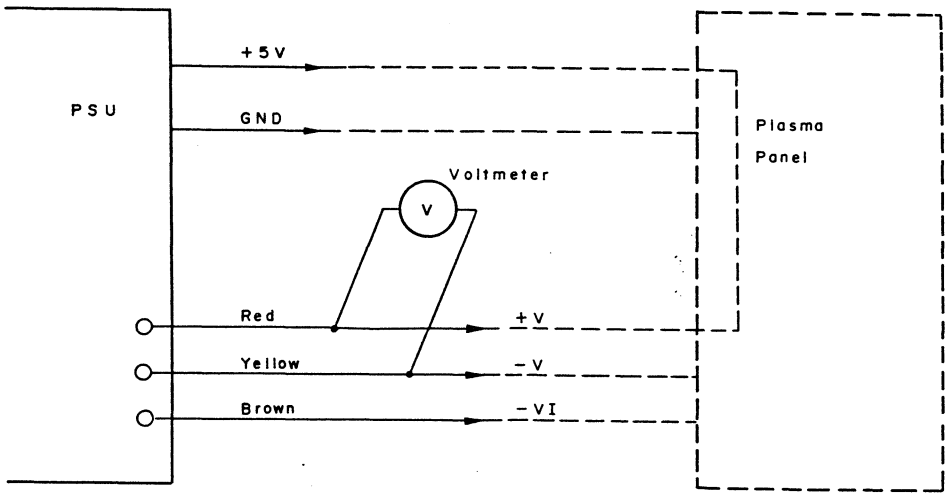
Figure 4-8 Secondary Control Circuits for Plasma

4.8 Volume Adjustment

Both the volume controls RV01 and RV20 in the secondary control circuits adjust output voltage; RV01 adjusts the +5 V low voltage output, and RV20 adjusts the -200 V output for plasma. The voltage at the connector point of the +5 V low voltage output is set at +5 V ±0.1 V: by providing all the output currents up to the rated values and by adjusting RV01. The voltage at the connector point of the 200 V plasma output is set at 205 ±1 V by adjusting RV20.

WARNING

Plasma output is shown below.
Be sure to measure the voltage between the +V and -V terminals and adjust to -205 ±1 V.



Though the voltage between +V and -V terminals is 205 V, the +V level becomes +5 V when that terminal is connected to the +5 V output through the plasma panel (-V is -200 V and -VI is -195 V).

5. TROUBLESHOOTING

This chapter describes how to shoot, analyze, and correct failures on the system.

Use the Troubleshooting Hints as an aid to analyze failure. It is recommendable to analyze the error event, environment, and peripheral circuits during troubleshooting.

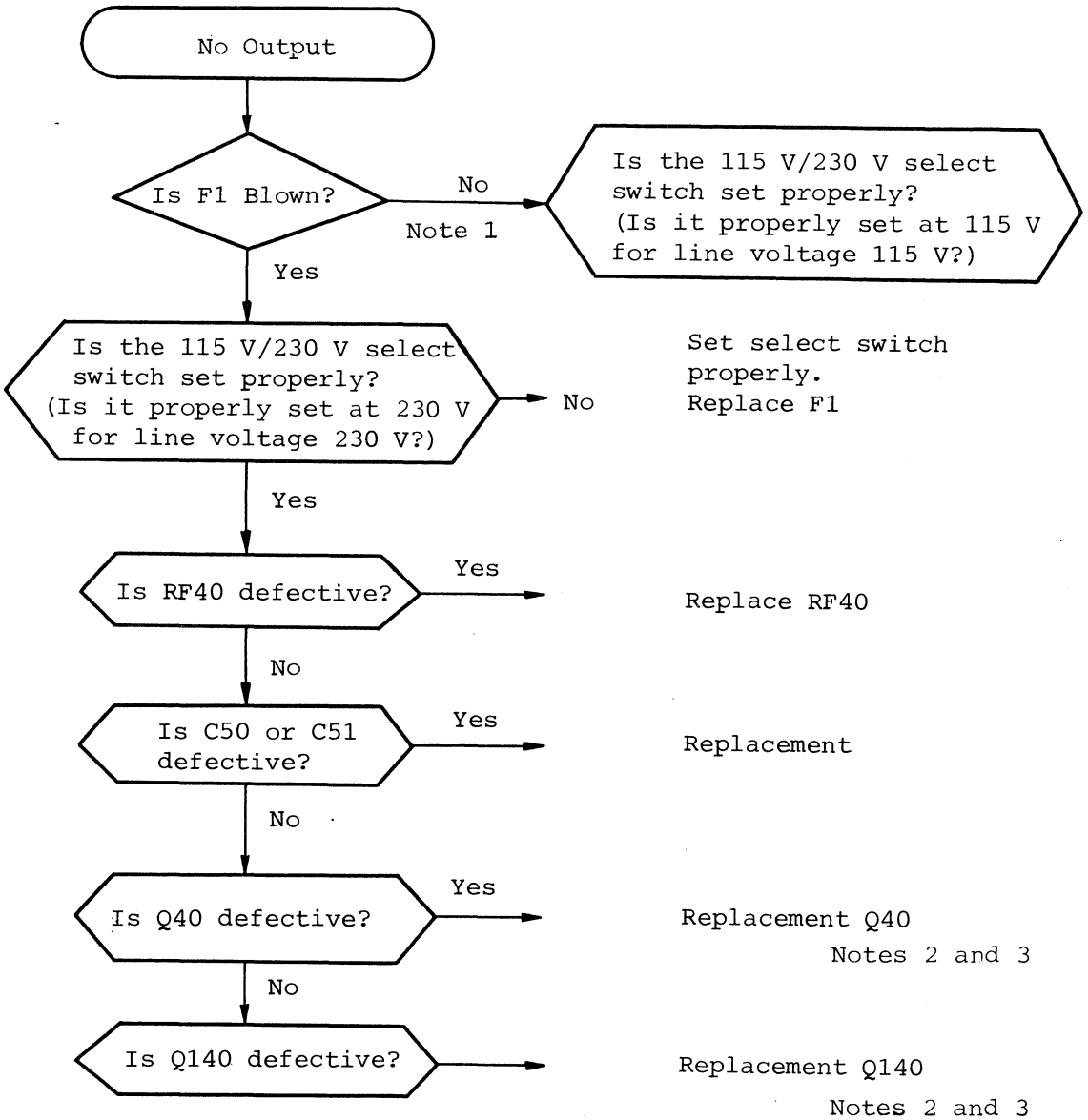
When a failure occurs on the power supply unit (PSU), the whole power-supply unit must be replaced by a new one (except a blown-fuse failure) at each service station. (The defective power supply unit must be sent back to our factory.)

When replacing blown fuses on both ① AC input (primary side) and ② DC output (secondary side) of the power supply unit, be sure to use Matsushita's genuine spare fuses.

WARNING:

This computer uses some particular parts for safety and protection. They are given international safety mark in drawings and replacement parts lists. Always use Matsushita's genuine parts to avoid unpredictable damages (electrical shock, burning, etc.).

5.1 No Output

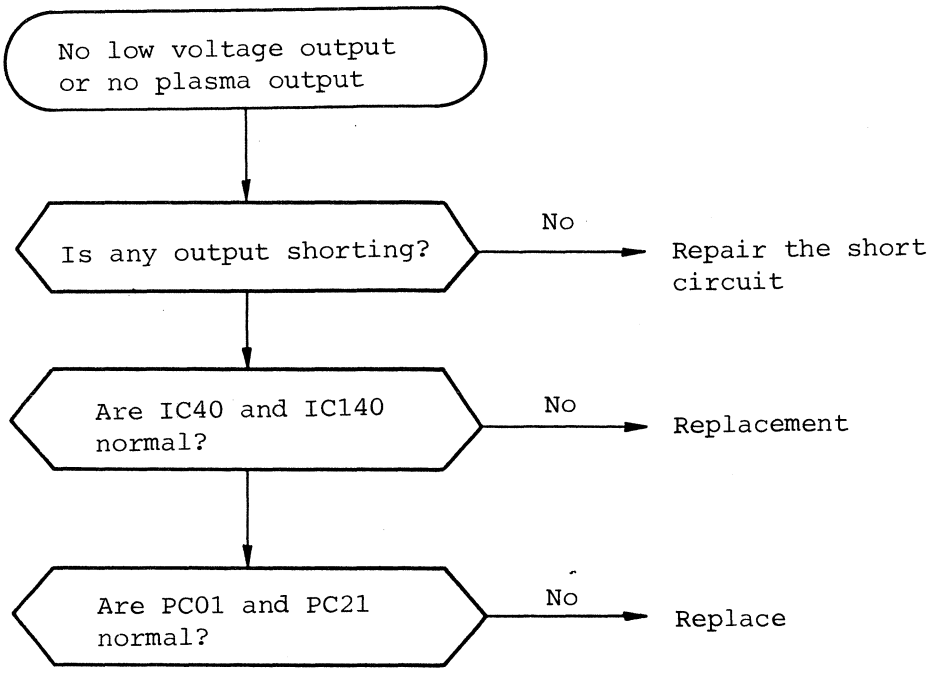


NOTES 1: When replacing fuses, use Matsushita parts with proper ratings.

2: Transistor destruction occurs when the feedback operation from the secondary side circuit does not work. Therefore the secondary side circuit and the photocoupler feedback circuit must also be checked.

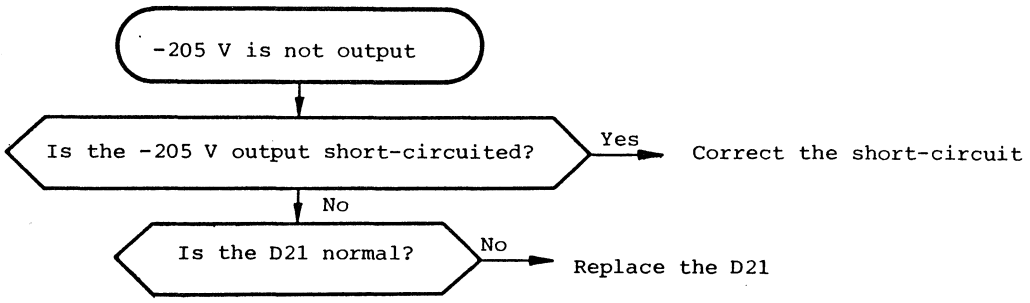
3: Transistor destruction occurs when the fan does not rotate normally. Therefore the fan rotation must also be checked.

5.2 No Low Voltage Output or No Plasma Output

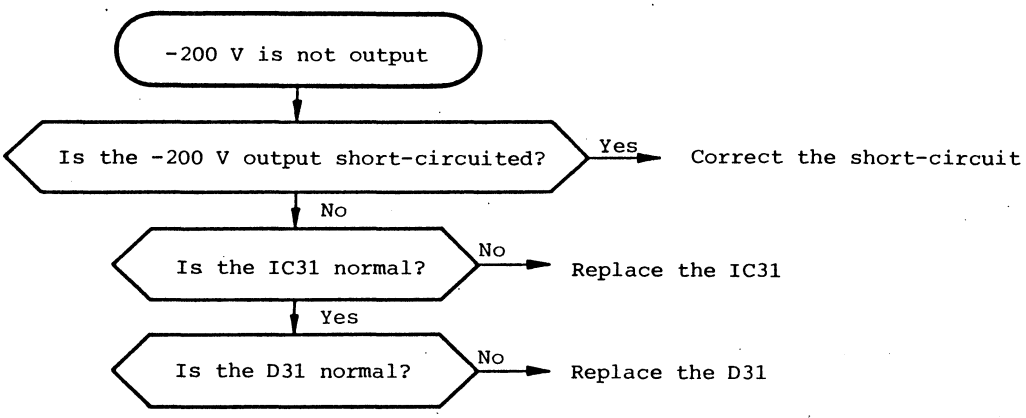


5.3 Partial Output

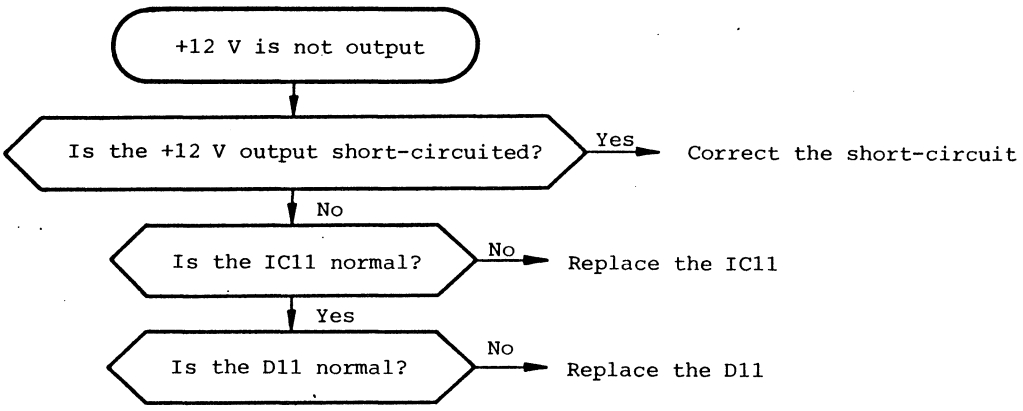
(-205 V)



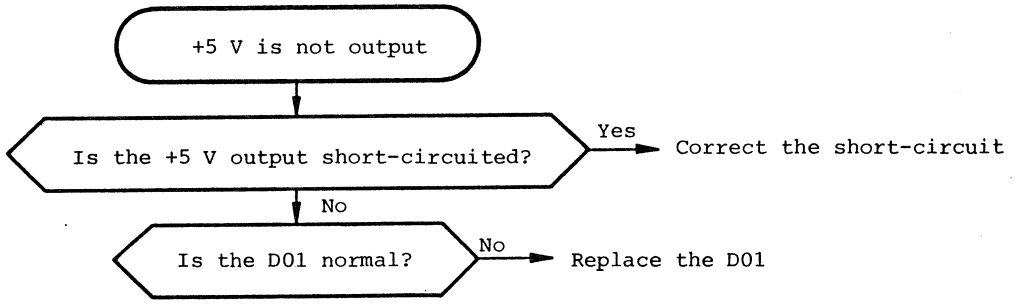
(-200 V)



(+12 V)

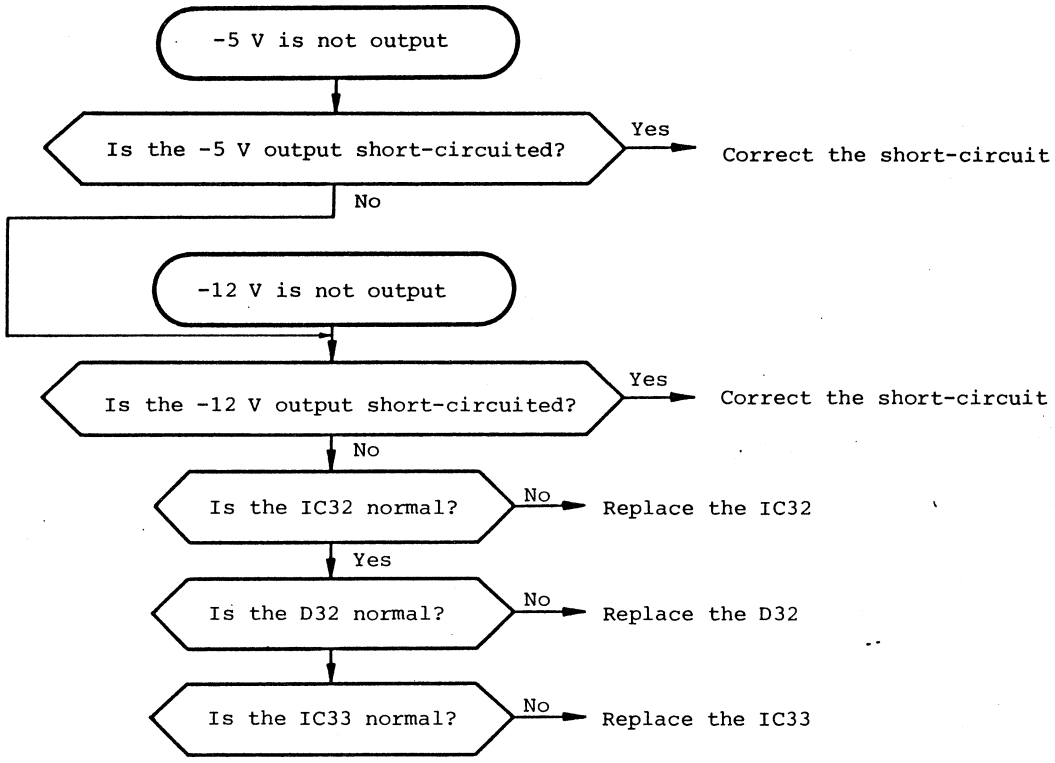


(+5 V)


+5 V is not output
Is the +5 V output short-circuited?
Yes
Correct the short-circuit
No
Is the D01 normal?
No
Replace the D01

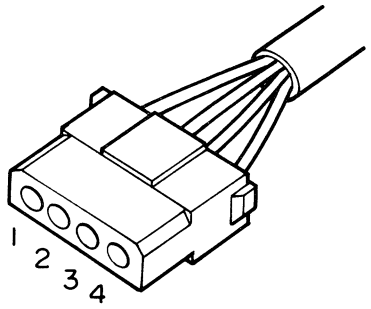
(-5 V)

(-12 V)


-5 V is not output
Is the -5 V output short-circuited?
Yes
Correct the short-circuit
No
-12 V is not output
Is the -12 V output short-circuited?
Yes
Correct the short-circuit
No
Is the IC32 normal?
No
Replace the IC32
Yes
Is the D32 normal?
No
Replace the D32
Is the IC33 normal?
No
Replace the IC33

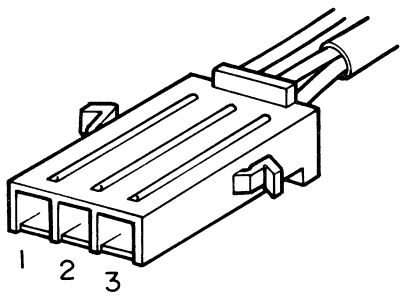
6. CONNECTORS

CN1
CN2



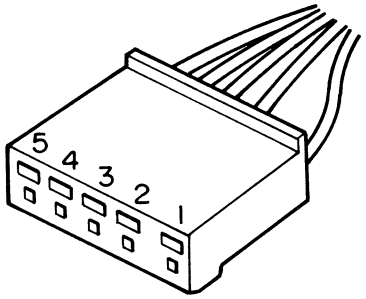
PCB side	CN side	Wire color
Pin No.	Pin No.	Center
1	1	Orange
2	2	Black
3	3	Black
4	4	Red

CN5



PCB side	CN side	Wire color
Pin No.	Pin No.	Center
1	1	Red
2	2	Yellow
3	3	Brown

CN3/CN4



CN3

PCB side	CN side	Wire color
Pin No.	Pin No.	Center
1	1	Black
2	4	Orange
3	5	Black
4	3	Red
5	2	Red

CN4

PCB side	CN side	Wire color
Pin No.	Pin No.	Center
1	3	Orange
2	1	Black
3	5	Black
4	2	Green
5	4	Blue

NOTE: CN No. is shown Power Supply Unit Parts Location.

7. REPLACEMENT PARTS LIST AND DRAWING

7.1 Exploded Drawing

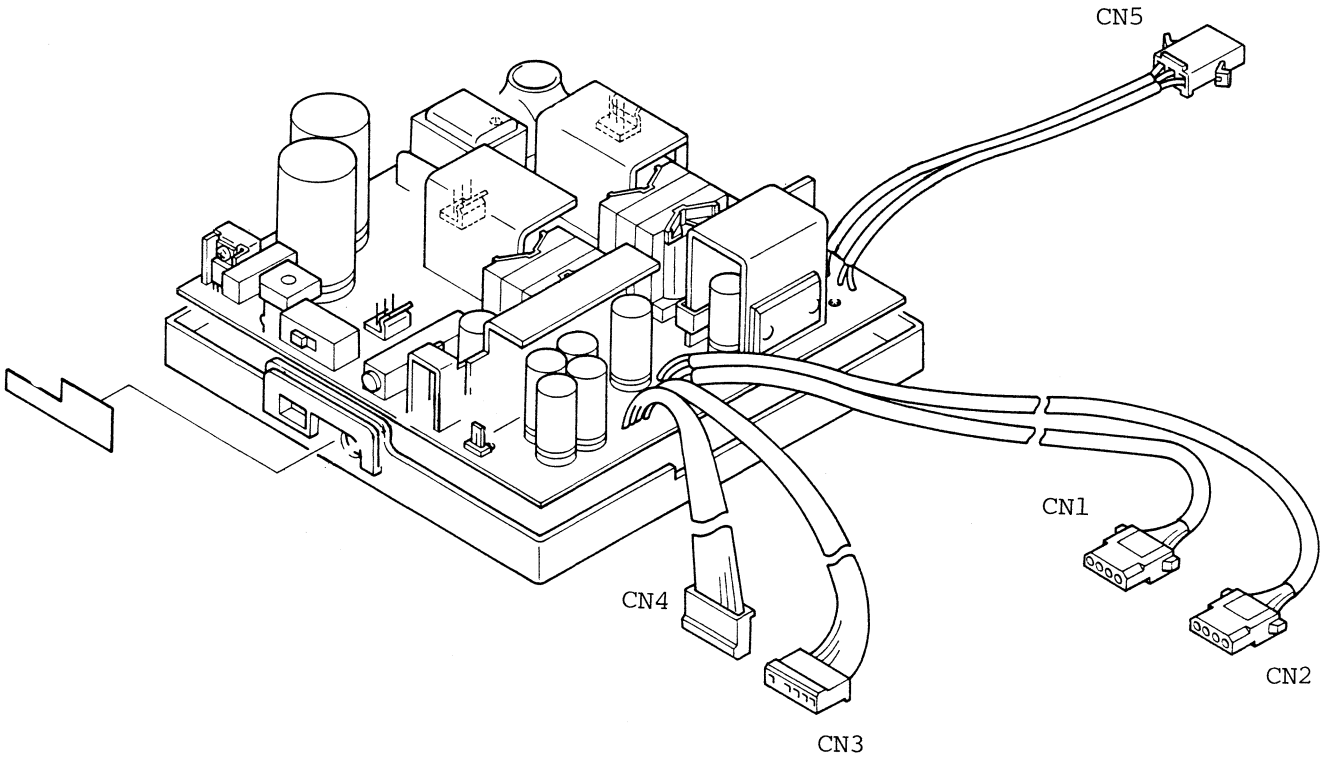


Figure 7-1 PSU Exploded View

7.2 Parts Location

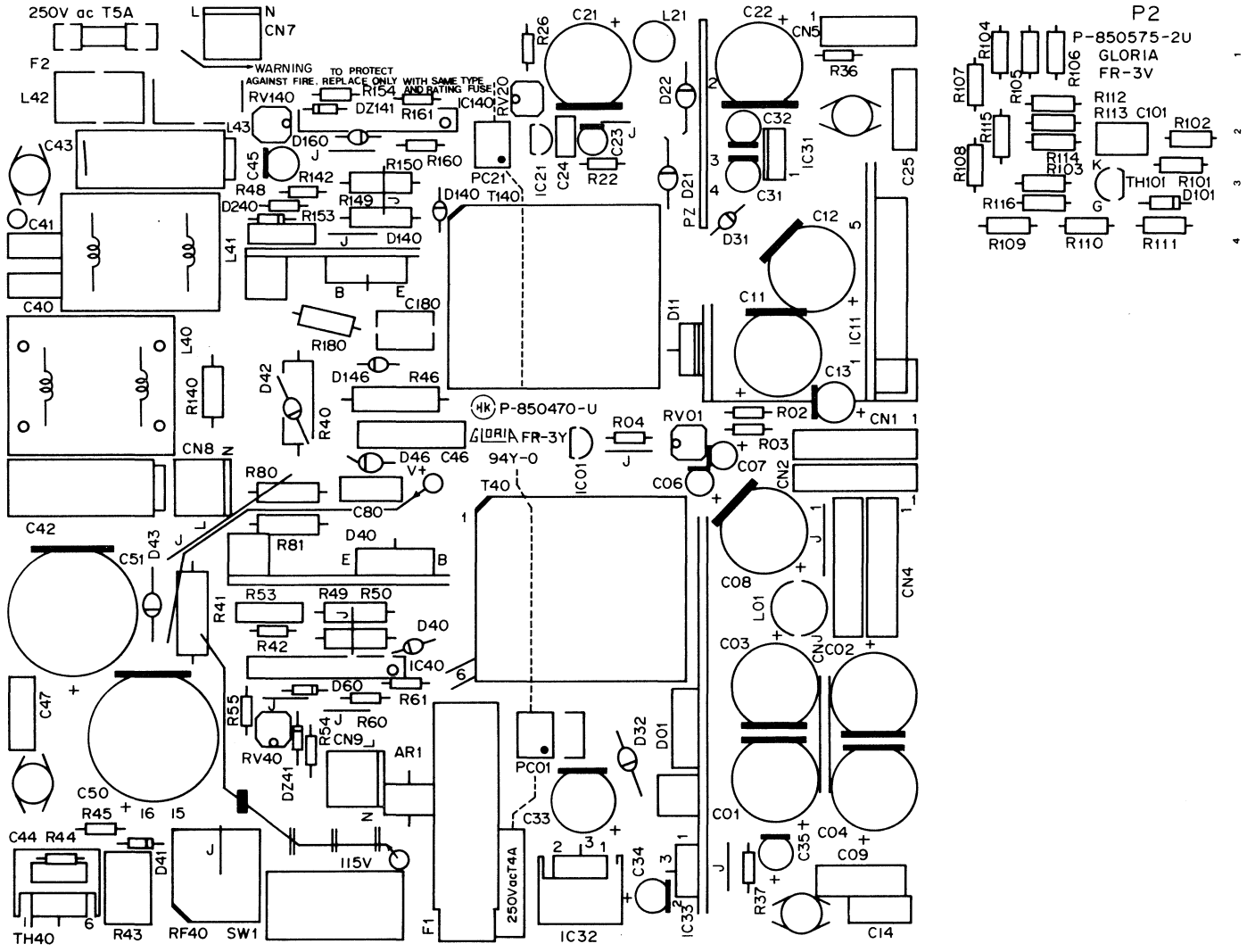


Figure 7-2 PSU Parts Location

7.3 Circuit Drawing

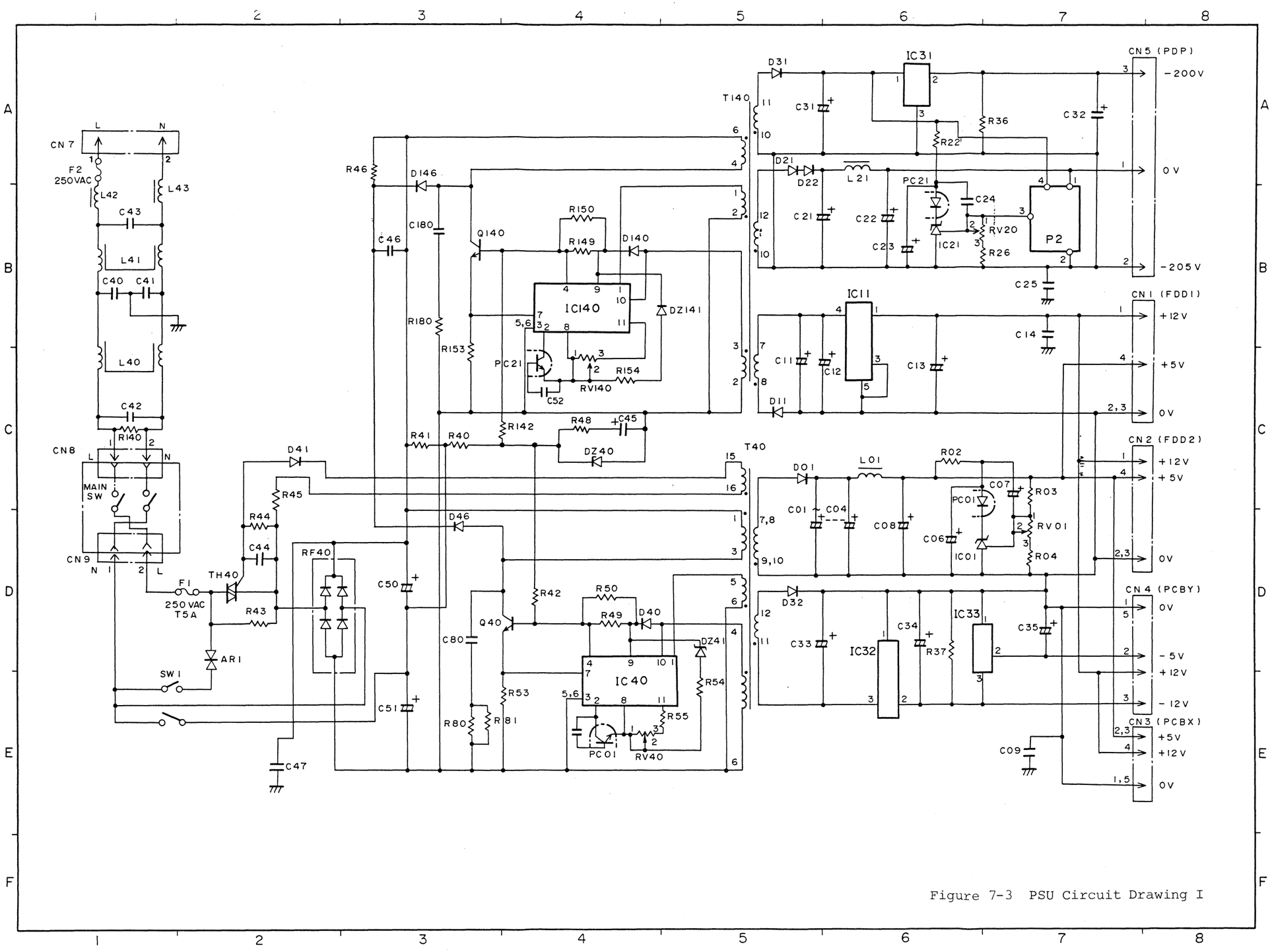


Figure 7-3 PSU Circuit Drawing I

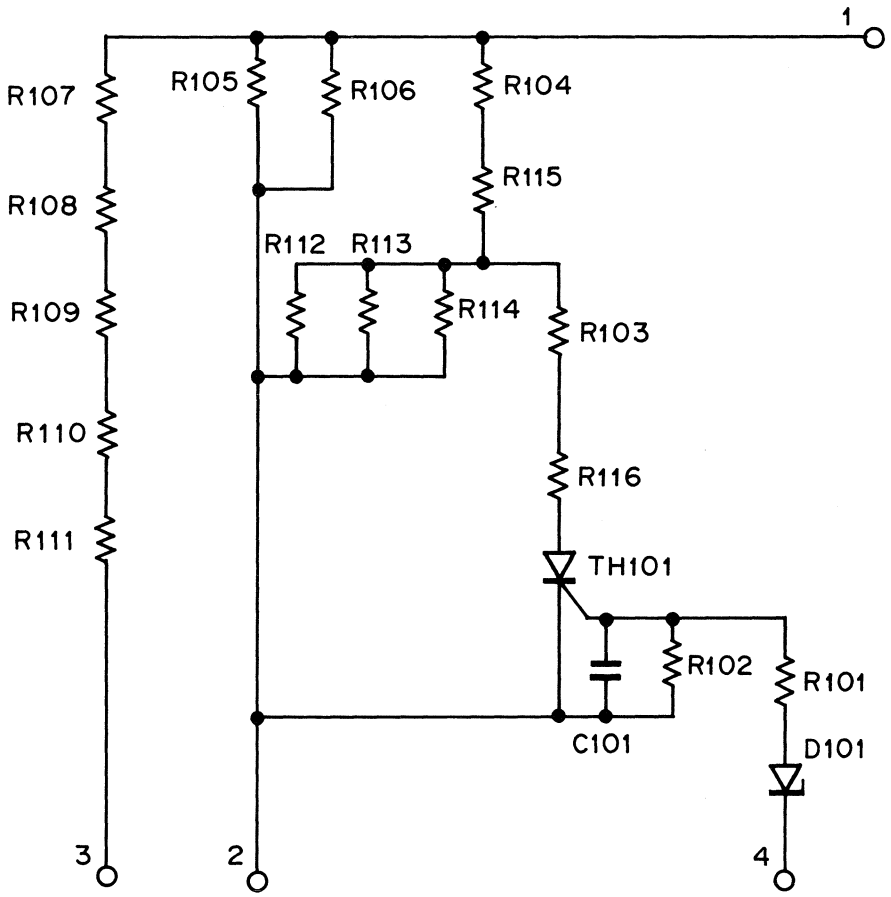


Figure 7-4 PSU Circuit Drawing II

ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

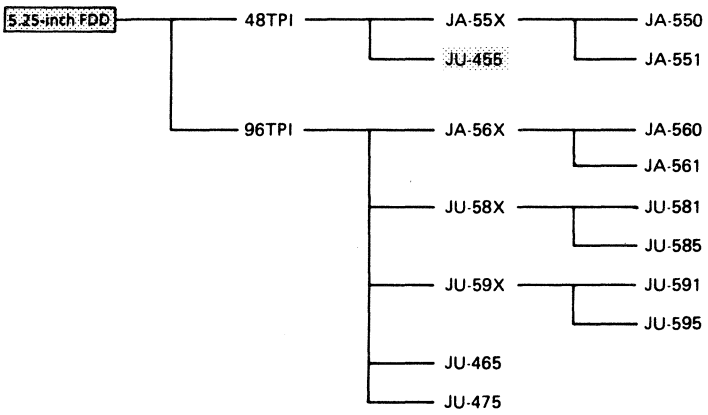
PART. I

1. INTRODUCTION

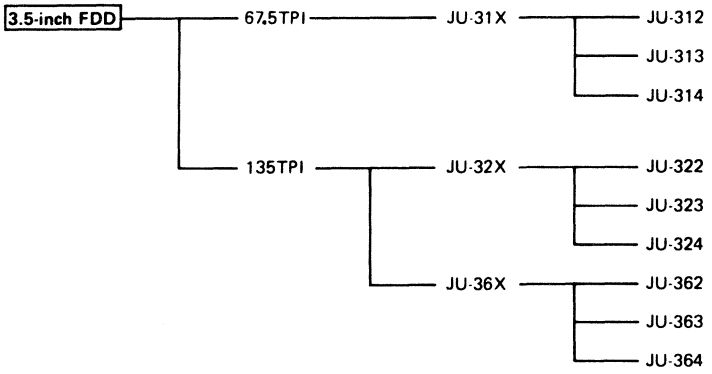
This service manual consists of two parts, Part I covering maintenance description, adjustment procedures, and trouble analysis and Part II disassembly and reassembly procedures parts list, and PCB circuits.
Part I encompasses maintenance instructions for all FDD models. Refer to the applicable items, and perform maintenance work on the FDD.

2. MODELS AND MODEL NUMBERS

2.1 5.25-inch FDD



2.2 3.5-inch FDD



3. SPECIAL TOOLS

The following special tools are used for FDD maintenance.

TABLE 3.1

Tool	Part No.				Quantity
	5.25-inch(48TPI)	5.25-inch(96TPI)		3.5-inch	
		JA-56x/JU-465	JA-58x/59x/JU-475		
Exerciser	FDD-EXT-5	※←	※←	※←	1
Alignment diskette	817-128	817-560	817-581	JU-01AA (DAD only)	1~2
Work diskette	2D	2DD	2HD	2DD	1~2
CMOS/TTL adaptor				YTFDD-CN35	1
Limmiter Adfust Tool (5.25-inch)					1
Oscilloscope (50 MHz)					1
Probe (10:1)					3
Frequency counter					1

Note: ※←: Stand for the same as left.
: DAD (Dynamic Alignment Diskette)

4. OUTLINE OF MAINTENANCE

- The following tools are required for maintenance of a Floppy Disk Drive. (FDD)

4.1 Alignment Diskette

Alignment diskette is used for head actuator alignment and index sensor adjustment.

- **Adjustments** (Refer to table 8.1)

(1) Specify an applicable model from Tabel 8.1, and make a read/write head radial adjustment at a specified track. (Sides 0,1)
(2) Make an index timing adjustment at a specified track. (Sides 0, 1)
(3) Make an azimuth measurement at a specified track. (Sides 0, 1)

CAUTION

Do not write when using alignment diskette. Check that write protect sensor is properly operating.

4.2 Exerciser

The exerciser enables you to make all adjustments and inspections necessary for an FDD. Its functions include the following:

(1) Seek increment or alternate tracks
(2) Read (but no data compare)
(3) Write 1F or 2F (All 0's or 1's)
(4) Head load (5.25-inch FDD with optional head loader)
(5) Recalibration to track 00

The exerciser has switches and indicators to execute a specified function.

5. DIAGNOSTIC PROCEDURES

5.1 Error Symptom Recognition

Errors that occur because of the wrong operating procedure, wrong programming, or use of a defective diskette, or soft errors due to external causes, such as contaminated air and random electrical noise, are often attributed to a drive failure or maladjustment.

Unless a visual inspection of the drive reveals an evident assembly fault or a defect, always confirm errors with another good diskette, and another known good drive.

5.2 Soft Error Detection and Correction

Soft errors are normally caused by the following:

(1) Contamination between read / write heads and diskette. This kind of contamination can be easily eliminated by the liner in the diskette.
(2) Random electrical noise, normally a few microseconds or less.
(3) Small defects in written data and / or track not detected during write operation may cause soft errors during read.
(4) Faulty grounding of the drive or host system can also cause a soft error.
(5) Wrong motor speed is another cause of soft errors.

Take the following steps on the controller side to recover from the soft errors mentioned above.

(1) Read the track again ten times or until the data is recovered.
(2) If Step (1) above fails to recover the data, access the adjacent. Then return the head to the original track.
(3) Repeat Step (1).
(4) Any error that cannot be corrected by the above procedure is irrecoverable.

5.3 Write Error

If an error occurs during write operation, it is usually detected during the next revolution by performing a read operation called write check. To correct an error, write again and repeat a write check operation. If the result is unsatisfactory after ten or more write operations, perform a read operation on another track to determine whether it is the diskette or the drive that is wrong. If an error persists, replace the diskette and repeat the above procedure.
If the error still persists, consider the drive defective. If the error is corrected, dispose of the diskette as defective.

5.4 Read Error

Most read errors are soft errors. Data can be recovered by following the recovery procedure mentioned in 5.2.

5.5 Seek Error

(1) Stepper motor or stepper motor drive circuit is faulty.
(2) **Faulty carriage**
There are two ways of seek error recovery. One is to recalibrate to track 00, and seek back to the original track. The other is to read the ID field, check the track number on which the head is located, and move the head away from it. And read it again.

5.6 Compatibility Error

The data which is written by one drive may not be read by another. This error is called a compatibility error, which can be caused mostly by the following. The check points are also mentioned below:
(1) Head misalignment: Refer to (Adjustments and Confirmation Item 9.5)
(2) Head output too low: Refer to (Adjustments and Confirmation Item 9.3)
(3) Motor speed difference: Refer to (Adjustments and Confirmation Item 9.1)

6. TROUBLE ANALYSIS

To determine the cause of trouble whether it lies in the FDD, diskette, or controller, replace the disk and FDD with good ones. If the FDD is assumed faulty as a result, follow the procedure below.

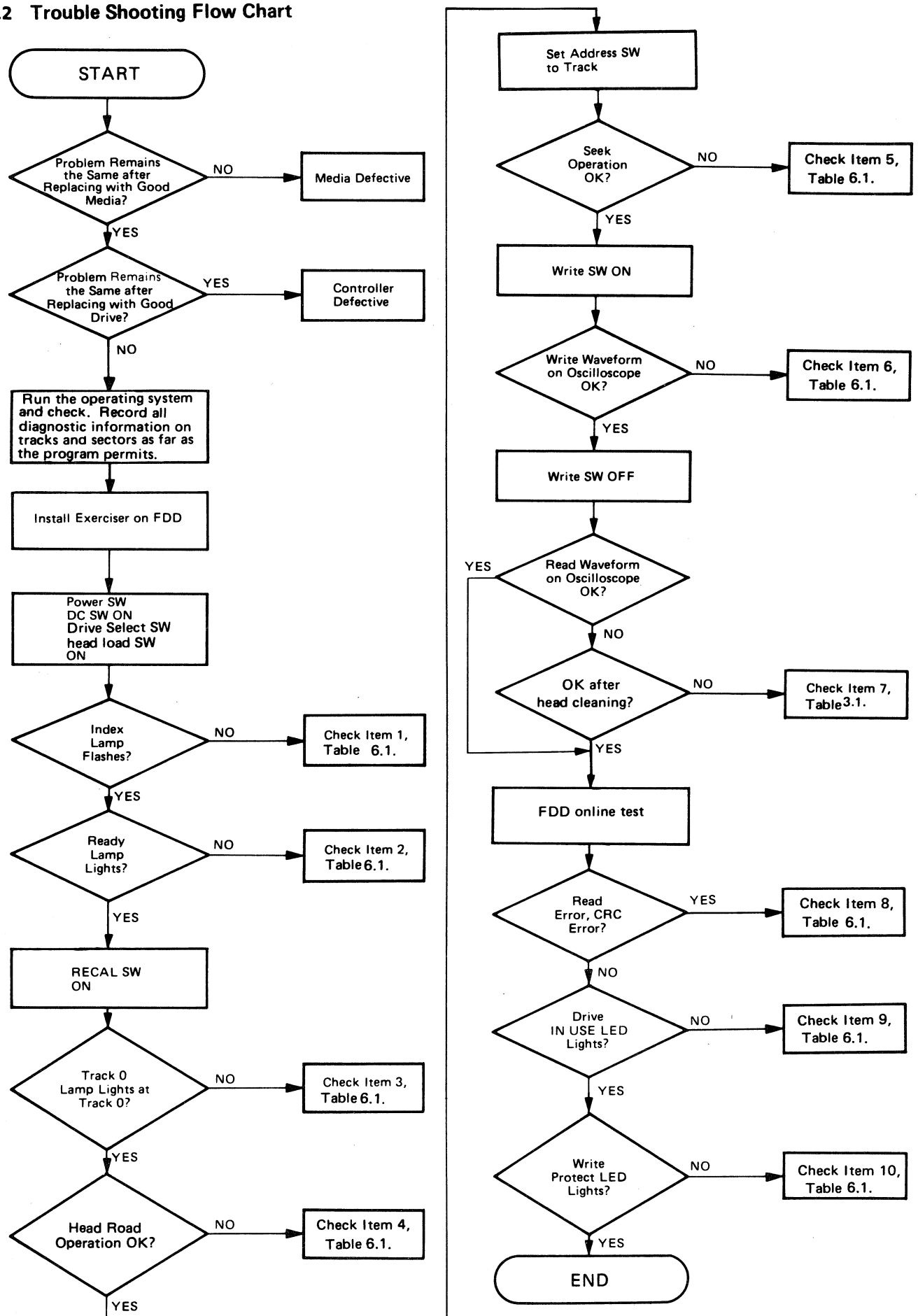
6.1 Trouble Analysis Procedure

FDD trouble may occur in any of the following ten forms.
(1) Index detection failure
(2) Not ready
(3) Track 0 undetectable
(4) No seek
(5) No write
(6) No read
(7) Read error
(8) IN USE LED won't light.
(9) Write protect undetectable
(10) No head load (5.25-inch FDD with optional head loader)

Check with the troubleshooting flowchart in 6.2.

CAUTION:
Be sure to switch power off before removing an FDD or PCB from the operating system.

6.2 Trouble Shooting Flow Chart



6.3 Trouble Analysis Table

Table 6.1

Item	Trouble	No.	Cause	5.25-inch	JU-3x3, 3x4	JU-3x2
1	Index detection failure	1	Collet part faulty	Replace		
		2	DD motor control PCB	Replace	Replace DD motor, Base assembly	Replace DD motor assembly
		3	DD motor faulty	Replace		
		4	Index LED faulty	Replace	Replace DD motor, Base assembly	Replace
		5	Index detector faulty	Replace		
		6	Index LED/index detector installation faulty	Adj.		
		7	PCB motor ON circuit	Repair	※ ←	※ ←
		8	PCB index detection circuit	Repair	※ ←	※ ←
2	Not ready	1	See Item 1.			
		2	PCB ready circuit	Repair	※ ←	※ ←
3	Track 0 detection failure	1	Track 00 assembly	Replace	※ ←	※ ←
		2	PCB track O detection failure	Repair	※ ←	※ ←
4	No head loading	1	See Item 1.			
		2	See Item 2.			
		3	HDL solenoid	Replace		
		4	PCB HDL circuit	Repair	※ ←	※ ←
5	No seek	1	Stepper motor	Replace	※ ←	※ ←
		2	Guide shaft contamination or damaged	Replace	※ ←	※ ←
		3	PCB stepper driver circuit	Repair	※ ←	※ ←
6	No WRITE	1	See Item 1.			
		2	See Item 4.			
		3	Head disconnected	Replace	※ ←	※ ←
		4	Head shorted	Replace	※ ←	※ ←
		5	HDL bail height wrong	Adj.		
		6	PCB write circuit	Repair	※ ←	※ ←
7	No READ	1	See Item 1.			
		2	See Item 4.			
		3	See Item 6.			
		4	PCB read circuit	Repair	※ ←	※ ←
8	READ ERROR	1	See Item 1.			
		2	See Item 4.			
		3	See Item 7.			
		4	Alignment	Adj.	※ ←	※ ←
		5	Azimuth	Unadjustable	※ ←	※ ←
		6	Burst	Adj.	Unadjustable	Unadjustable
		7	Asymmetry	Adj.	Adj.	
		8	Limiter	Unadjustable	Adj.	Adj.
		9	Flag 0	Adj.	※ ←	※ ←
		10	HDL time	Adj.		
		11	Index period	Adj.	Replace DD motor, Base assembly	Replace
		12	PCB read circuit	Repair	※ ←	※ ←
9	IN USE LED won't light.	1	LED part	Replace	※ ←	※ ←
		2	PCB IN USE circuit	Repair	※ ←	
10	Write protect failure	1	Write protect part	Replace	Replace DD motor, Base assembly	Replace
		2	Write protect circuit		※ ←	※ ←

Note: ※←: Stand for the same as left.

7. PREVENTIVE MAINTENANCE

No preventive maintenance is necessary for any type of FDDs under normal conditions of use.

8. MEASUREMENT ITEMS FOR EACH MODEL

Table 8.1

Item	Parameter	JU-312, 313, 314		JU-32X, 36X		JU-581, 585	
		TRK	Value	TRK	Value	TRK	Value
1	Index period	20	200 ± 3ms	40	200 ± 3ms	32	166.7 ± 0.2 ms
2	Output level	39	160 mV or more	79	180 mV or more	76	120 mV or more
3	Radial Alignment	20	75%	40	50%	32	70%
4	AZIMUTH	20	± 18'	40	± 18'	68	± 18'
5	Index burst	20	3 ± 1.5ms	40	3 ± 1.5ms	68	200 ± 200 µs
6	FLAG 0	From track 1 to track 2 and back	1:1	From track 1 to track 2 and back	1:1	From track 2 to track 3 and back	1:1
7	Limiter	− 1	Recalibrate and return to 0	− 1	Recalibrate and return to 0	− 1	Recalibrate and return to 0
8	Asymmetry	39	<600ns	79	<600ns	76	<350 ns
9	Head load time						<50 ms

Item	Parameter	JU-591, 595, 475		JU-455/465		JU-455-5	
		TRK	VALUE	TRK	Value	TRK	Value
1	Index period	32	166.7 ± 0.2 ms (High) 200 ± 0.2 ms (Low)	16/32	200 ± 0.2 ms	16	200 ± 0.2 ms
2	Output level	76	120 mV or more	39/79	140/120 mV or more	39	140/ mV or more
3	Radial Alignment	32	70%	16/32	70%	16	70%
4	AZIMUTH	68	± 18'	34/68	± 18'	34	± 18'
5	Index burst	68	200 ± 200 µs	34/68	200 ± 200 µs	34	200 ± 200 µs
6	FLAG 0	From track 2 to track 3 and back	1:1	From track 1 to track 2/track 2 to track 3 and back	1:1	From track 2 to track 3 and back	1:1
7	Limiter	− 1	Recalibrate and return to 0	− 1	Recalibrate and return to 0	− 1	Recalibrate and return to 0
8	Asymmetry	76	<350 ns	39/79	<600 ns	39	<600 ns
9	Head load time		<50 ms		<50 ms		

9. ADJUSTMENTS AND VERIFICATIONS

9.1 Motor Speed Adjustment and Verification (Index Period)

(1) Insert a diskette, run the motor, and clamp. Refer to the index period column of Table 8.1 for the applicable model.
(2) Step to the specified track.
(3) Connect a frequency counter to the INDEX signal.
5.25-inch: TP7
3.5-inch: IX
(4) Check that the frequency counter readings meet the specifications in the table.
(5) **Adjustment**
5.25-inch: Turn the speed control potentiometer on the motor control circuit board until the specificatisons are satisfied.
3.5-inch: No adjustment

9.2 Write Protect Verification

(1) Check that the exerciser's write protect lamp goes on and off as a media is inserted and removed as specified in the table below.

	Media with write protect hole open	Media with write protect hole closed
5.25-inch	OFF	ON
3.5-inch	ON	OFF

9.3 Head Output Verification

Use a new diskette if possible to identify head failure for this check.
(1) Insert a good diskette.
(2) Run the motor.
(3) Step to the track specified in the output level column of **Table 8.1.**
(4) Connect the oscilloscope probe as specified below.

	CH1	CH2	EXT
5.25-inch	TP1	TP2	TP7
3.5-inch	T1	T2	IX (INDEX)

Invert channel 2 and select the Add mode.
Set vertical deflection to 10 mV/division and horizontal deflection to 20 ms/division.
(5) Write 2F (all ones) on the entire circumference.
(In case of a double-sided FDD, repeat it on sides 0 and 1 using SIDE SELECT.)
(6) Check that the average output level meets the specifications of **Table 8.1**. If it does not meet the specifications, refer to Item 7 of the Trouble Analysis Table.

9.4 Output Modulation Verification

Modulation: M is calculated by the following formula.

$$M(\%) = \frac{Vmax - Vmin}{Vmax + Vmin} \times 100$$

using the value obtained in **9.3**, and check that the calculated value is 20% or less.

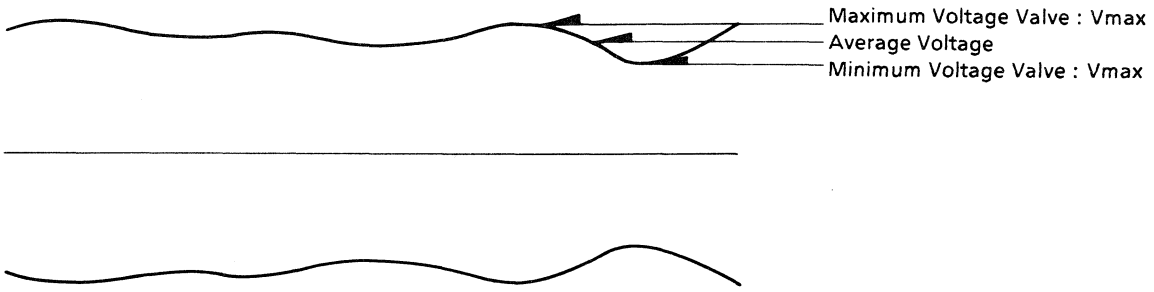


Fig. 9.1 Modulation

9.5 Radial Alignment Adjustment

Introduction

This adjustment is normally not necessary.

If the mounting screws for the stepper motor loosen, or if parts become defective, or if a compatibility error occurs, check and readjust according to the following procedure.

Steps (4) to (9) should be performed regardless of the type, CE or DAD alignment diskette used. Use an alignment diskette suitable to the type of FDD to be adjusted according to table 3.1.

(1) Insert an alignment diskette.

CAUTION:

Be sure to leave the alignment diskette under room conditions for 20 minutes before adjustment.

(2) Step to the track specified in the Radial alignment column of **Table 8.1**.

(3) Leave the oscilloscope in the same condition as mentioned in section 9.3.

- **Cats Eye System** 5.25-inch

(4) Check the output waveforms for sides 0 and 1. They should appear as in **Fig. 9.2.**

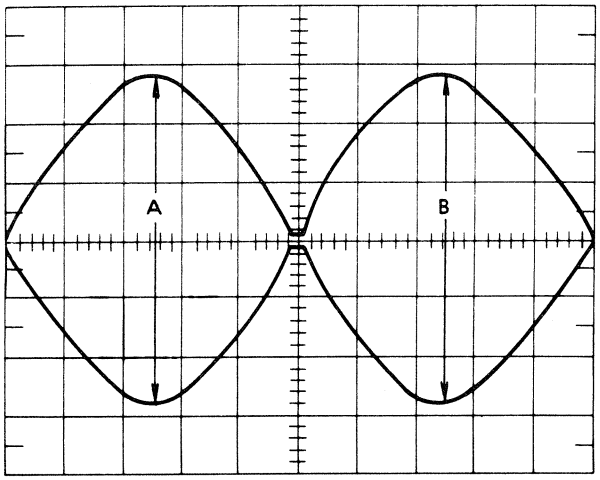
(5) The two waveforms should appear in the amplitude ratio in the R/A column of Table 8.1 or better.

(6) If the specified ratio is not satisfied, loosen the two mounting screws for the stepper motor.

(7) Move the stepper motor along the base by hand until the two waveforms assume approximately the same amplitude, and retighten the mounting screws. (See **Fig. 9.2.**)

(8) Step the head outward (track 0) and inward (track 40 or 79), and confirm that the adjustment has been completed.

(9) After the radial adjustment, be sure to confirm track 00 sensor adjustment **9.8** and carriage limiter **9.9.**



$A > B \quad : \frac{B}{A} \times 100$

$B > A \quad : \frac{A}{B} \times 100$

Fig. 9.2 Radial Alignment Waveforms (CATS EYE)

Note: Sides 0 and 1 are adjusted to agree at the factory. If they disagree, adjust them to meet the specifications of Table 8.1

- **DAD (Dynamic Alignment Diskette) 3.5-inch**

(4) Watch the output waveforms for sides 0 and 1. They should appear as shown in **Fig. 9.3**.

(5) Measure the timing levels A1 to A4 and B1 to B4 in **Fig. 9.3**, and calculate the lobe ratio from the following formulas.

$$\Sigma A > \Sigma B : \frac{\Sigma B}{\Sigma A} \times 100\% \qquad \Sigma A < \Sigma B : \frac{\Sigma A}{\Sigma B} \times 100\%$$

(6) The lobe ratio calculated by the above formulas should meet the specifications on item 3 of Table 8.1.

(7) If the above requirement is not met, loosen the two mounting screws for the stepper motor, adjust.

(8) Seek from track 0 to track 40 and from track 79 to track 40, and confirm that the adjustment has been completed.

(9) After the radial adjustment, be sure to confirm track 00 sensor adjustment **9.8** and head carriage limiter **9.9**.

Note: An alignment instrument for 3.5-inch FDDs permits accurate and easy adjustment because the lobe ratio is displayed on the instrument.

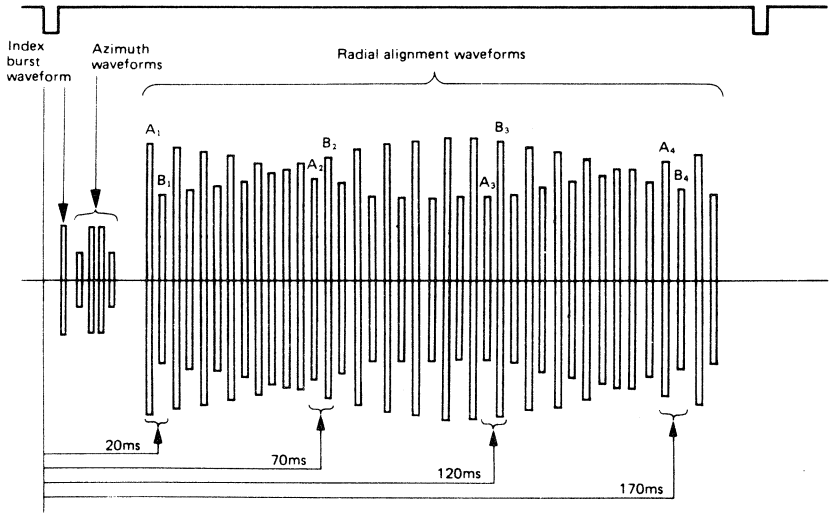
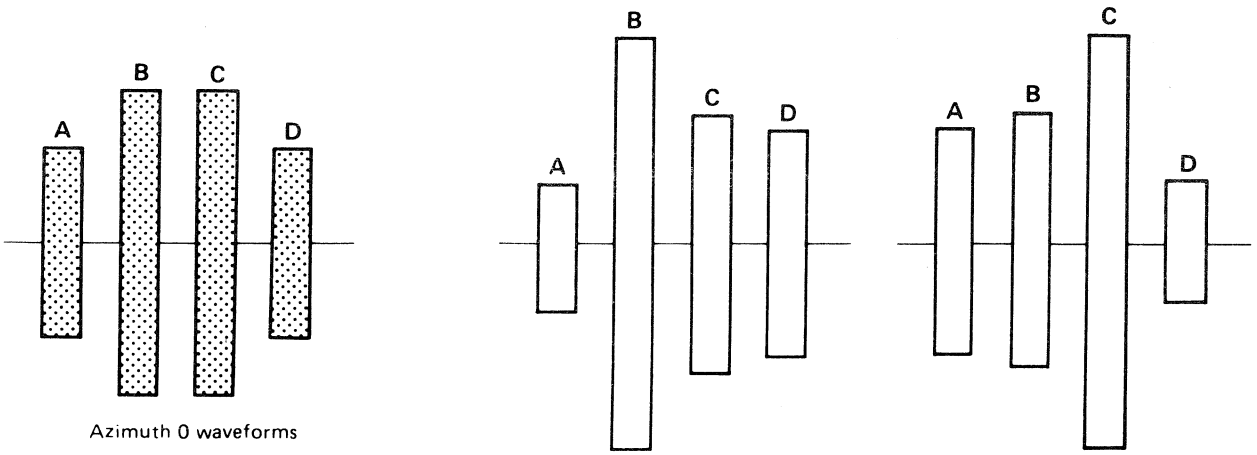


Fig. 9.3 Alignment Waveform (DAD)

9.6 Azimuth Verification

(1) Insert an alignment diskette. Seek to the track specified in the azimuth column of **Table 8.1**.
(2) Set the oscilloscope in the same conditions as in **8.3**, and set horizontal deflection to 0.5 ms/division.
(3) Measure as shown below.
(4) Confirm that the measured value meets the specifications in the azimuth column of **Table 8.1**.



Case of B > C

$$\text{Azimuth} = \frac{B - C}{B - D} \times (A)$$

3.5-inch (A) : CE → 30′
DAD → 15′

Case of B < C

$$\text{Azimuth} = \frac{C - B}{C - A} \times (A)$$

5.25-inch (A) : 12′

Fig. 9.4 Azimuth Waveforms

9.7 Index Burst Verification

(1) Insert an alignment diskette. Seek to the track specified in the I/B column of **Table 8.1**.
(2) Set the oscilloscope time base as follows:
5.25-inch: 50 μs/division
3.5-inch: 1 ms/division
(3) Check that the time from oscilloscope start to the first data pulse meets the I/B specifications of **Table 8.1**. (DAD system)
(4) If the specifications are not met, adjust as follows. (No adjustment necessary for 3.5-inch models)
- Loosen the index detector mounting screws enough to free the assembly.
- Adjust the timing to 200 ± 200 μsec.
- Retighten the screw.
- Check the timing again.

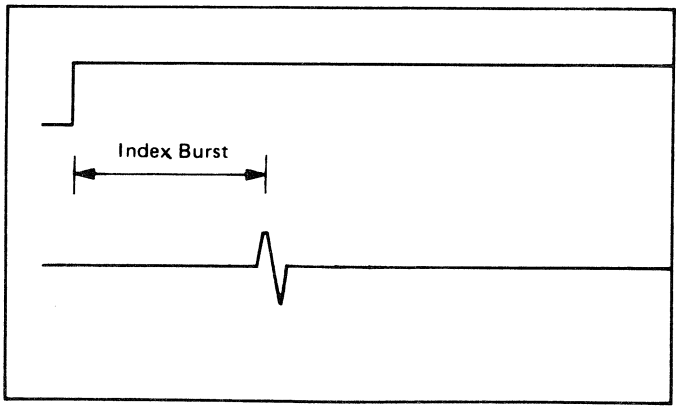


Fig. 9.5 Index Timing

9.8 Track 00 Sensor Adjustment

(1) Set the oscilloscope as follows.
Set horizontal deflection to 1 ms/division.

	CH1	EXT
5.25-inch	TP-8	TP-12
3.5-inch	ZP	SP

(2) Step between specified tracks at in the FLAG 0 item of Table 8.1 (Turn the seek delay switch on the exerciser to adjust 12 ms seek.)

(3) Loosen the track 0 sensor screw and adjust until the waveform on the oscilloscope appears as shown in **Fig. 9.6.**

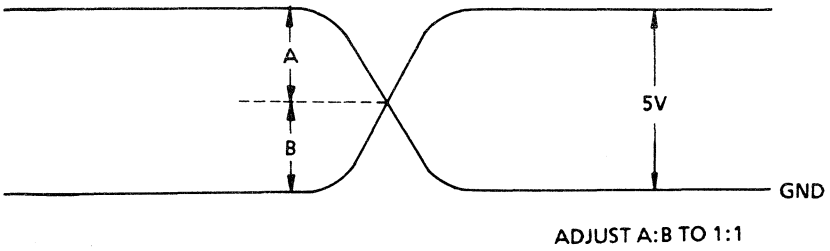


Fig. 9.6 Track 0 Waveform

9.9 Limiter Verification (5.25-inch)

(a.) Seek to track 00.

(b.) Push the carriage outward until it contacts the limiter, and recalibrate.
Make sure that the carriage moves inward and returns to track 00.

(c.) If the carriage does not return to track 00 in Step (b), or if it contacts the limiter of the stepper motor, the stepper motor assembly must be replaced because adjustment is useless.

9.10 Limiter Adjustment (3.5-inch)

(1) Seek to track 0.

(2) Write 2F data on track 0, and measure read level.

(3) Loosen the limiter mounting screw to free the limiter.

(4) Move the limiter until it just touches the head carriage on −1 track, and retighten the limiter mounting screw securely.

(5) Check that, when the RECAL switch on the exerciser is pushed ON, the head returns to track 0 and that the 2F output level is the same as that measured in Step (2).

9.11 Asymmetry Verification

(1) Insert a work diskette.

(2) Step to the track specified in the symmetry item of **Table 8.1**.

(3) Set the oscilloscope as follows:

	CH1	CH2
5.25-inch	TP-6	TP1
3.5-inch	RD	T1

(4) Write 1F.
(5) A read wave form is displayed on the oscilloscope as shown in **Fig. 9.7.**
(6) Confirm if it satisfies the value as shown in Fig. 8.1.

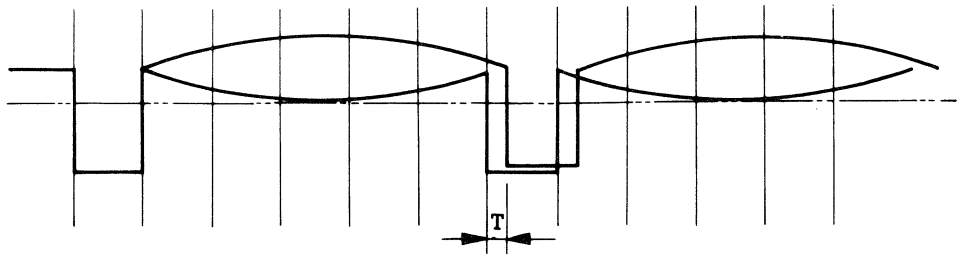


Fig. 9.7 Asymmetry Waveform

10. PANASONIC ALIGNMENT DISKETTE

Table 10.1. 5.25 inch Alignment Diskette

TPI	P/N		Index Burst	Azimuth	Radial	MODEL
48	817-128		34TRK	34TRK	16TRK	JA-55X JU-455
96	817-560		68TRK	68TRK	32TRK	JA-56X JU-465
96	817-581		68TRK	68RTRK	32TRK	JU-475 JU-58X JU-59X
100	817-570		61TRK	61TRK	36TRK	JU-570

Table 10.2. 3.5 inch Alignment Diskette

TPI	P/N		Index Burst	Azimuth	Radial	MODEL
67.5	JU-01AA		20	20	20	JU-31X
135	JU-01AA		40	40	40	JU-32X JU-36X

PART. II
11. REMOVALS AND INSTALLATIONS

11.1 PCB Removal and Installation (See Fig. 11.1)

(1) Remove the two printed circuit board mounting screws.
(2) Disconnect the connectors (J3 CON, J4 CON, J6 CON, J5 CON,J8CON) from the printed circuit board.
(3) Remove the printed circuit board by sliding it aslant.
(4) To reinstall, reverse the above procedure.
(5) Readjustment is not necessary after printed circuit board replacement.

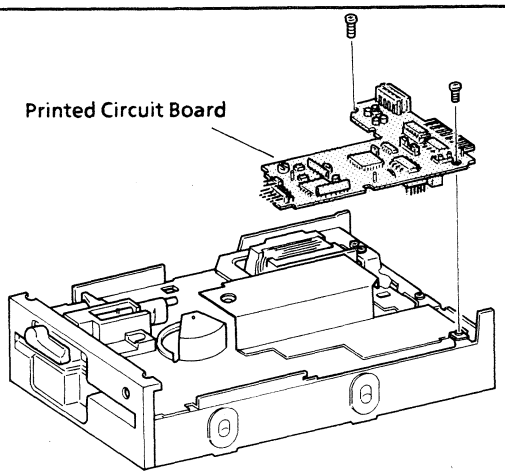


Fig. 11.1 Printed Circuit Board Removal

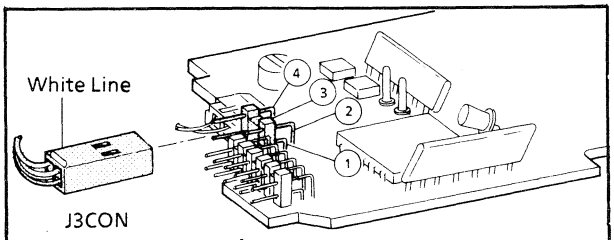


Fig. 11.1-1

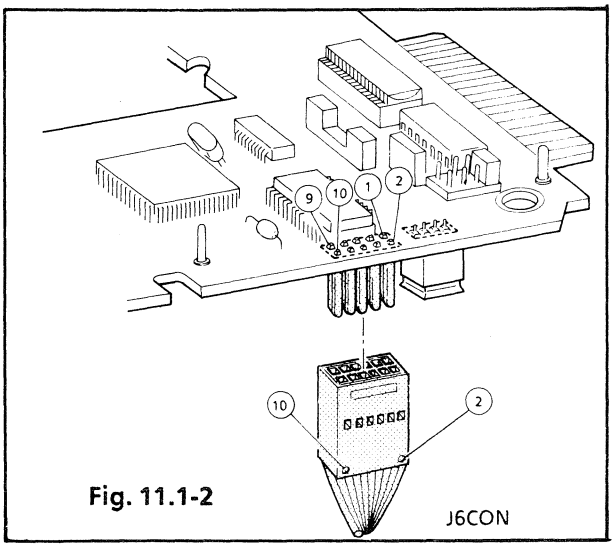


Fig. 11.1-2

Note:
Reverse connection prevention pin is not provided in J3 and J6. When installing the P.C.B. board, connect them so that the white line on the J3 connector is facing upwards and J6 connector pin No. matches the P.C.B. side pin No.

11.2 Front Plate Removal and Installation (See Fig.11.2)

(1) Operate the lock cam of the clamp assembly, and turn the clamp handle in the direction of clamping.
(2) Remove the clamp handle.
(3) Remove the two front plate mounting screws, and take off the front plate.
(4) Reverse the above procedure to reinstall.

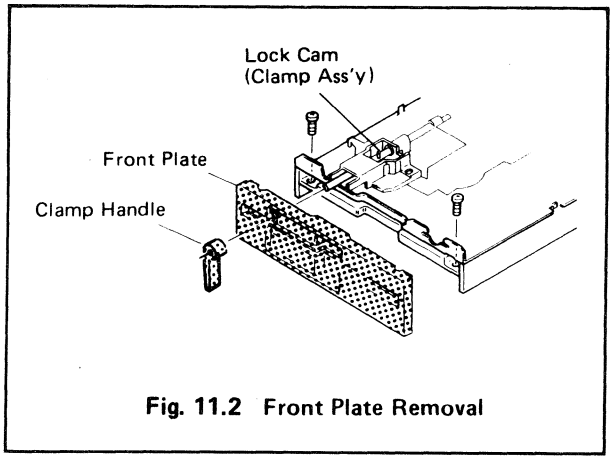


Fig. 11.2 Front Plate Removal

11.3 Track 00 Assembly Removal and Installation (See Fig. 11.3)

(1) Remove the track 00 assembly mounting screw and take out the track 00 assembly.
(2) Pull out the white, yellow, and green wires from J6 CON (10P).
(3) Reverse the above procedure to reinstall.
(4) After reinstallation, adjust the track 00 sensor as described in 9.8.

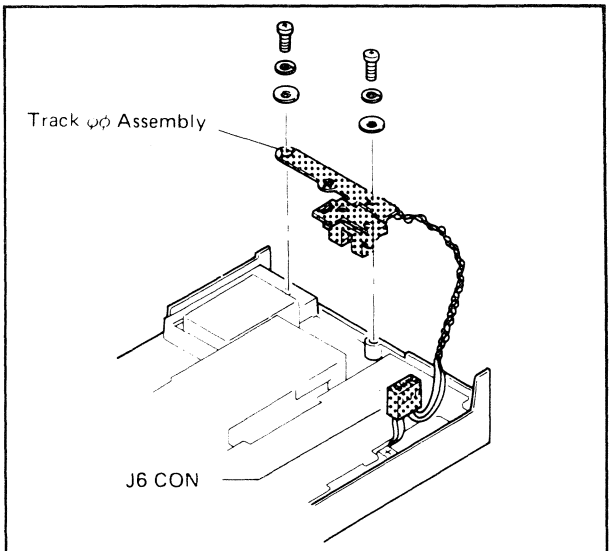


Fig. 11.3 Track 00 Assembly Removal

11.4 Collet Assembly Removal, Installation, and Adjustment (See Fig.11.4)

(1) Remove the Cartridge Guide Assembly as described in 11.7
(2) Remove the lifter spring from the lifter.
(3) Remove the E-ring from the lifter shaft.
(4) Remove the lifter from the Cartridge Guide.
(5) Remove the Collet Assembly from the Guide shaft.
(6) Reverse the above procedure to reinstall.
(7) After reinstallation, perform collet assembly center adjustment.
(8) Collet assembly center adjustment.
   a) Temporarily fasten the Cartridge Guide Assembly.
   b) Insert a diskette or dummy diskette and clamp it.
   c) Clamp repeatedly a few times to find a good fit between the collet and the inside diameter of the DD motor.
   d) Bind the screw of the Cartridge Guide.
   e) Check step c) again, if not good repeat steps a) through d) until the correct center adjustment is achieved.

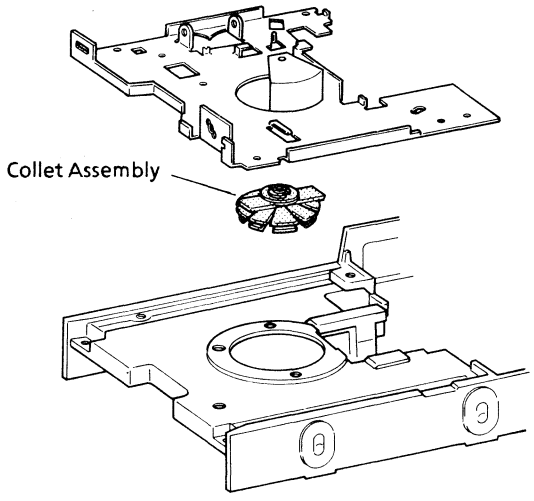


Fig. 11.4 Collet Assembly Removal

11.5 Clamp Assembly Removal and Installation

(1) Remove the front plate as described in 11.2.
(2) Remove the two clamp assembly mounting screws.
(3) Remove the clamp assembly.
(4) Reverse the above procedure to reinstall.

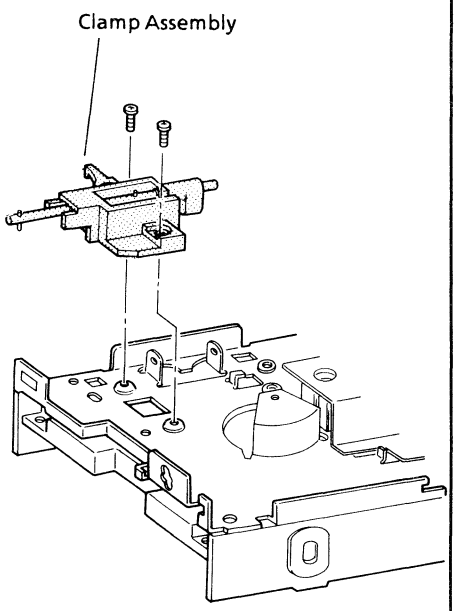


Fig. 11.5 Clamp Assembly Removal

11.6 Write Protect Sensor/Index Detector Assembly Removal and Installation (See Fig. 11.6)

(1) Remove the front plate as described in 11.2.
(2) Remove the write protect sensor mounting g screw and index detector mounting screw respectively.
(3) Remove the write protect sensor/index detector assembly.
(4) Reverse the above procedure to reinstall.
(5) When reinstalling the write protect sensor, exercise care so that the leads and write protect sensor will not project from the bottom and side of the base.
(6) After index detector installation, adjust the index timing as described in 9.7.

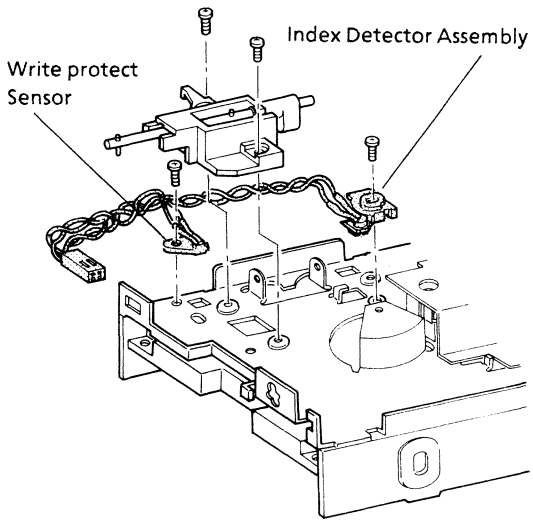


Fig. 11.6 Write Protect Sensor/Index Detector Assembly Removal

11.7 Cartridge Guide Assembly Removal and Installation (See Fig. 11.7)

(1) Remove the printed circuit board as described in 11.1.
(2) Remove the front plate as described in 11.2.
(3) Remove the shield plate mounting screw and take the shield plate off.
(4) Remove the write protect sensor as described in 11.6. It is not necessary to remove the index detector.
(5) Remove the four cartridge guide mounting screws and take out the cartridge guide assembly.
(6) After reinstallation, adjust the collet assembly as in 11.4 step (6) and adjust the index timing as in 9.7.
(7) When removing or reinstalling, be careful not to damage the carriage arm with the lifter.

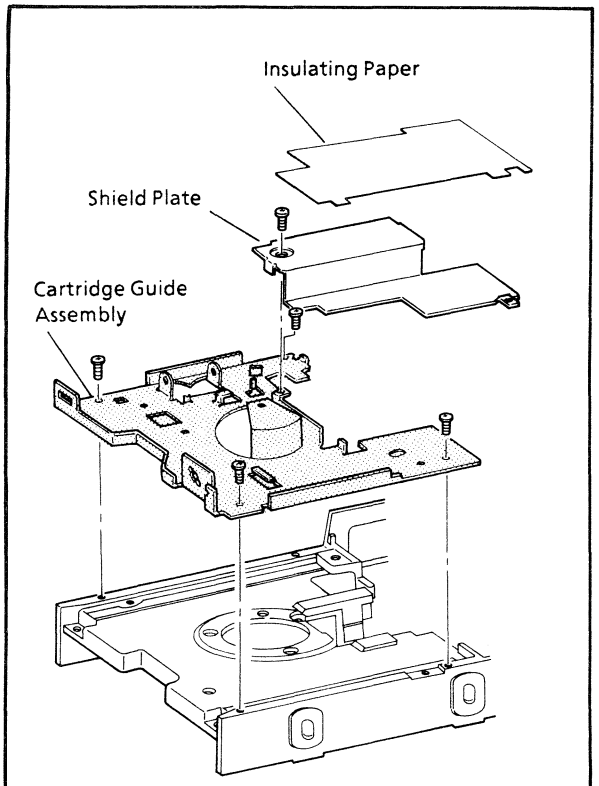


Fig. 11.7 Cartridge Guide Assembly Removal

11.8 Stepper Motor Assembly Removal and Installation (See Fig. 11.8)

(1) Remove the insulating paper and shield plate.
(2) Remove the track 00 sensor as described in 11.3.
(3) Remove the two (M2 x 4) actuator screws that fasten the actuator to the carriage arm assembly.
(4) Remove the two (M3 x 6) stepper motor assembly mounting screws and then the stepper motor.
(5) Reverse the above procedure to reinstall.
(6) After reinstallation, perform limiter check as in 9.10 and radial alignment adjustment as in 9.5.
(7) Adjust the track 00 sensor according to the instruction in 9.8.

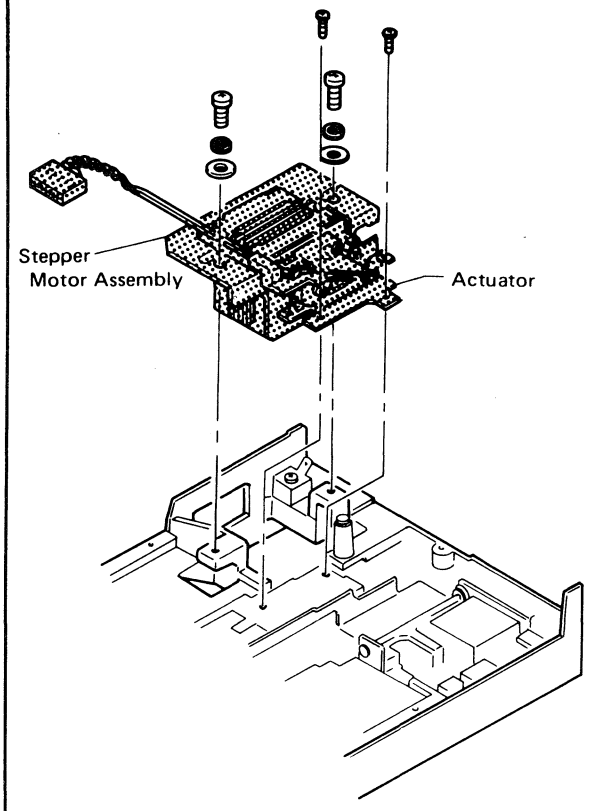


Fig. 11.8 Stepper Motor Assembly Removal

11.9 Carriage Arm Assembly Removal and Installation (See Fig. 11.9)

(1) Remove the printed circuit board as described in 11.1.
(2) Remove the insulating paper and shield plate.
(3) Remove the track 00 assembly as described in 11.3.
(4) Remove the stepper motor assembly as described in 11.8.
(5) Remove the two guide rod clamp mounting screws.
(6) Remove the carriage arm assembly, guide rod clamp, and guide rod.
(7) Pull out the guide rod from the carriage arm assembly.
(8) Reverse the above procedure to reinstall.
(9) After replacement, perform limiter adjustment as described in 9.10, track 00 sensor adjustment as described in 9.8, and radial alignment adjustment as described in 9.5.

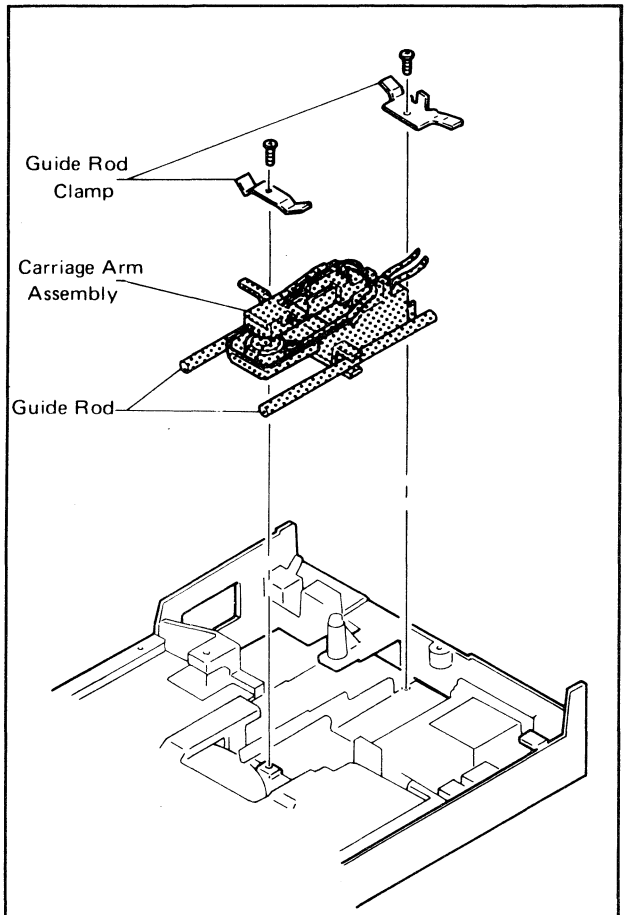


Fig. 11.9 Carriage Arm Assembly Removal

11.10 Drive Motor Removal and Installation (See Fig. 11.10)

(1) Remove the printed circuit board as described in 11.1.
(2) Remove the insulating paper and shield plate.
(3) Remove the front plate as described in 11.2.
(4) Remove the write protect sensor as described in 11.6.
(5) Remove the cartridge guide assembly as described in 11.7.
(6) Remove the three drive motor mounting screws and take off the drive motor from the base.
(7) Disconnect the drive motor connector pins from the connector.
(8) Reverse the above procedure to reinstall.
(9) When reinstalling, make sure that the drive motor connector is connected in the correct direction.
(10) After reinstallation, perform motor speed adjustment as described in 9.1 and also the adjustments necessary upon reinstallation of the cartridge guide as described in 11.7.

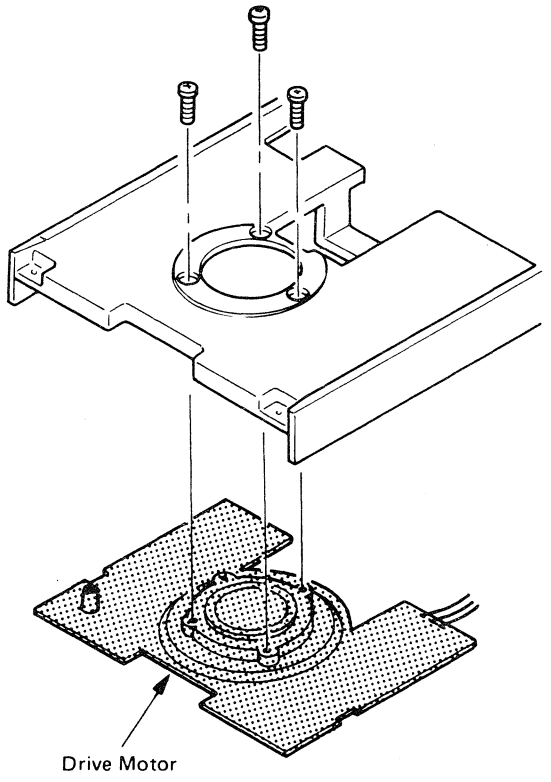


Fig. 11.10 Drive Motor Removal

11.11 LED Assembly Removal and Installation

(1) Remove the clamp handle and front plate.
(2) Disconnect the connectors J8 CON from the printed circuit board.
(3) Remove the LED Assembly by sliding it aslant from the Cartridge Guide Assembly.
(4) Reverse the above procedure to reinstall.

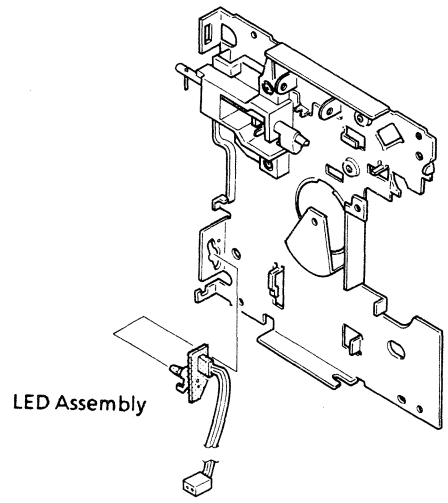
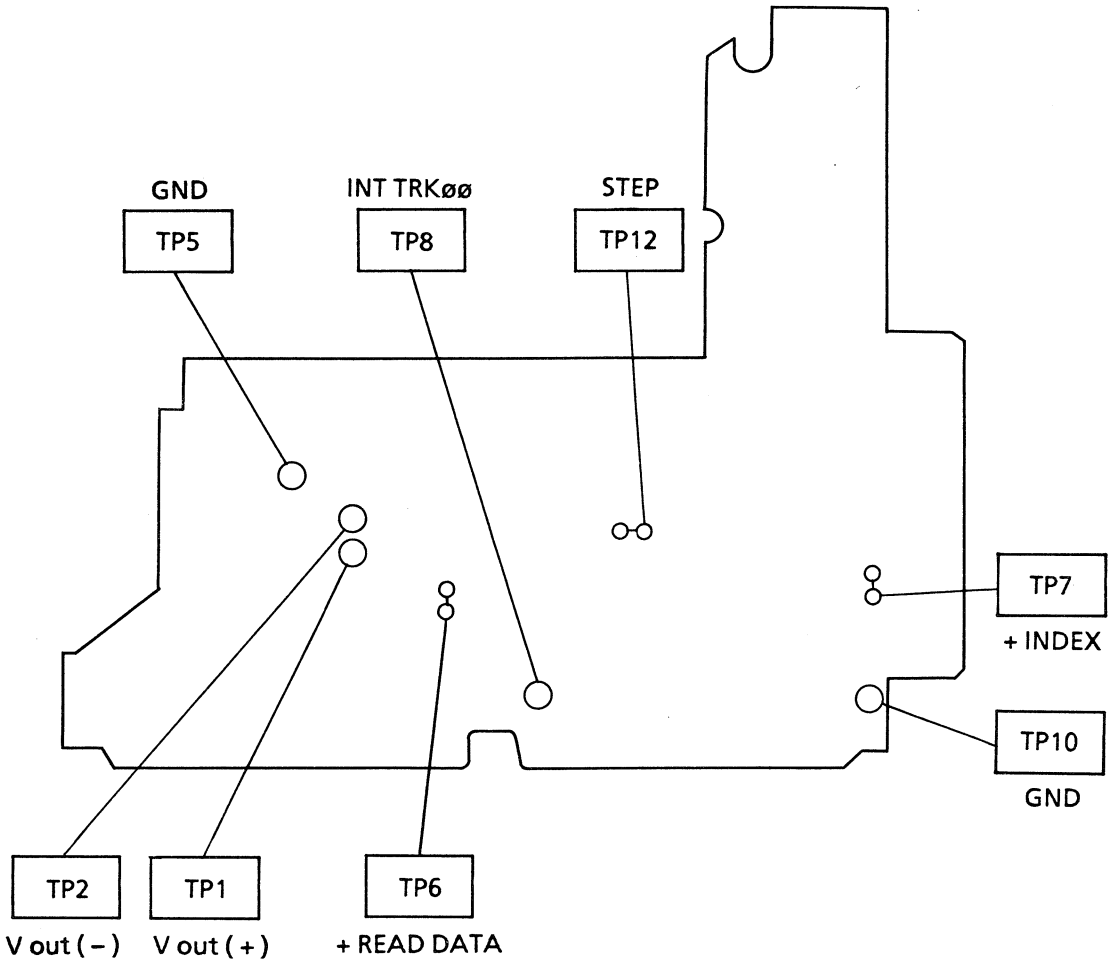


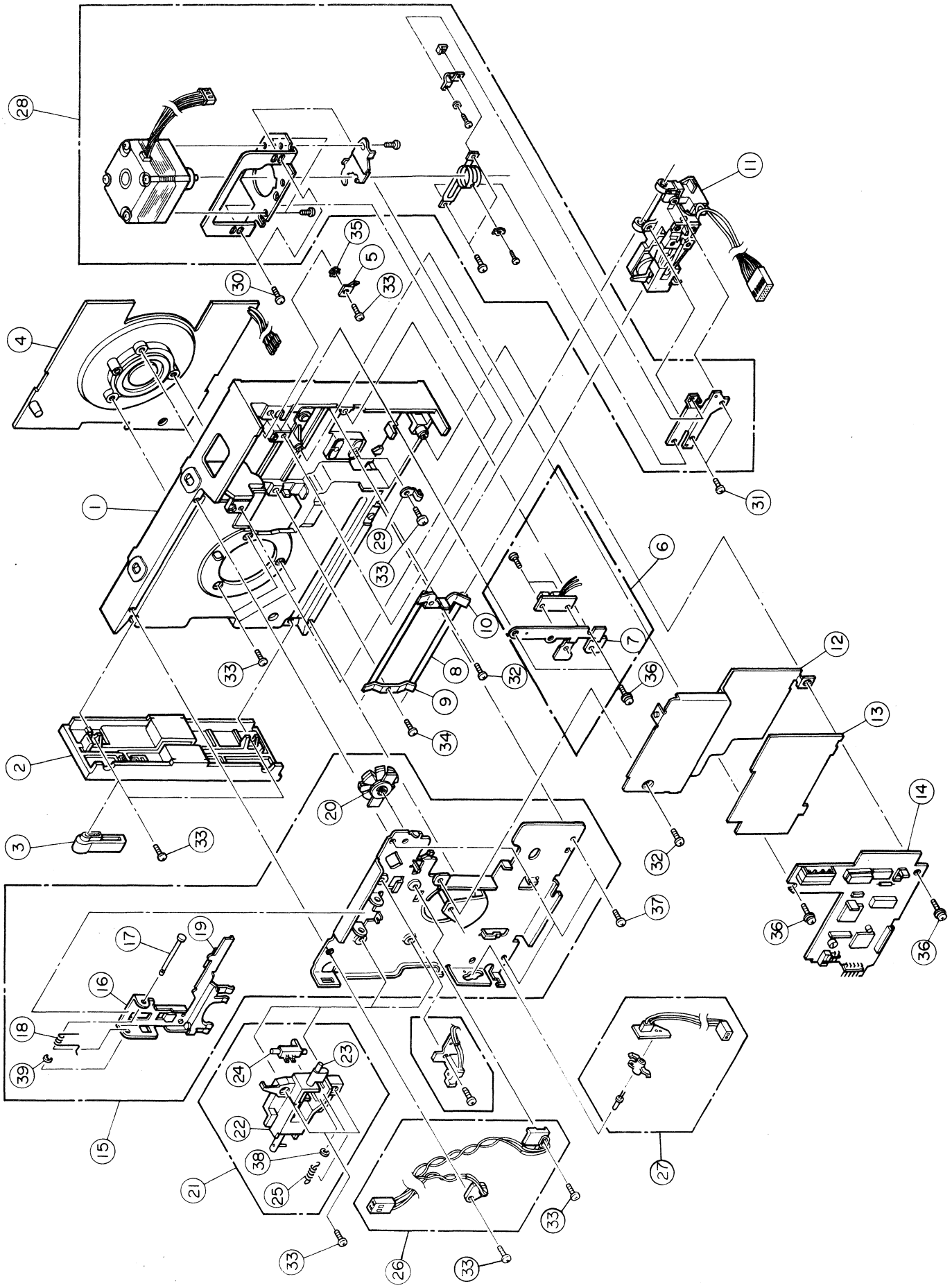
Fig. 11.11 LED Assembly Removal

12. TEST POINTS

Printed Circuit Board
(Top view)



13. EXPLODED VIEW



14. REPLACEMENT PARTS LIST

MODEL: JU-455-5

Ref. No.	Part No.	Description	Per Set (pcs.)
1	YTF3L01901B1	Base	1
2	333D26817682	Front Panel	1
3	YTF6A01090B3	Clamp Handle	1
4	YTFMD00790B4	Drive Motor	1
5	YJ617612	Faston	1
6	YTUF56TRK-2T	Sensor Assembly (For TRKø)	1
7	YTF2T01560B4	Bracket (For TRKø)	1
8	YTF2E02561B4	Guide Rod	2
9	333D46331360	Clamp (For Guide Rod Head)	1
10	YJF2E00580B4	Clamp (For Guide Rod End)	1
11	YTUF55HD	Head Carriage Assembly	1
12	YTF2H03582B3	Shield Plate	1
13	YTF2P03591B4	Insulating Paper	1
14	YTUF55PK-5	PCB Assembly	1
15	YTUF55CG	Cartridge Guide Assembly	1
16	YTF3C02732B3	Lifter	1
17	YTF4H01360B4	Lift Shaft	1
18	YTF4J01901B4	Lift Spring	1
19	333D46817500	Pat	1
20	YTUF56CLT2AN	Collet Assembly	1
21	UF45CP3CAE1	Clamp Assembly	1
22	YJF4F00341B2	Clamp Bearing	1
23	YTF4H01720B3	Clamp Cam Assembly	1
24	333D36817692	Lock Cam	1
25	333D46624770	Lock Spring	1
26	YTUF45WP4AAA	Write Protect Assembly	1
27	YTUF45LED	LED Assembly	1
28	YTUF55SM	Stepper Motor Assembly	1
29	YTF1G00500B4	Cord Clamp	1
30	YTF1E00300B4	Washer Head Screw	2
31	XSB2 + 4V	Screw (M2x4 Bind)	2
32	XSB3 + 4V	Screw (M3x4 Bind)	2
33	XSB3 + 6FX	Screw (M3x6 Bind)	11
34	XSB3 + 6V	Screw (M3x6 Bind)	1
35	XWC3B	Toothed Lock Washer	1
36	XYN3 + F6	Screw (M3x6 Sems)	4
37	Y-1283	Screw (M3x6 Bind)	3
38	XUC3	Retaining Ring	1
39	XUC2	Retaining Ring	1

Caution:
1. PCB Assembly is produced to order during the production period only.
2. When you order the aforementioned parts, be sure to specify "Part No." of the parts ordered.

15. REPLACEMENT PARTS LIST OF PCB

MODEL: JU-455-5

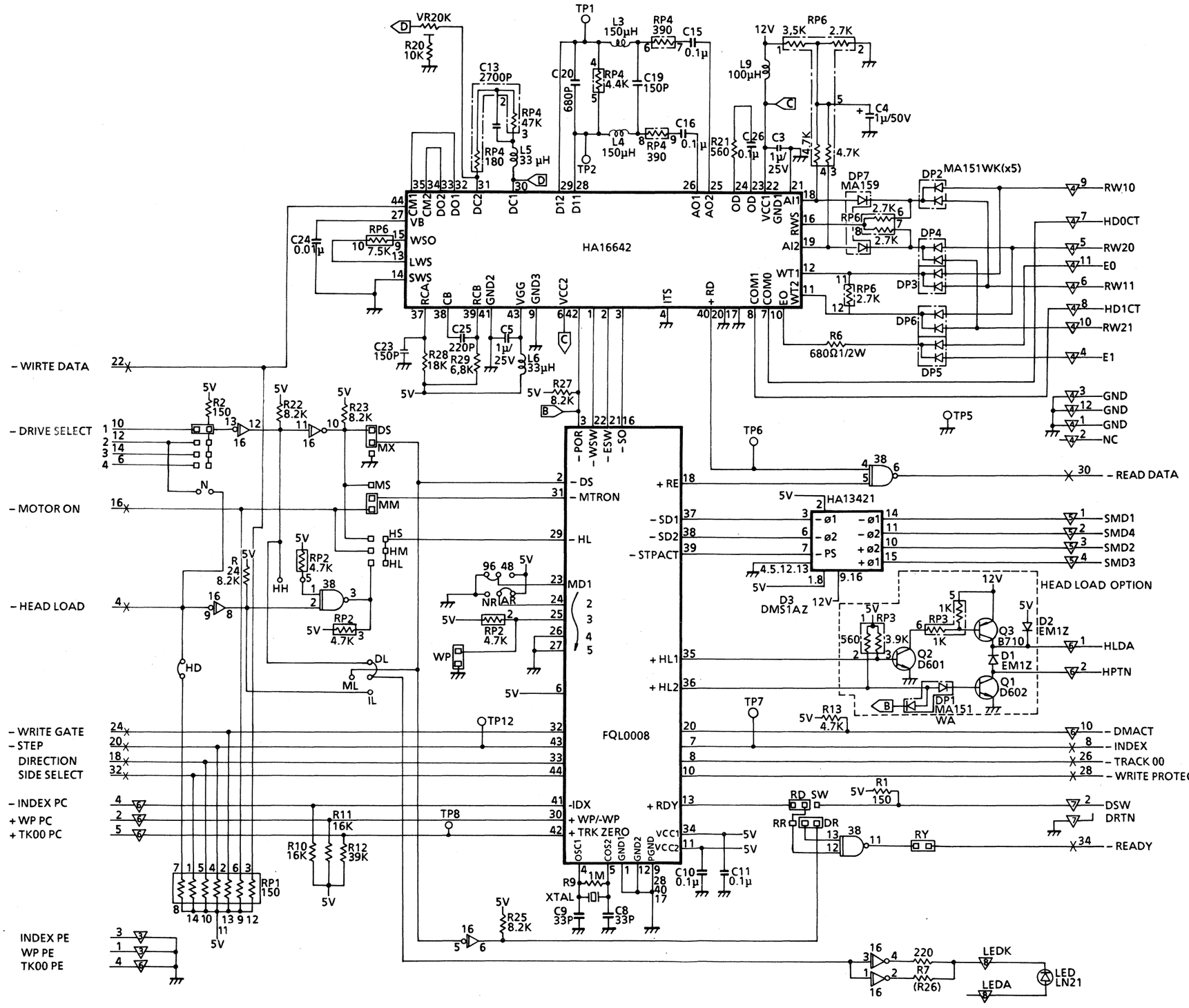
Component Side (Top)

Ref. No.	Part No.	Description	Per Set (pcs.)
R6	ERDS1TJ681	Carbon Resistor	1
C1	ECEA1HKS100E	Electrolyte Capacitor	1
C2,3,5	FCJ00080B400	Ceramic Capacitor	3
C4	ECEA1HKS010E	Electrolyte Capacitor	1
CN	FJC00080B400	Connector	1
CN	FJC00080B401	Connector	2
CN	FJC00090B402	Connector	2
CN2	YJ172294-1	Connector	1
CN2	YJ172296-1	Clamp	1
CN3	YTFFC4TLBW1B	Connector	1
CN4	YJFJC00230B4	Connector	1
CN7	YTFFC2LBW1B	Connector	1
CN8	FJC00180B400	Connector	1
IR1	EXBRB7151JW	Block Resistor	1
IR2	EXBP84472J	Block Resistor	1
IR4	EXBL85368J	Block Resistor	1
IR6	EXBG88359S	Block Resistor	1
L	FNC00030B426	Low-Frequency Coil	2
L	YJBL02RN2R62	Choke Coil	2
L5	FNC00030B418	Low-Frequency Coil	1
L6	ELEPG330KA	Choke Coil	1
L9	LAL03KH101K	Choke Coil	1
VR	EVMQ0G01KB24	Variable Resistor	1
X	YJCSA4.00MG	Resonator	1
16	DN74LS16-1S	IC	1
38	DN74LS38-1	IC	1
P	FJP00110B400	Plug	7
XV	YJDILB14P8JC	IC Socket	1
HA13421	HA13421	LSI	1
HA16642	HA16642MP	IC	1
FQL0008	FQL00081B4	LSI	1

Solder Side (Bottom)

Ref. No.	Part No.	Description	Per Set (pcs.)
R1,2,3	FRA00010B428	Chip Resistor	3
R7	FRA00040B432	Chip Resistor	1
R8	FRA00040B496	Chip Resistor	1
R9	FRA00050B420	Chip Resistor	1
R10,11	FRA00040B477	Chip Resistor	2
R12	FRA00040B486	Chip Resistor	1
R13	FRA00040B464	Chip Resistor	1
R20	FRA00040B472	Chip Resistor	1
R21	FRA00040B442	Chip Resistor	1
R22,23, 24,25, 27	FRA00040B470	Chip Resistor	5
R28	FRA00040B478	Chip Resistor	1
R29	FRA00040B468	Chip Resistor	1
C6,7,24	FCC00060B408	Chip Capacitor	3
C8,9	FCC00040B420	Chip Capacitor	2
C10,11, 15,16, 26	FCC00020B401	Chip Capacitor	5
C18	FCC00070B409	Chip Capacitor	1
C19,23	FCC00010B440	Chip Capacitor	2
C20	FCC00010B456	Chip Capacitor	1
C25	FCC00010B444	Chip Capacitor	1
CN5	YTB4B-PH	Connector	1
CN6	FJC00220B403	Connector	1
D	MA151WK-TW	Diode	5
D	MA151WK-TX	Diode	5
D	MA159-TW	Chip Diode	1
D	MA159-TX	Chip Diode	1

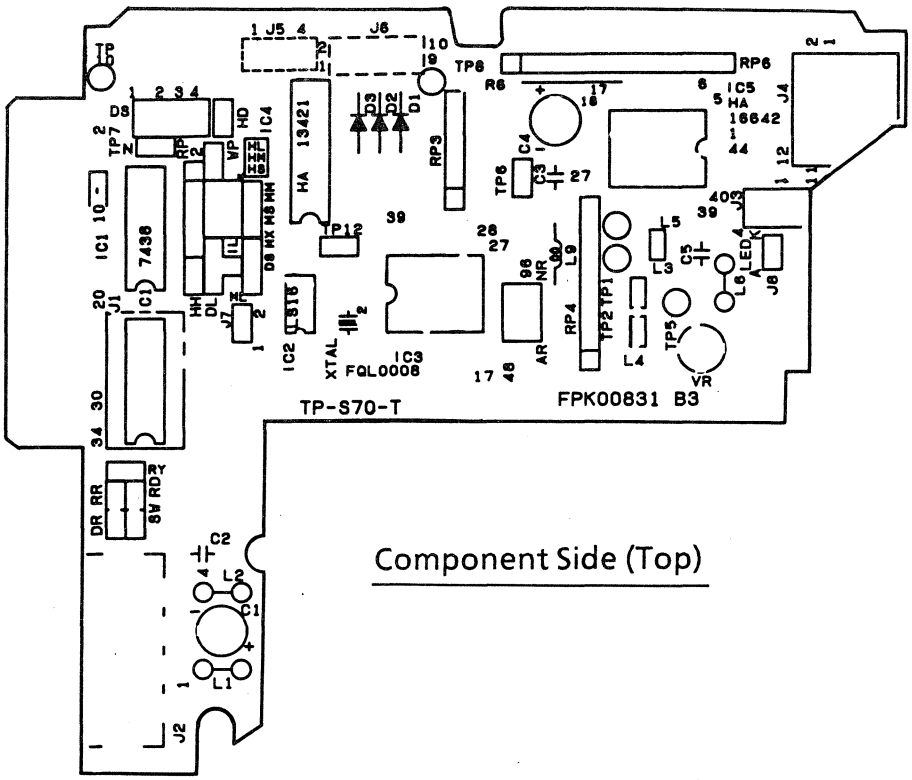
16. SCHEMATIC DIAGRAM (JU-455-5)

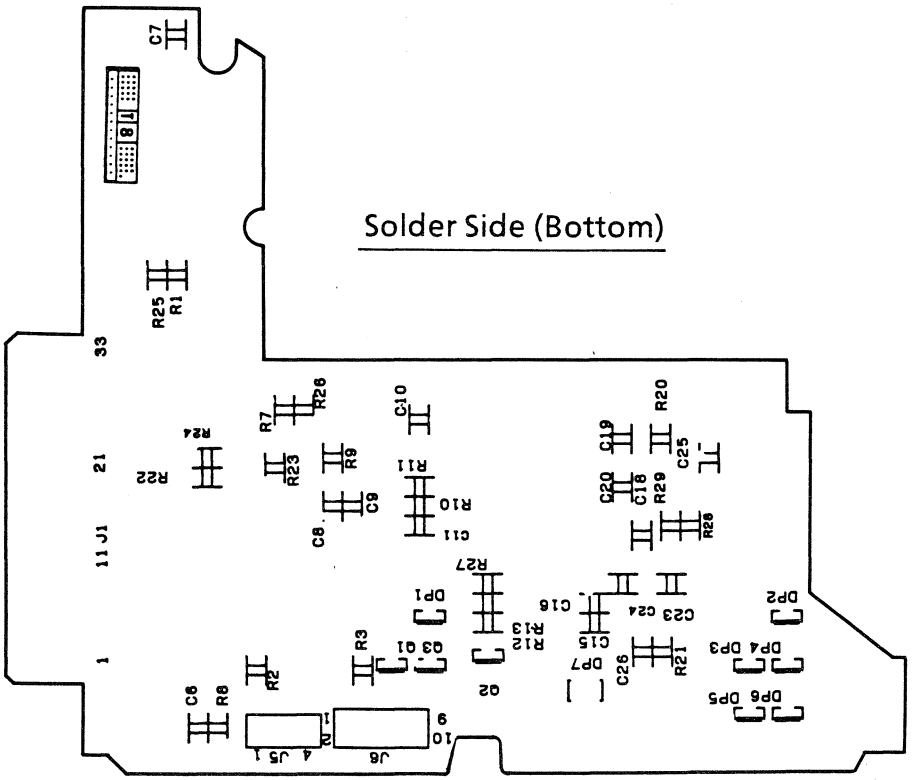


NOTE:

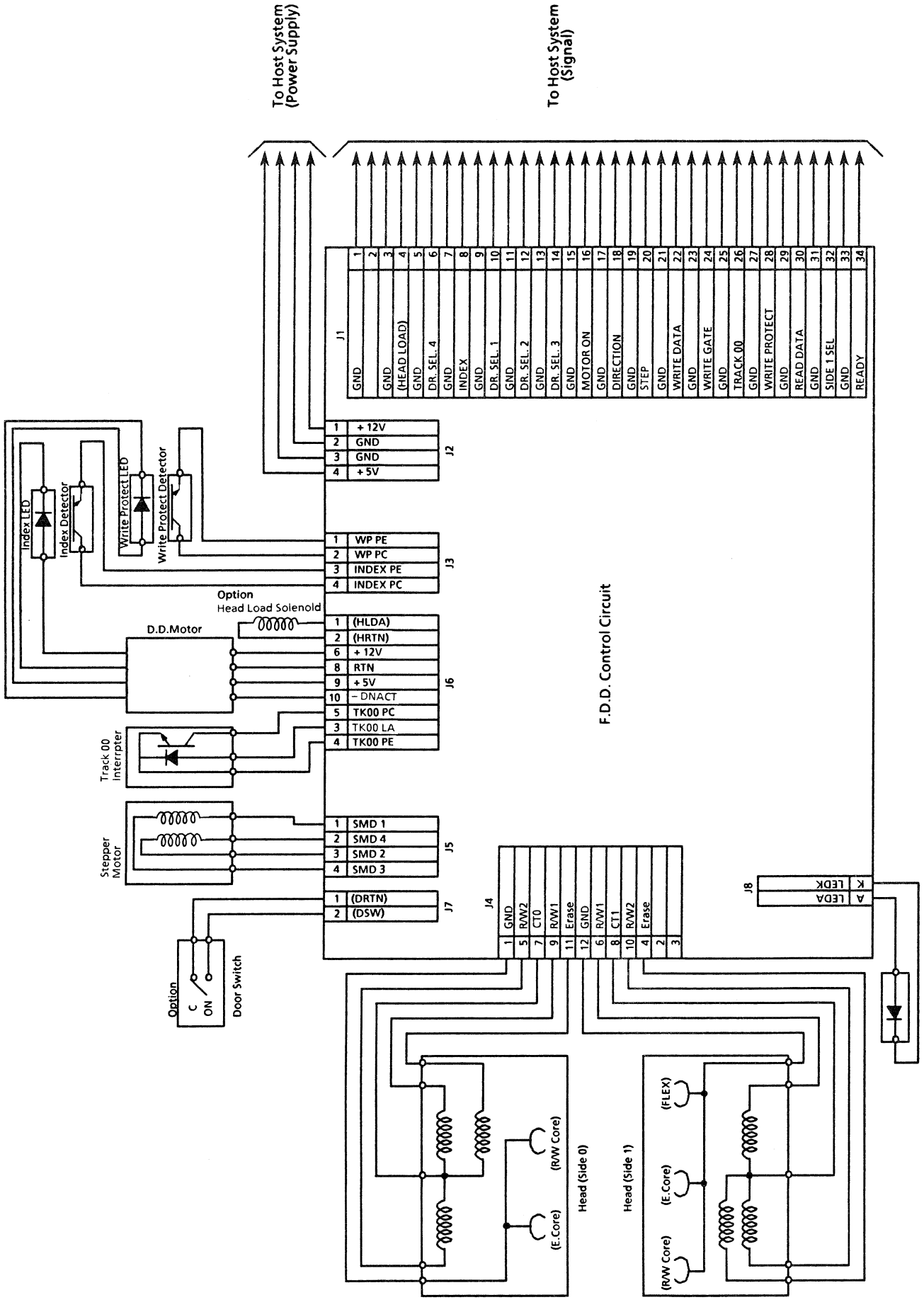
1. NOT USED R26

17. CIRCUIT BOARD





18. BLOCK DIAGRAM



APPENDIX

ADJUSTMENT

1. INTRODUCTION

This manual describes the operation of FDD (Floppy Disk Drive) maintenance program, a set of routines designed for the maintenance of FDD. The program is menu-driven, and the main menu provides access to the various maintenance routines, as shown below:

2.1 HEAD OUTPUT ALIGNMENT CALIBRATION

2.2 TRACK 00 SIGNAL CALIBRATION

2.3 CARRIAGE LIMIT CALIBRATION

2.4 INDEX TIMING CALIBRATION

2.5 AZIMUTH AND CAT'S EYE PATTERN CALIBRATION

2.6 HEAD CLEANING

2.7 MAINTENANCE DISK DRIVE ASSIGNMENT

2.8 (Reserved)

2.9 EXIT

2.8 MENU SELECTIONS 8 AND 9

2. OPERATING THE PROGRAM

The FDD maintenance program runs under MS-DOS. To run the program you will need four diskettes. The first is the diskette containing the maintenance program. The second is a "scratch diskette", which is a blank, formatted diskette. The third is an "alignment diskette, which is used for alignment purposes. The fourth is a head-cleaning diskette, which is used to perform the head cleaning procedure.

Insert the program diskette, wait for the DOS prompt, and start up the program as follows:

```
A>FDDMAINT  <ENTER>
```

When the program is loaded, the screen will display the following menu, showing the maintenance routines:

```
MAINTENANCE MENU

1.  HEAD OUTPUT ALIGNMENT CALIBRATION

2.  TRACK 00 SIGNAL CALIBRATION

3.  CARRIAGE LIMIT CALIBRATION

4.  INDEX TIMING CALIBRATION

5.  AZIMUTH AND CAT'S EYE PATTERN CALIBRATION

6.  HEAD CLEANING

7.  MAINTENANCE DISK DRIVE ASSIGNMENT

8.  (Reserved)

9.  EXIT

Current drive assignment is X:
SELECT MENU ? __
```

From the maintenance menu, you can run the individual maintenance routines, or assign the FDD to be maintained. After running the individual routines, you will be returned to the maintenance menu, from where you can run other routines or exit the program.

The individual maintenance routines are described in the following sections.

2.1 Head Output Alignment Calibration

The purpose of this routine is to measure the alignment of the read/write head. To run it, enter "1" from the maintenance menu. The following display will appear:

```
1.  HEAD OUTPUT ALIGNMENT CALIBRATION

Insert scratch diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

If you wish to abort the routine and return to the maintenance menu, press the <Escape> key. Otherwise, insert the scratch diskette in the drive indicated, and press any key. The next prompt will be:

```
Are you sure (Y/N)?
```

Type "Y" to continue. (If you type "N", you will be returned to the first message for this routine.)

The read/write head moves to TRACK 39, and performs a write operation on the entire diskette followed by a read operation on the entire diskette. The following display will appear:

```
HEAD Position = TRACK 39

Continuing READ operations

Check HEAD OUTPUT alignment

Press any key to return to the maintenance menu.
```

Press any key to stop the routine and return to the maintenance menu.

Note: This routine is used to check the operation of the read/write head as it writes to a diskette.

2.2 Track 00 Signal Calibration

The purpose of this routine is to measure the TRACK 00 output signal. To run it, enter "2" from the maintenance menu. The following display will appear:

```
2.  TRACK 00 SIGNAL CALIBRATION

Insert alignment diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

If you wish to abort the routine and return to the maintenance menu, press the Escape key. Otherwise, insert the alignment diskette in the drive indicated, and press any key. The screen will display:

```
HEAD continues to seek TRACK 00 and TRACK 01

Check TRACK 00 signal

Press any key to return to the maintenance menu
```

The read/write head performs continuous SEEK operations on TRACK 00 and TRACK 01.

Press any key to stop the routine and return to the maintenance menu.

2.3 Carriage Limit Calibration

The purpose of this routine is to measure the carriage limit. To run it, enter "3" from the maintenance menu. The following display will appear:

```
3.  CARRIAGE LIMIT CALIBRATION

Insert alignment diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

To run the routine, insert the maintenance diskette in the drive indicated, and press any key. The screen will display the following sub-menu.

```
1.  HEAD position at TRACK 00 (Carriage limit check)

2.  HEAD position at TRACK 39 (Carriage limit check)

3.  EXIT

SELECT MENU ? __
```

Enter "1" to move the head to TRACK 00. The following display will appear:

```
HEAD position = TRACK 00

Check carriage limit

Press any key to return to the sub-menu
```

Press any key to stop the routine and return to the sub-menu.

Enter "2" to move the head to TRACK 39. The following display will appear:

```
HEAD position = TRACK 39

Check carriage limit

Press any key to return to the sub-menu
```

Press any key to stop the routine and return to the sub-menu.

When you are finished with this routine, enter "3" from the sub-menu to return to the maintenance menu.

2.4 Index Timing Calibration

The purpose of this routine is to measure the index timing. To run it, enter "4" from the maintenance menu. The following display will appear:

```
4.  INDEX TIMING CALIBRATION

Insert alignment diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

To run the routine, insert the alignment diskette in the drive indicated, and press any key. The screen will display the following sub-menu.

```
1.  HEAD position at TRACK 01 (Index signal check)

2.  HEAD position at TRACK 34 (Index signal check)

3.  EXIT

SELECT MENU ? __
```

Enter "1" or "2" to move the head to TRACK 01 or TRACK 34, respectively. The following display will appear:

```
HEAD position = TRACK xx

Continuing READ operation

Check INDEX timing

Press any key to return to the sub-menu
```

Press any key to stop the routine and return to the sub-menu.

When you are finished with this routine, enter "3" from the sub-menu to return to the maintenance menu.

2.5 Azimuth and Cat's Eye Pattern Calibration

The purpose of this routine is to measure the azimuth and cat's eye patterns. To run it, enter "5" from the maintenance menu. The following display will appear:

```
5.  AZIMUTH AND CAT'S EYE PATTERN CALIBRATION

Insert alignment diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

To run the routine, insert the alignment diskette in the drive indicated, and press any key. The screen will display the following sub-menu:

```
1.  AZIMUTH pattern check     (HEAD moves from TRACK 00
       to TRACK 34)

2.  CAT'S EYE pattern check   (HEAD moves from TRACK 00
       to TRACK 16)

3.  CAT'S EYE pattern check   (HEAD moves from TRACK 34
       to TRACK 16)

4.  EXIT

SELECT MENU ? __
```

Enter "1" to run the azimuth pattern check. Enter "2" or "3" to run the cat's eye pattern checks. The following display will appear:

```
HEAD position = TRACK xx

Continuing READ operation

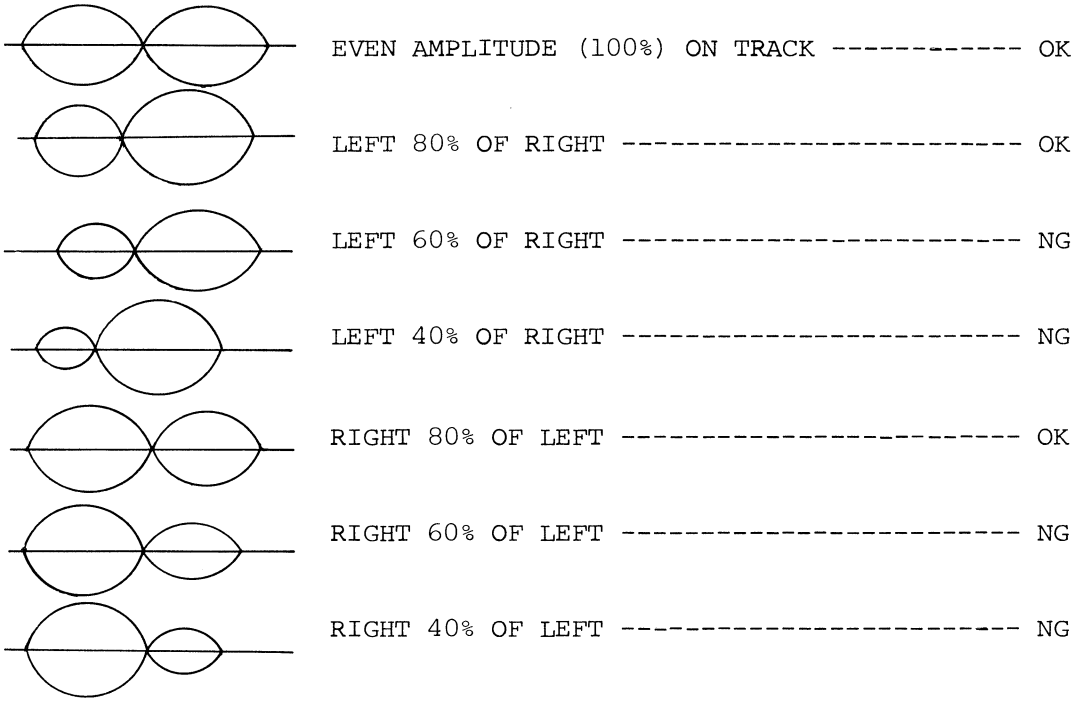
Check AZIMUTH or CAT's EYE pattern

Press any key to return to the sub-menu
```

Press any key to stop the routine and return to the sub-menu.

When you are finished with this routine, enter "4" from the sub-menu to return to the maintenance menu.

Note: Standard value: More than 80%
Track position: TR16



2.6 Head Cleaning

This is the routine for cleaning the disk heads. To run it, enter "6" from the maintenance menu. The following display will appear:

```
6. HEAD CLEANING

Insert cleaning diskette in drive x:

Press any key when ready (or press ESC key to return to the
maintenance menu)
```

To run the routine, insert the head cleaning diskette in the drive indicated, and press any key. The screen will display the following:

```
HEAD continuing SEEK operation between TRACK 00 and TRACK 39

Completes after repeating program execution ten times
```

The routine will repeat a complete cycle, from TRACK 00 to TRACK 39, ten times. The program will then return to the maintenance menu.

2.7 Maintenance Disk Drive Assignment

This routine allows you to assign the disk drive for maintenance. To run it, enter "7" from the maintenance menu. The following display will appear:

```
7.  MAINTENANCE DISK DRIVE ASSIGNMENT

Current drive assignment is x:

Assign disk drive (A or B) ? __
```

Enter the desired disk drive assignment. (When the program is started up, the default drive is B:) After you have entered the disk drive assignment (A or B), the program will return to the maintenance menu.

2.8 Menu Selections 8 and 9

Menu selection 8 from the maintenance menu is reserved for future expansion.

Menu selection 9 is the EXIT routine. Enter "9" from the maintenance menu to exit from the FDD maintenance program. Control will be returned to MS-DOS.

ORDER NO. DATA 85012
G3

Technical Guide

Portable Computer
JB-3300

I General
II Logic Unit
III Plasma Display Unit
IV Keyboard
V Power Supply Unit
VI Floppy Disk Drive
VII Option

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

VII-1 HARD DISK CONTROLLER

1. PREFACE

1.1 General

The NDC-5027M is a magnetic disk drive control board which is able to control one or two magnetic disk drives having an interface conforming with the Seagate ST506. Its host-side interface is compatible with the IBM personal computer.

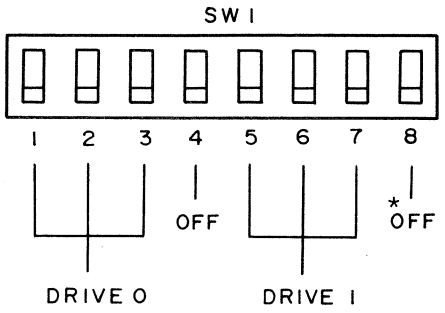
Although the NDC-5027M basically uses the same hardware as the NDC-5027M, its ROM socket firmware and BIOS program include a number of special features such as alternative functions and other additional items.

1.2 Specifications

Host interface:	Conforms to IBM personal computer.
No. of connectable devices:	1 or 2 magnetic disk drives with ST506 or equivalent interface
Sector length:	512 bytes per sector
Data error correction function:	Errors in 11-bit bursts correctable by 32-bit error correction code (ECC)

1.3 Correlation Table for Connected Magnetic Disk Drives

Under the fixed disk BIOS program, eight types of magnetic disk drives can be selected for each of the two disk drives (drive 0 and drive 1) by setting the DIP switch. The table below shows the correlation of DIP switch values and drive type settings.



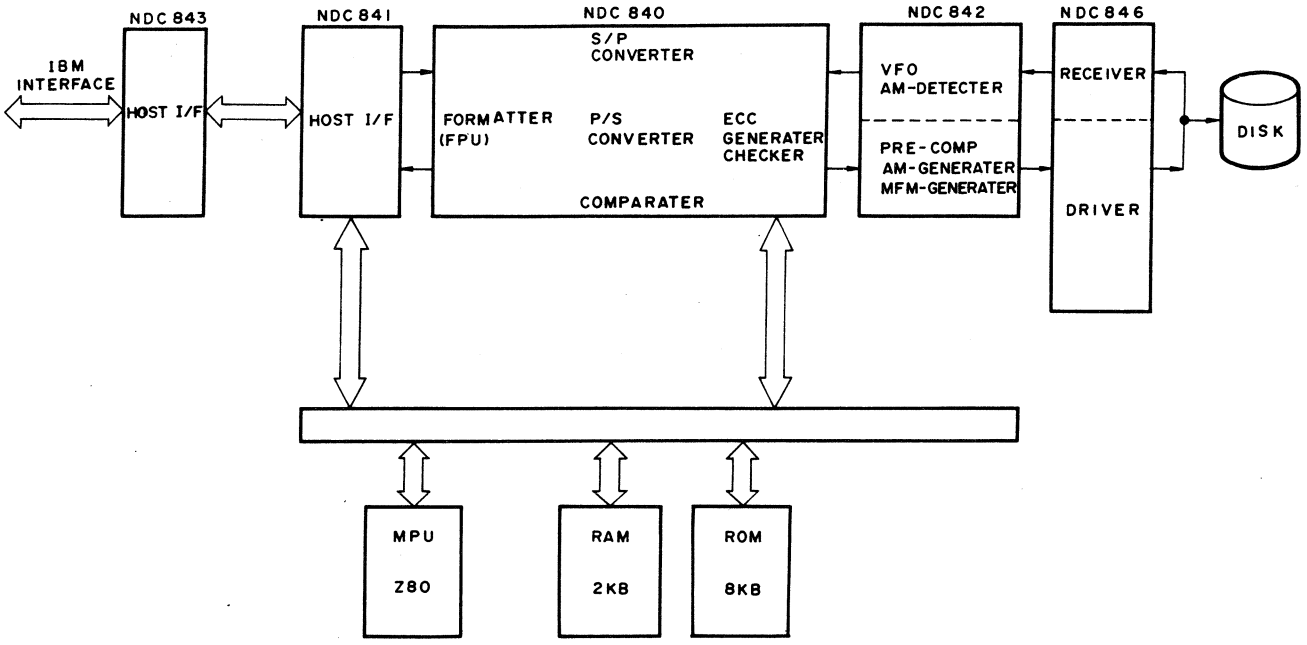
DRIVE TYPE	SW1			CYLINDER	HEAD	W.P.C.	R.W.C.
	1	2	3				
	5	6	7				
0	1	1	1	699	7	256	256
1	1	1	0	615	4	128	615
2	1	0	1	310	4	128	310
3	1	0	0	612	4	256	612
4	0	1	1	612	2	256	612
5	0	1	0	320	8	128	320
6	0	0	1	320	4	128	320
7	0	0	0	306	4	0	306

SW1 0: OFF
1: ON
W.P.C.: Starting write precompensation cylinder
R.W.C.: Starting reduced write current cylinder

*: OFF = Normal operating condition

ON = One disk drive is connected as drive 0 and its disk storage space is divided in half, one half of which is treated as drive 0 storage space and the other half as drive 1 storage space (simulation of two disk drives).

1.4 Block Diagram



(1) NDC 843

This LSI handles signal exchange between the IBM personal computer's I/O channel and the NDC 841 LSI.

(2) NDC 842

This LSI changes MFM data sent from the disk drive into NRZ data, changes NRZ data from the host computer into MFM data, and executes read and write operations vis-a-vis the disk drive.

(3) NDC 841

This LSI converts signals between the controller and the NDC 843 LSI for the IBM I/O channel.

(4) NDC 840

This LSI operates in the HDC according to commands sent from the MPU (Z80). It converts 8-bit parallel data sent by the host computer into serial data and also converts serial data sent by the disk drive into 8-bit parallel data. During write operation, it adds a 4-byte ECC to the end of the write data and, during read operation, it checks this pattern for read errors and corrects any errors detected (using an 11-bit burst).

2. PRINCIPAL SPECIFICATIONS

2.1 General Description

This controller is matched to the slot dimensions of the IBM-XT to enable easy mounting.

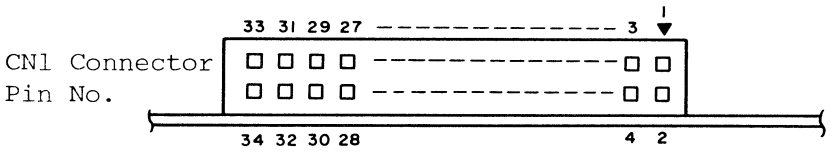
2.2 Power Supply

Required voltage:	DC +5V ±5%
Required current:	1.1 A (typical), 1.4 A (maximum)

2.3 Connectors

2.3.1 CN1

This connector is used by the drive control signal.

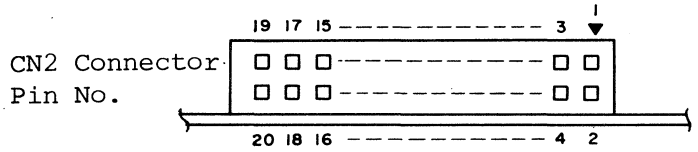


Signal Pin	Ground Pin	Signal Name
2	1	*Reduced Write
4	3	Head Select 2^2
6	5	Write Gate
8	7	Seek Complete
10	9	Track 00
12	11	Write Fault
14	13	Head Select 2^0
16	15	Reserved
18	17	Head Select 2^1
20	19	Index
22	21	Ready
24	23	Step
26	25	Drive Select 1
28	27	Drive Select 2
30	29	Reserved
32	31	Reserved
34	33	Direction in

Note: The JP6 setting can be used to change signal to Head Select 2^3. The setting method is described in section 3.2 below.

2.3.2 CN2 and CN3

These connectors are used by the drive data signals.



Signal Pin	Ground Pin	Signal Name
1	2	Drive Selected
3	4	Reserved
5	6	Spare
7	8	Reserved
9	11	Spare
10	12	Spare
13	15	+MFM Write Data
14	16	-MFM Write Data
17	19	+MFM Read Data
18	20	-MFM Read Data

2.3.3 CN4

This connector is used by the host interface.

Signal Name	Terminal No.	Function
A 19 A 18 ~ A 1 A 0	A 12 A 13 ~ A 30 A 31	Address Bus
D 7 D 6 ~ D 1 D 0	A 2 A 3 ~ A 8 A 9	Data Bus
IOR-	B 14	I/O Read
IOW-	B 13	I/O Write
AEN	A 11	Address Enable
RESET DRV	B 2	Reset Drive
IRQ5	B 23	Interrupt Request 5
DRQ 3	B 16	DMA Request 3
DACK3-	B 15	DMA Acknowledge 3
+5 V +5 V	B 3 B 29	+5 V Power
GND GND GND	B 1 B 10 B 31	GND

3. FUNCTION SETTINGS AND MOUNTING METHOD FOR NDC 5027M BOARD

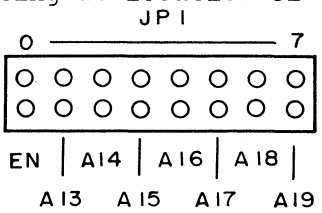
3.1 General Description

This section describes the jumper-plug function settings and mounting method for the NDC 5027M board.

3.2 Function Settings

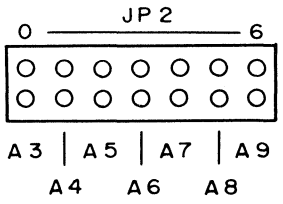
The functions are set using the jumper plugs as shown below.

JP1: Memory address setting at location C1 on the board



EN: Short-circuit this to enable use of the memory. The address setting is short circuit = 0 and open circuit = 1.
Address settings A13 to A19 are wired on the PCB to C8000Hex.

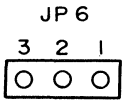
JP2: Controller base address setting



The address setting corresponds to short circuit = 0 and open circuit = 1.

Address settings A3 to A9 are wired on the PCB to 320 Hex.

JP6: Magnetic disk drive control signal and function setting



Switch operation of magnetic disk drive control signal No. 2. terminal:

Between 1 and 2: Reduced write current

Between 2 and 3: Head select 2

4. HOST INTERFACE

The NDC 841 and NDC 843 are for the host interface section. The NDC 841, when combined with the NDC 840 and other parts, is designed to facilitate configuration of a disk controller for the SASi interface.

The NDC 843 can be used to convert the timing of the SASi interface (with NDC 841-configured disk controller) to ensure compatibility with the IBM-PC/XT's bus timing.

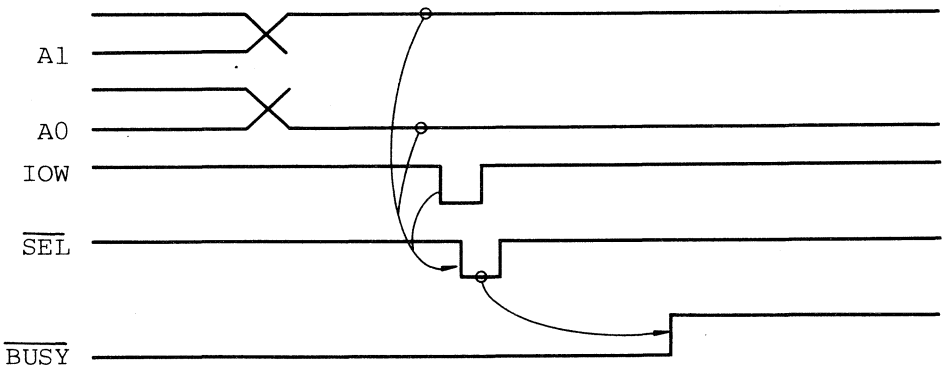
To write commands or data from the host computer, the commands or data are first set in the NDC 843's internal register and then are transferred to RAM by the NDC 840's DMA mode.

Similarly, to read status data or other data, the data are first read from RAM and set in the NDC 841's internal register, and then are read into the host computer.

4.1 Time Chart of Principal Operations

a. Controller selection (322H)

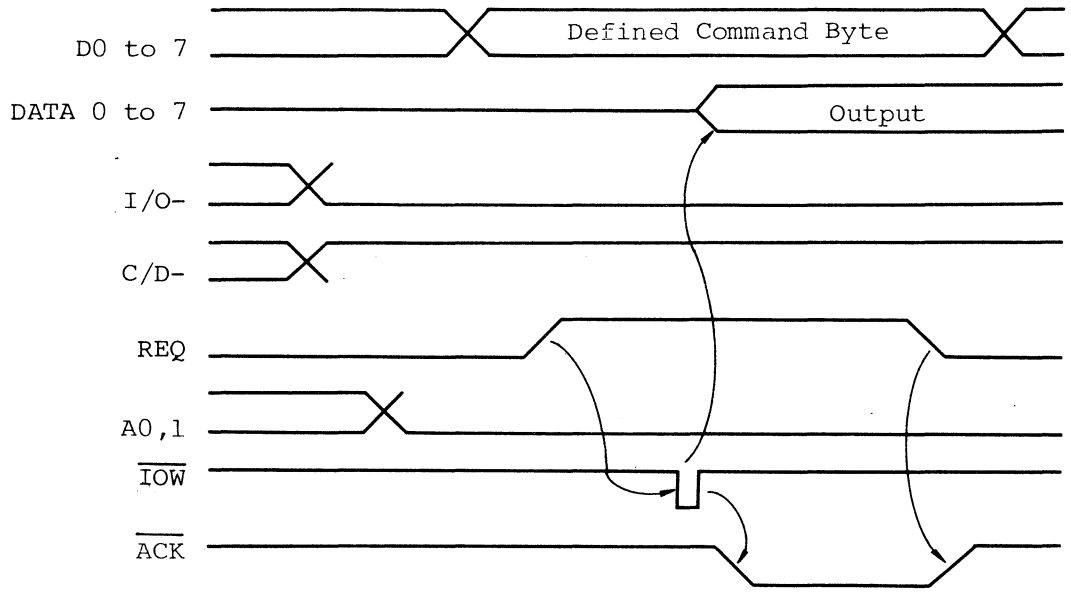
Select the controller before starting execution. When BUSY becomes active, terminate the selection.



4-1

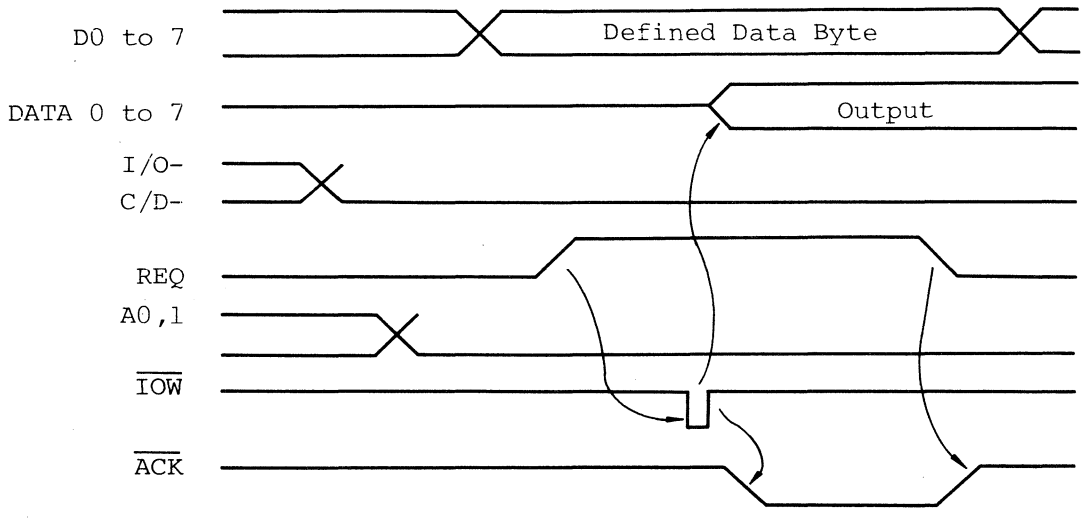
b. Command output (320H)

A request signal is received when the I/O and C/D signals each reach the "L" and "H" levels. When the command byte has been prepared to send to the controller in response to this, send an ACK signal.



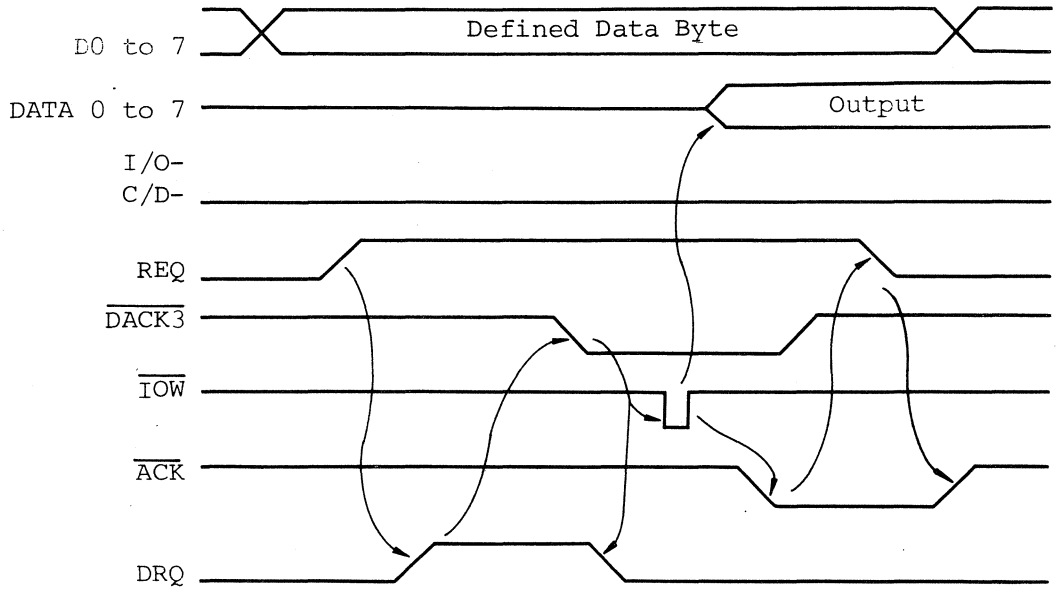
c. Data write (program mode) (320H)

A request signal is received when the I/O and C/D signals each reach the "L" level. When the data byte has been prepared to send to the controller in response to this, send an ACK signal.



d. Data write (DMA mode)

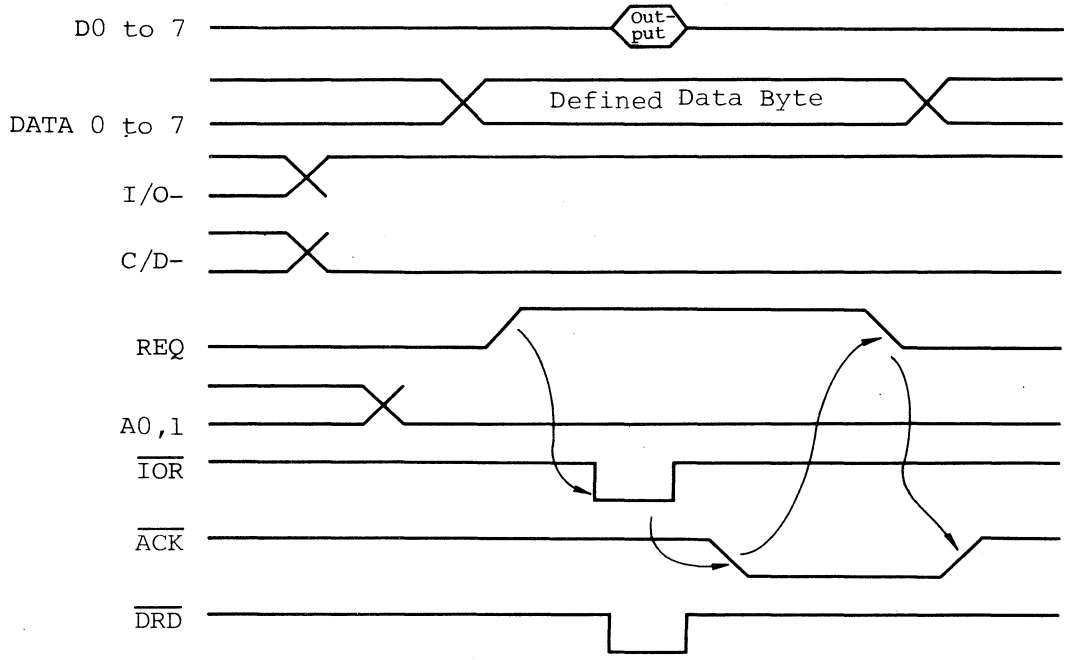
Set data bit 0 to "1" and record it on the mask register, then when a request signal is received, send a DRQ to begin DMA mode operation.



4-4

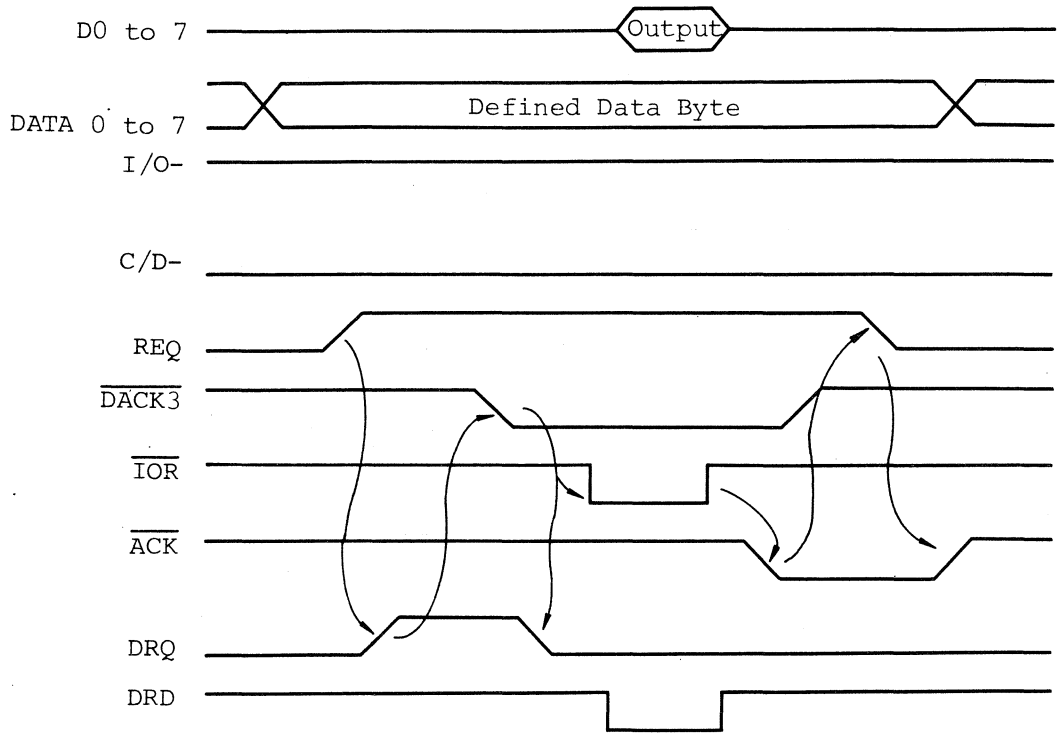
e. Data read (program mode) (320H)

A request signal is received when the I/O and C/D signals each reach the "L" and "H" levels. When the host computer has received the data byte in response to this, send an ACK signal.



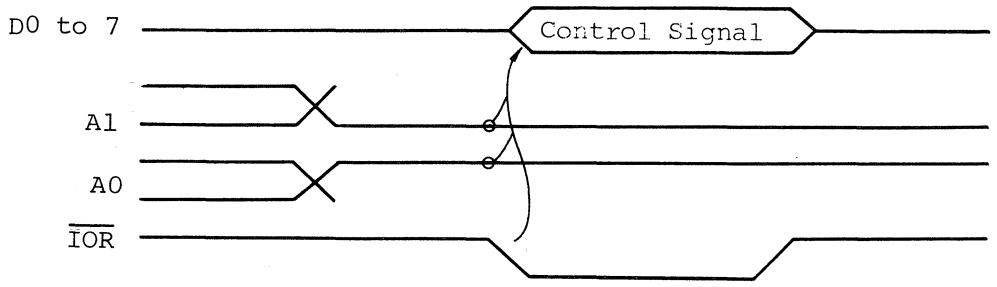
f. Data read (DMA mode)

Set data bit 0 to "1" and record it on the mask register, then when a request signal is received, send a DRQ to begin DMA mode operation.



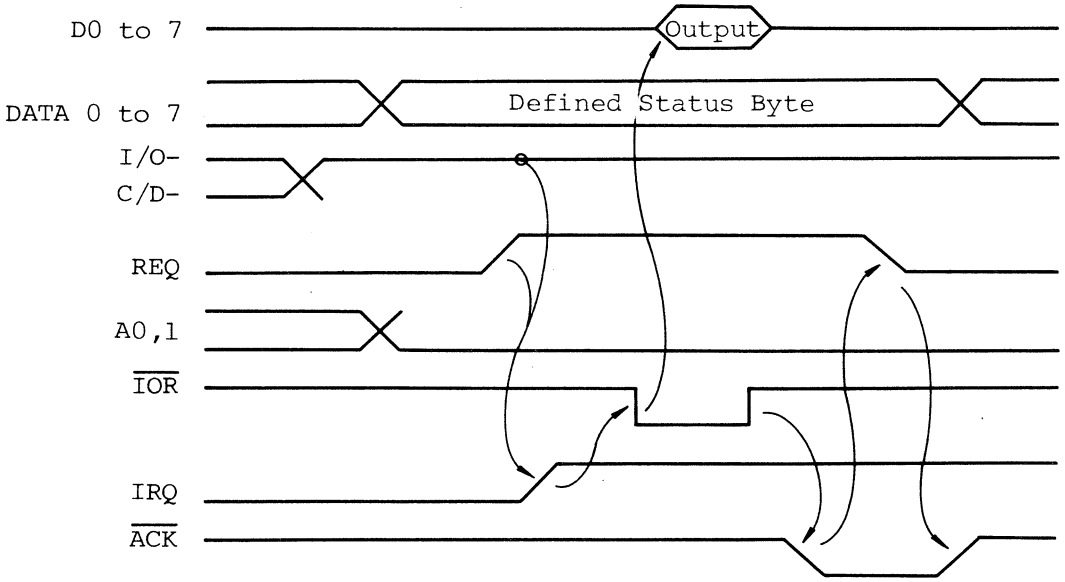
g. Status read (control signal) (321H)

Set the A0 and A1 signals to the "H" and "L" levels and read them so that the control signals REQ, I/O, C/D, BUSY, DRQ, and IRQ are read.



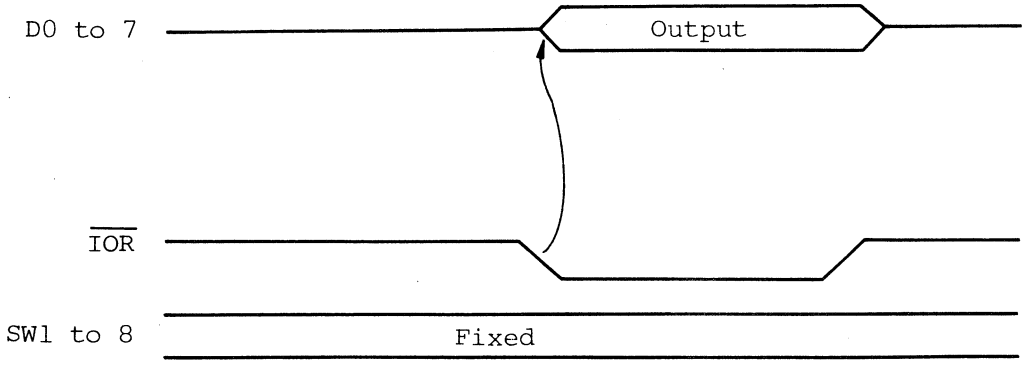
h. Status read (status byte) (320H)

When the controller has completed executing the command, it sets both the I/O and C/D to the "H" level and reads the status. The controller sends an ACK signal when the host computer has received the status byte.



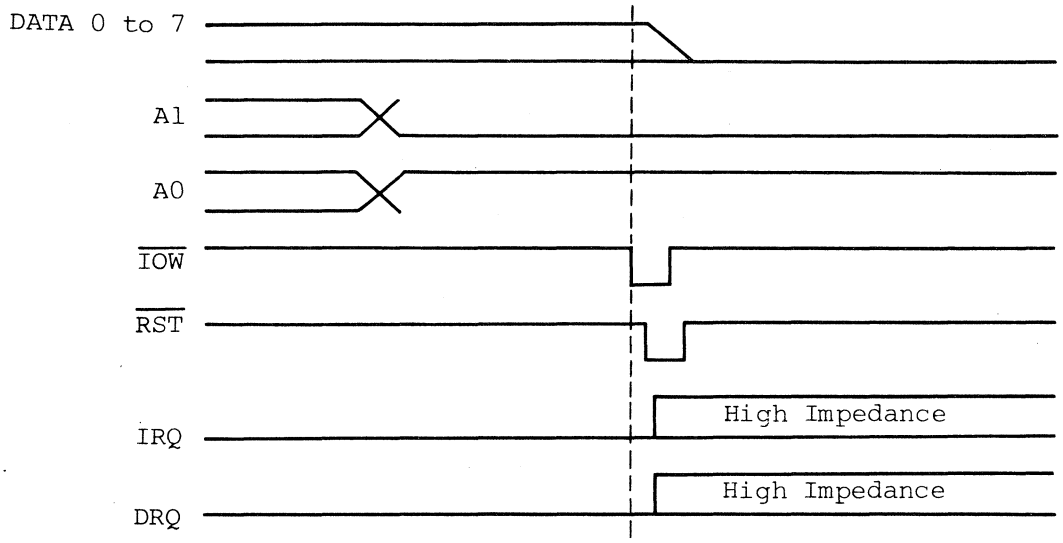
i. Switch read

The DIP switch status is read to D0 to 7.

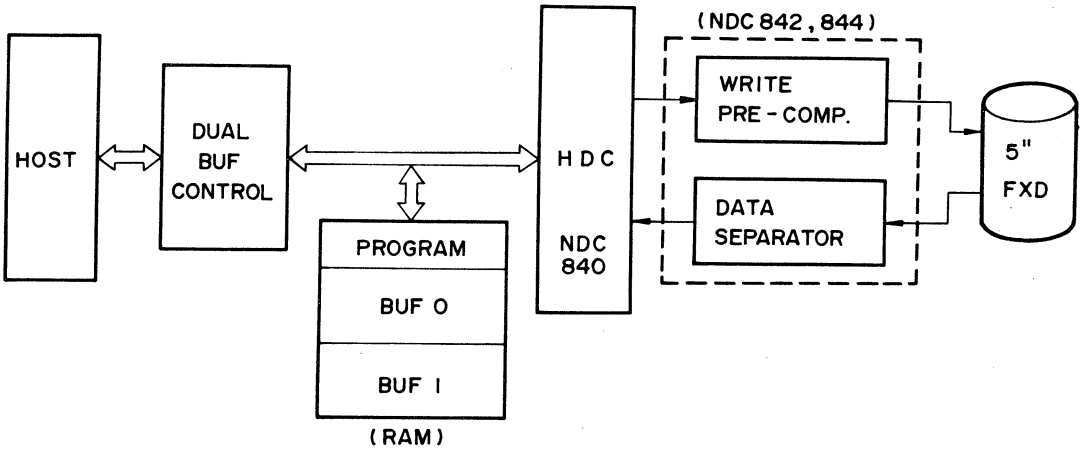


j. Reset

An IOW signal is received when A0 and A1 each reach the "H" and "L" levels.



4.2 Transmission Method



a. RAM

- o HDC program area
- o BUF0, BUF1 area

  Each buffer is a one-sector buffer.

  When a 2 kbyte-chip RAM is used, the maximum sector length is 512 bytes.

  Each buffer perform data transmission using the time-division mode.

b. Transmission speed for host computer and buffer

When transmitting data between the host and the 5-inch flexible disk drive, the data is temporarily stored in the buffer register to enable a freely selectable transmission speed. However, the sector interleave is determined by the transmission speed between the host and buffer. (For multisector mode)

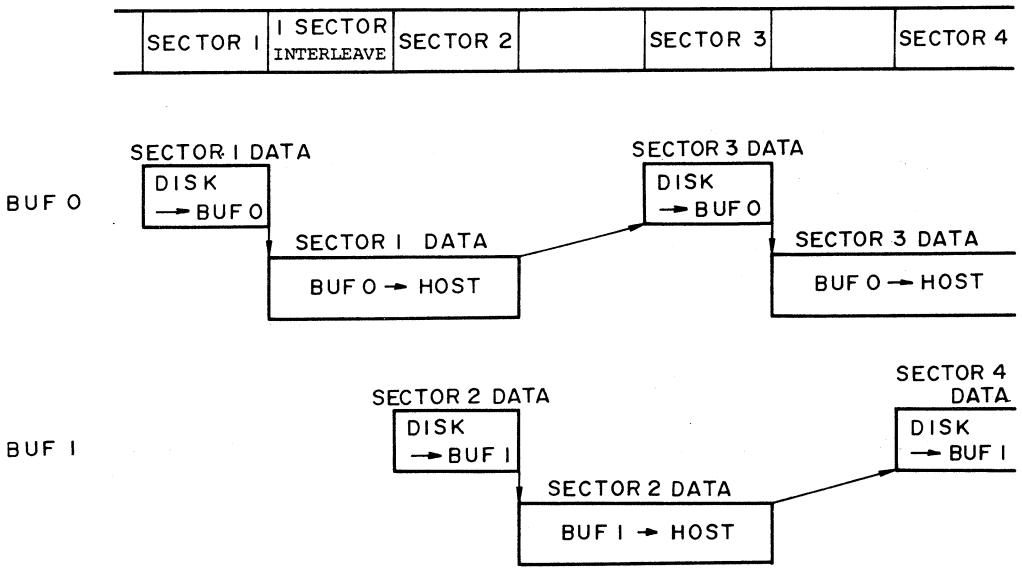
c. Dual buffer

When a dual buffer is used for the HDC, the host side's DMA transmission speed can be as fast (but not faster) than the disk drive's transmission speed, and even when the multisector mode is used, on-sector interleave transmission is possible with the host side's DMA transmission speed.

- o DMA transmission speed can be as fast (but not faster) then the disk drive's transmission speed.
- o The load for the host side hardware is light.
- o Cycle stealing and high-priority processing is possible for the host side.
- o Processing efficiency does not decrease when the multisector mode is used.

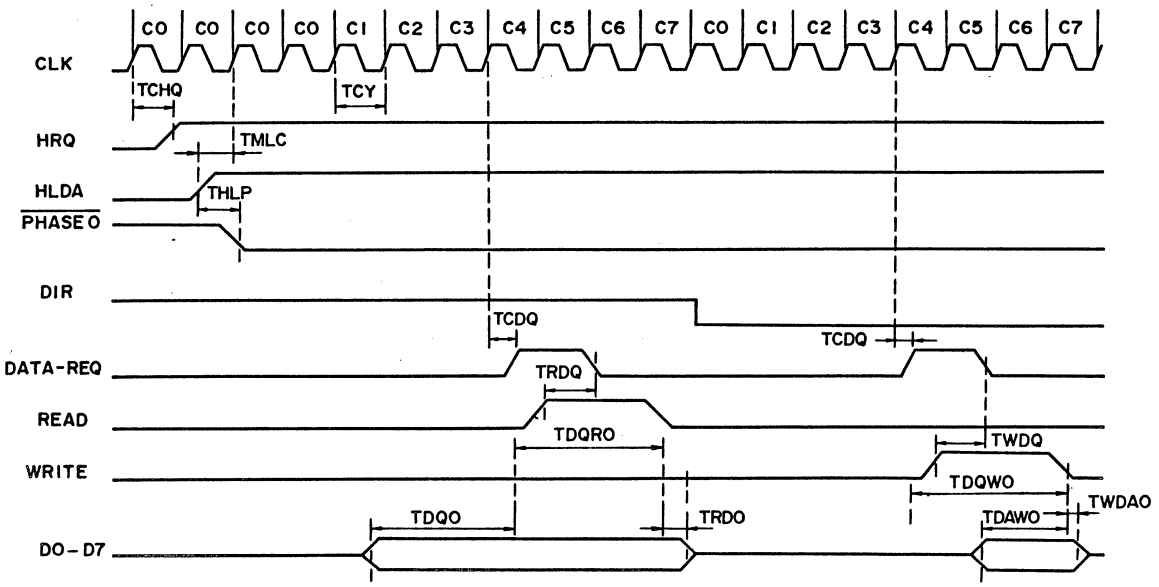
Example: Read data (from disk to host)

Disk drive transmission speed: 5M bit/s (1.6 µs/byte)
Host computer transmission speed: 3.2 µs/byte

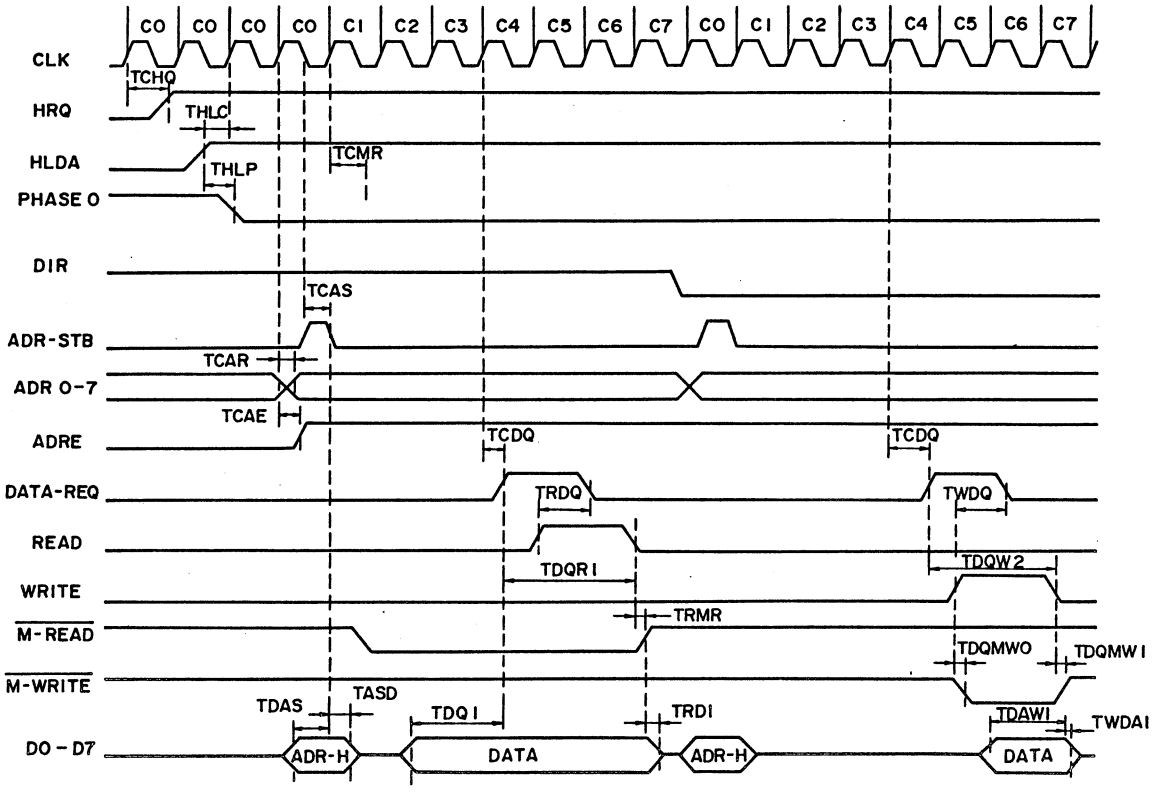


d. DMA transmission time chart

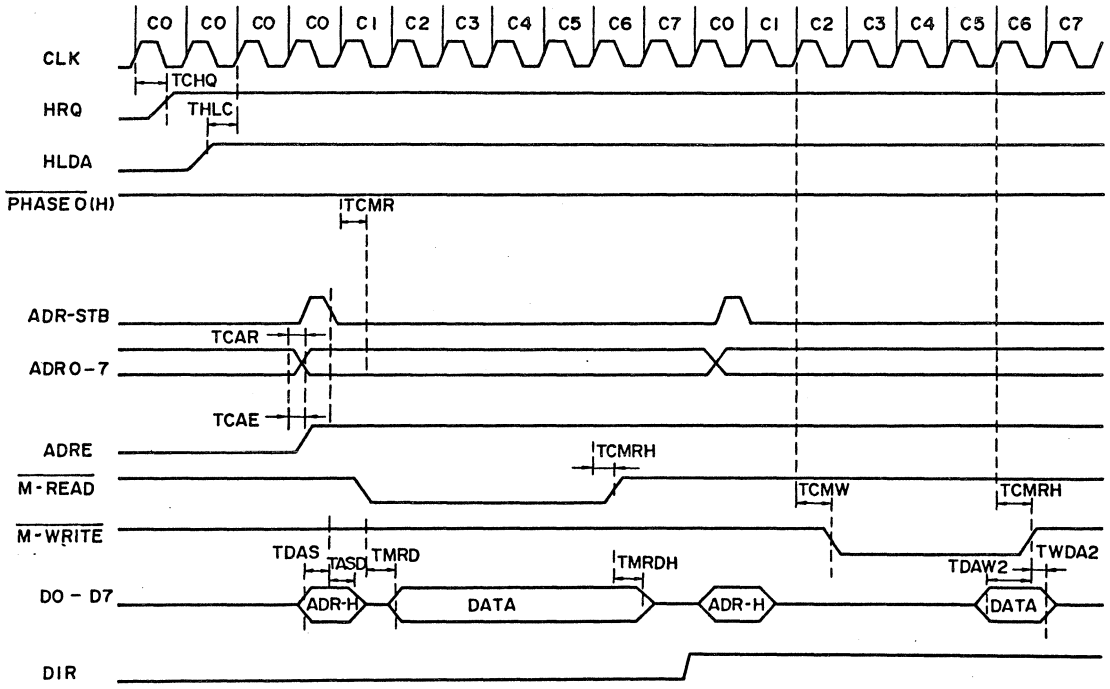
(1) Single mode, between disk and host



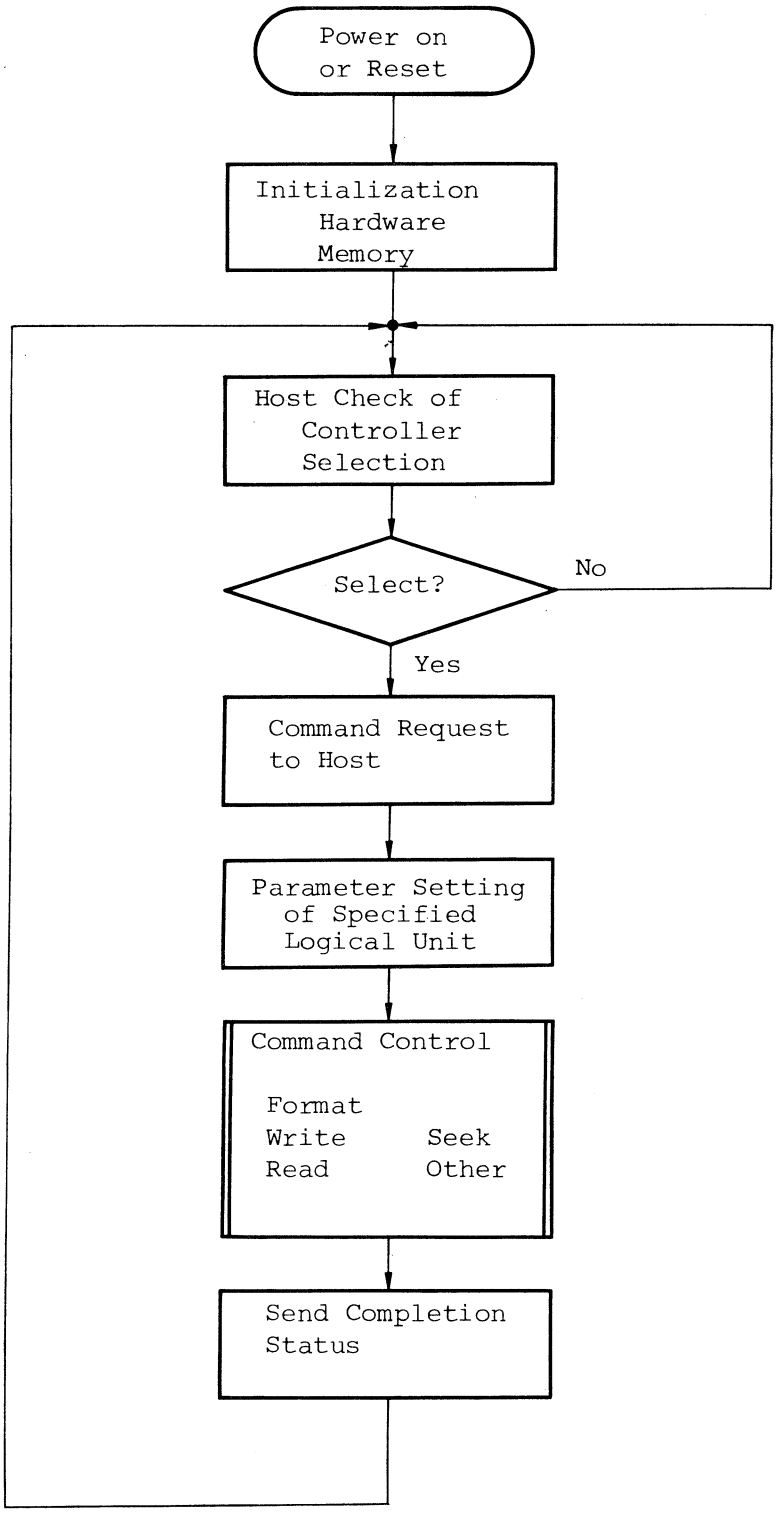
(2) Single mode, between memory (buffer) and host



(3) Single mode, between memory (buffer) and disk

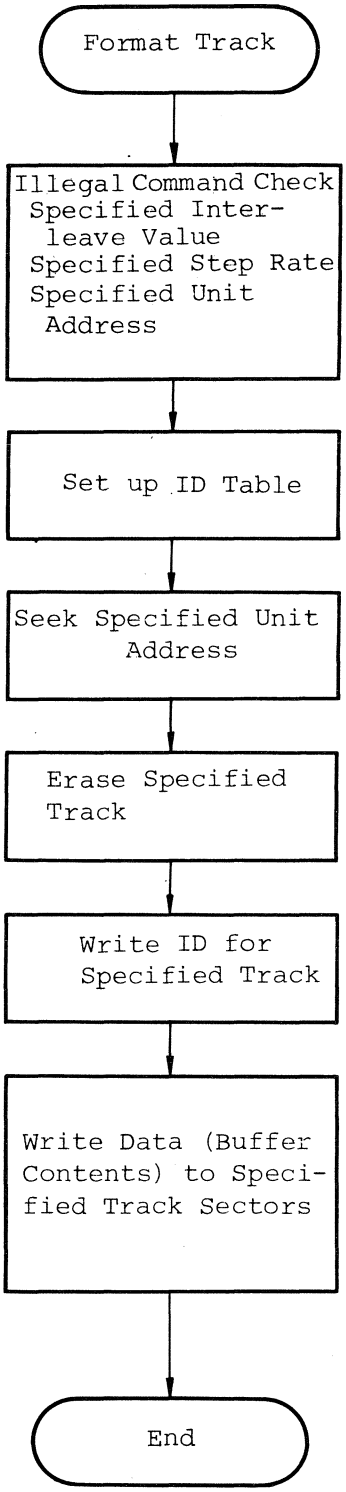


4.3 General Flowchart of Basic Operations



4.4 Main Command Flowchart

Format Track Command



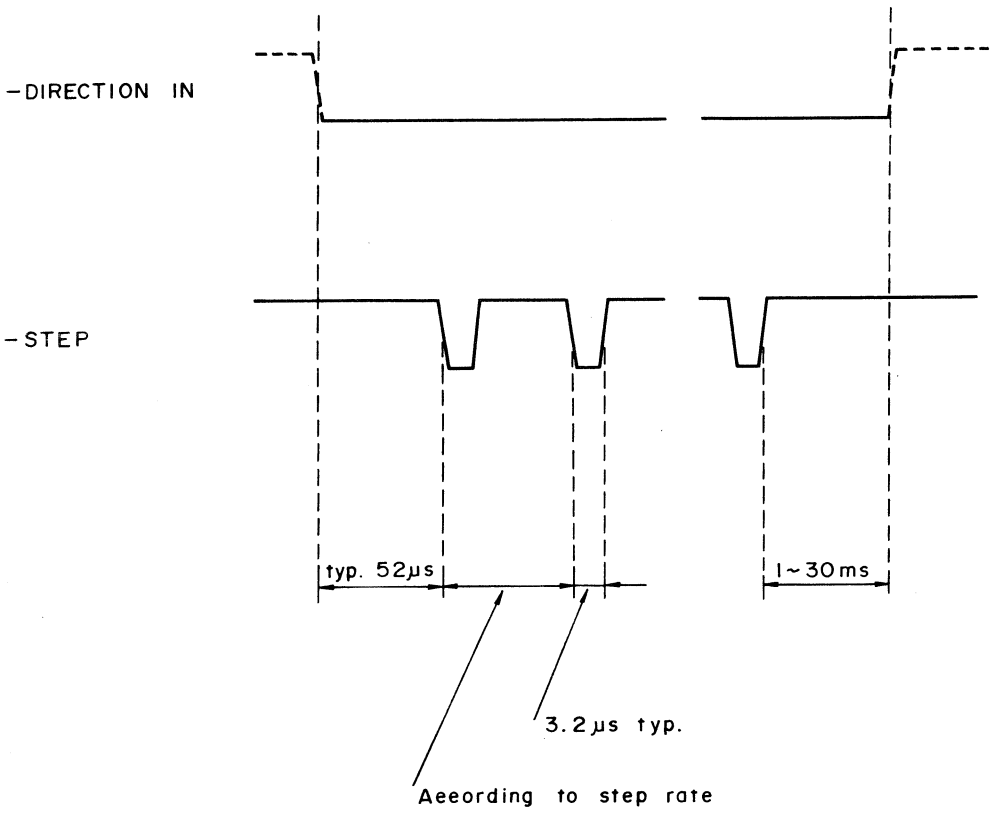
ID Table (Cylinder 001, head 02, interleave 5)

Cylinder	Head	Sector
0100	02	00
0100	02	07
0100	02	0E
0100	02	04
0100	02	0B
0100	02	01
0100	02	02
0100	02	0F
0100	02	05
0100	02	0C
0100	02	02
0100	02	09
0100	02	10
0100	02	06
0100	02	0D
0100	02	03
0100	02	0A

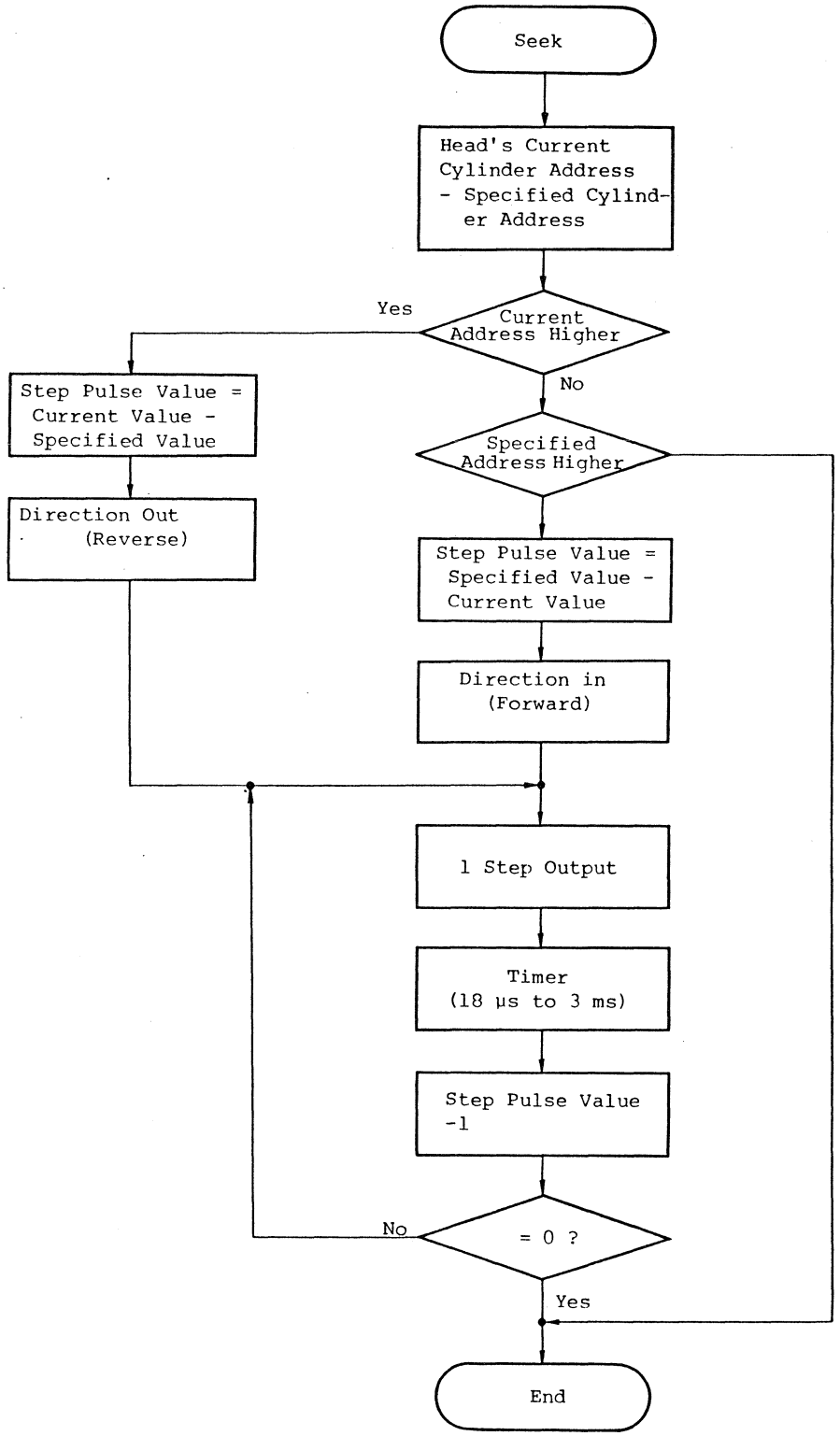
5. BASIC OPERATIONS

5.1 Seek Operation

The step pulse for the seek operation is produced by the FPU (NDC 840). The host issues a command to set the step rate value.



Seek Operation Flowchart:



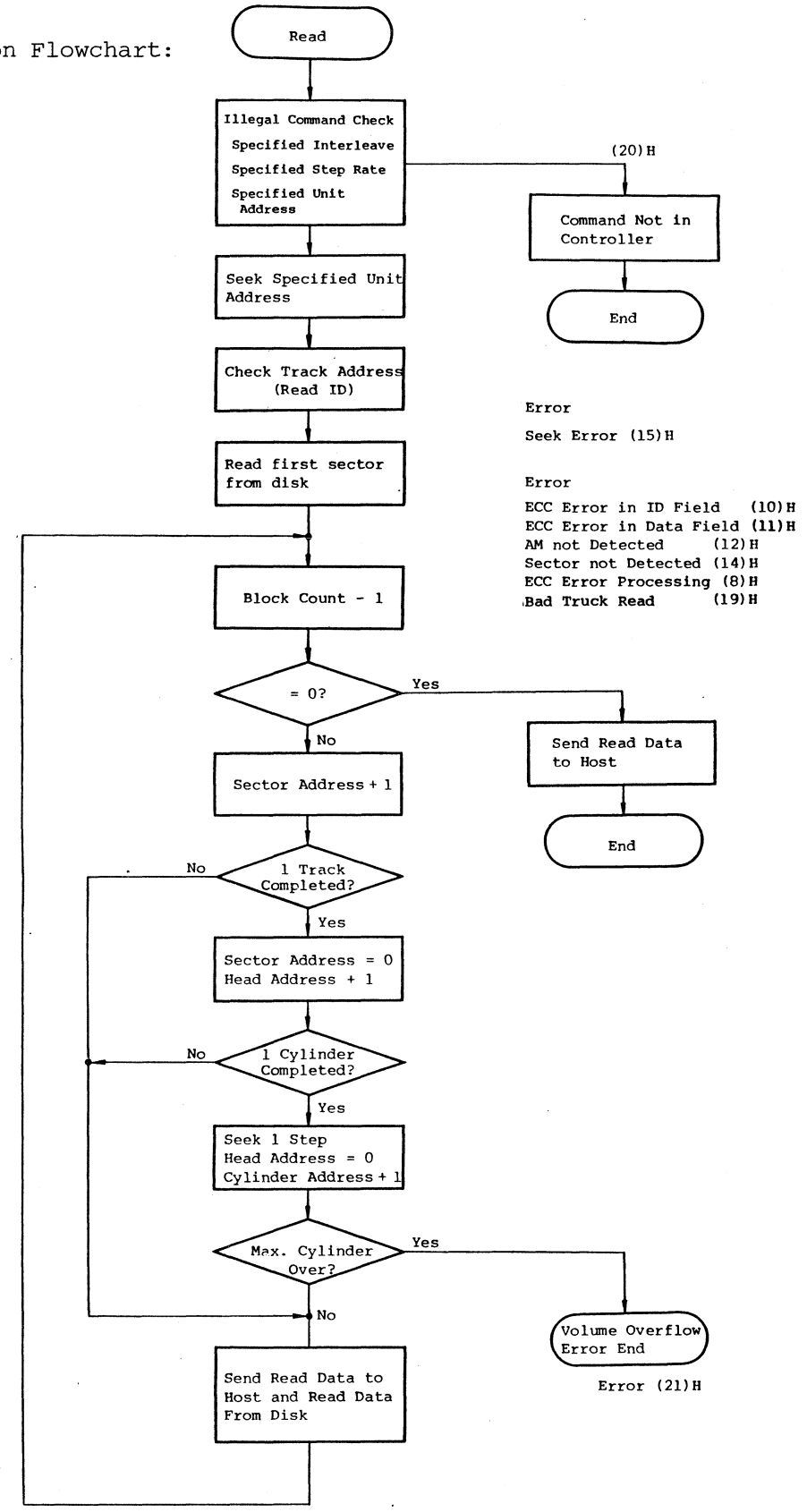
5.2 Read Operation

The data read operation begins with ID read to find the specified sector. Read the data field from where the appropriate ID field is found.

The MFM data read from the ID field and data field onto disk storage are first divided by the VFO LSi (NDC 842) into NRZ data and clock data and then are sent to the NDC 840 (serial-parallel convertor, error correction code). The data converted from serial to 8-bit parallel by the NDC 840 are sent to RAM by the NDC 840's DMA mode.

The NDC 840 executes error detection of read data, and if there are 11 bits or less of successive errors, it and the CPU Z-80 correct the error data.

Read Operation Flowchart:

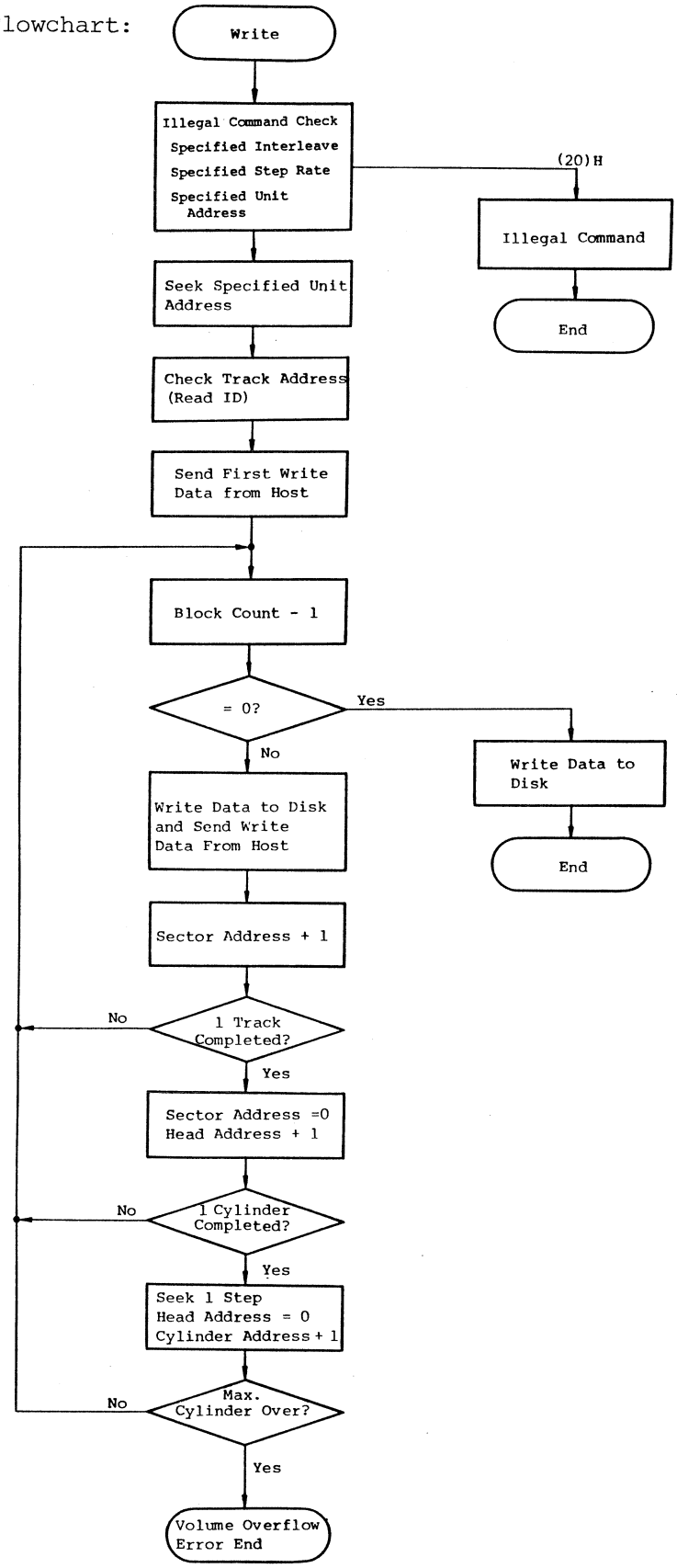


5.3 Write Operation

The data write operation beings with ID read to find the specified sector. Open a write gate and right the data at the place where the ID field is found.

The write data is sent from the host to RAM and from RAM to the NDC 840, where it is converted into serial data. Then, while the ECC (error correction code) generator generates the ECC, the data are sent to the MFM generator (NDC 842) for conversion into an MFM pattern. Finally, the data are sent to the disk. The ECC is tagged onto the end of the data and also sent to the disk.

Write Operation Flowchart:



6. DRIVE INTERFACE

6.1 Description of Drive Interface Signals

Control Signals:

a. $\overline{\text{REDUCED WRITE CURRENT}}$ CONT ⟶ Write current is descreased when this signal is low. Low when at cylinders 128 and under.

b. $\overline{\text{HEAD SELECT } 2^0 \text{ to } 2^2}$ CONT ⟶ A three-bit head address indicator.

c. $\overline{\text{WRITE GATE}}$ CONT ⟶ Write data is written to drive when this signal is low.

d. $\overline{\text{SEEK COMPLE COMPLETE}}$ CONT ⟶ When low, this signal indicates completion of seek operation. Read/write operations via $\overline{\text{READY}}$ signal are only possible when this signal is low.

e. $\overline{\text{TRACK0}}$ CONT ⟶ When low, this signal indicates that drive head has reached the outermost cylinder. Direction out (reverse) seek is executed until this signal is detected by the REZERO command. During the power on operation, the controller cannot transmit the $\overline{\text{DRDY}}$ signal until this signal has been detected.

f. $\overline{\text{WRITE FAULT}}$ CONT ⟶ This signal indicates abnormal condition in the disk drive. Read/write cannot be executed when this signal is low.

g. $\overline{\text{INDEX}}$ CONT ⟶ This is a pulse output once per disk revolution to indicate data track opening.

h. $\overline{\text{READY}}$ CONT ⟶ This signal indicates that the disk drive is operating normally. Seek, read, and write can only be executed when this signal is low.

i. $\overline{\text{STEP}}$ CONT ⟶ This pulse signal makes the head begin seeking. Each pulse seeks one cylinder. Use jumper plug inside board to select between 1 seek per pulse (normal mode) or high-speed seek using high-speed pulses (buffer mode).

j. $\overline{\text{DRIVE SELECT 1 to 4}}$ CONT ⟶ Use signal to select from among two or more disk drives connected to the controller. Up to two disk drives can be connected for each board mounted on the controller.
This signal is kept high (DE-SELECT status) except during seek, read, and write operations.

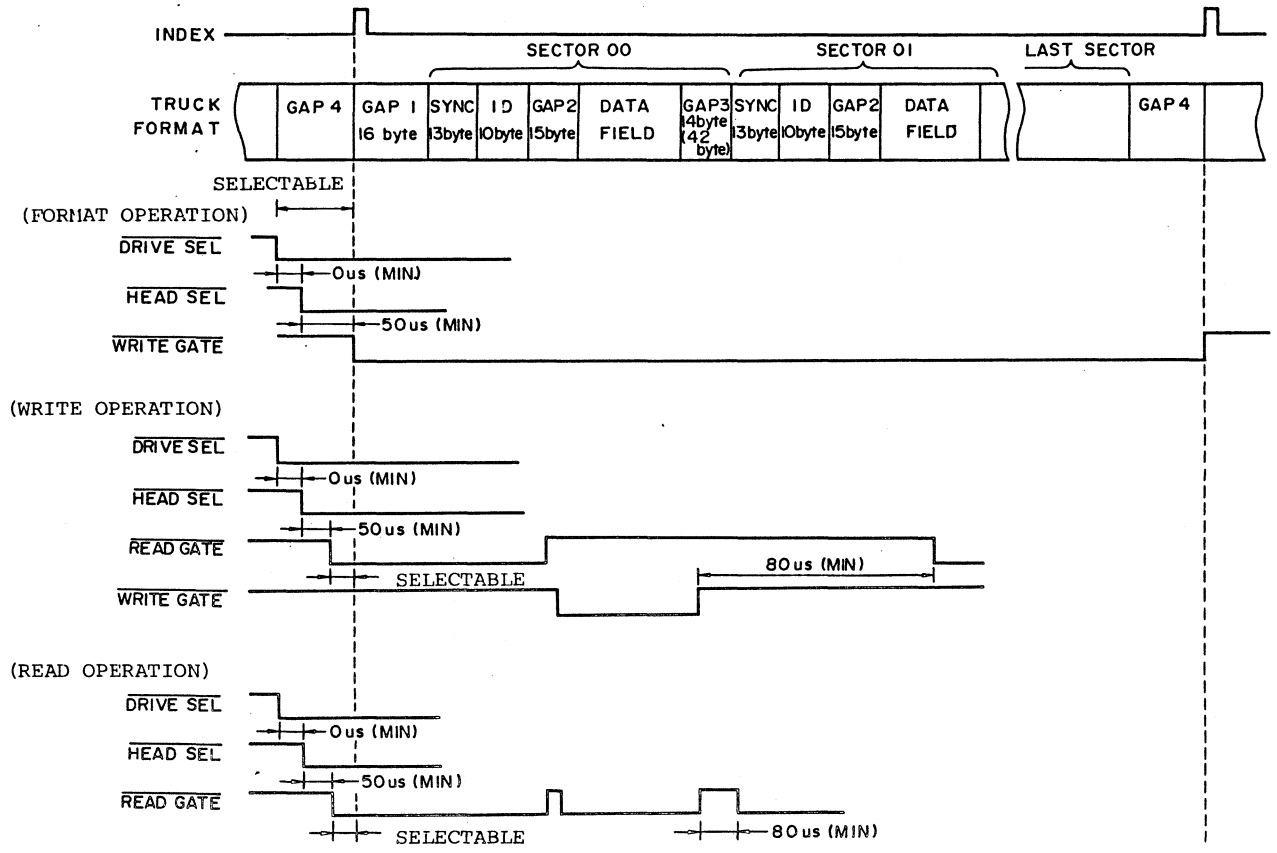
k. $\overline{\text{DIRECTION IN}}$ CONT ⟶ Use this signal to specify the head's seek direction. When this signal is low, the seek direction is forward (inward) and when high the seek direction is reverse (outward).

l. $\overline{\text{DRIVE SELECTED}}$ CONT ⟵ This signal is used to indicate the drive selected by one of the four $\overline{\text{DRIVE SELECT}}$ signals.

Data signals:

a. ±MFM WRITE DATA CONT ⟶ This data signal is written to the drive. It is sent as a differential signal.

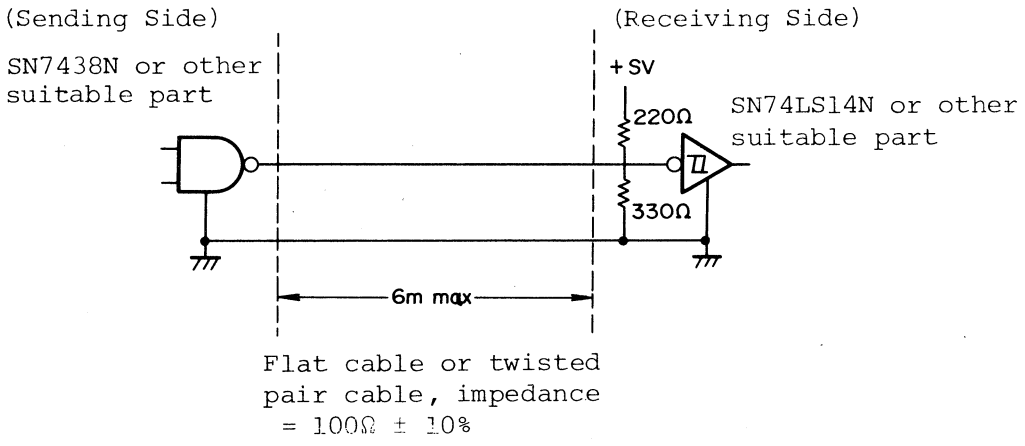
b. ±MFM READ DATA CONT ⟵ This data signal is read from the drive. It is sent as a differential signal.



6.2 Drive Interface Driver and Receiver

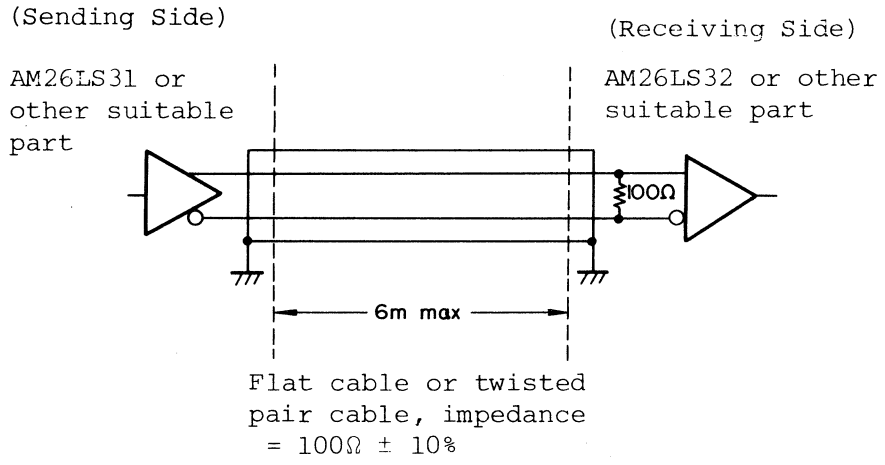
a. Control signals

The driver/receiver configuration for all of the CN1 connector's signals and the CN2 connector's DRIVE SELECTED signal is shown below.



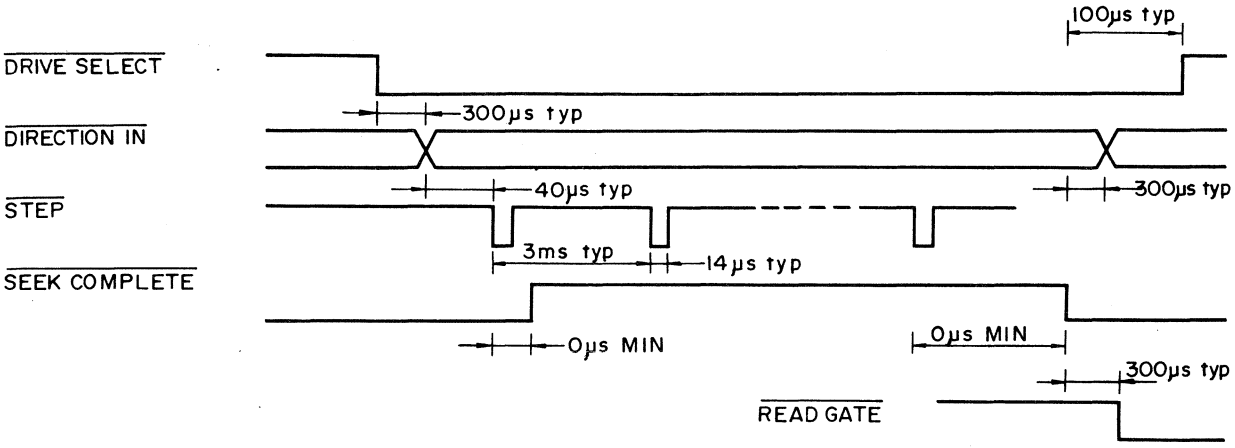
b. Data signals

The driver/receiver configuration for the CN2 connector's MFM READ/WRITE DATA signal is shown below.

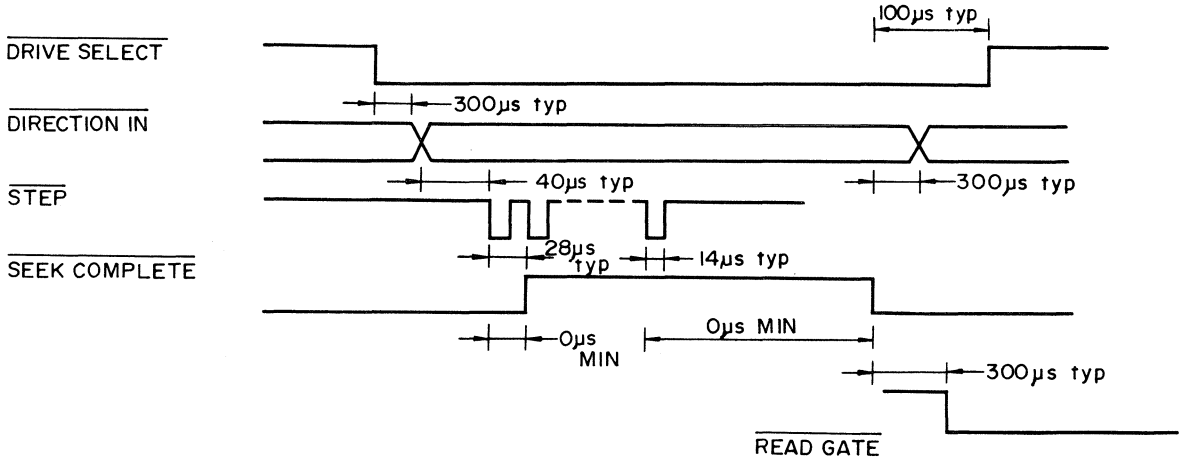


6.3 Drive Interface Timing

a. Seek operation (normal mode seek)



b. Seek operation (buffer mode seek)



7. ENCODER/DECODER AND DATA SEPARATOR

7.1 General Description

The NDC 842 has been developed to facilitate the interface between the magnetic disk drive and the controller. Incorporating all of the best features of the Tl NDC 10 (MB15546), this interface chip is able to connect the controller to a 5" disk drive and a floppy disk drive.

7.2 Principal Features

a. VFO data separation function

b. National PLL circuit and NDC 844/847 phase comparator are built-in.

c. MFM and FM recording method and response

d. Missing data pattern detection function

e. MFM write compensation support

f. 5 VDC single power supply

7.3 Operation of NDC 842

a. Reset input

(1) RST (RESET)

Clear all registers including the high active register and initialize the NDC 842 chip.

b. Clock input

(1) 4FC (4F-CLOCK)

This clock is used for internal control and for the write circuit. When set to half cycles, this clock is output as 2-F CLOCK.

(2) VCK (VCO-CLOCK)

This clock outputs the clock pulse for the VCO circuit. During the read operation, the clock generated by this clock is output as READ-CLOCK.

c. Clock output

(1) 2FC (2F-CLOCK)

This is the clock signal output by the 4F clock when set to 2-minute cycles.

(2) RCK (READ-CLOCK)

During the read operation, the READ-CLOCK pulse is output by the VCO-CLOCK. The READ-DATA signal is output synchronous to the READ-CLOCK pulse. At times other than during the read operation, the 2F clock's negative signal is output. 2F clock signal switching is set temporarily by the high level signal.

RAW DATA input and the DRIVE SELECT signal (RR1, RR2, and DS1) are used to input the receiver output for the data sent from the disk drive. The DSI signal is used to select between the RR1 and R2 signal. Their correlation is shown below.

DS1	RR1 & RR2
Low level	Selects RR1
High level	Selects RR2

(The leading edges of RR1 and RR2 are based on risen pulses. This is set by the disk drive.)

d. Read control signals

(1) RGT (READ-GATE)

This control signal is a HIGH ACTIVE gate signal for all read operations.

(2) AE0 (AM-ENABLE0)

Also a HIGH ACTIVE signal, this is active when needed for searching for missing block data (address marks). This signal is active not only during read operations, but also, in combination with the active AMW signal, is active to enable writing of index marks.

e. Write control signals

(1) WGT (WRITE-GATE)

This control signal is a HIGH ACTIVE gate signal for all write operations.

(2) AMW (AM-WRITE)

Also a HIGH ACTIVE signal, this is active when needed for writing data which include missing blocks (address marks). This signal and the AE1 signal are required simultaneously for writing index marks on floppy disks.

f. Other input and output related to read operations

(1) RDM (RAW-DATA-M)

This is a LOW ACTIVE signal which must be input to acknowledge the internal SYNC field, and it is the gate signal for the RAW DATA bit counter. Consequently, when the SYNC field is set as "00," a control signal that is at low level during detection of 1F cycle patterns (in MFM mode) or 2F cycle patterns (in FM mode).

(2) DD0, DD1, DD2 (DELAY-DATA 0, 1, & 2)

All of the leading edges are risen pulses. Although the raw data selected by the DS1 signal is fundamentally output as DD0, as long as there is no DD1 input, the DD0 can be a high level signal.

Alghough the DD1 signal is for correcting the width of raw data and inputs a pulse to delay only the data width portion.

Example: for a 5 Mbit/s disk drive, it inputs a delay of 10 to 25 ns.

The DD2 signal is input to the built-in phase comparator. Usually, the appropriate delay time is half the 4F-CLOCK cycle based on the DD0 signal.

(3) RSE, RSN, and RSL (READ-STROBE E, N, & L)

All of the leading edges are risen pulses. All three of these signals are input through the same gate by the strobe input to the internal data separator.

Because different disk drives have different inner and outer read margins for their media, the RSN is preset to the center and the data is input at locations offset in either direction from the center. The mode setting selection a type of strobe to help (when necessary) with error recovery.

The appropriate delay time, about the same as the DD2 time (half the 4F-CLOCK cycle), is set as the center.

g. Other input and output related to write operations

(1) WDN and WMD (WRITE-DATA-NRZ & WRITE-MODIFIED-DATA)

When serial NRZ data synchronized to the 2F clock is input to WDN from the HDC or FDC, the data modified by MFM or FM is output as WMD.

(2) PED, PND, and PLD (PRECOMPENSATION-EARLY, NORMAL, & LATE-DATA)

In MFM mode, only precompensation selections EXT and YES are effective.

The amount of compensation varies according to the type of disk drive.

During internal mode, when the compensation amount is not enough, PED is input for data offset to the inside of the center (PDN) and PLD for data offset to the outside of the center. WMD output must be used for generation of all three areas of data.

(3) DWD (DISK-WRITE-DATA)

This signal must be input to the disk interface output driver for serial data output including write precompensation, missing blocks, etc.

h. Write precompensation detection pattern

The precompensation bit patterns are shown in the table below.

-- HOW TO READ THE TABLE --

The bit patterns are monitored by the bit shift register, with the bit timing indicated by the third bit.

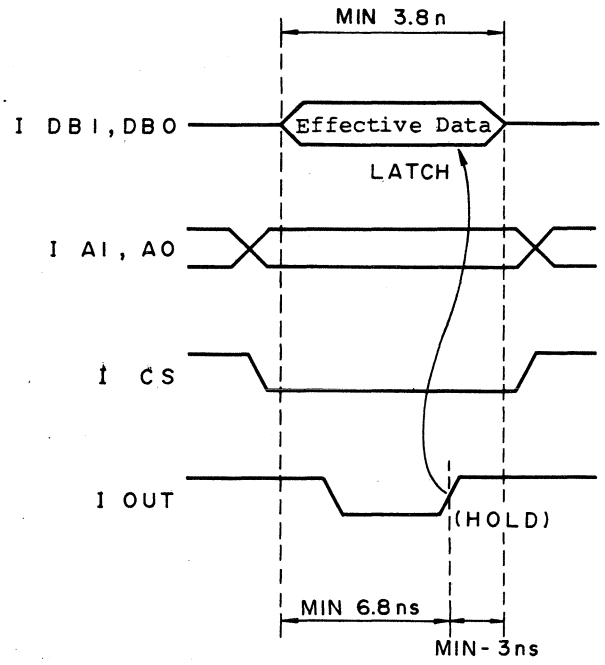
	Bit Pattern	Precompensation Data
0	0 0 0 0	NORMAL CLOCK
1	0 0 0 1	EARY CLOCK
2	0 0 1 0	NORMAL DATA
3	0 0 1 1	LATE DATA
4	0 1 0 0	———
5	0 1 0 1	———
6	0 1 1 0	EARY DATA
7	0 1 1 1	NORMAL DATA
8	1 0 0 0	LATE CLOCK
9	1 0 0 1	NORMAL CLOCK
A	1 0 1 0	NORMAL DATA
B	1 0 1 1	LATE DATA
C	1 1 0 0	———
D	1 1 0 1	———
E	1 1 1 0	EARY DATA
F	1 1 1 1	NORMAL DATA

* These data are effective during MFM mode.

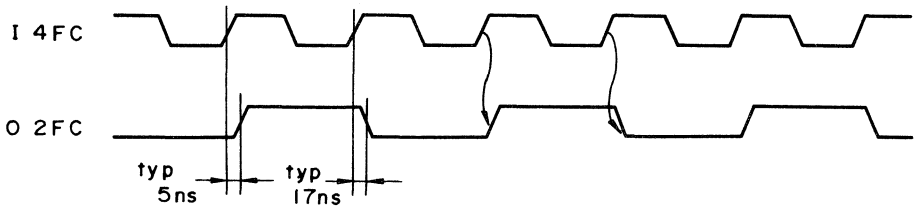
When internal precompensation is selected, 10 ns ±30% of precompensation is added.

7.4 Timing

a. Input of mode setting

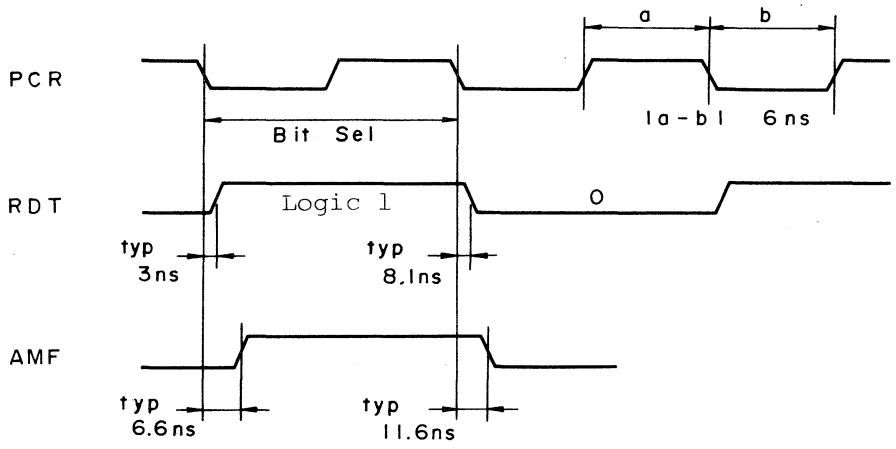


b. 4F clock input and 2F clock output

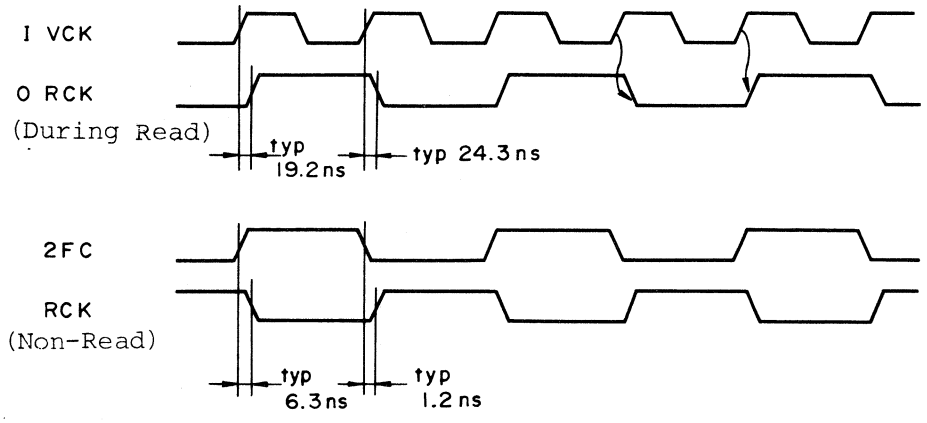


c. Read input and output

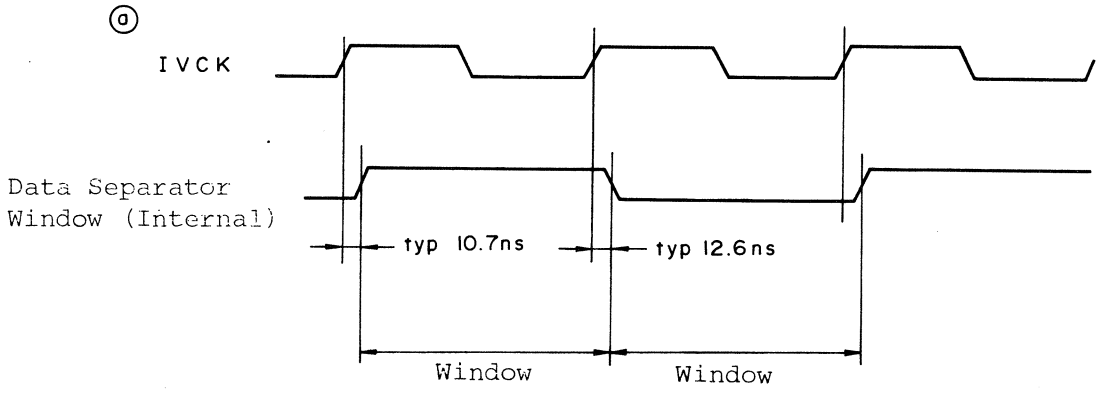
(1) Read clock and NRZ output data

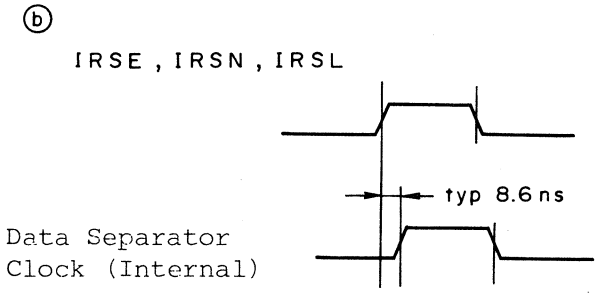


(2) Read clock (during read and non-read)



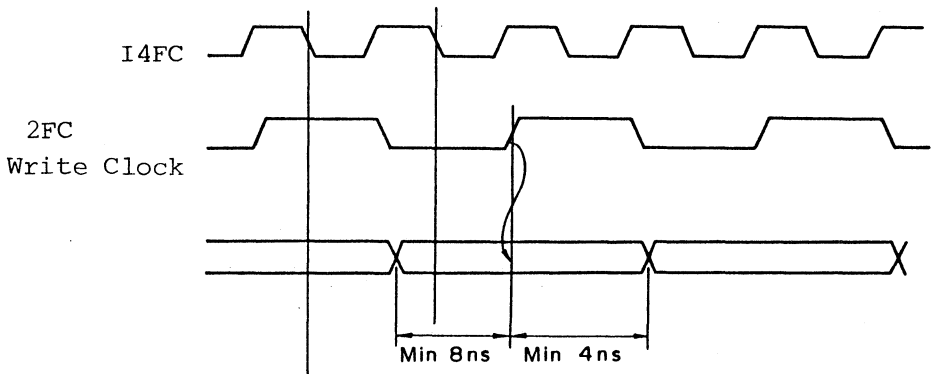
(3) iVCK and read strobe (iRSE, iRSN, and iRSL)



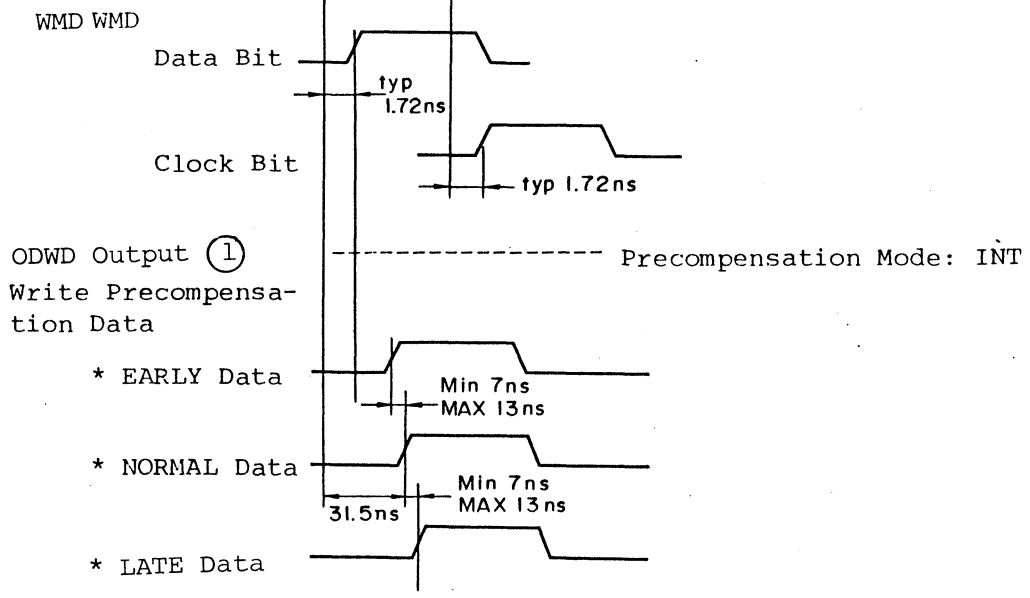


d. Write input and output

(1) Write clock and NRZ input data

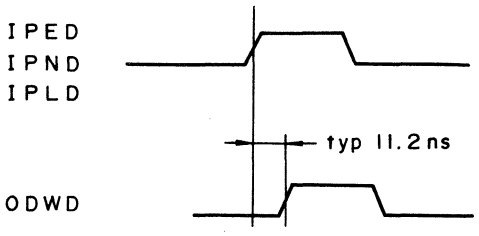


(2) MFM data



* Clock bit is the same for EARLY, NORMAL, and LATE data.

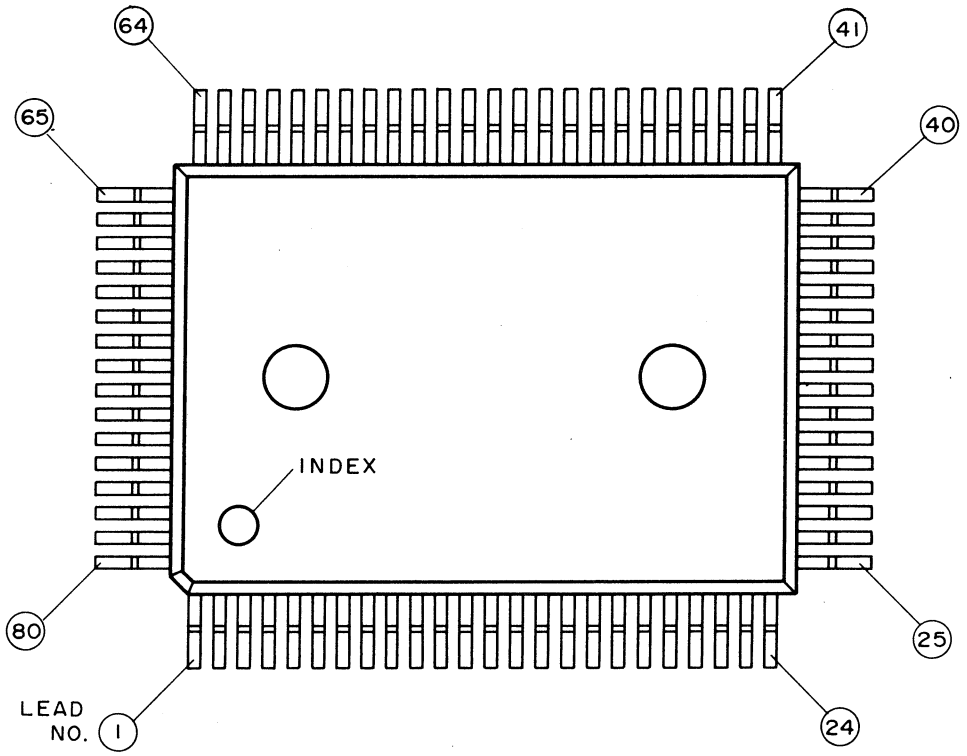
ODWD output ② ..... Precompensation mode: EXT



8. LSI SPECIFICATION

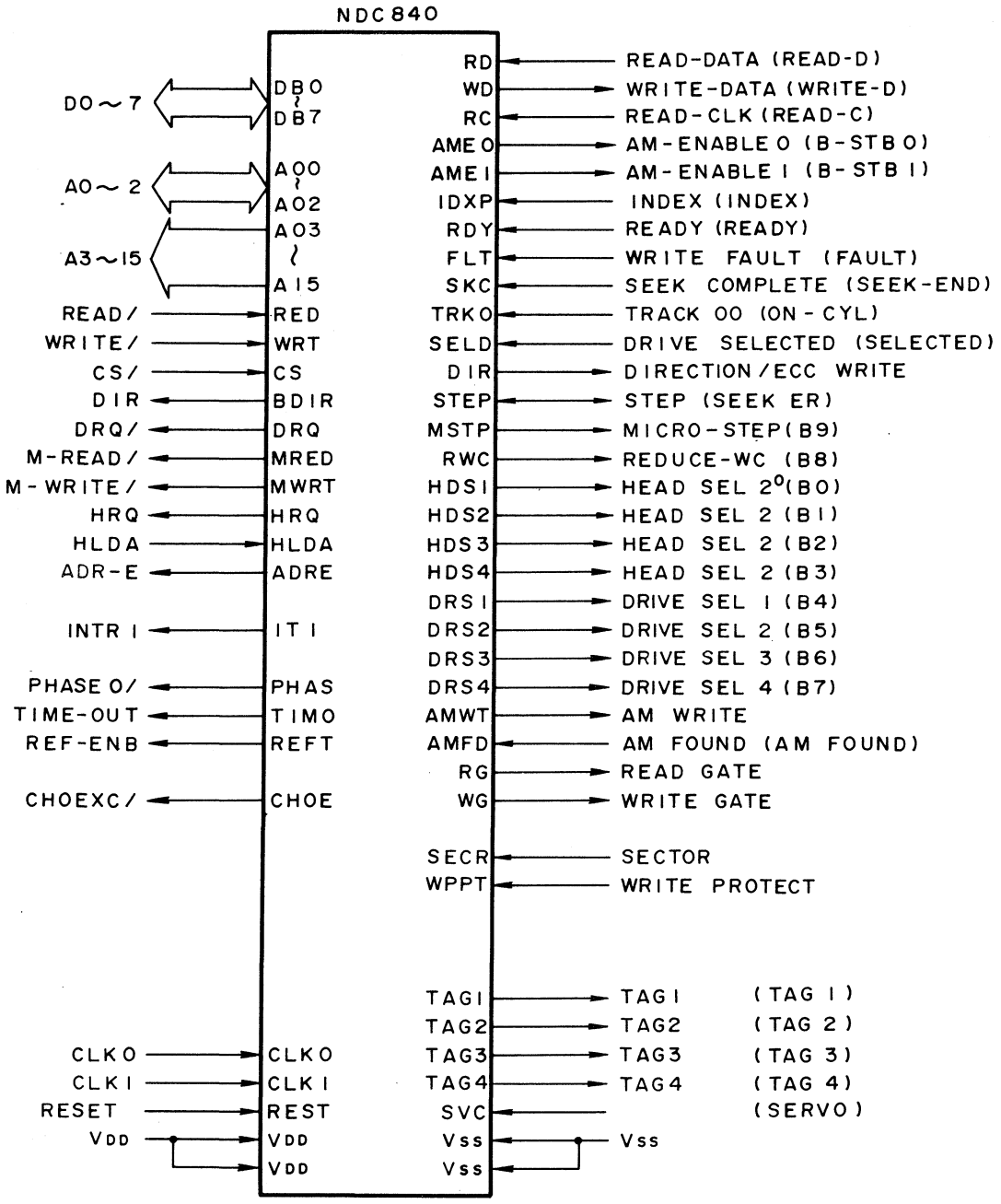
8.1 NDC 840

a. Pin assign



Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	O	HRQ	21	I	AMFD	41	O	DRS1	61	I/O	DB0
2	I	HLDA	22	O	RG	42	O	DRS2	62	O	A15
3	O	MRED	23	O	WG	43	O	DRS3	63	O	A14
4	O	MWRT	24	I	IDXP	44	O	DRS4	64	O	A13
5	I	RED	25	I	RDY	45	I	SECP	65	O	A12
6	I	WRT	26	I	FLT	46	I	WPRT	66	O	A11
7	O	IT1	27	I	SKC	47	O	TAG1	67	O	A10
8	O	BDIR	28	I	TRK0	48	O	TAG2	68	O	A09
9	O	DRQ	29	I	SELD	49	O	TAG3	69	O	A08
10	O	ADRE	30	O	DIR	50	O	TAG4	70	O	A07
11	I	CLK0	31	I/O	STEP	51	I	RD	71	O	A06
12	-	VSS	32	I	RC	52	-	VSS	72	I	CS
13	I	CLK1	33	-	VDD	53	O	WD	73	-	VDD
14	O	PHAS	34	I	SVC	54	I/O	DB7	74	I	REST
15	O	TIMO	35	O	MSTP	55	I/O	DB6	75	O	A05
16	O	REFT	36	O	RWC	56	I/O	DB5	76	O	A04
17	O	CHOE	37	O	HDS1	57	I/O	DB4	77	O	A03
18	O	AME0	38	O	HDS2	58	I/O	DB3	78	I/O	A02
19	O	AME1	39	O	HDS3	59	I/O	DB2	79	I/O	A01
20	O	AMWT	40	O	HDS4	60	I/O	DB1	80	I/O	A00

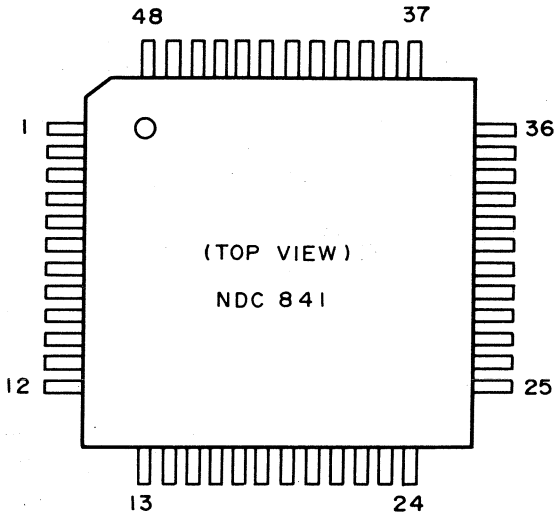
b. Interface Signals



* ( ): Used to control SMD interface signals.

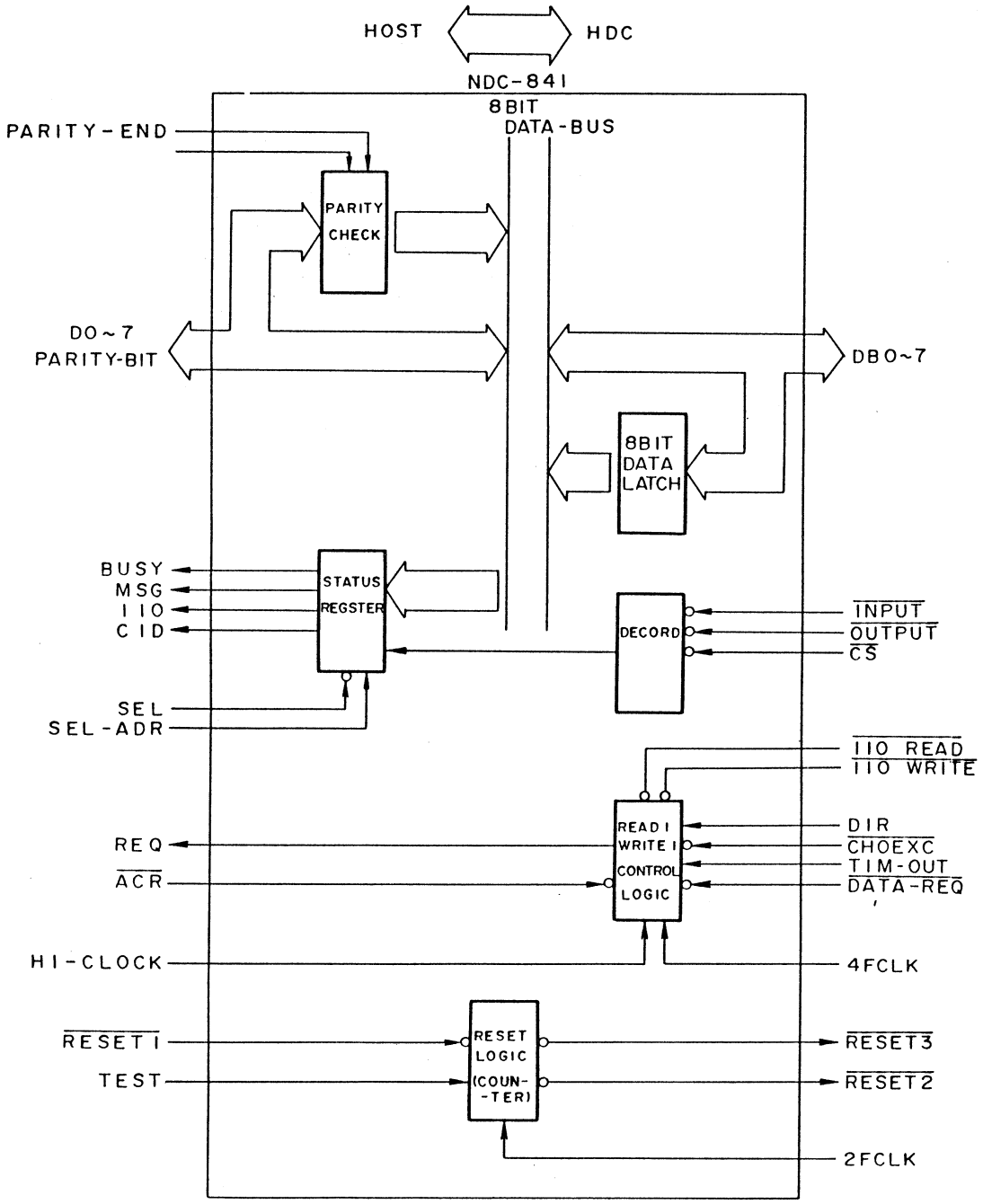
8.2 NDC 841

a. Pin assign



Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I/O	DB3	13	I	SEL-ADR	25	I/O	D2	37	I	$\overline{\text{CHQEXC}}$
2	I/O	DB2	14	I	PARITY ENB	26	I/O	D1	38	I	$\overline{\text{D-REQ}}$
3	I/O	DB1	15	I	EVEN/ODD	27	I/O	D0	39	I	TIM OUT
4	I/O	DB0	16	I	$\overline{\text{ACK}}$	28	I	HI-CLOCK	40	O	$\overline{\text{IO-READ}}$
5	I	2FCLK	17	I	$\overline{\text{SEL}}$	29	I	TEST	41	O	$\overline{\text{IO-WRITE}}$
6		GND	18	I	RESET	30	O	$\overline{\text{RESET3}}$	42	O	IFCLK
7	I	4FCLK	19		VCC	31		GND	43		VCC
8	O	BUSY	20	I/O	D7	32	I	$\overline{\text{RESET2}}$	44	I/O	DATA PARITY
9	O	MSG	21	I/O	D6	33	I	$\overline{\text{INPUT}}$	45	I/O	DB7
10	O	REQ	22	I/O	D5	34	I	$\overline{\text{OUTPUT}}$	46	I/O	DB6
11	O	I/$\overline{\text{O}}$	23	I/O	D4	35	I	$\overline{\text{CS}}$	47	I/O	DB5
12	O	C/$\overline{\text{D}}$	24	I/O	D3	36	I	DIR	48	I/O	DB4

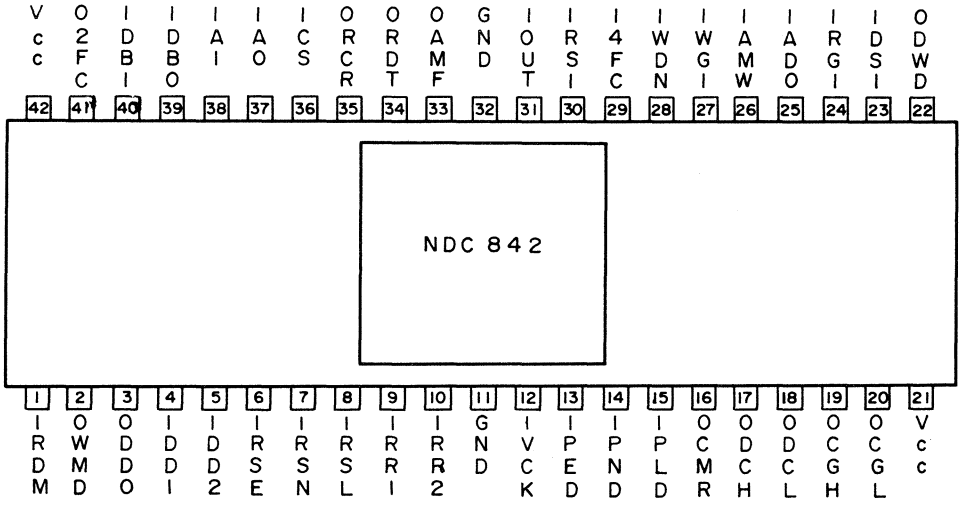
b. Block diagram



8.3 NDC 842

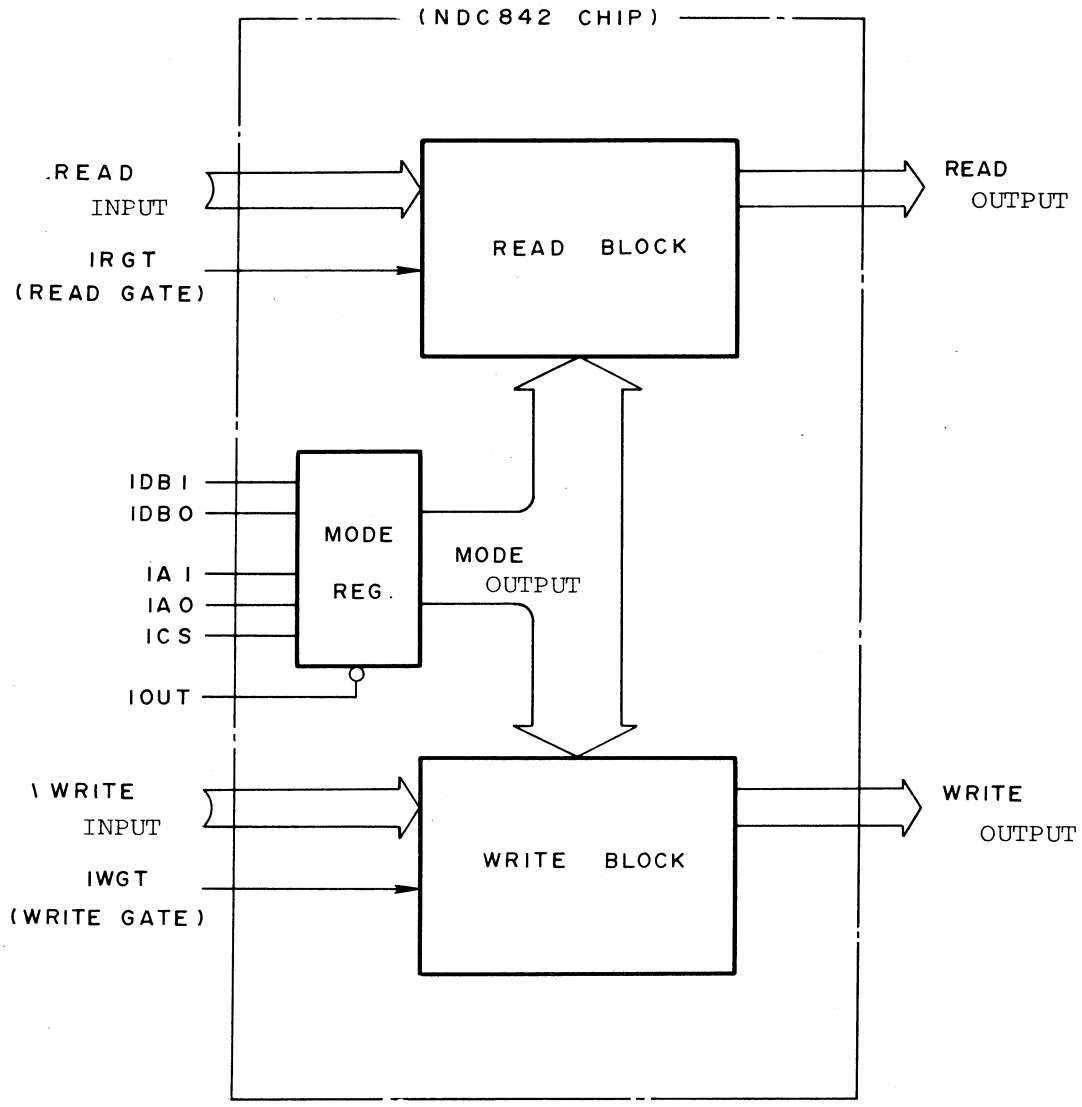
a. Pin assign

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	IRDM	11	GND	22	ODWD	32	GND
2	OWMD	12	IVCK	23	IDS1	33	OAMF
3	ODD0	13	IPED	24	IRGT	34	ORDT
4	IDD1	14	IPND	25	IAE0	35	ORCK
5	IDD2	15	IPLD	26	IAMW	36	ICS
6	IRSE	16	OCMP	27	IWGT	37	IA0
7	IRSN	17	ODCH	28	IWDN	38	IA1
8	IRSL	18	ODCL	29	14FC	39	IDR0
9	IRR1	19	OCGH	30	IRST	40	IDR1
10	IRR2	20	OCGL	31	IOUT	41	02FC
		21	VCC			42	VCC

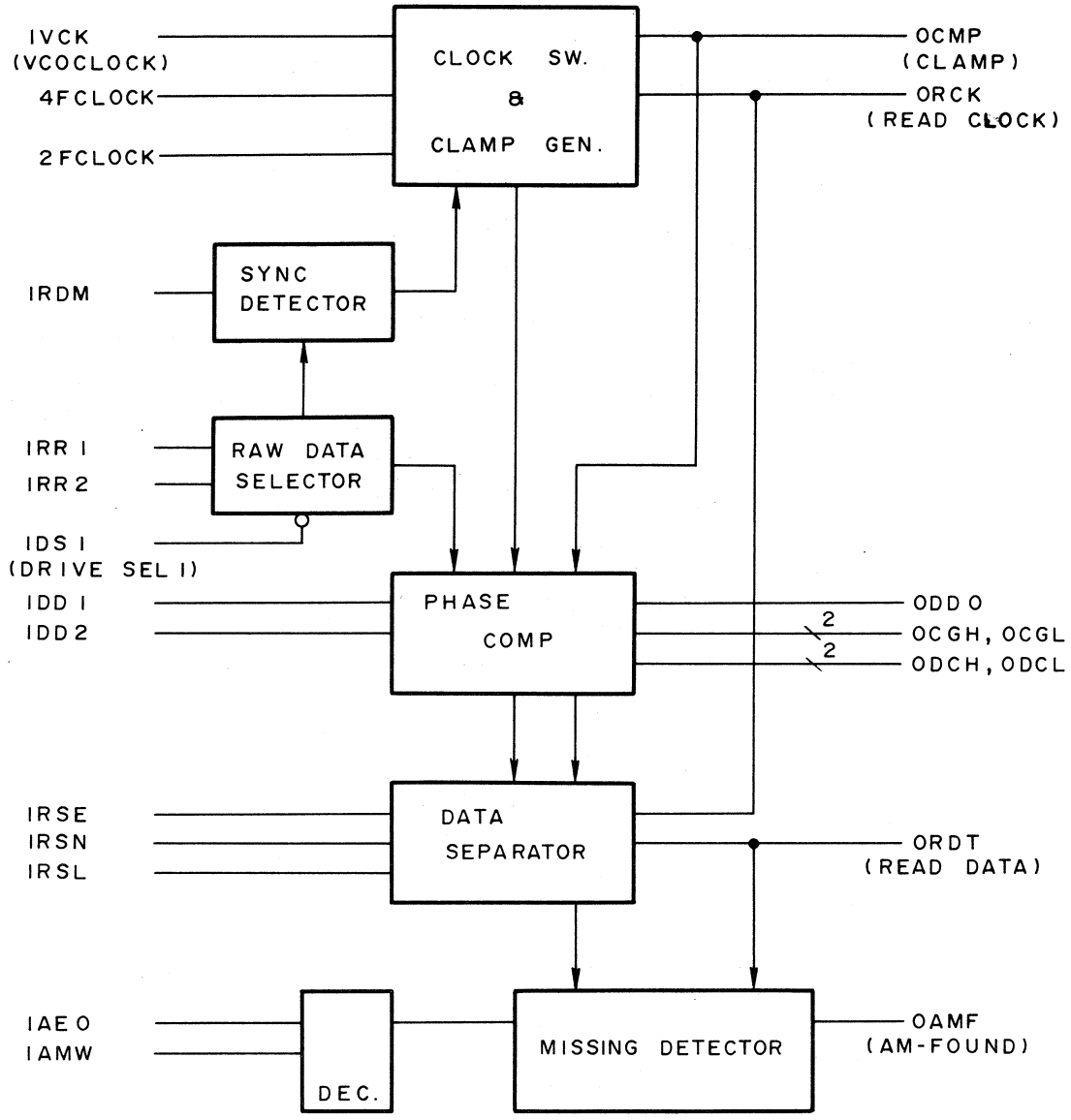


b. Block diagram

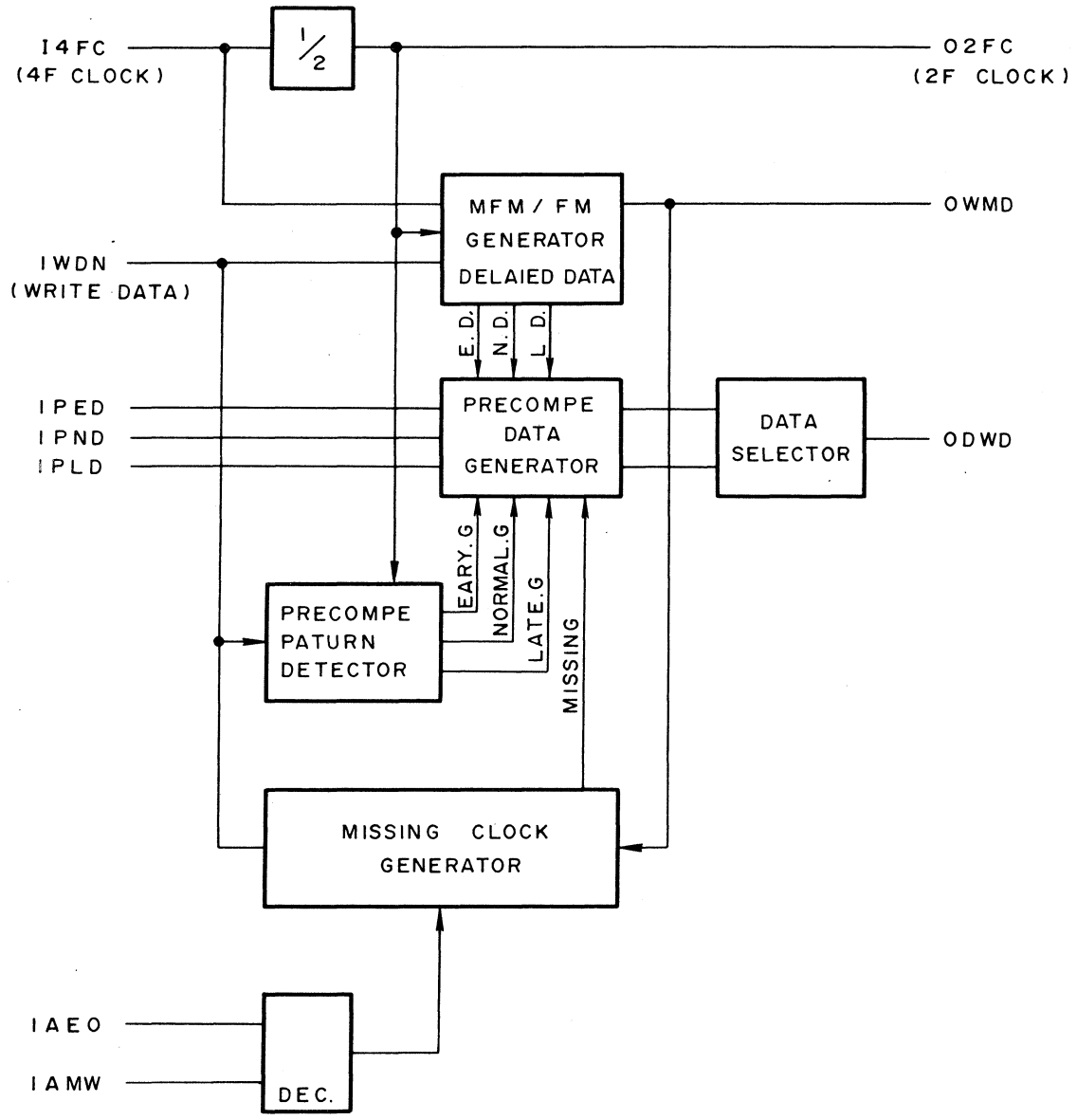
(1) Condiguration



(2) Read

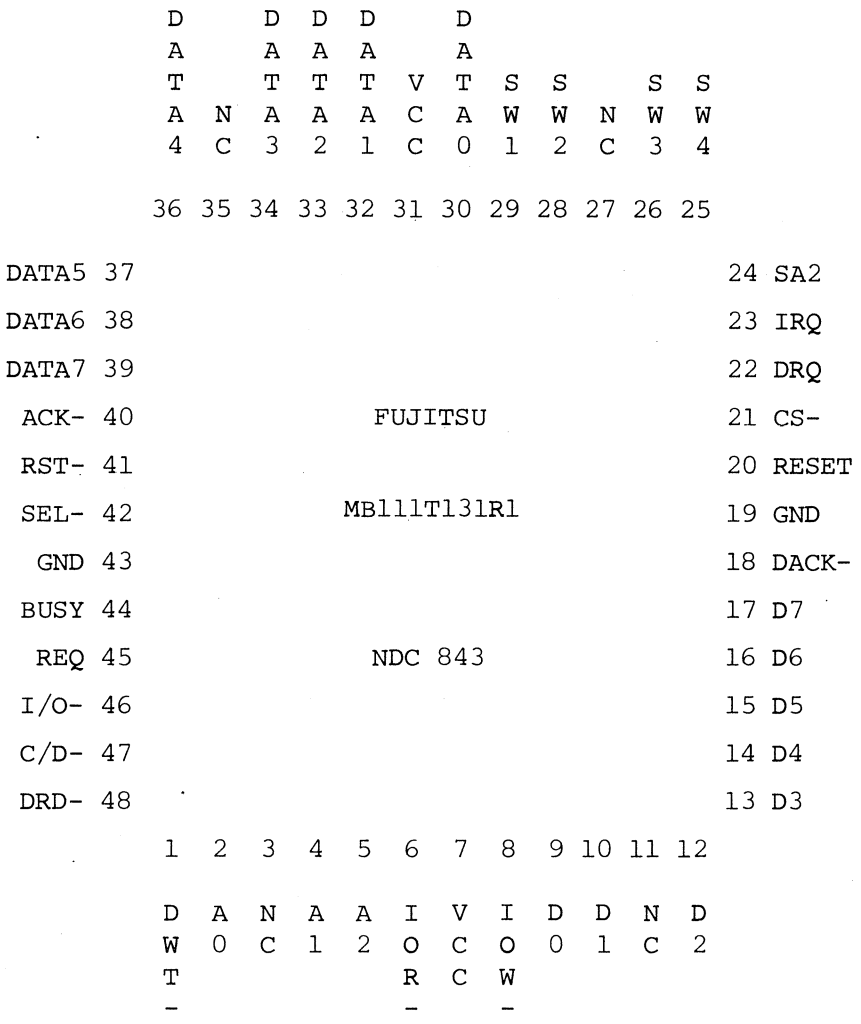

IVCK
(VCOCLOCK)
4FCLOCK
2FCLOCK
CLOCK SW.
&
CLAMP GEN.
OCMP
(CLAMP)
ORCK
(READ CLOCK)
IRDM
SYNC
DETECTOR
IRR 1
IRR 2
RAW DATA
SELECTOR
IDS 1
(DRIVE SEL 1)
IDD 1
IDD 2
PHASE
COMP
ODD 0
2
OCGH, OCGL
2
ODCH, ODCL
IRSE
IRSN
IRSL
DATA
SEPARATOR
ORDT
(READ DATA)
IAE 0
IAMW
DEC.
MISSING DETECTOR
OAMF
(AM-FOUND)

(3) Write


I4FC
(4F CLOCK)
1/2
O2FC
(2F CLOCK)
MFM / FM
GENERATOR
DELAIED DATA
OWMD
IWDN
(WRITE DATA)
E.D.
N.D.
L.D.
IPED
IPND
IPLD
PRECOMPE
DATA
GENERATOR
DATA
SELECTOR
ODWD
EARY.G
NORMAL.G
LATE.G
MISSING
PRECOMPE
PATURN
DETECTOR
MISSING CLOCK
GENERATOR
IAEO
IAMW
DEC.

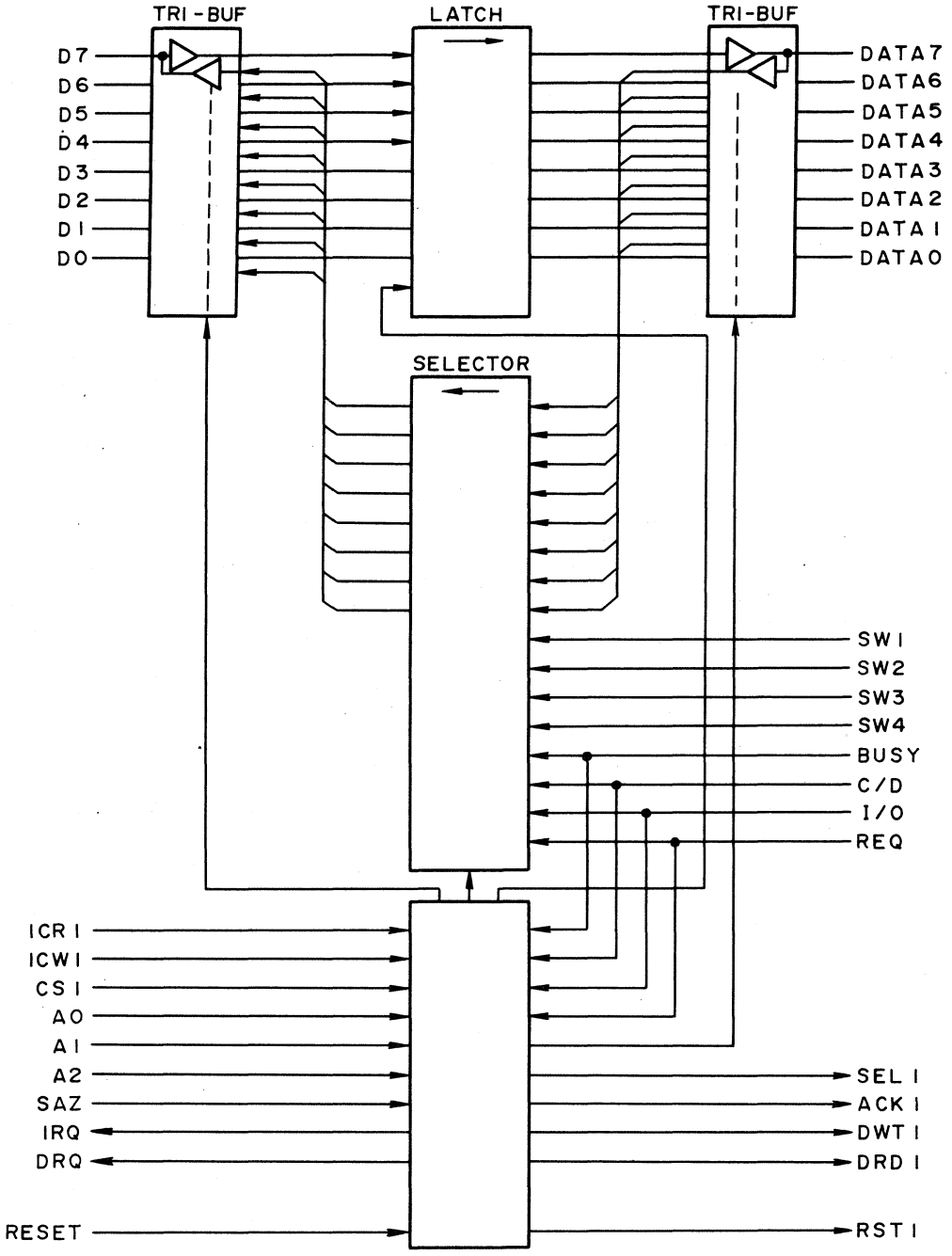
8.4 NDC 843

a. Pin assign



Pin	Signal		Pin	Signal		Pin	Signal		Pin	Signal	
1	DWT-	ODRD	13	D3	BS04	25	SW4	LSW4	37	DATA5	BS10
2	A0	IA0L	14	D4	BS03	26	SW3	LSW3	38	DATA6	BS09
3	(NC)		15	D5	BS02	27	(NC)		39	DATA7	BS08
4	A1	IA1L	16	D6	BS01	28	SW2	LSW2	40	ACR-	OACK
5	A2	IA2L	17	D7	BS00	29	SW1	LSW1	41	RST-	ORST
6	IOR-	IIOR	18	DACK-	IDA3	30	DATA0	BS15	42	SEL-	OSEL
7	Vcc		19	GND		31	Vcc		43	GND	
8	IOW-	LIOW	20	RESET	ODRQ	32	DATA1	BS14	44	BUSY	IBSY
9	D0	BS07	21	CS-	ODRQ	33	DATA2	BS13	45	REQ	IREQ
10	D1	BS06	22	DRQ	IRET	34	DATA3	BS12	46	I/O-	IIOB
11	(NC)		23	IRQ	ICSB	35	(NC)		47	C/D-	ICDB
12	D2	BS05	24	SA2	ISA2	36	DATA4	BS11	48	DRD-	ODRD

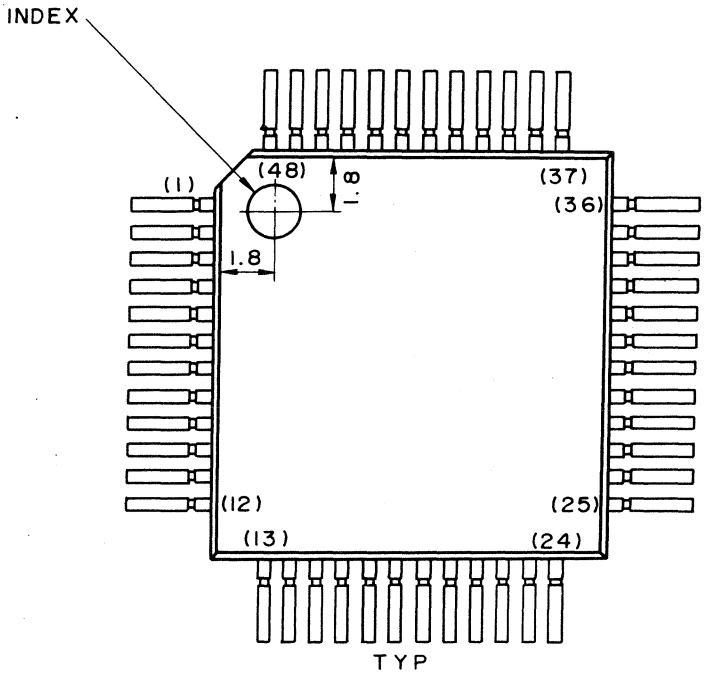
b. Block diagram



8.5 NDC 846

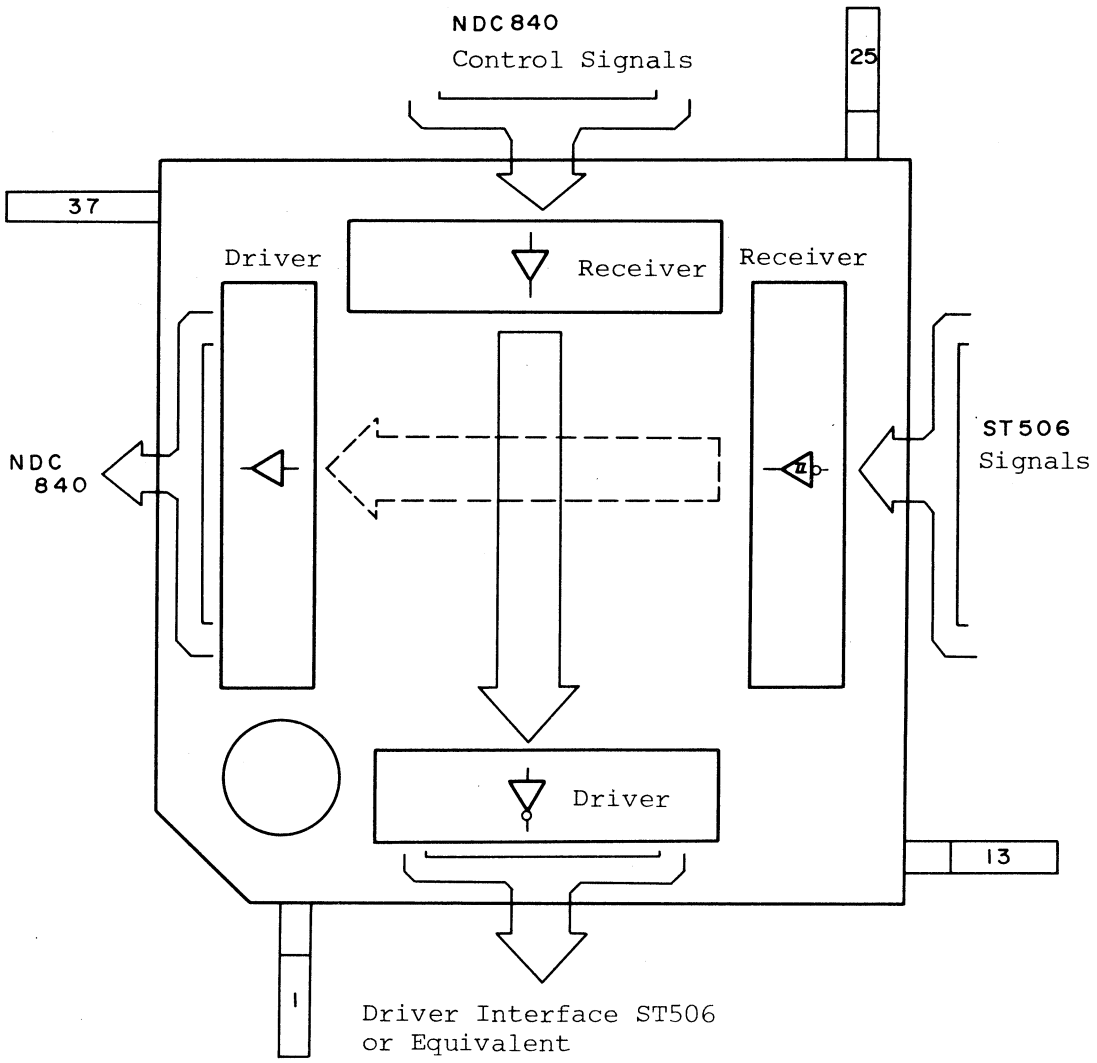
a. Pin assignment

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	O	INDEX	13	O	$\overline{DS-2}$	25	I	$\overline{INDEX}$	37	I	DS-2
2	O	VCO CLK	14	O	$\overline{DIR\ IN}$	26	I	$\overline{CLMP}$	38	I	DIR
3		NC	15	O	$\overline{STEP}$	27		NC	39	I	STEP
4	O	$\overline{VC1}$	16	O	$\overline{MSTP}$	28	I	VC1	40	I	$\overline{MSTP}$
5	O	$\overline{F1}$	17	O	$\overline{W-GT}$	29	I	F1	41	I	W-GT
6	O	$\overline{RWC}$	18	O	$\overline{HS-2-3}$	30	I	RWC	42	I	HS-2-3
7		VCC	19		GND	31		VCC	43		GND
8	O	$\overline{HS-2-0}$	20	I	$\overline{D-SEL}$	32	I	HS-2-0	44	O	D-SEL
9	O	$\overline{HS-2-1}$	21	I	$\overline{SKCMP}$	33	I	HS-2-1	45	O	SKCMP
10	O	$\overline{HS-2-2}$	22	I	$\overline{TRK00}$	34	I	HS-2-2	46	O	TRK00
11		NC	23	I	$\overline{W-FLT}$	35		NC	47	O	W-FLT
12	O	$\overline{DS-1}$	24	I	$\overline{RDY}$	36	I	DS-1	48	O	RDY

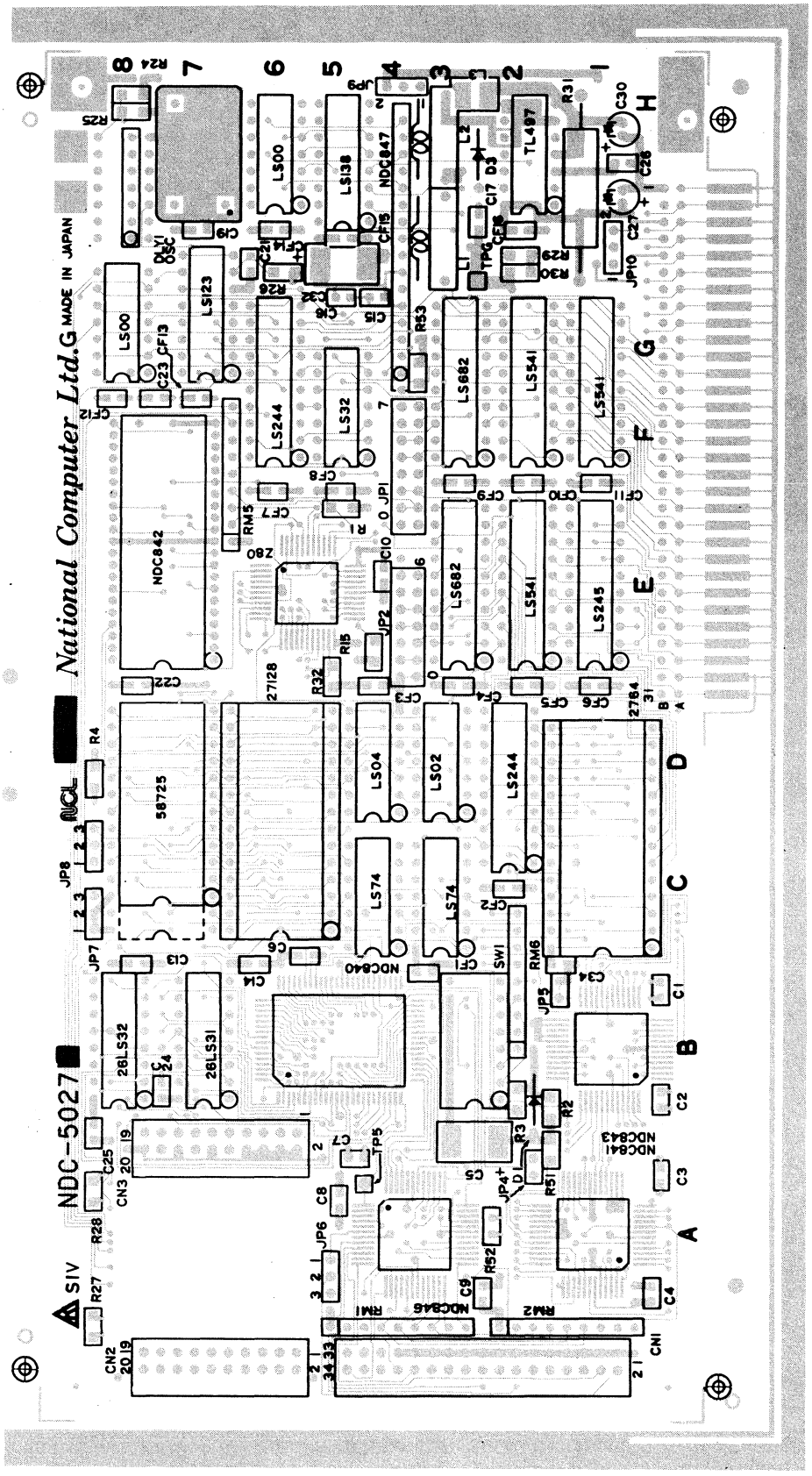


Note ( ): Pin Number

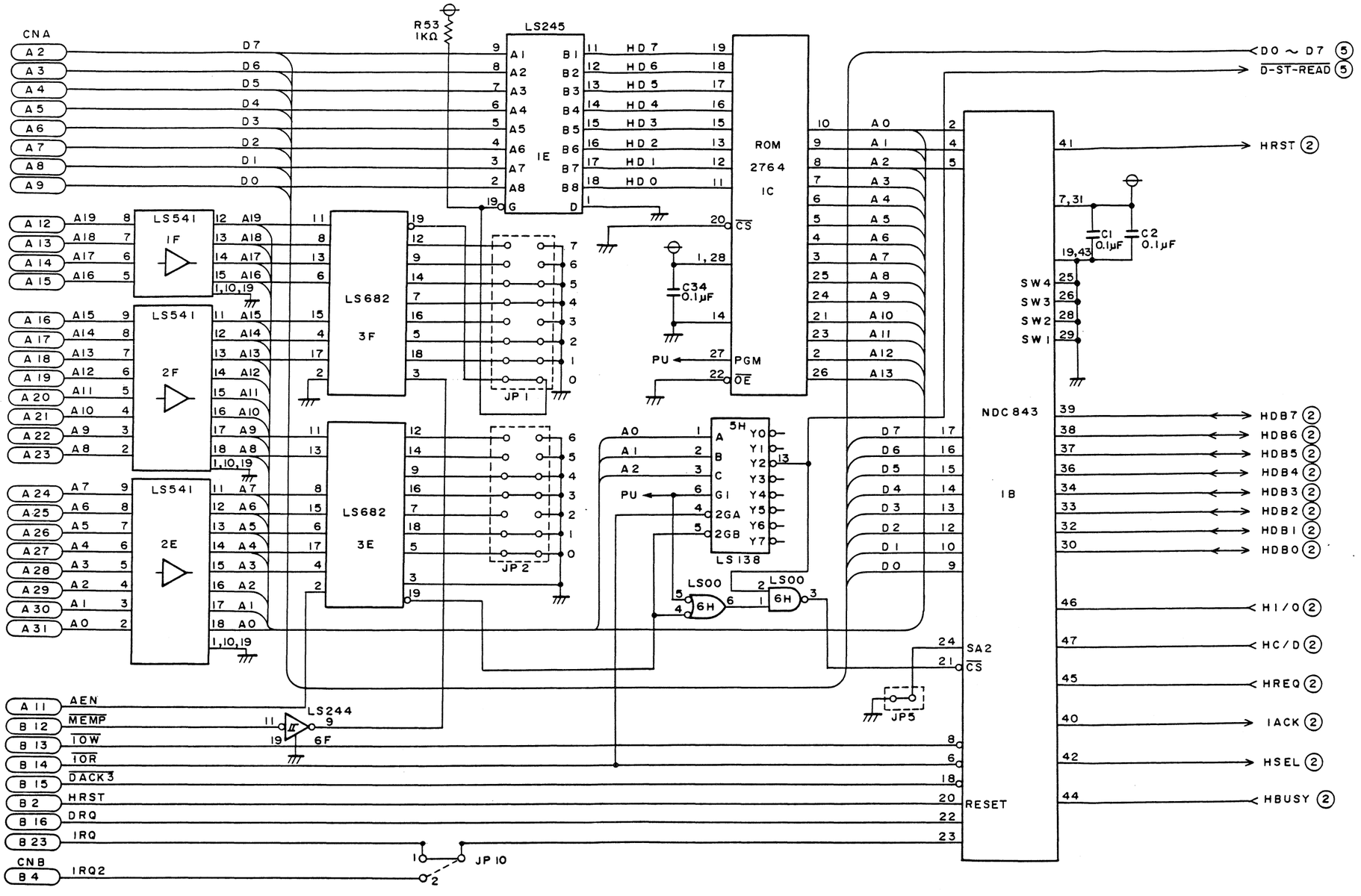
b. Block diagram



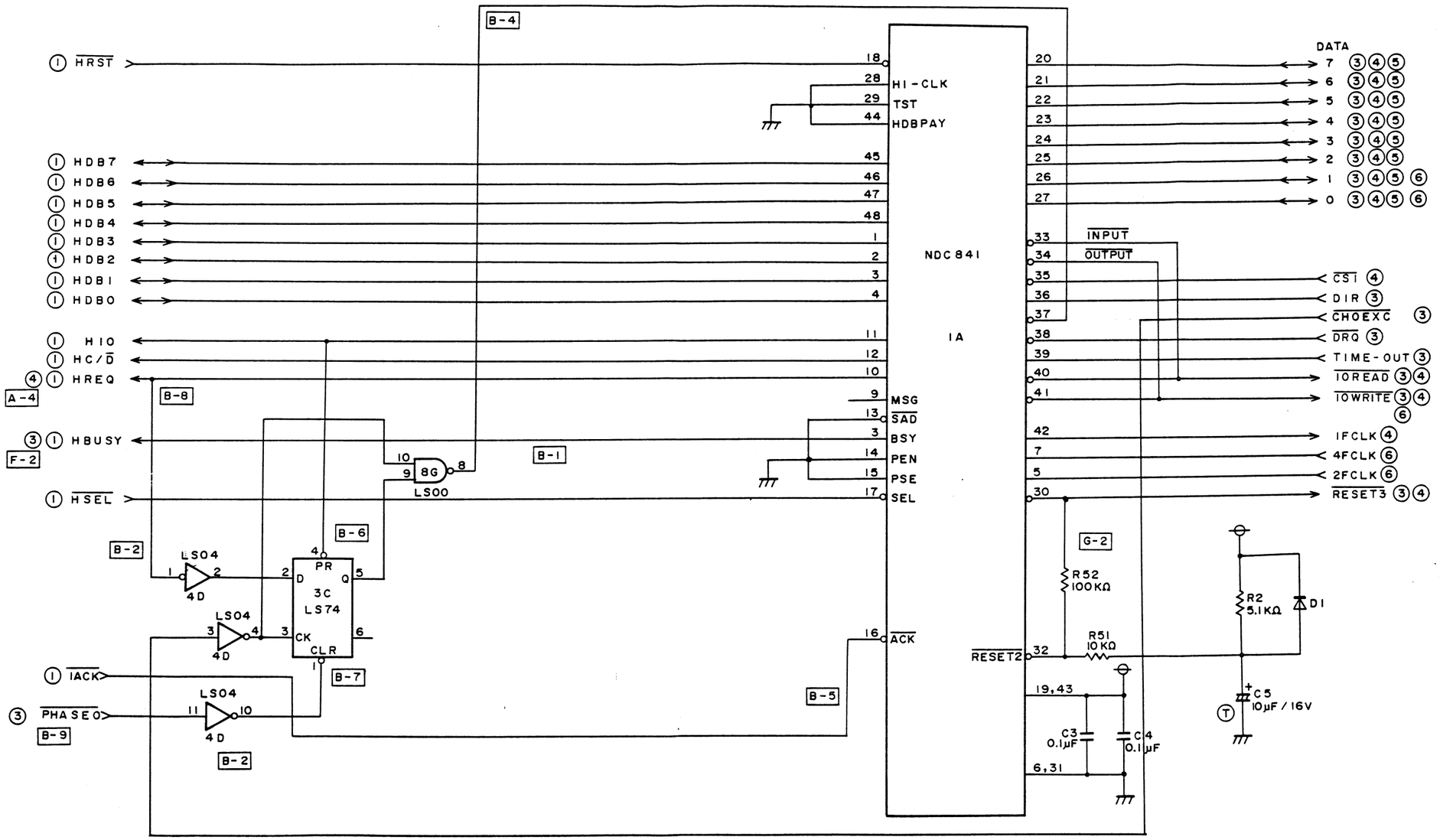
9. PARTS LOCATION



10. CIRCUIT DRAWING



Host Interface 1 (NDC 843)



Host Interface II (NDC 841)

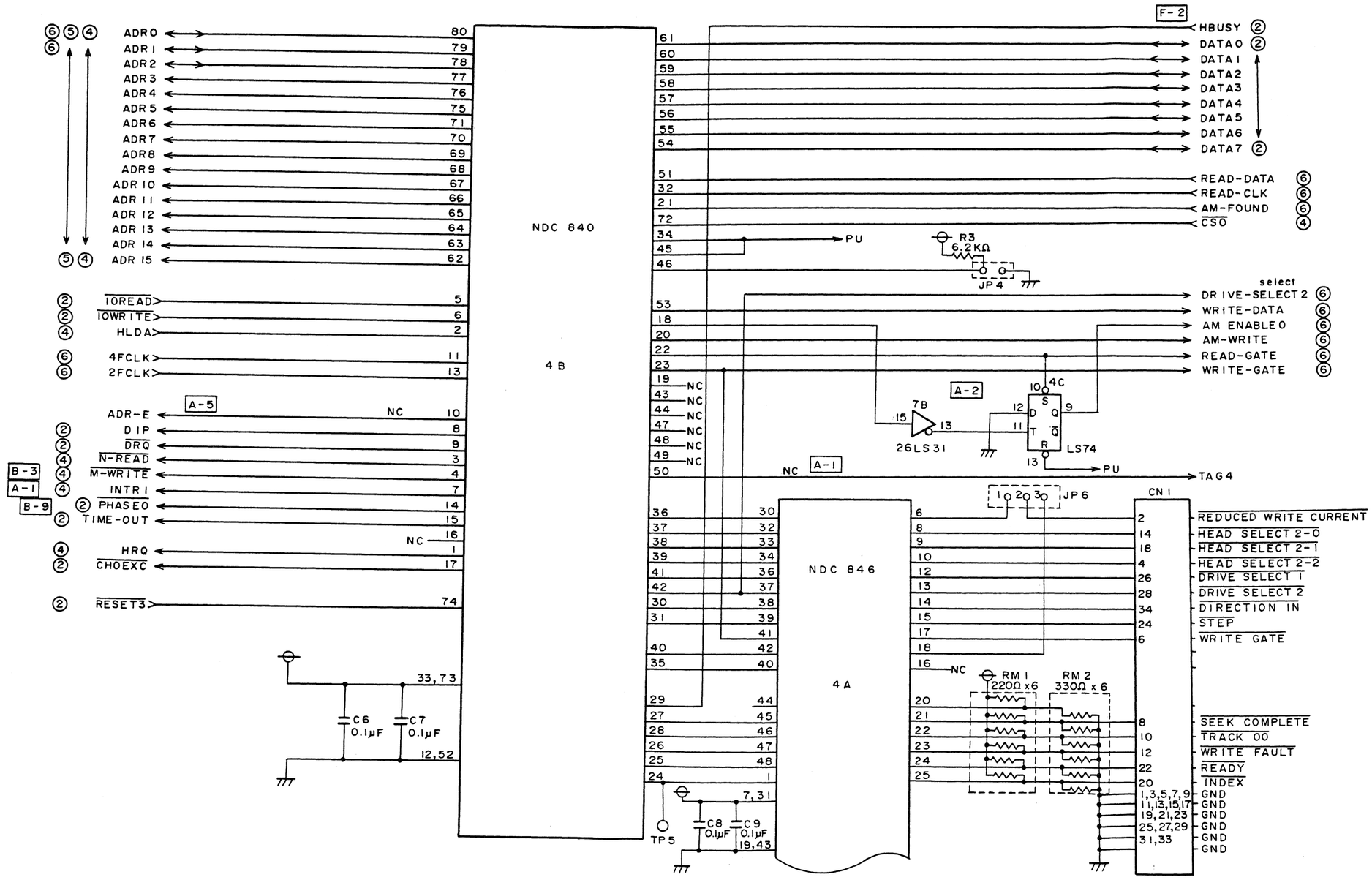
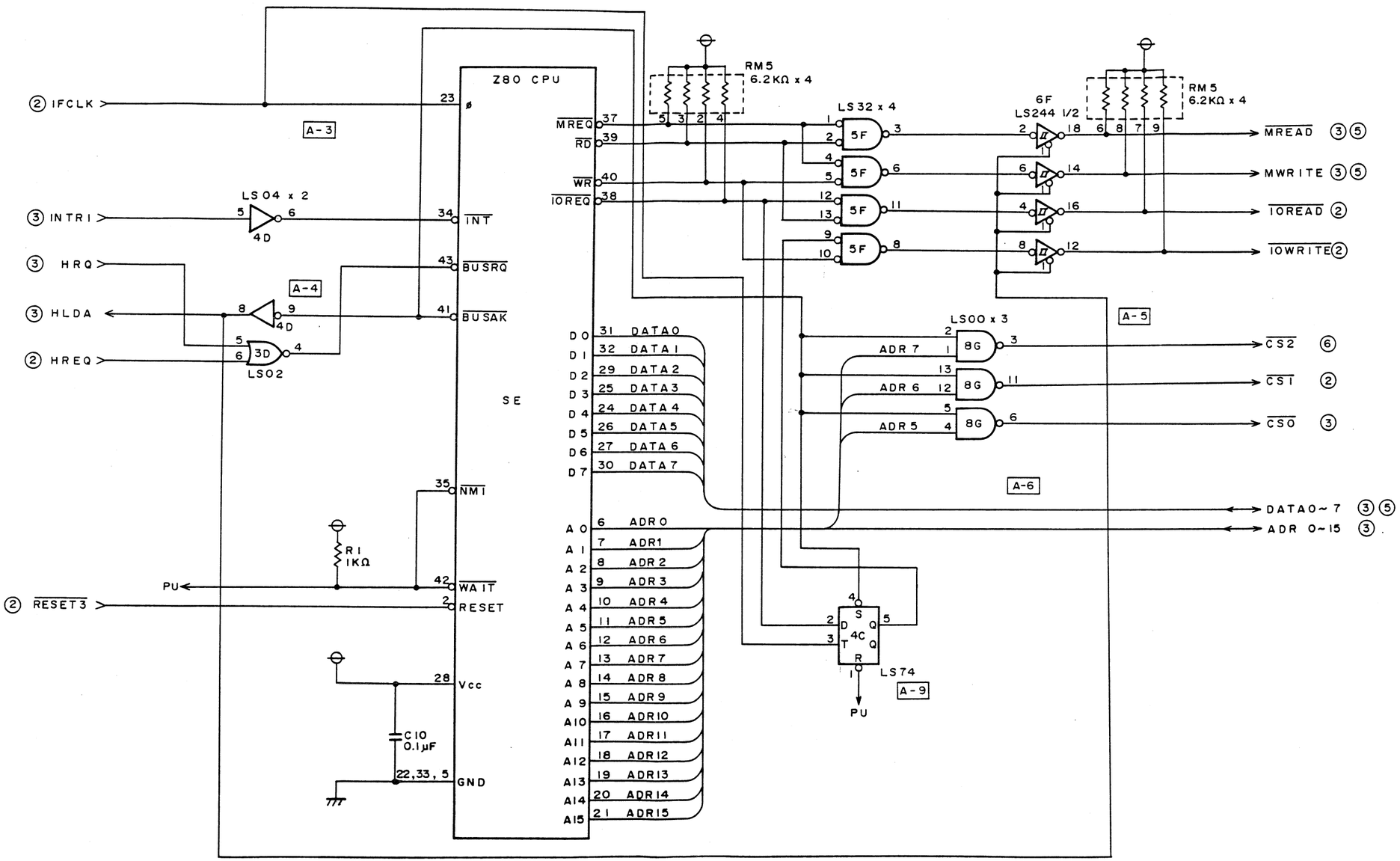
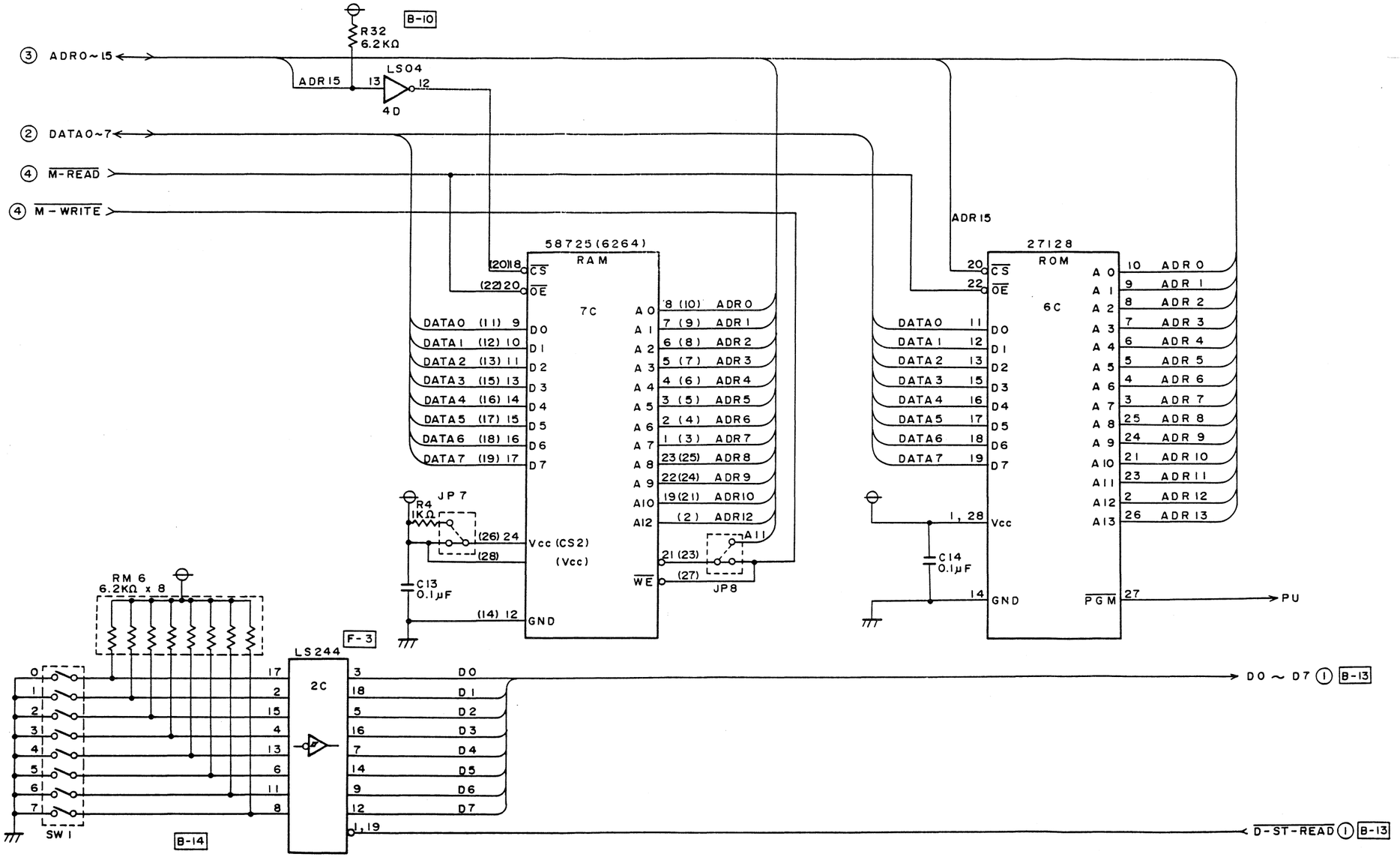
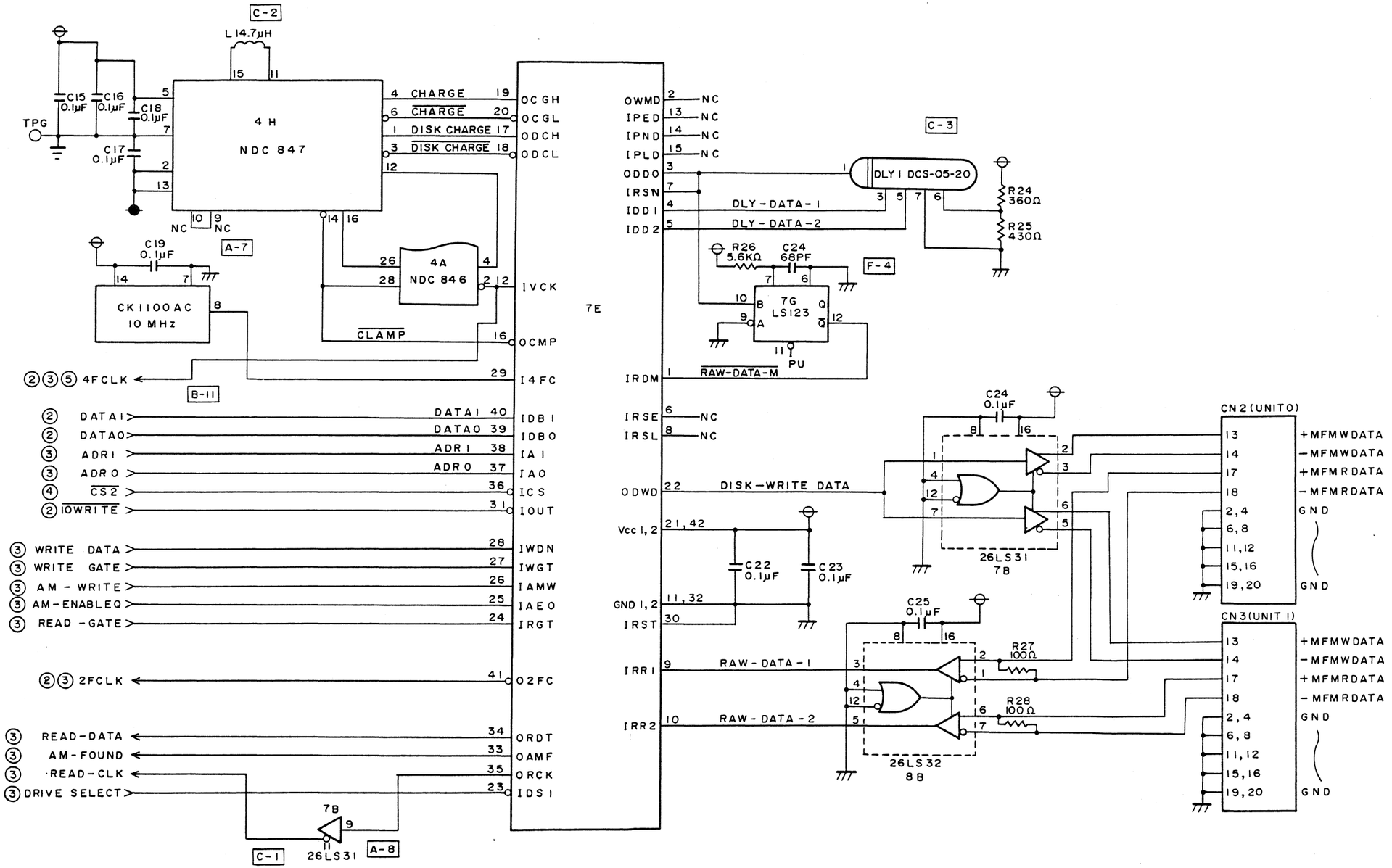
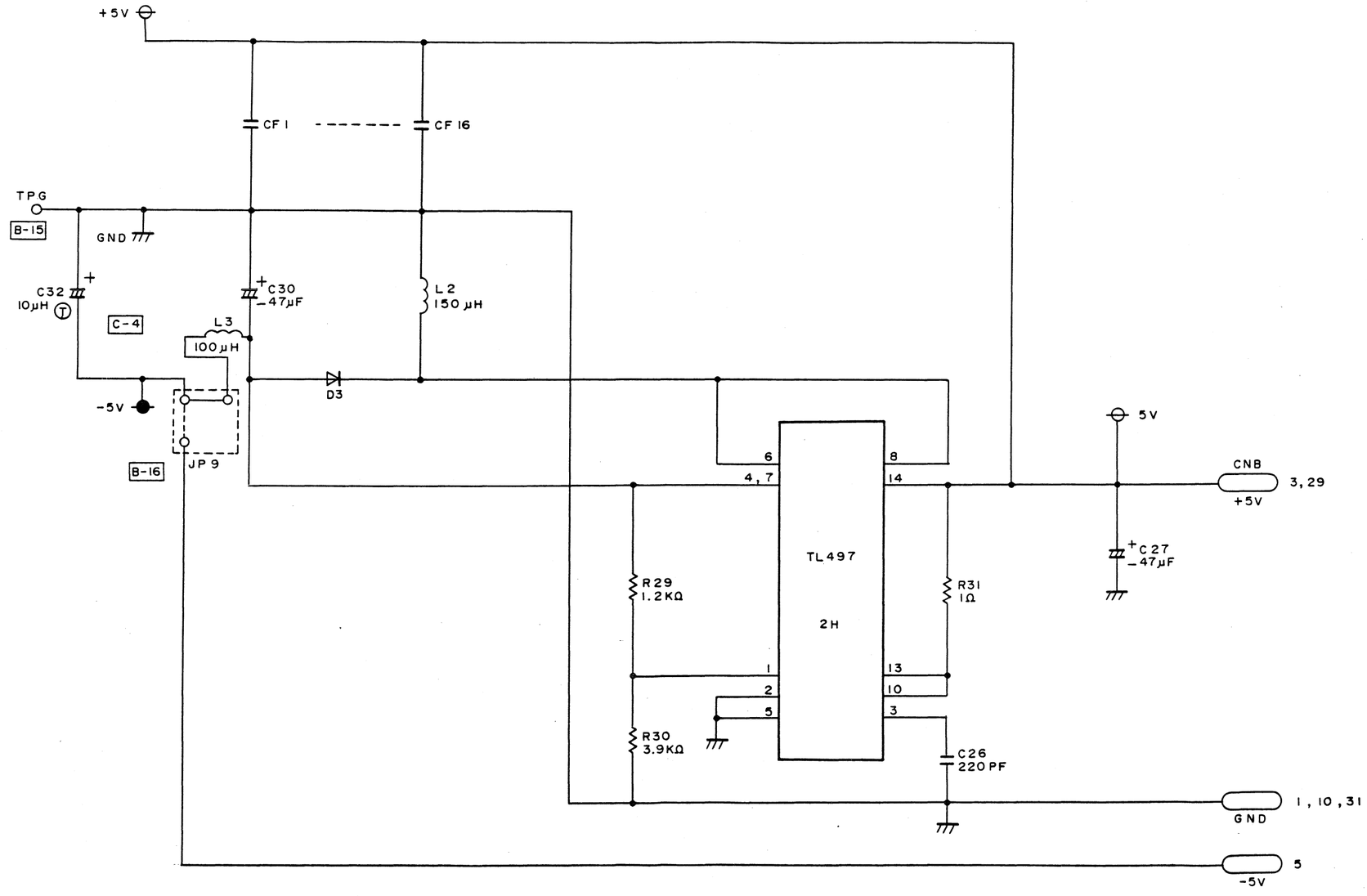


Figure 6-3 HDC


Z80 CPU
SE
② IFCLK
A-3
23 ø
③ INTR1
LS04 x 2
4D
34 INT
③ HRQ
43 BUSRQ
A-4
③ HLDA
4D
41 BUSAK
② HREQ
3D
LS02
35 NMI
R1
1KΩ
PU
42 WAIT
② RESET3
2 RESET
28 Vcc
C10
0.1μF
22,33, 5 GND
MREQ 37
RD 39
WR 40
IOREQ 38
RM5
6.2KΩ x 4
LS32 x 4
5F
6F
LS244 1/2
MREAD ③⑤
MWRITE ③⑤
IOREAD ②
IOWRITE ②
LS00 x 3
8G
A-5
ADR 7
ADR 6
ADR 5
CS2 ⑥
CS1 ②
CS0 ③
A-6
DATA0~7 ③⑤
ADR 0~15 ③
D0 31 DATA0
D1 32 DATA1
D2 29 DATA2
D3 25 DATA3
D4 24 DATA4
D5 26 DATA5
D6 27 DATA6
D7 30 DATA7
A0 6 ADR0
A1 7 ADR1
A2 8 ADR2
A3 9 ADR3
A4 10 ADR4
A5 11 ADR5
A6 12 ADR6
A7 13 ADR7
A8 14 ADR8
A9 15 ADR9
A10 16 ADR10
A11 17 ADR11
A12 18 ADR12
A13 19 ADR13
A14 20 ADR14
A15 21 ADR15
4C
LS74
A-9
PU


B-10
R32
6.2KΩ
③ ADR0~15
ADR15
LS04
13
12
4D
② DATA0~7
④ M-READ
④ M-WRITE
58725(6264)
RAM
7C
20(18) CS
22(20) OE
DATA0 (11) 9
DATA1 (12) 10
DATA2 (13) 11
DATA3 (15) 13
DATA4 (16) 14
DATA5 (17) 15
DATA6 (18) 16
DATA7 (19) 17
D0
D1
D2
D3
D4
D5
D6
D7
A0 8 (10) ADR0
A1 7 (9) ADR1
A2 6 (8) ADR2
A3 5 (7) ADR3
A4 4 (6) ADR4
A5 3 (5) ADR5
A6 2 (4) ADR6
A7 1 (3) ADR7
A8 23(25) ADR8
A9 22(24) ADR9
A10 19(21) ADR10
A12 (2) ADR12
A11
21 (23)
WE (27)
JP8
JP7
R4
1KΩ
(26) 24
Vcc (CS2)
(Vcc)
(28)
C13
0.1μF
(14) 12
GND
ADR15
27128
ROM
6C
20 CS
22 OE
1, 28 Vcc
C14
0.1μF
14 GND
A0 10 ADR0
A1 9 ADR1
A2 8 ADR2
A3 7 ADR3
A4 6 ADR4
A5 5 ADR5
A6 4 ADR6
A7 3 ADR7
A8 25 ADR8
A9 24 ADR9
A10 21 ADR10
A11 23 ADR11
A12 2 ADR12
A13 26 ADR13
PGM 27
PU
RM 6
6.2KΩ x 8
SW1
B-14
LS244
F-3
2C
0 17
1 2
2 15
3 4
4 13
5 6
6 11
7 8
3 D0
18 D1
5 D2
16 D3
7 D4
14 D5
9 D6
12 D7
1, 19
D0 ~ D7 ① B-13
D-ST-READ ① B-13


C-2
L 14.7μH
C15 0.1μF
C16 0.1μF
C18 0.1μF
C17 0.1μF
TPG
4 H
NDC 847
NC
NC
A-7
C19 0.1μF
CK1100AC
10 MHz
4A
NDC 846
4 CHARGE
6 CHARGE
1 DISK CHARGE
3 DISK CHARGE
12
CLAMP
OCGH
OCGL
ODCH
ODCL
IVCK
OCMP
7E
4FCLK
B-11
I4FC
DATA1
DATA0
ADR1
ADR0
CS2
IOWRITE
IDB1
IDB0
IA1
IA0
ICS
IOUT
WRITE DATA
WRITE GATE
AM - WRITE
AM-ENABLEQ
READ -GATE
IWDN
IWGT
IAMW
IAEO
IRGT
2FCLK
O2FC
READ-DATA
AM-FOUND
READ-CLK
DRIVE SELECT
ORDT
OAMF
ORCK
IDS1
7B
26LS31
C-1
A-8
OWMD
IPED
IPND
IPLD
ODDO
IRSN
IDD1
IDD2
IRDM
IRSE
IRSL
ODWD
Vcc 1, 2
GND 1, 2
IRST
IRR1
IRR2
NC
DLY-DATA-1
DLY-DATA-2
RAW-DATA-M
DISK-WRITE DATA
RAW-DATA-1
RAW-DATA-2
C-3
DLY1 DCS-05-20
R24 360Ω
R25 430Ω
R26 5.6KΩ
C24 68PF
F-4
7G LS123
PU
C22 0.1μF
C23 0.1μF
C24 0.1μF
26LS31
7B
C25 0.1μF
R27 100Ω
R28 100Ω
26LS32
8B
CN2(UNIT0)
CN3(UNIT1)
+MFMWDATA
-MFMWDATA
+MFMRDATA
-MFMRDATA
GND

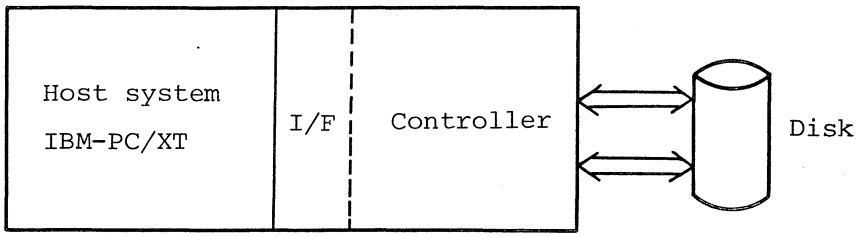

+5V
CF 1
CF 16
TPG
B-15
GND
C32
10μH
C-4
C30
47μF
L3
100μH
L2
150 μH
D3
-5V
B-16
JP 9
5V
CNB
3, 29
+5V
6
4, 7
8
14
TL497
2H
C27
47μF
R29
1.2KΩ
R31
1Ω
1
2
5
13
10
3
R30
3.9KΩ
C26
220 PF
1, 10, 31
GND
5
-5V

11. TROUBLESHOOTING

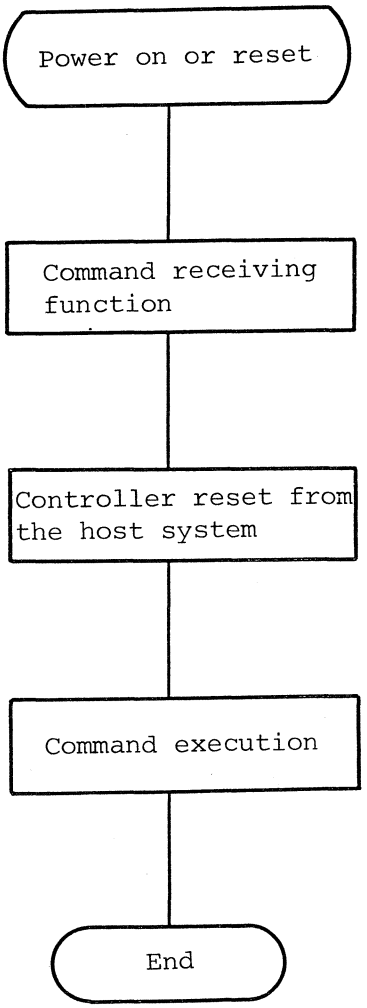
11.1 Outline

This section explains the analysis method for each sequence of the trouble analysis of the NDC-5027 Magnetic Disk Controller.

11.2 Configuration



11.3 Analysis Method



(1) BOOT ROM READ check

READ of the BOOT ROM cannot be made.

(a) BOOT ROM 2764 (IC) is faulty.

(b) Address comparator 74LS682 (3F) is faulty.

(c) Bus control 74LS245 (1E) is faulty.

(d) There is not JPI-0.

(2) Basic operation of the controller

Is the internal operation of the controller normal after its power has been turned on or it has been reset?

(a) Check if the RD signal is output from MPU Z-80 (6E) Pin 39.

(b) If the RD signal is not output;

- o Check if the BUSRQ signal from MPU Z-80 (6E) Pin 43 is on the LOW level.
- o Check if the INT signal from MPU Z-80 (6E) Pin 34 is on the LOW level.

(c) If the BUSRQ signal is on the LOW level;

- o NDC 840 LSI is faulty (FPU DMA).
- o NDC 841 LSI is faulty (HOST I/F).
- o 74LS02 (3D) is faulty.

(d) If the INT signal is on the LOW level;

- o NDC 840 LSI is faulty (FPU DMA).
- o 74LS04 (4D) is faulty.

(e) If the MPU Z-80 does not operate;

- o Check if the IF CLK is normal? (2.5 MHz)
- o Check if the RESET signal (Pin 2) is on the HIGH level?

(3) Controller select

(a) The controller hardware status is not in the command request mode after the controller has been selected.

- o Address comparator 74LS682 (3E) or decoder 74LS138 (5H) is faulty.
- o HOST I/F NDC 843 (1B) or NDC841 (1A) is faulty.
- o MPU Z-80 (6E) is faulty.
- o some of the MPU peripherals (74LS32 (5F), 74LS244 (6F), 74LS00 (8G), 74LS74 (4C), ROM (6C), or RAM (7C)) is faulty.

(b) DRQ does not rise even after one byte of command has been sent;

1) NDC 840 (4B) Pin 1 is on the HIGH level.

- o NDC 843 (1B) or NDC 841 (1A) is faulty.

2) NDC 840 (4B) Pin 1 is on the LOW level.

- o NDC 840 (4B) is faulty.
- o Some of MPU peripheral ICs is faulty.

(c) Does not start even after the command has been transferred;

1) NDC 840 (4B) Pin 1 is left on the HIGH level.

- o NDC 840 is faulty.
- o NDC 843 (1B) or NDC 841 (1A) is faulty.

(4) READ mode

(a) End IRQ does not rise even after the command has been transferred.

o HOST I/F NDC 843 (1B) or NDC 841 (1A) is faulty.

o NDC 840 (4B) is faulty (DMA).

(b) Always an error occurs after start.

1) Check if the outputs from NDC 847 (4H) Pin 2 and Pin 13 are -5 V.

o TL 497 (2H) is faulty.

o TL497 peripheral circuit is faulty.

2) Check if the output from NBC 847 (4H) Pin 8 is +0.5 v $\pm$2.0 V.

o NDC 847 (4H) is faulty.

3) Check the READ data from the disk.

o NDC 842 (7E) is faulty.

o NDC 840 (4B) is faulty.

o NDC 846 (4A) is faulty.

o 74LS123 (7G) is faulty.

(c) Some times an error occurs after the start.

1) Refer to (b) 1).

2) 74LS123 (7G) Pin 12

o Confirm the LOW level and 260 ns $\pm$30 ns.

(5) WRITE mode

(a) End IRQ does not rise after the command has been transferred.

o Refer to (4) (a).

(b) Always an error occurs after the start.

1) Refer to (4) (b) for errors in the ID section.

2) DATA WRITE errors

o NDC 842 (7E) is faulty.

o NDC 840 (4B) is faulty.

o NDC 846 (4A) is faulty.

o 26LS31 (7B) is faulty.

(c) Some times an error occurs after the start.

1) Refer to (4) (c) for errors in the ID section.

2) DATA WRITE errors

o Refer to (5) (b).

Printed in Japan 8601-50 A.S.K. 610403