MULTI LINE UNIT

DLV 11 J

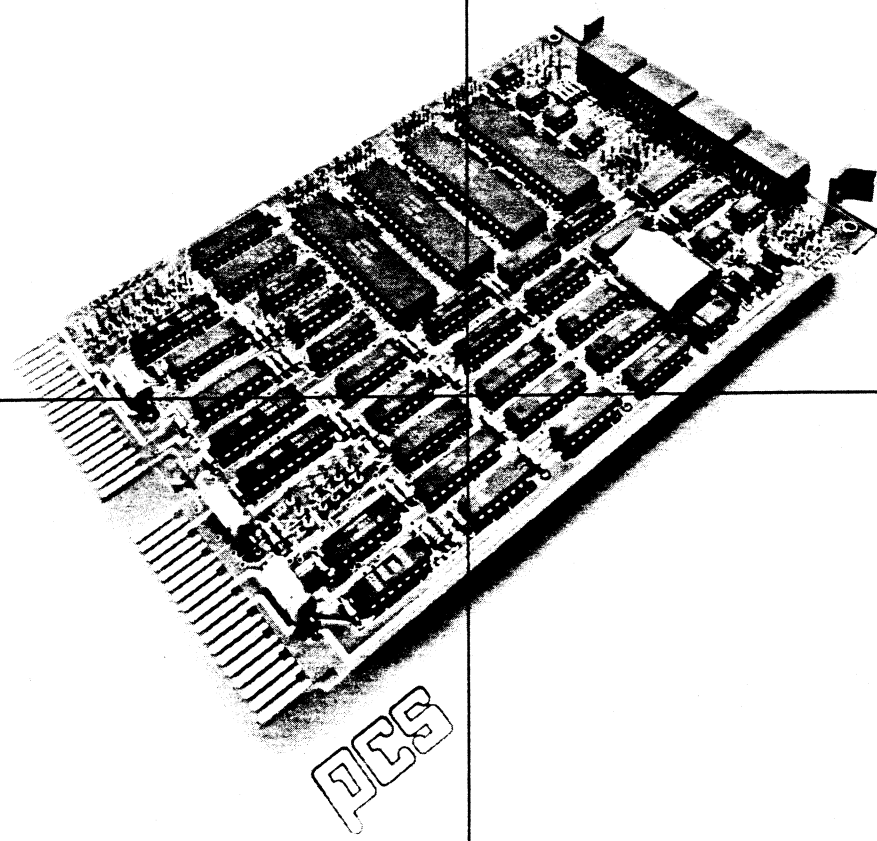
V 900.610

Periphere
Computer Systeme GmbH

Vier-Kanal asynchrones, serielles-Interface

Die DLV 11-J dient als Interface zwischen 4asynchronen, seriellen Kommunikations-[illegible]älen und dem Q-Bus im SII Rechner. [illegible]e führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit je einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom Q-Bus kommen aus und versieht diese mit Start-, Stop- und Paritätsbits.
Die PCS 900610 enthält 16 Device-Register, die vom Programm individuell adressiert werden können.

PCS 900.610



Für jeden Kanal (0-3) gibt es die

Empfangs-Kontroll/Status-Register	(RCSR)
Empfangsbuffer	(RBUF)
Sende-Kontroll/Status-Register	(XCSR)
Sendebuffer	(XBUF)

Technische Daten:

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS 422 oder 20 mA Linienstrom (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden: intern quarzgesteuerte Baud-Raten: 150, 300, 600, 1200, 2400, 4800, 9600, 19200 oder 38400 Baud
- extern gesteuerte Baud-Rate

Zeichenformate:

7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)

- Kanal 3 kann der Systemkonsole zugeordnet werden
- Bei Empfang eines „breaks" auf Kanal 3 kann der Prozessor in den Halt-Mode gehen oder einen Bootstrap durchführen.
- Hard- und Software äquivalent zu vier PCS 900615.

Größe	Dual Slot
Stromversorgung	+ 5V / 1A
	+ 12V/0,25A
normierte Busbelastung	1.0 AC, 1.0 DC

Option

Linienstrom-Pegelwandler für 4 Kanäle. Umsetzung von V24 auf 20mA Linienstrom (bis 9600 Baud)

PCS Periphere Computer Systeme GmbH · Pfälzer-Wald-Straße 36 · D–8000 München 90 · Telefon 089/68 10 21 · Telex 5 23 271

MILTI LINE UNIT

DLV 11 J

D 900.610

Beschreibung siehe:

Microcomputer Interfaces Handbook

DLV11-J
Four Asynchronous Serial Interfaces
900.610

Allgemeines

Die DLV11-J dient als Schnittstelle zwischen 4 asynchronen, seriellen I/O-Geräten mit V24-Anschluß und dem LSI11-Bus (Q-Bus).
Werden 20 mA Stromschleifen benötigt, so ist ein zusätzlicher Konverter (DLV11-KA) zu installieren.

Features

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS-422 oder 20 mA Stromschleife (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden:
  für quarzgesteuerte Baud-Raten:
  15Ø, 3ØØ, 6ØØ, 12ØØ, 24ØØ, 48ØØ, 96ØØ, 192ØØ oder 384ØØ Bits pro Sekunde. Bei Anwendung der DLV11-KA Option sind 11Ø Bit/s verfügbar
  für Zeichenformate:
  7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)
- Kanal 3 kann dem Bildschirminterface gewidmet werden.
- Kanal 3 kann bei Empfang eines 'breaks' entweder in den Halt-Mode gehen oder einen Bootstrap durchführen (auch keine Antwort ist möglich).
- Hard- und Softwareäquivalenz mit vier DLV11en

Spezifikationen

Identifikation	M8043
PCS-Nummer	900.610
Größe	Double Slot
Stromversorgung	+ 5V / 1 A
	+12V / 0,25A
normierte Busbelastung	1,0 AC, 1,0 DC

Funktionsbeschreibung

Die DLV11-J dient als Interface zwischen 4 asynchronen, seriellen Kommunikationskanälen und dem Q-Bus. Sie führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom LSI11-Bus kommen, aus und versieht diese mit Start-, Stop- und Paritätsbits.

Register

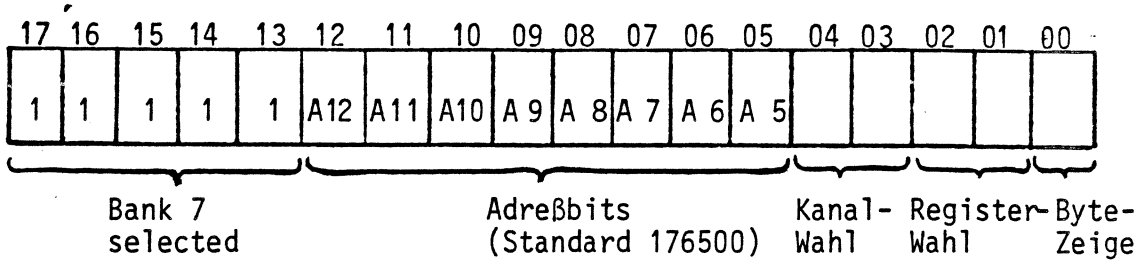
Allgemeines

Das folgende Kapitel enthält die für den Programmierer erforderliche Information über die Bedeutung der einzelnen Register und ihrer Bits.

Die DLV11-J enthält 16 Device-Register, die vom Programm individuell adressiert werden können. Für jeden Kanal (0-3) gibt es die

- Empfangs-Kontroll/Status-Register (RCSR)
- Empfangsbuffer (RBUF)
- Sende-Kontroll/Status-Register (XCSR)
- Sendebuffer (XBUF)

Über die Wire-Wrap-Jumpers läßt sich eine Basisadresse erzeugen. Dies ist das RCSR im Kanal Ø.
Bild 1 zeigt das Format der Device-Adresse sowie das Vektorformat.



Kanal-Wahl:	Adresse	Kanal
	00	0
	01	1
	10	2
	11	3

Register-Wahl:	Adresse	Register
	00	RCSR
	01	RBUF
	10	XCSR
	11	XBUF

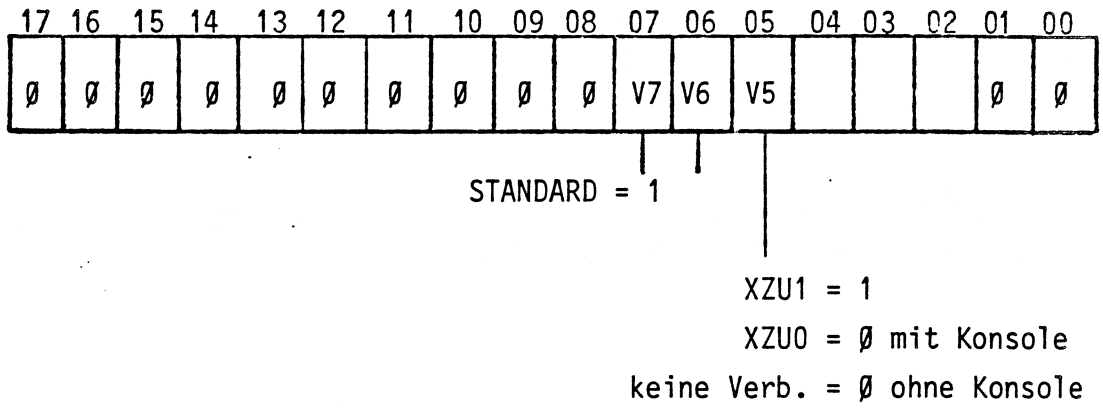


Bild 1

Die verbleibenden Device-Adressen folgen in 16 aufeinanderfolgenden Wortadressen. Es ist jedoch möglich, die letzten vier Adressen (Kanal 3) unabhängig dem Bildschirmterminal zuzuordnen. In diesem Falle wird die Adresse 177560-177566 sein. Soll ein Bildschirm betrieben werden, so muß die Device-Basis-Adresse eine der folgenden sein:

176500, 176540, 177500

Bild 2 zeigt die allgemeine Adreßbelegung, Bild 3 die Standardadressen.

Adresse	Device-Register	zugeordneter Vektor
	Kanal Ø	
Basis-Adresse		
(BA)	RCSR	Basis-Vektor (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Kanal 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	
	Kanal 2	
BA+20	RCSR	BV+20
BA+22	RBUF	
BA+24	XCSR	BV+22
BA+26	XBUF	
	Kanal 3	
177560	RCSR	60 } Konsole
177562	RBUF	
177564	XCSR	64 }
177566	XBUF	

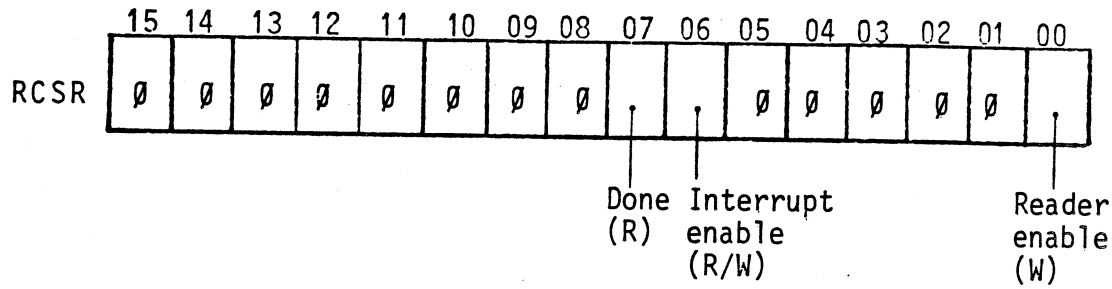
Bild 2

Adresse	Register	Vektor	
176500	RCSR	300	
176502	RBUF		Kanal Ø
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	
176512	RBUF		Kanal 1
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	
176522	RBUF		Kanal 2
176524	XCSR	324	
176526	XBUF		
176560	RCSR	60	
176562	RBUF		Kanal 3
176564	XCSR	64	
176566	XBUF		

Bild 3

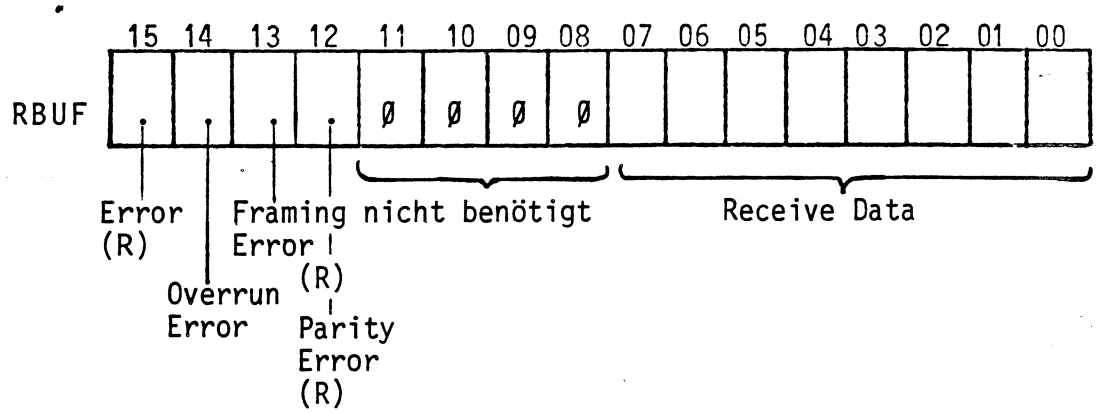
Es gibt 4 Wortformate, eines für jedes Device-Register innerhalb eines Kanals, die im folgenden beschrieben sind.

Receive Control/Status-Register



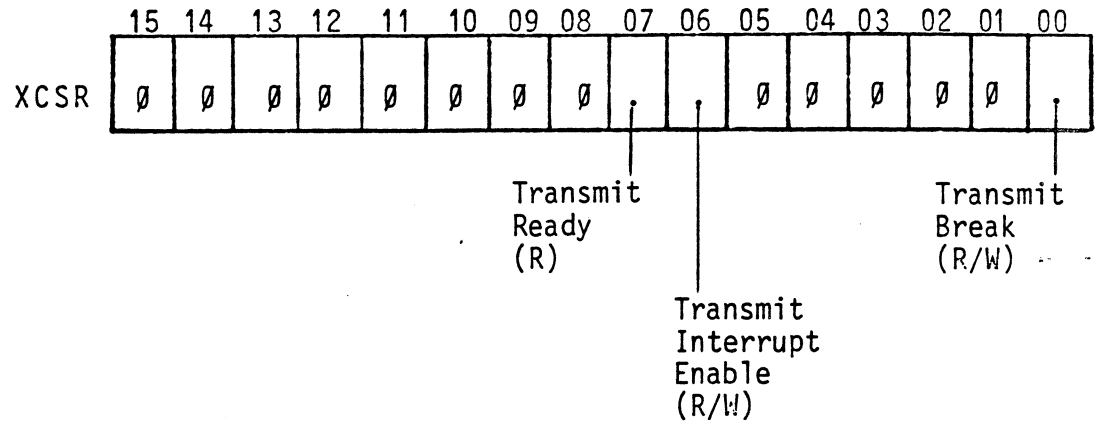
Bit	Beschreibung
8/15	Nicht benötigt. Beim Schreiben = Ø
7	Receiver Done. Wird gesetzt, wenn ein vollständiges Zeichen empfangen wurde und für die Eingabe in den Prozessor bereit ist. Das Bit wird automatisch gelöscht, wenn RBUF gelesen wird, BINITL angelegt wird oder das Bit Reader Enable gesetzt ist. Read Only Bit. Wenn das Bit 6 des RCSR gesetzt ist, bewirkt das Setzen des Bits 7 den Einsprung in eine Interrupt-Sequenz.
6	Receiver Interrupt Enable. Wird unter Programmkontrolle im Falle einer Receiver Interrupt Anforderung gesetzt (wenn ein Zeichen zur Obertragung in den Prozessor bereit ist). Wird gelöscht durch das Programm oder durch BINIT. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Reader Enable. Indem man dieses Bit setzt, geht der Lochstreifenleser am LT33-Terminal um ein Zeichen weiter. Durch das Setzen wird das Done-Bit (Bit 7) gelöscht. Write Only Bit. Die Benutzung dieses Bits setzt das Vorhandensein der DLV11-KA-Option voraus.

Receive Buffer



Bit	Beschreibung
15	Channel Error Status. Logisches 'OR' aus Bit 14,13 und 12. Read Only Bit.
14	Overrun Error. Wenn dieses Bit gesetzt ist, wird angezeigt, daß das Lesen eines Datums vor dem Senden eines neuen nicht beendet wurde. Wird durch BINIT gelöscht. Read Only Bit.
13	Framing Error. Das gesetzte Bit zeigt beim gelesenen Zeichen ein ungültiges Stop-Bit an. Wird durch BINIT gelöscht. Read Only Bit.
12	Parity Error. Die empfangene Parität stimmt nicht mit der erwarteten überein, wenn dieses Bit gesetzt ist. Falls das Device ohne Parität betrieben wird, ist dieses Read Only Bit immer Ø.
8-11	Nicht benötigt. Beim Lesen = Ø
Ø-7	Daten-Bits. Enthält 7 oder 8 Bits rechtsbündig. Read Only Bits.

Transmit Control/Status-Register



Bit	Beschreibung
8-15	Nicht benötigt. Beim Lesen = Ø
7	Transmit Ready. Wird gesetzt, wenn XBUF leer ist und ein neues Zeichen übertragen werden kann. Es wird ebenfalls durch INIT während einer Power-Up-Sequenz oder während einer Reset-Instruction gesetzt. Read Only Bit. Wenn das Transmitter Interrupt Enable Bit (Bit 6) gesetzt ist, bewirkt das Setzen des Transmit Ready Bits eine Interrupt-Sequenz.
6	Transmit Interrupt Enable. Wenn es erforderlich wird, eine Transmit Interupt Anforderung zu generieren, wird dieses Bit unter Programmkontrolle gesetzt. Während Power-Up oder Init-Function wird dieses Bit gelöscht. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Transmit Break. Wird unter Programmkontrolle gesetzt oder gelöscht. Wenn es gesetzt ist, wird eine zusammenhängende Leerzeichenkette übertragen. Transmit Done und Transmit Interrupt können jedoch weiter benutzt werden. Im gelöschten Zustand kann eine normale Zeichenübertragung stattfinden. Wird durch BINIT gelöscht. Read/Write Bit.

Einstellungen

Das folgende Kapitel beschreibt, wie der Anwender das Modul entsprechend seinem System und seiner Anwendung einstellen kann. Register-Adressen, Vektor, Übertragungs- und Interface-Funktionen sind durch Brücken einstellbar. Die Standardadreß- und Vektoreinstellung enthält nachfolgende Tabelle, ebenso die der Brücken und deren Position.

Brücke	Bed	Stellung	Std	Anw	Brücke	Bed	Stellung	Std	Anw	Brücke	Bed	Stellung	Std.	Anw
A12	Basis - Adresse	X-0 / X-1	X		A6	Adr.	R / J	X		-1	Konsole auf	X-0 / X-1	X	
A11		X-0 / X-1	X		A5		X-0 / X-1	X		C2	CH3	X-0 / X-1	X	
A10		X-0 / X-1	X		V7	Basis - Vec	R / J	X		Break Reakt. CH3	Inh. Halt Boot	R / X-H / X-B	X	
A9		X-0 / X-1	X		V6		R / J	X						
A8		X-0 / X-1	X		V5		X-0 / X-1			R10	Impulsformung bei V24 je nach Baud-Rate (Tabelle)		120k	
A7		R / J	X			Konsole	R	X		R23			120k	
					M		R / J	X						

Std.-Adr.: 177500 | Anw.-Adr.: | Std.-Vec: 300 | Anw.-Vec.:

Einstellung je Kanal		Ø			1			2			3		
Brücke	Bedeutung	Stellung	Std	Anw	Stellung	Std	Anw	Stellung	Std	Anw	Stellung	Std.	Anw
Baud-Rate	150 bd	0-U			1-U			2-U			3-U		
	300 bd	0-T			1-T			2-T			3-T		
	600 bd	0-V			1-V			2-V			3-V		
	1,2 kbd	0-W			1-W			2-W			3-W		
	2,4 kbd	0-Y			1-Y			2-Y			3-Y		
	4,8 kbd	0-L			1-L			2-L			3-L		
	9,6 kbd	0-N	X		1-N	X		2-N	X		3-N	X	
	19,2 kbd	0-K			1-K			2-K			3-K		
	38,4 kbd	0-Z			1-Z			2-Z			3-Z		
D	7 Datenbits	X-0			X-0			X-0			X-0		
	8 Datenbits	X-1	X		X-1	X		X-1	X		X-1	X	
S	1 Stop Bit	X-0			X-0			X-0			X-0		
	2 Stop Bits	X-1	X		X-1	X		X-1	X		X-1	X	
P	Parity enable	X-0			X-0			X-0			X-0		
	Parity inhibit	X-1	X		X-1	X		X-1	X		X-1	X	
E	Odd Parity	X-0			X-0			X-0			X-0		
	Even Parity	X-1	X		X-1	X		X-1	X		X-1	X	
M+N TERM	EIA RS 422	X-2			X-2			X-2			X-2		
M+N		100Ω			100Ω			100Ω			100Ω		
M	V24	X-3			X-3			X-3			X-3		
N	20mA mit 900 E11	X-3	X		X-3	X		X-3	X		X-3	X	
		X-R	X		X-R	X		X-R	X		X-R	X	

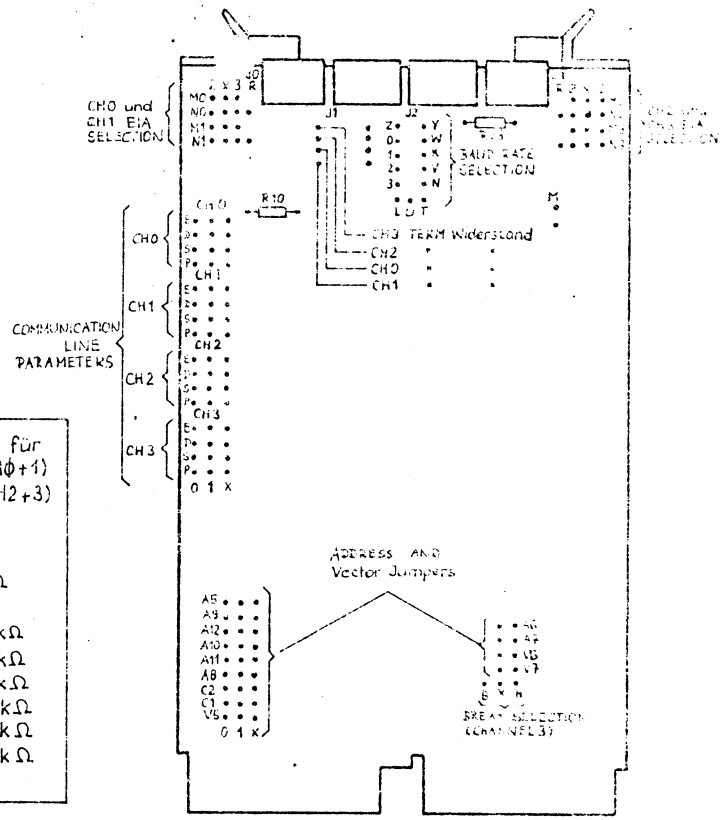
(U-Norm)

Tabelle für R10 (CH Ø+1) R23 (CH 2+3)

	1 MΩ
	820 kΩ
	430 kΩ
	200 kΩ
	120 kΩ
	51 kΩ
	22 kΩ

R = entfernt

J = eingesetzt



Standard: Anwendung

Einstell - Tabelle für DLV 11 - J (M8043)

B 900 610 3

UART-Funktionen

Die Funktion des UARTs (universeller asynchroner Empfänger und Sender) werden durch die Brücken D, S, P und E eingestellt - gemäß folgender Tabelle.

Bezeichnung	Kanal Parameter	X ZU Ø	X ZU 1	Bemerkungen
D	Nr. Datenbits	7	8	LSB zuerst übertragen
S	Nr. Stopbits	1	2	
P	Parität	Parität	keine	
E	gerade Parität	Ungerade erwartet	Gerade erwartet	Nur wenn P = Ø

Die Baud-Rate wird folgendermaßen eingestellt.

Bezeichnung	Baud-Rate	Brücke
U	150	nach Ø, 1, 2, 3 (Ø, 1, 2, 3 = Kanäle)
T	300	"
V	600	"
W	1 200	"
Y	2 400	"
L	4 800	"
N	9 600	"
K	19 200	"
Z	38 400	"

Zur Einstellung der Signalform bei den verschiedenen Baud-Raten sind folgende Widerstände nötig:

38,4 KB	22 K	R10 für CHØ und CH1
19,2 KB	51 K	
9,6 KB	120 K	
4,8 KB	200 K	
2,4 KB	430 K	
1,2 KB	820 K	
600 KB	1 M	R23 für CH2 und CH3
300 KB	1 M	
150 KB	1 M	
110 KB	1 M	

Bei Benutzung des Kanals 3 als Konsolen-
kanal läßt sich ein 'Break' folgendermaßen
verarbeiten:

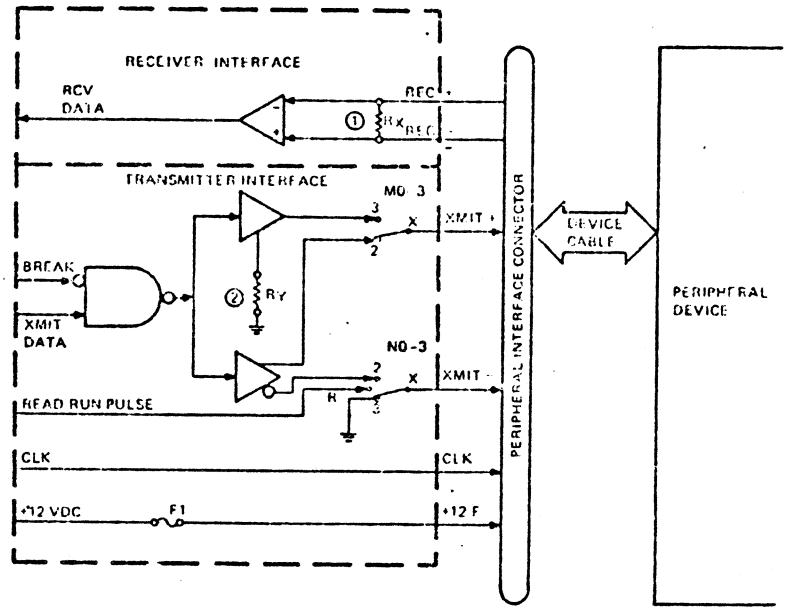
Boot	Brücke X nach B
Halt	Brücke X nach H
keine Antwort	keine Brücke

Schnittstellenfunktionen

Die Art der seriellen Schnittstelle wird durch
die folgende Tabelle bestimmt:

Brücke	EIA RS-422	EIA RS-232C, RS-423	20mA Stromschleife mit DLV11-KA
MØ-3	X nach 2	X nach 3	X nach 3
NØ-3	X nach 2	X nach 3	X nach R
Anschluß Widerstand (einer pro Kanal)	100 1/4W		
Signalformung (einer pro Paar)		nach obiger Tabelle	
Fuse 1			1,0 A Pico Fuse

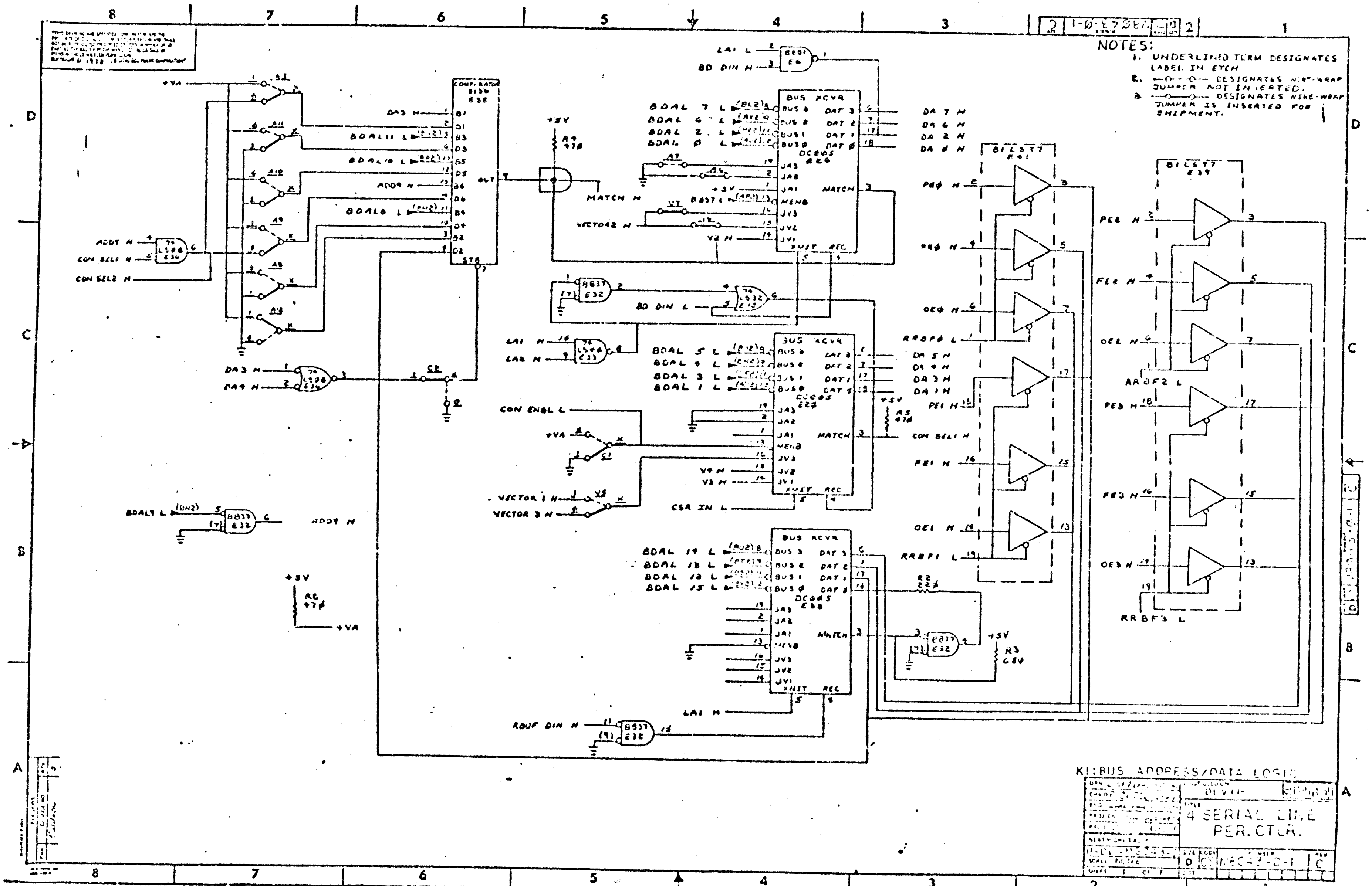
Bild 4 zeigt das Schlatbild eines typischen Interfaces.

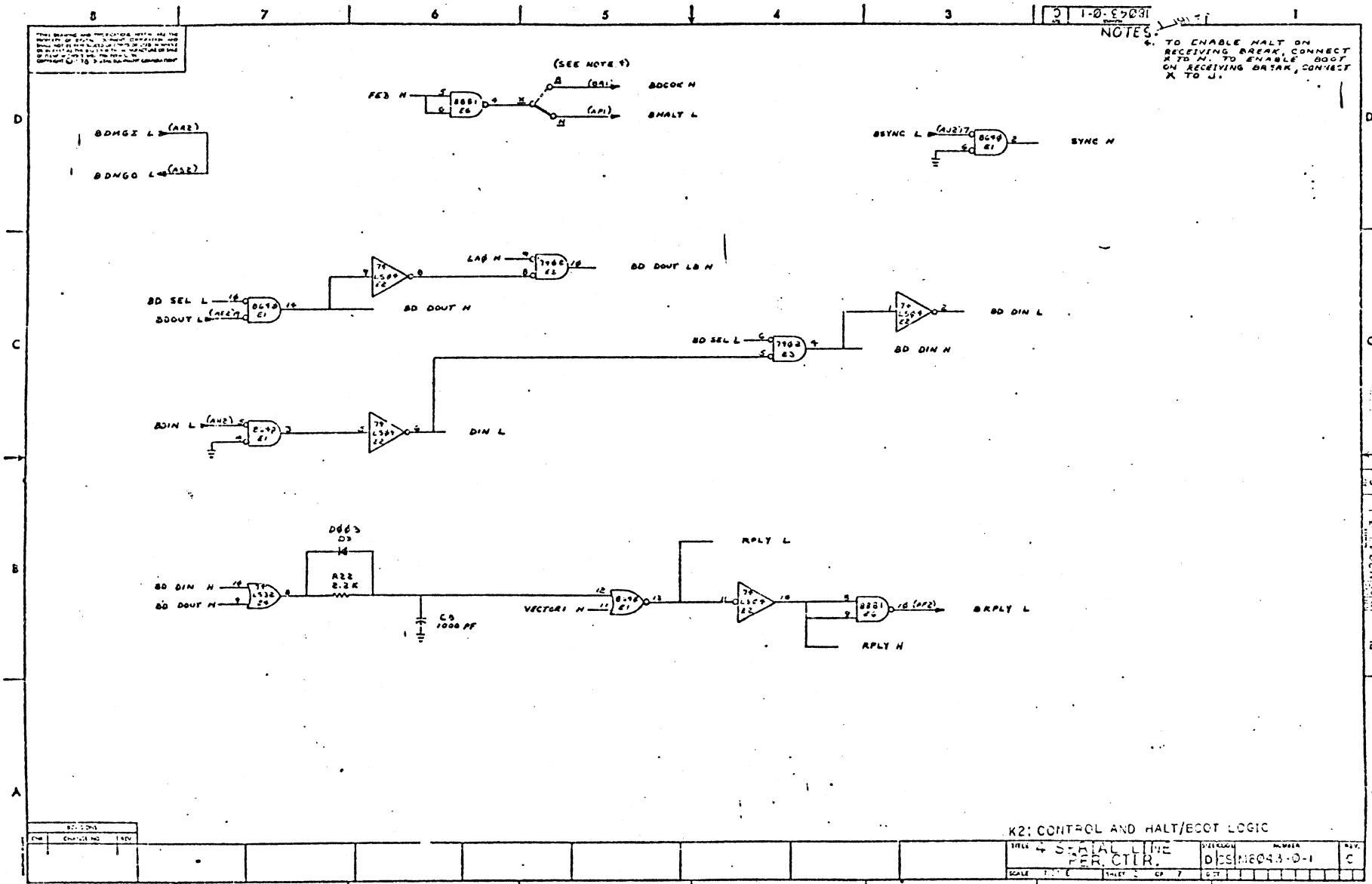


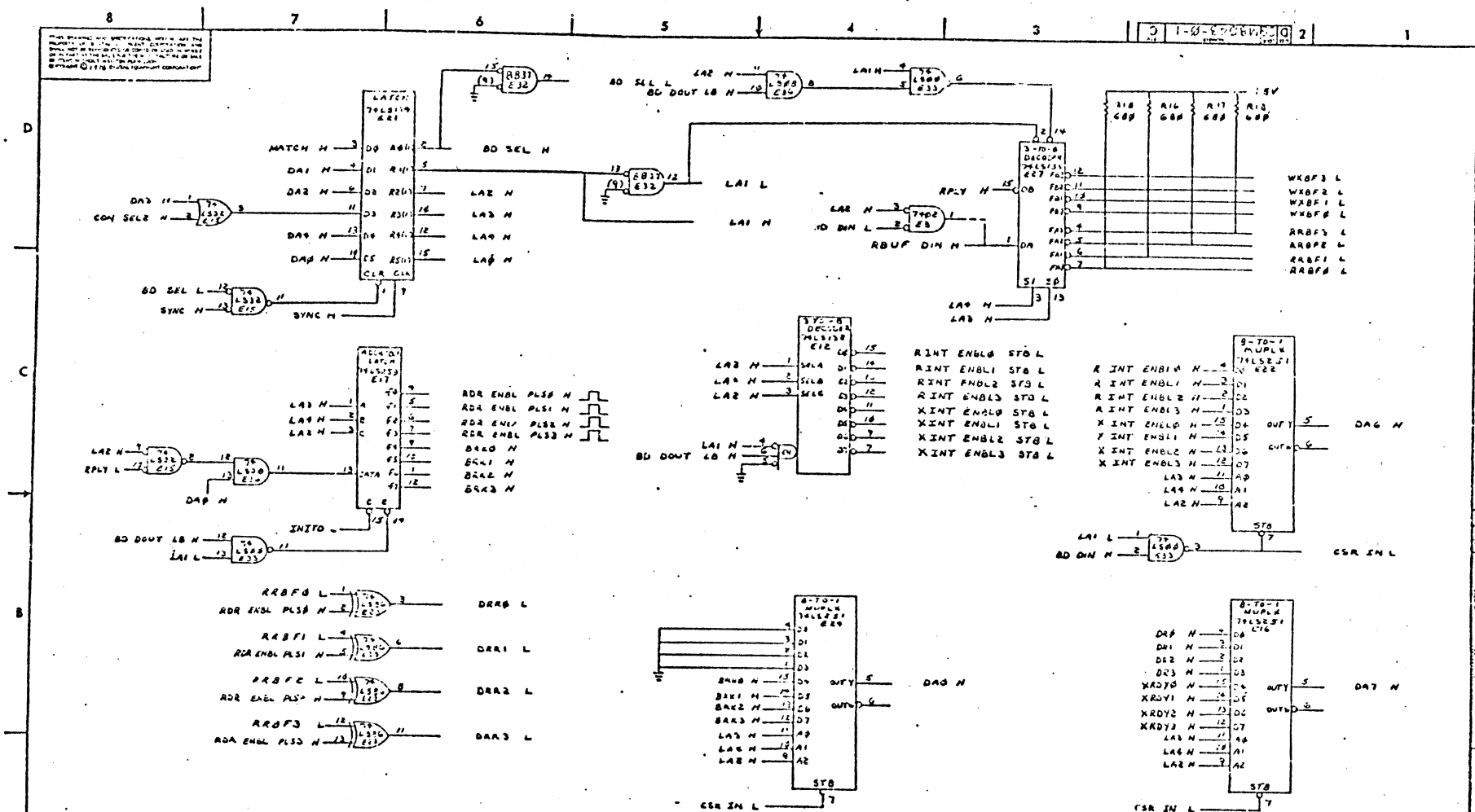
NOTES

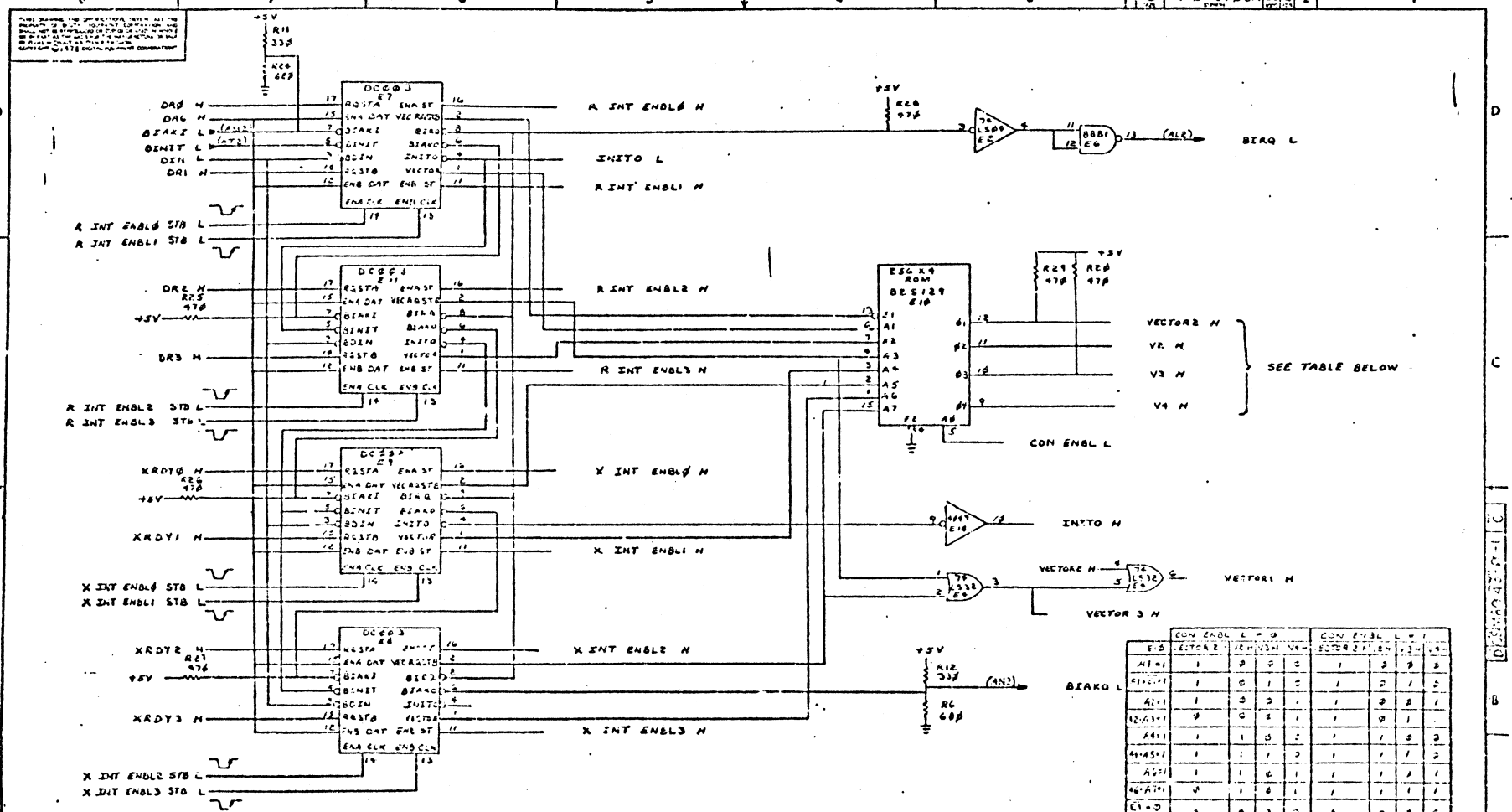
① R_X IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS 422 OPERATION (100 Ω, 1/4 W NON WIRE WOUND)
R30 - CHANNEL 0
R31 - CHANNEL 1
R32 - CHANNEL 2
R33 - CHANNEL 3

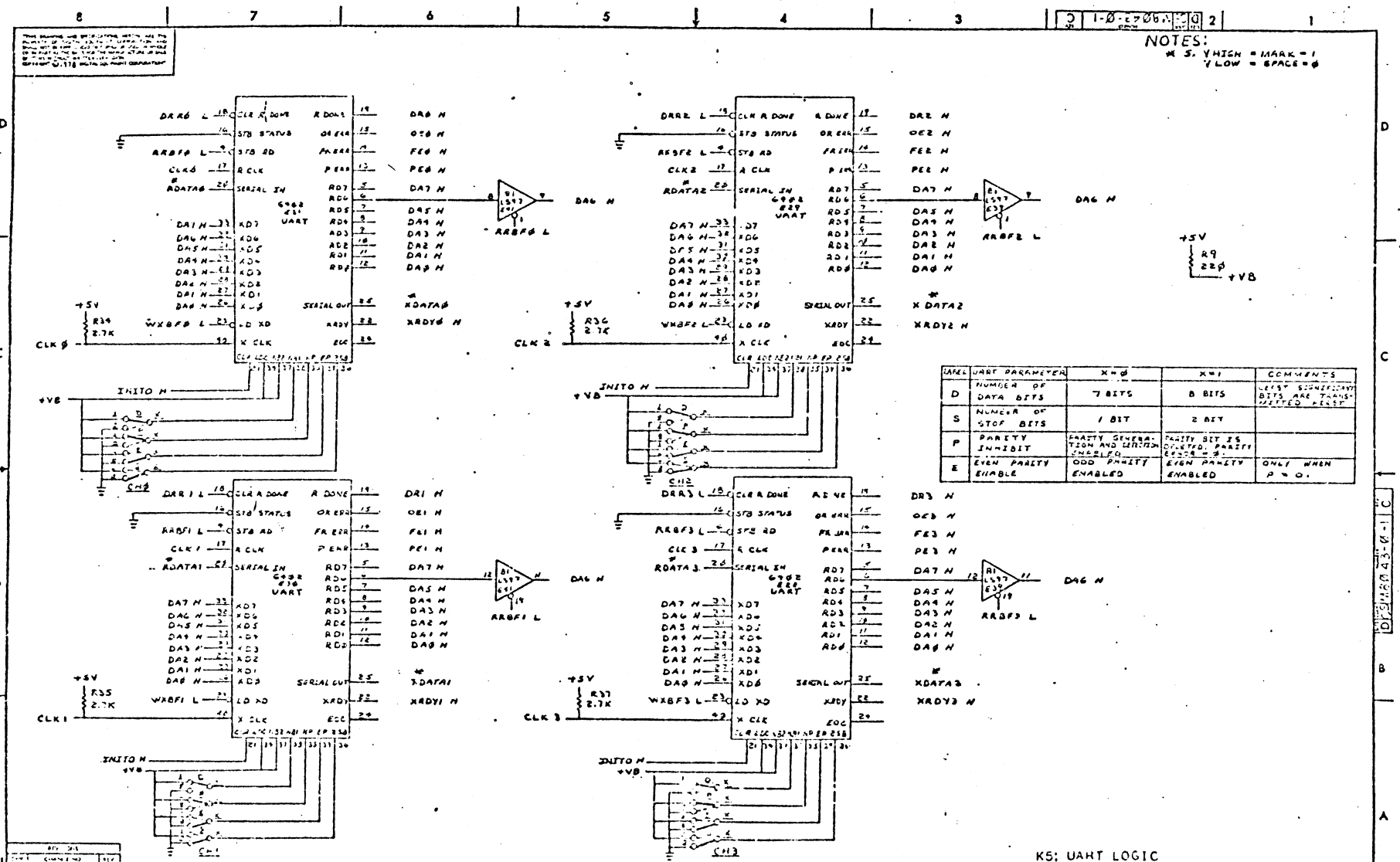
② R_Y IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS 232C/RS 423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3


NOTES:
1. UNDERLINED TERM DESIGNATES LABEL IN ETCH
2. —O—O— DESIGNATES WIRE-WRAP JUMPER NOT INSERTED.
3. —O——O— DESIGNATES WIRE-WRAP JUMPER IS INSERTED FOR SHIPMENT.
BUS XCVR
DC005
COMPARATOR
81LS97
MATCH H
VECTOR2 H
CON ENBL L
CSR IN L
RBUF DIN H
LAI H
KI1BUS ADDRESS/DATA LOGIC
4 SERIAL LINE PER. CTLR.

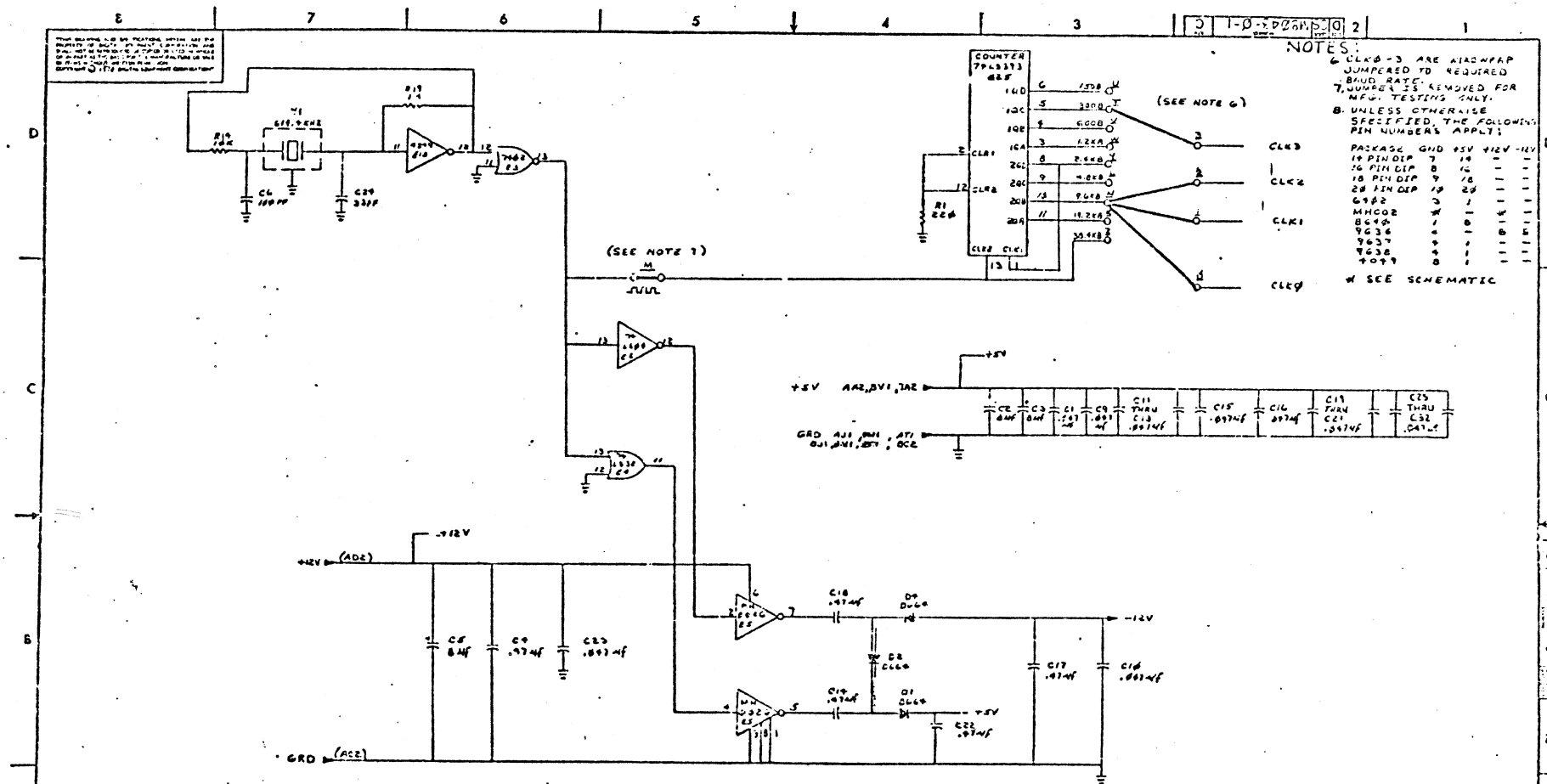

NOTES:
1. TO ENABLE HALT ON RECEIVING BREAK, CONNECT X TO M. TO ENABLE BOOT ON RECEIVING BASAK, CONNECT X TO J.
(SEE NOTE 1)
FE3 H
BDCOK H
BHALT L
BDMGI L
BDMGO L
BSYNC L
SYNC H
BD SEL L
BDOUT L
BD DOUT H
LAØ H
BD DOUT LØ H
BD DIN L
BD DIN H
BDIN L
DIN L
DØØ3
D3
A22
2.2K
C9
1000 PF
BD DIN H
BD DOUT H
VECTØ1 H
RPLY L
BRPLY L
RPLY H
K2: CONTROL AND HALT/BOOT LOGIC
SERIAL LINE PER. CTLR.
DCS-M6044-D-1

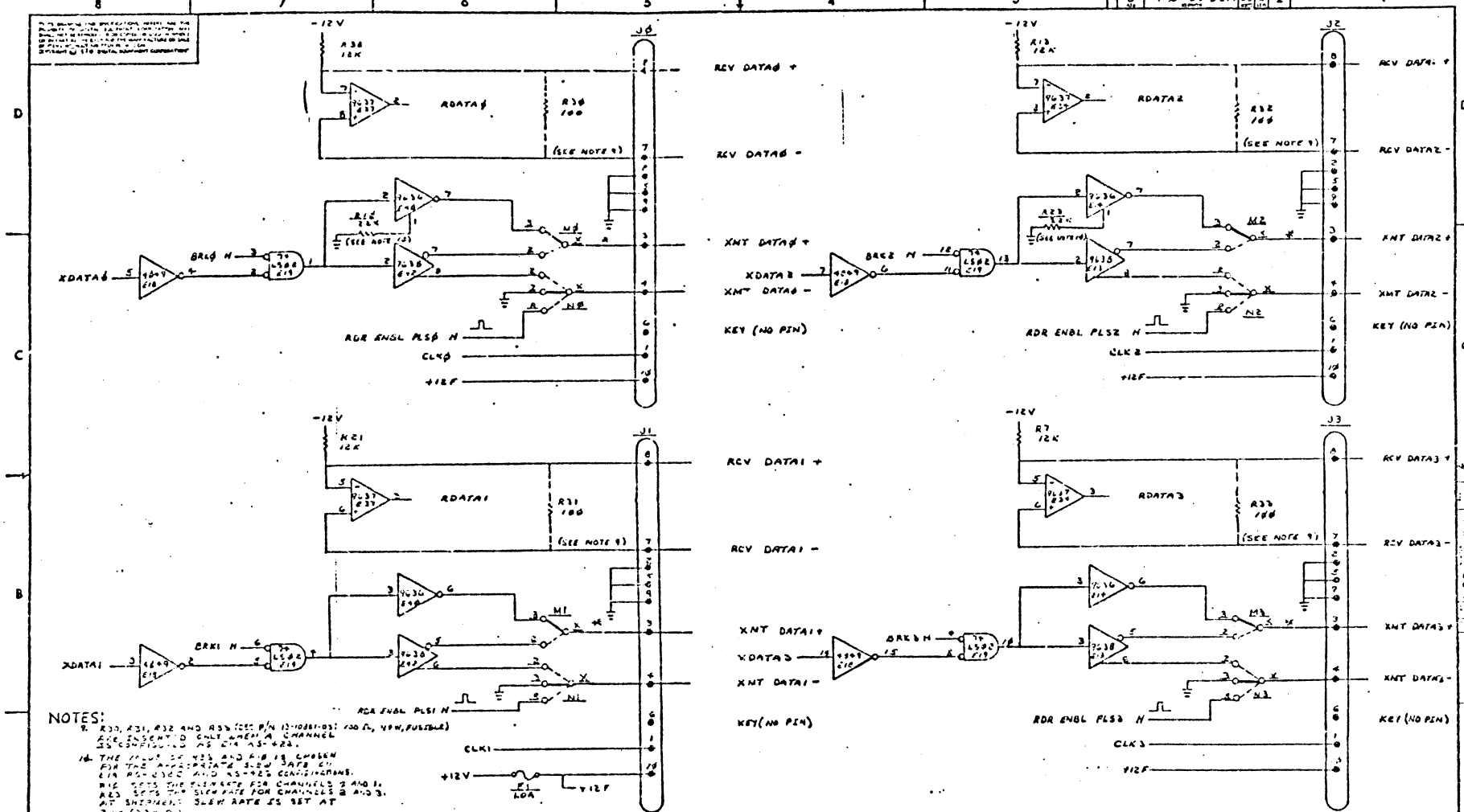

K3: ADDRESS LATCH AND REGISTER LOGIC
4 SERIAL LINE PER. CTLR.
MSC43-C-1
C
D
LATCH
MATCH H
DA1 H
DA2 H
DA9 H
DA8 H
BD SEL H
LA1 L
LA1 H
LA2 H
LA3 H
LA9 H
LA8 H
SYNC H
DA3
CON SEL2 H
BD SEL L
SYNC H
3-TO-8 DECODER
RPLY H
LA2 H
TO DIN L
RBUF DIN H
LA9 H
LA3 H
+5V
WK8F3 L
WK8F2 L
WK8F1 L
WK8F0 L
RR8F3 L
RR8F2 L
RR8F1 L
RR8F0 L
ADDRESS LATCH
LA3 H
LA9 H
LA2 H
RPLY L
DA8 H
INIT0 L
BD DOUT L8 H
LA1 L
RDR ENBL PLS8 H
RDA ENBL PLS1 H
RDA ENBL PLS2 H
RER ENBL PLS3 H
8AK0 H
8AK1 H
8AK2 H
8AK3 H
SYNC DECODER
LA3 H
LA9 H
LA2 H
LA1 H
BD DOUT L8 H
RINT ENBL0 STB L
RINT ENBL1 STB L
RINT ENBL2 STB L
RINT ENBL3 STB L
XINT ENBL0 STB L
XINT ENBL1 STB L
XINT ENBL2 STB L
XINT ENBL3 STB L
9-TO-1 MUPLX
R INT ENBL0 H
R INT ENBL1 H
R INT ENBL2 H
R INT ENBL3 H
X INT ENBL0 H
Y INT ENBL1 H
X INT ENBL2 H
X INT ENBL3 H
LA3 H
LA9 H
LA2 H
STB
OUT Y
OUT 6
DA6 H
LA1 L
BD DIN H
CSR IN L
RR8F0 L
RDR ENBL PLS0 H
RR8F1 L
RDA ENBL PLS1 H
RR8F2 L
RDA ENBL PLS2 H
RR8F3 L
RDA ENBL PLS3 H
DRR0 L
DRR1 L
DRR2 L
DRR3 L
8AK0 H
8AK1 H
8AK2 H
8AK3 H
LA3 H
LA9 H
LA8 H
LA2 H
CSR IN L
DA0 H
DA1 H
DA2 H
DA3 H
XRDY0 H
XRDY1 H
XRDY2 H
XRDY3 H
DA7 H


DR0 H
DR1 H
BIAKI L
BINIT L
DEN L
R INT ENBL0 STB L
R INT ENBL1 STB L
DR2 H
DR3 H
R INT ENBL2 STB L
R INT ENBL3 STB L
XRDY0 H
XRDY1 H
X INT ENBL0 STB L
X INT ENBL1 STB L
XRDY2 H
XRDY3 H
X INT ENBL2 STB L
X INT ENBL3 STB L
R INT ENBL0 H
INIT0 L
R INT ENBL1 H
R INT ENBL2 H
R INT ENBL3 H
X INT ENBL0 H
X INT ENBL1 H
X INT ENBL2 H
X INT ENBL3 H
BIAKO L
INIT0 H
VECTOR2 H
V2 H
V3 H
V4 H
SEE TABLE BELOW
CON ENBL L
VECTOR1 H
VECTOR 3 H
K4: INTERRUPT, VECTOR AND INIT LOGIC
4 SERIAL LINE PER. CTLR.
D-BS-8043-0-1
C



LABEL	UART PARAMETER	X=0	X=1	COMMENTS
D	NUMBER OF DATA BITS	7 BITS	8 BITS	LEAST SIGNIFICANT BITS ARE TRANSMITTED FIRST
S	NUMBER OF STOP BITS	1 BIT	2 BIT	
P	PARITY INHIBIT	PARITY GENERATION AND VERIFICATION ENABLED	PARITY BIT IS OMITTED, PARITY ERROR = 0	
E	EVEN PARITY ENABLE	ODD PARITY ENABLED	EVEN PARITY ENABLED	ONLY WHEN P = 0.


NOTES:
6. CLK0-3 ARE HARDWARE JUMPERED TO REQUIRED BAUD RATE.
7. JUMPER J5 REMOVED FOR MFG. TESTING ONLY.
8. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:
PACKAGE GND +5V +12V -12V
14 PIN DIP 7 14 — —
16 PIN DIP 8 16 — —
18 PIN DIP 9 18 — —
24 PIN DIP 12 24 — —
6952 3 1 — —
MHC02 # — # #
8640 1 8 — —
9636 4 — 8 8
9637 4 1 — —
9638 4 1 — —
7099 8 1 — —
SEE SCHEMATIC
(SEE NOTE 6)
(SEE NOTE 7)
CLK3
CLK2
CLK1
CLK0
+5V
-12V
GRD
(ADZ)
(ACZ)
K6: PWR DIST, BAUD RATE GEN & -12V CIRCUITRY
4 SERIAL LINE PER. CTLR.
DCS M8043-0-1
SCALE NONE



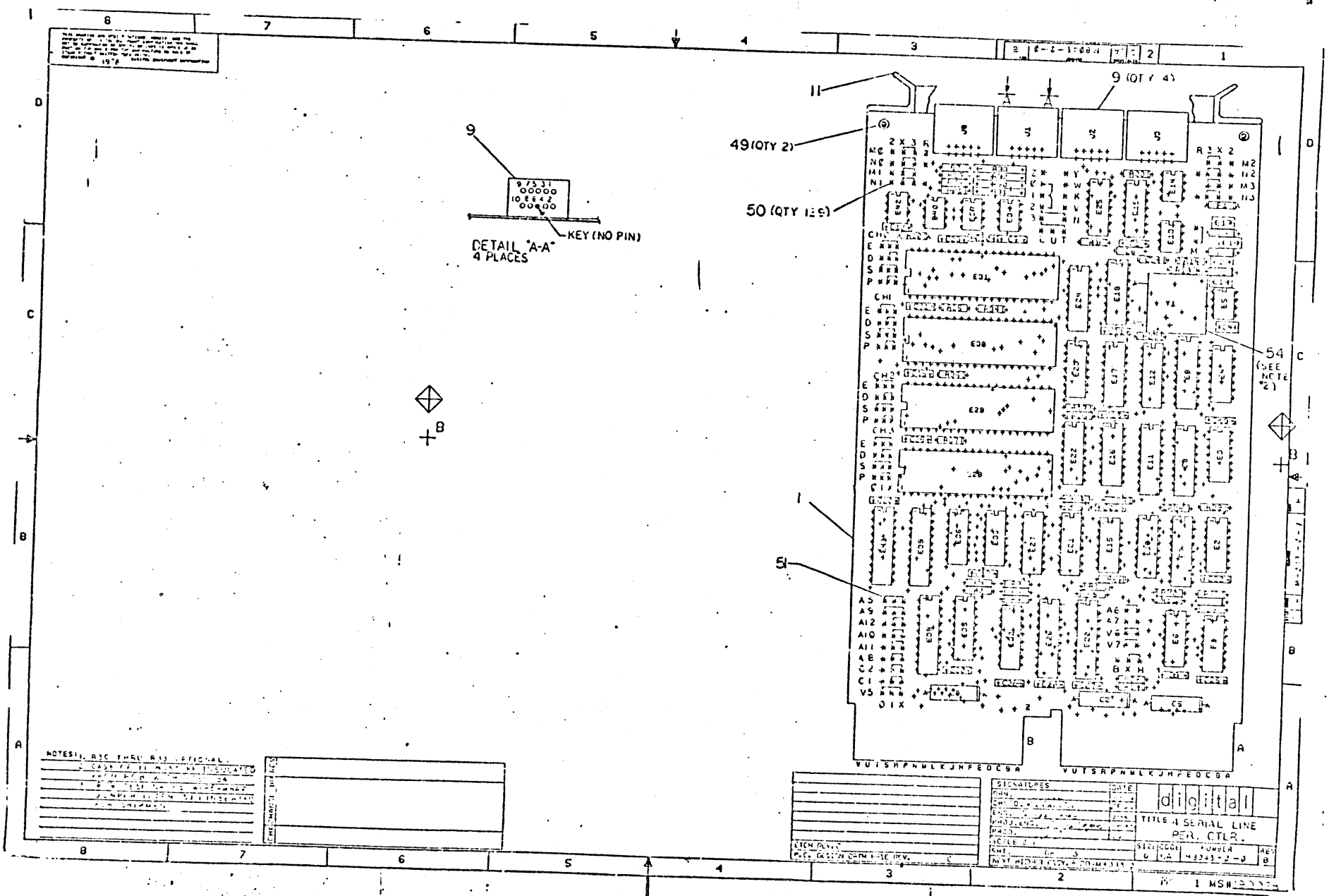
NOTES:

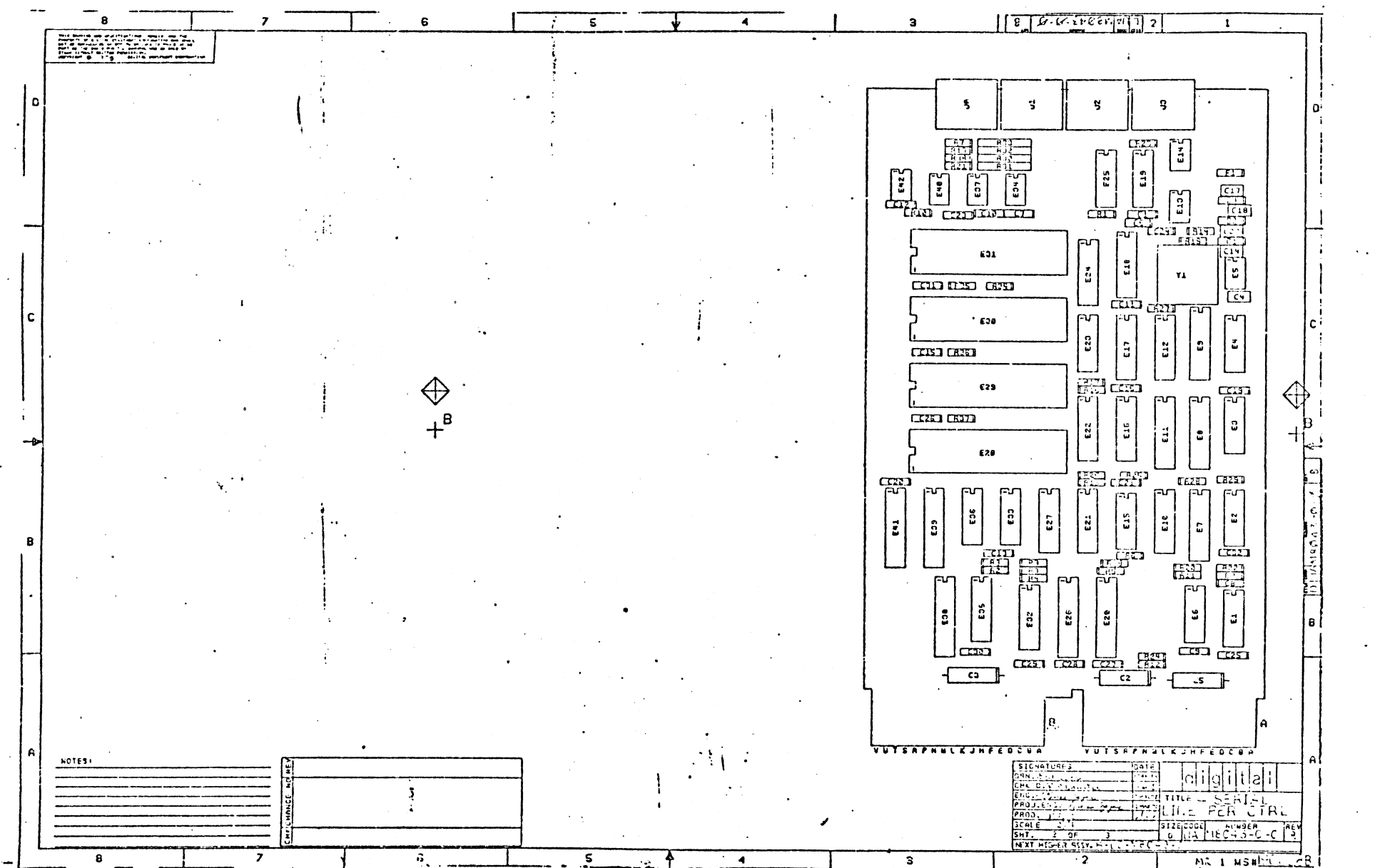
1. R30, R31, R32 AND R33 (SEE P/N 13-1088-03): 100 Ω, 1/4W, FUSIBLE)
   ARE PRESENT ONLY WHEN A CHANNEL IS CONFIGURED AS EIA RS-422.
2. THE VALUE OF R23 AND R38 IS CHOSEN FOR THE APPROPRIATE SLEW RATE OF EIA RS-232C AND RS-423 CONFIGURATIONS.
   R38 SETS THE SLEW RATE FOR CHANNELS 2 AND 3.
   R23 SETS THE SLEW RATE FOR CHANNELS 0 AND 1.
   AT SHIPMENT, SLEW RATE IS SET AT 2 MS (22K Ω).

* IF V LOW = MARK = 1
   V HIGH = SPACE = 0

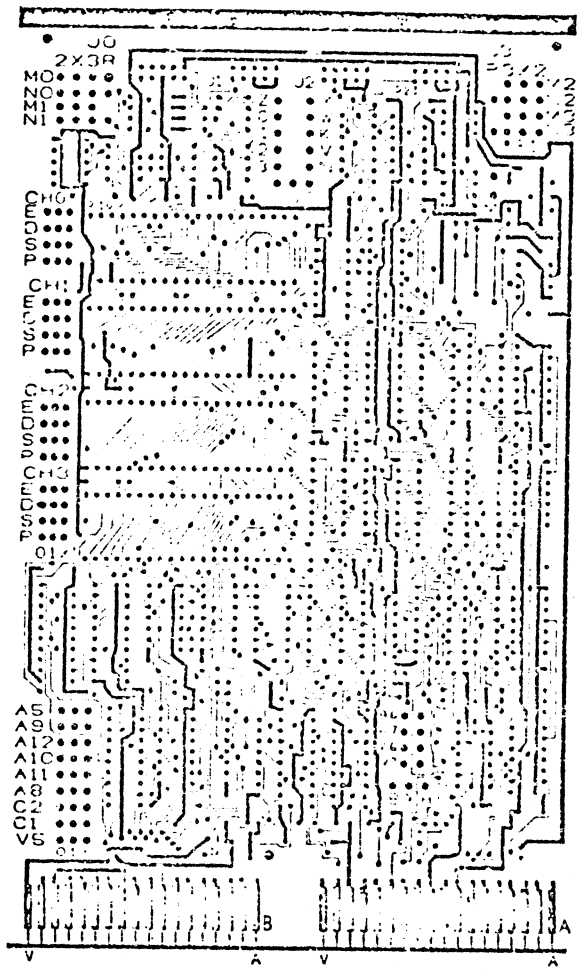
K7: LINE INPUT/OUTPUT LOGIC

TITLE 4 SERIAL LINE PER. CTLR.
DRAWING NUMBER DC336-0-1
REV C
SHEET 7 OF 7

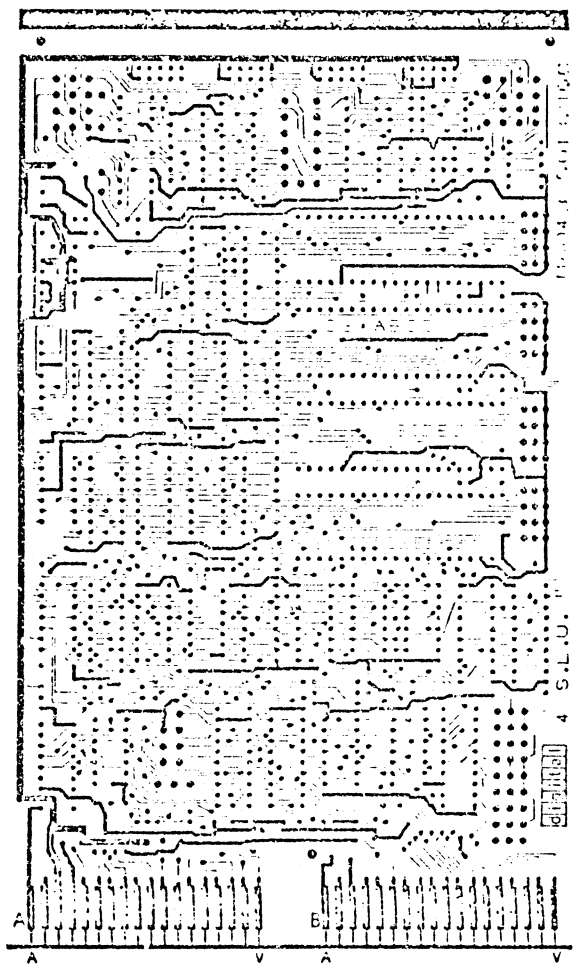

9
DETAIL "A-A"
4 PLACES
KEY (NO PIN)
11
9 (QTY 4)
49 (QTY 2)
50 (QTY 129)
54
(SEE NOTE 2)
1
51
digital
TITLE 4 SERIAL LINE
PER. CTLR.


NOTES:
digital
SERIAL LINE PCB CTRL

SIDE 1



SIDE 2



4 SERIAL LINE PER CTLR

DUA MSØ43 - Ø - Ø

MR 1

WIRE TABLE

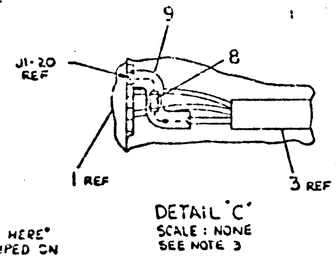
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONN	FROM WITH	TO CONN	TO WITH	REMARKS	
3	22	BLK	P1-2	ITEM 5	J1-7	ITEM 13		PAIR
		RED	P1-3	ITEM 5	J1-2	ITEM 13		
		DRAIN	—	ITEM 6 ENDS	J1-1, SEE NOTE 1	ITEM 13		
		DRAIN			CUT, SEE NOTE 2	—		PAIR
		BLK	CUT	—	CUT	—	SEE NOTE 2	
		WHT	P1-8	ITEM 5	J1-3	ITEM 13		
		BLK	CUT	—	CUT	—	SEE NOTE 2	PAIR
		GRN	P1-10	ITEM 5	—	—	SEE NOTE 3	
		DRAIN	CUT	—	CUT	—	SEE NOTE 2	
7		YEL	P1-7	ITEM 5	P1-9	ITEM 5	2 IN LONG	
7	22	YEL	J1-6	ITEM 13	J1-4	ITEM 13	2 IN LONG	

LEGEND

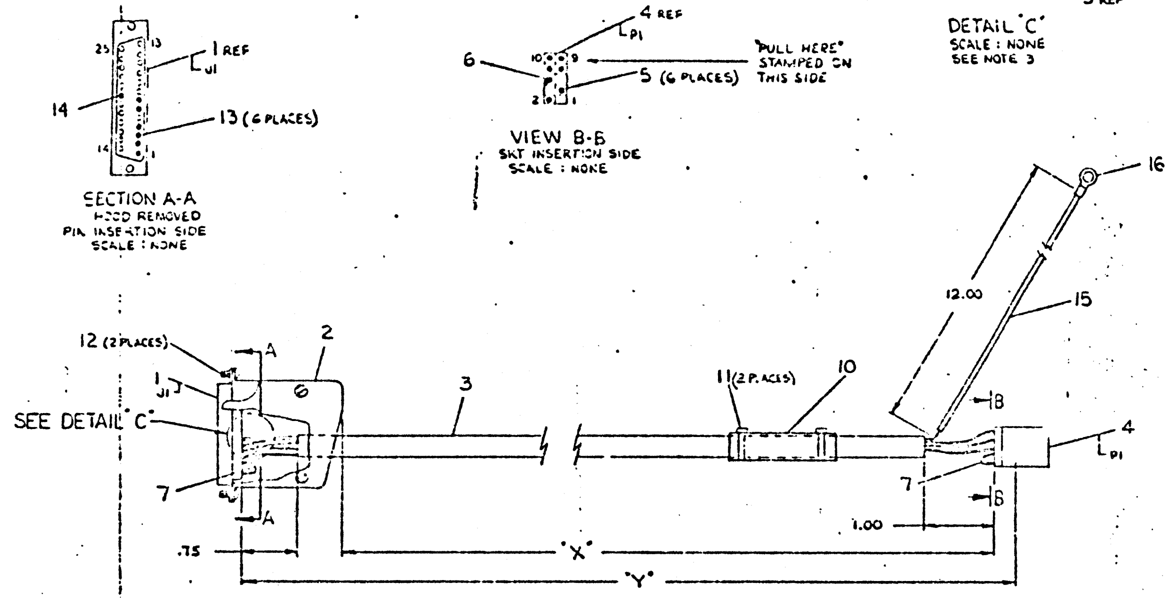
NUMBER	DIM "X" VAR.	DIM "Y" PRECUT VAR.
6C21B-05	5 FT 0 IN	5 FT ± 2 IN

NOTES:

1. DRAIN WIRES TO BE ENCLOSED WITH ITEM 15 FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER CONTACT OR TERMINAL.
2. MYLAR SHIELDS AND SPECIFIED WIRES ARE CUT FLUSH WITH JACKET.
3. AT J1 END, WIRE FROM P1-10 (GRN) IS SOLDERED TO ITEM 8. OTHER END OF ITEM 8 IS SOLDERED TO ITEM 14, ITEM 8 PUT ON AND INSTALLED IN J1-20.



DETAIL "C"
SCALE : NONE
SEE NOTE 3



SECTION A-A
HOOD REMOVED
PIN INSERTION SIDE
SCALE : NONE

VIEW B-B
SKT INSERTION SIDE
SCALE : NONE

QTY	DESCRIPTION	PART NO.	ITEM NO.
1	TERMINAL, RING	9007930	16
A/R	TUBING, THIN EXTRUDED 12GA	[illegible]	15
1	CONTACT, PIN	1210493-45	14
6	CONTACT, PIN	1210493-[illegible]	13
1	SCREW, RETAINER MALE	1210493-51	12
2	TIE WRAP	[illegible]	11
1	LABEL, CABLE IDENT	[illegible]	10
A/R	TUBING, HEAT SHRINK, CLR	[illegible]	9
1	RESISTOR, 150 Ω, 5%, ¼ W	[illegible]	8
A/R	WIRE, 22 AWG STRANDED (YEL)	[illegible]-44	7
1	PLUG, KEYING	1215416-00	6
6	CONTACT, SOCKET	1214267-00	5
1	TERMINATOR, HOUSING	1214268-00	4
A/R	CABLE, 3 PR, SHIELDED	[illegible]	3
1	HOOD & STRAIN RELIEF	1210493-50	2
1	SHELL & INSERT	1210493-[illegible]	1

TITLE: CABLE, MODEM ASSY.

MATERIAL: SEE PARTS LIST

SIZE: D

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DLV11-F ENGINEERING SPECIFICATION

10.0 ENVIRONMENTAL REQUIREMENTS

10.1 Ambient Temp

Operating	5°C to 60°C (41°F to 140°F)
Non-Operating	-40°C to 80°C (-40°F to 176°F)

10.2 Humidity

Operating	10% to 95%, Max wet bulb 32°C (90°F) and Min dew point 2°C (36°F)
Non-Operating	5% to 95%

10.3 Altitude

Operating	2.4km (8,000 ft)
Non-Operating	9.1km (30,000 ft)

SIZE	CODE	NUMBER	REV
A	[redacted]	DLV11-F-?	

DEC FORM NO [redacted]
DEA 100

contains a crystal oscillator which is connected to a dual baud rate generator which provides appropriate clock signals to the UART. A separate clock is available for the transmitter for split speed operation.

8.2.7 -12V Charge Pump

This circuit provides the -12 volts needed by the UART, the driver (1488) and the FOR RUN current loop. The maximum current supplied by this -12V charge pump is 40mA.

8.2.8 Reader Run Circuit

The Reader Run Circuit is used to advance the paper tape reader in the DEC modified TTY units. This is performed by setting bit 8 of the RCSR to a 1. The Reader Run Circuit then will advance the paper tape one position and serial data will start to be received from the TTY. The start bit of this serial data is used by the Reader Run Circuit to automatically reset the internal bit 8 flip-flop.

8.2.9 20mA Interface

This circuit converts TTL level serial data to standard 20mA Current Loop Serial Data and vice versa. This circuit allows direct connection to DECs LA36, VT52, etc. and to the DEC modified TTY. Both the receiver and transmitter may operate in either the active or passive mode.

8.2.10 EIA Interface

This interface provides the proper level converters for serial data for connection to EIA terminals such as the VT05 or the model 37 TTY through a null modem. (See EIA standard RS-232-C).

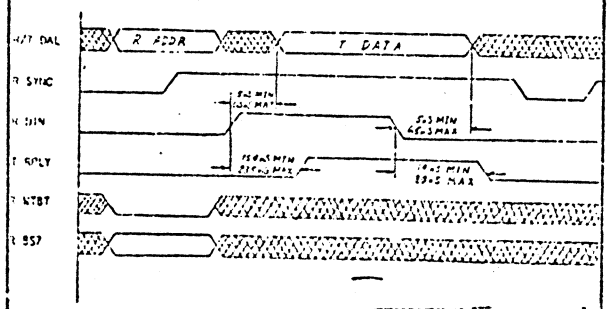
This circuit drives EIA Data Terminal Ready, EIA Request to Send signals to the ON position, thus making it possible for the DLV11-F to interface to the Model 103A2 datasets which will automatically answer incoming calls. This type of connection, however, does not provide for properly terminating the call.

EIA FORCE BUSY signal is also strapped ON for use with the model 103E modems.

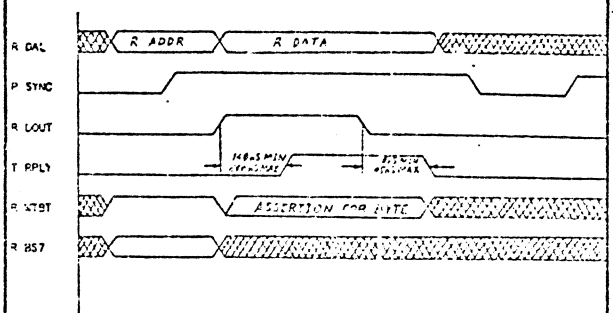
9.0 TIMING DIAGRAMS

In the following timing diagrams, signals are referenced from the output of the bus receiver to the input of the bus driver.

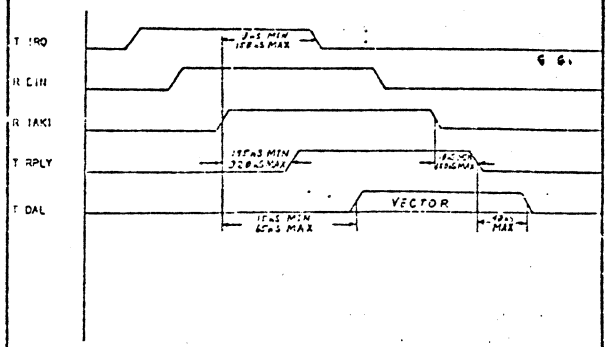
9.1 DAT Bus Cycle Timing



9.2 DATO or DATOB Bus Cycle



9.3 Interrupt Timing



Bit	Name	Meaning and Operation
1	RESERVED	Not applicable. Read as 0s.
0	BREAK	When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.

7.1.4 Transmitter Buffer Register

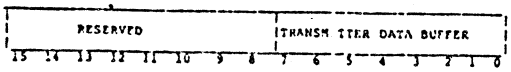


FIGURE 5 TRANSMITTER BUFFER REGISTER (XBUF) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-8	RESERVED	Not applicable. Undefined when read.
7-0	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right justified into the least significant bits. Write only bits. Undefined when read.

7.2 Interrupts

The DLV11-F has two interrupt channels: one for the receiver section and one for the transmitter section. These two channels operate independently; however, if simultaneous interrupt requests occur, the receiver has priority.

A transmitter interrupt can occur only if the interrupt enable bit (XMIT INT ENB) in the transmitter status register is set. With XMIT INT ENB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver data interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. With RCVR INT ENB set, setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus.

7.3 Timing Considerations

When programming the DLV11-F Asynchronous Line Interface, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter and break generation logic are discussed in the following paragraphs.

7.3.1 Receiver

The RCVR DONE flag (bit 7 in the RCSR) sets when the Universal Asynchronous Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

7.3.2 Transmitter

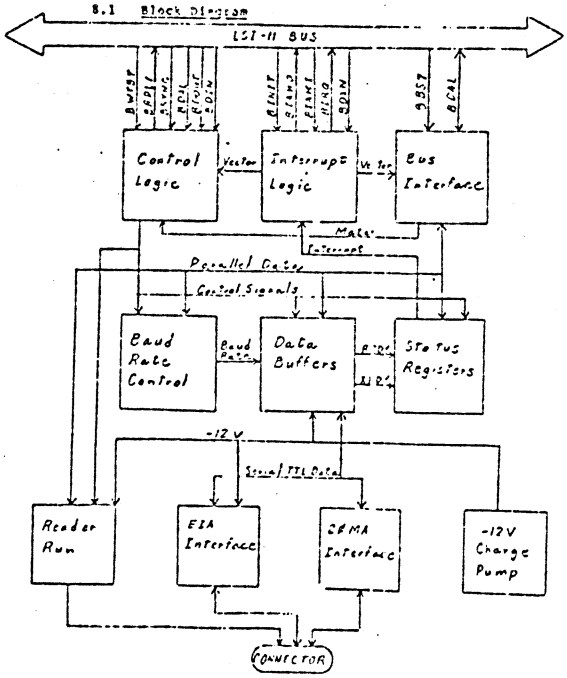
The transmitter section of the UART is also double buffered. The XMIT RDY flag (bit 7 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

7.3.3 Break Generation Logic

When the BPRAK bit is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. Therefore, because the transmitter section of the UART is double buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be a null.

8.0 LOGIC DESCRIPTION

8.1 Block Diagram



8.2 Logic Discussion

8.2.1 Bus Interface

The bus interface is comprised partly of DC005 transceiver chips. These chips contain bus transceivers that connect the BDAL lines with the internal tri-state bidirectional bus. This chip also provides jumper inputs for address selection and asserts a MATCH H open collector output signal when there is an address match. These chips also contain jumper inputs for vector address selection that allow the vector to be asserted on the BDAL lines of the bus.

8.2.2 Interrupt Logic

The interrupt logic provides for two interrupts, A and B, with A having the highest priority. Part A services the receiver interrupts and Part B services the transmitter interrupts.

8.2.3 Control Logic

The major portion of the control logic is provided by the DC004 protocol chip. The protocol chip receives BDIN, BDOUT, BSYNC, BWTBT and issues BRPLY. It also generates outputs based on the three least significant BDAL lines indicating which of the on-board registers are being addressed. It also indicates which byte or bytes are being operated on and whether the transaction is a DIN or, DOUT.

8.2.4 Status Registers

There are two status registers on the module, a receiver status register and a transmitter status register. Information is fed to the flip-flops comprising the status registers via the tri-state DAT bus. Information is read from the registers also through this same DAT bus.

8.2.5 Data Buffers

The data buffers are comprised of a Universal Asynchronous Receiver/Transmitter (UART). The UART accepts parallel data and serializes it with start bits and stop bits for transmitter operations. It also accepts serial data and changes it in parallel form for receiver operations.

8.2.6 Baud Rate Control

The baud rate is jumper selectable or program selectable over the range 50 - 19200 baud. The circuit

7.0 PROGRAMMING SPECIFICATION

All software control of the DLV11-F Asynchronous Line Interface is performed by means of four device registers. These registers are in sequential addresses and can be read or loaded (with the exceptions noted) using any LSI-11 instruction referring to their addresses.

Figures 2 through 5 show the bit assignments for the four device registers.

The reserved and write only bits are always read as 0s* (with the exception of the Transmitter Buffer Register). Loading reserved or read only bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by issuing a programmed RESET instruction or the occurrence of a power-up or power-down condition of the processor power supply.

In the following descriptions, "transmitter" refers to those registers and bits involved in accepting a parallel character from the LSI-11 Bus for serial transmission to the external device; "receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the LSI-11 Bus.

7.1 Device Registers

7.1.1 Receiver Status Register

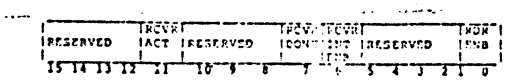


FIGURE 2 RECEIVER STATUS REGISTER (RCSR) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-12	RESERVED	Not applicable. Read as 0s.
11	RCVR ACT (Receiver Active)	When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the START bit which is the beginning of the input serial data from the device and is cleared by the leading edge of RCVR DONE.

*Bits in the Transmitter Buffer are undefined when used.

Bit	Name	Meaning and Operation
		Read only bit; cleared by INIT.
10-8	RESERVED	Not applicable. Read as 0s.
7	RCVR DONE (Receiver Done)	This bit is set when an entire character has been received and is ready for transfer to the LSI-11 Bus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set. Cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 0) is set. Read only bit. Cleared by INIT.
6	RCVR INT ENB (Receiver Interrupt Enable)	When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets. Read/write bit; cleared by INIT.
5-1	RESERVED	Not applicable. Read as 0s.
0	RDR ENB (Reader Enable)	When set, this bit advances the paper tape reader in DEC modified TTY units and clears the RCVR DONE bit (bit 7). This bit is cleared at the middle of a START bit which is the beginning of the serial input from an external device. Also cleared by INIT. Write only bit.

7.1.2 Receiver Buffer Register

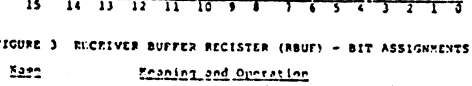


FIGURE 3 RECEIVER BUFFER REGISTER (RBUF) - BIT ASSIGNMENTS *

Bit	Name	Meaning and Operation
15	ERROR	Used to indicate that an error condition is present. This bit is the logical OR

Bit	Name	Meaning and Operation
		of OR ERR, FR ERR and P ERR (bits 14, 13, and 12 respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is not connected to the interrupt logic. Read only bit, cleared by removing the error producing condition. Cleared by INIT.
	NOTE:	ERROR indications remain present until the next character is received, at which time the error bits are updated.
14	OR ERR (Overrun Error)	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read only bit. Cleared by INIT.
13	FR ERR (Framming Error)	When set, indicates that the character that was read had no valid STOP bit. Read only bit. Cleared by INIT.
12	P ERR (Parity Error)	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read only bit. Cleared by INIT.
11-8	RESERVED	Not applicable. Read as 0s.
7-0	RECEIVED DATA BITS	Holds the character just read. If less than eight bits are selected, then the buffer is right justified into the least significant bit positions. In this case, the higher unused bit or bits read as 0s. Read only bits, not cleared by INIT.

7.1.3 Transmitter Status Register

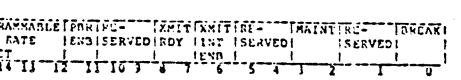


FIGURE 4 TRANSMITTER STATUS REGISTER (XCSR) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-12	PBR SEL (Programmable Baud Rate Select)	When set, these bits choose a baud rate from 50 - 19200 baud. See TABLE 1. Write only bits; read as 0s. Not cleared by INIT.
11	PBR END (Programmable Baud Rate Enable)	This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write only bit; read as 0. Not a latched bit.
10-8	RESERVED	Not applicable, read as 0s.
7	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT END (bit 6) is also set. Ready only bit. Set by INIT. Cleared by loading the transmitter buffer.
6	XMIT INT END (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set. Read/write bit; cleared by INIT.
5-3	RESERVED	Not applicable. Read as 0s.
2	MAINT (Maintenance)	Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed. Read/write bit; cleared by INIT.

6.0 CONFIGURATIONS

6.1 Jumper Definitions

Jumper	Definition
A3-A12	Jumpers inserted will provide a match with the corresponding bus Address bit. Selectable from 160000 to 177777.
V3-VP	Jumper inserted will assert the corresponding Vector address bit on the LSI-11 Bus. Selectable from 000 to 774.
R0-R3	UART Receiver and Transmitter baud rate select jumpers during common speed operation. UART Receiver only baud rate select jumpers during split speed. See Table 1.
T0-T3	UART Transmitter baud rate select jumpers during split speed operation and when the Maintenance Bit is set. See Table 1.
BG	Jumper inserted to enable Break Generation.
P	Jumper inserted for Parity generation by the UART. (Odd or even parity is selected by the -E jumper.)
-E	Jumper removed for Even parity and inserted for odd parity. (Receiver checks for appropriate parity and transmitter inserts the appropriate parity.)
1, 2	Selects desired number of data bits. (I = Inserted, R = Removed).

2	1	No. of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

C, C1	Jumpers inserted for Common speed operation on UART Receiver and Transmitter clocks. (Note that jumpers S and S1 must be removed.)
S, S1	Jumpers inserted for Split speed operation on UART Receiver and Transmitter clocks. (Note that jumpers C and C1 must be removed.)

Jumper	Definition
PD	Jumper inserted to enable Programmable Baud Rate.
M	Jumper inserted will assert the BUS HALT L on all received Framing Errors except when Maintenance Bit is set.
B, -B	B jumper inserted to assert BUS BCOK L on all received Framing Errors except when the Maintenance Bit is set. (-B jumper must be removed.)
1A,2A,3A	Jumpers inserted make the 20mA Current Loop receiver active. (Jumpers 1P and 2P must be removed.)
1P, 2P	Jumpers inserted make the 20mA Current Loop receiver passive. (Jumpers 1A, 2A and 3A must be removed.)
4A, 5A	Jumpers inserted make the 20mA Current Loop transmitter active. (Jumpers 3P and 4P must be removed.)
3P, 4P	Jumpers inserted make the 20mA Current Loop transmitter passive. (Jumpers 4A and 5A must be removed.)
-EP	Jumper removed enables the UART Error Flags to be read in the high byte of the Receiver Buffer.
MT	Jumper inserted to enable operation of the Maintenance bit (TCSR bit 2).
M, M1	Manufacturing use only.

NOTE: Jumpers are labelled to indicate whether they are inserted or removed to enable their corresponding features.

. (No additional marking) - Jumper inserted to enable feature.

("-" marking) - Jumper removed to enable feature.

TABLE 1

UART BAUD RATE SELECTIONS

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 (See Note 1)
Program Control (TCSR)					
Receive Jumpers	R3	R2	R1	R0	
Transmit Jumpers	T3	T2	T1	T0	Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200 (See Note 2)

I = Jumper Inserted = Program Bit Cleared

R = Jumper Removed = Program Bit Set

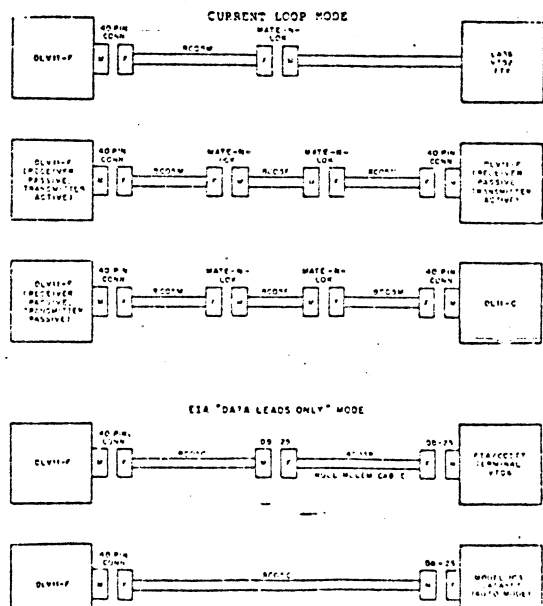
NOTE 1: Bit 11 of the TCSR (Write Only Bit) must also be set in order to select a new Baud Rate under program control. Also, jumper PD must be inserted to enable Baud Rate selection under program control.

NOTE 2: At 19.2K baud, actual clock frequency is 316.6 KHz (1.12% error).

6.2 Cable Configuration Example

FIGURE 1 illustrates the method of connecting cables between the DLV11s and associated external devices.

FIGURE 1



DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION — DATE 6 MARCH 73

TITLE DLV11-F ENGINEERING SPECIFICATION

REVISIONS

REV	DESCRIPTION	ECO NO	DWG NO	DATE	APPD BY	DATE

ENGR [signature] APPD [signature] | SIZE A | CODE | NUMBER DLV11-F | REV

DEC FORM NO [illegible]
DRA 108

SHEET 1 OF 35

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DLV11-F ENGINEERING SPECIFICATION

TABLE OF CONTENTS

SIZE A | CODE | NUMBER DLV11-F | REV

DEC FORM NO [illegible]
DRA 108

SHEET 2 OF 35

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DLV11-F ENGINEERING SPECIFICATION

1.0 SCOPE

The scope of this document is to present the description and specification for the DLV11-F (M8028 Asynchronous Line Interface. It describes the DLV11-F both physically and functionally.

SIZE A | CODE | NUMBER DLV11-F | REV

DEC FORM NO [illegible]
DRA 108

SHEET 3 OF 35

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DLV11-F ENGINEERING SPECIFICATION

2.0 GENERAL DESCRIPTION

The DLV11-F is an interface between an asynchronous serial line and the LSI-11 Bus. The LSI-11 Bus circuitry is designed in accordance with DEC Std 150, "LSI-11 Bus Specification". All circuitry is housed on one dual extended height module (M8028) and mounts in any standard LSI-11 backplane. The DLV11-F supports the following two modes of operation:

1. Current Loop Mode

   20mA current loop circuits are supplied to the external device via a female MATE-N-LOCK connector when used with the BC05M-XX cable.

2. EIA "Data Leads Only" Mode

   EIA drivers and receivers are supplied to the external device via a male DB25 connector used with the BC01V-XX cable.

SIZE A | CODE | NUMBER DLV11-F | REV

DEC FORM NO [illegible]
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SHEET 4 OF 35

3.0 APPLICABLE DOCUMENTS

EIA Standard (RS-232-C)

D-CS-M8017

A-MS-1913040 (DC005)

A-PS-1912729 (DC004)

A-PS-1912730 (DC003)

A-PS-2112623 (5016)

DEC Std. 160 (LSI-11 Bus Specification)

DEC Std. 102 (Computer Environment Std.)

4.0 POWER REQUIREMENTS

	AMPS Typ	AMPS Max	WATTS Typ	WATTS Max
+5 Volt ± 5%	1.0 Amps	1.5 Amps	5W	7.5W
+12 Volt ± 3%	150mA	230mA	1.8W	2.8W

5.0 EXTERNAL CONNECTIONS

5.1 DLV11-F Edge Connector Pinning

+5	AA2, BA2	BIRQ L	AL2
+12	AD2		
BBS7	AP2	BRPLY L	AF2
BDAL 0 L	AU2		
BDAL 1 L	AV2	BSYNC L	AJ2
BDAL 2 L	BE2		
BDAL 3 L	BF2	GND	AC2
BDAL 4 L	BH2	GND	AT1
BDAL 5 L	BJ2		
BDAL 6 L	BK2		
BDAL 7 L	BL2	GND	BC2
BDAL 8 L	BM2	BDCOK H	BA1
BDAL 9 L	BN2		
BDAL 10 L	BP2	GND	BT1
BDAL 11 L	BR2	MSPARE A +12V	AK1
BDAL 12 L	BS2	MSPARE A +12V	AL1
BDAL 13 L	BT2	MSPARE B	BK1
BDAL 14 L	BU2	MSPARE B (EXT R CLK)	BL1
BDAL 15 L	BV2		
BDIN L	AH2		
BDOUT L	AE2		
BHALT L	AP1		
BIAK 1 L*	AM2	SEPARI 3 (EXT T CLK)	BH1
BIAK 0 L*	AN2		
BINIT L	AT2		
BDMGIL*	AR2		
BDMGOL*	AS2		

* These signal pairs are not bussed but pass through this module in order to propogate the daisy chain.

5.2 40-Pin Connector Pinning

Header Pin	M8028 Module	BC01V Mader Cable	BC05M 20mA Cable
A	Ground		Ground
B	Ground		
C	Force Busy(EIA)	Force Busy	
D			
E	Serial Input(TTL)	Interlock In <---	Interlock In
F	Serial Output(EIA)	Transmitted Data	
H	20mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	Serial Input+(20mA)		Received Data +
L		External Clock	
M	EIA Interlock	Interlock Out ---	
N		Serial Clock Xmit	
P			
R		Serial Clock Rcvr	
S	Serial Input-(20mA)		Received Data -
T		Clear to Sent	
U			
V	Request to Send (EIA)	Request to Send	
W			
X		Ring	
Y			
Z		Data Set Ready	
AA	Serial Output+(20mA)		Transmitted Data+
BB		Carrier	
CC	Clock Input (TTL)		
DD	Data Terminal Rdy (EIA)	Data Terminal Rdy	
EE	Reader Run-(20mA)		Reader Run -
FF		202 Sec Xmit	
HH	Berg Clock Enb		
JJ		202 Sec Rcvr	
KK	Serial Output-(20mA)		Transmitted Data-
LL			
MM			
NN			
PP	Reader Run+(20mA)		Reader Run +
RR			
SS	Serial Output(TTL)		
TT	+5V		
UU	Ground		Ground
VV	Ground	Ground	Ground

Kanalunabhängige Brücken

Brücke	Bed	Stellung	Std	Anw	Brücke	Bed.	Stellung	Std.	Anw	Brücke	Bed	Stellung	Std.	Anw
A12	Basis - Adresse	X-0 X-1	X		A6	Adr.	R J	X		C1	Konsole auf	X-0 X-1	X	
A11		X-0 X-1	X		A5		X-0 X-1	X		C2	CH3	X-0 X-1	X	
A10		X-0 X-1	X		V7	Basis - Vec	R J	X		Break Reakt. CH3	Inh. Halt Boot	R X-H X-B	X	
A9		X-0 X-1	X		V6		R J	X						
A8		X-0 X-1	X		V5		X-0 X-1			R10	Impulsformung bei V24 je nach Baud-Rate (Tabelle)		120k	
A7		R J	X		M	Konsole	R J	X		R23			120k	

Std.-Adr. 177500 | Anw. - Adr.: | Std.- Vec: 300 | Anw. - Vec:

Einstellung je Kanal

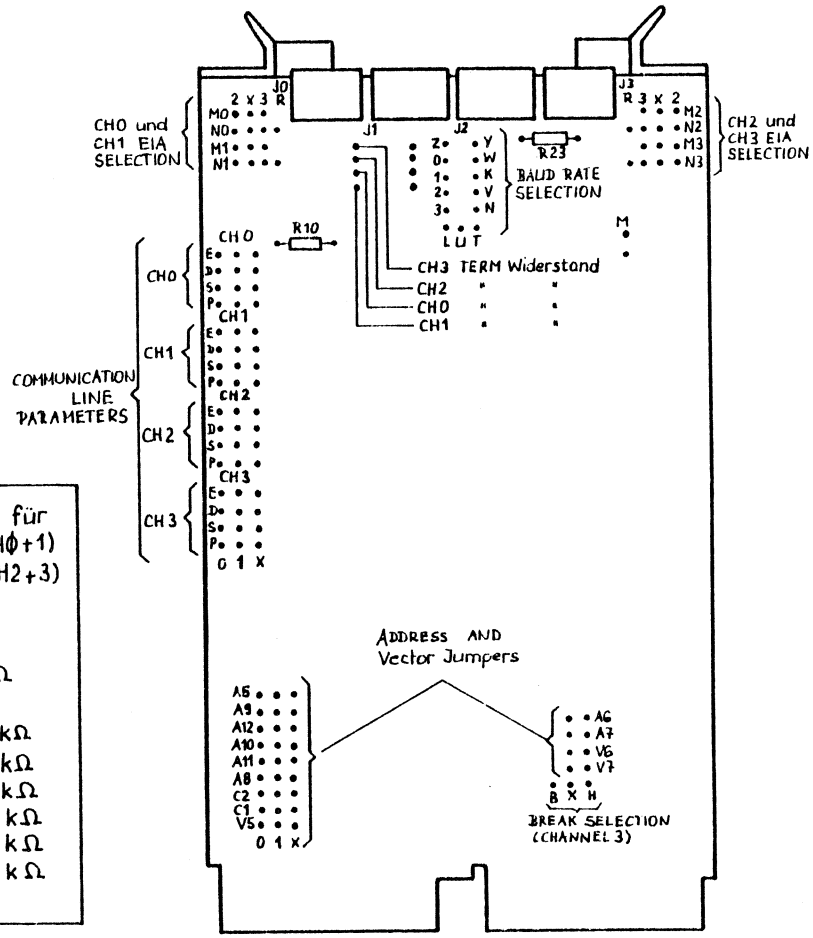
Brücke	Bedeutung	0 Stellung	0 Std	0 Anw	1 Stellung	1 Std	1 Anw	2 Stellung	2 Std	2 Anw	3 Stellung	3 Std.	3 Anw
Baud-Rate	150 bd	0-U			1-U			2-U			3-U		
	300 bd	0-T			1-T			2-T			3-T		
	600 bd	0-V			1-V			2-V			3-V		
	1,2 kbd	0-W			1-W			2-W			3-W		
	2,4 kbd	0-Y			1-Y			2-Y			3-Y		
	4,8 kbd	0-L			1-L			2-L			3-L		
	9,6 kbd	0-N	X		1-N	X		2-N	X		3-N	X	
	19,2 kbd	0-K			1-K			2-K			3-K		
	38,4 kbd	0-Z			1-Z			2-Z			3-Z		
D	7 Datenbits	X-0			X-0			X-0			X-0		
	8 Datenbits	X-1	X		X-1	X		X-1	X		X-1	X	
S	1 Stop Bit	X-0			X-0			X-0			X-0		
	2 Stop Bits	X-1	X		X-1	X		X-1	X		X-1	X	
P	Parity enable	X-0			X-0			X-0			X-0		
	Parity inhibit	X-1	X		X-1	X		X-1	X		X-1	X	
E	Odd Parity	X-0			X-0			X-0			X-0		
	Even Parity	X-1	X		X-1	X		X-1	X		X-1	X	
M+N TERM	Ü-Norm EIA RS 422	X-2 100Ω			X-2 100Ω			X-2 100Ω			X-2 100Ω		
M+N	V24	X-3			X-3			X-3			X-3		
M	20mA mit 900.611	X-3	X		X-3	X		X-3	X		X-3	X	
N		X-R	X		X-R	X		X-R	X		X-R	X	

Tabelle für R10 (CH0+1) R23 (CH2+3)

150 bd – 4,8 kbd	1 MΩ
9,6 kbd	820 kΩ
19,2 kbd	430 kΩ
38,4 kbd	200 kΩ
57,6 kbd	120 kΩ
76,8 kbd	51 kΩ
115,2 kbd	22 kΩ

R = entfernt

J = eingesetzt



					Freimaßtoleranzen		Standard: Bildschirm-Terminals (3=Konsole
							Anwendung:
					78	Tag / Name	Einstell - Tabelle für DLV 11 - J (M8043)
					Bearb	27.11. Hübner	
					Gepr	28.11. Hk	
					Norm		
a	369	6.12.78	Hü				B 900.610.3
Ausgabe	Änderung	Tag	Name		PERIPHERIE COMPUTER SYSTEME		

SLU4 - Serial I/O Board

Instruction Manual

(GTSC Mode 304)

D922101h0e0983

This manual describes how to use the hardware of SLU4 - Serial I/O Board

Document-No. D922101h0e0983

Trademarks:
MUNIX by PCS
DEC, PDP by DEC
UNIX by Bell Laboratories

MODEL 304

SERIAL I/O BOARD

TABLE OF CONTENTS

FEATURES

* Direct Replacement for DLV11-J Serial I/O Board
* Totally Compatible with DEC Software
* All Standard DEC Features
* Each Port Independently Configured for Either EIA RS-232, RS-422, or RS-423
* Four Level Vector Interrupt Structure, Ideal for Multi-User Applications
* Channel 3 can be Independently Configured as System Console

GENERAL

The Model 304 is a four channel serial I/O port for interfacing DEC's Q-bus to asynchronous serial data channels. The 304 is a direct replacement for the DEC four channel Serial I/O Board (Model DLV11-J). It is packaged on the standard 8.9" x 5.2" DEC style dual width board and is electrically and mechanically compatible with DEC's LSI-11, 11/2, and 11/23 Microcomputer Series.

Each channel consists of a UART which receives and converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. The UART's transmitter converts the computer's parallel data into serial form and automatically adds start, parity, and stop bits.

Each channel's data length can be configured for 7 or 8 bits. Parity is jumper selectable, odd or even, and parity checking and generation can be inhibited. Stop bits are jumper selectable; one or two.

The 304 can be used in a wide range of interface applications including printers, terminals, peripherals and remote data acquisition systems. Each channel can operate at one of nine jumper selectable data rates, from 150 to 38.4K baud, which are generated by an on-board clock. The user may also provide an external clock.

The line characteristics of each channel can be jumper configured to operate in accordance with EIA standard RS-232,

RS-422, or RS-423. Twenty milliamp current loop operation is possible when used in conjunction with the DEC DLV11-KA.

A unique feature of the 304 is the capability to support the LSI 11/23 four level interrupt structure. Channel 3 may also be configured as the system console, independent of the other three channels. Special pins are provided on each I/O connector which can be used to constantly assert the data terminal ready lines of the peripheral, and each channel can also be configured to provide a pulse output to control a paper tape reader.

SPECIFICATIONS

Bus Interface	Q-bus, DEC LSI-11, 11/2 & 11/23 compatible
Data Characteristics	
(Each Channel)	
No. of Channels	4
Data Protocol	Asynchronous serial
Baud Rates	Jumper Selectable 150, 300, 600, 1.2K, 2.4K, 4.8K, 9.6K, 19.2K 38.4K, Ext.
Line Discipline	Jumper Selectable EIA RS-232C, RS-422, or RS-423
Data Bits	Jumper Selectable 7 or 8
Stop Bits	Jumper Selectable 1 or 2
Parity	Jumper Selectable Odd, Even, None
Addressing	
Base Address Range	Jumper Selectable 776000_8 to 777740_8
Console Address	Jumper Selectable 777560_8 Channel 3 Only
Interrupts	
Priority Level	Jumper Selectable LSI-11 & 11/2 Level 4, Jumper Selectable LSI-11/12 Level 4, 5, 6, or 7
Base Vector Range	Jumper Selectable 0 to 740_8
Console Vector	60 only when console option is enabled

Mechanical & Environmental

Dimensions	DEC LSI-11 standard 8.9" x 5.2" half quad board
Power Requirements	5V @ 1 Amp, 12V @ .2 Amps
Bus Loading	1.5 Std. AC/1 Std. DC Load
Operating Temperature Range	0 to 55°C
Storage Temperature Range	0 to 75°C
Relative Humidity	To 85% non-condensing
Mating Connector	Amp #87133-5, Pin #87165-2

Q-BUS INTERFACE

The Q-Bus Interface consists of address/data transceivers, an address comparator, console decode logic and I/O select and control logic.

During the addressing portion of a bus cycle, the Address/Data transceivers are in the receive mode. Address lines 12 through 5, gated by bus line BBS7, are compared to the base address setting selected by the address selection jumpers. When the correct address is asserted by the processor, the comparator output (BDSEL) is asserted. This in conjunction with the assertion of BSYNC is used by the Select and Control Logic (SCL) to select the appropriate on-board register for the remainder of the bus cycle.

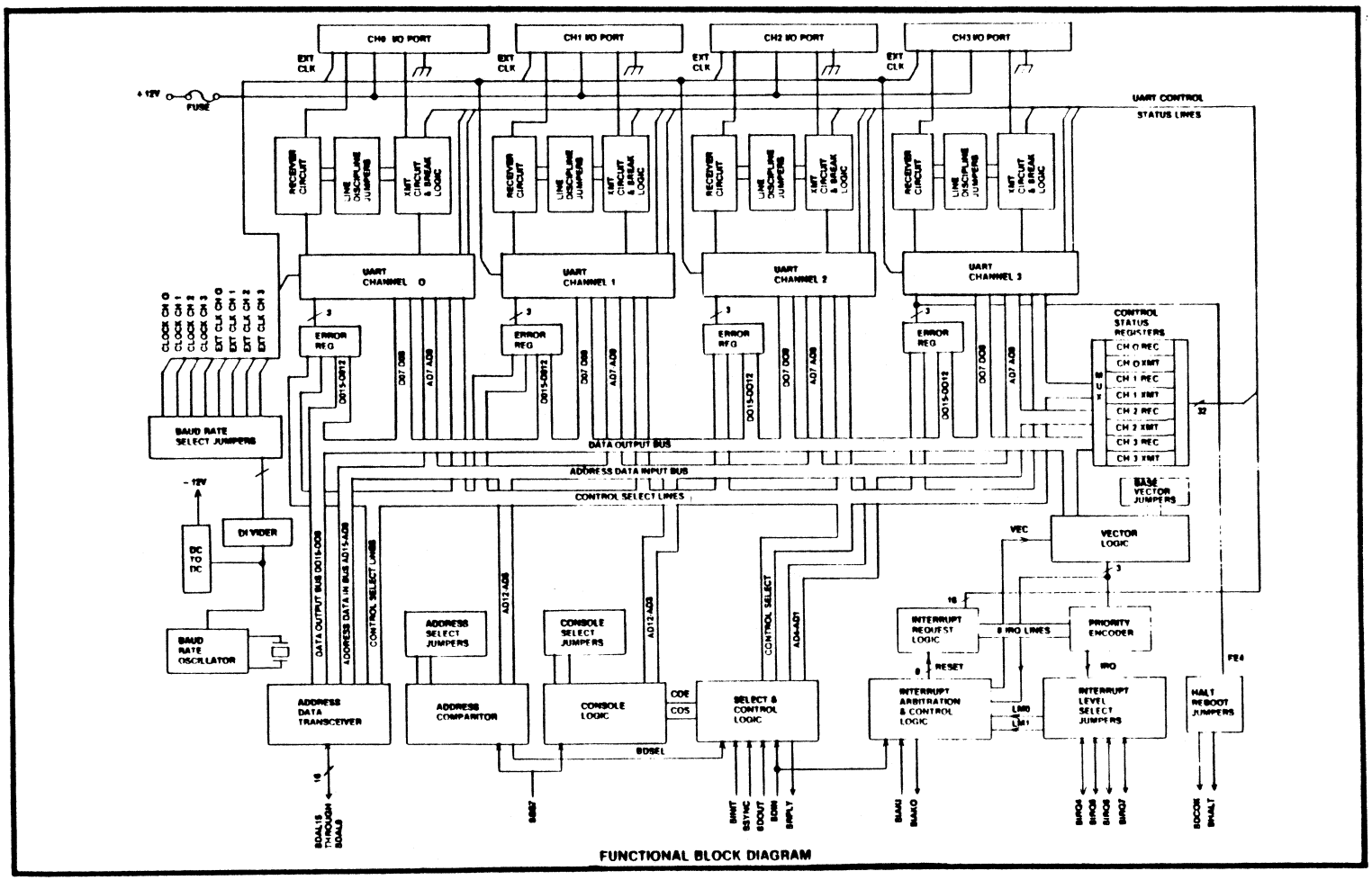
If the processor is performing a read, then the BDIN line is decoded in conjunction with the SCL to enable the tri-state buffers of the selected register, place the bus transceivers in their transmit mode, and then assert the BRPLY line.

If the processor is performing a write operation, then the register which is to be written to is selected during the Address/Data portion of the bus cycle and the BDOUT line is used to clock the latches of the receiving register, and to assert BRPLY.

INTERRUPT LOGIC

The interrupt handling logic consists of interrupt request logic, a priority encoder, level circuit logic, arbitration control, and vector logic.

The interrupt request logic consists of eight latches; one for each transmit or receive CSR. In order to generate an interrupt, two requirements must be met. First, the interrupt



FUNCTIONAL BLOCK DIAGRAM

MODEL 304

Functional Block Diagram

enable bit (Bit 6) in either the transmit or receive CSR must be set, and second, the appropriate condition flag must be set (Bit 7). These two logically anded signals clock the flop. The outputs of all eight flops are fed into the priority encoder. When the output of any flop goes high, the priority encoder generates a master interrupt request (IRQ). This signal is fed into the level select logic which in turn asserts the appropriate BIRQ lines. At the same time the arbitration logic monitors the bus to determine if a device on a higher interrupt level is requesting. If not, then when the interrupt grant signal BIAKI is received, the appropriate vector as determined by the priority encoder is placed on the bus, and if more than one channel is requesting, the channel of highest priority is cleared leaving the lower priority requests pending. Table 1 gives the priority level of each channel.

Channel	Level		Vector Offset
Channel 0 Receive	0	Highest Priority	Base Vector +Ø
Channel 1 Receive	1		Base Vector +10
Channel 2 Receive	2		Base Vector +20
Channel 3 Receive	3		Base Vector +30
Channel 0 Transmit	4		Base Vector +4
Channel 1 Transmit	5		Base Vector +14
Channel 2 Transmit	6		Base Vector +24
Channel 3 Transmit	7	Lowest Priority	Base Vector +34

TABLE 1

CONSOLE CHANNEL

When the console enable jumper is installed, Channel 3 will respond to the address of 177560_8, and the receiver will always have a vector address of 60_8. The transmitter vector will be 64_8. The console mode of operation is independent of the board's base address.

UART

Each channel consists of a Universal Asynchronous Receiver Transmitter (UART) which receives and converts serial data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. If a transmission error is detected, the nature of the error is outputed to an error

register which is read when the receive data register is read. Upon receiving the last stop bit, the receiver full flag is set (Bit 7 of the receive CSR). If the receiver interrupt enable bit is set (Bit 6), then the receiver full flag will generate an interrupt request.

The UART's transmitter converts the computer's parallel data into a serial format and automatically adds start, parity, and stop bits. When the transmitter buffer is ready to receive a byte of data for transmission, the transmitter ready flag is set (Bit 7 of the transmitter CSR). If the transmitter interrupt enable bit is set (Bit 6), then the transmitter ready flag will generate an interrupt.

CONTROL STATUS REGISTER (CSR)

Each channel contains a 16 bit receiver CSR and a 16 bit transmitter CSR. Bit 7 is a read only bit used as a status flag and Bit 6 is a read/write bit used to enable an interrupt request when Bit 7 gets set.

Bit 7 of the receiver CSR is used to indicate that the receiver contains new data. Bit 7 is cleared by reading the receiver's data register or by a software reset. When Bit 6 is set, an interrupt request is generated when Bit 7 is set.

Bit Ø of the receiver CSR is used to transmit a reader run pulse. This bit is a write only bit and always reads zero.

Bit 7 of the transmitter CSR, when set, indicates the transmitter buffer is empty and ready to transmit new data. Setting Bit 6 will generate an interrupt whenever Bit 7 is set.

Bit Ø, when set, will transmit a continuous break.

All unused CSR bits in both the transmitter and receiver CSR's will always read zero.

DATA REGISTERS

Each channel contains a Receiver Data Register (RDR) and a Transmitter Data Register (TDR). When data is received, it is placed in the RDR and Bit 7 of the Receiver CSR is set. The received data is obtained by reading this register and, thus, automatically clearing Bit 7.

Data to be transmitted is written to the TDR. This automatically clears Bit 7 of the Transmitter CSR. Here the data will remain until the transmitter is ready. The data is then placed into the transmitter setting Bit 7.

ERROR REGISTERS

Each channel contains a 4 bit error register which is comprised of Bits 15 through 12 of the RDR.

Bit 12 is the Parity Error (PE) Bit. A "1" indicates the receiver parity does not match the parity selected by the format jumpers. The PE bit remains set until parity matches on a succeeding character. When parity is inhibited, this bit always reads zero.

Bit 13 is the Framing Error (FE) Bit. A "1" indicates the first stop bit was invalid. The FE bit will stay set until the next valid character's stop bit is received.

Bit 14 is the Overrun Error (OE) Bit. A "1" indicates that the last character was not read from the RDR before a new character was received. The OE is reset at the next character's stop if Bit 7 of the Receive CSR cleared.

Bit 15 is the Error Flag (EF) and is the logical "oring" of the PE, FE, and OE bits. The setting of any error bit will set this bit.

EIA CIRCUIT

The EIA circuit for each channel consists of a differential line driver, line receiver, and a single ended line driver. Through the use of wire wrap jumpers, each channel can be configured to operate as RS-232C, RS-422, or RS-423.

Channels operating as RS-232C or RS-423 will configure the differential line receiver to operate single ended and utilize the single ended line driver. The slew rates of the line drivers are controlled by changing external resistors.

Channels which operate as RS-422 configure the differential line receiver for differential operation by adding a 100 ohm termination resistor, and utilize the differential line driver.

BAUD RATE GENERATOR

The baud rate generator consists of a crystal oscillator and divider. The oscillator base frequency is 4.1952 MHz which is divided to yield the nine baud rate clocks. Each channel can operate at any one baud rate independent of the other channels.

MODES OF OPERATION

Each channel of the 304 can operate in various line disciplines, data formats, and baud rates. The base address can be set so that the board can reside in any I/O page location. The vector can also be set to any address from 0_8 to 774_8, and the interrupt level can be set to 4, 5, 6, or 7. All of these operation modes are configured by setting wire wrap jumpers. Table 2 is a summary of the jumper selectable modes which the board can be configured to.

TABLE 2

Jumper Selectable Modes of Operation

Mode Description	Mode Selection
* Line Discipline	RS-232C, RS-422, or RS-423
* Baud Rate	150, 300, 600, 1200, 2400, 4800, 9600, 19.2K, 38.4K, External
* Serial Data Format	Data Bits, 7 or 8 Stop Bits, 1 or 2 Parity, Odd, Even, None
Base Address	160000_8 to 177740_8
Vector Base Address	Ø to 740_8
Console	Enable Channel 4 as System Console Address CH 4 = 177560_8 Vector CH4 = 60_8
Halt/Reboot on Break	Channel 3
Interrupt Level	4, 5, 6, or 7

* Channel to Channel Configurable

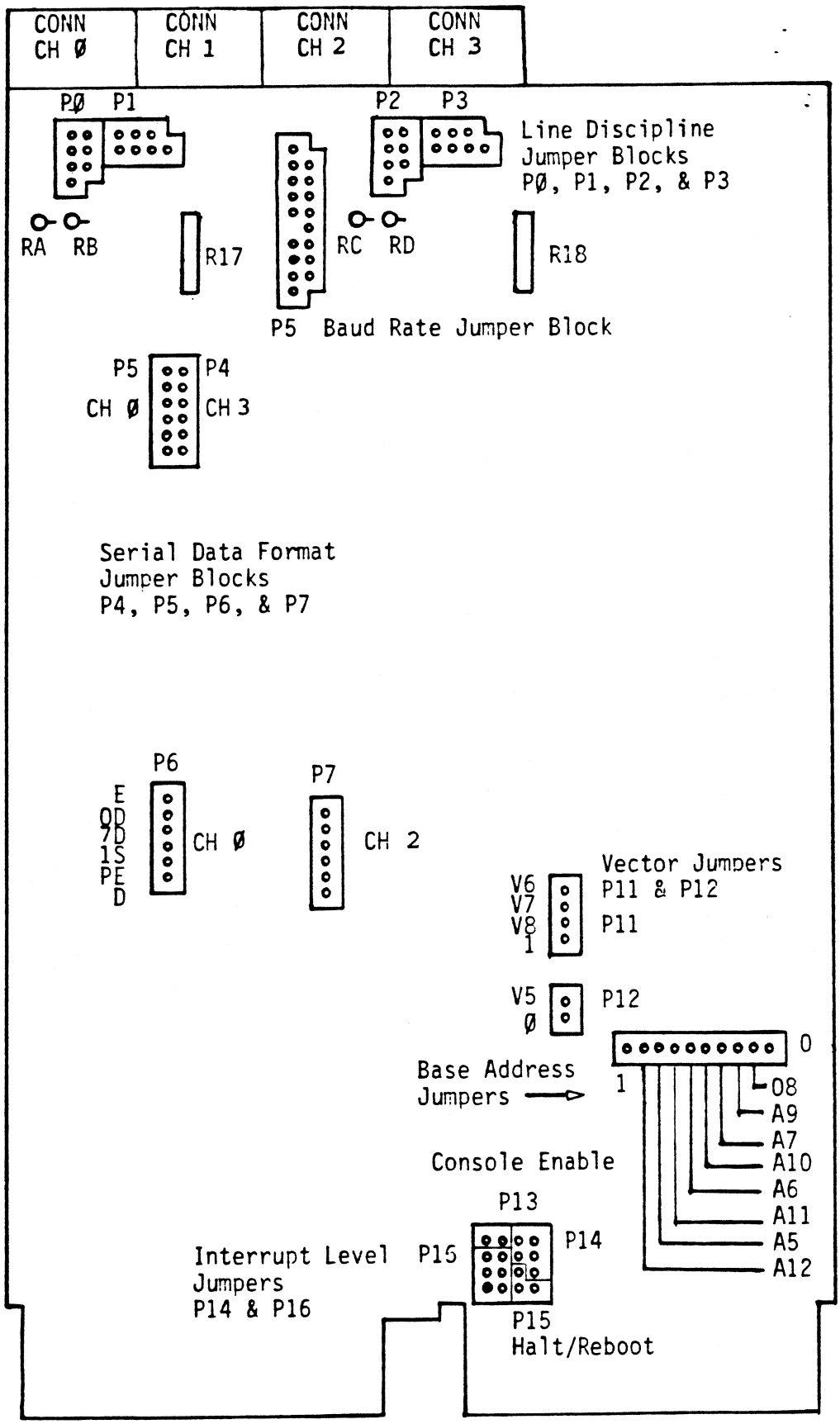


FIGURE 1

Model 304 Jumper Layout

FACTORY CONFIGURATION

The Model 304 is shipped configured as follows:

TABLE 3

Base Address	176500_8
Vector Base Address	300_8
CH3 Console Enabled	Yes
CH3 Halt on Break	Enabled
* Serial Data Format	1 Stop Bit, 8 Data Bits, No Parity
* Line Discipline	RS-232C
* Baud Rate	9600
Interrupt Level	4 (LSI 11)

* All Channels

SETTING THE BASE ADDRESS

The 304's base address can be set to reside anywhere within the I/O page. The location of the base address jumpers is found on Figure 1. To change the board's base address requires reconfiguring the base address jumpers. Figure 2 indicates the base address jumper post arrangement. To change an address bit from 0 to 1 or vice versa requires wire wrapping that bit to the post labeled 0 or 1.

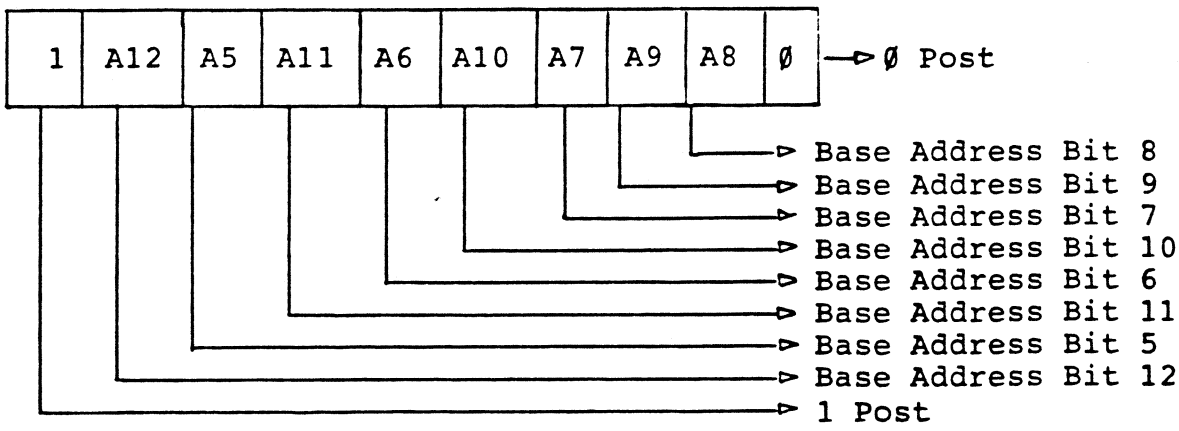


FIGURE 2

Base Address Jumpers

As an example, the factory configured base address is 176500_8. To set the base address requires wire wrapping A12, A11, A10, A8, and A6 to 1 and A9, A7, and A5 to 0. Refer to Table 4.

TABLE 4

Factory Configured Base Address

Base Address	Bit Number	Jumper Post Description	Jumper Destination
1	Bit 15	N/A	
	Bit 14	N/A	
7	Bit 13	N/A	
	Bit 12	A12	1
	Bit 11	A11	1
6	Bit 10	A10	1
	Bit 9	A9	Ø
	Bit 8	A8	1
5	Bit 7	A7	Ø
	Bit 6	A6	1
	Bit 5	A5	Ø
Ø	Bit 4	N/A	
	Bit 3	N/A	
	Bit 2	N/A	
Ø	Bit 1	N/A	
	Bit Ø	N/A	

SETTING THE VECTOR ADDRESS

The 304's vector address can be set from 0 to 740_8. The location of the vector selection jumpers are found by referring to Figure 1. Wire wrapping jumper posts V6, V7 or V8 to Post 1 will cause these vector bits to read as 1. No connection will cause these bits to read 0.

Connecting jumper post V5 to 0 will cause vector Bit 5 to read 0. No connection of V5 will cause vector Bit 5 to read as 1.

As an example, the factory configured vector is 300_8. This requires leaving Post V8 open, connecting V6 and V7 to Post 1 and connecting V5 to Post 0.

Table 5 is a vector configuration guide. Vector Posts V6, V7, or V8 should never be connected to Post 0 and Vector

Post V5 should never be connected to Post 1. THIS WILL RESULT IN AN ERRONEOUS VECTOR.

TABLE 5

Vector Selection Jumpers

Vector Base Address Octal	Vector Post P11 V8	V7	V6	Vector Post P12 V5
0	*	*	*	Ø
40	*	*	*	*
100	*	*	1	Ø
140	*	*	1	*
200	*	1	*	Ø
240	*	1	*	*
300	*	1	1	Ø
340	*	1	1	*
400	1	*	*	Ø
440	1	*	*	*
500	1	*	1	Ø
540	1	*	1	*
600	1	1	*	Ø
640	1	1	*	*
700	1	1	1	Ø
740	1	1	1	*

1 = Connect to Post 1 of P11
Ø = Connect to Post Ø of P12
* = Leave Post Open (No connection)

SETTING THE INTERRUPT LEVEL

The 304 can fully support the 11/23 multi-level interrupt structure. To do so requires that the 304 assert the appropriate interrupt request lines (BIRQ4, BIRQ5, BIRQ6 and BIRQ7) and monitor interrupt request lines of higher priority. Jumper post block P14 (Fig. 1) is used to select which interrupt request lines are to be asserted, and jumper post block P16 (Fig. 1) is used to select which interrupt request lines are monitored.

The 304 is factory configured to support systems which do not support a multi-level interrupt structure, which means that its priority level is strictly a function of its electrical locations relative to the processor. To change the configurations, refer to Table 6 and Figure 3 for proper jumper installation.

TABLE 6

Interrupt Level Configuration Jumpers

Interrupt Level	Level Request Jumpers P14			Level Monitor Jumpers P16	
	R5	R6	R7	LM1	LMØ
11/2 *	G	G	G	P	P
4	G	G	G	Q5	Q6
5	IR	G	G	P	Q6
6	G	IR	G	P	Q7
7	G	IR	IR	P	P

* This configuration is set at the factory and must be used in systems which do not support the multi-level interrupt.

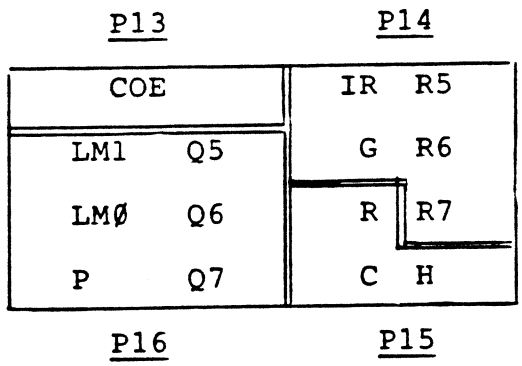


FIGURE 3

Interrupt Level, Console & Halt Reboot Jumpers

ENABLING THE CONSOLE

Channel 3 can be enabled as the system console independent of the base and vector address settings. To enable this option requires installing jumper P13. To disable this option requires removing jumper P13. Refer to Figure 1.

When the console is enabled, Channel 3 will respond to addresses 177560_8 to 177566 and will output a vector of 60 and 64 for the receiver and transmitter interrupts, respectively. Caution should be employed when the console is enabled so as not to set the base address equal to 177540 or a conflict will exist between Channel 2 and Channel 3.

By disabling the console, (remove jumper P13) and setting the board's base address equal to 177540 and setting the vector equal to 40_8, Channel 2 will act and respond as the system console.

SYSTEM HALT OR REBOOT

Any device communicating through Channel 3 can generate a system Halt or power up initialization by outputting a "BREAK".

To generate a system Halt on BREAK requires installing a jumper at P15 (Figure 3) from C to H. To generate a power fail reset, connect C to R. Refer to Figure 1 for jumper block P15's location.

SETTING THE BAUD RATE

Each channel of the 304 can communicate at one of nine jumper selectable baud rates or at an externally provided clock rate. Table 7 lists the baud rates and the jumper post identification letter. Figure 4 details the baud rate jumper block, the location of which can be found by referring to Figure 1.

Setting a channel to operate at a particular baud rate requires jumpering the appropriate pin whose letter represent the desired baud rate to the pin labeled for that channel (Refer to Figure 4).

As an example, the 304 is shipped from the factory with all 4 channels set to operate at 9600 baud. The baud rate jumper post C is connected to jumper posts CHØ, CH1, CH2, and CH3.

TABLE 7

Baud Rate Jumper Identification

Baud Rate	Letter
150	I
300	H
600	G
1200	F
2400	E
4800	D
9600	C
19.2K	B
38.4K	A

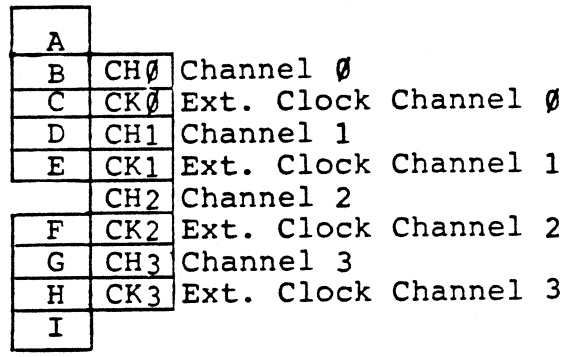


FIGURE 4

Baud Rate Jumper Block Detail P5

SETTING THE SERIAL DATA FORMAT

Each channel of the 304 can be configured to operate in the following data formats:

7 or 8 Data Bits
1 or 2 Stop Bits
Odd, Even, or with No Parity

Jumper posts P6, P5, P7, and P4 (Figure 1) are used to set the data formats of Channels Ø through 3 respectively. The jumper configuration of the various options are illustrated in Table 8. As an example, the 304 is configured for 8 data bits, 1 stop bit, and no parity. This requires jumpering PE and 7D to E and jumpering 1S to E. When parity is not enabled, the odd/even parity post has no effect but must be jumpered to either E or D. Figure 5 illustrates the format jumper arrangement.

TABLE 8

Format Jumper Configuration Guide

Format Option	Jumper Configuration
8 Data Bits	7D to D
7 Data Bits	7D to E
2 Stop Bits	1S to D
1 Stop Bit	1S to E
No Parity	PE to D
Parity	PD to E
Even Parity	OD to D
Odd Parity	OD to E

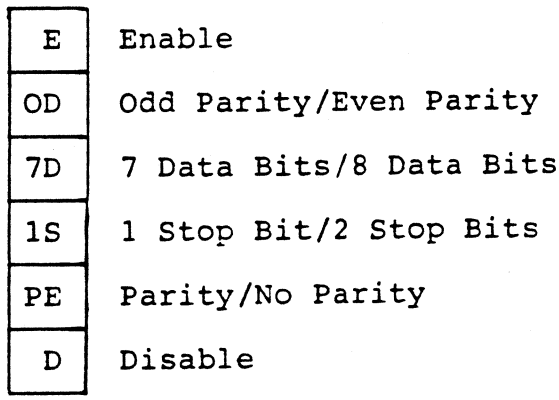


FIGURE 5

Serial Data Format Jumper Block Detail

(P4, P5, P6, & P7)

SETTING THE LINE DISCIPLINE

Each channel of the 304 can operate in any one of the following EIA line disciplines:

RS-232C
RS-422
RS-423

The jumper blocks used to configure Channels Ø through 3 are P0, P1, P2, and P3 (Figure 1), respectively. Table 9 illustrates the jumper configuration to set up each channel. As an example, the 304 is shipped from the factory with each channel set up to operate in RS-232C. This requires jumpering S+ to I+ and S- to I-. Figure 6 illustrates the layout of the line discipline jumper blocks.

TABLE 9

Line Discipline Jumper Configuration

	Line Discipline	Jumper Configuration
	RS-232C	I+ to S+, I- to S-
*	RS-422	I+ to D+, I- to D-
	RS-423	I+ to S+, I- to S-

* Add 100 ohm termination resistor, (RA, RB, RC, RD)

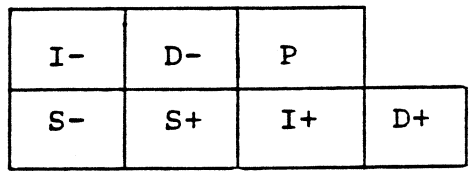


FIGURE 6

Line Discipline Jumper Block Layout

(P0, P1, P2, & P3)

When a channel is set up to operate in RS-422, a 100 ohm termination resistor must be installed at the input of the differential receiver. Table 10 lists the channel number and resistor name.

TABLE 10

RS-422 Resistor Installation Guide

Channel Ø	Install a 100 ohm resistor at RA
Channel 1	Install a 100 ohm resistor at RB
Channel 2	Install a 100 ohm resistor at RC
Channel 3	Install a 100 ohm resistor at RD

During data communication over long data leads it may be necessary to change the rise and fall times of the single ended line drivers used in RS-423 to reduce line reflections and the potential of data errors. R17 controls the transition time for Channels Ø and 1 and R18 controls Channels 2 and 3. The resistor installed at the factory is a 22K which sets the transition time at 2.2µs. Table 11 is a list of recommended resistor values as a function of baud rate which should be installed if line reflections become a problem.

TABLE 11

RS-423 Slew Rate Resistor Values

Baud Rate	Resistor Value in Ohms	Nominal Transition Times
150	1 Megohm	100 µsec
300	1 Megohm	100 µsec
600	1 Megohm	100 µsec
1200	820K Ohm	82 µsec
2400	430K Ohm	43 µsec
4800	200K Ohm	20 µsec
9600	100K Ohm	10 µsec
19.2K	51K Ohm	5.1 µsec
38.4K	22K Ohm	2.2 µsec

READER RUN PULSE

The reader run pulse is used to control a paper tape reader. To use this control requires connecting P- to I- at the appropriate line discipline jumper block (Figure 1). Figure 6 illustrates the location of this jumper with the line discipline jumper block.

SERIAL INTERFACE

Figure 1 illustrates the connector location for each channel.

CONNECTOR DESCRIPTION

Each channel is interfaced through a 10 pin header. Figure 7 illustrates the pin-out location. The mating connector is manufactured by AMP, Inc. Table 12 lists the parts which are required to assemble the mating connector. The connector may be obtained through AMP, AMP distributors, or GTSC.

TABLE 12

Model 304 Connector Assembly Parts List

AMP P/N	Description	Quantity/Connector
87133-5	Connector Shell	1
87179-1	Key Pin	1
87165-2	Pins	9

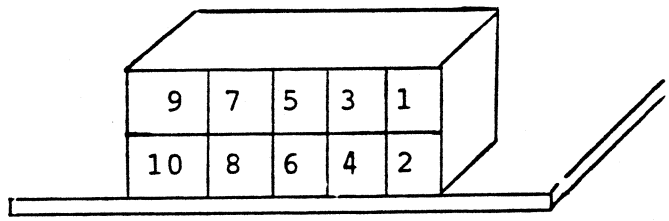


FIGURE 7

Model 304 Header Pin-out

The pin-out description of each header is as follows:

Pin No.	Description
1	Clock I/O
2	Signal Ground
3	Transmit Data +
4	Transmit Data -
5	Signal Ground
6	Key (No Pin)
7	Receive Data -
8	Receive Data +
9	Signal Ground
10	+12 Volts (Fused)

When a channel is configured for RS-232C or RS-423, Pin 7 must be externally tied to signal ground. This is typically done by connecting Pin 7 to Pin 9. Pin 1 is the external clock input.

LINE DISCIPLINE, CABLE LENGTH & DATA RATES

The two basic methods for electronic communications are single ended transmission and differential transmission. RS-232 was developed for single ended transmission over short distances at slow data rates. RS-423 extends the maximum data rate and cable length beyond that of RS-232. It also provides for wave shaping dependent on data rate and wire length to control reflections.

For communications over long distances, differential transmissions (RS-422) should be used to nullify effects of ground shifts and noise signals which appear as common mode. Table 13 lists the maximum recommended cable length and data rates for each line discipline.

TABLE 13

Key Aspects of RS-232,

RS-423 & RS-422

Specification	RS-232C	RS-423	RS-422
Mode of Operation	Single-ended	Single-ended	Differential
No. of Drivers & Receivers allowed on one line	1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers
Maximum Cable Length	50 feet	4000 feet	4000 feet
Maximum Data Rate	20 kb/s	100 kb/s	10 mb/s

PROGRAMMING

Figure 8 illustrates the functions of the four 16 bit registers which comprise each channel. Thus, the Model 304 occupies 16 contiguous blocks in the I/O page *. The registers which make up each channel are:

Receiver Control Status Register (RCSR)

Receiver Data Register (RDR)

Transmitter Control Status Register (TCSR)

Transmitter Data Register (TDR)

Table 14 illustrates the relationship between each channel's registers and the base address. When the console is enabled, any attempt to address Channel 3 through an address other than the console address will cause a bus time out error.

Testing Bit 7 of the RCSR is used to indicate that the UART has received new data. Reading the RDR will clear Bit 7. Setting Bit 6 of the RCSR will enable the receiver interrupts. When Bit 7 is set, an interrupt will be generated.

Bit Ø of the RCSR is used to generate the reader run pulse by setting this write only bit. This action will also clear Bit 7 of the RCSR.

Bits Ø through 7 of the RDR contain the data received by the UART. Bits 12 through 15 indicate any errors which have occurred during the reception of data.

Bit 7 of the TCSR indicates the status of the transmitter. When this bit is set, the transmitter is ready to receive a new byte of data for transmission. When this bit is cleared (Bit 7 = Ø), the transmitter is busy and no attempt to write the data to the TDR should be made. Setting Bit 6 of the TCSR will allow interrupts to be generated when Bit 7 is set.

Bit Ø of the TCSR is a read/write bit used to transmit a continuous break. A "1" written to Bit Ø will transmit a break (continuous Ø), a zero clears the break transmission.

* This only holds true if Channel 3 is not configured as the console.

Data which is to be transmitted is written to the TDR, but only if Bit 7 of the TCSR is set.

Table 15 lists the relationship between the vector jumper settings and each channel. Note, Channel 3's vector is that of the console when the console is enabled.

Table 16 illustrates the register and vector address when Channel 3 is configured as the system console.

TABLE 14

Register Address Offset

Register Description	Base Address Offset (Octal)
Channel Ø Receiver CSR	Base Address +0
Channel Ø Receiver Data Register	Base Address +2
Channel Ø Transmitter CSR	Base Address +4
Channel Ø Transmitter Data Register	Base Address +6
Channel 1 Receiver CSR	Base Address +10
Channel 1 Receiver Data Register	Base Address +12
Channel 1 Transmitter CSR	Base Address +14
Channel 1 Transmitter Data Register	Base Address +16
Channel 2 Receiver CSR	Base Address +20
Channel 2 Receiver Data Register	Base Address +22
Channel 2 Transmitter CSR	Base Address +24
Channel 2 Transmitter Data Register	Base Address +26
Channel 3 Receiver CSR	Base Address +30
Channel 3 Receiver Data Register	Base Address +32
Channel 3 Transmitter CSR	Base Address +34
Channel 3 Transmitter Data Register	Base Address +36

TABLE 15

Vector Address Offset

Interrupt Request Description	Vector Base Address Offset
Channel Ø Receive	Ø
Channel Ø Transmit	4
Channel 1 Receive	10
Channel 1 Transmit	14
Channel 2 Receive	20
Channel 2 Transmit	24
Channel 3 Receive	30
Channel 3 Transmit	34

TABLE 16

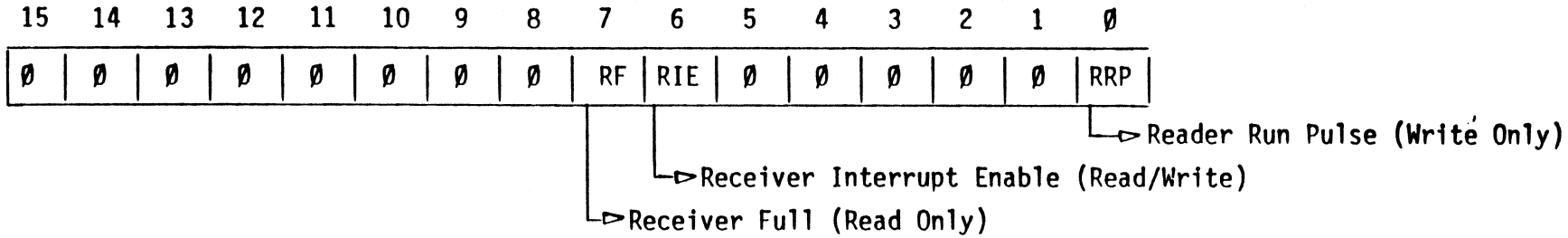
Console Register & Vector Addresses

When Console Option is Enabled

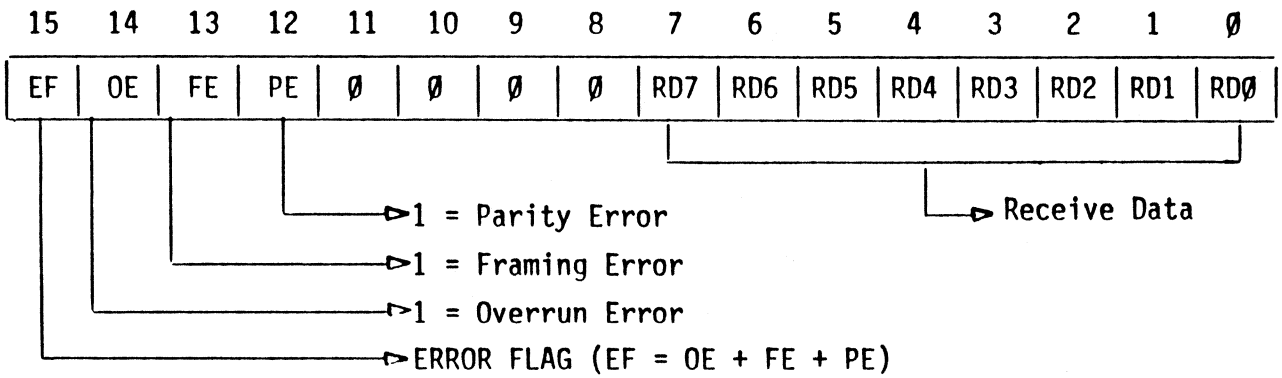
Channel 3 Register Description	Register Address
Receiver CSR	177560_8
Receiver Data Register	177562_8
Transmitter CSR	177564_8
Transmitter Data Register	177566_8
Receiver Interrupt Vector Address	60_8
Transmitter Interrupt Vector Address	64_8

FIG 8

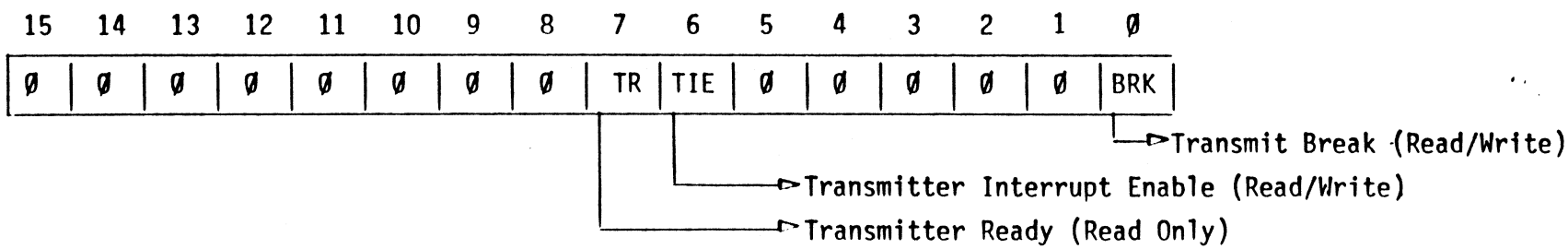
RECEIVER CSR



RECEIVER DATA REGISTER



TRANSMITTER CSR



TRANSMIT DATA REGISTER

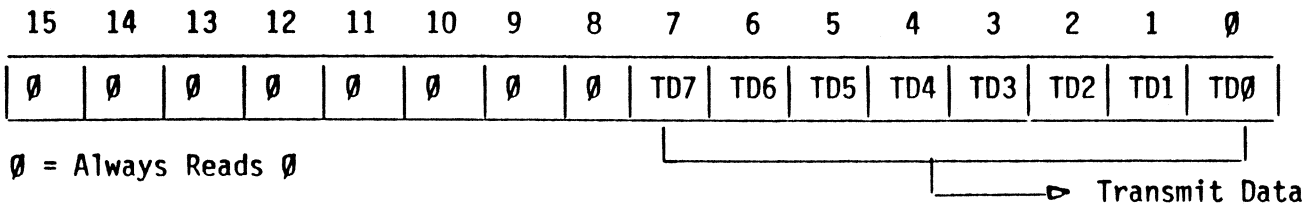


FIGURE 8 (Cont.)

Model 304 Serial I/O Port Register Formats

WARRANTY

GTSC warrants that its products, except software, will be free from defects in workmanship or material under normal use and service. GTSC under this warranty will, at its option, replace or repair without charge at its plant any products manufactured by GTSC.

Freight, insurance, and other charges incurred in returning the product to GTSC will be paid by the customer.

The terms of this warranty are 90 days from the original date of shipment. The warranty provisions do not extend to products which have been repaired or altered without prior written GTSC approval, or to products which became defective due to accident or to the customer's improper installation, application or maintenance.

This warranty is in lieu of any other warranty, that is expressed or implied, including warranties of merchantability and fitness for use. GTSC reserves the right to make any changes in the design or construction of its products at any time without incurring any obligation to make any changes to products previously delivered.

GTSC neither assumes nor authorizes any other person to assume for it any other liability in connection with the sales, installation or use of its products.

GTSC shall have no liability for incidental or consequential damages of any kind arising out of the sale, installation, or use of its products.

To exercise this warranty, call GTSC, Customer Service Department for a return authorization in the event that a product is to be returned for "In Warranty Repair".