RAYTHEON COMPUTER

AID DATA SHEET

MODEL

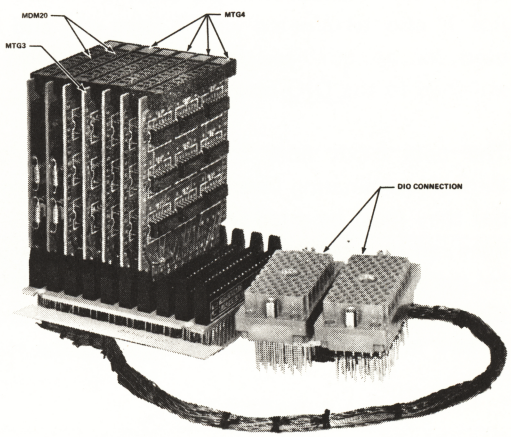
77001

DIRECT INPUT/OUTPUT INTERFACE

GENERAL

The Direct Input/Output Interface, Model 77001, attaches peripheral devices to the DIO Bus of the Central Processor. The Model 77001 provides all the timing and strobe signals necessary for direct transfer of data with the CPU accumulator register using DIN and DOT instructions. Device and Function fields of the instructions are decoded and furnished for selection and gating controls of attached devices. It also serves as a terminal for the External Sense Line and inputs to the Priority Interrupt System.

Figure 1 shows the relation between the DIO signals and those available as inputs and outputs to the 77001. Figure 2 shows the timing for the Raytheon 700 Series Direct Input/Output Bus. These define what is required to interface to the DIO bus and what is provided by the 77001. Figures 3 and 4 show typical first and second level system configurations using the 77001.



SPECIFICATIONS

DIGITAL INPUTS *

Function	No. of Lines	Unit DTL Load
Data Input Bus	16	1
Data Input Strobe-	1	1
Interrupt 1	1	1
Interrupt 2	1	1
Interrupt 3	1	1
Sense Line	1	1

MECHANICAL

Size	Approx. 4.125 x 4.5 x 3.75 inches = 10 card positions = 1 unit space
M Series Cards	MTG4 (4), MTG3 (1), MDM20 (2)
Spare connectors	1

* These signals refer to the peripheral device interface.

DIGITAL OUTPUTS *

Function	No. of Lines	Unit DTL Load
Data Output Bus	16	25
Function Bus	8	25
T0	1	25
T0-	1	25
T2	1	25
T2-	1	25
T4	1	25
T4-	1	25
Computer Clock	1	25
Computer Clock-	1	25
Computer Output Strobe	1	25
Computer Input Strobe	1	25
Computer Reset	1	25
Computer Reset-	1	25

AVERAGE POWER REQUIREMENTS

+5V	800 Milliamperes (±4% total regulation and accuracy) = 8 power units

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INPUTS

All inputs to the 77001 are properly terminated onto the DIO bus. The interface can handle three interrupt inputs which are connected by means of Berg clips to computer interrupt numbers one, two and three. These interrupt connections can be changed to any of the other available interrupts on the system. This allows the user to conveniently assign service priority levels for his particular application. An unused interrupt must either have its Berg clip removed from the connector or have its input grounded. Similarly, the same precautions must be taken with the sense line input. The sense line is also terminated with a Berg clip and it can be used for an auxiliary interrupt Input when properly attached to the DIO connector.

The data input lines to the 77001 are also routed through terminating inverters onto the DIO connectors, but they must be gated with a common strobe. The DIN lines can be gated so that a ground going level will transfer the data onto the bus. If a positive level is needed as the gating signal, the output of one of the available inverters in the 77001 can be wired to the strobe line.

OUTPUTS

Basically the 77001 is a first level interface to a Raytheon 700 Series computer. All basic timing and strobe signals from the computer via the DIO bus are routed through power inverters in the 77001 for gating and control in the general AID system. All AID functional blocks have sufficient input logic to use the basic control and timing pulses to perform their assigned tasks without additional logic.

The outputs from the computer accumulator are similarly routed through power inverters in the 77001 and are available for distribution to other AID blocks. All AID functional blocks designed to accept parallel digital data can operate from these outputs which are typically addresses, word counts, timing intervals, or output data values.

The eight address lines on the DIO bus that correspond to the device and function fields of the DOT and DIN instructions are decoded into two corresponding sets of sixteen lines. Decoding the address lines in this manner enables the selection of up to fifteen AID devices, each of which can perform sixteen functions. The devices must be selected so as not to conflict with other devices on the computer system. The two sets of sixteen lines are all available in the interface as bar terms with eight of the function terms routed through power inverters for general distribution. Several spare power inverters within the interface allow the user to conveniently select a device for his specific application. The spares increase the user's flexibility in the selection of devices and functions for a wide range of applications.

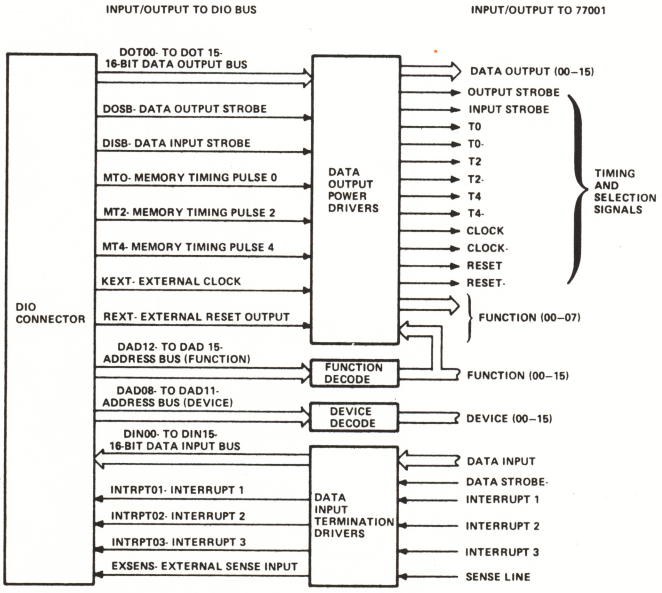


Figure 1. Block Diagram, Model 77001

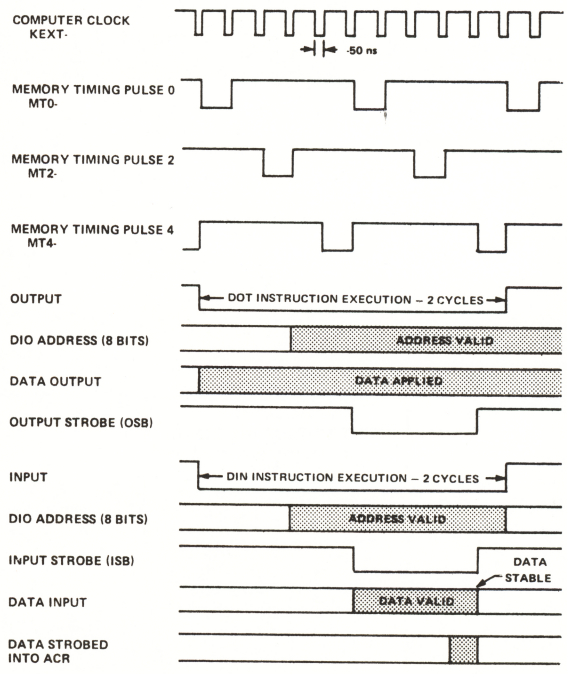


Figure 2-A. DIO Interface Timing Diagram, 703 CPU

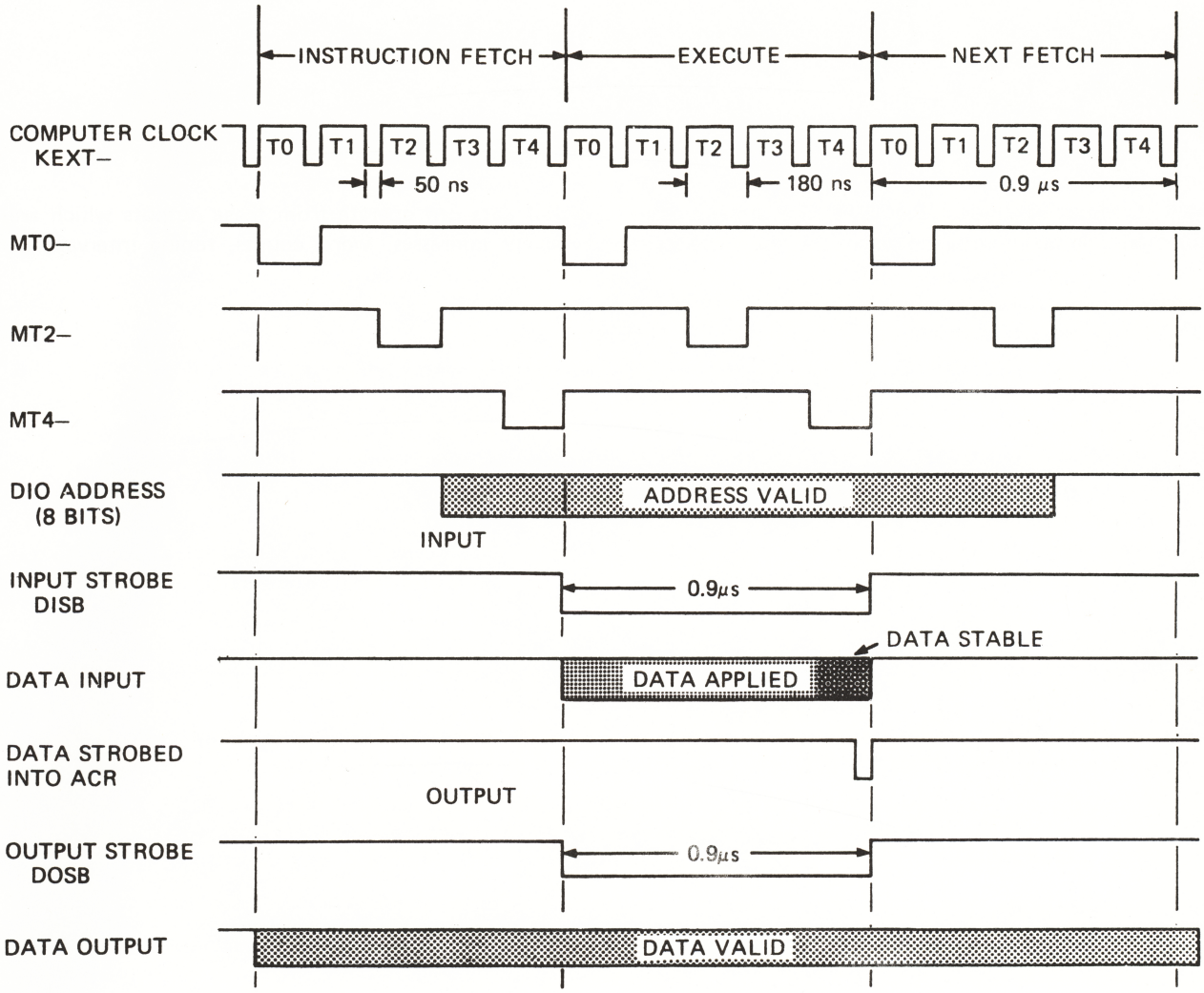
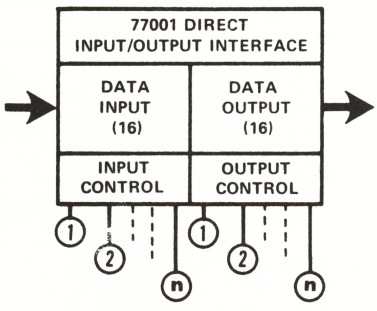


Figure 2-B. DIO Interface Timing Diagram, 706 CPU



	ITEM	MIGHT BE DEFINED AS
INPUT	1	DIN STROBE
	2	SENSE LINE
	•	•
	n	INTERRUPT 1
OUTPUT	1	DEVICE
	2	FUNCTION
	•	•
	n	RESET

Figure 3. Functional Configuration Diagram

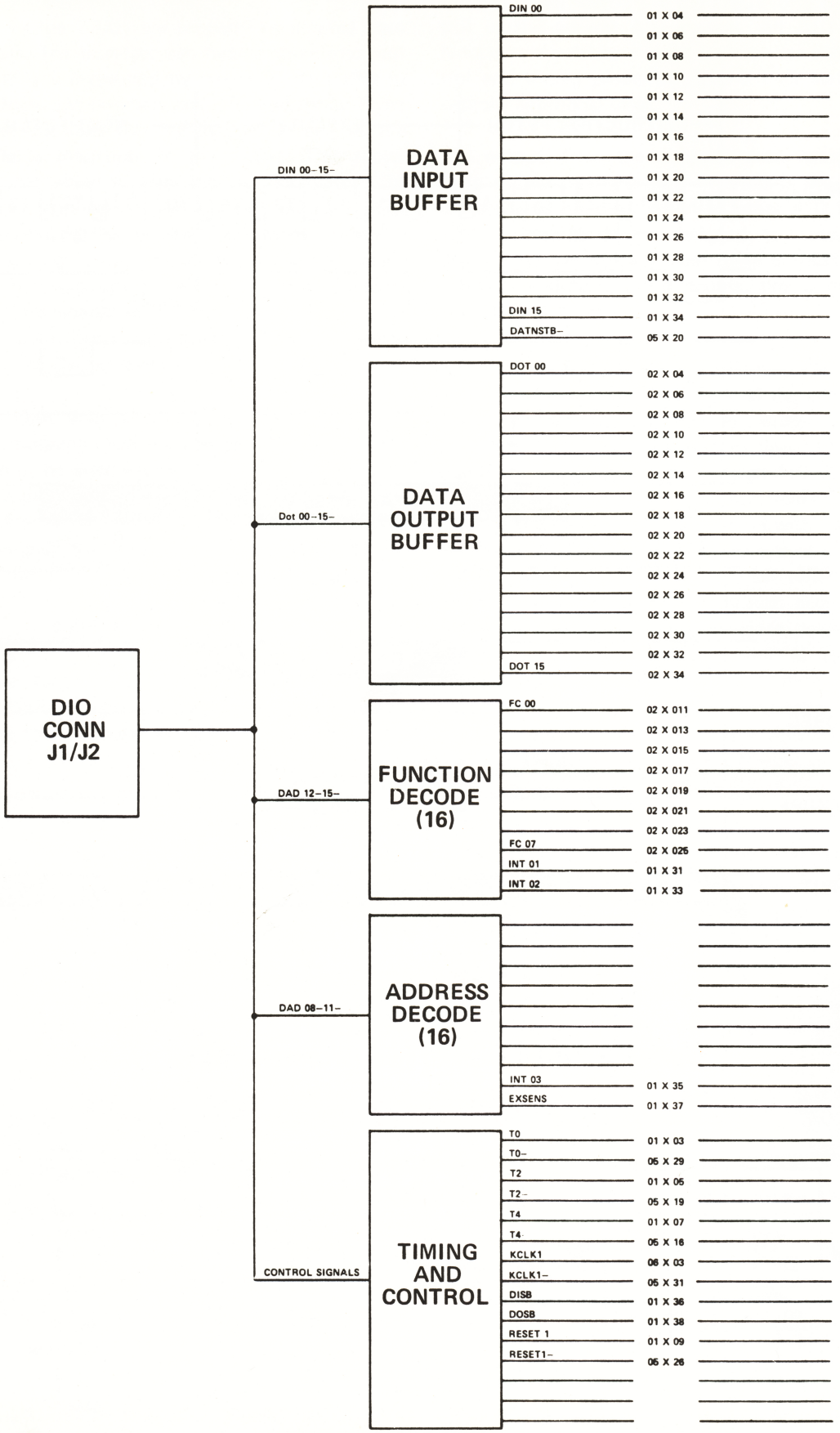


Figure 4. Wiring Diagram