RAYTHEON COMPUTER

AID DATA SHEET

MODEL

77007

DUAL CHANNEL BUFFER

GENERAL

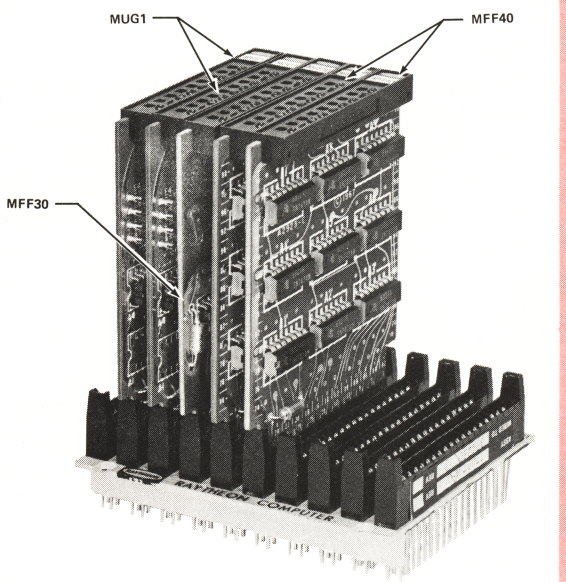
The 77007 has two 16-bit buffer registers with separate sets of control lines. The registers may be used for either input or output so that one 77007 may be used for:

Two channels of buffered digital input,

Two channels of buffered digital output, or,

One channel each of buffered digital input and buffered digital output.

Each register is handled as a data word. The 16-bit contents may be logically related such as 16-bit binary number or may be separately significant, such as a group of 16 discrete logic levels. The 77007 may also be used as control and status registers for other functional blocks. Channel Expanders, 77005 and 77006 may be attached to the 77007. The control logic has the facility for demand-response data transfers in the half-duplex mode.



SPECIFICATIONS

DIGITAL INPUTS

Function	No. of Lines	Unit DTL Load
Data Input Bus No. 1	16	1
Data Input Bus No. 1 Load Strobes	4	1
Data Input Bus No. 1 Disconnect Strobes	4	1
Data Input/Output Bus No. 1 Reset Strobes	3	1
Data Output Bus No. 1 Respond Strobes	4	1
Data Input Bus No. 2	16	1
Data Input Bus No. 2 Load Strobes	4	1
Data Input Bus No. 2 Disconnect Strobes	4	1
Data Input/Output Bus No. 2 Reset Strobes	3	1
Data Output Bus No. 2 Respond Strobes	4	1

POWER REQUIREMENTS

+5V	400 Milliamperes (±4% regulation and accuracy) = 4 Power Units

DIGITAL OUTPUTS

Function	No. of Lines	Unit DTL Drive
Data Output Bus No. 1	16	10
Data Output Bus No. 1 Stable and Ready to Read	1	12
Data Output Bus No. 1 Has Been Read and New Information May Be Entered	1	12
Data Output Bus No. 2	16	10
Data Output Bus No. 2 Stable and Ready to Read	1	12
Data Output Bus No. 2 Has Been Read and New Information May be Entered	1	12

MECHANICAL

Size	Approx. 4.125 x 4.5 x 3.75 inches = 10 Card Positions = 1 Unit Space
M Series Cards	MFF40 (2), MUG1 (2), MFF30 (1)
Spare Connectors	1

RAYTHEON COMPUTER – 2700 SO. FAIRVIEW ST., SANTA ANA, CALIF. 92704 (714) 546-7160 TWX 910 595-1570

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INPUTS

Digital inputs to the 77007 are (a) two Data Buses of 16 lines each and (b) functional strobes:

- *Load Strobes*
- *Disconnect Strobes*
- *Reset Strobes*
- *Response Strobes*

Load Strobes

These strobes gate data into a Buffer Storage Register. When all strobes go *true* (>2.5V), information on the Input Bus is gated into the Storage Register. Unwired strobes have the effect of being *true*. At the same time information is gated into the Storage Register, the Response signal (BUFCLR) is reset. When one of the Load strobes goes to the *false* state (<1.5V), the *Buffer Ready* signal is set (BUFRDYX).

Disconnect Strobes

The *Disconnect* strobes perform as the *Load* strobes except that the *Buffer Ready* term is not set. If the disconnect function is not used, one of the strobe lines must be grounded.

Reset Strobes

The *Reset* strobes perform the same function as the *Disconnect* strobes, thus allowing independent methods of resetting the *Ready* and *Response* terms. As above, if the reset function is not needed, one of the *Reset* strobes must be grounded.

Response Strobes

When all response strobes go *true* (>2.5V), the *Buffer Ready* term resets to the *false* state (0.0V). When one of the *Response* strobes goes to the *false* state (<1.5V), the *Response* signal (BUFCLR) sets.

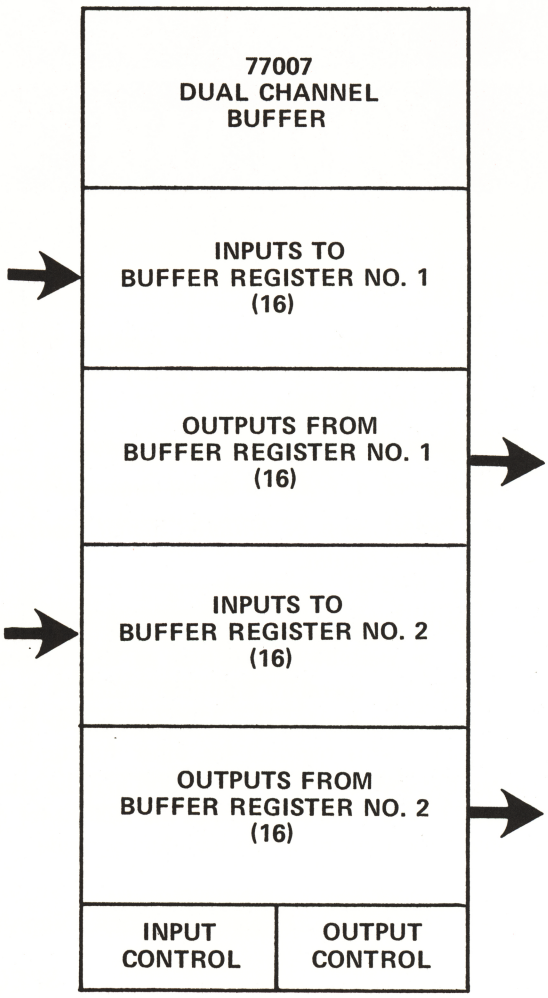

Figure 1. Functional Configuration Diagram

OUTPUTS

Outputs of the 77007 are (a) two Data Buses of 16 lines each and (b) two lines for each bus which are typically used for *Data Interlock* or *Ready/Respond* operation. One line (BUFRDY) typically raises when data in its corresponding register is stable, and when the input device wants to notify the output device that data is ready for transfer. When the output device is ready to read the data, and the *Buffer Ready* line is raised, it then reads the information and provides a *Response* strobe (or *Qualified* strobe). This causes a *Response* line to be raised (BUFCLR), and thereby notifies the input device that the information has been read.

Information can also be entered into the Buffer Register without setting the *Buffer Ready* line, while simultaneously resetting the *Response* line. This type of function is typically required when the Buffer Register is attached to the DIO Interface (77001) as a buffered output channel where the *Response* line is fixed to an interrupt level. For example, after a block transfer of data, the user would typically want to turn the interrupt off, or disconnect the device, without signaling the output device that new data is ready. The same type of operation might be required when the 77007 is connected as a buffered input channel. That is, after an external device has transferred a certain amount of data, the user might wish to read a word and turn off the interrupt stimulus without notifying the external device that it has read the last information enetered.

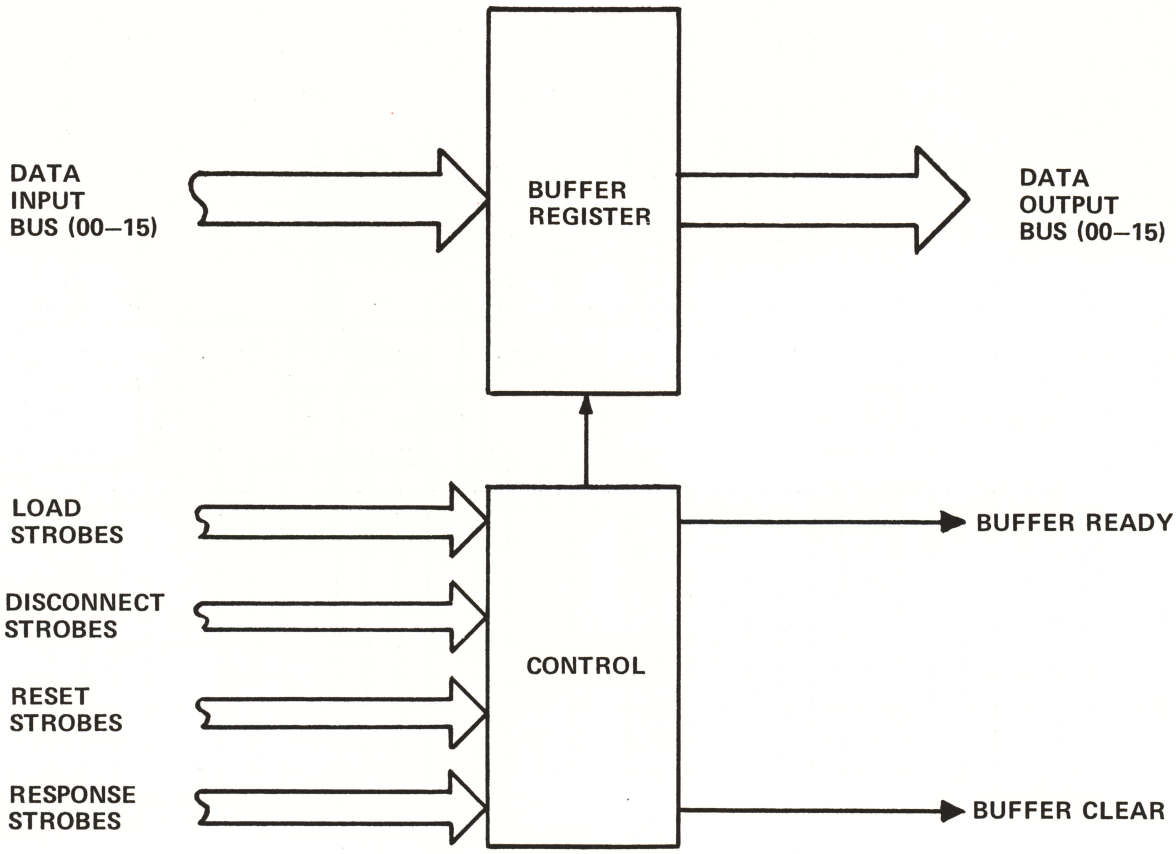

Figure 2. Block Diagram, Model 77007 (Typical 2 Places)

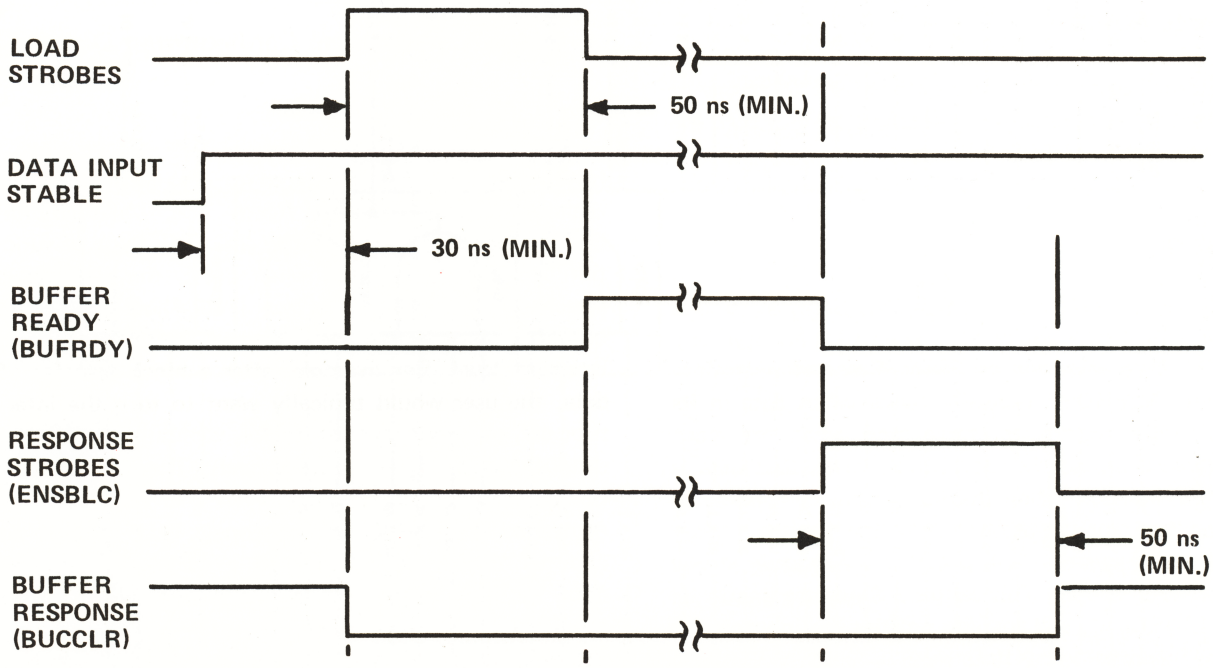

Figure 3. Timing Diagram

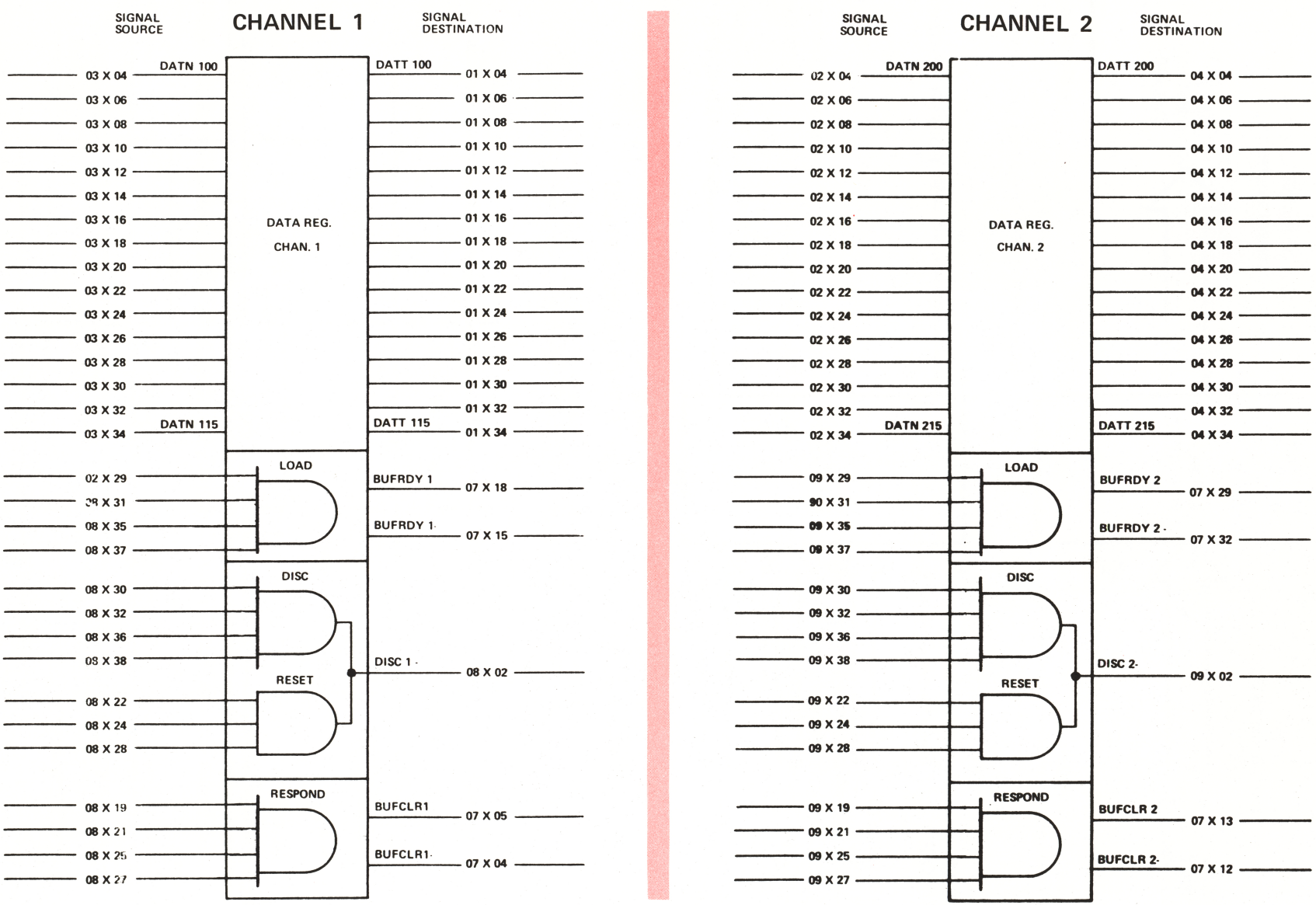

Figure 4. Dual Channel Buffer Wiring Diagram