RAYTHEON COMPUTER

AID DATA SHEET

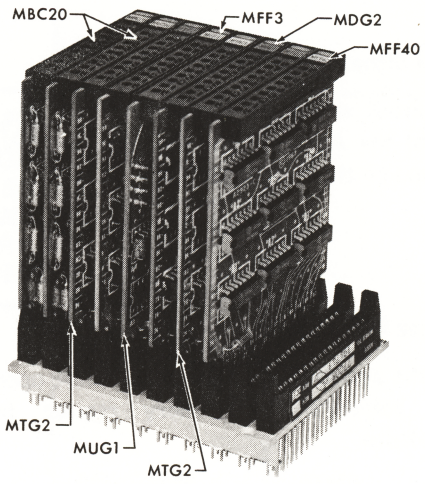
MODEL

77008

DATA CONTROLLER

GENERAL

The 77008 Data Controller provides for attachment of analog to digital converters, digital to analog converters and other devices. Control is furnished for multiplexer addressing up to 256 channels in either random or sequential mode. Conversion cycles may be clocked or free running. Control information and direct data are transferred over the 77001. Data transfers to CPU memory over a DMA channel require the 77002 and 77003.



SPECIFICATIONS

DIGITAL INPUTS

Function	No. of Lines	Unit DTL Load
Address (major device)	1	3
Respond to accumulator bits command (FCx0)	1	1
Input data and enable conversion command (FCx1)	1	1
Input data only command (FCx2)	1	1
External clock	1	2
DMA acknowledge	1	2
ADC busy	1	1
ADC frame sync	1	1

AVERAGE POWER REQUIREMENT

+5V	800 Milliamperes (±4% regulation and accuracy) = 8 Power Units

DIGITAL OUTPUTS

Function	No. of Lines	Unit DTL Drive
External clock enable	1	26.6
Start	1	26.6
Error status	1	26.6
Busy status	1	8
Frame sync status	1	8
Memory request	1	8
Interrupt	1	8
Address	16	18.6
Data input enable	1	8

MECHANICAL

Size	Approx. 9.125 x 9.5 x 3.75 inches = 10 Card Positions = 1 Unit Space
M Series Cards	MFF40 (1), MTG2 (2), MDG2 (1), MUG1 (1), MFF3 (1), MBC20 (2).
Spare Connectors	None

INPUTS

The inputs to the 77008 are:

Control signals from the 77001,

Response from the 77002,

Status from the ADC or other device and,

Clock from a 77021 or external source.

Control Signals From 77001

The control signals from the 77001 set the operating mode of the ADC system and enable *start* pulses to be generated by the controller.

Response From 77002

When the system is configured for DMA operation, the 77002 responds to memory request by issuing acknowledge.

Status

The controller monitors the ADC *Busy* and *Frame Sync* signals to provide interrupt or memory request timing as well as system status.

External Clock

The controller provides *Start* pulse to the ADC system. The *Start* interval is provided by an external source when the controller is set to a clocked mode.

OUTPUTS

The 77008 outputs are:

START pulse and address to the external device,

Status bits to the 77001 via a 77005,

Interrupt via the 77001,

Memory request to the 77002, and

External clock enable.

The ADC digitized data is normally gated into the DIO input bus through a 77005.

FUNCTIONAL DESCRIPTION

The 77008 Data Controller provides steering control for multiple data paths. Control is provided for addressing up to 256 separate input or output data channels in a half-duplex mode. Channels may be multiplexed inputs to an analog-to-digital converter, holding registers for digital-to-analog converters or other digital registers such as the 77005 Input Channel Expander, 77006 Output Channel Expander or 77007 Dual Channel Buffer. The 77008 is required for all ADC attachments in AID systems and is also required for multiple channel interfaces to the DMA channel.

Control information and direct data transfers are made over the 77001 DIO Interface. Address selection for DIO operation may be either random or sequential. In the sequential mode, the sequence advance may be timed from an external clock source.

For DMA operation, addressing is sequential and data channels are scanned at the free running rate or at a rate established by an external clock. Prerequisites for DMA operation are the 77002 DMA Interface and 77003 DMA Channel Controller. Normally the number of points in the scan sequence must agree with the word count furnished initially to the 77003. A special AID system option is available for selecting an automatic sequence mode for larger block transfers. In this mode, the buffer length is specified for 77003 word count initialization and the sequence length is specified for the 77008. Data are transferred continuously with the scanning sequence repeated until the word count is exhausted.

For concurrent operations over the DMA channel, such as simultaneous analog input and output, two 77008's are required.

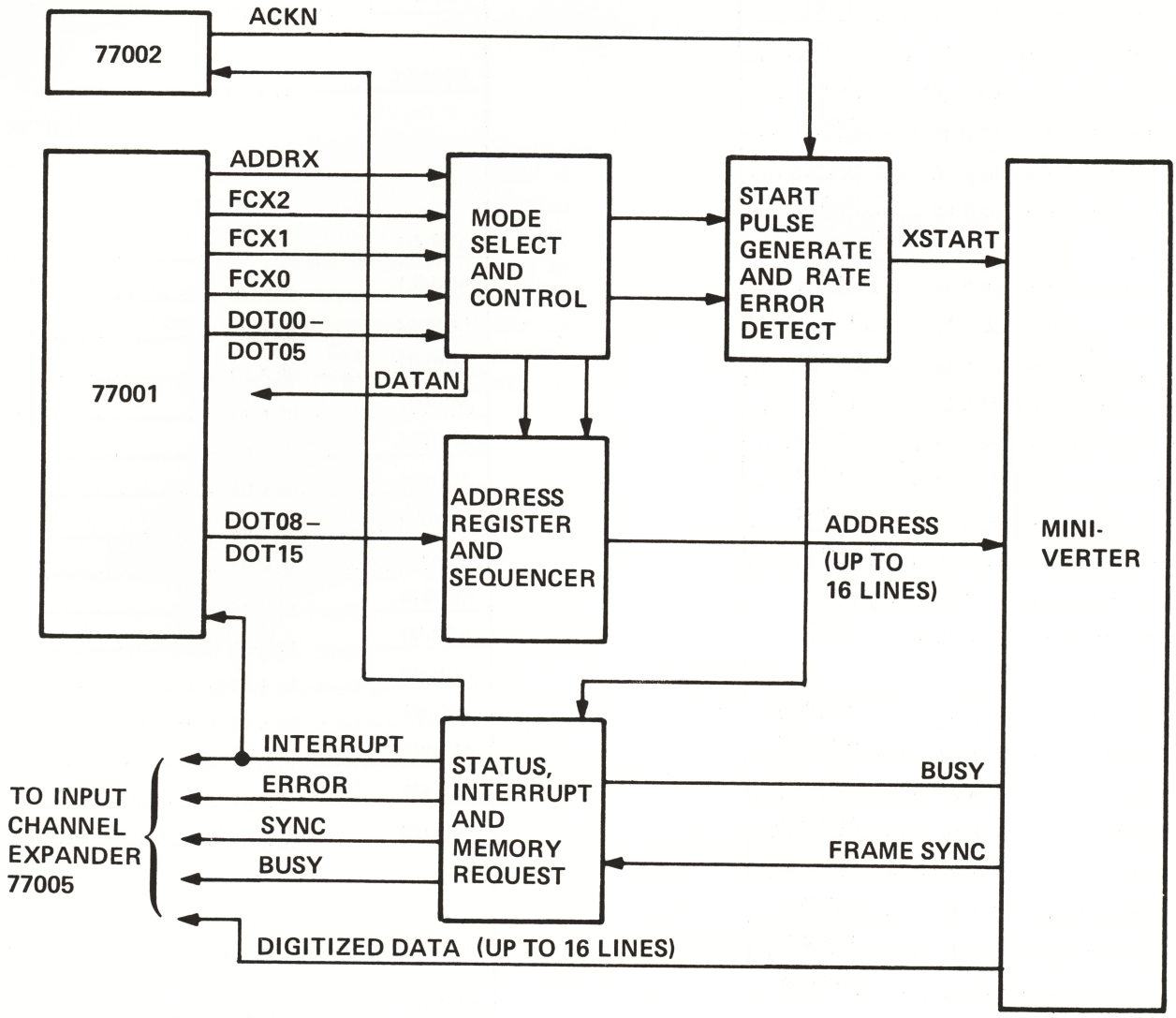


Figure 1. 77008 Data Controller in Miniverter Configuration

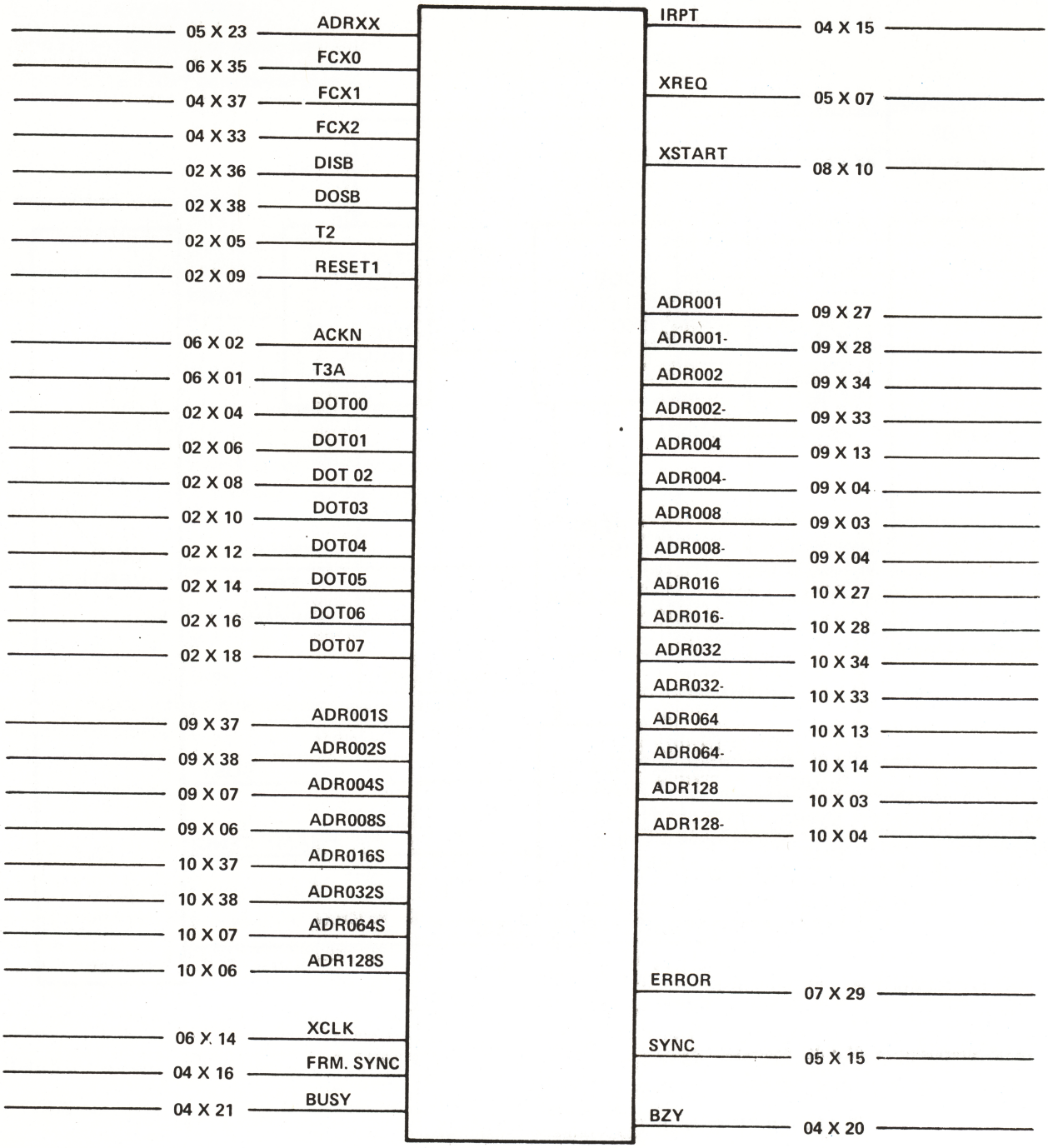


Figure 2. 77008 Wiring Diagram