RAYTHEON COMPUTER

AID DATA SHEET

MODEL

77011

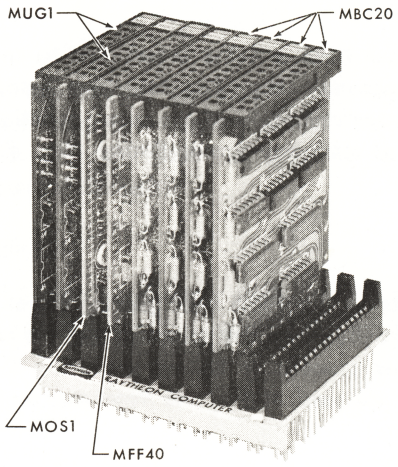
ELAPSED TIME COUNTER

GENERAL

The 77011 Elapsed Time Counter consists of a 16-bit bi-directional counter and an associated 16-bit storage register. The control logic permits the 77022 to be used in a variety of counting applications including:

- *Elapsed or Interval Time Count*
- *Single or Bi-directional Event Count*
- *Interval Timer*

The register section permits the counter contents to be interrogated completely asynchronously, without interference or interruption of the counting function. The 77011 units may be connected in series to form count lengths in multiples of 16 bits.



SPECIFICATIONS

DIGITAL INPUTS

Function	No. of Lines	Unit DTL Load
Preset Data	16	2.67
Preset Strobes	4	1
Reset Strobes	4	1
Reset– Strobe	1	1
Run Enable Direct Set	4	1
Run Enable Direct Reset	4	1
Run Enable J-K Inputs	2	1
Run Enable Clock Input	1	2
Transfer Enable Dirct Set–	1	1
Transfer Enable Direct Reset	1	1
Transfer Enable J-K Inputs	2	1
Transfer Enable Clock Input	1	2
External Clock Strobes	3	1
External Clock Strobe–	1	10.68
Up/Down	1	10.68
Carry In–	1	2.67
Count Zero Halt Input	1	1
Register Transfer Strobes	4	1
Transfer Input–	1	3
Enable Phase C Delay	1	1

DIGITAL OUTPUTS

Function	No. of Lines	Unit DTL Drive
Data	16	10
Reset	1	8
Run Enable	1	12
Transfer Enable	1	12
Count Zero Halt Output	1	8
Gated Clock	1	10
Phase A Delay Clock	1	25
Phase C Delay Clock–	1	24
Carry Out–	1	9

MECHANICAL

Size	Approx. 4.125 x 4.5 x 3.75 inches = 10 Card Positions = 1 Unit Space
M Series Cards	MBC20 (4), MFF40 (1), MOS1 (1), MUG1 (2)

POWER REQUIREMENTS

+5V	1000 Milliamperes (±4% regulation and accuracy) = 10 Power Units
-5V	1.2 Milliamperes = less than 1/50 Power Unit

INPUT SIGNALS

Preset Data

The preset data inputs form a 16-line data bus connected to counter section preset gates. The bus lines are positive true and a true data line during the strobe interval will set its associated counter bit *on.*

Preset Strobes

These strobes form a 4-line preset gate to enable the 16-line preset data bus. The four-term gate permits flexible system definition of the preset function. *When not used, at least one Preset Strobe term should be grounded.*

Reset

These inputs form a 4-line reset gate to clear all counter states. When used with the preset strobe, the reset gate should either precede or be overlapped by the preset gate. *When not used, at least one Reset gate term should be grounded.*

Reset—

Reset— is a single line negative true signal used to clear all counter states. This signal is logically OR'ed with the 4-line reset gate and is usually defined as a manual reset.

Run Enable Direct Set

These inputs go to a 4-line flip-flop direct set gate used to set the run enable (RUNENB) control flip-flop to its true state. The four-term gate permits flexibility in system timing. *If the run enable control flip-flop is to be used in a clocked mode, at least one term of the preset gate should be grounded.*

Run Enable Direct Reset

This 4-line gate is used to direct clear the run enable control flip-flop. The flip-flop will also be cleared by the normal reset inputs. *When not used, at least one term of the direct reset gate should be grounded.*

Run Enable Clocked Control

The Run Enable J and K gate inputs and associated clock term are also available for clocked mode operation of the RUNENB flip-flop. Note that the RUNENB signal (09 X 03) is not directly wired to any control term and becomes a portion of the 77011 logic only at the user's discretion. When not used as 77011 control, the flip-flop may be used for associated external functions.

Transfer Enable Direct Set-

This single-line negative true signal sets the transfer enable flip-flop (XFRENB) to its true state. The flip-flop will also be set by the normal Reset signals.

Transfer Enable Direct Reset

This single-line positive true signal resets the transfer enable flip-flop. When 77011 units are used in series and are to be interrogated by more than one command, the first interrogation command is usually used to reset the XFRENB flip-flop. *When the flip-flop is used and only the clocked mode is required, this input should be grounded.*

Transfer Enable Clocked Control

The J and K gate inputs and their associated clock are available for clocked functions. On multiple transfer operations the trailing edge of the *last interrogation may be used to set* the flip-flop. As with the run enable flip-flop, the XFRENB signal (10 X 03) is not directly wired to any control term and becomes a portion of the control logic only by user connection.

External Clock

This 3-line gate term allows gating of the counted input. With the clock proper as one term, two additional gate levels are available. Typical 77011 operation would connect one gate term to the RUNENB signal. When this configuration is used, the actual Counter Clock input should be connected to Phase A Delay Clock to prevent count ambiguity.

External Clock—

This is a single-line negative true signal which is logically OR'ed with the normal external clock signal. *When the false level clock is to be used, at least one of the external clock gate terms should be grounded.*

Count Clock

The Count Clock signal is the actual counted input to the 16-bit counter. This signal is not connected to any control term and must be wired at the user's discretion. Normal connections might be:

- External to other system equipment
- Internal to the gated clock output for synchronous system operation.
- Internal to Phase A Delay Clock for asynchronous operation.

Up/Down

The counter up/down control line must be maintained at a logical 1 or positive level for up, and at a logical 0 or ground for down.

Carry In–

The counter is supplied with a negative true Carry In– level which may be used when the units are connected in series. For example, to form a 32-bit counter the Carry Out– of the lesser significant bits is connected to the Carry In– of the more significant group.

In addition, the Carry In– signal may be connected to the Carry Out– of a single group via the count 0 halt gate. In this configuration, the unit may be used as an interval timer by counting up (or down) from a preset count and halting – with the count 0 halt output level forming the *complete* level. *When not used, the Carry In– signal should be grounded.*

Count Zero Halt

An auxiliary gate (10 X 26) may be used to halt the counter at either an all zeros or all ones condition. The input and output of this inverting gate must be wired by the user and may be used as a system inverter if not required by the 77011.

Register Transfer Control

These inputs go to a 4-line gate which may be wired to the actual Counter-to-Register strobe gates to permit the counter contents to be set into register form under external system control. When the control is synchronous with respect to the counting function, the gate output may be wired to the XFER– input directly.

For asynchronous operation the gate may be wired to the Phase C Clock Delay enable input and the XFER– input connected to the Phase C Clock Delay false output.

Transfer Control

This single negative true line (XFER–) connects to the register transfer strobe drivers. This line will normally connect to:

- The output of the register transfer input gate for synchronous operation.
- The Phase C Clock Delay false output for asynchronous operation.

Enable Phase C Delay

This single control line enables the Phase C Delay Clock (and the register transfer). For computer DIO interrogation, this line normally would connect to the register transfer input gate output (10 X 23). For multiple transfer requirements the signal would connect to the XFRENB level previously noted.

OUTPUT SIGNALS

Reset

This single-line positive true signal expresses the logical sum of the Reset and Reset– inputs. The signal may connect to the reset input of units in series or to external control elements.

Run Enable

The Run Enable output is a single-line flip-flop signal normally connected to an input of the external clock control gate.

Transfer Enable

This output is a single-line flip-flop signal normally connected to the Phase C Clock Enable when multiple 77011 interrogations are to be implemented.

Gated Clock

This output is a single clock pulse line formed from either the gated external clock or the External Clock– inputs. This signal connects to the count clock input when the counter operation is synchronous with the external equipment.

Phase A Delay Clock

This output is a delayed clock formed from the External Clock inputs and used when the count function is asynchronous to enabling or other system terms. Use of this clock to connect to the Count Clock input prevents erroneous *half-clocks* from being formed and large count errors being introduced into the 77011.

Phase C Delay Clock–

This delayed negative true clock connects to the XFER– input when asynchronous system register interrogation may occur. The delay between Phase A and C is controlled by the *Phase B Delay* and is set to compensate for any counter propagation delays.

Data

These lines form a 16-line register data bus suitable for direct connection with other AIDS elements.

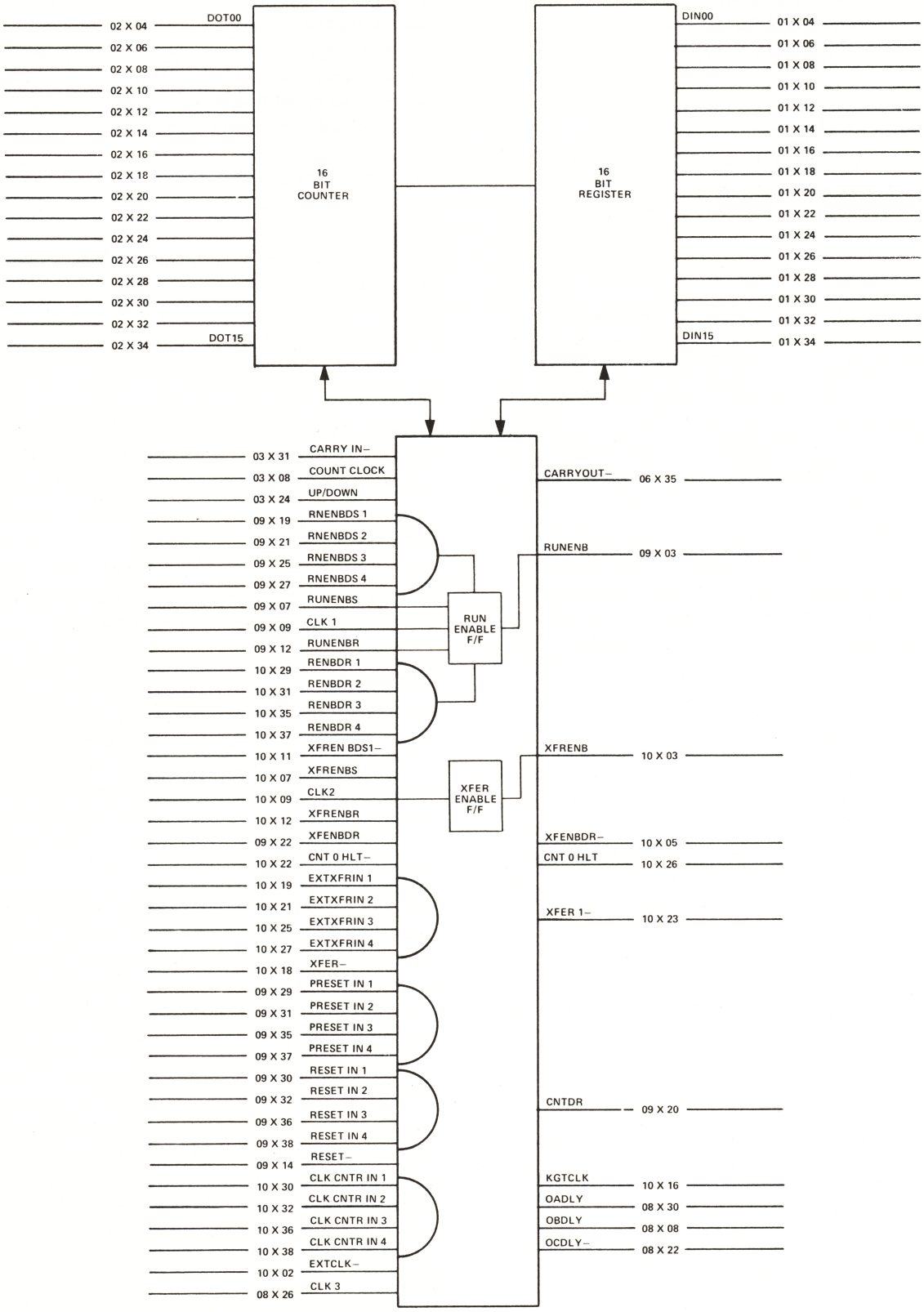


Figure 1. 77011 Wiring Diagram