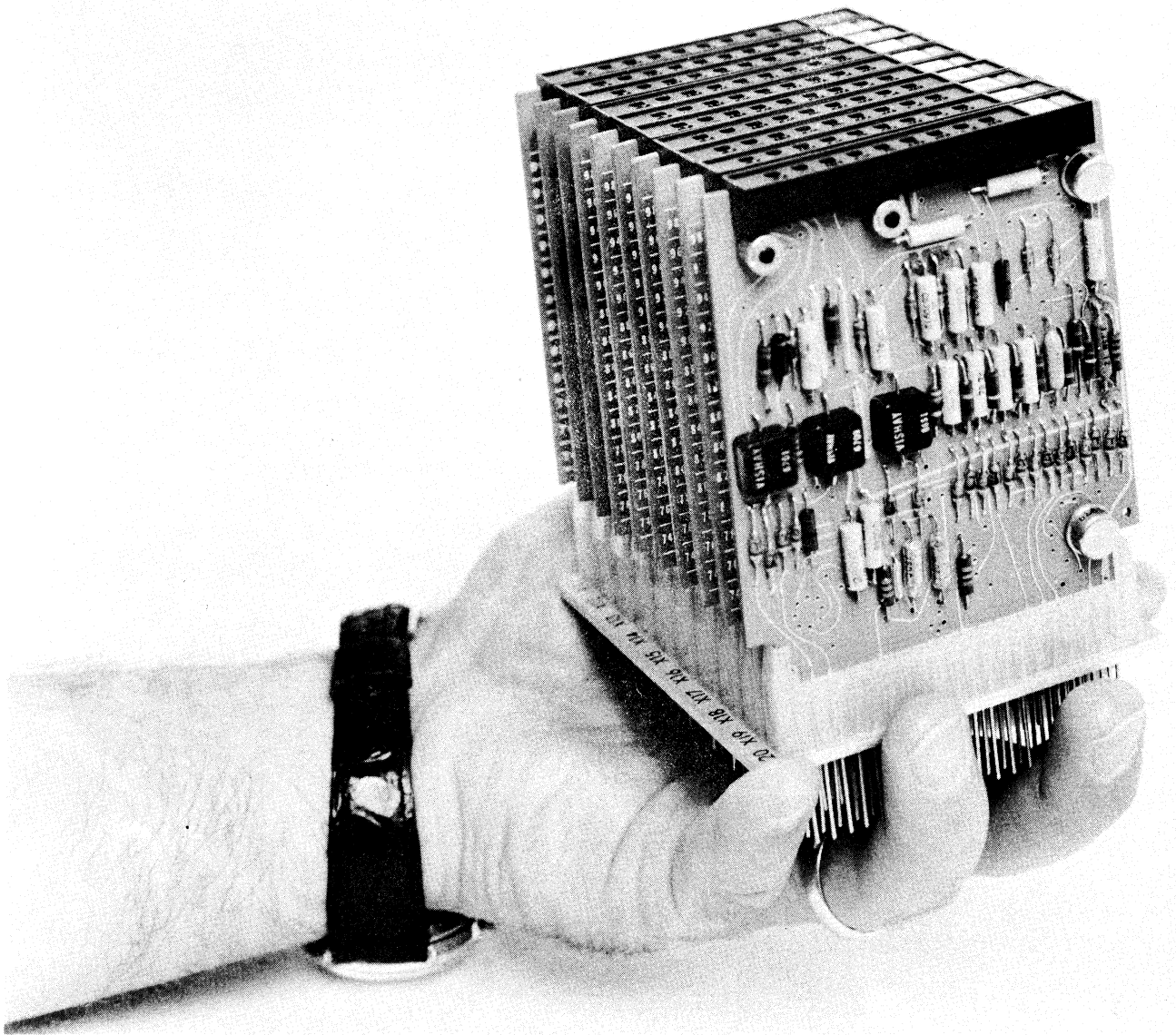


RAYTHEON  
**AID**

APPLICATIONS  
INTERFACE  
DEVICE



# RAYTHEON AID

is the nearest device yet to a universal interface for a digital computer. Designed for attaching peripheral equipment to the Raytheon 703 and 706 computers, AID is a systems approach to solving the problems of program control over a wide variety of data characteristics and control functions.

AID handles the details of how to get data through the computer and allows the user to concentrate on system objectives which solve his problem. Means provided are:

**Functionally Modular Hardware** — an economical way of obtaining variety in the interface.

**Systematic Components** — an easily altered or expanded system is more flexible, has a longer life and provides a greater return on the original investment.

**Systems Assurance** — specific price/performance characteristics and programming efficiency are reviewed by Raytheon applications engineers.

**Computer Checkout** — the final criteria of a successful system is a functional test.

## MODULAR HARDWARE

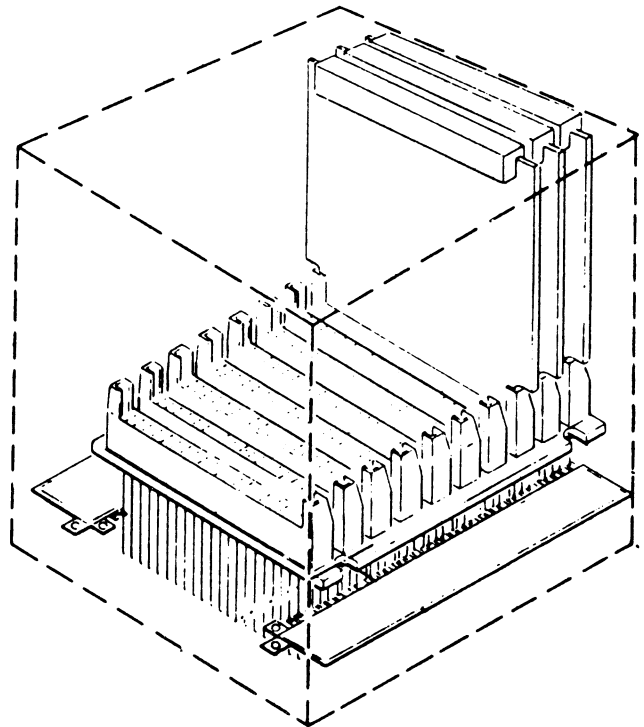
AID hardware consists of functional blocks. Characteristics of each block meet the requirements for a unique phase of the data transfer process. A particular interface is then assembled by combining the appropriate blocks. Advantages derived from this approach are:

An interface can be chosen to meet specific user requirements.

For a system with multiple devices there is a minimum of hardware duplication.

Organization with standard controls simplifies software.

The degree to which a computer front-end needs to be tailored to the application will vary. In most cases, for data acquisition or control systems, selecting the appropriate AID blocks is all that is necessary. However, AID hardware is compatible with Raytheon's M-series analog and digital logic modules. This allows an economical means of adapting to even the most sophisticated system's requirements.



## **FUNCTIONAL COMPONENT DESCRIPTIONS**

### **77001 Direct Input/Output Interface.**

Attachment to the DIO bus of the central processor is made by the 77001. It provides the timing and logical responses for direct transfer of data with the CPU accumulator register using DIN and DOT instructions. Device and Function fields of the instructions are decoded and furnished for selection and gating controls of attached devices. It also serves as a terminal for the External Sense Line and inputs to the Priority Interrupt system.

### **77002 Direct Memory Access Interface.**

Attachment to the DMA bus of the central processor is made by the 77002. It controls the logical sequence of address and data presentation for demand-response transfer of data with CPU main memory.

### **77003 Direct Memory Access Channel Controller.**

Control of block data transfers with CPU memory is provided by the 77003. It is initialized from the 77001 by loading a word count and starting address from the CPU program. After each data word is transferred over the 77002 the address is automatically incremented to the next higher memory location in preparation for another transfer. At the same time the word count is decremented by one for each transfer. Upon reaching a word count of zero the transfer operation is terminated and an interrupt signal generated to alert the CPU program of the channel ending condition.

### **77004 Priority Line Controller.**

Up to four individual request signals are accommodated by the 77004. Outputs are the "OR" indication of the requests and the status of the input lines. The 77004 is used for attachment to the External Sense line, for expansion of a single Priority Interrupt level, or for steering control of the 77002 and 77003 when used in a multiplexer configuration.

### **77005 Input Channel Expander.**

Provides gating logic for attaching up to four

groups of 16 lines each to an input data connection.

### **77006 Output Channel Expander.**

Provides gating logic for attaching up to four groups of 16 lines each to an output data connection.

### **77007 Dual Channel Buffer.**

Two 16-bit buffer registers with separate sets of control lines are furnished in the 77007. Buffers may be used for either input or output so that one 77007 may be used for two channels of buffered digital input, for two channels of buffered digital output, or for one channel each of buffered digital input and buffered digital output. Each register is handled as a data word. 16-bit contents may be logically related such as a 16-bit binary number or may be separately significant such as a group of 16 discrete logic levels. The 77007 may also be used as control and status registers for other functional blocks. Channel Expanders, 77005 and 77006, may be attached to the 77007.

### **77008 ADC Controller**

The 77008 provides for attachment of analog to digital converters. Control is furnished for multiplexer addressing in either random or sequential mode. Conversion cycles may be clocked or free running. Control information and direct data are transferred over the 77001. Data transfers to CPU memory over a DMA channel require the 77002 and 77003.

### **77009 DAC Controller.**

The 77009 provides data steering for a group of digital to analog converters. It provides addressing in either random or sequential mode and data transfer may be clocked. Data transfers from CPU memory over the DMA channel require the 77002 and 77003.

### **77010 Relay Output Buffer.**

Characteristics of the 77010 are equivalent to a single 16-bit register output of the 77007. Output is contact closure of 16 reed relays.



### **77011 Elapsed Time Clock/Counter.**

The 77011 consists of two 16-bit counters. Counters may be operated as two independent 16-bit counters or in tandem as one 32-bit counter. Pulse input may be from an external source or the output of 77023 or 77024 Clock Pulse Generators. Each 16-bit section may be preset or read by the appropriate direct data transfer over the 77001.

### **77021 Count/Interval Compare Indicator.**

The basic 77021 is a 16-bit counter attached to a 16-bit compare circuit. In normal operation when the binary count equals the compare word an output pulse is generated and the counter is reset to zero but enabled to continue counting. The compare word may be prewired for a fixed count indication or may be attached to an output channel buffer of the 77007 for preset count indication. When 77021 input is the output of either Clock Pulse Generator an interval timer output results. Two variations are offered for use with the 77007.

1. After compare the counter is reset but disabled until a subsequent data transfer is made to the 77007.
2. Output is a pulse stream equal to the number of counts in the compare word.

### **77022 Sense Line Expander.**

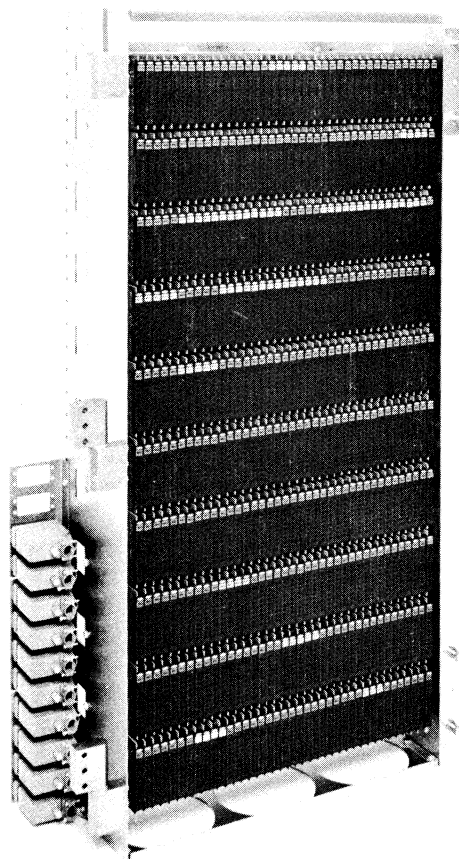
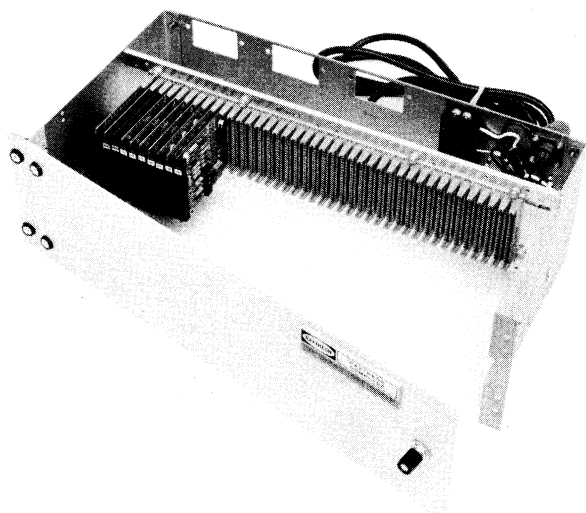
Input for 16 discrete levels is provided. Upon program command the 16 levels are compared with the word contained in the CPU accumulator. Output is a signal indicating the "OR" condition of any "1" and "ON" results of the comparison. This output is attached to the External Sense Line.

### **77023 Clock Pulse Generator – 60 Hz.**

Operates on line frequency to produce timing pulses for use with 77011 and 77021 as timers. Pulse conditioning is available for two external pulse sources.

### **77024 Clock Pulse Generator – 1.0 MHz.**

Operates with a crystal controlled frequency source to produce timing pulses for use with 77011 and 77021 as timers. Frequency stability is 0.02% over the operating environment of the central processor.

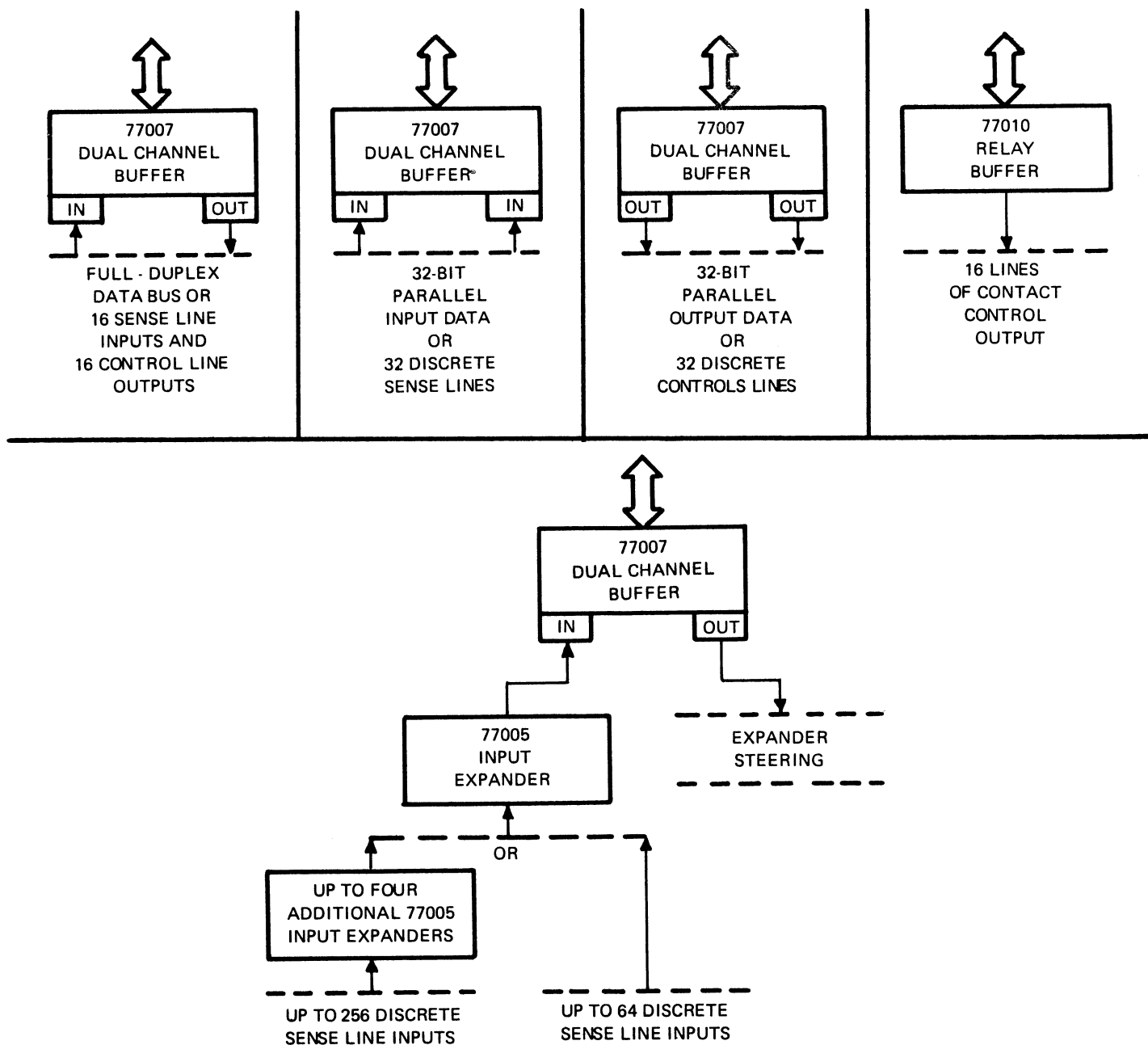


## DATA INTERFACES

### Digital Data

Digital data words are handled in groups of 16-bits by the 77007 Dual Channel Buffer. Buffer register controls are independent in the 77007 but to an external device the control signals may be made to occur simultaneously, which has the effect of a 32-bit data path. The path may be further expanded by simultaneous gating of multiple 77007's. When the external device is capable of maintaining its line levels, the input path may be

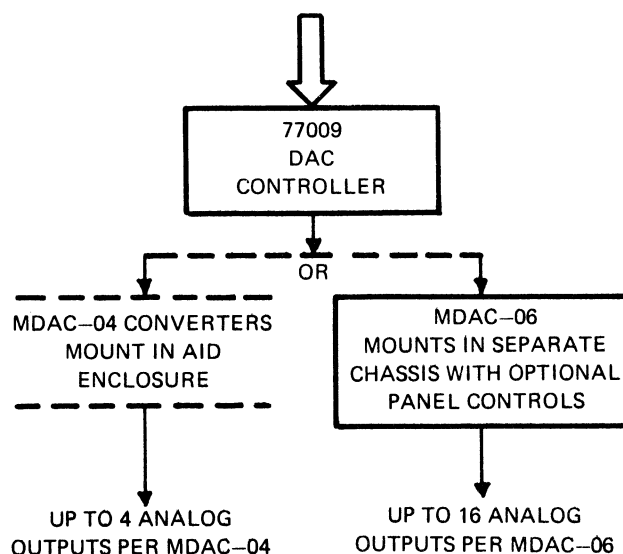
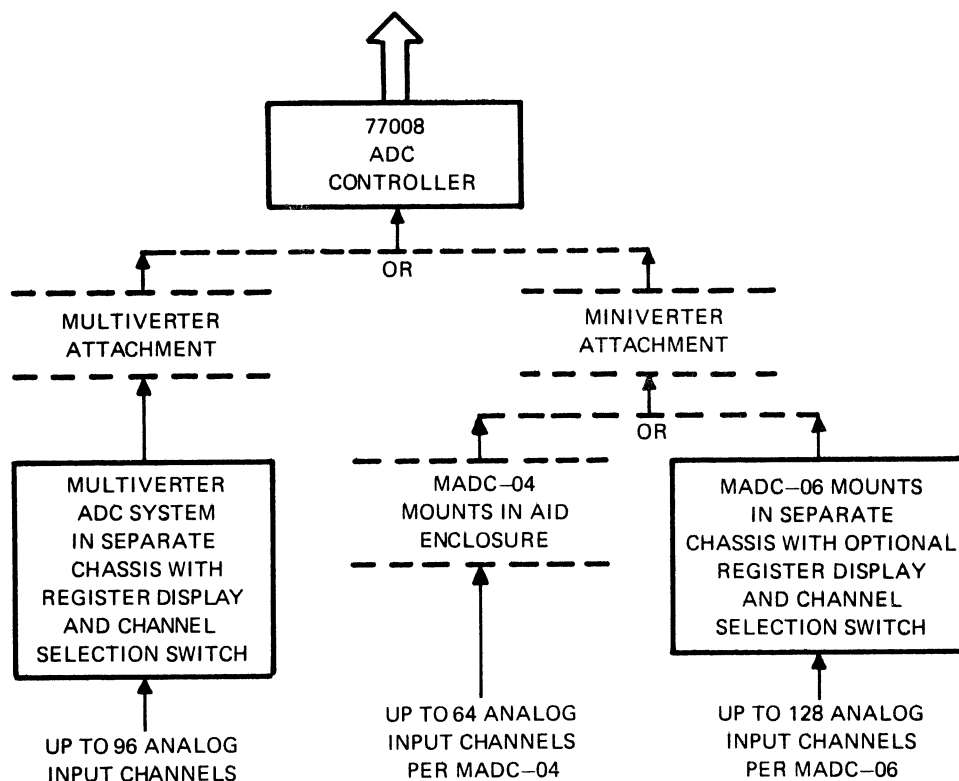
expanded by the 77005 Input Channel Expander. This is especially useful for a large number of discrete input lines. Furthermore, the 77005 may be expanded by attaching to it up to four additional 77005's, which provides a capability for 256 lines. For momentary discrete outputs or selected paths of 16 output lines a similar approach may be taken using the 77006 Output Channel Expander. For expanding output to devices which have no buffering capability, multiple 77007's are used to maintain line levels. The 77010 Relay Output Buffer provides contact output.



## Analog Data

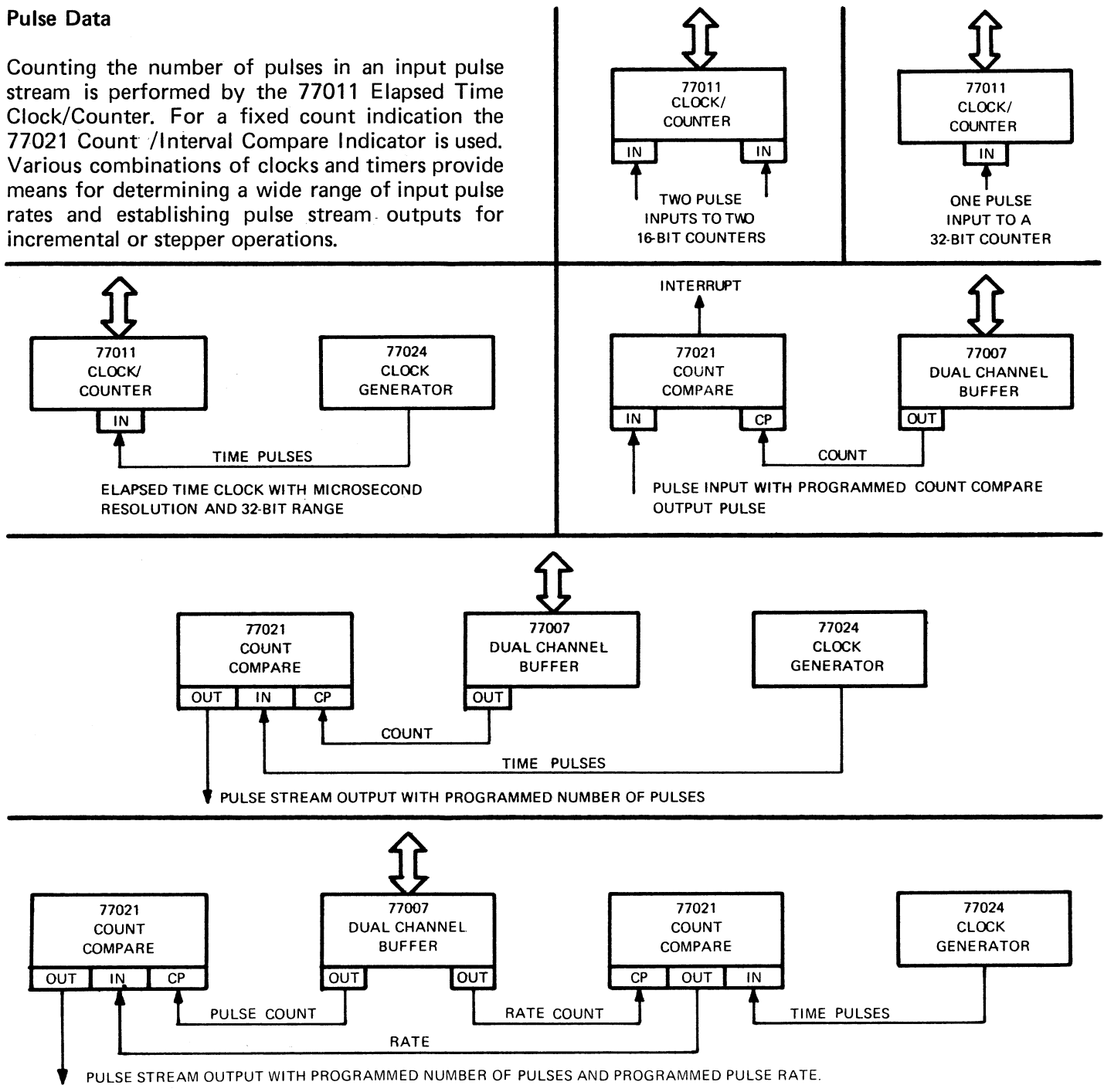
Raytheon's complete line of analog-digital conversion equipment may be attached to the CPU by AID hardware. Resolutions of 10-bit, 12-bit or 15-bit binary and 13-bit BCD data are available in standard Converters. Analog input through the Multiverter or Miniverter systems requires the 77008 ADC Controller. These systems include a sample and hold amplifier and multiplexer

switches. Their operation is described in Bulletins SP-288 and SP-205C along with their capacity for analog input signals. Up to 16 digital to analog converters may be attached to the 77001 DIO Interface without a controller when the steering address is furnished in the four least significant bits of the data words. Analog output of data transferred over a DMA channel requires the 77009 DAC Controller for steering.



## Pulse Data

Counting the number of pulses in an input pulse stream is performed by the 77011 Elapsed Time Clock/Counter. For a fixed count indication the 77021 Count /Interval Compare Indicator is used. Various combinations of clocks and timers provide means for determining a wide range of input pulse rates and establishing pulse stream outputs for incremental or stepper operations.



## Timing Pulses

77023 and 77024 Clock Pulse Generators used with 77011 and 77021 Counters provide for sampling intervals, elapsed time measurements, and program intervals. A wide range of timing intervals is obtained by the 77021 and 77024 combination where the 77021 divides the frequency of the 77024 output.

## Control and Status Data

In addition to the 77024 Priority Line Controller and the 77022 Sense Line Expander any of the discrete data components may be used for control and status information. Hence, a means is available for diagnosis and test of the front-end system that is fully compatible with data handling methods.



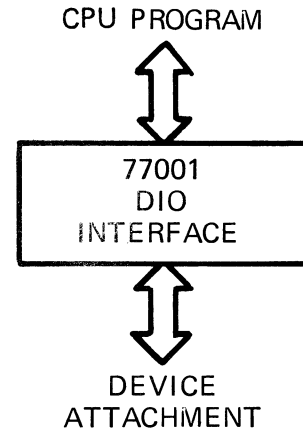
## CHANNEL STRUCTURE

AID performs a data channel function in communicating with the CPU over the Direct Input/Output Bus and Direct Memory Access Channel. Basic configurations of AID blocks allow

communication with peripheral equipment in three modes: Direct, Select, or Multiplex. Each mode has particular advantages for different device characteristics and the modes may be mixed in a front-end system to obtain the best data handling capability for a given application.

### Direct Mode

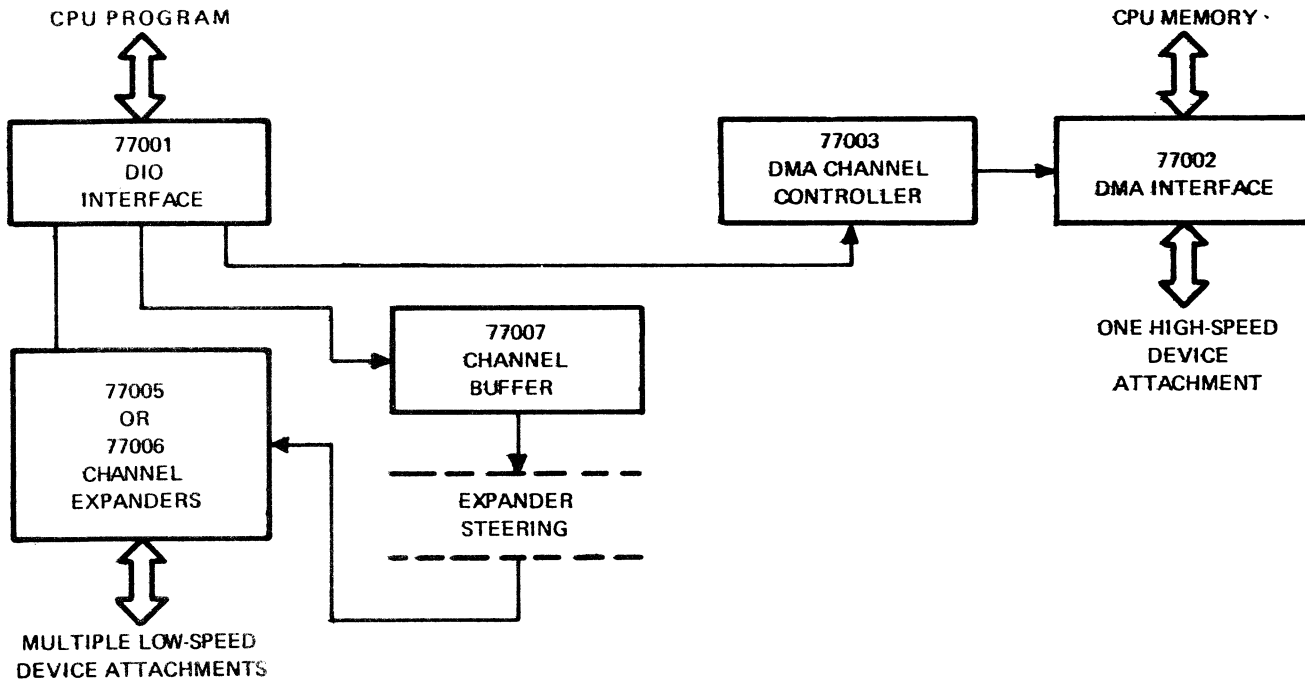
Direct mode provides immediate data transfer under direct program control. Demand-response logic of the data transfer is performed by the CPU program in conjunction with a priority interrupt or the external sense line. General use is for a small number of devices communicating with the CPU accumulator register and for the transfer of control or status information in the Select and Multiplex modes. Maximum data rates vary from 24,000 words/second with a 703 CPU using priority interruptions of a problem program to rates approaching 278,000 words/second with a 706 CPU executing a dedicated I/O program. Transfer is over the 77001 DIO Interface.



### Select Mode

Select mode provides both immediate and memory buffered data transfers. It requires selecting a data path before the actual data transfer is made. General uses are for asynchronous communication with a large number of devices, for burst transfer with a selected high-speed device, or for matching

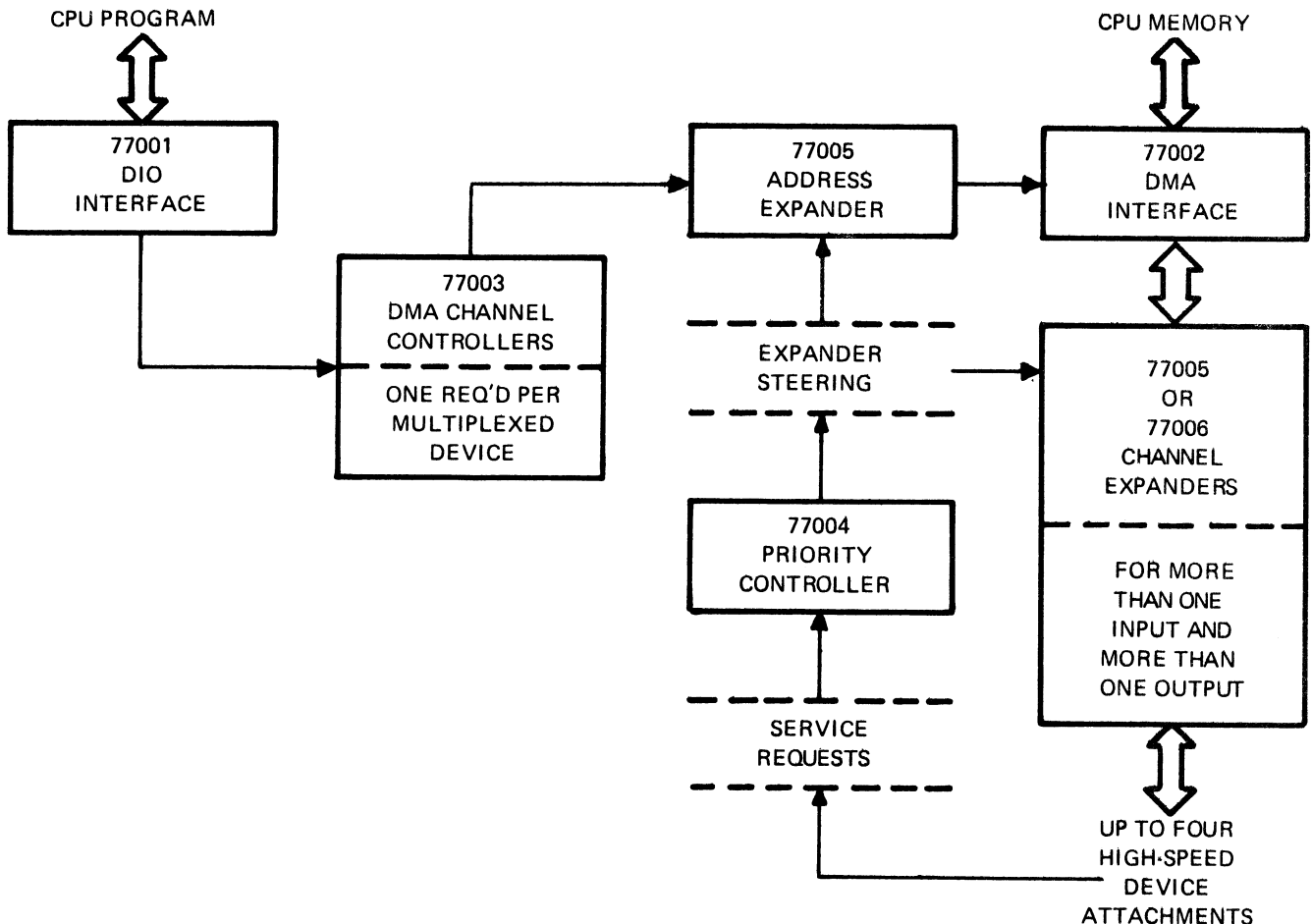
the response of slow-speed devices. Maximum burst rate approaches CPU memory speed for data transfer over the 77002 DMA Interface under control of the 77003 DMA Channel Controller. Communication with a large number of devices over the DIO Interface will in general require a 77007 Dual Channel Buffer to provide steering signals for gating the appropriate data path.



## Multiplex Mode

Multiplex mode provides asynchronous memory buffered transfers for up to four concurrently operating devices. Priority is assigned to each device on a sequential scan basis. Instantaneous transfer rate of the highest priority device is

one-fourth of the CPU memory speed. Data is transferred over the 77002 DMA Interface and one 77003 DMA Channel Controller is required for each operating device. 77003's connect to the 77002 through a 77005 Input Channel Expander and their gating sequence is determined by a 77004 Priority Line Controller.



## HOUSING, POWER AND CABLES

Chassis for mounting the functional blocks are furnished in incremental sizes which fit Raytheon's standard processor cabinets and conform to 19 inch EAI mounting standards. Unless otherwise noted in the AID System Planner each functional block requires one space unit in the chassis, and each chassis size has a specific number of space units available for mounting functional blocks. Chassis sizes for 8 to 40 blocks are swing-out gates for easy access to cable connectors.

As a general rule the 77036 Power Supply will

furnish adequate power for eight to ten functional blocks in the average system. However, if a large number of line drivers are employed the capacity of the power supply is less. Power ratings for the functional blocks and power supplies are shown in the AID System Planner. For large systems where power requirements exceed the 77036 capacity, either multiple 77036's or the 77037 power supply may be used. This provides alternatives in mounting to take advantage of available space.

The 77040 DIO Cable will be required for all systems. Only systems with the 77002 DMA Interface require the 77041 DMA Cable.

# AID SYSTEM PLANNER

## FUNCTIONAL BLOCKS

Model No.	Description	Power Units Required	Space Units Required
77001	DIO Interface	8	1
77002	DMA Interface	9	1
77003	DMA Channel Controller	8	1
77004	Priority Line Controller	3	1
77005	Input Channel Expander	3	1
77006	Output Channel Expander	9	1
77007	Dual Channel Buffer	2	1
77008	ADC Controller	5	1
77009	DAC Controller	5	1
77010	Relay Output Buffer	3	1
77011	Elapsed Time Clock/Counter	8	1
77021	Count/Interval Compare Indicator	Total of three 77021, 77022, 77023 or 77024 mount in one 77029 Utility Mounting Block.	
77022	Sense Line Expander		
77023	Clock Pulse Generator		
77024	Clock Pulse Generator		
77029	Utility Mounting Block	5	1

## MOUNTING CHASSIS

Model No.	Space Units Available	Panel Space Required, inches	Depth, inches
77030	4	5¼	15¾ (Provides space for 77036)
77031	8	8¾	7½
77032	16	15¾	7½
77033	24	21	7½
77035	32	28	7½
77035	40	35	7½

## POWER SUPPLIES

Model No.	Power Units Furnished	Power Required	Mounting Requirements
77036	50	1.0 amp at 105-125 VAC	4 contiguous space units in 77031-35.
77037	100	2.0 amp at 105-125 VAC	3½ inches panel space.
77038	200	4.0 amp at 105-125 VAC	3½ inches panel space

## CABLES

77040	DIO Cable	77040 and 77041 are furnished in standard lengths of 6 feet.
77041	DMA Cable	

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