THE UNIVAC 1108: ADVANCED, PROGRAM-COMPATIBLE SUCCESSOR TO THE 1107.

The 1108 represents a controlled outgrowth of its predecessor system, the 1107. As such, it has the advantages of proved logical concepts, established software, compatibility with existing UNIVAC 1107 software, and use of standard 1107 peripherals. The 1107, being a tremendously sophisticated system itself, provides a firm base for the advancement of this new system.

COMPATIBILITY

One of the most attractive features of the 1108 is 1107 upward compatibility. Standard 1107 programs can run on the 1108. Recompilation is necessary only when it is desired to utilize the new 1108 features.

ENHANCED SOFTWARE

1108 Software will continue to be drum-oriented and will be enhanced to make profitable use of expanded core memory and additional repertoire. A truly integrated executive system will combine the classic simplicity of the monitor with full real-time and multi-programming capability. Improvements to compilers in the form of language extensions and logic speedups (both in the compilers themselves and the object code produced) will account for generally increased throughput at all levels. The 1108 system will follow the 1107 Package-B Program Library and Allocator Concepts in the manipulation and construction of user programs. Most "system" software will be resident in the System Drum Library.

MEMORY-BASIC SPEED ADVANTAGE

A control and core memory speedup of 5.3 over the 1107 yields the following basic cycle-times:

Control Memory – Read Access - 125 Nanoseconds (.125 Microseconds)

Main Memory – Read Access - 400 Nanoseconds
Read-Restore - 750 Nanoseconds

Basic Instruction Cycle Time – Alternate Bank - 750 Nanoseconds
Same Bank - 1.5 Microseconds

Overlapping of banks provides an "effective" cycle time (i.e. acquisition of data and next instruction in same memory cycle) of .375 nanoseconds.

CONTROL MEMORY

Control Memory is of the same configuration used in the 1107, with the exception of the Real-Time clock, which now uses only 18 bits of register 100 (RØ), and the T-register (R3), which is now used to capture the special function register upon occurrence of an interrupt. The memory is physically constructed of word-addressed arrays of integrated circuit flip-flop modules, the most advanced devices on the market today.

MAIN MEMORY

Increased memory size (131,072 words) and modularity (16K increments) allow more incremental pricing and, of course, make the system much more attractive from a growth standpoint. The minimum memory size is 32K in two banks. Each bank (a total of four) holds a maximum of 32K and has separate addressing and readout registers to permit overlapping. Systems software will run in the basic 32K configuration and is optimized for 65K.

PARITY CHECKING

Both main and control memory are parity-checked. The parity levels are non-addressable and totally under hardware control. A parity error causes an interrupt to a fixed location in main memory.

IMPROVED MEMORY LOCKOUT

The 1108 is able to "Lock-In" contiguous memory areas in each of the four banks, incrementally, in modules of 1024 words, as opposed to the 1107 Lock-In capability of 2048 words. There are several advantages to increased Lockout gradation.

1. Less wastage of available core memory area caused by a program "spilling" into an extra bank. Assignment of smaller memory increments by the executive system allows the memory to accommodate more programs, at a more effective level of usage.

2. Smaller incremental increases actually tend to drive buffer sizes up. Programmers are able to specify larger program buffer areas, but escape being penalized a full 2K when an increase requires a "spill" to another module. This makes for more efficient use of peripherals as ratios of access time (or start-stop time) come down with respect to actual useful transfer time.

3. The executive program itself can be expanded with less percentage of penalty to the system.

ENHANCED REPERTOIRE

Significant improvements, particularly in the arithmetic area, have been incorporated into the repertoire. These include:

FIXED POINT – DOUBLE PRECISION

Double-Precision adds and subtracts operate on full 72-bit operands in accumulators and memory. Bit 2^{71} is the sign-bit. All remaining bits are data or sign-extended bits.

FLOATING POINT

Three modes of Floating Point operation are available. Mode 1 or 2, below, is selected (programmed) according to the contents of the special function register. These use the original 1107 Floating Point commands. Mode 3, below, is an entire new set of full double-precision commands unique to the 1108.

Mode 1 – This is the original 1107 single-precision floating point command. It procures a one-word operand from memory and produces a two-word result in (A), the most significant portion, and (A + 1) the residue or error portion. By accumulating the residue it is possible to determine how much accuracy is being lost in repeated calculations.

Mode 2 – Full single-precision, rounded. Uses the basic floating point word format (sign, 8 bit characteristic, 27 bit mantissa) of the 1107. Operates on a one-word operand from memory. Produces a one-word result, rounded, in the specified A-Register. A + 1 is unaffected by execution. Because it deals with a one-word operand, this instruction executes faster than Mode 1 or 3 and can be used to advantage when great accuracy is not required.

Mode 3 – Full Double-Precision. – Utilizes a two-word operand from memory (U, U + 1) in conjunction with a dual accumulator operand (A, A + 1). Both the mantissa and the characteristic have extended range. (1 bit sign, 11 bit characteristic, 60 bit mantissa).

DOUBLE-OPERAND COMMANDS

The 1108 is able to perform double loads, stores, shifts and has additional commands for packing, unpacking, shifts, scaling, and testing of double-length operands.

LOGICAL INSTRUCTIONS

Masked Alphanumeric Comparison – enables the 1108 to perform logical comparison of words, i.e., bit 35 is regarded as a data-bit rather than a sign-bit. Comparison is performed only on those portions of the word which have corresponding 1-bits in the Mask Register (location 102).

Left Shifts – provides increased flexibility in bit-manipulation. For example, by simple combinations of single-left and double-right shifting, a bit pattern can be expanded or developed with greater facility.

SYSTEM INSTRUCTIONS

Added to the 1108 repertoire are instructions which are designed specifically to enhance the switching speed between operating programs and the executive system. Also, the addition of guard mode renders the executive totally invulnerable to alteration or destruction by programs operating under it.

A new register called the Internal Function Register has been added. This register is not addressable and is dealt with through special instructions.

Load Internal Function Register. – reserved for executive use. Upon executing this instruction, the following conditions are established.

1. Guard mode becomes operative.
2. Memory lockout becomes effective.
3. Carry and overflow designators are set or cleared.
4. Floating point mode (full single or partial double) is selected.
5. Logical memory addresses are assigned.

Items 1 and 2 are implicit in the execution of this instruction. The remainder depend on bit patterns loaded into the register. The only way to capture the IFR is by an interrupt, at which time it is written in register R3 (location 103).

Set Internal Function.— an augmentative instruction to "Load Internal Function." Provided to allow programs to dynamically alter floating point or logical addressing mode.

EXECUTIVE RETURN

This instruction provides for returning control to the executive system by forcing an interrupt. Since an interrupt has occurred, guard mode and memory lockout will not be in effect, and information regarding the mode of the program (the IFR) is captured in register R3 (location 103). If control is to be returned to the same program, its mode can be re-established merely by reloading the contents that were in R3 into the IFR.

The A and U fields of the Executive Return Instruction are not used. Hence, they may contain a variety of codes indicating the purpose of the return.

GUARD MODE

Real-time programming requires considerably more protective philosophy than other applications. The guard mode makes it impossible for a program to inadvertently interfere with the executive system or other programs. It does this by inhibiting the execution of:

I/O instructions
Executive-use instructions
Storage to control memory locations 40-100 (I/O Access-Control words and Real-Time clock)
Storage into locked-out areas (as determined by lockout register)
Program stops or wait for interrupt.

Thus, any mix of programs including debugging runs, can be safely operated with complete assurance of non-interference. If a program should violate one of the provisions of the guard mode, an interrupt to the executive system occurs and the offending program can be removed from the environment.

The above instructions add up to a more powerful development of software concepts through hardware provisions, and a greatly simplified control-exchange and protection system.

INPUT-OUTPUT

ESI (Externally-Specified Index) now equips the 1108 system with full Real-Time communications capability, by providing for the automatic routing and storage of messages being multiplexed into communications-subsystem channels.

A fixed address, provided by the communications subsystem, calls out an access control word which, in turn, routes the message without program intervention. At the end of a message, an ESI-interrupt is generated which gives control to the Real-Time program. Many message buffers may be in the process of being filled at one time, accepting data at the natural rate of the communications devices. The result? Less requirement for expensive I/O buffers and less time required to service individual messages. In effect, each input device is given its own "buffer" in the computer.

Input-Output Channels are now incrementally priced. 8, 12, or 16 channels are available.

PERIPHERAL SUBSYSTEMS

The 1108 will be fully compatible with existing 1107 peripheral subsystems, enabling change-over with a minimum of operational disruption. In addition, an advanced line of peripheral equipment will be available soon to match the high 1108 central-processor speeds.