OPTIONAL INSTRUCTION SET

an option for the
Varian Data Machines 620/f
Computer System

Ma. 2

Specifications Subject to Change Without Notice

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FOREWORD

The 620/f Optional Instruction Set manual defines and explains the logical, electrical, and mechanical parameters that control and interface between a Varian Data Machines 620/f computer and the Instruction Set Option.

The six sections of the manual:

- Introduce the optional instruction set in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware with drawings and parts lists

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SECTION 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

The *620/f Optional Instruction Set (OIS)* is a mainframe option for the Varian Data Machines 620/f computer system. The OIS communicates with the central processing unit (CPU) via the instruction (I) register and the CPU control and decode logic. Primarily, the OIS provides a hardware multiply/divide (M/D) capability that reduces programming steps for multiplication and division subroutines. The OIS also includes control logic for the optional Bit Test (BT) and Skip If Register Equal (SRE) instructions.

The OIS card contains all the circuitry to provide the option, and plugs into the CPU tray which slides into the mainframe of the computer.

Multiplication in the 620/f system consists of successive addition of the multiplicand, with appropriate shifts to the right. Division is accomplished by a magnitude comparison of the divisor and dividend, successive subtractions between the divisor and dividend (if required), and with appropriate left shifts of the partial quotient and partial remainder. Once a program shifts of the partial quotient and partial remainder. When a multiplication or division instruction is implemented, the OIS completes the operation.

When a BT or SRE instruction is implemented, as in the M/D instructions, the OIS controls the sequencing.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers and numbers with a leading zero are octal.

1.2 FUNCTIONAL DESCRIPTION

The OIS is functionally divided into eight sections (figure 1-1). The inputs to the OIS include: 620/f CPU control lines, instruction decodes, data loop signals, etc. The outputs from the OIS include: control and data lines to the 620/f data loop and control circuitry.

1.2.1 BT Control Logic

The BT control logic provides for sequencing control and comparison for the BT instruction. This block decodes the bit of the A or B register to be tested, tests that bit, and provides the appropriate control and enabling signals to the BT-SRE state counter and the CPU control logic.

1.2.2 SRE Control Logic

The SRE Control Logic provides for sequence and control for the SRE instruction. This block decodes the register to be used in the SRE instruction and provides the needed control signals to the BT-SRE state counter and CPU control logic.

1.2.3 BT-SRE State Counter

This counter provides the needed timing states to the SRE and BT control logics. This block also provides control signals to the CPU control logic.

1.2.4 Multiply/Divide Control Logic

The Multiply/Divide Control Logic provides control signals to the multiply and divide state counters, overflow detection logic, and CPU control logic. This section includes the sign bit comparison and storage logic, multiply correction logic, divide correction logic, quotient and product bit storage and control logic, etc.

1.2.5 Multiply State Counter

The Multiply State Counter provides the needed state timing for a multiply instruction, and provides an enable to the Multiply/Divide shift counter.

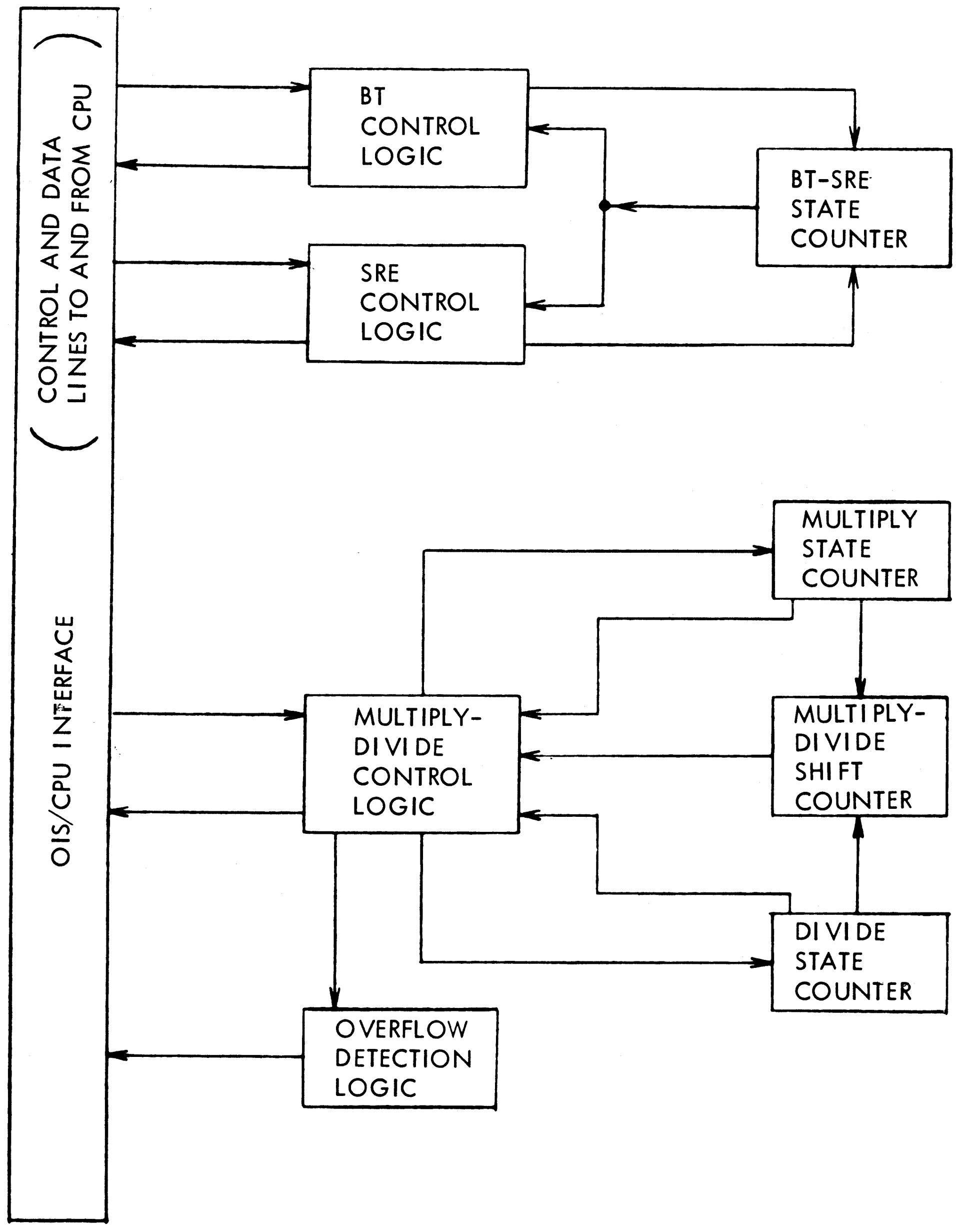

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Figure 1-1. Optional Instruction Set Block Diagram

1.2.6 Divide State Counter

The Divide State Counter provides state timing for a divide instruction. This counter also enables the Multiply/Divide shift counter.

1.2.7 Multiply/Divide Shift Counter

The Multiply/Divide Shift Counter counts the number of shift operations performed during a multiplication or division instruction and provides needed information to the Multiply/Divide control logic.

1.2.8 Overflow Detection Logic

If overflow occurs during a multiplication or division instruction, the overflow detection logic enables the setting of the overflow flip-flop.

1.3 SPECIFICATIONS

The physical, electrical, and operating specifications of the OIS are listed in table 1-1.

Table 1-1. OIS Specifications

Parameter	Description
Multiply Algorithm	R • B + A = A,B where A = initial A register contents B = multiplier in B register R = multiplicand in memory A,B = result in the A and B registers (most significant half in A, least significant half in B) The A register sign bit contains the sign of the product; the B register sign bit is reset to zero

Table 1-1. OIS Specifications

Parameter	Description
Multiply Capability	Maximum multiplier: 32,767 (−32,768) Maximum multiplicand: 32,767 (−32,768) Maximum product: 1,073,741,824 (exceeds the capacity of the A and B registers by one and sets overflow)
Divide Algorithm	A,B / R = B,A where A,B = dividend in the A and B registers (most significant half in A, least significant half in B) R = divisor in memory B,A = result (quotient in the B register, remainder in the A register) The B register sign bit contains the sign of the quotient; the A register sign bit, the sign of the dividend
Divide Capability	Maximum divisor: 37,767 (−32,768) Maximum dividend: 1,073,741,823 (− 1,073,741,824) Maximum quotient: 32,767 (−32,768) A larger quotient sets the overflow indicator

Table 1-1. OIS Specifications *(continued)*

Parameter	Description
SRE Instruction	If A, B, or X = R, skip two memory addresses where A = A register contents B = B register contents X = X register contents R = memory contents Addressing modes: relative to the P register, postindexing with the X or B register, direct, or indirect.
BT Instruction	Test one bit of the A or B register (for zero or one) and jump if the condition is met Addressing modes: direct or indirect
Logic Levels	Positive logic: True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc Negative (interface) logic: True (low): 0.0 to +0.5V dc False (high): +2.4 to +5.5V dc
Size	One 3-by-15-inch (7.7 x 38.1 cm) wired-socket card
Input Power	+5V dc at 0.6 ampere
Interconnection	Plugs into the 620/f CPU motherboard
Operational Environment	0 to 50 degrees C, 10 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

2.1 PHYSICAL DESCRIPTION

The OIS circuitry is on a 3-by-15-inch (7.7 x 38.1 cm) wired-socket card (DM274). This circuit card accommodates up to sixty-four 14-pin, four 16-pin, and one 24-pin dual in-line sockets. (Refer to figure 2-1 and the parts list in section 6.)

2.2 SYSTEM LAYOUT AND PLANNING

The OIS card mounts in slot 4 of the mainframe CPU tray. The CPU tray card slots are numbered 1 through 14, from rear to front, facing the front panel (figure 2-2). CPU tray connectors P1, P2, and P3 mate with connectors J8, J9, and J10, respectively, on the mainframe backplane (part number 44P0430). CPU tray connectors J46 and J47 connect to the front (DM254) display card via flat cables.

2.3 SYSTEM INTERCONNECTION

Card slot 4 of the mainframe CPU tray is the only connector wired for the OIS. This connector allows the OIS to communicate with the CPU control and data signals via the backplane wiring.

2.4 SIGNAL INTERFACE

2.4.1 620/f-OIS Interface

The 620/f-OIS CPU interface signals are listed in table 2-1.

Table 2-1. Interface Signals

Signal Name	Source	Destination	Function
AY00 –	CPU	OIS	The 16 bits (0-15) of the A input to the adder packages
AY01 –	CPU	OIS	
AY02 –	CPU	OIS	
AY03 –	CPU	OIS	
AY04 –	CPU	OIS	
AY05 –	CPU	OIS	
AY06 –	CPU	OIS	
AY07 –	CPU	OIS	
AY08 –	CPU	OIS	
AY09 –	CPU	OIS	
AY10 –	CPU	OIS	
AY11 –	CPU	OIS	
AY12 –	CPU	OIS	
AY13 –	CPU	OIS	
AY14 –	CPU	OIS	
AY15 –	CPU	OIS	
AC1AO –	OIS	CPU	OIS enable to adder controls S1 and S2.
AC2AO –	OIS	CPU	OIS enable to adder controls S3 and S4.
AEQB	CPU	OIS	The A input to the adder is equal to the B input to the adder.
ALC –	CPU	OIS	110 nanoseconds CPU clock signal.
A15	CPU	OIS	Output of the A register bit 15.
BREGO	CPU	OIS	The contents of the B register equal zero.
B000	CPU	OIS	Output of B register bit 0.

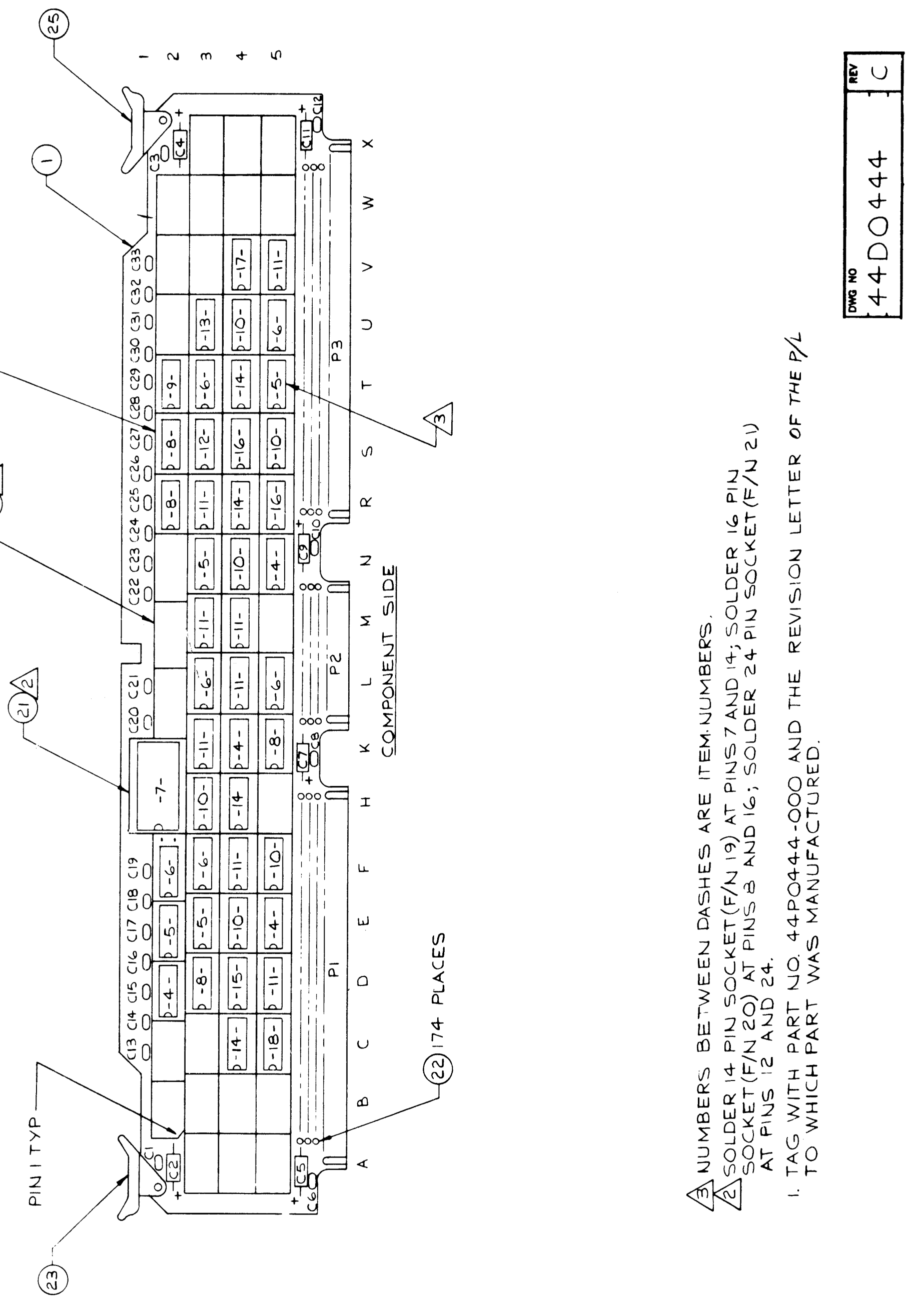

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Figure 2-1. Component Board Layout

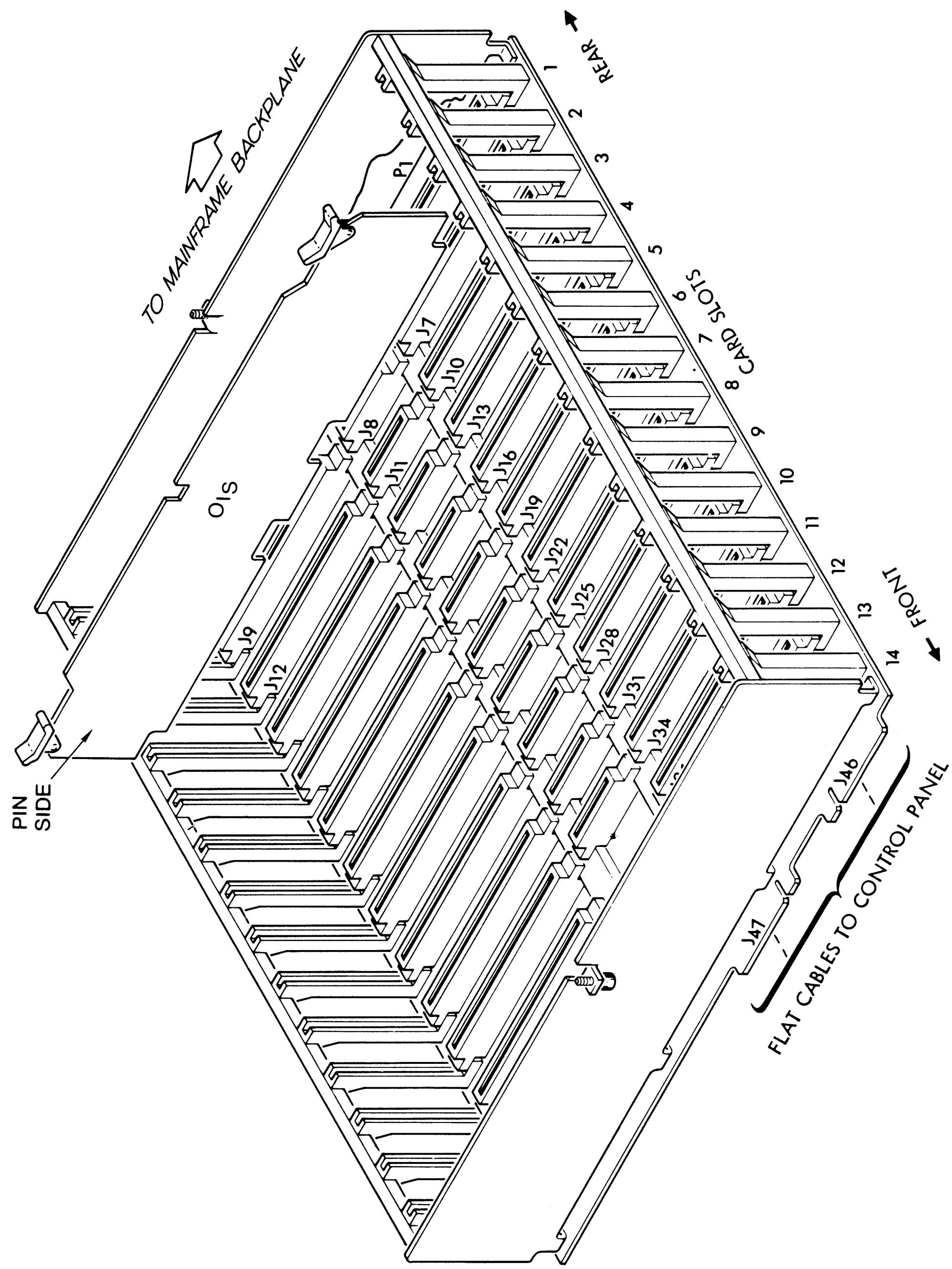

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Figure 2-2. OIS Card Location

Table 2-1. Interface Signals *(continued)*

Signal Name	Source	Destination	Function
B14O +	CPU	OIS	Output of B register bit 14.
B15O −	CPU	OIS	Inverted output of B register bit 15.
CB15 −	CPU	OIS	Bit 15 of the C-bus.
DIV −	CPU	OIS	Decode for divide instruction.
DSC1 −	OIS	CPU	Divide state counter flip-flop.
EAAO −	OIS	CPU	Low for clock A register.
EAXAO −	OIS	CPU	Low to gate the A register to AYXX − adder inputs.
EBAO −	OIS	CPU	Low for clock B register.
EBT −	CPU	OIS	Decode for BT instruction.
EBXAO −	OIS	CPU	Low to gate the B register to AYXX − adder inputs.
EN1BO −	OIS	CPU	Enable setting of B register bit 0.
EPXAO −	OIS	CPU	Low to gate the P register to AYXX − adder inputs.
EXXSK −	OIS	CPU	Low to gate the X register to AYXX − adder inputs.
FINAO −	OIS	CPU	Exit term for setting CPU timing flip-flop IFC.

Table 2-1. Interface Signals *(continued)*

Signal Name	Source	Destination	Function
IF2 –	CPU	OIS	220-nanosecond processing portion of instruction fetch cycle.
INTX –	CPU	OIS	Low indicates that the current instruction is an interrupt address.
I00O +	CPU	OIS	I register outputs.
I01O +	CPU	OIS	
I02O +	CPU	OIS	
I03O +	CPU	OIS	
I04O +	CPU	OIS	
I05O +	CPU	OIS	
I05O –	CPU	OIS	
MDEAB –	OIS	CPU	Enables the C bus to the A and B register inputs.
MDIMP –	OIS	CPU	OIS installed signal.
MSC1	OIS	CPU	Multiply state counter flip-flop 1.
MUL –	CPU	OIS	Decode for multiply instruction (active low).
MUL3 –	OIS	CPU	Multiply A register bit 15 input enable.
OF4	CPU	OIS	The three operand fetch (OFF) timing states.
OF5	CPU	OIS	
OF5 –	CPU	OIS	
OF6	CPU	OIS	
OPOF –	OIS	CPU	Active low overflow detect to enable overflow flip-flop.

Table 2-1. Interface Signals *(continued)*

Signal Name	Source	Destination	Function
OPTEL –	OIS	CPU	Enable the clock to the L register (active low)
OPTEP –	OIS	CPU	Enable the clock to the P register (active low)
OSAFC –	OIS	CPU	Enable setting of AFC flip-flop (active low)
RST –	CPU	OIS	System reset.
R15 –	CPU	OIS	R register bit 15 (active low)

2.4.2 OIS Logic Levels

Positive logic levels:

True (high)	=	+2.4 to +5.5V dc
False (low)	=	0.0 to +0.5V dc

Negative logic levels:

True (low)	=	0.0 to +0.5V dc
False (high)	=	+2.4 to +5.5V dc

SECTION 3
OPERATION

There are no operating controls or indicators on the OIS card. The OIS is completely under software control.

SECTION 4 THEORY OF OPERATION

The operation of the OIS is described as a series of sequences that exercise the option. As an aid to understanding the following descriptions, refer to figure 4-1, the mnemonics in section 4-5, the specifications in table 1-1, and the OIS logic diagram (section 6, drawing 91D0212). In the following, three-digit numbers in parentheses indicate the chip location on the logic diagram. The first number calls out the sheet; the following letter and number, the chip location on the OIS circuit card.

Signal mnemonic levels, referred to in the theory of operation, are the levels of the signals at their point of origin or entry into the OIS. Stages of inversion are disregarded for the purpose of clarity. Signals resulting from the outputs of flip-flops are designated FF set and FF reset if they are high when the flip-flop is set or reset, respectively. J-K flip-flops (74H108) are negative-going edge-triggered; D flip-flops (74H74) are positive-going edge-triggered.

The number in parentheses after each section title references the functional block of figure 4-1.

The Texas Instruments 74150 multiplexer chip (1H2) selects one of 16 (or one of eight) data sources. It serves as a five-variable-function generator that performs parallel-to-serial conversion. The multiplexer contains inverter/drivers to supply fully complementary, on-chip, binary-decoding data selection to the AND/OR inverter gate. The 74150 has a strobe input, which, when low, enables the selected function.

4.1 BIT TEST (BT) CONTROL LOGIC (1, 3)

Figure 4-2 illustrates the successful execution of a BT instruction by a given bit in the A or B register being tested for an expected high or low. Assume in figure 4-2 that the instruction was loaded into the I register and then decoded as a BT instruction.

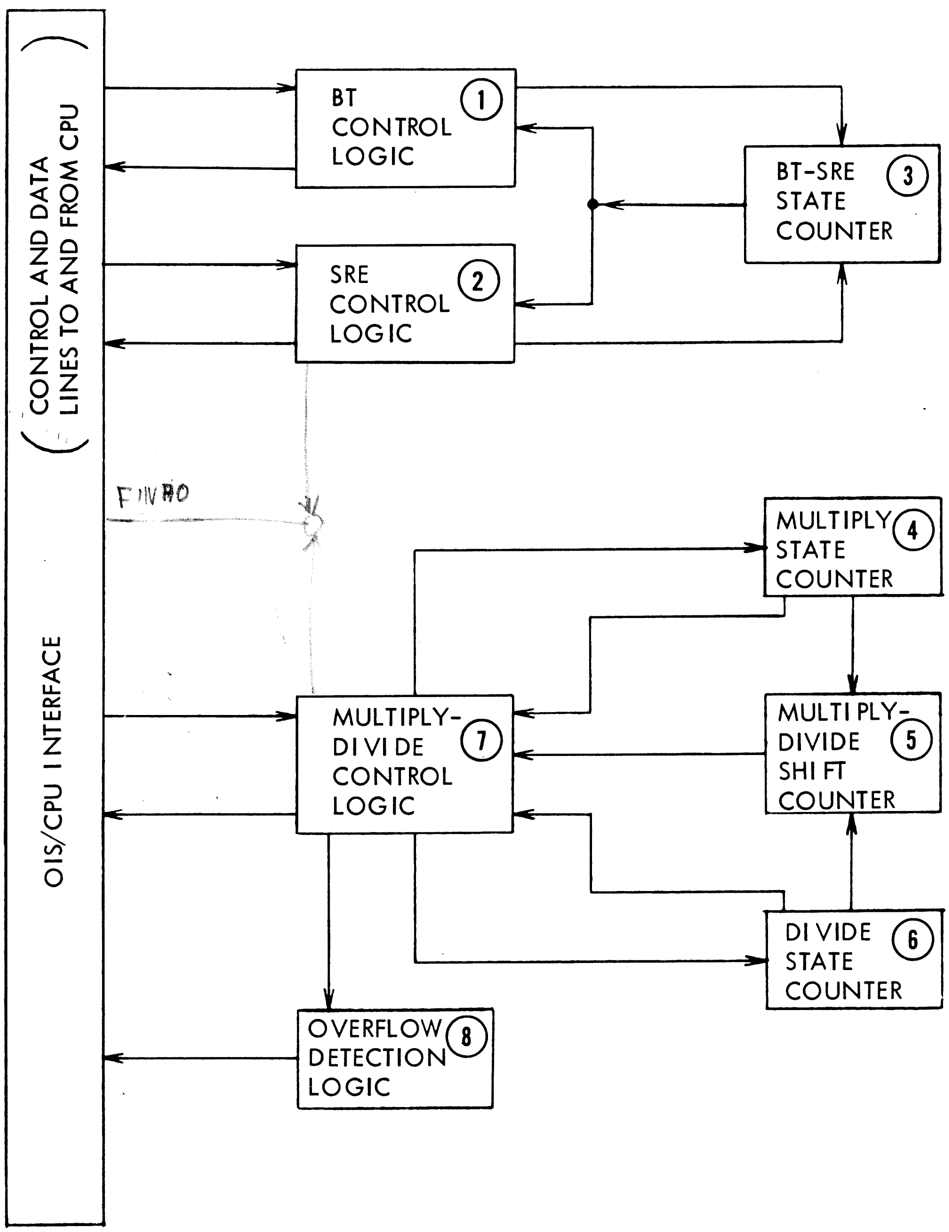

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Figure 4-1. Functional Block Diagram

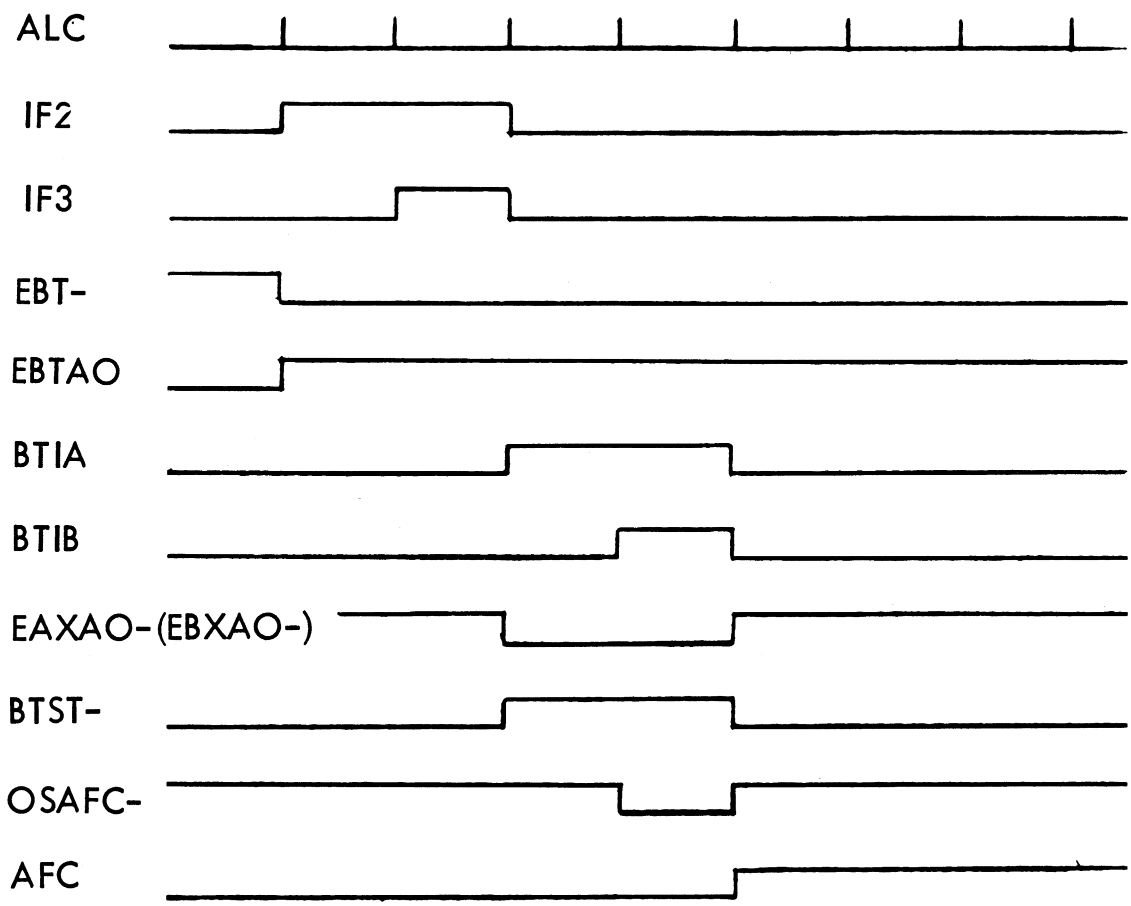

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Figure 4-2. BT Timing, Condition Met

At the leading edge of IF2 (from the CPU), the BT instruction is decoded to enable EBTAO high (1T3). BT1A (3V5) set output goes high on the trailing edge of IF3. At the same time, the register being tested is enabled to adder inputs AY00 through AY14 (1H2) via EAXAO – or EBXAO – low. The condition (high or low)of the selected bit of the A or B register is tested, and BTST – (1N3) is enabled high. Next, the BT1B flip-flop (3V5) is set to enable OSAFC – low to set the AFC flip-flop (drawing 91D0217, 2M4) in the CPU. On the next system clock (ALC), the BT1A and BT1B flip-flops are reset. The CPU then executes an address-fetching cycle (AFC) to enable the jump address.

Figure 4-3 illustrates an unsuccessful execution of the BT instruction (i.e., the selected bit in the selected register is in error. Assume in figure 4-3 that the instruction is loaded in the I register.

The timing for this function is identical to that illustrated in figure 4-2 to the trailing edge of BT1B. SKIP1 – (3T5) and reset output EPXAO – of the SRE1 flip-flop are enabled low for incrementing the P register through the adder. SRE2 sets, and the P and L register clocks are enabled by OPTEP – (2C5) and OPTEL – (2C5) low. Also, exit signal FINAO – goes low at this time. On the trailing edge SRE2, the incremented P register value is loaded in the L and P registers, and CPU timing flip-flop IFC (drawing 91D0217, 1M5) sets. The CPU then fetches the next instruction from memory.

4.2 SKIP IF REGISTER EQUAL (SRE) CONTROL LOGIC

Figure 4-4 shows the timing for an SRE instruction when the skip condition is met by either the A, B or X register contents equaling the operand (R register contents) and the next two memory addresses are to be skipped. Assume that the SRE instruction is loaded in the I register.

After the CPU decodes the SRE instruction, operand fetch flip-flop OFF (drawing 91D0217 2E2) sets and the operand is loaded in the R register. This occurs during OF4.

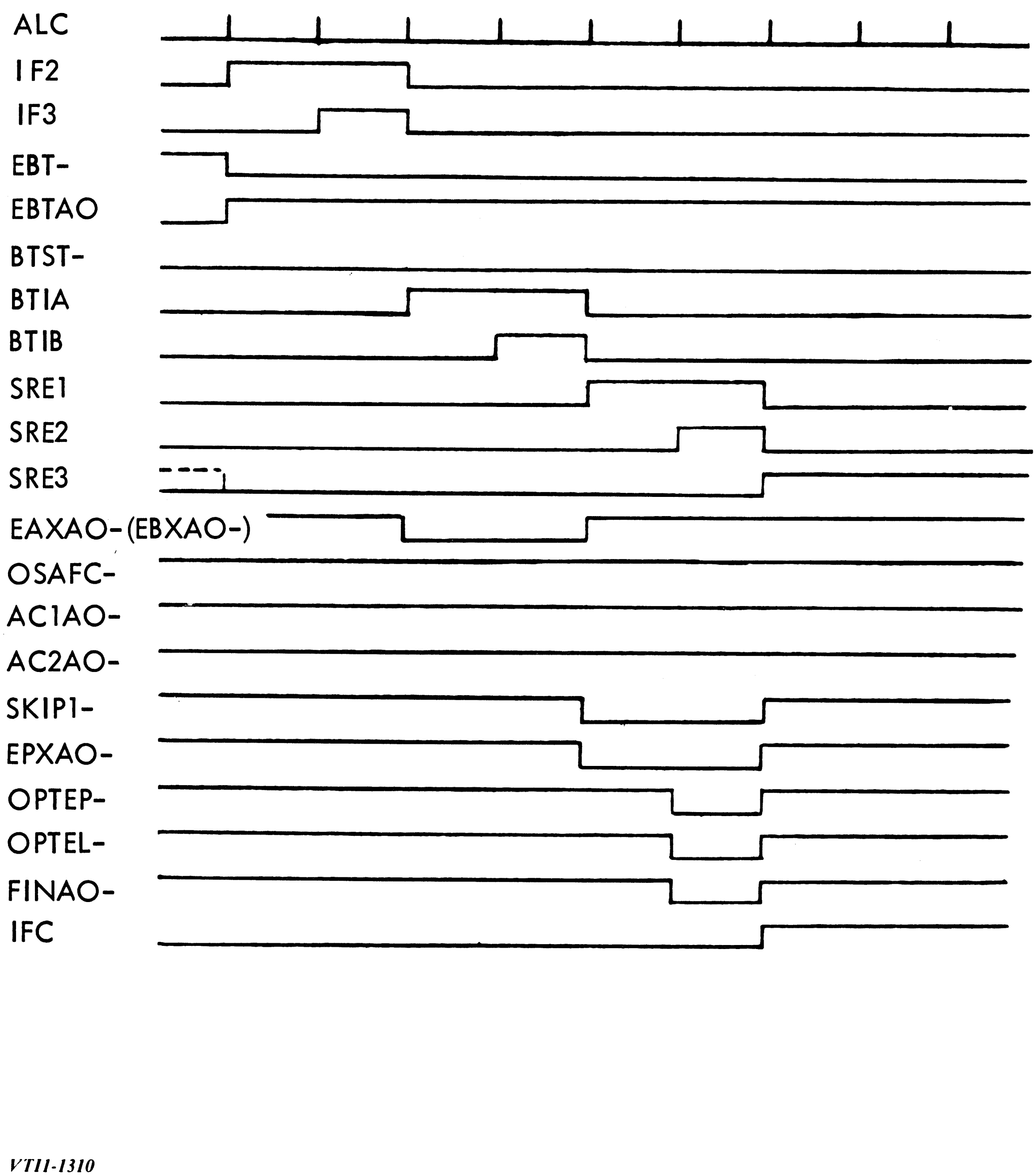

Figure 4-3. BT Timing, Condition Not Met

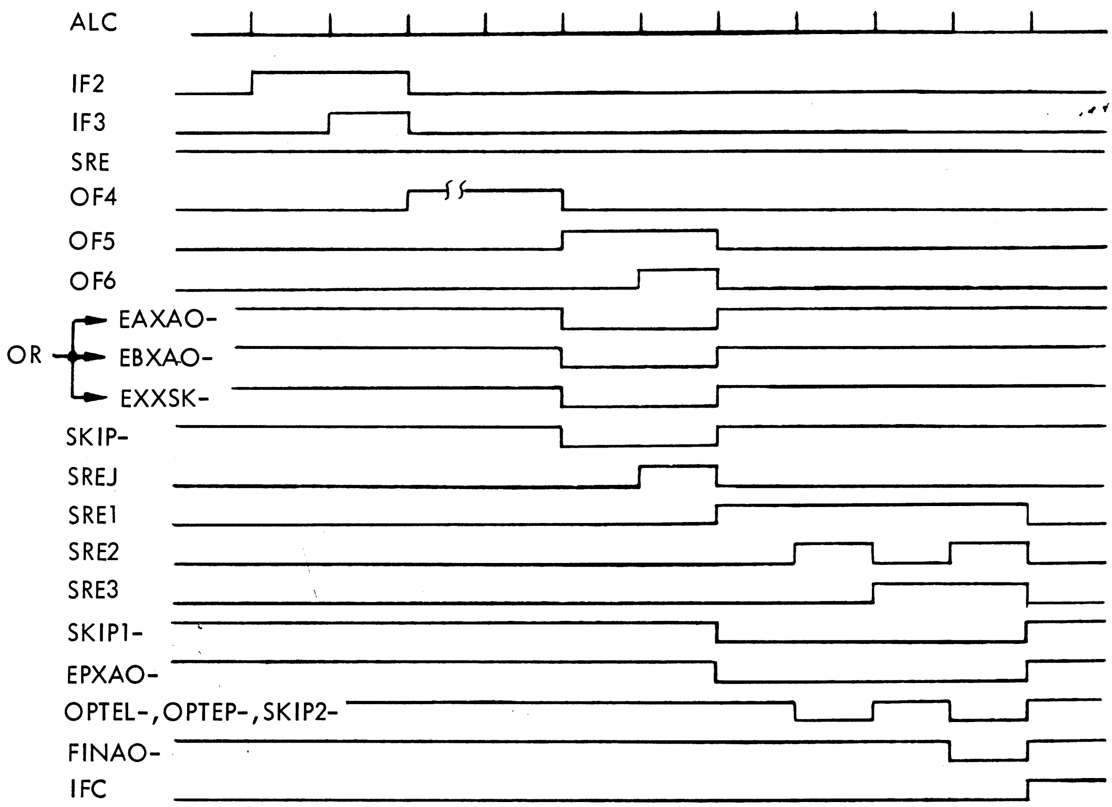

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Figure 4-4. SRE Timing, Condition Met

On the leading edge of OF5, the register to be compared with the operand is enabled via EAXAO –, EBXAO –, or EXXSK – low to the adder inputs (AY00 through AY14). The R register contents are then compared to the contents of the register to be tested. If the SRE instruction is successfully executed, the tested register is equal to the operand; the adder inputs are thus equal, making SEQB high (from the CPU) and enabling SKIP – (2F2) low to disable the setting of CPU timing flip-flop IFC (drawing 91D0217, 1M5). This inhibits the fetching and execution of the next instruction in memory.

OF6, SRE, and AEQB high (2R2) produce SREJ1 – low to enable the BT-SRE state counter to set SREJ high. On the trailing edge of OF6, BT-SRE state counter flip-flop 1 (SRE) is set (2F4). SRE1 set initiates the skipping of two memory addresses. With SRE1 enabled, the adder control lines (SKIP1 – low) are set for an incrementation, and the P register is enabled to the adder with EPXAO – low. SRE2 (2F2) then goes high, enabling the clocks to the P and L registers via OPTEF – and OPTEL – low. The P and L registers are incremented by one on the trailing edge of SRE2. SRE3 sets and the next ALCAO clock sets SRE2 a second time. With SRE2 and SRE3 high, exit signal FINAO – (1F5) goes low. On the trailing edge of SRE2 and SRE3, the P and L registers are incremented for the second time, and the IFC flip-flop sets. The instruction at the incremented address is then loaded in the I register to end the SRE instruction sequence.

Figure 4-5 shows the timing of an SRE instruction during which the tested register does not equal the operand and skipping does not occur.

The unsuccessful SRE operation is basically the same as that of a successfully executed instruction in which the equality of the A, B, or X register contents and the operand occurs, except that SKIP – does not set and the BT-SRE counter is not enabled. Instead, the IFC flip-flop sets on the trailing edge of OF6.

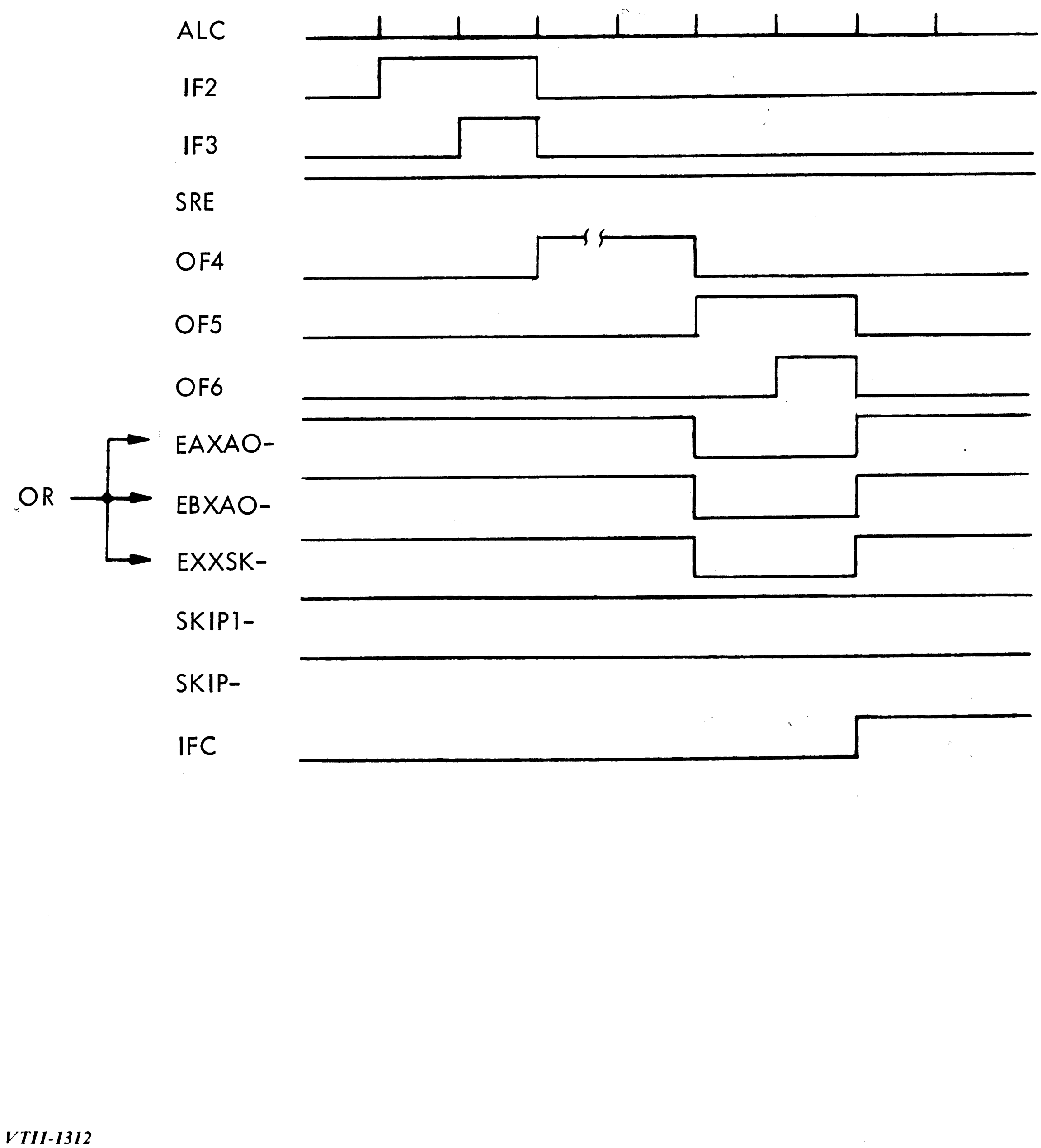

Figure 4-5. SRE Timing, Condition Not Met

4.3 MULTIPLICATION

4.3.1 Algorithm Summary

The OIS multiplication algorithm is:

$$R \cdot B + A = A,B$$

where

A	=	initial A register contents
B	=	multiplier in B register
R	=	multiplicand in memory
A,B	=	result in A and B registers

During multiplication, the contents of the effective memory address are multiplied by the contents of the B register, then the A register contents are added to the product. The result is placed in the A and B registers, with the most significant half in the A register and the least significant half in the B register. The sign of the result is in bit 15 (sign bit) of the A register. The B register sign bit is always set to zero. The largest positive multiplier or multiplicand in an operating register in the CPU is thus 15 binary bits.

The maximum product of the largest positive multiplier and multiplicand is 1,073,676,289. Since the combined capacity of the A and B registers is 1,073,741,823, this product does not set the overflow indicator.

The maximum product of the largest negative multiplier and multiplicand is – 1,073,741,824, one greater than the combined A and B register capacity. In this case, the overflow indicator sets and the combined A and B registers indicate a product of – 1,073,741,824. This is the only case in which multiplication alone causes setting of the overflow indicator.

The multiplication algorithm is structured so that if the multiplier is a negative number, an internal correction is performed on the product. This correction subtracts the multiplicand from the product as follows:

$$\text{corrected product} = (P) - (R)$$

The OIS provides this correction, and no software is required.

4.3.2 Logic and Timing (4, 5, 7)

Figure 4-6 shows the timing of a Multiplication (MUL) instruction using direct addressing. Assume that the CPU is initialized, the instruction is loaded in the I register, and the instruction is decoded. Assume also that the multiplier is negative (correction required), the multiplicand is positive, and overflow does not occur. The timing is basically the same for any type of multiplication instruction (i.e., MUL, MULI, and MULE).

During CPU timing state OF4, the OIS stores the sign of the multiplier (B register, bit 15) in sign bit storage flip-flop SGNB (2R5). In the present case, SGNB is set (B is negative).

After OF4 and on entry to CPU state OF5, the multiply-state counter flip-flops (2K3, 2L4) are enabled (MSC1, MSC2, and MSC3). MSC2 sets on the leading edge of OF6. The A register is enabled to the adder via EAXAO − (1S3) low. Adder control lines AC1AO − (1N4) and AC2AO − (1U4) and SKIP1 − (3T5) go low for an addition operation. The A register contents on the AYxx − adder inputs and the R register contents (multiplicand) on the AZxx − adder inputs are added. The sum is enabled by MDEAB − (3E4) low to the inputs of the A and B registers via the C bus. MSC3 sets, and, if the multiplier's least significant bit (LSB) is one, EAAO − (3U4) low enables the A register clock. Also, on the trailing edge of MSC3, the data on the C bus are clocked into the upper half of the accumulator (A register) by ALC. If the B register's LSB is not one, EAAO − remains high, and clocking does not occur at the A register.

Next, MSC1 sets as MSC2 and MSC3 reset. When MSC1 is entered, EMOLD low is enabled for a right-shift operation. SC1 also enables the .multiply/divide shift counter (2M3, 2L4) when the clocks to the A and B registers are enabled by EAAO − (3U4) and EBAO − (3T5) low. The sign of the partial product is stored in the MUL3 − flip-flop (3S4). On the trailing edge of MSC1, the A and B registers are clocked by ALC and the contents shifted one bit to the right. The multiply/divide shift counter is also incremented.

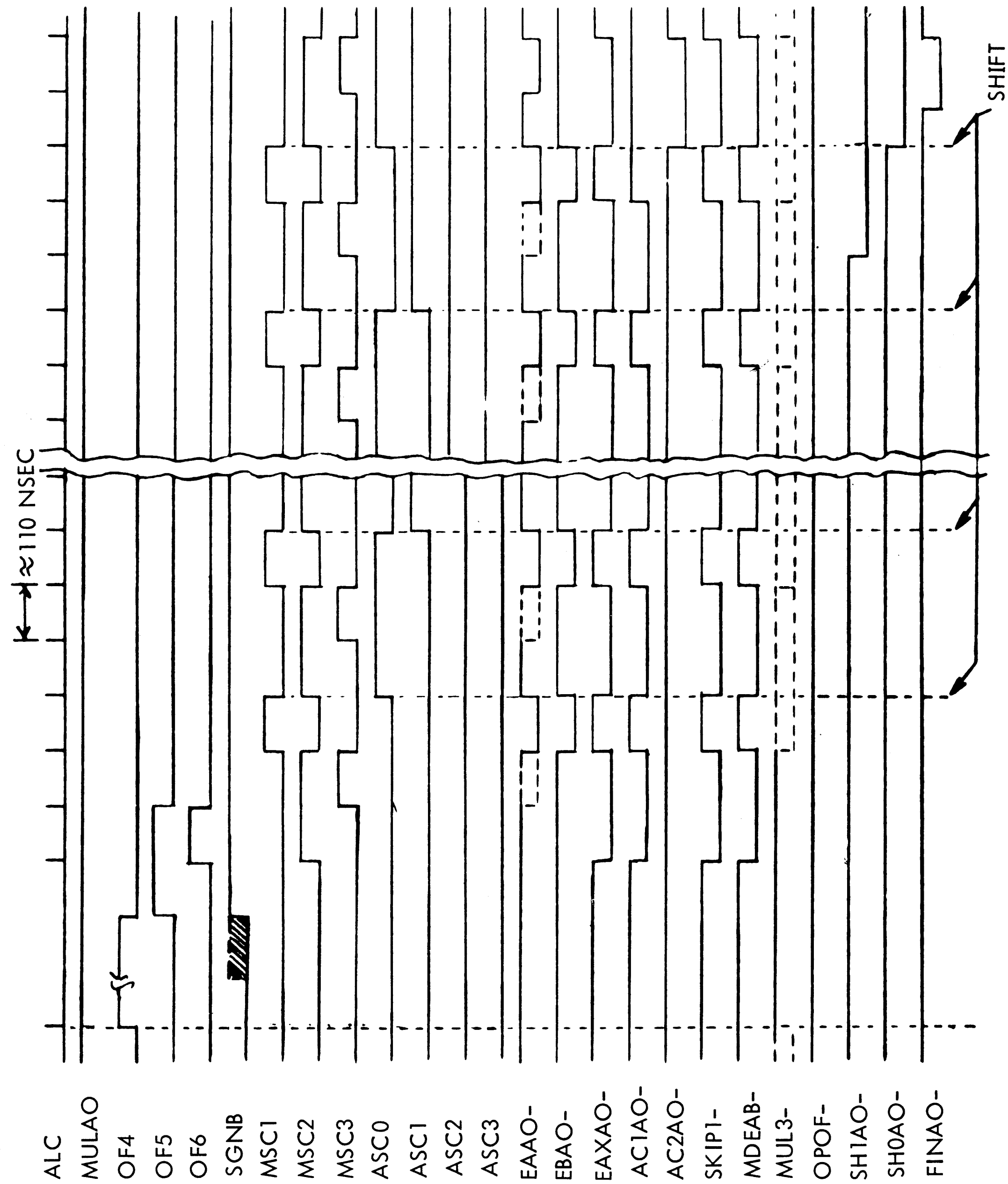

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Figure 4-6. Multiplication Timing

MSC2 again sets and AC1AO –, AC2AO –, and SKIP1 – set for a second addition of the A and R registers. The sum is clocked into the A register as a partial product if the B register's LSB is one. A second shift operation then occurs as described above. This process (adding the A and R registers, clocking the A register if required, incrementing the multiply/divide shift counter, and right-shifting the result) continues until SHOAO (2K4) sets.

The correction phase is entered with MSC2 and SH0AO high. AC1AO –, AC2AO –, and SKIP1 – set for a subtraction operation. The contents of the R register are subtracted from the product in the A register. This sequence occurs even though the multiplier (in the B register) is negative. MSC3 then sets, and, because the multiplier is negative, a correction is required. The correction is performed when the result of the above-described subtraction is clocked into the A register by EAAO – low. If the correction is not required, clocking does not occur. Also, during MSC3, IFC flip-flop enabling signal FINAO – (1F5) goes low and IFC sets on the next ALC. The next instruction is then fetched to end the multiplication sequence.

4.3.3 Overflow Detection (8)

Overflow detection during a multiplication operation occurs during SH0AO. If the multiplier (SGNB) and multiplicand (R15A) are both negative (high), they produce MOFX (1K4) high, which is ANDed (1D4) with the result of the subtraction during SH0AO and MSC2 (both high). If the result is negative (CB15A high), MOF – goes low to product OPOF – low and set the overflow flip-flop (drawing 91D0218, 2R3) on the control II card of the CPU.

4.4 DIVISION

4.4.1 Algorithm Summary

The division algorithm is:

$$A,B \ / \ R = B,A$$

where

A,B	=	dividend in A and B registers
R	=	divisor in memory
B,A	=	result (quotient in B register, remainder in A register)

The dividend is contained in the combined A and B registers with the sign in bit 15 of the A register. The B register sign bit is not used. The divisor is in the effective memory address. The quotient and its sign are placed in the B register, and the remainder (with the sign of the dividend), in the A register. If the quotient exceeds the capacity of the B register (+32,767 or −32,768), the overflow indicator sets.

Internal corrections are performed on the division result if one of the following occurs:

a. The quotient is negative (one's complement correction)

−37 / 40

The dividend is negative and an integer multiple of the divisor (negative dividend-integral divide correction)

−15 / 5

These corrections are hardware-implemented and require no software correction.

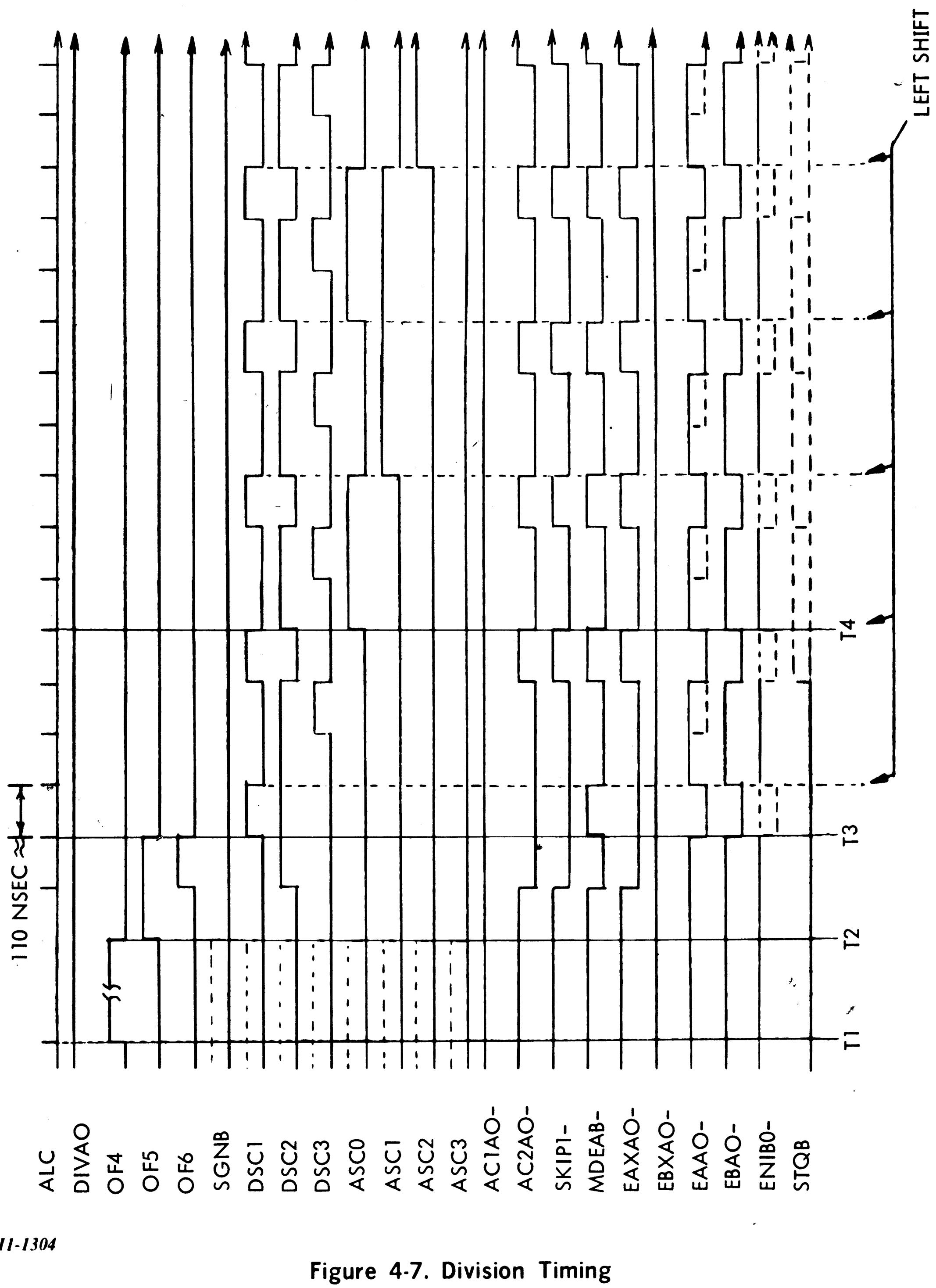
4.4.2 Logic and Timing (5, 6, 7)

Figure 4-7 illustrates the timing of a typical division operation. Assume that correction is not required and that overflow does not occur. The following example shows a division that satisfies the conditions described above:

Decimal	**Octal**
80 / 40 = 2	0120 / 050 = 02

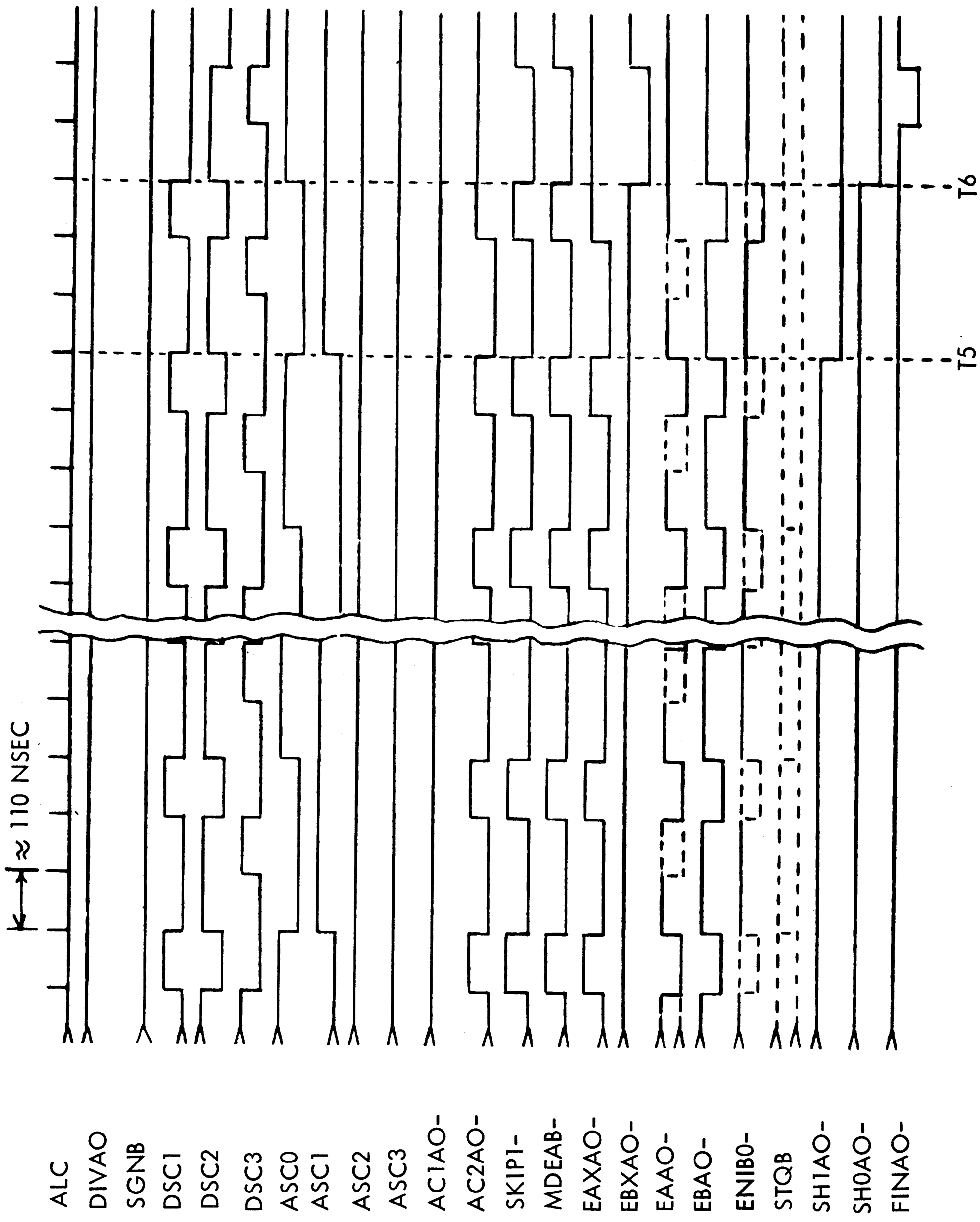
Before execution:

A register	=	000000
B register	=	000120
R register	=	000050



VT11-1304

Figure 4-7. Division Timing



VTII-1305

Figure 4-7. Division Timing *(continued)*

After execution:

A register	=	000000
B register	=	000002
R register	=	000050

Assume also that the instruction is loaded in the I register and is already decoded as a division operation (DIVAO):

Dividend Sign A15	Divisor Sign R15	Adder Control Lines AC1AO	AC2AO	Function
0	0	1	0	SUB (A − R)
0	1	0	1	ADD [A + (− R)]
1	0	0	1	ADD (− A + R)
1	1	1	0	SUB [− A − (− R)]

The above operation includes a magnitude comparison of the A and R registers to set the adder control lines for the proper sequence of operations (addition or subtraction) and to prepare for overflow detection.

The A register is enabled to the adder inputs via EAXAO (1S3) low, and a trial subtraction is performed between the A and R registers to test for overflow (section 4.4.3)

DSC1 then sets, the dividend sign (A15) and divisor sign (R15) are compared, and the resulting quotient sign bit is enabled to the B register's LSB via EN1BO − (1F5) low. Also, during DSC1, the A and B registers are enabled via EAAO − (3U4) and EBAO − (3T5) low for a left-shift operation.

On the trailing edge of DSC1, the A and B registers are shifted one bit to the left and the quotient sign bit is stored in bit 0 of the B register.

The OIS again enters the timing state in which DSC1 is low, DSC2 is high, and DSC3 is low. A second trial subtraction is performed between the A and R registers; the result is enabled by MDEAB – low (on the C bus) to the A register inputs. DSC3 then sets with DSC1 low and DSC2 high. If the result of the trial subtraction is that SGNB (dividend sign) and CB15 (partial remainder sign) are equal, the A register clock is enabled by EAAO – low:

SGNB	CB15	SG*CB	EAAO
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

where

SGNB	=	dividend sign bit
CB15	=	partial remainder sign bit
SG*CB	=	exclusive-AND of SGNB and CB15
EAAO	=	A register clock enable

During DSC3, the divisor sign (R register, bit 15) and the partial remainder sign (C bus, bit 15) are compared and the resulting quotient bit is enabled by STQBD (2D2) to store quotient bit flip-flop STQB (2R5).

R15	CB15	R*CB	STQBD
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

where

R15	=	divisor sign bit
CB15	=	partial remainder sign bit
R*CB	=	exclusive-AND of R15 and CB15
STQBD	=	input to STQB flip-flop

The OIS again enters DSC1 (DSC2 and DSC3 low). The A and B registers are enabled for a second left-shift with EAAO – and EBAO – low. ASCO, ASC1, ASC2, and ASC3 (2L4, 2M3, 2R3) are enabled by DISCR – low when DSC1 and DSC2 – (T3) are high. During this time also, the quotient bit stored in STQB (2R5) is enabled by EN1BO – (1F5) low to the B register LSB. On the trailing edge of DSC1, the A and B register contents are left-shifted one bit, the quotient bit is stored in bit 0 of the B register, and the multiply/divide state counter is incremented by one.

The process of trial subtraction, loading the results if required, left-shifting, quotient bit storage, and incrementation of the shift counter continues until SHOAO (figure 4-7).

The last subtraction, comparison, and left-shift operation occur when the OIS enters SH1AO. Also during SH1AO, the negative dividend/integral divide correction is actuated (if required). No correction is required in the examples of figure 4-7, as described below.

During SHOAO, adder control lines AC1AO –, AC2AO –, and SKIP1 – set for an incrementation, and the B register is enabled to the adder inputs by EBXAO – (1E3) low. If correction is required, the B register is incremented by EBAO – (3T5) low. Also during SHOAO, exit signal FINAO – is enabled, and, on the trailing edge of DSC3, the CPU exits the division routine and is readied by IFC set (drawing 91D0217, 1M5) to fetch the next instruction.

The timing illustrated in figure 4-7 remains basically the same for any division operation (i.e., DIV, DIVI, and DIVE).

4.4.3 Overflow Detection (8)

Typical timing for division overflow detection is shown in figure 4-8. Conditions that cause overflow are tested for during OIS timing of DSC1 (2M4) high, DSC2 (2M4) high, and DSC3 (2R3) low (the divide state counter). The conditions of overflow are:

a. The dividend is equal to the divisor:

DOF1 = BREGO · AEQB · DSC2A · DSC1

where

DOF1	=	division overflow path 1
BREGO	=	B register equal to zero
AEQB	=	A register equal to R register

b. The dividend is larger than the divisor:

DOF2 = SG*CB · DSC2 · DSC1

where

SGNB	CB15A	SG*CB	DOF2
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

and

SGNB	=	dividend sign bit
CB15A	=	partial remainder sign bit
SG*CB	=	exclusive-AND of SGNB and CB15A
DOF2	=	division overflow path 2

If overflow occurs, the overflow flip-flop is set by OPOF − (1E3) low on the trailing edge of DSC1. The division operation, using the contents of the A, B, and R registers, is performed even if overflow occurs.

A user-written program detects overflow and provides the needed program action.

4.4.4 One's Complement Correction

The timing of a one's complement correction operation is shown in figure 4-9. This correction is required if the quotient is negative. At T6, adder control lines AC1AO −, AC2AO −, and SKIP1 − set for an incrementation, and the B register is enabled by EBXAO − (1E3) low to the adder input.

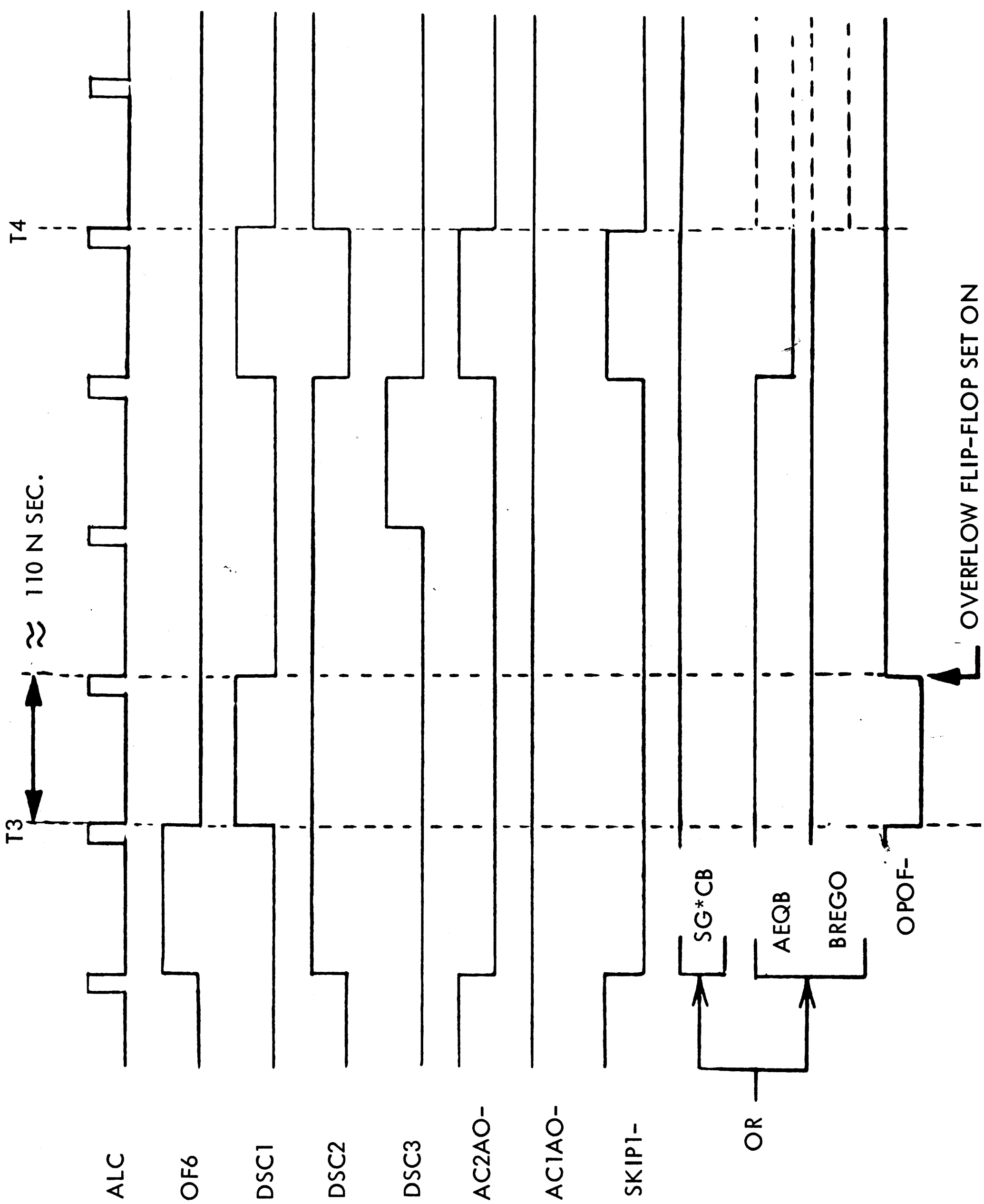


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Figure 4-8. Division Overflow Timing

A correction is detected at the same time, and DIVCOR (1F2) is high. This produces DVCOR – low to enable EBAO – low, which, in turn, enables the B register clock. This occurs when DSC3 is entered (DSC1 low, DSC2, and DSC3 high). Exit signal FINAO – also goes low. On the trailing edge of DSC3, the B register is incremented by one, and the IFC flip-flop sets to fetch the next instruction.

4.4.5 Negative Dividend-Integral Division Correction

Figure 4-10 illustrates timing of a negative dividend-integral division operation. This correction is required if the dividend is negative and an integer multiple of the divisor; for example:

10 / 2 = 5 and no remainder

Because of the structure of the division algorithm, the A register is cleared of erroneous partial remainders. This is accomplished during SH1AO. When DSC3 is set during SH1AO, clear A register signal CLRAR (3T5) goes high to enable the A register clock via EAAO – (3U4) low. During DSC3 also, the C bus is disabled from the A register inputs. On the trailing edge of DSC3, the A register is cleared to zero. The remainder of the timing is the same as shown in figure 4-9.

4.5 MNEMONICS

The mnemonics used in the OIS are listed alphabetically in table 4-1. A brief description of each signal's function is given in the description column; an asterisk in this column indicates that the mnemonic description is given in table 2-1 above. The source column lists the sheet numbers and chip locations on the OIS logic diagram (section 6).

Table 4-1. OIS Mnemonics

Mnemonic	Source		Description
	Sheet and Chip No.		
AC1AO –	1	N04-006	*
AC2AO –	1	U04-006	*
AEQB	2	P03-028	*

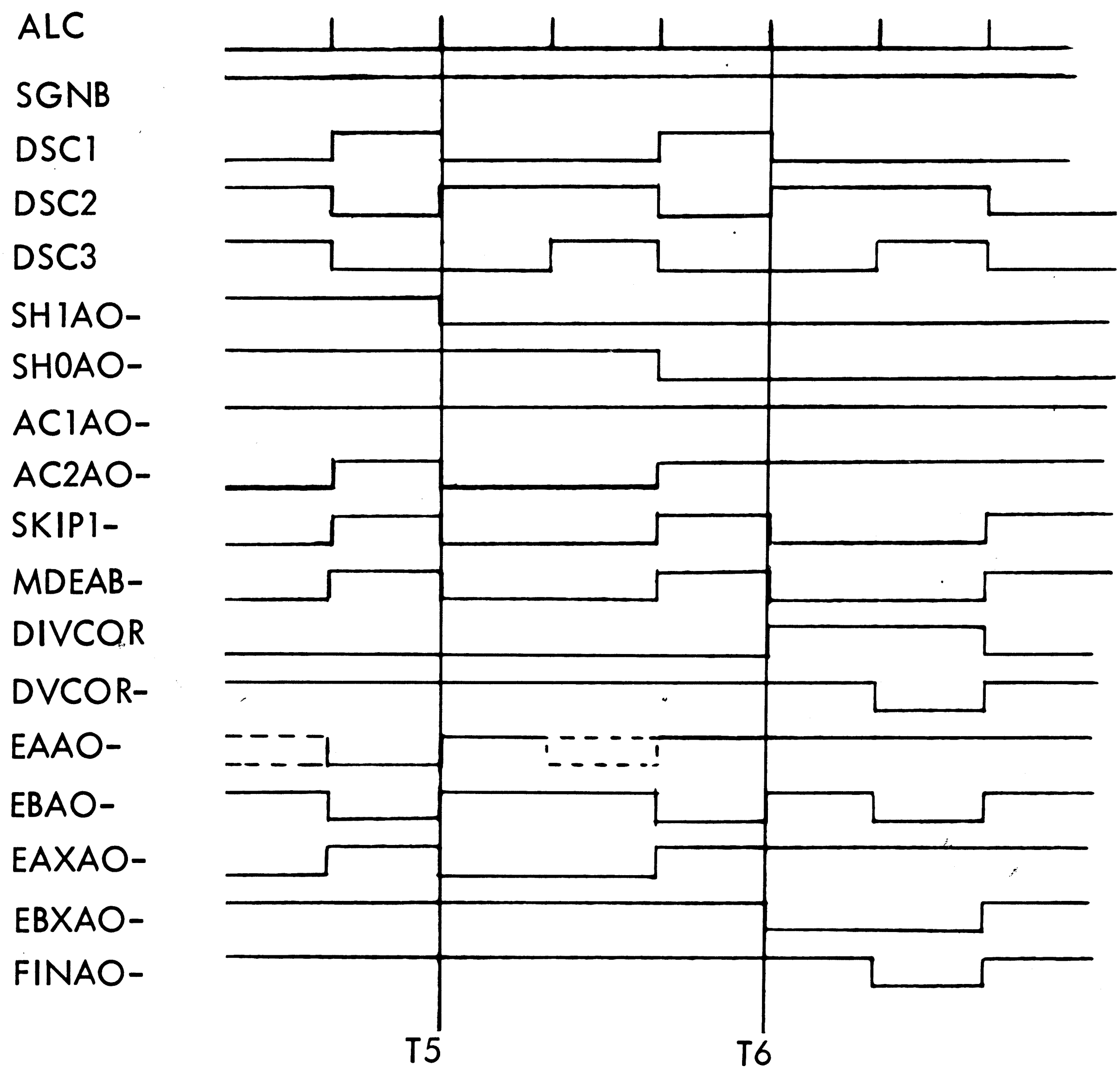

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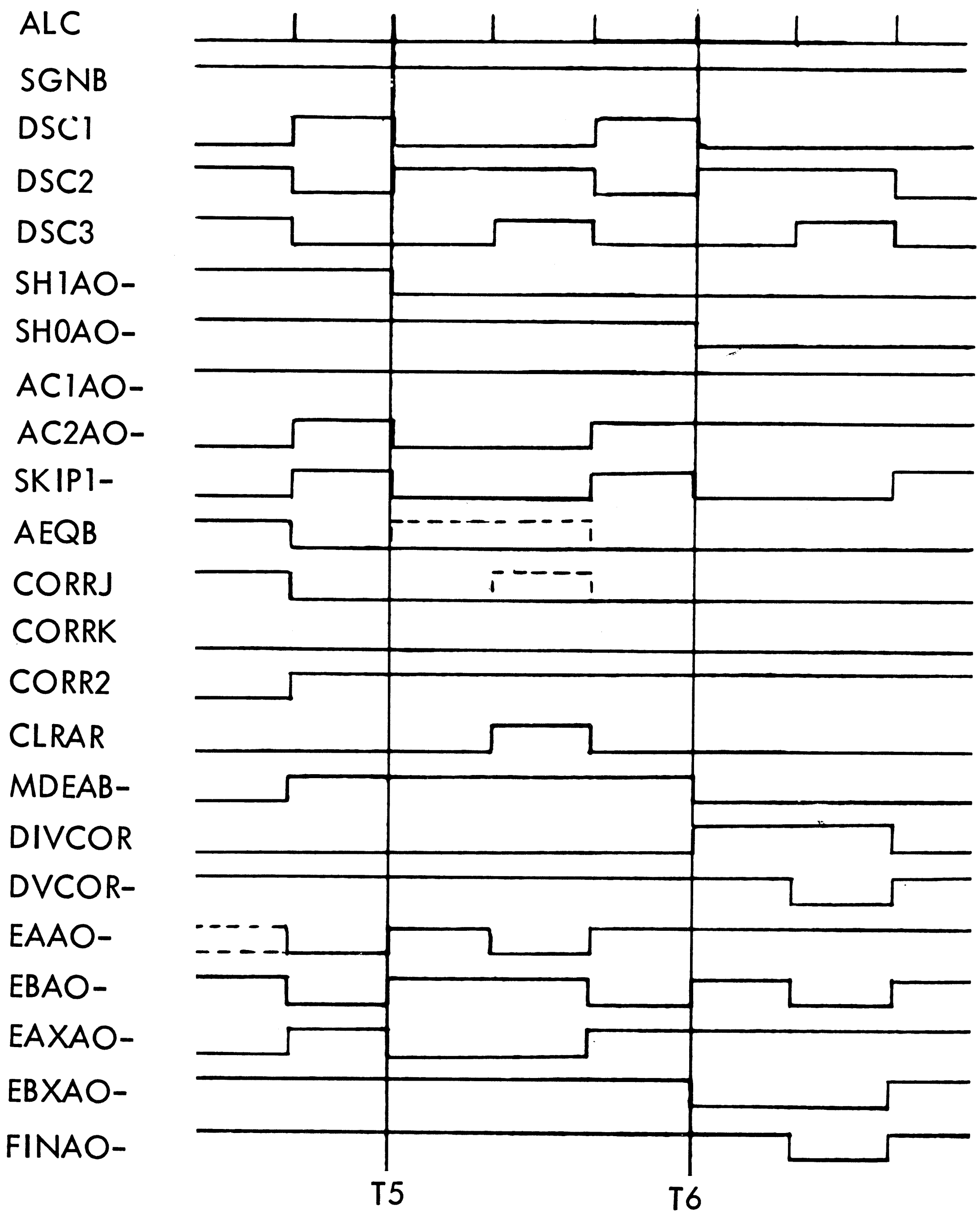
Figure 4-9. One's Complement Correction Timing



VT11-1308

Figure 4-10. Negative Dividend-Integral Division Timing

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
ALC –	2	P03-072	*
ALCAO	2	V04-006	Clocks the MULT/DIVIDE shift and state counters.
ALCAO –	2	T04-012	Inverted from ALCAO to clock the store quotient flip-flop.
ALCAO1	2	S02-008	Clocks the bit and SRE state counter.
ASCO	2	R03-006	Set output of start flip-flop for MULT/DIVIDE shift counter.
ASCOJK	2	T03-006	ORed output of MSC1- and DISCR-.
ASC1	2	M03-002	Set output of MULT/DIVIDE shift counter flip-flop.
ASC1JK	2	N05-011	ANDed output of ASCOJK and ASCO.
ASC2	2	M03-006	Set output of MULT/DIVIDE shift counter flip-flop.
ASC2JK	2	N03-012	ANDed output of ASC1JK, ASC1, and ASCOJK.
ASC3	2	L04-002	Set output of MULT/DIVIDE shift counter flip-flop.
ASC3JK		N03-006	ANDed output of ASCOJK, ASC2 and ASC2JK.
AY00 –	1	P01-065	*
AY01 –	1	P01-066	*
AY02 –	1	P01-067	*

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
AY03 –	1	P01-068	*
AY04 –	1	P01-069	*
AY05 –	1	P01-070	*
AY06 –	1	P01-071	*
AY07 –	1	P01-072	*
AY08 –	1	P01-073	*
AY09 –	1	P01-074	*
AY10 –	1	P01-075	*
AY11 –	1	P01-076	*
AY12 –	1	P03-005	*
AY13 –	1	P03-006	*
AY14 –	1	P03-009	*
AY15 –	1	P01-063	*
A1SFB	3	S05-006	Set input to MUL3 –
BTSRX –	3	U05-011	ANDed output of SRE1 and BTSRE
A15AO –	3	R04-004	Inverted from A15O.
A15O	1	P01-025	*
BREGO	1	P01-019	*
BTSRE	3	U05-006	ORed output of SREAO – and EBINT –.
BTSRX –	3	D05-011	ANDed output of SRE1 and BTSRE
BTST	2	R04-008	Inverted from BTST –.
BTST –	1	N05-008	ORed output of BTI – and BTO –.
BT0 –	1	K05-006	ANDed output of EBTAO, IO50+, and STAT.
BT1 –	1	K05-012	ANDed output of EBTAO, STAT –, and IO5O –.
BT1A	3	V05-002	Set output of first Bit Test

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
			successful flip-flop.
BT1B	3	V05-006	Set output of second Bit Test successful flip-flop.
B000	3	P01-050	*
B000A	3	E05-011	ANDed output of WERE03 and B000.
B000A –	3	R04-002	Inverted from B000A.
B140 –	2	P01-052	*
B150 –	1	P03-027	Bit 15 from B register.
B150AO	1	C04-004	Inverted from B150 –.
CB15	1	P03-010	*
CB15A	1	T04-008	Inverted from CB15A –.
CB15A –	1	T04-006	Inverted from CB15.
CLRAR	3	T05-012	ANDed output of SH1AO, SH0AO –, and CORCLR.
CLRAR –	3	T04-004	Inverted from CLRAR.
CORR	1	E04-008	Inclusive AND output of CORR2, CORR2 –, B15AAO, and B150 –
CORRJ –	3	R04-006	Inverted from CORR2J.
CORR2	2	D05-006	Flip-flop set output of negative divide correction logic.
CORR2 –	2	D05-005	Flip-flop reset output of negative divide correction logic.

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
CORR2J	2	E02-012	ANDed output of AEQB, SGNB, and DSC3.
CORR2K	2	E03-012	ANDed output of B14O –, SH1AO –, and DSC1.
CORCLR	3	F02-008	ORed output of CORR2 – and CORRJ –.
DISCR –	2	T03-003	ANDed output of DSC1 and DSC2 –.
DIV –	1	P01-017	*
DIVAO	1	C04-008	Inverted from DIV –.
DIVCOR	1	E02-008	ANDed output of CORR, DSC2, and SH0AO.
DOF1 –	1	D04-006	Divide overflow ANDed output of BREG0, AEQB, DSC2A, and DSC1.
DOF2 –	1	D03-008	Divide overflow ANDed output of DSC1, DSC2, and SG*C8.
DS –	2	L05-006	ANDed output of OF6 and DSC2.
DSC1	2	M04-002	Set output of divide state counter flip-flop one.
DSC1 –	2	M04-003	Reset output of divide state counter flip-flop one.
DSC1J	2	L05-008	ORed output of ED – and DS –.
DSC2	2	M04-006	Set output of divide state

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
			counter flip-flop two.
DSC2 –	2	M04-005	Reset output of divide state counter flip-flop two.
DSC2A	2	C04-012	Inverted from DSC2 –.
DSC2J	2	L05-011	ORed output of EDS – and DSC1 –.
DSC3	2	R03-002	Set output of divide state counter flip-flop three.
DSC3 –	2	R03-003	Reset output of divide state counter flip-flop three.
DSC3A	2	C04-010	Inverted from DSC3 –.
DSC3J	2	K04-006	ANDed output of DSI – and DSC2.
DSGN –	2	R02-006	ANDed output of DIVAO, OF4, and A15O.
DSI –	2	S03-008	ORed output of RAO6, OF6AO, and DSC1 –.
DVCOR –	3	R02-008	ANDed output of DSCB, SH0AO, and DIVCOR.
EAAO –	3	U04-008	
EAAOX	3	U03-008	Expander input to clock A register gating.
EAAOX –	3	U03-006	Expander tie point for clock A register gating.
EAM	1	N05-006	ANDed output of SH0AO –

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
			and DSC2.
EATA1 –	1	T03-008	ANDed output of DSC2 and SG + R.
EATA2 –	1	S02-012	ANDed output of I04O –, BT1A, and EBTAO.
EATA3 –	1	S02-006	ANDed output of SRE, OF5AO, and I03O +.
EAXAO –	1	S03-006	*
EBAO –	3	T05-006	*
EBINT –	3	U05-003	ANDed output of INTX – and EBTAO.
EBT –	1	P03-035	*
EBTAO	1	T03-011	ANDed output of EBT – and RAO5.
EBTA1 –	1	D03-012	ANDed output of OFBAO, I04O +, and SRE.
EBTA2 –	1	D03-006	ANDed output of I04O +, BT1A, and EBTAO.
EBTA3 –	1	F03-011	ANDed output of DSC2 and SH0AO.
EBTJ	3	E05-006	ANDed output of IF3 and EBTAO.
EBXAO –	1	E03-006	*
ED –	2	L05-003	ANDed output of DSC3 and SH0AO –

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
EDS −	2	F03-003	ANDed output of OF5AO and DIVAO.
EN1B0 −	1	F05-008	*
EPXAO −	2	F04-003	*
ETSM −	2	F03-006	ANDed output of OF5AO and MULAO.
EXXSK −	3	K05-008	*
E1B0	1	D02-011	ANDed output of DSC2A and SG+R.
FINAO −	1	F05-006	*
GNDAO −		H03-007	Logic ground
IF2 −	2	P01-028	*
IF2AO −	2	V04-008	ANDed output of IF2RST, RAO2, and RAO1.
IF2RST	2	F02-011	ORed output of IF2 − and RST −.
IF3	3	P03-036	Instruction fetch cycle three.
INTX −	3	P03-034	*
I00O+	1	P03-011	*
I01O+	1	P03-012	I register output.
I02O+	1	P03-013	*
I03O+	1	P03-014	*
I04O+	1	P03-015	*

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
I040 –	1	P03-016	Complement of I040+.
I050+	1	P03-017	*
I050 –	1	P03-018	Complement of I050+.
MDEAB –	3	E04-006	*
MDEX	1	F02-003	ORed output of DSC3 – and MSC3 –.
MDIMP –	1	D05-007	*
MOF –	1	D04-008	ANDed output of SH0A0, MSC2, CB15A, and MOFX.
MOFX	1	K04-011	ANDed output of R15A0 and SGNB.
MSC1	2	K03-002	*
MSC1 –	2	K03-003	Reset output of MSC1 flip-flop.
MSC1J	2	D02-008	ANDed output of SH0A0 – and MSC3.
MSC2	2	K03-006	Set output of multiply state counter flip-flop two.
MSC2 –	2	K03-005	Reset output of MSC2 flip-flop.
MSC2J	2	F03-008	ORed output of ETSU – and MSC1 –.
MSC3	2	L04-006	Set output of multiply state counter flip-flop three.
MSC3 –	2	L04-005	Reset output of MSC3 flip-flop.

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
MSGN –	2	R02-012	ANDed output of MULAO, B15OAO, and OF4.
MUAE	3	E05-008	ANDed output of SH0AO – and MSC3.
MUL –		P03-056	Multiply sign bit from CPU to storage register.
MULAO	1	T04-010	Inverted from MUL –.
MUL3 –	3	S04-005	*
OF4	1	P01-023	*
OF5 –	1	P01-026	*
OF5AO	1	H04-004	Inverted from OF5 –.
OF6	1	P01-020	*
OF6AO –	1	C04-006	Inverted from OF6.
OPOF –	1	E03-008	*
OPTEL –	2	C05-004	Inverted from SRE2.
OPTEP –	2	C05-006	Inverted from SRE2.
OSAFC –	3	U05-008	*
PSGN –	2	N05-003	ORed output of MSGN – and DSGN –.
R*CB	1	H03-008	Inclusive AND gating of R15AO, CB15A –, R15 –, and CB15A.

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
RAO1	3	T02-001	Pull-up resistor.
RAO2	3	T02-002	Pull-up resistor.
RAO3	3	T02-003	Pull-up resistor.
RAO4	3	T02-004	Pull-up resistor.
RAO5	3	T02-005	Pull-up resistor.
RAO6	3	T02-006	Pull-up resistor.
RAO7	3	T02-008	Pull-up resistor.
RST –		P01-032	*
R15 –	1	P01-057	*
R15AO	1	H04-002	Inverted from R15 –.
SG+R	1	H03-006	Inclusive AND of SGNB, R15AO, R15 –, and SGNB –.
SG*CB	1	N04-008	Inclusive AND of SGNB, SGNB –, CB15A, and CB15A –.
SG*R	1	C04-002	Inverted from SG+R.
SGNB	2	R05-005	Set output of the sign bit storage flip-flop.
SGNB –	2	R05-006	Reset output of the sign bit storage flip-flop.
SH0AO	2	K04-003	ANDed output of ASC0 and SHAO.
SH0AO –	2	H04-010	Inverted from SH0AO.
SH1AO	2	N03-008	ANDed output of ASC1, ASC2,

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
			and ASC3.
SH1AO –	2	H04-008	Inverted from SA1AO.
SKIP –	2	F02-006	ANDed output of SRE and AEQB.
SKIP1 –	3	T05-008	ORed output of DSC2 –, MSC2 –, and BTSRX –.
SKIP2 –		C05-002	Inverted from SRE2.
SRE	1	P01-018	Skip if register equal signal from CPU.
SREAO –	3	H04-006	Inverted from SRE.
SREJ	2	L03-003	ORed output of SREJ2 – and SREJ1 –.
SREJ1	2	E02-006	ANDed output of OF6, SRE, and AEQB.
SREJ1 –	2	R04-012	Inverted from SREJ1.
SREJ2 –		L03-006	ANDed output BT1B and BTST.
SREK	2	K04-008	ANDed output of SREKE and SRE2.
SREKE	2	L03-008	ORed output of EBT – and SRE3 –.
SRE1	2	F04-002	Set output of SRE state counter flip-flop one.
SRE2	2	F04-006	Set output of SRE state counter flip-flop two.
SRE3 –	2	D05-003	Reset output of SRE state counter flip-flop three.

Table 4-1. OIS Mnemonics *(continued)*

Mnemonic	Source		Description
STAT	1	H04-012	Decoded output of the adder.
STAT –		H02-010	Inverted from STAT.
STQB	2	R05-009	Set output of store quotient bit flip-flop.
STQBD	2	D02-003	ANDed output of R*CB and DSC3A.
WIRE03	3	S05-008	Exclusive ORed output of R15AO, A15O, A15AO –, and R15 –.
WIRE2	3	E05-003	ANDed output of DSC2 and DSC1 –
5VAO	1	H02-024	Five volt tie point.

4.6 PROGRAMMING

There are no operating controls on the OIS; all functions are controlled by the computer program or from the manual controls on the computer front panel.

4.6.1 Description of Instructions

Eight instructions are recognized by the OIS (table 4-2). They include two one-word instructions (one for each type of multiplication and division) and six two-word instructions.

Table 4-2. OIS Instruction Set

Mnemonic	Octal Code	Description	Time/Cycles
MULT	16XYYY*	Multiply; single-word	8.5
DIV	17XYYY*	Divide; single-word	8.5
MULTI	006160	Multiply Immediate; double-word	8.5

Table 4-2. OIS Instruction Set *(continued)*

Mnemonic	Octal Code	Description	Time/Cycles
DIVI	006170	Divide Immediate; double-word	8.5
MULTE	00616X*	Multiply Extended; double-word	9.5
DIVE	00617X*	Divide Extended; double-word	9.5
BT	0064ZW*	Bit Test; double-word	1-2
SRE	0066ZX*	Skip if Register Equal; double-word	3-3.5

* For the definition of variables and instruction formats, refer to document number 98 A 9908 003.

4.6.2 Examples of Multiplication and Division

The following examples are provided for further understanding of the operation of the OIS. Both decimal and octal numbers are provided for clarity. Negative numbers are shown in two's complement form.

Example 1

Signed multiplication:

$$-56 * 1212 = -67{,}872$$

$$(0177710) * (002274) = (017777573340)$$

Before execution:	After execution:
A register = 000000	A register = 0177775
B register = 0177710	B register = 073340
R register = 002274	R register = 002274

Example 2

Signed division:

−1,234 / 616 = −2, with remainder

(01777777545) / (01150) = (0177776) with remainder

Before execution:	After execution:
A register = 01777777	A register = 0177776
B register = 075456	B register = 0177776
R register = 001150	R register = 001150

In these examples:

a. Before execution, the A register contains the high-order half of the dividend, and, after execution, the remainder.

b. Before execution, the B register contains the low-order half of the dividend, and, after execution, the quotient.

c. The R register contains the divisor from memory.

4.6.3 Typical BT Instruction Usage

Example 1 illustrates a typical BT operation. The A register is being tested for one in bit 0. The condition is met and a jump operation is performed.

Example 1

A register contents = 000001

Jump condition: Test bit 0 of the A register for one

Condition met: Jump to the specified address

The following example indicates that bit 3 of the B register is to be tested for zero. Because bit 3 is one, a jump does not occur and the next instruction in sequence is executed.

Example 2

B register contents = 000077

Jump condition: Test bit 3 of the B register for zero

Condition not met: Execute the next instruction

4.6.4 Typical SRE Instruction Usage

In the following example, the contents of the effective memory address (R register) are compared with the contents of the A register. Because they are equal, the next two addresses in memory are skipped and the instruction in the third address is executed. If the contents of the two registers are not equal, the next instruction in sequence is executed.

Example

A register contents = 011000

R register (memory) contents = 011000

Skip condition: A register = R register

Condition met: Skip the next two memory addresses

SECTION 5
MAINTENANCE

Maintaining the OIS consists of executing the Test Executive Program, part 2 (document 98 A 9908 960, volume I, chapter II), troubleshooting, and, if required, making repairs.

If repair is indicated it is recommended that the entire DM254 circuit card be replaced after a general check for proper voltage, loose chips, broken wires, obvious shorts, etc.

5.1 TEST EQUIPMENT

The following is a list of recommended test equipment and tools for the maintenance of the OIS circuit card.

a. Multimeter, Triplett Type 630

b. Extender Card

c. Oscilloscope, Tektronix Type 547

5.2 TEST PROGRAMS

Using the operational techniques outlined in the Varian 620 Test Programs Manual (document 98 A 9908 960), load and execute the Test Executive Program. This test exercises the following sequence of instructions: MUL, DIV, MULI, DIVI, MULE, DIVE, BT, and SRE.

The BT test checks selected bits of the A and B registers for true or false. The SRE test compares the A and B registers in the following addressing modes: relative, direct, indirect, indexed by X, and indexed by B. Both skip and no-skip conditions are tested.

5.3 ERROR REPORTING

Errors detected in the OIS tests (except the BT and SRE subtests) are reported through a common error control subroutine (K09). If SENSE switch 1 is set, the program halts at K23 when an error is detected. If SENSE switch 1 is reset, the program outputs the address of the error print routine and the contents of the A, B, and X registers on the Teletype and continues the test. The address of the instruction in error is indicated by the

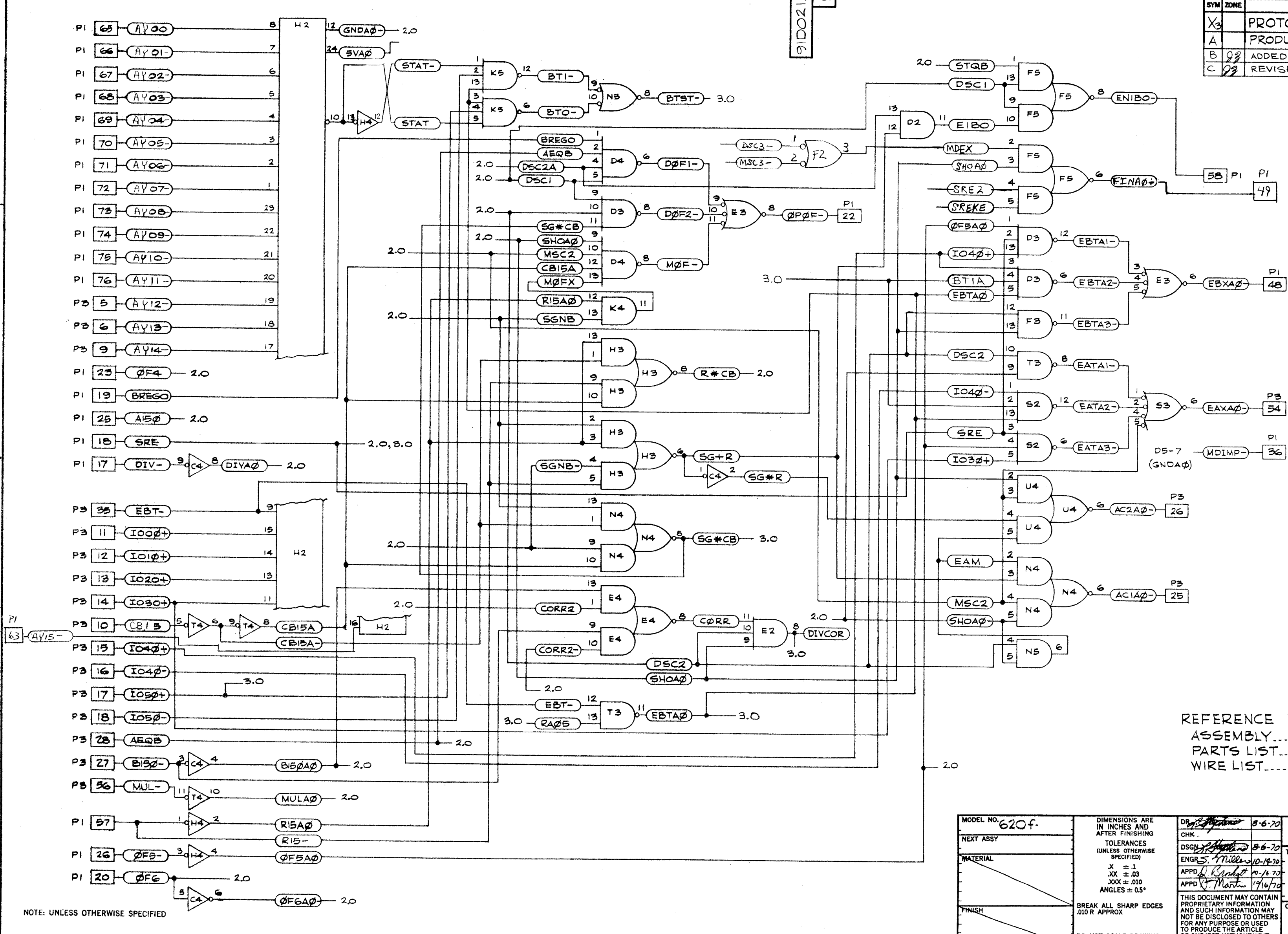
X register contents and the original X register contents are saved at KSVX (refer to the program listing for the address).

Errors in the BT and SRE subtests are reported in a similar manner, but contain separate error reporting subroutines.

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains the logic schematics and parts list for the OIS. The OIS logic schematic is drawing number 91D0212. Included also are sheets of CPU logic that illustrate CPU control of and response to the OIS circuitry.

Drawing Number	Applicable Sheets
91D0212	All
91D0214	5
91D0216	4, 5
91D0217	1, 2, 4, 5



SYM	ZONE	REVISIONS DESCRIPTION	APPROVED	DATE
X3		PROTOTYPE RELEASE		
A		PRODUCTION RELEASE EN 4854	S. Miller	10-14-70
B		ADDED P3-21 & T2-9 PER EN 4913		2/4/71
C		REVISED PER EN 5008		2/9/71

REFERENCE DRAWINGS

ASSEMBLY..... 44D0444

PARTS LIST.... 44P0444

WIRE LIST...... 95W0647

NOTE: UNLESS OTHERWISE SPECIFIED

MODEL NO. 620f

NEXT ASSY

MATERIAL

FINISH

DIMENSIONS ARE IN INCHES AND AFTER FINISHING

TOLERANCES (UNLESS OTHERWISE SPECIFIED)

.X ± .1

.XX ± .03

.XXX ± .010

ANGLES ± 0.5°

BREAK ALL SHARP EDGES .010 R APPROX

DO NOT SCALE DRAWING

DR 8-6-70

CHK

DSGN 8-6-70

ENGR S. Miller 10-14-70

APPD 10-16-70

APPD 10/16/70

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varian data machines /a varian subsidiary 2722 michelson drive / irvine / california / 92664

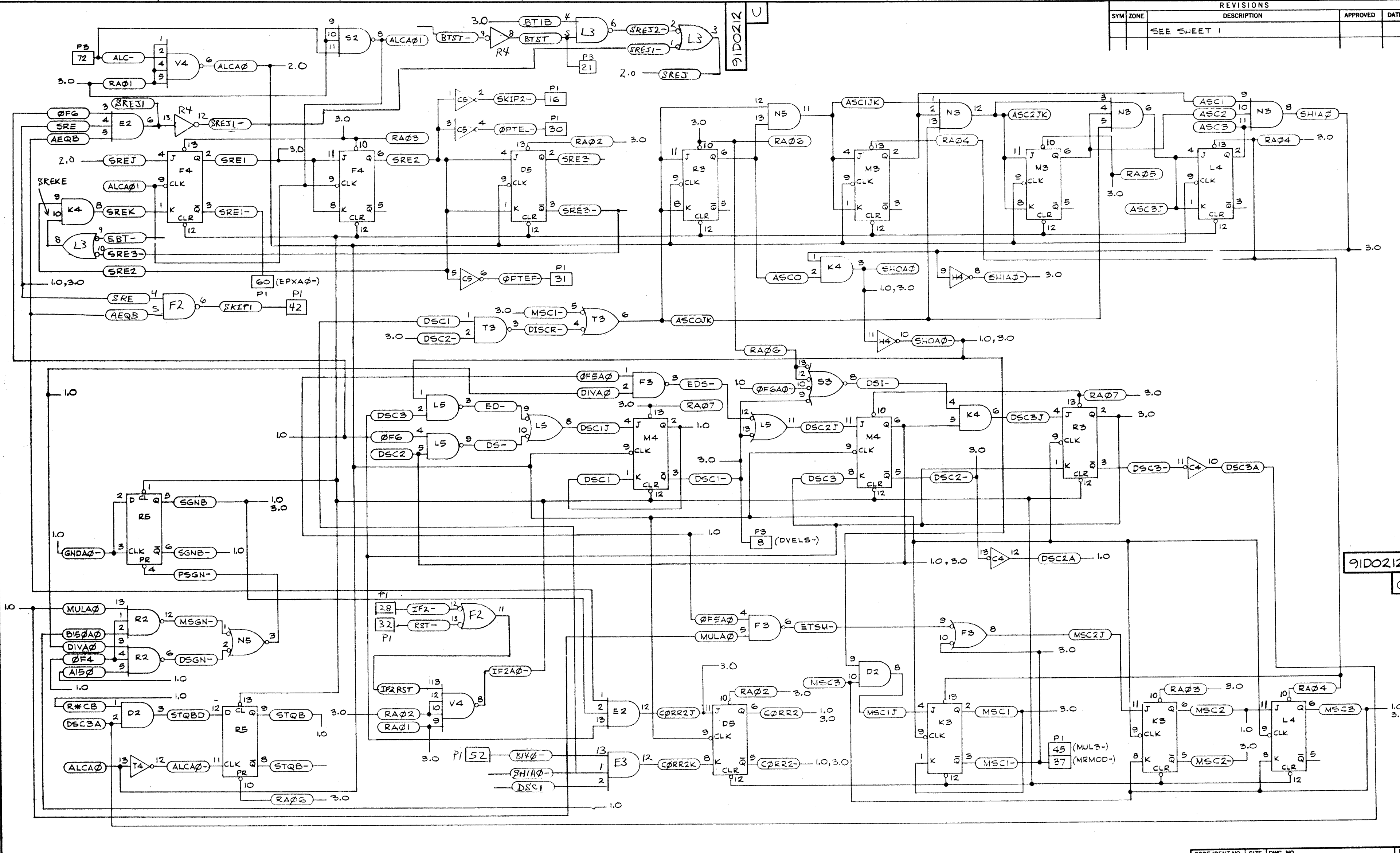
TITLE LOGIC DIAGRAM, ARITHMETIC OPTION

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	91D0212	C

SCALE NONE

SHEET 1 OF 3

REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
		SEE SHEET 1		



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21101	D	91D0212	C
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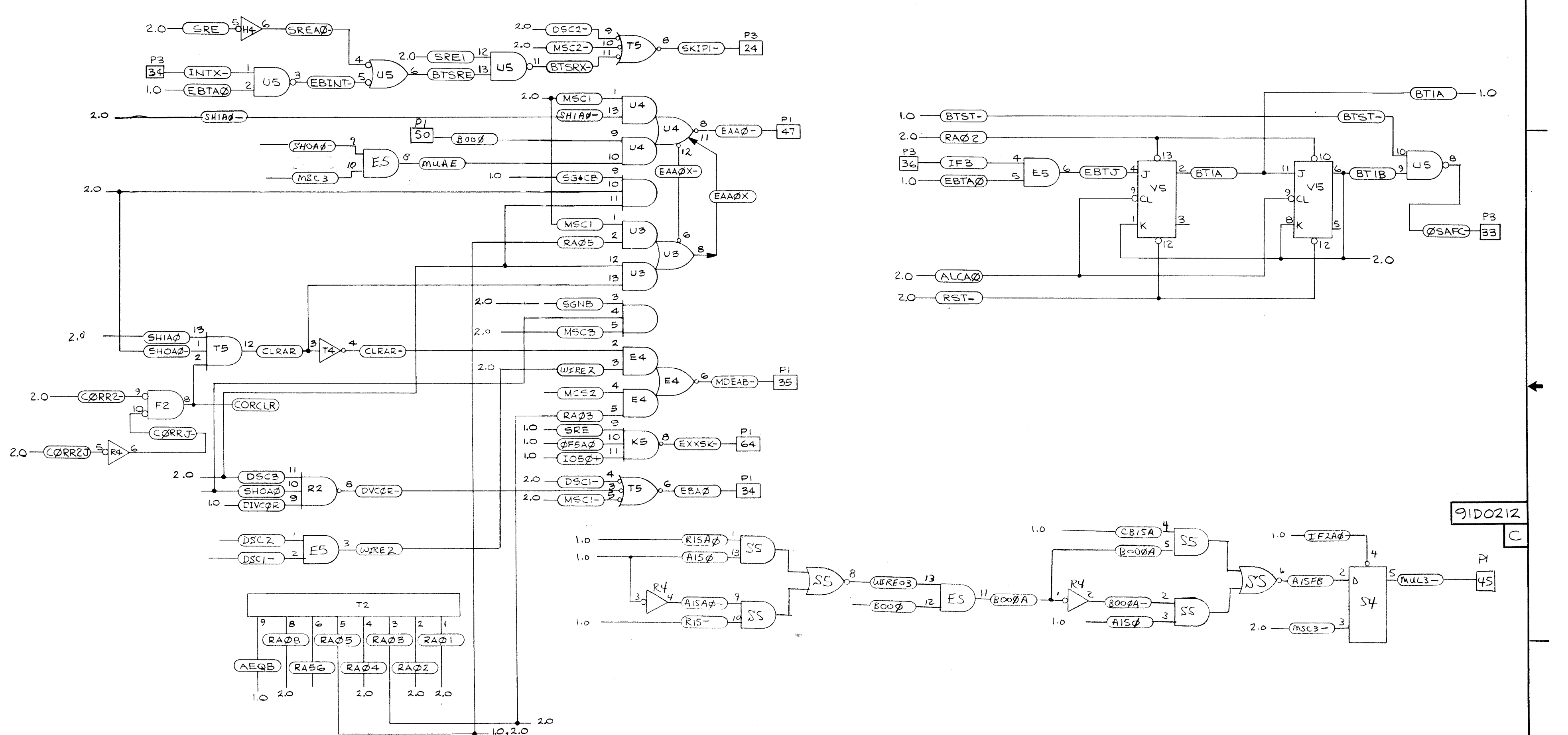
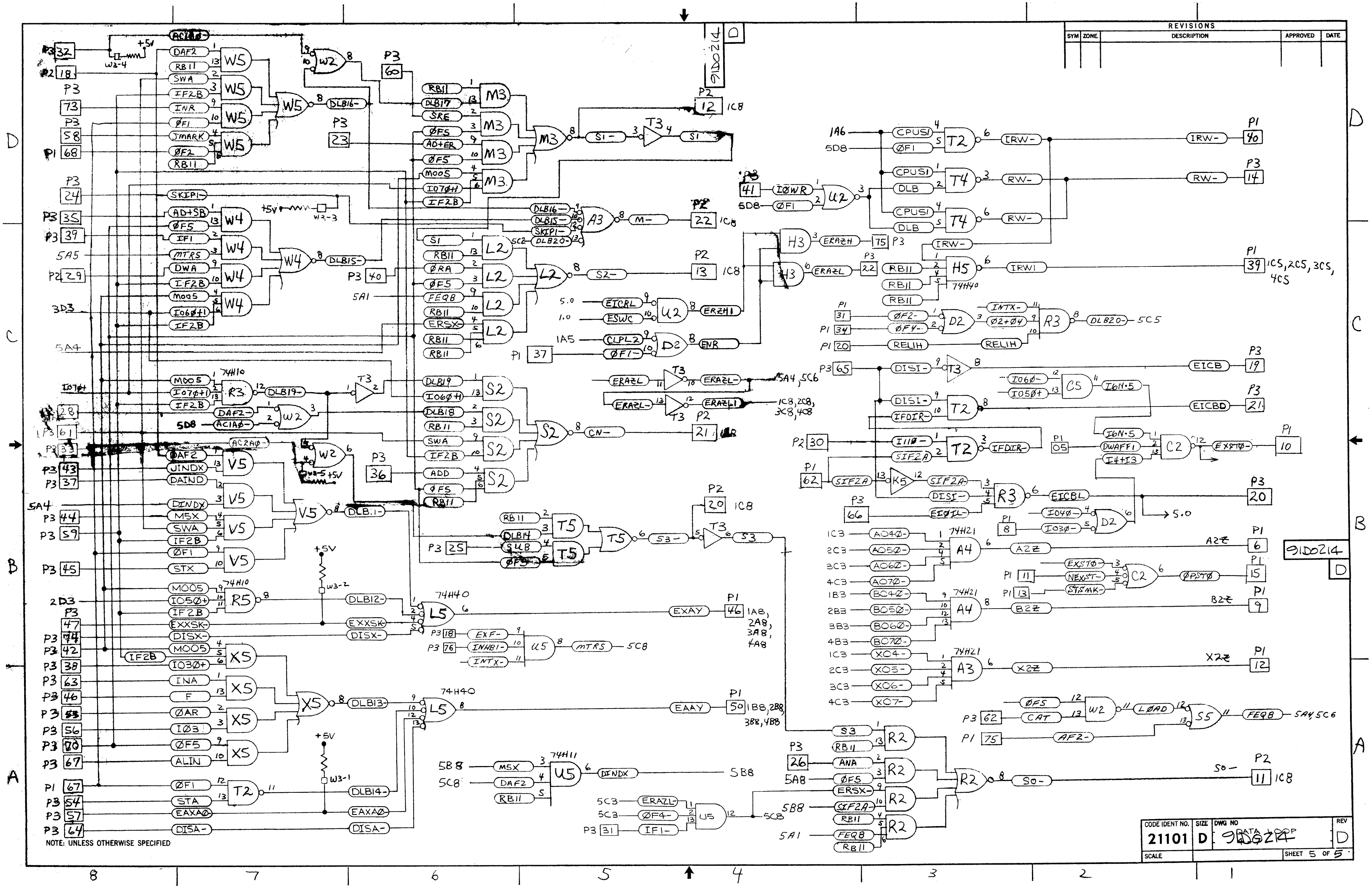
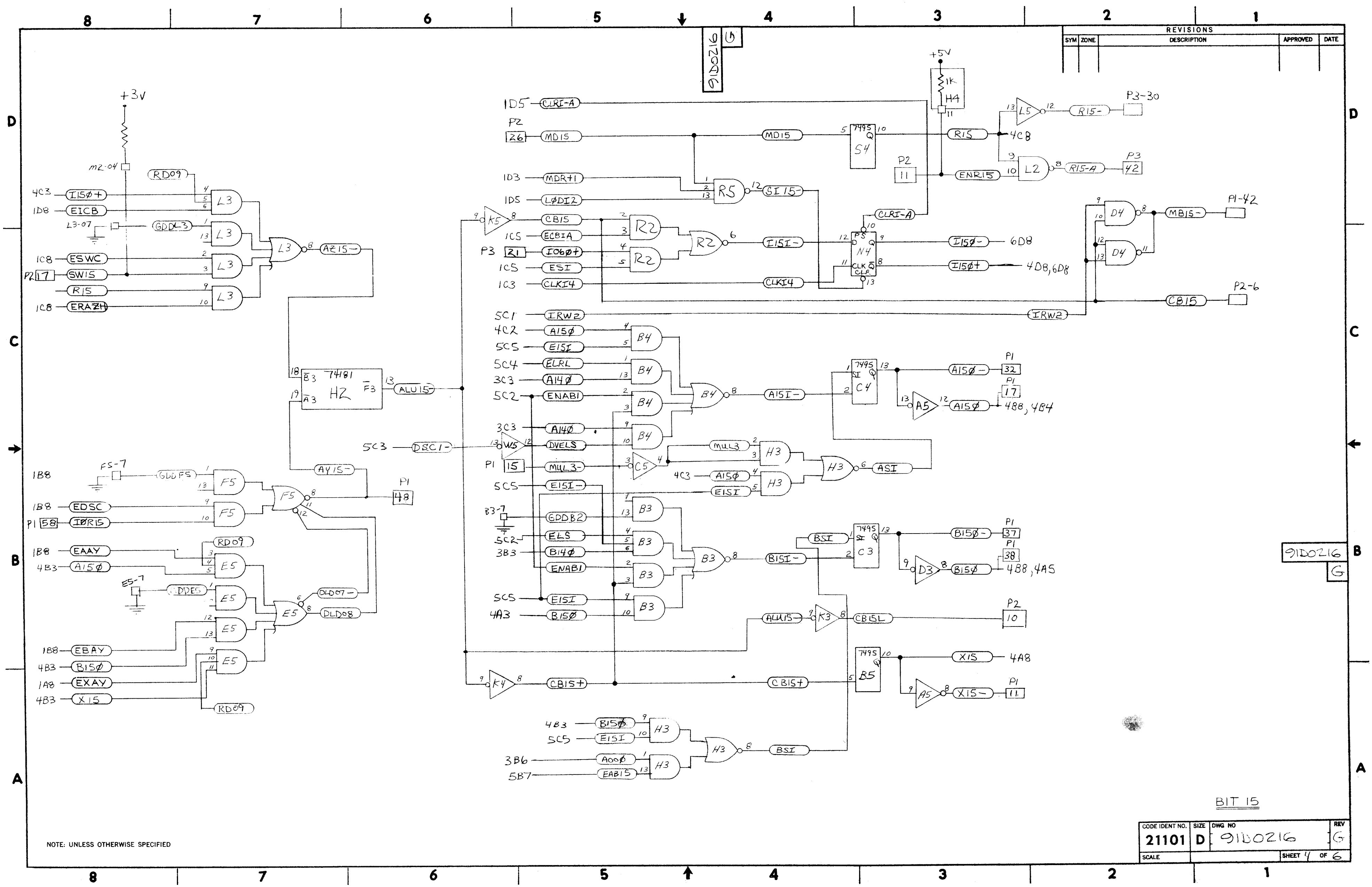


NOTE: UNLESS OTHERWISE SPECIFIED

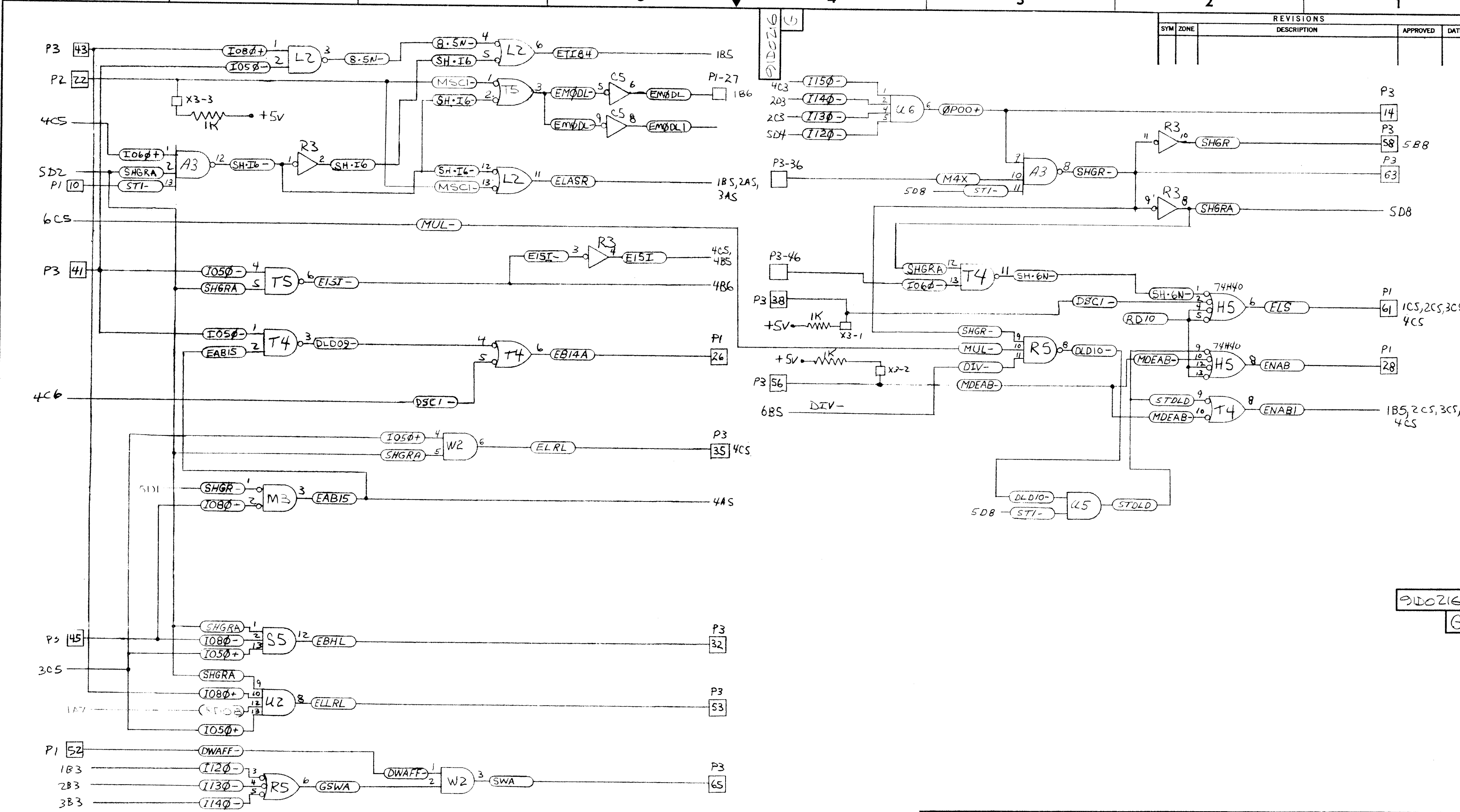
REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
		SEE SHEET 1		

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	91D0212	C
SCALE NONE		SHEET 3 OF 3	


REVISIONS
SYM
ZONE
DESCRIPTION
APPROVED
DATE
91D0214
NOTE: UNLESS OTHERWISE SPECIFIED
CODE IDENT NO. 21101
SIZE D
DWG NO
DATA LOOP
REV D
SCALE
SHEET 5 OF 5



REVISIONS
SYM ZONE DESCRIPTION APPROVED DATE
91D0216 G
BIT 15
CODE IDENT NO. 21101
SIZE D
DWG NO 91D0216
REV G
SCALE
SHEET 1 OF 6
NOTE: UNLESS OTHERWISE SPECIFIED
+3V
+5V
74181 H2
7495 S4
7495 C4
7495 C3
7495 B5
N4
ALU15
AZ15-
AY15-
MD15
SI 15-
CLRI-A
CB15
MB15-
IRW2
R15-
R15-A
ENR15
I15I-
I15Ø-
I15Ø+
CLKI4
A15I-
A15Ø-
A15Ø
ASI
B15I-
B15Ø-
B15Ø
BSI
CB15L
CB15+
X15
X15-
DSC1-
DLD07-
DLD08
P3-30
P1-42
P2-6
4C8
6D8
4D8,6D8
4B8,4B4
4B8,4A5
4A8



REVISIONS

SYM	ZONE	DESCRIPTION	APPROVED	DATE

NOTE: UNLESS OTHERWISE SPECIFIED

MODEL NO.	620/f
NEXT ASSY	
MATERIAL	
FINISH	

DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
BREAK ALL SHARP EDGES .010 R APPROX
DO NOT SCALE DRAWING

DR	D.D. KRIEWALDT
CHK	
DSGN	
ENGR	
APPD	
APPD	

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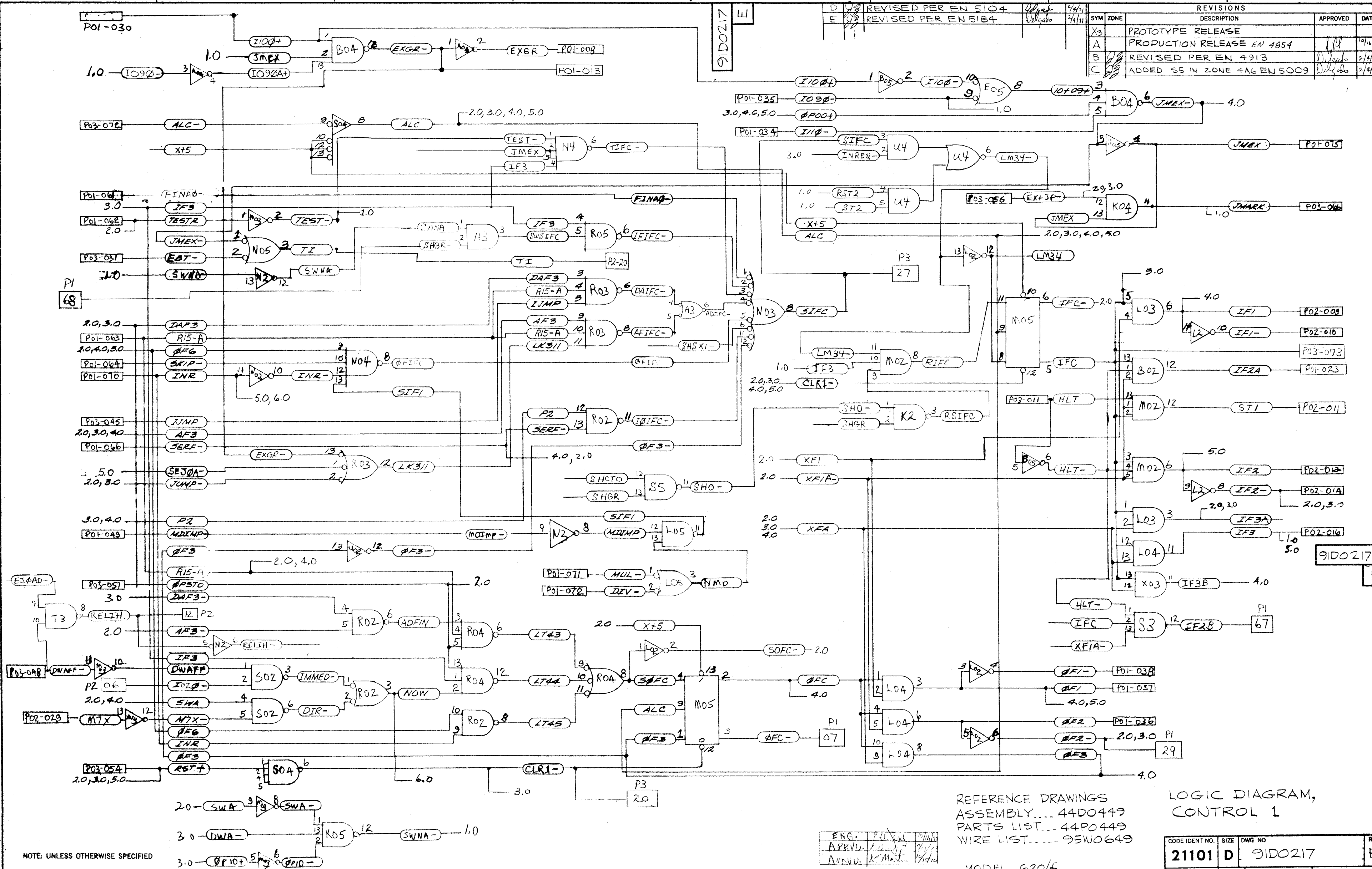
TITLE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	9IDC216	G

SCALE | SHEET 5 OF 6



		REVISIONS		
SYM	ZONE	DESCRIPTION	APPROVED	DATE
X3		PROTOTYPE RELEASE		
A		PRODUCTION RELEASE EN 4854		10/14/70
B		REVISED PER EN 4913		2/4/71
C		ADDED S5 IN ZONE 4A6 EN 5009		2/4/71
D		REVISED PER EN 5104		4/4/71
E		REVISED PER EN 5184		2/4/71

REFERENCE DRAWINGS
ASSEMBLY.... 44D0449
PARTS LIST.... 44P0449
WIRE LIST..... 95W0649

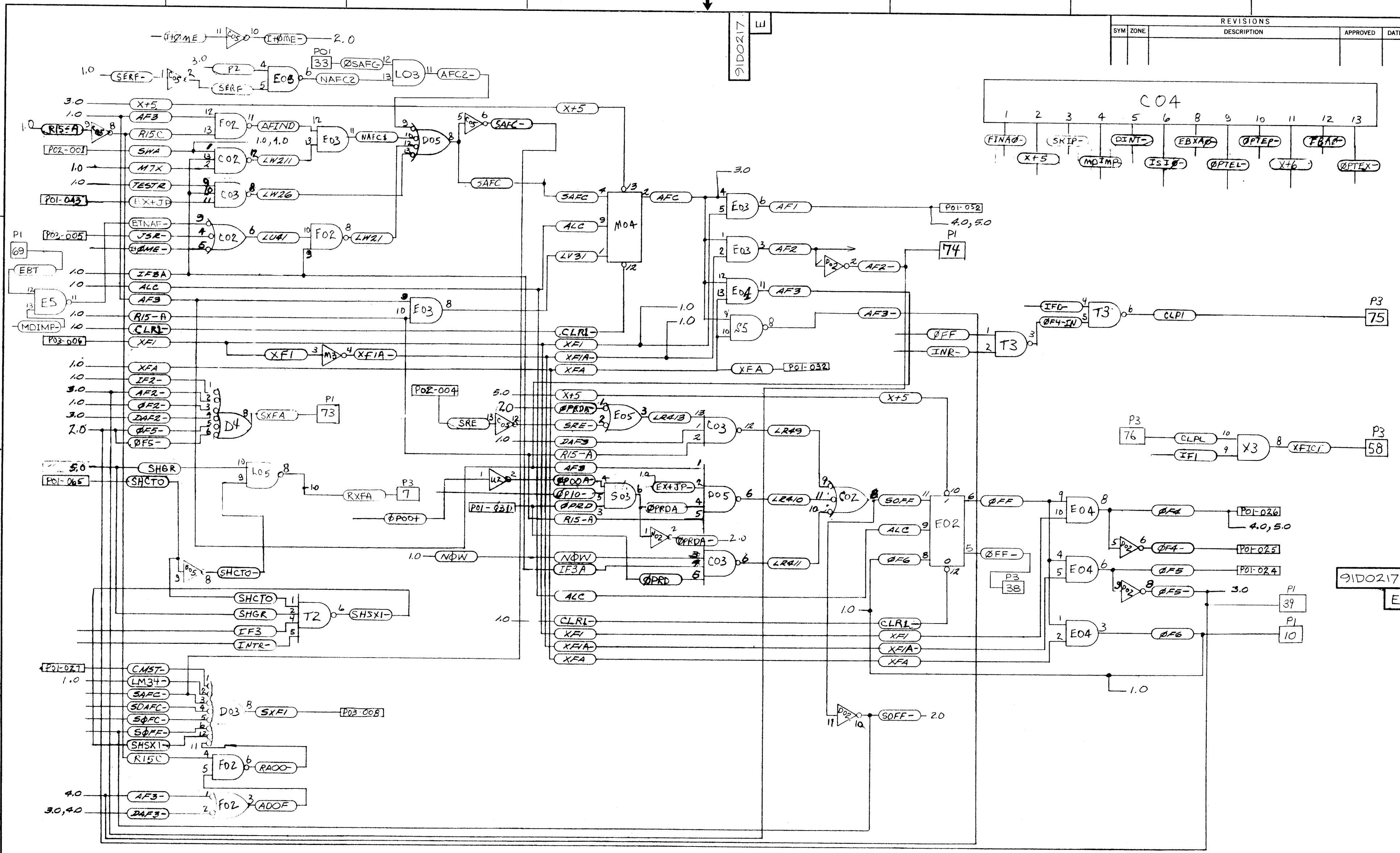
MODEL 620/f

LOGIC DIAGRAM,
CONTROL 1

NOTE: UNLESS OTHERWISE SPECIFIED

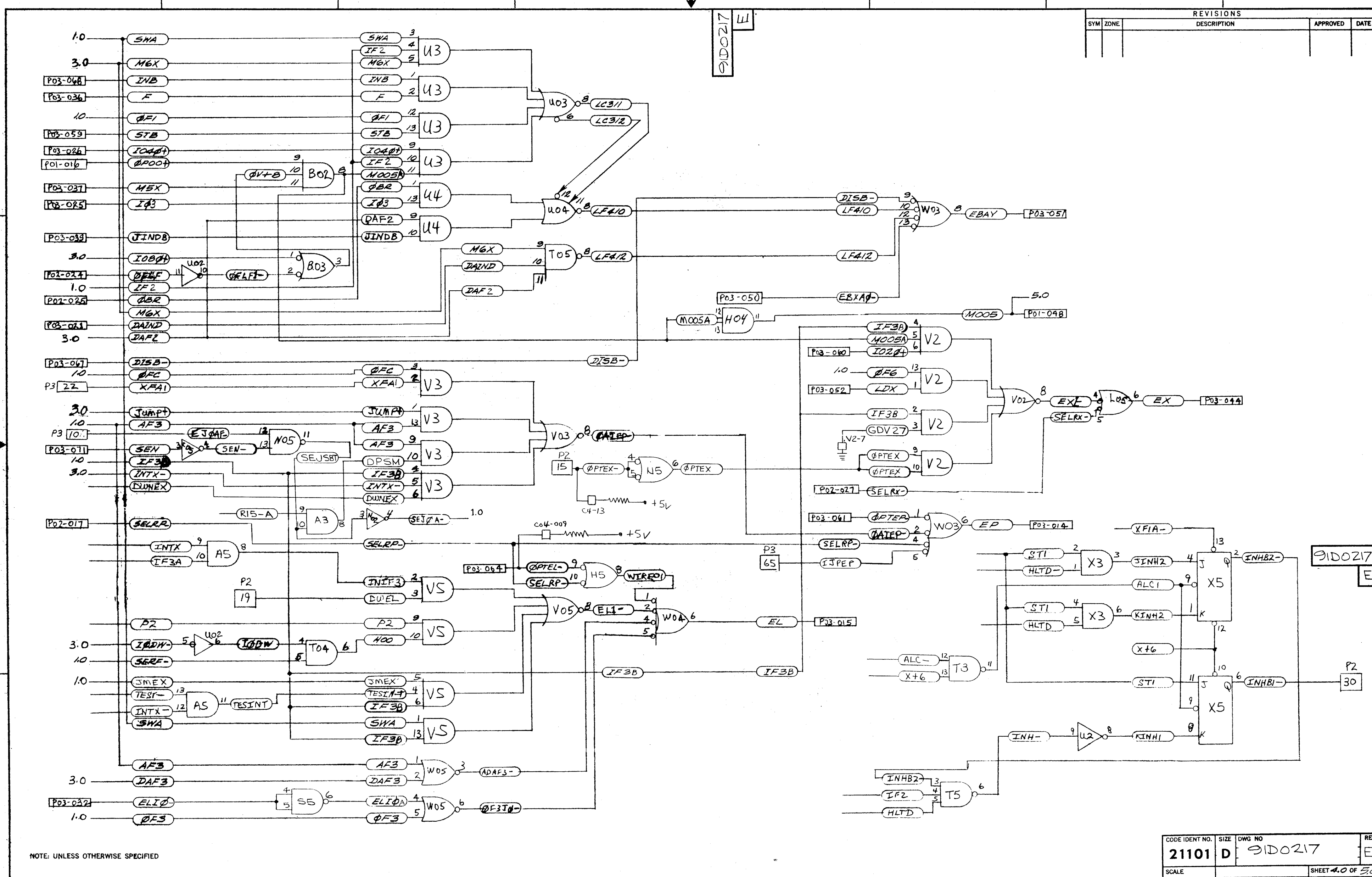
CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	91D0217	E

SHEET 10 OF 50

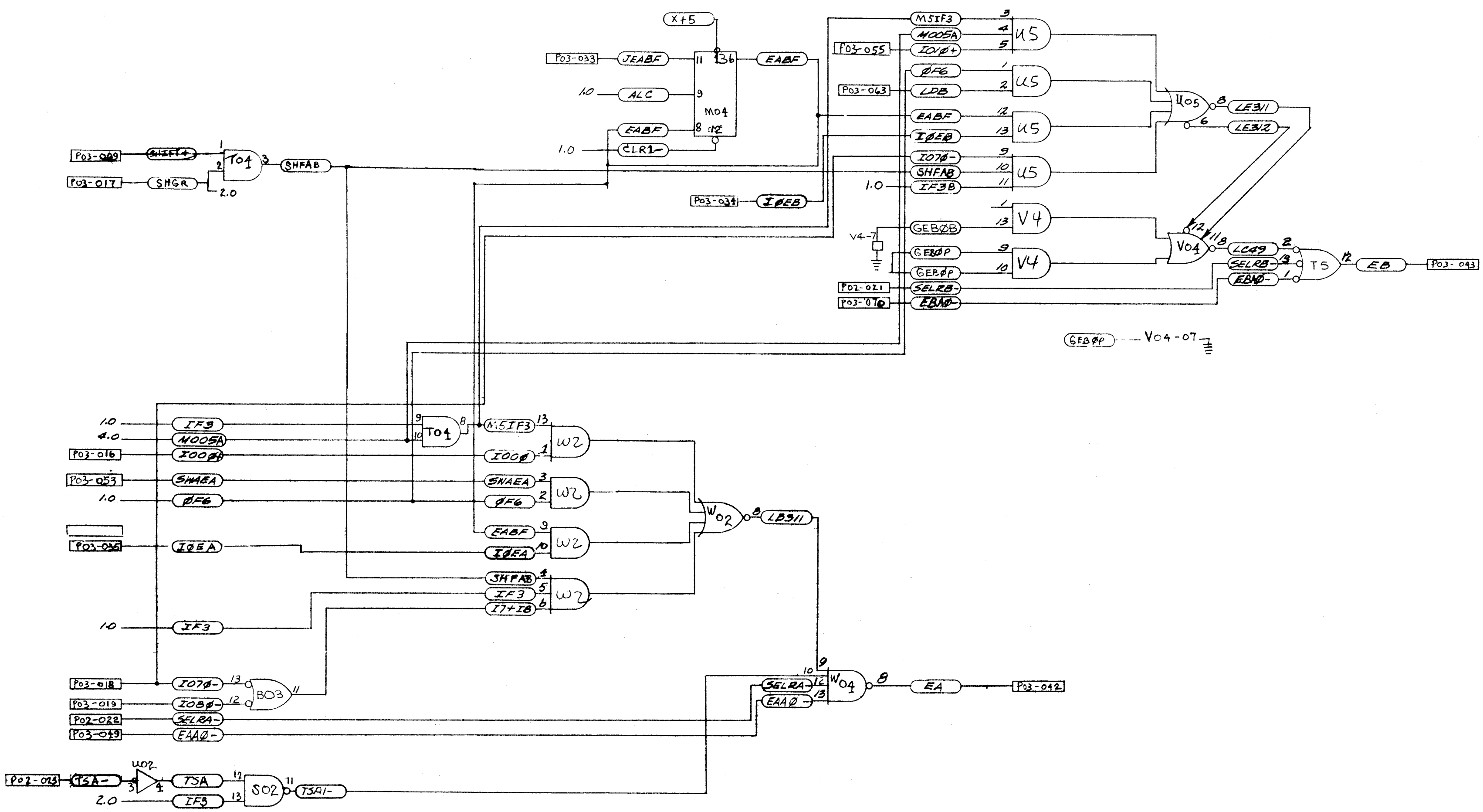


NOTE: UNLESS OTHERWISE SPECIFIED

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	91D0217	E
SCALE		SHEET 20 OF 50	



9ID0217
E
REVISIONS
SYM ZONE DESCRIPTION APPROVED DATE
NOTE: UNLESS OTHERWISE SPECIFIED
CODE IDENT NO. 21101
SIZE D
DWG NO 9ID0217
REV E
SCALE
SHEET 4.0 OF 50



91D0217 E

REVISIONS

SYM	ZONE	DESCRIPTION	APPROVED	DATE

NOTE: UNLESS OTHERWISE SPECIFIED

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	91D0217	E
SCALE		SHEET 5.0 OF 50	

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DWG. NO. 44P0444

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO 000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
-	REF	44D0444 C	ASSY		
-	REF	95W0647 E	WIRE LIST		
-	REF	91D0212 D	LOGIC DIAGRAM		
1	1	40D0439-000	P.W. BOARD		
27	2	71A0009-003	CAPACITOR, .1 uf	C1,3,6,8,10,12, THRU 33	
6	3	71N0200-225	CAPACITOR, 2.2uf	C2,4,5,7, 9, & 11	
4	4	49A0104-000	INTEGRATED CIRCUIT	(MC 3001)	
4	5	49A0022-000	INTEGRATED CIRCUIT	(74H11)	
6	6	49A0039-000	INTEGRATED CIRCUIT	(74H00)	
1	7	49A0097-000	INTEGRATED CIRCUIT	(74150)	
4	8	49A0554-001	INTEGRATED CIRCUIT	(74H10)	
1	9	49A0025-000	INTEGRATED CIRCUIT	(VDM 0025)	
6	10	49A0093-001	INTEGRATED CIRCUIT	(74H50)	
8	11	49A0099-000	INTEGRATED CIRCUIT	(74H108)	
1	12	49A0094-001	INTEGRATED CIRCUIT	(74H21)	
1	13	49A0098-000	INTEGRATED CIRCUIT	(74H62)	
4	14	49A0023-000	INTEGRATED CIRCUIT	(74H04)	
1	15	49A0056-000	INTEGRATED CIRCUIT	(74H20)	

NEXT ASSY | MODEL NO 620f | APPD D. Burkett

REV	A	B	C	D	E	F
EN NO	4847	4913	5008	5194	5269	5334
DATE	10-13-70	11-23-70	1/29/71	2/3/71	4/26/71	4/26/71
DR	[illegible]	GRL	[illegible]	WGD	[illegible]	[illegible]
CHK	[illegible] 10-13-70	RAS 11/24/70	[illegible] 2/1/71	WBQ 2/4/71	[illegible]	[illegible]

TITLE: PARTS LIST
OPTIONAL INST SET ASSY

DWG NO 44P0444 | REV F

SHEET 1 OF 2

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DWG. NO. 44P0444

PARTS LIST

CODE IDENT: 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
						000					
						2	16	49A0082-001	INTEGRATED CIRCUIT	(74H74)	
						1	17	49A0019-000	INTEGRATED CIRCUIT	(74H40)	
						1	18	49A0061-000	INTEGRATED CIRCUIT	(74H05)	
						64	19	58A0060-000	SOCKET, 14 PIN		
						4	20	58A0060-001	SOCKET, 16 PIN		
						1	21	58A0060-002	SOCKET, 24 PIN		
						174	22	58A0062-002	POST, WIRE WRAP		
						1	23	16S1057-066	CARD HANDLE		
						0	24	53A0333-040	WIRE, KYNAR	30 AWG, YELLOW	
						1	25	16S1057-047	CARD HANDLE		

NOTES:

DWG NO 44P0444 | REV F

SHEET 2 OF 2

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