POWER FAILURE/RESTART

an option for the
Varian Data Machines 620/f
Computer System

Specifications Subject to Change Without Notice

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ADDENDUM

620/f Power Failure/Restart Manual

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Not only must the PF/R threshold be readjusted when the power supply and/or the PF/R card is changed, it must also be readjusted whenever a change from 50 to 60 Hz (or vice versa) operation is made, or whenever there is an increase in the load on the +5V dc supply.

FOREWORD

The 620/f Power Failure/Restart Manual defines and explains the logical, electrical, and mechanical parameters that control and interface between a Varian Data Machines 620/f computer and the power failure/restart option.

The six sections of the manual:

- Introduce the power failure/restart in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware with drawings and parts lists

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SECTION 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

The *Model 620/f-14 Power Failure/Restart (PF/R)* is a mainframe option for the Varian Data Machines 620/f computer system. The PF/R provides an orderly shutdown of the CPU and memory in case of power failure or turn-off and restarts the program when power is restored.

A single circuit card contains the entire PF/R. If the real-time clock option is also used in the computer system, it is located on the same card. The PF/R plugs into the central processing unit (CPU) tray of the computer.

Power input to the computer is indirectly monitored by the PF/R. A power failure monitor voltage in the computer power supply is constantly being sensed to determine power status. If the monitor voltage drops (due to power failure or power turn-off), the PF/R causes an interrupt. This interrupt has the second-highest priority in the system. The CPU then executes a user-programmed service routine (SAVE) that places the contents of volatile registers (A, B, X, P, and overflow) into memory. The program stops, the memory is disabled, and the system is reset. The power-down service routine cannot be interrupted by lower-priority options or controllers.

When power is restored, the PF/R enables the memory. The CPU executes a user-programmed service routine (RESTORE) that restores the contents of the volatile registers, and the system resumes service of the program in progress at the time of interrupt.

If a power failure or turn-off is detected while the computer is in the step mode, memory is protected, but the contents of the volatile registers are lost.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers and numbers with a leading zero are octal.

1.2 FUNCTIONAL DESCRIPTION

The PF/R is functionally divided into five circuits: control sequencer logic, system start logic, interrupt request logic, power-up/power-down logic, and interrupt priority logic. Figure 1-1 shows the PF/R functional block diagram.

1.2.1 Control Sequencer Logic

This logic section controls critical power-down and power-up functions. The control sequencer monitors the CPU power supply voltage level and sends control signals to logic circuits that generate inhibiting and enabling outputs to the CPU and memory.

1.2.2 System Start Logic

When a power-up sequence is in process, the system start logic generates a signal to reinstate run mode in the CPU.

1.2.3 Interrupt Request Logic

The interrupt request logic generates signals during power-up and power-down processing to initiate the interrupt request cycle and define the interrupt memory addresses (040, 041, 042, and 043).

1.2.4 Power-Up/Power-Down Logic

When the power supply power failure alarm (PFA) signal goes high, power-up is in process and the power failure feedback (PFF) signal reenables the memory. When PFA goes low, power-down is in process; the CPU system is reset and the PF/R loads a no operation (NOP) instruction into the CPU instruction (I) register.

1.2.5 Interrupt Priority Logic

During power-up or power-down processing, the interrupt priority logic disables lower-priority option interrupts.

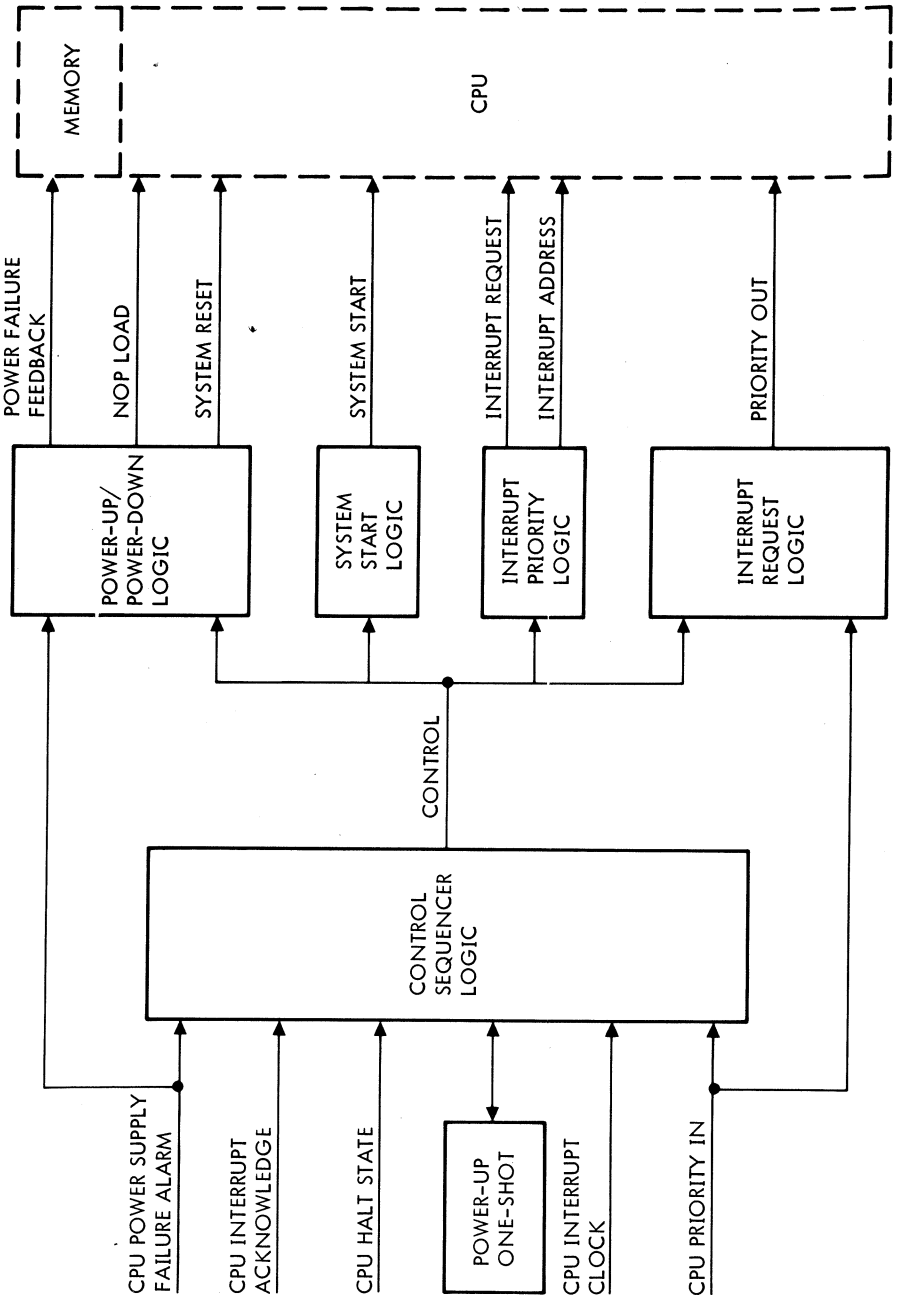

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Figure 1-1. Power Failure/Restart Block Diagram

1.3 SPECIFICATIONS

The functional, physical, and electrical PF/R specifications are listed in table 1-1.

Table 1-1. Power Failure/Restart Specifications

Parameter	Description
Organization	Contains control sequencer logic, system start logic, interrupt request logic, power-up/power-down logic, and interrupt priority logic
Interrupt Memory Addresses	SAVE routine at 040 and 041 and RESTORE routine at 042 and 043
Priority Assignment	Normally second-highest with respect to DMA/interrupt priority assignment (exceeded only by memory protection (MP))
Power-Down Timing	Disables memory and the CPU in less than 2 milliseconds after power loss; up to 300 microseconds allowed for SAVE routine execution
Power-Up Timing	Power-up restoration is typically 40 milliseconds; up to 400 microseconds allowed for RESTORE routine to be executed

Table 1-1. Power Failure/Restart Specifications *(continued)*

Parameter	Description
Logic Levels:	
I/O	Negative Logic True: 0.0 to +0.5V dc False: +2.8 to 3.6V dc
Internal	Positive Logic True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Size	Occupies approximately 15 IC sockets on a 3-by-15-inch (7.7 x 38.1 cm) circuit card; shares card with RTC
Interconnection	Plugs into 620/f CPU tray
Input Power	+5V dc ± 5 percent at 0.5 ampere
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

It is recommended that Varian Data Machines customer service engineers install the PF/R. Logic diagrams, assembly drawings, and wiring information are provided at the time of purchase.

2.1 PHYSICAL DESCRIPTION

The PF/R is on a 3-by-15-inch (7.7 x 38.1 cm) wired-socket card (part number 44P0483-000). If the system includes the Model 620/f-13 Real-Time Clock (RTC), this circuit card is shared with the RTC. Circuit elements are integrated circuits and discrete components (figure 2-1). All connections to the PF/R are made through the 190-terminal card-edge connector, which mates with the corresponding connector in the CPU tray.

2.2 SYSTEM LAYOUT AND PLANNING

The PF/R circuit card (DM289) is located in card slot 14 of the CPU tray. The card slots in the CPU tray, which is mounted in the mainframe, are numbered 1 through 14 from rear to front when you face the 620/f front panel. Figure 2-2 shows the PF/R mounted in the CPU tray.

2.3 SYSTEM INTERCONNECTION

The PF/R circuit card is inserted into its designated card slot when the CPU tray is extended out the front of the mainframe and held by an extender assembly bolted to the front of the mainframe.

Insert the card into the mounting guides of slot 14 with the component side of the card toward the backplane connectors.

Apply moderate pressure to seat the card-edge connectors firmly into the mating connectors on the CPU tray. To prevent damage to the connectors or to the nylon guides, be sure to apply even pressure across the top of the card during insertion.

The card has ejector handles for unseating it from its mating connectors. To remove a card, lift the inside edge of the ejector handles, then lift the card from the slot.

SECTION 2
INSTALLATION

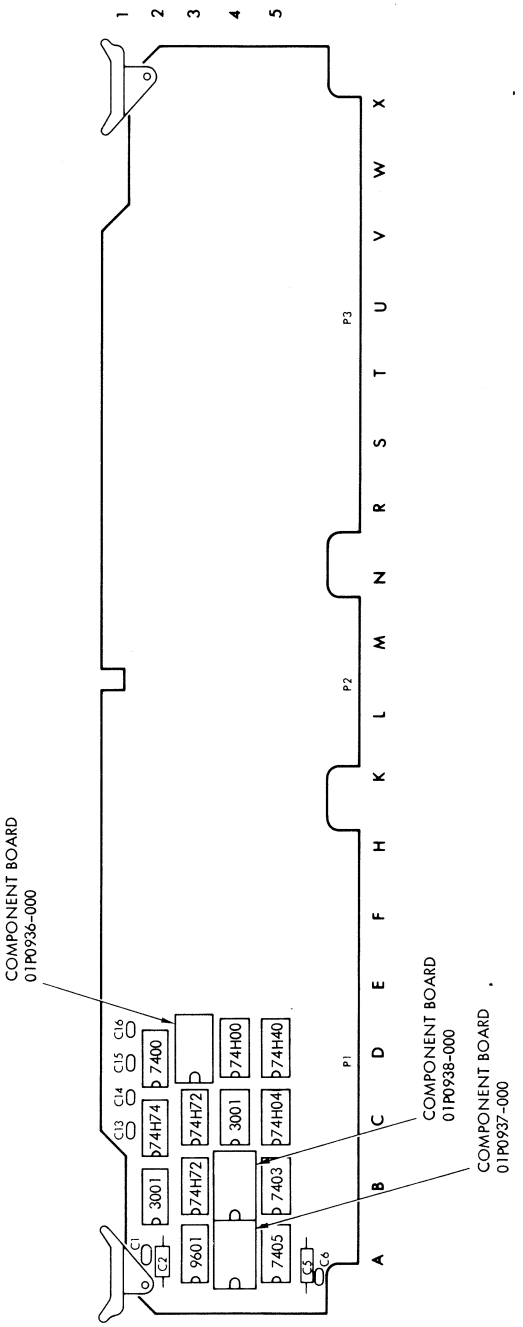

Figure 2-1. PF/R Component Layout Assembly

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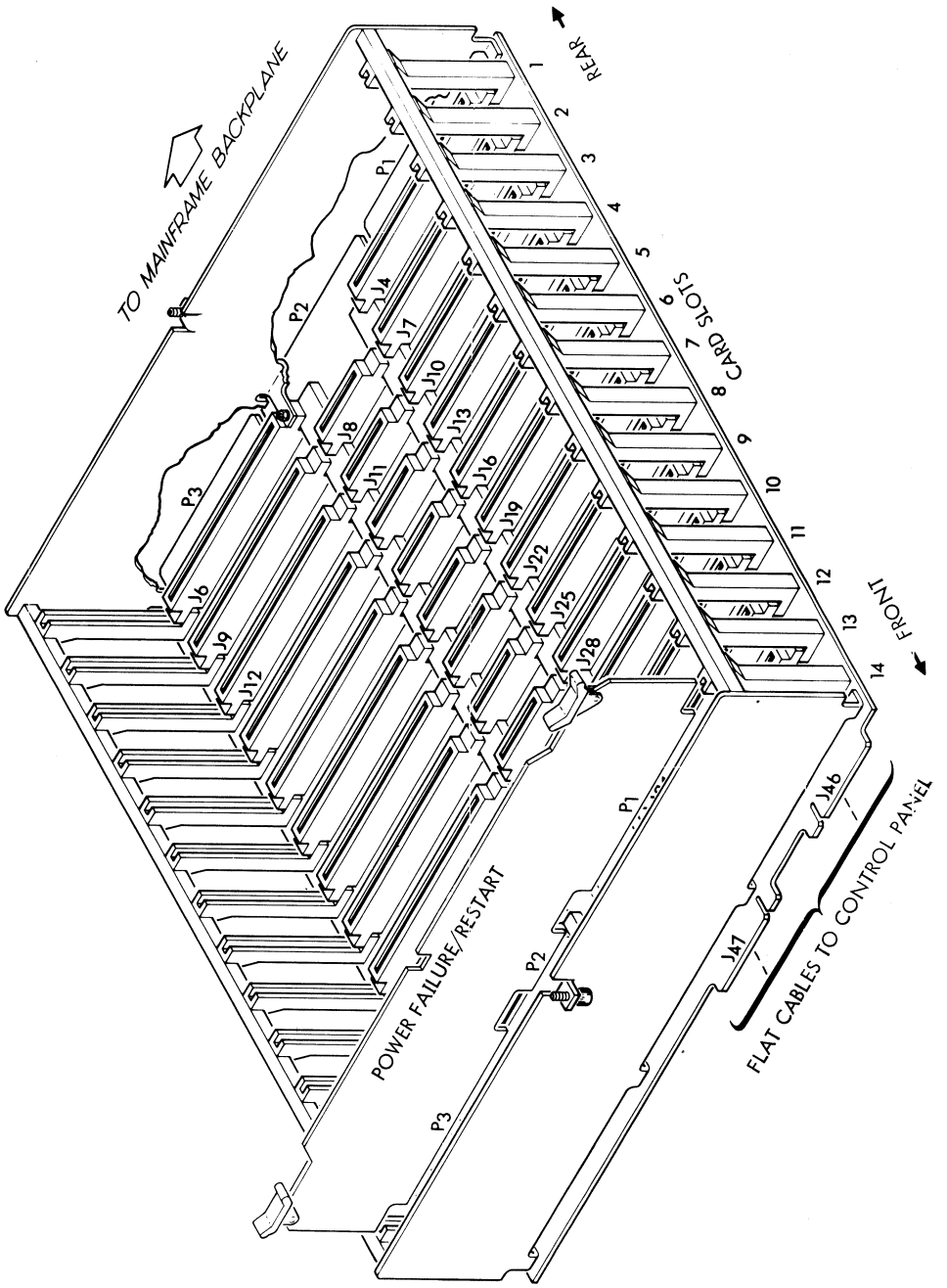


Figure 2-2. PF/R Card Location

2.4 INTERFACE SIGNALS

The PF/R interfaces with the computer via control lines listed in table 2-1. A circuit card connector pin number follows each signal mnemonic. Refer to section 4 for the mnemonic definitions.

Table 2-1. PF/R Interface Signals

Signal	Pin Number	Signal	Pin Number
Input			
ALC–	P1-24	PFA	P1-12
IUAX–C	P1-19	PRMIX–	P1-21
IUCX–C	P1-20	ST1	P1-22
Output			
AB01–C	P1-15	OPTEI–	P1-08
AB05–C	P1-16	PFACT–	P1-11
BM09–	P1-05	PFF	P1-13
BM11–	P1-06	PFLST–	P1-09
IURX–	P1-14	PFRST–	P1-10
OPECB–	P1-07	PRN1X–	P1-23

SECTION 3
OPERATION

There are no operating controls or indicators on the PF/R circuit card. The PF/R functions are under program control from the CPU.

SECTION 4
THEORY OF OPERATION

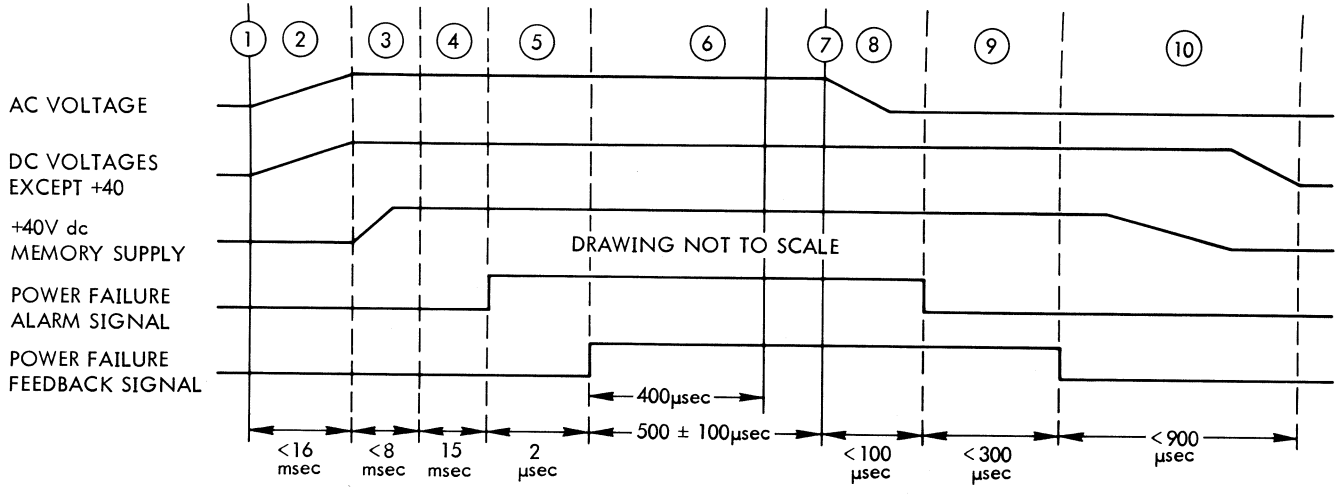
In the following descriptions of PF/R operation, numbers in parentheses indicate the location of circuit elements and signals on the PF/R logic diagram (section 6). The first number locates the sheet; the following letter and number, the area on that sheet.

4.1 POWER SUPPLY STATUS

When power is lost or below threshold, the Power Failure Alarm (PFA) signal (2C4) from the 620/f power supply goes low, causing the PF/R to generate an interrupt request to the CPU to execute the SAVE routine. When the power-down sequence (section 4.2) is complete, the PF/R generates the Power Failure Feedback (PFF) signal (2C1) low, disabling memory. The +40V dc memory supply output is grounded by a detection circuit in the power supply approximately 1 millisecond after PFA goes low.

When power is restored, PFA is held low and +40V dc is held at ground until the ac line voltage is greater than 105V ac and all dc voltages (except +40V dc) rise above threshold. The +40V dc clamp to ground is removed. PFA goes high 15 milliseconds after the +40V dc output is within 4 percent of threshold. The positive-going edge of PFA triggers a power-up sequence and PFF is asserted to memory in less than 2 microseconds. PFF high initiates execution of the RESTORE routine and a return to the program in process when the power was lost.

Figure 4-1 illustrates power supply-to-PF/R timing.



NOTES:

1. POWER TURN ON
2. ALL DC VOLTAGE EXCEPT +40 MEMORY SUPPLY REGULATED
3. +40V dc REGULATED TO WITHIN 4 PERCENT
4. DELAY BEFORE THE POWER FAILURE ALARM (PFA) SIGNAL GOES HIGH
5. POWER FAILURE FEEDBACK (PFF) SIGNAL RAISED
6. EXECUTION OF RESTORE ROUTINE AND INTERRUPTS ENABLED (400µsec MAX)
7. POWER TURN OFF (EARLIEST POSSIBLE DETECTION)
8. POWER SUPPLY DETECTION OF POWER LOSS
9. EXECUTION OF SAVE ROUTINE. PF/R DETECTS THE HALT INSTRUCTION AND SETS PFF LOW, DISABLING THE MEMORY
10. +40V dc DECAYS, DISABLING MEMORY PRIOR TO OTHER DC VOLTAGES DECAYING BELOW REGULATION BAND

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Figure 4-1. 620/f Power Supply-to-PF/R Timing

4.2 POWER-DOWN SEQUENCE

When power is on, control sequencer logic flip-flops PFQ1 (2C2), PFQ2 (2C2), and PFQ4 (2B3) are set. When power is lost, PFA goes low and remains low as long as the power failure conditions are true. PFA low and the timing out of the one-shot (2C3) resets PFQ1. PFQ2 being set when PFQ1 is reset enables the interrupt request logic, which places IURX–C low (2B1), AB05– (2B1), and PFACT– low (2B1) on the AB bus to the CPU to request an interrupt, define the interrupt address, and inhibit the priority memory access (PMA) and direct memory access (DMA) circuits, respectively. As power goes down, the one-shot sets, preventing the premature initiation of a power-up cycle.

The CPU, after executing the instruction in process when the PF/R interrupt is requested, places the Interrupt Acknowledgement (IUAX–C) signal (2D4) on the AB bus to the PF/R, jumps to the interrupt address of the SAVE routine (040), and executes the routine. During this time, the enabled interrupt priority logic generates PRN1X– high (2B1) to inhibit all other interrupts.

A halt instruction at the end of the SAVE routine (section 4.5.1) produces ST1 (2B4), which resets PFQ4 (2B3). The power-up/power-down logic is enabled and asserts PFRST– (2C1) to reset the system and set PFF low. BM09–, BM11–, OPECB–, and OPTEI– are sent to the CPU data loop logic to load a NOP instruction in the I register. PFF low disables the memory, preventing further program-processing. Approximately 2 milliseconds after PFA goes low, the power supply grounds the +40V dc memory supply output, disabling both the CPU and memory.

Figure 4-2 illustrates the power-down sequence timing.

SECTION 4
THEORY OF OPERATION

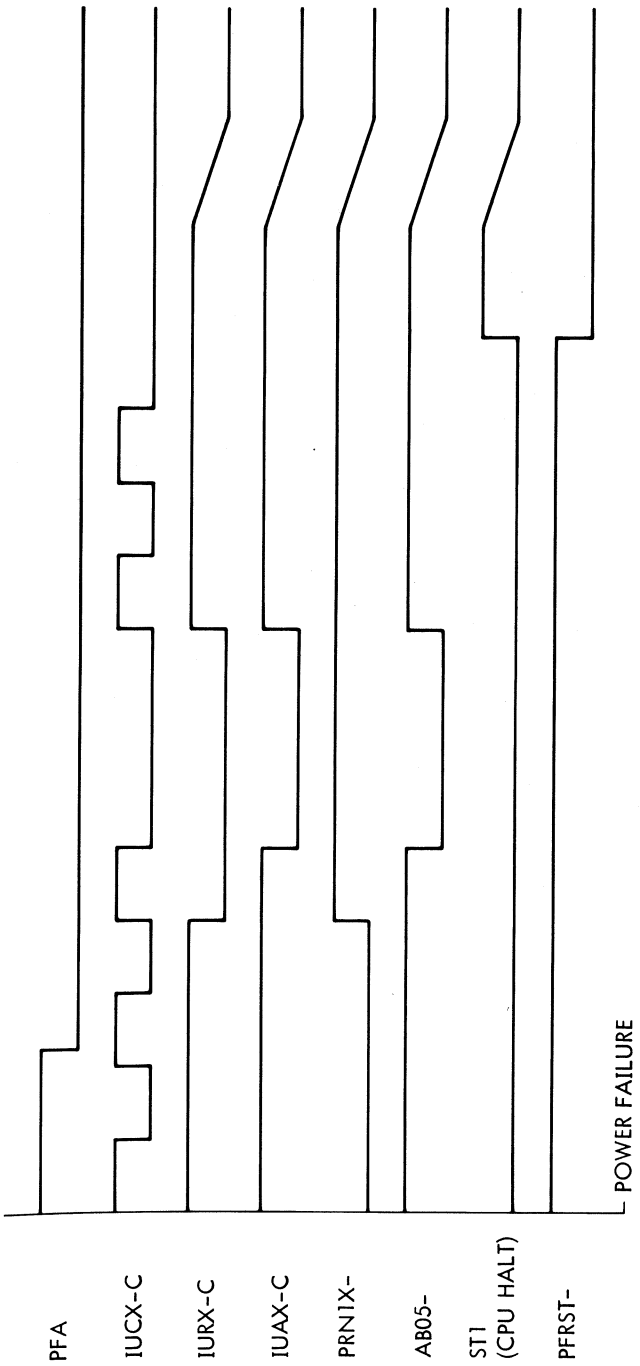

Figure 4-2. Power-Down Timing

4.3 POWER-UP SEQUENCE

When power is restored to the system, PFQ4 is reset by capacitor C1 (2B3). The power-up/power-down logic asserts BM09–, BM11–, OPECB–, and OPTEI– low to the CPU data loop logic, which loads a NOP instruction in the I register. PFRST– low produces a system reset. CPU operations are disabled until PFA goes high 15 milliseconds later. With PFA high, PFQ4 sets. The power-up/power-down logic no longer asserts BM09–, BM11–, OPECB–, and OPTEI–, the system reset is removed, and IUCX–C is enabled, thus enabling the control sequencer logic.

With the control sequencer logic enabled, PFQ1 sets and PFQ2 remains reset. In this state, the control sequencer logic sets PFOS, and, approximately 900 nanoseconds later, the system start logic generates PFLST – (2A1) to put the CPU in run mode. The PF/R interrupt request logic transmits IURX–C, AB01–, and AB05– on the AB bus to the CPU to request an interrupt and define the interrupt address. PFACT– inhibits the PMA and DMA circuits.

The CPU executes the NOP instruction previously loaded in the I register, places IUAX – C low on the AB bus to acknowledge the interrupt request, jumps to the interrupt address (042) of the SAVE routine, and executes the routine. During this time, PRN1X– high disables all other interrupts. This signal is asserted when the PFOS is set, either PFQ1 or PFQ2 is reset, or PRM1X– (2A4) is low.

After executing the RESTORE routine, the CPU jumps to the next instruction of the program in process when power was lost and reenables system interrupts. PFQ1, PFQ2, PFQ3, and PFQ4 are set, PFLTCH is reset, and the control sequencer logic is quiescent until further power failure processing is required.

Power-up sequence timing is illustrated in figure 4-3.

SECTION 4
THEORY OF OPERATION

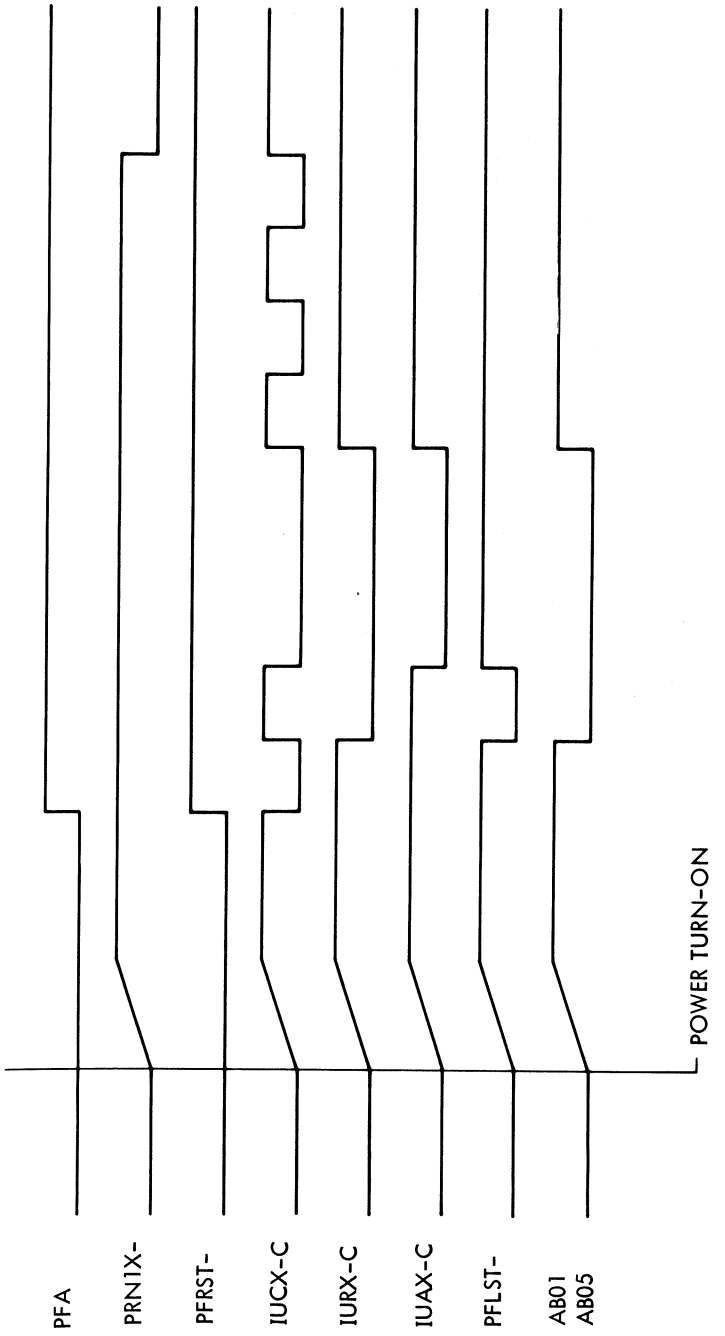

Figure 4-3. Power-Up Timing

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4.4 MNEMONICS

PF/R signal mnemonics are listed alphabetically in table 4-1. The source column lists the location of the signal's source on logic diagram 91C0260 (section 6). The first number is the drawing sheet number, and the following letter and number, the location coordinates. Each signal's function is briefly described.

Table 4-1. PF/R Mnemonic Definitions

Mnemonic	Source	Description
AB01-05	2A1 2B1	Internal I/O bus (AB) lines; bits 1 and 5 used to generate interrupt addresses (power-down interrupt address 040 and power-up, 042)
ALC–	2B4	Alternate clock; a free-running CPU clock
BM09– BM11–	2D1	External entry to adder (ALU) bits 9-11; loads a NOP instruction into the I register
IUAX–C	2D4	Interrupt acknowledgement
IUCX–C	2D4	Interrupt clock
IURX–C	2B1	Interrupt request
OPECB–	2C1	Enables BMxx to adder (ALU); loads a NOP instruction into the I register
OPTEI–	2C1	Enables I register data and clock; loads a NOP instruction into the I register

SECTION 4
THEORY OF OPERATION

Table 4-1. PF/R Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
PFA	2C4	Power failure alarm from the 620/f power supply; high for power-up and low for power-down
PFACT–	2B1	Power failure active; inhibits PMA and DMA
PFALC–	2B4	Alternate clock; internal free-running clock
PFCLMP	2B4	Clamp; resets PFQ4 when PFPFA– is true
PFENBA	2B3	Enable amplified
PFF	2C1	Power failure feedback; PF/R response to PFA. When high, enables the memory
PFHLD	2B3	Hold; when high, holds PFQ4 – high
PFIEB	2A2	Internal interrupt address enable
PFIRQ	2A2	Internal interrupt request
PFIUAX	2D4	Internal interrupt acknowledgement
PFIUCX	2D4	Internal interrupt clock
PFLH2	2A2	Latch; inverted from PFLTCH
PFLST–	2A1	Power failure start signal; sent to the CPU to put the computer into the run mode
PFLTCH	2A3	Latch; indicates computer reset

Table 4-1. PF/R Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
PFOCAP	2C3	One-shot capacitor connection
PFORES	2C3	One-shot resistor connection
PFOSG	2C4	One-shot grounded input connection
PFOS	2C3	One-shot output
PFPFA–	2C3	Internal power failure alarm
PFPULL	2C4	Pull-up resistor connection
PFPRMX	2A4	Internal power failure interrupt priority input
PFQ1	2C2	Least-significant control sequencer flip-flop
PFQ2	2C2	Most-significant control sequencer flip-flop
PFQ3	2A2	Start pulse generator flip-flop
PFQ4	2B3	Initializing flip-flop; set when power is on
PFRST–	2C1	Power failure reset; sent to the CPU for system reset
PFST1 and 2	2B3	Power failure control sequencer state 1 and 2
PRM1X–	2A4	Power failure interrupt priority input
PRN1X–	2B1	Power failure interrupt priority output
ST1	2B4	CPU halt state; indicates CPU is not executing a program

4.5 PROGRAMMING

4.5.1 Considerations and Restrictions

The user writes the PF/R SAVE and RESTORE service routines. During power-down interrupt addresses 040 and 041 process the SAVE routine and during power-up interrupt addresses 042 and 043 process the RESTORE routine.

If the computer is in the halt mode during a power loss, the PF/R interrupt request is not acknowledged, the memory and CPU are immediately disabled, and the contents of the volatile registers are lost.

If the program instruction in process when power is lost is a multilevel addressing instruction, the CPU's acknowledgement of the PF/R interrupt request can be delayed indefinitely.

A halt instruction must be located at the end of the SAVE routine. The halt indicates that the SAVE routine has been executed.

The user should program a halt flag in his service routine to indicate that power failure occurred in the halt mode and to prevent spurious data being loaded in the volatile registers.

The RESTORE routine execution time must not exceed 400 microseconds, and the SAVE routine, 300 microseconds.

4.5.2 Sample Program

Table 4-2 shows a typical PF/R service routine.

Table 4-2. Typical Service Routine

Label	Mnemonic	Operand	Comment
	ORG	040	
	JMPM	PWDN	
	JMP	PWRU	
		POWER-DOWN PROCESSOR (SAVE)	
	ORG	02203	
PWDN	ENTR	0	
	STA	SAVA	SAVE A,B,X REGISTERS
	STB	SAVB	
	STX	SAVX	
	TZA		CHECK/SAVE OVERFLOW
	DATA	005511	INCR A IF OVFL SET
	STA	SAVO	
	INR	HLTF	SET PF/R FLAG
PHLT	HLT		
		POWER-UP PROCESSOR (RESTORE)	
PWRU	LDA	HLTF	CHECK PWR-UP IN RUN
	JAZ	PHLT	
	TZA		CHECK PF/R FLAG
	STA	HLTF	

Table 4-2. Typical Service Routine *(continued)*

Label	Mnemonic	Operand	Comment
	(Coding to reinstate 620/f optional hardware after a power failure must be defined here. The total execution time not to exceed 100 microseconds.)		
	LDA	SAVO	SET UP OVFL FLAG
	JAZ	* + 3	
	SOF		
	LDA	SAVA	RETURN A,B,X REGISTERS
	LDB	SAVB	
	LDX	SAVX	
	JMP*	PWDN	RETURN TO PROGRAM
SAVA	DATA	0	
SAVB	DATA	0	
SAVX	DATA	0	
SAVO	DATA	0	
HLTF	DATA	0	
	END		

SECTION 5
MAINTENANCE

PF/R maintenance consists of running the PF/R test program, troubleshooting, and making repairs, if required. The PF/R test program (part number 92A0102-008), described in the 620 test programs manual (document number 98 A 9908 960), in conjunction with the 620/f maintenance manual (document number 98 A 9908 050), helps isolate an error condition. Troubleshooting is facilitated by familiarization with the operation of the PF/R and use of the logic diagram (section 6).

5.1 EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the PF/R.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM265 Extender Card, part number 44P0437

d. CPU Extender Cables

e. Card Puller, Titchener type 1731

f. Squarewave generator

g. Autotransformer, Variac or equivalent

5.2 TEST PROGRAM

The PF/R test program is an integral part of the MAINTAIN II test program system. It is provided as part of the regular troubleshooting package for the 620/f computer.

PF/R operation should be periodically checked using the PF/R test program, under the control of the test executive program (part number 92A0107-001). This test verifies that volatile registers and memory are not modified by a loss of power. Malfunctions are reported in the form of error messages and/or codes.

The PF/R test program is described in detail in the 620 test programs manual (document number 98 A 9908 960).

SECTION 5
MAINTENANCE

5.3 TROUBLESHOOTING

With the computer turned off and the control panel opened on its hinges, disconnect the CPU tray from the motherboard. Extend the CPU tray out the front of the mainframe and connect an extender cable between CPU tray connectors P1, P2, and P3 and backplane connectors J8, J9, and J10. Firmly attach the CPU tray to a bracket mounted on the front of the mainframe.

After removing the card retainer bar, disconnect PFA at connector P1, pin 12. A suggested method of disconnecting the signal is to place masking tape on P1-12 so that PFA is isolated. Adjust the squarewave generator for a 250-Hz output, with a voltage swing of from 0 to 4 volts. With the squarewave generator turned off, connect the output (PFA simulated) to component location D2, pin 1.

Install the PF/R card (DM289) on an extender card (part number 44P0437). Turn on the squarewave generator.

The computer can then be turned on to begin troubleshooting.

5.3.1 Input Power

Verify +5V dc ± 5 percent and common (ground) at the following connector locations:

+5V dc	Common
P1-75	P1-1
P1-78	P1-2
P1-79	P1-3
P1-80	P1-4
P3-1	P3-77
P3-2	P3-78
P3-3	P3-79
P3-4	P3-80

5.3.2 Signal Test

Load the PF/R test program, following the directions given in the 620 test programs manual (document number 98 A 9908 960). The program responds to power-down and power-up sequences initiated by the test operator. With the PF/R cycling in the system-reset/power-up/power-up-quiescent/power-down sequence, and, using an oscilloscope, verify that the signals listed in table 5-1 are generated. When testing is complete, reconnect PFA at P1-12.

Table 5-1. Signal Test Summary

PF/R State	Signal	Location	Condition
System Reset	PFQ4	C2-9	High-to-low transition (start of PF/R state)
	PFST1	C4-6	Low-to-high transition (end of PF/R state)
	PFQ2	C3-8	Low
	PFQ1	B3-8	Low
	PFLTCH	D2-8	High
	BM09–	P1-5	Low
	BM11–	P1-6	Low
	OPTEI–	P1-8	Low
	OPECB–	P1-7	Low
	PFRST–	P1-10	Low
	PFF	P1-13	Low
	PFACT–	P1-11	Low
Power-Up	PFST1	C4-6	Low-to-high transition (start of PF/R state)
	PFST1	C4-6	High-to-low transition (end of PF/R state)
	PFST2	C4-8	Low
	PFLTCH	D2-8	High
	IURX–C	P1-14	Low
	PRN1X–	P1-23	High
	PFLST–	P1-9	Negative pulse of 450 nsec < time < 900 nsec
	PFOS–	A3-6	Negative pulse of 420 μsec < time < 580 μsec

SECTION 5
MAINTENANCE

Table 5-1. Signal Test Summary *(continued)*

PF/R State	Signal	Location	Condition
Power-Up *(continued)*	AB01– C	P1-15	Low when IUAX– C is asserted
	AB05–	P1-16	Low when IUAX– C is asserted
	IUAX– C	P1-19	Assertive
Power-Up Quiescent	PFST1	C4-6	High-to-low transition (start of PF/R state)
	PFST2	C4-8	Low-to-high transition (end of PF/R state)
	PFQ2	C3-8	High
	PFQ1	B3-8	High
Power-Down	PFST2	C4-8	Low-to-high transition (start of PF/R state)
	PFQ4	C2-9	High-to-low transition (end of PF/R state)
	PFST1	C4-6	Low
	IURX– C	P1-14	Low
	PRN1X–	P1-23	High
	PFACT–	P1-11	Low
	PFLTCH	D2-8	Reset
AB05 – P1-16 Low when IUAX – C is			asserted
	PFQ4	C2-9	Reset when CPU halts

5.3.3 Performance Test

Verifying the performance of the PF/R in the 620/f computer system requires use of the PF/R test program. The 620 test programs manual describes loading and operating procedures, expected results, and error conditions; refer to document number 98 A 9908 960. In this test, power-down/power-up sequences are initiated by turning power off and on from the 620/f control panel.

5.3.4 Marginal AC Power Test

To verify that the PF/R properly initiates a power-down sequence when ac power is below 105V ac, plug the 620/f ac power line in a heavy-duty autotransformer, and run the performance test (section 5.3.3), leaving the control panel power switch ON. Adjust the autotransformer for 110V ac and slowly change the voltage to 104V ac. A power-down sequence should be initiated when input goes below threshold.

5.4 REFERENCE DOCUMENTS

In addition to this manual, the documents listed below are useful aids to understanding and maintaining the PF/R.

a. 620/f Reference Handbook (98 A 9908 001)

b. 620/f Maintenance Manual (98 A 9908 050)

c. 620 Test Programs Manual (98 A 9908 960)

d. DM256 Assembly Drawing (44D0483-000)

e. DM256 Logic Diagram (91C0260)

f. DM256 Wire List (95W0722)

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains the logic diagram and parts information for the PF/R.

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS
   1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C16	C3A C7-12

REFERENCE DRAWINGS	
44D0483	ASSEMBLY
44P0483	PARTS LIST
95W0722	WIRE LIST
40D0457	P.W. BOARD
97D0535	ARTWORK
97D0536	SILKSCREEN (COMP.)
97D0537	SILKSCREEN (CKT)
97D0541	SOLDER MASK

DR MANCARELLA	4-27-71	
CHK WKO	4/30/71	
DSGN ——		
ENGR G. C. GRAY	12/14/70	
APPDA. WHITCOMB	12/14/70	
APPD C. NEAT	12/14/70	

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2722 michelson drive / irvine / california / 92664

TITLE
LOGIC DIAGRAM-POWER FAIL/RESTART

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0260	D

SCALE —— 620/f-14 SHEET 1.0

1/70 DIETERICH-POST CLEARPRINT 1000H-B

CONNECTOR P1

PIN	FUNCTION	SHEET
1	+5V	
2	GRD	
3	+5V	
4	GRD	
5	BM09-	7.0
6	BM11-	7.0
7	OPECB-	7.0
8	OPTEI-	7.0
9	PFLST-	6.0
10	PFRST-	7.0
11	PFACT-	6.0
12	PFA	7.0
13	PFF	7.0
14	IURX-C	7.0
15	AB01-C	7.0
16	AB05-C	7.0
17		
18		
19	IUAX-C	6.0
20	IUCX-C	6.0
21	PRMIX-	7.0
22	STI	6.0
23	PRNIX	7.0
24	ALC-	6.0
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
40		

CONNECTOR P1

PIN	FUNCTION	SHEET
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
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65		
66		
67		
68		
69		
70		
71		
72		
73		
74		
75		
76		
77	+5V	
78	GRD	
79	+5V	
80	GRD	

CONNECTOR P2

PIN	FUNCTION	SHEET
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
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20		
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22		
23		
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25		
26		
27		
28		
29		
30		

NOTE: P2 AND P3 NOT USED

CONNECTOR

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0260	D
SCALE		SHEET 4.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8

CONNECTOR P3

PIN	FUNCTION	SHEET
1	+5V	
2	GRD	
3	+5V	
4	GRD	
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20	THESE PINS RESERVED FOR REAL TIME CLOCK PORTION OF THE BOARD.	
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
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36		
37		
38		
39		
40		

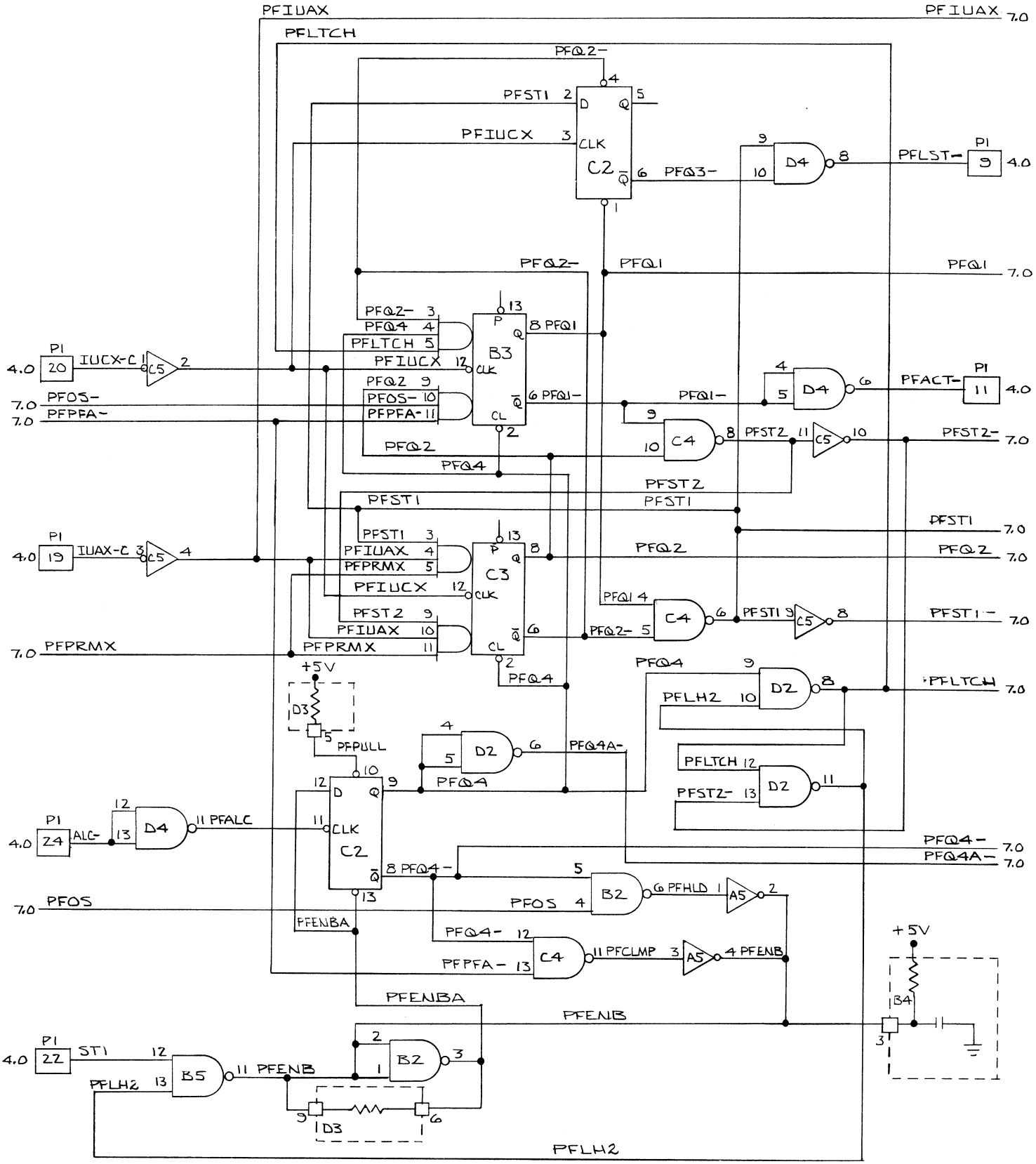
CONNECTOR P3

PIN	FUNCTION	SHEET
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
55		
56		
57		
58		
59		
60	THESE PINS RESERVED FOR REAL TIME CLOCK PORTION OF THE BOARD.	
61		
62		
63		
64		
65		
66		
67		
68		
69		
70		
71		
72		
73		
74		
75		
76		
77	+5V	
78	GRD	
79	+5V	
80	GRD.	

CONNECTOR

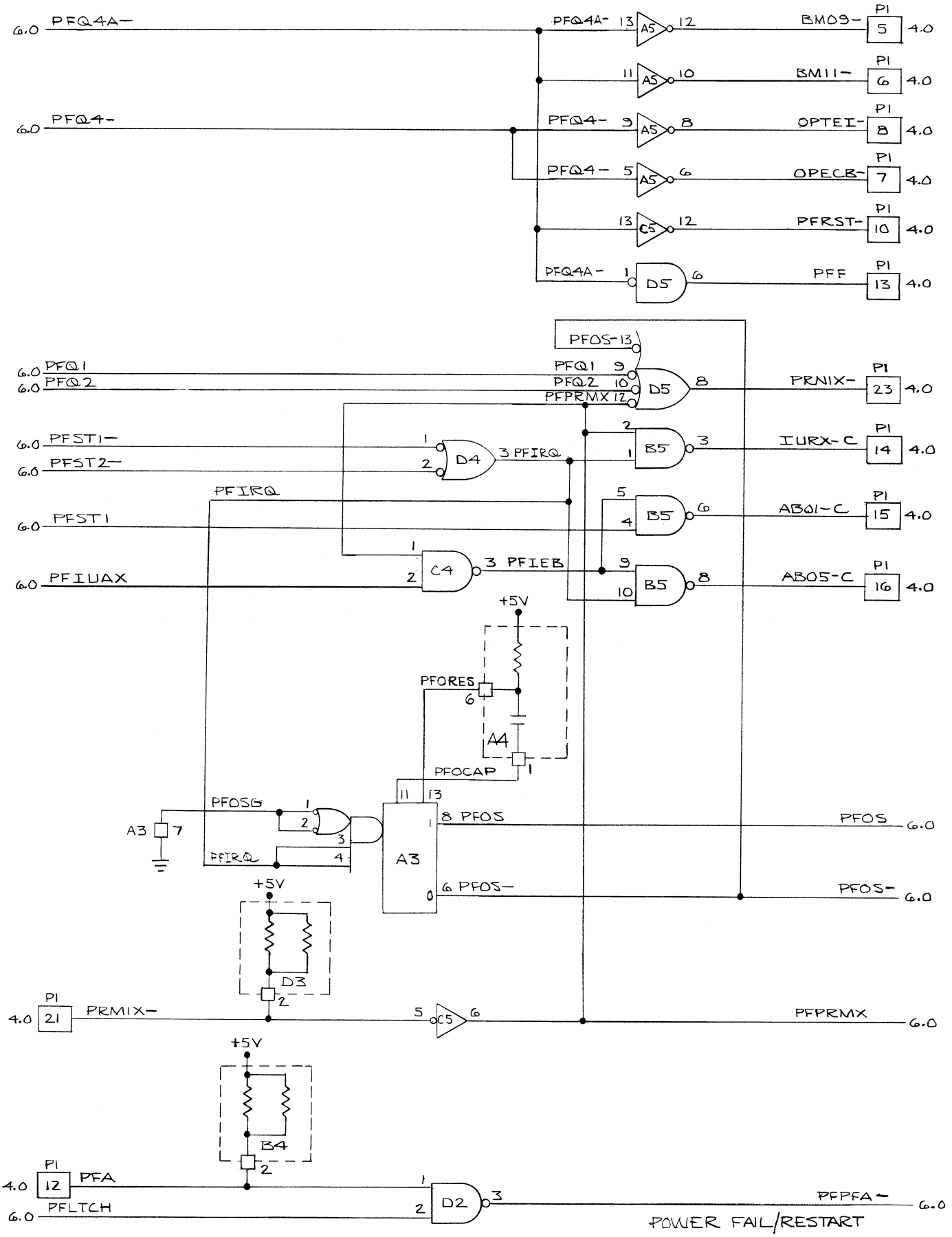
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0260	D
SCALE		SHEET 5.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8



POWER FAIL/RESTART

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0260	D
SCALE		SHEET 6.0	



POWER FAIL/RESTART

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0260	D
SCALE		SHEET 7.0	

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DWG. NO. 44P0483

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				REF	REF	REF	–	44D0483C	ASSEMBLY		
				REF	–	REF	–	91C0260D	LOGIC DIAGRAM		
				REF	–	REF	–	95W0722D	WIRE LIST		
				REF	–	REF	–	98A0579A	TEST SPEC		
				REF	REF	–	–	91B0259A	LOGIC DIAGRAM		
				REF	REF	–	–	95W0721C	WIRE LIST		
				REF	REF	–	–	98A0578A	TEST SPEC		
				1	1	1	1	40D0457-000B	BOARD DETAIL		
				1	–	1	2	49A0019-000	I.C. SN74H40N		
				2	–	2	3	49A0020-000	I.C. SN74H72N		
				1	–	1	4	49A0023-000	I.C. SN74H04N		
				1	–	1	5	49A0524-000	I.C. U6E960129		
				1	–	1	6	49A0039-000	I.C. SN74H00N		
				1	–	1	7	49A0082-001	I.C. SN74H74N		
				3	2	1	8	49A0007-000	I.C. SN7400N		
				4	3	1	9	49A0081-001	I.C. SN7403N		
				3	1	2	10	49A0104-000	I.C. MC3001P		

NEXT ASSY 01A0950 | MODEL NO | APPD A. Whitcomb

TITLE: PARTS LIST
PFR/RTC ASSEMBLY

REV	X_1	X_2	A	B	C	D	/	E	F	G	–
EN NO			5106	5167	5244	5269		5343	5347	5365	5377
DATE	11-2-70		12/11/70	4/26/71	4/26/71	4/26/71		4/26/71	4/26/71	4/26/71	4/26/71
DR	GRL										
CHK	AWW										

DWG NO 44P0483 | REV G

SHEET 1 OF 3

96A0017-000B

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DWG. NO. 44P0483

QUANTITY REQ'D PER DASH NO							PARTS LIST			CODE IDENT: 21101	
				002	001	000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				1	1	-	11	49A0575-000	I.C. SN7405N		
				2	2	-	12	49A0005-000	I.C. SN7410N		
				1	1	-	13	49A0006-000	I.C. SN7420N		
				1	1	-	14	49A0010-000	I.C. SN6006N		
				12	12	-	15	49A0012-000	I.C. SN7474N		
				2	2	-	16	49A0022-000	I.C. SN74H11N		
				8	8	-	17	49A0040-000	I.C. SN7404N		
				1	1	-	18	49A0060-000	I.C. SN74H30N		
				1	1	-	19	49A0086-000	I.C MC4006P		
				3	3	-	20	49A0091-001	I.C. SN74193N		
				2	2	-	21	49A0093-001	I.C. SN74H50N		
				3	3	-	22	49A0094-001	I.C. SN74H21N		
				2	2	-	23	49A0099-000	I.C. SN74H108N		
				5	5	-	24	49A0112-000	I.C. SN7493N		
				1	-	1	25	01P0936-000	COMPONENT BD.		
				1	-	1	26	01P0937-000	COMPONENT BD.		
				1	-	1	27	01P0938-000	COMPONENT BD.		
				1	1	-	28	01P0979-000	COMPONENT BD.		
				1	1	-	29	01P0980-000	COMPONENT BD.		
				1	1	-	30	01P0981-000	COMPONENT BD.		
				1	1	-	31	01P1069-000	COMPONENT BD.		

NOTES:

DWG NO 44P0483 REV G

SHEET 2 OF 3

96A0017-001B

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DWG. NO. 44P0483

PARTS LIST

CODE IDENT: 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				66	51	15	32	58A0060-000	CONNECTOR, 14 PIN		
				3	3	-	33	58A0060-001	CONNECTOR, 16 PIN		
				1	1	1	34	16S1057-057	CARD HANDLE		
				1	1	1	35	16S1057-070	CARD HANDLE		
				31	25	6	36	71A0009-003	CAPACITOR, 0.1 uf	C1, 3, 6, 8, 10, 12 THRU 37	
				6	4	2	37	71N0200-225	CAPACITOR, 2.2 uf	C2, 4, 5, 7, 9, 11	
				174	174	174	38	58C0170-000	WIRE WRAP POST		
				0	0	0	39	53A0333-040	WIRE, YELLOW	30 AWG	
				1	-	1	40	49A0061-000	IC. SN74H05N		

NOTES:

DWG NO 44P0483

REV G

SHEET 3 OF 3

96A0017-001B

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