MEMORY PROTECTION

an option for the
Varian Data Machines 620/f
Computer System

Specifications Subject to Change Without Notice

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FOREWORD

The 620/f Memory Protection Manual defines and explains the logical, electrical, and mechanical parameters that control and interface between a Varian Data Machines 620/f computer and the memory protection option.

The six sections of the manual:

- Introduce the memory protection option in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware wirh drawings, parts lists, and wire lists

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1.1 SYSTEM OVERVIEW

The *Model 620/f-05 Memory Protection (MP)* is a mainframe option for the Varian Data Machines 620/f computer system. The MP prevents unauthorized entry into and modification of protected areas of core memory by programs residing in unprotected areas.

A single circuit card contains the entire MP. The MP card plugs into the central processing unit (CPU) tray of the computer.

The MP divides core memory into blocks (or segments) of 512 consecutive words. Under program control, these segments can be selectively designated protected. Segments not specifically designated protected are, therefore, unprotected. The MP stores the protected/unprotected status of the segments in four 16-bit mask registers. These registers can store the status of up to sixty-four 512-word segments. Thus, the MP is suitable for use in any 620/f installation, including the maximum 32,000-word (32K) memory system. Figure 1-1 illustrates typical memory segment assignments.

Using the stored memory-segment status, the MP monitors the address of the current instruction and that of the following instruction and the location specified by the effective address to determine error conditions.

When a program is operating from an unprotected segment, the MP detects the following operations as errors:

a. Program overflow into a protected area

b. Writing in a protected area

c. Jumping to a protected area

d. Executing an I/O instruction in an unprotected area

e. Executing a halt instruction in an unprotected area

If these operations are attempted, the program aborts and jumps to one of eight preassigned memory addresses. From these addresses, the program can be directed to a user-written subroutine for analysis and correction.

SECTION 1
INTRODUCTION

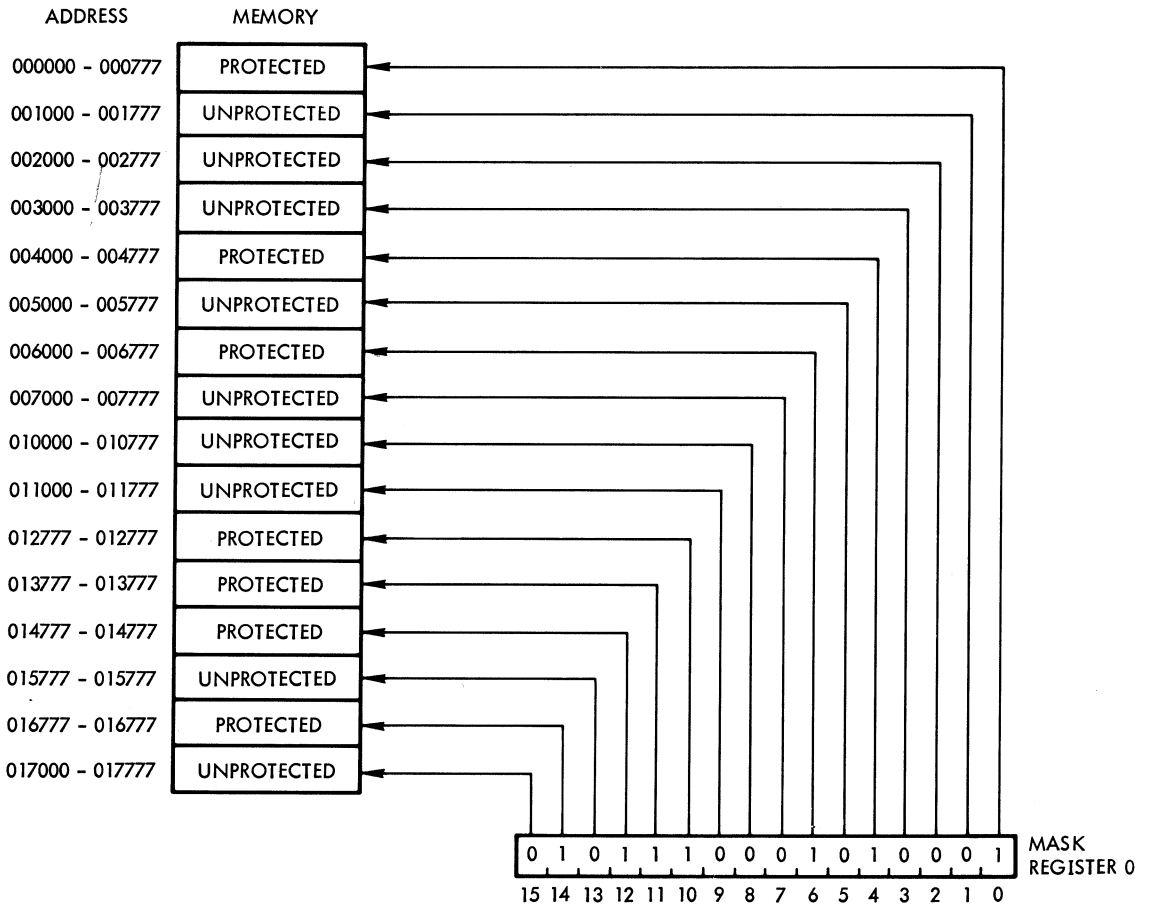

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Figure 1-1. Memory Assignment Example

SECTION 1
INTRODUCTION

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers, and numbers with a leading zero are octal.

1.2 FUNCTIONAL DESCRIPTION

The MP is functionally divided into eleven sections: A-bus receiver, device address decoder, function control logic, segment address register, mask register, segment address status logic, error detector, CPU control logic, interrupt request logic, instruction address register, and A-bus driver (figure 1-2).

1.2.1 A-Bus Receiver

This section buffers the A-bus signals from the CPU and inverts them for use in the mask register, device address decoder, and function control logic.

1.2.2 Device Address Decoder

This section decodes MP device address 045 from A-bus lines AB00 – C through AB05 – C and presents the address, with FRYX – C and IUAX – C, to the function control logic for identification of external control and data transfer instructions to MP.

1.2.3 Function Control Logic

This section responds to external control and data transfer instructions from the CPU by providing control signals to the error detector, mask register, and A-bus driver.

1.2.4 Segment Address Register

This section stores the contents of C-bus bits 9-14 for use by the segment address status logic, instruction address register, and mask register. These six bits comprise the memory segment address.

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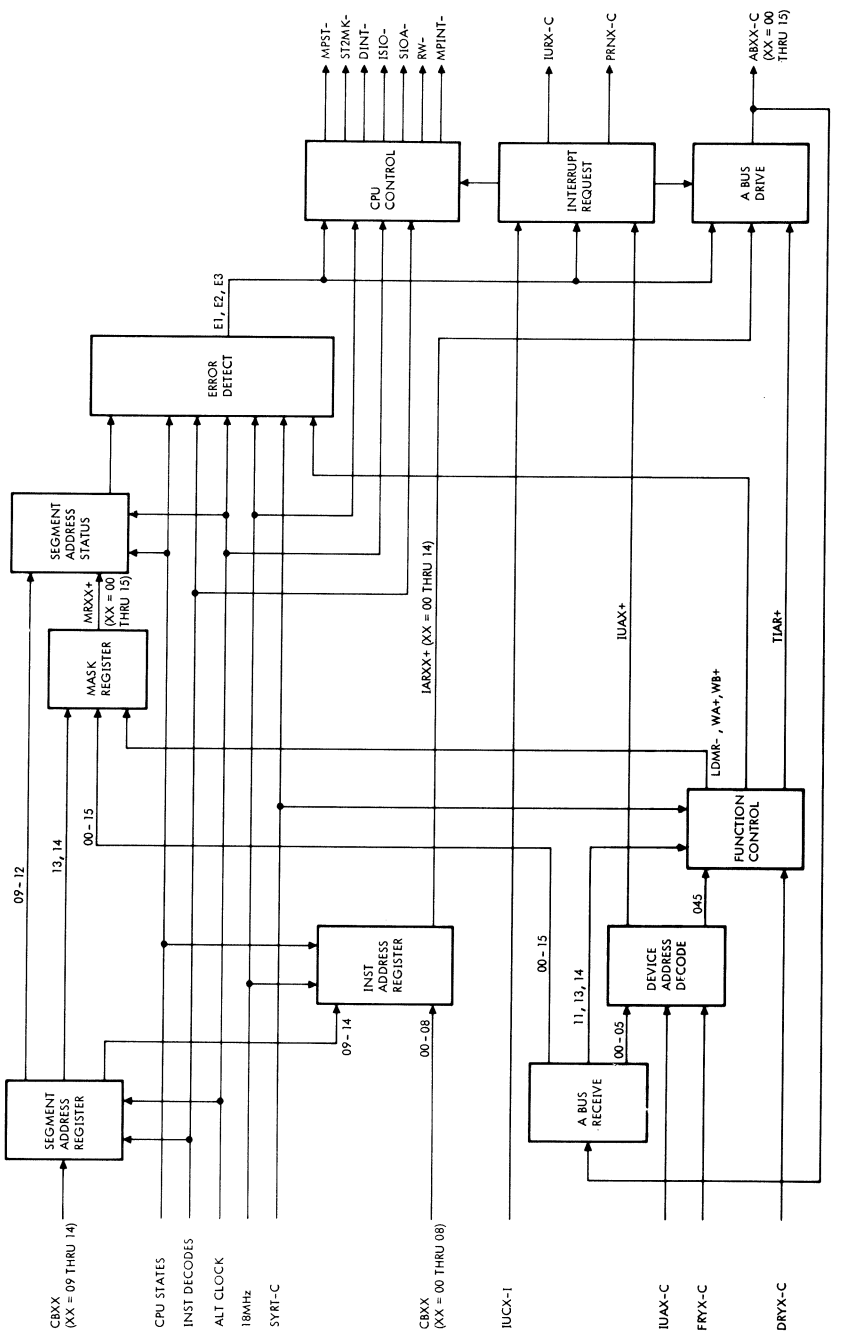

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Figure 1-2. Memory Protection Block Diagram

1.2.5 Mask Register

This section stores the status, protected or unprotected, of all segments of memory. Setting a bit in the mask register protects the corresponding 512-word segment of memory. If a bit is reset, the corresponding segment is unprotected.

During error detection by the MP, mask register outputs, selected by the most significant two bits of the segment address register output, are gated to the segment address status logic.

1.2.6 Segment Address Status Logic

This section decodes the least significant four bits of the 16-bit address stored in the segment address register. The result is ANDed with the corresponding status output of the mask register to determine whether the addressed segment of memory is protected or unprotected. The status thus determined is gated to the error detector and represents the status of the effective address or of the current word.

1.2.7 Error Detector

This section detects and stores error conditions as determined by the segment address status logic, CPU state, CPU instruction, and timing. Error conditions remain stored until the resultant interrupt cycle is complete. Section 1.3 defines the MP-detected error sequences.

1.2.8 CPU Control Logic

This section generates special signals to control CPU operation during an error sequence.

1.2.9 Interrupt Request Logic

This section raises an interrupt request to the CPU when an error is detected by the error detector. It disables lower-priority device controller interrupts during MP interrupt servicing.

1.2.10 Instruction Address Register

At the end of each instruction fetch memory cycle, this section stores the contents of the CPU P register plus one. It is continually updated until an error is encountered, at which time the MP is disabled by the resultant error interrupt. Further updates are thus inhibited until an I/O instruction in the error subroutine reenables the MP.

The nine least significant bits of the instruction address register are loaded from C bus bits 0-8. The six most significant bits are loaded from the output of the segment address register.

1.2.11 A-Bus Driver

This section gates the interrupt address to the A-bus during an interrupt. It also gates the contents of the instruction address register to the A-bus during a data transfer in operation.

1.3 ERROR SEQUENCES

MP detects the following error types: halt, overflow, I/O, write, and jump.

1.3.1 Halt Error

A halt error occurs if:

a. A halt instruction located in an unprotected memory segment is executed.

b. A halt instruction located in any area of memory is executed using an execute instruction that is located in an unprotected segment.

When a halt error is detected, the program completes execution of the halt instruction and the CPU halts after fetching the instruction at the interrupt address. After a 110-nanosecond delay, the MP causes the CPU to enter the run mode, at which time the instruction at the interrupt address is executed.

NOTE

MP does not detect a halt error if the halt is caused by pressing the STEP switch on the computer control panel. To prevent inadvertent use of STEP, lock the control panel switches by setting the power switch to PWR ON DISABLE.

1.3.2 Overflow Error

An overflow error occurs if a program is operating from an unprotected segment and the P register increments into a protected segment.

NOTE

When the last address in an unprotected segment contains the second word of a jump, indexed jump, jump and mark, jump and set return, or bit test instruction for which the jump condition is met, an overflow error does not exist.

When an overflow error is detected, the last instruction in the unprotected segment is executed, even if the second word of a two-word instruction is located in the protected segment. The CPU is then interrupt to address 030.

An I/O, write, or jump error can occur simultaneously with an overflow error.

1.3.3 I/O Error

An I/O error occurs when:

a. Execution of a one-word I/O instruction or the first word of a two-word I/O instruction from a location in an unprotected segment is attempted.

b. Execution of an I/O instruction located anywhere in memory is attempted using an execute instruction in an unprotected segment.

When an I/O error is detected, the I/O instruction in process is executed and the CPU is interrupted to address 022 (or to 032 if an overflow error also exists). In all such cases, however, external control instructions and data transfers between the CPU and device controllers are inhibited; thus, the contents of memory and the A, B, and X registers are not modified by the I/O instruction.

1.3.4 Write Error

A write error occurs when an attempt is made to write into a location in a protected area and either the instruction is located in an unprotected area or the instruction is the result of an execute instruction located in an unprotected area. If a write error is detected, the instruction is executed; however, the write cycle is changed to a read cycle. The CPU is then interrupted to address 024 (or to 034 if an overflow error also exists).

1.3.5 Jump Error

A jump error occurs when an attempt is made to jump or skip to a location in a protected area and the first word of the jump-type instruction lies in an unprotected area. If a jump error is detected, the instruction is executed; however, the write cycle is changed to a read cycle in the case of a jump-and-mark instruction. The CPU is then interrupted to address 026 (or to 036 if an overflow error also exists.)

1.3.6 Intermediate Conditions

In several cases, error detection occurs late in the execution of the instruction or immediately after instruction execution during the forced interrupt wait state. The detection of the error is based in part on conditions existing earlier in the execution cycle and, in the case of execute instructions, before execution is initiated.

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Therefore, the following intermediate conditions are detected and stored by the MP:

a. If a one-word instruction or the first word of a two-word instruction lies in the last address of an unprotected area, the MP sets the W1UP flip-flop during the fetch portion of the execution cycle.

b. If an execute instruction lies in an unprotected area, the EXUP flip-flop is set 110 nanoseconds after the CPU enters state IF1 of the fetch portion of the instruction to be executed. This condition exists until the fetch portion of the execution of the second instruction following the execute instruction.

1.3.7 Multiple Errors

1.3.7.1 ONE-WORD INSTRUCTIONS

Halt, I/O, write, and overflow errors can occur during the execution of a one-word instruction from an unprotected area. Halt, I/O, and write errors are mutually exclusive and cannot occur in combination since they depend on the instruction being executed. However, an overflow error can occur simultaneously with any of them.

When both I/O and overflow errors occur, the overflow interrupt address (030) masks the interrupt address of the I/O error (022), resulting in the composite address of 032.

Similarly, the simultaneous occurrence of write and overflow errors produces the composite address of 034. The overflow error interrupt address (030) masks the interrupt address of the write error (024).

Detection of an overflow error is inhibited during a halt instruction. (Note that a halt error necessarily exists when overflow occurs during a halt instruction.)

1.3.7.2 TWO-WORD INSTRUCTIONS

The following tabulations illustrate possible error combinations during the execution of two-word instructions from an unprotected area.

Both words in an unprotected area, but neither word is in the last address

Instruction	Definite Error	Conditional Error
I/O	I/O	----
Extended write or increment and replace	----	Write
Immediate write or increment and replace	----	Write
Execution (condition met)	----	Halt or I/O, but not simultaneously
Jump, jump and mark, indexed jump, jump and set return, or bit test (condition met)	----	Jump
Skip if register equal (condition met)	----	Jump

First word in the last address of an unprotected area, second word protected

Instruction	Definite Error	Conditional Error
I/O	Overflow, I/O	----
Extended read	Overflow	----
Extended write or increment and replace	Overflow	Write
Immediate read	Overflow	----
Immediate write or increment and replace	Overflow	Write
Execution (condition met)	Overflow	----
Execution (condition not met)	Overflow	----
Jump, jump and mark, indexed jump, jump and set return, or bit test (condition met)	Overflow	Jump
Jump, jump and mark, or bit test (condition not met)	Overflow	----
Skip if register equal (condition met)	Overflow, jump	----
Skip if register equal (condition not met)	Overflow, jump	----

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Second word in the last address of an unprotected area, next area protected:

Instruction	Definite Error	Conditional Error
I/O	Overflow, I/O	----
Extended read	Overflow	----
Extended write or increment and replace	Overflow	Write
Immediate read	Overflow	----
Immediate write or increment and replace	Overflow	Write
Execution (condition met)	Overflow	----
Execution (condition not met)	Overflow	----
Jump, jump and mark, indexed jump, jump and set return, or bit test (condition met)	----	Jump
Jump, jump and mark, or bit test (condition not met)	Overflow	----
Skip if register equal (condition met)	Overflow, jump	----
Skip if register equal (condition not met)	Overflow, jump	----

1.4 SPECIFICATIONS

The MP functional, physical, and electrical specifications are listed in table 1-1.

Table 1-1. Memcry Protection Specifications

Parameter	Description
Organization	Consists of A-bus receiver, device address decoder, function control logic, segment address register, mask register, segment address status logic, error detector, CPU control logic, interrupt request logic, instruction address register, and A-bus driver
Capability	Protects up to sixty-four 512-word memory segments
Operational Modes	Detects halt, overflow, I/O, write, and jump errors
Priority Assignment	Always assigned the highest priority with respect to the DMA/interrupt scheme
I/O Capability	Six external control and eight data transfer instructions
Timing Sources	18-MHz and 9-MHz clocks from CPU
Logic Levels	
Internal	Positive logic:
True:	+2.4 to +5.25V dc
False:	0.0 to +0.45V dc
I/O	Negative logic:
True:	0.0 to +0.45V dc
False:	+2.4 to +5.25V dc

Size	One 3-by-15-inch (7.7 x 38.1 cm) wired-socket circuit card
Interconnection	Plugs into slot 12 of the 620/f CPU motherboard
Input Power	+5.0V dc at 2.5 amperes
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation

It is recommended that Varian Data Machines Customer Service engineers install the MP. Logic diagrams, assembly drawings, and wiring information are provided at the time of purchase.

2.1 PHYSICAL DESCRIPTION

The MP is on a 3-by-15-inch (7.7 x 38.1 cm) wired-socket card (part number 44P0480-000). Circuit elements are intergrated circuits (ICs) and discrete components (figure 2-1). All connections to the MP are made through the 190-terminal card-edge connector that mates with the corresponding connector in the CPU tray.

2.2 SYSTEM LAYOUT AND PLANNING

The MP ciruit card is located in card slot 12 of the CPU tray. The card slots in the CPU tray are numbered 1 through 14 from rear to front as you face the front panel. Figure 2-2 shows the MP card mounted in the CPU tray.

2.3 SYSTEM INTERCONNECTION

The MP ciruit card is inserted into its designated card slot when the CPU tray is extended out the front of the mainframe and held by an extender assembly bolted to the front of the mainframe.

Insert the card into the mounting guides of slot 12 with the component side of the card toward the backplane connectors.

Apply moderate pressure to seat the card-edge connectors firmly into the mating connectors on the CPU tray. To prevent damage to the connectors or to the nylon guides, ensure that even pressure is applied across the top of the card during insertion. Avoid applying excessive pressure on the CPU tray and the extended assembly by supporting them from beneath during card insertion.

The card has ejector handles for unseating it from its mating connectors. To remove a card, lift the inside edge of the ejector handles; then lift the card from the slot.

SECTION 2
INSTALLATION

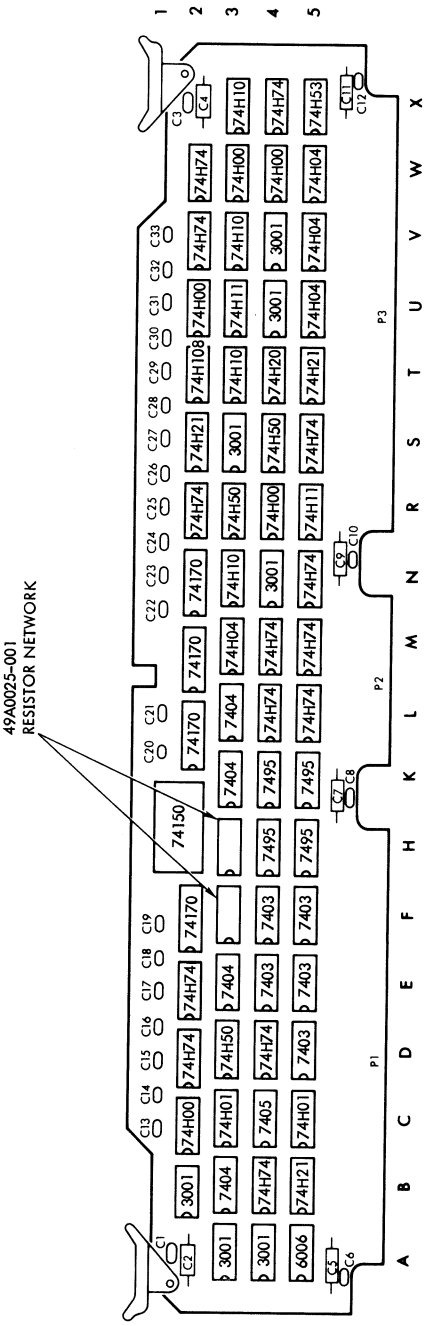

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Figure 2-1. MP Component Layout Assembly

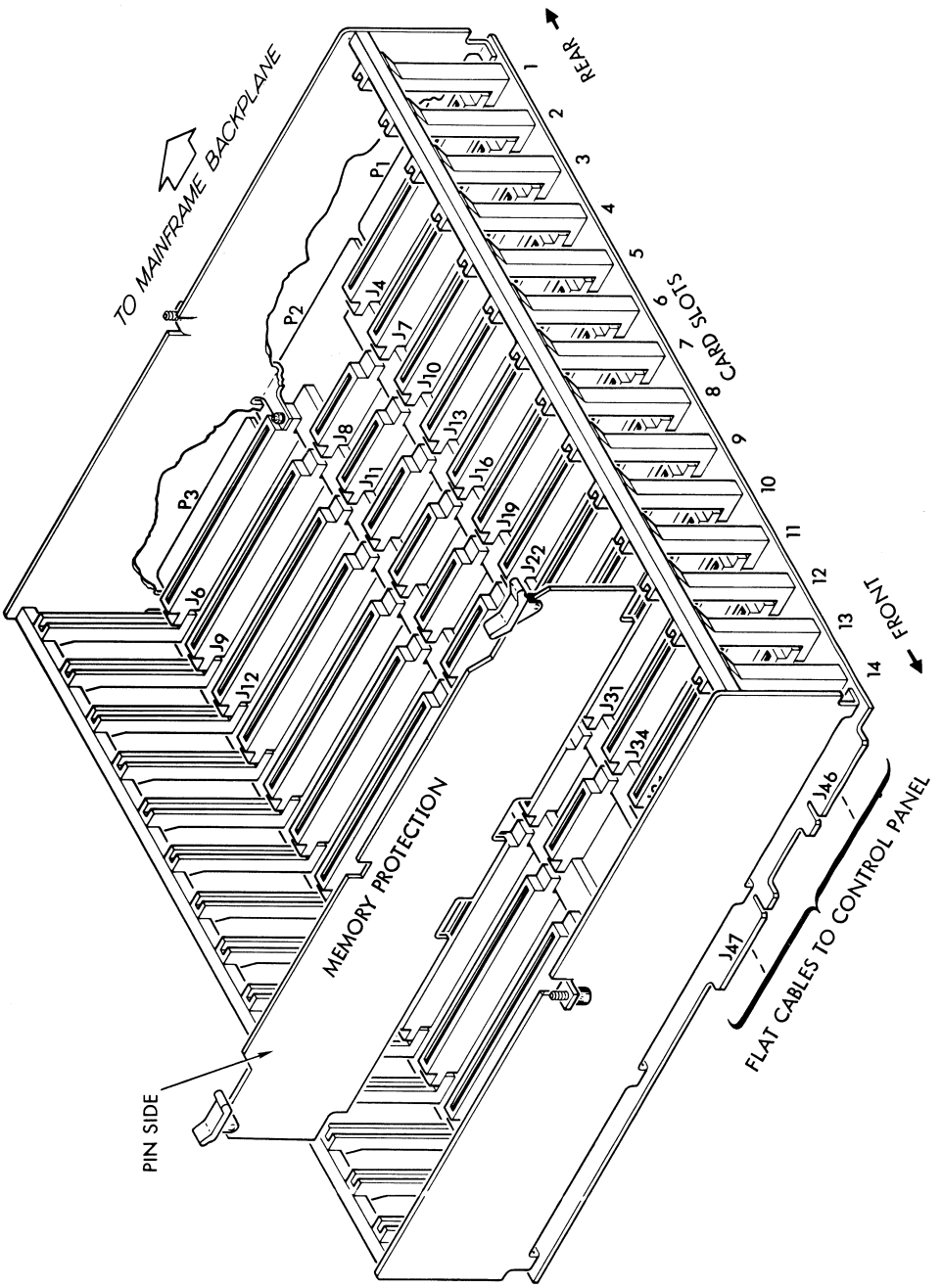

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Figure 2-2. MP Card Location

SECTION 2
INSTALLATION

2.4 SIGNAL INTERFACES

The MP interfaces with the computer via the control lines listed in tables 2-1 and 2-2. A ciruit-card connector pin number follows each signal mnemonic. For definitions of the mnemonics, refer to section 4.

Table 2-1. MP Input Interface Signals

Signal	Pin Number	Signal	Pin Number
AB00 – C	P1-76	CB11	P3-20
AB01 – C	P1-75	CB12	P3-21
AB02 – C	P1-74	CB13	P3-22
AB03 – C	P1-72	CB14	P3-24
AB04 – C	P1-71	DRYX – C	P1-6
AB05 – C	P1-70	DWA	P3-69
AB06 – C	P1-69	DWAI	P1-51
AB07 – C	P1-68	EBT –	P1-31
AB08 – C	P1-67	EL	P3-50
AB09 – C	P1-66	EP	P3-14
AB10 – C	P1-65	EXC	P3-60
AB11 – C	P1-64	EXF	P3-16
AB12 – C	P1-63	EXGR	P1-9
AB13 – C	P1-62	EXGR –	P1-7
AB14 – C	P1-61	FRYX – C	P1-12
AB15 – C	P1-60	HLT	P3-23
ALC –	P1-73	HLTD	P1-58
CB00	P3-5	IF1	P3-10
CB01	P3-6	IF2	P3-33
CB02	P3-7	IF3	P3-34
CB03	P3-8	IJMP	P3-45
CB04	P3-9	INHB1 –	P3-29
CB05	P3-11	INR	P1-47
CB06	P3-12	INTR	P3-46
CB07	P3-13	INTX –	P3-42
CB08	P3-17	IOC –	P3-39
CB09	P3-18	IUAX – C	P1-8
CB10	P3-19	IUCX – C	P1-10
IUR	P1-29	POI	P1-48

Table 2-1. MP Input Interface Signals *(continued)*

Signal	Pin Number	Signal	Pin Number
JSR –	P3-43	RUN +	P1-49
JUMP –	P3-41	SKIP2 –	P1-73
OF1	P1-38	SRE	P3-32
OF2	P3-66	STJMK –	P3-40
OF4	P1-26	ST1	P1-59
OF5 –	P1-18	ST2	P3-26
OPSTO	P3-57	ST2 –	P3-25
OP10 +	P1-50	SYRT – C	P1-17
OSAFC –	P1-37	TESTR	P1-57
PA –	P3-28	XFA	P1-32
		XF1 –	P3-15

Table 2-2. MP Output Interface Signals

Signal	Pin Number	Signal	Pin Number
AB00 – C	P1-76	AB12 – C	P1-63
AB01 – C	P1-75	AB13 – C	P1-62
AB02 – C	P1-74	AB14 – C	P1-61
AB03 – C	P1-72	DINT –	P3-31
AB04 – C	P1-71	ISIO –	P1-56
AB05 – C	P1-70	IURX – C	P1-28
AB06 – C	P1-69	MPINT –	P3-27
AB07 – C	P1-68	MPST –	P3-30
AB08 – C	P1-67	PRN3X –	P1-14
AB09 – C	P1-66	RW –	P1-27
AB10 – C	P1-65	SIOA –	P3-74
AB11 – C	P1-64	ST2MK –	P1-30

SECTION 3
OPERATION

There are no operating controls or indicators on the MP circuit card. Data and control are under CPU program control (refer to section 4.13).

SECTION 4
THEORY OF OPERATION

The following subsections describe the eleven functional sections of the MP: A-bus receiver, device address decoder, function control logic, segment address register, mask register, segment address status logic, error detector, CPU control logic, interrupt request logic, instruction address register, and A-bus driver. The MP mnemonics are listed in section 4.12 and programming considerations are given in section 4.13.

In the following descriptions, numbers in parentheses indicate the location of the chips on the circuit card. The first number locates the sheet; the following letter and number designate the chip location.

4.1 A-BUS RECEIVER

The A-bus receiver buffers the A-bus signals, AB00 – C through AB15 – C (7E3, 7L3, 7K3), from the CPU and inverts them to AB00 + through AB15 + to provide data paths for the mask register, device address decoder, and function control logic functions.

The inverted A-bus signals are routed to the four mask registers to establish the protected and unprotected areas of memory. AB00 + through AB05 + go to the device address decoder to derive the MP device address (8B5). AB06 +, AB07 +, AB08 + (8B4. 8E2), AB11 + (8C3), AB13 +, and AB14 + (8D3) represent the coded external control and data transfer instructions in function control operations.

4.2 DEVICE ADDRESS DECODER

The device address decoder decodes the state of AB00 + through AB05 + (8B5) in the presence of FRYX – C (8C4) and IUAX – C (8B3) to generate the MP Device Address (DAF45) signal (8B5). DAF45 then goes to the function control logic.

4.3 FUNCTION CONTROL LOGIC

External control (EXC) instructions on AB06 +, AB07 +, AB08 + (7K3), and AB11 + (7K3) are decoded and, with DAF45 +, set flip-flops WA (8E2), WB (8E2) and ENMP (8B4). WA + and WB + select a mask register. When AB14 + (7E3) and DAF45 + are true, flip-flop LDM is set. LDM +, with the CPU Data Ready (DRYX – C) signal (8B3), loads the data from the A-bus receiver into the selected mask register.

The ENMP flip-flop (8B4) sets when the MP is addressed by EXC instruction 0100645 and is reset by 0100745. ENMP + activates the instruction address register, segment address status logic, and error detector. The ENMP, LDM, and TIAR flip-flops can be reset by SYRT – C (8B3). When AB13 + (7E3) and DAF45 + (8B5) are true, flip-flop TIAR (8D2) is set to transfer the data on AB00 – C through AB14 – C from the instruction address register to the CPU.

4.4 SEGMENT ADDRESS REGISTER

C-bus signals CB09 through CB14 are used as data inputs to flip-flops SAR09 through SAR14 (9L4, 9L5, 9M5). During the CPU memory access time, SSAR + (9N3) clocks the six flip-flops. SAR13 + and SAR14 + select a mask register. SAR09 + through SAR12 + select one of the 16 outputs of the mask register. SAR09 + through SAR14 + are also routed to the instruction address register during IF3 (state 3 of the CPU instruction fetch cycle).

4.5 MASK REGISTER

The mask register consists of four 4x4 register files. Each register file provides four bits of a selected mask register (7H2).

Each of the four MP mask registers contains 16 bits corresponding to 8,192 words of memory and each mask register bit controls a 512-word segment of memory. If the mask bit is one, the corresponding 512-word segment is protected; if zero, the segment is unprotected. Mask register 0 controls the low-order 8,192 words of memory, and mask register 3, the high-order 8,192 words. The mask register bit assignment is illustrated in figure 4-1.

WA + and WB + select a mask register for writing. LDMR – (8C2) is generated from the function control logic to load the data on AB00 + through AB15 + into a selected mask register. SAR13 + and SAR14 + from the segment address register select a mask register for reading out to the segment address status logic.

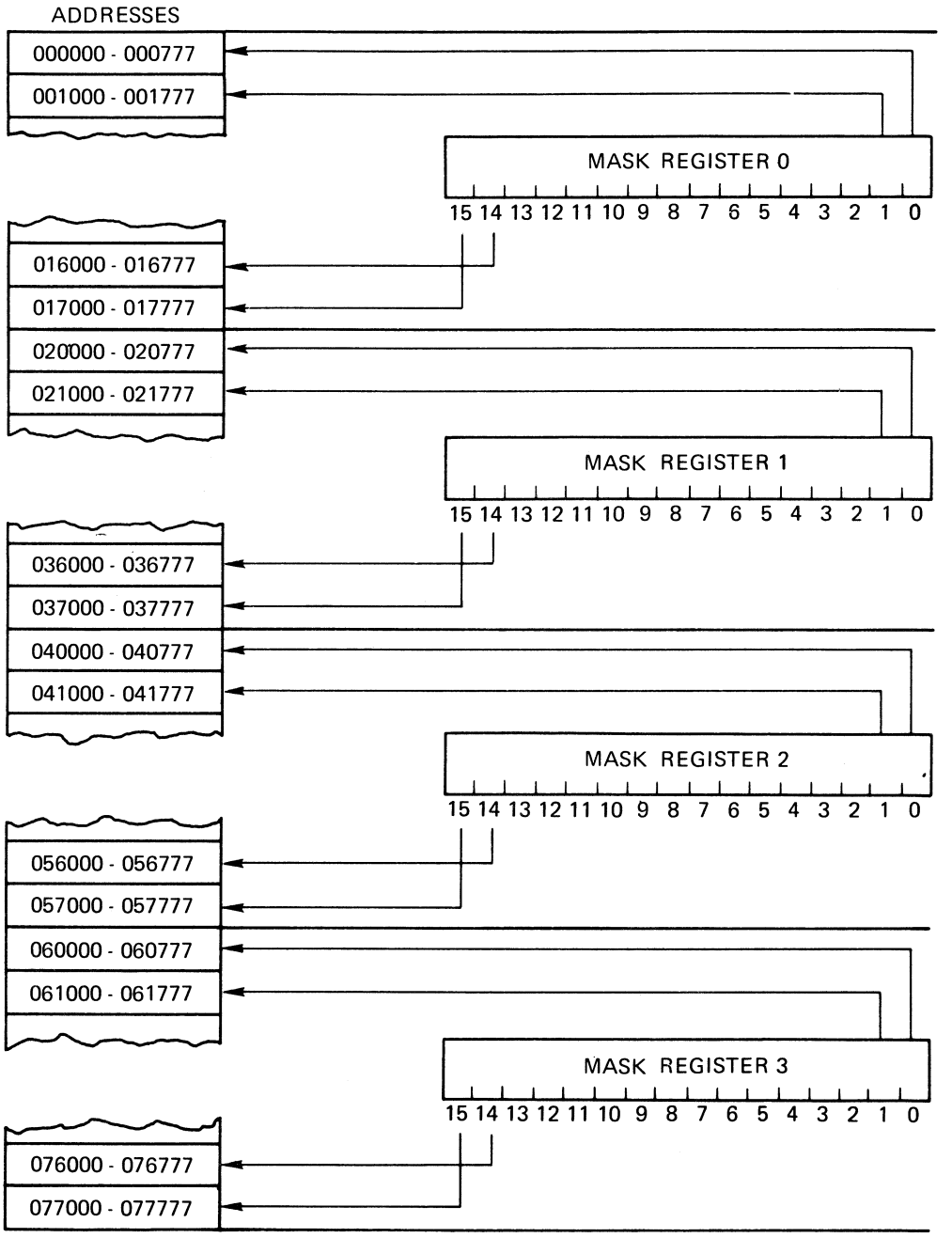

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Figure 4-1. Mask Register Bit Assignment

4.6 SEGMENT ADDRESS STATUS LOGIC

The segment address status logic detects the status of the addressed 512-word segment of memory. The protected/unprotected status of the addressed segment, EAPA + (7M3), is then gated to the error detector as the status of the effective address or as the status of the current word.

SAR09 + through SAR12 + from the segment address register are decoded, and the result selects one of the outputs of the mask register, MR00 + through MR15 + (7F2, 7L2, 7M2, 7N2). The status of the addressed memory segment, EAPA + is output to the error detector. If EAPA + is true, the addressed 512-word segment is protected. If EAPA + is false, it is unprotected.

The CUPA flip-flop (12N5) stores the information that an instruction word or effective address is in an unprotected or protected area. CUPA is clocked by the UDP flip-flop 110 nanoseconds after the P register in the CPU is incremented or changed. The UDP flip-flop is set each time the P register is modified. CUPA is routed to the error detector.

4.7 ERROR DETECTOR

Error detector outputs are routed to the CPU control logic, interrupt request logic, and the A-bus driver. Figure 4-2 shows the error detection timing diagram.

The W1UP flip-flop (15W2) stores the unprotected or protected status of the address of the first word of each instruction. During the instruction fetch cycle of any instruction, detection of the above condition occurs when the CPU enters the IF3 state. If a one-word instruction or the first word of a two-word instruction lies in the last address of an unprotected area, W1UP is set.

The EXGRM flip-flop (15W2) is set by an execute (XEC) instruction. If W1UP is also set, EXUP sets. Detection of this condition occurs 110 nanoseconds after state IF1 of the next instruction-fetch cycle is entered. EXUP remains set until the fetch cycle of the second instruction following the XEC instruction. EXUP – is routed to the error flip-flops.

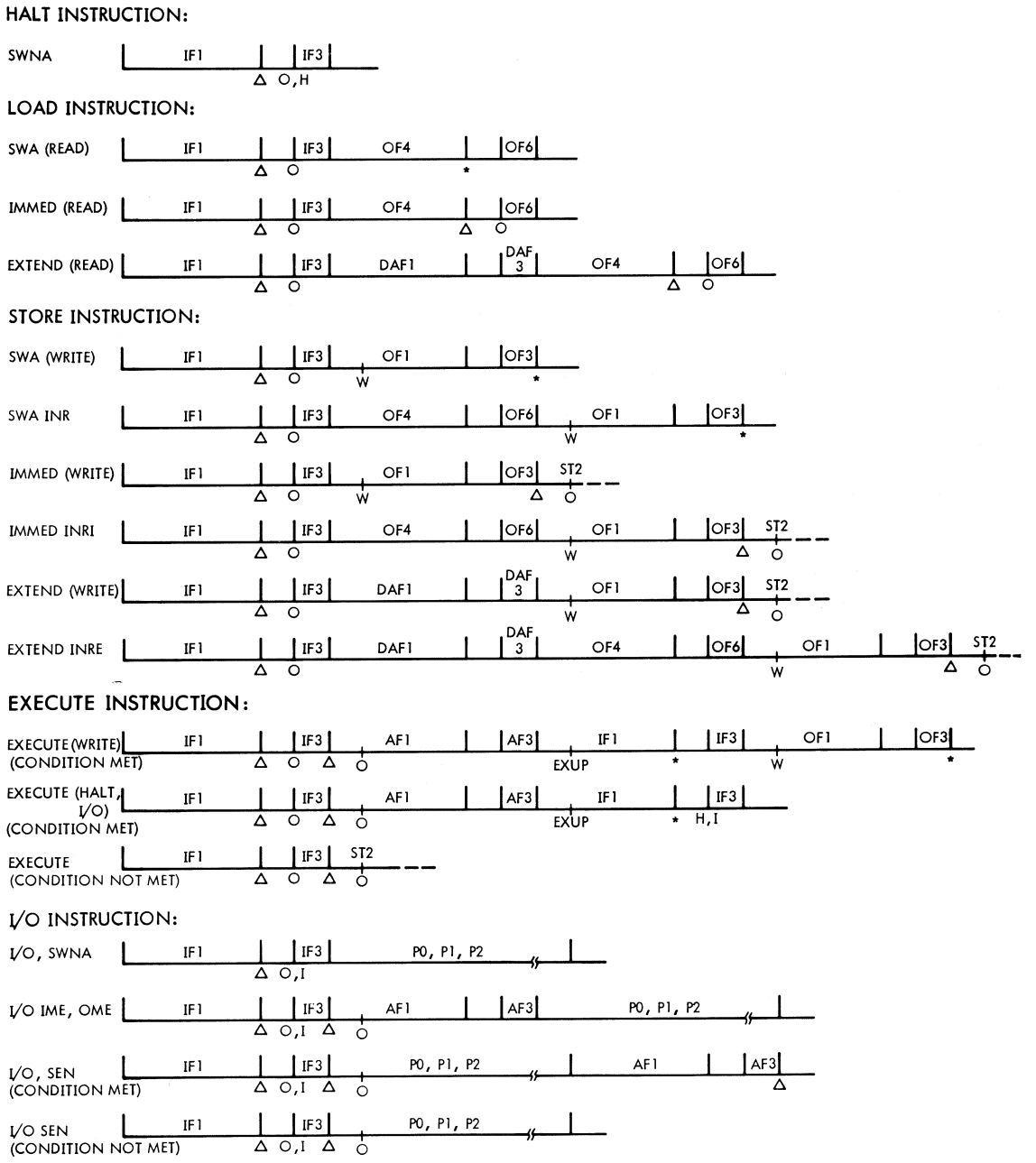

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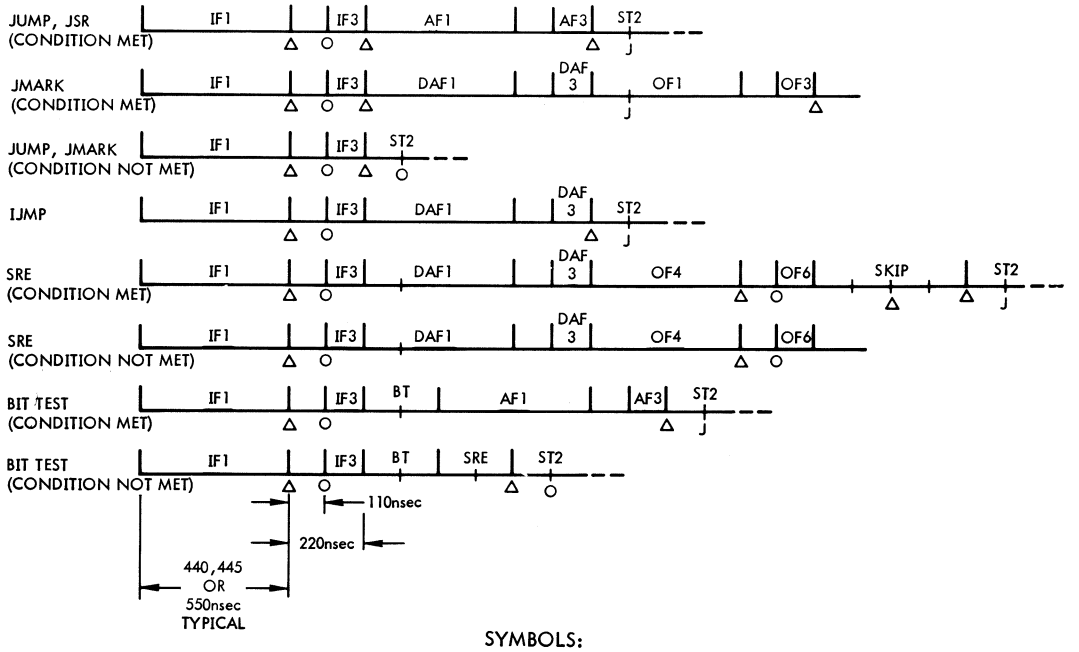
Figure 4-2. Error Detection Timing

SECTION 4
THEORY OF OPERATION

JUMP, JUMP AND MARK INSTRUCTION:



SYMBOLS:

H	=	Halt error
I	=	I/O error
O	=	Overflow
W	=	Write error
J	=	Jump error
△	=	P register contents changed
*	=	P register clocked but contents unchanged

INSTRUCTION ABBREVIATIONS:

SWNA	=	One-word nonaddressing
SWA	=	One-word addressing
INR	=	Increment and replace
IME	=	Input to memory
OME	=	Output from memory
SEN	=	Sense I/O
IMMED	=	Immediate
INRI	=	Increment and replace immediate
EXTEND	=	Extended
INRE	=	Increment and replace extended
BT	=	Bit test
JSR	=	Jump and set return
IJMP	=	Indexed jump
JMARK	=	Jump and mark
SRE	=	Skip if register equal

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Figure 4-2. Error Detection Timing *(continued)*

The AM and BM flip-flops (15T2) comprise a 110-nanosecond counter for control timing and error detection. The counter is held reset except during memory access, the first part of an I/O cycle, or the CPU interrupt wait state ST2. ENCT + (15T3) enables the 18-MHz clock to the counter when the MP is enabled.

The ST2E flip-flop (15V2) stores the CPU interrupt wait state. It is set during all but the first 165 nanoseconds of ST2. ST2E − clocks EB1 in the A-bus driver and ST2E + resets flip-flop EXGRM.

JMGR + (14W4), JMSGR + (14C3), and JSGR + (14W4) are ORed combinations of the jump- and skip-type instruction decodes (14T5) from the CPU instruction register.

JMGR + gates the D input of the JMTF flip-flop (15S5). JSGR + is routed to the CPU control logic as part of the dummy interrupt (DINT) gating logic (13X5).

The JMTF flip-flop (15S5) enables the setting of the E3 overflow error flip-flop (16S5) except during jump-type instructions (excluding skip) for which the test condition is true. If the second word of a two-word instruction is in the last address of an unprotected area and if JMTF is set, an overflow error, E3, is detected.

JMTF is clocked in state IF3 during the execution of two-word addressing instructions (except extended, immediate, and skip if register equal) or in state OF2 for extended and immediate instructions. JMTF is dc reset by the BM flip-flop when the BM flip-flop is set.

The E1 flip-flop (16R2) sets when it detects halt and I/O errors. CE1 − (16N3) clocks E1, and RB − (14U4) resets it. For a halt error, the CPU is interrupted to address 020, and, for an I/O error, to address 022 or to 032 if an overflow error also occurs.

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During the instruction fetch cycle, halt errors are detected upon entry to CPU state IF3. The CPU halts to enter state ST1 after fetching the instruction at the interrupt address. Detection of the halt error causes the MP to hold MPST – true. Thus, CPU reenters the run mode 110 nanoseconds after halting in ST1. MPST – is removed when the error interrupt has been processed.

During the instruction fetch cycle, I/O errors are detected upon entry to CPU state IF3. The contents of memory and of the A, B, and X registers remain unmodified by the I/O instruction when the Inhibit Start I/O (ISIO –) is held true immediately before and during CPU state P0. The MP makes the Simulated I/O Active (SIOA –) signal true 110 nanoseconds after the CPU enters state P0. The CPU steps to state P1 110 nanoseconds later. The MP then makes SIOA – false 110 nanoseconds after entering state P1. The CPU steps to state P2 110 nanoseconds later from which it then exits automatically after another 110 nanoseconds to complete I/O instruction execution.

The E2 flip-flop (16R2) detects write and jump errors. It is clocked by CE2 – (16S2) and reset by RB – .

If an operand store instruction (with either a one-word or the first word of a two-word instruction lying in an unprotected area) attempts to write into a protected area or, if it is being executed by an XEC instruction that lies in an unprotected area, the E2 flip-flop is set, indicating a write error. For a write error, the CPU is interrupted to address 024 (or to 034 if an overflow error also occurs).

All store-type instructions end with an operand store cycle. Write errors are detected 110 nanoseconds after CPU state OF1 of the store cycle is entered to change the write cycle to a read cycle. To change a write cycle to a read cycle, the read/write input (RW –) to the memory must be near OV within 150 nanoseconds after the Memory Start (MST –) signal goes true at the beginning of state OF1.)

The E2 flip-flop is set when a jump error is detected. A jump error occurs when a jump, indexed jump, jump and mark, jump and set return, bit test, or skip if register equal operation into a protected area is attempted from an unprotected area. For a jump error, the CPU is interrupted to address 026 or to 036 if an overflow error also occurs.

A jump error is detected at the beginning of the OF1 portion of a jump and mark operand cycle. Thus, as in the case of the other operand store instructions, the error is detected during the last instruction cycle.

The jump, indexed jump, jump and set return, and bit test instructions end with an address cycle. The final (effective) address is not available until the final address cycle is nearly complete. To provide time for error detection, the Simulated (Dummy) Interrupt (DINT –) signal is held true during AF3 or DAF3 of the last address cycle. The CPU is thus forced to go to the interrupt wait state ST2, and error detection occurs 110 nanoseconds after entering ST2. If no jump error is detected and overflow does not occur, DINT – goes false and the CPU executes the next instruction. If a jump error is detected, DINT – remains true, holding the CPU in ST2 while an interrupt request is issued by the MP.

The optional Skip If Register Equal (SRE) instruction terminates in a special skip cycle, and the final address is not available until late in the final cycle. Jump error detection for an SRE instruction is, therefore, the same as that for a jump instruction.

A jump error cannot occur during the conditional jump instructions if the jump condition is not met. However, overflow errors can occur.

The E3 flip-flop (16S5) detects overflow errors. If a one-word instruction or either the first or second word of a two-word instruction lies in the last address of an unprotected area and the next instruction in sequence lies in a protected area, the E3 flip-flop is set for an overflow error. If the second word of a jump-type or jump and mark instruction lies in an unprotected area, E3 can be dc set by DCE3 – (16T4). E3 is clocked by CE3 – (16S4) and reset by RB – . For an overflow error, the CPU is interrupted to address 030. If an overflow error is detected concurrently with an I/O, write, or jump error, the CPU is interrupted to composite interrupt address 032, 034, or 036, respectively.

For a one-word instruction and the first word of a two-word instruction, overflow errors are detected when the CPU enters state IF3 during the instruction fetch cycle. For the second word of a two-word instruction (except extended), overflow errors are detected 110 nanoseconds after the CPU leaves state IF3. For the second word of an extended instruction, overflow errors are detected when OF6 is entered (read) or 110 nanoseconds after leaving OF3 (write or INR).

With the MP enabled, TIEN + (the first half of CPU state IF2) enables the clock to halt, I/O, and overflow error detection, and to the W1UP flip-flop. TIEN + also enables the clock to the instruction address register.

RB – resets the E1, E2, and E3 flip-flops at the end of the MP interrupt. Resetting the flip-flops causes the IURX (11B4) and EB1 (11D4) flip-flops to reset. The error flip-flops can be reset by SYRT – C or by the INTI flip-flop (10M4). INTI – inhibits error detecton.

4.8 CPU CONTROL LOGIC

The CPU control logic generates seven special signals to control CPU operations: ISIO –, SIOA –, MPINT –, DINT –, ST2MK –, MPST –, and RW –.

When an error is detected during execution of an I/O instruction, the ISIO gate (13C5) and SIOA flip-flop (13X4) are activated. ISIO – inhibits the CPU start I/O signal to the I/O section, thereby inhibiting I/O operations. SIOA – simulates the I/O active signal, causing the CPU to proceed through the I/O sequence (P0, P1, and P2) even though the I/O section is inhibited.

The MPINT gate (13A5) provides parallel gating with a CPU circuit to bypass most of the interrupt inhibits for noninterruptable instructions. The number of noninterruptable instructions was decreased so that, in a real-time operating system, interrupts can be more rapidly processed.

When any error is detected, the MP must wait until the next trailing edge of IUCX – C before raising its interrupt request. To guarantee that no further instructions are executed by the CPU after the error is detected, DINT – (13X5), which is routed directly to the CPU, is brought true. DINT – true forces the CPU to ST2 after executing the instruction and holds the CPU in that state until the MP interrupt request is raised.

If a jump condition is not met, DINT – sets the CPU to ST2 to allow for overflow error detection.

The ST2 mask logic (12T4), with DINT –, holds the CPU in ST2 to prevent initiation of the I/O cycle. ST2MK – true inhibits the interrupt sequence when DINT – is true until the MP detects an error, at which time ST2MK – goes false and the interrupt sequence is allowed to proceed. If no error is detected, DINT – goes false, followed by ST2MK –. The CPU then proceeds to the next instruction.

The MPST1 flip-flop (12X4) stores a halt instruction and enables the MPST + (12S2) gate, when a halt error is detected, MPST – (12W5) true restarts the CPU immediately after the CPU halt that results when a halt is attempted in an unprotected area.

The RW logic gate (12C5) controls the read/write control line to the memory. If a write or jump error is detected, RW – goes true (at the beginning of state OF1), changing the memory write cycle to a read cycle to prevent memory modification.

4.9 INTERRUPT REQUEST LOGIC

In the interrupt request logic, the IURX flip-flop (11B4) generates the MP interrupt request (IURX +) signal to the CPU when an error is detected by the error detector. IURX + is set on the trailing edge of the CPU Interrupt clock (IUCX – C) signal (11B3) when E123 + (11C3) is true.

When an MP interrupt request is raised, priority signal PRN3X – (11A5) goes high and disables priority to all device controllers lower in the 620/f priority chain.

4.10 INSTRUCTION ADDRESS REGISTER

The 15-bit instruction address register (IAR) stores the value of the P register plus one at the end of each instruction fetch cycle. The IAR is updated at each instruction fetch cycle until the MP detects an error. The MP can, thus, locate the address of the instruction in error. During an error interrupt routine, further update of the IAR is inhibited until the MP is reenabled.

IAR00 + through IAR14 + (10H4, 10H5, 10K4, 10K5) from the IAR are routed to the A-bus driver and, during a data transfer in, are gated out to the CPU. Bits CB00 through CB08 arrive directly from the C-bus, and are clocked into the IAR by CLAIR. SAR09 + through SAR14 + arrive from the segment address register and are clocked into the IAR by CUIAR.

The interrupt inhibit (INTI) flip-flop (10M4) inhibits error detection by the MP during the processing of interrupts generated by other device controllers. Also, flip-flop DWAFF (10K5) generates DWAFF + to the error detector during DWAI.

4.11 A-BUS DRIVER

The A bus driver gates error interrupt addresses to the CPU during an MP-generated error interrupt. This circuit also gates the contents of the instruction address register to the CPU during a data transfer in.

The error interrupt addresses are encoded on A-bus lines AB01 – C through AB04 – C. When the MP-generated IURA + (11B2) is true, the interrupt address gates are enabled depending on the detected error conditions. Also, flip-flop EB1 + is set when I/O or jump errors are detected. Note that EB1 + is used to make AB01 – C true so that the interrupt address is maintained on the A bus during interrupt acknowledgement.

The A-bus driver also transfers the contents of the instruction address register (IAR) to the A-bus. AB00 – C to AB14 – C correspond to the contents of IAR00 + through IAR14 +. The transfer is accomplished when the function control logic receives a transfer in instruction, i.e., the TIAR flip-flop is set. TIAR + (6D4) gates IAR00 + through IAR07 + to the A bus as bits AB01 – C through AB07 – C. Similarly, bits IAR08 + through IAR14 + are gated out to the A-bus as AB08 – C through AB14 – C by TIARA + (8M3).

4.12 MNEMONICS

The mnemonics used in the MP are listed alphabetically in table 4-1. The source column lists the location of the signal's source on MP logic diagram 91C0257; the first number is the drawing sheet number and the following letter and number, the chip location on the circuit card (except for connector P1 and P3). Refer to section 6 for the logic diagram. Each signal's function is briefly described.

Table 4-1. MP Mnemonic Definitions

Mnemonic	Source	Description
AB00 – C to AB15 –	11D5,11E4, 11F4,11E5, 11F5	620/f CPU internal I/O data lines
AB00 + to AB15 +	7E3,7L3, 7K3	A bus driver output to the mask register
AB134 –	8C4	ANDed A-bus, function ready, and interrupt acknowledge signals to form a partial decode of the MP device address
ALCA –	13V5	Alternate clock (inverted); clocks the SIOA flip-flop
ALC –	P3-72	Gated 9.0-MHz alternate clock from CPU; inhibited during XF1 portion of each memory cycle
AM +	15T2	Output of the first flip-flop of a two-flip-flop 110-nanosecond counter; used in error detection
BIF1 –	9R4	Timing window for loading the segment address register and lower half of instruction address register

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
BM	15T2	Output of the second flip-flop of a two-flip-flop 110-nanosecond counter; provides control section timing
CB00-CB07 CB08 CB09-CB14	P3-5 to P3-13 P3-17 P3-18 to P3-24	C-bus bits 0-14; buffered outputs from the adders of the CPU data loop
CCUPA –	12N4	Clock input to the CUPA flip-flop
CEB1 +	11A3	Clock input to the EB1 flip-flop
CENMP +	8B5	Clock input to the ENMP flip-flop
CEXUP –	15V3	Clock input to the EXUP flip-flop
CE1 –	16N3	Clock input to the E1 flip-flop
CE2 –	16S2	Clock input to the E2 flip-flop
CE3 –	16S4	Clock input to the E3 flip-flop
CJMTF –	15S4	Clock input to the JMTF flip-flop
CLDM –	8D3	Clock input to the LDM flip-flop
CLIAR +	10R5	Clock input to bits 0-8 of the Clock input to bits 0-8 of the instruction address register
CRE –	14W4	Clock input to the RE flip-flop segment address register
CSARA +	9N4	Clock input to bits 9-11 of the segment address register

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
CSARB +	9N4	Clock input to bits 12-14 of the
CST2E –	15U2	Clock input to the ST2E flip-flop
CTIAR –	8D3	Clock input to the TIAR flip-flop
CUDP –	12N3	Clock input to the UDP flip-flop
CUIAR +	10R5	Clock input to bits 9-14 of the instruction address register
CUPA	12N5	Output of the CUPA flip-flop; stores the protected/unprotected status of each instruction word and of the effective address
CWAB –	8C3	Clock input to the WA and WB flip-flops
DAF45 +	8B5	MP device address 045 decoded and ANDed with the function ready and interrupt acknowledge signals
DCENM –	8U3	Dc reset input to the ENMP flip-flop
DCE3 –	16T4	Dc set input to the E3 flip-flop
DEXUP –	15V3	D input to the EXUP flip-flop
DE1 –	16R3	D input to the E1 flip-flop
DE2 –	16R3	D input to the E2 flip-flop
DE3 –	16T3	D input to the E3 flip-flop
DINT –	13X5	Dummy (simulated) interrupt to CPU; places and holds CPU in the interrupt wait state (ST2) to provide time for error detection

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DJMTF –	15B2	D input to the JMTF flip-flop
DRYXM +	8B3	Inverted from DRYX -C
DRYX – C	P1-6	Data Ready signal on CPU internal I/O control bus
DSIOA –	13W3	D input to the SIOA flip-flop
DWA	P3-69	Decoded two-word addressing signal from the CPU instruction register; when true, the register contains a two-word instruction
DWAFF +	10K5	Output of DWAFF flip-flop; set during immediate or extended two-word addressing instructions
DWAFM –	10U5	Inverted from DWAFF
DWAI	P1-51	Decoded two-word immediate addressing signal from the CPU instruction register; when true, the register contains an extended or immediate two-word addressing instruction
DWIF3 +	15R5	State IF3 during all two-word addressing instructions except extended, immediate, and skip if register equal
DWINR –	16B2	All extended, immediate, and skip if register equal (two-word) instructions except increment and replace
DWOF2 +	15S3	State OF2 during all extended and immediate (two-word) instructions

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DW0I +	13B2	Operand store or increment and replace during extended or immediate (two-word) instructions with MP enabled; enables dummy interrupt
DWSRE	16A3,16E4	OR of extended, immediate, and skip if register equal instruction register decodes
EAPA –	7H2	Status of the address of the first or second word of an instruction or of the effective address
EBT –	P1-31	When true, the instruction register contains a bit test instruction
EB1 +	11D4	Enable A-bus bit 1 flip-flop; stores conditions for which bit 1 must be made true during an MP-generated interrupt
EDINT +	13V4	Enable dummy interrupt; enables MP and indicates that no externally generated interrupt is in process
EDWAF +	13A4	Extended or immediate instruction with MP enabled
EFB1 –	13V4	Generated when EXF and INHB1 are false; inhibits the dummy interrupt
EL	P3-50	Enables CPU L register clock
ENCT +	15T3	Enables the AM/BM counter
ENDE3 –	16U4	Enables MP and resets flip-flop E3

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
ENIOC +	15S3	18-MHz clock gated to AM/BM counter when the MP is enabled
ENJMS +	13A4	Indicates that a jump, jump and mark, or skip instruction is in the instruction register
ENMP +	8B4	MP enabled flip-flop; stores enabled/ disabled MP status
EP	P3-14	Enables CPU P register clock
EXC	P3-60	When true, the instruction register contains an external control instruction
EXEN −	10A4	Indicates that the instruction register does not contain an execute instruction
EXFGM +	13A4	Execute instruction decoded but execution condition not met
EXFT2 +	13S3	Execute instruction decoded, execute condition not met, and test not true during IF2
EXF −	P3-16	Execute condition met flip-flop; set at the end of IF2 during an execute instruction if the execution condition is met
EXGR	P1-7,P1-9	When true, the instruction register contains an execute instruction
EXGRM	15W2	Execute group flip-flop; set when an execute instruction is in process

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
EXGU –	16R4	Inhibits detection of I/O and halt errors during an execute instruction if the first word of the instruction is in a protected area
EXTR +	16T5	First half of CPU state OF5 during a non-INR extended, immediate, or SRE instruction with MP enabled; gates clock to overflow error detect flip-flop E3
EXUP –	15V2	Execute unprotected flip-flop; set when the first word of an execute instruction lies in an unprotected area
E1	16R2	Error flip-flop 1; stores detection of halt and I/O error conditions
E123 +	11C3	Indicates when one or more of the error flip-flops are set
E2	16R2	Error flip-flop 2; stores detection of write and jump error conditions
E3	16S5	Error flip-flop 3; stores detection of overflow error conditions
FRYX – C	P1-12	Function ready signal on the CPU internal I/O control bus
GRD1 –	N3-7	Ground to IC N02
GRD2 –	M3-7	Ground to IC M02
GRD3 –	L3-7	Ground to IC L02
GRD4 –	F2-11	Ground to IC F02
GRD5 –	K3-7	Ground to IC H02

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
GRD6 –	X4-7	Ground to D input MPST1 flip-flop
GRD7 –	D4-7	Ground to D input of RE flip-flop
GRD8 –	T2-8	Ground to K input of BM flip-flop
HLT	P3-23	CPU halt flip-flop
HLTD	P1-58	When true, the instruction register contains a halt instruction
HLTDM –	16U5	Inverted from HLTD
HST2 –	12X3	Gates EL to set the MPST1 flip-flop when a halt occurs during ST2 of an MP-generated interrupt
IAR00 + to IAR14 +	10H4,10H5, 10K4,10K5, 10M4	Instruction address register bits 0-14; store address of the first word of the instruction during which an error occurred
IBR1 –	13V4	Halt decode or step
IFPR –	14X3	Resets the error flip-flops upon completion of an MP-generated interrupt
IF1	P3-10	State 1 of the CPU instruction fetch cycle; the next instruction is fetched during this state

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
IF2	P3-33	State 2 of the CPU instruction fetch cycle; registers are selected and modified during this state
IF3	P3-34	State 3 of the CPU instruction fetch cycle; occurs during the last half of IF2; registers are modified during this state
IJMP	14V5	When true, the instruction register contains an indexed jump instruction
INHB1 –	P3-29	Inhibit 1 flip-flop; in conjunction with inhibit 2 flip-flop, sequences and controls setting of the CPU HLT flip-flop
INR	P3-47	When true, the instruction register contains an increment and replace instruction
INRM –	13E3	Inverted from INR
INTI –	P3-M4	Interrupt inhibit flip-flop; inhibits error detection by the MP during an externally generated interrupt
INTR	P3-46	CPU interrupt flip-flop; stores detection of an interrupt request
INTX –	P3-42	CPU interrupt inhibit flip-flop; inhibits certain CPU function (e.g., incrementing the P register) during processing of the instruction at the interrupt address
IOC –	P3-39	CPU 18-MHz clock

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
IOCE3 +	16U2	E3 flip-flop output
IOCM +	9W5	18-MHz clock after inversion
ISIO −	13C5	MP-generated inhibit start I/O signal to the CPU; inhibits start I/O (P0) to the I/O section
IUAX +	8B3	Inverted from IUAX − C
IUAX − C	P1-8	CPU interrupt acknowledgement on the internal I/O control bus
IUCXM +	11B3	Inverted from IUXC −C
IUCX − C	P1-10	CPU interrupt clock on the internal I/O control bus
IUR	P1-29	Interrupt request to the CPU and MP from the I/O control section
IURA +	11B2	MP-generated interrupt request acknowledgement
IURI +	13R4	Removes DINT − during the last half of the interrupt cycle and sets the RE flip-flop
IURX	11B4	MP-generated interrupt request
IURX − C	11C4	CPU interrupt request on the internal I/O control bus
JCM +	16A3	Jump or skip instruction with condition met
JE2 −	11C2	Jump error detected during a jump, jump and mark, or skip instruction

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
JGR –	14T5	Indexed jump and set return, enable bit test, or jump instruction
JMCU +	16U4	Second word of a jump or jump and mark instruction in an unprotected area
JMGR +	14W4	Jump or jump and mark instruction
JMSGR +	14C3	Jump, jump and mark, or skip if register equal instruction
JMS25 +	13U3	Jump, jump and mark, or skip instruction occurring other than during OF2 or OF5
JMTF	15S5	Enables a part of overflow detection except during jump and jump and mark instructions for which the test condition is true
JSGR +	14W4	Jump plus skip if register equal instructions
JSR –	P3-43	When true, the instruction register contains a jump and set return instruction
JTT –	15X3	Test condition true during a jump or jump and mark instruction
JUMP –	P3-41	When true, the instruction register contains a jump instruction
LDMR –	8C2	Loads the selected mask register during the data ready portion of the data transfer out instruction

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
LDM +	8D2	Load mask flip-flop; set during the data transfer portion of any data transfer out instruction addressed to the MP
MPINT −	13A5	Output of MP interrupt inhibit gate; parallel with the interrupt inhibit gate in the CPU
MPST +	12S2	Starts the CPU when a halt occurs after detection of a halt error
MPST1 +	12X4	Enables MPST; resets on the trailing edge of MPST to inhibit extra MPST pulses when operating in step mode
MR00 + to MP15	7F2,7L2, 7M2,7N2	Output of mask register bits 0-15
OF1 −	P1-38	State 1 of the operand store cycle during which the operand is stored in memory
OF2	P3-66	State 2 of the operand store cycle during which the P register is selected and incremented
OF2M −	13W5	Inverted from OF2
OF4	P1-26	State 4 of the operand fetch cycle during which the operand is fetched from memory

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
OF5 –	P1-18	State 5 of the operand fetch cycle during which registers are selected and modified
OPINR +	13W3	Operand store or increment and replace instruction
OPSTO	P3-57	When true, the instruction register contains a store instruction (including jump and mark)
OP10 +	P1-50	When true, the instruction register contains an I/O instruction
OP10M –	16U5	Inverted from OP10 +
OSAFC –	P1-37	Causes entry into an address cycle (sets CPU flip-flop AFC) during a bit test instruction if the bit test condition is met
OSIF3	15C2	OSAFC or instruction fetch state 3
PA –	P3-28	Flip-flop in the CPU I/O sequencer
POI	P1-48	CPU I/O sequence state P0 during which the start I/O signal is requested
PRN3X –	11A5	Priority out line from MP
RB –	14U4	Resets the error flip-flops and MPST1
RE	14D4	Resets the error flip-flops via RB at the end of an MP-generated interrupt

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
REXGR +	15T3	EXGRM flip-flop dc reset
RMSK -	12W4	Resets the ST2 mask latch when a non-MP-generated interrupt request occurs and the MP is not also requesting an interrupt
RSTRT -	12V4	MPST1 flip-flop dc set
RUDP -	12N4	UDP flip-flop dc reset
RUN +	P1-49	Output of the step/run latch, which is operated by the STEP/RUN switch on the CPU control panel
RW -	12C5	Read/write control line to memory
SAR09 + to SAR14 +	9L4,9L5, 9M5	Segment address register bits 9-14; store the segment address on the C bus
SEB1 +	11C2	D input set of the EB1 flip-flop
SIOA -	13X4	Simulated I/O active signal; simulates I/O active from the I/O section when an I/O error is detected
SKIP2 -	9C5	Indicates that the P register is being incremented during a skip if register equal instruction
SMSK -	12V3	Sets the ST2 mask latch when ST2 is entered for error detection
SRE	P3-32	When true, the instruction register contains a skip if register equal instruction

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
SREM –	14V6	Inverted from SRE
SRINT –	14U4	ORed output of a system reset and non-MP-generated interrupt in process
SSAR +	9N3	Gates IOC to clock the segment address register flip-flops
STJMK –	P3-40	When true, the instruction register contains a jump and mark instruction
ST1	P1-59	CPU state 1 during which the CPU is halted
ST2	P3-25,P3-26	CPU interrupt wait state 2
ST2E	15V2	State 2 enable flip-flop; set during all but the first 165 nanoseconds of ST2; clocks EB1 flip-flop and resets EXGRM flip-flop
ST2MK –	12T4	State 2 mask; inhibits ST2 to the I/O section during ST2 error detection
SYRTA –	8M3	Inverted from SYRT –C
SYRTM +	8B3	Inverted from SYRT –C
SYRT –C	P1-17	System reset from CPU internal I/O control bus
TESTR	P1-57	Test true; indicates condition met during conditional instructions

Table 4-1. MP Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
TIAR ±	8D2	Transfer instruction address register flip-flop; set during last half of a data transfer in instruction addressed to the MP
TIARA +	8M3	Buffered output of TIAR flip-flop; gates bits 7-14 of the instruction address register to the A bus during a data transfer in instruction addressed to the MP
TTIF2 −	13U2	Gates TESTR during CPU state IF2
T1EN + T1ENX +	14U3, 16A3	Timing window indicating the first half of CPU state IF2, MP enabled, except during processing of an instruction via an execute instruction
T1 −	15W3	ALC clock pulse selected by T1EN
UDP −	12N5	P register update flip-flop; set each time the P register is modified, except during IF3 or OF5
UPE2 +	16S3	Indicates that either the first word of a two-word instruction or an execute instruction is unprotected and the E2 flip-flop is reset
UP +	16U2	Indicates that either the first word of a two-word instruction or an execute instruction is unprotected
V1 +	N3-14	+5V dc to IC N02
V2 +	M3-14	+5V dc to IC M02

V3 +	L3-14	+ 5V dc to IC L02
V4 +	F2-16	+ 5V dc to IC F02
V5 +	K3-14	+ 5V dc to IC H02
WA +	8E2	Write address line A to the 4x4 register file mask registers
WB +	8E2	Write address line B to the 4x4 register file mask registers
W1UP	15W2	Word 1 unprotected flip-flop; stores the protected/unprotected status of the first word of each instruction
XFA	P1-32	CPU cycle flip-flop; denotes last 110 nanoseconds of any CPU cycle
XFAM -	9U5	Inverted from XFA
XFAOF -	9R4	Selects the last 110 nanoseconds (XFA) of any CPU cycle, except operand fetch (OFF -); loads segment address register
XF1	P3-15	Indicates state 1 of all CPU cycles, except operand fetch
ZEROA -	9L4	470-ohm pull-up resistor
ZEROB -	9L5	470-ohm pull-up resistor
ZEROC -	10K5	470-ohm pull-up resistor
ZEROD -	15V2	470-ohm pull-up resistor

4.13 PROGRAMMING CONSIDERATIONS

A prerequisite to implementing the MP is an executive program operating in the computer system from a protected segment of memory. The executive allocates the assignment of protected and unprotected memory segments and implements enabling and disabling of the MP. The user writes the MP service routines to conform to the considerations and restrictions described in the following subsections.

4.13.1 Device and Error Addresses

The MP device address is 045. The interrupt addresses assigned to MP error interrupts are:

Error	Address	Error	Address
Halt	020	Write	024
Overflow	030	Write plus overflow	034
I/O	022	Jump	026
I/O plus overflow	032	Jump plus overflow	036

Interrupt addresses and error subroutines must reside in a protected memory segment. Thus, addresses 00 through 0777 must be designated a protected segment to include the executive, error addresses, and error-processing subroutines.

4.13.2 DMA, PMA, and Interrupt Operations

Direct and priority memory access and interrupt functions are independent of a stored program, and do not originate directly from a protected or unprotected memory segment. However, I/O is initiated by the executive program, which resides in a protected segment. Thus, these operations are considered to be operating from a protected area and are not restricted by the MP. The user must ensure that the executive program provides proper memory access to these sources.

Detection of a jump error is inhibited during memory access or interrupt-processing to allow a jump to the appropriate subroutine.

4.13.3 Uninterruptable Instruction Sequences

With MP, all 620/f instructions are interruptable except:

a. Halt (HLT)

b. External Control (EXC)

c. Execute (XEC). Interrupts are not recognized between the processing of this instruction and the instruction executed by it if the condition is met, nor between this instruction and the next one in sequence if the condition is not met.

d. Instructions executed in step mode.

The MP detects the attempted execution of the above as errors.

4.13.4 Memory Wrap-Around

The wrap-around capability of the 620/f allows the addressing of nonexistent memory cells when memory capacity is exceeded. The MP does not have this capability. Thus, segments that exceed existing memory must be designated protected so that a jump, overflow, or store operation from an unprotected segment to nonexistent memory is detected as an error.

4.13.5 Priority Assignment

The MP is assigned the highest priority in the 620/f external device priority chain. Thus, the power failure/restart (PF/R), which normally takes highest priority if it is installed in the the system, is assigned second-highest interrupt priority.

If MP error and PF/R interrupt requests occur simultaneously, the CPU first services the MP interrupt, then the power/down subroutine. This action provides a valid return address and a correct indication that the instruction in process at the time of the interrupt is in error.

4.13.6 Mask Register Segment Assignments

Figure 4-1 summarizes the mask register segment assignments (refer to section 4.5). As shown storing a one in a mask register bit protects the corresponding memory segment; a zero produces a corresponding unprotected segment.

The mask register contents are volatile. To prevent their loss during power shut-down, the user must assign four memory addresses for nonvolatile storage of the MP mask.

4.13.7 Extended Processing Time

If a program is operating from an unprotected area and the MP is enabled, the processing time for certain instructions is extended. This results because error detection occurs following the execution of the instruction and during the CPU interrupt wait state (ST2). The affected instructions are:

a. Immediate write (including INRI)

b. Extended write (including INRE)

c. Execute when the condition is not met

d. Unconditional jump (including jump and set return and indexed jump)

e. Conditional jump (except jump and mark) when the jump condition is met

f. All conditional jump when the jump condition is not met

With the 620/f memory full-cycle time of 750 nanoseconds, the extension of processing time for each affected instruction is 130 nanoseconds.

4.13.8 MP I/O Instructions

Table 4-2 lists the instructions for programmed communication between the MP and the CPU.

Table 4-2. MP Instructions

Mnemonic	Code	Description
	External Control	
EXC 045	0100045	Select mask register 0
EXC 0145	0100145	Select mask register 1
EXC 0245	0100245	Select mask register 2
EXC 0345	0100345	Select mask register 3
EXC 0645	0100645	Enable MP
EXC 0745	0100745	Disable MP
	Transfer	
CIA 045	0102545	Clear and input instruction address register contents to A register
CIB 045	0102645	Clear and input instruction address register contents to B register
IME 045	0102045	Input instruction address register contents to memory
INA 045	0102145	Input instruction address register contents to A register

Table 4-2. MP Instructions *(continued)*

Mnemonic	Code	Description
INB 045	0102245	Input instruction address register contents to B register
OME 045	0103045	Output memory contents to mask register
OAR 045	0103145	Output A register contents to mask register
OBR 045	0103245	Output B register contents to mask register

4.13.8.1 MASK REGISTER LOADING

To load a mask register:

a. Select the register using a select mask register external control instruction (refer to figure 4-2 and table 4-2).

b. Issue one of the data transfer out instructions (OME, OAR, and OBR) to load the mask register.

MP need not be enabled for this procedure.

4.13.8.2 ENABLING AND DISABLING MP

The MP is enabled by the EXC 0645 instruction. This status is lost when power is shut down.

It is disabled by:

a. Issuing an EXC 0745 instruction

b. A system reset, either manually from the computer control panel or automatically by the power supply or PF/R

The MP must be disabled when power is restored to the system so that the contents of the mask register can be reinstated. When this is accomplished, MP can be reenabled.

4.13.8.3 INSTRUCTION ERROR ADDRESS TRANSFER

The address (plus one) of an instruction in error can be transferred to the CPU with a data tansfer in instruction (CIA, CIB, IME, INA, or INB) for use during the processing of error subroutines.

4.13.8.4 EXITING FROM AN UNPROTECTED AREA

To return to the executive program (protected segment) upon completion of program execution, issue a jump instruction to a previously assigned address in protected memory. This action produces an error interrupt. The jump error subroutine executes the jump after recognizing the special jump address.

4.13.9 Protected Area Operation

When a program is operating in a protected segment of memory, the MP detects no errors. An instruction is defined as protected if the first (or only) word of the instruction resides in a protected segment.

To avoid extending the processing time of a protected-segment program because of attempted error detection, disable the MP while in the protected area.

4.13.9.1 ENTERING A PROTECTED AREA

The MP is automatically disabled during an MP interrupt, and the EXC 0745 instruction need not be issued. The MP interrupt causes a jump to an interrupt address in protected memory, where the program can proceed without the restrictions of a program operating from unprotected memory.

The unprotected-to-protected boundary can also be crossed when another external device requests an interrupt. In this case, the first instruction of the interrupt-processing subroutine must be an EXC 0745 (disable MP) instruction.

4.13.9.2 LEAVING A PROTECTED AREA

To leave a protected memory segment and enter unprotected memory:

a. In the next-to-last address of the exit subroutine, issue an EXC 0645 instruction to enable the MP, then the jump-type instruction to the unprotected area.

b. Overflow into the unprotected area by issuing an EXC 0645 in the last address of the protected area.

4.13.10 Step Mode Operation

The MP detects errors when the operator "steps through" a stored program. In step mode, if an error interrupt occurs when START is pressed, the resulting interrupt-processing subroutine is entered the next time START is pressed.

To prepare the system for stepping through a sequence of instructions:

a. Load a HLT instruction in the I register.

b. Load the address of the first instruction in the P register.

c. Press START for each instruction.

The MP is disabled and no errors detected if, during the stepping procedure, the REPEAT switch is set.

MP maintenance consists of running the MP test program, troubleshooting, and making repairs, if required. The MP test program, decribed in the 620 test programs manual, in conjunction with the 620/f maintenance manual, helps isolate an error condition. Troubleshooting is facilitated by familiarization with the operation of the MP and use of the logic diagram (section 6).

5.1 EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the MP.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM265 Extender Card, part number 44P0437

d. CPU Extender Cables

e. Card Puller, Titchener type 1731

5.2 TEST PROGRAM

The MP test program is an integral part of the MAINTAIN II test program system. It is provided as part of the regular troubleshooting package for the 620/f computer.

MP operation should be checked with the MP test program (part number 92A0105-002), under the control of the test executive program (part number 92A0107-001). MP malfunctions are reported in the form of error messages and/or codes.

The MP test program is decribed in detail in the 620 test programs manual (document number 98 A 9908 960).

5.3 TROUBLESHOOTING

With the computer turned off and the control panel opened on its hinges, disconnect the CPU tray from the motherboard. Extend the CPU tray out the front and connect an extender cable between CPU tray connectors P1, P2, and P3 and backplane connectors J8, J9, and J10. Firmly attach the CPU tray to a bracket mounted on the front of the mainframe.

After removing the card retainer bar, install the MP card on an extender card.

The computer can then be turned on to begin troubleshooting.

5.3.1 Input Power

Verify +5V dc ± 5 percent and common (ground) at the following locations:

+5V dc	Common
P1-77	P1-1
P1-78	P1-2
P1-79	P1-3
P1-80	P1-4
P3-1	P3-77
P3-2	P3-78
P3-3	P3-79
P3-4	P3-80

5.3.2 Control Panel Reset

Verify that the following MP flip-flops are set by momentarily grounding the signal at the specified input pin. Then, verify that the flip-flops can be changed from set to reset using the RESET switch on the computer control panel.

Flip-Flop	Input Pin	Signal	Output Pin
ENMP	H03-011	ZEROA –	B04-008
LDM	H03-011	ZEROA –	D02-006
TIAR	H03-011	ZEROA –	D02-008
IURX	H03-010	ZEROC – *	B04-005
EB1	H03-010	ZEROC – *	D04-009
E1	H03-010	ZEROC – *	R02-005
E2	H03-010	ZEROC – *	R02-008
EXUP	H03-012	ZEROD –	V02-008
MPST1	H03-012	ZEROD –	X04-006
E3	T04-008	DCE3 –	S05-006

* Load zero in the I register first on each step.

To test the INTI flip-flop (output pin M04-008):

a. Press RESET.

b. Load zero in the I register.

c. Momentarily ground ZEROB – (M04-013) to set the flip-flop.

d. Momentarily ground ZEROC – (H03-010) to reset the flip-flop.

5.3.5 Manual Tests

Performing the following manual tests, in conjunction with the MP test program, ensures a thorough test of the operation of the MP.

Before executing the test subroutines decribed below, press RESET and set run mode.

5.3.3.1 MASK REGISTER ADDRESSING

Select a mask register and verify that its contents are not altered by data transfer out operations.

Address	Instruction	Mnemonic	Decription
000100	100045	EXC	Select mask register 0
000101	010113	LDA	
000102	103145	OAR	Load mask register
000103	010114	LDA	
000104	103105	OAR	Addressing test 1
000105	103165	OAR	Addressing test 2
000106	103155	OAR	Addressing test 3
000107	103141	OAR	Addressing test 4
000110	103147	OAR	Addressing test 5
000111	103144	OAR	Addressing test 6
000112	000077	HLT	
000113	052525	DATA	
000114	125252	DATA	

Begin at address 000100. After execution of the HLT instruction, verify that the contents of mask register 0 are 052525.

5.3.3.2 ERROR DETECTION PAUSES

Verify that the CPU pauses in CPU state ST2 for 220 nanoseconds after executing the following instructions:

a. Increment and replace extended

b. Store register extended

c. Conditional jump, with jump condition met and not met

d. Execute, with jump condition not met

Address	Instruction	Mnemonic	Description
000140	100045	EXC	Select mask register 0
000141	006010	LDAI	Set up mask
000142	000001		
000143	103145	OAR	Load mask register
000144	100645	EXC	Enable MP
000145	001000	JMP	Jump to unprotected area
000146	001120		
001120	006044	INRE	
001121	000017		
001122	006054	STAE	
001123	000016		
001124	001002	JAP	
001125	001127		
001126	000000	HLT	
001127	001004	JAN	
001130	001126		
001131	003004	XAN	
001132	001126		
001133	001000	JMP	
001134	001120		

5.3.3.3 I/O INTERRUPT CONTROL

Using the sample subroutine described below, verify that:

a. ISIO – prevents normal performance of the I/O sequence.

b. SIOA – advances the CPU through the states of the I/O sequence.

c. Acknowledgement of an MP interrupt request disables MP until reenabled by an I/O instruction.

d. No interrupts occur when the MP is disabled, even when programs containing known errors are executed; in this case, change the contents of address 000124 to 005000 (NOP) for this step only.

e. PRN3X – is held false (open collector, 1K pull-up required) to lock out lower-priority external device controllers during an MP-generated interrupt.

Address	Instruction	Mnemonic	Description
000022	001000	JMP	I/O error interrupt address
000023	000124		
000120	100045	EXC	Select mask register 0
000121	006010	LDAI	Set up mask
000122	000001		
000123	103145	OAR	Load mask register
000124	100645	EXC	Enable MP
000125	001000	JMP	
000126	001100		
001100	005000	NOP	
001101	100045	EXC	I/O instruction unprotected
001102	000007	HLT	

5.3.3.4 INTERRUPT CONTROL

Verify that the CPU can be interrupted from a program operating in an unprotected area to a subroutine in a protected area by a non-MP-generated interrupt request. Verify that no errors are detected and that the MP does not generate an error interrupt request.

Address	Instruction	Mnemonic	Description
000000	001000	JMP	Control panel interrupt address
000001	000010		
000010	005000	NOP	
000011	000077	HLT	Halt after successful test
000012	001000	JMP	Return to unprotected area
000013	001140		
000026	001000	JMP	
000027	000040		
000040	000777	HLT	Halt on test failure
000150	100045	EXC	Select mask register 0
000151	006020	LDBI	Set up mask
000152	000001		
000153	103245	OBR	Load mask register
000154	100645	EXC	Enable MP
000155	001000	JMP	Jump to unprotected area
000156	001140		
001140	001000	JMP	Loop in unprotected area
001141	001140		

Start execution of the subroutine at address 000151. During the unprotected-area loop, issue a control panel interrupt by pressing RESET. The program should halt with 000012 in the P register. To reenter the loop in the unprotected area, press START.

5.3.3.5 UNINTERRUPTABLE INSTRUCTIONS

Verify that non-MP-generated interrupt requests are not recognized by the CPU immediately following the execution of noninterruptable instructions (section 4.13.3).

Address	Instruction	Mnemonic	Description
000000	001000	JMP	Control panel interrupt address
000001	000162		
000160	006010	LDAI	Load A register positive
000161	000077		
000162	100045	EXC	External control instruction
000163	003004	XAN	Execute, condition not met
000164	000077		Loop
000165	001000	JMP	
000166	000162		

Start execution of the subroutine at address 000161. Ground IURX – C on the CPU motherboard and, in run mode, verify with an oscilloscope that MPINT – is inhibited during HLTD and the execution of the EXC and XEC instructions.

5.3.3.6 STEP MODE OPERATION

Verify that non-MP-generated interrupt requests are not recognized by the CPU immediately following the execution of a non-HLT, non-EXC, and non-XEC instruction in step mode.

Address	Instruction	Mnemonic	Description
000000	001000	JMP	Interrupt address
000001	000002		
000002	000007	HLT	
000166	001000	JMP	Loop at 000166
000167	000166		

Ground IURX – C on the CPU motherboard and step through the loop at 000166. Verify that no interrupts occur.

5.4 REFERENCE DOCUMENTS

In addition to this manual, the documents listed below are useful aids to understanding and maintaining the MP.

a. 620/f Reference Handbook (98 A 9908 002)

b. 620/f Maintenance Manual (98 A 9908 050)

c. 620 Test Programs Manual (98 A 9908 960)

d. Assembly Drawing (44D0480)

e. Logic Diagram (91C0257)

f. Wire List (95W0719)

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains logic schematics and parts information for the MP.

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS:
   1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0, 16.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C33	
P3	

REFERENCE DRAWINGS	
44D0480	ASSEMBLY
44P0480	PARTS LIST
95W0719	WIRE LIST
40D0439	P.W. BOARD
97D0490	ARTWORK
97D0493	SILKSCREEN(COMP)
97D0492	SILKSCREEN(CKT)

DRN MANCARELLA	1 JULY 71	varian data machines /a varian subsidiary 2722 michelson drive / irvine / california / 92664
CHK RAG	7/23/71	
DSGN		TITLE: LOGIC DIAGRAM- MEMORY PROTECT
ENGR T. E. HANSON	1/18/71	
APPD D.A. SENKBEIL	1/19/71	
APPD		

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE	620 f	SHEET 1.0	

REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
C	6m	UPDATED AND REDRAWN PER E.N. 5545 AND 5182	RJJ	7/23/71

TABLE OF CONTENTS

CODE IDENT NO.	SIZE	DWG NO	REV
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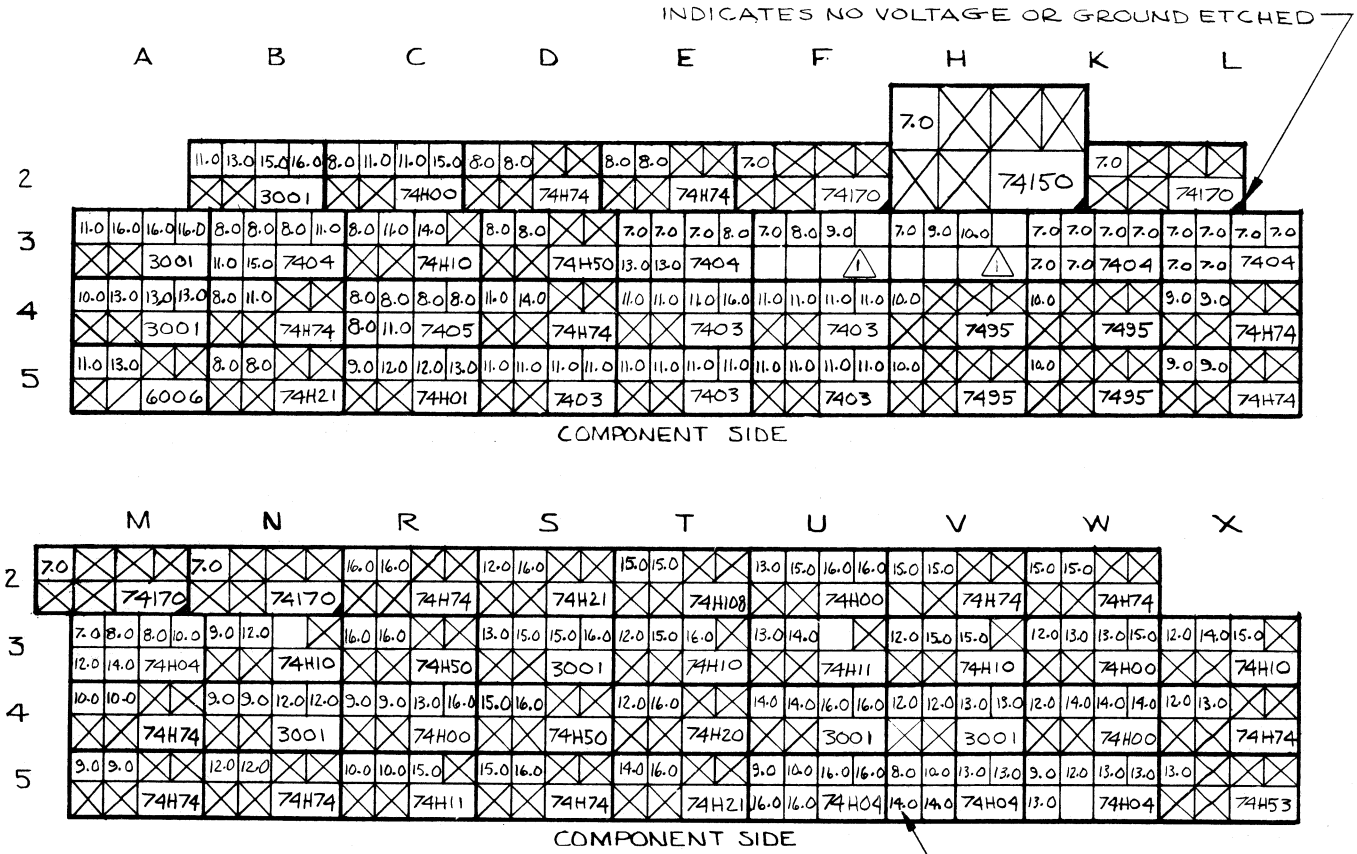

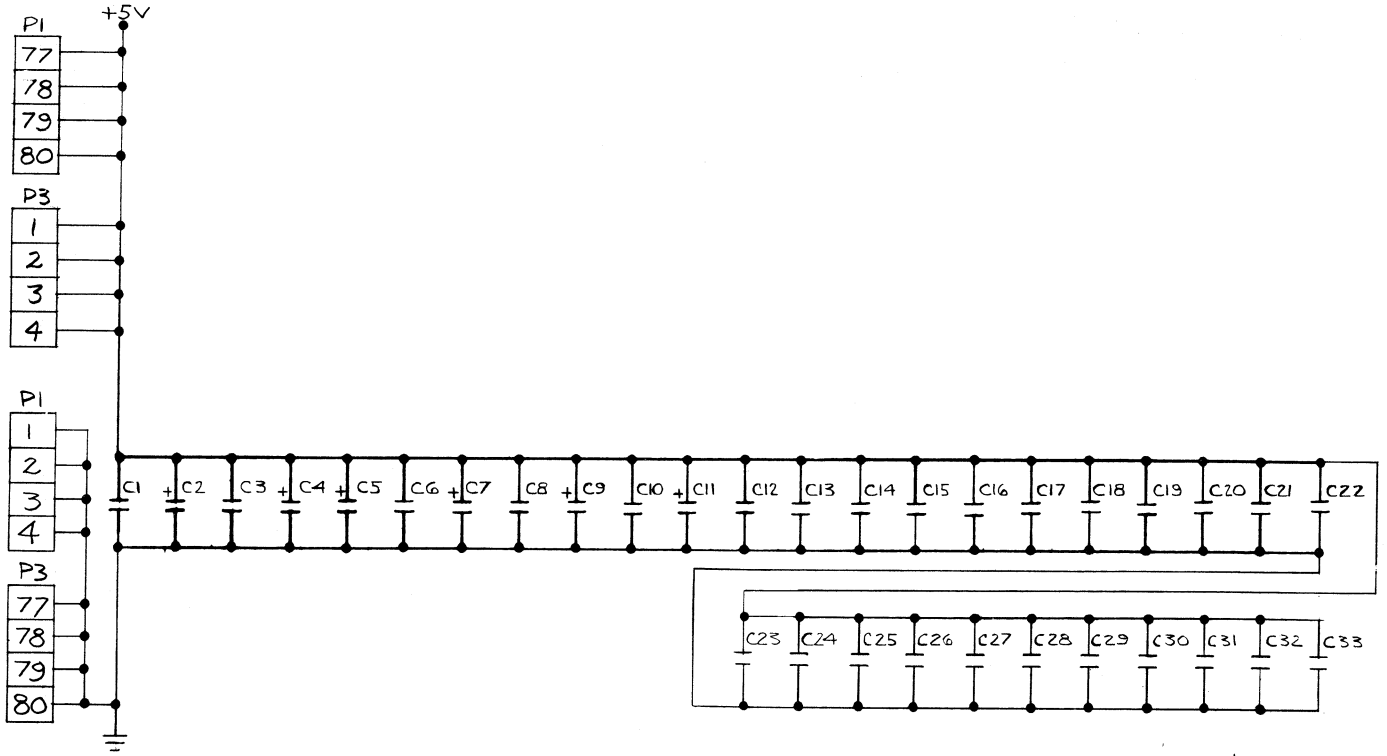

CAPACITORS C2, 4, 5, 7, 9, 11 ARE 2.2 μf, 20 V
CAPACITORS C1, 3, 6, 8, 10, 12 THRU 33 ARE .1 μf 100V

COMPONENT MAP & DECOUPLING

CODE IDENT NO.	SIZE	DWG NO	REV
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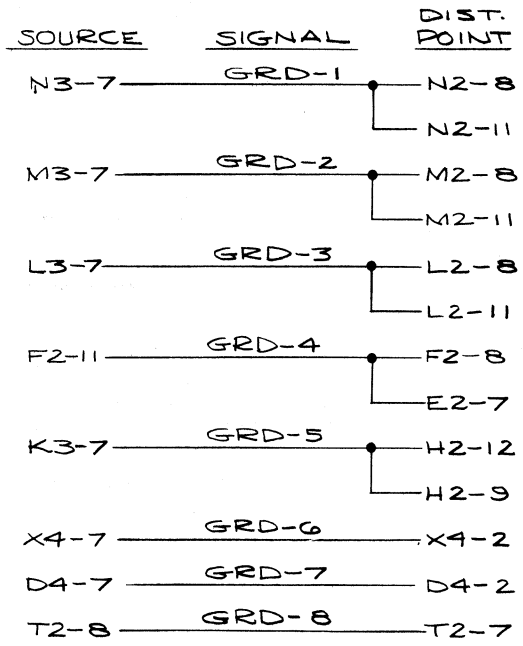
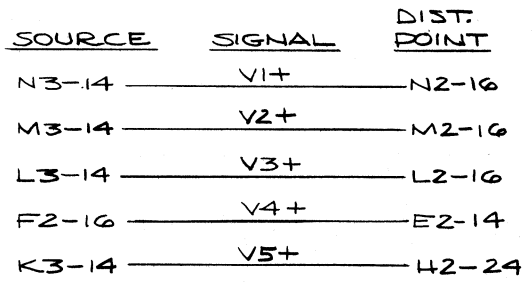




POWER AND GRD WIRED DISTRIBUTION

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE		SHEET 4.0	

CONNECTOR P1

PINS	FUNCTION	SHEET
1	GRD	
2	GRD	
3	GRD	
4	GRD	
5		
6	DRYX-C	8.0
7	EXGR -	13.0
8	IUAX-C	8.0
9	EXGR	15.0
10	IUCX-C	11.0
11		
12	FRYX-C	8.0
13		
14	PRN3X-	11.0
15		
16		
17	SYRT-C	8.0
18	ØF5-	16.0
19		
20		
21		
22		
23		
24		
25		
26	ØF4	9.0
27	RW-	12.0
28	IURX-	11.0
29	IUR	13.0
30	ST2MK-	12.0
31	EBT-	14.0
32	XFA	9.0
33		
34		
35		
36		
37	ØSAFC-	15.0
38	ØF1-	16.0
39		
40		

CONNECTOR P1

PINS	FUNCTION	SHEET
41		
42		
43		
44		
45		
46		
47		
48	PØI	13.0
49	RUN+	13.0
50	ØP10+	13.0
51	DWAI	10.0
52		
53		
54		
55		
56	ISIØ -	13.0
57	TESTR	15.0
58	HLTD	16.0
59	STI	12.0
60	AB15-C	7.0
61	AB14-C	7.0
62	AB13-C	7.0
63	AB12-C	7.0
64	AB11- C	7.0
65	AB10- C	7.0
66	AB09-C	7.0
67	AB08- C	7.0
68	AB07-C	7.0
69	AB06-C	7.0
70	AB05-C	7.0
71	AB04-C	7.0
72	AB03-C	7.0
73	SKIP2-	9.0
74	AB02-C	7.0
75	AB01-C	7.0
76	AB00-C	7.0
77	+5V	
78	+5V	
79	+5V	
80	+5V	

CONNECTOR P2

PINS	FUNCTION	SHEET
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		

CONNECTOR

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0257	C
SCALE		SHEET 5.0	

CONNECTOR P3

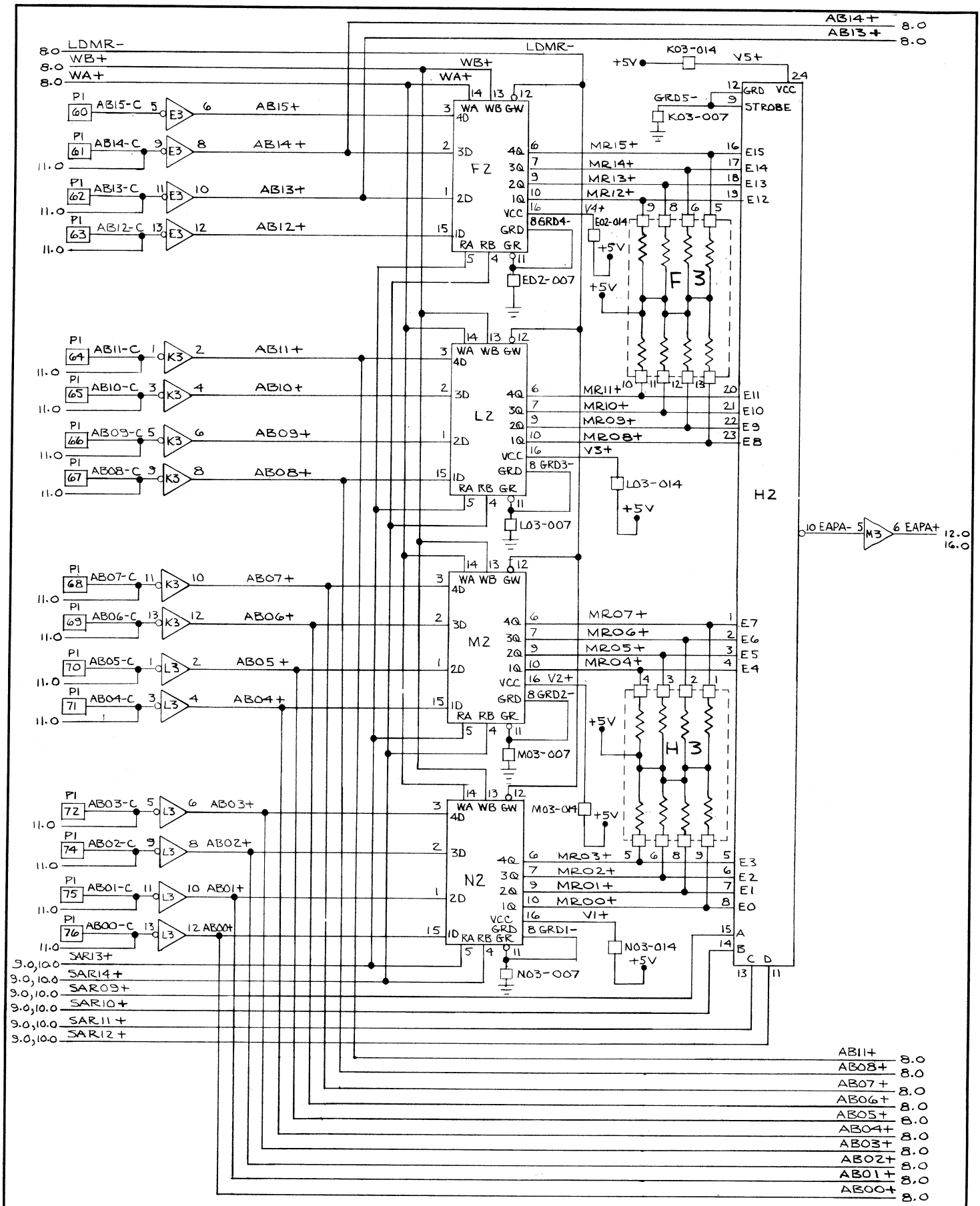
PINS	FUNCTION	SHEET
1	+5V	
2	+5V	
3	+5V	
4	+5V	
5	CB00	10.0
6	CB01	10.0
7	CB02	10.0
8	CB03	10.0
9	CB04	10.0
10	IFI	9.0
11	CB05	10.0
12	CB06	10.0
13	CB07	10.0
14	EP	12.0
15	XFI-	15.0
16	EXF-	13.0
17	CB08	10.0
18	CB09	9.0
19	CB10	9.0
20	CB11	9.0
21	CB12	9.0
22	CB13	9.0
23	HLT	12.0
24	CB14	9.0
25	ST2-	15.0
26	ST2	15.0
27	MPINT-	13.0
28	PA-	15.0
29	INHBI-	12.0
30	MPST-	12.0
31	DINT-	13.0
32	SRE	14.0
33	IF2	14.0
34	IF3	13.0
35		
36		
37		
38		
39	IØC-	9.0
40	STJMK-	14.0

CONNECTOR P3

PINS	FUNCTION	SHEET
41	JUMP-	14.0
42	INTX-	10.0
43	JSR-	14.0
44		
45	IJMP	14.0
46	INTR	12.0
47	INR	13.0
48		
49		
50	EL	12.0
51		
52		
53		
54		
55		
56		
57	ØPSTØ	13.0
58		
59		
60	EXC	13.0
61		
62		
63		
64		
65		
66	ØF2	13.0
67		
68		
69	DWA	15.0
70		
71		
72	ALC-	10.0
73		
74	SIØA-	13.0
75		
76		
77	GRD	
78	GRD	
79	GRD	
80	GRD	

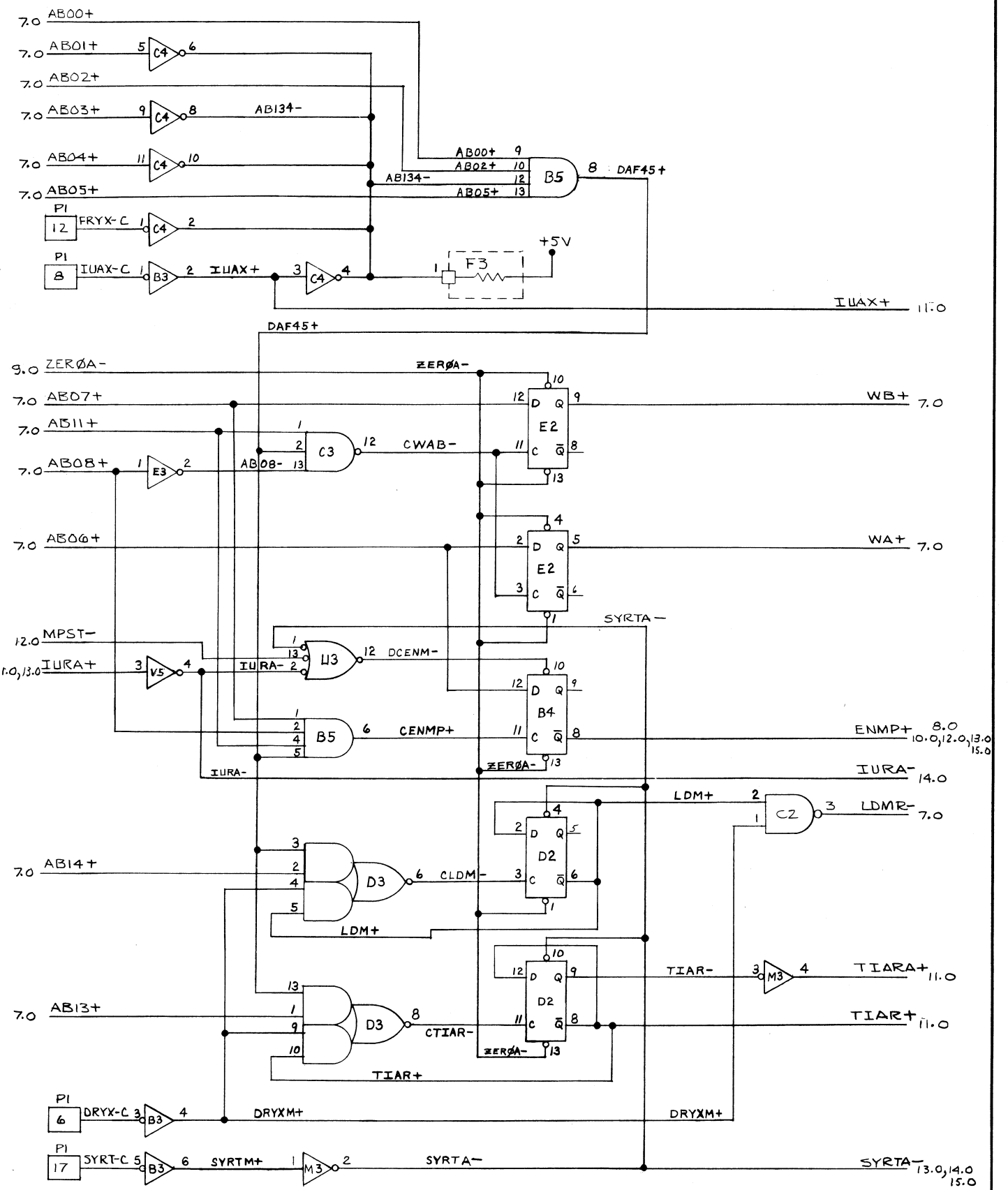
CONNECTOR

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0257	C
SCALE			SHEET 6.0



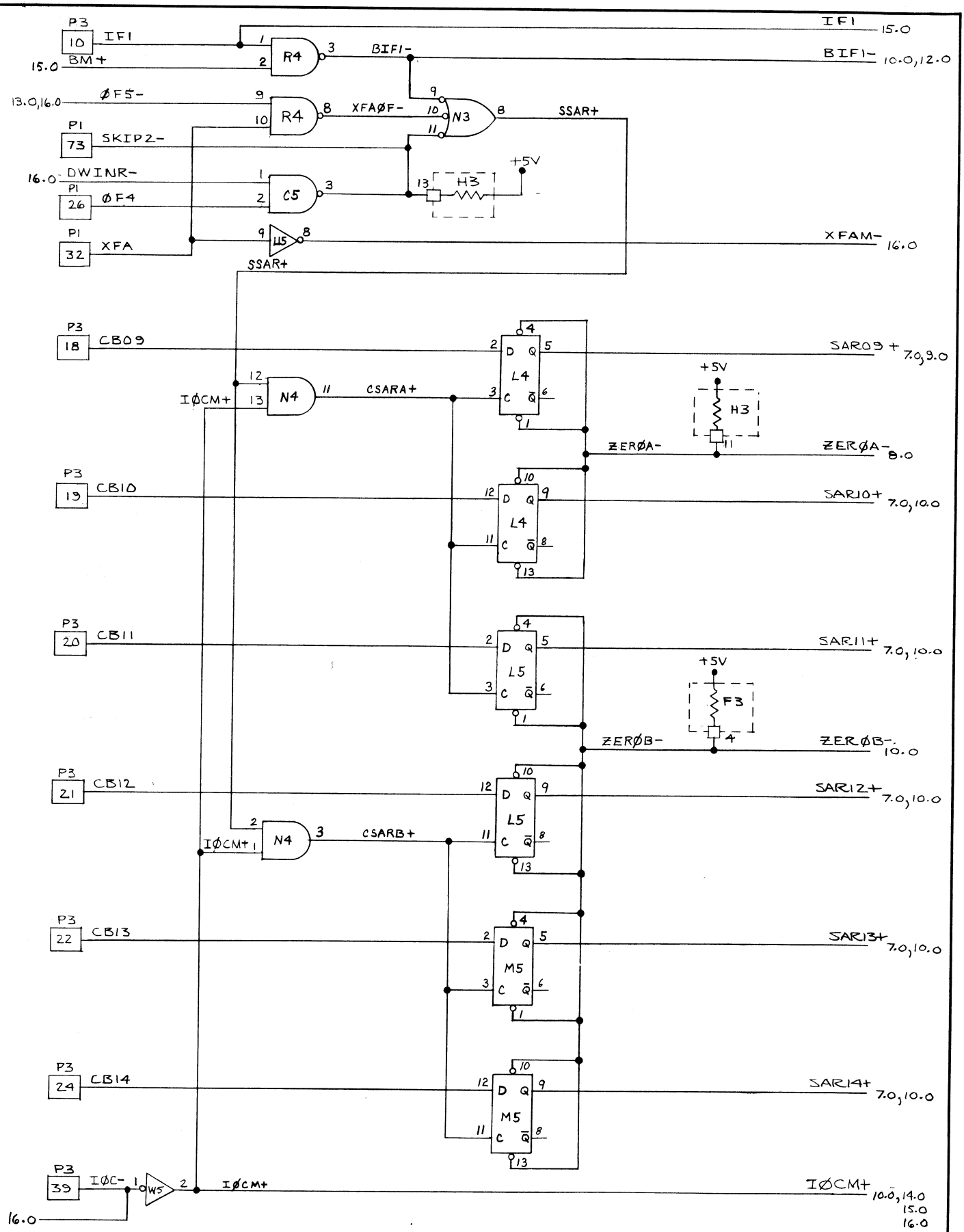
A-BUS RECEIVE MASK REGISTERS & SEGMENT ADDRESS STATUS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE		SHEET 70	



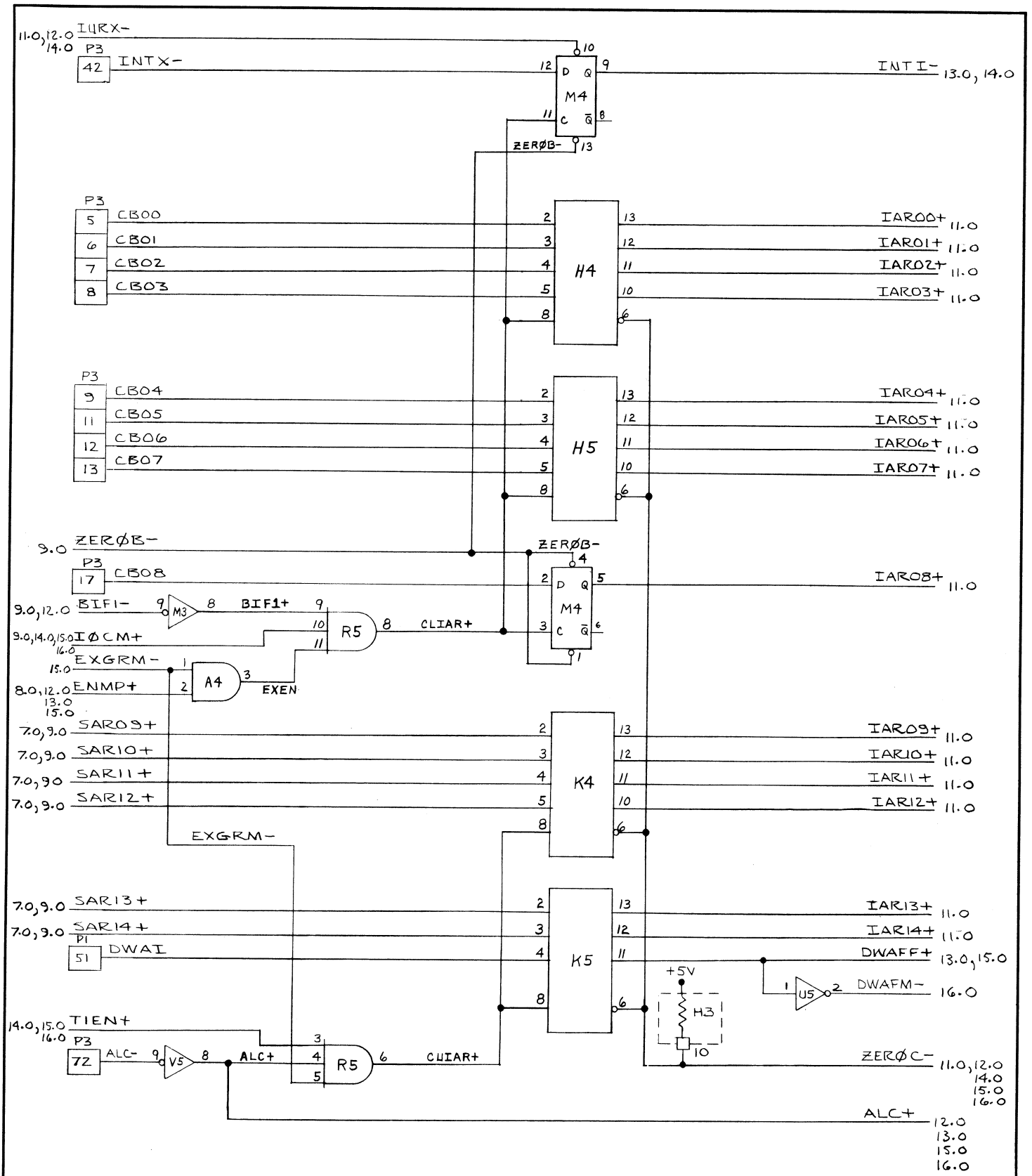
DEVICE ADDRESS DECODE AND FUNCTION CONTROL

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 8.0



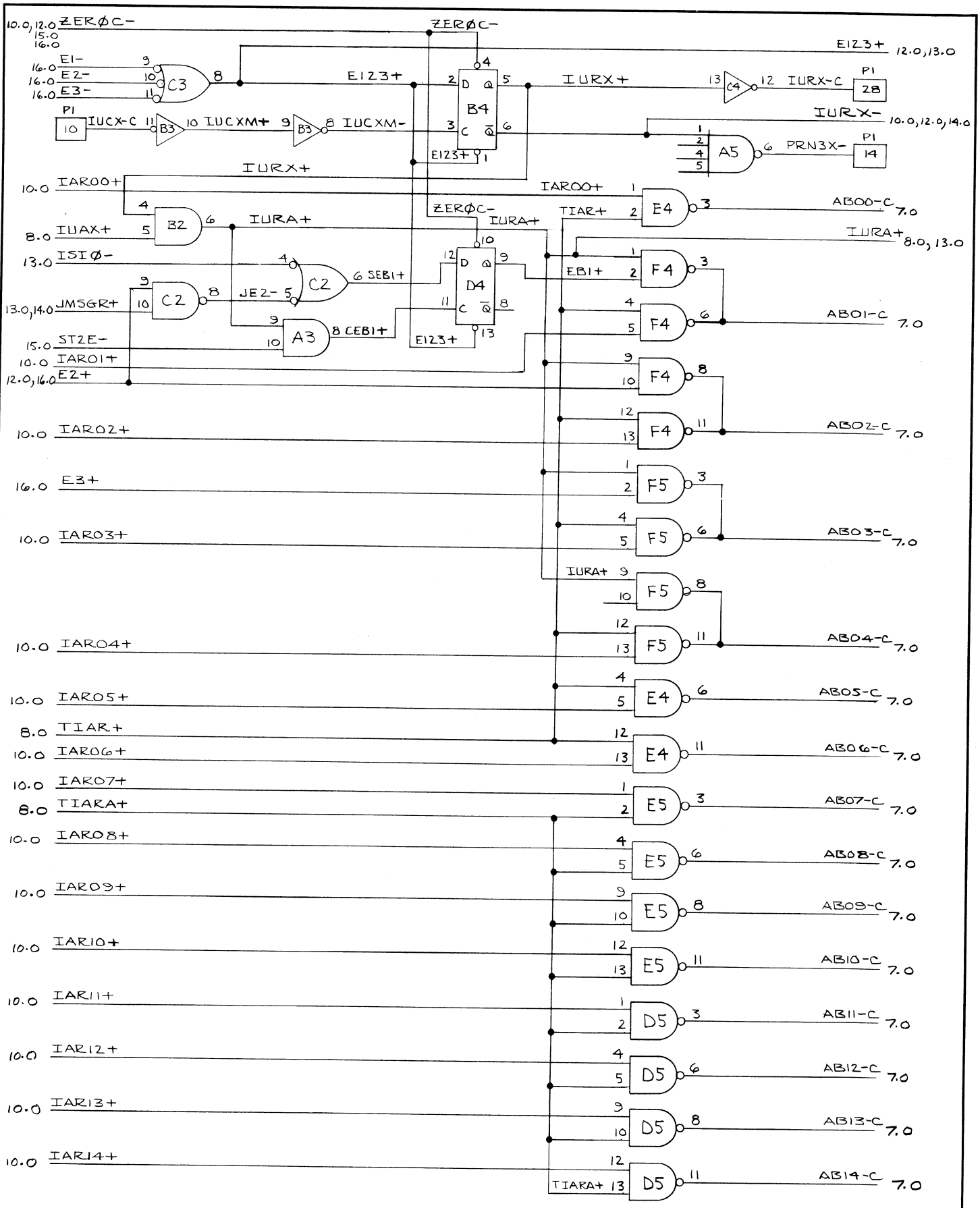
SEGMENT ADDRESS REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE		SHEET 9.0	



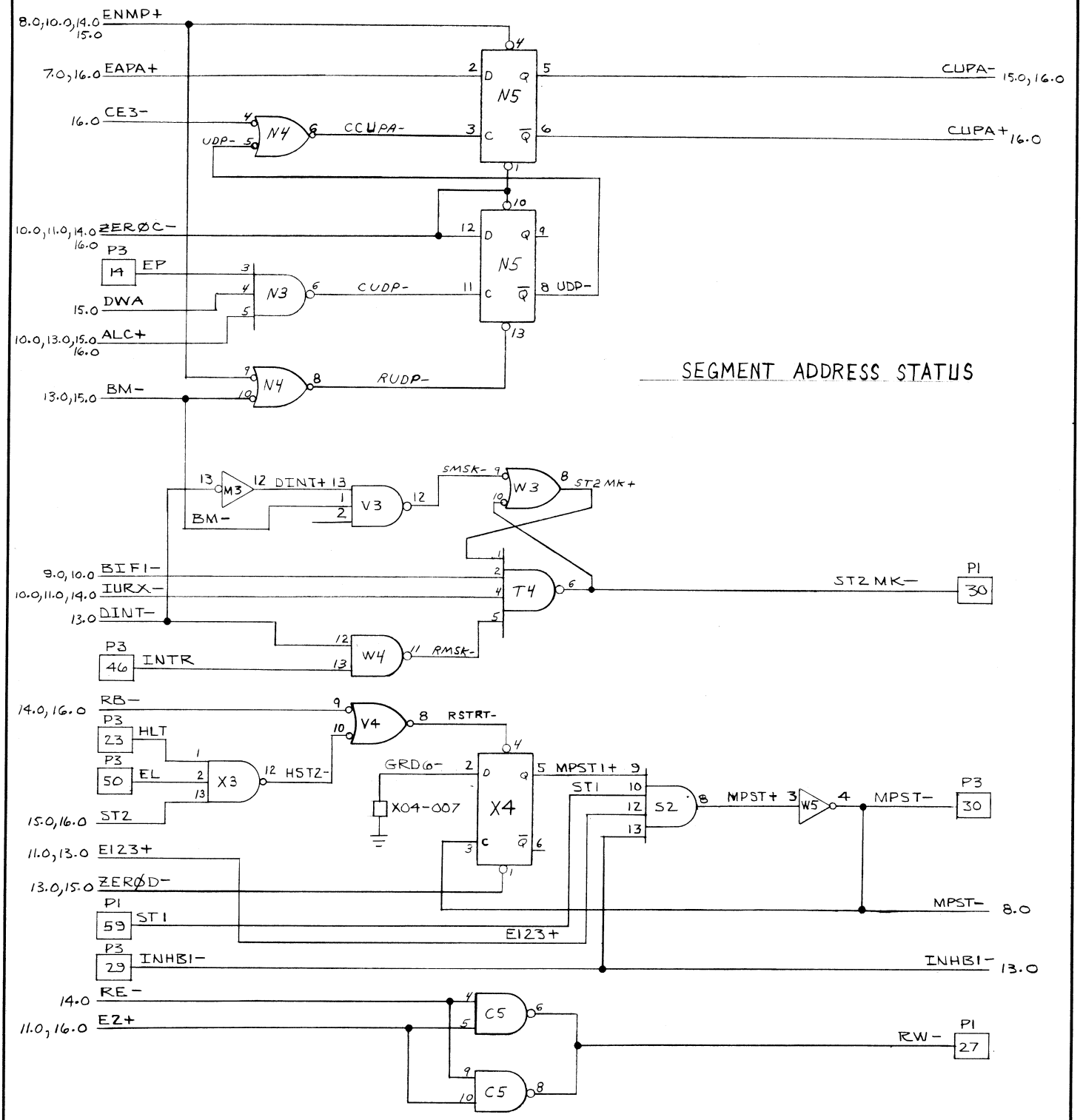
INSTRUCTION ADDRESS REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 10.0



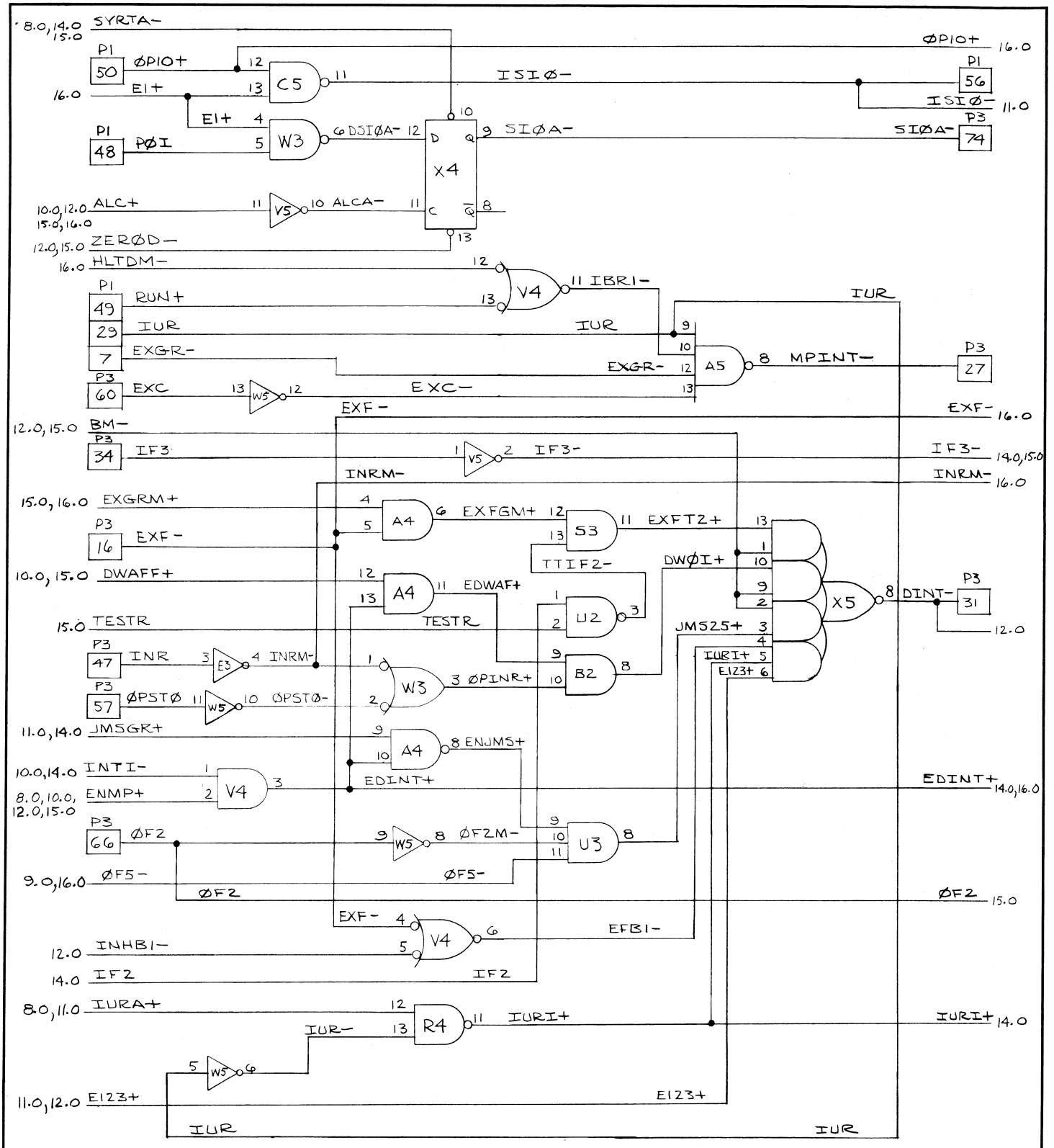
INTERRUPT REQUEST & A-BUS DRIVE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100257	C
SCALE		SHEET 11.0	



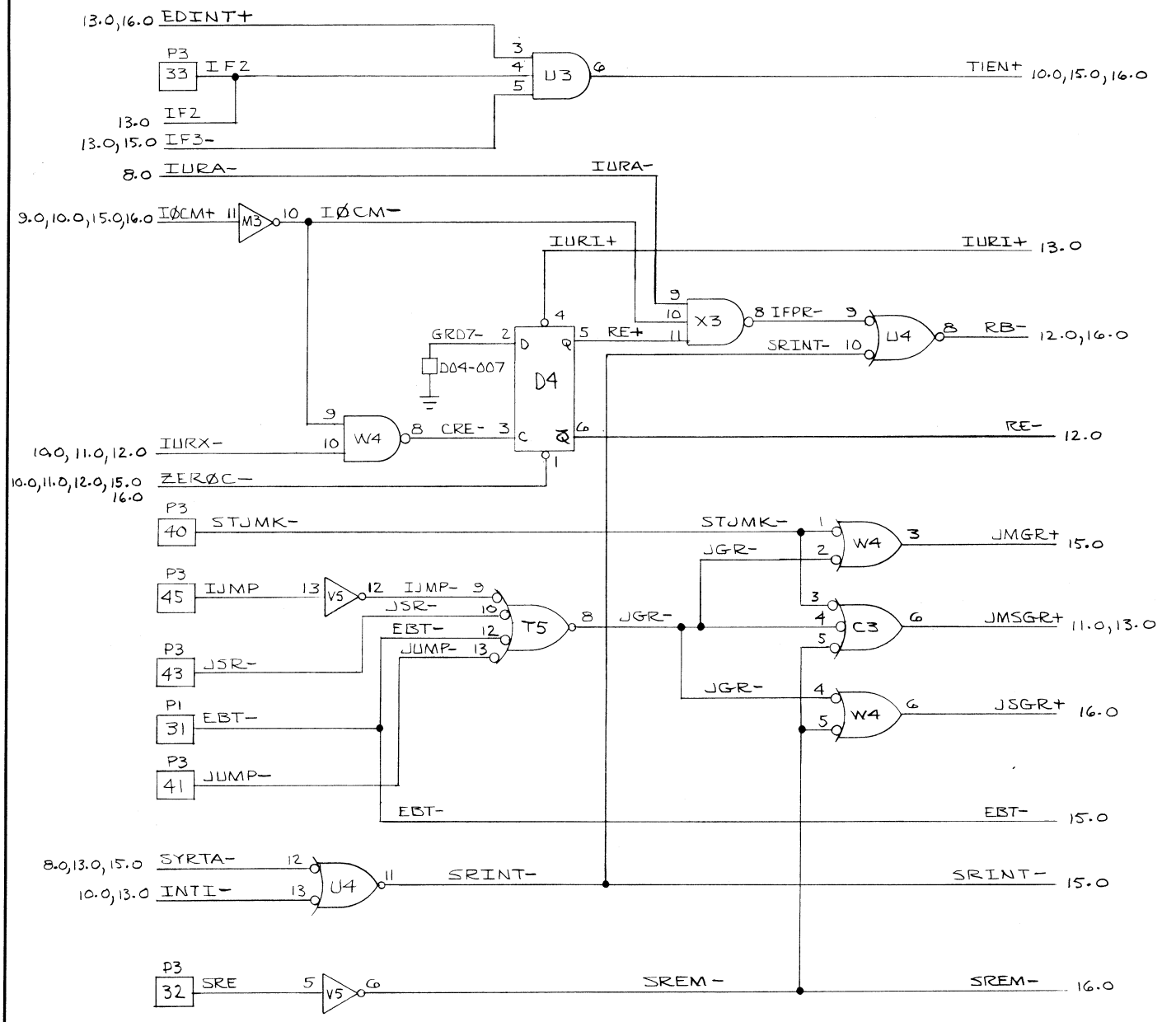
CPU CONTROL

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 12.0



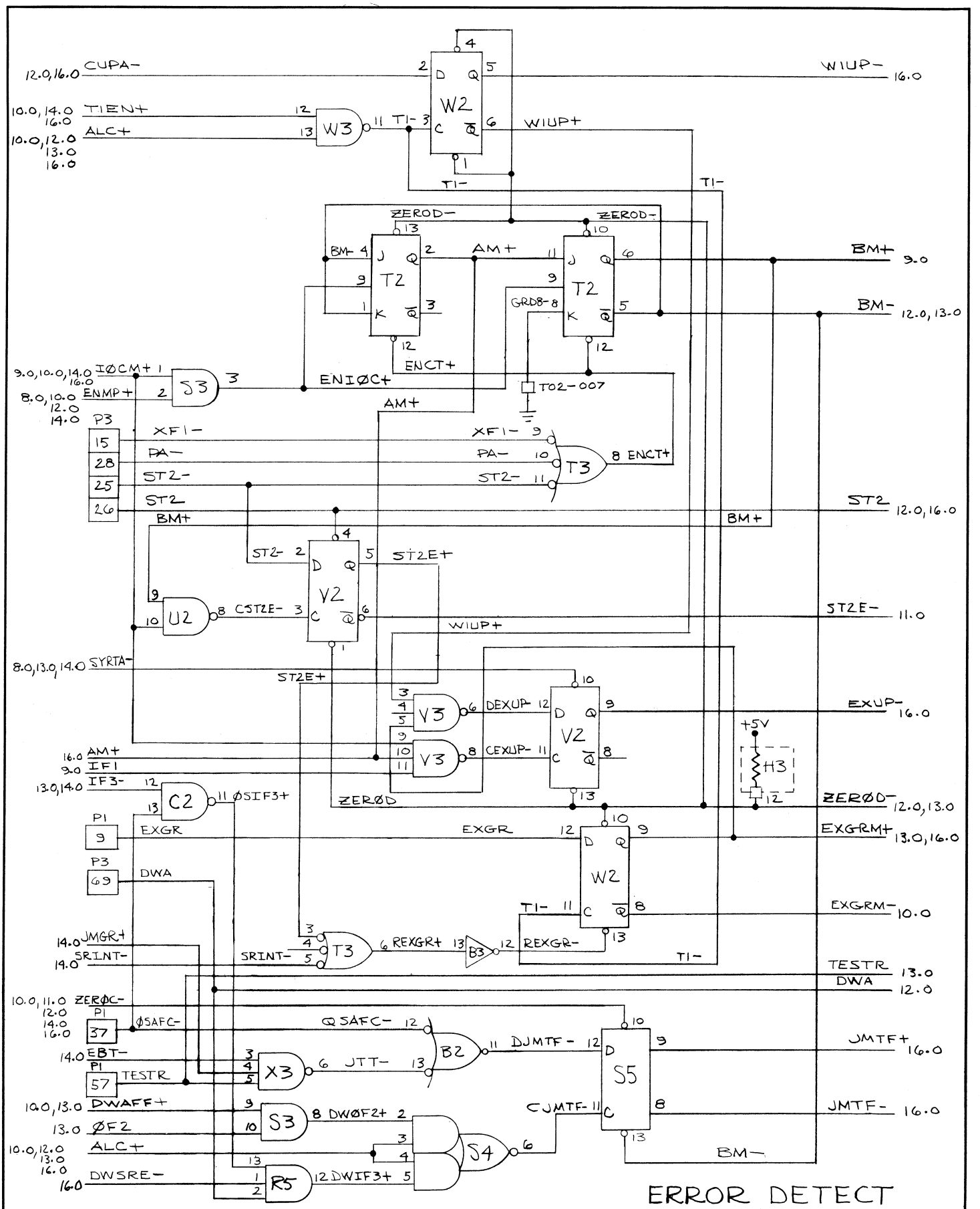
CPU CONTROL

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 13.0



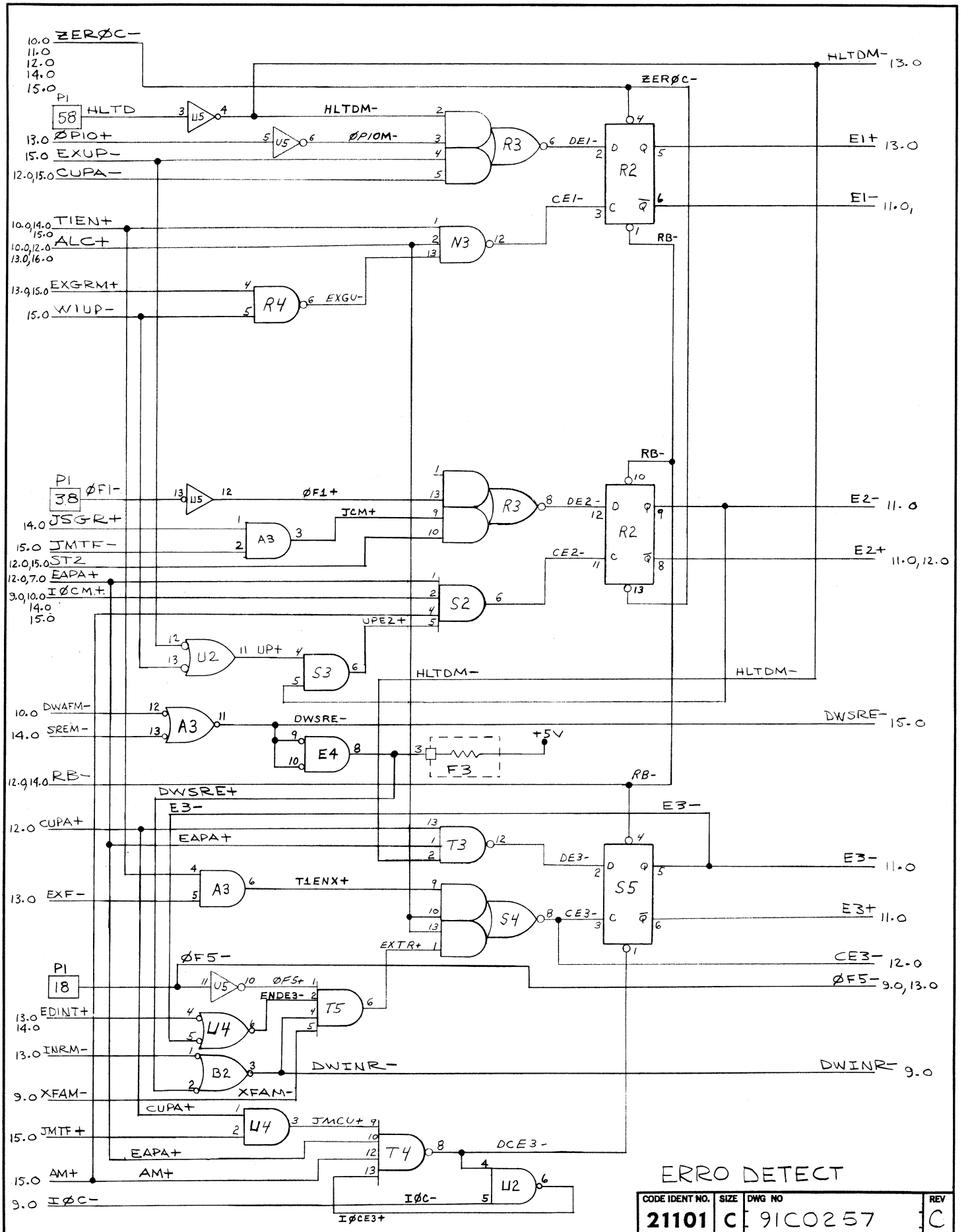
ERROR DETECT

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 14.0



ERROR DETECT

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE		SHEET 15.0	



ERRO DETECT

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0257	C
SCALE			SHEET 16.0

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DWG. NO. 44P0480

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO 000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
REF	-	98A0566 B	PPS		
REF	-	44D0480 B	ASSEMBLY		
REF	-	91C0257 C	LOGIC DIAGRAM		
REF	-	95W0719 C	WIRE LIST		
1	1	40D0439-000	P.W. BOARD		
1	2	49A0010-000	I.C. SN6006N		
2	3	49A0025-001	RESISTOR NETWORK		
4	4	49A0040-000	I.C. SN7404N		
5	5	49A0081-001	I.C. SN7403N		
14	6	49A0082-001	I.C. SN74H74N		
4	7	49A0090-001	I.C. SN7495N		
3	8	49A0093-001	I.C. SN74H50N		
3	9	49A0094-001	I.C. SN74H21N		
1	10	49A0097-000	I.C. SN74150N		
7	11	49A0104-000	I.C. MC3001P		
1	12	49A0106-000	I.C. SN74H53N		

NEXT ASSY 01P0947 | MODEL NO 620/f-05 | APPD

REV	X1	X2	X3	A	B	C	-	D
EN NO				5181	5182	5269	5476	5545
DATE			1/19/71	1/19/71	4/26/71	4/26/71	5/26/71	7-1-71
DR								
CHK								

TITLE: PARTS LIST
MEMORY PROTECT
OPTION

DWG NO 44P0480 | REV D

SHEET 1 OF 2

96A0017-000B

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DWG. NO. 44P0480

PARTS LIST

CODE IDENT: 21101

QUANTITY REQ'D PER DASH NO						000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
						4	13	49A0108-000	I.C. SN7417ON		
						2	14	49A0022-000	I.C. SN74H11N		
						4	15	49A0023-000	I.C. SN74H04N		
						5	16	49A0039-000	I.C. SN74H00N		
						1	17	49A0042-000	I.C. SN74H01N		
						5	18	49A0554-001	I.C. SN74H10N		
						1	19	49A0056-000	I.C. SN74H20N		
						1	20	49A0575-000	I.C. SN7405J		
						27	21	71A0009-003	CAPACITOR, 0.1uf 100V	C1,3,6,8,10,12-33	
						6	22	71A0200-225	CAPACITOR, 2.2uf 20V	C2,4,5,7,9,11	
						64	23	58A0060-000	SOCKET, 14 PIN		
						4	24	58A0060-001	SOCKET, 16 PIN		
						1	25	58A0060-002	SOCKET, 24 PIN		
						174	26	58A0062-002	WIRE WRAP POST		
						1	27	16S1057-068	CARD HANDLE		
						1	28	16S1057-055	CARD HANDLE		
						0	29	53A0333-040	WIRE, YELLOW	30 AWG	
						1	30	49A0099-000	I.C. SN74H108N		

NOTES:

DWG NO 44P0480

REV D

SHEET 2 OF 2

96A0017-001B

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